Electron Microscopy Characterization of GaN-on-GaN Vertical Power Devices

by

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ABSTRACT

Wide bandgap semiconductors are of much current interest due to their superior electrical properties. This dissertation describes electron microscopy characterization of GaN-on-GaN structures for high-power vertical device applications.

Unintentionally-doped (UID) GaN layers grown homoepitaxially via metal-organic chemical vapor deposition on freestanding GaN substrates, were subjected to dry etching, and layers of UID-GaN/*p*-GaN were over-grown. The as-grown and regrown heterostructures were examined in cross-section using transmission electron microscopy (TEM). Two different etching treatments, fast-etch-only and multiple etches with decreasing power, were employed. The fast-etch-only devices showed GaN-on-GaN interface at etched location, and low device breakdown voltages were measured (~ 45-95V). In comparison, no interfaces were visible after multiple etching steps, and the corresponding breakdown voltages were much higher (~1200-1270V). These results emphasized importance of optimizing surface etching techniques for avoiding degraded device performance.

The morphology of GaN-on-GaN devices after reverse-bias electrical stressing to breakdown was investigated. All failed devices had irreversible structural damage, showing large surface craters (~15-35 microns deep) with lengthy surface cracks. Cross-sectional TEM of failed devices showed high densities of threading dislocations (TDs) around the cracks and near crater surfaces. Progressive ion-milling across damaged devices revealed high densities of TDs and the presence of voids beneath cracks: these features were not observed in unstressed devices. The morphology of GaN substrates grown by hydride vapor-phase epitaxy (HVPE) and by ammonothermal methods were

correlated with reverse-bias results. HVPE substrates showed arrays of surface features when observed by X-ray topography (XRT). All fabricated devices that overlapped with these features had typical reverse-bias voltages less than 100V at a leakage current limit of 10^{-6} A. In contrast, devices not overlapping with such features reached voltages greater than 300V. After etching, HVPE substrate surfaces showed defect clusters and macro-pits, whereas XRT images of ammonothermal substrate revealed no visible features. However, some devices fabricated on ammonothermal substrate failed at low voltages. Devices on HVPE and ammonothermal substrates with low breakdown voltages showed crater-like surface damage and revealed TDs (~25μm deep) and voids; such features were not observed in devices reaching higher voltages. These results should assist in developing protocols to fabricate reliable high-voltage devices.

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CHAPTER 1

INTRODUCTION

1.1 Power Electronics

The advancement of power electronics is critical for efficient production and future sustainable supply of electrical energy. The Department of Energy (DoE) has reported that approximately 40% of all energy consumed in United States is first converted into electricity [1]. This amount increases to approximately 60% when considering electric vehicles and electricity-based public transportation [2]. Electricity as the primary consumption of energy will continue to expand as the fastest growing form of end-use energy. Power electronics is currently handling almost 40% of all electricity being consumed in this country and this amount is expected to increase to 80% by 2030 [3].

Power electronics can be considered as the technology that interfaces between electrical sources and electrical load. It also provides a mechanism that transfers power from the source to the load by controlling the respective currents and voltages [4], as depicted in Figure 1. The electrical source and the electrical load often differ in frequency, voltage amplitude, and the number of phases [5]. Thus, power electronics must provide utilities with the ability to deliver power more effectively to their customers while providing increased reliability for bulk power generation and distribution systems.

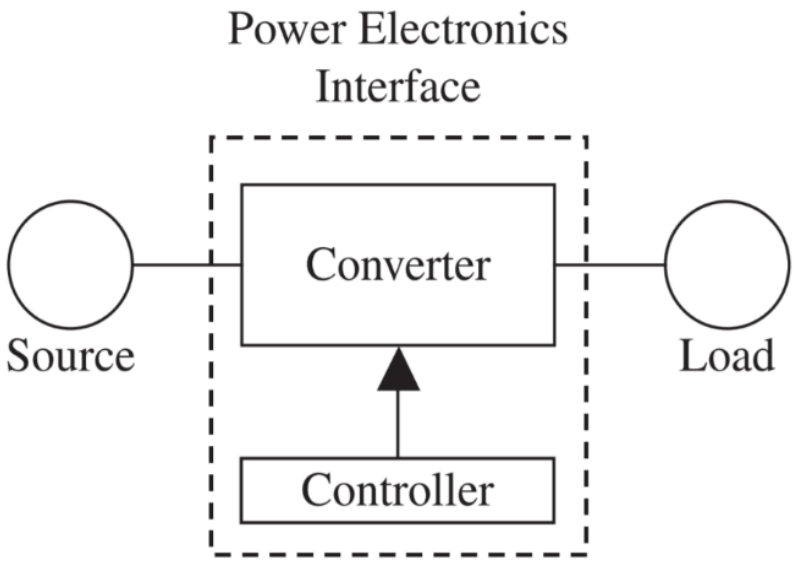

Figure 1.1. Schematic illustrating power electronics interface between source and load [4].

1.2 Power Devices Based on Gallium Nitride

The performance of commercial silicon-based power electronic devices, such as thyristors, metal-oxide semiconductor field-effect transistors (MOSFETs), and insulated-gate bipolar transistors (IGBTs), is rapidly nearing material property limits [6]. Wide-bandgap semiconductors are of much current interest due to the many advantages offered by devices made of these materials compared to Si-based devices. Table 1.1 compares the electronic properties of several wide-bandgap materials with those of Si. Figure 1.2 is a schematic comparison between Si, silicon carbide (SiC), and gallium nitride (GaN) for important device characteristics. The wide-bandgap materials have clear advantages over silicon for power device applications.

Material	Band Gap	Electric Breakdown Field	Electron Mobility	Electron Saturation Velocity	Thermal Conductivity
	E_g (eV)	E_c (MV/cm)	μ_n ($cm^{2/}$V.s)	V (10^7 cm/s)	λ (W/cm. K)
Si	1.12	0.3	1500	1	1.5
GaAs	1.43	0.4	8500	2	0.46
GaN	3.44	3.9	1250	2.2	2.3
4H-SiC	3.26	2	1000	2	4.9
6H-SiC	2.86	2.4	400	2	4.9
Diamond	5.45	10	3800	2.7	22

Table 1.1. Comparison of electrical properties [9-17].

The combination of wide bandgap and chemical stability at elevated temperatures makes GaN-based devices suitable for applications in high temperature and harsh environments. Moreover, GaN has large electron mobility and saturation velocity compared to Si, which allows high frequency operations [7]. The breakdown electric field of GaN is much higher compared with Si, allowing for the design of power devices with higher operating voltages and reduced leakage currents [8]. Furthermore, GaN power devices have larger bandgap and low intrinsic carrier concentration. The relatively low bandgap of Si (1.12 eV) means that Si-based devices (MOSFETs, thyristors, etc.) require large critical thickness for high voltage applications, which leads to high resistance and conduction losses in devices [19]. Moreover, the low Si bandgap means large intrinsic carrier concentrations which will increase leakage currents as the temperature increases [20]. Lower electrical breakdown field as well as bandgap mean thicker drift regions with

low doping levels in order to achieve high blocking voltages, which in turn translate to high conduction losses. GaN has a higher critical electrical field than Si which leads to thinner voltage-blocking layers and reduced on-resistance in devices such as MOSFETs relative to Si [21]. GaN also has higher electron mobility, high saturation velocity and high thermal conductivity. These advantages allow for the design of power devices for high voltage and high temperature operations [22]. Fast switching GaN power devices greatly increase efficiency and provide smaller device systems [23].

Although silicon carbide (SiC) diodes are commercially available with rapidly incremental market share for high efficiency devices, GaN-based power devices are of increased interest because their material-based figure of merit (FOM) parameters are considerably higher than those of SiC [2, 23-24]. The power figure of merit (PFOM) is directly influenced by the cubed electric breakdown field (E_c), and is a parameter used to compare wide bandgap materials most suitable for vertical power device applications. Figure 1.3 shows the specific on-resistance ($R_{sp,ON}$) versus device breakdown for GaN, SiC, and Si. GaN has a clear advantage over Si or SiC given that the electric breakdown field for GaN is roughly 1.6 times greater than that of SiC, and 10 times more than that of Si [25].

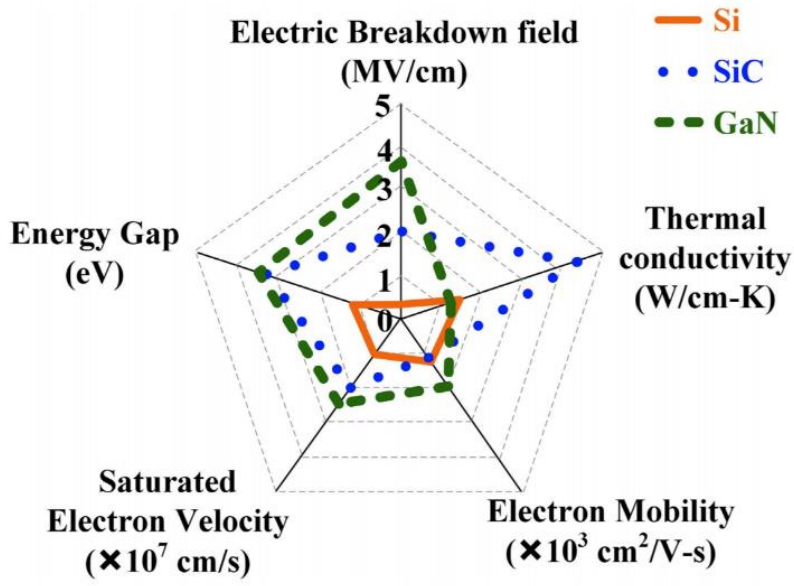

Figure 1.2. Comparison of electronic properties of wide bandgap materials (GaN and SiC) relative to those of Si [18].

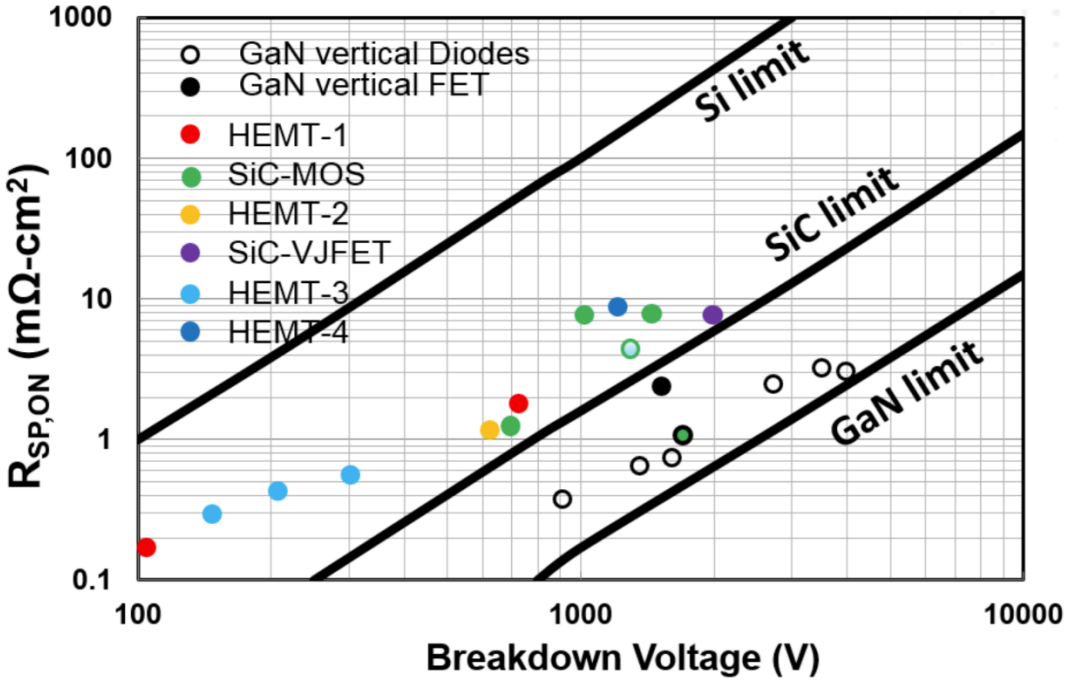

Figure 1.3. Specific on-resistance ($R_{sp,ON}$) vs. breakdown voltage (V) for different devices and material limits [25].

1.3 Properties of Gallium Nitride

1.3.1 Crystal Structure

The group III-nitrides are direct band-gap semiconductors with band-gap energies ranging from 0.7eV (InN), to 3.4eV (GaN) and 6.2eV (AlN). By forming ternary group III-nitride alloys such as indium gallium nitride ($In_xGa_{1-x}N$) and aluminum gallium nitride (AlGaN), as well as quaternary alloys, band-gap energies can be engineered to cover the entire wavelength range from deep-ultraviolet (UV) to near-infrared (IR) [26].

Table 1.2 compares some important physical properties of GaN with those of AlN and Si. The group III-nitrides have the thermodynamically-stable wurtzite structure as well as two unstable structures (zincblende and rock-salt). Each atom is tetrahedrally coordinated to four other atoms through sigma bonds originating from the sp^3 hybrid atomic orbitals. The stacking sequence of wurtzite is ..AaBbAaBb.. along the <0001> direction [27]. Figure 1.4 shows a schematic of the wurtzite GaN unit cell with two interpenetrating hexagonal-close-packed (hcp) sublattices [28]. The polar *c*-plane is marked in green whereas non-polar planes are marked in blue and red. Figure 1.4 (b) shows the atomic arrangements for *m*-plane projection as well as the size of the unit cell marked in red. The length and direction of lattice parameters *a* and *c* are also marked.

GaN-on-GaN heterostructure devices are most commonly grown on *c*-plane GaN substrates, which is a high symmetry/low index orientation. The reasons for electronic and optoelectronic industrial devices being grown with this orientation are the commercial availability of cost-effective substrates, as well as surface stability and good

surface morphology under different growth conditions [29]. The planes of anions alternate with planes of cations in the *c* direction for wurtzite GaN, which gives a non-centrosymmetric structure with spontaneous polarization. Since the *c*-plane is polar, GaN devices grown on this plane have electric fields that can affect device performance [30]. When devices without electrostatic fields are required, GaN can be grown on *m*-plane or *a*-plane since these surfaces are non-polar. It has been reported that devices without internal electrostatic fields can be grown epitaxially on non-polar planes [31].

Material	Symmetry	Lattice Parameters (nm)	Coefficient of thermal expansion 10^{-6} (K^{-1})	Bond length (nm)
GaN (Wurtzite)	Hexagonal	*a*= 0.319 *c*= 0.519	5.59 (along a) 3.17 (along c)	0.194
GaN (Zincblende)	Cubic	*a*= 0.452	-	-
AlN (Wurtzite)	Hexagonal	*a*= 0.311 *c*= 0.498	4.2 (along a) 5.3 (along c)	0.189
AlN (Zincblende)	Cubic	*a*= 0.438	-	-
Si	Cubic	*a*= 0.543	3.59	-

Table 1.2. Comparison between physical properties of GaN, AlN and Si [27, 32].

The GaN crystal structure has spontaneous polarization along the *c*-axis due to the large ionicity of the Ga-N bonds, which means that Ga-polar basal (0001) planes in the wurtzite structure are not equivalent to N-polar ($000\bar{1}$) planes [32]. Figure 1.5 illustrates the atomic arrangements in Ga-polar and N-polar GaN. This difference can be critical in some applications because of the dependence of many physical properties on crystal

polarity, including polarization, etching, and growth. Thus, while the *c*-direction is the most stable for growth, most studies have been conducted on Ga-polar (0001) GaN rather than N-polar ($000\bar{1}$) GaN [33].

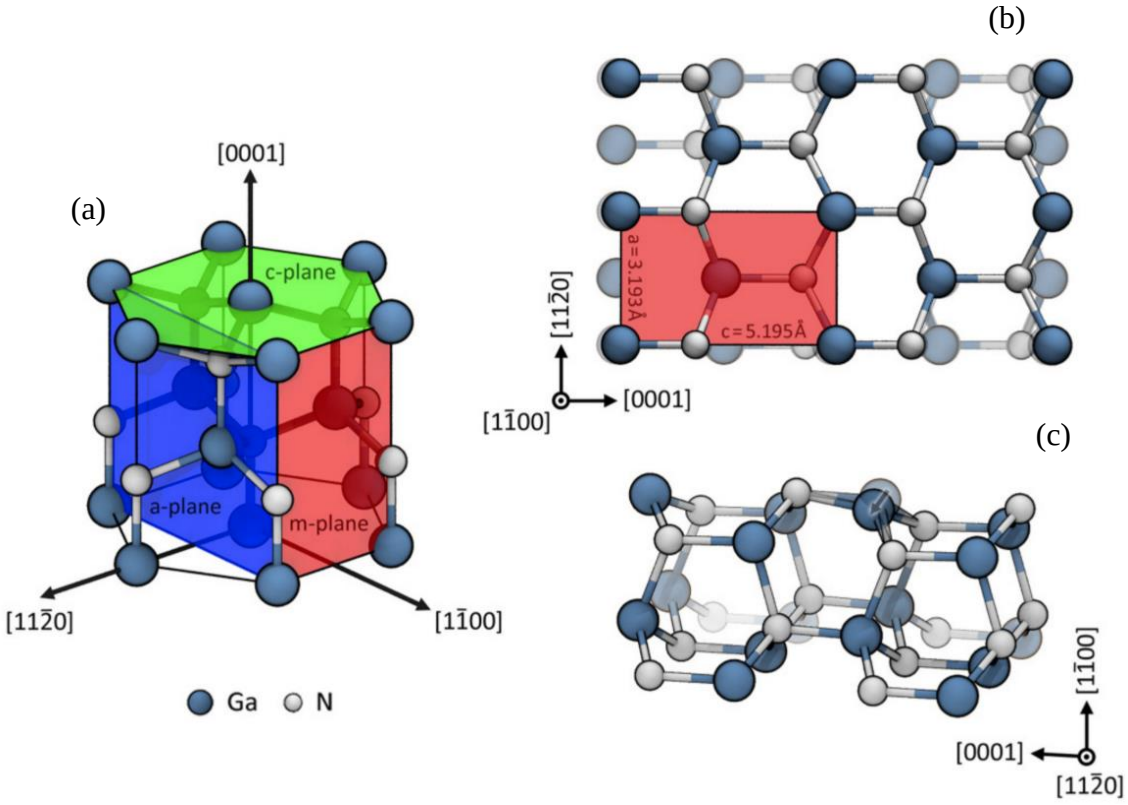

Figure 1.4. (a) Representation of wurtzite GaN unit cell with important crystal surface planes. Polar *c*-plane and non-polar *m*- and *a*-planes marked in green, red, and blue, respectively; (b) *m*-plane GaN atomic arrangement, definition of unit cell marked in red and atoms below top atomic double layers are shown in translucent; and (c) Atomic arrangement viewed with slightly tilted *m*-plane. [28]

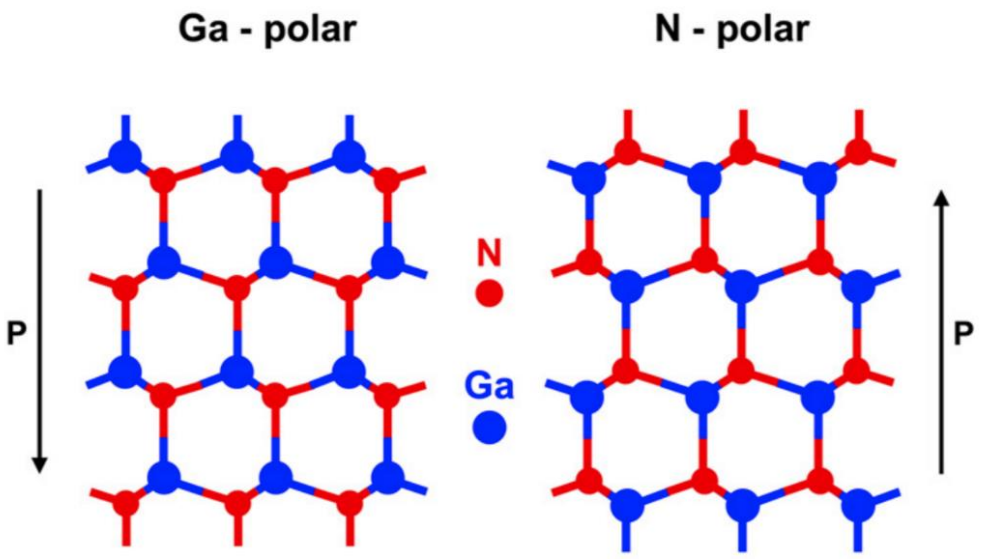

Figure 1.5. Schematic of atomic arrangements in Ga- and N-polar GaN. Direction of spontaneous polarization dipole (P) indicated by arrows [33].

1.3.2 Structural Characterization

The stacking of semiconductors devices with multiple layers, whether homoepitaxial or heteroepitaxial, introduces more complexity to the overall device structure. Since the rapid acceleration of "minimization of design" rule for semiconductor devices, electron microscopy characterization has become a crucial technique that allows investigation and control of device quality from the size/scale of an entire packaged device down to the atomic level. Whether it be impurities from growth, oxidation/damage during etching, diffusion from metal contacts during fabrication, or device failure during operation; it becomes critical to investigate the causes that lead degraded performance and device breakdown. Given the scale and size of semiconductor devices, characterization techniques such as transmission electron microscopy (TEM), scanning transmission electron microscopy (STEM), and focused ion beam (FIB) play critical roles

in identifying and resolving materials and fabrication issues, and thereby advancing semiconductor device research.

1.3.3 Structural Defects

Defects in materials are important because they may negatively impact key electrical properties. Given that material layers are mostly grown at finite temperatures away from equilibrium, defects commonly appear in the grown layers [34].

Defects can be divided into four types [35]:

a. Zero-dimensional point defects, such as vacancies and atomic site substitution;
b. One-dimensional line defects, such as dislocations;
c. Two-dimensional planar defects, such as stacking faults and inversion domain boundaries;
d. Three-dimensional volume defects, such as voids, cracks and nanopipes.

1.3.3.1 Point Defects

Figure 1.6 shows a schematic of point defects. Point defects can be classified as vacancies, substitutional atoms, or interstitial atoms. Interstitial atoms are impurities that occupy space between atoms arranged in a regular crystal lattice. Most commonly, the interstitial site tends to have lower free energy than the neighboring sites. Interstitial atoms can be foreign impurities or atoms from the same crystal. Similarly, substitutional atoms can be considered as atoms that replace or substitute the original atoms of the crystal lattice. Substitutional atoms occupy the lattice site of the crystal which is

chemically most suitable or similar to the crystal atoms. In semiconductors, this concept is used to classify foreign atoms as impurities (unintentionally doped) or dopants (intentionally introduced). For example, unintentionally doped atoms in GaN are most often oxygen (O) and carbon (C). Oxygen occupies the chemically similar N site whereas C is reported to be amphoteric in nature [36, 37]. If the substitutional atom originates from the host crystal, for example if the first atom of a binary semiconductor occupies the site of the second atom, then this is referred to as an anti-site defect. When a site in crystal lattice is unoccupied, then it is referred to as a vacancy. In binary semiconductors such as GaN, the vacancies can be either cation (Ga) or anion (N).

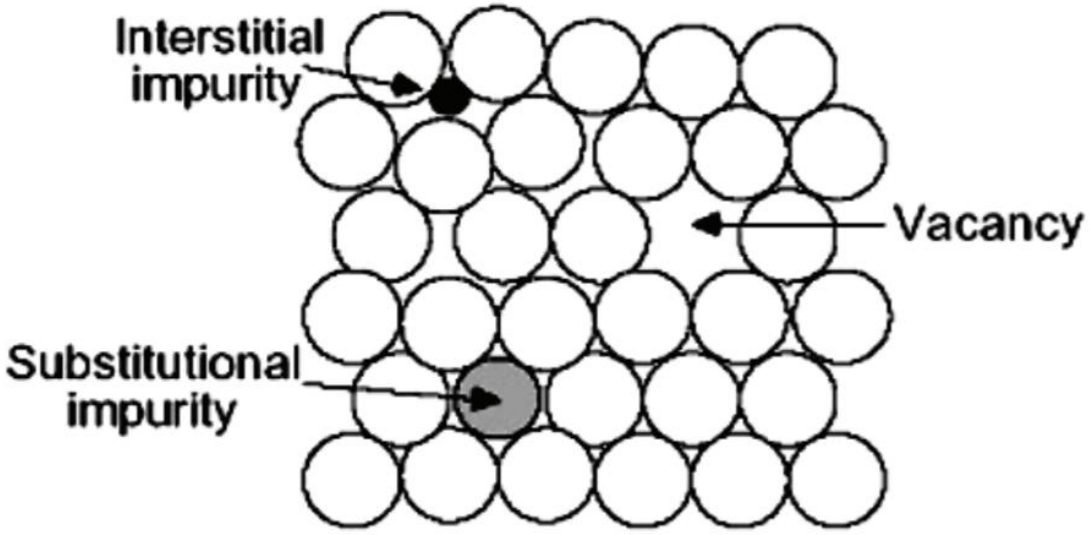

Figure 1.6. Schematic of possible point defects in a crystal lattice [34].

1.3.3.2 Line Defects

Any irregularity in the regular arrangement of atoms along a line in a crystal can be referred to as a dislocation. This irregularity can occur due to misalignment of atoms or vacancies. The presence of dislocations may cause large lattice distortions over very

short distances, often referred to as the dislocation core, and small distortions at large distances, which are often referred to as lattice deformation. Dislocations can be characterized by their Burgers vector (***b***) which defines the magnitude and direction of lattice discontinuity due to the dislocation. Dislocations are defined as edge dislocations, screw dislocations, and mixed dislocations [34].

Figure 1.7 shows schematics of edge and screw dislocations. A screw dislocation occurs because of displacement of planes with respect to each other due to shear stress. The Burgers vector of a screw dislocation is parallel to the dislocation line. An edge dislocation can be described as the presence of an extra plane of atoms in a crystal, where the Burgers vector of the dislocation is perpendicular to the dislocation line. The extra plane of atoms would be under compressive stress while subjecting neighboring planes to tensile stress. Dislocations which have both edge and screw dislocation components are termed mixed dislocations. Edge, screw, and mixed dislocations are commonly observed in GaN-based epitaxial layers, mostly depending on the specific growth method [39].

1.3.3.3 Planar Defects

Planar defects are two-dimensional crystallographic defects that are related to lattice planes such as grain boundaries, twin boundaries and stacking faults. Stacking faults are atomic displacements which interrupt the normal stacking of the crystal lattice [39]. Stacking faults in GaN mostly occur on the (0001) basal-plane and are referred to as basal-plane stacking faults. These can be considered as layers with local cubic stacking. Stacking faults which lie in $(1\bar{1}00)$ and $(11\bar{2}0)$ prism planes are referred to as prismatic faults [40].

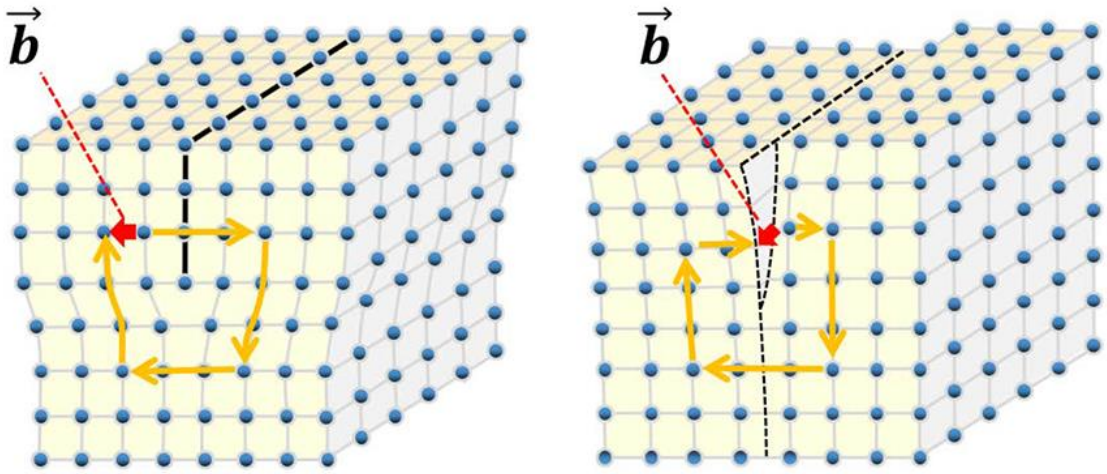

Figure 1.7. Schematic of: (a) Edge dislocation, (b) Screw dislocation [38].

1.3.3.4 Volume Defects

Volume defects, such as precipitates, voids and nanopipes are three-dimensional defects. Nanopipes are hollow tunnel-like defects and have open-core screw dislocation character [34]. These defects mostly occur along the growth direction [0001] and those that terminate at the free surface are often referred to as pin-holes [40]. The openings in the material can be few nanometers in width up to as large as few microns [41]. Some studies report that oxygen impurities are linked with the formation of these defects [42].

1.4 Lateral Devices vs Vertical Devices

High-electron mobility transistors (HEMTs) are comprised of AlGaN/GaN heterostructures and usually have a lateral device geometry. A 2-dimensional electron gas (2DEG) is often formed at AlGaN/GaN interfaces in these power devices. Due to the high-density 2DEG, which is a low-resistance drift region, HEMT devices have low on-resistance with high breakdown voltage [45].

Vertical device structures have received much recent attention with the development and commercial availability of free-standing GaN substrates. Vertical structures have several advantages over lateral structures, such as improved current density, smaller chip size and high breakdown voltage [44, 45]. Figure 1.8 compares the power range for lateral and vertical devices [48]. A recent study reported breakdown voltage of 3.7 kV with a vertical *p-n* diode device structure, which represents a significant improvement over lateral devices [46]. This leads to significant reduction in size of vertical devices for performance comparable with lateral devices. For example, the size of a GaN-on-Si HEMT device with breakdown voltage of ~650V is approximately 6 times larger than a vertical GaN device with breakdown voltage of ~1200V for similar current-carrying capability [47].

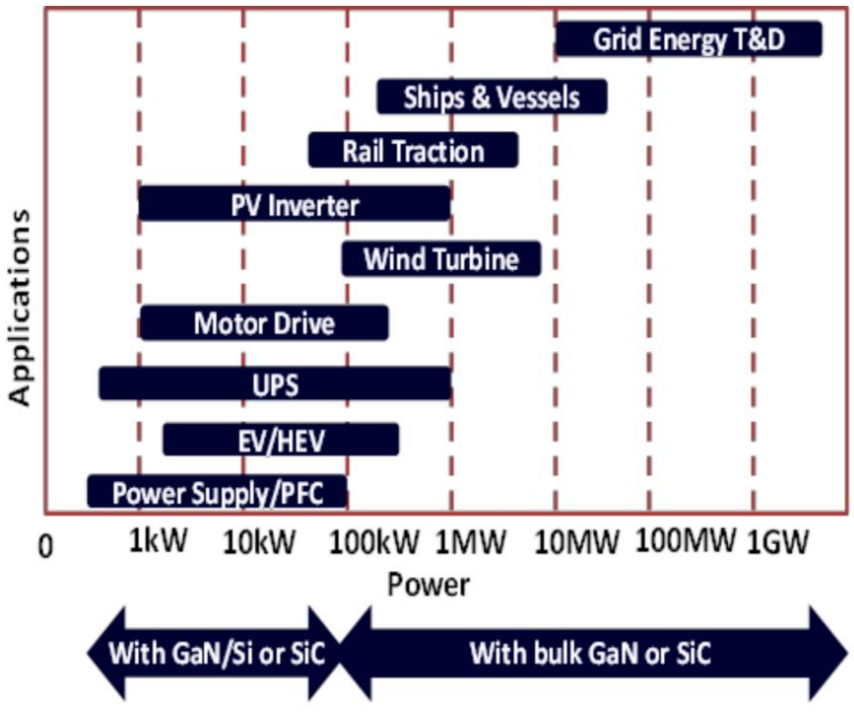

Figure 1.8. Comparison between Lateral (GaN/Si or SiC) and Vertical (GaN/GaN) devices in terms of power capacity [48].

1.5 Outline of Dissertation

The research of this dissertation has involved the characterization of vertical GaN-on-GaN power devices primarily using transmission electron microscopy (TEM). Scanning electron microscopy (SEM) and focused ion beam (FIB) techniques have also been heavily used.

A brief outline of this dissertation is as follows:

Chapter 1 has provided an introduction to the important physical and electrical properties of GaN as well as motivation for this research.

Chapter 2 provides a brief description of growth and characterization techniques.

Chapter 3 describes an investigation of GaN layers that were etched using high radio frequency (RF) power and multiple steps of decreasing RF power. Transmission electron microscopy was used to characterize the etch damage at interfaces after *p*-GaN regrowth.

Chapter 4 describes the structural changes observed in GaN-on-GaN devices subjected to reverse-bias stress testing. The device morphology after breakdown was investigated using a combination of focused-ion-beam cross-sectional milling, scanning electron microscopy and transmission electron microscopy.

Chapter 5 describes an investigation of the effect of substrate morphology on the reverse-bias electrical response of GaN-on-GaN vertical *p*-*n* devices. The fabricated devices were characterized by X-ray topography (XRT), scanning electron microscopy (SEM) and transmission electron microscopy (TEM), and the results have been correlated with electrical performance.

Chapter 6 describes an investigation of atomic-layer-etched (ALE) and regrown GaN-on-GaN vertical devices.

Chapter 7 describes preliminary investigations and possible future work required to understand the cause(s) of device breakdown behavior from a materials perspective and ensure reliable performance in future generation of devices.

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CHAPTER 2

EXPERIMENTAL METHODS

This chapter provides a brief description of the techniques commonly used to grow epitaxial GaN films, and an overview of the experimental techniques that were used in this research for characterization of defect morphology.

2.1 Growth Methods

2.1.1 Metal Organic Chemical Vapor Phase Deposition (MOCVD)

Figure 2.1 shows a schematic of an MOCVD system. MOCVD is a form of vapor deposition in which chemical sources are transported to a substrate surface where they react to produce by-products that are incorporated into the growing film. The technique is commonly used to grow epilayers with thicknesses of tens of microns due to its high growth rate (2-5 microns/hour), precise control on growth thickness, doping control and instrument maintenence [1]. Since many materials of interest have low vapor pressure, making it difficult to transport them in the gaseous state, metals are chemically attached to an organic compound, which results in very high vapor pressure and assists with transport within the MOCVD chamber. The substrate temperature plays an important role in the growth process since it directly affects nucleation and diffusion on the wafer surface. The weak organic-metal bonds are broken at the high temperature of the substrate, resulting in metal deposition on the wafer surface [2]. The gaseous by-products are transferred out of the chamber through carrier gas flow. MOCVD thus enables the

growth of GaN layers on solid substrates/wafers using organo-metallic compounds as represented by equation (1).

For GaN growth, the source gases are usually trimethylgallium (TMG) and ammonia (NH_3) and the carrier gas is H_2 or N_2. Bis(cyclopentadienyl) Cp_2Mg and silane (SiH_4) are used for doping. The growth temperatures are typically in the range ~1000-1100°C.

$$(CH_3)_3Ga\ (g) + NH_3\ (g) \rightarrow GaN\ (s) + 3(CH_3)\ H \uparrow \qquad (1)$$

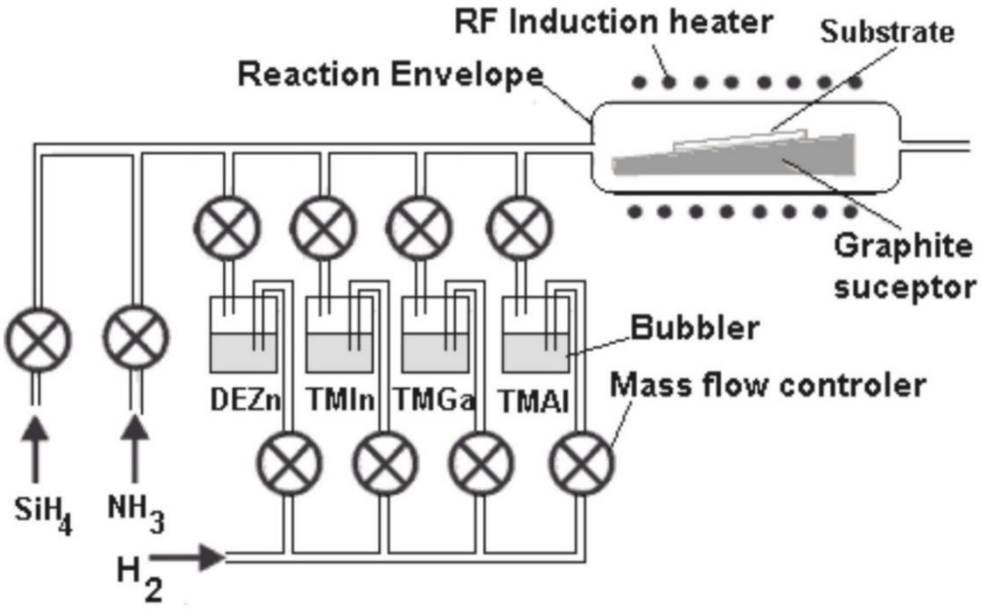

Figure 2.1. Schematic of metal organic chemical vapor deposition system [2].

2.1.2 Molecular Beam Epitaxy (MBE)

MBE is a high-precision and well-established deposition technique for the epitaxial growth of semiconductor films [4]. Figure 2.2 shows a schematic of a typical MBE system. A shortcoming of MBE is the relatively low growth rate (1-1.5 μm/hour)

compared to MOCVD or hydride vapor phase epitaxy (HVPE), but the technique allows for highly controlled growth of ultra-thin layers. Growth in an MBE chamber is conducted under ultra-high vacuum conditions, and the base pressure is typically $<10^{-10}$ Torr when the system is not in use [4]. MBE growth is temperature-sensitive due to the vapor pressure of III-V elements which have high heats of vaporization. Most of the source elements are held in effusion cells (pyrolytic crucibles) and heated with precise temperature control [4]. The substrate is rotated throughout the growth process to ensure uniform films over the entire surface area. The growth of semiconductors using MBE is a result of interplay between impinging atoms or molecular form of elements onto the substrate surface. The stoichiometry and substrate temperature influence the surface geometry and surface reconstruction or atomic arrangements. Reflection-high-energy electron diffraction (RHEED) in the chamber is used to monitor the quality of growth during the MBE growth [5-6]. The impinging atoms diffuse across the surface to bond to surface sites, and atomic rearrangements then occur, forming the growing crystal. These surface processes are generally rapid compared to the impingement of new atoms, which leads to well-ordered and uniform layers. Plasma-assisted MBE is the method widely used for the growth of group III-nitrides, and the temperature range for GaN growth is typically 700°C-800°C.

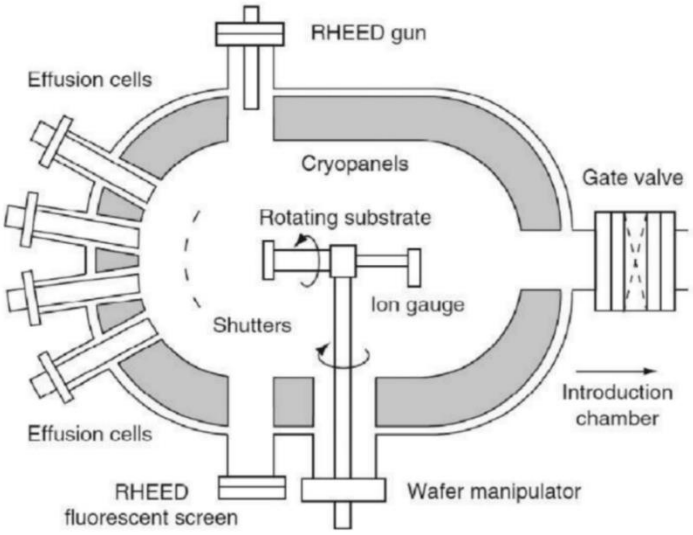

Figure 2.2. Schematic of molecular beam epitaxy system [4].

2.1.3 Hydride Vapor Phase Epitaxy (HVPE)

The technique of HVPE is generally employed to grow very thick GaN layers (>150 µm) and is widely used nowadays to fabricate freestanding GaN substrates. Figure 2.3 shows a schematic of an HVPE chamber. The growth rates can be as high as 100 µm/hour. The reaction chamber is kept at atmospheric pressure and the substrates are placed on a rotating wafer holder [2, 6]. The reaction chamber contains two zones, a source zone, and a growth zone. The source-zone temperature is kept at ~800-900°C and HCl is passed through a Ga metallic crucible into the source zone [3]. The HCl reacts with the metal and forms GaCl in the source zone. This by-product is injected into the growth zone through a shower head, where it reacts with NH_3 at the substrate surface to form GaN at ~1000-1100°C [3, 7-8].

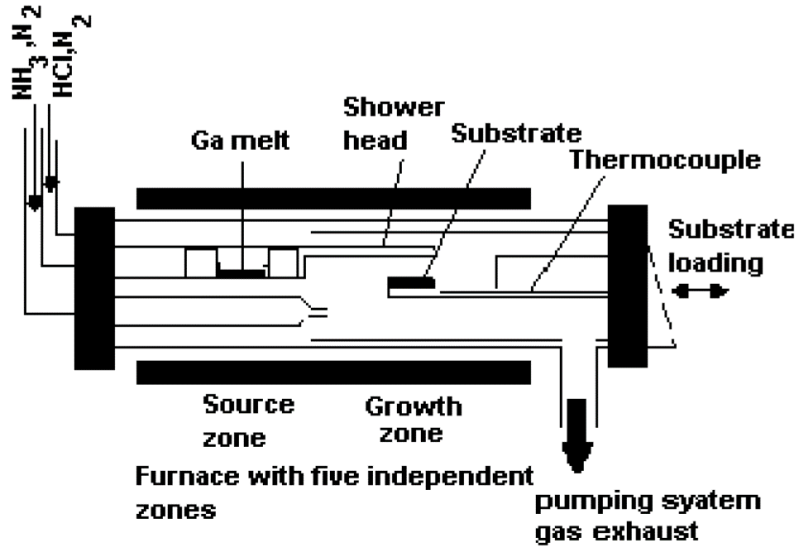

Figure 2.3. Horizontal hydride vapor phase epitaxy reactor [2].

2.2 Characterization Techniques

The characterization techniques used in this dissertation research are briefly described in the following.

2.2.1 Scanning Electron Microscopy (SEM)

In SEM, a focused electron beam is scanned across the sample in a raster-like pattern. Electrons scattered from the surface and near-surface regions are then used to create an image of the scanned area. The energy of the electron beam in an SEM is much less than in a transmission electron microscope, with typical energies ranging from 2keV to 30keV. The electrons that scan across the sample surface produce signals that can be used to create different types of images of the scanned area, for example, secondary electron images and back-scattered electron images [9]. Figure 2.4 illustrates the signals

that are generated when an energized electron beam hits the sample surface [10]. The resolution that can be achieved with an SEM varies in the range from 0.5 to 5 nm [11].

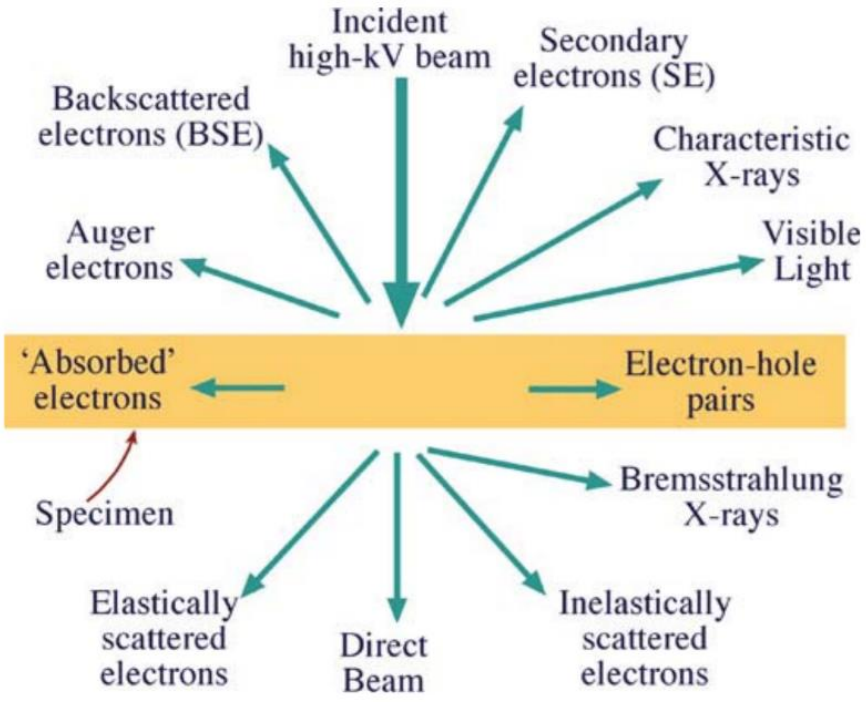

Figure 2.4 Schematic showing the generation of many different signals when the incident electron beam of an SEM interacts with a sample surface [10].

2.2.2 Focused Ion Beam (FIB)

The FIB is widely used for site-specific analysis, imaging, chemical analysis, milling, deposition, micromachining, lithography, and TEM sample preparation [9]. The increasing complexity of semiconductor device structures and complex materials systems necessitate the use of FIB milling for preparing thin TEM samples that are often lifted-out from deeply buried site-specific locations. Ionized metal ions, typically Ga^+ ions, are produced by a liquid metal ion source in the FIB column and focused onto the sample

surface for milling. A tungsten (W) needle tip is used to extract liquid Ga from a reservoir into a cone (radius ~ 5-10 nm), and a high extraction field (0.108 V/cm) is used for this purpose [12]. Emitted Ga^+ ions, due to field ionization and post-ionization, are accelerated down the FIB column. The Ga ions are generally focused using electrostatic lenses rather than magnetic lenses due to the much larger mass of ions compared to electrons. By varying the strength of the electrostatic lens in combination with different aperture sizes, probe current densities (pA to nA) and probe diameters (5nm to 0.5μm) can be systematically varied. When the accelerated metal ions hit the specimen surface, surface atoms are removed and the sample is milled away due to sputtering [12, 13]. This process also results in Ga^+ ion implantation and the depth of implantation depends on the accelerating voltage: for example, the penetration depth is as much as ~20nm at 25keV [12, 13]. This implantation of gallium ions is a serious problem during FIB specimen preparation since it can impact the results obtained during localized chemical analysis. Another common problem during FIB specimen preparation is amorphization due to ion implantation. This problem can be reduced by milling the specimen using low energy during the final stages of sample preparation. The ion-specimen interaction also produces secondary electrons, which can allow surface imaging during the milling process.

Gallium ion sources are widely used for FIB milling for the following reasons [12]:

1. Ga exists in the liquid state at near room temperature due to its low melting point (T_m= 29.8 °C)
2. Ga ions can be focused to small probe size (diameter < 10nm).
3. Long metal-ion source life because of low Ga volatility.

4. Low Ga vapor pressure and viscous liquid behavior so Ga can be used in pure form.
5. The Ga ion beam can also be used to image the sample surface.

In addition, organometallic vapors can be injected into the FIB chamber to deposit materials on to the sample surface. For example, Pt can be deposited for surface protection as well as for sample lift-out purposes.

In recent dual-beam instruments, the FIB and SEM function in tandem, as shown schematically in figure 2.5. This arrangement allows very convenient operation for semiconductor characterization since the SEM can be used simultaneously for imaging while the FIB milling is taking place.

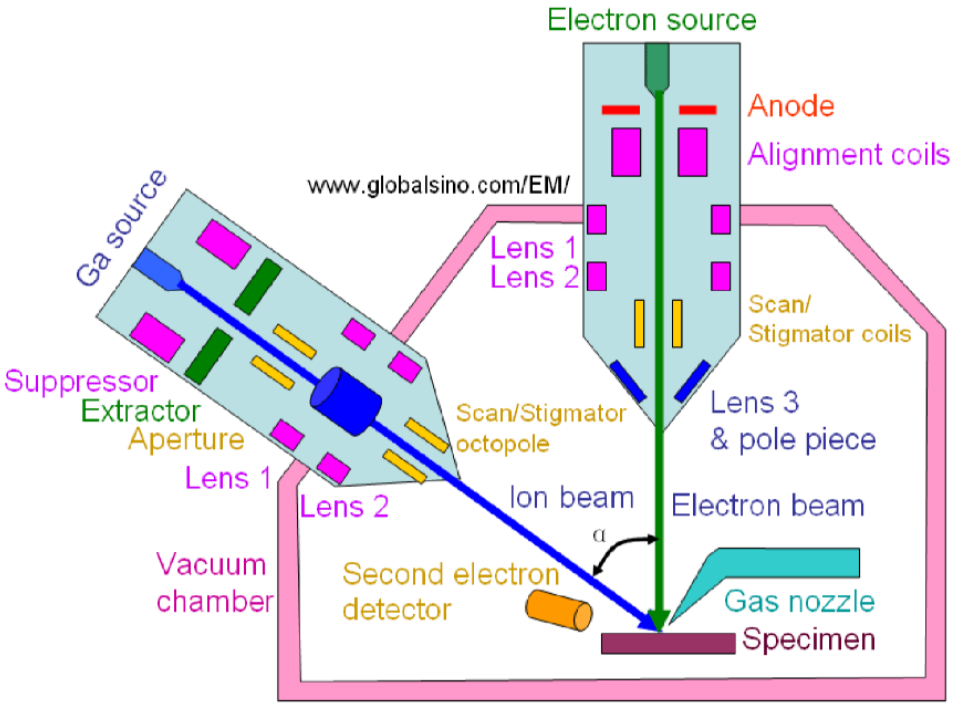

Figure 2.5 Schematic of dual-beam FIB-SEM [9].

2.2.3 FIB Specimen Preparation Using *in situ* Lift-Out

Lamellae that are of the desired thickness and size suitable for TEM observation can be fully prepared within the dual-beam FIB-SEM chamber. The following steps briefly summarize a general approach that can be used for reliable TEM lamella preparation using the NOVA FIB-SEM.

The sample is attached to a mount using copper tape, and a small strip of carbon tape is used to prevent charging. The mount is loaded into the system. A thin rectangular strip, typical size of 15 µm x 4 µm x 500 nm, of carbon is deposited on the sample surface using the carbon vapor system, followed by deposition of a thin platinum strip (300nm) using the electron beam mode at 5keV (1.6nA beam current). This is followed by deposition of a much thicker Pt strip (~2 microns) with the desired size, typically 12 µm x 2 µm x 2µm, using the ion-beam mode (Ga^+ ions) at 30keV (0.1nA). The Pt-deposited region is trenched out by ion-milling on both sides at 30keV (7nA) followed by making undercuts. A micromanipulator is used to insert a tungsten needle, which is the Omniprobe tool in the NOVA 200 FIB. The needle is placed immediately adjacent to the sample and then Pt-welded to the sample. The sample is then cut-off using the Ga ion beam and lifted clear of the bulk specimen. The lamella is mounted on a Cu-grid, and then initially thinned at 30keV (0.3nA) and finally cleaned at 5keV (0.23nA). A similar procedure can be used with the Helios G5 instrument, which has the added advantage of allowing final milling to be done at beam energies as low as 500 eV when really thin lamellae are required.

2.2.4 Transmission Electron Microscopy (TEM)

The TEM is an indispensable instrument for semiconductor characterization due to its capability to acquire structural and analytical information over scales ranging from sub-Ångstrom to microns. The electron gun, electron accelerator, and several condenser lenses form the electron beam that is incident onto the sample. The objective lens and several magnifying lenses then produce the final magnified image. The images produced are affected by aberrations from the objective lenses, which blur out the sample information and reduce the attainable resolution [14].

There are multiple modes of TEM operation for imaging and collecting further useful information. Diffraction-contrast images are formed with small objective apertures, using either the transmitted beam (bright field - BF) or one of the diffracted beams (dark field - DF) to form the image. High-resolution images are formed by phase-contrast imaging, where many scattered electron interfere to form an image, and involves using either a large or no objective aperture. High-resolution TEM can provide images of crystal structure at the atomic scale [15].

The latest generation of TEMs with aberration correction can easily achieve spatial resolution on the sub-Ångstrom scale, whereas TEMs without aberration correction can only achieve resolutions in the range of 1.5 to 3 Å [15]. The resolution of TEMs without aberration correction is insufficient to identify individual atomic columns along higher-index zone axes, and at many crystal defects or interfaces.

2.2.5 X-ray Topography (XRT)

X-ray topography is a non-destructive technique that can be used to map growth defects and non-uniformity within single crystals at depths of up to tens of microns. XRT can be performed in transmission or reflection geometry and is capable of imaging wafers that are up to 300 mm in diameter [16]. This method mostly utilizes Cu $K_{\alpha 1}$ as X-ray source at operating voltage of 50 kV and 30 mA current. The XRT technique has been used in this dissertation research to probe the underlying morphology of bulk GaN substrates grown by HVPE and ammonothermal methods, as described in Chapter 5.

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CHAPTER 3

ETCHED AND REGROWN GAN-ON-GAN VERTICAL *p-n* POWER DEVICES

This chapter describes structural investigations of etched and regrown GaN-on-GaN vertical *p-n* devices that were provided by the group of Professor Yuji Zhao. A manuscript describing some of these results has been published in the Journal of Electronic Materials.

3.1 Introduction

Previous generations of GaN devices have been grown on substrates such as SiC and sapphire, resulting in high defect densities (10^8-10^{10} cm^{-2}) because of the large lattice mismatch between materials [1-6]. These defect densities then limit possible GaN applications because of degraded device performance. Recent developments in growth using high-vapor-pressure epitaxy (HVPE) have led to the commercial availability of freestanding GaN substrates with defect densities of $<10^6$ cm^{-2} [7]. These bulk GaN substrates can then be used to grow epitaxial GaN-on-GaN composites with greatly reduced defect density ($<10^4$ cm^{-2}), making it possible to fabricate high-power GaN-on-GaN vertical devices [8].

The etching of mesa structures is commonly used to terminate or isolate high-voltage GaN devices, in particular to reduce low-voltage breakdown at junction edges [1,9]. Mature semiconductor devices based on Si or SiC have well-established termination techniques whereas suitable schemes for the development of GaN devices are still under development. The mechanisms utilized for the former materials systems, such as lateral doping profiles by ion implantation, are not suitable for GaN [18]. Chemical or

plasma etching is essential for selective-area doping in order to create complicated device structures and to fabricate integrated circuits [11]. Since doping is also done during epitaxial growth, the development of an effective etching technique for GaN is required in order to create vertical power devices with the desired stacking or edge termination [9].

Control of etching effects is crucial for the fabrication of GaN-on-GaN heterostructures. The quality of the etched surface can directly affect device performance since etching may lead to a rough regrowth interface, as well as precipitation of dopants and the continued growth of dislocations from existing defects. These factors can all contribute to degraded device performance. For example, surface roughness and near-surface damage during etching are likely to cause current leakage and lead to low breakdown voltages. Even though the density of threading defects (TDs) is generally less in epitaxial devices, the random presence of TDs is liable to increase the severity of device breakdown and also reduce device reliability. TDs are known to act as trap states in GaN films, and are considered to be responsible for locally high reverse-leakage current due to the presence of metastable acceptor- and donor-like states in the vicinity of defects [12-15]. The negative effects on leakage current caused by dislocations present in GaN films grown heteroepitaxially on sapphire substrates is well-known [16-17]. This current research has investigated the microstructure of GaN-on-GaN heterostructures after the initial GaN surfaces had been etched in different ways, and additional GaN was grown. This GaN etching and regrowth was intended to replicate the process required to achieve selective-area doping when fabricating vertical devices.

3.2 Materials and Methods

Devices for investigation were grown homoepitaxially by metal-organic chemical vapor deposition (MOCVD) on 2-inch *c*-plane n^+ GaN substrates with a carrier concentration of ~10^{18} cm^{-2}. The substrates were obtained from Sumitomo Electric Industries Ltd. Hydrogen gas was used as the carrier gas and the growth temperature was ~1040°C. Ammonia, trimethylgallium, bis(cyclopentadienyl)magnesium, and silane were used as precursors for N, Mg and Si dopants, respectively. The doping concentrations in the *p*-GaN layers, as measured by secondary-ion mass spectroscopy (SIMS), were ~7x10^{19} cm^{-3} of Mg, while the thick unintentionally-doped (UID) GaN layers had 1.0x10^{16} cm^{-3} of Si [10]. Nine microns of UID-GaN was grown on the GaN substrates for all devices before removal from the MOCVD chamber, except for one control sample, and transfer to a separate chamber for etching, as described below. The surfaces of the UID-GaN wafers were then treated using either a rapid dry-etch by inductively-coupled plasma (ICP) or a process involving multiple ICP dry-etching treatments with progressively decreasing power. These treatments are summarized in Tables 3.1 and 3.2, respectively.

Table 3.1. ICP etching treatment for fast-etch-only devices.

Step	ICP Power	RF Power	Cl_2	BCl_3	Ar	DC Bias	Etch time	Etch rate
1	400	70	30	8	5	159	2 min	~288nm/min

After completion of the etching treatments, wafers were transferred back into the MOCVD chamber, followed by growth of thin UID-GaN insertion layers with

thicknesses of ~25-60 nm. Finally, Mg-doped *p*-GaN layers with thicknesses in the range of 300-500 nm were grown on all samples. The activation of the regrown *p*-GaN layers was carried out by rapid thermal annealing at 700 ºC for 20 min in a N_2 environment.

Table 3.2. ICP treatment with four-step etching process. Etching started with high RF power, which was then progressively decreased.

Steps	ICP Power	RF Power	Cl_2	BCl_3	Ar	DC Bias	Etch time	Etch rate
1	400	70	30	8	5	159	2 min	~288 nm/min
2	400	35	30	8	0	95	1 min	~140 nm/min
3	400	5	30	8	0	21	2 min	~20 nm/min
4	400	2	30	8	0	15	3 min	~8 nm/min

All devices were cleaned in acetone/isopropyl alcohol and then hydrochloric acid to remove native surface oxides before deposition of metal contacts. Electron-beam evaporation was used to deposit metal stacks of Pd/Ni/Au (10 nm/20 nm/50 nm) for *p*-GaN ohmic contacts. Mesa isolation, with mesa diameters ranging from 90 µm to 210 µm, was also achieved using ICP dry etching. Mesa isolation and hydrogen-plasma passivation were used for the edge termination [18-20]. *n*-GaN ohmic contacts were deposited by electron-beam evaporation of metal stacks of Ti/Al/Ni/Au (20 nm/130 nm/50 nm/150 nm), on the backsides of the GaN substrates. The PlasmaTherm Apex ICP chlorine-based tool, which is a load-locked, inductively-coupled plasma etch system, was used for etching, and the process gases were BCl_3Cl_2, Ar and N_2. The samples for etching were placed on a 4-inch Si carrier wafer. Current-voltage (I-V) measurements (which were limited to 1000V) were made using a Keithley 2410 source-meter, and a Tektronix

370A was used for higher breakdown voltage measurements. The ramp rate (bias step) was 1V and the dwell time for each point was 100ms.

Samples suitable for cross-sectional observation by transmission electron microscopy (TEM) were prepared by focused-ion-beam (FIB) milling with a FEI Nova 200 FIB-SEM dual-beam system, with initial thinning done at a Ga ion energy of 30 keV and final thinning done at 5 keV. A FEI-Philips CM-200 FEG TEM operated at 200 kV was used for imaging the device cross-sections.

3.3 Results and Discussion

The growth of UID-GaN, as well as etching and regrowth/over-growth with *p*-GaN, are drawn schematically in Figure 3.1. The location of the etched area at the interface between the original UID-GaN and the thin UID-GaN insertion layer is indicated by the red line in Figure 3.1 (a). The effects of etching are obviously most likely to appear at this interface, as well as possibly within the *p*-GaN, and hence these regions are of most interest.

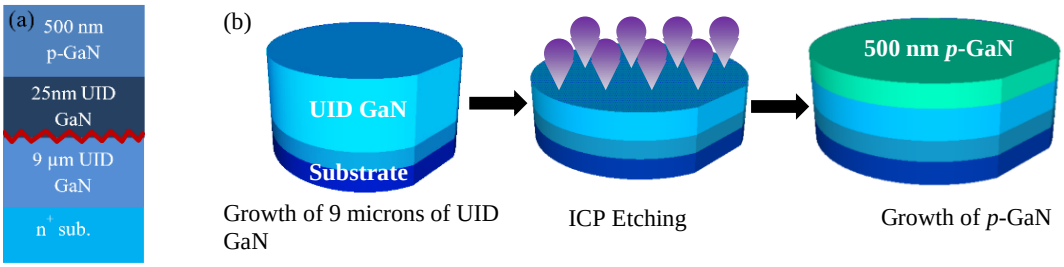


Figure 3.1. Schematics: (a) Device structure, with red line indicating location of etching done before regrowth; and (b) ICP etching and *p*-GaN regrowth process [21].

Figure 3.2. (a) compares typical reverse-bias characteristics for the fast-etch-only and multiply-etched devices, and figure 3.2 (b) compares the electrical performance of the three types of devices under forward-bias conditions. There was a marked difference in the typical breakdown voltages (BV), which ranged from 45-95V for the fast-etched devices but ranged from 1200-1270V for the multiply-etched devices. In comparison, the BV ranged from 600 to 700V for as-grown devices [22]. Moreover, the leakage current for fast-etch-only devices was much higher in comparison with the multiply-etched devices, and the as-grown devices had low leakage current compared to fast-etch-only and multiply-etched devices [22].

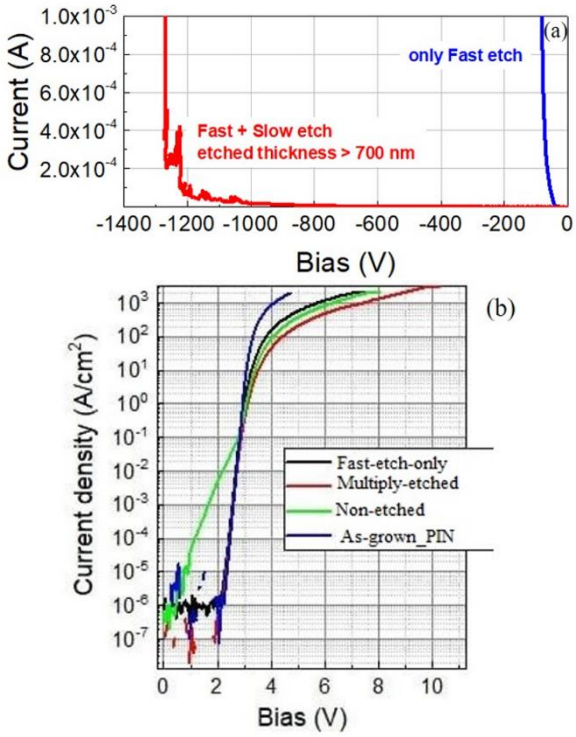


Figure 3.2. (a) Reverse *I-V* characteristics showing typical breakdown voltages for fast-etch-only and multiply-etched devices; (b) Forward *I-V* curves for fast-etch-only, multiply-etched and non-etched devices.

Figure 3.3 shows a cross-section TEM micrograph of the non-etched/as-grown control device. No visible interface can be observed in this heterostructure, and the separate UID-GaN/*p*-GaN layers are indistinguishable. Figures 3.4 and 3.5 show TEM micrographs of the fast-etch-only device structure taken at low and higher magnifications. These images reveal a clearly visible interface between the *p*-GaN and UID-GaN layers, as indicated by the arrows. The interface has a high concentration of small precipitates, and further precipitates and growth defects are also visible within the *p*-GaN layers (see enlargements in Figs. 3.5 (c) and (d)). Figures 3.5 (c) is a higher-magnification image of region 'C' from 3.5 (b), which shows a large 'V'-shaped defect, while figure 3.5 (d) shows a higher magnification image of region 'D' from 3.5 (b) which shows a cluster of small defects. Figure 3.5 (e) is a dark-field TEM image which clearly shows the regrowth interface. Small and large, some 'V'-shaped, defects are spread all over the area within the *p*-GaN layer. Figure 3.5 (f) is a bright-field image which shows small 'V'-shaped defects along the top surface of the *p*-GaN layer. These several images also show indications of precipitation which is concentrated within and around the 'V'-shaped defects.

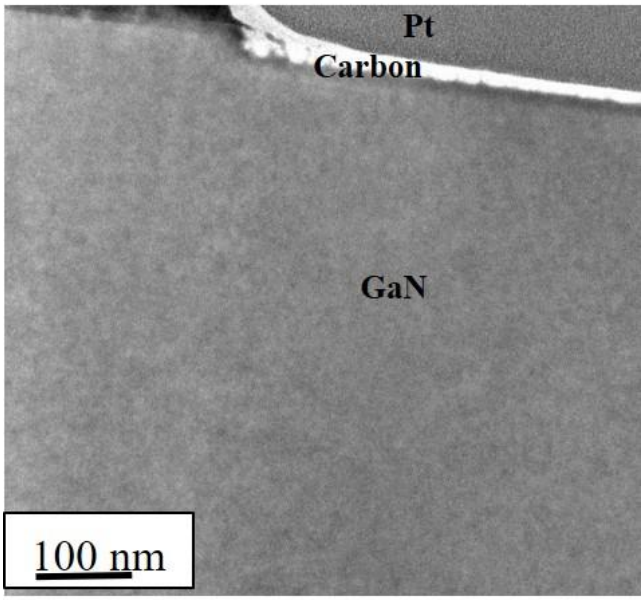


Figure 3.3. Cross-section TEM micrograph showing upper region of non-etched *p*-GaN/UID-GaN control structure with no visible interface (Pt and carbon are deposited for surface protection during FIB milling).

For comparison purposes, figures 3.6 (a) and (b) show TEM cross-section micrographs of a multiply-etched and regrown device, at low and higher magnifications, respectively. The location of the interface is apparent because of the presence of precipitates, thought to be magnesium, in the *p*-GaN layer, so that the separate *p*-GaN and UID-GaN layers can be distinguished. This particular device had been subjected to an applied reverse bias of 1kV without exhibiting device breakdown, before the FIB cross-sectioning was done.

From a closer comparison of figures 3.5 and 3.6, for example, it is clear that the effects of etch damage are substantially reduced by modifying the etching procedure. The fast-etch-only device showed a thick interface with a high density of precipitates concentrated near the interface. The high leakage current of these devices and their breakdown at low voltage (45-95V) can most likely be attributed to surface roughness

induced by etching, which was revealed in a previous atomic-force microscopy study of similar as-grown and etched devices [22].

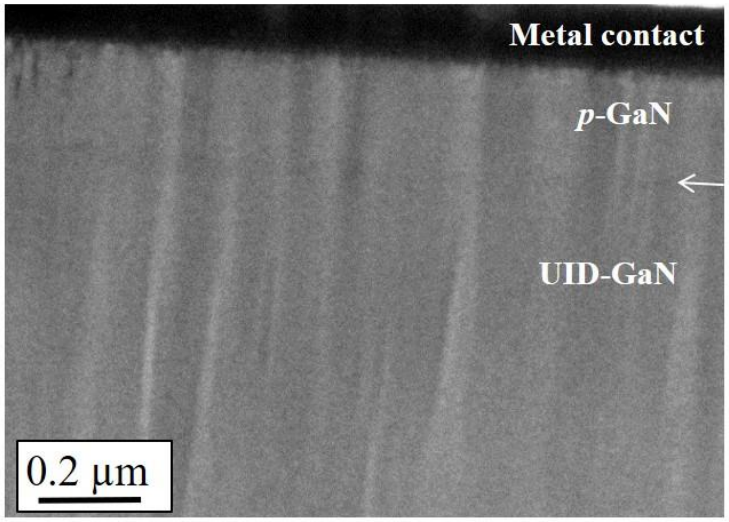
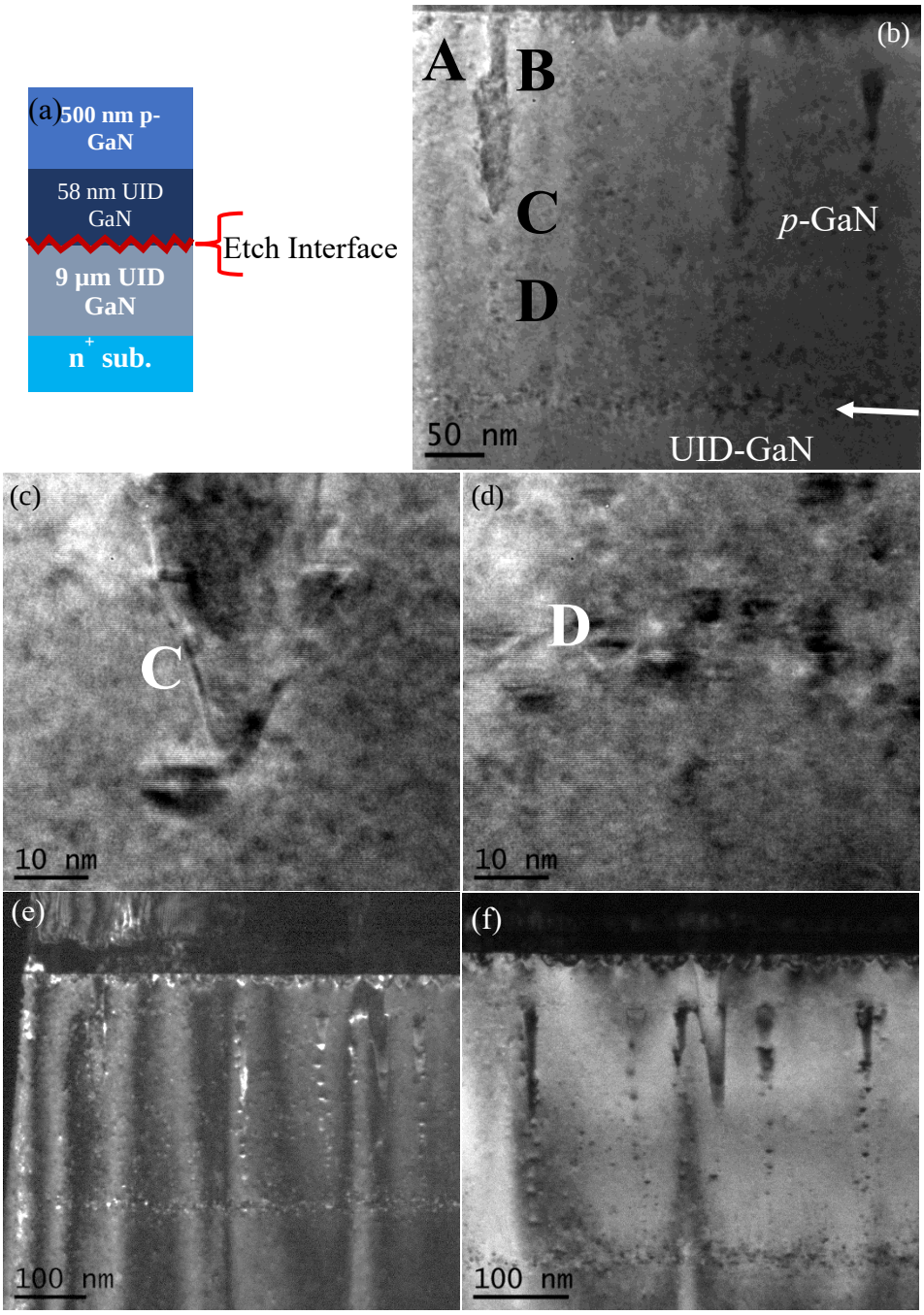


Figure 3.4 Cross-section TEM micrograph of fast-etch-only device. Arrow indicates location of *p*-GaN/UID-GaN interface.

The etched area had a significant segregation of precipitates near the interface, as well as silicon, oxygen and magnesium which were detected from SIMS analysis [10]. The presence of Si could possibly be due to left-over residue in the MOCVD chamber, which was deposited on the surfaces when the devices were re-introduced for *p*-GaN regrowth after the etching treatments. As a donor dopant, Si would create a thin layer with *n*-type behavior, and it would contribute to early device breakdown by acting as a Zener tunnel diode. However, this early breakdown was avoided in later devices which had been treated with multiple etch rates.



3.5 (a) Schematic of device structure. Cross-sectional TEM micrographs of fast-etched device: (b) Medium-magnification; (c) High-magnification image of area marked as 'C' in (a); (d) High-magnification image of area marked as 'D' in (a); (e) Dark-field (0002) image shows clear interface between *p*-GaN and UID-GaN interface; (f) Bright-field image clearly shows regrowth interface and defects.

The fast-etch-only device showed the presence of many small defects within the *p*-GaN layer. These defects varied in size with the largest being near the surface and smallest being close to the interface. Variations in Mg concentration throughout the *p*-GaN growth could have influenced the size of these defects, as observed earlier by Tomiya [23], who reported that higher Mg concentration tended to reduce the size of defects while increasing their density. Moreover, these defects would act as sites for Mg precipitation within *p*-GaN and contribute to decreased electrical conductivity and increased on-resistance [24].

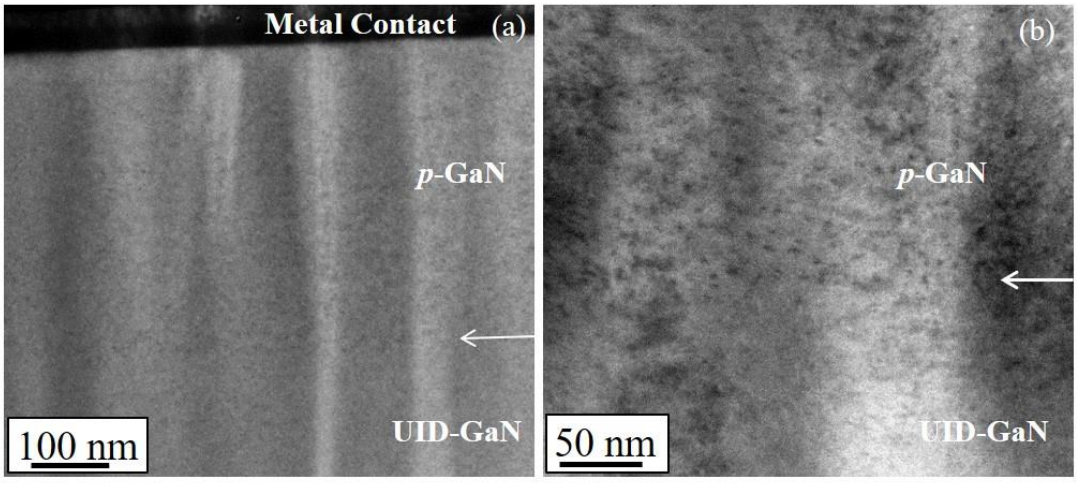


Figure 3.6. (a) Cross-section TEM micrograph of *p*-GaN/UID-GaN interface (arrowed) of multiply-etched device after being stressed to reverse bias of 1kV; (b) Higher-magnification micrograph of *p*-GaN/UID-GaN interface (arrowed) for same device. Small precipitates visible in *p*-GaN layer are tentatively identified as Mg precipitates caused by device annealing.

In comparison, the multiply-etched devices achieved reverse bias of 1kV without breakdown. Thus, it was clear that the etching-induced damage, rather than Mg precipitates in the *p*-GaN layer, had contributed to the lower breakdown voltage. The reduced etch damage as a result of the multiple etching steps lessened the negative effects

on device performance, in agreement with the TEM cross-sectional images, which showed no indication of interface precipitates or other defects.

Finally, in order to develop a sense for repeatability of device behavior, in particular for any leakage current/breakdown voltage hysteresis, one of the multiply-etched devices was stressed to a reverse bias of 1kV for 10 biasing cycles. Significantly, the device showed no sign of failure nor any change in performance. Figures 3.7 (a) and (b), respectively, are lower and higher magnifications of TEM cross-section images showing this particular device. Figure 3.7 (c) shows the region of *p*-GaN/UID-GaN interface at higher magnification. The region of the interface is not populated by precipitates, as can be seen in figure 3.7, although some are faintly visible in the *p*-GaN layer.

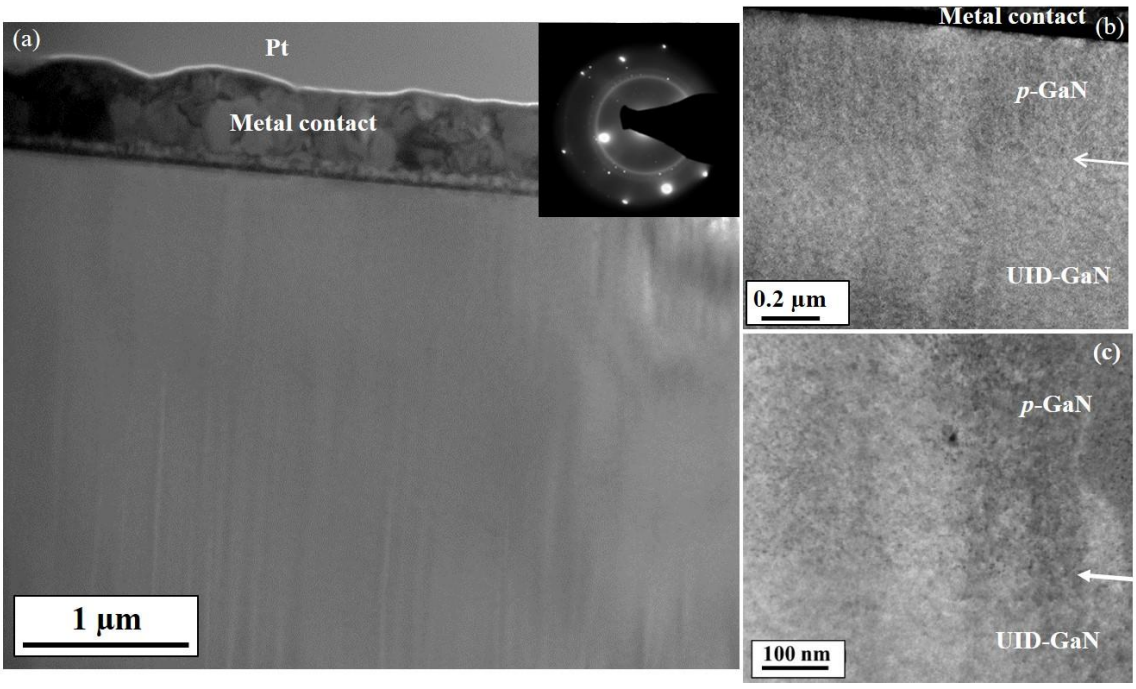


Figure 3.7. (a) Cross-section TEM micrograph of multiply-etched device after stress-testing to reverse bias of 1kV for 10 biasing cycles; (b) Micrograph showing *p*-GaN/UID-GaN interface; (c) Higher-magnification electron micrograph showing region of *p*-GaN/UID-GaN interface (arrowed) for same device.

3.4 Conclusions

Etching of UID-GaN layers with high RF power and high etch rate was found to damage the regrowth interface and cause considerable degradation of device performance. Fast-etch-only devices had typical BVs in the range of 45-95V compared to BVs in the range of 600-700V for as-grown devices. The affects of etch damage was clearly observable in TEM images. The interface between *p*-GaN and UID-GaN layers was visible as well as large concentrations of precipitates along the interface. Many small growth defects and precipitates were observed within the *p*-GaN layer. Smaller defects were visibly closer to the interface whereas larger defects were located closer to the surface. These defects would deteriorate device performance. Multiple etching stages, finishing with lower RF power and slow etch-rate, lead to improved device performance, and no visible interfacial growth defects were observed. Multiply-etched devices had BVs in the range of 1200-1270V, thus performing much better than fast-etch-only devices. The fast etching had clearly contributed to early device breakdown, whereas an improved etching process with progressively reducing RF power led to significantly improved better device performance. Similar etching procedures should be used in the future fabrication of high-power vertical *p*-*n* devices.

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CHAPTER 4

STRUCTURAL BREAKDOWN IN GaN-ON-GaN VERTICAL *p-n* POWER DEVICES

This chapter describes an investigation of structural breakdown in GaN-on-GaN vertical *p-n* devices that had been stressed to failure under reverse bias. The stressed devices were provided by the group of Professor Yuji Zhao. The major results from these studies have been published [1].

4.1. Introduction

High densities of threading dislocations (TDs) (10^8~10^{10} cm^{-2}) contribute to non-radiative recombination and scattering centers, and limit the performance of electrical and optical GaN-based devices [2]. Hence, minimizing the defect density is critical to maximizing device performance [3]. Buffer layers, such as AlN, are commonly used to alleviate lattice-mismatch and differences in thermal expansion between GaN and common substrates, but fabrication of these layers adds to overall cost and complexity. Recent developments in growth using hydride vapor pressure epitaxy (HVPE) have led to the availability of freestanding GaN substrates with defect densities less than ~10^6 cm^{-2} [4]. Epitaxial GaN-on-GaN layers can be grown with reduced defect density (<10^4 cm^{-2}) using these bulk substrates, making it feasible to fabricate vertical high-power GaN-on-GaN devices with high breakdown voltages [5,6].

Despite the reduced dislocation density in homoepitaxially-grown GaN vertical devices, it is still possible that the random presence of TDs could result in major reverse-

bias current leakage and eventual device breakdown. For example, TDs were reported to increase the current leakage path in GaN-based devices [7], and another study reported that TDs were responsible for leakage current and breakdown [8]. A study of GaN-based light-emitting diodes (LEDs) grown on sapphire by metalorganic chemical vapor deposition (MOCVD) suggested that leakage current was related to dislocations [9], and another study suggested that V-defects and associated TDs were responsible for high leakage current [10]. It was also reported that GaN-based blue-light LEDs, grown on freestanding GaN substrates by MOCVD, had suppressed leakage current due to low TD density [11]. Studies of GaN-on-GaN templates grown by molecular beam epitaxy (MBE) found that reverse-bias leakage occurred at dislocations with a screw component [12]. It was also concluded that screw dislocations were more detrimental for gate leakage than edge or mixed dislocations [13]. A study of AlGaN/GaN high electron mobility transistors (HEMTs) correlated increased gate leakage current with defects near gate edges [14], and HVPE-grown GaN Schottky diodes with micro-pipe defects were also reported to show increased leakage current [15].

A detailed investigation on the effect of dislocations on the performance of vertical GaN *p-n* diodes/devices is lacking. Although it was suggested that TDs caused leakage in vertical diodes grown by MOCVD [16], microscopy-based studies do not appear to have been reported. Such studies seem crucial for further device development since the structural and electrical properties of devices depend sensitively not only on the growth method and the growth conditions, but also on the presence of dopants, impurities, and the device structure [7]. This current study has investigated the morphology of GaN-on-GaN vertical devices that had been electrically stressed to breakdown. A major objective

of the study was to gain insight into the failure mechanism and to establish whether surface treatment or surface etching methods during regrowth would have any impact on the device failure.

4.2. Experimental Details

Growth of the investigated devices basically followed the same process described in the previous chapter. Two sets of devices were investigated in this study, labelled here as A-series and L-series. Both sets were surface-treated (UV-ozone 45 min. + HF 5 min. + HCl 5 min.) before regrowth. The UV-ozone treatment oxidized the UID-GaN surface, and the following treatments with HF and HCl were intended to remove surface contaminants. In addition, the A-series devices were etched using inductively-coupled plasma (ICP) dry-etching. The ICP dry-etching procedure was a sequence of etching steps intended to remove the surface layer and minimize etch damage, which was achieved by employing four consecutive etching steps with decreasing RF-power (70W, 35W, 5W and 2W) [17]. More details about the growth and treatment procedures can be found elsewhere [18] and in the previous chapter. The L-series devices showed breakdown voltages in the range of 200-750V with typical reverse-leakage current densities of 10 A/cm^2 at breakdown, whereas the A-series devices exhibited substantially higher breakdown voltages of 1070-1270 V with typical reverse-leakage current densities of 4 A/cm^2 at breakdown.

Samples suitable for cross-sectional observation by transmission electron microscopy (TEM) were prepared by focused-ion-beam (FIB) milling using a FEI Nova 200 dual-beam system, with initial thinning done at 30 keV and final thinning done at 5

keV. Scanning electron micrographs were also recorded with the Nova 200 during progressive milling across the surface craters that were observed to be present in failed devices. A Philips-FEI CM-200 FEG transmission electron microscope (TEM) operated at 200 keV was used for structural imaging. All the TEM images were taken with samples oriented at $[1\bar{1}00]$ zone axis. High-resolution TEM images were taken by phase-contrast imaging with no objective aperture. Low-magnification and medium-magnification images were taken using a medium-sized objective aperture for improved image contrast.

4.3. Results

Examples of plan-view SEM images of devices L5, L6, L7, L12, L14 and L16 after they had been reverse-bias-stressed to breakdown, are shown in figure 4.1. This set of devices had been regrown with an insertion layer of 250nm, followed by another 500nm of *p*-GaN, after the surface layer of the original UID-GaN had been chemically treated. All stressed devices showed extensive, crater-like surface pits, and most also showed evidence for lengthy cracks extending across parts of the craters and even outside the device region in some cases. Sixteen devices were stressed to breakdown and all 16 showed similar crater-like surface damage with varying crater depths. The measured depths of these craters ranged from 13 to 38 microns, as illustrated schematically in figure 4.2.

Lift-out with the FIB was performed across the crack on Device L14, as indicated by the arrow in figure 4.1(e), and the corresponding TEM image is shown in figure 4.3. This cross-sectional image reveals a high density of dislocations along the left side of the

crack, which appear to be more concentrated immediately adjacent to the crack and towards the GaN surface. For comparison, figure 4.4(a) shows a cross-sectional TEM image of an unstressed device, where the white arrow indicates the position of the interface between *p*-GaN and the insertion layer. No dislocations or cracks are visible and no structural damage due to surface treatment can be observed between the insertion layer and the UID-GaN layer. The enlargement in figure 4.4(b) shows the *p*-GaN/insertion layer/UID-GaN region where there are no visible defects or surface damage, although the top *p*-GaN layer shows evidence for Mg precipitates, as reported previously in Chapter 3.

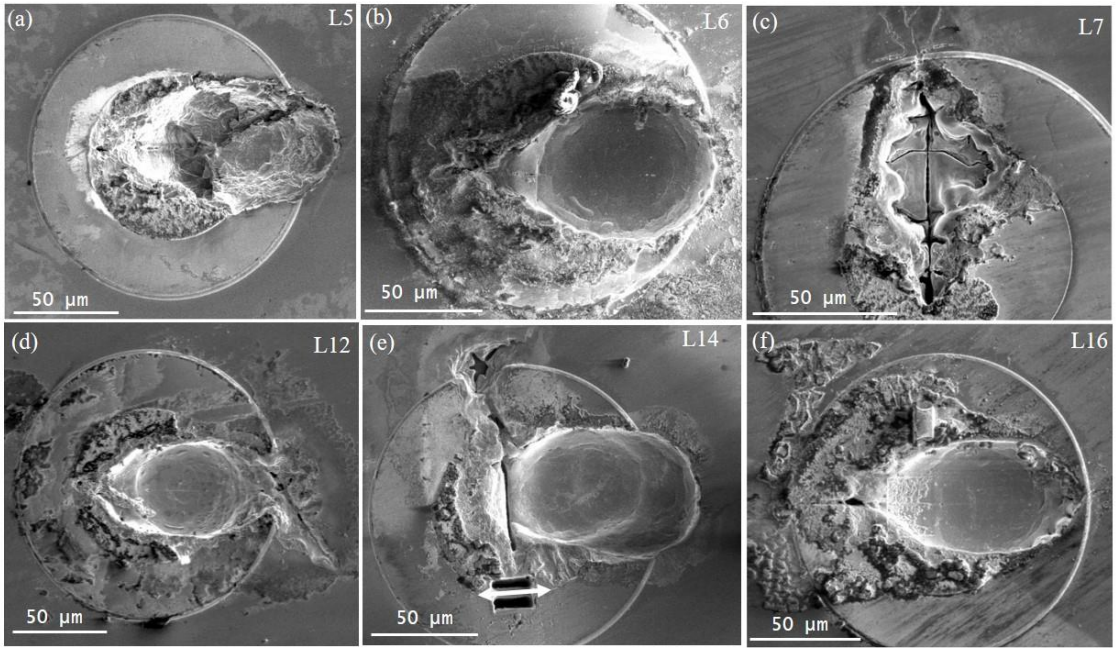

Figure 4.1 SEM images showing examples of devices that had been reverse-bias-stressed to electrical breakdown, revealing extensive surface damage, including deep craters and wide cracks: (a) Device L5, (b) Device L6, (c) Device L7, (d) Device L12, (e) Device L14, and (f) Device L16.

In order to appreciate the full extent of defect formation in the failed devices, Device L16 was progressively milled in cross-section across the surface crater and then repeatedly imaged *in situ* with the SEM after another roughly 5 microns had been milled away. Figure 4.5(a) shows a plan-view SEM image of the original device after failure, before commencement of trenching. Milling started at the top of the crater at the position indicated by the arrow, and then proceeded progressively upwards. Figures 4.5(b)-5(h) are a series of SEM images showing the progress of this milling over an area of roughly 30μm x 25μm. Figure 4.5(b) reveals a collection/cluster of voids that are present in the GaN substrate beneath the crack. Figures 4.5(c)-5(e) show parts of the same void cluster after additional material, about five microns at a time, had been removed. Figures 4.5(c)-5(f) show a cluster of threading dislocations at the center of the image, right below the crack, and away from the surface crack. Figure 4.5(e) shows a threading dislocation extending from the crater surface into deep within the substrate, over a vertical distance of almost 80 microns.

In addition to the chemical etching used for processing of the L-series, devices A1 and A2 of the A-series were ICP-dry etched, followed by the growth of a 50-nm-thick GaN insertion layer and overgrowth with 500 nm of *p*-GaN. Device A1 suffered electrical breakdown at a reverse bias of ~1.27kV. It was then studied for surface anomalies, as represented by the SEM image in figure 4.6. The surface shows pits near the center of the circular contact, with a long crack that extends across part of the device to outside the device region. The crater and the crack surface morphology appear similar to that observed for the L-series devices despite the considerable difference in breakdown voltages.

Device ID	L1	L2	L3	L4	L5	L6	L7	L8	L9	L12	L13	L14	L15	L16
Depth (μm)	20	13	22	38	35	25	28	35	20	36	30	37	34	16

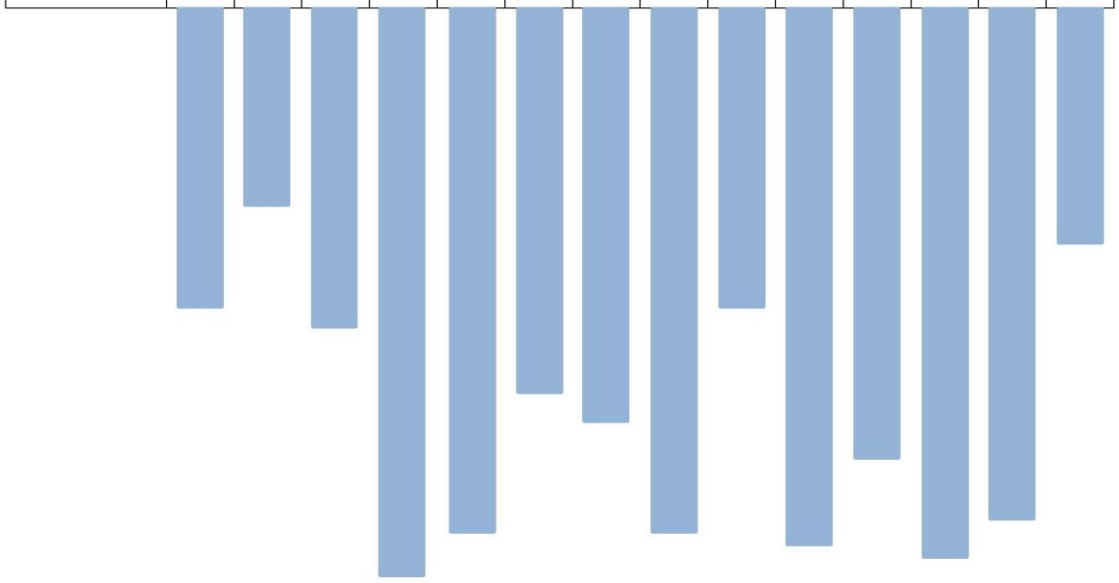

Figure 4.2. Schematic illustrating maximum crater depths in Series L devices after they had been stressed to failure.

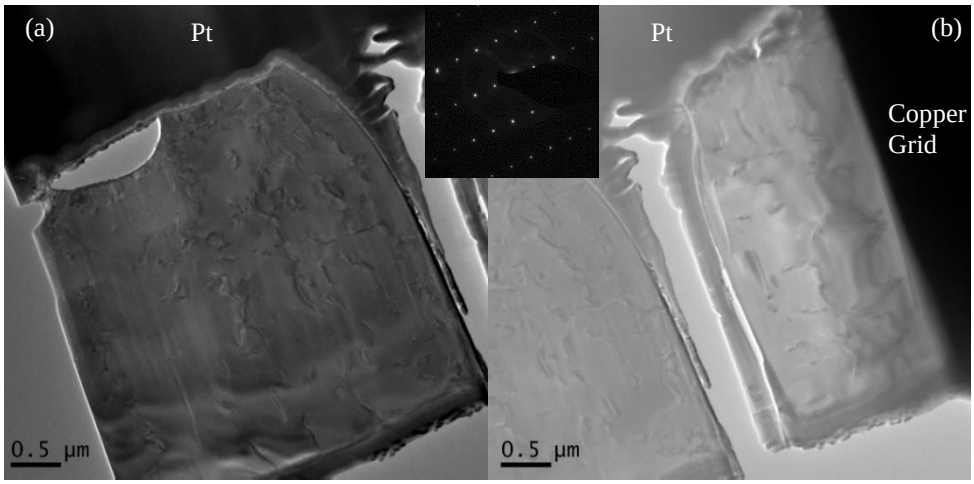

Figure 4.3. TEM cross-section images of Device L14 from lift-out location marked in figure 4.1(e), showing left side (a), and right side (b), of crack with dislocations more concentrated towards crater surface and near crack region.

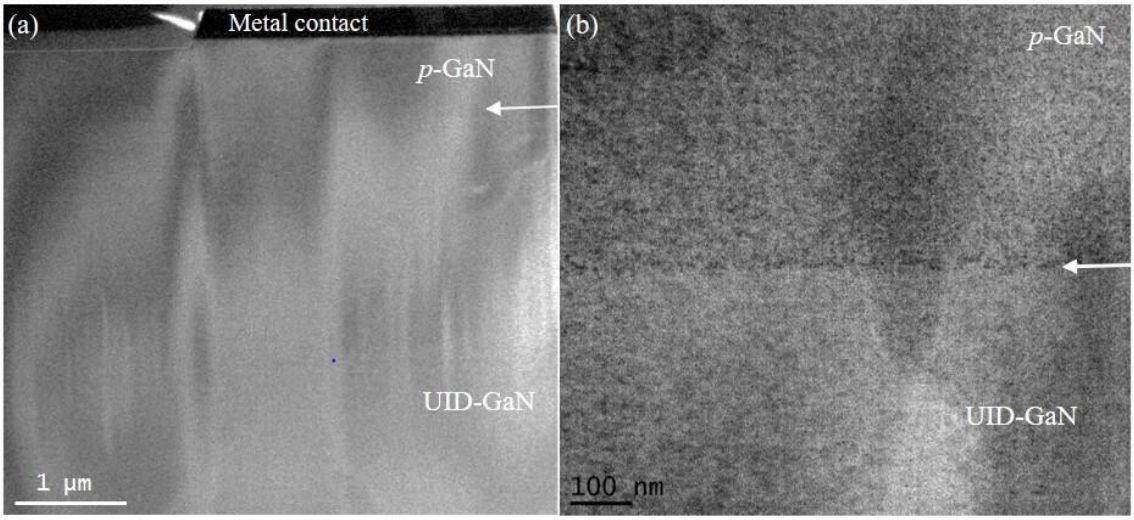

Figure 4.4 (a) TEM cross-section image of unstressed device showing absence of dislocations across the sample; and (b) Enlargement of *p*-GaN/insertion layer/*UID*-GaN region showing no surface-treatment damage or structural defects, although some precipitates are visible in *p*-GaN layer.

A cross-section sample suitable for TEM observation was lifted-out across the visible crack of Device A1, as marked on figure 4.6 by the double-headed arrow. Figure 4.7 shows corresponding TEM images. Figure 4.7(a) reveals that the entire top surface region here is riddled with dislocations, not unlike the L-series devices, and a crack is also visible that penetrates downward by more than 4 microns from the crater surface. Locations marked from 'A' to 'D' on Fig. 4.7(a) are shown in the series of images from Fig. 4.7(b) to Fig. 4.7(e). Left and right sides of the large crack are shown in Figures 4.7(c)-7(d), respectively. Figure 4.7(e) from location 'D' shows another crack that extends almost 2 microns downwards from the crater surface. Dislocations here are concentrated close to the crack and along the top surface, as clearly visible in Figs. 4.7(c)-7(e). The GaN top surface is not flat/even because of the irregular loss of surface material that occurred during the device breakdown.

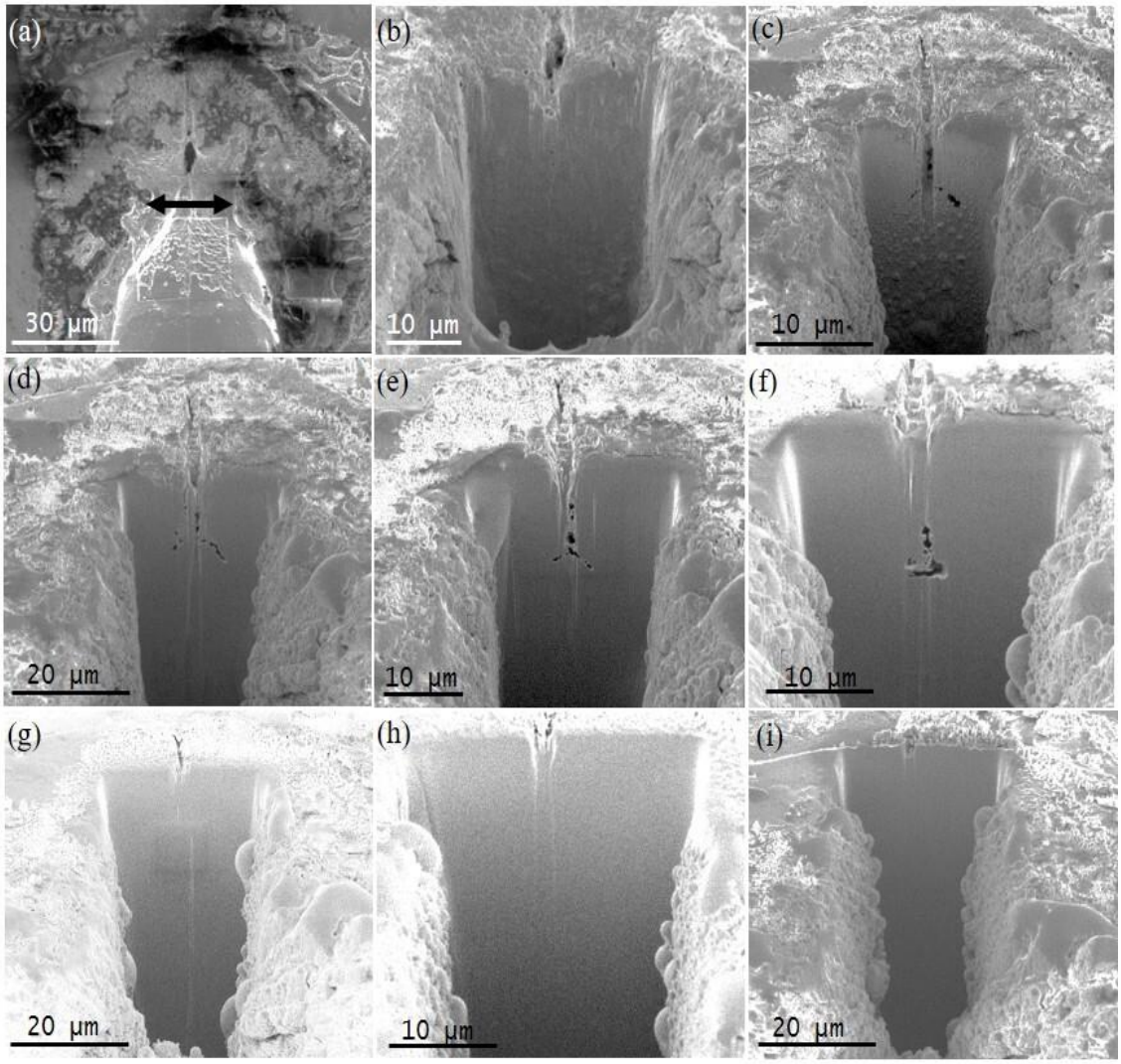

Figure 4.5. Series of SEM images of Device L16, showing progressive cross-sectional milling across area of 30µm (length) x 25µm (depth): (a) Plan-view image showing location where milling started (black double-arrowed line); (b) Cross-section image after 5 microns of milling, showing presence of voids right below surface crack; (c) Cluster of voids; (d) Voids extending from surface just below crack to ~16 microns deep; (e) Voids and TDs; (f) Presence of TD cluster all over area; (g-h) TDs extending from substrate; (i) Milled almost to edge of device.

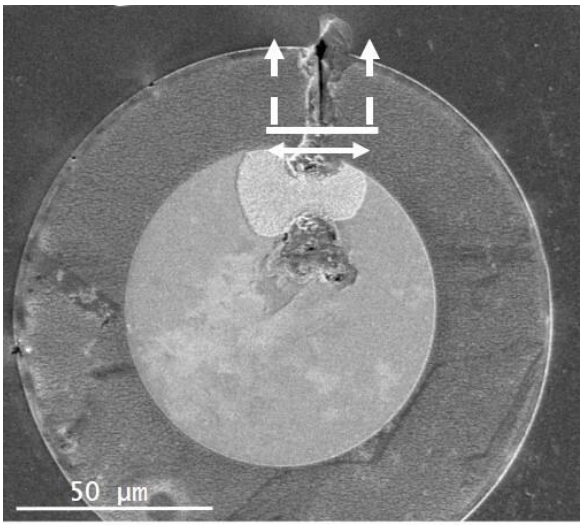

Figure 4.6. Plan-view SEM image of Device A1 after reverse-bias breakdown at ~1.27 kV, showing surface pits and crack. White arrowed lines indicate location of cross-sectional milling and double-arrowed line indicates position of TEM lift-out.

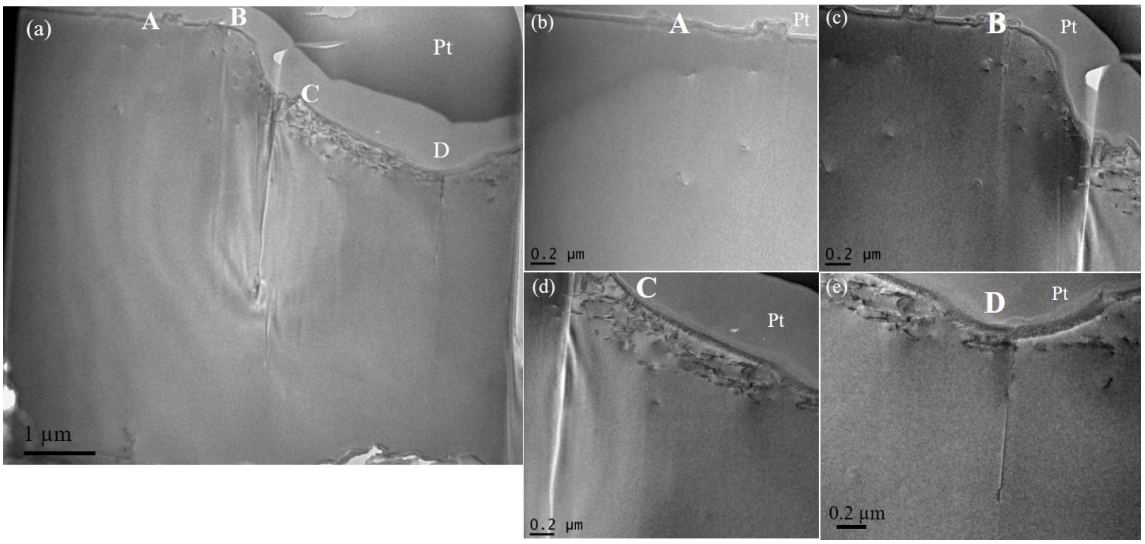

Figure 4.7. Cross-section TEM images after lift-out of Device Al across surface crack, from location marked with double-arrowed line in figure 7: (a) Low-magnification image showing large crack about 4 microns deep, as well as smaller cracks and presence of dislocations concentrated near cracks and surface. Locations marked as 'A', 'B', 'C' & 'D' shown in following series of images; (b) High-magnification image of location 'A' showing precipitates within *p*-GaN; (c) High-magnification image of location 'B' showing precipitates and left-side of large crack; (d) High-magnification image of location 'C' showing right-side of large crack and surrounding dislocations; and (e) High-magnification image of location 'D' showing 2-micron deep smaller crack and surrounding dislocations.

Figure 4.8 shows a sequence of cross-sectional SEM images of Device A1 after progressive milling had been done, along the direction indicated by the arrowed lines on figure 4.6. Figures 4.8(a) and 4.8(c) reveal the presence of TDs all across the milled region, while figure 4.8(b) shows a TD that extends about 49 microns downwards from the crater surface. Figures 4.8(d) and 8(e) show that the surface crack is almost 10 microns deep, and that TDs are present everywhere.

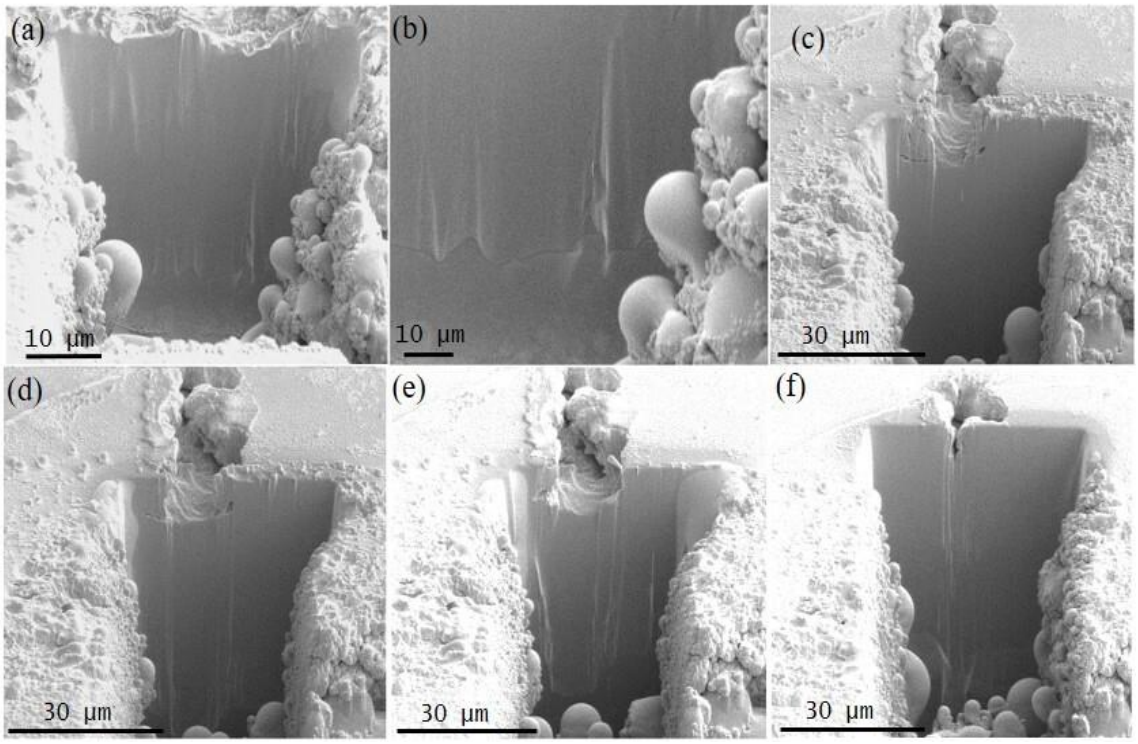

Figure 4.8. Series of SEM images of Device A1 after progressive cross-sectional milling across area of 40µm (length) x 25µm (depth), from location marked with arrowed white lines in Fig. 6: (a) TDs all over milled area; (b) High-magnification image focused on TD that extended ~49 µm down from crater surface; (c) Voids concentrated nearer to crack; (d) Surface crack that appears to be ~10 µm deep extending into device; (e) TDs near and well away from crack and extending deep into substrate; and (f) Milling stopped at edge of device and surface crack extending beyond the device is observed.

Finally, for comparison purposes, Fig. 4.9 shows TEM images of the equivalent Device A2, which was not subjected to any electrical tests. Fig. 4.9(a) shows that no

dislocations or cracks are present in the lifted-out region. The enlargement in Fig. 4.9(b) shows the *p*-GaN/insertion-layer/UID-GaN area, and no etching-based damage or structural defects are visible.

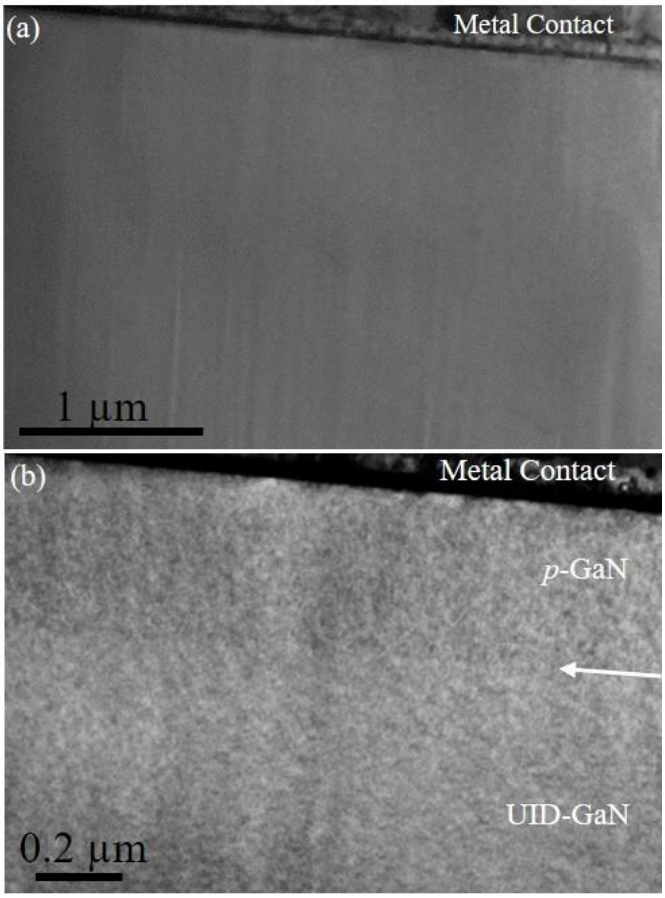

Figure 4.9. Cross-section TEM images of Device A2 which was not subjected to any electrical tests: (a) Low-magnification image shows no cracks or dislocations; (b) High-magnification image of *p*-GaN/insertion-layer/UID-GaN area shows no visible etch damage or defects.

4.4. Summary

This chapter has described the irreversible structural changes observed in two sets of GaN-on-GaN high-power devices after they had been reverse-biased to the point of electrical breakdown. Surface-treated devices (Series L) showed deep craters and lengthy

cracks after failure had occurred. The craters extended across much of each failed device and had depths of tens of microns. The failed devices also showed the presence of cracks, clusters of voids and TDs under the craters. The cracks typically extended about 6-10 microns downwards. The voids were present in the substrate region while TDs were present across entire devices extending deep into the substrate. Devices that had been etched and then overgrown (Series A) showed similar morphology after failure although their breakdown voltages were considerably higher. Cracks were again observed on the cratered surfaces of the failed devices, while cross-section TEM images showed the formation of threading dislocations that were concentrated close to the cracks and near the crater surfaces. Similar dislocations were never observed in unstressed devices subjected to identical etch-regrowth treatment.

The presence of pre-existing defects in devices before regrowth does not seem to be an important factor in device failure since the Series-L and Series-A devices were grown on similar substrates but they had significantly different breakdown voltages. The lower breakdown voltages for the surface-treated devices can most likely be attributed to surface oxidation during UV-ozone treatment similar to the devices studied in Chapter 3. Overall, these results provide highly useful information about the reliability of vertical power electronics and should contribute to the design of better future devices.

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CHAPTER 5

IMPACT OF SUBSTRATE MORPHOLOGY ON REVERSE-BIAS STRESS-TESTING OF GaN-ON-GaN VERTICAL *p-n* DEVICES

This chapter describes an investigation of the impact of substrate morphology on the reverse-bias electrical response of GaN-on-GaN vertical *p-n* devices. The stressed devices were provided by the group of Professor Yuji Zhao. The principal results are in the process of being prepared for publication.

5.1 Introduction

Wide-bandgap semiconductors are highly promising materials for power applications. GaN-based devices are of particular interest because of their enhanced electrical performance in comparison with traditional Si-based devices such as thyristors, metal-oxide semiconductor field-effect transistors, and insulated-gate bipolar transistors. GaN offers these advantages because of its intrinsic material properties, which include wide bandgap (3.44 eV), high critical electric field (~10x Si), low intrinsic carrier concentration, high thermal conductivity (~1.5x), and high saturation velocity (~3x) [1-5]. Vertical GaN devices are preferred to lateral devices for better packaging, higher efficiency, high-current and high-voltage applications [6-7].

Previous generations of GaN devices grown on common substrates, such as Si, SiC and sapphire, had very high defect densities (10^8-10^{10} cm^{-2}), primarily due to the large lattice mismatch between materials [8]. The high density of threading dislocations (TDs) contributes to non-radiative recombination and scattering centers that eventually limit device performance [9]. Since such defects can affect breakdown voltage, leakage

current, device reliability, high-temperature reverse bias and operating lifetime, it is critical to minimize defect densities [10]. Developments in growth techniques such as hydride vapor pressure epitaxy (HVPE) and ammonothermal methods have led to the availability of freestanding GaN substrates with defect densities of lower than ~10^6 cm^{-2} [11]. Epitaxial GaN-on-GaN layers can be grown with even lower defect density (<10^4 cm^{-2}) using these bulk substrates, in turn making it feasible to fabricate vertical high-power GaN-on-GaN devices with high breakdown voltages [12].

Although these developments in growth techniques have led to bulk GaN substrates with substantially less defects, the random locations of these defects is still liable to cause inferior device performance. For example, it is well known that TDs are the most likely reason for leakage current in GaN-based devices [13-14]. These TDs could act as trap centers due to the presence of metastable acceptor- and donor-like states in the vicinity of the defects [15-16]. Increased leakage current has been reported in GaN-based devices grown by various methods such as molecular beam epitaxy (MBE) [17-18], metal-organic vapor phase epitaxy (MOCVD) [19,20], and HVPE [21]. Since defects cannot be avoided altogether, device fabrication should be concentrated when possible in areas with minimized defect densities, rather than areas with large defect concentrations, in order to avoid defect-related current leakage and possible device breakdown. It has been reported that HVPE-grown GaN substrates with extensive regions of low dislocation density (~10^5 cm^{-2}) could be obtained by deliberately concentrating the dislocations around pits with predetermined locations [22]. Another report suggested that the selective growth of GaN by HVPE, through openings in an SiO_2 mask, likewise reduced the dislocation density (TDs~10^7 cm^{-2}) in overgrown layers [23]. One study

reported that bulk GaN grown by HVPE achieved a low etch-pit density (EPD) of ~10^6 cm^{-2} by removal of the base Si substrate at high temperature [24].It was also reported that bulk GaN with "near-perfect" crystal quality (EPD of ~$3x10^2$ cm^{-2}) could be obtained by HVPE GaN regrowth after the intentional formation of an ordered array of etch pits in the base GaN layer; it was stated that the etch pits transformed into voids after regrowth and thus did not propagate dislocations into the overgrown layers [25]. Another study reported bulk GaN grown by ammonothermal methods, again with low dislocation density (<10^6 cm^{-2}) [26].

Given these developments of bulk GaN substrates of high quality, there is much interest in understanding how the morphology of these substrates might influence subsequent device behavior. Devices may also be impacted by processing methods such as plasma etching for selective-area doping that are used to create complicated device structures, and edge-termination techniques such as hydrogen passivation [27-29]. The complexity of possible causes for degraded devices can lead to confusion over the exact reason(s) for device failure. The work described in this chapter has involved an investigation of GaN-on-GaN vertical devices that were grown on HVPE substrates originating from two different sources and one ammonothermal substrate. The fabricated devices were characterized by X-ray topography (XRT), scanning electron microscopy (SEM) and transmission electron microscopy (TEM), and the results have been correlated with electrical performance, as measured in terms of leakage current under reverse-bias conditions.

5.2 Experimental Details

Three GaN substrates from different sources were used for device fabrication. Two were grown by the HVPE method and are labelled here as S-1 and S-2. The third substrate was grown by ammonothermal methods and is labelled here as S-3. These freestanding n^+-GaN substrates were 2-inch *c*-plane with carrier concentrations of ~10^{18} cm^{-2}. Unintentionally-doped (UID) GaN drift layers with thicknesses in the range of 2.0-2.4 microns were grown on all three GaN substrates by MOCVD, followed by overgrowth with Mg-doped *p*-GaN layers with thicknesses of 300-500 nm. Activation of the regrown *p*-GaN layers was carried out by rapid thermal annealing at 700 ºC for 20 min in a N_2 environment. Devices fabricated on each wafer had sizes ranging from 60-300 µm in diameter and are identified later according to their size.

Metal stacks of Pd/Ni/Au (10 nm/20 nm/50 nm) for *p*-GaN ohmic contacts were deposited by electron-beam evaporation. Mesa isolation and hydrogen-plasma passivation were used for edge termination. Metal stacks of Ti/Al/Ni/Au (20 nm/130 nm/50 nm/150 nm) for ohmic contact were deposited by electron-beam evaporation on the backsides of the GaN substrates. Native surface oxides were removed before deposition of the metal contacts by cleaning with acetone/isopropyl alcohol, followed by hydrochloric acid. The PlasmaTherm Apex ICP chlorine-based tool, which is a load-locked, inductively-coupled plasma (ICP) etch system, was used for etching, and the process gases were BCl_3Cl_2, Ar and N_2. The samples were placed on a 4-inch silicon carrier wafer for etching.

Current-voltage (I-V) measurements (limited to a maximum of 1000 V) were made using a Keithley 2410 source-meter. The ramp rate (bias step) was 1 V and the

dwell time for each point was 100 ms. All of the fabricated devices in this study had turn-on voltages of ~3.4 V, as measured from forward I-V characteristics. The reverse I-V characteristics of the devices were compared with respect to a specific leakage current cut-off, which was set at 10^{-6} A in order to avoid irreversible device breakdown. Some of the devices that were later used for cross-sectional observation were reverse-bias stressed until breakdown had occurred.

XRT images of the various wafers were taken with a Rigaku XRT-100, operated at 50 kV voltage and 30 mA current. All XRT measurements were taken under reflection mode with Cu $K_{\alpha 1}$ X-ray source. Samples suitable for cross-sectional TEM observation were prepared by focused-ion-beam (FIB) milling using a FEI Nova 200 dual-beam system, with initial thinning done at 30 keV and final thinning done at 5 keV. Scanning electron micrographs were also recorded during FIB milling. A Philips-FEI CM-200 FEG TEM operated at 200 keV was used for structural imaging.

5.3 Results

Figure 5.1 compares reverse-bias curves for the devices fabricated on Wafer S-1, with Fig. 5.1 (a) showing results for devices that had high reverse-bias voltages before the leakage current limit of 10^{-6} A was reached, and Fig. 5.1(b) showing those devices with low reverse-bias voltages. Table 5.1 lists the maximum voltages applied to each of these devices.

Figure 5.2 (a) is an XRT image of Wafer S-1 that shows a two-dimensional array of dark spots, which are roughly equally spaced with separation distances of ~1 mm. The red circles indicate locations of fabricated devices that had reverse-bias voltages of less

than 100 V before the leakage current cutoff threshold, whereas the white circles indicate the locations of devices with reverse-bias voltages of greater than 300 V. Figure 5.2 (b) shows a low-magnification SEM image of the devices fabricated at the locations circled in Fig. 5.2 (a). These have varying diameters, ranging from 60 μm to 300 μm, and are identified according to their size. Correlation of these images with the corresponding device measurements in Table 5.1, shows that fabricated devices that overlapped with the dark spots had reverse-bias voltage limits of less than 100 V and are thus considered to have performed poorly. In contrast, devices in locations away from such regions had reverse-bias voltages of greater than 300V before reaching the pre-specified leakage current threshold.

Table 5.1. Summary of I-V measurements for Wafer S-1			
60-1 Good (-320V)	100-1 Good (-300V)	200-1 Good (-300V)	300-1 Bad (<-50)
60-2 Bad (<-50)	100-2 Good (-330V)	200-2 Good (-320V)	300-2 Bad (<-50)
60-3 Bad (-150V)	100-3 Good (-330V)	200-3 Bad (<-50)	300-3 Bad (<-50)

Figure 5.3 shows an XRT image of Wafer S-2, where the red and white circles again indicate the locations of fabricated devices that showed low and high reverse-bias thresholds, respectively. Discontinuous, mostly vertical, features are visible that are roughly separated by ~ 1 mm. Table 5.2 shows corresponding I-V measurements of these devices. Those fabricated in locations overlapping with the discontinuous, vertical features had excessive leakage current under relatively low reverse-bias voltage, whereas

devices located away from such features performed more robustly, reaching reverse-bias voltage limits of greater than 300 V.

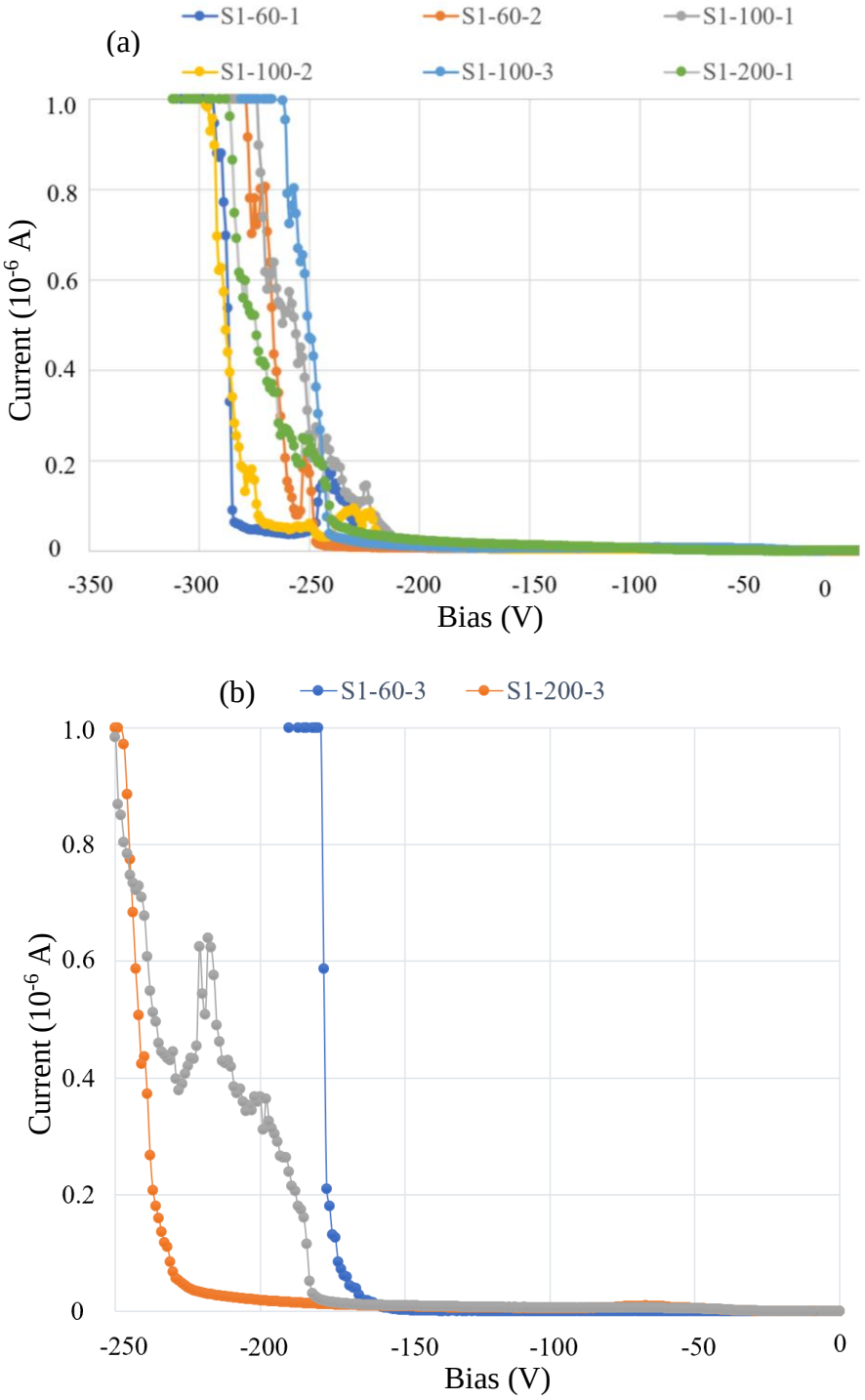

Figure 5.1. (a) Reverse-bias I-V curves for devices on Wafer S-1 that showed large reverse-bias voltages before reaching cut-off limit of 10^{-6} A; (b) Corresponding curves for devices on Wafer S-1 with lower reverse-bias voltage limits.

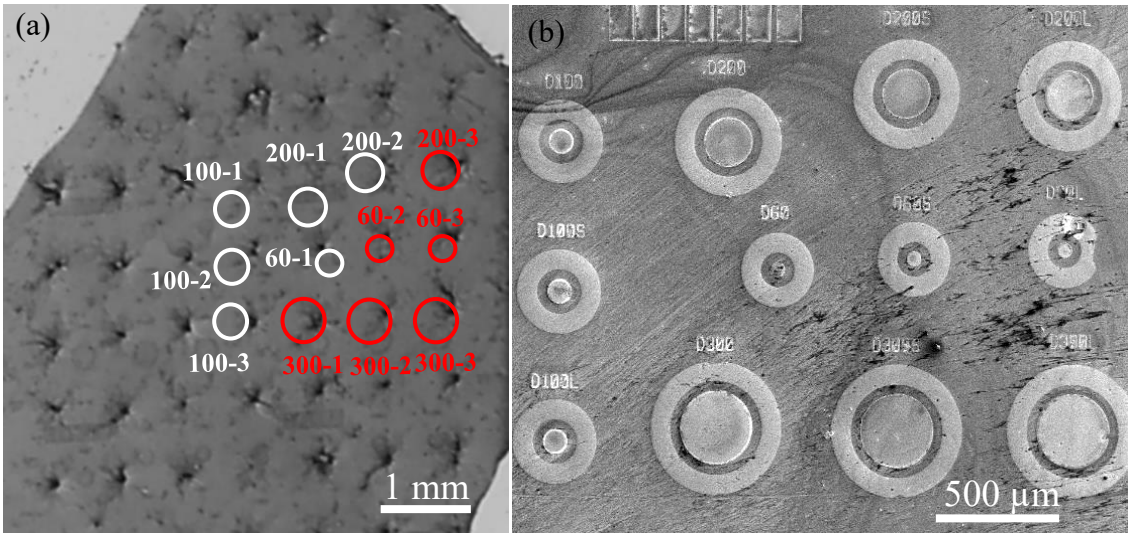

Figure 5.2. (a) XRT image of HVPE-grown Wafer S-1 showing two-dimensional array of dark spots with ~1mm separation. Circles indicate locations where devices were later fabricated. (b) Low-magnification SEM image showing devices fabricated at locations indicated in (a).

Table 5.2. Summary of I-V measurements for Wafer S-2			
60-1 Good (-310V)	100-1 Good (-290V)	200-1 Good (-330V)	300-1 Bad (-250V)
60-2 Good (-280V)	100-2 Good (-315V)	NA	NA
60-3 Bad (-185V)	100-3 Good (-280V)	200-3 Bad (-250V)	NA

Figure 5.4 is an XRT image of Wafer S-3, which is the GaN-on-ammonothermal GaN substrate, with red and white circles again indicating the locations of fabricated devices which showed low and high reverse-bias voltage limits, respectively. No noticeable morphology features are visible. However, devices fabricated on this wafer did not perform consistently, as shown by the electrical results summarized in Table 5.3.

Some devices reached high reverse-bias voltages of greater than 320V without significant leakage, whereas some devices only reached reverse-bias voltage limits in the range of 50-200V before substantial leakage current started to occur.

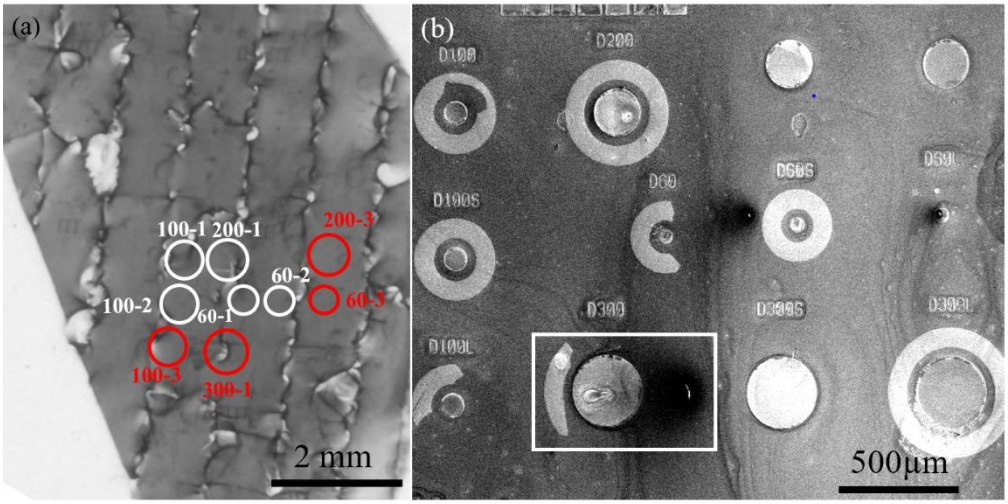

Figure 5.3. (a) XRT image of HVPE-grown Wafer S-2 showing discontinuous and vertical features with lateral separation of roughly ~1mm spacing. Circles indicate locations where devices were later fabricated. (b) Low-magnification SEM image showing devices fabricated at locations indicated in (a), the device within the box was stress-tested to breakdown: see Fig. 5.10.

Table 5.3. Summary of I-V measurements for Wafer S-3			
NA	100-1 Good (-370V)	200-1 Bad (-115V)	300-1 Bad (-50)
60-2 Bad (-50)	100-2 Good (-380V)	200-2 Bad (-240V)	NA
60-3 Bad (-185V)	100-3 Good (-380V)	200-3 Good (-340)	300-3 Good (-320)

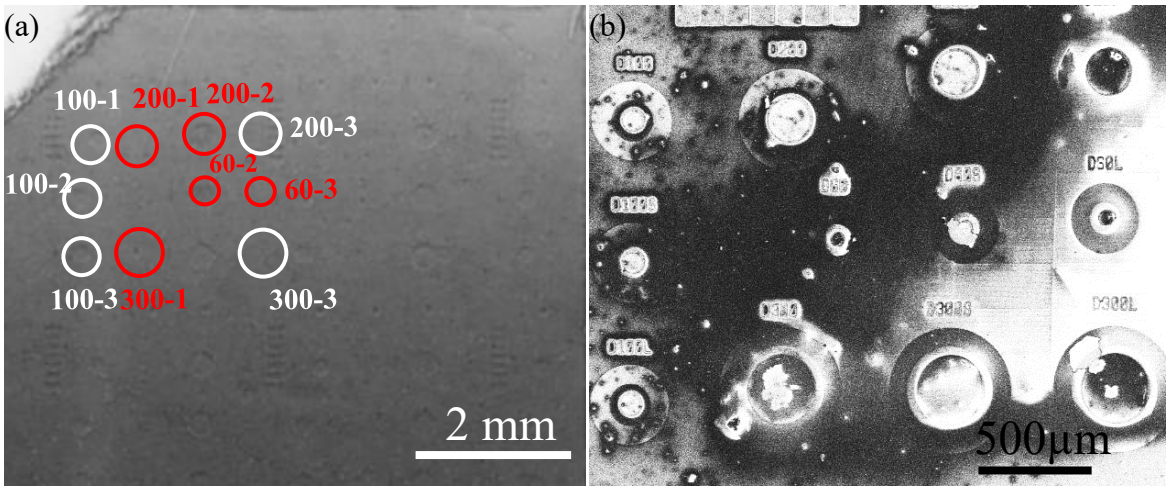

Figure 5.4. (a) XRT image of Wafer S-3 as grown by ammonothermal method. No macroscopic-sized features are visible. Circles indicate locations where devices were later fabricated. (b) Low-magnification SEM image showing devices fabricated at locations indicated in (a).

In order to provide further insight into this dependence of device behavior on surface and sub-surface features, two HVPE-grown wafers nominally similar to S-1 were etched and then observed by SEM. These two wafers, labelled here as S-A and S-B, were etched using ICP recipes with different RF power. Wafer S-A was etched with an RF power of 70 W for 2 minutes, which removed ~500 nm of the top surface layer, while Wafer S-B was etched with reduced RF power of 5 W for 2 minutes, which removed a surface layer of ~40 nm. Figure 5.5 shows XRT images of these two wafers: The regions observed by SEM after etching are circled.

Figure 5.6 shows plan-view SEM images of Wafer S-A after etching at the location circled in Fig. 5.5(a). Some surface features are faintly visible in Fig. 5.6 (a) but no large macroscopic-sized defect can be seen. Figure 5.6 (b) shows a medium-magnification image of the area indicated by the box in Fig. 5.6 (a): A cluster of pits,

labeled as L1, L2, L3 and L4, is visible. Figure 5.7 shows enlarged SEM images of these four regions. Figures 5.7 (a) and 5.7 (b) show inverted, hexagonal-shaped pyramidal pits of different sizes. Figure 5.7 (c) shows a region with 5-6 closely-packed hexagonal pits, and Figure 5.7 (d) shows a continuous and large defect, possibly formed by the amalgamation of several pits.

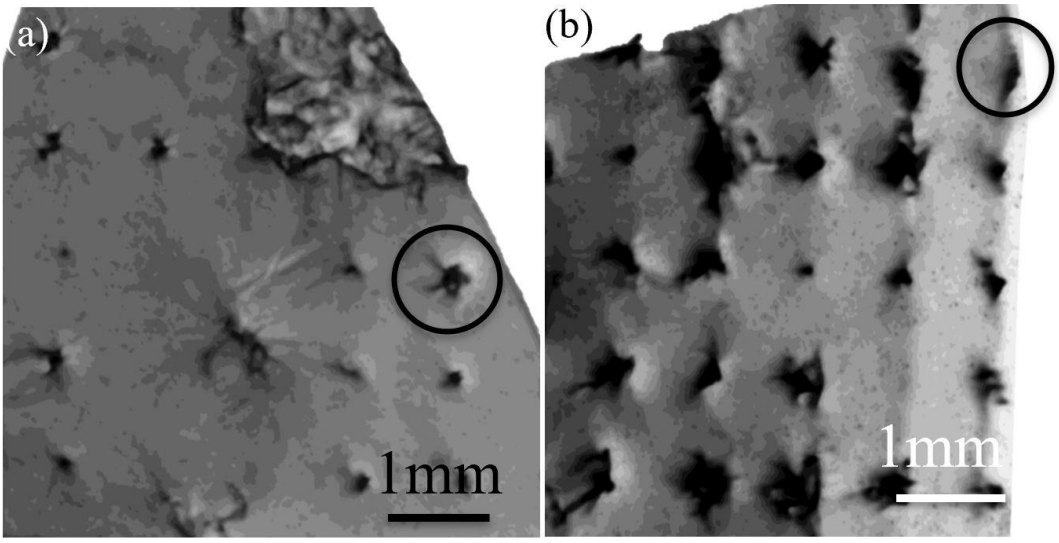

Figure 5.5. XRT images: (a) Wafer S-A; and (b) Wafer S-B. Enlargements of the circled regions are shown in later figures.

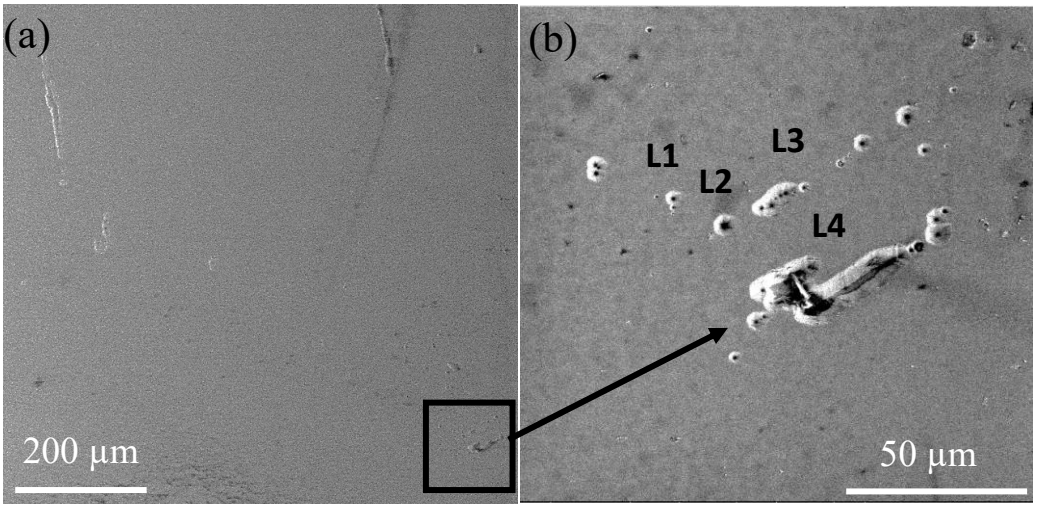

Figure 5.6. (a) Plan-view SEM image of Wafer S-A showing the location marked by circle in Fig. 5.5 (a): (b) Medium-magnification image showing cluster of defects from location marked in (a).

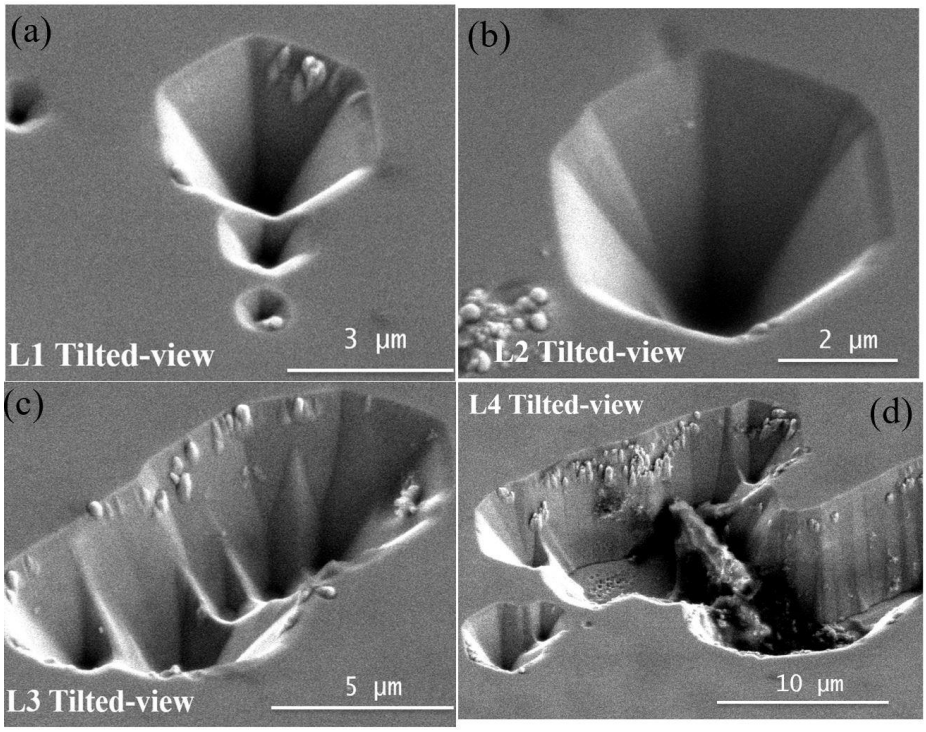

Figure 5.7. Enlarged images of Wafer S-A showing the locations marked in Fig. 5.6 (b): (a) Series of inverted-hexagonal pyramidal pits at location L1; (b) Large pit with width ~5.5 microns at location L2; (c) Closely-packed hexagonal pits ~5-6 number; (d) Large, irregular pit likely formed by amalgamation of several smaller pits.

Figure 5.8 shows SEM images of Wafer S-B from the location circled in Fig. 5.5(b). No noticeable surface features such as those visible in Fig. 5.7, could be seen. Clearly, the etching rates have played an important role in exposing the surface features observed in wafers by XRT. Thus, the faster, (deeper) etching has helped in exposing significant sub-surface features that are observed by XRT but are not revealed by the reduced (shallower) etching.

In order to better appreciate the possible role played by substrate defect morphology in device failure, the device 60-2 on Wafer S-3, which suffered premature breakdown (<50 V), was progressively milled in cross-section across the visibly damaged surface, and then imaged *in situ* with the SEM after completion of each milling cycle.

Figure 5.9 (a) shows an SEM image of the device before commencement of trenching. The series of SEM images in Figs. 5.9 (b)-5.9 (g), each taken after another roughly 5 microns had been progressively milled away, show the substantial presence of threading dislocations extending deep (~ 26 microns) into the substrate. Finally, Fig. 5.9 (h) shows a plan-view image taken after the milling had been completed.

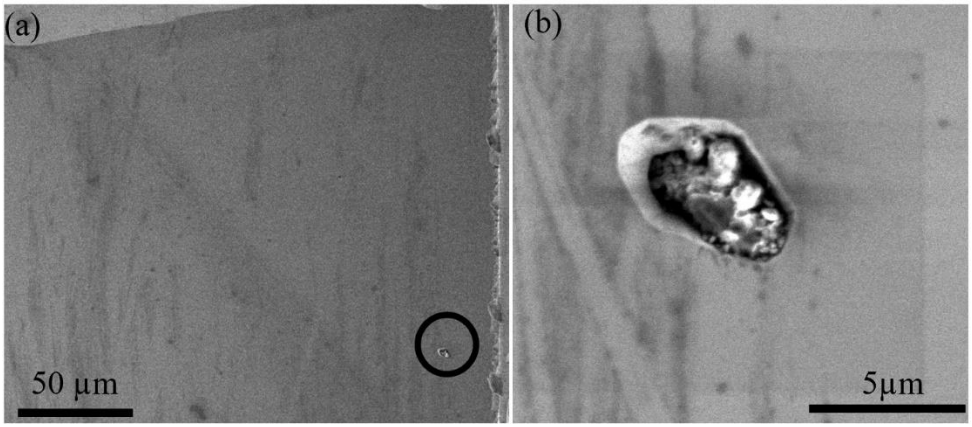

Figure 5.8. Plan-view SEM images of Wafer S-B from location circled in Fig. 5.5(b): (a) Low-magnification image showing no substantial surface features; (b) Higher-magnification image showing irregular surface pit at location circled in (a).

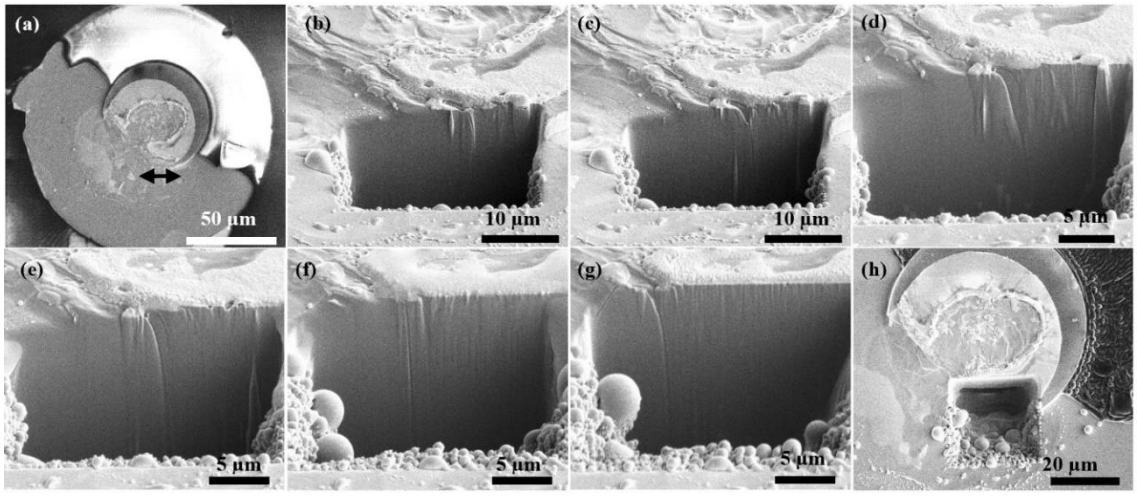

Figure 5.9. Series of SEM images of Device 60-2 on Wafer S-3, showing progressive cross-sectional milling across surface area of 25µm (length) x 25µm (depth): (a) Plan-view image, also showing location where milling started (double-arrowed line); (b-g) Cross-section images each taken after 5 microns of milling, showing presence of dislocations; (h) Plan-view image taken after completion of milling.

The device 300-1 on Wafer S-2, whose location was overlapping with the features observed in XRT image (device marked by rectangular box in Fig. 5.3(b)), was similarly progressively milled in cross-section across an area of 40 microns x 30 microns. This particular device had suffered premature breakdown and showed crater-like surface damage, as marked by an arrow in Fig. 5.10(a). This crater-like pit was 100 microns long, almost 50 microns wide at its center, and almost 30 microns deep. The series of SEM images shown in Fig. 5.10(b)-10(g), reveal the presence of threading dislocations penetrating deep into the substrate as well as clusters of voids, similar to the results reported in Chapter 4. Similar progressive milling that was undertaken on devices with high reverse-bias voltages (>300 V) showed an absence of dislocations or voids. These results agree with previous studies where devices that had been reverse-bias stressed to failure showed the presence of dislocations, cracks and voids in SEM and TEM images.[30]

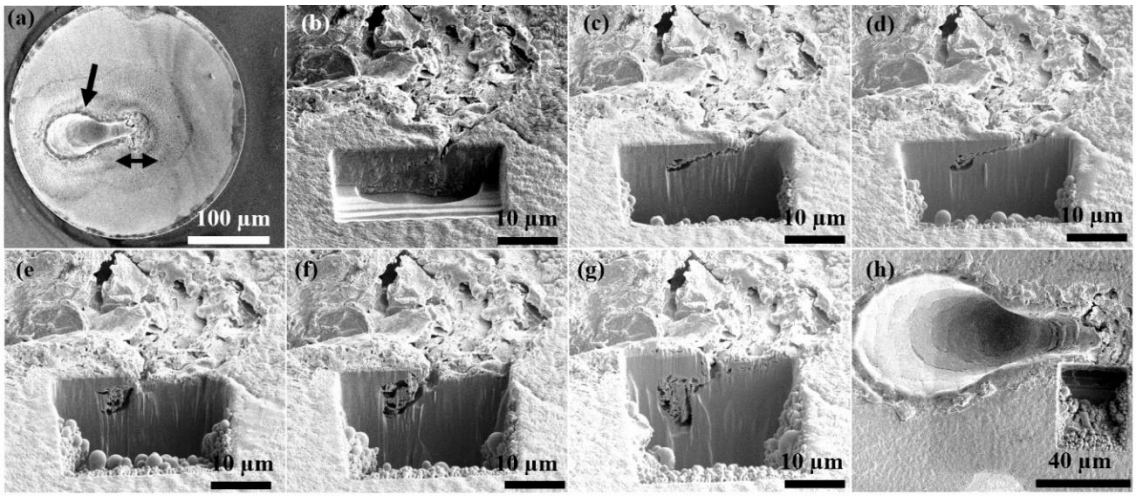

Figure 5.10. Series of SEM images of Device 300-1 on Wafer S-2, showing progressive cross-sectional milling across surface area of 40µm (length) x 30µm (depth): (a) Plan-view image showing location where milling started (double-arrowed line) and crater-like surface pit (arrowed); (b-g) Cross-section images each taken after 5 microns of milling, showing presence of cluster of voids and dislocations; (h) Plan-view image taken after completion of milling.

5.4 Summary

The morphology of GaN substrates grown by hydride vapor-phase epitaxy (HVPE) and by ammonothermal methods has been correlated with reverse-bias stress testing of GaN-on-GaN *p-i-n* devices. GaN substrates grown by HVPE showed ordered, well-separated arrays of surface features when observed using X-ray topography (XRT). All fabricated devices that overlapped with these features had typical reverse-bias voltages of less than 100V before reaching a leakage current limit that was set at 10^{-6} A. In contrast, devices not overlapping with such features had reverse-bias voltages of greater than 300V for a similar leakage current limit. After surface etching, the surfaces of the HVPE substrates showed evidence for defect clusters and macro-pits, whereas XRT images of the ammonothermal GaN substrate revealed no visible features. However, some devices fabricated on the ammonothermal substrate failed to reach equivalent reverse-bias voltages. Devices on HVPE and ammonothermal substrates with low breakdown voltages showed crater-like surface damage. Progressive ion-milling across such devices revealed the presence of threading dislocations penetrating deep into the substrate (~25 microns) and voids; these features were not observed in devices with high reverse-bias voltages and low leakage current. The results from this study should be of assistance in devising protocols to reliably fabricate high-power devices.

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CHAPTER 6

PLASMA-ENHANCED ATOMIC-LAYER-ETCHED GaN-ON-GaN DEVICES

This chapter describes an investigation of atomic-layer-etched (ALE) and regrown GaN-on-GaN vertical devices. The devices were grown by the group of Professor Yuji Zhao. The ALE processing and XPS measurements were performed by the group of Professor Robert Nemanich.

6.1 Introduction

The etching of mesa structures is commonly used to terminate or isolate high-voltage GaN devices to reduce low-voltage breakdown at junction edges. Etch termination techniques are well established for Si semiconductors, but suitable schemes are still under development for GaN devices [1-2]. Even though the density of threading defects (TDs) is reduced in epitaxial devices grown on bulk GaN substrates, dislocations caused by etch damage are liable to increase the severity of device breakdown effects and degrade device reliability [3]. TDs are known to act as trap states in GaN films and are considered as being responsible for locally high reverse leakage current due to the presence of metastable acceptor- and donor-like states in the vicinity of the defects [4-6]. The development of an improved *in situ* etching technique should help in the fabrication of complicated device structures, allowing selective-area doping with minimal etch damage.

6.2 Experimental Details

In these initial exploratory studies, devices designated here as A1, A2 and A3, were grown homo-epitaxially by metal-organic chemical vapor deposition (MOCVD) on 2-inch *c*-plane n^+ GaN substrates with a carrier concentration of ~10^{18} cm^{-2} and at a growth

temperature of ~1040°C. Approximately 4-5 microns of UID-GaN was grown on the device followed by plasma-enhanced atomic-layer-etching (PEALE) with a precise etch rate of 5 Å/cycle. This precise Ångstrom-scale etching was achieved by application of "super-cycles" that consisted of five alternating steps of hydrofluoric acid (HF) and trimethylaluminum (TMG) cleaning after each oxidation (via O_2 RF plasma) step. The removal rate and thickness measurements were conducted with an *in situ* multi-wavelength ellipsometer. The surface composition for all devices after etching was determined by *in situ* X-ray photoelectron spectroscopy (XPS). Hydrogen passivation was performed on two devices, A2 and A3, after PEALE to remove surface impurities and maintain Ga/N ratio. Mg-doped *p*-GaN layers with thicknesses in the range of 400-500 nm were grown on all samples. Details about device fabrication have been given in previous chapters. Samples suitable for cross-sectional TEM observation were prepared using the FEI Nova 200 dual-beam system, with initial thinning at 30 keV and final thinning at 5 keV. All scanning electron microscopy (SEM) images were taken on the Nova. A Philips-FEI CM-200 FEG TEM operated at 200 keV was used for imaging.

6.3 Results

The structure of all devices subjected to PEALE and regrown with *p*-GaN, is illustrated in Fig. 6.1. Figure 6.2 is an XPS plot of Device A1, which indicates the presence of oxygen. Plan-view SEM images were taken at different magnification to observe features of the regrown surface. Figure 6.2(b) is the low-magnification SEM image of Device A1 and shows a mostly uniform surface but with some irregularities in the form of dark spots. Figure 6.2(c) is a higher-magnification image of one of the dark spots shown circled in Fig. 6.2(b), and reveals what appears to be growth interruptions, roughly 10-

20μm in size, in the *p*-GaN region. Figure 6.2(d) is a higher-magnification image showing a more uniform area, as also circled in Fig. 6.2(b), revealing extensive patches of GaN apparently without complete coalescence.

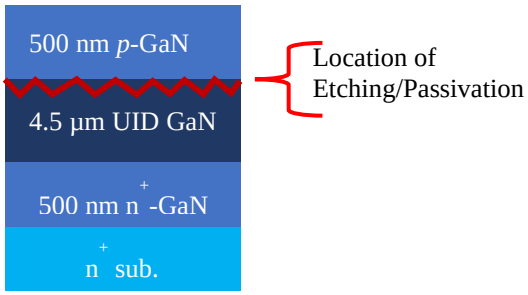

Figure 6.1. Schematic of device structure, also indicating location of etching and passivation treatment.

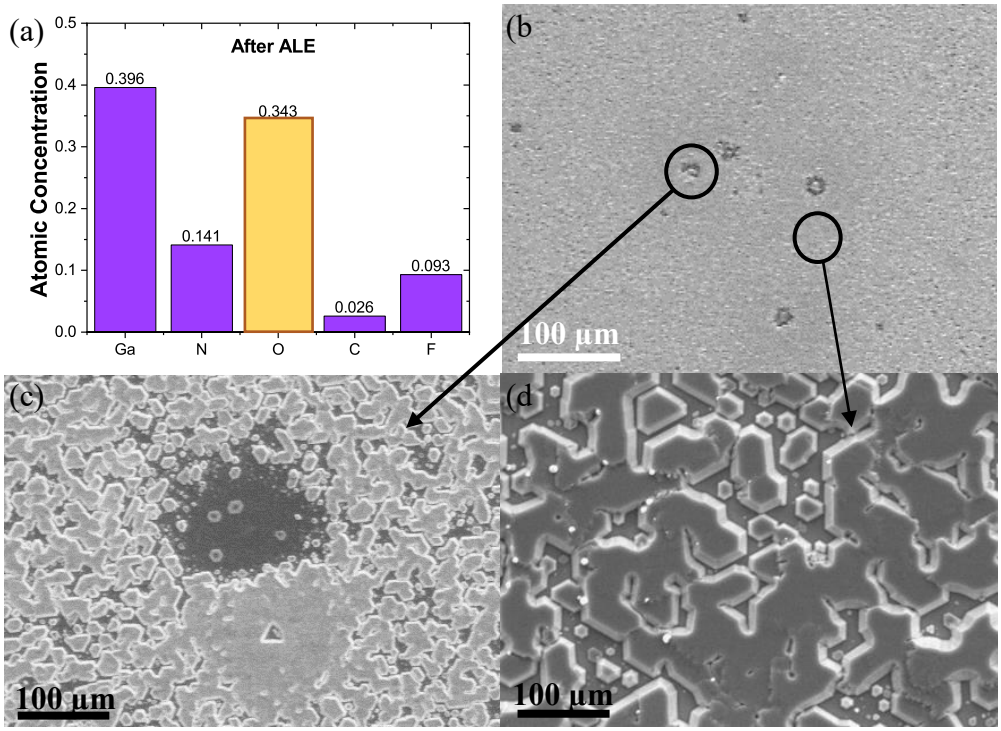

Figure 6.2. (a) *In situ* XPS plot showing elemental compositions after ALE etching (Courtesy of K. Hatch); (b) Low-magnification SEM image showing regrowth surface; (c) High-magnification SEM image showing growth interruptions at location marked in (b); and (d) High-magnification SEM image from location marked in (b).

Figure 6.3 shows a series of cross-sectional TEM images of the Device A1. The interface between *p*-GaN and UID-GaN interface can be clearly observed in Fig. 6.3(a). Figures 6.3(b)-6.3(f) are higher-magnification TEM images taken at the locations marked in Fig. 6.3(a). Figure 6.3(g) is a higher-resolution image taken at the interface region. Threading dislocations and dislocation loops are visible within the *p*-GaN. The presence of these defects within the *p*-GaN layer was not due to the innate quality of the UID-GaN or the substrate since no defects were observed in these regions. These results seem to show that the presence of oxygen at the surface before the *p*-GaN regrowth, as evident in Fig. 6.2(a), has most likely affected the material quality.

The Device A2 was subjected to 10 nm of PEALE followed by hydrogen (H_2) plasma cleaning, before *p*-GaN regrowth. Plasma cleaning removed surface oxygen contamination and provided the best Ga/N ratio possible for initiation of the regrowth. The XPS plot in Fig. 6.4(a) clearly shows surface oxidation after ALE but negligible oxygen after hydrogen passivation. Figure 6.4(b) is a plan-view SEM image taken at low magnification showing light area with dark circles. Figure 6.4(c) shows medium-magnification SEM image taken at location marked as 'A' in Fig. 6.4(b). The dark circle is ~ 400 μm in diameter with light and dark regions. Figures 6.4(d)-6.4(e) show images taken at dark and light regions in Fig. 6.4(c) (marked). The dark regions are interruptions in *p*-GaN growth with GaN islands clustered together, whereas the light areas are *p*-GaN with truncated hexagonal pits, Figure 6.4(f) shows the location of TEM lift-out.

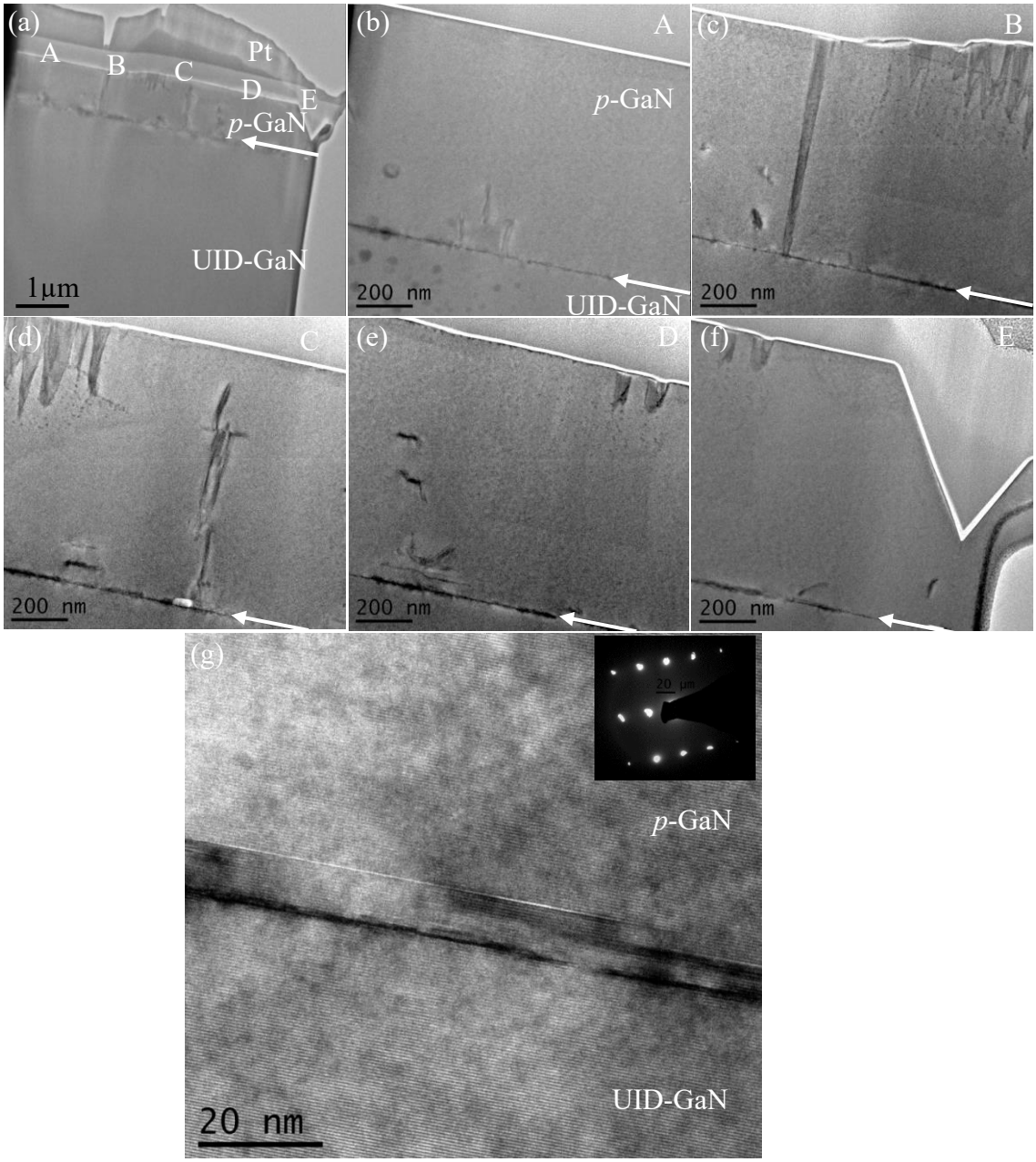

Figure 6.3. (a) Low-magnification TEM image showing *p*-GaN/UID-GaN interface (white arrow); Higher-magnification images showing defects within *p*-GaN and visible *p*-GaN/UID-GaN interface: (b) Location 'A', (c) Location 'B', (d) Location 'C', (e) Location 'D', (f) Location 'E'; and (g) High resolution TEM image showing *p*-GaN/UID-GaN interface region.

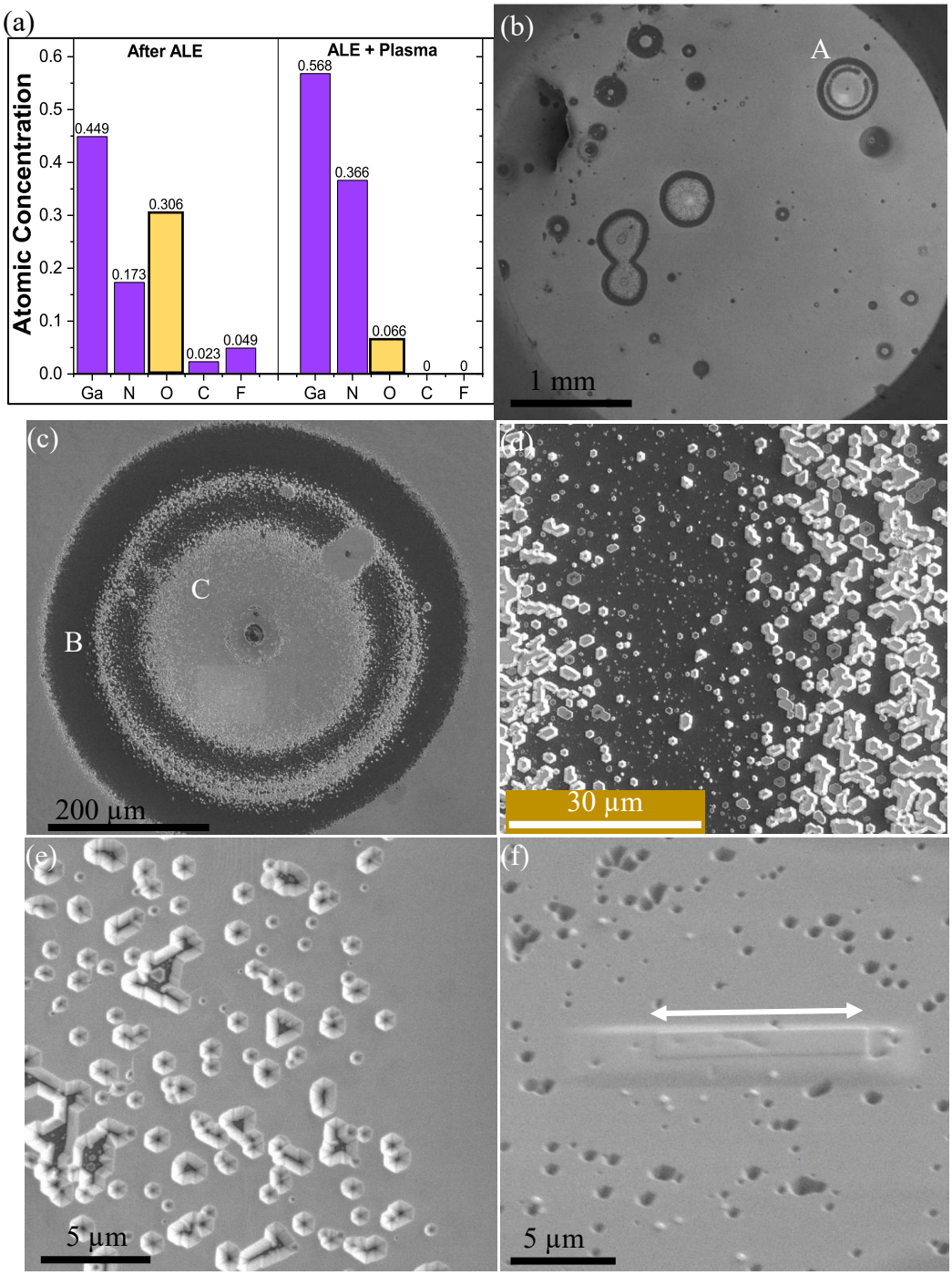

Figure 6.4. (a) *In situ* XPS plot (Courtesy of K. Hatch) after ALE (left) and after passivation treatment (right); (b) Low-magnification SEM image showing mostly uniform area but with dark circles; (c) Medium-magnification SEM image from location 'A'; (d) High-magnification SEM image from location 'B'; (e) High-magnification SEM image from location 'C'; and (f) High-magnification SEM image showing the location (arrowed) of TEM lift-out.

Figure 6.5 shows a series of cross-sectional TEM images of Device A2. Figure 6.5(a) shows a low-magnification TEM image, where the interface between *p*-GaN and UID-GaN (white arrow) can be clearly observed. Figures 6.5(b) and 6.5(c), from locations 'A' and 'B', respectively, show threading defects and dislocation loops within the *p*-GaN. Pits can be clearly observed along the *p*-GaN/UID-GaN interface indicating that the surface before the regrowth was not flat and clean. Figure 6.5(d) shows defects within the *p*-GaN layer. The high-resolution TEM image in Fig. 6.5(e) shows the presence of impurities and defects inside the UID-GaN near the interface. Figure 6.5(f) is a high-resolution TEM image indicating the presence of dislocation loops just below the interface. In comparison, the TD density deep inside the UID-GaN is much reduced.

Figures 6.6(a) and 6.6(b) are TEM images taken under 2-beam diffraction conditions at locations 'B' and 'C' in Fig. 6.5(a), respectively, showing dislocation loops near the interface region. Figures 6.6(c) and 6.6(d) are weak-beam dark-field (WBDF) images showing dislocation loops and defects near the interface region. Even though the oxidation at the interface was negligible after plasma cleaning, as observed by XPS, the image clearly shows presence of defects. These are attributed to hydrogen diffusion from the surface into the device during plasma cleaning. After plasma treatment, the devices were transferred to MOCVD chamber where the high growth temperature (≈1100°C) could have caused the hydrogen to diffuse into the UID-GaN, leading to defects during the regrowth.

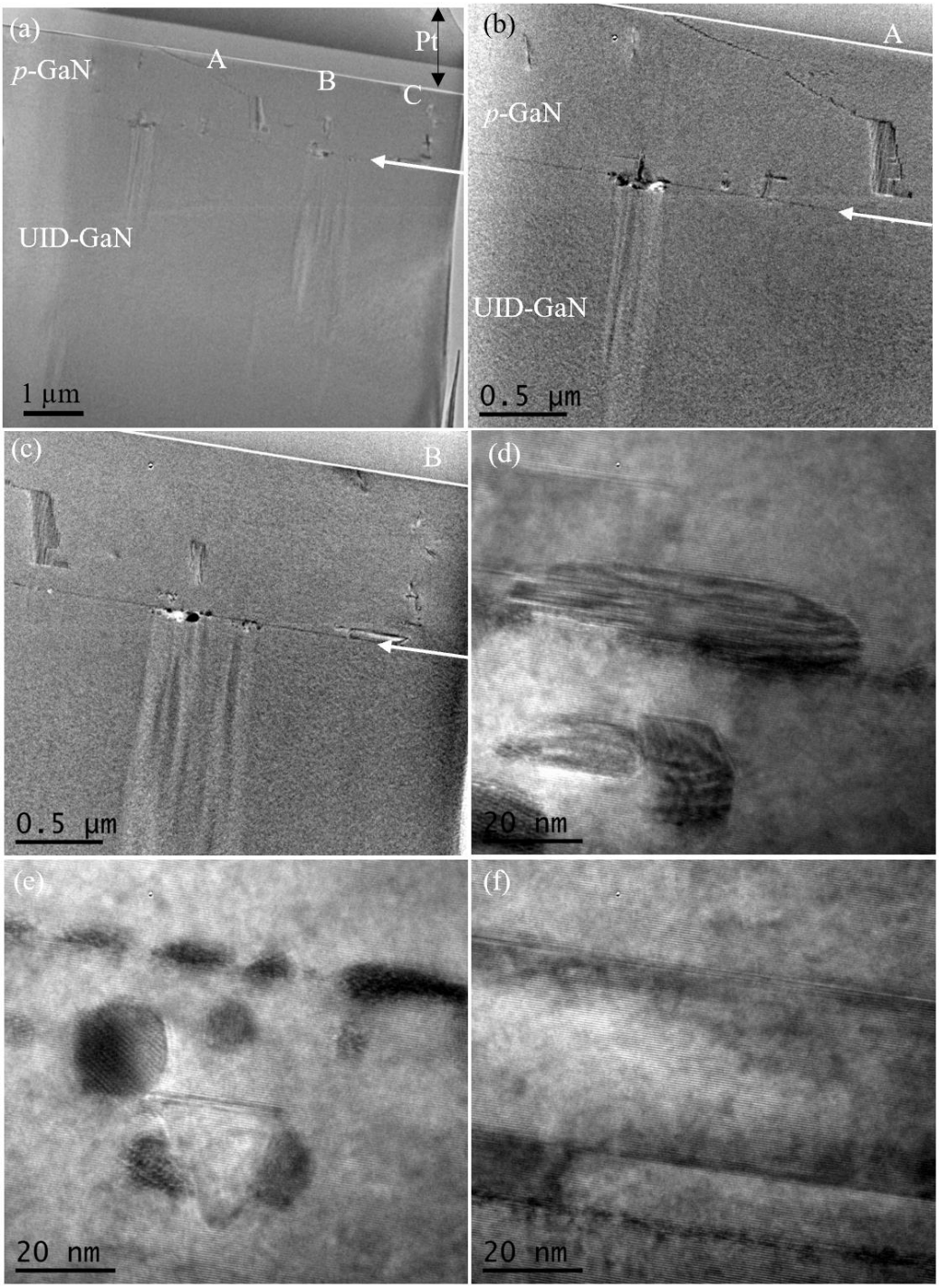

Figure 6.5. (a) Low-magnification TEM image showing *p*-GaN/UID-GaN interface (white arrow). High-magnification TEM images showing defects within *p*-GaN and UID-GaN taken: (b) Location 'A'; (c) Location 'B'; (d) High-resolution TEM image showing defects within *p*-GaN; (e) High-resolution TEM image showing 'V'-shaped defect within UID-GaN; and (f) High-resolution TEM image showing dislocation loop near top of UID-GaN layer.

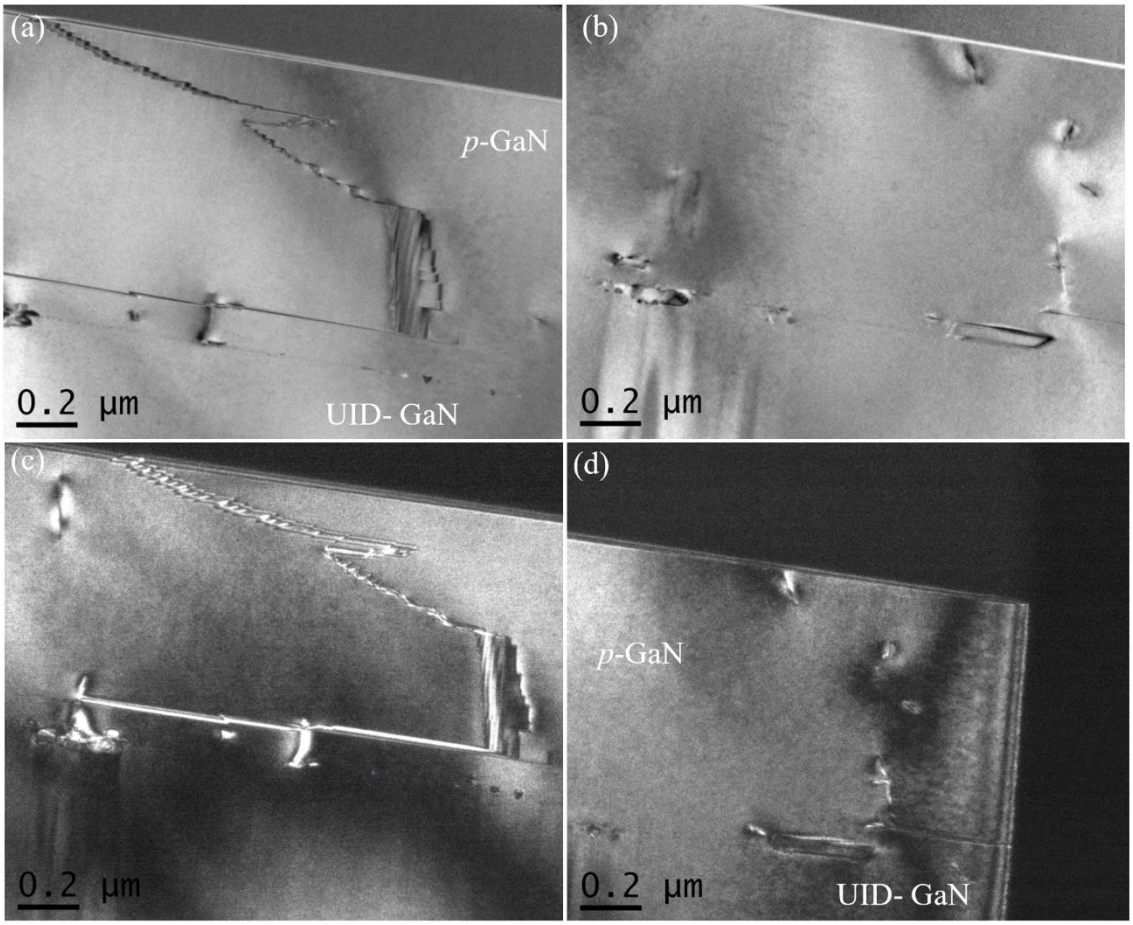

Figure 6.6. (a) Location 'B' in Fig. 6.5(a) under two-beam conditions; (b) Location 'C' in Fig. 6.5(a) under two-beam conditions; (c) WBDF image from location 'B'; and (d) WBDF image from location 'C'.

Device A3 was subjected to 20 nm of PEALE treatment, followed by hydrogen (H_2) plasma cleaning, before *p*-GaN regrowth. Figure 6.7(a) shows the XPS plot after passivation: the surface composition shows negligible oxygen. Figure 6.7(b) is a plan-view SEM image clearly showing GaN island growth. Figure 6.7(c) clearly shows small and large GaN islands without coalescence. Figure 6.7(d) is a TEM image taken from across one of the GaN islands, shown in Fig. 6.7(c) (white circle). The TEM image shows that the entire surface is riddled with defects as well as voids. Surface oxidation due to deep ALE

and hydrogen diffusion due to passivation resulted in lack of coalescence during regrowth and higher vertical growth than lateral growth, leading to tall *p*-GaN islands.

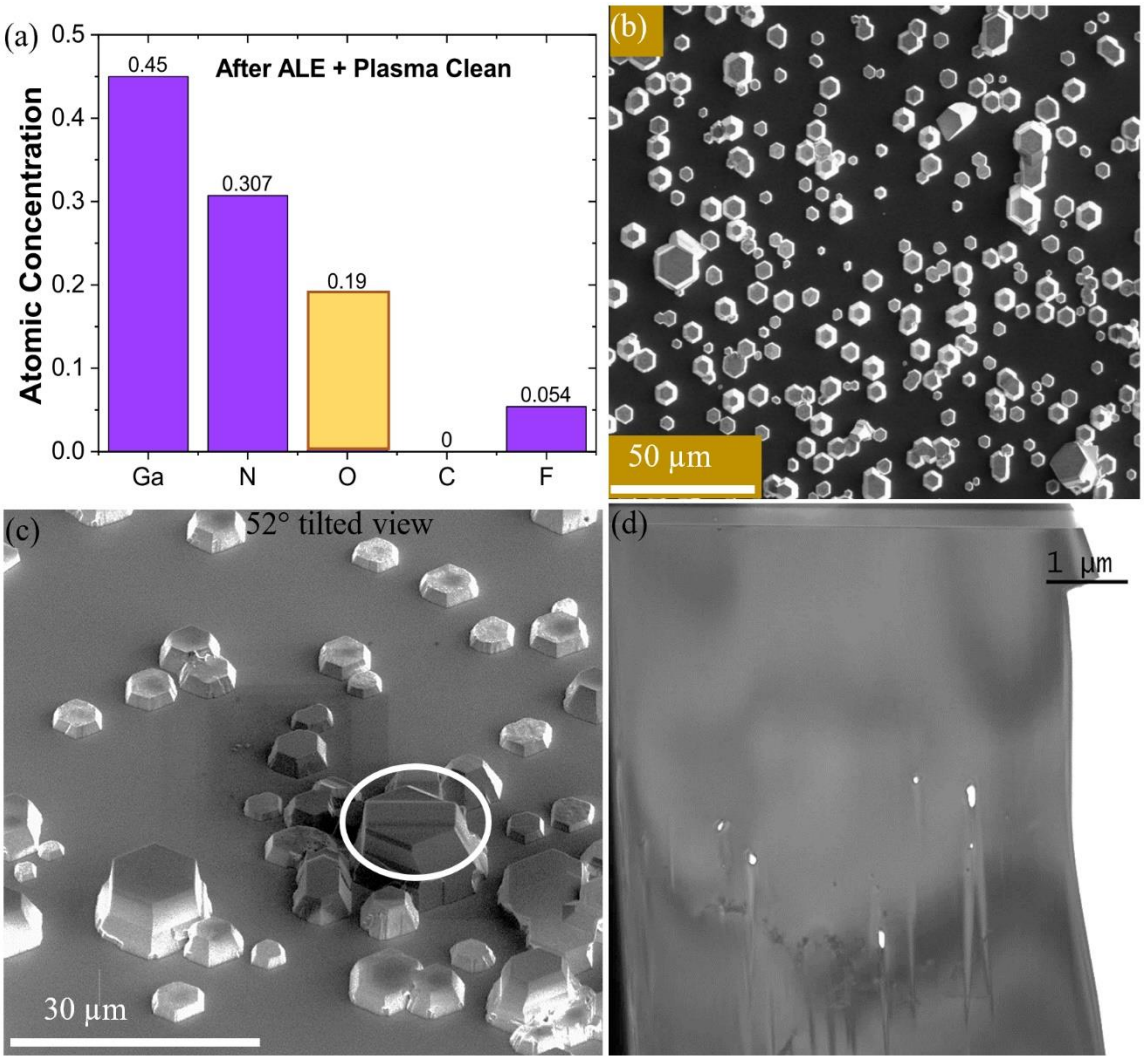

Figure 6.7. (a) *In situ* XPS plot for GaN surface after ALE and passivation; (b) SEM image showing hexagonal-shaped GaN islands; (c) SEM image showing small and large GaN islands; (d) Cross-sectional TEM image, taken at location circled in (c), showing defects deep inside the UID-GaN.

6.4 Discussion and Summary

The initial trials of *in situ* PEALE technique using oxidation and hydrogen plasma cleaning has resulted in unintended regrowth defects in GaN devices. The initial etching process caused surface oxidation before regrowth, which lead to irregularities in the *p*-GaN layer growth. The plan-view SEM images revealed incomplete GaN coalescence, and TEM images revealed a visible regrowth interface and the presence of defects within the *p*-GaN region. Hydrogen plasma passivation to remove oxidation post-etching was shown to be successful in terms of oxygen removal but had the unintended consequence of hydrogen diffusion into the base GaN layer, leading eventually to defects within *p*-GaN and UID-GaN layers. These caused incomplete GaN coalescence and lead to the formation of truncated hexagonal-shaped pits across the *p*-GaN. Some areas showed the presence of individual GaN islands of varying size.

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CHAPTER 7

FUTURE WORK

The research of this dissertation has involved an investigation of several of the more important materials issues and problems that are likely to impact the future reliability of GaN-based vertical power devices. Further studies from the materials perspective are still needed to understand the challenges of fabricating GaN-on-GaN devices and to establish protocols that eliminate, or at least minimize, device breakdown. These issues and some preliminary results are briefly presented and discussed in this chapter:

7.1 Factors Causing GaN-on-GaN Device Breakdown: Preliminary Results

In initial studies, two samples were grown homo-epitaxially by metal-organic chemical vapor deposition (MOCVD) on 2-inch *c*-plane HVPE-grown n^+ GaN substrates with carrier concentration of ~10^{18} cm^{-2} and growth temperature of ~1040°C. Approximately 20 microns of UID-GaN was grown on the two samples followed by growth of Mg-doped *p*-GaN layers with thicknesses in the range of 400-500 nm. Details about device fabrication have been given in previous chapters. Devices on one of the samples, designated here as Set B1, were hydrogen plasma treated for device edge termination at an ICP power of 300 W, an RF power of 10 W, and a pressure of 8 mTorr. The devices designated as Set B2 were mesa devices. Figures 7.1(a) and 7.1(b) are illustrations of these devices. The devices were thermally annealed at a temperature of 400°C to passivate the *p*-GaN layer. Samples suitable for cross-sectional TEM observation were prepared using a FEI Nova 200 dual-beam system, initial thinning at 30 keV and then final thinning at 5

keV. All scanning electron microscopy (SEM) images were taken on the Nova. A Philips-FEI CM-200 FEG TEM operated at 200 keV was used for imaging.

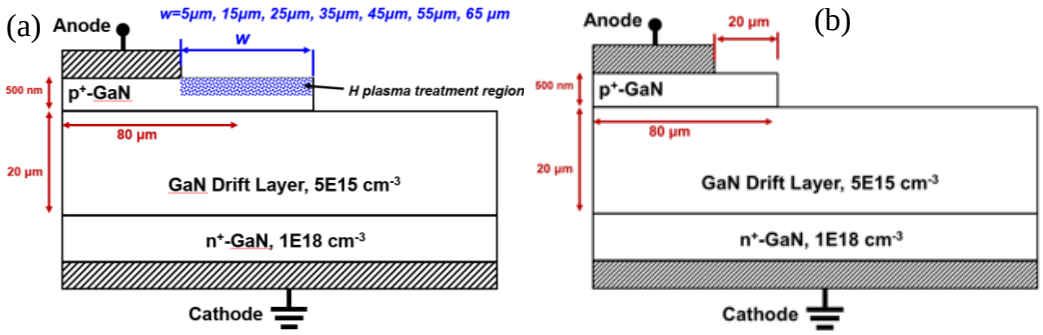

Figure 7.1. Illustration (not to scale) of devices: (a) B1, and (b) B2.

Figure 7.2 show plan-view SEM images of three different B1 devices, which had been reverse-bias stressed to typical breakdown voltages ranging from 1300V to 1650V. The device failures were marked by deep cracks, as observed previously, in some cases extending across the entire device. In order to better understand the possible reasons behind the device failure, the device shown in Fig. 7.2(b) was progressively milled in cross-section across part of the crack, and then imaged *in situ* after completion of each milling cycle. Figure 7.3(a) shows this device before commencement of trenching; the arrows indicate the location of the milled area. The series of images in Figs. 7.3 (b-h), each taken after roughly 5 microns had been progressively milled away, reveal a dense array of many threading dislocations extending deep (~ 45 microns) into the substrate. The crack itself was measured in this region to extend ~35 microns down from the surface which is well below the thickness of the UID-GaN layer, and it may have been even deeper in the central

region of the device. Finally, Fig. 7.3 (h) shows a plan-view image taken after completion of milling.

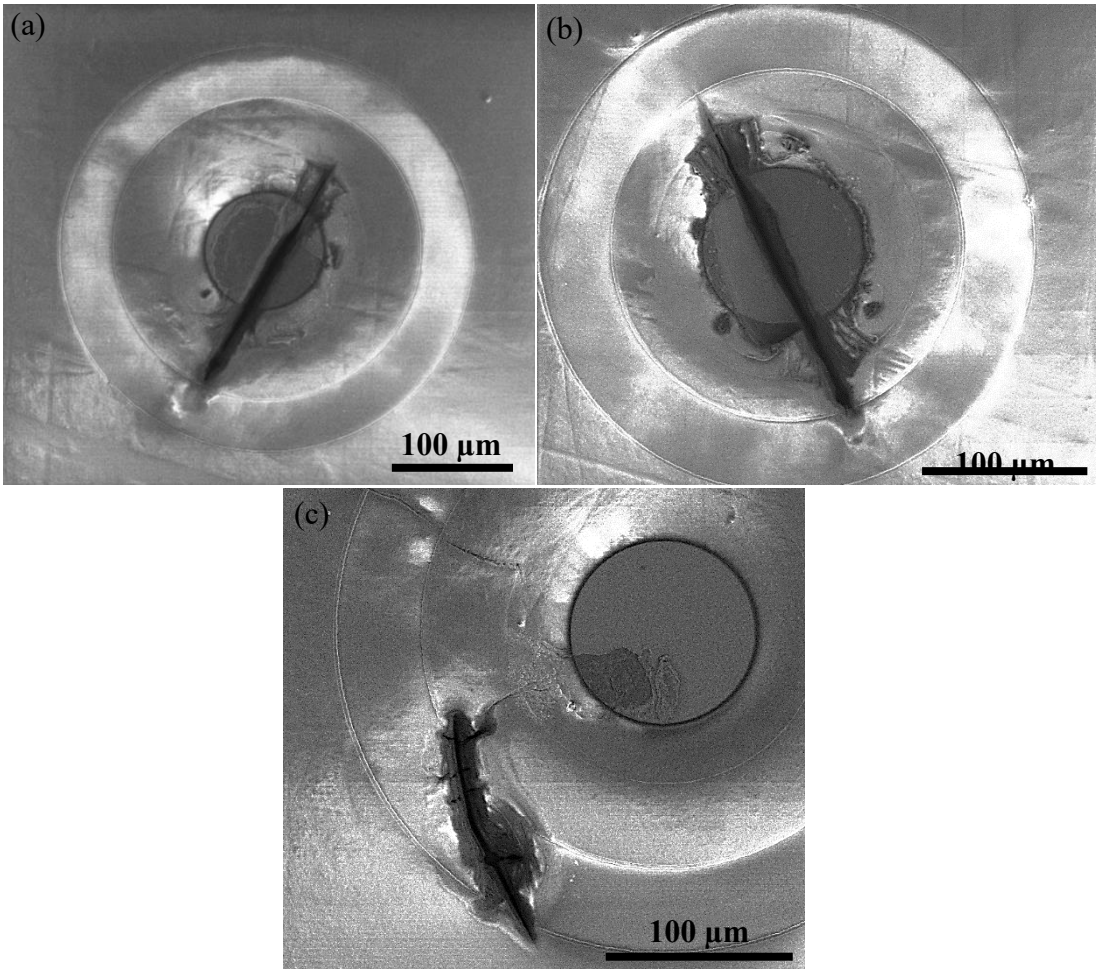

Figure 7.2. Plan-view SEM images of B1 devices.

Figure 7.4 shows a low-magnification SEM image of the B2 devices. Two types of irreversible failure, designated as Type I and Type II, were observed in these devices when reverse-bias stressed to breakdown at typical voltages ranging from 1800V to 2000V. Failed Type I devices are indicated by black circles in Fig. 7.4.and are differentiated by a large surface crack, sometimes extending across the entire failed device. The insert in Fig. 7.4 shows a representative XRT image of the wafer used for growth of these devices. This

image shows a two-dimensional array of features roughly equally spaced (~1 mm). It was already established, as shown in Chapter 5, that the substrate morphology played a critical role in the device behavior; since devices fabricated above these features had premature breakdown with visible surface damage such as “craters” and deep cracks. Thus, the Type I breakdown mode is clearly closely correlated with the substrate morphology.

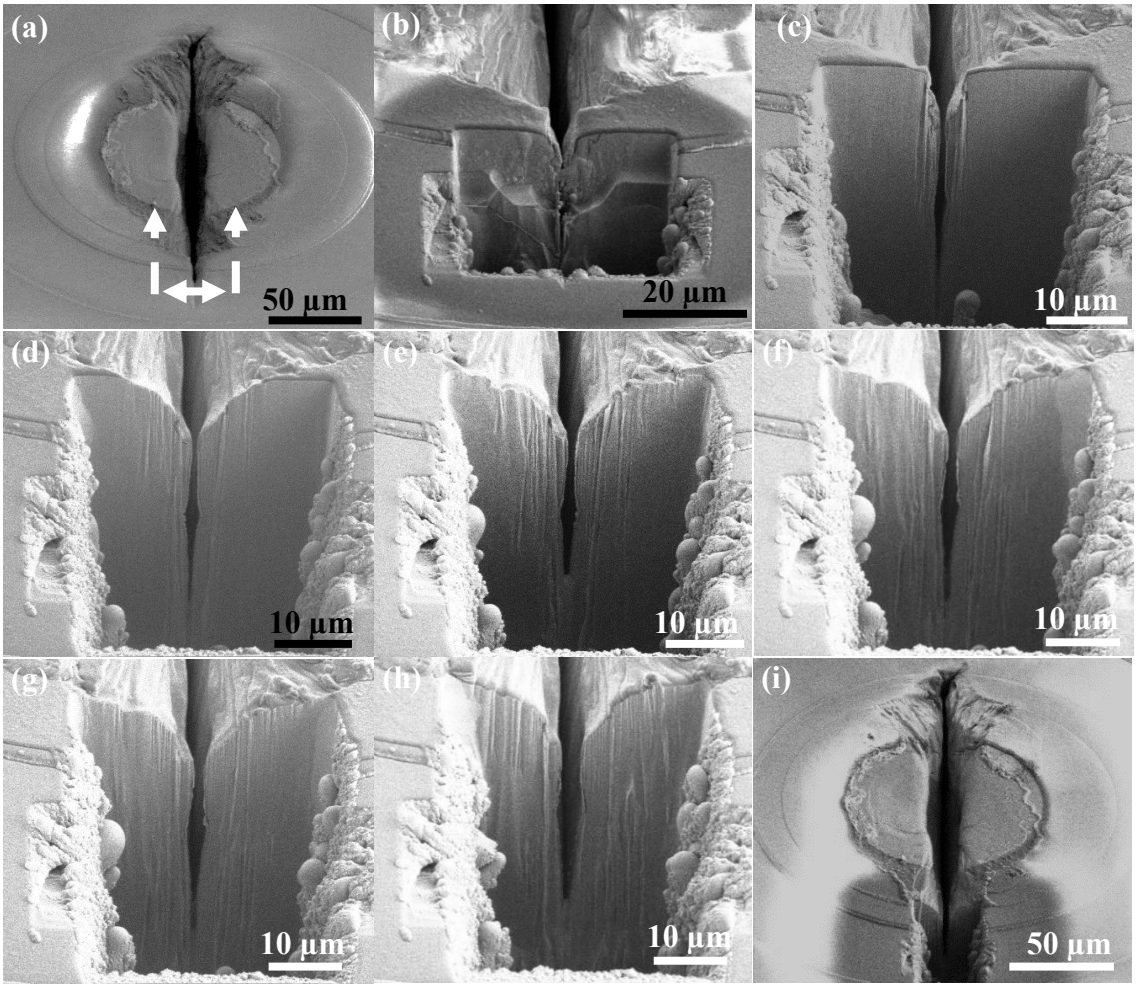

Figure 7.3. Series of SEM images of Device B1, showing progressive cross-sectional milling across part of the failed device: (a) SEM image showing a large crack across the device and the location where milling started (arrowed line); (b-h) Cross-section images each taken after 5 microns of milling, showing high density of TDs; (h) SEM image taken after completion of milling.

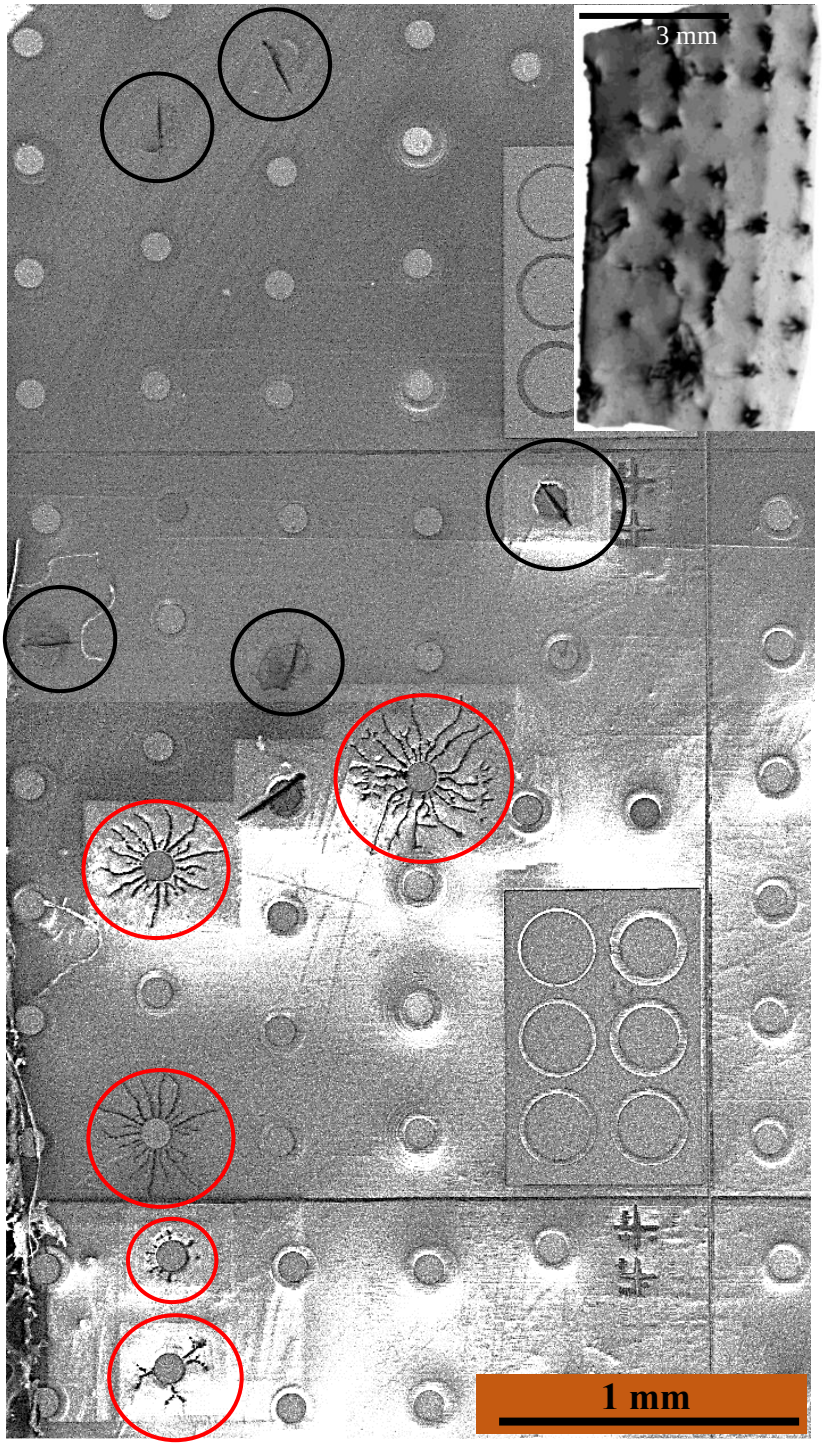

Figure 7.4. Low-magnification SEM image showing two types of breakdown when the B2 devices were reverse-bias stressed to failure: black circles indicate Type I breakdown and red circles indicate Type II breakdown. Insert shows XRT image with roughly equally spaced (~1mm) array of surface features.

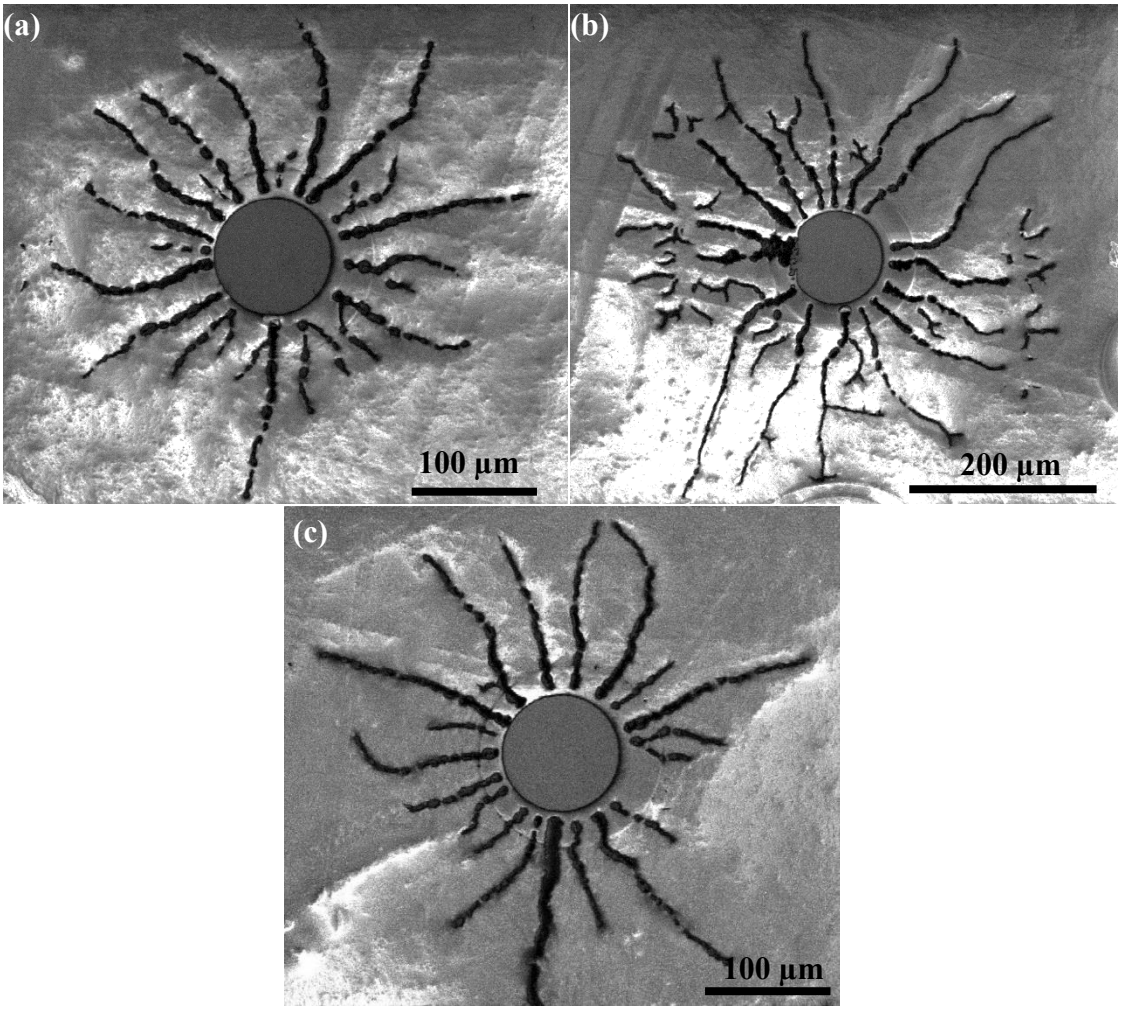

Figure 7.5. SEM images showing the Type II breakdown mode with cracks branching outwards rather than deep cracks and surface crater.

Failed Type II devices are indicated by red circles in Fig. 7.4. Figure 7.5 is a set of plan-view SEM images showing examples of Type II breakdown. This breakdown mode was differentiated by branching of surface cracks extending outwards from the device. In order to better understand this breakdown mode and nature of cracks, one of the devices was progressively milled in cross-section, and then imaged *in situ* with the SEM after each milling cycle. Figure 7.6(a) shows the device before commencement of milling: the milling

location is indicated by arrowed lines. Figures 7.6(b-d) are SEM images taken after another roughly 5 microns had been progressively milled away. The branching surface crack extends ~ 8 microns deep into the substrate and threading dislocations are again visible. Figures 7.6(e-f) show progressive milling of another crack, indicated by the circle in Fig. 7.6(b), which also shows the presence of threading dislocations and another crack (~ 5 microns deep).

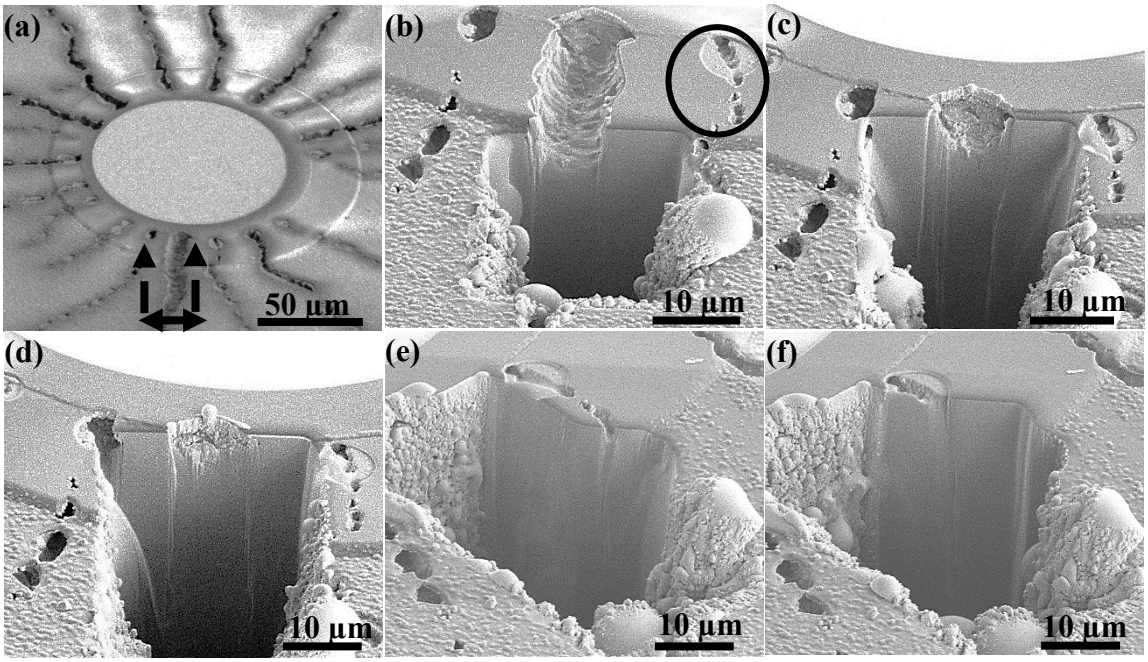

Figure 7.6. Series of SEM images of Type-II breakdown in Device B2, showing progressive cross-sectional milling across surface area: (a) SEM image, showing outwards branching cracks and location of milling marked by arrowed lines; (b-d) Cross-section images each taken after 5 microns of milling, showing presence of TDs and crack; (e-f) SEM images taken after milling of smaller crack circled in (b).

7.2 Outlook

Device breakdown under extreme reverse-bias conditions is clearly more complicated than originally thought. In some cases, large cracks develop that are correlated with underlying macroscopic defects in the HVPE-grown GaN substrate and these cracks extend well beyond the thickness of the UID-GaN layer. In other cases,

cracks extend radially outwards from the edges of the devices into the surrounding material, leaving the device itself apparently undamaged. Further work is required to understand the cause(s) of this Type II breakdown behavior from a materials perspective. Identifying the origins of these different types of breakdown should then assist in developing fabrication protocols that will ensure reliable performance in future generation of devices.

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