From Fully Depleted Silicon-on-insulator Towards Graphene-based Spintronic Applications

by

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ABSTRACT

In the last few decades, extensive research efforts have been focused on scaling down silicon-based complementary metal-oxide semiconductor (CMOS) technology to enable the continuation of Moore's law. State-of-art CMOS includes fully depleted silicon-on-insulator (FDSOI) field-effect-transistors (FETs) with ultra-thin silicon channels (6 nm), as well as other three-dimensional (3D) device architectures like Fin-FETs, nanosheet FETs, etc. Significant research efforts have characterized these technologies towards various applications, and at different conditions including a wide range of temperatures from room temperature (300 K) down to cryogenic temperatures. Theoretical efforts have studied ultrascaled devices using Landauer theory to further understand their transport properties and predict their performance in the quasi-ballistic regime.

Further scaling of CMOS devices requires the introduction of new semiconducting channel materials, as now established by the research community. Here, two-dimensional (2D) semiconductors have emerged as a promising candidate to replace silicon for next-generation ultrascaled CMOS devices. These emerging 2D semiconductors also have applications beyond CMOS, for example in novel memory, neuromorphic, and spintronic devices. Graphene is a promising candidate for spintronic devices due to its outstanding spin transport properties as evidenced by numerous studies in non-local lateral spin valve (LSV) geometries. The essential components of graphene-based LSV, such as graphene FETs, metal-graphene contacts, and tunneling barrier, were individually investigated as part of this doctoral dissertation.

In this work, several contributions were made to these CMOS and beyond CMOS technologies. This includes comprehensive characterization and modeling of FDSOI nanoscale FETs from room temperature down to cryogenic temperatures. Using Landauer theory for nanoscale transistors, FDSOI devices were analyzed and modeled under quasi-ballistic operation. This was extended towards a virtual-source modeling approach that accounts for temperature-dependent quasi-ballistic transport and back-gate biasing effects. Additionally, graphene devices with ultrathin high-k gate dielectrics were investigated towards FETs, non-volatile memory, and spintronic devices. New contributions were made relating to charge trapping effects and their impact on graphene device electrostatics (Dirac voltage shifts) and transport properties (impact on mobility and conductivity). This work also studied contact resistance and tunneling effects using transfer length method (TLM) graphene FET structures and magnetic tunneling junction (MTJ) towards graphene-based LSV.

DEDICATION

This dissertation is dedicated to my family and my partner who have supported and encouraged me continuously throughout my education.

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I am profoundly grateful for the support and encouragement I have received throughout my doctoral journey. Completing this dissertation would not have been possible without the unwavering support of numerous individuals who have played a pivotal role in shaping my academic and personal growth.

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This dissertation represents not only my individual efforts but also the collective influence of these remarkable individuals. I am honored to be a part of such a supportive network. Thank you for believing in me and helping me reach this significant milestone.

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INTRODUCTION

1.1 Background and Motivation

The undergoing development of modern Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) technology to follow Moore's law trends, as shown in Fig. 1, has resulted in critical length reaching dimensions of a few nanometers. Unlike long-channel transistors where transport mainly obeys drift-diffusion[1], transport in short-channel devices is now approaching the quasi-ballistic or ballistic regime, which indicates that carriers undergo few or negligible scattering while transporting across the channel. Thus, it's now essential for electrical engineers to reframe our understanding of charge transport in state-

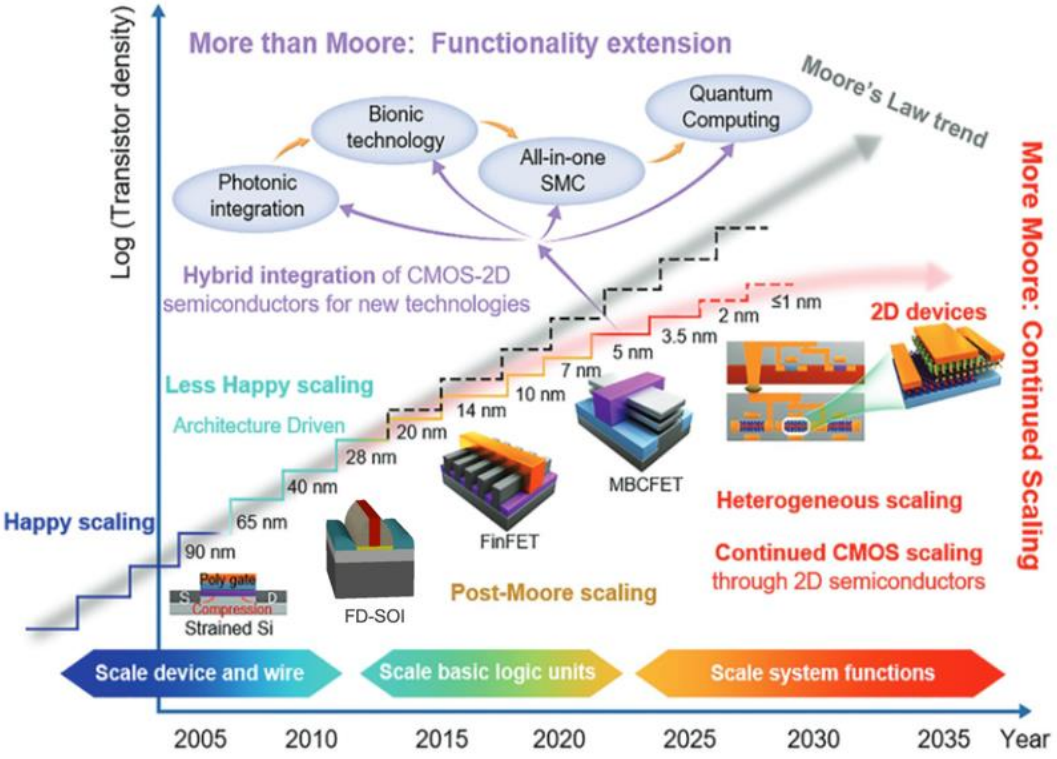

Fig. 1. Illustration shows the scaling trends of CMOS devices through the years that is getting hard to follow the Moore's Law

of-the-art nanoscale CMOS devices. This extends to applications where devices operate at cryogenic temperatures or under conditions that may result in charge-trapping effects to better understand their impact on device characteristics within this quasi-ballistic transport regime.

As shown in the Fig. 1, fully depleted silicon-on-insulator (FDSOI) is considered a state-of-art technology that was developed and scaled down to 22 nm CMOS nodes in recent years. FDSOI is suitable for applications that requires a balance between the power, performance, and cost because of its unique structure with a structurally isolated channel and its back-gate capabilities. Modern FDSOI with an ultra-thin silicon channel provides excellent electrostatic gate control, eliminating the need for significant doping in the channel region and mitigating variability due to random dopants as well as charged impurity scattering. Moreover, the isolation provided by the buried oxide (BOX) helps reduce the S/D capacitances and lowers source-to-drain leakage improving energy efficiency and performance of the transistor. Last but not the least, the threshold voltage of the FDSOI can be manipulated by applying a back-gate voltage under the BOX, which could enable the low power operation[2,3].

Significant research work has focused on FDSOI technologies with ultrathin silicon channels, including in both 28 nm and 22 nm CMOS nodes, towards cryogenic operation. For example, the temperature dependence of 28 nm FDSOI parameters down to cryogenic temperature was reported as well as the sensitivity of I-V characteristics to back-gate biasing by Becker *et al.*[4]. Moreover, the coupling between the front and the back gate was investigated down to cryogenic temperature for a 28 nm FDSOI[5]. The findings from these

studies suggested that mobility in short channel device is less sensitive to scattering effects at cryogenic temperature, which was attributed to quasi-ballistic transport. Even though these works provide good analysis on the cryogenic operation of FDSOI, the temperature dependence of quasi-ballistic transport in these short channel FDSOI has not been thoroughly studied. Thus, my PhD work studied nanoscale FDSOI MOSFETs, including the effects of back-gate biasing and channel length down to cryogenic temperatures. My research work then transitioned from ultra-thin FDSOI towards 2D material-based devices, individually focusing on the main components of graphene-based non-local LSV structures. Here, Landauer theory and similar models that were used on FDSOI were applied to analyze graphene-based 2D FETs.

An alternative to bulk semiconductors (e.g., silicon) as the main component of modern electronic technologies are emerging 2D materials such as transition metal dichalcogenides (TMD) and graphene. These materials have attracted many research interests in post-silicon era due to their unique electronic and transport properties. As shown in Fig. 2, TMD materials, such as MoS_2, can typically provide high ON/OFF ratios due to their moderate

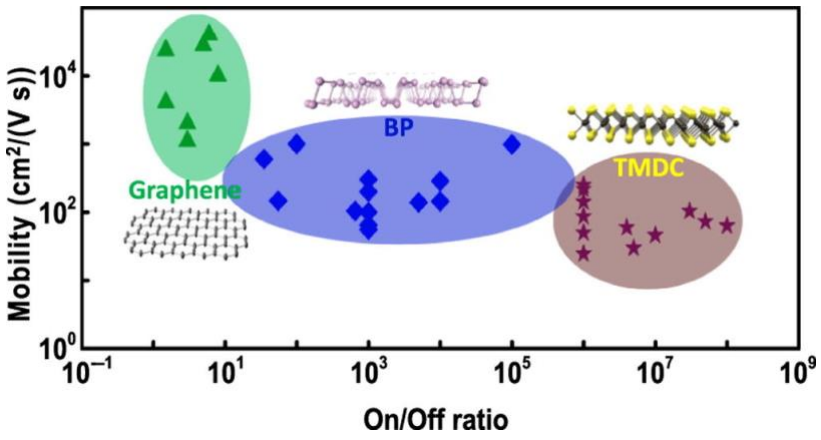

Fig. 2. Carrier mobility versus current on/off ratio reported for typical 2D materials electronics[6].

bandgap, which makes them suitable for CMOS logic devices. However, TMDs have relatively low mobility compared to the other 2D materials like black phosphorus (BP) as shown in the blue shaded region or compared to graphene as shown in green in Fig. 2[6].

While graphene is not a semiconductor since it has zero bandgap and it's not a material that can replace silicon as the channel material in CMOS logic devices, it still has many other applications. For example, graphene has been used for interconnects[7], biomedical application[8–11], and in flexible wearable electronic devices[12]. Moreover, graphene-based devices have demonstrated much higher speeds than traditional silicon-based devices, making them an attractive option for high-frequency applications such as RF communications[13,14]. Additionally, graphene is being explored for its potential use in memory and neuromorphic computing, a type of artificial intelligence that mimics the way the brain processes information[15–18]. These applications are all based on graphene's superior properties such as high mobility, as shown in Fig. 2, high thermal conductivity, high mechanical strength, low dimensionality. Graphene also exhibits long spin diffusion length, where spin information can travel over long distance without significant loss. Moreover, graphene also has a low spin-orbit coupling (SOC), which can maintain the spin coherence through a longer distance [19–21]. Thus, graphene has a great potential to work as a channel material in the spintronic devices, such as non-local lateral spin valve (LSV) [22].

LSV device consists of four contacts as shown in Fig. 3, where the two contacts on the two ends are nonmagnetic contacts and the two contacts in the middle are made with ferromagnetic metals, and there is a tunneling barrier underneath the ferromagnetic contacts.

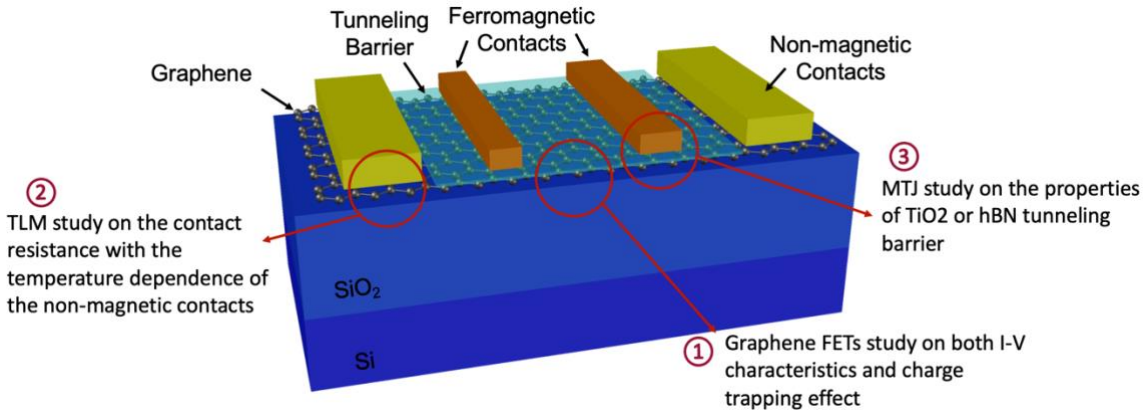

Fig. 3. The structure of the non-local lateral spin valve (LSV) consists of the components of graphene-FET, TLM, and MTJ structure, which were all investigated.

During the operation of the LSV device, the current carrying the spin signal would inject through one side of the non-magnetic and magnetic contacts pair, and the spin would accumulate at the interface of ferromagnetic contact. Then, the spin would diffuse laterally through the channel from the injector contacts pair in both directions. The non-local spin signal will reach the other non-magnetic and magnetic contacts pair and get detected and measured while applying an in-plane magnetic field along the y-direction. This four terminal LSV structure measurement would reduce the background noise signal from the charge currents because there is no net charge flow between two ferromagnetic contacts.

As illustrated in Fig. 3, the LSV consists of several key components/functions that are worth investigating and that make up a large part of this dissertation. These include the electrical properties and gate tunability in graphene FETs, the resistance of non-magnetic contacts on graphene, and the resistance of tunneling junction on graphene. Moreover, it is essential to better understand the transport properties of very thin layer two-dimensional materials that serve as the LSV channel by doing the electrical characterization. Here, due

to the atomic thinness of the graphene channel, its transport properties can be severely impacted by impurities near the channel. Consequently, charge trapping effect were investigated in this work to gain a better understanding on the impact of such impurities. Additionally, to gain better understanding on the resistance and the electrical properties of the contacts and tunneling barriers, which are very important to resolve conductivity mismatch issue in spintronics, graphene-based transfer length method (TLM) and the magnetic tunneling junction (MTJ) devices were investigated as part of this reserach.

CHAPTER 2

Cryogenic Characterization and Analysis of Nanoscale FDSOI FETs

2.1 FDSOI Technology

With the continued downscaling of CMOS technologies, the channel in modern metal-oxide-semiconductor field-effect-transistors (MOSFETs) is approaching a few nanometers in length. The channel length of the measured devices in this project ranges from 18 to 150 nm. Unlike long-channel devices, where transport can be described with a drift-diffusion formalism [1], modern short-channel devices require a different formalism that accounts for quasi-ballistic transport[23,24]. Thus, a quasi-ballistic model is necessary to analyze the transport properties of the nanoscale FDSOI MOSFETs studied in this work. For this purpose, I presented current voltage (I–V) measurements and analysis of FDSOI MOSFETs at various temperatures from 300 down to 10 K. Therefore, the purpose of this study is to establish the cryogenic transport properties of a modern nanoscale FDSOI CMOS technology, in the context of quasi-ballistic transport, given the growing interest of cryogenic nanoscale electronics for quantum computing applications [4,5,25–31]. Previous studies have explored temperature trends in the electrical characteristics of nanoscale MOSFETs, including a 28-nm FDSOI [4,5,26,27]and more recently a 22-nm FDSOI [28–30]. For example, Beckers et al. [4] reported the temperature dependence of MOSFET parameters down to cryogenic temperatures and the sensitivity of I–V characteristics to back-gate biasing in a 28-nm FDSOI. In Paz's work[5], the coupling between front and back gates is explored down to 4.2 K for a 28-nm FDSOI. There, mobility was characterized for long and short channel devices, and short channel devices were less sensitive to temperature.

That result was attributed to quasi-ballistic transport, but no analysis of quasi-ballistic transport was presented. Recently, threshold voltage, ON-state current, transconductance, and low-frequency noise parameters [28], as well as RF parameters[29] were studied in a 22-nm FDSOI as a function of temperature. While these studies provide a good description for cryogenic operation in FDSOI, the temperature-dependence of quasi-ballistic transport characteristics in nanoscale FDSOI MOSFETs has not been thoroughly studied.

This work presents new measurements and analysis of nanoscale FDSOI MOSFET electrical characteristics, including the effects of back-gate biasing and channel length over a wide range of temperatures from 300 down to 10 K. Based on transport theory of nanoscale transistors[23,24], I analyze their quasi-ballistic transport behavior as a function of temperature. The analysis of quasi-ballistic operation includes the effects of back-gate biasing, series resistance, and channel length. I observed that quasi-ballistic operation persists at cryogenic temperatures for FDSOI MOSFETs, where bulk devices show a more significant reduction in ballistic ratio. This is attributed in part to a smaller contribution from ionized impurity scattering at low temperatures in FDSOI devices due to lower doping in the channel compared to bulk.

Moreover, this work presents a virtual source (VS) compatible charge model that accounts for quasi-ballistic transport, back-gate biasing, and temperature. The model is experimentally validated against measured I-V characteristics using extracted parameters for mobility, series resistance, and threshold voltage. The model calculations are in good agreement with experimental I-V characteristics for all temperatures ranging from 300 to 10 K including the effect of back-gate bias.

2.2 Device Parameters and Measurement Setups

The N-MOSFET that characterized and measured in the study is the commercial 22 nm Fully Depleted SOI fabricated by GlobalFoundries. Two types of transistors were measured, which are enhanced gates (EG) with thicker gate oxide, and standard gate (SG) with thinner gate oxide. The schematic of the transistor and the typical cross-section views of the transistors are shown in Fig. 4 (a) and (b), where the channel length of these devices range from 18 to 150 nm, and the channel width are all 1 μm. The thickness of buried oxide is 20 nm with a 6 nm thick Silicon channel[25].

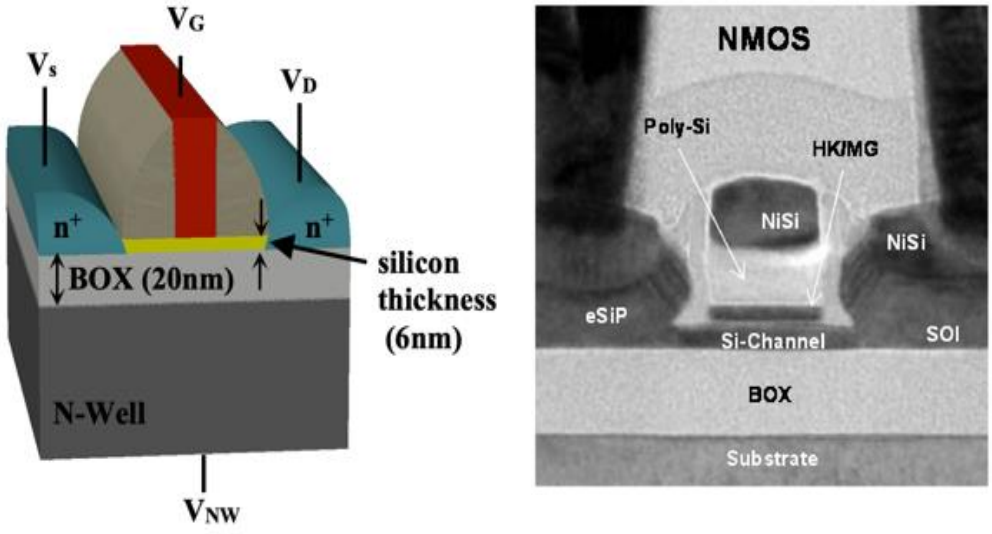

Fig. 4. (a). Schematic of the NMOS Flip Well with enhanced gate device SLVT-N. (b). Typical cross-section view of NMOS and PMOS ©[2016] IEEE[25]

Transfer characteristics were measured for the devices with different channel length for both types of transistors (EG: L = 60, 70, 80, 90, 100, 120, and 150 nm; SG: L = 18, 20, 22, 24, 28, 32, and 40 nm) by sweeping the gate voltage (V_g) from -0.2 V to 1 V for the temperature from 10 K to 300 K (10, 40, 70, 150, 240, 300 K) with low drain voltage (V_{ds}) set to 0.1 V, and back gate voltage (V_{bg}) was set to five different levels (-2, -1, 0, 1, 2 V) .

Low V_{ds} was used in the measurement so that the self-heating is negligible due to the low operating power.

2.3 Measurement Data and Analysis

Fig. 5a shows the results for the transfer characteristics for the EG transistor with 90 nm channel length with the back gate voltage V_{bg} = 0 V. The y-axis (I_d) in the plot is in logarithmic scale so that it can reveal the temperature dependence of the subthreshold region more clearly. From 300 K to 10 K, the threshold voltages are increased, and the subthreshold slope (SS) are improved for both short and long channel FETs, which is due to the intrinsic temperature dependence of the current[32]. Fig. 5b is showing an I_d-V_g curves plotted in linear scale with a transconductance calculated by $g_m = \partial I_d/\partial V_g$. In the linear scale, the on-state current in strong inversion operation are easier to observe the temperature dependence, which higher on-current was observed at lower temperature. The transconductance is related to mobility, and Fig. 5b is showing that the transconductance

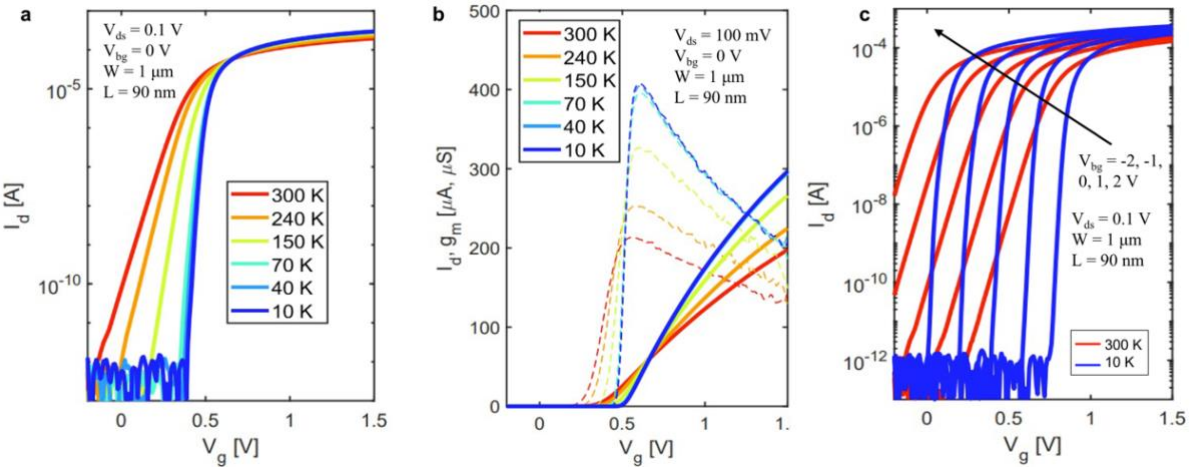

Fig. 5. (a) Measured drain current (I_d) versus gate voltage (V_g) for different temperatures and V_d = 0.1 V for EG FDSOI MOSFET. (b) Measured I_d (solid line) and transconductance (g_m) (dashed line) versus V_g. (c) I_d–V_g characteristics measured at 300 and 10 K with different back-gate voltage (V_{bg}).

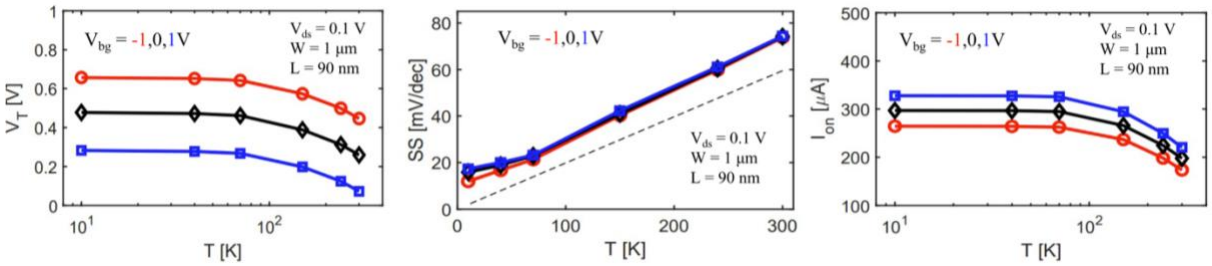

Fig. 6. (a) Extracted threshold voltage (V_T) versus temperature (T). (b) Extracted SS versus temperature. (c) Extracted ON-state current (I_{ON}) versus temperature. The extractions of V_T, SS, and I_{ON} are shown for $V_{bg} = -1$, 0, and 1 V.

peak is improving while temperature decreasing. Fig. 5c plotted the I_d-V_g curves at 10 K and 300 K for the same device, but with different levels of back-gate bias varied from -2 to 2 V with 1 V increment. It's evident that the back-gate bias is having a significant impact on the I_d-V_g characteristics, and it induced a large threshold voltage (V_T) shifting towards a negative direction, which is corresponding to a reduction in V_T.

The threshold voltage (V_T) was extracted from the I_d-V_g curves at three levels of back-gate bias with a fixed value of normalized drain current, where I_d/W = 0.3 $\mu A/\mu m$, and plotted in Fig. 6a. The change of V_T induced different back-gate bias was similar across different temperature levels. While the temperature dropped below 50 K, the V_T varies linearly with temperature with a small plateau. The threshold voltage (V_T) is increasing with lowering temperature is due to the carrier freeze out, where the electrons are confined in donors at a lower temperature. Then, the Subthreshold swing (SS) was extracted and plotted in Fig. 6b. SS is getting lower while having temperature decreasing, and the values were all remained slightly higher than the fundamental limits (~60 mV/dec at 300 K) for all temperature levels. In Fig. 6c, the on-current, which was extracted at V_g = 1.5 V, was

plotted for three back-gate bias. Since the effect of back-gate bias is negligible on *SS*, the impact on the on-current can be traced back to the shifts in threshold.

To better understand the low-filed carrier transport and the resistance, I started with the drain current I_d expression given by

$$I_D = \frac{W}{L}\mu_{app}C_{inv}(V_G - V_T)V_{DS} \tag{1}$$

C_{inv} is the gate capacitance in strong inversion, which is approximately equal to the oxide capacitance C_{ox}. μ_{app} is apparent mobility, which is combined by effective mobility (μ_{eff}) and ballistic mobility (μ_{ball}) with Matthiessen's rule[33] as

$$\frac{1}{\mu_{app}} = \frac{1}{\mu_{eff}} + \frac{1}{\mu_{ball}} \tag{2}$$

where $\mu_{eff} = \frac{\lambda_0 v_T}{2K_BT/q}$ and $\mu_{ball} = \frac{Lv_T}{2K_BT/q}$. The ballistic mobility (μ_{ball}) is dependent on the channel length, and effective mobility (μ_{eff}) is not. Both mobility components are dependent on the temperature. λ in the formula is the mean-free path, and the unidirectional thermal velocity is $v_T = \sqrt{2k_BT/\pi m^*}$, where m^* represents the effective mass.

To eliminate the effect of series resistance (R_{SD}), V_{DS} in (1) is divided with I_D and combined with (2) to obtain the total resistance:

$$R_{TOT} = \frac{L}{W\mu_{eff}C_{inv}(V_g - V_t)} + \frac{2K_BT/q}{Wv_TC_{inv}(V_g - V_t)} + R_{SD} \tag{3}$$

This expression contains three components, where the first part of the right-hand side in (3) is effective resistance (R_{eff}), which is dependent with channel length *L*, and the second part is ballistic resistance (R_{ball}), where the channel length *L* was canceled out, and the last term is the source/drain series resistance (R_{sd}). The R_{TOT} calculated from the measured data

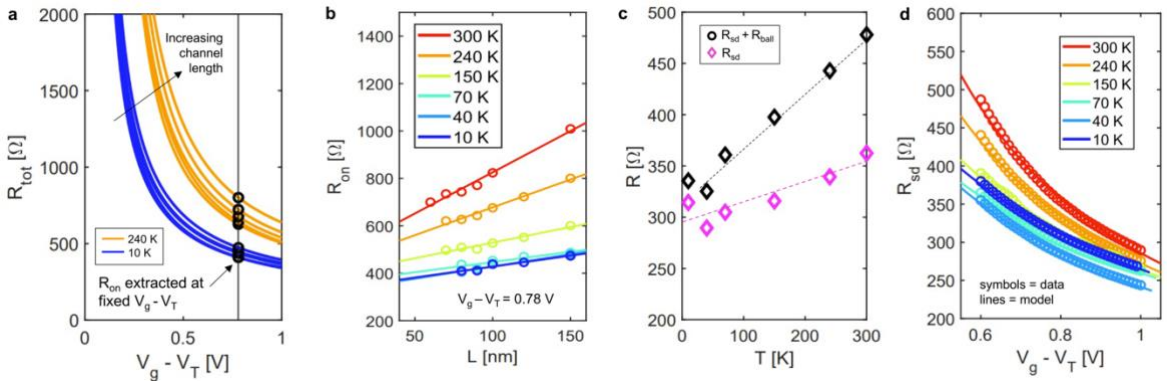

Fig. 7. (a) Total resistance (R_{TOT}) versus gate overdrive (i.e., $V_g - V_T$) for various channel lengths at 240 and 10 K. (b) ON-resistance ($R_{ON} = R_{TOT}$ at $V_g - V_T = 0.78$ V) versus channel length at various temperatures. (c) Extracted series resistance (R_{SD}) with and without contribution from channel ballistic resistance (R_{ball}) as a function of temperature. (d) Experimentally extracted R_{SD} (circles) versus $V_g - V_T$ at various temperatures and model fits (solid lines).

for the EG transistor for different temperature levels across various channel length are plotted in Fig. 7a. Then, the on-resistance (R_{ON}) can be extracted at a fixed $V_g - V_T = 0.78$ V and plotted in Fig. 7b as a function of channel length L for various temperatures from 10 K to 300 K. As shown in (3), the only term that is channel length dependent is R_{eff}, so that I can extrapolate the R_{ON} data to L=0 and obtain $R_{ball} + R_{sd}$, which is then plotted in Fig. 7c.

Furthermore, I calculated the R_{ball} for each temperature level and subtract it from $R_{ball} + R_{sd}$ to isolate the series resistance R_{sd}, which is plotted in Fig. 7c with pink diamonds. It's evident that the R_{sd} is improved with reduced temperature, which is consistent with previous work[29]. Fig. 7d plots R_{sd} as a function of $V_g - V_T$ at various temperature levels to investigate the gate voltage dependency of R_{sd}. The symbols are the measured data, and the solid lines were the empirical model given by $R_{sd}(V_g) = R_{sd0}/[1 + \alpha(V_g - V_T) + R_{ext}]$[34,35].

While μ_{ball} can be calculated for each temperature level as a function of channel length, effective mobility μ_{eff} can be extracted for each temperature as the slope of R_{ON} as a function of L from Fig. 7b based on (3). As shown in Fig. 8. a and b, which are the apparent mobility μ_{app} as a function of channel length L for EG (from 60 up to 150 nm) devices and SG (from 18 up to 40 nm) devices across various temperatures, the dashed lines are the μ_{eff} and μ_{ball}, where μ_{eff} is a constant throughout the different channel length. The solid line is the modeled μ_{app} obtained from (2), where it fits well to the extracted μ_{app}. As shown in both plots, the experimental μ_{app} are mainly distributed in the transient quasi-ballistic region. By comparing Fig. 8a and Fig. 8b, the SG devices with shorter channel length are further into the quasi-ballistic region towards left, while the EG devices with a longer channel length are only slightly into the quasi-ballistic region. Moreover, both EG and SG devices are showing an increase in μ_{app} while decreasing the temperature.

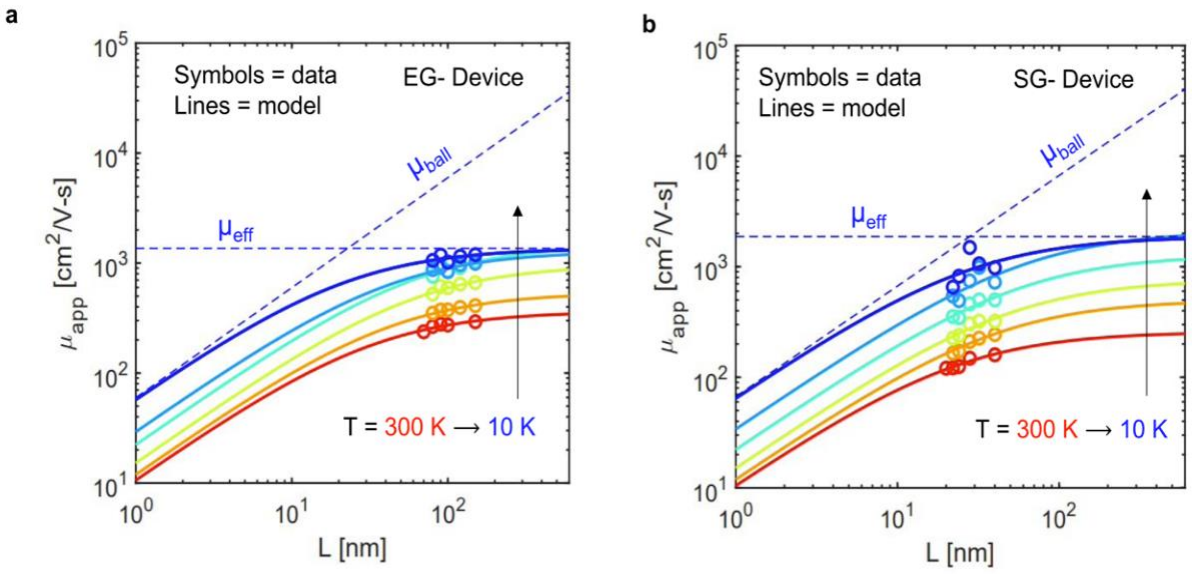

Fig. 8. Experimentally extracted (circles) and model calculations (lines) of apparent mobility (μ_{app}) versus channel length (L) for different temperatures for (a) EG FDSOI MOSFETs and (b) SG FDSOI. Dashed lines are the model based on 10 K.

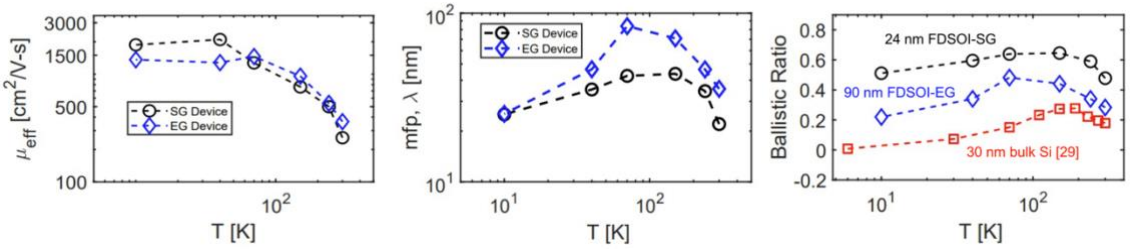

Fig. 9. (a) Extractions of effective mobility (μ_{eff}) versus temperature for both SG and EG devices. (b) Extracted mean free path (λ) versus temperature for both SG and EG devices. (c) Ballistic ratio versus temperature for SG L = 24 nm FDSOI (black circles), EG L = 90 nm FDSOI (diamonds), and bulk Si MOSFET L = 30 nm (squares).

Then, I investigated the temperature dependence of the effective mobility μ_{eff}, which is plotted in Fig. 9a for both EG (L = 90 nm) and SG (L = 24 nm) devices. As the results shown, both devices are having the effective mobility μ_{eff} initially increase significantly with reducing the temperature down to around 100 K, which is largely contributed by the reduction of phonon scattering[23]. While the temperature dropped down below 100K, this reduction of phonon scattering becomes less significant, and ionized impurity scattering may start having impact on the carrier transport. To further investigate the scattering mechanism, the experimental mean free path (λ) was extracted for both EG and SG devices from μ_{eff} and plotted in Fig. 9b. For the temperature dropping from 300 K to 100 K, λ is showing the same increasing trends as μ_{eff}, which is indicating the reduction of phonon scattering. While temperature reducing from 100 K to 10 K, λ decreases due to more significant impact from ionized impurity scattering.

The ballistic ratio was also investigated by calculating $\lambda/(\lambda + L)$ for both EG and SG devices and plotted in Fig. 9c. The ballistic ratio is ranged from 0 to 1, where 0 stand for $L \gg \lambda$ and corresponds to significant scattering in the channel, and 1 stand for $\lambda \gg L$ and

it indicates ballistic transport[36]. Because SG device has shorter channel length (L = 24 nm) compared to EG device (L = 90 nm), the ballistic ratio is larger as shown in Fig. 9c. The temperature dependence of the ballistic ratio is showing the same trends as μ_{eff} while temperature dropping from 300 K to 100 K, where the phonon scattering is dominated and become less significant with temperature reducing. Ionized impurity scattering start becoming dominated when temperature is below 100 K, which leads to a reduction in the ballistic ratio. The ballistic ratio for a bulk silicon device[35] is also plotted and compared to the devices in this project. In the bulk Si device, the ballistic ratio drops significantly to 0 at low temperature T = 10 K, and this indicating that the ionized impurity scattering in the FDSOI is less severe at a low temperature compared to the bulk Si device. Moreover, unlike the FDSOI devices, where the peak of ballistic ratio appears around 100 K, the peak of bulk Si devices appears around 200 K, which is an indication of a more severe ionized impurity scattering. This is because the lower doping in the ultrathin channels in the FDSOI MOSFETs compared to the high doping in the channel of the bulk Si devices provided by halo implants.

2.4 Landauer-based Model

Virtual Source (VS) model was in to fit for FDSOI MOSFETs from room temperature to cryogenic temperatures. Drain current is given by

$$I = \frac{W}{L}\mu_{app}Q_{inv}(V_{ds} - \mathrm{I}_d\mathrm{R}_{sd}) \tag{4}$$

This formula is like (1) with the effect of source-drain series resistance. To better modeling the effects of back-gate bias (V_{bg}) in the devices, I extend the empirical expression for the inverse charge density Q_{inv} to include V_{bg}:

$$Q_{inv} = \phi_t C_{inv} m\, ln(1 + e^{\frac{V_g - (V_{T0} - \alpha V_{bg} - \delta V_{ds})}{m\phi_t}}) \quad (5)$$

In (5), α, δ, and ϕ_t are all fitting parameters that is related to the effects of back-gate biasing V_{bg} and the drain-source voltage on the threshold voltage V_T. By combining (4) and (5), the drain current I_d can be calculated as a function of gate bias V_g. Thus, I can calculate the model for the EG device with L = 90 nm at V_{ds} = 0.1 V and V_{bg} = -2, -1, 0, 1, and 2 V, and plotted the results along with the experimental data in Fig. 10 (a)-(f). The good fitting between the model and the experimental data in both weak and strong inversion region was shown for all the temperatures. There is a small discrepancy at a higher V_g region and it's

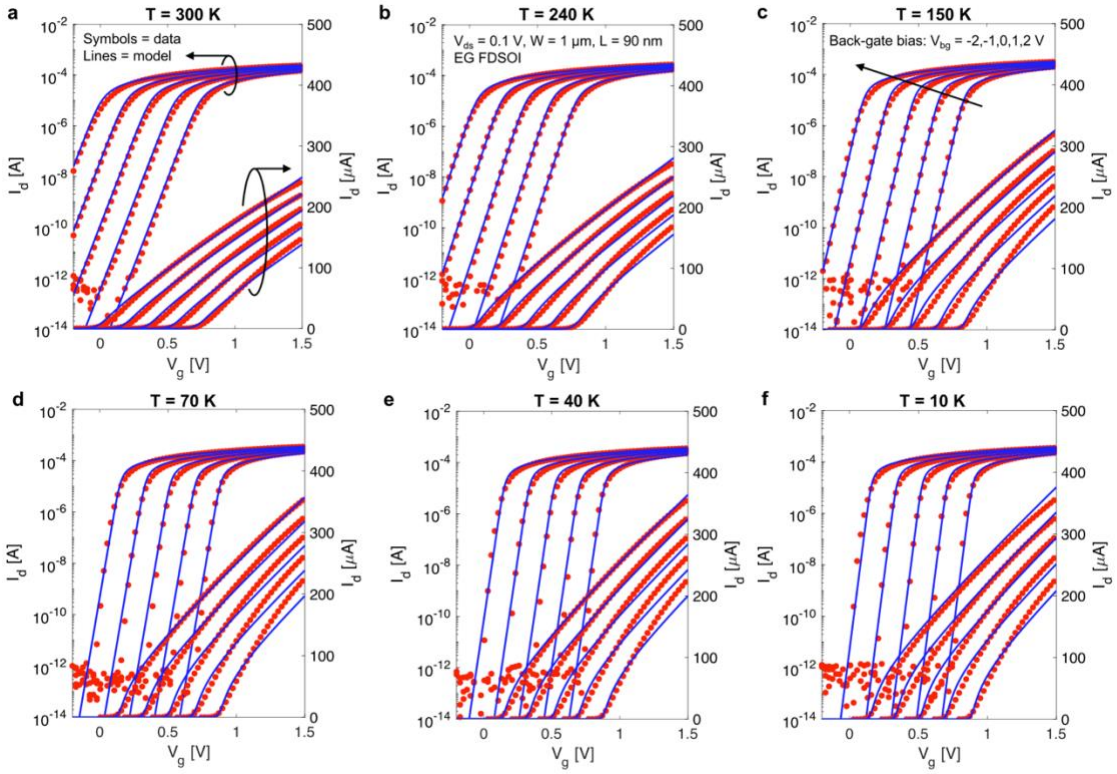

Fig. 10. Measured Id–Vg characteristics (red dots) in logarithm and linear scale and compared against model calculations (solid lines) for EGFD - SOI n-channel MOSFET with L = 90 nm, W = 1 µm. The experimental data and model fits are shown for five different back-gate voltages and for the following temperatures: (a) T = 300 K; (b) T = 240 K; (c) T = 150 K; (d) T = 70 K; (e) T = 40 K; and (f) T = 10 K.

more likely due to the lack of gate-voltage dependency for effective mobility in the model. And the larger discrepancies at a lower temperature indicating that the dominant scattering mechanisms, such as surface roughness, is having a larger gate-voltage dependence compared to the dominant scattering mechanisms at a higher temperature, which is phonon scattering.

2.5 Conclusion and Contribution

This chapter analyzes quasi-ballistic transport in nanoscale FDSOI MOSFETs at cryogenic temperatures down to 10 K including the effects of back-gate biasing. I_d–V_g characteristics are measured for standard as well as EG (SG and EG) devices with channel lengths ranging from 18 to 40 nm for SG and from 60 to 150 nm for EG. Important transistor electrical parameters and their modulation with back-gate bias are extracted and presented as a function of temperature down to 10 K. I analyze resistance by separating the components due to channel, ballistic, and series resistance as a function of channel length and temperature. From this analysis, I can extract series resistance and mobility. Analysis of mobility reveals the quasi-ballistic charge transport properties of FDSOI devices under test. Moreover, I extract mean free path and ballistic ratio and their dependence on temperature from 300 down to 10 K for SG and EG devices with different channel lengths. The temperature dependence shows the contribution from phonon and ionized impurity scattering. Compared to bulk Si MOSFETs, FDSOI devices reveal a smaller contribution from ionized impurity scattering at low temperatures as evidenced by a smaller reduction of the ballistic ratio (proportional to mobility) as temperature is reduced below 100 K. This is attributed to a lower doping concentration in the channel of FDSOI compared to bulk Si

CMOS. Additionally, I demonstrate the application of a VS compact modeling approach for FDSOI MOSFETs at cryogenic temperatures. Here, I propose an extension to the expression for inversion charge density to account for the effects of temperature and back-gate biasing on threshold voltage. Using an empirical model to account for the gate voltage dependence of series resistance and a model for apparent mobility based on Matthiessen's rule, I obtained very good agreements between calculations of drain current and experiments for temperatures ranging from 300 down to 10 K. The agreement between model calculations and data suggests that the VS modeling approach contains sufficient physics even in its compact mathematical formulation to maintain validity in its description of drain current of FDSOI MOSFETs down to cryogenic temperatures. This would beneficial the device analysis in the future research projects not only on Si based devices, but also on the devices based on novel materials such as graphene and TMDs.

CHAPTER 3

Current-Voltage Characterization of Graphene-FETs

3.1 Graphene-based Applications

Graphene emerged as a promising electronic material with exceptional properties including high electrical conductivity, mechanical strength, chemical stability, large surface area, etc. [8–10,37]. At the device-level, graphene field-effect transistors (GFETs) with high carrier mobility attracted considerable interest for high-frequency RF applications [38]. Its large surface-area-to-volume ratio makes it very sensitive to its surrounding environment and attractive for use in sensors [39,40], and memory technology [41,42]. Additionally, graphene was recently explored for potential use in devices for neuromorphic computing, a type of computing architecture that mimics the structure and functionality of the brain [15,16]. In memory, sensing, and neuromorphic applications, the sensitivity of GFET characteristics to charge trapped in the vicinity of the graphene channel has been explored as a non-volatile mechanism to store information (memory devices) and/or to manipulate an internal device state variable (sensors and neuromorphic devices) [17]. I noted that similar effects and applications have been reported with carbon nanotube devices [43–49].

In this chapter, the investigation centered on the fabrication and examination of graphene-FET devices at various temperatures, with a primary focus on their transport properties and the impact of temperature on the electrical characteristics.

3.2 Device Fabrication and Preparation

Staring with a wafer with 300 nm SiO_2 and diced it into 1.5 x 1.5 cm substrate, positive photoresist was spin-coated following by exposing the bottom independent gate pattern

with the laser writer. After developing, 20 nm SiO_2 was dry etched with fluorine-based plasma to create a trend for the gate as shown below in Fig. 11a, which will help to lower the height of the gold gate above the substrate surface to improve the uniformity of atomic layer deposition (ALD) layers to avoid the gate leakage. Afterwards, 5 nm chromium (Cr) and 25 nm gold (Au) were deposited on the surface following by a 2 or 5 nm HfO_2 ALD as shown in Fig. 11b.

The monolayer CVD-grown graphene was purchased from GROLLTEX, which came on a copper film. The copper film was etched by ferric chloride ($FeCl_3$) with PMMA coated on the top, and after cleaning the PMMA/Graphene film in HCl for 30 mins and DI water for 1 hours, it was transfer onto the targeting substrate and then cleaned by the Acetone. Then, the PMMA/LOR/positive photoresist is coated on the substrate with PMMA acting as a sacrificial layer to protect the monolayer graphene from peeling away during the

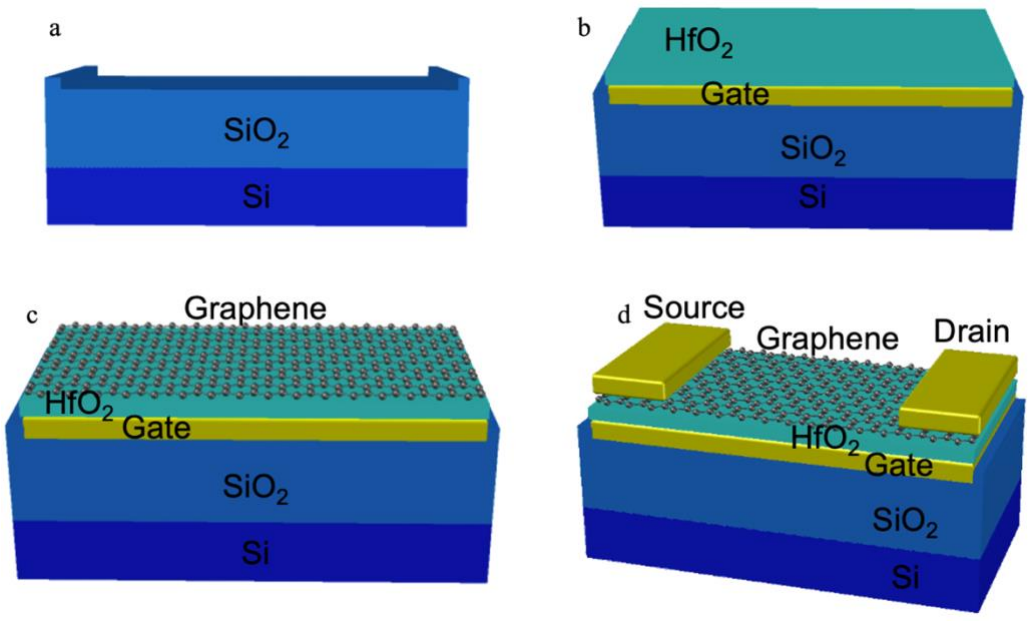

Fig. 11. Fabrication process of the graphene-based charge trapping device.

fabrication process. The fluorine-based plasma dry etching was used to define the shape of the channel area, and this would not only etch the graphene outside the channel region, but it would also remove the HfO_2 film that covers the gold contact pads to ensure a good electrical connection for the measurements.

The drain and source contacts were then defined by photolithography following by a forming gas H_2/Ar annealing at 125 °C for 30 mins to ensure a good contacting quality. The last step is depositing 5 nm Cr and 25 nm Au with lift-off process. Since I was using photolithography and customized photomasks, 20 x 20 grids, which is 400 in total, of graphene FETs can be fabricated a time as shown in Fig. 12a. The enlarged picture of the channel area is showing in Fig. 12b, where the channel length is 10 µm and width is 5 µm. The structure and the measurement setup of this high-k gate dielectric FET is illustrated in

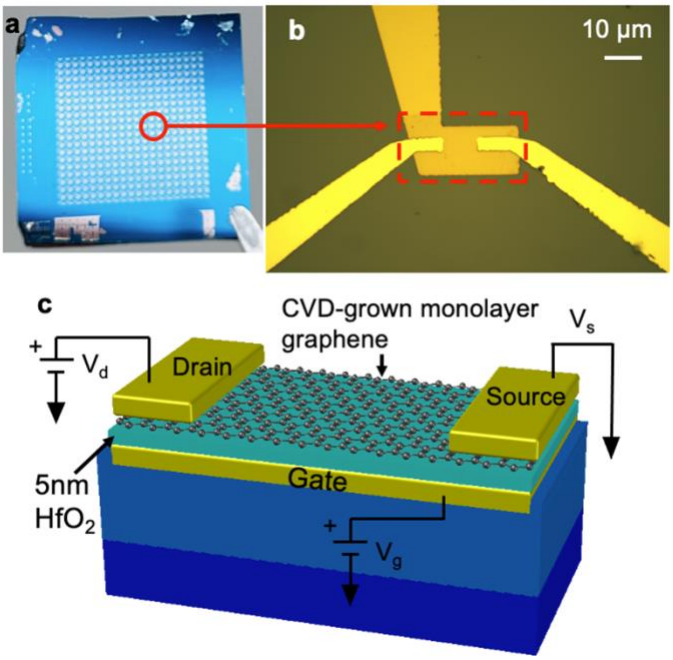

Fig. 12. a) picture of one 1.5 cm x 1.5 cm substrate with large area fabricated graphene FETs. b) Higher magnification image of graphene FET. c) The device structure illustration of the graphene FET.

Fig. 12c. The samples were in-situ annealed at 350 °C overnight to remove the hysteresis of the devices due to the interface impurities at the interface between the graphene and the high-k gate dielectric film.

3.3 Electrical Characterization and Temperature Dependence

The I_d-V_g measurements were taken at various temperature, where the gate voltage V_g was sweeping from -2 to 2 V with the drain voltage V_d set to 1 V. As shown in the Fig. 13, where the drain current is plotted as a function of the gate voltage across three different temperature levels (100 K, 200 K, and 300 K). To rule out the effect of the impurities, the Dirac point (V_{dirac}), which also refers to the charge neutrality point (CNP), which is the voltage level that the lowest current level occurs, of the IV curve at each temperature were aligned together. The current in the on-state region is showing a clear reduction with the

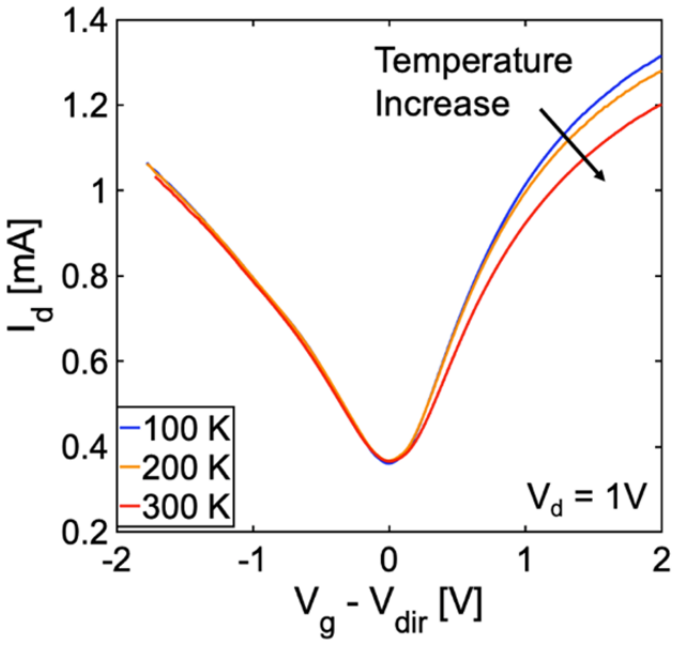

Fig. 13. Measured drain current (I_d) versus gate voltage (V_g) across various temperature levels (100 K, 200 K, 300 K) with aligned Dirac point (V_{dirac}) V_d = 1V

temperature going from 100 K to 300 K, and this is indicating the phonon scattering is getting more dominated in the channel[23,50–53].

To further investigate into the transport properties of the graphene-FET, I extracted the conductivity σ from the experimental data by firstly calculate the conductance (G) from I_d/V_{ds}, then σ can be calculated from $\sigma = G \times (\frac{L}{W})$, where L is the channel length 10 nm, and W the channel width 5 nm. The unit of conductivity (σ) was then converted to the quantum of conductance (*i.e.*, $2q^2/h \approx 77\ \mu S$) so that the quantitative results can be directly obtained as a function of carrier density (n_s) [22]. The carrier density (n_s) was estimated from $n_s = (C_{ox}/q)\ (V_g - V_{dir})$, where q is the electronic charge, and C_{ox} is the gate oxide capacitance per unit area. The conductivity was then plotted as a function of the sheet carrier density in Fig. 14. The rest of the analysis will be focusing on the electron

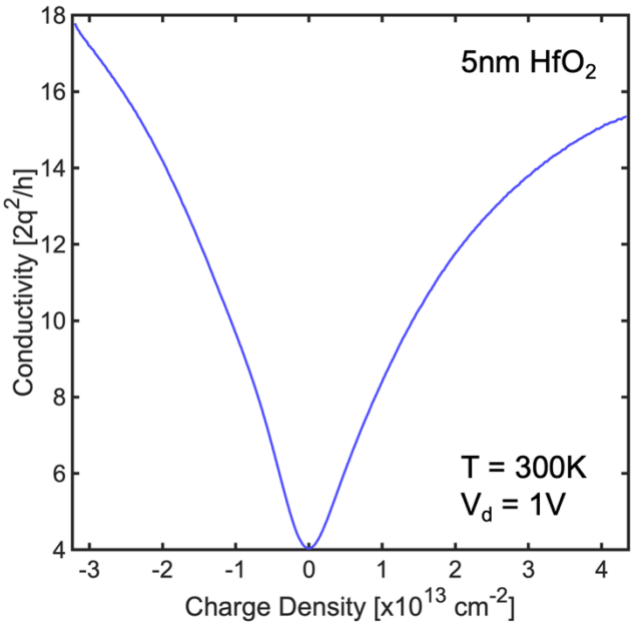

Fig. 14. Conductivity (σ) of the graphene-FET as a function of the carrier density (n_s)

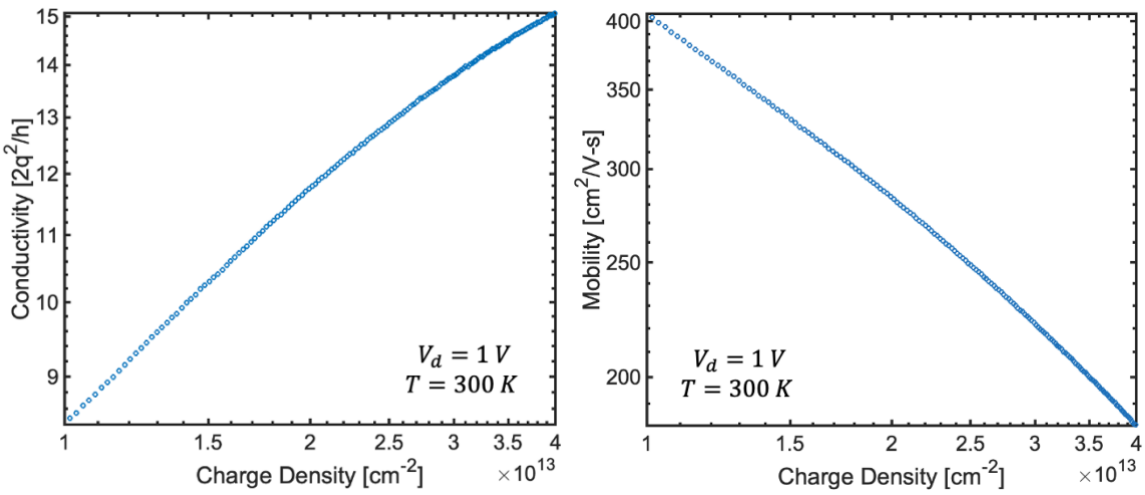

Fig. 15. Conductivity (σ) and mobility (μ) of the electron in the graphene-FET as a function of the carrier density (n_s) in log-log scale.

side of the measurements because it's showing a better temperature dependence as shown in the Fig. 13, which corresponding to the positive V_g - V_{dirac} region.

The mobility (μ) of the graphene FET can be obtained from the conductivity (σ) with $\mu = \sigma_n/(qn_s)$ for each fixed sheet carrier density (n_s) level for the electron side, and both conductivity and mobility of the electron can be plotted as a function of the carrier density in log-log scale as shown in the Fig. 15. The results are showing the increase of the conductivity due to higher electron charge density, while this would lead to more scattering in the channel, and this would degrade the mobility of the device as shown in the second figure.

3.4 Trapped Charge and the Hysteresis

The Graphene FETs with two different thickness of HfO_2, which are 2 nm and 5 nm, were tested. The drain current (I_d) was measured as a function of the gate voltage (V_g), while applying a constant drain voltage (V_d) at four temperature levels from 10 K to 300 K.

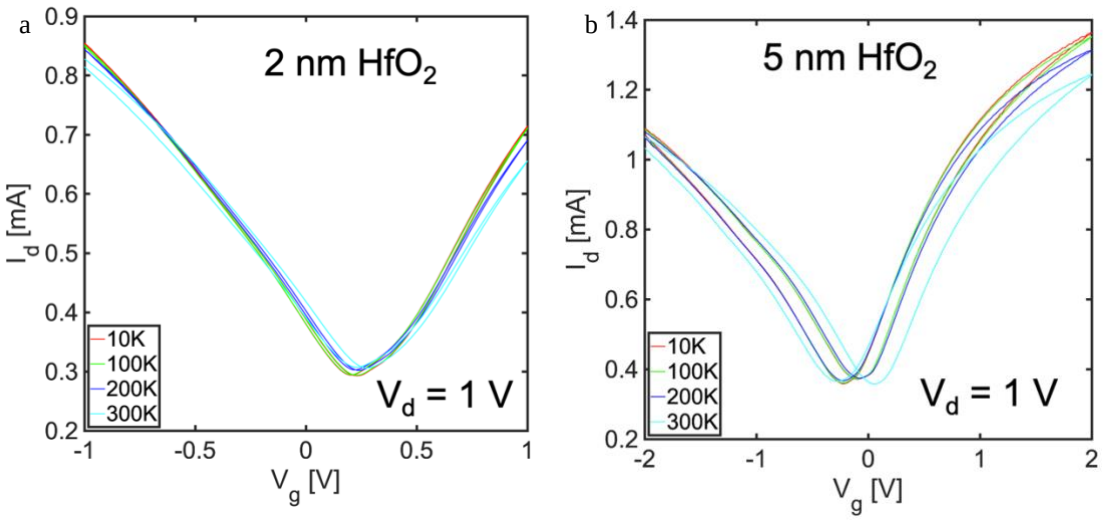

Fig. 16. Measured Id–Vg for the Graphene FET device with a) 2nm and b) 5nm gate oxide at various temperature levels. Large hysteresis is observed in 5nm HfO_2 device.

The results for both transistors in Fig. 16 are showing some hysteresis for all different temperature levels. Moreover, the hysteresis in the device with thicker gate oxide is having an obviously larger hysteresis compared to the device with thinner gate oxide, and this is indicating that there is more interface trapped charges in the 5 nm HfO_2 devices that impact the carrier transport. Thus, it's important to understand the effects of the trapping charges in these graphene-based devices, and this trapped charge can be utilized potentially as memory device as shown in Fig. 17[17] or the synaptic graphene-based FET as shown in Fig. 18[18].

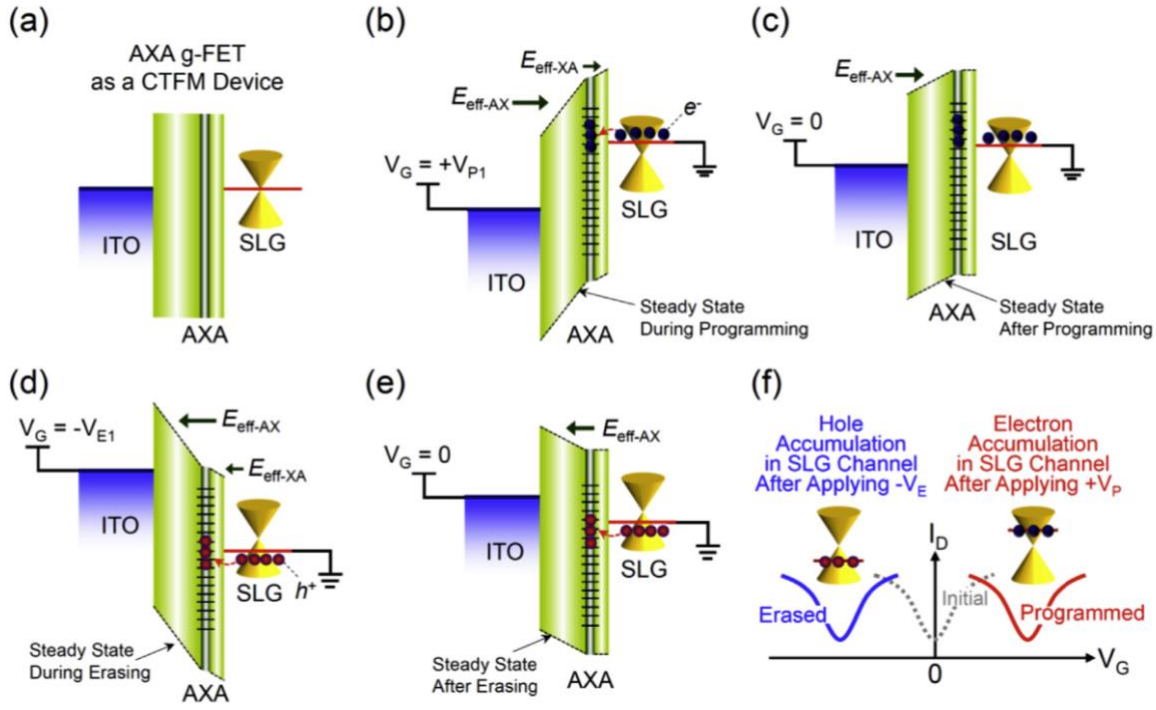

Fig. 17. Graphene based charge-trap flash memory that consists of gate oxide stacks to program and erase with the trap charges in the stacks as a memory window[17].

Lee's group fabricated this graphene-based flash memory device that contain a high-k/low-k/high-k oxide stacks, where the low-k layer is for trapping the charges. By applying a different gate pulse, either electrons or holes would be injected and trapped into the charge trapping layer as shown in Fig. 17b and d. This trapped charge would affect the transport properties of the device and would shift the position of the CNP towards the positive V_g side, which is mainly electrons storage, or towards negative side, which is holes storage correspondingly. The difference between the CNP of the erasing and programing is the storage window, as shown in Fig. 17f[17].

This trapped charge mechanism can also be utilized to mimic the human's neuron system by using the Graphene FET as a synaptic device as shown in Fig. 18. The middle

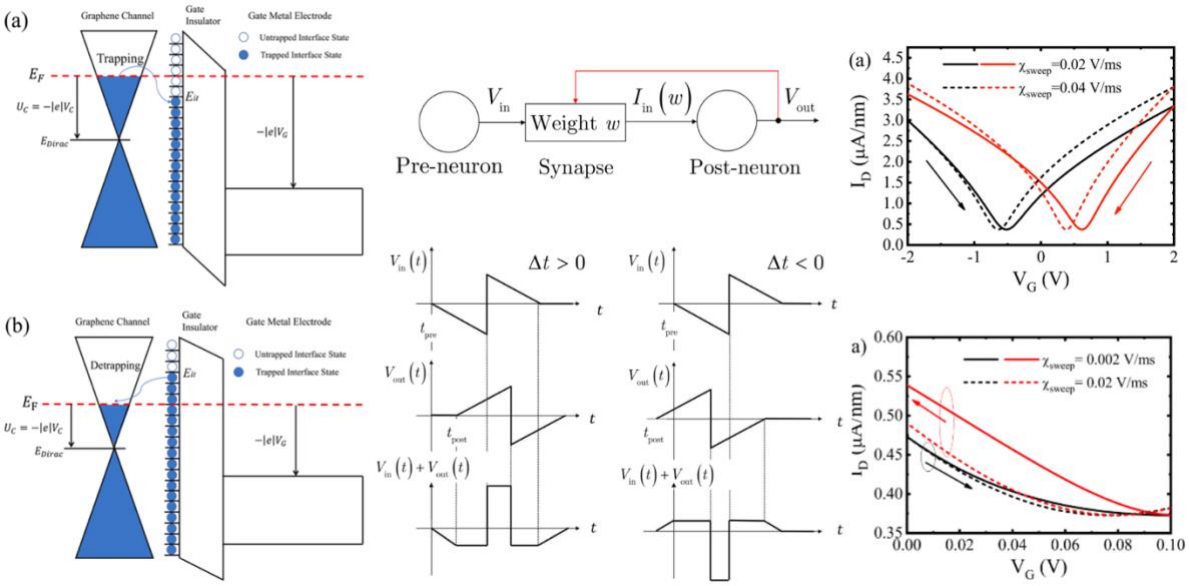

Fig. 18. Graphene FET based synaptic device to mimic human's neuron system [18]

top figure is showing the illustration of the device, where it consists of a pre-neuron and a post-neuron, and it's connected by the synapse, which is the graphene-based FET that can provide a weight factor ω. Similar as the memory device shown in Fig. 17, this graphene FET in the synaptic device is also utilizing the charge trapping mechanism. The left two figures in Fig. 18 are showing the energy band diagram, where when a different gate bias have been applied, the graphene FET can either be programed by trapping the electrons from the graphene channel into the traps at the interface or be erased by releasing the electrons from the traps back into the graphene channel. By manipulating the amount of the trapped charges at the interface, the hysteresis of the graphene transport curves can be adjusted as shown in the right two figures, and the size of the hysteresis are used as different weight factor ω in the synaptic system.

Prior investigations primarily revolved around modeling, characterization, and the utilization of CNP shifts in memory devices or their incorporation into neuromorphic computing devices. In my research, the primary emphasis was placed on the examination of a comparable charge trapping mechanism occurring at the interface, the subsequent scattering effects it induced, and the resulting impact on the transport properties of graphene-FET devices. This encompassed an analysis of parameters like conductivity, mobility, and mean-free-path in the low-field region.

CHAPTER 4

Scattering Mechanism of the Graphene-based Charge Trapping Devices

4.1 Charge Trapping Effects

The operation (writing and reading) of graphene-FET memory and neuromorphic devices can be driven through electrical stimulation (e.g., with the application of a pulsed terminal voltage, typically the gate) making it compatible with conventional electronic technology. A field-driven buildup of fixed charge, commonly known as charge trapping, results in charge redistribution inside the GFET with a measurable electrostatic impact in device operation. This impact is typically observed as a voltage shift in the current-voltage (I-V) characteristics of GFETs and quantified with shifts in Dirac voltage (a.k.a., the charge neutrality point)[54]. While several studies have investigated charge-trapping-induced electrostatic effects in GFETs from shifts in Dirac point voltage (V_{dir}) [17,18,54,55], the impact on charge transport is less commonly studied and far less understood. Nonetheless, trapped charge near the graphene channel and gate dielectric interface in GFETs is expected to enhance scattering with a detrimental impact on device performance[33]. Consequently, this effect should be investigated in GFETs with few-nanometers-thin high-k dielectrics and independent gates, which are most likely to be used in ultrascaled devices with 2D channel materials[56–58]. Many previous works are focused on GFETs with thick SiO_2 gate dielectrics on silicon substrates that are used as global back gate. [54,59,60]

In this chapter, I investigated the effects of charge trapping on the transport properties of GFETs with high-k gate dielectrics. Specifically, devices with monolayer graphene channels and 5 nm HfO_2 gate dielectrics are pulsed at the gate terminal to stimulate charge

trapping, and then tested by measuring their current-voltage (I-V) characteristics. I quantified the impact of charge trapping not only by electrostatic shifts in I-V response, but also by degradation in conductivity and mobility as a function of bias (i.e., as a function of sheet carrier density). The results show a degradation in conductivity and mobility as well as a transition in their dependence on sheet carrier density. Using a model based on Landauer transport theory[33,36,61,62], I correlated trapping-enhanced charged-impurity scattering to degradation in conductivity and mobility. Moreover, I quantified the reduction in carrier backscattering mean free path as a function of buildup in the density of charged impurities. Roughly, a buildup of 7×10^{12} cm^{-2} in trapped charge resulted in 30% reduction of (charged-impurity) backscattering mean-free-path.

4.2 Measurement and Data Analysis

The charge trapping effect induced by a voltage pulse on the gate was investigated. The drain current (I_d) as a function of gate voltage (V_g) was measured before any pulses applied as the initial state of the device. To introduce the charge trapping, a gate pulse with V_g = 2.5 V was applied on the gate for 5 s, while having a drain voltage V_{ds} = 1 V. A total number of 20 pulses were applied and an I_d-V_g measurement was performed immediately after each pulse. The charge trapping effects were studied for the positive gate pulses at the room temperature condition, where the negative pulses conditions and the low temperature (below 200 K) measurements were also performed, but the shifting of CNP and the degradation of the on-state current were both negligible.

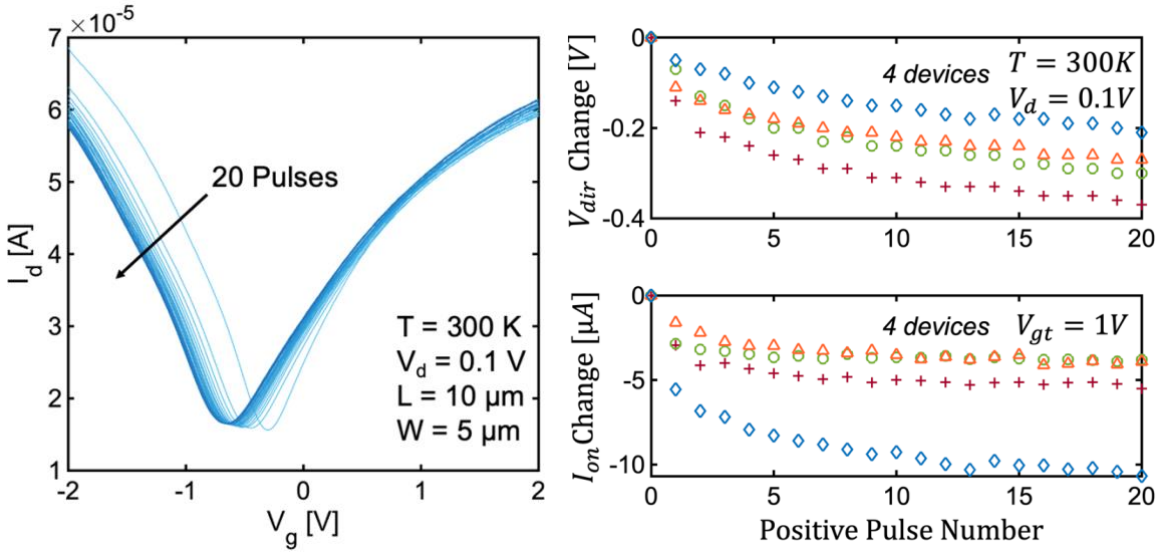

Fig. 19. a). Drain current (I_d) versus gate voltage (V_g) with V_{ds} = 0.1 V after 20 times 5 s 2.5 V positive voltage pulses applied on the gate. b). Top: Charge Neutrality Point (CNP) shifting after 20 number of pulses in 4 devices with the same parameters. Bottom: The deduction of the on-current level with number of gate pulses, extracted at a fixed V_{gt} level, where $V_g - V_{dir}$ = 1 V.

In Fig. 19a, the I_d-V_g results after 20 pulses with the initial states were showing, where the light blue curve on the top is the initial condition before applying any gate pulses. The impact from the gate pulses on the CNP shifting and the current levels are evident. To better see the change on the CNP and on-state currents, the CNP value was subtracted by the CNP at the initial state to extract the change of CNP after each pulse, and the results have been shown in the top figure of Fig. 18b. The extracted results from four devices with the same configurations were shown and the shifting directions are towards the negative direction for all devices, and the difference between the devices are contributed from the variation from device to device. Another less obvious effect related to transport is a reduction in on-state current (I_{on}) associated with enhanced charged impurity scattering [63–65]. The similar extraction can be done for the on-current (I_{on}), where the I_{on} can be extracted

at a fixed $V_g - V_{dir} = 1$ V, and the value after each pulse was subtracted by the initial state I_{on}. The bottom figure of Fig. 19b is showing the change of the I_{on} as a function of pulse numbers for four devices. In the first five pulses, the changes of the I_{on} were more rapid compared to the change after pulse number 5, which indicates that most of the empty traps near the interface are filled and less carriers are getting trapped, and this led to less significant impact on the degradation.

The energy band diagram in Fig. 20a illustrates the alignment of graphene bands next to the 5 nm HfO_2 gate dielectric layer and metal gate (Au). Here I indicated estimates of the Au metal gate work function (~5.1 eV) [66], affinity and bandgap for HfO_2 (~1.8 eV and ~5.9 eV respectively) [67], as well as the affinity for graphene (~4.6 eV) [68]. As noted, these parameters result in a smaller energy barrier for injection of holes from metal gate into HfO_2 (~2.5 eV) compared to electrons (~3.3 eV). This could help explain why I observe a buildup of positive charge (determined from negative voltage shifts in I-V measurements) with application of positive V_g pulses. Fig. 20b illustrates the energy band diagram at the charge-trapping (pulse) biasing condition with large $V_g > 0$ V. As shown, I attribute the

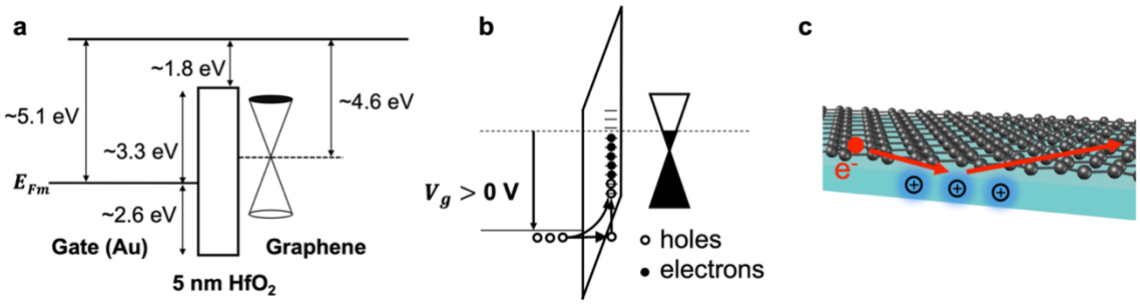

Fig. 20. a). The band diagram of the devices with gate voltage $V_g = 0$ V (Initial state). b). The band diagram of the devices with applying a positive voltage pulse (5 s $V_g = 2.5$ V) on the gate. c). The charge trapped near the interface of graphene and high-k dielectric would introduce charge impurity scattering while electrons flowing through the channel.

buildup of positive charge to injection of holes from the metal gate to traps in the HfO_2 gate dielectric. The trapped charge introduces long-range scattering potentials that affect the transport of electrons in the graphene channel as illustrated in Fig. 20c. Ultimately, this reduced the mean-free-path (i.e., average distance traveled between scattering events) degrading conductivity and mobility.

To investigate the impact of the trapped charge on the conductivity (σ) of the device, I extracted the σ as mentioned in the previous chapter for the graphene initial study. The results of σ as a function of n_s for all 21 measurements are shown in Fig. 21, where the dependency of the conductivity on the carrier density was obviously impacted by the trapped charges with more gate pulses applied.

By looking closely on a smaller range of the carrier density on the electron conduction side from 1.5 to $3 \times 10^{13}\ cm^{-2}$, the change of the dependency of conductivity on the

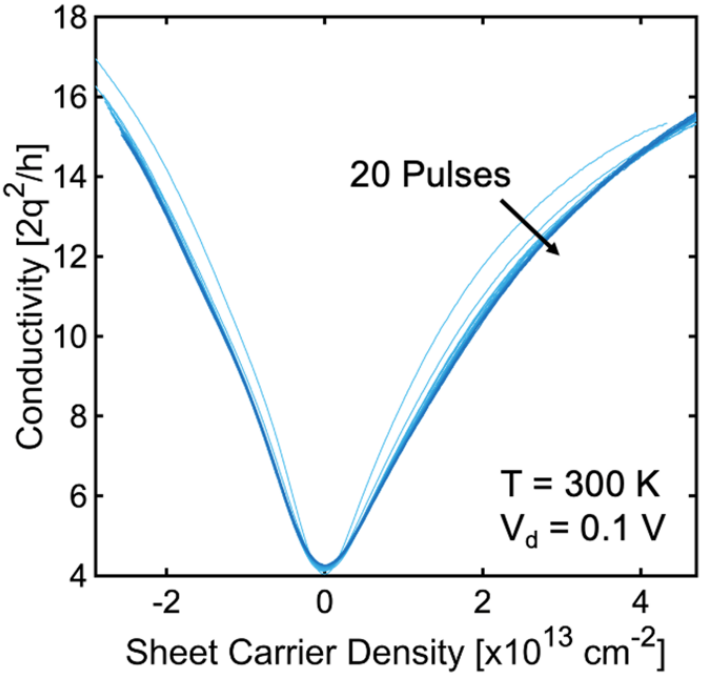

Fig. 21. The extracted conductivity (σ) as a function of sheet carrier density (n_s).

carrier density can be easier to identify as shown in Fig. 22a. The red symbol on the top is the initial state σ, which is approximately having a sub-linear dependency on the n_s (red dashed line is ~ $(n_s)^{1/2}$). With more gate pulses applied, where more trapped charges were introduced, the dependency on the n_s are start getting steeper and closer to the linear dependency (~ n_s). Charged impurity scattering is theoretically predicted to have a linear $\sigma(n_s)$ relationship for graphene [64,65,69]. To better see the change in the slope of these σ (n_s) curves, the power exponents of the curves were extracted from the logarithmic figure and plotted in Fig. 22b as a function of the number of gate pulses. It's noticeable that at the initial state, the dependency is close to ~ $(n_s)^{1/2}$ sub-linear at 0.52, and with more gate voltage pulses applied, the power exponent starts increasing from 0.52 to 0.6 after 6 pulses, indicating that the dependency is getting closer to linear (~ n_s), and some scattering mechanism was induced by the trapped charge and getting more dominated with more

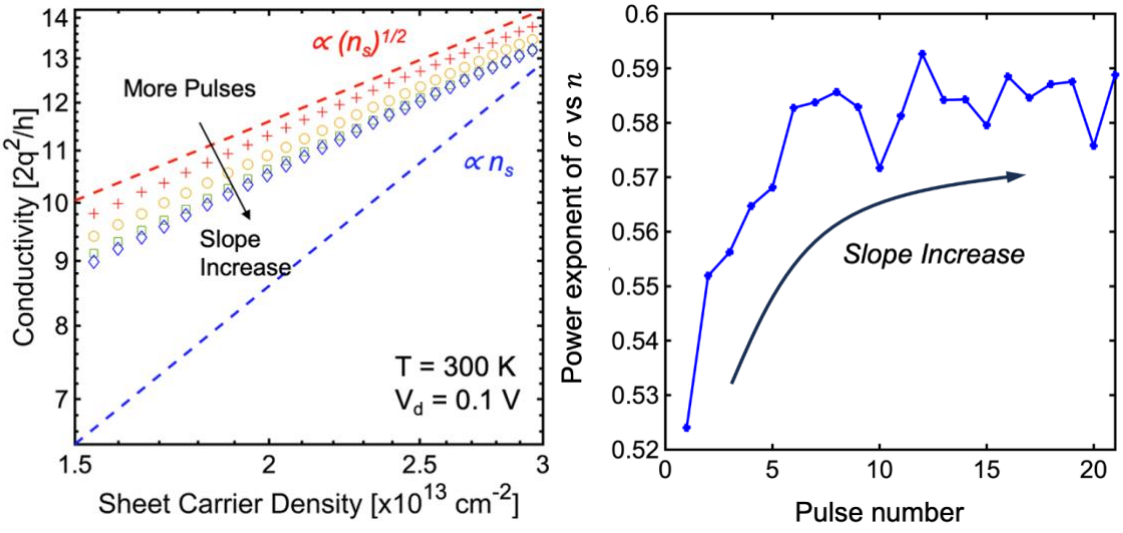

Fig. 22. a). The change of conductivity (σ) dependency on the sheet carrier density (n_s) with the dependency initially from ~ $(n_s)^{1/2}$ and getting closer to linear. b). The extracted power exponents for $\sigma_n(n_s)$ after each pulse versus the number of pulses.

applied pulses, and it starts to limit the conductivity of the carriers in the channel. This same trend was extracted and observed in the other devices.

I further investigate the degradation of the conductivity and the mobility due to the induced trapped charge. The mobility (μ) was obtained with $\mu = \sigma_n/(qn_s)$. By having the amount of the CNP shifting from ($V_{dir} - V_{initial}$), the density of the trapped charge density (N_T) can be estimated with the $N_T = (C_{ox}/q)(V_{dir} - V_{initial})$. Both conductivity and mobility were extracted for the measurements after each pulse at a fixed carrier density level $n_s = 1.88 \times 10^{13}\ cm^{-2}$, which is corresponding to $V_g - V_{dir} = 1\ V$. Fig. 23 is showing the results of extracted mobility and conductivity as a function of trapped charge density. It's evident that more gate pulses induced higher density of trapped charge, and it's degrading both conductivity and mobility. This is another indication that the trapped

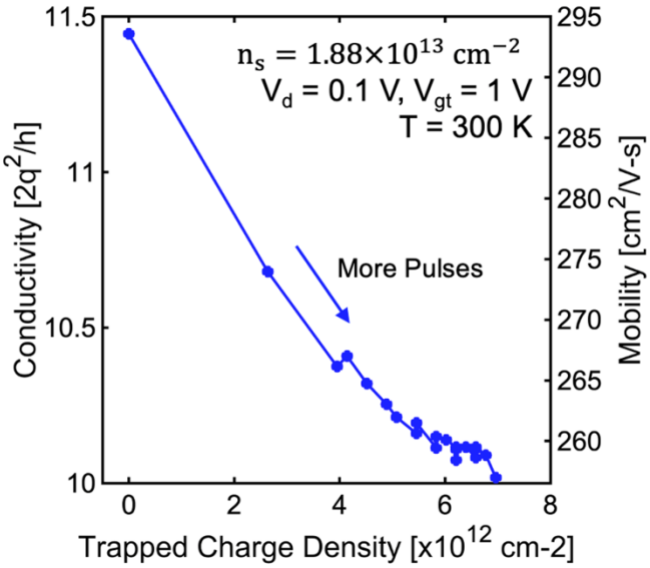

Fig. 23. The degradation of conductivity (left) and mobility (right) at a fixed V_{gt} as a function of the trapped charge density (N_T).

charges near the interface introduced more scattering and it's getting more dominated to limit the carrier transport.

4.3 Landauer-based Model Assist Analysis

To understand more on the scattering mechanism associated with the charge trapping, the model that was used in the first FDSOI project was also applied here. This modeling analysis is based on Landauer approach, where drain current can be expressed as[62,70–72]

$$I_d = \frac{2q}{h}\int M(E)T(E)[f_S(E) - f_D(E)]dE \quad (1)$$

Where M(E) is the energy dependent density of modes in the channel and it's obtained from the band structure of graphene as $M(E) = 4W|E|/(h v_F)$, where W is the channel width and v_F is the constant electron velocity (≈10^8 cm/s)[33,73]. $T(E)$ is the transmission coefficient and $T(E) = \lambda(E)/[\lambda(E) + L]$, where L is the channel length, and $\lambda(E)$ is the energy dependent backscattering mean free path[74]. The applied bias on the drain and source contribute to the fermi functions difference, which is denoted by $f_S(E) - f_D(E)$. This expression can be simplified with Taylor series expansion due to low field transport based on the near equilibrium approximation that $f_S(E) - f_D(E) \approx (-\partial f/\partial E)(qV_{ds})$. The formula (1) can be re-written, and the conductance can be obtained as

$$G = \frac{I_d}{V_{ds}} = \frac{2q^2}{h}\int \frac{\lambda(E)}{\lambda(E)+L}\left(\frac{4WE}{h v_F}\right)\left(-\frac{\partial f}{\partial E}\right)dE \quad (2)$$

There are two types of carrier transports were considered, which includes ballistic transport, where T = 1 due to $L >> \lambda$; and diffusive transport, where $T = \lambda/L$. From the conductivity equation $\sigma = G * L/W$, the ballistic conductivity (σ_{ball}) can be expressed as

$$\sigma_{ball} = L\left(\frac{2q^2}{h}\right)\left(\frac{4k_B T_L}{h v_F}\right) F_0(\eta_F) \quad (3)$$

where F_0 is the Fermi-Dirac integrals of order 0. The general format of Fermi integrals can be defined as shown in [75]:

$$F_i(\eta_F) \equiv \frac{1}{\Gamma(i+1)} \int_0^\infty \frac{\varepsilon^i d\varepsilon}{1 + \exp(\varepsilon - \eta_F)} \quad (4)$$

In formula (4), i is the order of the Fermi-Dirac integral. The gamma Γ is the factorial function, where $\Gamma(\mathrm{n}) = (\mathrm{n}-1)!$. ε and η_F are defined as $\varepsilon = (E - E_C)/k_B T$, and $\eta_F \equiv (E_F - E_C)/k_B T_L$.

The devices are mainly operating in the diffusive transport regime instead of ballistic transport, which means the transport is limited by the scattering. Two types of scattering were considered in the model, the first one is charged impurity scattering (ci), which is impacted by the induced trapped charge in the device, and the second scattering is the short-range scattering (sr), which is mainly induced by the defects in the graphene and the lattice imperfections. As mentioned earlier, the transmission coefficient will be in the diffusive transport case with the impact of scattering, that the coefficient will be $T = \lambda/L$. And this energy dependent $\lambda(E)$ can be modeled with the power law function[33,74,76], $\lambda_0(E/K_B T_L)^s$, where λ_0 is the fitting parameter, and s is the exponential factor determined by the dimensionality of the scattering mechanism, which is dependent on the proportionality to the density of the states (s = 1 for charge impurity scattering and s = -1 for short-range scattering). Thus, the $\lambda(E)$ can be expressed independently for each of the scattering mechanism, and after putting it back to the formula (2), the derived charge impurity limited conductivity (σ_{ci}) and short-range limited conductivity (σ_{sr}) can be written as

$$\sigma_{ci} = \lambda_{0ci}\left(\frac{2q^2}{h}\right)\left(\frac{4k_B T_L}{hv_F}\right)F_1(\eta_F) \quad (5)$$

$$\sigma_{sr} = \lambda_{0sr}\left(\frac{2q^2}{h}\right)\left(\frac{4k_B T_L}{hv_F}\right)F_{-1}(\eta_F) \quad (6)$$

Carrier density (n_s) can be modeled with the fermi function and the density of the states by

$$n_s(E_F) = \int D(E)f(E)dE = \frac{2}{\pi}\left(\frac{k_B T_L}{hv_F}\right)^2 F_1(\eta) \quad (7)$$

The total modeled conductivity can be obtained by Matthiessen's rule as $1/\sigma = 1/\sigma_{ball} + 1/\sigma_{ci} + 1/\sigma_{sr}$. Fig. 24a plots σ versus n_s where symbols are the experimental data and lines are the model calculations. The individual diffusive components (i.e., σ_{ci} and σ_{sr}) are shown with dashed lines, and the total conductivity (σ) is shows as solid lines. The data was fitted prior to any charge-trapping pulses as well as after various consecutive voltage pulses (arrows indicate change in conductivity with more pulses). The fit to experimental data was accomplished by adjusting the charged-impurity backscattering mean free path fitting parameter λ_{0ci}. Thus, the effect is attributed to a reduction in σ_{ci}, which is consistent with transport degradation due to trapped charge buildup near the graphene channel/insulator interface resulting from voltage pulses on the gate. In the fitting process, it confirms that parameter λ_{0ci} is inversely proportional to trapped charge density (n_T) obtained from shifts in Dirac voltage. A small change (increase) in σ_{sr} was noted and it was also introduced to better fit the data (especially for large n_s), but here I focus on the more significant effects of charged impurity scattering. Nonetheless, the physical origin of

this adjustment may be from self-healing/annealing of defects and should be studied further[77].

With this modeling approach I can better explain my experimental observations regarding the dependence of conductivity on sheet carrier density, $\sigma(n_s)$. Firstly, the observed square-root dependence prior to pulsing is explained as the combined effect of charged-impurity and short-range scattering which individually have square-root and linear dependence on n_s respectively. As shown in Fig. 24a, the experimental values fall in a range of n_s where I have a transition from σ_{ci} to σ_{sr} as the dominant scattering effect. Next, with increasing number of pulses (increasing density of charged impurities) a more significant contribution from σ_{ci} makes the overall conductivity move closer towards a linear dependence on n_s. I do not observe a transition to completely linear dependence (i.e.,

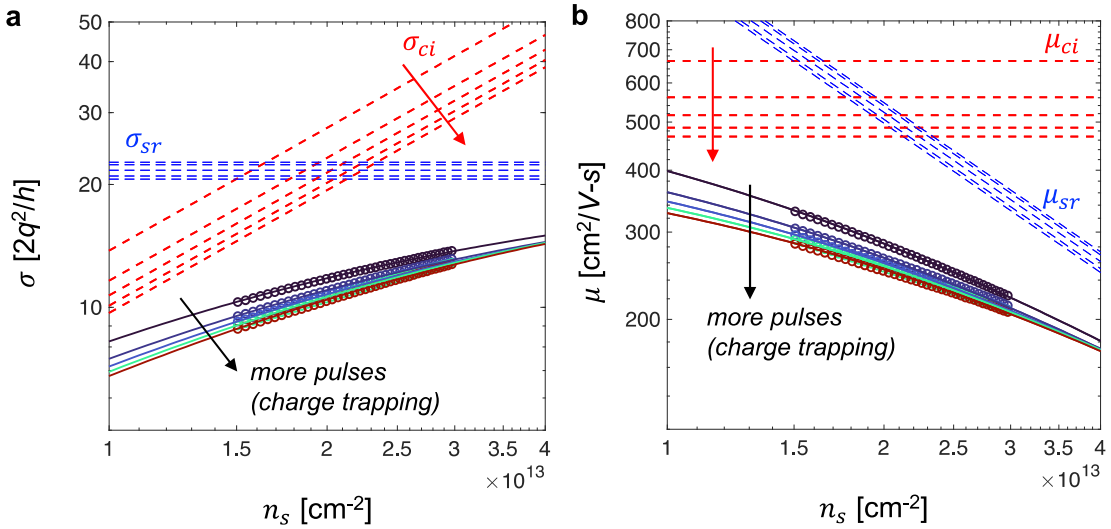

Fig. 24. a). modeled conductivity (colored solid lines) limited by charge impurity scattering (σ_{ci} – colored dashed lines) and short-range scattering (σ_{sr} – black dashed line), and b). modeled mobility (colored solid lines) limited by μ_{ci} (colored dashed lines) and short-range scattering μ_{sr} (black dashed line), fitted to the experimental data (symbols) before and after 12 gate voltage pulses.

$\sigma \sim n_s$) since short-range scattering effects continue to play a role on conductivity, especially for large n_s[78–80]. Nonetheless, with the more dominant contribution from σ_{ci}, the transition to a short-range scattering dominated conductivity is pushed to larger n_s[33].

The mobility can be obtained as $\mu = \sigma/qn_s$. Fig. 24b plots μ versus n_s where symbols are the experimental data and lines are the model calculations. The individual components (μ_{ci} and μ_{sr}) are shown with dashed lines, and the total mobility obtained using Matthiessen's rule ($1/\mu = 1/\mu_{ci} + 1/\mu_{sr}$) is shows as solid lines. To obtain further insight on the impact of charged impurities on the transport properties of the graphene FETs I extract the corresponding energy-averaged backscattering mean free path as [33]

$$\langle \lambda_{ci}(E) \rangle = \frac{\int M(E)\lambda_{ci}(E)\left(-\frac{\partial f}{\partial E}\right)dE}{\int M(E)\left(-\frac{\partial f}{\partial E}\right)dE}. \quad (5)$$

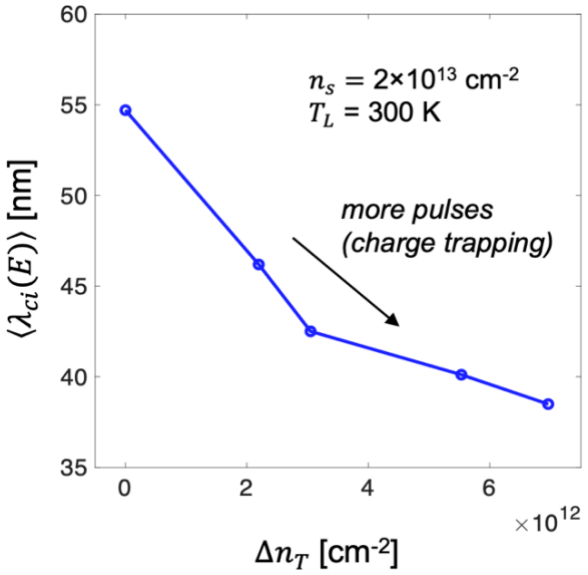

Fig. 25. Calculated mean-free-path ($\langle \lambda_{ci}(E) \rangle$) as a function of the trapped charge buildup.

This represents a weighted average of the mean-free-path over the Fermi-window (i.e., $-\partial f/\partial E$) centered around the (bias-dependent) Fermi level. The calculation of $\langle \lambda_{ci}(E) \rangle$ is shown in Fig. 25 as a function of trapped charge buildup (Δn_T) for fixed sheet carrier density of n_s = 2×10^{13} cm^{-2}. This corresponds to $V_g - V_{dir} \approx 1\ V$. As shown, the average mean-free path (corresponding to charged-impurity scattering) decreases from about 55 nm down to about 38 nm for a trapped charge buildup of ~7×10^{12} cm^{-2} at this biasing condition.

4.4 Conclusion and Contribution

In this chapter, I reported on experimental and theoretical analysis of charge trapping effect in graphene field effect transistors (GFETs) with ultrascaled 5 nm high-k gate dielectrics HfO_2. Charge-trapping experiments based on applying the gate voltage pulses are used to characterize the electrostatic effects, which lead to the shifts in voltage at the Dirac point, as well as transport degradation, which shown by the reduction in on-state current, attributed to buildup of charged impurities, which is induced by the trapped charge inside a 5 nm HfO_2 gate dielectric interfacing the graphene channel. Theoretical analysis based on the Landauer equation allows correlating trapping-enhanced charged-impurity scattering to degradation in the transport properties such as conductivity, mobility, and mean-free-path. This work also provides new insights about the significance of charged-impurities on the reliability and performance of graphene devices with high-k gate dielectrics that operate based on charge-trapping mechanisms or that simply have a high-k oxide layer adjacent to a graphene channel. Specifically, I establish that with gate-voltage pulsing the well-known shifts in Dirac voltage are accompanied by a significant degradation in conductivity and mobility as well as a transition towards dominance of

charge impurity scattering as evidenced by their dependence on sheet carrier density. This is crucial for devices such as graphene-based non-volatile memory, memristive and neuromorphic devices, graphene FETs, and many others.

Chapter 5

Analysis of Contact Resistance Using Graphene FETs TLM Structure

5.1 Importance of Contact Resistance

The formation of an ohmic contact involves a direct connection between a ferromagnetic metal and the semiconductor channel material. However, this ohmic contact at the junction can compromise the efficiency of spin injection and polarization, a phenomenon known as the conductivity mismatch. The root of this conductivity mismatch problem lies in the substantial difference in conductivity between ferromagnetic metals and semiconductors. This can be illustrated with the circuit shown in Fig. 26[81], where the resistances of two ferromagnetic contacts and the semiconductor can be categorized into two distinct channels. The top and bottom channels correspond to spin-up and spin-down polarization, respectively.

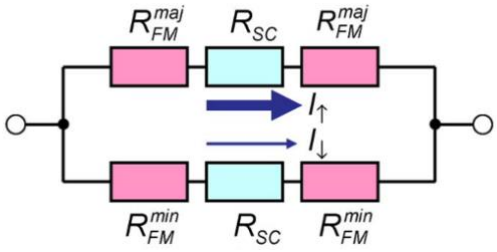

Fig. 26. Resistance of ohmic contacts for spin-up and spin-down channels without tunneling barriers.

While the resistance of the semiconductor typically exceeds that of ferromagnetic metals, the bulk of the voltage drop occurs within the semiconductor region. Consequently, the spin-dependent resistance, emanating from the ferromagnetic contacts, has a minimal impact on the current within the spin-up and spin-down channels. Here, the primary determinant of current is the spin-independent resistance of the semiconductor.

To address the issue of conductivity mismatch, an effective approach involves incorporating a tunneling barrier at the interfaces of the ferromagnetic metal and semiconductor junction, rather than relying on ohmic contacts. This tunneling barrier typically takes the form of an ultrathin insulator, which introduces a metal/semiconductor Schottky barrier at the interface. Although the tunnel resistance (contact resistance) itself is inherently spin-dependent, it becomes intricately linked with the adjacent ferromagnetic metals.

As a result, when the spin-dependent contact resistance is comparable or slightly higher than the semiconductor resistance, the cumulative resistances for the spin-up and spin-down channels exhibit significant differences. This configuration ultimately ensures that the total current passing through the structure becomes spin-polarized, a phenomenon illustrated in Fig. 27. This innovative approach effectively overcomes the conductivity mismatch problem and holds promise for advancing the efficiency and performance of spintronic devices.

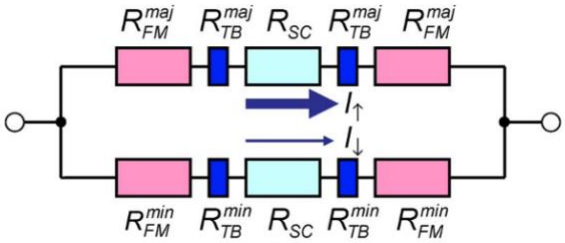

Fig. 27. Resistance of spin-up and spin-down channels with tunneling barriers resistance.

However, when the contact resistance surpasses a critical threshold compared to the conductor resistance, it poses a potential limitation on the flow of carriers within the channel. This condition can be visually depicted in Fig. 28, where R_{SF} represents the influence of spin flip. In situations where the contact resistance is excessively large, the

resistance of both the ferromagnetic materials and the semiconductor can be effectively disregarded. The spin-flip resistance can be approximated as a short circuit under these circumstances. While this configuration doesn't significantly affect the parallel arrangement, where the spin polarization remains consistent on both sides of the semiconductor, it has a notable impact in the anti-parallel configuration.

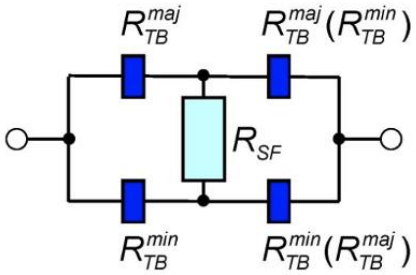

Fig. 28. Resistance of spin-up and spin-down channels with large tunneling barriers resistance.

In the anti-parallel configuration, this short circuit disrupts the spin polarization, resulting in the combined resistance for both the parallel and anti-parallel orientations being nearly identical. This phenomenon renders the tunnel magnetoresistance (TMR) effectively zero. TMR is calculated using the formula $(R_{AP}-R_P)/R_P$, where R_{AP} represents the measured resistance during the anti-parallel configuration, and R_P denotes the measured resistance during the parallel configuration. Ideally, TMR should yield values significantly greater than a few percent, rather than approaching zero. This measure is indicative of the effectiveness of spin polarization within the channel, and its optimization is critical for the overall performance of spintronic devices[82].

Hence, the contact resistance assumes a critical role and necessitates meticulous study and optimization. It should be tailored to match or slightly exceed the magnitude of the resistance within the semiconductor channel, ensuring the creation of an efficient tunneling

barrier. Several key components were investigated to address this issue, including the study of contact resistance in ohmic contacts, the channel resistance, and the resistance after the incorporation of a tunneling barrier. These investigations collectively form the foundation for establishing efficient spintronic devices, where the careful management of contact resistance plays a pivotal role in achieving desired performance and characteristics.

5.2 Transfer Length Methods (TLM) Structure

Using the transfer length methods, which involves electrical measurements of the same channel with varying channel lengths, provides a powerful tool for extracting crucial parameters of the device. This method enables the extraction of contact resistance, channel resistance, and mobility, offering valuable insights into the device's behavior and performance.

In our study, we implemented a TLM structure featuring a monolayer graphene channel and a 5 nm HfO_2 insulator, as illustrated in Fig. 29. The contacts utilized in this structure are non-magnetic and consist of 5 nm Cr and 35 nm Au. These contacts were directly

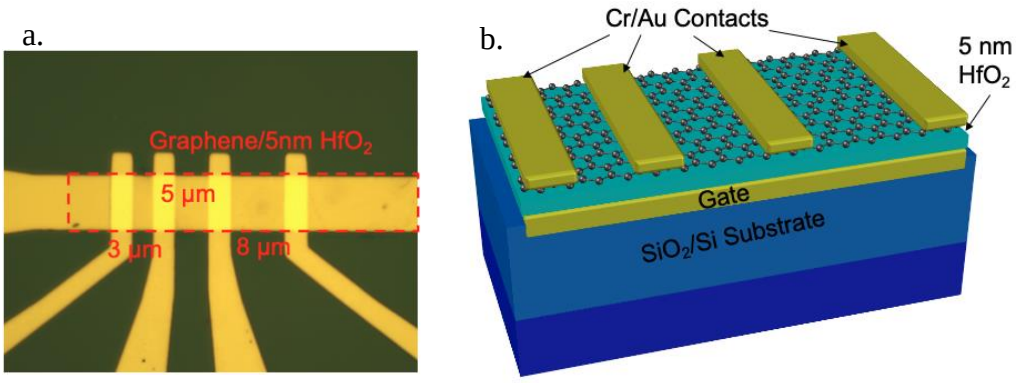

Fig. 29. a. Microscopy picture of the TLM structure based on graphene with 5 nm HfO_2. b. Schematic illustration of the TLM structure.

deposited onto the graphene channel to establish an ohmic contact. The device itself encompasses three distinct channel lengths, measuring 3 µm, 5 µm, and 8 µm, respectively.

The I_d-V_g measurements for each channel length condition were performed at various temperature levels from cryogenic temperature 10 K to room temperature 300K, where the drain voltage is at a fixed value V_d = 1 V. The drain current was normalized to the width of the electrodes, which is 8 µm. The normalized drain current at room temperature T = 300 K was plotted as a function of the aligned gate voltage (V_{gt}) as shown in Fig. 30 for all three channel length conditions. As the channel length increases, we observe a corresponding decrease in the current level. This decrease in current serves as a clear indicator of the rising resistance within the channel. Longer channel lengths inherently result in increased resistance, a fundamental relationship that underscores the importance

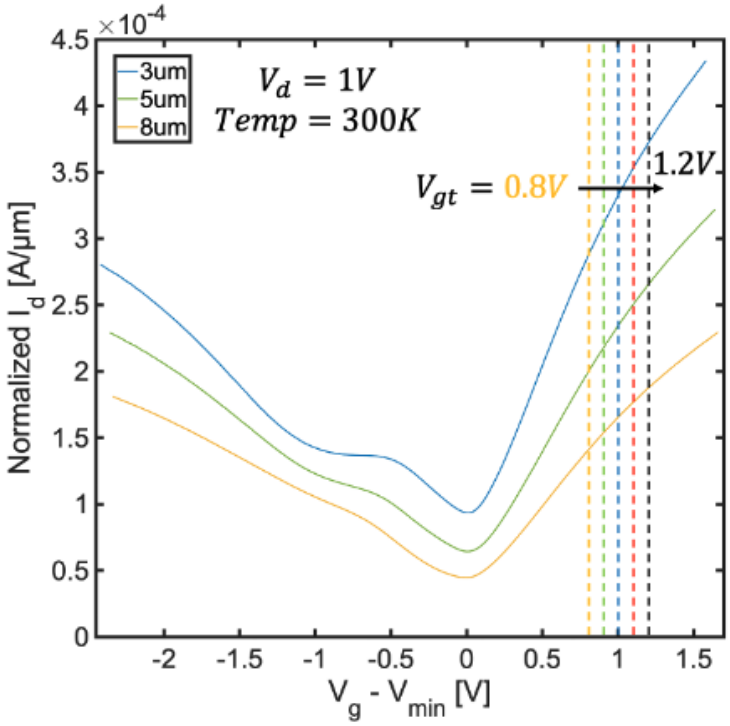

Fig. 30. Normalized drain current I_d as a function of aligned gate voltage V_g - V_{min} (V_{gt}) at room temperature T=300 K with V_d=1 V across three different channel length.

of channel length in determining the device's electrical behavior. The channel resistance is then calculated for each channel length at five different V_{gt} levels as shown by the colored dashed lines in Fig. 30a ranging from V_{gt} = 0.8 V to 1.2 V. Then, the resistance at each V_{gt} level was plotted as a function of channel length as shown in Fig. 31.

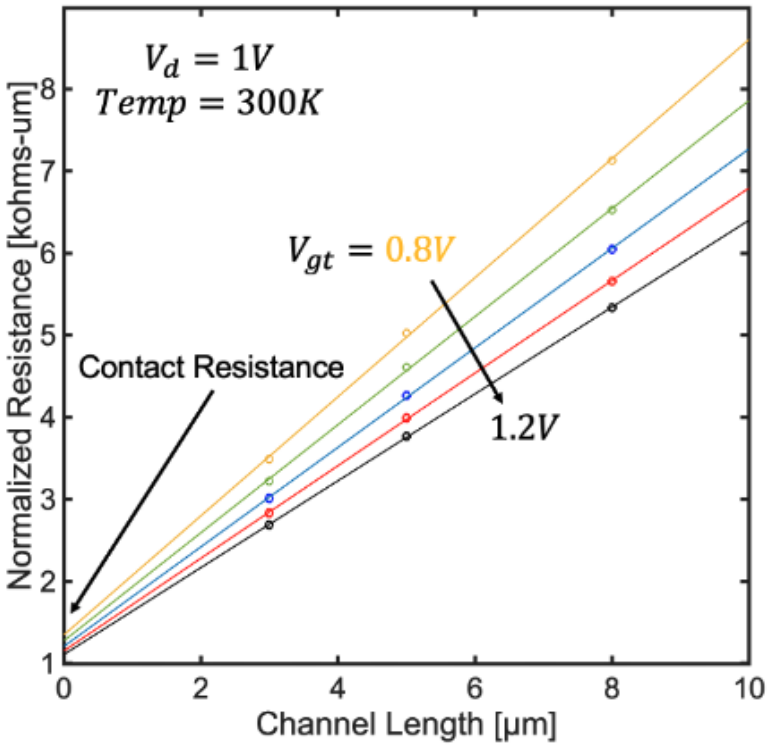

Fig. 31. Normalized resistance was calculated for three channel length at different V_{gt} levels, and plotted as a function of channel length, the contact resistance can be extracted.

To extract the contact resistance, we employ the resistance formula $R_{total} = R_{sh} * L + R_c$, where R_{sh} represents the sheet resistance of the graphene channel and R_c is the normalized contact resistance of the device. By extrapolating the resistance as a function of the channel length to the y axis where L = 0, we can determine the contact resistance at each V_{gt} level. This estimation is conducted under different sheet carrier densities, which are represented by $n_s = \frac{C_{ox}}{q}(V_g - V_{dirac})$. These values of contact resistance at various V_{gt}

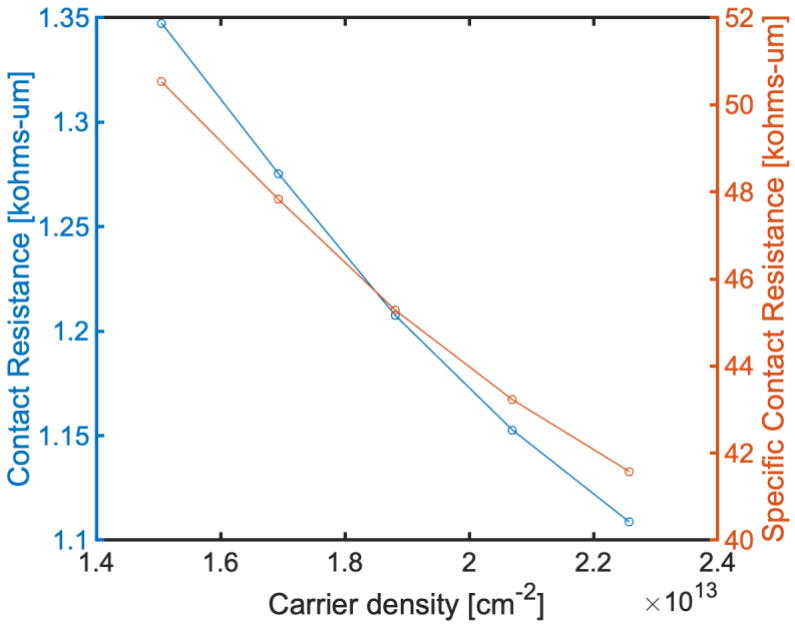

Fig. 32. The extracted contact resistance and the specific contact resistance at room temperature T = 300 K as a function of the sheet carrier density, which correspond to five different V_{gt} levels.

levels and sheet carrier densities are then plotted as a function of sheet carrier density, depicted by the blue curve in Fig. 32. It's evident from the plot that the contact resistance decreases as the sheet carrier density increases, primarily due to the improved conductivity associated with higher carrier concentrations. This phenomenon underscores the crucial role of carrier density in shaping the behavior of the contact resistance.

Furthermore, we evaluated the specific contact resistance (R_{sp}), calculated using the formula $R_{sp} = R_c * W * \frac{A}{L}$, where R_c represents the contact resistance normalized to the width. The results of this calculation were plotted as the function of sheet carrier density, and these values are represented by the orange curve in Fig. 32.

In the analysis, the sheet resistance of the channel is determined by calculating the slope of each curve in Fig. 31. Additionally, mobility, after factoring out the influence of contact

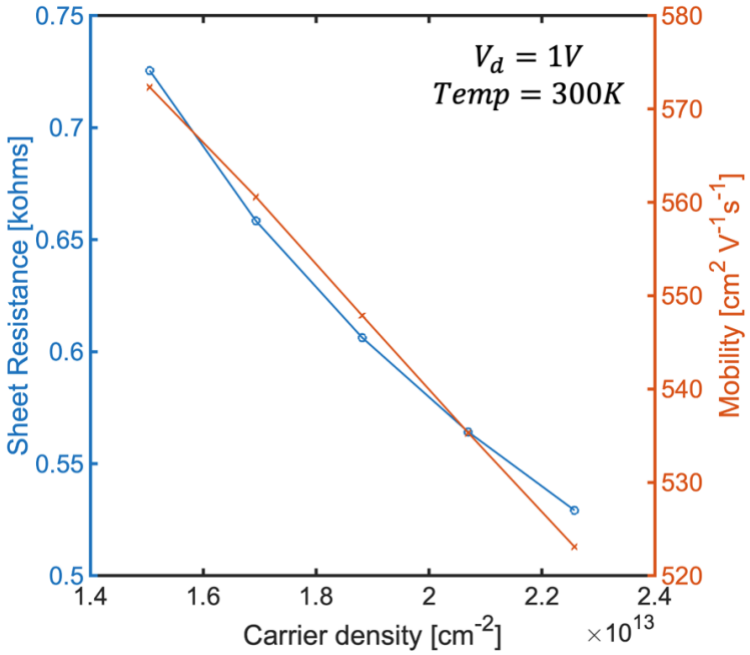

Fig. 33. The extracted sheet resistance of the channel at room temperature T = 300 K and the mobility as a function of the sheet carrier density.

resistance, is calculated using the equation $\mu = \frac{1}{qn_s R_{sh}}$ for each fixed sheet carrier density level. The results are presented in Fig. 33, where the sheet resistance is represented in blue, and the mobility is depicted in orange as a function of carrier density. The sheet resistance exhibits a decline as carrier density increases, reflecting the improvement in conductivity with a higher carrier concentration. In contrast, the mobility of the channel decreases as carrier density rises, indicating increased scattering due to the greater number of carriers. This observation emphasizes that the effect of elevated sheet carrier density on enhancing conductivity outweighs the impact of increased scattering.

The actual graphene channel resistance at each channel length can be calculated by using total resistance subtracted by the extracted contact resistance at each channel length. In Fig. 34, the graphene channel resistance is plotted as a function of the sheet carrier

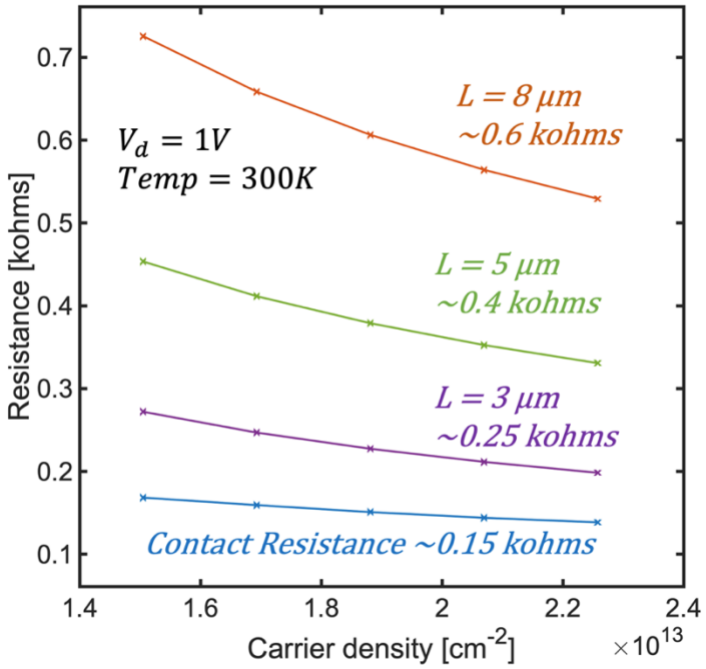

Fig. 34. The comparison between the ohmic contact resistance level and the graphene channel resistance levels at each different channel length.

density along with the level of the contact resistance. It's evident that the level of channel resistance is notably higher than the contact resistance observed in ohmic contacts lacking an insulator as a tunneling barrier. As mentioned in the previous section, this difference in resistance gives rise to the conductivity mismatch issue, which, in turn, significantly degrade the efficiency of spin injection the retention of spin information in LSV devices.

Consequently, the addition of a tunneling barrier becomes imperative to transform the ohmic contact into a Schottky barrier. Furthermore, it's essential to ensure that the contact resistance is adjusted to a level that aligns closely with the channel resistance. This critical aspect will be explored further in the next chapter.

5.3 Temperature Dependence

The same set of measurements was conducted across a range of temperature levels from 10 K to 300 K. The methods used earlier allowed for the extraction of sheet resistance and mobility at each temperature level, and the results have been visualized in Fig. 35.

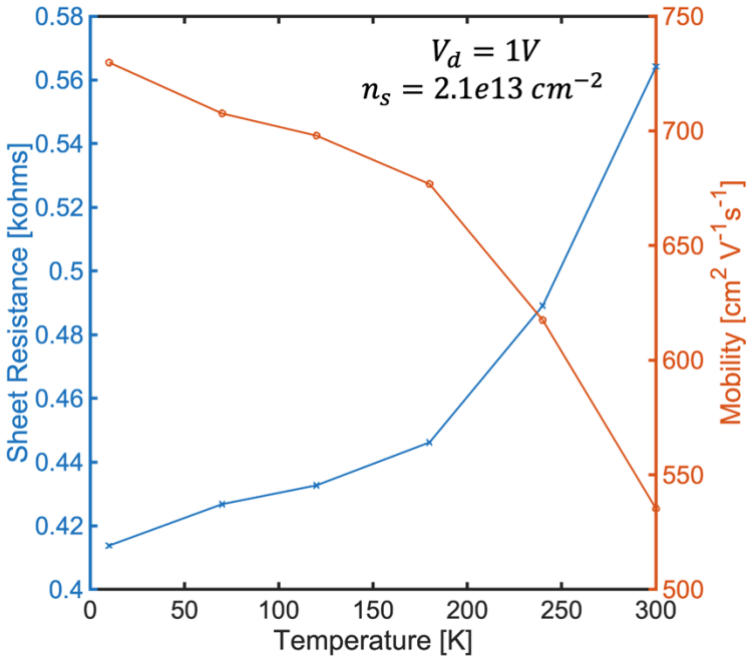

Fig. 35. The comparison between the ohmic contact resistance level and the graphene channel resistance levels at each different channel length.

Notably, the mobility demonstrates an upward trend as the temperature decreases. This phenomenon can be attributed to reduced phonon scattering within the channel, a conclusion consistent with our findings in the case of ultra-thin FDSOI devices. The improved mobility at lower temperatures also contributes to a reduction in the sheet resistance of the channel. This observation underscores the importance of temperature in shaping the electrical characteristics of the device, with lower temperatures facilitating more efficient charge transport and less scattering-induced resistance.

Chapter 6

Tunneling Barrier Investigation

6.1 Magnetic Tunneling Junction (MTJ) Structure

The magnetic tunneling junction (MTJ) devices, which consists of the tunneling barriers sandwiched by two ferromagnetic contacts in between as shown in Fig. 36a, provide an effective means to investigate the contact resistance of the tunneling barrier.

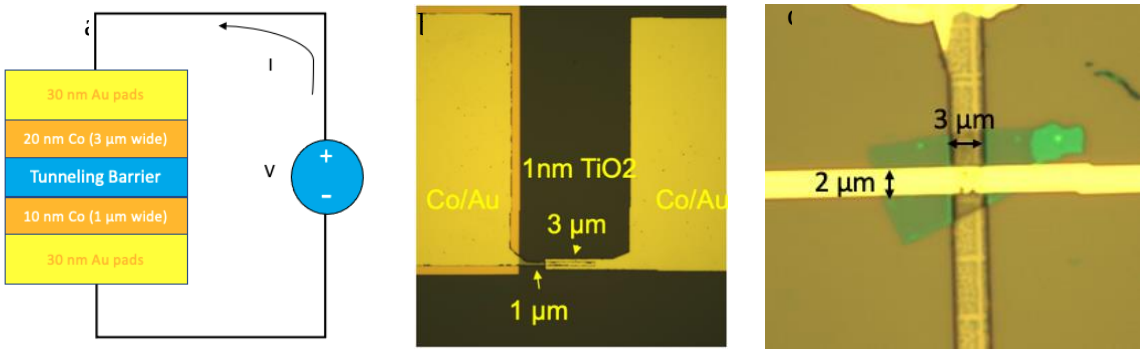

Fig. 36. a. The test structure for the contract resistance of the MTJ. b. The microscopy photo of the MTJ structure with Co contacts and 1nm TiO_2 tunneling barrier. c. The photo of the MTJ device with Co contacts and a few layers hBN as tunneling barrier.

Typical materials employed as tunneling barriers in spintronic devices encompass Al_2O_3, MgO, TiO_2, and hexagonal Boron Nitride (hBN). These materials are widely utilized due to their desirable properties in facilitating tunneling and spin-polarized transport. In addition, commonly used materials for the ferromagnetic contacts include Cobalt (Co), Iron (Fe), and Permalloy ($Ni_{81}Fe_{19}$), which are selected for their favorable magnetic characteristics.

In my research, I specifically investigated MTJ devices featuring Cobalt (Co) contacts with Titanium dioxide (TiO_2) and hBN as the tunneling barriers. These configurations,

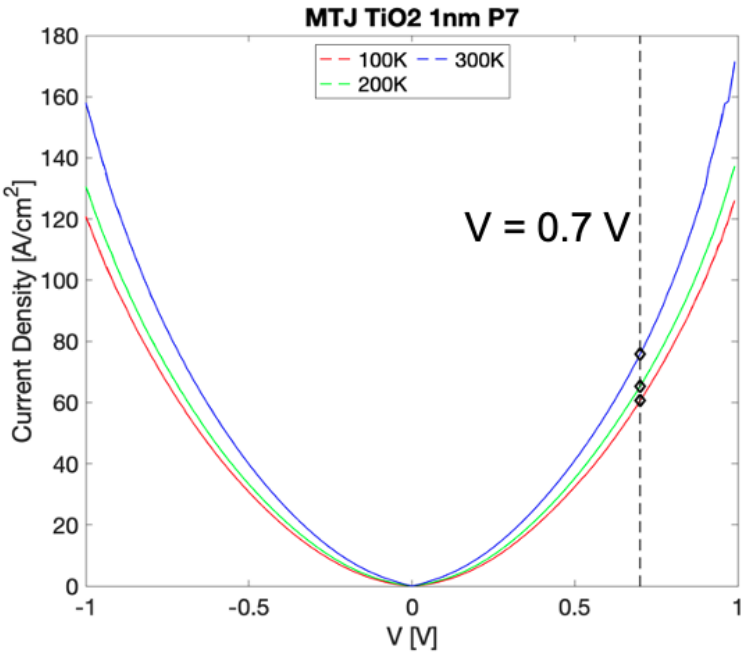

Fig. 37. Current Density as a function of voltage applied on the junction at various temperature levels for the MTJ with TiO2 as tunneling barrier.

depicted in Fig. 36 b and c, served as the focal points of our study, allowing for a detailed exploration of contact resistance.

The widths of the top and bottom electrodes are intentionally varied, with the bottom electrode measuring 1 µm for the TiO_2 device (3 µm for the hBN device), while the top electrode is 3 µm for the TiO_2 device (2 µm for the hBN device). This difference in electrode width serves a specific purpose: to induce distinct coercivity levels in these contacts within the LSV devices. Coercivity determines the external in-plane magnetic field required to switch the magnetic orientation in these contacts. By having different coercivity levels, we create conditions for achieving either parallel or antiparallel configurations that correspond to the spin orientations in the two contacts as we sweep the external magnetic field. This feature is of paramount importance in the functionality of

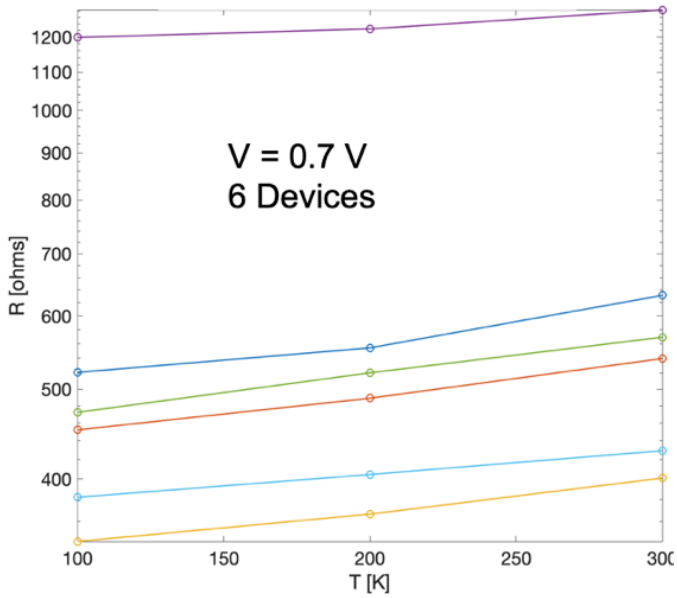

Fig. 38. The total resistance of the junction extracted at a fixed voltage level 0.7 V for 6 different devices.

LSV devices, as it facilitates the control and manipulation of spin orientations. Moreover, differing coercivity can also be achieved by utilizing different ferromagnetic materials for the top and bottom electrodes. For example, varying coercivity levels have been realized by constructing the top electrode with Cobalt (Co) and the bottom electrode with Iron (Fe) [82]. This strategic use of materials allows for further tailoring of the magnetic behavior of the device to meet specific requirements and objectives.

The electrical measurements I_d-V_g were performed on both MTJ devices at various temperatures to extract the total resistance across the junction with the materials as the tunneling junction. The I_d-V_g results at three different temperature levels (100 K, 200 K and 300 K) for the MTJ with the 1 nm TiO_2 are plotted in Fig. 37. Subsequently, the total resistance of the junction was determined at a fixed voltage level (V = 0.7 V) and plotted in Fig. 38 as a function of the temperature for 6 devices. Notably, the total resistances of

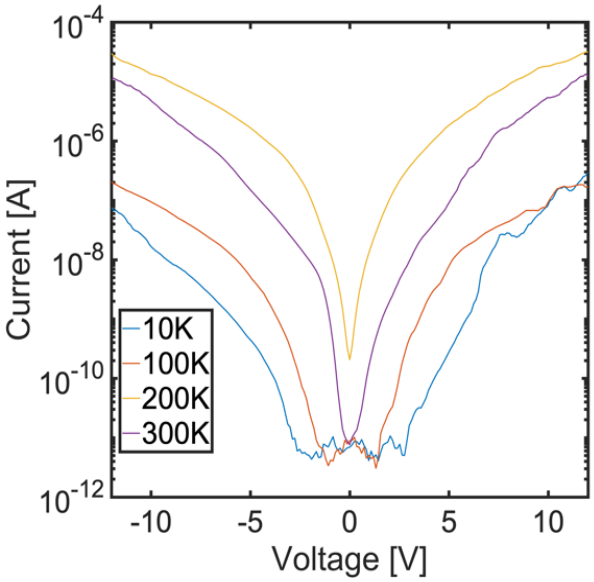

Fig. 39. Current as a function of voltage applied on the junction at various temperature levels for the MTJ with hBN as tunneling barrier.

the junctions are distributed around 500 ohms for devices incorporating 1 nm TiO_2 tunneling barrier and 1μm width contact.

Fig. 39 is presenting the measured current as a function of the voltage applied on the hBN MTJ device for four temperature levels from 10 K to 300 K. The total resistance across the junction was extracted for each temperature at a fixed voltage level at V = 6 V. Subsequently, the extracted resistances are depicted in Fig. 40, and it's worth noting that the resistance levels are several orders of magnitude higher compared to the MTJ device featuring a 1 nm TiO_2 tunneling barrier.

There are several potential explanations for this marked difference. The first reason pertains to the quality of the junction and the hBN flake, which may not be flawless, and the contacts may not be perfectly clean. The second possible factor contributing to the higher resistance is the thickness of the hBN flake, which has been confirmed to be around

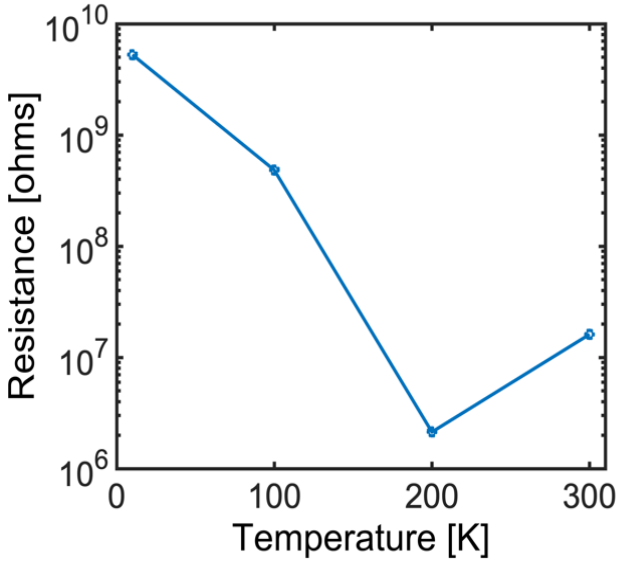

Fig. 40. The total resistance of the junction extracted at a fixed voltage level 6 V.

10 nm through AFM analysis. This thickness equates to approximately 26 layers of hBN, and it is likely the primary factor responsible for the significantly elevated resistance observed in the junction compared to the 1 nm TiO_2 configuration.

6.2 Conclusion on Tunneling Barrier Investigation

As observed in Fig.34, the contact resistance with the ohmic contact is approximately 0.15 kohms, a value significantly lower than the graphene channel resistance. This difference gives rise to the conductivity mismatch issue, which can be effectively resolved by introducing a tunneling barrier beneath the ferromagnetic contacts to enhance spin injection efficiency.

In the specific case of a channel length of 8 µm, the channel resistance approaches 0.6 kohms. To rectify the mismatch issue, the tunneling barrier should offer a resistance close to 0.5 kohms. Hence, TiO_2 emerges as a superior choice for the tunneling barrier compared to hBN for several reasons. First and foremost, a 1 nm TiO_2 barrier provides a resistance

of approximately 0.5 kohms, aligning perfectly with the 8 μm graphene channel resistance and effectively mitigating the conductivity mismatch.

Secondly, the fabrication process for TiO_2 involves metal deposition or sputtering, enabling precise control over the resulting thickness using specialized equipment. In contrast, hBN presents greater challenges in terms of fabrication and controlling the number of layers in the tunneling barrier, particularly within the current laboratory setup.

Therefore, TiO_2 stands out as the superior choice for a tunneling barrier, offering advantages in both contact resistance and fabrication control, ultimately addressing the conductivity mismatch issue in LSV devices more effectively than hBN.

CHAPTER 7

CONCLUSION

Over the past seven decades, silicon has been the key component of the semiconductor industry, serving as the primary channel material. The evolution of semiconductor device structures has been developed from planar designs to the advent of more advanced architectures, including fully-depleted silicon-on-insulator (FDSOI) and fin-field-effect-transistors (FinFETs). However, the continuation of Moore's Law and the constant push to scale down device dimensions, has resulted in a surge in research towards alternative materials, including 2D materials. Commonly studied 2D materials include transition metal dichalcogenides (TMDs) and graphene, which offer intriguing prospects for the next generation nanoscale devices.

To advance the understanding of transport properties in nanoscale devices based on both silicon and 2D materials, and to explore their potential applications in the realm of spintronics, my Ph.D. works started with an investigation on the nanoscale FDSOI devices, which was assisted by the Landauer theory and the virtual source (VS) model. Here, commercial ultra-thin nanoscale FDSOI devices were characterized from room temperature (300 K) down to cryogenic temperatures (10 K). My research focused intently on the quasi-ballistic transport regime and considered the significant impact of the back-gate biasing.

Through the course of my study on FDSOI, different components of resistance were analyzed including the channel, ballistic, and series resistance as we vary channel length and temperature. Our experimental analysis was thoroughly supported by mathematical

modeling, which allowed to calculate and study mobility as a function of temperature and channel length in the quasi-ballistic regime. In parallel, other key parameters related to transport were also extracted, including mean-free-path and the ballistic ratio. My research uncovered the characteristics of quasi-ballistic transport in these nanoscale FDSOI devices, indicating the potential for high performance, especially at low temperatures compared to bulk CMOS FETs. The temperature-dependent analysis provided valuable insights into the contributions of both phonon and ionized impurity scattering to the overall resistance. Moreover, I proposed new techniques to account for temperature and back-gate bias in the virtual-source (VS) modeling approach for nanoscale transistors. These resulted in good alignment between VS model and experimental data across various range of temperatures and back-gate bias, underscoring the robustness and applicability of the proposed modeling approach.

While the study was primarily conducted on silicon-based devices, its implications extend beyond this realm. The knowledge gained from studying nanoscale devices with bulk semiconducting channels (i.e., silicon), paves the way for a deeper understanding of devices using emerging materials, such as graphene, which exhibits exceptionally high mobility. Accordingly, nanoscale graphene-based devices also function within the ballistic or quasi-ballistic regime.

The transition from silicon-based structures to 2D material-based structures represents a shift in the semiconductor landscape soon. This transition has led to a new focus on the development of graphene-based electrical and spintronic devices, such as non-local lateral spin valves (LSVs). Within this context, my research investigated key components of

graphene-based LSVs, including the graphene channel, ohmic contacts, and tunneling barriers, with a view to advancing the understanding of the behavior and performance of the graphene-based spintronics.

Initial investigations into graphene-based FETs revealed the impact from trapped charges at the interface between the graphene channel and the dielectric film. These trapped charges induced a pronounced influence on the transport properties, raising questions about the nature of this impact. My research started on a thorough exploration of this effect, with a particular emphasis on graphene FETs with thin high-k gate dielectrics (HfO_2). This detailed analysis uncovered the buildup of the charge impurities locating at the gate dielectric material interfacing the graphene channel. These impurities, in turn, had impact on the electrostatic phenomena and contributed to the degradation of transport (i.e., degraded mobility/conductivity). The findings pointed to the presence of trapped-charge-induced (charged impurity) scattering, which serves as a significant factor degrading the conductivity, mobility, and mean-free-path in graphene-based devices. This finding has contributed to the development of graphene-based non-volatile memory, memristive, and neuromorphic devices, as well as graphene FETs.

In addition to the impact of trapped charge impurities in the graphene-based channel, my research also investigated other pivotal components of LSV devices, including contact resistance, channel resistance, and tunneling barriers. The objective was to uncover and mitigate the challenges related to conductivity mismatch, which is a common issue in spintronic devices. The study revealed that resistance of the graphene channel was larger in comparison to the resistance of ohmic contacts between the metal and graphene. This

observation highlighted the existence of the conductivity mismatch issue in graphene-based LSV devices.

Pushing towards more efficient graphene-based LSV and other spintronic applications led me to investigate tunneling barriers with ferromagnetic contacts, which provide a barrier to help increase contact resistance and resolve the mismatch with the graphene channel resistance. I examined the performance of two specific materials -titanium dioxide (TiO_2) and hexagonal Boron Nitride (h-BN) as tunneling barriers with cobalt (Co) contacts. The results of the investigations indicated that a 1 nm TiO_2 tunneling barrier in conjunction with Co ferromagnetic contacts exhibited a consistent resistance level that matched closely with the resistance of the graphene channel. This finding has significant implications for the development of graphene-based LSV devices and other spintronic applications, positioning them as promising candidates for future memory and logic device technology.

In summary, my comprehensive investigations have led to a more profound understanding of the transport properties and performance characteristics of nanoscale devices, spanning both silicon-based and 2D material-based systems. The deeper understanding of the quasi-ballistic charge transport in nanoscale FDSOI devices and the impact of the trapped charge impurities in graphene-based devices are noteworthy contributions to the field of semiconductor research. Furthermore, my work in investigating the conductivity mismatch issue in spintronic devices brings me a step closer to studying the graphene-based LSVs and other spintronic applications.

These advancements have significant implications for future memory and logic device technology, opening doors to the development of more efficient and effective devices. As

we look ahead, my Ph.D. research presented here underscores the profound interesting and unique properties of the novel materials and the device design on the performance of emerging nanoscale technologies. It offers valuable insights for future advancements in the field of semiconductor research and provides a robust foundation for continued exploration into the potential of 2D materials in the world of electronics and spintronics.

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