Investigation of Emerging Power Electronics Technologies in EV Applications

by

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ABSTRACT

Due to the reduced fuel usage and greenhouse emission advantage, the sales of electric vehicles (EV) have risen dramatically in recent years. Generally speaking, the EVs are pursuing higher power and lighter weight, which requires higher power density for all the power electronics converters in the EVs. To design higher density power converters, three key emerging power electronics technologies are investigated in this study.

First, the PCB-based magnetics are beneficial for improving the power density due to their low-profile structure. However, the high winding capacitance is considered one of the significant drawbacks of PCB-based magnetics. In this study, a novel winding structure is proposed to cut down the winding capacitance by 75% with little compromise of the winding loss.

Second, the synchronous rectifiers (SR) are usually utilized to improve the system efficiency and power density compared with the conventional diode bridge rectifiers for the AC/DC stage in the power converters. The SRs are desired to be turned off at current zero-crossing to generate a minimal loss. However, the precise current zero-crossing detection is very challenging in high-frequency and high-power-density converters. In this study, a high-dv/dt-immune and parameter-adaptive SR driving scheme is proposed to guarantee the zero-current switching (ZCS) of SRs in various operating conditions and improve the system efficiency by 1.23%.

Finally, Gallium Nitride (GaN) semiconductors are considered less lossy than Silicon (Si) semiconductors. However, the voltage rating of the commercial GaN HEMTs is limited to 600/650 V due to the lateral structure, which is not suitable for the 800 V or higher dc-link voltage EV systems. Stacking the low-voltage rating devices is a straightforward approach to sustain higher dc-link voltage. However, unbalanced

voltage sharing can occur, which can damage the low-voltage rating devices in the stack. In this study, a novel active current source gate driver is proposed to suppress the over-voltage of the stacking devices below 10% for all operating conditions without sacrificing switching speed or switching energy.

The above emerging power electronics technologies are investigated thoroughly in the dissertation. The proposed approaches are practical for improving power converters' density in future EV applications.

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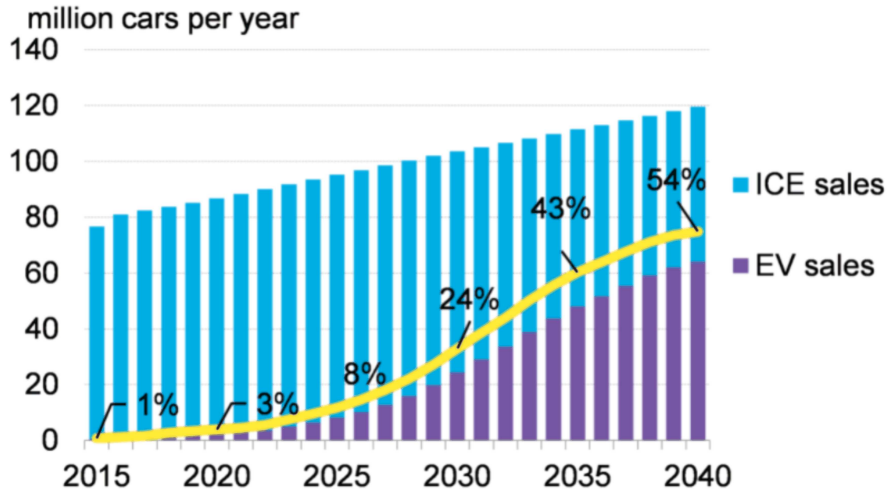
Chapter 1

INTRODUCTION

1.1 Overview of Power Electronics Converters in EVs



Source: Bloomberg New Energy Finance

Figure 1.1: Annual Global Light-duty Vehicle Sales (from Bloomberg New Energy Finance).

All-electric vehicles (EVs), also referred to as battery electric vehicles, have an electric motor instead of an internal combustion engine (ICE). Due to the reduced fuel usage and greenhouse emission advantage, the sales of EVs have risen dramatically in recent years [2]. The annual global light-duty vehicle sales are shown in Fig. 1.1. It is estimated that EVs will account for 54% of all new light-duty vehicle sales globally by 2040.

The U.S. Department of Energy presents the key components of an all-electric car, which is shown in Fig. 1.2. Based on this structure, there are three key power

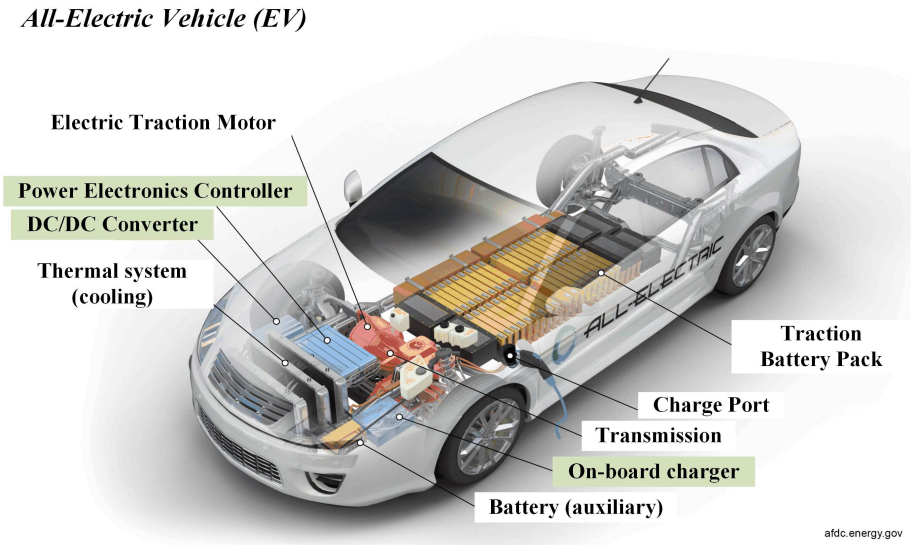


Figure 1.2: Key Components of an All-electric Car (from U.S. Department of Energy Website).

electronics converters inside an EV, which include the power electronics controller (traction inverter), the on-board charger and the DC/DC converters. There are also crucial power electronics converters outside an EV, such as the off-board charger (or fast battery charger) [3], which will benefit from the emerging technologies investigated in this study as well.

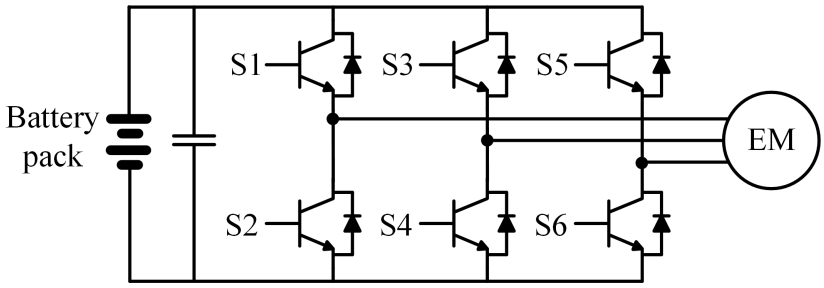


Figure 1.3: Two-level Voltage-source Three-phase Inverter for EV Traction Drive.

A traction inverter is a unit that manages the flow of electrical energy delivered by the traction battery, controlling the speed of the electric traction motor and the torque it produces. In terms of the topology for EV traction inverters, the most popular one is the two-level voltage-source three-phase inverter, which is shown in

Fig. 1.3. Because of the mature, robust, and reliable technology [4], this topology is dominated in the commercial EV traction inverters. For the power semiconductor devices, most of the manufacturers still select Si IGBTs due to the low cost and mature technology. However, with the fast growth of wide-band-gap (WBG) devices, the industry has adopted the SiC-based traction inverter. For example, Tesla Model 3 is equipped with a full SiC-based traction inverter [5]. The U.S. Department of Energy sets aggressive targets for the power density of the electric traction drive system. Based on their electrical and electronics technical team roadmap in 2017, the power density of the traction inverter should reach 100 kW/L (1638.7 W/inch^3) by 2025.

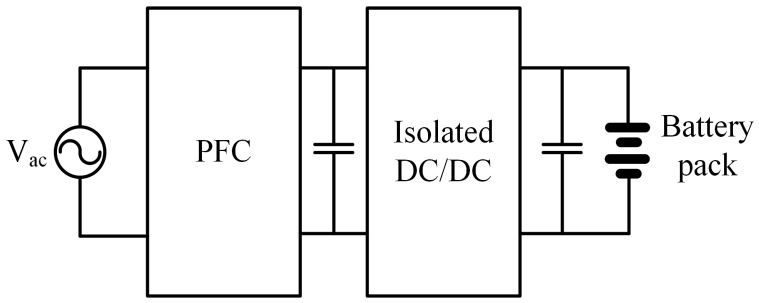


Figure 1.4: The Structure of a Typical Isolated Two-stage EV On-board Charger.

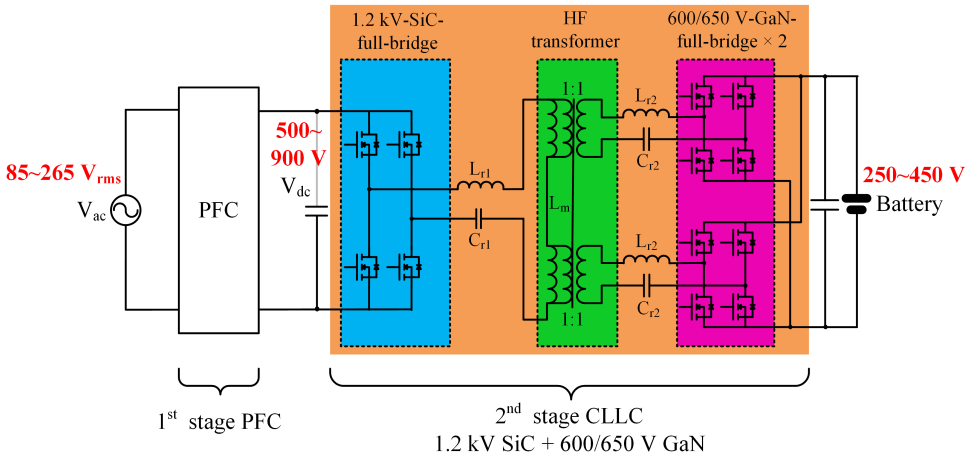


Figure 1.5: Example of a 6.6 kW/500 kHz WBG-based EV OBC.

The on-board charger (OBC) is utilized to take the incoming AC electricity supplied via the charge port and convert it to DC power for charging the traction battery. It also communicates with the charging equipment and monitors battery characteristics such as voltage, current, temperature, and state of charge while charging the pack. A large variety of topologies can be employed for EV on-board charger [2]. The on-board chargers can be categorized into isolated /non-isolated, unidirectional/bidirectional, single-stage/two-stage, and different power levels (level-1, level-2) [2]. The structure of a typical isolated two-stage EV on-board charger is shown in Fig. 1.4. The first stage is a power factor correction (PFC) converter. The second stage is an isolated DC/DC converter, which is normally used to regulate the output voltage and provide galvanic isolation. Common candidates for the isolated DC/DC stage include series resonant converter (SRC), phase-shifted full-bridge converter (FSFB) and LLC/CLLC resonant converter [6]. Both SRC and FSFB have difficulties in terms of efficiency and voltage regulation for light load conditions [7–10]. The LLC/-CLLC resonant converters are able to obtain zero-voltage switching (ZVS) and good voltage regulation for full load range [11–19]. Meanwhile, the secondary rectifiers can achieve zero-current switching (ZCS). With the employment of the synchronous rectifiers (SR), the efficiency can be maintained very high at the resonant frequency. In particular, the CLLC resonant converter acquires a symmetrical gain curve that guarantees similar operating frequency and power losses at both power flow directions. The major drawback of the LLC/CLLC resonant converter is the drop of efficiency when the operating frequency is far from the resonant frequency. To improve the system efficiency and the density of passive components, the variable PFC dc-link solution which adjusts dc-link voltage to minimize the gain variation in the LLC/-CLLC resonant converter is adopted [20–24]. This approach can achieve a narrow switching frequency range at wide battery voltage. The WBG devices also have in-

disputable advantages for the on-board chargers due to their capability of operating at a very higher frequency and the low-loss characteristics. With the employment of soft-switching topologies, such as LLC/CLLC resonant converters, the switching frequency can be pushed to several 100 kHz or even MHz levels. The significantly increased switching frequency is beneficial for cutting down the size of the passive components. Meanwhile, due to the low-loss characteristics of the WBG devices, the heat sinks can be kept small. Therefore, the power density can be greatly improved with the employment of the WBG devices. A good example of 6.6 kW/500 kHz WBG-based high-power-density EV OBC is shown in Fig. 1.5 [25]. The CLLC resonant converter is selected for the isolated DC/DC stage to achieve the bidirectional power flow. As mentioned previously, the variable dc-link strategy is utilized to reduce the operating frequency range of the CLLC resonant converter and significantly improve the efficiency of the isolated DC/DC stage. With the reasonable compromise of the efficiency for the PFC stage, the system overall efficiency is still greatly improved. Meanwhile, with the very high switching frequency (500 kHz), the system power density is significantly improved as well. Similarly, the U.S. Department of Energy sets targets for the power density of the on-board charger. Based on their electrical and electronics technical team roadmap in 2017, the power density of the on-board charger should reach 4.6 kW/L (75.4 W/inch^3) by 2025.

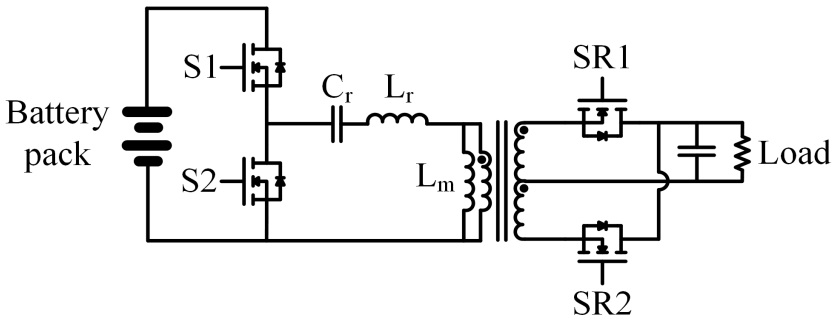


Figure 1.6: The Schematic of LLC Resonant Converter.

The DC/DC converters transfer higher-voltage DC power from the traction battery pack to the lower-voltage DC power needed to run vehicle accessories and recharge the auxiliary battery. Since the voltage conversion ratio is high (e.g. from 380 V to 12 V), the transformer is typically utilized to achieve the high step-down ratio. One of the most attractive topologies for this application is LLC resonant converter [26], as shown in Fig. 1.6. As discussed previously, LLC resonant converter can achieve ZVS for the entire load range. The switching frequency of the converter can be upgraded to the MHz level with the employment of WBG devices, so the size of the passive components will be significantly reduced. Meanwhile, the secondary side (low-voltage side) output current is typically high for this application, so the synchronous rectifier (SR) is usually utilized to reduce the conduction loss compared with the conventional diode bridge rectifier. Therefore, the size of the heat sinks can be reduced as well. Again, the U.S. Department of Energy sets targets for the power density of the DC/DC converters. Based on their electrical and electronics technical team roadmap in 2017, the power density of the DC/DC converter should reach 4.6 kW/L (75.4 W/inch^3) by 2025.

1.2 Challenges in Magnetics Design for High Power Density Converters

The improvement of the power density is a significant task for the future development of EVs.

The magnetic components typically occupy a large portion of the volume in a power electronics converter. The magnetic components in EV power converters typically include the isolation transformers, filter inductors, boost inductors, resonant inductors, and common mode (CM) chokes. Conventional wire-wound magnetics are usually bulky and labor-intensive. PCB-based magnetics (planar magnetics) are beneficial for improving the power density of the converters due to their low-profile

structure. In particular, PCB-based magnetics are very suitable for the isolation transformer because the leakage inductance and ac winding loss can be minimized with the interleaved winding structure (flux-cancellation). The advantages of the PCB-based magnetics are not strong for the inductors because the magnetomotive force and magnetic flux generated by each turn is added not subtracted.

For the high frequency operating conditions, the planar transformer stands out for the following reasons.

First, the PCB trace windings are extremely thin and the number of turns is very few. Skin effect and proximity effect are significantly diminished for the planar transformer, especially at high frequency where Litz wire becomes less attractive. Hence, planar transformer has lower ac winding loss. Second, the better coupling in geometry minimizes the leakage inductance and the ac winding loss. Third, the low profile characteristics and the high filling factor make the power density of the planar transformer very high. Fourth, the better insulation property of the FR4 brings space saving for the high voltage operation. Fifth, the PCB winding has better thermal dissipation which enables the PCB winding to sustain higher current density. Last but not least, the fixed and reliable winding structure makes the parasitic parameters controllable. The fabrication and assembly process is much easier compared with Litz-wire wound transformer. It is good for mass production.

As is shown in Fig. 1.7, the low-profile planar magnetic components reduce the height of the power converter. The box volume of the converter is significantly improved. As a result, the power density of ASU's 3.3 kW CLLC resonant converter [27] is almost four times that of Infineon's 3 kW LLC resonant converter that employs the conventional Litz-wire magnetic components. Despite of the advantages, there are still several challenges for the successful appliance of the planar transformer, especially for the high-power-density applications.

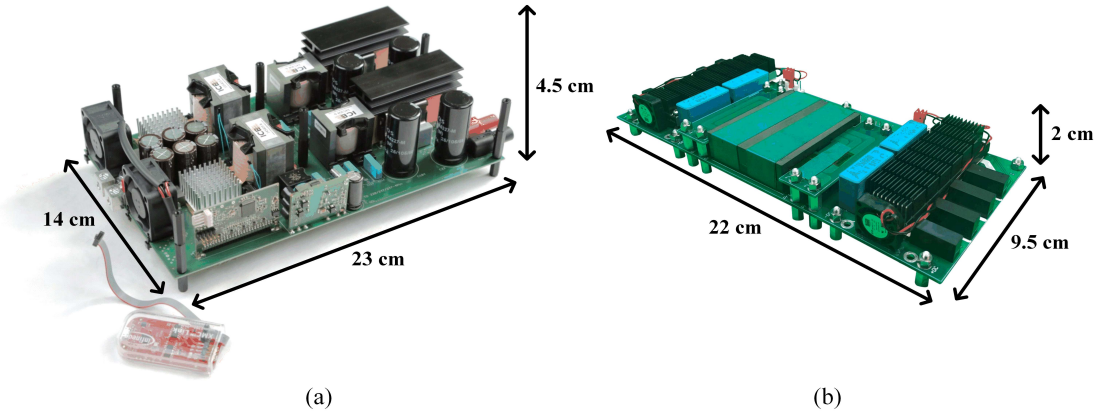


Figure 1.7: (a) Infineon's 3 kW LLC Resonant Converter with Litz-wire Transformer. (b) ASU's 3.3 kW CLLC Resonant Converter with Planar Transformer.

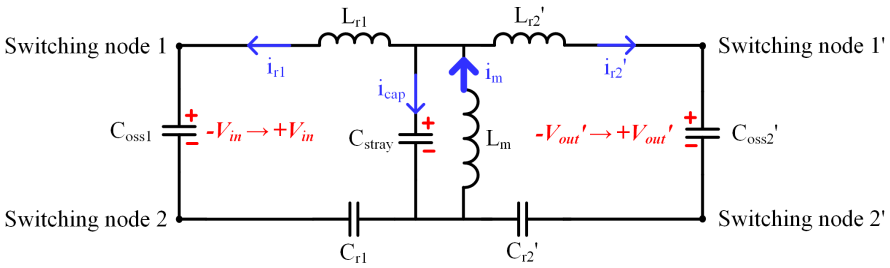


Figure 1.8: Equivalent Circuit of CLLC Resonant Converter During the Dead-time.

First, the intra-winding capacitance (the stray capacitance between turns of each winding) is high compared to wire-wound transformer, because of the large overlapping area and small distance between the adjacent turns. This will affect the soft-switching, transformer and converter efficiency and the waveform quality, which will be explained as follows. The ZVS will be harder to achieve, because the magnetizing current (i_{m}) thus will not only flow to charge and discharge the device junction capacitance (C_{oss1}, C'_{oss2}) but also be distributed into the intra-winding capacitance (C_{stray}) during the dead-time, as shown in Fig. 1.8. The C_{stray} represents the total winding stray capacitance referred to the primary side and it can be seen as an equivalent intra-winding capacitor. Although a higher magnetizing current can be applied

but more conduction loss will be produced and the system efficiency drops. The voltage regulation will be affected as well [28], which results in wider operating frequency range. The transformer current quality and utilization will be degraded due to the dv/dt introduced resonance between the intra-winding capacitance and the resonant inductor. To address this challenge, the authors in [28] proposed the strategy of placing the turns in a specific fashion to minimize the electric field intensity. Meanwhile, the permittivity is reduced by inserting the Kapton tape between the adjacent turns of each winding. However, complicated inter-board connections are required and it is labor intensive to insert the Kapton tapes between different boards, which makes this winding structure difficult to manufacture and less cost-effective.

The second challenge for the planar transformer is the high inter-winding capacitance (the stray capacitance between different windings). Usually, interleaving of primary and secondary winding is adopted for multi-winding configuration [29] to reduce the leakage flux and the corresponding ac winding loss. But this will result in large overlapping area and small distance between primary and secondary windings, which is the root cause of the high inter-winding capacitance. The inter-winding capacitance is usually a major path for the common-mode (CM) current [30–32]. The dv/dt induced CM current will flow into the secondary side and then enter the earth ground and will be seen by the LISN eventually. In order to meet the conducted EMI standard, a larger EMI filter is required to bypass the CM current flowing into LISN, which greatly impacts the system power density [7]. The common approaches to suppress the CM current due to the high inter-winding capacitance can be grouped into two categories. The first one is to use passive cancellation and balance technique [33–36]. Basically, the principle is to create an additional 180^{o}-phase-shifted CM current with the same magnitude to cancel the original CM current through the inter-winding capacitance. However, this method requires additional passive components and it is

sensitive to the tolerance. The second category is to employ shielding layers between the primary winding and secondary winding [37, 38]. The shielding layer is connected to the primary side ground and has the same layout with the secondary winding. The CM current from the primary side will flow into the shielding layer and then circulate back to the primary side ground. The CM current from the secondary side will circulate back as well, because there is no voltage potential difference between the secondary winding and the shielding layer. The major drawback of this method is the additional eddy current losses in the shielding layer. Actually, the above two mechanisms do not cut down the physical inter-winding capacitance between the primary winding and secondary winding. They either compensate or bypass the CM current. In this study, the physical inter-winding capacitance is significantly reduced by increasing the distance between the primary winding and the secondary winding.

The third challenge for the high-power-density planar transformer is the thermal management. Planar transformer winding usually sustains higher current density compared with Litz-wire wound transformer [29, 39]. In particular, for EV on-board charger (OBC), the transformer has the characteristics of high volt-second and low current. The maximum volt-second and the maximum output dc current are compared with an example 1 kW/1 MHz 380 V-12 V LLC described in the literature [40], which is shown in Table 1.1.

The volt-second of EV OBC is 9.5 times of the volt-second of the 380 V-12 V LLC, while the output dc current is only 1/4 of the 380 V-12 V LLC. In general, the winding loss is not a dominant factor, hence, the winding width is not necessary to be over-designed to reduce the DCR of the winding. To save the footprint, the winding can be designed close to its thermal limited width. The FR-4 material has much lower thermal conductivity compared with copper. The thermal dissipation capability for PCB inner layers is much worse than the outer layers, because the heat generated

Table 1.1: Volt-second and Output Current Comparison Between 6.6 kW/500 kHz EV OBC and 1 kW/1 MHz 380 V-12 V LLC.

Parameters	6.6 kW/500 kHz EV OBC	1 kW/1 MHz 380 V-12 V LLC
Maximum volt-second	4.5×10^{-4} V·s	4.75×10^{-5} V·s
Maximum output dc current	22 A	83.33 A

in the inner layers needs to go through the low-thermal-conductive FR-4 material to reach the air. Researchers in [41–43] propose different methods of integrating resonant inductors into the transformer. Those methods can be grouped into two categories. The first mechanism is to use the air to conduct the leakage flux. The main drawbacks are the greatly magnified ac winding loss and the EMI issues caused by unconstrained magnetic fields. The second mechanism is to use magnetic material to conduct the leakage flux. In this method, the low-permeability magnetic shunt suffers from high core loss. In [23], the leakage flux is diverted into a third leg of the ferrite core. The extra loss is reduced to 15%∼17% of transformer total losses. To sum, the magnetic integration is a good approach to reduce magnetic component counts and improve the system power density, but it also makes the thermal management of the transformer harder. Therefore, an alternative approach is employed in this study to utilize external resonant inductors. The corresponding power losses are produced outside the transformer, so the thermal stress of the transformer is reduced. Moreover, by putting the windings only on the outer layers of the PCB through magnetic core reconfiguration, the thermal stress can be further released.

1.3 Challenges in Precise and Robust Gate Driving for Synchronous Rectifiers

For the power electronics converters in EVs, synchronous rectifiers (SR) are widely used in the AC/DC stage because the conduction loss and reverse recovery loss are significantly reduced compared with the conventional diode bridge rectifiers. However, the precise and robust gate driving for synchronous rectifiers (SR) is challenging in high-frequency and high-power-density converters.

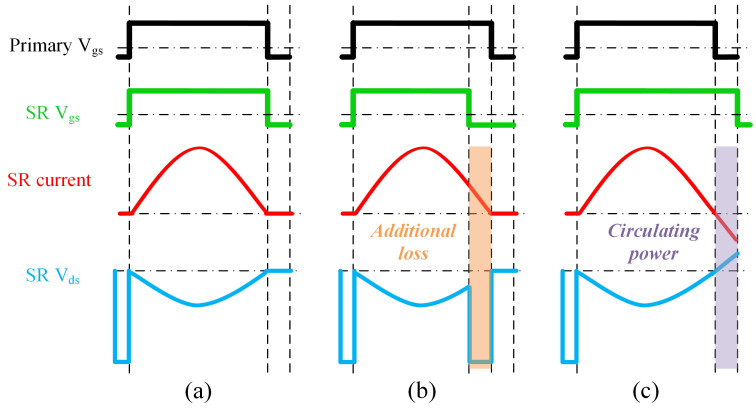


Figure 1.9: SR Current and Voltage Waveforms for Different Gate Driving Schemes. (a) SR ZCS Turn-off. (b) SR Early Turn-off. (c) SR Delayed Turn-off.

The SR is desired to be turned off exactly at the current zero-crossing moment (ZCS) to produce a minimal loss, as shown in Fig. 1.9(a). If the SR is turned off earlier than the current zero-crossing moment, the current will go through the reverse channel of the switch at the gate-off period. Since the voltage drop of the reverse channel at the gate-off period is significantly higher than the voltage drop on the R_{dson}, additional conduction loss will be produced, as shown in Fig. 1.9(b). If the SR is turned off later than the current zero-crossing moment, the current will change its direction and flow from the drain to the source of the device. This reverse current is the so-called circulating current which flows from the load to the source.

The circulating current will increase the current amplitude in the system and result in additional conduction loss as well, as shown in Fig. 1.9(c). Meanwhile, the circulating current is in the opposite direction of the magnetizing current. If the primary side switches are experiencing the dv/dt switching transient at this time, ZVS will be harder to achieve. It is because part of the magnetizing current is compensated by the circulating current. Therefore, it is very critical to achieve the zero current turn-off for the SR to guarantee the high efficiency of the system. It should be mentioned that, prior to the turn-on of the SR, the magnetizing current will flow through the reverse channel during the gate-off period if the dv/dt transient finishes. This is why a large negative V_{ds} occurs prior to the turn-on of the SR, as shown in Fig. 1.9. The magnetizing current is assumed to be much smaller than the load current, hence, the SR current is shown to be zero before the arrival of the turn-on signal.

A lot of efforts have been spent on investigating the SR driving schemes in the past. The open-loop SR driving is the simplest method [44–46]. However, it is hard to guarantee the accuracy, because the resonance inductance and capacitance may change for different load and different temperature conditions, which results in a changeable resonant frequency. The current transducer (CT)-based methods are employed in [47, 48]. Although CT is able to measure the SR current with good accuracy, the bulky size impedes its application for high power density designs. Meanwhile, at very high switching frequency ($\geq$500 kHz), the CT becomes very lossy and the extra loss produced in the CT will lower the system efficiency. Meanwhile, the parasitics in the CT (leakage inductance and winding stray capacitance) will degrade its accuracy at very high frequency. The Rogowski coil-based current sensing is another approach [49]. Since the Rogowski coil is open-circuited, the loss generated in the coil is minimal. However, the integral circuit is required to converter the sensed open-winding voltage to the current signal. Meanwhile, the Rogowski coil still belongs

to the additional current sensing element and consumes power. The SR drain-to-source voltage ($V_{\rm ds}$) sensing is another popular approach. Basically, this approach utilizes SR on-state resistance ($R_{\rm dson}$) as a shunt resistor and the sensed $V_{\rm ds}$ voltage reflects the current in the SR. Since this approach does not require any additional current sensing elements, it will not introduce extra losses and it is suitable for high power density applications. This approach has been employed in the off-the-shelf commercial SR drivers for Si device. Basically, the commercial SR drivers use two threshold voltages. When the sensed $V_{\rm ds}$ is more negative than the first threshold voltage, it reflects the conduction of the SR body diode (Si device). Then the SR driver outputs the turn-on signal. When the sensed $V_{\rm ds}$ drops to less negative than the second threshold voltage, the SR driver outputs the turn-off signal. However, there are several pain-points for commercial SR drivers. First, since the second threshold voltage is very close to zero (typically around 10 mV), it is very sensitive to the noise. Second, due to the inevitable parasitic inductance in the device package, the measured $V_{\rm ds}$ may lead the device current by a phase angle, which results in an earlier turn-off event. A carefully designed capacitive compensation circuit is proposed in [50]. However, the device package inductance and $R_{\rm dson}$ need to be determined in advance. Since the device $R_{\rm dson}$ is greatly affected by the junction temperature, the precision of the compensation circuit will be degraded at a wide junction temperature range. Third, since the commercial SR drivers are designed to drive Si device, zero turn-off voltage is utilized, which is not suitable to safely drive the low-threshold GaN device. Last but not least, the voltage rating of commercial SR drivers is usually below 200 V which is limited by the voltage rating of the blocking diode or the blocking FET. Therefore, the commercial SR drivers can not be directly utilized in the 250 V$\sim$450 V battery charger operating condition.

The digital adaptive SR driving scheme is proposed in [51, 52]. This adaptive

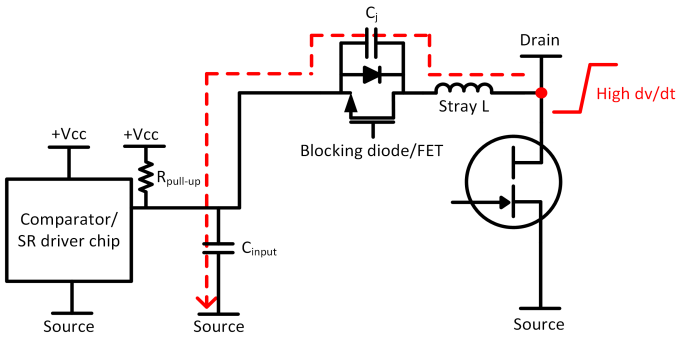


Figure 1.10: Displacement Current Path During the SR Drain-to-source Voltage Rising Transient.

driving scheme has been validated in a 1-kW 400 V/12 V LLC prototype with Si-based SRs. By adaptively tuning the SR on-state duration in the next control cycle based on the whether the body diode (for Si device) conducts, the body diode conduction time is minimized in a few switching cycles. This method only utilizes one threshold voltage. Once the sensed V_{ds} is more negative than the threshold voltage, which means the body diode of SR conducts, then the SR on-time is increased by a small interval in the next control cycle. Otherwise, the SR on-time is reduced by a small interval in the next control cycle. The turn-on moment of the SR is synchronized with its corresponding primary side switches. The advantages of this method are listed as follows. First, since the body diode voltage drop is usually much larger than the device R_{dson} voltage drop, there is a big clearance between the threshold voltage and zero, which makes this approach less sensitive to the noise. Meanwhile, this approach fits the GaN device even better, because the reverse channel voltage drop of GaN device during gate-off period is even larger. The threshold voltage can be designed even further away from zero. Second, this approach reaches the current zero-crossing moment by several steps, not by one step, hence, it is not affected by the voltage and current phase difference due to the parasitic inductance. Third, the sensing delay and

propagation delay are not critical. As long as the delayed signal is still within the detection zone of the controller in one switching cycle, the adaptive on-time tuning function will not be affected. However, this adaptive SR driving scheme is only verified in low-voltage and low dv/dt applications. The output voltage in [52] is only 12 V. Meanwhile, the junction capacitance of low-voltage high-current Si-based SR is in the nF range, so the dv/dt is only around 0.1 V/ns. The authors in [53] attempt to implement the adaptive driving scheme in high voltage and high dv/dt scenarios, but sufficient experimental validation is lacking. For GaN-based SR in EV OBC, the voltage and dv/dt are much higher than the case in [52]. The maximum battery voltage is around 450 V (can be even higher) and the dv/dt can exceed 10 V/ns. The increased voltage and dv/dt brings the following challenges for this approach.

First, a blocking diode or a blocking FET is required to block the high voltage from the comparator or the SR driver chip when the SR is off, as shown in Fig. 1.10. When the drain-to-source voltage of the SR rises, the junction capacitance of the blocking diode/FET needs to be charged to the output dc voltage. The input capacitance of the comparator/SR driver chip and the junction capacitance of the blocking diode/FET form a capacitive voltage divider. Therefore, the input voltage for the comparator/SR driver chip may exceed the maximum allowable voltage during this transient. Similar phenomenon will occur during the SR dv/dt falling transient as well. In [54], an external capacitor is added to increase the input capacitance of the SR driver chip to avoid the over-voltage, but this approach will introduce significant sensing delay. Second, the high dv/dt can induce significant oscillation between the network capacitance and the loop stray inductance. The oscillation can greatly distort the sensed V_{ds} voltage.

To achieve a fine-controlled synchronous gate driving of GaN-based SR in a high dv/dt operating condition, this study presents a complete driving scheme. First, a

novel drain-to-source voltage sensing circuit is proposed to address the over-voltage and oscillation issues caused by the high dv/dt. A low-impedance branch is paralleled with the input of the comparator/SR driver to bypass the displacement current and clamp the output at a low voltage level during the high dv/dt transients. The resistance of the additional parallel branch helps to damp the oscillations induced by the high dv/dt. The self-driven mechanism is utilized to avoid any additional control signals or gate drivers, which makes the circuit operation simple and reliable. Second, the negative turn-off voltage is utilized to avoid the mis-triggering for the low-threshold GaN devices. Last but not least, the adaptive SR on-time tuning is applied to eliminate the influence from the loop stray inductance and the propagation delay. The proposed SR driving scheme can be extended to SiC-based SR and Si-based SR as well.

1.4 Challenges in Dynamic Voltage Balancing for Series-connected GaN HEMTs

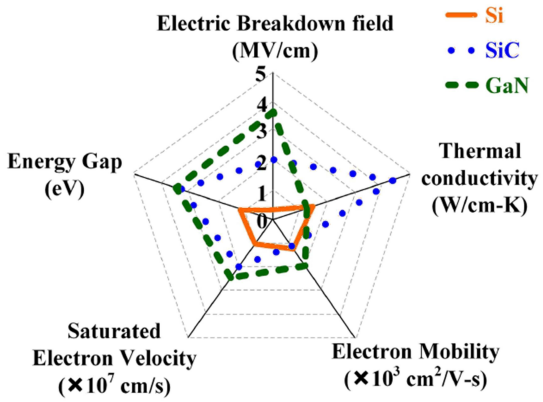


Figure 1.11: Property Comparison of Different Semiconductor Materials [1].

The wide-band-gap (WBG) power semiconductors for power electronics including

automotive applications have been an area of significant research attention and the U.S. Department of Energy (DoE) has invested heavily in their commercialization through the Advanced Research Projects Agency-Energy (ARPA-E) [4]. The property of different semiconductor materials is compared in Fig. 1.11. Except for the thermal conductivity, GaN is superior than the other two materials in terms of all the other aspects.

In EV traction inverters, Silicon Carbide (SiC) devices are favored than Si-IGBTs due to the much reduced switching energy and the high operating temperature capabilities. However, the reverse recovery loss of the intrinsic body diode of the SiC devices is still inevitable. Though external SiC Schottky diode can be paralleled with the SiC MOSFETs to cut down the reverse recovery loss, the costs will be increased.

Gallium Nitride (GaN) power devices offer low specific on-state resistance, fast switching speed and high operating temperature capabilities compared with Silicon (Si) counterpart [55–57]. All of these are beneficial for the efficiency, power density, specific power, as well as the reliability of power electronics converters [58]. Though Silicon Carbide (SiC) excels in high-temperature applications, the material characteristics of GaN are superior in high-efficiency, high-frequency converters [1]. In particular, due to the absence of the intrinsic body diode in the structure, the reverse recovery loss in GaN devices are totally eliminated. Therefore, GaN devices will consume less switching energy. Meanwhile, GaN devices have much smaller input capacitance compared with SiC devices, so the gate driving loss can be reduced as well.

However, unlike the SiC devices, which have the availability of 1.7 kV rating device on the market and 15 kV rating device in the research stage [59, 60], the highest voltage rating of the commercial GaN HEMTs is only at 600/650 V level because of the lateral structure, as shown in Fig. 1.12. The vertical GaN devices are

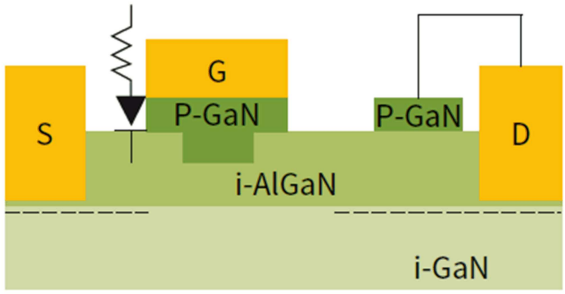


Figure 1.12: Structure of Infineon's GaN HEMT.

considered to have higher voltage rating [61], but they have not yet been produced on a commercial level. The insufficient voltage rating of GaN HEMTs hinders their appliance in the future EV systems, which has 800 V or higher dc bus voltage.

Table 1.2: Critical Parameters of a 1.2 kV/30 A SiC MOSFET and Two Series-connected 600 V/30 A GaN HEMTs.

Parameters	Single 1.2 kV SiC MOSFET	Two series-connected 600 V GaN HEMTs
Part number	CREE C3M0075120J	Infineon IGOT60R070D1
Typical on-resistance (R_{dson})	75 mΩ	55 mΩ × 2
Output capacitance (C_{oss})	58 pF	72 pF ÷ 2
Reverse recovery charge (Q_{rr})	109 nC	0
Gate charge (Q_{g})	48 nC	5.8 nC × 2

Stacking converters and stacking switches are the two most common approaches to block higher dc-link voltage. The cascaded H-bridges and multilevel converters can be categorized as the stacking converter solution. The advantages of this solution include

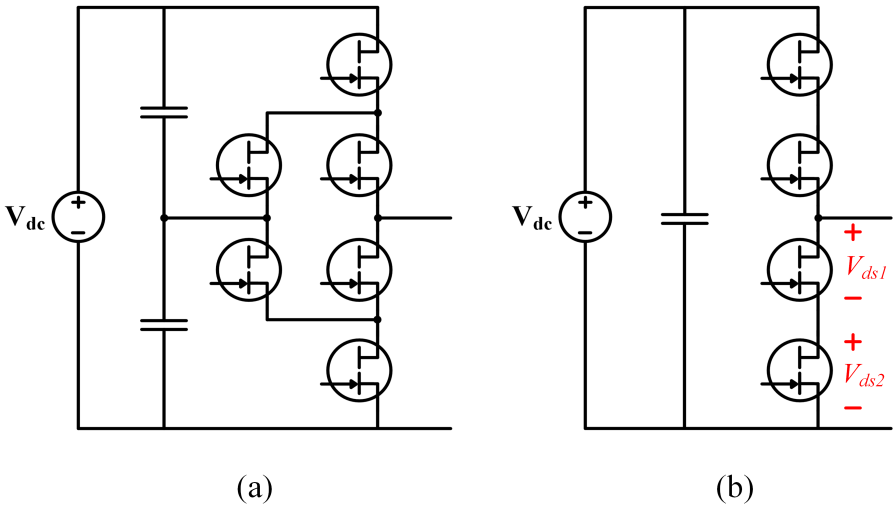


Figure 1.13: Two Solutions of Blocking High DC-link Voltage. (a) Multilevel Converter. (b) Stacking Switches.

lower dv/dt, lower EMI and lower output harmonics [62]. However, the complexity of the hardware structure as well as the control scheme are greatly increased for this solution. As is shown in Fig. 1.13(a), the active-neutral-point-clamped converter (ANPC) is a widely-used three-level converter topology for commercial PV inverters. Stacking switches is much simpler in terms of both the hardware structure and the control scheme. As is shown in Fig. 1.13(b), the series-connected GaN-based converter can be controlled as the two-level converter, and the component counts and hardware complexity are both reduced. The two series-connected 600/650 V GaN HEMTs can compete with the 1.2 kV SiC MOSFET and the three series-connected 600/650 V GaN HEMTs can compete with the 1.7 kV SiC MOSFET. The critical parameters of a 1.2 kV SiC MOSFET and two series-connected 600 V GaN HEMTs with similar current rating are listed in Table 1.2. Though the equivalent R_{dson} of series-connected GaN is higher than the R_{dson} of a single SiC MOSFET, the reverse recovery charge is completely eradicated for the series-connected GaN solution. The output capacitance and the gate charge are reduced significantly for the series-connected GaN solution as

well. The deficiency of higher equivalent R_{dson} for the series-connected GaN solution can be compensated by increasing the die size or paralleling the devices. Meanwhile, for the general medium-voltage hard switching applications, the switching loss can be more dominant [60]. The series-connected GaN solution can improve the system efficiency compared with the SiC solution [63]. Moreover, cost reduction of GaN devices will progress faster than for SiC devices due to significantly lower substrate costs and Si-CMOS manufacturing line compatibility [64].

The biggest challenge for the stacking switches approach is to address the dynamic voltage sharing issue among the switches in the stack, which can cause over-voltage breakdown for the individual low-voltage switch. As is shown in Fig. 1.13(b), the drain-to-source voltages of the two bottom switches may not be the same during the gate-off states. It is more challenging for the series-connected GaN solution, because of the extremely fast switching speed and the highly nonlinear Miller capacitance. Meanwhile, GaN devices are more vulnerable to the over-voltage damage due to the lack of avalanche breakdown mechanism [1]. The drain-to-source voltage imbalance among the series-connected switches can be introduced by the following factors. First, the gate driving loop can have discrepancies for the switches in the stack. The gate driving signals can be unsynchronized due to the variance of the propagation delays in the path. The gate driving loop parasitics can be different as well if the circuit connection and layout are not the same for different channels. Second, the device parameter tolerance can cause the unbalanced dynamic voltage sharing. The device input capacitance, output capacitance and the threshold voltage are all within certain range after the manufacturing process. The dynamic voltage sharing can be affected by the tolerance of these parameters. Last but not least, the displacement current flowing through the device-to-ground parasitic capacitances will cause distinctions in the gate current as well as in the drain current for different switches in the stack. The

distinctions in the gate or drain current will naturally result in unbalanced voltage sharing for different switches, even if the gate driving loops and device parameters are perfectly matched. The last factor is considered to be the major cause for the unbalanced voltage sharing for the series-connected fast-switching switches [65–67]. In particular, the GaN devices have very small input and output capacitances, so the device-to-ground parasitic capacitances will have a stronger effect on the dynamic voltage sharing for the series-connected GaN devices.

Some researchers have been working on the topic of series-connected GaN devices. In [68], a 1.2 kV super-cascode GaN transistor is demonstrated, which is based on two series-connected depletion-mode GaN. The structure has the same drawbacks as the typical cascode GaN, such as the undesired voltage sharing between the low-voltage Si MOSFET and the high-voltage depletion-mode GaN during the switching transient and large parasitic inductance in the package due to the multiple dies [69]. Meanwhile, an extra balancing capacitor is needed to assist the dynamic voltage sharing, which introduces additional loss. In [64], a 1.2 kV GaN transistor is made up by the series connection of an enhancement-mode GaN transistor and a depletion-mode GaN transistor. A charge-pump-based gate driver circuit is used to properly drive the top device. However, the device parameter mismatch can be severe for the two different type of GaN devices and no discussion is made on the dynamic voltage sharing for the two devices. An integrated gate driver circuit is proposed in [63, 70] to solve the issue of voltage imbalance for series-connected enhancement-mode GaN devices and a detailed mathematical model is developed as well. However, for this open-loop method, the circuit parameters need to be carefully tuned to achieve the desired switching timing for the series-connected devices, which makes this method very sensitive to the variance in the operating conditions, such as load current, dc-link voltage and temperature. To sum, a practical strategy for addressing the voltage

imbalance issues in series-connected GaN devices is lacking in the existing literatures.

However, a lot of efforts have been conducted for the voltage balancing of the series-connected IGBT in the past [71–77]. In recent years, a lot of researchers began to focus on the voltage balancing of series-connected SiC MOSFETs as well [65, 66, 78–80]. Most of the voltage balancing strategies can be grouped as the drain-side approach and the gate-side approach [65]. The snubber-based strategies belong to the drain-side approach. The pure passive snubber is usually very lossy. To reduce the additional loss produced by the snubber, the active energy recovery snubber circuits are proposed in [74, 79] with the cost of increasing circuit complexity and decreasing the circuit reliability. However, the device drain-to-source voltage rising slew rate is penalized with the employment of the snubber circuit. More switching energy will be produced during the switching transients. For the gate-side approach, the coupled gate driving method utilizes a single gate driver to drive all the series-connected switches in the stack [78, 81–84], in which the gate driving circuit parameters including the extra voltage balancing components need to be carefully tuned to achieve desired switching timing for each individual switch. It makes this method less adaptive to variable operating conditions. Hence, this method is not suitable for mass production. The active gate driving control is another main-stream strategy on the gate-side. In [66, 85], the gate driving signals are actively controlled to attain the desired switching timing for the series-connected switches. This approach is called the active gate delay control. For the conventional voltage source gate driver, the timing of the gate driving signal is the only control freedom. The unit step in the controller needs to be very small (below 1 ns) to achieve the satisfying voltage balancing, which makes the accuracy of this approach not reliable. In [65], a current mirror is in series with a large extra Miller capacitor to serve as a controllable extra Miller capacitor. The drain-to-source dv/dt of each device can be regulated to achieve well-balanced voltage sharing.

However, this strategy is only suitable for the devices with large input capacitance, such as high current rating power modules and Si devices, in which the turn-off dv/dt is mostly determined by the charging speed of the Miller capacitance. For the discrete wide-band-gap (WBG) devices, the input capacitance is significantly smaller. During the turn-off transient, the input capacitance can be discharged below the threshold before the drain-to-source voltage starts to rise and no Miller plateau will be observed in the gate-to-source voltage. In other words, during the dv/dt transient, the device channel is already cut off and the device can be regarded as a junction capacitor. The value of the extra Miller capacitor needs to be dominant in the output capacitance ($C_{\mathrm{oss}} = C_{\mathrm{gd}} + C_{\mathrm{ds}}$) in order to regulate the dv/dt properly. For discrete GaN devices, the intrinsic Miller capacitance is extremely small and it is significantly smaller than its drain-to-source capacitance (C_{ds}). The large extra Miller capacitor will greatly slow down the dv/dt of the switch and more switching energy will be produced during the switching transient. Meanwhile, the large extra Miller capacitor will enhance the crosstalk between the power loop and the gate driving loop. The gate driving loop will be more sensitive to the dv/dt and ringings in the power loop.

In this study, a controllable current-source-based gate driver is proposed. The gate current pulse-width and amplitude are directly controlled, so the device switching timing and dv/dt can be regulated with fine accuracy. Regardless of the origin of the voltage imbalance, the drain-to-source voltages of the switches in the stack can always be roughly equalized for both soft switching and hard switching scenarios. Meanwhile, without the employment of the lossy snubber circuits or the extra Miller capacitor, the switching energy and switching speed of the device are almost not compromised. Moreover, the current mirror circuits are utilized as the fast-responded discontinuous pulsed current sources, so the extra gate driving loss is negligible. Sufficient experiments have been conducted to validate the proposed current source gate

driver and the voltage balancing strategies in a variety of operating conditions.

1.5 Proposed Dissertation Outline

The proposed outline for this dissertation is organized as follows. Chapter 2 presents the design and optimization of the PCB-based magnetics. In particular, a novel low-stray-capacitance and well-heat-dissipated planar transformer is introduced. Chapter 3 discusses the high-dv/dt-immune, parameter-adaptive synchronous rectifiers (SR) gate driving scheme. The proposed bi-directional drain-to-source voltage sensing circuit is introduced in this chapter as well. Next, Chapter 4 presents the proposed active current source gate driver, which is used for balancing the dynamic voltage sharing in the series-connected GaN HEMTs. The root causes of the voltage imbalance and the proposed voltage balancing strategies for different switching scenarios are discussed as well. Finally, Chapter 5 concludes this dissertation and discusses the future work.

Chapter 2

DESIGN AND OPTIMIZATION OF PCB-BASED MAGNETICS

As mentioned in the introduction, the PCB-based magnetics can improve the converter power density significantly. In particular, PCB-based transformer (planar transformer) is advantageous because the leakage inductance and ac winding loss can be minimized with the interleaved winding structure (flux-cancellation). This chapter is organized as follows.

First, a generalized design and optimization approach of the planar transformer is proposed. Then the core and winding structure of the transformer is investigated to minimize the winding stray capacitance with a reasonable compromise of the winding loss. A low-stray-capacitance and well-heat-dissipated transformer configuration is proposed. Next, the proposed design methodology and transformer structure are implemented in a 6.6 kW/500 kHz CLLC resonant converter. Finally, experimental tests are conducted to verify the proposed approaches.

2.1 Generalized Design Methodology for Planar Transformers

The design of planar transformer is discussed in a lot of literatures [23, 26, 28, 29, 40, 86], but a generalized design methodology is lacking. Compared with conventional transformers, the PCB winding structure is fixed to some degree, which makes the planar transformer easier to be parameterized. In terms of optimization, some advanced optimization algorithms are conducted for the conventional wire-wound transformer [87, 88]. Although the optimal design can be found out, it is hard to find relations and trade-offs between different parameters and objectives due to too many free variables. This study proposes a generalized design methodology for high-power-density

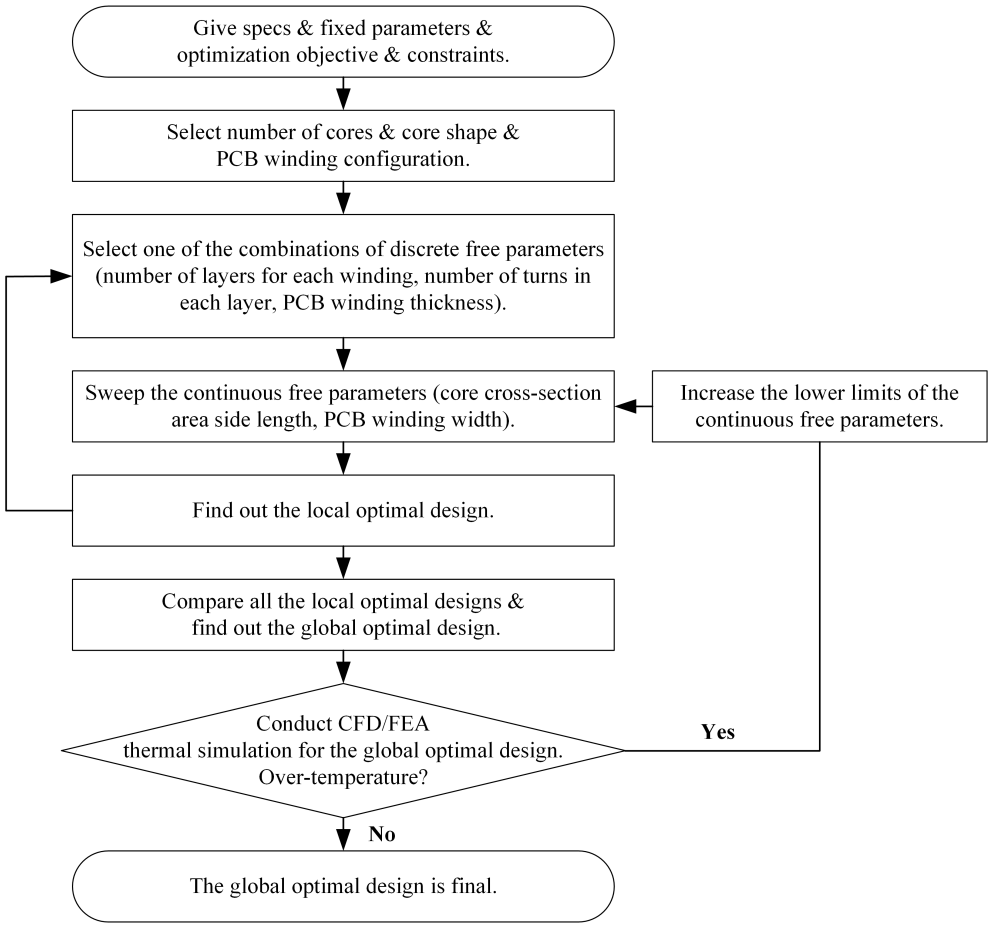


Figure 2.1: Proposed Generalized Design Methodology for High-power-density Planar Transformers.

planar transformers. By analyzing the core and winding geometries, only a few free parameters are needed for the optimization. By sweeping the free parameters, the trends of the objectives are easy to observe. The optimal design can be found for the given objectives and constrains.

The proposed design methodology for high-power-density planar transformers is shown in Fig. 2.1. This methodology is generalized for the design and optimization of non-integrated planar transformers. As mentioned before, transformer core loss or winding loss have to be compromised if the resonant inductor is integrated. The integrated design will have more challenges in thermal management, especially when

a large leakage inductance value is required. Moreover, to achieve a certain leakage inductance value, transformer winding structure is confined to some degree, which will hinder the optimization process in terms of efficiency or power density. The proposed design methodology is explained as follows.

2.1.1 Specifications, Fixed Parameters, Objective and Constraints

Specifications for a planar transformer include the operating frequency (f), excitation voltage waveform ($v(t)$), winding current waveform ($i(t)$), turns ratio (n) and required magnetizing inductance (L_{m}) value. It should be mentioned that the winding current waveforms can be obtained from the circuit simulation to get more accurate result.

The fixed parameters include the magnetic core Steinmetz parameters (α, β, and k), the insulation distance between different turns in the primary windings (δ_{pp}), the insulation distance between different turns in the secondary windings (δ_{ss}), the insulation distance between the primary windings and secondary windings (δ_{ps}), the insulation distance between the core and the primary windings (δ_{cp}), the insulation distance between the core and the secondary windings (δ_{cs}), thickness of each PCB (t_{pcb}) and the distance between different layers in the PCB (t_{ll}).

The optimization objective can be expressed as a weighting function of transformer total losses (P_{total}) and the box volume (V):

$$f = \min\left\{W_1 \cdot P_{\mathrm{total}} + W_2 \cdot V\right\} \tag{2.1}$$

where f is the objective function; W_1 and W_2 are weighting factors, which can be defined according to the requirements.

The constraints for planar transformer design can be summarized as follows. It should be noticed that not all the constraints are required for each design.

1. $B_{\max} < B_{\text{sat}}$. The maximum flux density in the core ($B_{\max}$) is normally much less than the saturation flux density (B_{sat}) of the core material in a high frequency transformer.

2. $J < J_{\max}$. The current density (J) in the winding should be smaller than the maximum allowable current density ($J_{\max}$). $J_{\max}$ is limited by the allowable winding temperature rise.

3. $P_{\text{total}} < P_{\text{total(required)}}$ or $\eta > \eta_{\text{required}}$. The total losses (P_{total}) or the efficiency (η) of the planar transformer can be restricted according to the requirement.

4. $V < V_{\max}$. The box volume of the planar transformer (V) can be confined according to the required maximum box volume or the required minimum power density. Compared to conventional transformers, the footprint of planar transformer is increased, hence, it is more meaningful to consider the box volume rather than consider just the core volume.

5. $g < g_{\max}$. The air-gap length (g) should be confined as well. If g is too large, the fringing flux can cause more winding loss.

6. Minimize L_{lk}. The leakage inductance value (L_{lk}) is not a design target for this methodology, because an external inductor is assumed to be employed. However, for a certain space, a larger leakage inductance indicates stronger leakage magnetic field intensity, which can cause more ac winding loss. Therefore, the leakage inductance value should be minimized.

7. Minimize C_{intra} and C_{inter}. This is usually not considered in the conventional transformer design. However, this factor can not be ignored, since the planar transformer normally has much higher winding stray capacitance. The

drawbacks of high intra-winding capacitance (C_{intra}) and high inter-winding capacitance (C_{inter}) have already been discussed in the introduction. Since the winding stray capacitance is closely related to the winding structure, an optimized winding configuration should be selected.

8. $T_{\text{core}} < T_{\text{curie}}$ and $T_{\text{winding}} < T_{\text{pcb(max)}}$. The core temperature ($T_{\text{core}}$) should be much less than the Curie temperature (T_{curie}) and the winding temperature (T_{winding}) should be less than the PCB maximum allowable temperature ($T_{\text{pcb(max)}}$). It is hard to analytically calculate the temperature rise for planar transformers. For this constraint, it should be checked after the optimal design is obtained. CFD or FEA thermal simulation can be employed. If the temperature rise is out of the desired range, the design should be discarded.

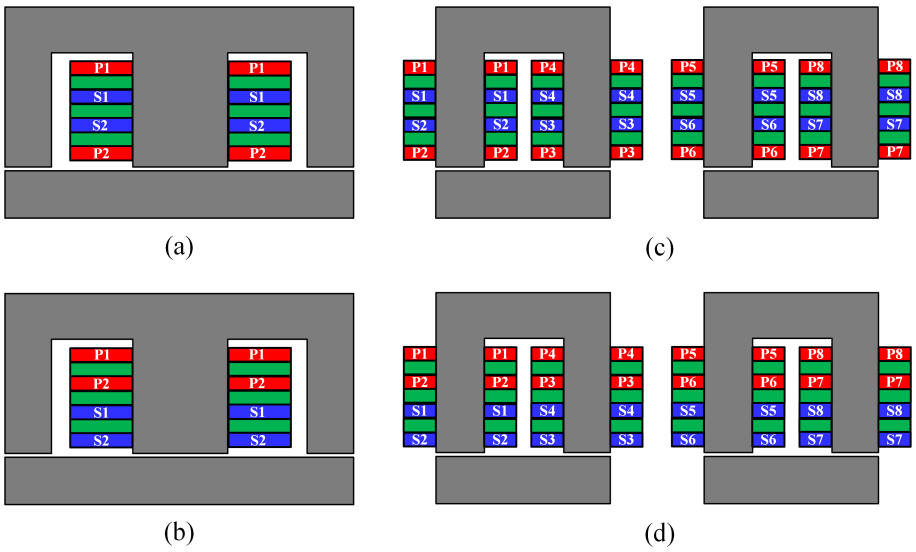


Figure 2.2: Typical Core and Winding Configurations of Planar Transformers. (a) Single-core (E-I Core) Interleaved Winding. (b) Single-core (E-I core) Non-interleaved Winding. (c) Multiple-core (U-I core) Interleaved Winding. (d) Multiple-core (U-I core) Non-interleaved Winding.

2.1.2 Selection of Number of Cores, Core Shape and Winding Configuration

For the high-power-density applications, the conventional single-core transformer is not the only option. The series-connected multiple-core solution needs to be considered as well, since it can distribute the total power into multiple cores and ease the voltage and thermal stress on each single core.

The magnetic core shape and PCB winding configuration are closely related. For E-I core or E-E core, windings are wound around the center pillar. For U-I core or U-U core, windings can be wound around both side pillars. There are other core shapes, such as pot core. For the winding structure, an alternating placement (interleaving) of primary and secondary windings in the vertical direction along the same core pillar is commonly used to achieve the most H-field cancellation, which can reduce the leakage inductance and ac winding loss. However, this structure will boost the inter-winding capacitance. The typical core and winding configurations are shown in Fig. 2.2. Advanced winding structures should be considered to cut down the inter-winding capacitance without sacrificing a lot of the ac winding loss.

Meanwhile, the windings can be wound on a single PCB or multiple PCBs. For each PCB, windings can be placed in a single layer or in multiple layers. Different winding configurations greatly impact the leakage inductance, ac winding loss, winding stray capacitance, as well as the winding thermal dissipation. One of the core and winding configurations should be selected for this step and the following optimization is based on the selected core shape and winding structure.

2.1.3 Selection of Combination of Discrete Free Parameters

In planar transformers, the number of layers for each winding (m), the number of turns in each layer (N_0) and the PCB winding thickness (t_w, typically = 1 oz, 2 oz, 3 oz...) can be seen as discrete free parameters. The three parameters are all free design parameters, but their values are discrete. Meanwhile, all three parameters are small integers. The number of layers for each winding is constrained by the cost of PCB and the number of turns in each layer is restricted by the footprint area or the box volume. The winding thickness should be confined as well due to the high frequency operation. For the operating frequency $\geq$ 500 kHz, the winding thickness should be no more than 3 oz. Therefore, the combinations of the three parameters are very limited. For this step, one of the combinations should be chosen.

2.1.4 Sweeping the Continuous Free Parameters

The cross-section area of the core (A_e) and the winding width (b_w) are continuous free parameters. They can be chosen as any value within certain range. Here, the core shape is selected as U-I core as an instance (Fig. 2.3). The two sides of the cross-section surface are a_1 and a_2, respectively. To employ fewer variables, k_0 is defined as the ratio of a_1 by a_2.

$$k_0 = \frac{a_1}{a_2} \tag{2.2}$$

k_0 is actually the length by width ratio of the cross-section surface and its value can be manipulated to improve the system power density, which will be discussed later in this study. When the ratio of a_1 by a_2 is a constant, it can be defined that $a_2 = a$ and $a_1 = k_0 a$. Then only two variables (a and b_w) are free continuous parameters. The other geometry-related parameters, loss-related parameters and the leakage inductance value can be expressed by a, b_w, fixed parameters and the selected

discrete free parameters.

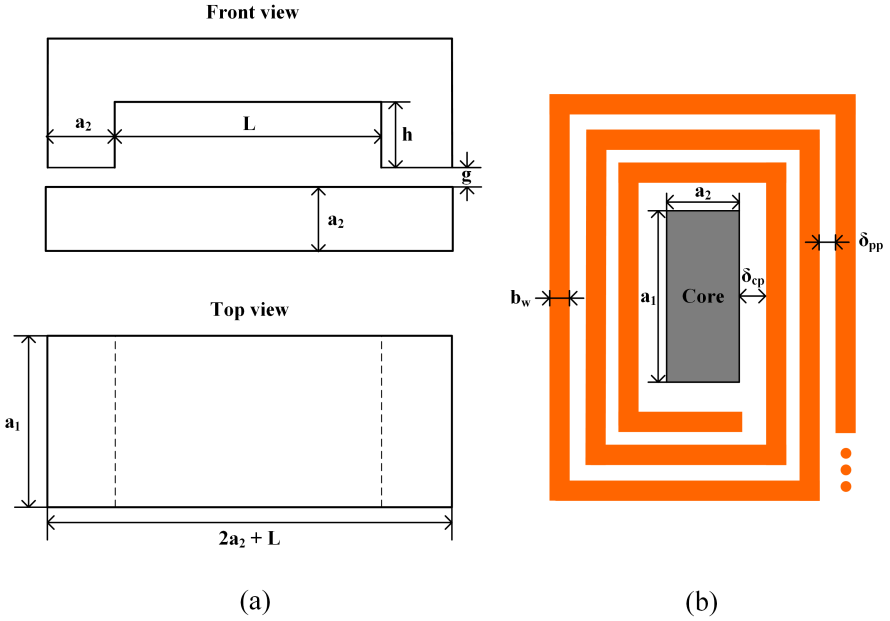


Figure 2.3: (a) U-I Core Sets Geometry. (b) Cross-section View and Winding Geometry for Each Pillar.

First, the geometry-related parameters are derived as follows. The derivations are based on a single U-I core, single multilayer PCB planar transformer.

$$L = 2\delta_{\text{cp}} + (N_0 - 1) \cdot \delta_{\text{pp}} + N_0 \cdot b_{\text{w}} \tag{2.3}$$

$$h = t_{\text{pcb}} + 2\delta_{\text{cp}} \tag{2.4}$$

$$g = \frac{\mu_0 \cdot k_0 a^2 \cdot (m \cdot N_0)^2}{2L_{\text{m}}} \tag{2.5}$$

$$V_{\text{core}} = 2k_0 a^2 \cdot (h + L + 2a) \tag{2.6}$$

$$\begin{aligned} V = {} & [k_0 a + N_0 b_{\text{w}} + (N_0 - 1)\delta_{\text{pp}} + 2\delta_{\text{cp}}] \cdot \\ & [L + 2a + N_0 b_{\text{w}} + (N_0 - 1)\delta_{\text{pp}} + 2\delta_{\text{cp}}] \cdot \\ & (2a + g + h) \end{aligned} \tag{2.7}$$

$$
\begin{aligned}
l_{\mathrm{w0}} &= 2{N_0}^2 \cdot b_{\mathrm{w}} + 2(k_0+1) \cdot N_0 \cdot a \\
&\quad + 4N_0 \cdot \delta_{\mathrm{cp}} + 4N_0 \cdot (\frac{N_0}{2} - 1) \cdot \delta_{\mathrm{pp}}
\end{aligned}
\tag{2.8}
$$

where L is the length of the window; h is the height of the window; g is the length of air-gap; V_{core} is the core volume; V is the transformer box volume and l_{w0} is the total length of each winding in one layer.

According to (2.5), the air-gap length is inversely proportional to the required magnetizing inductance value. The total reluctance in the transformer magnetic circuit is dominated by the reluctance of the air-gap, so the magnetizing inductance value can be tuned by adjusting the air-gap length in practical designs.

Second, the loss-related equations are derived as follows.

$$
B_{\mathrm{max}} = \frac{\int_0^{\frac{T}{4}} v(t)dt}{m \cdot N_0 \cdot k_0 a^2} \tag{2.9}
$$

$$
P_{\mathrm{core}} = K_{\mathrm{waveform}} \cdot k \cdot f^{\alpha} \cdot {B_{\mathrm{max}}}^{\beta} \cdot V_{\mathrm{core}} \tag{2.10}
$$

$$
R_{\mathrm{dc}} = m \cdot \rho_{\mathrm{Cu}} \cdot \frac{l_{\mathrm{w0}}}{b_{\mathrm{w}} \cdot t_{\mathrm{w}}} \tag{2.11}
$$

$$
P_{\mathrm{winding}} = \sum_{h=1}^{\infty} F_{\mathrm{ac(h)}} \cdot {I_{\mathrm{h}}}^2 \cdot R_{\mathrm{dc}} \tag{2.12}
$$

$$
P_{\mathrm{total}} = P_{\mathrm{core}} + P_{\mathrm{winding}} \tag{2.13}
$$

where B_{max} is the maximum flux density in the core; P_{core} is the core loss; K_{waveform} represents the core loss density under different excitation voltage waveforms [89, 90]; R_{dc} is the winding dc resistance value; ρ_{Cu} is the resistivity of copper; P_{winding} is the winding loss; $F_{\mathrm{ac(h)}}$ is the winding ac factor for h^{th} harmonic component, which can be estimated by Dowell's model [91] or by FEA simulation and P_{total} is the transformer total loss.

According to (2.9), the maximum flux density in the core is proportional to the volt-second of the excitation source. The high operating frequency can reduce the volt-second and avoid the saturation of the core, but the side effect is the increased core loss and ac winding loss.

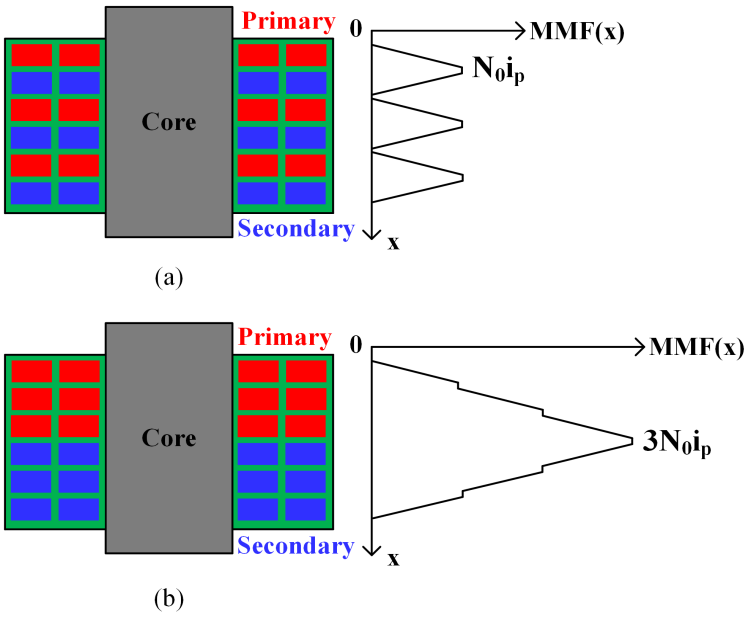


Figure 2.4: (a) MMF Distribution of Interleaved Winding Structure. (b) MMF Distribution of Non-interleaved Winding Structure.

Third, the leakage inductance value (L_{lk}) can be calculated by:

$$L_{\mathrm{lk}} = \frac{\mu_0 \cdot l_{\mathrm{w0}} \cdot b_{\mathrm{w}}}{I_{\mathrm{p}}^2} \cdot \int_0^{t_{\mathrm{pcb}}} H(x)^2 dx \tag{2.14}$$

where I_{p} is the rms value of primary winding current; t_{pcb} is the thickness of the PCB and $H(x)$ is the magnetic field strength along the vertical direction, which is related to the winding configuration. The MMF distribution of the interleaved and non-interleaved winding structures are shown in Fig. 2.4, where the gap MMF is assumed to be negligible.

From (2.14), it is clear that the leakage inductance value reflects the energy stored in the space among the windings. Any methods of increasing the leakage inductance

is either to enhance the magnetic field intensity or enlarge the space for the leakage flux. Usually, the increased magnetic field intensity will magnify the proximity effect and more ac winding loss will be produced.

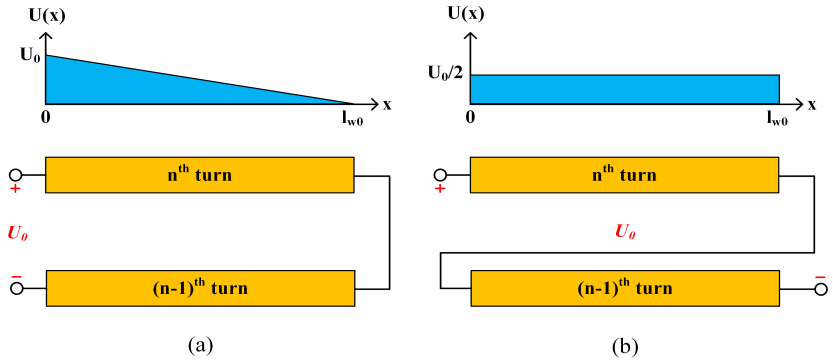


Figure 2.5: (a) Voltage Distribution Between Adjacent Turns in Different Layers (Connection Method 1). (b) Voltage Distribution Between Adjacent Turns in Different Layers (Connection Method 2).

Last but not least, the winding stray capacitance can be calculated.

To calculate intra-winding capacitance, it is reasonable to make two assumptions. First, the stray capacitance between the turns in the same layer can be ignored, because the turn-facing area in the same layer is much smaller than the turn-facing area in different layers [29]. Second, the stray capacitance between non-adjacent turns can be neglected as well, because the distance between non-adjacent turns is usually much larger than the distance between adjacent turns. Then the key is to calculate the stray capacitance between the adjacent turns in different layers. According to the principle of conservation of energy, the intra-winding capacitance between the two adjacent turns can be derived as:

$$C_{\text{turn-to-turn}} = \frac{\varepsilon_0 \varepsilon_{\text{r}} \cdot \int_V E^2 dV}{U^2} \tag{2.15}$$

where ε_0 is the vacuum permittivity; ε_{r} is the relative permittivity of the medium; E is the electric field intensity between the two turns; V represents the space/volume

between the two turns and U is the voltage different between the two terminals.

It is clear that the intra-winding capacitance between the adjacent turns is closely related to the electric field intensity distribution [92]. Since the distance between the two layers is fixed, the electric field intensity distribution is proportional to the voltage distribution. For analysis purpose, the turns are straightened as shown in Fig. 2.5. The voltage distribution between the turns changes for different connections of the adjacent turns, which will result in different turn-to-turn intra-winding capacitance value. Since the voltage distribution only varies along the winding (x-axis), (2.15) can be expressed as,

$$C_{\text{turn-to-turn}} = \frac{\varepsilon_0 \varepsilon_{\text{r}} \cdot b_{\text{w}} \cdot t_{\text{ll}} \cdot \int_0^{l_{\text{w0}}} E(x)^2 dx}{{U_0}^2} \tag{2.16}$$

where b_{w} is the winding/turn width and t_{ll} is the distance between two layers.

Once the turn-to-turn intra-winding capacitance value is obtained, the lumped intra-winding capacitance for each winding can be derived as,

$$C_{\text{intra(lumped)}} = \frac{1}{\frac{1}{C_{\text{1-to-2}}} + \frac{1}{C_{\text{2-to-3}}} + \frac{1}{C_{\text{3-to-4}}} + ... + \frac{1}{C_{\text{(m-1)-to-m}}}} \tag{2.17}$$

where m is the number of layers for each winding.

For the calculation of inter-winding capacitance, the single lumped capacitor model and the four lumped capacitor model can be employed, as shown in Fig. 2.6. The two models here are suited for the two-winding transformer and they can be extended for multi-winding transformer as well.

For the single lumped capacitor model, the transformer can be seen as a two-terminal device. The primary side winding is shorted and the secondary side winding is shorted as well. If a RLC meter is utilized to measured the parameter across the primary side and the secondary side, the measured capacitance value is the lumped capacitor value (C_0). This capacitor can also be regarded as the total value of the

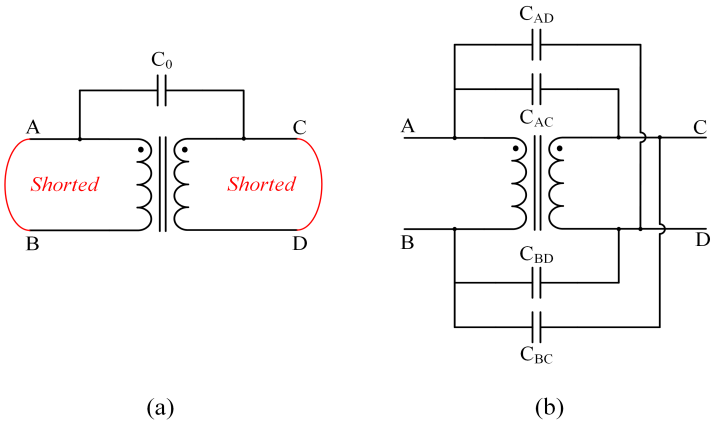


Figure 2.6: (a) Single Lumped Capacitor Model of Inter-winding Capacitance. (b) Four Lumped Capacitor Model of Inter-winding Capacitance.

distributed capacitance between the primary winding and the secondary winding. If the primary winding and the secondary winding have the same length of l_{w}, the inter-winding capacitance value for the unit length can be seen as C_0/l_{w}. Moreover, the single lumped capacitor can be calculated according to the winding geometry,

$$C_0 = \frac{\varepsilon_0 \varepsilon_{\mathrm{r}} \cdot b_{\mathrm{w}} \cdot l_{\mathrm{w}}}{t_{\mathrm{ll}}} \tag{2.18}$$

In reality, the transformer is a four-terminal device, so the four lumped capacitor model is more practical to represent its terminal characteristics. Again, if we assume the primary winding and the secondary winding have the same length, which is the case for matrix transformer, the total displacement current can be calculated as [38],

$$i_{\mathrm{dis}} = \frac{C_0}{2}\dot{V}_{\mathrm{A}} + \frac{C_0}{2}\dot{V}_{\mathrm{B}} - \frac{C_0}{2}\dot{V}_{\mathrm{C}} - \frac{C_0}{2}\dot{V}_{\mathrm{D}} \tag{2.19}$$

The total displacement current can also be derived as,

$$\begin{aligned} i_{\mathrm{dis}} = (C_{\mathrm{AC}} + C_{\mathrm{AD}})\dot{V}_{\mathrm{A}} + (C_{\mathrm{BC}} + C_{\mathrm{BD}})\dot{V}_{\mathrm{B}} \\ -(C_{\mathrm{AC}} + C_{\mathrm{BC}})\dot{V}_{\mathrm{C}} - (C_{\mathrm{AD}} + C_{\mathrm{BD}})\dot{V}_{\mathrm{D}} \end{aligned} \tag{2.20}$$

According to the principle of conservation of the displacement current, we have

$$C_{\mathrm{AC}} = C_{\mathrm{BD}} = C_{\mathrm{BC}} = C_{\mathrm{AD}} = \frac{C_0}{4} \tag{2.21}$$

Since all the interested parameters are expressed by a, b_{w} and the fixed parameters, the local optimization objective can be written as a function of a and b_{w} as well.

$$f(a, b_{\mathrm{w}}) = \min\left\{W_1 \cdot P_{\mathrm{total}}(a, b_{\mathrm{w}}) + W_2 \cdot V(a, b_{\mathrm{w}})\right\} \tag{2.22}$$

By sweeping a and b_{w}, the plot of $W_1 \cdot P_{\mathrm{total}}(a, b_{\mathrm{w}}) + W_2 \cdot V(a, b_{\mathrm{w}})$ can be obtained. The constraints will work as the boundary conditions and shape the plot. The minimum value of the plot is the local optimal design for the selected set of discrete free parameters.

2.1.5 Global Optimization and Validation

The same optimization process should be conducted for each combination of discrete free parameters. After all the combinations are evaluated and compared, the global optimal design is found out. Next, the thermal performance of this design should be validated by CFD or FEA thermal simulation. If the temperature rise is too much, the lower limits for the side length of core cross-section area (a) or the PCB winding width (b_{w}) should be elevated and the optimization process should be conducted once again until the temperature rise of the global optimal design meets the requirement. Then the global optimal design is considered as the final design.

For the implementation of the proposed design methodology, only numerical calculations are required except for the thermal simulation, which makes the optimization process simple and fast.

It should be mentioned that the design and optimization of the planar inductor is very similar to the design of planar transformer. Most of the design methodology proposed above is applicable to the planar inductor design and optimization as well. There are only two crucial differences. First, the maximum flux density (B_{max}) in a planar inductor is usually calculated by the peak current rather than the volt-second,

since the resonant inductor voltage is not clamped by the source. Second, there is no flux cancellation between the adjacent turns in an inductor, because the current directions are all the same. Therefore, the number of turns for a planar inductor should be as few as possible to avoid the excessive ac winding loss.

2.2 Investigation of Low-stray-capacitance and Well-heat-dissipated Transformer Configuration and Trade-off Analysis

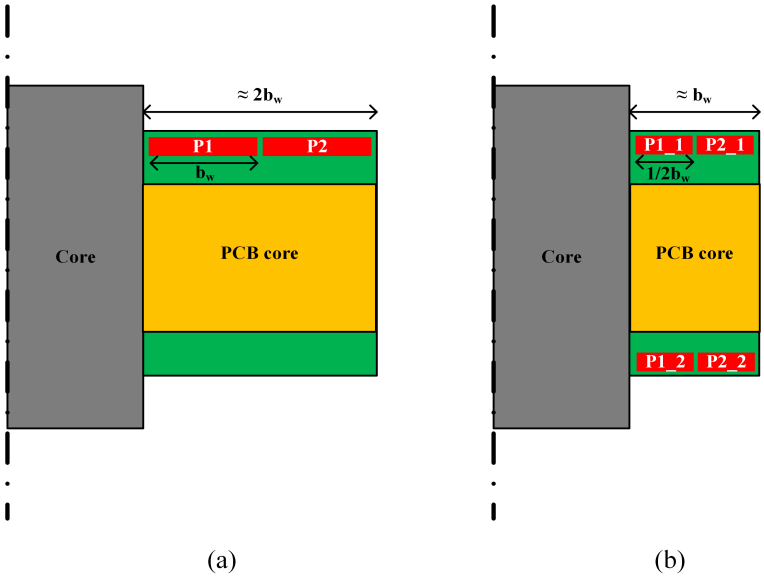


Figure 2.7: (a) Parallel Routing Strategy to Reduce Intra-winding Capacitance. (b) Split-turn Routing Strategy to Reduce Intra-winding Capacitance.

2.2.1 Reduction of Intra-winding Capacitance

When the number of turns for each winding is determined, the key is to cut down the turn-to-turn intra-winding capacitance. According to (2.16), two practical approaches can be taken. One is to reduce the physical stray capacitance between adjacent turns. The other approach is to minimize the electric field intensity between turns.

To reduce the physical stray capacitance, either cutting down the overlapping area or increasing the distance between adjacent turns can be employed. The parallel routing (horizontal routing) of adjacent turns is an effective way to reduce the overlapping area, as shown in Fig. 2.7(a). The overlapping area is decreased from the winding length by width to the winding length by thickness and the thickness of PCB windings is typically much smaller than the width of PCB windings. However, this approach increases the winding footprint area, because the vertical space in the PCB has not been utilized.

To minimize the electric field intensity between turns, the split-turn strategy can be applied. As shown in Fig. 2.7(b), one turn is split into two parts and the two paralleled half-turns are aligned with each other vertically (P1_1 and P1_2; P2_1 and P2_2). Since there is no voltage difference along the winding between the two half-turns, the equivalent stray capacitance between them is zero. Then the intra-winding capacitance is determined by the stray capacitance between paralleled adjacent half-turns, which has been significantly reduced. If the insulation distance between adjacent turns is assumed to be negligible compared with the winding width, the winding footprint area is half of the footprint area of the configuration in Fig. 2.7(a). However, multiple layers are required for each winding in this structure.

2.2.2 Reduction of Inter-winding Capacitance

Similarly, the inter-winding capacitance can be cut down by either reducing the physical stray capacitance or minimizing the electric field intensity between the primary winding and the secondary winding. The principle of the shielding layer approach [37, 38] is actually minimizing the voltage difference between the shielding layer and the secondary winding, so the equivalent inter-winding capacitance between the shielding layer and the secondary winding is zero. As mentioned before,

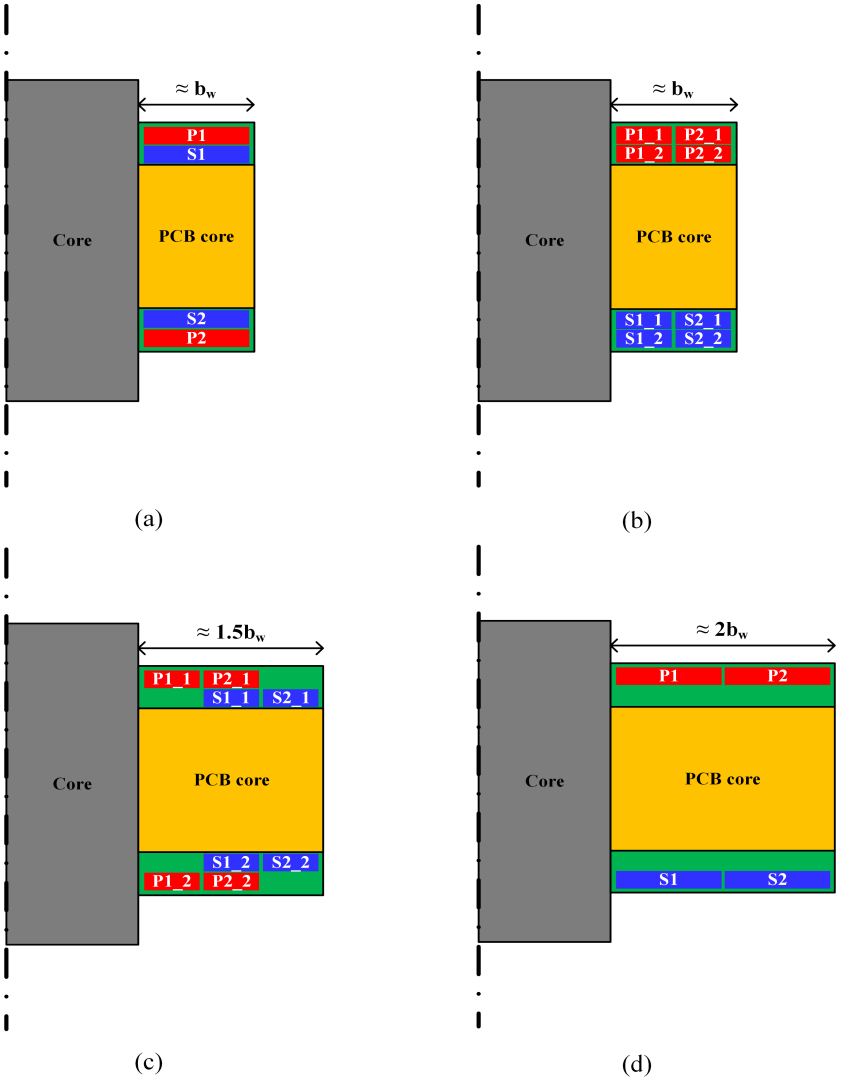


Figure 2.8: (a) Conventional Interleaved Winding Structure (Reference). (b) Split-turn Non-interleaved Winding Structure. (c) Split-turn Interleaved and Partially Mis-aligned Winding Structure. (d) Paralleled Routing Winding Structure.

the major drawback of employing a shielding layer is the increased eddy current loss, which lowers the system efficiency. Therefore, reducing the physical stray capacitance between the primary winding and the secondary winding is investigated in this study. Combined with the methods of reducing the intra-winding capacitance, four different winding configurations are shown in Fig. 2.8 to cut down both the intra-winding capacitance and inter-winding capacitance. A four-layer PCB is utilized and

the primary winding and the secondary winding are both assumed to have two turns, which is for the case of a 1:1 transformer or a unit core for a matrix transformer. The reference case is shown in Fig. 2.8(a), which has the commonly used interleaved winding structure [40]. The configuration in Fig. 2.8(b) reduces the inter-winding capacitance by halving the overlapping area and increasing the distance between the primary winding and the secondary winding. According to a standard 1.6-mm four-layer PCB stack-up, the distance between the two middle layers (PCB core) is 1200 μm, while the distance between the top two layers and the distance between the bottom two layers are only 140 μm. The configuration in Fig. 2.8(c) reduces the inter-winding capacitance by halving the overlapping area. The interleaved winding structure is still maintained. Finally, the configuration in Fig. 2.8(d) reduces the inter-winding capacitance by increasing the distance between the primary winding and the secondary winding.

Table 2.1: Per Unit Value of Interested Parameters for Different Winding Configurations.

Parameters	Case (a)	Case (b)	Case (c)	Case (d)
Intra-winding capacitance	1	1.57	1.42	0.24
Inter-winding capacitance	1	0.065	0.187	0.082
Leakage inductance	1	3.99	1.66	4.81
AC winding loss	1	1.22	1.17	1.13
Winding footprint area	1	1	1.5	2

To compare the above winding configurations, FEA simulations are employed. The magnetic field intensity distributions for different scenarios are shown in Fig.

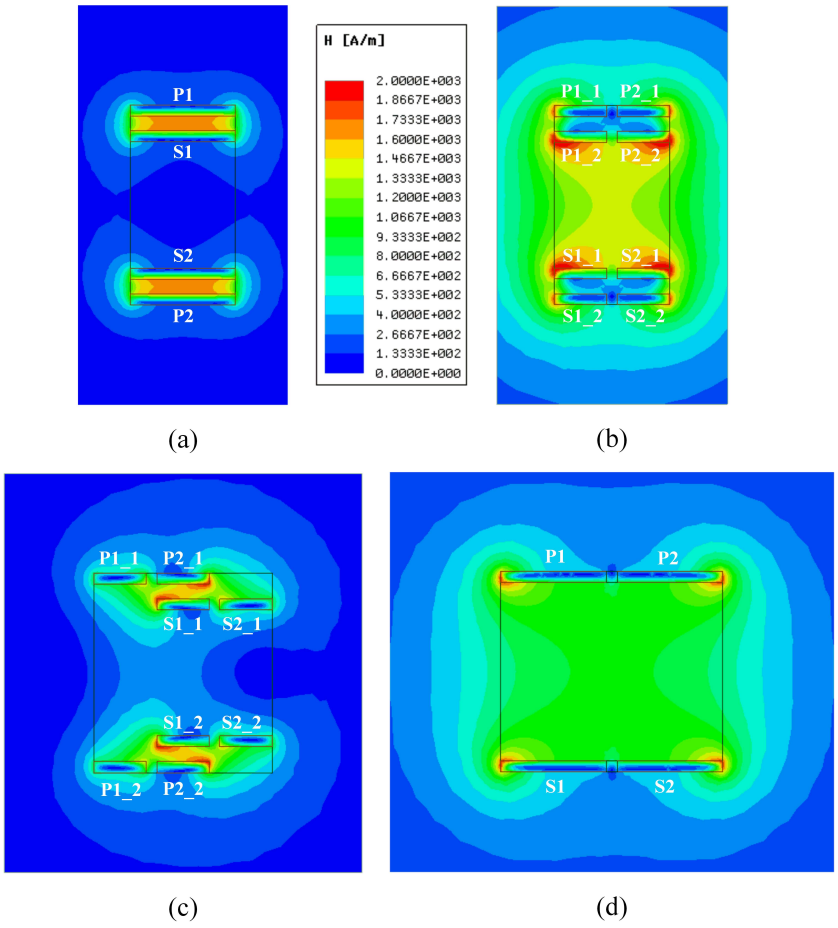


Figure 2.9: Magnetic Field Intensity Distributions for Different Winding Configurations. (a) Conventional Interleaved Winding Structure (Reference). (b) Split-turn Non-interleaved Winding Structure. (c) Split-turn Interleaved and Partially Misaligned Winding Structure. (d) Paralleled Routing Winding Structure.

2.9. The current density distributions for different scenarios are shown in Fig. 2.10. The total intra-winding capacitance (the sum of primary side and secondary side), inter-winding capacitance, leakage inductance value, ac winding loss and the winding footprint area are evaluated for all configurations and summarized in Table 2.1. It should be noticed that the corresponding parameters for the reference case [case (a)] are regarded as the per unit for each row in the table and insulation distance between the adjacent turns are assumed to be negligible compared with the winding width.

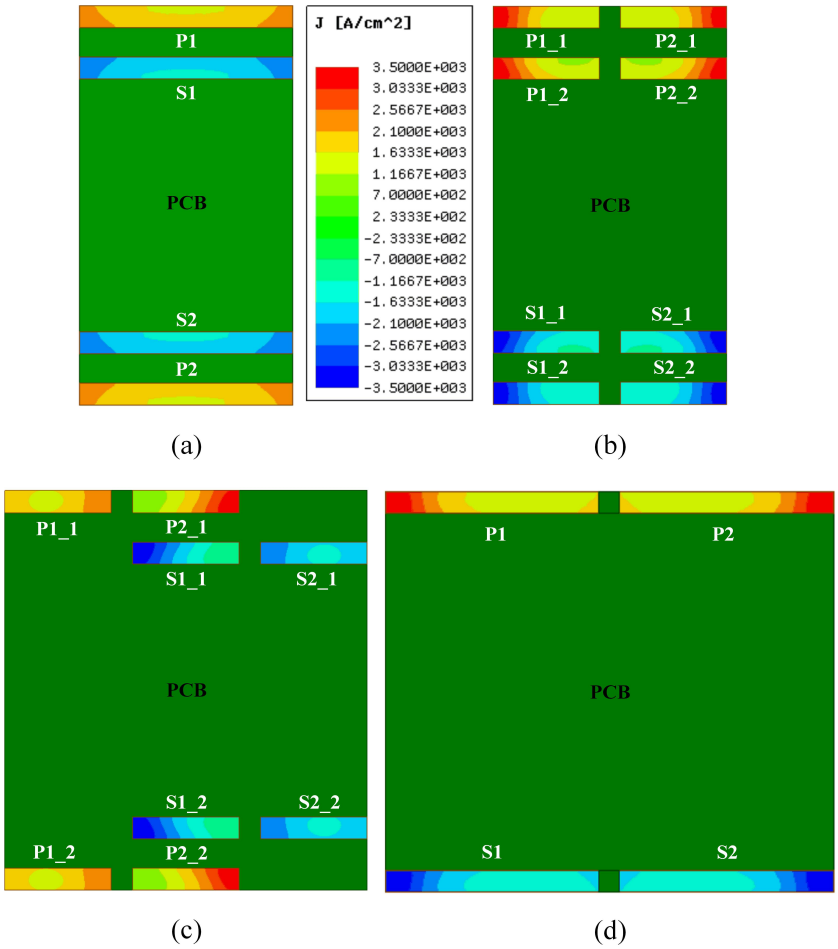


Figure 2.10: Current Intensity Distributions for Different Winding Configurations. (a) Conventional Interleaved Winding Structure (Reference). (b) Split-turn Non-interleaved Winding Structure. (c) Split-turn Interleaved and Partially Mis-aligned Winding Structure. (d) Paralleled Routing Winding Structure.

For the intra-winding capacitance, case (d) exhibits the minimum value. For case (b), there is no voltage difference between the two paralleled half turns (P1_1 and P1_2; P2_1 and P2_2), but the voltage difference between the two diagonal half turns (P1_1 and P2_2; P2_1 and P1_2) is not zero. This is the reason why the intra-winding capacitance of case (b) is higher than the reference case [case (a)]. The same reason applies for case (c). To cut down the intra-winding capacitance, the winding configuration in case (d) is the best option.

In terms of the inter-winding capacitance, both case (b) and case (d) present less than 10% of the inter-winding capacitance value for the reference case. Since case (b) has much higher intra-winding capacitance compared with case (d), case (d) is the best choice by taking consideration of both intra-winding capacitance and inter-winding capacitance.

However, case (d) displays the largest leakage inductance among all the cases due to the increased space between the primary winding and the secondary winding. Based on the FEA simulation in Fig. 2.9(d), the overall magnetic field intensity is still kept low, which will not magnify the ac winding effect significantly. The quantitative analysis of ac winding loss is conducted in the next paragraph. For the leakage inductance value in a single PCB, it is normally no more than several 100 nH [93]. If the LLC/CLLC resonant converter is deigned for variable-frequency operation (D2D operation), the required resonant inductance value is usually in the μH range. The increased leakage inductance in the PCB can be used as part of the resonant inductor. If the LLC/CLLC resonant converter is designed for fixed-frequency operation (DCX operation), the required resonant inductance value can be very small. The increased leakage inductance in the PCB can be used as the entire resonant inductor. For both scenarios, the increased leakage inductance in the PCB will not affect the system operation.

Another crucial concern of employing a novel winding structure is the increased ac winding loss. From the FEA simulation results, the ac winding loss for case (b), case (c) and case (d) are all higher than the reference case. Case (d) produces the minimum additional ac winding loss, which is 13% higher than the reference case. Suppose the transformer efficiency is 99% and the core loss and winding loss are nearly equal. The additional ac winding loss will only cause 0.065% drop of the transformer efficiency. Moreover, according to the current density distribution in

Fig. 2.10(d), only the edge of the turns has significantly higher current density (edge effect). When the width of the turns is extended, the ratio of the high-current-density portion will be reduced. Hence, the extra ac winding loss will be diminished as well. Based on the FEA simulation result, when the winding width by thickness ratio is 40:1, the extra ac winding loss compared with the reference case becomes less than 5%. For case (b) and case (c), since the winding width is half of that in case (d), the ratio of the high-current-density portion is larger than case (d), which leads to the smaller effective conduction area. Therefore, more ac winding loss will be produced by case (b) and case (c).

The increase of DCR for the winding should be considered as well. For case (b), (c), (d), since the paralleled routing strategy is employed in one layer, the equivalent winding length of the outer turn is larger than the inner turn, which causes the increase of the DCR of the winding. This issue can be released by utilizing the matrix transformer structure. The matrix transformer, which is defined as an array of elemental transformers interwired to form a single transformer [94]. It has been successfully used for high turns-ratio applications [16, 26, 40, 86]. The key is to split a single core to multiple identical cores or pillars and employ very few number of turns for each unit. The matrix transformer boosts the space utilization rate and reduces the footprint, because of the high core-area by winding-area ratio. Since very few turns (normally 1$\sim$2 turns) are wound for each unit core or unit pillar in one layer, the increase of the equivalent winding length is insignificant. Meanwhile, as mentioned earlier, the EV on-board charger belongs to high volt-second and low-current applications. The core cross-section area dominates the transformer footprint and the winding width is significantly smaller compared with the core dimension. Therefore, the percentage for equivalent winding length increase is minor. It should be noted that the employment of matrix transformer structure may increase the core

loss. When the turns for multiple cores or pillars are connected in parallel, the same volt-second will be applied on every magnetic component. The core loss can be elevated due to the increase of total core volume (2.10). However, the compromise in the core loss can be minimal thanks to the high core-area by winding-area ratio for the matrix transformer. The window area for each core or pillar in matrix transformer is small, so the core length is small. If the conventional single-core structure is utilized, the window area can be considerable due to larger winding width, which increases the core's length and volume. Hence, the increased total core volume by employing the matrix transformer structure can be insignificant. The elevated core loss can be negligible as well.

The reduction of the transformer winding stray capacitance will benefit the system efficiency. During the dead-time, the magnetizing current will charge and discharge both the device junction capacitances and the transformer winding stray capacitance, as shown in Fig. 1.8. The junction capacitance of the discrete WBG device is normally in the range of tens of pF to two hundred pF. It is in the same range or even smaller than the planar transformer winding stray capacitance. If the CLLC converter operates at fixed frequency (DCX operation), the magnetizing inductance is designed only for the sake of achieving ZVS. If the transformer winding stray capacitance is dominated in the paralleled capacitive branch shown in Fig. 1.8, the reduction of the winding stray capacitance will diminish the required magnetizing current significantly. Then the primary side device conduction loss and the winding loss will be reduced because of the diminished total current. The percentage of the loss reduction depends on the ratio of the magnetizing current to the load current. This loss reduction will be very obvious for light load conditions. If the CLLC converter operates at variable frequency (D2D operation), the magnetizing inductance value is normally designed to satisfy the desired voltage regulation capability. For this scenario, although the mag-

netizing current is not reduced, the dv/dt of the switch will be increased for the case with smaller winding stray capacitance, which cuts down the device switching loss. Moreover, since the transformer stray capacitance draws less current, the magnetizing current is large enough to charge and discharge higher junction capacitance value. Therefore, higher current rating device can be utilized without the worry of losing ZVS. For the same voltage rating, the device R_{dson} is almost reversely proportional to device current rating. The device conduction loss will be significantly reduced. Based on the above discussion, the reduction of the winding stray capacitance can boost the system efficiency significantly, hence, a little compromise of the transformer winding loss is reasonable.

The winding footprint area is doubled for case (d). However, as mentioned before, the EV on-board charger belongs to high volt-second and low-current applications. The core cross-section area dominates the transformer footprint, so the increased winding footprint area will not increase the transformer footprint significantly. Meanwhile, since all the conductors are in the outer layers of PCB, the thermal dissipation capability is improved. The winding width can be diminished to save the winding footprint area. Moreover, the EMI filter size can be cut down because of the significantly reduced inter-winding capacitance (91.8% reduction). If the inter-winding capacitance is the dominant path for the CM current in the circuit, the magnitude of the CM noise will be reduced by 21.7 dB, which is almost as good as the shielding layer technique claimed in [95]. The system power density can be improved. Therefore, the paralleled routing structure [case (d)] can significantly cut down both the intra-winding capacitance and inter-winding capacitance with little compromise or even boost of the system efficiency and power density. This winding structure is selected as the proposed low-stray-capacitance winding configuration.

Another observation from the FEA simulation results is the magnified leakage in-

ductance and the ac winding loss in case (c), though the interleaved structure is employed. It is because the vertical mis-alignment between the primary winding and the secondary winding weakens the magnetic field cancellation. The uncanceled magnetic flux will enhance the ac winding effect and lead to higher winding loss. Therefore, the primary winding and the secondary winding should be vertically overlapped as much as possible to maintain the good magnetic flux cancellation.

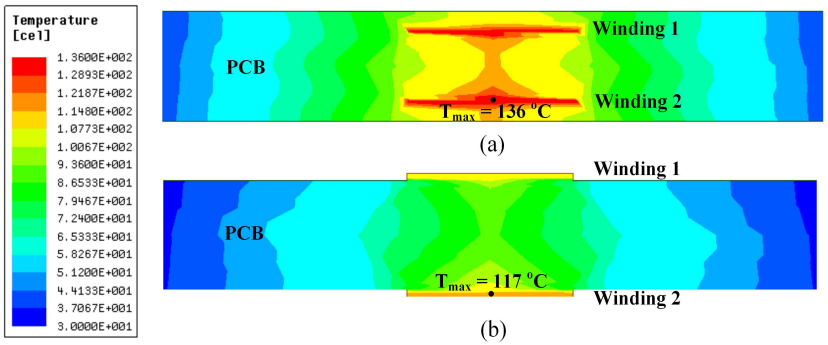


Figure 2.11: (a) CFD Thermal Simulation of Inner-layer PCB Windings. (b) CFD Thermal Simulation of Outer-layer PCB Windings.

2.2.3 Enhancement of Winding Thermal Dissipation

By placing the windings on the outer layers of the PCB, the thermal dissipation capability of the windings will be improved, because the heat transfer coefficient is elevated. CFD thermal simulations are conducted for inner-layer PCB windings and outer-layer PCB windings, respectively (Fig. 2.11). Each winding is set to generate the same power loss and the PCBs receive 20 CFM top-side forced-air cooling. The ambient is set to be 20 °C. It is shown that the maximum temperature for the outer-layer PCB winding is around 20 °C lower than the inner-layer PCB winding at the same condition.

To sum, the keys for constructing a low-stray-capacitance and well-heat-dissipated planar transformer are listed as follows.

1. Each winding should only be routed in one layer. There should not be any vertical overlapping between different turns of the same winding.

2. Primary winding and secondary winding should be vertically overlapped as much as possible.

3. Primary winding and secondary winding should be placed in the two outer layers of the PCB.

2.3 Design and Optimization of the Planar Transformer for 6.6 kW/500 kHz CLLC Resonant Converter

Table 2.2: Specifications and Fixed Parameters of Desired Planar Transformer.

Parameters	Values
Operating frequency	500 kHz
Primary side voltage	±900 V (square wave)
Primary side current	11.3 Arms
Secondary side current	8.7 Arms
Turns ratio	2:1:1
Desired magnetizing inductance	31 μH
Selected core material	Hitachi ML27D
Insulation space	$\delta_{pp} = \delta_{ss} = 20$ mil; $\delta_{ps} = \delta_{cp} = \delta_{cs} = 80$ mil
PCB thickness	1.6 mm

A high-efficiency, high-power-density planar transformer is required to be designed for the 6.6 kW/500 kHz CLLC resonant converter in Fig. 1.5. The design and optimization process follows the methodology proposed in this study.

First, the specifications and fixed parameters of the desired planar transformer are listed in Table 2.2. The objective is to design a high-power-density transformer with efficiency higher than 98.9% (just for this design and not necessary to be this specific number). According to (2.1), the objective function is a weighting function of the transformer total loss and the box volume, which is a multi-objective function. In order to simplify the optimization process, the transformer box volume is selected as the single objection function. The total loss (or efficiency) becomes a constraint in the optimization. Therefore, the local objective function can be written as:

$$\begin{gathered} f(a, b_{\mathrm{w}}) = \min\{V(a, b_{\mathrm{w}})\} \\ \text{Efficiency constraint: } P_{\mathrm{total}}(a, b_{\mathrm{w}}) < 1.1\% \times 6.6 \text{ kW} \end{gathered} \tag{2.23}$$

Except for the efficiency constraint, other applied constraints include core maximum flux density and winding maximum current density.

$$\begin{aligned} B_{\max} &< 0.52 \text{ T}(B_{\mathrm{sat}}) \\ J_{\max} &< 3300 \text{ A/cm}^2 \end{aligned} \tag{2.24}$$

It should be mentioned that the maximum winding current density constraint is based on the allowed winding temperature rise, which is estimated by empirical equations.

Second, the number of cores, core shapes and PCB winding configurations need to be established. Since the required turns-ratio is 2:1:1, the primary number of turns is not equal to the secondary number of turns. It is not practical to use a single core to achieve the proposed winding configuration. Two cores with 1:1 turns ratio can be series-connected in the primary side to construct a 2:1:1 matrix transformer. For each unit core or pillar, it is easy to implement the 1:1 turns ratio. The primary winding and secondary winding can be routed in exact the same fashion. The perfect

vertical overlapping between the primary and secondary windings will minimize the leakage inductance and ac winding loss. By series-connecting the core units, it is easy to achieve high turns-ratio without losing the benefit of almost perfect magnetic flux cancellation.

In this design, two U-I cores are interwired as a matrix transformer to utilize the proposed winding structure. The core and winding configuration is shown in Fig. 2.12, the primary windings are placed on the top layer and the secondary windings are placed on the bottom layer. The primary windings of the two cores are both on the top layers. They are series-connected by a PCB trace in a middle layer or by a jumper wire. The secondary windings are independent for each core. The arrows in Fig. 2.12 represent the corresponding current direction. It is clear that the secondary induced current direction is opposite of primary current, which achieves the flux cancellation between the primary and secondary windings.

Next, one combination of the discrete parameters (m, N_0, t_w) needs to be selected. Obviously, for the proposed winding structure, there is no vertical overlapping for primary winding or secondary winding itself, so the number of layers for each winding (m) equals to 1. Since the operating frequency is 500 kHz, the winding thickness (t_w) should not exceed 3 oz, in order to avoid excessive ac winding loss due to skin effect and proximity effect. Meanwhile, the optimization objective is to find the minimum box volume of the planar transformer, hence it is reasonable to use a thicker PCB winding for saving the footprint area. The number of turns for each layer (N_0) should not be a large integer, because it will increase the footprint area, as well as the transformer box volume. Moreover, for the proposed split-core winding structure, N_0 should be an integer multiple of 4, which means at least one turn of winding is wound on each pillar of each unit core. To sum, the combinations of the discrete free parameters are listed as follows.

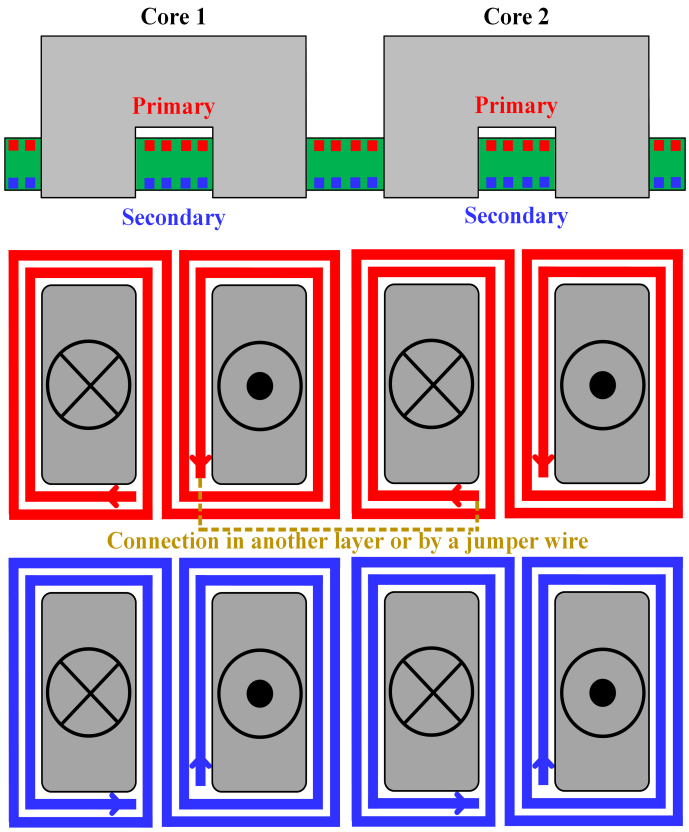


Figure 2.12: Core and Winding Configuration of Proposed Planar Matrix Transformer.

$$m = 1; t_{\mathrm{w}} = 3; N_0 = 4, 8, 12, 16, 20, 24, 28... \tag{2.25}$$

Then local optimization can be conducted by sweeping the core cross-section area side length (a) and the winding width (b_{w}). Here, the length by width ratio of the cross-section surface (k_0) is selected as 6 to match the dimension of other components in the power converter and boost the system power density. The plot of $V(a, b_{\mathrm{w}})$ for one of the local optimizations ($m = 1$, $t_{\mathrm{w}} = 3$ and $N_0 = 8$) is shown in Fig. 2.13. The edge in this plot is shaped by the constraints. The lower limit of a is restricted by the B_{sat} and the efficiency constraints and the lower limit of b_{w} is confined by the J_{max} and the efficiency constraints. The efficiency constraint also removes points from the

plane, which causes the serrated edge. The local optimal design is found out with the transformer box volume of 127.7 cm^3. Meanwhile, since the core loss, winding loss and total loss are all functions of the cross-section area side length (a) and the winding width (b_w), the 3D plot of the core loss and winding loss for different design points can be obtained, as shown in Fig. 2.14. From the 3D plot, it is clear that our optimal design (minimum box volume) does not present the minimum total loss, but the total loss of our optimal design point satisfies the efficiency constraint (98.9%). It is reasonable to sacrifice a little bit of efficiency to achieve much higher power density as long as it is thermally viable.

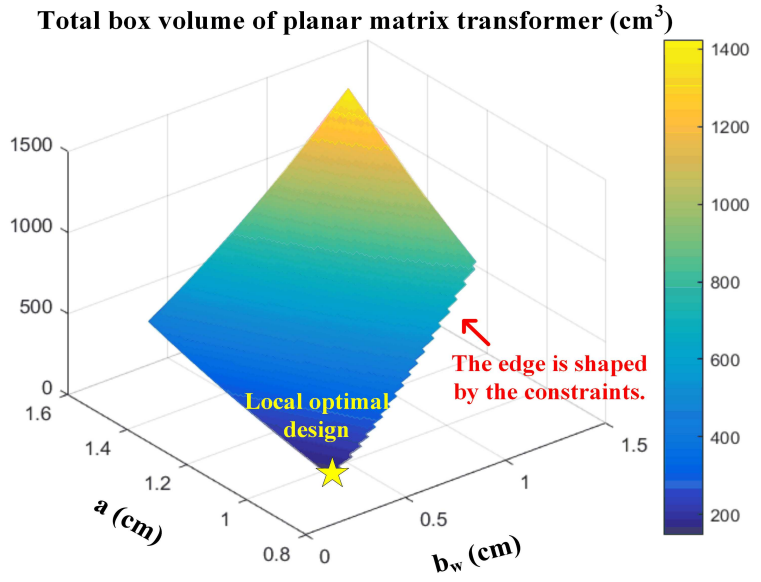


Figure 2.13: Local Optimization (Minimum Box Volume) at $m = 1$, $t_w = 3$ and $N_0 = 8$.

The same process is conducted for other N_0 values, which is to place different number of turns on each layer. Table 2.3 presents the minimum transformer box volume for different N_0. Meanwhile, in terms of system power density, a smaller footprint area of the planar transformer is preferred. The system height is decided by the tallest component in the system. Due to the low profile characteristics of

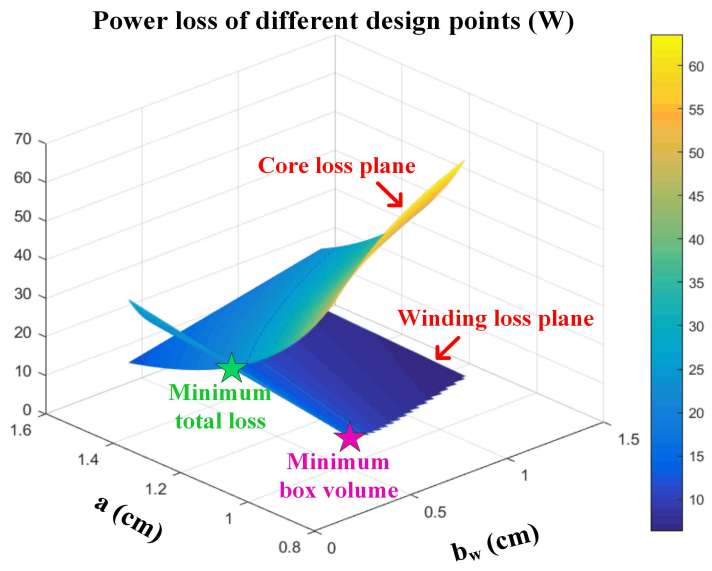


Figure 2.14: Power Loss for Different Design Points of the Planar Matrix Transformer at $m = 1$, $t_{\mathrm{w}} = 3$ and $N_0 = 8$.

Table 2.3: Minimum Transformer Box Volume and Minimum Transformer Footprint Area for Different N_0.

N_0	Minimum transformer box volume (cm^3)	Minimum transformer footprint area (cm^2)
4	No solution	No solution
8	127.7	70.3
12	122.1	73.6
16	127	87
20	149	108
24	183.7	135
28	190.3	196.8

the planar transformer, it is usually not the tallest component in the system. The minimum footprint area for different N_0 is listed in Table 2.3 as well.

To consider both the minimum box volume and the minimum footprint area, N_0

Table 2.4: Key Parameters for the Global Optimal Design.

Parameters	Values
Power rating	6.6 kW
Operating frequency	500 kHz
Number of cores	2
Core material	Hitachi ML27D
Core side length a_1, a_2	5.34 cm, 0.89 cm
Core cross-section area	4.75 cm^2
Maximum flux density	118 mT
Turns ratio	2:1:1
Number of turns	8 (pri.); 4 (sec.); 4 (sec.)
Winding thickness t_w	3 oz (105 μm)
Winding width b_w	100 mil (2.54 mm)
Core loss	50.6 W
Winding loss	18.9 W
Total loss	69.5 W
Efficiency	98.9%

= 8 is selected as the global optimal design, which has exactly the same core and winding structure shown in Fig. 2.12. The key parameters of the global optimal design are listed in Table 2.4.

To validate the global optimal design, electromagnetic FEA simulation and thermal CFD simulation are conducted for each unit U-I core. The results are shown in Fig. 2.15 and Fig. 2.16, respectively. From the electromagnetic simulation, the average B_{max} for the cross-section area is 114 mT, which basically coincides with the designed value. Then the generated core loss and winding loss are imported into the thermal model. The ambient temperature is set to be 20 °C and the planar trans-

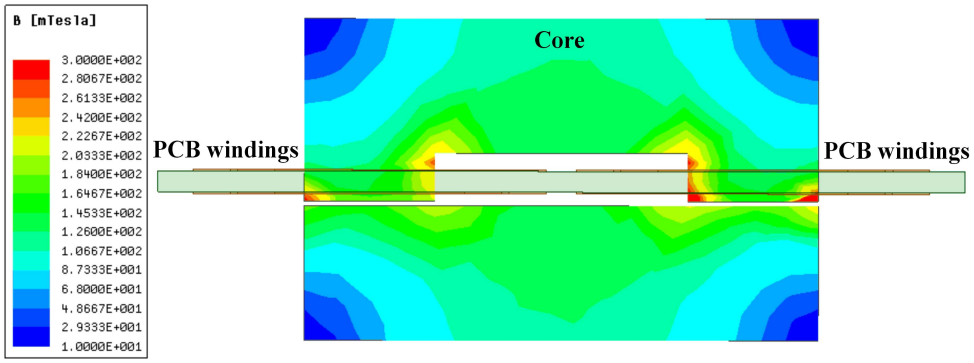


Figure 2.15: Electromagnetic FEA Simulation (Maxwell 3D Transient) for the Global Optimal Design.

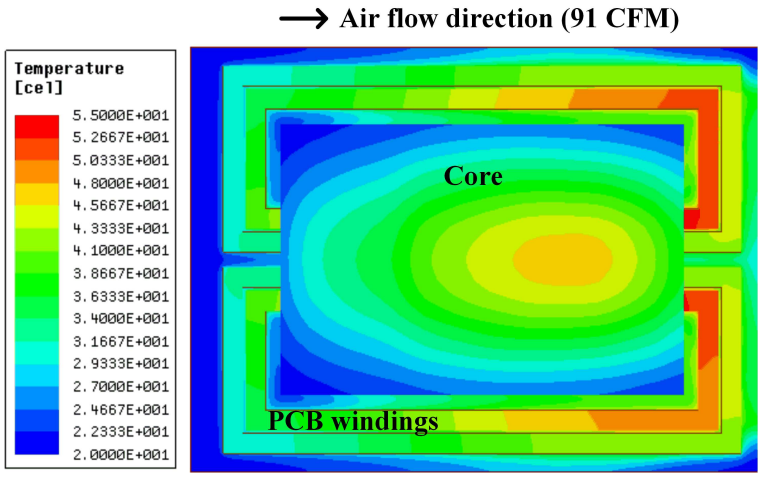


Figure 2.16: Thermal CFD Simulation (Icepak Steady-state) for the Global Optimal Design.

former receives 91 CFM forced-air cooling, which is the air flow of the selected fan blower. The simulated temperature rise is acceptable for this design, so the global optimal design is considered as final.

2.4 Experimental Verification

To validate the proposed transformer design, two planar transformers are designed for the 6.6 kW/500 kHz CLLC resonant converter by following the methodology proposed in this study. The first transformer prototype utilizes the conventional single

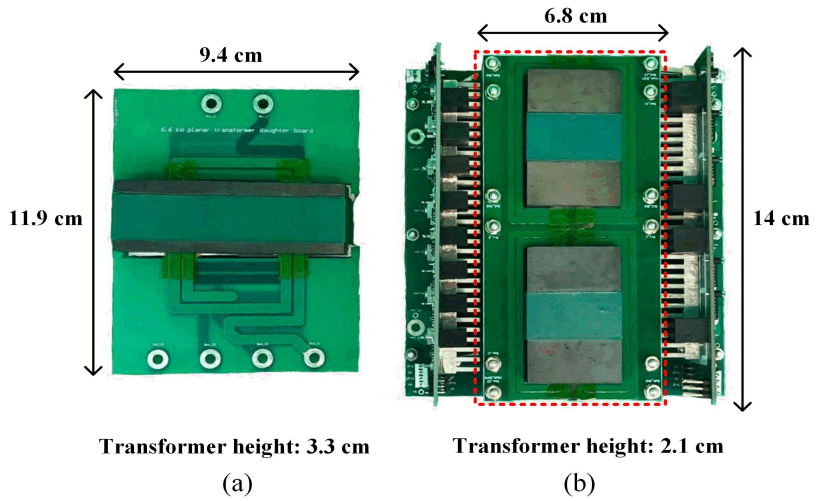


Figure 2.17: Pictures of the Two Planar Transformers. (a) Transformer 1. (b) Transformer 2.

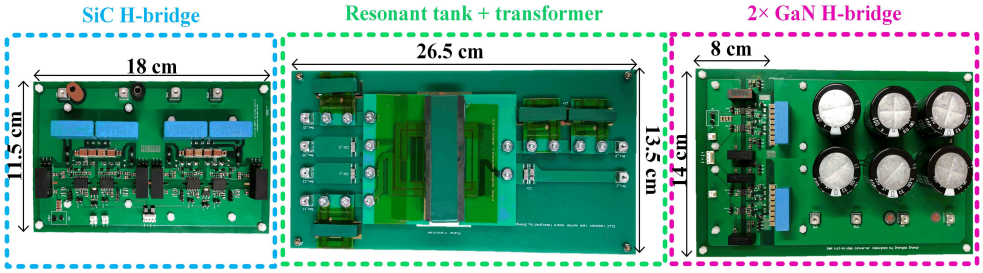


Figure 2.18: Modular-designed 6.6 kW/500 kHz CLLC Resonant Converter Prototype (Prototype 1).

E-I core with interleaved windings [Fig. 2.4(a)], while the second transformer employs the proposed core and winding configuration (Fig. 2.12). The two transformers are shown in Fig. 2.17. The key parameters are summarized in Table 2.5. To evaluate the circuit performance, two 6.6 kW/500 kHz CLLC resonant converter prototypes are built employing the two different transformer designs, respectively. The 6.6 kW full load tests are conducted for both prototypes. The battery charging profile is: when the battery voltage is below 300 V, the circuit output is controlled in the constant current mode (22 A); when the battery voltage is above 300 V, the circuit output is

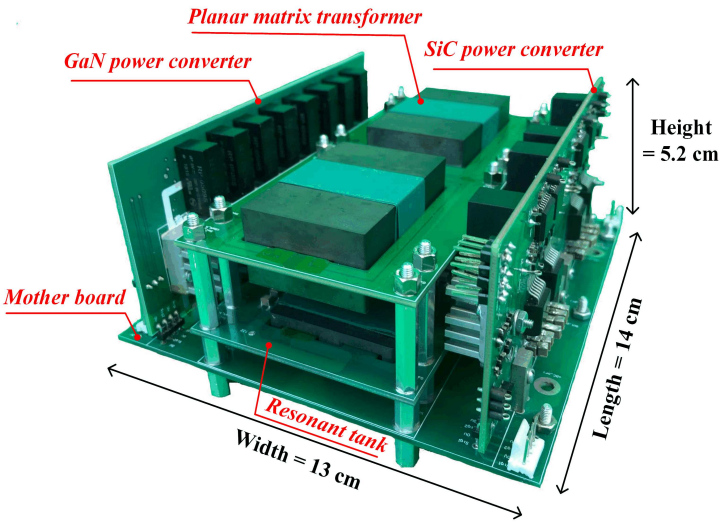


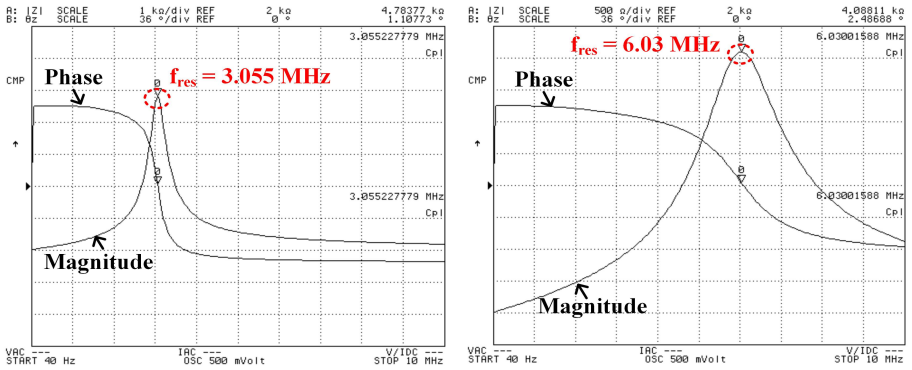
Figure 2.19: Integrated-designed High-power-density 6.6 kW/500 kHz CLLC Resonant Converter (Prototype 2).

controlled in the constant power mode (6.6 kW). Prototype 1 is a modular-designed CLLC resonant converter with transformer 1, as shown in Fig. 2.18. Prototype 2 is an integrated-designed high-power-density CLLC with transformer 2, as shown in Fig. 2.19. CREE C2M SiC MOSFET (C2M0080120D) is utilized in prototype 1 as the primary side switch, and CREE C3M SiC MOSFET (C3M0075120J) is utilized in the high-power-density CLLC converter (prototype 2). The two devices have similar R_{dson}, which presents the similar per unit current conduction loss. The only difference is that the latter device has 27.5% smaller junction capacitance, which presents 27.5% higher dv/dt under the same magnetizing current in the switching transient. The secondary side device is the same for the two CLLC resonant converters (GaN System GS66508B).

For the first challenge mentioned in the introduction, the high intra-winding capacitance introduced problems for soft-switching, transformer and converter efficiency, and waveform quality, the proposed design addresses them very well, which can be

Table 2.5: Key Parameters of Two Planar Transformer Prototypes.

Parameters	Transformer 1	Transformer 2
Core and winding configuration	Single E-I core with interleaved winding [Fig. 2.4(a)]	Proposed configuration (Fig. 2.12)
Power rating	6.6 kW	6.6 kW
Operating frequency	500 kHz	500 kHz
Number of cores	1	2
Core material	Hitachi ML27D	Hitachi ML27D
Core cross-section area	8.07 cm^2	4.75 cm^2
Maximum flux density	93 mT	118 mT
Number of turns	6 (pri.); 3 (sec.); 3 (sec.)	8 (pri.); 4 (sec.); 4 (sec.)
Winding thickness	3 oz (105 μm)	3 oz (105 μm)
Winding width	160 mil (4.06 mm)	100 mil (2.54 mm)
Magnetizing inductance	31 μH	31 μH



(a) (b)

Figure 2.20: (a) Measured Open-circuit Impedance Curve of Transformer 1 (Primary-referred). (b) Measured Open-circuit Impedance Curve of Transformer 2 (Primary-referred).

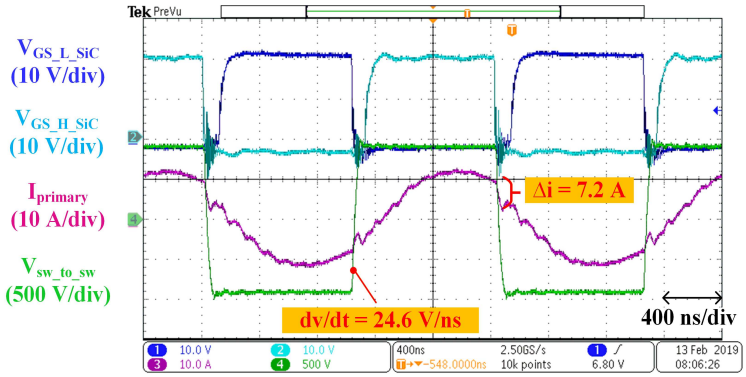


Figure 2.21: Measured Full-load Primary Side Waveforms of CLLC Resonant Converter Prototype 1 (450 V Battery Voltage and Charging Mode).

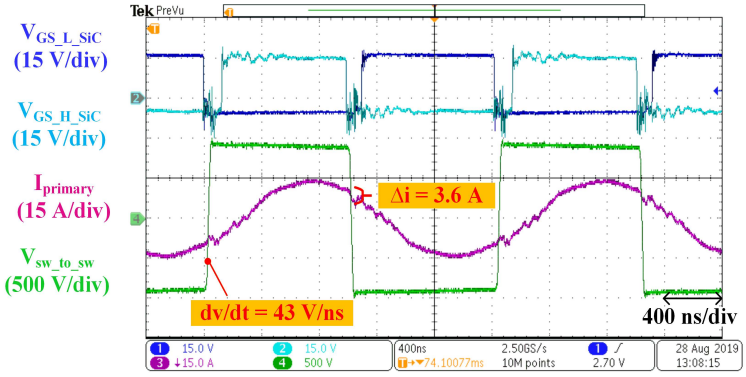


Figure 2.22: Measured Full-load Primary Side Waveforms of CLLC Resonant Converter Prototype 2 (450 V Battery Voltage and Charging Mode).

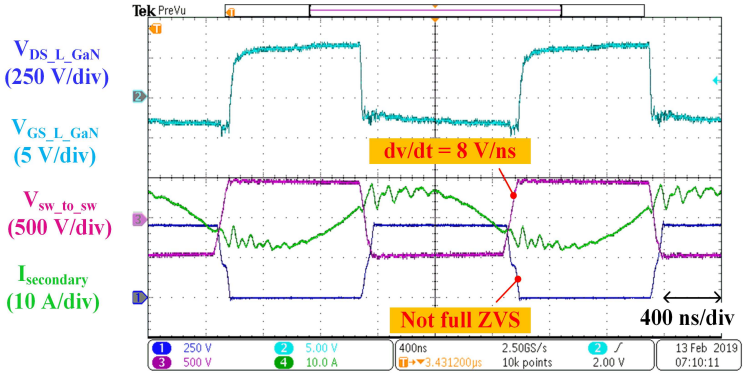


Figure 2.23: Measured Full-load Secondary Side Waveforms of CLLC Resonant Converter Prototype 1 (450 V Battery Voltage and Charging Mode).

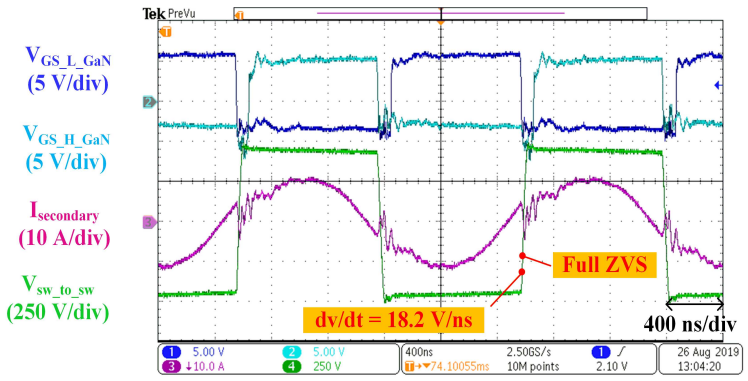


Figure 2.24: Measured Full-load Secondary Side Waveforms of CLLC Resonant Converter Prototype 2 (450 V Battery Voltage and Charging Mode).

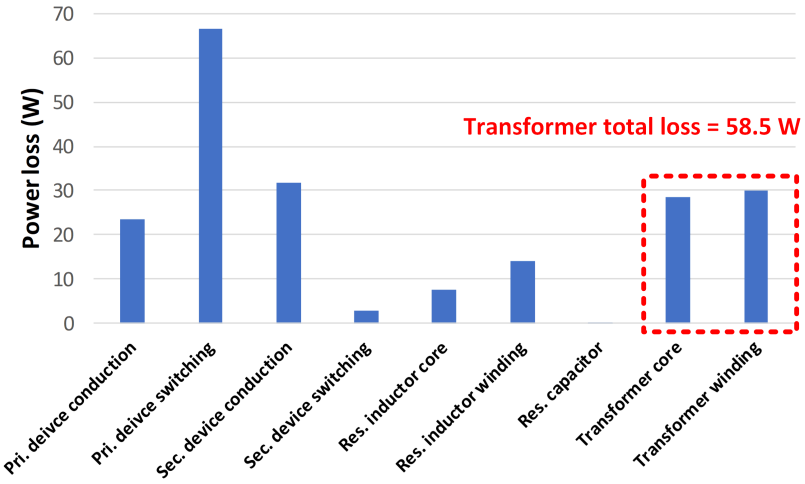


Figure 2.25: Power Loss Breakdown of CLLC Resonant Converter Prototype 1 (450 V Battery Voltage and Charging Mode).

verified from the impedance curves in Fig. 2.20 and experimental waveforms in Fig. 2.21 to Fig. 2.24.

First of all, the winding stray capacitance of the two transformers can be obtained through measuring the input impedance on the primary side (by Agilent 4294A Impedance Analyzer), while keeping the secondary side open-circuited. The measured impedance curves for the two transformers are shown in Fig. 2.20. Since the secondary side of the transformer is open-circuited, the resonance occurs between the

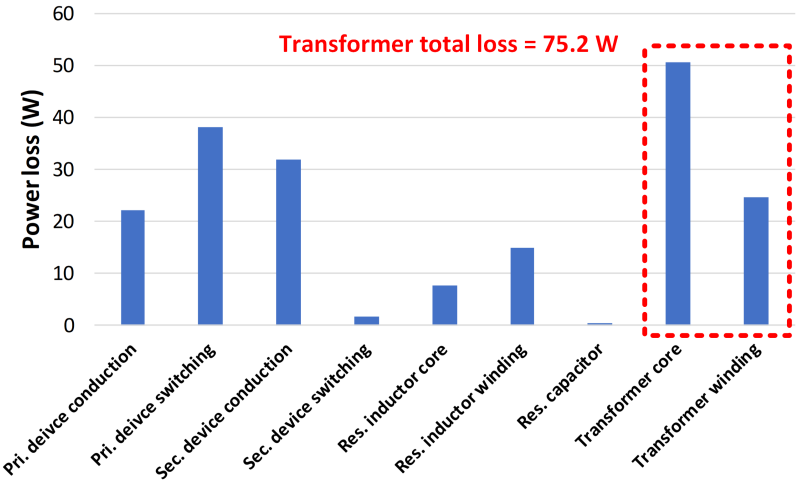


Figure 2.26: Power Loss Breakdown of CLLC Resonant Converter Prototype 2 (450 V Battery Voltage and Charging Mode).

transformer magnetizing inductance and the total winding stray capacitance referred to the primary side. Based on the resonance frequency of the impedance curve and the magnetizing inductance value (31 μH for both designs), the total stray capacitance for transformer 1 and transformer 2 can be calculated as 87.5 pF and 22.5 pF, respectively. Therefore, the total winding stray capacitance is almost cut down by four times compared with the conventional design (transformer 1).

Second, the soft-switching is fully achieved on both primary side and secondary side switches at full operating range for prototype 2. However, prototype 1 presents a soft-switching implementation with much lower dv/dt on primary side and partial hard-switching on the secondary side. As shown in Fig. 2.21 to Fig. 2.22, on primary side, the dv/dt of prototype 2 is 1.75 times of the dv/dt for prototype 1. Here, the dv/dt labeled in the figures are the dv/dt occurs between the two switching nodes. The dv/dt arises between the device drain-to-source is half of the labeled value. This 1.75 times dv/dt increase is due to two reasons. One is that the four times smaller winding stray capacitance in prototype 2 will draw much less current from the

magnetizing inductance, and the majority of the magnetizing current is used to charge and discharge the device junction capacitance during the switching transient. This can also be verified from the observation on the primary side current drop at the beginning of the dead-time. The magnitude of the current drop in prototype 1 (7.2 A as shown in Fig. 2.21) is twice than the current drop in prototype 2 (3.6 A as shown in Fig. 2.22). Another reason for the dv/dt increase is that the primary device in prototype 2 has 27.5% smaller junction capacitance, which results in 27.5% higher dv/dt. Since the final dv/dt increases by 75% from prototype 1 to prototype 2, the majority of the improvement comes from the winding stray capacitance reduction. This dv/dt improvement can benefit the efficiency (less switching loss). On the secondary side, the measured waveforms for prototype 1 and 2 are shown in Fig. 2.23 and Fig. 2.24, respectively. The ZVS is not fully achieved in prototype 1 due to the lack of the charging and discharging current during the switching transient, so additional hard-switching loss will be generated. For prototype 2, thanks to the significantly reduced winding stray capacitance, sufficient magnetizing current is diverted to the secondary side and ZVS is completely achieved at all operating conditions.

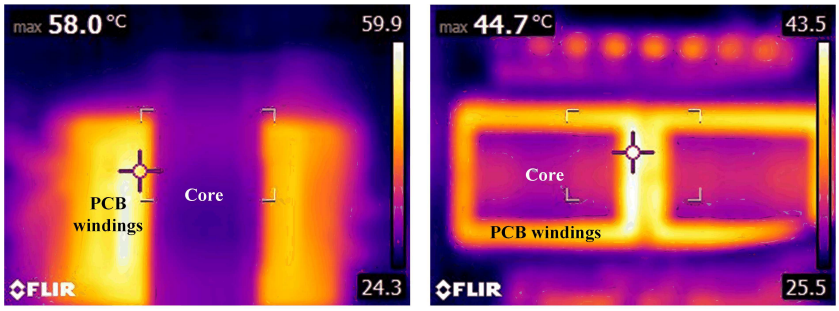
Third, the efficiency of prototype 2 is improved due to the stray capacitance reduction. Since prototype 1 and prototype 2 employ the same magnetizing inductance value, the conduction loss of the converters is similar. However, the much higher dv/dt in prototype 2 brings lower switching loss. Moreover, based on the testing waveforms for prototype 2, the dv/dt finishes much earlier than the end of the dead-time, which means the magnetizing current is sufficient to charge and discharge much larger junction capacitance. If the switch with higher current rating is selected, the conduction loss will be significantly reduced due to the lower R_{dson}.

Fourth, the ac current waveform quality in prototype 2 is improved, which can brings transformer loss reduction. The frequency of the ripple current increases from

10 MHz∼15 MHz to 20 MHz∼30 MHz (resonance between the resonant inductor and the winding stray capacitance), so the THD is reduced significantly.

For the second challenge mentioned in the introduction, the high inter-winding capacitance due to the conventional interleaved winding structure, the proposed design addresses it very well. The primary winding and secondary winding are placed on top and bottom layers, respectively, to cut down the large inter-winding capacitance, which is verified by the impedance curve Fig. 2.20 and experiment waveforms of Fig. 2.21 to Fig. 2.24. The total winding stray capacitance is reduced by 75%. At the same time, the leakage inductance and ac winding factor (the ratio of ac winding loss by dc winding loss) have been reduced as well. The measured leakage inductance for transformer 1 is around 350 nH, and for transformer 2 is around 100 nH, which is reduced by 72%. According to the measured efficiency for the two CLLC converter prototypes, the power loss breakdown for the two converters can be conducted, which are shown in Fig. 2.25 and Fig. 2.26, respectively. Based on the measured efficiency and the power loss breakdown, the winding loss of transformer 1 is 30 W, and the winding loss of transformer 2 is 24.6 W. The variance from the theoretical calculation is probably due to the connection and termination in the windings. The dc winding loss (calculated by winding DCR) in transformer 1 is 11 W, and in transformer 2 is 16.7 W. Therefore, the ac winding factor of transformer 2 is 46% lower than transformer 1. For transformer 1, since the interleaved winding structure is utilized, the leakage inductance and ac winding loss should be minimized. However, in practical implementation, since the PCB turns in the two non-adjacent layers need to be connected, the windings on the adjacent layers will not be perfectly vertically overlapped due to the insulation distance. Therefore, the leakage inductance and corresponding ac winding loss are increased due to the partial mis-alignment [Fig. 2.11 (c)]. For the proposed winding structure, because no connections are needed

for non-adjacent layers, the primary winding and the secondary winding can be perfectly vertically overlapped. The experimental results prove the characteristics of low-leakage-inductance and low-ac-winding-loss of the proposed winding structure.



(a) (b)

Figure 2.27: (a) Thermal Image of Transformer 1 under Full-load Testing. (b) Thermal Image of Transformer 2 under Full-load Testing.

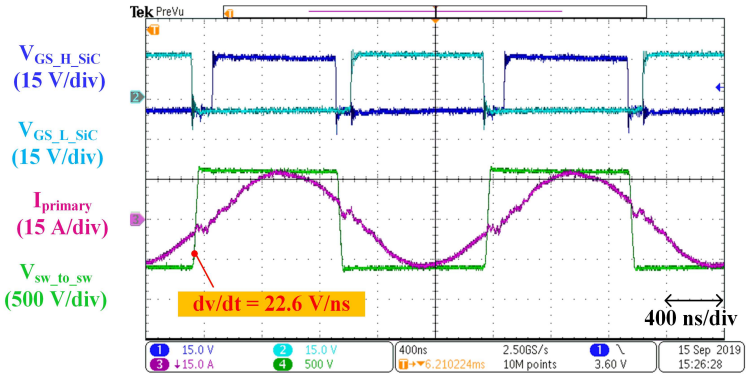


Figure 2.28: Measured Full-load Primary Side Waveforms of CLLC Resonant Converter Prototype 2 (300 V Battery Voltage and Charging Mode).

For the third challenge mentioned in the introduction, thermal management of the transformer, the proposed design addresses it very well. The pain-point of the thermal management in transformer is the temperature rise at the winding. By placing all the windings on top and bottom layers of the PCB only, the temperature rise can be kept low enough to avoid the need for heat sinks. Extra eddy current loss in the heat sinks will be produced if heat sinks are utilized to cool down the magnetic cores and

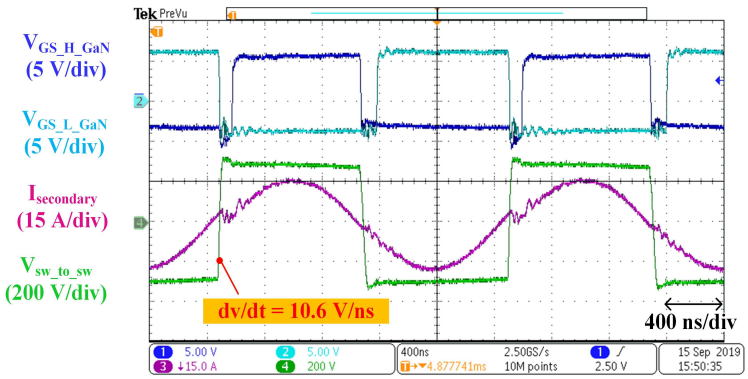


Figure 2.29: Measured Full-load Secondary Side Waveforms of CLLC Resonant Converter Prototype 2 (300 V Battery Voltage and Charging Mode).

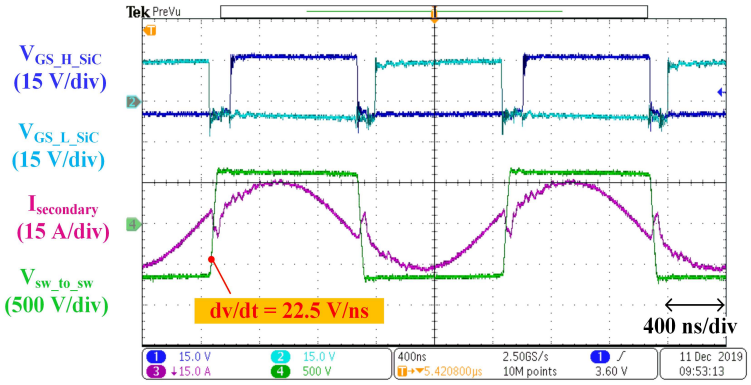


Figure 2.30: Measured Full-load Secondary Side Waveforms of CLLC Resonant Converter Prototype 2 (320 V Battery Voltage and Discharging Mode).

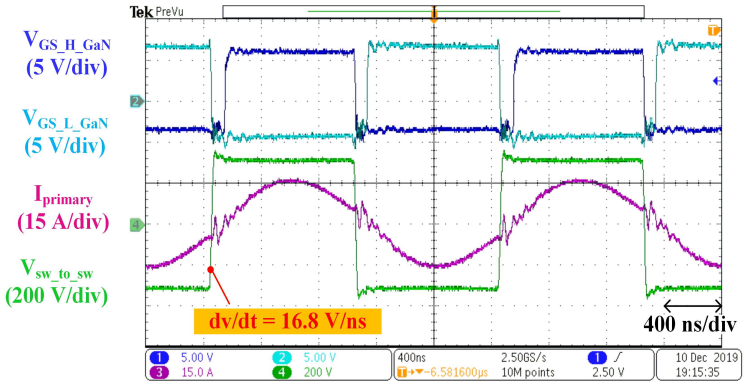


Figure 2.31: Measured Full-load Primary Side Waveforms of CLLC Resonant Converter Prototype 2 (320 V Battery Voltage and Discharging Mode).

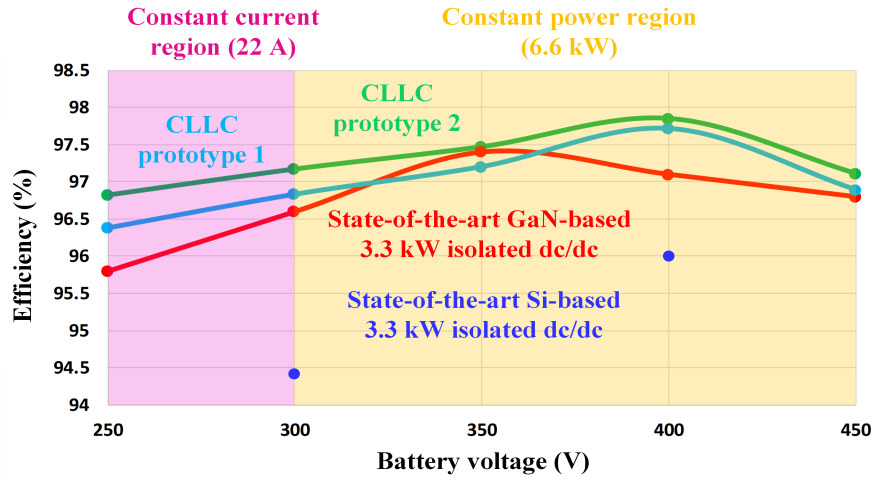


Figure 2.32: System Efficiency Curves for Different Battery Voltages (Charging Mode).

windings [96]. The improvement is verified by the temperature measurements during the full power testing. To compare the thermal performance of the two transformers. The two CLLC prototypes are tested under the same ambient temperature (20 °C) and the same cooling condition. The corresponding thermal images are shown in Fig. 2.27. The maximum temperature of transformer 2 is 44.7 °C at its winding hot spot. The maximum temperature of transformer 1 is 58 °C at its winding hot spot. The temperature rise of transformer 2 is 13.3 °C lower than transformer 1, even though the winding current density of transformer 2 is 1.6 times higher. The proposed winding structure has much better thermal dissipation capability. It should be mentioned that the experimental temperature rise for transformer 2 seems lower than the CFD simulation in Fig. 2.16. The testing time (around 10 minutes) may not be long enough for the transformer to reach its real thermal equilibrium, which results in the lower temperature rise, but the temperature distribution of the CFD simulation basically coincides with the experiment result.

Except addressing these three challenges, the optimization design methodology of

the transformer brings significant improvements on the converter efficiency and power density.

To verify the efficiency improvement, the efficiency measurements are conducted for the 6.6 kW/500 kHz high-power-density CLLC resonant converter (prototype 2) under different battery voltage scenarios. The circuit operates at constant current mode (22 A) at the low battery voltage range (250 V$\sim$300 V) and constant power mode (6.6 kW) at the higher battery voltage range (300 V$\sim$450 V). The experimental waveforms for the 300 V battery voltage and charging mode case are shown in Fig. 2.28 and Fig. 2.29, and waveforms for the 320 V battery voltage and discharging mode case are shown in Fig. 2.30 and Fig. 2.31. The efficiency is measured by Yokogawa WT500 Power Analyzer. The measured efficiency respect to different battery voltage in the charging mode is shown in Fig. 2.32. It is shown that the peak efficiency of the converter reaches 97.85% at battery voltage of 400 V. The full-load efficiency (battery voltage $\geq$ 300 V) maintains above 97% for the entire battery charging profile. Compared to prototype 1, the system efficiency is improved by 0.15%$\sim$0.45%, as shown in Fig. 2.32. Compared to the state-of-the-art GaN-based [97] and Si-based [98] counterparts, the proposed design (prototype 2) exhibits 0.45%$\sim$1.85% peak efficiency improvement and 0.54%$\sim$2.08% average efficiency improvement, as shown in Fig. 2.32.

In terms of the power density, both transformer and converters demonstrate significantly improved power density. For the transformer, the dimension changes from 11.9 cm$\times$9.4 cm$\times$3.3 cm to 14 cm$\times$6.8 cm$\times$2.1 cm, as shown in Fig. 2.17. Therefore, it is concluded that the proposed split core matrix transformer design and winding configuration enhance the power density of the transformer by 46%. For the entire power converter, the dimension shrinks from 14 cm$\times$60.5 cm$\times$4 cm to 14 cm$\times$13 cm$\times$5.2 cm, as shown in Fig. 2.18 and Fig. 2.19. Therefore, the CLLC system power

density is increased by 78%.

2.5 Conclusion

This study proposes a novel core and winding configuration of planar transformer to address the challenges of high intra-winding capacitance, high inter-winding capacitance and thermal management in the conventional planar transformers. The new design is verified through sufficient experimental tests. The test results validate that the proposed method can effectively address the three challenges, to achieve lower switching loss, lower transformer and converter loss, higher power density, and better thermal dissipation all at the same time. Moreover, the generalized design methodologies are proposed for the planar transformer. It is validated through experiments that the optimized efficiency and power density can be achieved by following the proposed design steps and rules. Two 6.6 kW/500 kHz CLLC resonant converter prototypes are built, tested and compared in the lab. The prototype 2, which employs the proposed transformer structure and the design methodologies, presents the outstanding 97.85% peak efficiency and 114 W/inch^3 power density.

Chapter 3

HIGH-DV/DT-IMMUNE, PARAMETER-ADAPTIVE SYNCHRONOUS RECTIFIERS GATE DRIVING SCHEME

As mentioned in the introduction, the precise and robust gate driving for synchronous rectifiers (SR) is very challenging in high-frequency and high-power-density converters. A high-dv/dt-immune and parameter-adaptive synchronous rectifier driving scheme is proposed and verified in this chapter. This chapter is organized as follows.

First, a full-GaN-based modular-designed CLLC resonant converter is introduced, which is used as the isolated DC/DC stage in an EV on-board charger. Then the operating principle of the proposed SR drain-to-source voltage sensing circuit is presented. Next, the post-processing circuit and the adaptive on-time tuning algorithm is introduced. The practical design guidelines and considerations are also presented for the proposed SR driving scheme. Finally, the proposed SR driving scheme is validated on the 3.3 kW/500 kHz full-GaN-based modular-designed CLLC resonant converter prototype.

3.1 Full-GaN-based Modular-designed CLLC Resonant Converter for EV OBC

With the emergence of wide-band-gap (WBG) power semiconductor devices, it is possible to upgrade the switching frequency to several 100 kHz or even MHz levels. The size of passive components will shrink a lot at very high switching frequency. Meanwhile, with the employment of soft-switching topologies, the excessive switching loss can be avoided. The size for the cooling system can be kept small. The system

power density can be significantly improved.

The synchronous rectifier is usually preferred rather than the conventional diode bridge rectifier to achieve higher efficiency. The SiC Schottky diode is utilized in [99] to cut down the diode reverse recovery loss. However, the forward voltage drop on a SiC Schottky diode is still higher than the voltage drop on a GaN device on-state resistance (R_{dson}) for the similar current rating. The conduction loss can be greatly reduced when the GaN-based synchronous rectifiers are employed.

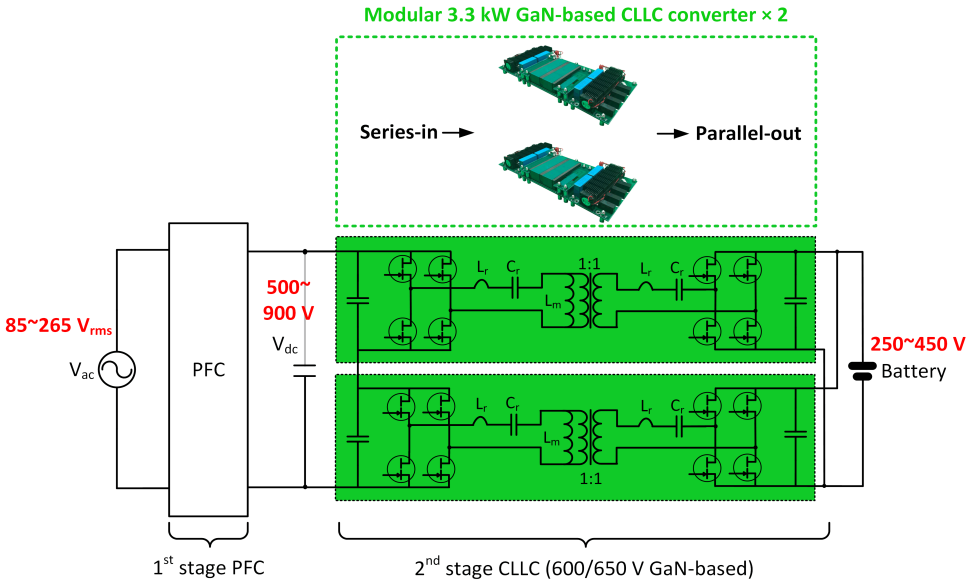


Figure 3.1: The Selected Structure of a Single-phase 6.6 kW Variable PFC DC-link EV On-board Charger with GaN-based SR.

The major drawback for LLC/CLLC resonant converter is the drop of efficiency when the operating frequency is far away from the resonant frequency. For the conventional fixed PFC dc-link solution (typically around 400 V), the voltage regulation range of the LLC/CLLC stage is large, due to the wide battery voltage (typically 250 V∼450 V) during the charging process. As a result, the operating frequency range of the LLC/CLLC stage is wide. To improve the system efficiency and the density of passive components, the variable PFC dc-link solution is adopted to maintain a nar-

Table 3.1: Parameters of a Single 1.2 kV/30 A SiC MOSFETs and Two 600 V/30 A GaN HEMTs.

Solutions	A single 1.2 kV/30 A SiC MOSFET	Two 600 V/30 A GaN HEMTs
Device part number	CREE C3M0075120J	Infineon IGOT60R070D1
Typical R_{dson}	75 mΩ	55 mΩ $\times$ 2
C_{oss}	58 pF	72 pF $\div$ 2

row switching frequency range at wide battery voltage [20–25]. An adequate topology for a 6.6 kW OBC is shown in Fig. 3.1. Instead of selecting 250 V$\sim$450 V as the dc-link voltage, it is more reasonable to select 500 V$\sim$900 V (twice of the battery voltage) since the PFC can only boost the voltage. H-bridge structures are selected instead of half-bridge structures, because the resonant capacitor does not need to block any dc-link voltage in H-bridge structures. The voltage rating of the resonant capacitor is significantly reduced and the small-packaged, low-profile ceramic capacitors can be employed to save the space. Two 600/650 V GaN-based H-bridges are series-connected on the primary side to sustain the 500 V$\sim$900 V dc-link voltage and two parallel-connected 600/650 V GaN-based full-bridge converters are employed on the battery side to reduce the conduction loss. This structure can be regarded as the series-in-parallel-out (SIPO) connection of two 1:1 dc transformers (DCX). The two dc transformers are identical, so each dc transformer is a 3.3 kW power converter module. A single 1.2 kV SiC-based H-bridge can be employed for the primary side as well [24, 25].

The off-the-shelf 1.2 kV/30 A SiC MOSFET and 600 V/30 A GaN HEMT are selected and the critical parameters are listed in Table 3.1. The equivalent R_{dson} of the two GaN HEMTs is 110 mΩ, which is 47% higher than the R_{dson} of a single

SiC MOSFET at the same current rating. However, the equivalent C_{oss} of the two GaN HEMTs is 36 pF, which is 38% lower than the C_{oss} of a single SiC MOSFET at the same current rating. It can be concluded that for the same operating condition, the SiC solution will exhibit lower conduction loss due to the lower R_{dson}. The GaN solution will exhibit lower switching loss due to the higher dv/dt (less over-lapping loss). Since the conduction loss is normally dominated in ZVS converters, the SiC-based solution has the advantage in terms of efficiency. However, the SiC-based solution will lose the benefits of the modular design. For the modular design, the primary side circuits and the secondary side circuits can be designed exactly the same, so it is easier to optimize the layout and power density for the unit power converter module. In this study, the modular-designed GaN-based solution is selected. It is reasonable to compromise a little bit of the efficiency to have a more compact and scalable modular design.

The biggest concern for the variable dc-link solution is the efficiency compromise of the PFC stage because of the elevated boost ratio. However, since the isolated dc-dc stage has more weight on the loss in the total loss chart, which is mainly due to the high-frequency transformer loss and the high conduction loss on the secondary side device. The loss reduction on the LLC/CLLC stage is higher than the loss increase on the PFC stage, so the overall efficiency is still enhanced [23].

For the variable dc-link solution, the variable-frequency-modulation for the LLC/CLLC resonant converter is still a must. Typically, the PFC dc-link has 5%$\sim$10% double-line frequency voltage ripple. If the LLC/CLLC resonant converter operates as a pure dc transformer, the double-line frequency harmonic current will flow into the battery and affect its lifetime [23, 25]. Therefore, it is necessary for the LLC/-CLLC to perform a small range of voltage regulation to compensate the double-line frequency voltage ripple from the PFC dc-link.

As long as the switching frequency is not at the resonant frequency, the gate signals of SRs are different from the gate signals of the corresponding primary switches. Even if the initial switching frequency equals the resonant frequency, the resonant frequency can shift for different load and different temperature conditions. Therefore, the gate signals of the primary side switches can not be directly utilized to drive the SR.

As mentioned in the introduction part, the SR is desired to be turned off exactly at the current zero-crossing moment (ZCS). If the SR is turned off earlier than the current zero-crossing moment, the current will go through the reverse channel of the switch at the gate-off period. Since the voltage drop of the reverse channel at the gate-off period is significantly higher than the voltage drop on the R_{dson}, additional conduction loss will be produced. The additional conduction loss is more severe for GaN device due to its unique reverse conduction characteristics. GaN device has low threshold voltage (typically around 1 V), hence, the negative turn-off voltage is preferred to avoid mis-triggering. With the employment of negative turn-off voltage, the reverse channel voltage drop of the GaN device at the gate-off period is elevated. For instance, for Infineon e-mode GaN (IGOT60R070D1), the reverse channel voltage drop can be higher than 6.4 V when -5 V gate turn-off voltage is applied. Therefore, it is very critical to achieve ZCS turn-off for the GaN-based SR in different operating conditions to improve the system efficiency. However, it is challenging to obtain the precise and robust gate driving for the SR in the high efficiency and high power density applications. As mentioned in the introduction part, the over-voltage and oscillation issues brought by the high dv/dt and high voltage during the switching transients for the controller side need to be addressed. Meanwhile, the early turn-off of the SR caused by the device package stray inductance should be solved as well.

3.2 Operating Principle of the Proposed SR Drain-to-source Voltage Sensing Circuit

The novel V_{ds} sensing circuit is the most critical part in the proposed SR driving scheme. To better explain the circuit operation, the self-driven mechanism of the auxiliary switches and the SR V_{ds} sensing/blocking function are presented separately as follows.

3.2.1 Self-driven Mechanism of the Auxiliary Switches

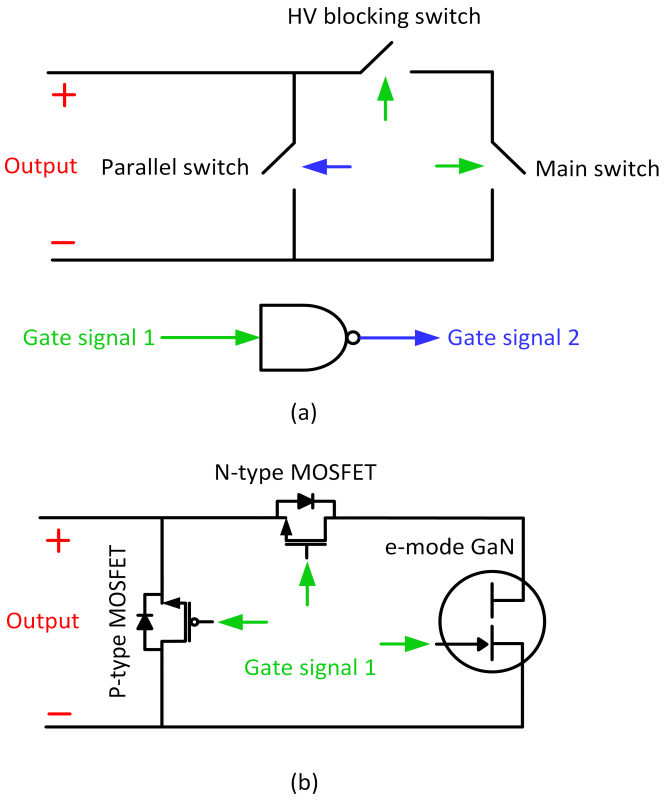


Figure 3.2: (a) Basic Topology with the Parallel Bypassing Branch. (b) Basic Topology with Self-driven Auxiliary Switches.

As mentioned in the introduction part, the displacement current induced by the high dv/dt may cause the over-voltage of the comparator/ SR driver chip (shown in

Fig. 1.10). A straightforward idea is to employ a low-impedance branch which is in parallel with the input of the comparator/SR driver to bypass the displacement current. This is the initial motivation for this novel voltage sensing circuit. However, this parallel branch should not affect the normal V_{ds} detection of the sensing circuit. Therefore, the parallel branch should be kicked in when the SR turns off, but it should be disconnected when the SR turns on. This function can be easily achieved by an auxiliary switch with the complimentary gate driving logic with the SR (main switch). Meanwhile, for the high voltage blocking MOSFET, it has the same gate driving logic with the SR. The basic sensing circuit topology is shown in Fig. 3.2(a).

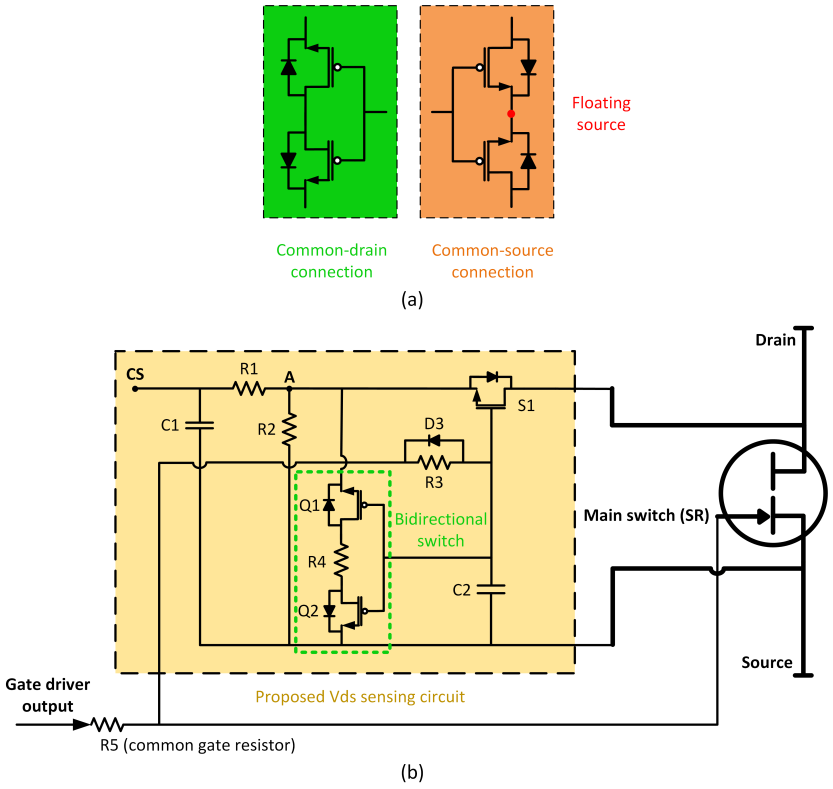


Figure 3.3: (a) Two Connections of P-type MOSFETs. (b) Schematic of the Proposed V_{ds} Sensing Circuit.

The next task is how to drive the auxiliary switches. If additional gate drivers are employed, it is hard to guarantee the synchronization with the main switch (SR) due

to the variance of the gate driver propagation delays. The self-driven approach is to drive all the switches with the original gate drive voltage alone. The complimentary gate driving logic can be accomplished by using a different type of semiconductor. For P-type MOSFET, the turn-on threshold voltage is negative, so this type of MOSFET will be turned on when the gate-to-source voltage is more negative than the threshold voltage. The basic self-driven topology is shown in Fig. 3.2(b). This topology has been implemented in the off-the-shelf commercial current sensing IC (Infineon IR25750LPBF). However, this IC can only measure the positive $V_{\rm ds}$ voltage, because the body diode of the P-type MOSFET will clamp the potential of the output (measured $V_{\rm ds}$) to almost zero once negative drain-to-source voltage is detected. A single P-type MOSFET can only sustain a unidirectional voltage. The bidirectional switch concept can be utilized to solve this problem. The two P-type MOSFETs should be connected in series to form a bidirectional switch to sustain the bidirectional $V_{\rm ds}$.

There are two ways to connect the two P-type MOSFETs in series, as shown in Fig. 3.3(a). Although the common source connection method guarantees the same gate-to-source voltages for the two switches, the source potential is floating. It is hard to control the switching event of the two switches due to the uncertain source potential. The common drain connection method is selected for this study, even though the gate-to-source voltages for the two switches are not exactly the same. It will be demonstrated later in this study that this connection achieves well-synchronized gate driving for the two P-type MOSFETs with only little timing difference.

The complete SR drain-to-source voltage sensing circuit is shown in Fig. 3.3(b). A small resistor (R_4) is added between the drains of the two switches. The extra resistor has little influence on the gate-to-source voltages of the two switches. The employment of the extra resistor has multiple purposes. First, it will limit the transient current flowing into Q_1, Q_2 and S_1 when a large negative $V_{\rm ds}$ occurs, as shown

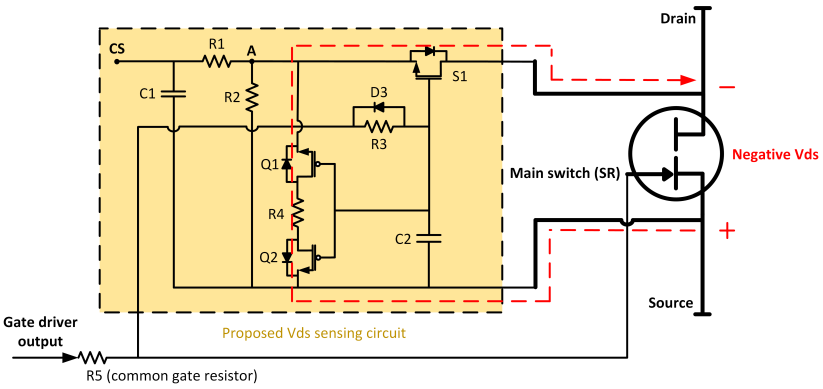


Figure 3.4: Transient Current Path During SR Early Turn-off or Delayed Turn-on Transient.

in Fig. 3.4. This phenomenon usually happens during the transients when the SR turns off before the current decays to zero (early turn-off) or when the SR turns on after the dv/dt transient finishes (delayed turn-on). In these transients, Q_1, Q_2 are on and S_1 is off. The current will flow through the reverse channel of the GaN switch while the negative gate-to-source voltage is applied. The amplitude of this negative V_{ds} voltage is typically several volts. Most of the negative V_{ds} voltage will drop on R_4 during these transients, hence, adequate resistance value should be selected to prevent the over-current/thermal damage for those low-current rating auxiliary switches. The peak of the transient current can be expressed by:

$$i_{\text{pk}} = \frac{|V_{\text{ds}}| - V_{\text{diode-S1}}}{2R_{\text{dson-Q}} + R_4} \tag{3.1}$$

where $V_{\text{diode-S1}}$ is the forward biased voltage of the body diode of S_1 and $R_{\text{dson-Q}}$ is the on-state resistance of the P-type MOSFETs.

Second, this resistor increases the impedance of the bidirectional switches to ensure the impedance of the Q_1-Q_2-R_4-S_1 series branch is larger than the impedance of the reverse channel of the SR at the gate-off state. Otherwise, the main current will flow through the Q_1-Q_2-R_4-S_1 series branch when the SR turns off early or turns on late, which may damage these low-current rating auxiliary switches. Although the SR

(main switch) is a high current rating device, due to the unique reverse conduction characteristic of GaN, the reverse channel impedance at gate-off period can be higher than the R_{dson} of the low-current rating Si device.

Last but not least, the resistor R_4 helps to damp the oscillation between the network capacitance and loop stray inductance. However, this resistor should not be too large to affect the low-impedance bypassing function for the displacement current. The detailed design equations of R_4 will be presented later. It should be mentioned that the reduction of the loop stray inductance is also very critical to suppress the oscillation induced by the high dv/dt. As shown in Fig. 1.10, the trace length between the drain of the SR and the input of the comparator/SR driver chip should be minimized and this trace should not be overlapped with the main current loop of the SR.

The resistor R_2 is a voltage divider resistor. When S_1 and the SR are on, R_2 and the R_{dson} of S_1 form a voltage divider. To guarantee the sensing accuracy, most of the sensed V_{ds} should drop on R_2. The output voltage before the filter (the point A to source voltage) can be written as:

$$V_{\text{A-to-source}} = \frac{R_2}{R_2 + R_{\text{dson-S1}}} \cdot V_{\text{ds}} \tag{3.2}$$

where $R_{\text{dson-S1}}$ is the on-state resistance of S_1. Therefore, the resistance of R_2 should be significantly higher than the R_{dson} of S_1.

To avoid the over-voltage for the control circuits (comparator/SR driver chip), the high voltage blocking MOSFET (S_1) should be turned on after the main switch is turned on and it should be turned off before the main switch is turned off in order to safely block the high output dc voltage. This function can be attained by R_3, C_2 and D_3 in the circuits [Fig. 3.3(b)]. The turn-on delay for S_1 is introduced by R_3 and C_2, while the turn-off action is much faster through the Schottky diode D_3. Since

the Si device has higher threshold voltage than the GaN device, S_1 should be turned off earlier than the main switch even with the same turn-off gate resistor (R_5). To increase the margin for the earlier turn-off, additional turn-off gate resistance can be applied for the main switch turn-off gate path.

A small output filter (R_1 and C_1) is utilized to remove the high frequency noise before the input of the comparator/SR driver chip. The filter size should not be too large to introduce too much delay and attenuation for the measured V_{ds}. The design equations for this output filter will be presented later as well.

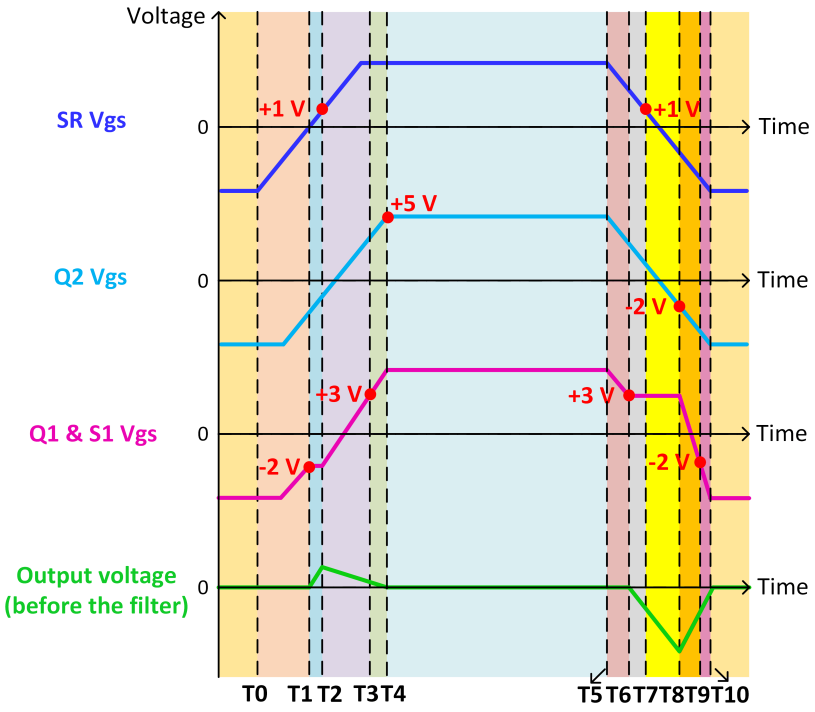


Figure 3.5: Theoretical Gate Driving Voltages for the SR and the Auxiliary Switches and the Output Voltage of the Sensing Circuit Before the Filter in One Switching Cycle.

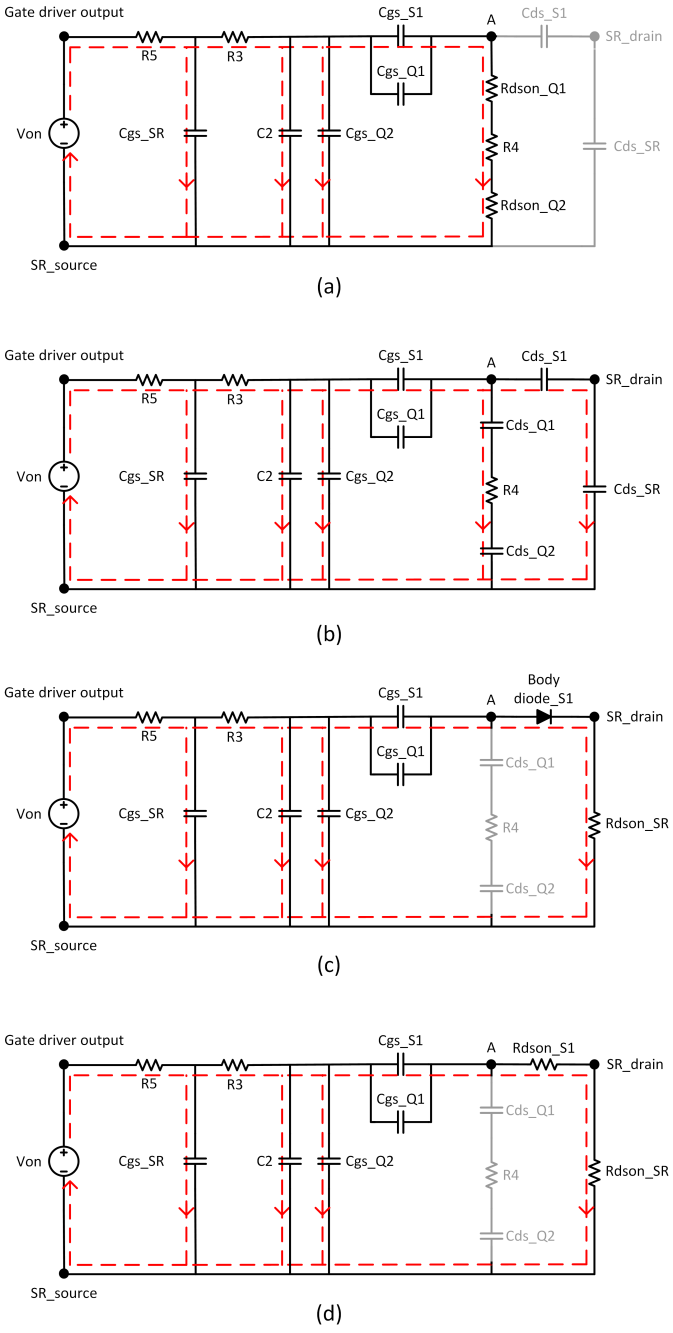


Figure 3.6: Equivalent Circuits for Different Intervals During the Turn-on Transient. (a) $T0{\sim}T1$. (b) $T1{\sim}T2$. (c) $T2{\sim}T3$. (d) $T3{\sim}T4$.

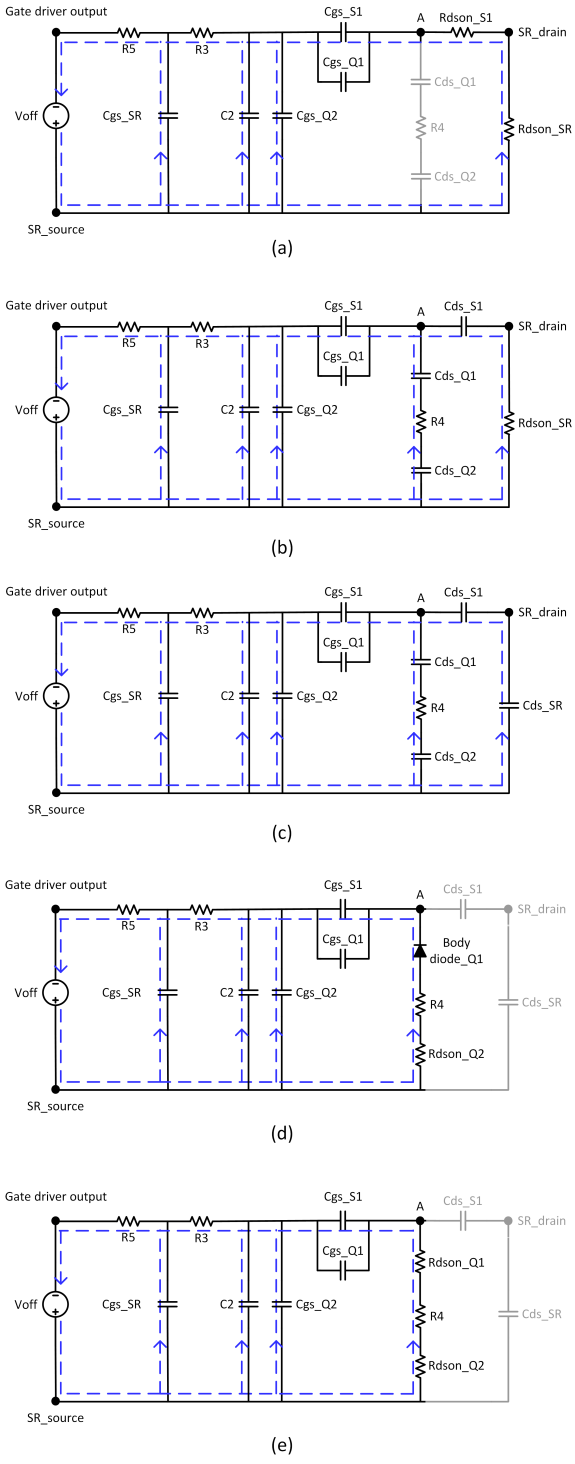


Figure 3.7: Equivalent Circuits for Different Intervals During the Turn-off Transient. (a) $T5{\sim}T6$. (b) $T6{\sim}T7$. (c) $T7{\sim}T8$. (d) $T8{\sim}T9$. (e) $T9{\sim}T10$.

After introducing the basic functions for each element in the proposed $V_{\rm ds}$ sensing circuit, the self-driven mechanism of the auxiliary switches will be explained as follows. To better present the operating principle, the following assumptions are made. The turn-on voltage from the gate driver output is +5 V. The turn-off voltage from the gate driver output is -5 V. The threshold voltage of the SR is +1 V. The threshold voltage of the N-type auxiliary switch (high voltage blocking MOSFET) is +3 V. The threshold voltage of the P-type MOSFET is -2 V. These assumptions are based on the actual device parameters. The theoretical gate driving voltages of the SR and the auxiliary switches are shown in Fig. 3.5. It should be noticed that the $C_{\rm gs}$ charging and discharging are shown to be linear for simplicity. Meanwhile, the output voltage of the sensing circuit before the filter (the point A to source voltage) is shown in Fig. 3.3(b) as well. The time-domain operation in each switching cycle is presented as follows.

1. Before $T0$. During this interval, the -5 V turn-off voltage is applied steadily on gate-to-source of the SR and all three auxiliary switches. Therefore, Q_1 and Q_2 are on; S_1 and the SR are off. It should be noticed that even though S_1 is off, the circuit is still capable of sensing the negative $V_{\rm ds}$ voltage through the body diode of S_1, as shown in Fig. 3.4.

2. $T0 \sim T1$. During this interval, the SR and S_1 begins to turn on, while Q_1 and Q_2 begins to turn off. Due to the turn-on delay introduced by R_3 and C_2, the rising of gate-to-source voltage for the auxiliary switches lags the rising of gate-to-source voltage for the SR. The equivalent circuit during this interval is shown in Fig. 3.6(a). Since Q_1 and Q_2 are still on, the voltage drop on the $R_{\rm dson}$ and R_4 is small. The $V_{\rm gs}$ of Q_1 and the $V_{\rm gs}$ of Q_2 are almost equal during this interval.

3. $T1 \sim T2$. This interval begins when the gate-to-source voltage of Q_1 and Q_2 increase above the threshold voltage (-2 V). At this time, Q_1 and Q_2 are off due to the driving logic of the P-type MOSFETs. The equivalent circuit during this interval is shown in Fig. 3.6(b). The C_{gs} of Q_1, the C_{gs} of S_1 and the C_{ds} of off-state switches form a capacitive voltage divider. The relation of the gate-to-source voltage for the three auxiliary switches during this interval can be expressed by:

$$\begin{aligned} V_{\text{gs-Q1}} = V_{\text{gs-S1}} = (Z_{\text{Cgs-S1}} // Z_{\text{Cgs-Q1}}) \cdot 1 / [Z_{\text{Cgs-S1}} // Z_{\text{Cgs-Q1}} + \\ (Z_{\text{Cds-S1}} + Z_{\text{Cds-SR}}) // (Z_{\text{Cds-Q1}} + R_4 + Z_{\text{Cds-Q2}})] \cdot V_{\text{gs-Q2}} \end{aligned} \tag{3.3}$$

Since the C_{ds} is usually much smaller than the C_{gs}, the impedance for the C_{ds} part is much higher. More voltage will drop on the C_{ds} part during this transient. The output voltage before the filter ($V_{\text{A-to-source}}$) increases due to the voltage drop on the C_{ds} part. For simplicity, it is assumed that the V_{gs} of S_1 and Q_1 remains the same during this interval (shown in Fig. 3.5).

4. $T2 \sim T3$. This interval begins when the gate-to-source voltage of the SR rises above its threshold voltage (+1 V). Then the R_{dson} of the SR and the body diode of S_1 will short the point A to the source. The charging for C_{gs} of S_1 and C_{gs} of Q_1 starts to accelerate. The equivalent circuit for this interval is shown in Fig. 3.6(c).

5. $T3 \sim T4$. This interval begins when the gate-to-source of S_1 climbs above its threshold (+3 V). Then S_1 is on and it can be regarded as a resistor in the equivalent circuit, as shown in Fig. 3.6(d). The positive gate driver power

supply will continue to charge the C_{gs} of Q_1, the C_{gs} of Q_2 and the C_{gs} of S_1 up to the supplied voltage (+5 V).

6. $T4{\sim}T5$. During this interval, the +5 V turn-on voltage is applied steadily on gate-to-source of the SR and all three auxiliary switches. Therefore, Q_1 and Q_2 are off; S_1 and the SR are on.

7. $T5{\sim}T6$. During this interval, the SR and S_1 begins to turn off, while Q_1 and Q_2 begins to turn on. Due to the existence of D_3, the discharging for the gate-to-source voltage of the SR and the discharging of gate-to-source voltage of Q_2 are almost synchronous. Since the SR and S_1 are still on, the V_{gs} of Q_1 and S_1 are almost equal to the V_{gs} of Q_2. The equivalent circuit during this interval is shown in Fig. 3.7(a).

8. $T6{\sim}T7$. This interval starts when the gate-to-source voltage of S_1 drops below the threshold voltage (+3 V). The equivalent circuit during this interval is shown in Fig. 3.7(b). The C_{gs} of Q_1, the C_{gs} of S_1 and C_{ds} of the off-state switches form a capacitive voltage divider. Since the SR is still on, it can be regarded as a resistor (R_{dson}). The relation of the gate-to-source voltage for the three auxiliary switches during this interval can be expressed by:

$$\begin{aligned} V_{\text{gs-Q1}} = V_{\text{gs-S1}} = (Z_{\text{Cgs-S1}} // Z_{\text{Cgs-Q1}}) \cdot 1/[Z_{\text{Cgs-S1}} // Z_{\text{Cgs-Q1}} + \\ (Z_{\text{Cds-Q1}} + R_4 + Z_{\text{Cds-Q2}}) // (Z_{\text{Cds-S1}} + R_{\text{dson-SR}})] \cdot V_{\text{gs-Q2}} \end{aligned} \tag{3.4}$$

Since the C_{ds} is usually much smaller than the C_{gs}, more voltage will drop on the C_{ds} part during this transient. The output voltage before the filter ($V_{\text{A-to-source}}$) changes due to the voltage drop on the C_{ds} part. For simplicity, it is assumed

that the V_{gs} of S_1 and Q_1 remains the same during this interval (shown in Fig. 3.5).

9. $T7 \sim T8$. This interval starts when the gate-to-source voltage of the SR drops below the threshold voltage (+1 V). The equivalent circuit during this interval is shown in Fig. 3.7(c). Since the SR is off, it should be regarded as a C_{ds} capacitor. The relation of the gate-to-source voltage for the three auxiliary switches during this interval can be expressed by:

$$\begin{aligned} V_{\text{gs-Q1}} = V_{\text{gs-S1}} = (Z_{\text{Cgs-S1}} // Z_{\text{Cgs-Q1}}) \cdot 1 / [Z_{\text{Cgs-S1}} // Z_{\text{Cgs-Q1}} + \\ (Z_{\text{Cds-Q1}} + R_4 + Z_{\text{Cds-Q2}}) // (Z_{\text{Cds-S1}} + Z_{\text{Cds-SR}})] \cdot V_{\text{gs-Q2}} \end{aligned} \tag{3.5}$$

Since the C_{ds} is usually much smaller than the C_{gs}, more voltage will drop on the C_{ds} part during this transient. The output voltage before the filter ($V_{\text{A-to-source}}$) continues to be reversely charged. For simplicity, it is assumed that the V_{gs} of S_1 and Q_1 still remains the same during this interval (shown in Fig. 3.5).

10. $T8 \sim T9$. This interval starts when the gate-to-source voltage of Q_2 decreases below its threshold voltage (-2 V). The negative power supply starts to charge the C_{gs} of Q_1 and the C_{gs} of S_1 through the R_{dson} of the SR, R_4 and the body diode of Q_1 branch. The equivalent circuit for this interval is shown in Fig. 3.7(d).

11. $T9 \sim T10$. This interval starts when the gate-to-source voltage of Q_1 decreases below its threshold voltage (-2 V). Then Q_1 can be seen as a resistor in the circuit at this time. The equivalent circuit for this interval is shown in Fig. 3.7(e). The negative power supply of the gate driver will continue to charge the gate-to-source capacitance of all the switches up to the supplied voltage (-5 V).

12. After $T10$. This interval is the same with the interval before $T0$. The -5 V turn-off voltage is applied steadily on the gate-to-source capacitance for all the switches. Therefore, Q_1 and Q_2 are on; S_1 and the SR are off.

There are several other critical points to be mentioned for the self-driven mechanism.

First, the turn-on delay of the auxiliary switches shown in Fig. 3.5 is not long. If the turn-on delay is long enough, the SR gate-to-source voltage may reach its threshold voltage before Q_1 and Q_2 are off. Then the turn-on process will jump from the process in Fig. 3.6(a) to the process in Fig. 3.6(c). Since Fig. 3.6(b) mode is skipped, the output voltage before the filter will not change. The longer turn-on delay time is preferred for hard switching scenarios to guarantee Q_1 and Q_2 are still on during the dv/dt transient. For hard switching scenarios, the dv/dt transient occurs when the SR gate-to-source voltage reaches its Miller plateau voltage, which is a little bit higher than the threshold voltage. During the dv/dt transient, Q_1 and Q_2 should be in the on-state to provide a low-impedance bypassing path for the displacement current. For the soft switching (ZVS) scenario, the turn-on delay can be designed shorter, because the dv/dt transient finishes before SR gate-to-source voltage starts to rise.

Second, for the output voltage before the filter, there is a negative pulse voltage during the turn-off transient, as shown in Fig. 3.5. As explained before, this negative pulse voltage is due to the gate-to-source voltage difference between Q_1 and Q_2. This negative pulse voltage needs to be filtered out, because it may affect the normal detection of the SR $V_{\rm ds}$. Fortunately, the pulse width of this voltage is very narrow. It typically only lasts for 5$\sim$20 ns, during which the gate-to-source voltage of the SR drops from its threshold to the turn-off voltage. A small output filter (R_1 and C_1)

will remove this pulse voltage with introducing little time delay.

Third, for the theoretical analysis, the switch is considered to be a constant R_{dson} resistor when the V_{gs} exceeds its threshold voltage and it is considered to be a C_{ds} capacitor when V_{gs} drops below its threshold voltage. In reality, once the V_{gs} drops, the channel resistance increases, hence, the voltage drop on the R_{dson} during the transient is larger for the real case. The real V_{gs} waveforms will be nonlinear, but the basic trend and characteristics will coincide with the theoretical linear analysis.

Last but not least, the gate-to-drain capacitance (C_{gd}) for all the switches are not presented in the equivalent circuits. Since C_{gd} is typically very small, the impedance of this capacitance is high during the transient. To simplify the equivalent circuits, the charging/discharging current through the C_{gd} path is not considered.

From the above analysis, it is clear that all the auxiliary switches can be driven by the original gate-to-source voltage for the SR alone. The V_{gs} of Q_1 and the V_{gs} of Q_2 are well-synchronized with only little timing difference.

3.2.2 SR Drain-to-source Voltage Sensing and Blocking

The proposed V_{ds} sensing circuits have six different operation modes in each switching cycle. The timing of the six operation modes for different SR turn-off scenarios are presented in Fig. 3.8.

1. Mode 1: The sensing circuit is in Mode 1 when the SR is off and its V_{ds} is the output dc voltage. For Mode 1, the high dc-link voltage is blocked by the body diode of S_1. Since Q_1 and Q_2 are on during this period, the output voltage before the filter ($V_{\text{A-to-source}}$) equals to the voltage drop on R_{dson} of the two P-MOSFETs and R_4, which is almost zero. The circuit diagram for Mode 1 is shown in Fig. 3.9.

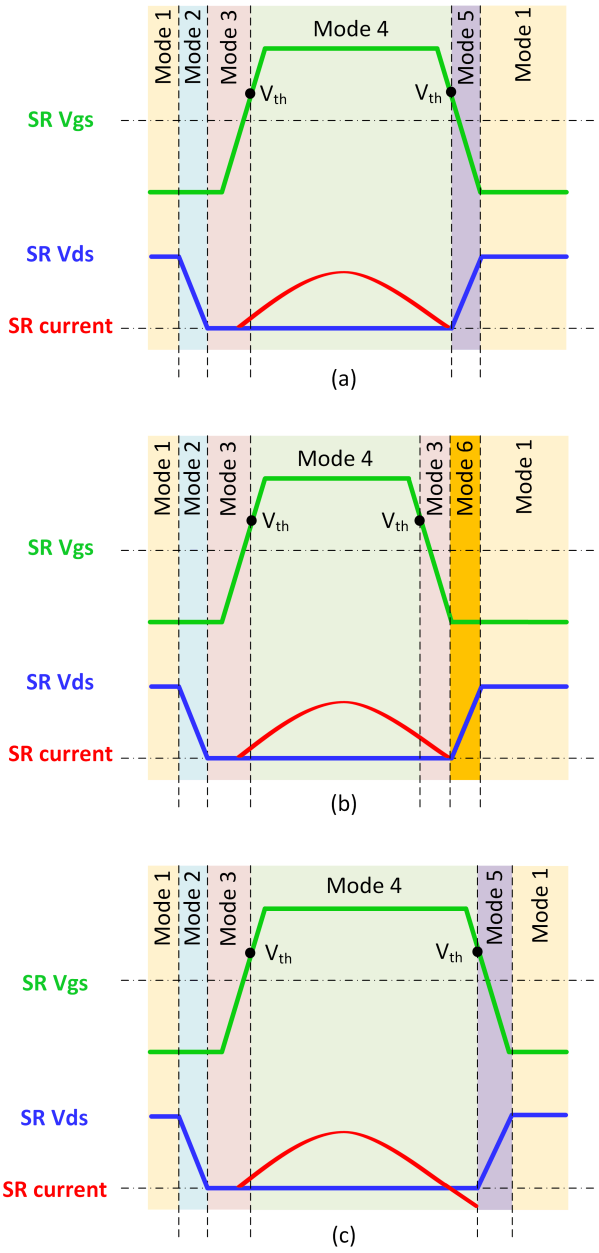


Figure 3.8: Timing of Different Operation Modes for Different SR Turn-off Scenarios. (a) ZCS Turn-off. (b) Early Turn-off. (c) Delayed Turn-off.

2. Mode 2: The sensing circuit is in Mode 2 when the $V_{\rm ds}$ of the SR drops. Due to the zero-voltage turn-on (ZVS) operation, the SR is not yet turned on during the $V_{\rm ds}$ falling transient. Therefore, Q_1 and Q_2 are still on, which provide a low impedance path for S_1 junction capacitance discharging current. Thus, the

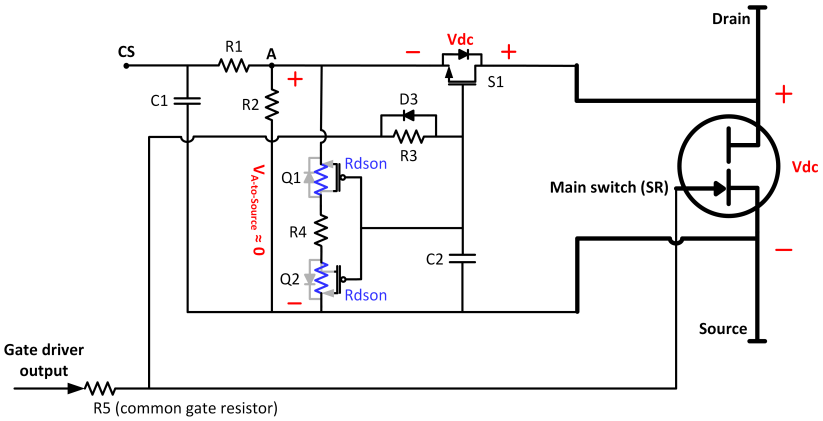


Figure 3.9: Circuit Diagram for Mode 1.

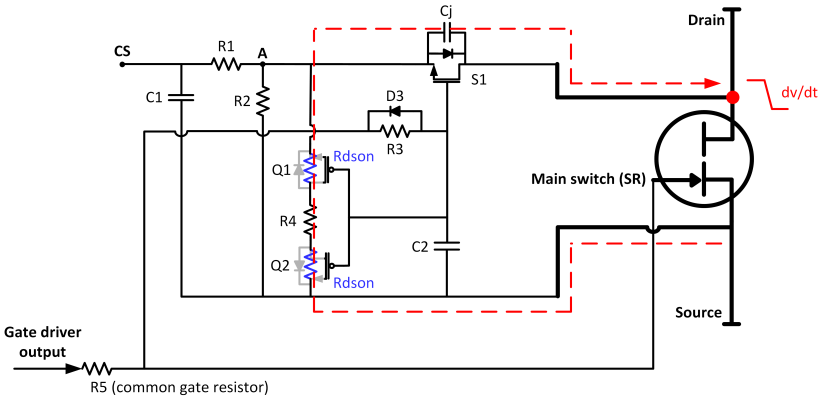


Figure 3.10: Circuit Diagram for Mode 2.

transient current will not flow into the output, which prevents the over-voltage of the comparator/SR driver chip. The circuit diagram for Mode 2 is shown in Fig. 3.10. The output voltage before the filter is still almost to zero.

3. Mode 3: The sensing circuit is in Mode 3 when a large negative V_{ds} occurs. As mentioned earlier, this phenomenon happens when the SR turns on after the dv/dt transient finishes or the SR turns off before the SR current decays to zero. Q_1 and Q_2 are still on during this period. The transient current will flow through Q_1, Q_2 and the body diode of S_1, as shown in Fig 3.4. Most of the V_{ds} drops on R_4 and its resistance value limits the amplitude of the transient

current. The output voltage before the filter almost equals to the large negative V_{ds} of the SR.

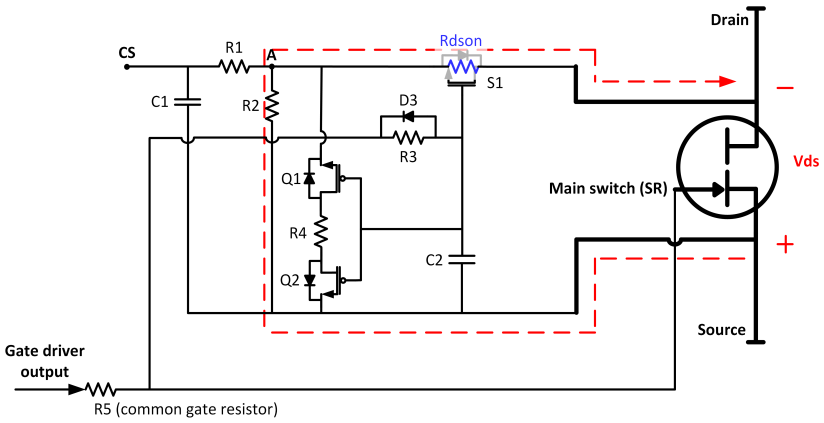


Figure 3.11: Circuit Diagram for Mode 4.

4. Mode 4: The sensing circuit is in Mode 4 when the SR is turned on. During this period, Q_1 and Q_2 are off; S_1 and the SR are on. R_2 and the R_{dson} of S_1 form a voltage divider to sense the V_{ds}. Since R_2 is significantly larger than the R_{dson} of S_1, the output of the sensing circuit is almost equal to the V_{ds} of the SR. The circuit diagram for Mode 4 is shown in Fig. 3.11. It should be mentioned that according to the self-driven mechanism of the auxiliary switches, which is shown in Fig. 3.5, the output of the sensing circuit can have a transient positive pulse voltage due to difference between the gate-to-source voltage of Q_1 and Q_2. This positive pulse voltage may influence the detection of the real V_{ds} of the SR. However, this transient lasts very short period. Moreover, the positive pulse voltage will not affect the adaptive SR on-time tuning. The adaptive SR on-time tuning algorithm only cares about the negative pulse voltage, which will be explained later in this study. After this short transient, the output of the sensing circuit before the filter will reflect the real V_{ds} of the SR.

5. Mode 5 and Mode 6: The sensing circuit is in Mode 5 when the SR is turned

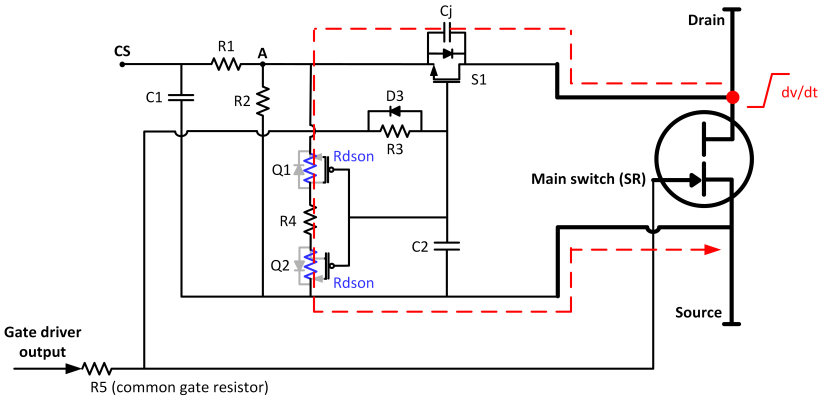


Figure 3.12: Circuit Diagram for Mode 6.

off and its drain-to-source voltage rises at the same time. The sensing circuit is in Mode 6 when the SR is turned off before its drain-to-source voltage rises. As shown in Fig. 3.8, Mode 5 happens for the SR ZCS turn-off and delayed turn-off scenarios and Mode 6 happens for the SR early turn-off scenario. For simplicity, the gate-to-source voltage and the dv/dt transient are shown to be linear in Fig. 3.8. Mode 6 is desired to guarantee the safe and reliable operation of the sensing circuit. The circuit diagram for Mode 6 is shown in Fig. 3.12. Since the dv/dt transient occurs after the SR is turned off, Q_1 and Q_2 are already on. The charging current for the junction capacitance of S_1 will flow through the low-impedance Q_1-R_4-Q_2 branch, which will not affect the output of the sensing circuit. However, if the dv/dt transient happens during the SR gate-to-source voltage falling transient, there will be a small interval (typically 5$\sim$20 ns) when Q_1 and Q_2 are not yet turned on, which is shown as $T7\sim T9$ in Fig. 3.5. During this period, Q_1 and Q_2 can not provide a low-impedance path to bypass the charging current for the junction capacitance of S_1. There are two approaches to address this issue. First, an extra gate resistor can be placed on the turn-off path of the SR. In this way, Q_1 and Q_2 will reach the threshold voltage (-2 V) before the V_{gs} of the SR falls below its threshold voltage (+1 V).

Then a low-impedance path can bypass the transient current introduced by the dv/dt. The second approach is to make the SR turn off a little bit earlier than the current zero crossing moment. Since the duration is very short (typically 5∼20 ns) and the SR current is close to zero, the efficiency compromise due to the extra conduction loss produced during the short interval can be negligible. The second approach is employed in this study. The 'very-short' early turn-off is achieved automatically by the output filter and the post-processing circuits, which will be explained in the next section.

To sum, the proposed SR drain-to-source voltage sensing circuit is capable of adequately sensing and blocking V_{ds} of the SR for any SR turn-off scenarios.

3.3 Post-processing of the Sensed SR Drain-to-source Voltage

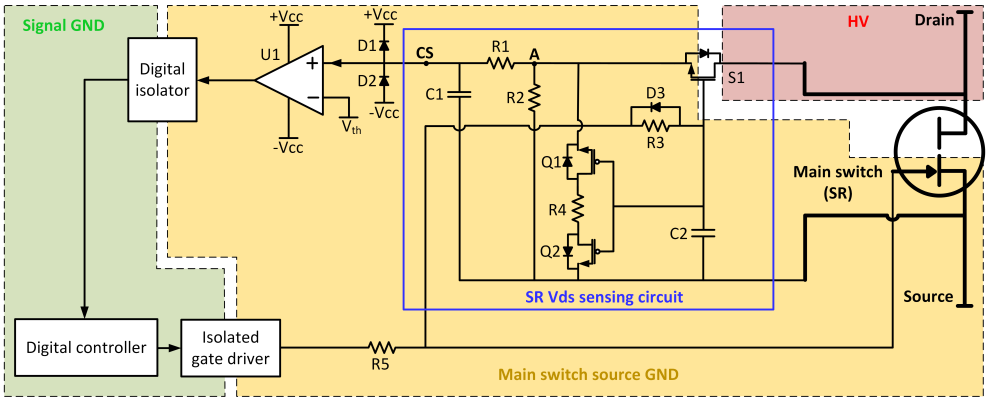


Figure 3.13: The Complete Schematic of the Proposed SR Driving Scheme.

The complete schematic of the proposed SR driving scheme is shown in Fig. 3.13. The isolated dc-dc power supply for the digital isolator and the gate driver is not demonstrated in this schematic. It should be mentioned that the digital isolator is not necessary for the secondary side low-side SR, because the signal ground is in the same potential with the source of the low-side switch.

A small output filter is employed after point A (shown in Fig. 3.13) to remove the high frequency noise with introducing little delay. Then the measured $V_{\rm ds}$ is compared by a negative threshold voltage. The magnitude of the negative threshold voltage should be higher than maximum voltage drop on the SR $R_{\rm dson}$ and lower than the voltage drop on the SR during the gate-off state. When $V_{\rm ds}$ of the SR equals to the output dc voltage, the input for the non-inverting terminal of the comparator ($U1$) is almost zero referred to the source. Therefore, the output of the comparator is high for this condition. When the SR is reversely conducted at the gate-on period, a small negative voltage will be sensed by the non-inverting terminal of the comparator. The output of the comparator is high as well. Only when the SR is reversely conducted at the gate-off period, the potential on the non-inverting terminal will be lower than the potential on the inverting terminal. Then the output of the comparator goes low. By detecting the low state or the falling edge of the comparator output, the state of the gate for the SR is known.

Next, the output of the comparator is transferred to the controller. The adaptive algorithm is implemented in the controller [52]. The logic of the adaptive SR on-time tuning algorithm is shown in Fig. 3.14. It should be noticed that there is a low-state before the SR is tuned on. It is because the SR is not turned on right after the dv/dt transient finishes, which is normal due to the design margin for the dead-time. The second low-state reflects the SR turn-off timing, hence, the detection zone should starts after the turn-on of the SR. In this study, the detection zone starts at 1/4 of one switching cycle. Eventually, the SR will jump between 'State C' and 'State D' shown in Fig. 3.14. The ΔT represents the unit tuning step in the controller and it is selected to be 6.67 ns in this study. By employing the adaptive on-time tuning algorithm, the SR achieves the shortest gate-off reverse channel conduction. It should be mentioned that one of the benefits of the adaptive on-time tuning algorithm is its good sensitivity

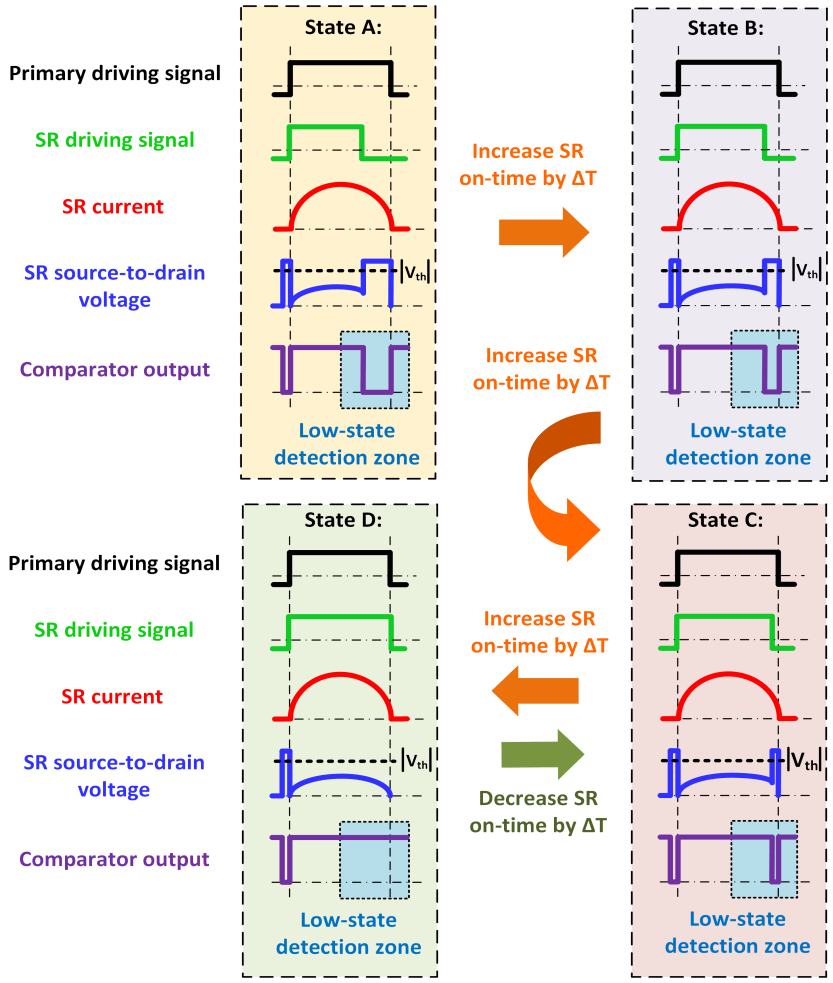


Figure 3.14: The Adaptive SR On-time Tuning Logic.

to the low current and excellent immunity to the noise. For the conventional method, the SR turn-off timing is totally based on when the sensed drain-to-source voltage magnitude drops below the turn-off threshold. Since the magnitude of the turn-off threshold is typically very small (around 10 mV), it is very hard to differentiate the voltage drop of the normal conduction and the noise voltage. For the adaptive on-time tuning approach, only one high threshold voltage is needed to detect whether the reverse conduction at the gate-off period occurs. The source-to-drain voltage drop at the gate-off period of GaN is significantly higher than the source-to-drain voltage drop for the gate-on period regardless of the drain current. The threshold

voltage can be set far away from zero, which brings good immunity to the noise. The adaptive SR on-time tuning approach does not care about the source-to-drain voltage magnitude during the gate-on periods, hence, this approach has no issues in low current conditions.

The Schottky diodes D_1 and D_2 are utilized to prevent the input positive over-voltage and negative over-voltage for the comparator (just for protection). The comparator should be powered by a dual power supply, because a negative threshold voltage is needed. The negative threshold voltage can be generated from a resistive voltage divider between the source and the negative power supply ($-V_{\text{cc}}$). It should be mentioned that the capacitance for the output RC filter includes C_1, the junction capacitance of D_1 and D_2 and the input capacitance of the comparator (U_1). Therefore, the time constant for the output filter can be written as:

$$\tau = R_1 \times (C_1 + C_{\text{D1}} + C_{\text{D2}} + C_{\text{input-U1}}) \tag{3.6}$$

This output filter will remove the high frequency noise, as well as very short negative pulse. The very short negative pulse should be filtered out for the following reasons. First, the self-driven mechanism can produce a short negative pulse (5$\sim$20 ns), as shown in Fig. 3.5. This negative pulse needs to be removed, otherwise, the on-time of the SR will be increased all the time due to the detection of the low-state. Second, as mentioned earlier, to ensure the low-impedance path to bypass the transient displacement current, the SR should be turned off a little bit earlier than the current zero-crossing moment, as shown in Fig. 3.8 and Fig. 3.12. The very short negative pulse is eliminated by the output filter, so the comparator can only detect the negative pulse longer than some duration. The duration of the undetected negative pulse is the period of SR early turn-off. In this way, the SR will be turned off a little bit earlier than the actual current zero-crossing moment automatically.

The transient displacement current will be safely bypassed and the compromise of the efficiency is almost negligible due to the very short duration of the early turn-off.

3.4 Practical Design Guidelines and Considerations for the Proposed SR Driving Scheme

3.4.1 Auxiliary Switches

As shown in Fig. 3.13, the voltage rating of S_1 should be higher than the maximum output dc voltage and the voltage rating of Q_1 and Q_2 should be higher than the maximum voltage drop of the SR at gate-off state.

The low-current rating auxiliary switches can be preliminarily selected. Typically, the current rating can be from tens of mA to 2 A. R_4 can be designed to limit the peak of the transient current according to (3.1).

3.4.2 Turn-on Delay Circuit

The turn-on delay circuit for the auxiliary switches includes R_3, C_2, as well as the gate-to-source capacitance of the switches. Since the equivalent circuit changes during the turn-on transient, the time constant should be in a certain range. According to the equivalent circuits in Fig. 3.6, the time constant of the turn-on delay circuit can be expressed as:

$$R_3 \times (C_2 + C_{\text{gs-Q2}}) < \tau < R_3 \times (C_2 + C_{\text{gs-Q2}} + C_{\text{gs-Q1}} + C_{\text{gs-S1}}) \tag{3.7}$$

As mentioned earlier, due to the ZVS operation of the switches in LLC/CLLC, the turn-on delay can be designed shorter, which can be tens of nanoseconds. For hard switching applications, the turn-on delay should be longer to ensure the dv/dt transient finish prior to the turn-on of S_1.

3.4.3 Voltage Divider Circuit

When S_1 is on, the R_{dson} of S_1 and R_2 form a voltage divider, as shown in Fig. 3.11. The R_{dson} of the 600-V/tens-of-mA N-type MOSFET is typically from tens of Ohm to one hundred Ohm. Therefore, a good selection for the R_2 is tens of kilo-Ohm.

3.4.4 Current Limit Resistor

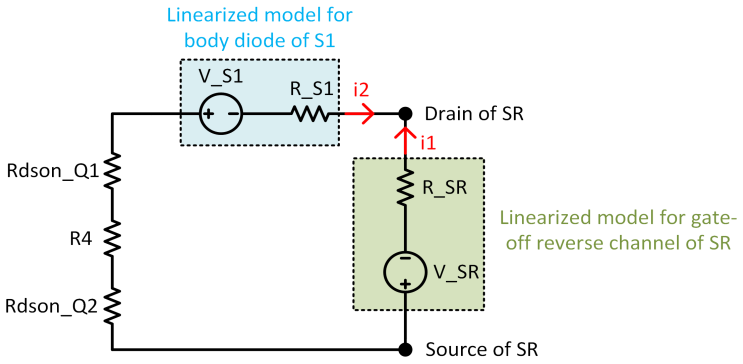


Figure 3.15: Equivalent Circuit During the SR Delayed Turn-on or Early Turn-off Periods.

R_4 is a critical component in this circuit. As mentioned before, R_4 has multiple functions. First, R_4 needs to provide a low-impedance path for the transient displacement current. Second, R_4 will limit the magnitude of the transient current flowing through the auxiliary switches. Last but not least, R_4 should be large enough to ensure the impedance of the Q_1-Q_2-R_4-S_1 series branch is larger than the impedance of the reverse channel of the SR at the gate-off state. Otherwise, the main current will flow through the Q_1-Q_2-R_4-S_1 series branch when the SR turns off early or turns on late, which may damage these low-current rating auxiliary switches.

The first two conditions can be easily expressed as:

$$\begin{aligned} R_4 &<< R_1 + \frac{1}{2\pi f_{\text{BW}} \cdot C_{\text{total}}} \\ R_4 &> \frac{|V_{\text{ds-max}}|}{i_{\text{pk-max}}} \end{aligned} \tag{3.8}$$

where f_{BW} is the equivalent bandwidth for the dv/dt transient; C_{total} is the total capacitance for the input of the comparator; $V_{\text{ds-max}}$ is the maximum SR drain-to-source voltage drop during the gate-off period (before the rise of the dv/dt); $i_{\text{pk-max}}$ is the maximum allowable pulse current restricted by the auxiliary switch current rating. In (3.8), if a value is ten times smaller than another, it can be considered as 'far less than'.

For the last condition, it can be analyzed by the equivalent circuit in Fig. 3.15. During the SR delayed turn-on or early turn-off periods, if the gate-to-source voltage of the SR is negative, the GaN-based SR will exhibit the behavior of a diode with a large voltage drop. For simplicity, the body diode behavior of S_1 and the 'diode-like' behavior of the GaN-based SR can be linearized. Meanwhile, R_{dson} of Q_1 and Q_2 can be ignored due to their small value. Then the following relations need to be satisfied:

$$\begin{aligned} i_2 &= \frac{V_{\text{SR}} - V_{\text{S1}}}{R_4 + R_{\text{S1}}} + \frac{R_{\text{SR}}}{R_4 + R_{\text{S1}}} \cdot i_1 \\ \frac{V_{\text{SR}} - V_{\text{S1}}}{R_4 + R_{\text{S1}}} &<< i_{\text{load}} \\ i_2 &<< i_1 \end{aligned} \tag{3.9}$$

where V_{S1}, R_{S1}, V_{SR} and R_{SR} are the linearized parameters shown in Fig. 3.15; i_2 is the current flowing in the auxiliary switches; i_1 is the current flowing in the SR and i_{load} represents the rated load current.

Equation (3.9) will determine another lower limit of R_4.

3.4.5 Output Filter

For the output filter, it should filter out the unwanted short negative pulse with introducing little time delay. The time constant (τ) for the output filter should satisfy:

$$\frac{1}{1+2\pi f_{\text{unwanted}} \cdot \tau} < \frac{V_{\text{th}}}{-V_{\text{cc}}} \tag{3.10}$$

where f_{unwanted} is the bandwidth of the unwanted narrow pulse; $-V_{\text{cc}}$ is the negative power supply for the gate driver and V_{th} is the threshold voltage for the comparator.

3.4.6 Turn-on Timing for the SR

The turn-off timing of the SR has been discussed throughly through this study. By implementing the proposed SR driving scheme, the SR almost attains the ZCS turn-off for any scenarios. The turn-on timing for the SR is critical as well. If the SR is turned on before the dv/dt transient finishes, the circulating current will occur, which will introduce extra loss. If the SR is turned on much later than the end of the dv/dt transient, the load current will flow through the reverse channel of the GaN device during the gate-off period and additional loss will be generated as well. The ideal turn-on timing is to turn on the SR right after the dv/dt transient finishes. It is hard to achieve this timing by using open-loop methods, because the duration for the dv/dt transient changes for different operating conditions. As mentioned in the introduction part, the commercial SR driver chip detects the first large voltage drop of V_{ds} of the SR and then outputs the turn-on signal. This method usually has long turn-on delay, which is typically from 80 ns to 200 ns. The additional conduction loss during the delay can be significant for the high-frequency-operation of GaN devices.

In this study, the open-loop turn-on method is taken. First, the primary side switch needs to have sufficient dead-time to guarantee the ZVS for both primary side switches and secondary side switches under all operating conditions. The minimum

required dead-time for the primary switch can be calculated as,

$$t_{\text{d-min}} = (1+\nu) \cdot 8(C_{\text{oss1}} + C'_{\text{oss2}} + C_{\text{stray}}) \cdot f_{\max} \cdot L_{\text{m}} \tag{3.11}$$

where ν represents the margin; C_{oss1} is the junction capacitance for the primary side device; C'_{oss2} is the junction capacitance of the secondary side device referred to the primary side; C_{stray} is the winding stray capacitance referred to the primary side; $f_{\max}$ is the maximum operating frequency and L_{m} is the magnetizing inductance.

Second, the turn-on timing of the SR should be exactly the same with the corresponding primary side switch. With the employment of sufficient dead-time, the dv/dt transient should already finish for both primary side and secondary side prior to the turn-on of the primary side switches. Therefore, the SR can be turned on right after the end of the dead-time without the worry of hard-switching or circulating current. It should be also mentioned that, in this study, the primary side and secondary side switches and gate driver circuits are exactly the same, which makes the propagation delay for both sides almost the same. This is one of the advantages of the modular design. If the switches or the gate driver circuits are not the same for the primary side and the secondary side, extra effort needs to be spent on compensating the propagation delay difference.

The dead-time is designed for the worst scenario and some margin is usually reserved as well. Therefore, for most of the operating conditions, there will be some delay (around 10∼50 ns) between the end of the dv/dt transient and the turn-on starting point of the SR. However, the extra loss produced during this period is significantly reduced compared with the commercial SR drivers, which typically has 80∼200 ns turn-on delay.

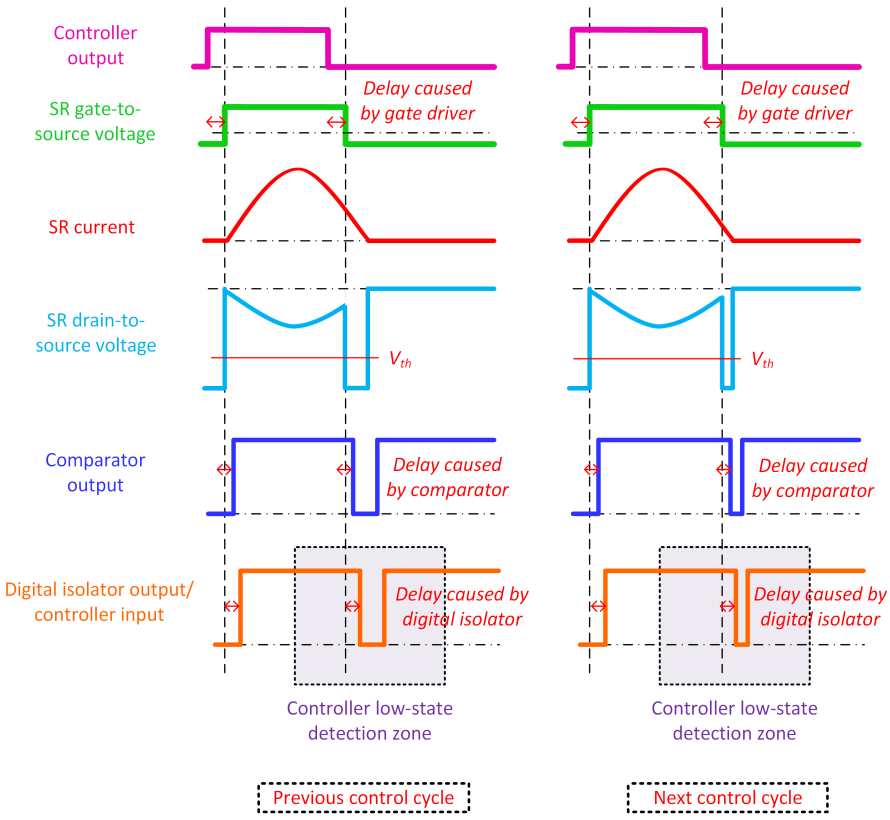


Figure 3.16: Timing Diagram of Signals for Each Stage of the Proposed SR Driving Scheme.

3.4.7 Propagation Delay in the Path

Actually, one of the benefits for the adaptive SR on-time tuning approach is the independence of the propagation delay in the path. The SR gate signal is not directly generated by the measured drain-to-source voltage. Instead, the SR turn-on timing is synchronized with the corresponding primary switch and the SR on-time duration is tuned adaptively based on the logic of whether the reverse conduction at the gate-off period occurs. Therefore, the propagation delays in the path will not affect the SR gate signal timing.

The timing diagram of signals for each stage is shown in Fig. 3.16. For the previous control cycle, the controller gives a certain width of on-state signal for the SR. Since

the SR is turned off before its current declines to zero, there will be a duration of high source-to-drain voltage drop due to the reverse conduction at the gate-off period. This sensed SR drain-to-source voltage will be compared with the threshold voltage (-2.5 V). Next, the comparator outputs the corresponding logic signal. If the sensed voltage is lower than the threshold, the output of the comparator will go low. Otherwise, the comparator output will keep high. There will be typically tens-of-nanosecond delay between the comparator input pulse and comparator output pulse, as shown in Fig. 3.16. Then the comparator output will go through the digital isolator. The logic will keep the same, but another tens-of-nanosecond delay will be introduced by the digital isolator. Eventually, the output of the digital isolator will be monitored by the controller. From Fig. 3.16, it is clear that as long as the delayed signal is still within the detection zone of the controller, the adaptive logic will be operated as normal. The duration of the detection zone is half of the switching cycle. If the switching frequency is 500 kHz, the duration of the detection zone is 1 μs, which is significantly longer than the total propagation delay in the path (typically below 100 ns). In the next control cycle, the controller will output a pulse width longer on-time duration for the SR. The duration of the large source-to-drain voltage drop for the SR will be reduced. Then the duration of the low-state output of the comparator will be reduced as well. Eventually, the controller will detect the low-state and increase the on-time duration again in the following control cycle. The two control cycles shown in Fig. 3.16 are just two states during the adaptive SR on-time tuning process. The complete adaptive SR on-time tuning approach can be referred to Fig. 3.14.

It should be mentioned that the turn-off propagation delay introduced by the gate driver can be automatically compensated by the adaptive on-time tuning algorithm. If the SR is turned off later than the current zero-crossing moment, then no low-state will be detected by the controller. In the next control cycle, the con-

troller will reduce the SR on-time duration, which is equivalent to advance the SR turn-off timing. Therefore, any turn-off delay introduced by the gate driver can be compensated automatically. Meanwhile, as discussed before, the turn-on timing of the SR is synchronized with the corresponding primary side switch. Since the same gate drivers and same switches are employed for both primary side and secondary side, the turn-on propagation delay introduced by the gate driver will be almost the same for both sides. The turn-on delay brought by the gate driver will not affect the normal operation as well.

3.4.8 Insulation Consideration of the Proposed SR Driving Scheme

Based on Fig. 3.13, it is clear that there are two insulation barriers for the proposed SR driving circuit. The first barrier is between the signal ground and the main switch source and the second barrier is between the main switch source and the main switch drain. The clearance and creepage distances are determined by the the maximum operating voltage and the pollution degree. Meanwhile, the maximum insulation voltage level is restricted by the insulation voltage rating of the isolation components.

For the first insulation barrier, the digital isolator, the isolated gate driver and the isolated dc-dc power supply (not shown in Fig. 3.13) are placed across this barrier. The maximum working insulation voltage for those components should be higher than the maximum operating voltage. For the second insulation barrier, the high-voltage MOSFET ($S1$) and the main switch are placed across this barrier. The voltage rating of the two switches should be higher than the maximum operating voltage. In this study, the maximum operating voltage (maximum battery voltage) is 450 V, so a 600 V rating high-voltage MOSFET is sufficient to block the dc-link voltage.

It should be mentioned that, for the proposed SR driving scheme, the drain-to-

source voltage sensing and comparing are implemented on the secondary side of the isolated gate driver, which has the same ground as the main switch source. There is no high dv/dt on the secondary side of the isolated gate driver, so the drain-to-source voltage sensing and comparing is very robust. There will be some common-mode (CM) current flowing into the signal ground through the isolation capacitances of these isolated components (gate driver, signal isolator and the isolated dc-dc). The common-mode current can be suppressed by the employment of the CM chokes, the selection of high dv/dt immunity components and the appropriate PCB layouts.

3.4.9 Extension to SiC and Si Devices

Table 3.2: Parameters of Different Types of 600/650 V Power Semiconductors.

Semiconductor	GaN	SiC	Si
Part number	Infineon IGOT60R070D1	CREE C3M0060065K	Infineon IPB60R060C7
Typical R_{dson}	55 mΩ	60 mΩ	60 mΩ
Time-related C_{oss}	102.5 pF	132 pF	1050 pF
Typical threshold voltage	1.2 V	2.3 V	3.5 V
Typical gate drive voltage	+5 V/-5 V	+15 V/-4 V	+10 V/0 V
V_{sd} at the gate-off period (10 A drain current)	7.35 V	5.7 V	0.82 V

The same sensing circuit and the adaptive SR on-time tuning algorithm can be applied to SiC MOSFETS, as well as the Si MOSFETs. Three off-the-shelf 600/650 V power switches of different semiconductor materials with similar R_{dson} have been

selected. The critical parameters of the three switches are shown in Table 3.2. The differences among the semiconductors and the effects on the performance of the sensing circuits are discussed as follows.

First, the self-driven mechanism of the auxiliary switches is able to work for all the three types of the semiconductor switches. However, the following differences should be mentioned for the SiC and Si scenarios. The turn-on and turn-off delays should be adjusted for the SiC and Si scenarios. According to Table 3.2, the SiC and Si switches have higher threshold voltage than GaN switches. To guarantee the main switch is turned on prior to the auxiliary switches, the time constant of R_3 and C_2 [shown in Fig. 3.3(b)] should be increased a little bit to slightly delay the turn-on timing of the auxiliary switches. Meanwhile, the main switch should be turned off later than the auxiliary switches. Additional turn-off resistance can be added on the turn-off gate loop for the main switch. In this way, the high voltage will be safely blocked by the high-voltage MOSFET (S_1) in any conditions. Meanwhile, negative turn-off voltage should be employed for Si scenario. For the proposed sensing circuit, the negative turn-off voltage is a must, because the P-type MOSFETs need negative gate-to-source voltage to be turned on. For Si device, the threshold voltage is relatively high, so zero turn-off voltage can be utilized. The negative turn-off voltage is also widely used for Si device to prevent the mis-triggering. As long as the negative turn-off voltage is below the threshold voltage of the P-type MOSFETs (typically -2 V), the self-driven mechanism will not be affected.

Second, the sensing and blocking function of the proposed sensing circuit will work for the SiC and Si scenarios. As mentioned earlier, the biggest challenge for the sensing circuit is to bypass the displacement current during the high dv/dt transients. According to Table 3.2, the time-related junction capacitance of the GaN switches is smaller than the other two semiconductor switches. Therefore, for a certain magne-

tizing current, the dv/dt for the GaN-based converter will be 30% higher than the SiC-based converter and 924% higher than the Si-based converter, which are estimated based on the charging and discharging time for the junction capacitance. Sufficient experimental results have demonstrated that the sensing and blocking function works very well for the GaN scenarios, which will be presented in the experimental section. Therefore, the sensing and blocking function will work for SiC and Si scenarios where lower dv/dt occurs.

Last but not least, the post-processing of the sensed drain-to-source voltage will work for SiC and Si scenarios. The key for adaptively reaching the current zero-crossing moment is to differentiate the body diode conduction ('diode-like' conduction for GaN) and the R_{dson} conduction. In other words, the source-to-drain voltage drop (V_{sd}) at the gate-off period should be significantly larger than the source-to-drain voltage drop at the gate-on period. In this way, the threshold voltage can be set far away from zero, which brings good noise immunity. Based on Table 3.2, at 10 A drain current, the source-to-drain voltage drop for GaN is 7.35 V at the gate-off period (-5 V turn-off voltage). If the device gate is turned on, the voltage drop is only 0.55 V. The large clearance makes it really easy to separate the gate-on and gate-off scenarios based on the sensed drain-to-source voltage. Similarly, for SiC device, at 10 A drain current, the source-to-drain voltage drop is 5.7 V at gate-off period (-4 V turn-off voltage). If the device gate is turned on, the voltage drop is only 0.6 V. The clearance is still very large. For Si device, the body diode voltage is relatively low (0.82 V), which is similar to the voltage drop of the R_{dson}. To differentiate the source-to-drain voltage drop between the gate-off and gate-on states, smaller R_{dson} switches should be selected, because the body diode voltage drop will not be decreased significantly for higher current rating switches. In [52], the Si-based SR is employed and the same post-processing approach is successfully verified. Since the R_{dson} of the

selected Si device is extremely low, there is still a relatively large clearance between the gate-on and gate-off source-to-drain voltage drops.

To sum, the application of proposed SR driving scheme can be extended to SiC and Si devices.

3.5 Experimental Verification

3.5.1 High-power-density 3.3 kW/500 kHz CLLC Resonant Converter Prototype

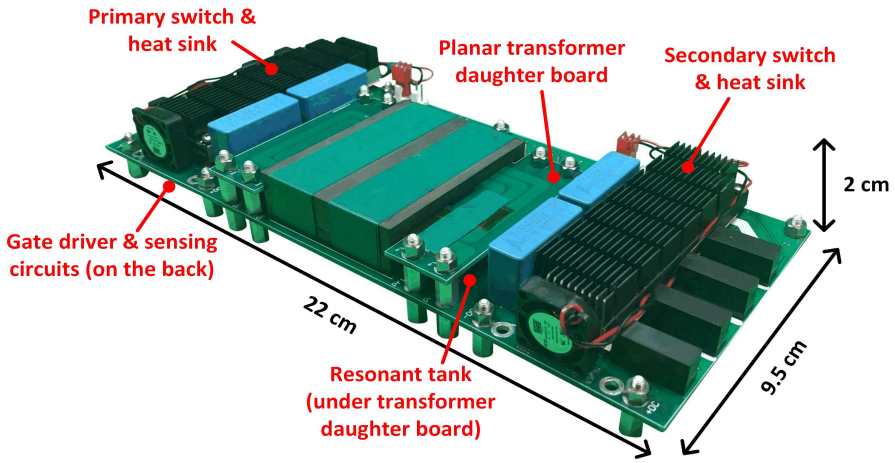


Figure 3.17: The 3.3 kW/500 kHz High-power-density CLLC Resonant Converter Prototype.

To validate the operation of the proposed SR driving scheme. A 3.3 kW/500 kHz GaN-based CLLC resonant converter prototype is built, as shown in Fig. 3.17. The prototype uses the same circuit topology as shown in Fig. 3.1. The output voltage range (battery voltage range) for the CLLC converter is 250∼450 V. When the battery voltage is below 300 V, the converter operates in the constant current mode (11 A output current); when the output voltage is above 300 V, the converter operates in the constant power mode (3.3 kW). The prototype can be regarded as a 3.3 kW dc

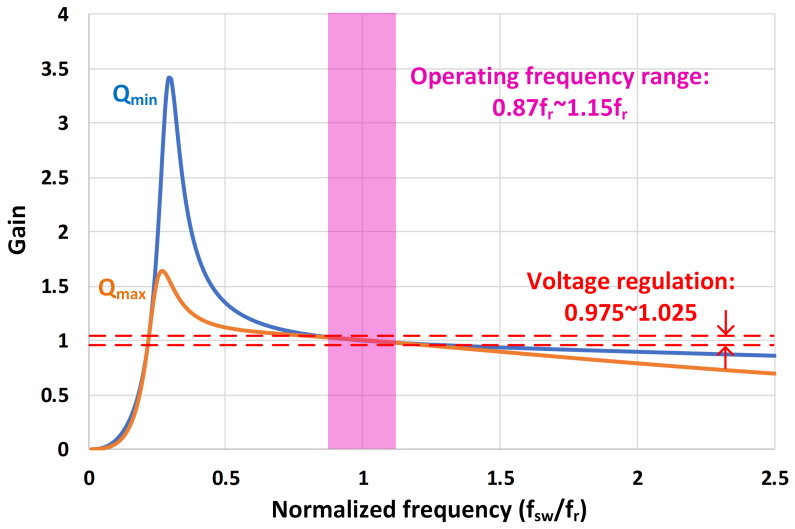


Figure 3.18: Gain Curves for the Heaviest Load and Lightest Load Conditions of the Designed CLLC Resonant Converter.

Table 3.3: Key Parameters for the 3.3 kW/500 kHz CLLC Prototype.

Parameters	Values
Power rating	3.3 kW
Resonant frequency	500 kHz
Output voltage range	250∼450 Vdc
Primary side device	Infineon IGOT60R070D1
Secondary side device (SR)	Infineon IGOT60R070D1
Resonant inductance value	$L_{\mathrm{r}} = 1.535\ \mu$H
Resonant capacitance value	$C_{\mathrm{r}} = 66$ nF
Magnetizing inductance value	$L_{\mathrm{m}} = 15.5\ \mu$H
Voltage gain range	0.975∼1.025
Switching frequency range	435∼575 kHz

transformer module. A 6.6 kW CLLC resonant converter can be constructed by the series-in-parallel-out connection of the two modules and then can be utilized as the isolated dc-dc stage for a level-2 EV OBC. The modular structure can be easily scaled up to higher power rating OBC as well (10 kW and above). The planar transformer is employed to boost the converter power density. Meanwhile, the low-profile inductors and small-packaged ceramic capacitors are utilized. These resonant elements are placed under the transformer daughter board, which can save the overall footprint. The gate driver circuits, the proposed drain-to-source voltage sensing circuit and the post-processing circuit are placed on the back of the mother board. The height of these integrated circuit components is extremely small. The low-profile design makes the total height of the prototype is only 2 cm. The power density of this prototype

Table 3.4: Parameters for the Proposed SR Drain-to-source Voltage Sensing Circuit.

Parameters	Values
R_1	250 Ω
C_1	20 pF
R_2	50 kΩ
R_3	67 Ω
C_2	100 pF
R_4	10 Ω
S_1	Diodes DMN60H080DS
Q_1 and Q_2	Onsemi FDN352AP
U_1	Linear Technology LT1711IMS8
V_{th}	-2.5 V
Digital controller	Texas Instrument TMS320F28335

reaches 130 W/inch^3. The key parameters of the CLLC converter prototype are listed in Table 3.3. Here, it is assumed that the double-line frequency voltage ripple (peak-to-peak) from the PFC dc-link is 5% of the dc-link voltage. Therefore, the CLLC resonant converter needs to have the 0.975∼1.025 voltage regulation capability to compensate the double-line frequency voltage ripple to prevent the harmonic current flowing into the battery. By carefully designing the resonant tank parameters, the operating frequency of the CLLC resonant converter is from 435 kHz to 575 kHz. This is a narrow operating frequency range, which guarantees the high efficiency of the CLLC resonant converter. The gain curves for the heaviest load and lightest load conditions are shown in Fig. 3.18. The design and optimization of the resonant elements can be referred to [25]. Moreover, the parameters for the proposed SR drain-to-source sensing circuit and the post-processing circuit are listed in Table 3.4. The digital controller is not integrated in this prototype.

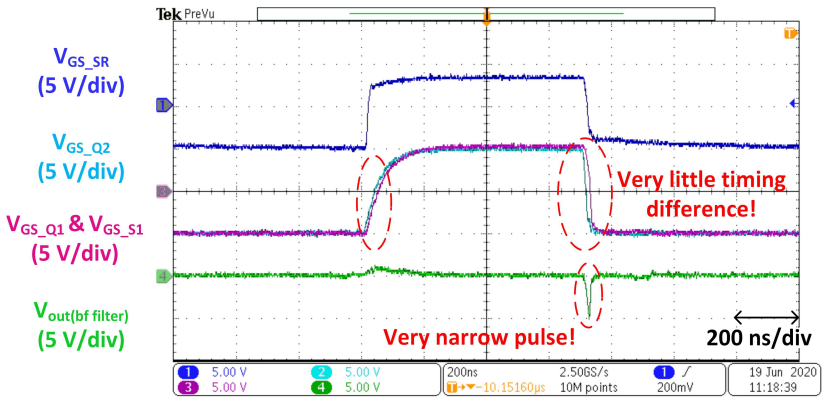


Figure 3.19: Experimental Waveforms of the Gate-to-source Voltages and the Output Voltage of the Sensing Circuit (Before the Filter).

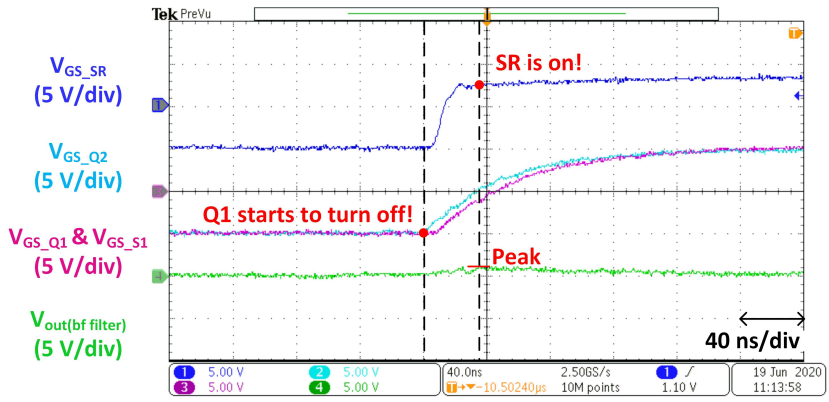


Figure 3.20: Turn-on Transient Waveforms of the Gate-to-source Voltages and the Output Voltage of the Sensing Circuit (Before the Filter).

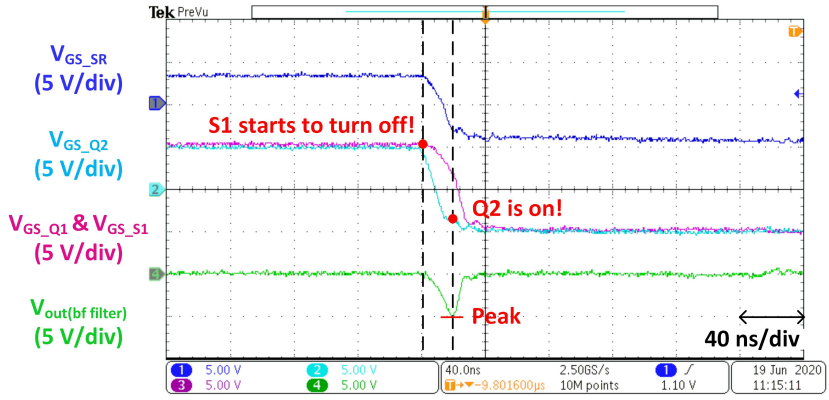


Figure 3.21: Turn-off Transient Waveforms of the Gate-to-source Voltages and the Output Voltage of the Sensing Circuit (Before the Filter).

3.5.2 Validation of the Self-driven Mechanism for the Proposed Sensing Circuit

The self-driven mechanism of the proposed SR drain-to-source voltage sensing circuit can be validated according to the experimental waveforms in Fig. 3.19 to Fig. 3.21. Based on the waveforms in Fig. 3.19, the SR and all the auxiliary switches are properly turned on and turned off by using the original gate-to-source voltage of the SR alone. There is a little timing difference between the gate-to-source voltages of Q_1 and Q_2, which is due to the transient capacitive voltage divider effect as discussed

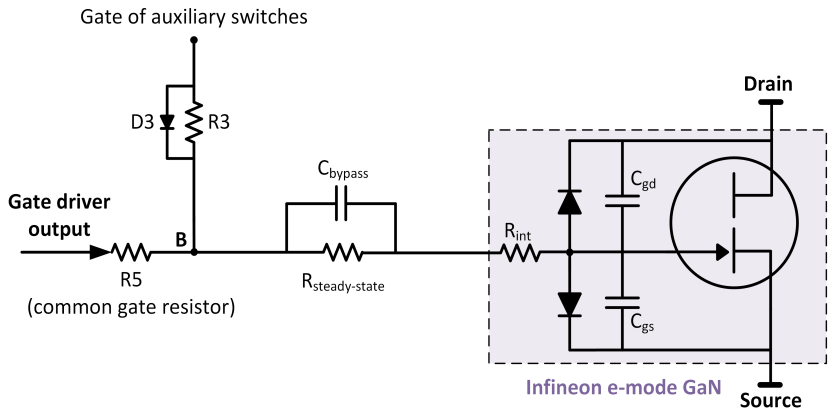


Figure 3.22: Circuit Diagram for the Gate Driving of Infineon E-mode GaN.

previously. The difference results in the a narrow negative pulse in the output voltage waveform. Since the duration of this pulse is very short (around 20 ns), it can be easily removed by a small output filter. It should also be mentioned that the gate drive voltage from the gate driver output is +5 V/-5 V. The selected Infineon GaN device is actually a current-driven device (gate injection transistor). The gate current during the turn-on transient determines its turn-on speed and the gate current during the steady-state on-time determines its R_{dson}. It has an intrinsic diode between its gate and source. During the steady-state on-time, the intrinsic diode will clamp its gate-to-source voltage at around +3.5 V if the 20 mA gate current is constantly drawn from the gate driver power supply. The gate driving circuit in Fig. 3.22 is utilized to properly turn on the Infineon GaN device. During the turn-on transient, a bypassing capacitor (C_{bypass}) will short the large gate resistor ($R_{\text{steady-state}}$) to provide sufficient transient current to turn on the GaN device. During the steady-state on-time, the large gate resistor ($R_{\text{steady-state}}$) will be kicked in to limit the steady-state current at around 20 mA. Meanwhile, the voltage difference between the gate driver output and the intrinsic diode voltage drop will be sustained by $R_{\text{steady-state}}$, hence, the voltage of point B referred to the source is still around +5 V, which guarantees the low R_{dson}

of the auxiliary switch S_1.

For the turn-on transient as shown in Fig. 3.20, the output voltage of the sensing circuit starts to rise when Q_1 starts to turn off and reaches the peak after the SR is on. For the theoretical analysis in Fig. 3.5, the output voltage of the sensing circuit should start to rise when the gate-to-source voltage of Q_1 leaves its threshold voltage. It should arrive at the peak when the gate-to-source voltage of the SR reaches its threshold voltage. The difference is due to the change of the device channel resistance for the real case. As mentioned earlier, for the real case, the device channel resistance begins to increase once the V_{gs} drops. Meanwhile, the device channel resistance can still be high when the V_{gs} does not reach its steady-state turn-on value. For the theoretical analysis, once the V_{gs} is beyond the threshold voltage, the device is considered to be a constant small resistor. Despite of the difference, it can be concluded that the experimental results basically coincide with the theoretical analysis.

For the turn-off transient as shown in Fig. 3.21, the output voltage of the sensing circuit starts to drop when S_1 starts to turn off and reaches the negative peak when the Q_2 is on. For the theoretical analysis in Fig. 3.5, the output voltage of the sensing circuit should start to fall when the gate-to-source voltage of S_1 leaves its threshold voltage. It should arrive at the peak when the gate-to-source voltage of Q_2 reaches its threshold voltage. The difference is due to the same reason as discussed for the turn-on transient. It can be concluded that the experimental results basically coincide with the theoretical analysis as well.

3.5.3 Validation of the Adaptive SR On-time Tuning Function

The adaptive SR on-time tuning function can be verified by the experimental waveforms in Fig. 3.23 and Fig. 3.24. Without the implementation of the adaptive

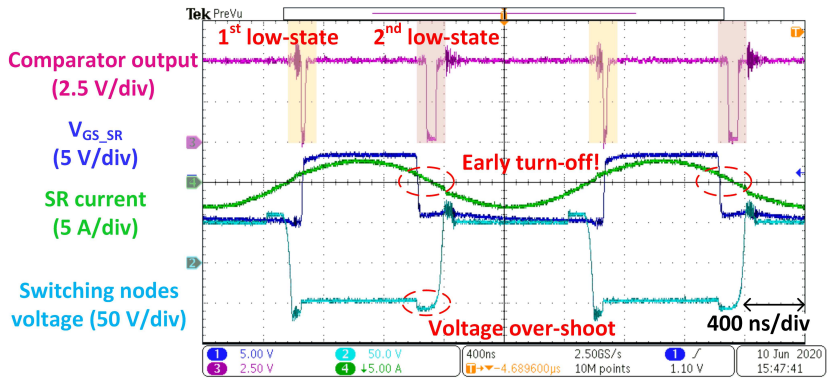


Figure 3.23: Experimental Waveforms Without Implementation of the Adaptive SR On-time Tuning.

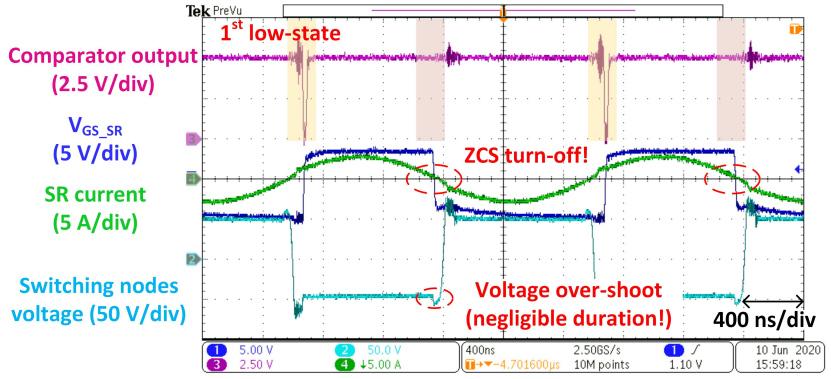


Figure 3.24: Experimental Waveforms with Implementation of the Adaptive SR On-time Tuning.

SR on-time tuning, as shown in Fig. 3.23, the comparator outputs two low states in one switching cycle. The first low-state represents the delayed turn-on of the SR, which is due to the over-designed dead-time for this operating condition. The second low-state reflects the early turn-off of the SR. The voltage over-shoot in the switching node voltage waveforms is exactly due to the large source-to-drain voltage drop during the gate-off period. The over-shoot in the switching node voltage is another indicator for the SR delayed turn-on or early turn-off. After implementing the adaptive on-time tuning algorithm in the controller, the second low-state is gone, which means the SR almost achieves the ZCS turn-off, as shown in Fig. 3.24. Meanwhile, the duration of

the over-shoot in the switching node voltage is reduced to negligible duration.

It should be mentioned that the first low-state does not necessarily occur in Fig. 3.24. As discussed earlier, the first low-state is due to the delayed turn-on of the SR. Since the turn-on timing of the SR is synchronized with the corresponding primary side switch (open-loop), it does not matter whether the first low-state occurs or not. The adaptive SR on-time tuning algorithm only deals with the turn-off timing of the SR. In each switching cycle, the detection of the low-state starts from 1/4 of the period, so the output state of the comparator during the turn-on transient will be skipped by the controller.

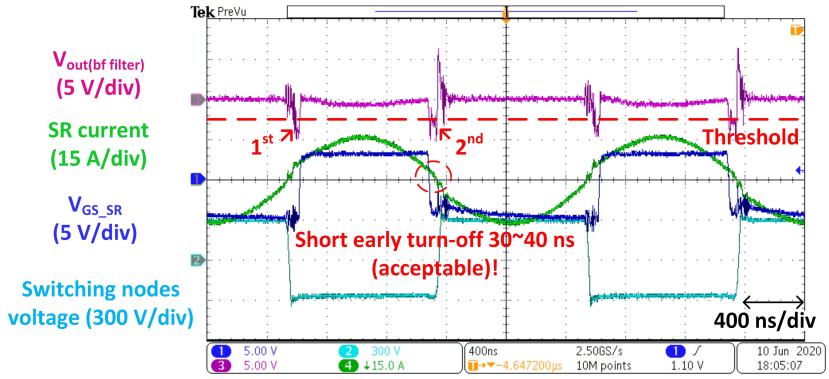


Figure 3.25: Sensing Circuit Output Before the Filter for 500 kHz Switching Frequency and 300 V Battery Voltage Scenario.

3.5.4 Validation of the Sensing and Blocking Performance for the Proposed Sensing Circuit

To verify the voltage sensing and blocking performance of the proposed voltage sensing circuit, the 3.3 kW full-load tests are conducted. The full-load testing waveforms for the 500 kHz switching frequency, 300 V battery voltage case are shown in Fig. 3.25 to Fig. 3.27.

The pink waveform in Fig. 3.25 is the sensing circuit output before the filter. Ac-

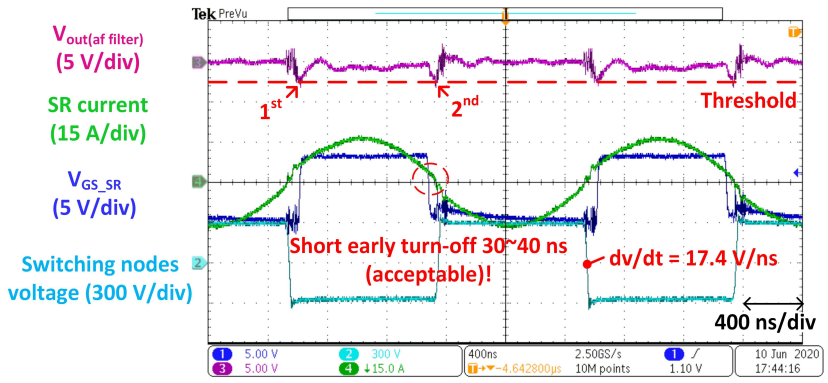


Figure 3.26: Sensing Circuit Output After the Filter (Comparator Input) for 500 kHz Switching Frequency and 300 V Battery Voltage Scenario.

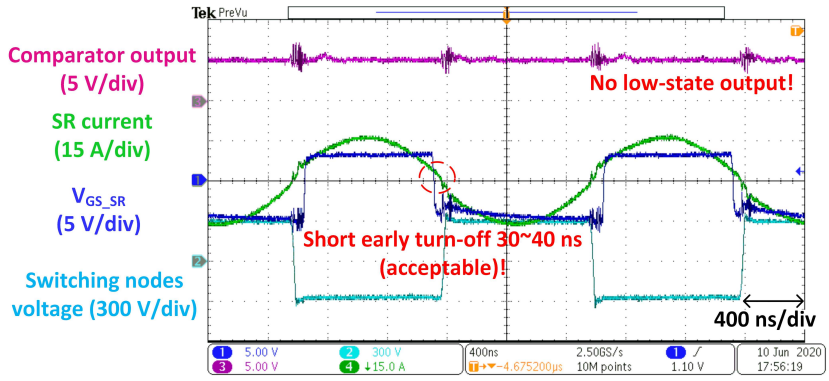


Figure 3.27: Comparator Output for 500 kHz Switching Frequency and 300 V Battery Voltage Scenario.

tually, it is the originally sensed SR drain-to-source voltage. For each switching cycle, the sensed SR drain-to-source voltage exceeds the threshold voltage (-2.5 V) twice. One is for the delayed turn-on and the other is for the early turn-off. However, the filter attenuates the originally sensed SR drain-to-source voltage. The pink waveform in Fig. 3.26 is the sensing circuit output after the filter. It is clear that the voltage magnitude is below the threshold for the whole switching cycle. The sensing circuit output after the filter is actually the input for the comparator. Since the comparator input does not exceed its threshold voltage during the entire switching cycle, the output of the comparator will not go low. As shown in Fig. 3.27, the pink waveform is

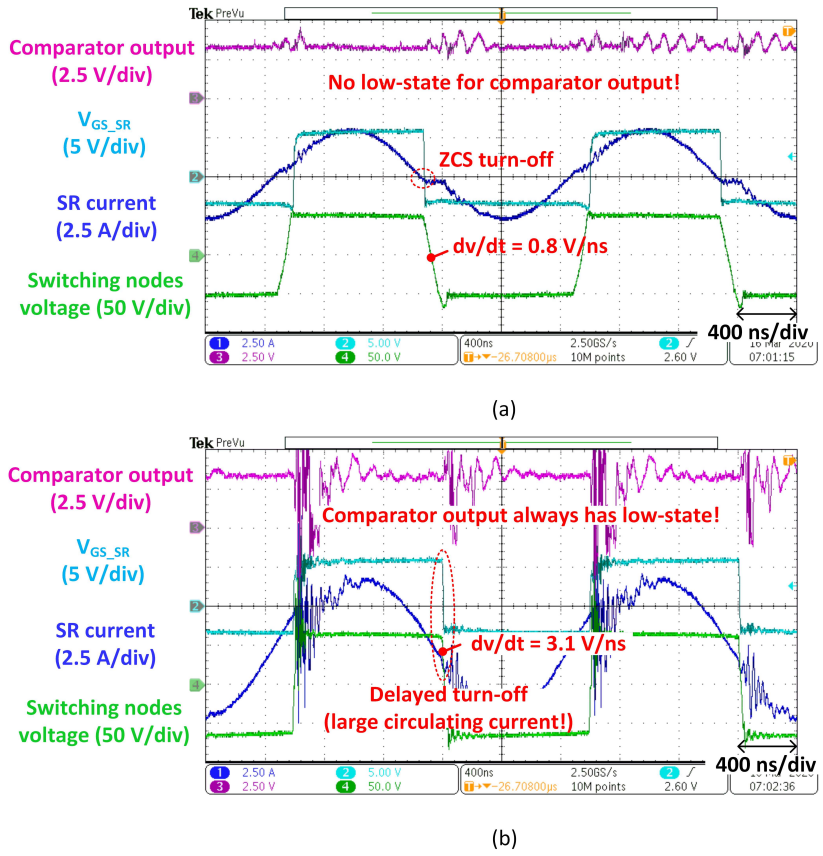


Figure 3.28: (a) Experimental Waveforms for the Conventional Sensing and Blocking Approach at 50 V Output Voltage. (b) Experimental Waveforms for the Conventional Sensing and Blocking Approach at 70 V Output Voltage.

the comparator output which exhibits no low-state during the entire switching cycle. Since no low-state is detected by the controller, the controller will decrease the SR on-time by a small interval in the next control cycle. Then the low-state will appear and the controller will increase the SR on-time by a small interval. Eventually, the SR on-time will be adjusted between the two states ('State C' and 'State D') as shown in Fig. 3.14. The captured waveform is actually 'State D' in Fig. 3.14, which exhibits no low-state in the detection zone.

From these experimental waveforms, several conclusions can be made.

First, the voltage sensing and blocking capability of the proposed SR drain-to-

source voltage sensing circuit is good. According the Fig. 3.26 and Fig. 3.27, the comparator input and output are very clean during both the sensing period (when SR is turned on) and blocking period (when SR is turned off) even at very high dv/dt (17.4 V/ns). The dv/dt labeled here is the dv/dt between the two switching nodes of the H-bridge, and the dv/dt at the device drain-to-source is half of this value. To make a comparison, the conventional method for the low-voltage, low dv/dt sensing and blocking approach is implemented in another prototype. The conventional method employs only a blocking diode and a pull-up resistor and no parallel bypassing branch is utilized, as shown in Fig. 1.10. The experimental results are shown in Fig. 3.28. To prevent the over-current due to wrong gate driving of the SR, the load is set to be very light in Fig. 3.28. At 50 V output voltage, the dv/dt between the switching nodes is 0.8 V/ns. The comparator output is normal and the adaptive on-time tuning function works. However, at 70 V output voltage, the comparator output has huge oscillation and over-voltage, which comes from the comparator input side, because the comparator has no isolation between the input side and output side. The oscillation and over-voltage issues are induced by the increased dv/dt (3.1 V/ns). The controller will falsely detect the low-state all the time and increase the on-time up to the preset limit value. In Fig. 3.28(b), huge circulating current is observed, because the SR is still on after the current crosses zero. Therefore, for the conventional approach, the comparator input and output suffer from over-voltage and oscillation problems even at very low output voltage and very low dv/dt. The proposed SR drain-to-source voltage sensing circuit addresses the over-voltage and oscillation issues introduced by the high voltage and high dv/dt pretty well.

Second, the SR exhibits a 30∼40-ns early turn-off by using the proposed SR driving scheme. In Fig. 3.25, it is clear that the output of the sensing circuit has a 30∼40-ns narrow pulse during the turn-off transient and the magnitude of the narrow

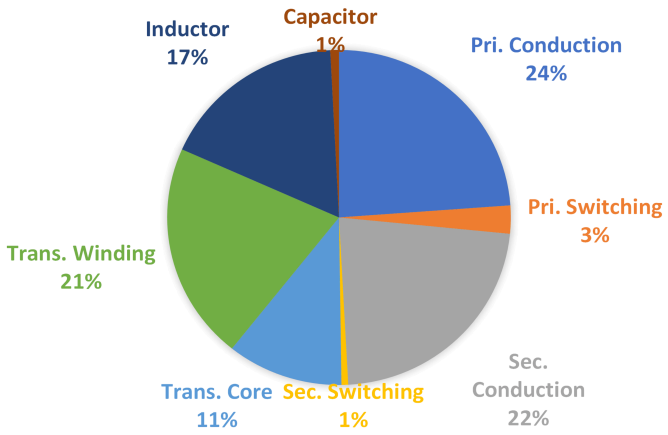


Figure 3.29: Power Loss Breakdown of the CLLC Resonant Converter in the 500 kHz, 300 V Battery Voltage Condition.

pulse exceeds the threshold. However, this narrow pulse is attenuated by the output filter. In Fig. 3.26, the magnitude of the filtered narrow pulse is below the threshold. The output of the comparator will not have a low-state during the turn-off transient, so the SR on-time will not be extended in the next control cycle. The filter size can be reduced to make the SR turn-off point closer to the current zero-crossing moment. The minimum time constant of the filter can be reduced to 10 ns, which is enough to attenuate the magnitude of the unwanted negative narrow pulse (shown in Fig. 3.21) below the level of threshold. However, the 30∼40 ns early turn-off is acceptable for this study. The system power loss breakdown is conducted for the 500 kHz, 300 V battery voltage case based on the theoretical calculations and SPICE simulations, as shown in Fig. 3.29. There can be some difference between the calculations and the actual power loss produced in each component. To reduce the calculation errors, the power loss breakdown is conducted for multiple operating points and reasonable compensations are made based on the measured efficiency (total power loss) of the CLLC converter prototype. According to the power loss breakdown, the conduction loss of the SR occupies 22.6% of the total loss for the CLLC converter under the

condition of 30∼40-ns early turn-off. If the SR achieves ideal ZCS turn-off, the system efficiency can only be improved by 0.27%. Since the improvement is quite insignificant, the 30∼40-ns early turn-off is acceptable for this design.

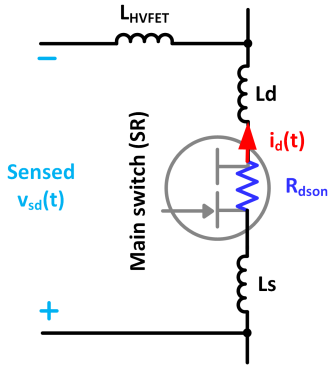


Figure 3.30: Parasitic Inductances in the Loop for the Conventional Approach.

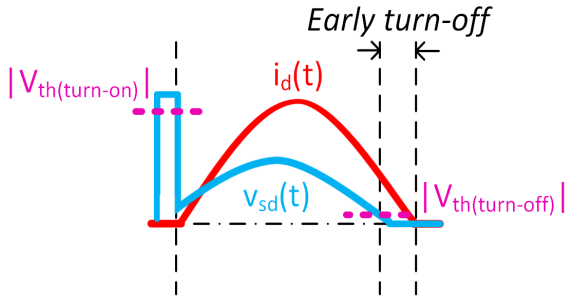


Figure 3.31: SR Early Turn-off Event in the Conventional Approach.

For the conventional SR driving scheme which is employed in the commercial SR drivers, the parasitic inductances in the device package as well as in the sensing loop will result in the early turn-off of the SR. As shown in Fig. 3.30, L_{d} is the drain side parasitic inductance of the SR; L_{s} is the source side parasitic inductance of the SR and L_{HVFET} is the parasitic inductance in the package of the high-voltage blocking FET. These inductances and the R_{dson} of the main switch form a inductive branch, so the sensed source-to-drain voltage ($v_{\mathrm{sd}}(t)$) will lead the device drain current ($i_{\mathrm{d}}(t)$) by a phase angle. For the conventional approach, the turn-off timing of the SR

totally depends on when the sensed source-to-drain voltage drops below the turn-off threshold ($V_{\text{th(turn-off)}}$), as shown in Fig. 3.31. Therefore, the turn-off timing of the SR will be prior to the zero current-crossing moment. Additional conduction loss will be produced. For the adaptive on-time tuning approach, though the parasitic inductances exist as well, the SR turn-off timing is not based on when the sensed v_{sd} drops below $V_{\text{th(turn-off)}}$. Instead, the turn-off timing is adaptively tuned according to whether the large voltage drop in the reverse channel occurs, as shown in Fig. 3.14. Therefore, the adaptive on-time tuning approach is able to avoid the early turn-off event caused by the parasitic inductances.

To make a quantitative analysis, the device package parasitic inductances are obtained from the SPICE models. In this study, $L_{\text{d}} = 1.5$ nH, $L_{\text{s}} = 1.3$ nH and $L_{\text{HVFET}} = 1$ nH. The total stray inductance in the sensing loop is 3.8 nH, if the PCB trace stray inductance is ignored. The typical R_{dson} of the selected SR is 55 mΩ. Therefore, the voltage-to-current phase angle caused by the parasitic inductances can be estimated by,

$$\theta = \arctan\left(\frac{2\pi \cdot f \cdot L_{\text{stray}}}{R_{\text{dson}}}\right) \tag{3.12}$$

where f is the resonant frequency and L_{stray} is the total stray inductance in the sensing loop.

At 500 kHz resonant frequency, the phase lead is 12.3$^{\text{o}}$, so the duration of the early turn-off can be calculated as,

$$\Delta T_{\text{early-turn-off}} = \frac{12.3^{\text{o}}}{180^{\text{o}}} \cdot \frac{T}{2} \tag{3.13}$$

where T is the period of the current.

Therefore, the early turn-off caused by the parasitic inductances in the device package is around 70 ns. The 70-ns early turn-off will make the CLLC converter system efficiency drop by 1.5%, which is significant. The proposed driving scheme will only make the system efficiency drop by 0.27% compared to the ideal ZCS turn-off scenario.

To sum, compared to the conventional method, the proposed SR driving scheme will save 10.15 W power loss for each SR and improve the system efficiency by 1.23%. Meanwhile, the over-voltage and oscillation issues caused by the high dv/dt are solved very well by the proposed approach.

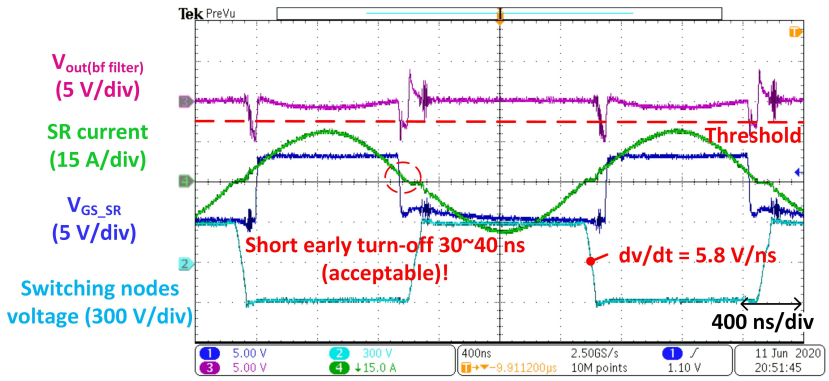


Figure 3.32: Experimental Waveforms for 435 kHz Switching Frequency, 300 V Battery Voltage Scenario.

Full-load experiments for other switching frequency and other battery voltage scenarios are conducted as well, as shown in Fig. 3.32 to Fig. 3.36.

In Fig. 3.32, the switching frequency is lower than the resonant frequency. The battery voltage is 300 V and the dc output current is around 11 A (heaviest load current condition). The pink waveform in this figure is the sensing circuit output before the filter, which is the originally sensed SR drain-to-source voltage. Similarly, the originally sensed SR drain-to-source voltage exceeds the threshold voltage (-2.5 V) twice in each switching cycle. Due to the attenuation from the filter, the voltage

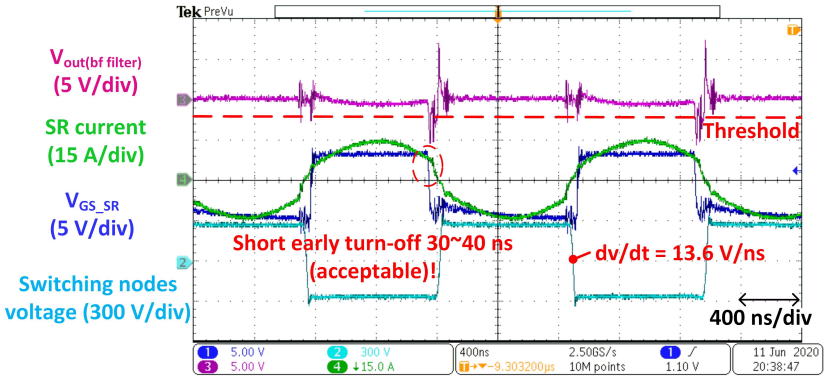


Figure 3.33: Experimental Waveforms for 575 kHz Switching Frequency, 300 V Battery Voltage Scenario.

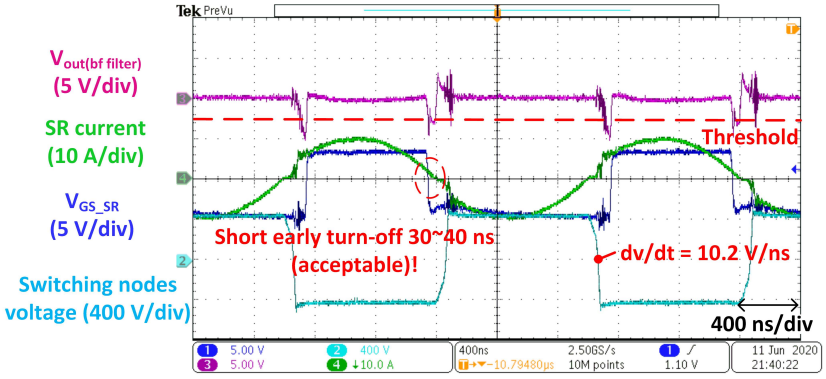


Figure 3.34: Experimental Waveforms for 500 kHz Switching Frequency, 450 V Battery Voltage Scenario.

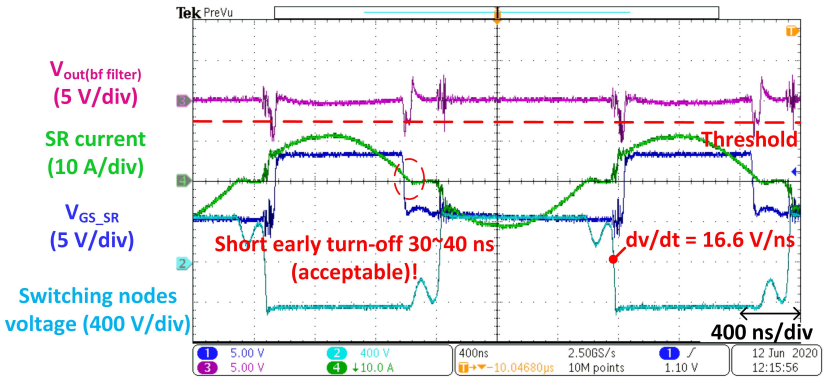


Figure 3.35: Experimental Waveforms for 435 kHz Switching Frequency, 450 V Battery Voltage Scenario.

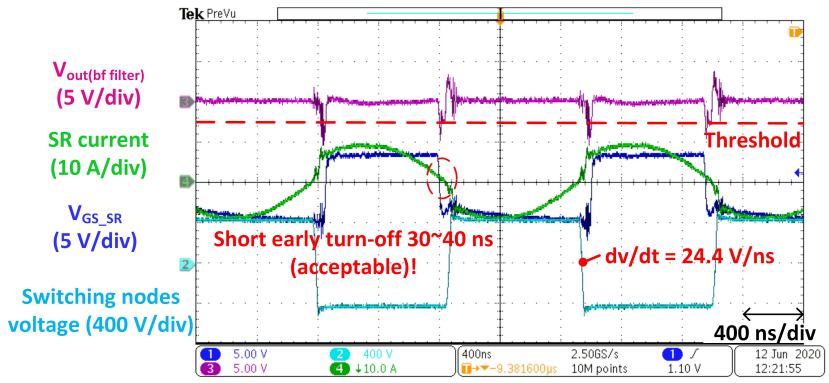


Figure 3.36: Experimental Waveforms for 575 kHz Switching Frequency, 450 V Battery Voltage Scenario.

enters the comparator input terminal does not exceed the threshold. The SR is turned off 30∼40-ns prior to the current zero-crossing moment, which is acceptable in terms of the system efficiency.

In Fig. 3.33, the switching frequency is higher than the resonant frequency. The battery voltage is 300 V and the dc output current is around 11 A (heaviest load current condition). The pink waveform in this figure is the sensing circuit output before the filter, which is the originally sensed SR drain-to-source voltage. For the turn-on transient, the sensed voltage is no longer beyond the threshold, which implies the SR is turned on right after the dv/dt transient finishes. For the turn-off transient, the duration of the early turn-off is short, though the amplitude of the current at the turn-off moment is relatively high. It is still acceptable in terms of the system efficiency.

The experimental waveforms for 450 V battery voltage scenarios (lightest load current conditions) are shown in Fig. 3.34 to Fig. 3.36. Similarly, the 30∼40-ns narrow pulse can be detected by the sensing circuit and the magnitude is beyond the threshold. The output filter attenuates the magnitude of the narrow pulse below the threshold, so the output of the comparator will not go low. The 30∼40-ns early

turn-off phenomenon is observed for all the cases. As discussed above, the system efficiency drop caused by the 30∼40-ns early turn-off is acceptable.

Finally, it is clear that the proposed SR drain-to-source sensing circuit works fine for all the output voltage scenarios and all the operating frequency scenarios even at 12.2 V/ns drain-to-source dv/dt transient (Fig. 3.36).

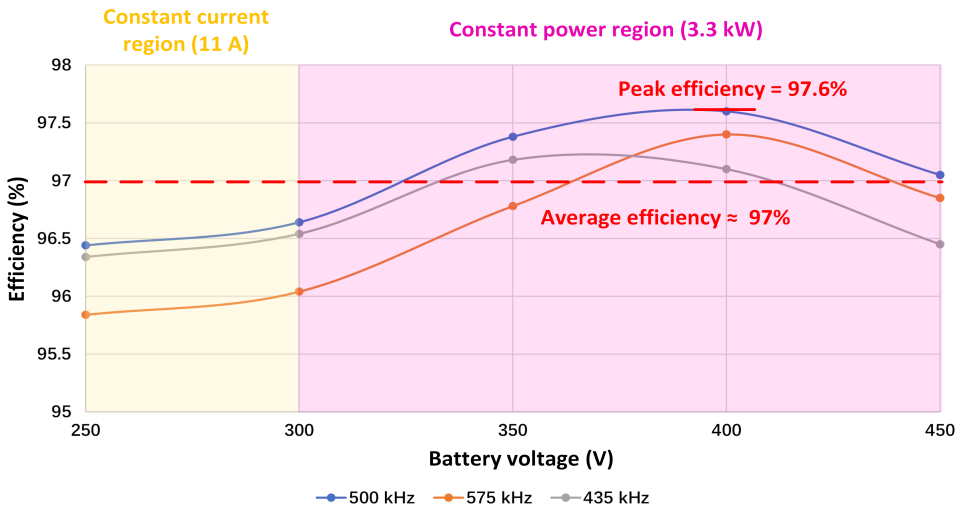


Figure 3.37: Efficiency Curves of the CLLC Resonant Converter for Different Operating Conditions.

3.5.5 Converter Efficiency Evaluation for Different Operating Conditions

The efficiency of the CLLC resonant converter is measured by Yokogawa WT500 Power Analyzer. The efficiency curves for different operating conditions are shown in Fig. 3.37. With the employment of the proposed SR driving scheme and the appropriate design of the power converter, the prototype achieves the peak efficiency of 97.6% and the average efficiency of around 97% for the whole operating frequency range. The peak efficiency of one state-of-the-art 3.3 kW GaN-based LLC converter is 97.4% [97]. However, since its switching frequency is only around 180 kHz, the

power density is not comparable to the presented prototype.

It should be mentioned that the control power (including the cooling fan) for the converter is supplied by a separate dc power supply. The total control power is 12 V $\times$ 0.56 A = 6.72 W, which can be obtained from the output voltage and output current of the dc power supply. The loss for this part is not included in the system efficiency evaluation. If the control power loss is considered, the system efficiency will be reduced by 0.2%, which is not significant.

Meanwhile, the proposed SR driving scheme brings little increase of the system cost and system complexity. The proposed method employs the low current rating Si-based auxiliary switches, which are very cheap compared with the GaN main switches. The comparator and the digital isolator are also low-cost. The low current rating Si devices have very tiny packages (SOT-363), hence the total footprint of the circuit will not be increased significantly. Moreover, the SR on-time tuning algorithm utilizes very simple logic. It does not need complicated calculations in the controller. In [52], the SR on-time tuning algorithm is implemented in very low-cost digital controllers. To sum, the proposed SR driving scheme addresses the issues of over-voltage and oscillation brought by the high dv/dt and achieves fine-controlled synchronous gate driving without increasing the system cost and complexity significantly.

3.6 Conclusion

This study presents a fined-controlled synchronous gate driving scheme for the GaN-based SR, which can be extended to Si-based and SiC-based SRs as well. To address the issues of over-voltage and oscillation caused by the high voltage and high dv/dt, a novel drain-to-source voltage sensing circuit is proposed. Three Si-based auxiliary switches are driven by using the original gate drive voltage for the SR alone, which makes the circuit operation simple, reliable and low-cost. Sufficient experiments

are conducted to prove the excellent performance of the proposed sensing circuit in various operating conditions. With the employment of post-processing circuits and the adaptive on-time tuning algorithm, the SR almost achieves ZCS turn-off for all scenarios. The proposed SR gate driving scheme is very suitable for the high-power-density and high-efficiency applications, because no additional current sensing device is required and the low-current rating auxiliary switches have very tiny packages. A 3.3 kW/500 kHz CLLC resonant converter prototype which employs the proposed drain-to-source voltage sensing and post-processing circuits is built and verified in the lab. The prototype exhibits an outstanding power density of 130 W/inch^3 and very high peak efficiency of 97.6%. In the future, the proposed synchronous gate driving scheme can be utilized for SiC-based SR in higher voltage level applications.

Chapter 4

ACTIVE CURRENT SOURCE GATE DRIVER FOR DYNAMIC VOLTAGE SHARING IN SERIES-CONNECTED GAN HEMTS

As mentioned in the introduction, the 600/650 V voltage rating of commercial GaN HEMTs is not sufficient for high battery voltage (800 V and above) EV applications. Stacking switches is a straightforward approach to enable GaN HEMTs to sustain higher dc-link voltages. However, the dynamic voltage imbalance issues must be addressed to avoid over-voltage breakdown for the low-voltage rating GaN devices. This chapter is organized as follows.

First, the root cause for the voltage imbalance in different switching scenarios is analyzed. Then the proposed voltage balancing schemes in different switching scenarios are presented. Next, the operating principles of the proposed active current source gate driver is introduced. Finally, the proposed current source gate driver and the voltage balancing schemes are verified in a series-connected GaN-based multiple pulse tester.

4.1 Review of the Root Cause for the Voltage Imbalance in Different Switching Scenarios

As mentioned in the introduction, the dynamic voltage imbalance can be caused by: 1) the discrepancies in the gate driving loops; 2) the device parameter tolerance; and 3) the device-to-ground displacement currents for the series-connected switches in the stack. For the discrepancies in the gate driving loops, it can be alleviated by using symmetrical connections and circuit layouts for different channels in the stack. For the device parameter tolerance, it can be overcome by adding small external gate-

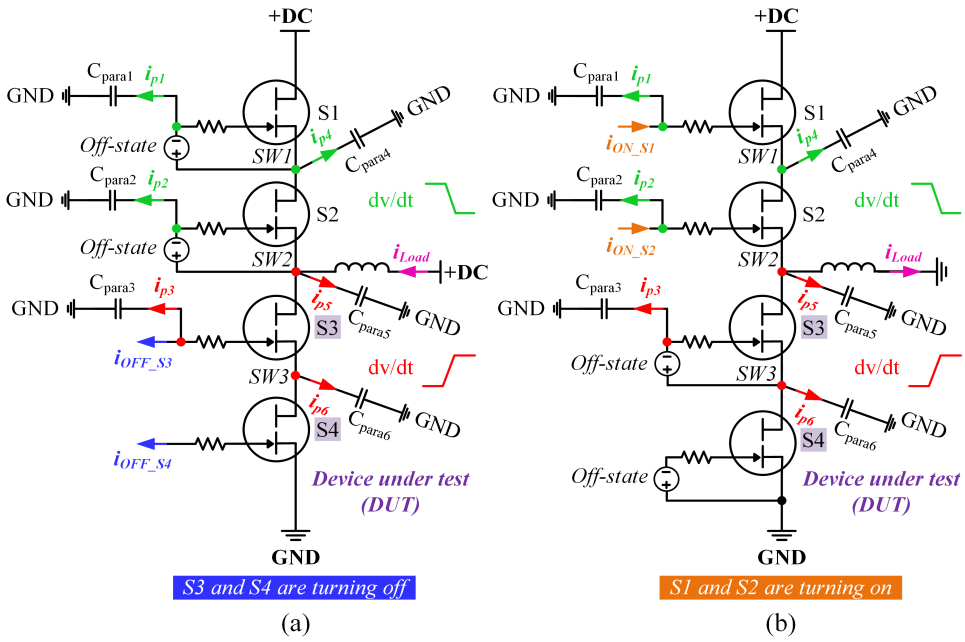


Figure 4.1: (a) Device-to-ground Displacement Currents During the Lower Arm Switches (DUT) 'Soft' Turn-off Transient. (b) Device-to-ground Displacement Currents During the Lower Arm Switches (DUT) 'Hard' Turn-off Transient.

to-source/drain-to-source capacitors. However, for the device-to-ground displacement currents, it is hard to be passively compensated because the device-to-ground parasitic capacitance is typically unknown. Therefore, the active compensation mechanism should be employed. Basically, the major focus of this study is to actively compensate for the voltage imbalance brought by the device-to-ground displacement currents. The effects of the device-to-ground displacement currents on the dynamic voltage sharing for the series-connected devices have already been discussed in the previous studies [65, 66, 100–106]. Here, a short review of those effects in different switching scenarios is conducted as follows.

4.1.1 'Soft' Turn-off Scenario

As is shown in Fig. 4.1(a), two GaN switches are connected in series for both upper arm and lower arm in a phase-leg. The load inductor is paralleled with the upper arm. The upper arm switches (S_1 and S_2) are in the gate-off state, and the lower arm switches (S_3 and S_4) are actively turning off. The lower arm switches are regarded as the device under test (DUT). Since the load current will assist the charging/discharging of the device junction capacitances during this transient, the lower arm switches are experiencing a 'soft' turn-off process. For the 'soft' turn-off scenario, the device drain-to-source dv/dt can be restricted by either the device gate current (i_{gate}) or the device drain current (i_{drain}) [100], as illustrated in the following equation:

$$\begin{aligned} i_{\text{gate}} &\geq C_{\text{gd}} \frac{dV_{\text{ds}}}{dt} \\ i_{\text{drain}} &\geq (C_{\text{gd}} + C_{\text{ds}}) \frac{dV_{\text{ds}}}{dt} \end{aligned} \tag{4.1}$$

where C_{gd} is the device gate-to-drain capacitance (Miller capacitance) and C_{ds} is the device drain-to-source capacitance. Both C_{gd} and C_{ds} are functions of V_{ds}.

For the devices with large input capacitance, such as Si devices and high-current SiC power modules, drain-to-source dv/dt is typically restricted by the gate current during the 'soft' turn-off transient. Most of the gate driver supplied current is utilized to charge the Miller capacitance during the rising dv/dt transient. However, for the devices with small input capacitance, such as discrete WBG devices (SiC and GaN) or even Si super-junction MOSFETs, the device drain-to-source dv/dt is typically determined by the drain/load current during the 'soft' turn-off transient. With the excessive gate driver supplied current, the device gate-to-source capacitance (C_{gs}) will be quickly discharged below its threshold. Therefore, the device channel can be already cut off before its drain-to-source voltage starts to rise. Then the device

becomes an equivalent junction capacitor, and the charging speed of the junction capacitor is determined by the drain/load current amplitude [100]. This fast turn-off property is beneficial for reducing the device turn-off energy because the overlapping between the device drain-to-source voltage and current is minimized. The extremely fast turn-off process of the discrete WBG devices is also called the nearly 'lossless' turn-off in [107].

However, due to the device-to-ground parasitic capacitances, the actual gate current and drain current of the series-connected switches are different even with well-matched gate drivers and device parameters. The device gate-to-ground parasitic capacitances are labeled as C_{para1}, C_{para2}, and C_{para3} in Fig. 4.1. Since there is almost no dv/dt between the gate of S_4 and the power ground, minimal displacement current will be produced. The parasitic capacitance between the gate and ground for S_4 is not shown in the figure. In the real system, the gate-to-ground parasitic capacitances consist of the isolation capacitance for the isolated DC/DC power supplies, the isolation capacitance for the isolated gate drivers, and the device gate to heat sink parasitic capacitance (if the heat sink is grounded). The device drain/source-to-ground parasitic capacitances are labeled as C_{para4}, C_{para5} and C_{para6} in Fig. 4.1. Similarly, since there is no dv/dt between the drain of S_1 and the power ground, no displacement current will be generated. The parasitic capacitance between the drain and ground for S_1 is not shown in the figure as well. In the real system, the major drain-to-ground parasitic capacitance comes from the PCB interlayer capacitance for the discrete devices. For the fast-switching GaN-based power converters, the flux-cancellation PCB layout techniques are usually employed to reduce the power loop parasitic inductance. To achieve the flux-cancellation between the switching nodes and the power ground, they are normally placed in two adjacent layers of a PCB and overlapped pretty well. Suppose the overlapping area between the switching node and

the power ground is only 10 mm×10 mm. In that case, the interlayer stray capacitance will be around 30 pF, which is already significant compared with the junction capacitance of the discrete GaN devices.

Based on Fig. 4.1(a), the gate currents of S_3 and S_4 can be written as:

$$\begin{aligned} i_{\text{gate(S3)}} &= i_{\text{OFF(S3)}} + i_{\text{p3}} \\ i_{\text{gate(S4)}} &= i_{\text{OFF(S4)}} \end{aligned} \tag{4.2}$$

where $i_{\text{OFF(S3)}}$ and $i_{\text{OFF(S4)}}$ are the gate driver supplied turn-off currents for S_3 and S_4, respectively; i_{p3} is the gate-to-ground displacement current for S_3.

Meanwhile, due to the existence of the drain/source-to-ground displacement currents, the relation between the drain currents of S_3 and S_4 can be expressed as:

$$i_{\text{drain(S3)}} = i_{\text{drain(S4)}} + i_{\text{p6}} \tag{4.3}$$

where i_{p6} is the drain-to-ground displacement current for S_4.

It is clear that S_3 has both higher gate current and higher drain current than S_4. As discussed earlier, the drain-to-source dv/dt is typically determined by the drain/load current for the discrete GaN devices. If no compensation mechanism is implemented, the top-sitting switch S_3 will have higher dv/dt than the bottom-sitting switch S_4 due to the bigger drain current, which can eventually cause the over-voltage breakdown.

4.1.2 'Hard' Turn-off Scenario

As is shown in Fig. 4.1(b), the upper arm switches (S_1 and S_2) are actively turning on, and the lower arm switches (S_3 and S_4) are in the gate-off state. The load inductor is paralleled with the lower arm for this scenario. Since the load current will not assist charging/discharging of the device junction capacitances during this transient, the upper arm switches are experiencing 'hard' turn-on. Meanwhile, the drain-to-source

voltage of the lower arm switches will be passively pulled up. Therefore, the lower arm switches can be regarded as experiencing 'hard' turn-off.

Since the lower arm switches are already in the gate-off state during this transient, the dv/dt will be determined by the drain current from the dc-link. Based on (4.3), the top-sitting switch S_3 has a higher drain current than the bottom-sitting switch S_4 due to the existence of the drain-to-ground displacement current. Therefore, the top-sitting switch S_3 will have higher dv/dt than the bottom-sitting switch S_4, which can eventually cause the over-voltage breakdown. As mentioned earlier, this phenomenon is also called the voltage imbalance of series-connected body-diodes in [101]. The voltage imbalance for this scenario is hard to compensate from the gate side with the conventional voltage source gate driver because the gates are already in the off state for the switches with rising drain-to-source voltages.

It should be mentioned that the device-to-ground displacement currents also affect the slew rate of falling dv/dt for the turn-on switches. As long as the turn-on timing is very synchronized for all the switches in the stack, the over-voltage breakdown is unlikely to occur during the turn-on transient. However, if there is several nanosecond turn-on timing difference among the series-connected switches, the over-voltage can still occur [85]. The drain-to-source voltage of the delayed turn-on switch will start to rise at first and then starts to fall when its gate-to-source voltage reaches the turn-on threshold. Therefore, it is still very critical to guarantee the consistency of the gate driving circuits for different channels in the stack [100].

4.2 Proposed Voltage Balancing Schemes in Different Switching Scenarios

To address the voltage imbalance issue, the current source gate driver strategy is adopted. The basic idea is to utilize additional compensation gate current to coun-

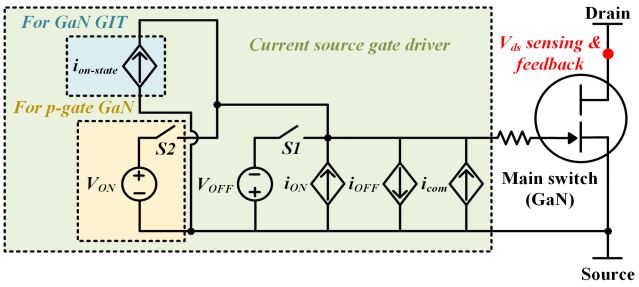


Figure 4.2: Simplified Schematic of the Proposed Current Source Gate Driver.

teract the effects from the device-to-ground displacement currents. The simplified schematic of the proposed current source gate driver is shown in Fig. 4.2. The critical operating principles are highlighted as follows.

1) The main switch turn-on and turn-off gate currents are provided by the controlled current sources i_{ON} and i_{OFF}, respectively. Additional compensation current is generated from another controlled current source i_{com}, and the compensation current direction is opposite to the turn-off gate current.

2) The negative voltage source (V_{OFF}) is still required to sustain the steady-state turn-off voltage. However, the voltage source is only for clamping the steady-state gate-to-source voltage rather than providing the transient turn-off gate current. The auxiliary switch S_1 determines when the active negative voltage clamping is kicked in the circuit.

3) For the voltage-driven type p-gate GaN devices, another positive voltage source (V_{ON}) is needed for clamping the steady-state turn-on gate-to-source voltage, which is controlled by the auxiliary switch S_2. For the current-driven type GaN gate injection transistors (GIT), another small current source ($i_{\text{on-state}}$) is required to provide the constant on-state gate current (around 20 mA).

4) Though the current direction of i_{ON}, i_{com} and $i_{\text{on-state}}$ is the same, separate controlled current sources are desired instead of using a single one. The turn-on

gate current is typically in the range of hundreds of mA or even higher, but the compensation gate current and the on-state gate current are in the range of tens of mA. If a single controlled current source is utilized, the current regulation range is huge, which is hard to meet the high-resolution and fast-transient requirement for the gate driver of GaN devices. This is the same reason for employing the additional small current source i_{com} to precisely tune the overall gate current rather than directly regulating the output current of i_{OFF}.

The following part presents the voltage balancing schemes with the proposed current source gate driver for both soft and hard-switching scenarios.

4.2.1 Voltage Balancing Scheme in 'Soft' Turn-off Scenario

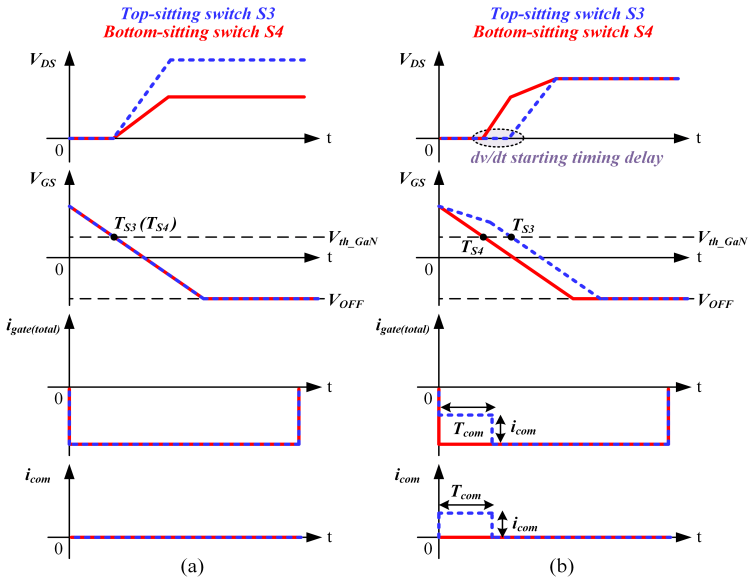


Figure 4.3: Voltage Balancing Scheme in 'Soft' Turn-off Scenario with Current Source Gate Driver. (a) Without Active Gate Current Control. (b) With Active Gate Current Control.

As mentioned earlier, for the discrete GaN devices, the dv/dt is typically determined by the drain/load current amplitude during the 'soft' turn-off transient. Due to the small input capacitance, the GaN device gate can be quickly discharged below

the threshold before its drain-to-source voltage starts to rise. Therefore, the rising dv/dt can not be directly regulated by tuning the supplied gate current amplitude. However, the starting timing of the rising dv/dt can be adjusted, which may compensate for the voltage imbalance brought by the slew rate difference. Actually, this voltage balancing strategy is the so-called active gate delay control in [66, 85]. The drawbacks of the active gate delay control with the voltage source gate driver have already been discussed earlier in the introduction part. The implementation of active gate delay control by employing the current source gate driver is shown in Fig. 4.3. The circuit diagram for the 'soft' turn-off scenario is referred to Fig. 4.1(a).

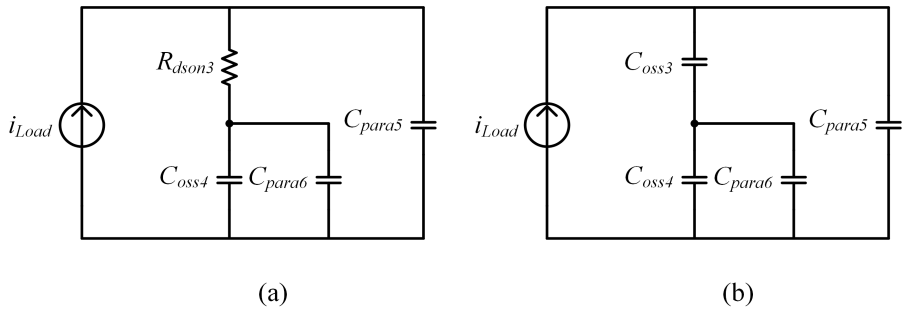


Figure 4.4: (a) Equivalent Circuit for the Lower Arm Switches When S_4 Is Off and S_3 Is On. (b) Equivalent Circuit for the Lower Arm Switches When Both Switches Are Off.

As is shown in Fig. 4.3(a), without the active gate current control, the top-sitting switch S_3 exhibits higher dv/dt compared with the bottom-sitting switch S_4, due to the higher drain current. By regulating the pulse width (T_{com}) or amplitude (i_{com}) of the compensation gate current, the dv/dt starting timing (T_{S3}) of the top-sitting switch $S3$ is delayed by certain duration. The equivalent circuits during the 'soft' turn-off transient are shown in Fig. 4.4. The parameters are consistent with the parameters defined in Fig. 4.1. When S_4 is turned off and S_3 is still on, S_3 is a small on-state resistor (R_{dson}), as shown in Fig. 4.4(a). Hence, the drain-to-source voltage of S_3 remains very low during this interval. Once S_3 is turned off, it is equivalent to a

junction capacitor (C_{oss}), as shown in Fig. 4.4(b). Then the drain-to-source voltage of S_3 will rise with a larger slew rate compared to S_4, due to the higher drain current. As a result, both switches can have equalized off-state drain-to-source voltages, though the dv/dt of the two switches are not same, as shown in Fig. 4.3(b).

The product of T_{com} and i_{com} is actually the compensation gate charge (Q_{com}). The two control variables T_{com} and i_{com} can be tuned to achieve the desired voltage sharing. The resolution of T_{com} is restricted by the controller minimum clock cycle. As mentioned earlier, the sub-nanosecond unit time step is required for the controller if the signal timing is the only control variable, which is the case for the voltage source gate driver [66, 85]. The compensation current amplitude can be set at a relatively small value for the proposed current source gate driver. High-resolution tuning can still be achieved even with a larger unit time step for the compensation pulse width. Hence, the voltage balancing control will be more reliable for the proposed approach. The detailed control algorithm of T_{com} and i_{com} will be introduced later.

4.2.2 Voltage Balancing Scheme in 'Hard' Turn-off Scenario

As discussed earlier, the voltage imbalance in the 'hard' turn-off scenario is caused by the drain-to-ground displacement currents. Since the switches with the rising drain-to-source voltage are already in the gate-off state during the dv/dt transient, the voltage imbalance can not be suppressed by adjusting the turn-off timing of the switches. One of the strategies is to trigger the gate of the switch that has higher dv/dt during the rising dv/dt transient to reduce the device impedance, so the average dv/dt during the switching transient is reduced. Then the well-balanced voltage sharing among the switches can be achieved [100]. The implementation of this strategy by employing the current source gate driver is shown in Fig. 4.5. The circuit diagram for the 'hard' turn-off scenario is referred to Fig. 4.1(b).

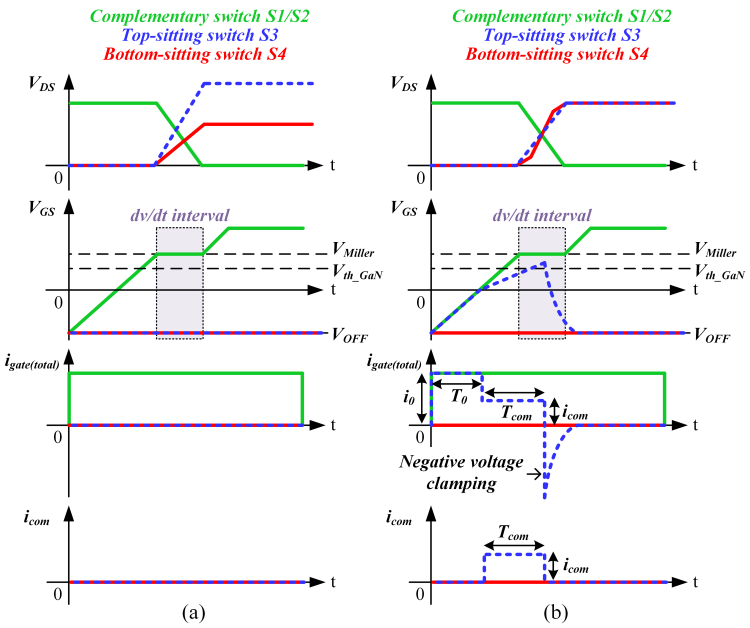


Figure 4.5: Voltage Balancing Scheme in 'Hard' Turn-off Scenario with Current Source Gate Driver. (a) Without Active Gate Current Control. (b) With Active Gate Current Control.

As is shown in Fig. 4.5(a), without the active gate current control, the top-sitting switch S_3 exhibits higher dv/dt compared with the bottom-sitting switch S_4, due to the higher drain current. In the hard-switching scenario, the dv/dt starts when the gate-to-source voltage of the complementary switches (S_1/S_2) reaches the turn-on Miller plateau. During this interval, both S_3 and S_4 are in the gate-off state without active gate current control. To suppress the voltage imbalance, the gate of S_3 is actively triggered, as shown in Fig. 4.5(b). The proposed active current control in the 'hard' turn-off scenario has the following three steps.

1) At the beginning, the large gate current i_0 is actively injected into the gate with the duration of T_0. This current can be considered as the 'pre-charge' current, and it can be generated by the turn-on current source (i_{ON} in Fig. 4.2). Hence, the gate-to-source voltage of S_3 rises simultaneously with the gate-to-source voltage of the complementary switches (S_1/S_2) during this interval. It should be mentioned that

the large 'pre-charge' current i_0 is used to reduce the rise time of the gate-to-source voltage for S_3. If the small compensation current is applied during the entire interval, the starting timing of the compensation current needs to be advanced a lot, which will extend the required dead-time between the turn-off and turn-on switches. The fixed duration T_0 can be selected as the time needed for the gate-to-source voltage of S_3 rising from the negative turn-off voltage to zero.

2) At T_0, the injection of i_0 is stopped, and the small compensation current i_{com} is added into the gate to continue elevating the gate-to-source voltage of S_3. The pulse width of the compensation gate current is T_{com}. The small amplitude of i_{com} achieves the 'fine-tuning' of the gate-to-source voltage of S_3.

3) At $T_0 + T_{\text{com}}$, the injection of i_{com} is stopped, and the active negative voltage clamping is kicked in the circuit to turn off the gate of S_3. Eventually, S_3 is completely in the gate-off state again.

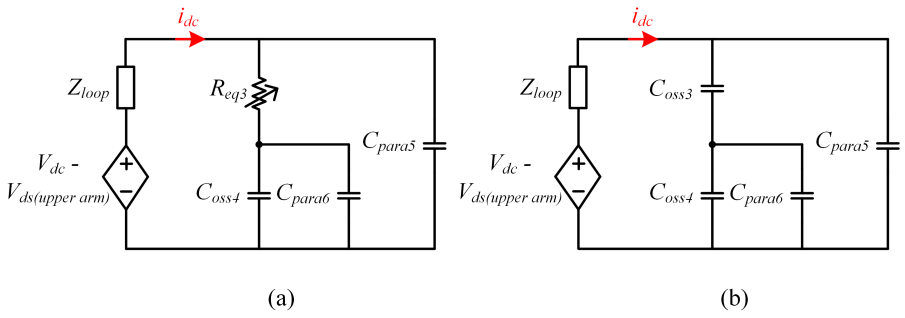


Figure 4.6: (a) Equivalent Circuit for the Lower Arm Switches During the 'Hard' Turn-off Transient When V_{gs} of S_3 Is Just Above the Threshold. (b) Equivalent Circuit for the Lower Arm Switches During the 'Hard' Turn-off Transient When V_{gs} of S_3 Is Below the Threshold.

During the dv/dt interval, when the gate-to-source voltage (V_{gs}) of S_3 exceeds the threshold, its impedance will be reduced significantly. Since V_{gs} of S_3 is just above the threshold, it should be regarded as a large equivalent resistor (R_{eq}) rather than the small on-state resistor (R_{dson}). The equivalent circuit for this situation is shown

in Fig. 4.6(a). The parameters are consistent with the parameters defined in Fig. 4.1. When the gate-to-source voltage of S_3 is below the threshold, it goes back to the high-impedance junction capacitor (C_{oss}), as shown in Fig. 4.6(b). Therefore, with the proposed strategy, the average dv/dt of S_3 can be reduced, and the equalized voltage sharing among the series-connected switches can be obtained, as shown in Fig. 4.5(b). It should be noted that though V_{gs} of S_3 is elevated during the dv/dt interval, the gate of S_4 is always completely off during the entire interval. Hence, the dc-link shoot-through will not occur for the proposed voltage balancing strategy.

Similar to the 'soft' tun-off scenario, T_{com} and i_{com} are the two free control variables. By appropriately regulating T_{com} and i_{com}, the well-balanced voltage sharing can be obtained for the series-connected switches in the stack. The detailed control algorithm of T_{com} and i_{com} will be introduced later.

4.3 Operating Principles of the Proposed Closed-loop Current Source Gate Driver

4.3.1 Hardware Architecture

The complete schematic of the proposed current source gate driver is shown in Fig. 4.7. The detailed operating principles of each part are introduced as follows.

Current mirror circuits

The current mirror circuits are utilized as the fast-responded, discontinuous current sources. The current source can be obtained by employing the current source inverter (CSI) as well [108]. However, there will be continuous flowing current in the switches for CSI, which will lead to the additional gate driving loss. The current mirror circuits are the voltage-controlled current sources. When the control voltage for the

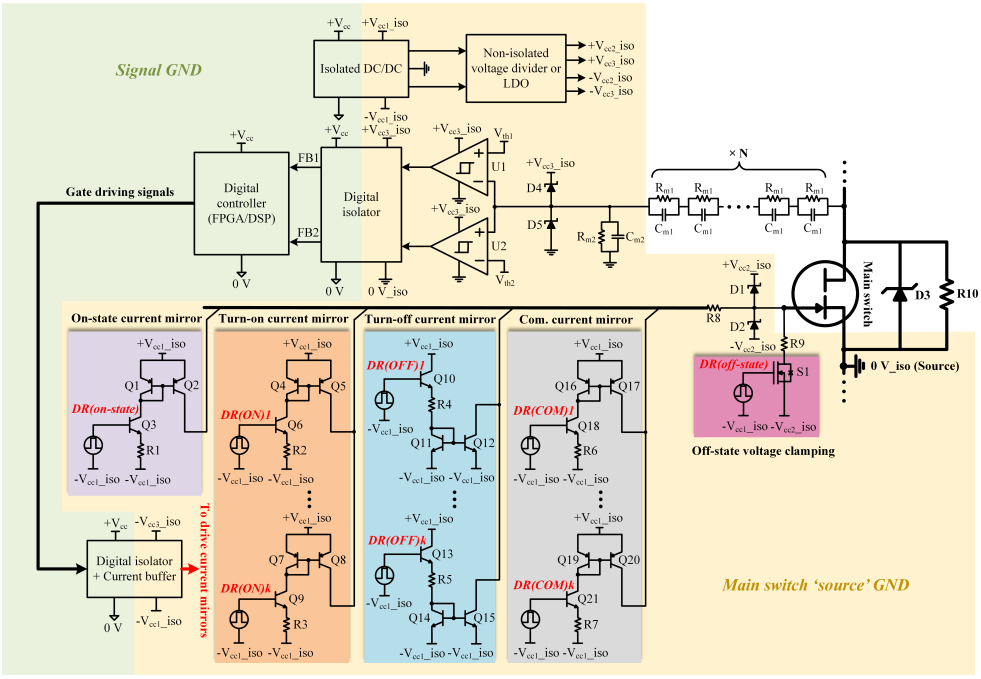


Figure 4.7: Complete Schematic of the Proposed Current Source Gate Driver.

current mirrors is in the low state, there will be no 'idle' loss. Therefore, the gate driving loss for the current mirror-based current source gate driver is comparable to the conventional voltage source gate driver [100].

Four sets of current mirror circuits are included in the proposed current source gate driver: the turn-on current mirror circuit (providing i_{ON}); the turn-off current mirror circuit (providing i_{OFF}); the compensation current mirror circuit (providing i_{com}) and the on-state current mirror circuit (providing $i_{\text{on-state}}$), which is only required for GaN GIT. Meanwhile, multiple current mirrors (k) are paralleled with separate driving signals for generating multilevel i_{ON}, i_{OFF} and i_{com}. Hence, the turn-on/turn-off speed as well as the magnitude of the compensation gate current can be regulated by enabling different level current mirrors.

The turn-on gate current (i_{ON}) from each current mirror circuit can be calculated as (taking the Q_4-Q_5-Q_6 current mirror as an example):

$$i_{\mathrm{ON}} = \frac{V_{\mathrm{drive(on)}} - V_{\mathrm{BE}}}{R_2} \tag{4.4}$$

where $V_{\mathrm{drive(on)}}$ is the driving voltage across Q_6 and R_2; V_{BE} is the base-to-emitter voltage drop for the BJTs (around 0.7 V).

Similarly, the turn-off gate current (i_{OFF}) from each current mirror circuit can be calculated as (taking the Q_{10}-Q_{11}-Q_{12} current mirror as an example):

$$i_{\mathrm{OFF}} = \frac{V_{\mathrm{drive(off)}} - 2V_{\mathrm{BE}}}{R_4} \tag{4.5}$$

where $V_{\mathrm{drive(off)}}$ is the driving voltage across Q_{10}, R_4 and Q_{11}.

The compensation current amplitude and on-state current amplitude can be calculated by (4.4) as well.

Based on (4.4) and (4.5), it is clear that the current mirror output current amplitude is determined by the driving voltage amplitude and the resistance value. To regulate the current amplitude, one solution is to change the driving voltage amplitude. Then the continuous varying output current can be realized. However, this solution needs to involve either the digital-to-analog converter (DAC) or the analog controller on the secondary side, which makes the structure of the gate driver more complicated. Another solution is to adjust the number of active current mirrors. Since several current mirrors are paralleled, the discrete varying output current can be obtained by enabling different level current mirrors. The latter solution is employed to simplify the gate driver structure for the proposed current source gate driver.

For the practical design of the current mirror circuits, the following rules should be followed. First, the switching speed of the current mirror transistors should be fast enough to ensure the gate current for the main switch reach the desired value most of the time within its switching transients [100]. The commercial state-of-the-art small-signal transistors have minimal input and output capacitances. For example,

for Diodes Incorporated 40 V/200 mA transistor pair (DMMT3904W), the input capacitance and output capacitance is only 8 pF and 4 pF, respectively. Based on the characteristics of the small-signal transistors, they are able to provide a very high slew rate pulse current. Second, since the slew rate of the pulse current is also limited by the gate loop stray inductance, the flux-cancellation technique should be employed for the gate driving loop PCB layout.

Voltage clamping circuits

One of the concerns for the current source gate driver is about the gate voltage clamping during the steady off-state or on-state due to the lack of the voltage source. The breakdown voltage of the Zener diode can be used to sustain the desired off-state or on-state gate-to-source voltage. However, it is found that the Zener diode clamping can not guarantee the stable off-state or on-state gate-to-source voltage in [100]. For the proposed current source gate driver, the isolated power supply is still needed to power the secondary side current mirror circuits, so the power supply can be directly used to clamp the gate voltage. As is shown in Fig. 4.7, during the off-state, the low-voltage MOSFET S_1 will be turned on to clamp the gate-to-source voltage to the desired off-state voltage ($-V_{\text{cc2\_iso}}$). The resistor R_9 is used to limit the peak transient current amplitude flowing through S_1. The pulse current rating of S_1 should exceed the peak transient current amplitude when S_1 is just turned on. It should be mentioned that the active on-state voltage clamping is not needed for the current-driven GaN GIT, but it is required for the voltage-driven p-gate GaN to achieve the stable on-state voltage. Meanwhile, the off-state/on-state active voltage clamping is only kicked in during the steady off-state/on-state. The current mirror circuits still supply the device gate current during the switching transients, so the gate driver is still based on the controllable current sources. Moreover, the Schottky

diodes D_1 and D_2 are utilized to suppress the gate-to-source voltage overshoot and undershoot during the switching transients.

Sensing circuit and window comparator

The voltage divider circuit is employed to sense the device drain-to-source voltage during the steady off-state. The pure resistive voltage divider is found to have a slow transient response, so the capacitive voltage divider is also employed [65, 109]. Based on the voltage divider operating principle, the sensed device drain-to-source voltage can be written as:

$$V_{\text{sense}} = \frac{R_{\text{m2}}}{N \cdot R_{\text{m1}} + R_{\text{m2}}} \cdot V_{\text{ds}} = \frac{\frac{C_{\text{m1}}}{N}}{\frac{C_{\text{m1}}}{N} + C_{\text{m2}}} \cdot V_{\text{ds}} \tag{4.6}$$

where V_{sense} is the sensed off-state drain-to-source voltage and N is the number of R_{m1} and C_{m1} parallel branches.

Larger capacitors (C_{m1} and C_{m2}) will help to improve the sensing circuit transient response. However, the series-connected sensing capacitors are directly placed between the drain and source of the main switch, so they are equivalent to the snubber capacitors. If C_{m1} and C_{m2} are set to be too large, the sensing circuit will slow down the main switch switching speed and produce an additional loss. Therefore, the total value of the sensing capacitors should be significantly lower than the device junction capacitance value.

As is shown in Fig. 4.7, the sensed drain-to-source voltage is the input for the window comparator. The window comparator has two thresholds (V_{th1} and V_{th2}), which indicate the desired off-state drain-to-source voltage range. The upper threshold V_{th1} represents the upper limit of the desired voltage range, while the lower threshold V_{th2} reflects the lower limit of the desired voltage range. If the desired voltage sharing is $\pm 10\%$ of the average voltage, the two thresholds can be expressed as:

$$V_{\text{th1}} = \frac{R_{\text{m2}}}{N \cdot R_{\text{m1}} + R_{\text{m2}}} \cdot \frac{V_{\text{dc}}}{M} \cdot 110\%$$
$$V_{\text{th2}} = \frac{R_{\text{m2}}}{N \cdot R_{\text{m1}} + R_{\text{m2}}} \cdot \frac{V_{\text{dc}}}{M} \cdot 90\% \tag{4.7}$$

where V_{dc} is the dc-link voltage and M is the number of the series-connected main switches.

Employing the window comparator brings two key benefits compared with the single threshold comparator. First, the over-voltage and the under-voltage of the main switch can be detected. When the under-voltage occurs, the over-voltage must occur for the other switches in the stack. Second, once the detected voltage is within the desired range, the digital tuning process is stopped, improving the closed-loop control's stability. The detailed adaptive digital tuning process in different switching scenarios will be explained later.

Meanwhile, it is obvious that the measured drain-to-source voltage is directly compared to the average value, so the voltage balancing strategy is independent for each switch. If the sensed voltages are compared with each other among the switches in the stack, the sequencing algorithm needs to be involved in the controller, which makes the control logic more complicated.

Moreover, when M switches are connected in series, the voltage balancing strategy can be implemented for $M-1$ switches. When the sensed drain-to-source voltages of the $M-1$ switches are all within the desired range, the last switch will achieve the desired drain-to-source voltage automatically. Hence, if two switches are connected in series, the proposed voltage balancing strategy can be employed for just one switch.

The output states of the window comparator are summarized in Table 4.1. The digital isolator is employed to transfer the outputs of the window comparator to the digital controller on the primary side. Based on the two feedback signals (FB1 and

Table 4.1: Output States of the Window Comparator.

Input	U_1 output	U_2 output	Voltage sharing
$V_{\text{sense}} < V_{\text{th2}}$	'1'	'0'	Under-voltage
$V_{\text{th2}} < V_{\text{sense}} < V_{\text{th1}}$	'1'	'1'	Desired voltage range
$V_{\text{sense}} > V_{\text{th1}}$	'0'	'1'	Over-voltage

FB2), the controller will implement the appropriate tuning algorithm for the compensation current mirrors in the next control cycle. The detailed tuning algorithms in different switching scenarios will be discussed later. It should be mentioned that the hysteresis comparators are recommended to prevent the state toggles caused by the ringings in the sensed voltage. Moreover, the Schottky diodes D_4 and D_5 are utilized to protect the input of the window comparator.

Power supplies

As is shown in Fig. 4.7, the isolated DC/DC power supply is needed for powering the current mirror circuits, digital isolators, current buffers, and comparators on the secondary side. A single isolated power supply with the non-isolated voltage dividers or low-dropout regulators (LDOs) can satisfy all the desired driving and signal conditioning voltage levels for the proposed current source gate driver.

First, the isolated DC/DC power supplies should have bidirectional outputs ($+V_{\text{cc1\_iso}}$ and $-V_{\text{cc1\_iso}}$) because the negative turn-off gate voltage is usually desired for the low-threshold GaN devices to prevent the mis-triggering during the switching transients [27, 110]. The main switch source should be set as the ground for the secondary side of the isolated DC/DC power supply. Meanwhile, the current mirror power supply voltage should be wider than the GaN device gate-to-source voltage range to guaran-

Table 4.2: Practical Selection of Driving and Signal Conditioning Voltage Level for GaN Devices.

Parameters	Symbol	Voltage level referred to the main switch source
Current mirror positive supplied voltage	$+V_{\text{cc1\_iso}}$	+9 V
Desired maximum gate-to-source voltage	$+V_{\text{cc2\_iso}}$	+6 V
Window comparator positive supplied voltage	$+V_{\text{cc3\_iso}}$	+5 V
Current mirror negative supplied voltage	$-V_{\text{cc1\_iso}}$	-9 V
Off-state gate-to-source voltage	$-V_{\text{cc2\_iso}}$	-6 V
Current mirror driving voltage	$-V_{\text{cc3\_iso}}$	-4V (+5 V referred to the current mirror ground)

tee the BJTs operate in the forward active region [100]. The desired gate-to-source voltage range for the main switch is from $-V_{\text{cc2\_iso}}$ to $+V_{\text{cc2\_iso}}$.

Second, the driving voltage of the current mirrors should be referred to their negative supplied voltage (the current mirror ground), so it can be negative ($-V_{\text{cc3\_iso}}$) referred to the main switch source ground.

Finally, since the window comparator refers to the main switch source ground, another positive supply voltage ($+V_{\text{cc3\_iso}}$) should be generated for powering the comparator and the following digital isolator. It should be mentioned again that only the widest bidirectional voltages ($+V_{\text{cc1\_iso}}$ and $-V_{\text{cc1\_iso}}$) are directly obtained from the isolated DC/DC power supply. All the other voltage levels are generated from the secondary side non-isolated voltage dividers or LDOs. Since all the components sit on the main switch source ground, no additional isolation is needed for the sec-

ondary side of the proposed gate driver. A practical selection of driving and signal conditioning voltage levels for GaN devices is listed in Table 4.2.

Static voltage sharing resistors and transient voltage suppressor (TVS) diodes

The static voltage sharing resistor (R_{10}) is utilized for equalizing the steady-state voltage sharing. Its value should be in the range of hundreds of kΩ, so the additional loss generated in the resistor is negligible. Since its value is so large, it will not help the device dynamic voltage balancing at all.

The transient voltage suppressor (TVS) diode (D_3) should be employed to prevent the over-voltage breakdown of the main switch for the initial few switching cycles because the closed-loop control is one-control-cycle delayed. Since the TVS diode only dissipates the energy of voltage spike for very few switching cycles, the size of the TVS diodes can be very compact. Meanwhile, for the state-of-the-art 500 V$\sim$600 V TVS diode, the junction capacitance is only around 10 pF, which has minimal impact on the main switch switching speed.

To sum, the proposed current source gate driver has the following outstanding features:

1) Functionality.

The proposed gate driver provides a multilevel turn-on gate current, turn-off gate current, and compensation gate current. The fast-responded, flexible current sources can regulate the gate current to various profiles. Therefore, the proposed gate driver can not only counteract the voltage imbalance brought by the device-to-ground displacement current but actively control the device di/dt and dv/dt to balance the device switching energy and turn-off voltage overshoot. The latter function is achieved by using a multilevel voltage source gate driver in [111]. The same function can be

easily achieved by using the proposed multilevel current source gate driver as well.

2) Simplicity.

The proposed gate driver has a very simplified architecture. The pure digital implementation eliminates the analog-to-digital converters (ADC) and the digital-to-analog converters (DAC). Meanwhile, no analog PI controllers and sample-and-hold circuits are involved as well. All the secondary side components (except for the sensing circuit) sit on the main switch source ground, so no other isolation is needed. In [65, 109], since the current mirror circuit is referred to the main switch gate, an additional isolation stage is required. Moreover, all the selected components are in tiny packages so that the size can be very compact for the proposed gate driver.

3) Reliability.

The proposed gate driver can achieve reliable voltage balancing control for the series-connected GaN devices. The window comparator monitors both over-voltage and under-voltage of the main switch during the off-state. When the sensed voltage is within the desired voltage range, the digital tuning process stops. Meanwhile, the compensation gate current can be set at very small amplitude, so extremely fine adjustment of the device rising drain-to-source voltage starting timing and slew rate can be achieved without requiring the controller to have a very tiny resolution. Moreover, the TVS diode is employed to avoid the over-voltage breakdown for the device during the very first few switching cycles.

4) Low cost.

The cost of the additional components for the proposed current source gate driver is negligible compared to the cost of main switches (GaN). The current mirror circuits are built by low-cost BJTs, and the sensing circuits are made up of inexpensive surface mount capacitors and resistors. For the controller, FPGA is selected for the purpose of fast prototyping. In the future, the cheap micro-controller and logic gates can be

employed to reduce the cost further. The parameters and part numbers of all the selected components will be presented in the experimental verification part.

4.3.2 Control Algorithm

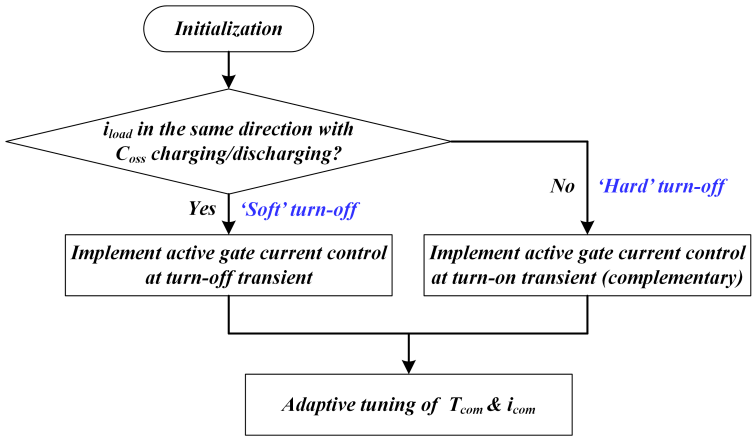


Figure 4.8: The Proposed Top-level Control Algorithm.

Based on the previous analysis, two control variables (T_{com} and i_{com}) are available for balancing the voltage sharing of the series-connected switches, which is equivalent to regulate Q_{com}. For the proposed current source gate driver, the regulation range and resolution of i_{com} are restricted by the number of paralleled current mirrors. However, for T_{com}, it can be regulated in a large range with the controller minimum time step size. Therefore, T_{com} is selected as the major control variable.

In this way, the change of the compensation gate charge for each unit step is:

$$Q_0 = \Delta t \cdot i_{\text{com}} \tag{4.8}$$

where Δt is the unit time step in the controller.

It is clear that if i_{com} is fixed, Q_0 will be consistent for all operating conditions, which may be not ideal regarding the transient response and steady-state errors. In particular, in the 'soft' turn-off scenario, the dv/dt is determined by the load current

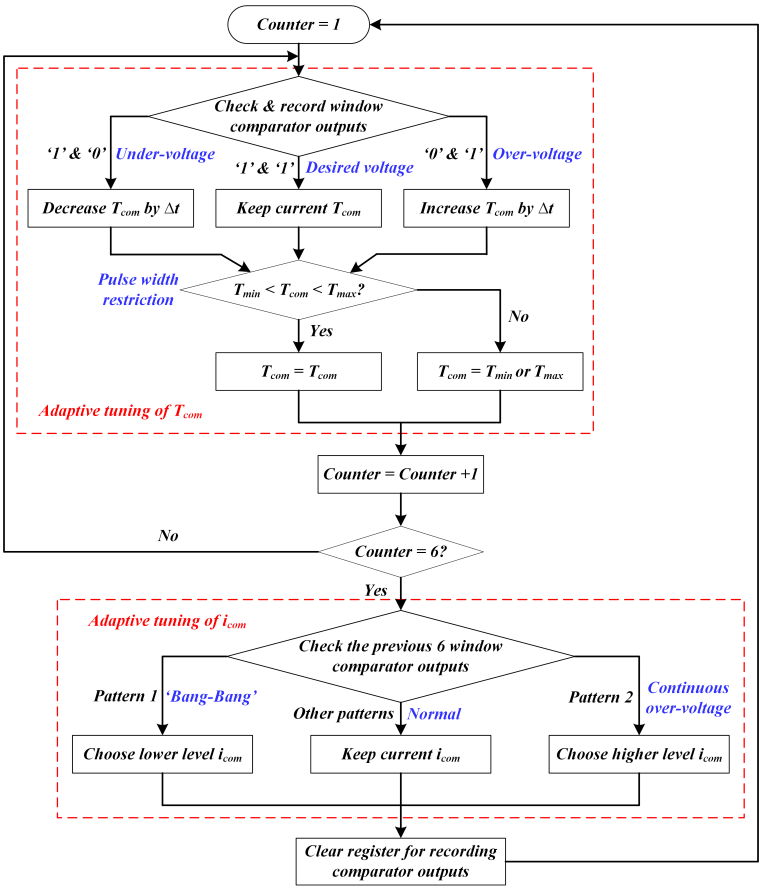


Figure 4.9: The Proposed Control Algorithm for T_{com} and i_{com}.

amplitude. In light load conditions, the dv/dt is low, so the desired turn-off timing difference between the series-connected switches is relatively large [100]. Larger Q_0 is preferred in this situation to obtain a faster transient response. However, in heavy load conditions, the dv/dt is high, so the desired turn-off timing difference between the series-connected switches becomes smaller. Then smaller Q_0 is preferred in this situation to do the 'fine-tuning'; otherwise, large steady-state errors may occur.

The proposed current source gate driver provides different levels of Q_0 by tuning i_{com} discretely, so the adaptivity to different operating conditions is excellent. In the 'soft' turn-off scenario, higher levels of current mirrors are enabled to generate larger Q_0 for lighter load conditions, and lower levels of current mirrors are enabled

to generate smaller Q_0 for heavier load conditions. In the 'hard' turn-off scenario, the dv/dt is determined by the gate current amplitude of the complementary turn-on switch rather than the load current amplitude [112]. Hence, lower levels of current mirrors ('fine-tuning') should be enabled for a more enormous turn-on gate current situation. The unit time step can be kept at the minimum interval Δt for the best tuning resolution.

Another possible solution for varying Q_0 is to keep i_{com} fixed but adjust the unit time step Δt for different operating conditions. However, this solution has the same drawback as the voltage source gate driver, where the signal timing is the only control variable. To achieve the 'fine-tuning' for higher dv/dt scenarios, the minimum Δt needs to be set very small (below 1 ns), so the accuracy is easy to be affected by signal jitters [85]. In this study, the controller minimum time step is selected to be 5 ns, which has much better immunity to signal jitters.

To sum, for the proposed current source gate driver, the compensation gate current pulse width (T_{com}) is selected as the major control variable, while the compensation gate current amplitude (i_{com}) is utilized to provide variable tuning resolutions for adapting to different operating conditions. The detailed control algorithm of T_{com} and i_{com} is introduced as follows.

The proposed top-level control algorithm is shown in Fig. 4.8. After the initialization, the load current direction needs to be known to determine the device turn-off scenario, which can be obtained from the load current sensor. If the load current direction is the same as the device junction capacitance charging/discharging direction, the device will experience 'soft' turn-off [shown in Fig. 4.1(a)]. Then the active gate current control is implemented at device turn-off transient, as shown in Fig. 4.3. If the load current direction is the opposite to the device junction capacitance charging/discharging direction, the device will experience 'hard' turn-off [shown in

Fig. 4.1(b)]. Then the active gate current control is implemented at complementary device turn-on transient, as shown in Fig. 4.5. Once the switching scenario of the device is determined, the adaptive tuning of T_{com} and i_{com} should be executed next.

The proposed control algorithm for T_{com} and i_{com} is shown in Fig. 4.9. A counter is utilized to trigger the adaptive tuning of i_{com} after six control cycles for T_{com}. Within each control cycle of T_{com}, the window comparator outputs will be detected and recorded at first. The two outputs of the window comparator reflect the voltage sharing of the device during the steady off-state. According to Table 4.1, three output states are possible:

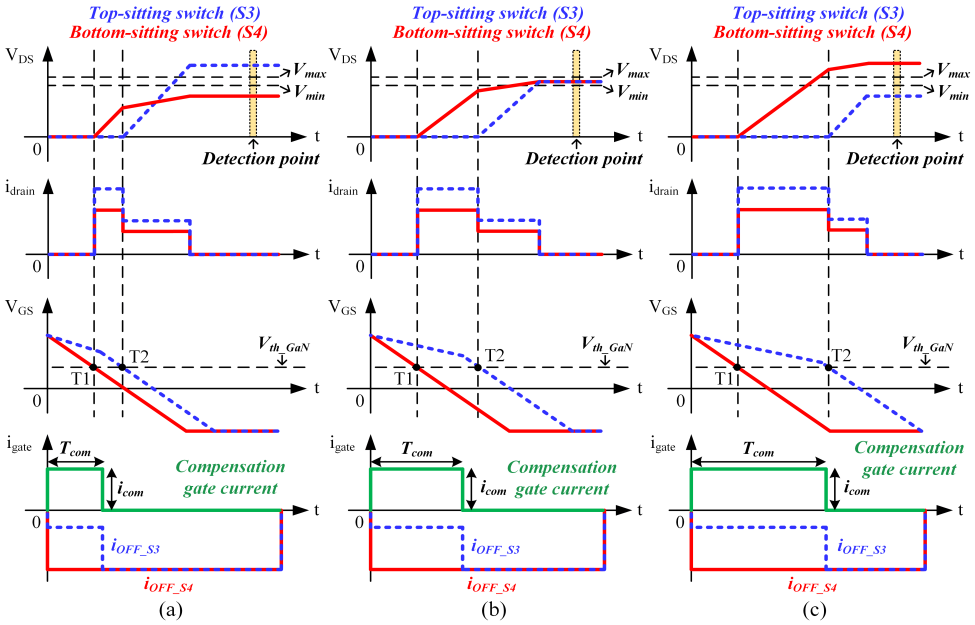


Figure 4.10: Different States During the Adaptive Tuning of T_{com} in 'Soft' Turn-off Scenario. (a) Under-compensated State (S_3 Over-voltage). (b) Well-compensated State. (c) Over-compensated State (S_3 Under-voltage).

1) If the two outputs are '1' & '0', the device V_{ds} is below the desired range, which indicates over-compensation. In the next control cycle, T_{com} should be decreased by a unit time step Δt.

2) If the two outputs are '0' & '1', the device V_{ds} is beyond the desired range, which

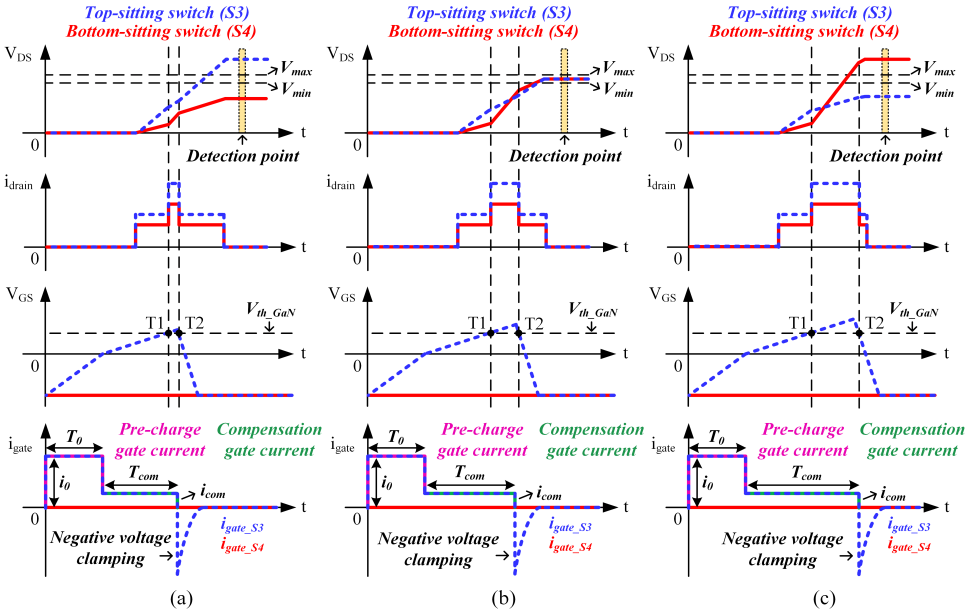


Figure 4.11: Different States During the Adaptive Tuning of T_{com} in 'Hard' Turn-off Scenario. (a) Under-compensated State (S_3 Over-voltage). (b) Well-compensated State. (c) Over-compensated State (S_3 Under-voltage).

indicates under-compensation. In the next control cycle, T_{com} should be increased by a unit time step Δt.

3) If the two outputs are '1' & '1', the device V_{ds} is within the desired range. In the next control cycle, T_{com} should remain the current value.

The three possible situations during the adaptive tuning of T_{com} for 'soft' turn-off and 'hard' turn-off scenarios are presented in Fig. 4.10 and Fig. 4.11, respectively. In Fig. 4.10, T_1 and T_2 illustrate the turn-off timing for the two series-connected switches. In Fig. 4.11, T_1 and T_2 illustrate the timing when the gate-to-source voltage of the top-sitting switch crosses the threshold. Meanwhile, the profile of the device drain currents is related to the transition of the equivalent circuits for different intervals, which has been discussed earlier (shown in Fig. 4.4 and Fig. 4.6). Moreover, the detection point in both figures represents the timing for checking the window comparator outputs. To avoid the influence of device turn-off V_{ds} ringings,

sufficient margin should be reserved between the end of the turn-off transient and the detection point.

Then T_{com} needs to be restricted within the reasonable range (T_{min}~T_{max}). T_{min} should be large than the unit time step Δt. For 'soft' turn-off scenario, T_{max} should not exceed the pulse width of the turn-off gate current (T_{OFF}). For 'hard' turn-off scenario, T_{max} should not exceed the difference of pulse width for the turn-on gate current and the pulse width for the pre-charge gate current (T_{ON} - T_0).

When one control cycle of T_{com} is finished, the counter should be added by 1. If the counter reaches 6, the adaptive tuning of i_{com} will be triggered. The level of i_{com} will be determined by the pattern recognition of the recorded previous six states of the window comparator outputs:

1) Pattern 1 is defined as: '1' & '0', '0' & '1', '1' & '0', '0' & '1', '1' & '0', '0' & '1'; or '0' & '1', '1' & '0', '0' & '1', '1' & '0', '0' & '1', '1' & '0'. Based on Table 4.1, this pattern indicates the device is swapping between the under-compensated state and the over-compensated state for consecutive three times (the 'bang-bang' phenomenon), which means the change of compensation gate charge during each unit time step (Q_0) is too large. Hence, once this pattern is detected, lower level i_{com} should be selected to increase the tuning resolution.

2) Pattern 2 is defined as: '0' & '1', '0' & '1', '0' & '1', '0' & '1', '0' & '1', '0' & '1'. Based on Table 4.1, this pattern indicates the device is in the under-compensated state for consecutive six cycles, which means the change of compensation gate charge during each unit time step (Q_0) is too small. Hence, once this pattern is detected, higher level i_{com} should be selected to accelerate the transient response.

3) For all the other patterns, i_{com} remains at the current level.

After the adaptive tuning of i_{com} is finished, the register for recording the comparator outputs should be cleared. Then the counter should return to 1.

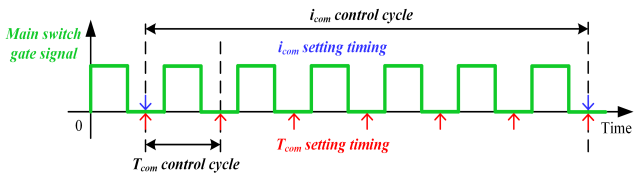


Figure 4.12: Indication of Timing for the Control Signals.

The timing of the control signals is shown in Fig. 4.12. It is clear that T_{com} should be updated during the main switch off period every switching cycle, while i_{com} should be updated during the main switch off period every six switching cycles. Therefore, the control cycle for i_{com} is six times of that for T_{com}. It should be noted that updating i_{com} every six switching cycles is just a reasonable selection for balancing the control stability and transient response in this study, which is not a must.

To sum, with employing adaptive tuning for T_{com} and i_{com}, the proposed current source gate driver is capable of compensating for the voltage imbalance brought by the device-to-ground displacement currents in different operating conditions.

4.4 Experimental Verification

4.4.1 Experimental Setup

Prototype design

A series-connected GaN-based multiple pulse tester (MPT) prototype with the proposed closed-loop current source gate driver (CSGD) is designed and fabricated as shown in Fig. 4.13. The MPT is a half-bridge converter. Two series-connected GaN HEMTs are employed for both the upper arm and the lower arm of the MPT. The schematic of the MPT is the same as the circuit shown in Fig. 4.1. The two upper arm switches are labeled as S_1 (top-sitting switch) and S_2 (bottom-sitting switch), while the two lower arm switches are labeled as S_3 (top-sitting switch) and S_4 (bottom-

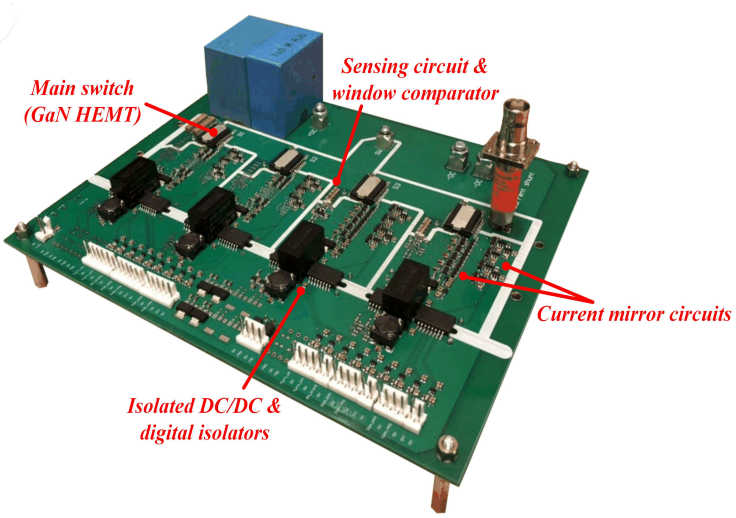


Figure 4.13: Prototype of a Series-connected GaN-based Multiple Pulse Tester with the Proposed Current Source Gate Driver.

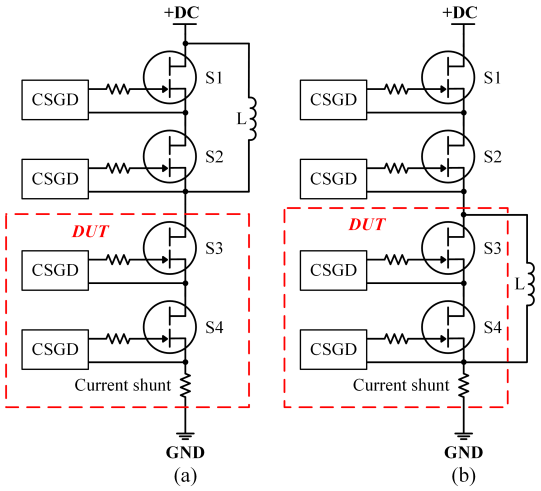


Figure 4.14: Schematic of Testing Circuits for Different Switching Scenarios. (a) 'Soft' Turn-off Scenario. (b) 'Hard' Turn-off Scenario.

sitting switch). Meanwhile, the lower arm switches are regarded as the device under test (DUT), and the lower arm device current is measured by T&M Research SDN-414 current shunt. When the 'soft' turn-off scenario is investigated, an air-core inductor needs to be paralleled with the upper arm switches [shown in Fig. 4.14(a)]; when the 'hard' turn-off scenario is investigated, an air-core inductor needs to be paralleled with the lower arm switches [shown in Fig. 4.14(b)]. Although only two switches

are connected in series for the prototype, the proposed gate driver and the adaptive voltage balancing scheme can be extended for more switches-in-series scenarios.

It should be mentioned that this prototype is just for proof of concept, so the power density is not optimized. The power density optimization of the series-connected GaN-based power converter will be explored in the future study. Infineon 600 V/30 A e-mode GaN (IGOT60R070D1) devices (GIT) are employed in this prototype. The active off-state gate voltage clamping circuit and the TVS diodes are on the back of the board presented in Fig. 4.13. The selected components for the proposed closed-loop current source gate driver are listed in Table 4.3. The labels of components are consistent with the labels presented in Fig. 4.7.

Verification of the current mirror circuit and the active voltage clamping circuit

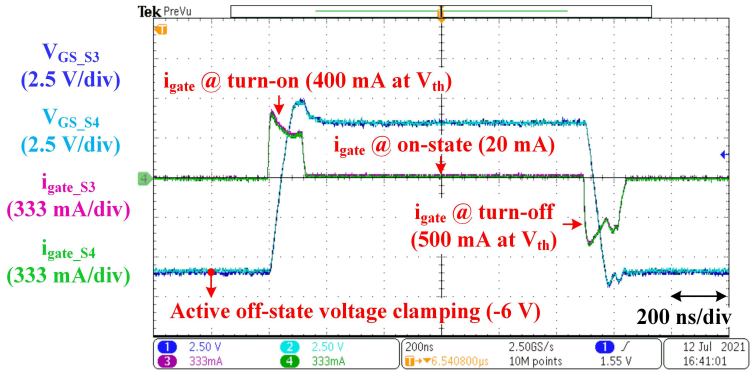


Figure 4.15: Gate-to-source Voltages and Gate Currents of the Device under Test (S_3 and S_4).

To validate the essential functions of the current mirror circuit and the active voltage clamping circuit, the gate-to-source voltage waveforms and gate current waveforms are captured without the main power as shown in Fig. 4.15. It should be mentioned that the captured gate current waveforms are the voltage waveforms across the 3-Ω gate resistor, so 1 volt across the gate resistor represents 330 mA gate current. From

Table 4.3: Selected Components for the Proposed Closed-loop Current Source Gate Driver.

Components	Values
Main switch	Infineon IGOT60R070D1
Q_1, Q_2, Q_4, Q_5, Q_7, Q_8, Q_{16}, Q_{17}, Q_{19}, Q_{20}	Diode Incorporated DMMT3906W
Q_3, Q_6, Q_9, Q_{10}, Q_{13}, Q_{18}, Q_{21}	On Semiconductor FMB3904
Q_{11}, Q_{12}, Q_{14}, Q_{15}	Diode Incorporated DMMT3904W
S_1	On Semiconductor BSS138
D_1, D_2, D_4, D_5	STMicroelectronics STPS140Z
D_3	Littelfuse 1.5SMC550CA
R_1	422 Ω
R_2, R_3	21 Ω
R_4, R_5	17 Ω
R_6, R_7	82 Ω
R_8	3 Ω
R_9	10 Ω
R_{10}	330 kΩ
R_{m1}, R_{m2}	250 kΩ and 6.2 kΩ, respectively
C_{m1}, C_{m2}	54 pF and 2180 pF, respectively
Number of R_{m1} and C_{m1}	4
U_1, U_2	Analog Device ADCMP601
Isolated DC/DC	RECOM Power R12P209D/P
Digital isolator	Analog Device ADuM260N
Digital controller	Xilinx Spartan-6 FPGA
Controller unit time step	5 ns

the experimental waveforms, the following conclusions can be made.

1) The current mirror circuit can successfully drive the GaN devices. The device gate-to-source voltage slew rate is determined by the current mirror output current amplitude during the turn-on and turn-off switching transients. The turn-on gate current is selected to be 400 mA, and the turn-off gate current is chosen to be 500 mA in this study for balancing the switching energy and device turn-off voltage overshoot. Meanwhile, the constant small current (around 20 mA) from the current mirror is injected into the gate during the entire on-state to maintain the low R_{dson} of the GaN device (GIT).

2) The active off-state voltage clamping circuit is able to sustain the off-state gate-to-source voltage at the desired -6 V during the entire off-state. Since the active clamping circuit is kicked in after the turn-off switching transient, the turn-off transient gate current is still determined by the current mirror circuit.

3) Since the closed-loop control is disabled for now, the desired turn-on and turn-off gate currents are the same for both of the lower arm switches (S_3 and S_4). Based on the experimental waveforms, very synchronized gate-to-source voltages are obtained for both turn-on and turn-off transients, which indicates the highly consistent design and circuit layout for the gate driving circuits of different channels.

Verification of the sensing circuit and the window comparator

To validate the basic functions of the sensing circuit and the window comparator circuit, the multiple pulse test is conducted and the captured sensing circuit output and feedback signals for the top-sitting switch (S_3) are shown in Fig. 4.16. Since the closed-loop control is disabled for now, the top-sitting switch (S_3) will have a higher off-state drain-to-source voltage. The desired off-state drain-to-source voltage for S_3 is 300 V (the dc-link voltage is 600 V). To check the output states of the feedback

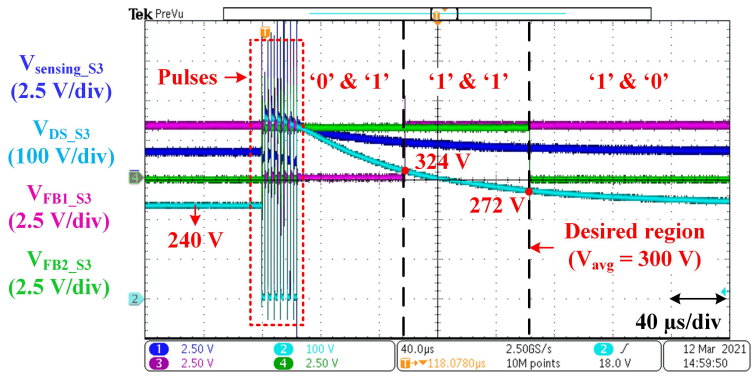


Figure 4.16: Sensing Circuit Output and Feedback Signals for the Lower Arm Top-sitting Switch (S_3).

signals in the under-voltage scenario as well, the actual dc-link voltage is set to be around 480 V. The initial off-state V_{ds} of S_3 will be around 240 V, which is below the desired voltage range.

The two feedback signals (FB1 and FB2) are the isolated outputs of the window comparator. As is shown in Fig. 4.16, when the last pulse finishes, V_{ds} of S_3 is far above 300 V. The states of the two feedback signals are '0' and '1', which indicates the over-voltage of S_3. After a short period, V_{ds} of S_3 drops within the desired voltage range (272 V∼324 V), and the states of the two feedback signals change to '1' and '1'. Eventually, V_{ds} of S_3 declines below the desired voltage range. The states of the two feedback signals change to '1' and '0', which represents the under-voltage of S_3. Since the experimental results are consistent with the desired output of the window comparator (shown in Table 4.1), the functions of the sensing circuit and the window comparator are valid.

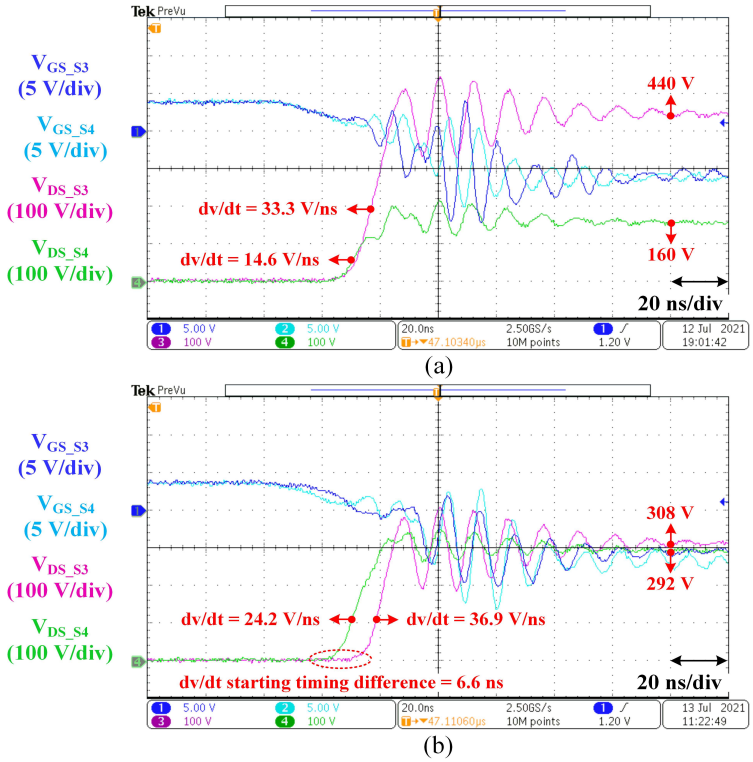


Figure 4.17: Waveforms for Lower Arm Switches 'Soft' Turn-off in 600 V_{dc} and 26 A Load Current Condition. (a) Without Active Gate Current Control. (b) With Active Gate Current Control.

4.4.2 Verification of the Proposed Voltage Balancing Scheme in 'Soft' Turn-off Scenario

Voltage balancing effectiveness

The waveforms for the lower arm switches (S_3, S_4) 'soft' turn-off transient in 600 V_{dc} and 26 A load current condition are captured. The testing circuit is the same as Fig. 4.14(a). As shown in Fig. 4.17(a), without the active gate current control, S_3 exhibits higher dv/dt than S_4, which results in 46.7% over-voltage for S_3 compared with the desired average value (300 V). It is clear that during most of the time in the dv/dt transient the gate-to-source voltages of the two switches already drop below the threshold (around 1 V). Therefore, the voltage sharing difference is caused by the

variance in the drain current because of the contribution from the drain-to-ground displacement current (labeled as i_{p6} in Fig. 4.1).

With the implementation of the active gate current control, the total turn-off gate current for S_3 is reduced due to the compensation current, so the dv/dt starting timing of the S_3 is delayed appropriately (6.6 ns). Though the dv/dt of S_3 is still higher than S_4, the two switches can reach the steady-state value at the same time because of the starting timing difference. As a result, the over-voltage for S_3 is cut down to 2.7% compared with the desired average value, as shown in Fig. 4.17(b). The experimental result successfully validates the theoretical analysis in Fig. 4.3.

Switching energy discussion

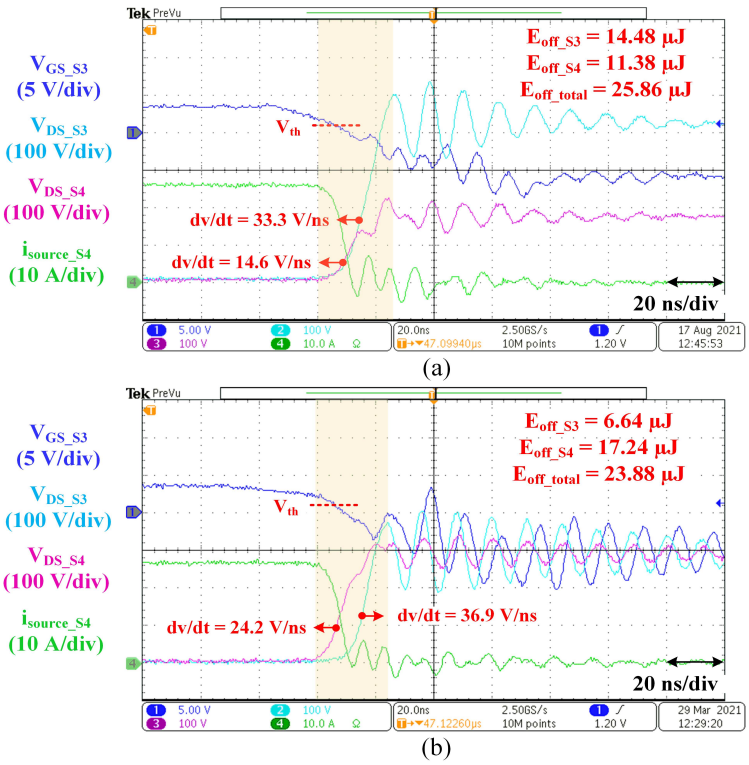


Figure 4.18: Switching Energies for Lower Arm Switches 'Soft' Turn-off at 600 V_{dc} and 26 A Load Current. (a) Without Active Gate Current Control. (b) With Active Gate Current Control.

The switching energies for the lower arm switches (S_3 and S_4) 'soft' turn-off at 600 V_{dc} and 26 A load current are shown in Fig. 4.18. The source current of the bottom-sitting switch (S_4) is monitored by T&M Research SDN-414 current shunt. Based on the experimental waveform, the following conclusions can be made.

1) Without the active gate current control, the rising dv/dt of the top-sitting switch (S_3) is higher than the rising dv/dt of the bottom-sitting switch (S_4). By actively delaying the dv/dt starting timing for S_3, the well-balanced voltage sharing is obtained.

2) Since no snubber circuit or extra Miller capacitor is employed, the switching speed and switching energy of GaN devices are not compromised. With the active gate current control, the total 'soft' turn-off energy becomes even lower. The device channel current is cut down significantly once one of the switches in the series-connected stack is turned off. Therefore, the delayed turn-off switch (S_3) produces much-reduced turn-off energy. Meanwhile, for the top-sitting switch (S_3), it is clear that the drain-to-source voltage starts to rise after its gate-to-source voltage drops below the threshold (around 1 V), which means the device channel is already cut off before the dv/dt transient. Hence, the turn-off energy is minimized.

3) With the active gate current control, since the device voltage and current overlapping is larger for the bottom-sitting switch (S_4), the turn-off energy of S_4 is larger than that of S_3. It is an intrinsic drawback for the so-called active gate delay control voltage balancing scheme as pointed out in [100]. However, this phenomenon can have little impact on the thermal balance among the series-connected switches in real applications [100]. The 'hard' turn-on loss of the GaN devices is typically dominant for hard-switching applications, such as the PWM converters. As long as each device's 'hard' turn-on loss is comparable, the thermal balance among the series-connected switches will not be an issue. For soft-switching applications, such

as LLC resonant converters, the unbalanced turn-off loss will play a more important role, but the other losses (conduction loss, dead-time loss) need to be considered as well. If the unbalanced turn-off loss is not dominant in the device's total loss, it will have an insignificant effect on the practical heat sink design. In the future study, the converter-level verification will be conducted for soft-switching applications to evaluate the thermal performance of each device under this voltage balancing scheme.

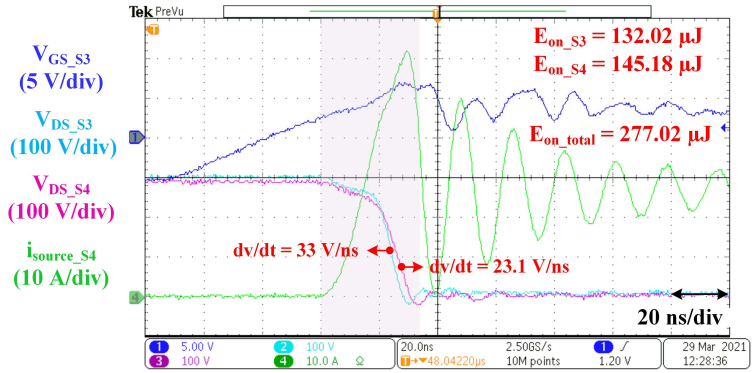


Figure 4.19: Switching Energies for Lower Arm Switches 'Hard' Turn-on at 600 V_{dc} and 26 A Load Current.

Under the same testing circuit [shown in Fig. 4.14(a)], the lower arm switches experience a 'hard' turn-on process. The switching energies for the lower arm switches (S_3 and S_4) 'hard' turn-on at 600 V_{dc} and 26 A load current are shown in Fig. 4.19. The active gate current control is not implemented during the turn-on transient because the drain-to-source voltages of the series-connected switches are heading to zero, and the over-voltage is less likely to occur. Based on the experimental waveform, the following conclusions can be made.

1) The falling dv/dt of the top-sitting switch (S_3) is higher than the falling dv/dt of the bottom-sitting switch (S_4) as well, because S_3 has higher gate current than S_4 (contributed by the gate-to-ground displacement current). However, since the drain-to-source voltages of the two switches are heading to zero, the over-voltage is unlikely to occur. Meanwhile, the starting timing of the falling dv/dt is very synchronized for

the two switches, which implies the consistency of the design and circuit layout for different channels.

2) The 'hard' turn-on energies for the two switches are comparable, and their values are significantly larger than the 'soft' turn-off energies (shown in Fig. 4.18) at the same load current condition. Therefore, as discussed before, the device 'hard' turn-on loss will be dominant in the hard-switching applications. The thermal balance will not be an issue as long as the 'hard' turn-on energies are comparable among the series-connected switches. It should be noted that the turn-on energies of the two switches can be significantly different if the gate-to-ground displacement current is large compared with the supplied turn-on gate current. For this situation, the proposed current source gate driver can easily compensate the contribution from the gate-to-ground displacement current. Then the balanced turn-on energies for the series-connected switches will be obtained.

4.4.3 Verification of the Proposed Voltage Balancing Scheme in 'Hard' Turn-off Scenario

Voltage balancing effectiveness

The testing circuit for the lower arm switches 'hard' turn-off is the same as Fig. 4.14(b). When the upper arm switches (S_1, S_2) are 'hard' turned on, the drain-to-source voltages of the lower arm switches (S_3, S_4) are forced to be pulled up and the voltage imbalance occurs, as shown in Fig. 4.20(a). It is clear that the gate-to-source voltage of S_3 is far below the threshold when the dv/dt occurs, so the impedance of S_3 is very high during this transient. The existence of the drain-to-ground displacement current will lead to the variance in the device drain currents, which results in voltage imbalance. In the operating condition of 600 V_{dc} and 26 A load current, the top-

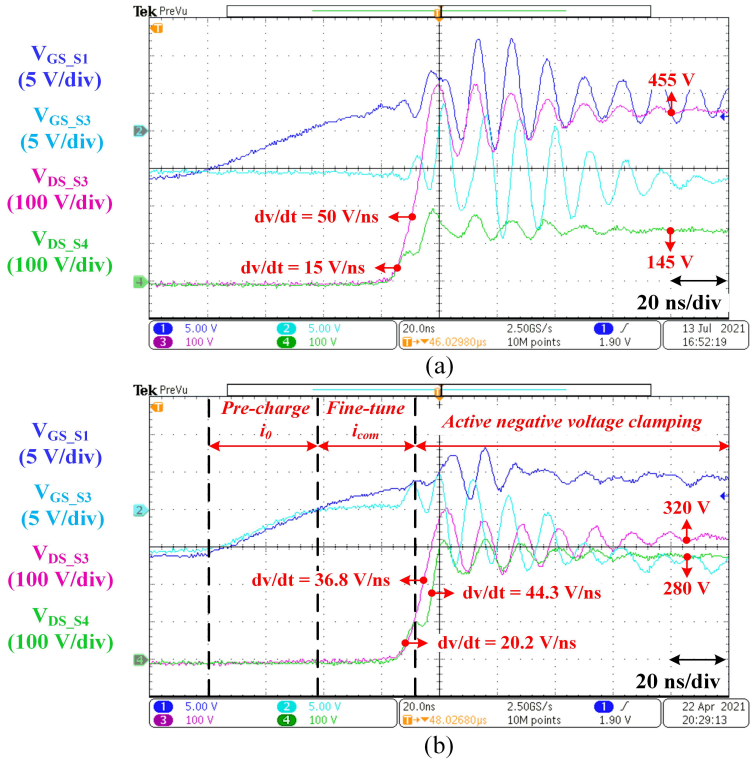


Figure 4.20: Waveforms for Lower Arm Switches 'Hard' Turn-off in 600 V_{dc} and 26 A Load Current Condition. (a) Without Active Gate Current Control. (b) With Active Gate Current Control.

sitting switch S_3 exhibits higher dv/dt than the bottom-sitting switch S_4 does, which results in 51.7% over-voltage for S_3 compared with the desired average value (300 V).

With the implementation of the active gate current control, the compensation current is actively injected into the gate of S_3 to elevate its gate-to-source voltage closer to the threshold voltage when the dv/dt occurs. The large pre-charge gate current i_0 is used to reduce the rise time for the gate-to-source voltage of S_3, and the small compensation gate current i_{com} is employed to achieve the 'fine-tuning'. Right after the end of the compensation current pulse, the active negative voltage clamping is kicked in to safely turn off the gate of S_3. In this way, the average dv/dt of S_3 is decreased due to its reduced impedance. The over-voltage of S_3 is cut down to 6.7% compared with the desired average value, as shown in Fig. 4.20(b). The experimental

result successfully validates the theoretical analysis in Fig. 4.5.

Switching energy discussion

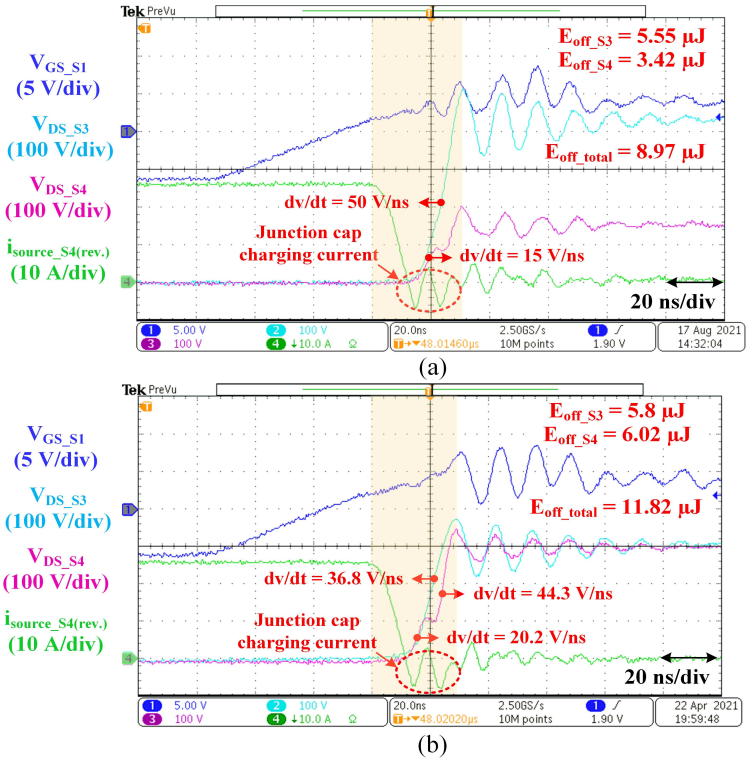


Figure 4.21: Switching Energies for Lower Arm Switches 'Hard' Turn-off at 600 V_{dc} and 26 A Load Current. (a) Without Active Gate Current Control. (b) With Active Gate Current Control.

The switching energies for the lower arm switches (S_3 and S_4) 'hard' turn-off at 600 V_{dc} and 26 A load current are shown in Fig. 4.21. The source current of the bottom-sitting switch (S_4) is monitored by T&M Research SDN-414 current shunt. The actual current is flowing from the device source to drain in this scenario. Since the positive voltage across the current shunt represents the current flowing from the device drain to source, the current direction is reversed in Fig. 4.21. The turn-off dv/dt and turn-off energies of the two switches are shown in Fig. 4.21 as well. Based on the experimental waveform, the following conclusions can be made.

1) Without the active gate current control, the rising dv/dt of the top-sitting switch (S_3) is higher than the rising dv/dt of the bottom-sitting switch (S_4). After implementing the active gate current control, the average rising dv/dt of the top-sitting switch (S_3) is comparable to that of the bottom-sitting switch (S_4), which results in balanced voltage sharing.

2) With the active gate current control, the turn-off energies for the two switches are very close and very minimal. During the dv/dt transient, since the load current has already been transferred to the complementary turn-on switches, only the junction capacitance charging current will flow through the lower arm switches. The overlapping between the device voltage and current is very limited. Due to one of the device channels' reopening, the total 'hard' turn-off energy is slightly higher than the uncompensated scenario. However, the difference is negligible compared with the complementary switch 'hard' turn-on energy. As shown in Fig. 4.19, the total 'hard' turn-on energy is 277.02 μJ. The increased 'hard' turn-off energy contributes less than 1% of the total switching energy during the hard-switching transient, which can be completely ignored. This result also verifies that the proposed voltage balancing scheme in the 'hard' turn-off scenario will not introduce significant additional loss.

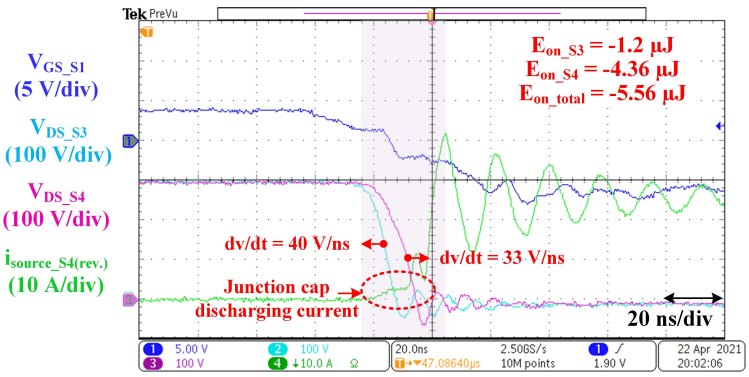


Figure 4.22: Switching Energies for Lower Arm Switches 'Soft' Turn-on at 600 V_{dc} and 26 A Load Current.

Under the same testing circuit [shown in Fig. 4.14(b)], the lower arm switches

experience a 'soft' turn-on. The switching energies for the lower arm switches (S_3 and S_4) 'soft' turn-on at 600 V_{dc} and 26 A load current are shown in Fig. 4.22. Again, the active gate current control is not implemented during the turn-on transient because the drain-to-source voltages of the series-connected switches are heading to zero, and the over-voltage is less likely to occur. Based on the experimental waveform, the following conclusions can be made.

1) The falling dv/dt of the top-sitting switch (S_3) is higher than the falling dv/dt of the bottom-sitting switch (S_4), because S_3 has a higher drain current than S_4, which is contributed by the drain-to-ground displacement current. However, since the two switches' drain-to-source voltages start to decline simultaneously, over-voltage is unlikely to occur.

2) The 'soft' turn-on energies for the two switches are very minimal. Since the energies are released from the device junction capacitors, a negative sign is added to represent the direction. In soft-switching applications, such as LLC resonant converters, the energies will be recycled.

To sum, the switching energies generated during the 'hard' turn-off and 'soft' turn-on transients are both insignificant compared with the device 'hard' turn-on energy. The proposed voltage balancing scheme in the 'hard' turn-off scenario will not introduce significant additional loss.

4.4.4 Verification of the Proposed Closed-loop Control Strategy in Different Operating Conditions

Since the load current direction is fixed in the experimental setup (shown in Fig. 4.14), the switching scenario of the device is determined. Hence, it is unnecessary to implement the top-level control algorithm, which is only required for the converter-level operation. The proposed closed-loop control strategy for the compensation gate

current pulse width and amplitude is verified in different switching scenarios.

'Soft' turn-off scenario

To verify the proposed closed-loop control strategy in the 'soft' turn-off scenario, the multiple pulse test is conducted under the 600 V dc-link condition. The frequency of the continuous pulses is 500 kHz. The air-core inductor is paralleled with the upper arm switches, and the lower arm switches experience 'soft' turn-off, as shown in Fig. 4.14(a).

First, the captured waveform for the open-loop case is shown in Fig. 4.23(a). The initial voltage sharing between the two lower arm switches is balanced, which is due to the employment of the large static voltage sharing resistor (R_{10} in Fig. 4.7). However, when the first switching event occurs, a severe voltage imbalance is observed. The top-sitting switch (S_3) has higher drain-to-source voltage than the bottom-sitting switch S_4 does, which is consistent with the previous theoretical analysis.

Second, the captured waveform for the closed-loop (only with T_{com} control) case is shown in Fig. 4.23(b). The adaptive tuning of the compensation gate current pulse width (T_{com}) is implemented, and the unit time step (ΔT) is selected to be 5 ns. The 5-ns unit time step is not very short, so it has good immunity from signal jitters, improving the control reliability. Based on the previous analysis, the desired turn-off delay for the top-sitting switch is larger in lighter load conditions and becomes shorter in heavier load conditions for the 'soft' turn-off scenario. Since the constant i_{com} is applied for the entire load range, the voltage balancing performance is not ideal. In lighter load conditions, it takes a lot of steps to achieve the desired turn-off delay for the top-sitting switch, which brings the slow transient response as shown in Fig. 4.23(b). In heavier load conditions, the change of the gate charge is too large for each unit step, so severe voltage imbalance occurs again, and the 'bang-bang' phenomenon

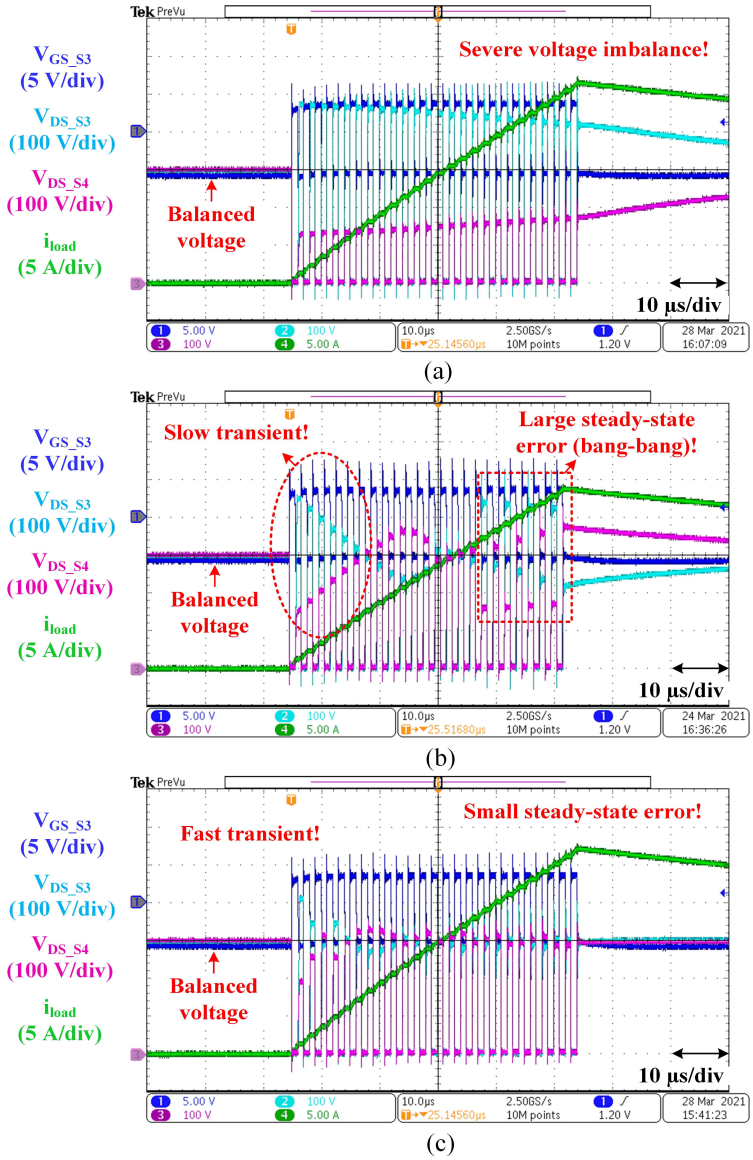


Figure 4.23: Multiple Pulse Test for Lower Arm Switches 'Soft' Turn-off Scenario at 600 V_{dc}. (a) Open-loop. (b) Only with T_{com} Closed-loop Control. (c) With Both T_{com} and i_{com} Closed-loop Control.

is observed for the voltage sharing between the two switches, as shown in Fig. 4.23(b).

Finally, the captured waveform for the closed-loop (with both T_{com} and i_{com} control) case is shown in Fig. 4.23(c). The adaptive tuning of the compensation gate current pulse width (T_{com}) and amplitude (i_{com}) are both implemented. In lighter load conditions, i_{com} is set to be larger to improve the transient response; in heavier

load conditions, i_{com} is set to be smaller to guarantee the 'fine-tuning' of the turn-off delay. It should be noted that the control cycle for i_{com} is set to be twice rather than six times of the switching cycle in the 'soft' turn-off scenario. Since the load current changes rapidly during the multiple pulse test, a shorter control cycle of i_{com} improves the transient response. In the actual converter-level operation, the change of load current is typically much slower, so the control cycle of i_{com} can be set longer. As is shown in Fig. 4.23(c), the well-balanced voltage sharing (small steady-state error) is achieved for the entire load range with the fast transient response, which validates the proposed closed-loop control strategy in the 'soft' turn-off scenario.

Moreover, the two series-connected 600 V GaN devices are targeted at 800 V dc-link applications. The multiple pulse test is conducted for the 'soft' turn-off scenario under 800 V dc-link as well.

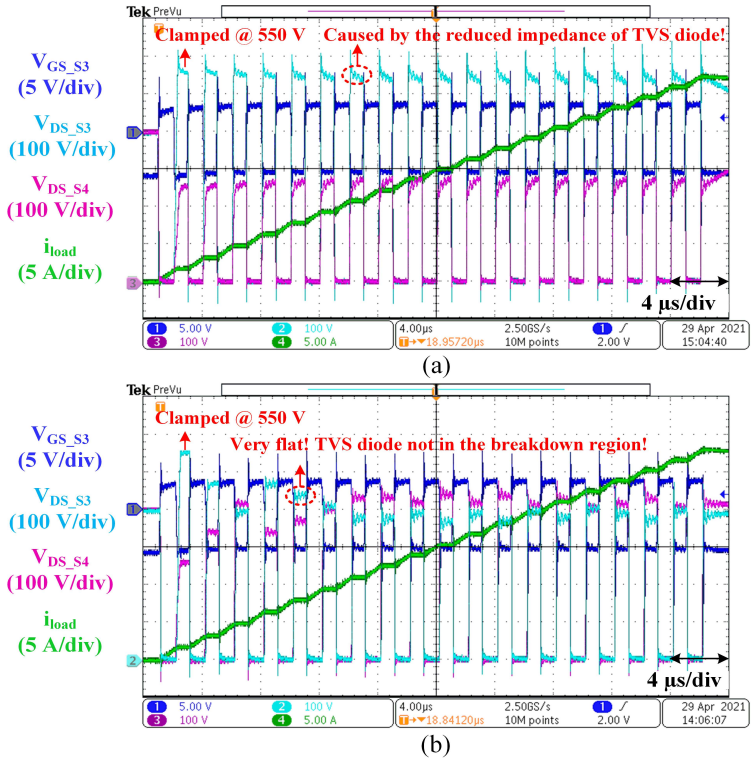


Figure 4.24: Multiple Pulse Test for Lower Arm Switches 'Soft' Turn-off Scenario at 800 V_{dc}. (a) Open-loop. (b) With Both T_{com} and i_{com} Closed-loop Control.

The experimental results for the 'soft' turn-off scenario without and with the proposed closed-loop control are shown in Fig. 4.24. Meanwhile, the nominal breakdown voltage for the selected TVS diode is 550 V (D_3 in Fig. 4.7), which is used for the transient over-voltage protection of the main switch. When the closed-loop control is not implemented, as shown in Fig. 4.24(a), severe voltage imbalance occurs, and the drain-to-source voltage of the top-sitting switch (S_3) is clamped by the TVS diode for every pulse. Due to the accumulated thermal stress, the leakage current of the TVS diode becomes larger with the emergence of more 'over-voltage' pulses. Therefore, the loss generated in the TVS diode will be considerable. If no active voltage balancing strategy is implemented, the TVS diode can be burned eventually. When the proposed closed-loop active gate current control is implemented, as shown in Fig. 4.24(b), the well-balanced voltage sharing is achieved, and the off-state drain-to-source voltage is very 'flat' for all the pulses, which indicates that the TVS diode is not in the breakdown region (except for the first pulse). Therefore, the leakage current in the TVS diode is minimal, and the loss generated in the TVS diode is insignificant.

'Hard' turn-off scenario

To verify the proposed closed-loop control strategy in the 'hard' turn-off scenario, the multiple pulse test is conducted under the 600 V dc-link condition. The frequency of the continuous pulses is 500 kHz. The air-core inductor is paralleled with the lower arm switches, and the lower arm switches experience 'hard' turn-off, as shown in Fig. 4.14(b).

First, the captured waveform for the open-loop case is shown in Fig. 4.25(a). The first channel is the gate-to-source voltage of the upper arm complementary switch (S_1). When S_1 is 'hard' turned on, the lower arm switches (S_3 and S_4) are experiencing the 'hard' turn-off. When the first switching event occurs, a severe voltage imbalance

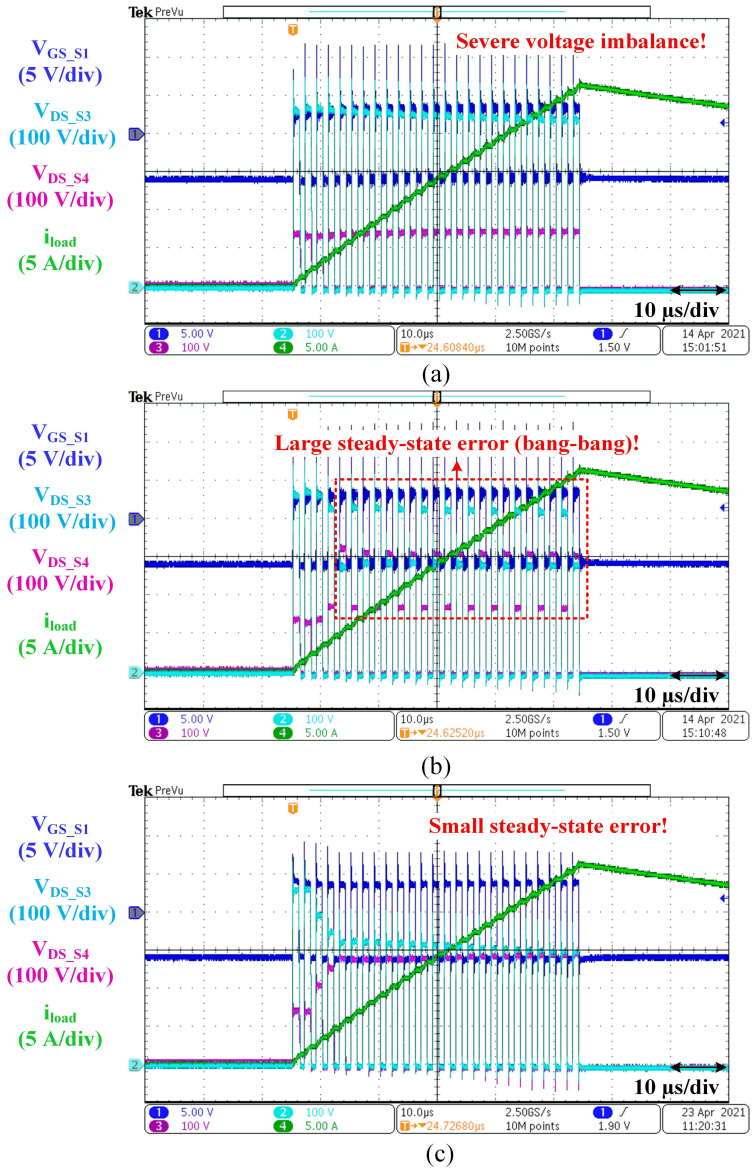


Figure 4.25: Multiple Pulse Test for Lower Arm Switches 'Hard' Turn-off Scenario at 600 V_{dc}. (a) Open-loop. (b) Only with T_{com} Closed-loop Control. (c) With Both T_{com} and i_{com} Closed-loop Control.

is observed. The top-sitting switch (S_3) has higher drain-to-source voltage than the bottom-sitting switch (S_4) does, which is consistent with the previous theoretical analysis.

Second, the captured waveform for the closed-loop (only with T_{com} control) case is shown in Fig. 4.25(b). The adaptive tuning of the compensation gate current pulse

width (T_{com}) is implemented, and the unit time step (ΔT) is selected to be 5 ns. The change of the gate charge is too large for each unit step, so the severe voltage imbalance occurs again after the fifth pulse, and the 'bang-bang' phenomenon is observed for the voltage sharing between the two switches, as shown in Fig. 4.25(b). The steady-state error can be suppressed by using a smaller compensation gate current. However, if the same amplitude is applied for all the pulses, it will take many pulses to reach the desired well-balanced voltage sharing (slow transient).

Last but not least, the captured waveform for the closed-loop (with both T_{com} and i_{com} control) case is shown in Fig. 4.25(c). The adaptive tuning of the compensation gate current pulse width (T_{com}) and amplitude (i_{com}) are both implemented. Since the dv/dt is not determined by the load current in the 'hard' turn-off scenario, the desired Q_{com} will not change rapidly with the load current. The control cycle of i_{com} is set to be six times the switching cycle in the 'hard' turn-off scenario. As is shown in Fig. 4.25(c), the well-balanced voltage sharing is achieved for the entire load range (except for the first few pulses), which validates the proposed closed-loop control strategy in the 'hard' turn-off scenario.

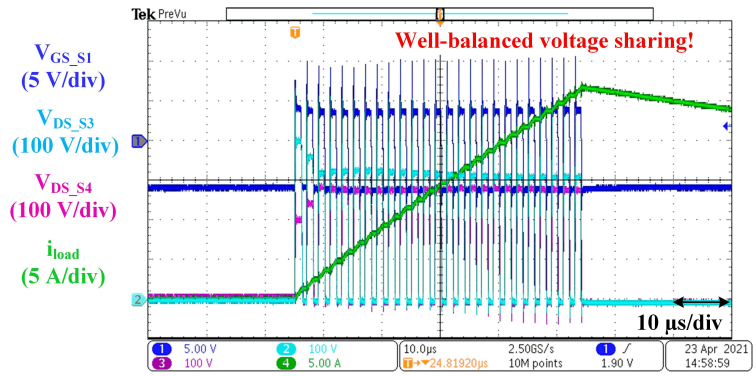


Figure 4.26: Multiple Pulse Test for Lower Arm Switches 'Hard' Turn-off Scenario with the Proposed Closed-loop Control Strategy (550 mA Turn-on Gate Current for the Complementary Switches).

It should be mentioned that the switching speed (dv/dt) is determined by the

turn-on gate current amplitude rather than the load current amplitude for the hard-switching scenario. To verify the proposed voltage balancing scheme in different switching speed (dv/dt) situations, the turn-on gate current of the complementary switches is increased from 400 mA to 550 mA. The experimental results of the multiple pulse test for this situation are shown in Fig. 4.26, which shows the satisfying voltage balancing performance as well. Therefore, it can be concluded the proposed voltage balancing scheme is valid for different load conditions and different switching speed conditions in the 'hard' turn-off scenario.

Moreover, the multiple pulse test is conducted for the 'hard' turn-off scenario under 800 V dc-link as well.

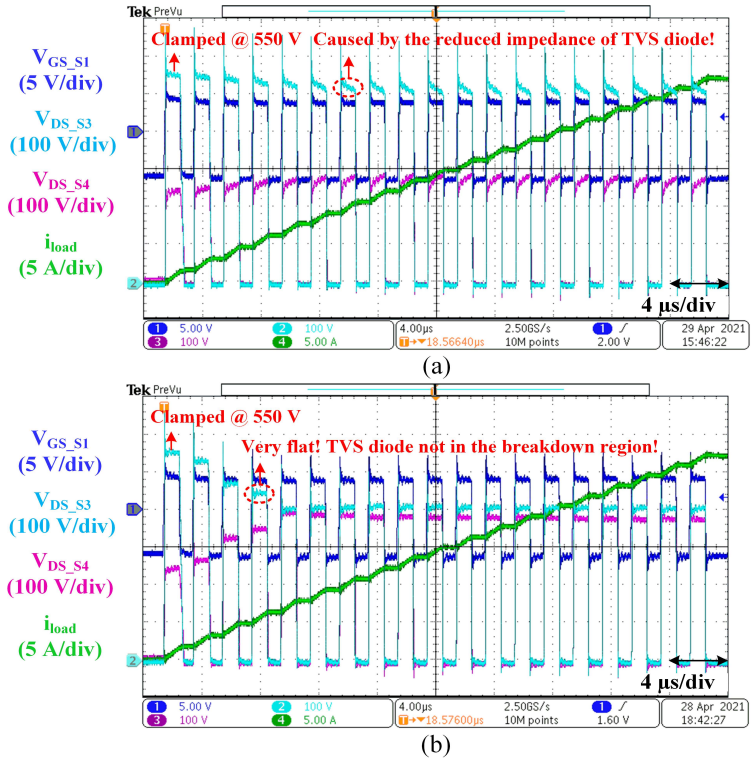


Figure 4.27: Multiple Pulse Test for Lower Arm Switches 'Hard' Turn-off Scenario at 800 V_{dc}. (a) Open-loop. (b) With Both T_{com} and i_{com} Closed-loop Control.

The experimental results for the 'hard' turn-off scenario without and with the proposed closed-loop control are shown in Fig. 4.27. Similar to the 'soft' turn-off

scenario, without the closed-loop control, the TVS diode is in the breakdown region for every pulse to dissipate the 'over-voltage' energy, as shown in Fig. 4.27(a). After the closed-loop control is implemented, the TVS diode will leave the breakdown region from the second pulse, as shown in Fig. 4.27(b). Therefore, the loss generated in the TVS diode is insignificant.

To sum, the proposed closed-loop control strategy works well for both 'soft' turn-off and 'hard' turn-off scenarios in 800 V dc-link conditions. Meanwhile, the TVS diode is only used to clamp the voltage for the first pulse, so the generated loss in the TVS diode is highly insignificant. The size and power rating of the TVS diode can be minimal as well.

4.5 Conclusion

In this study, a novel closed-loop current source gate driver is proposed for addressing the voltage imbalance issue in the series-connected GaN HEMTs. The low-loss, low-cost, and fast-responded current mirror circuits are utilized to drive the GaN devices, which can actively counteract the voltage imbalance brought by the device-to-ground displacement currents. Meanwhile, the digital adaptive voltage balancing scheme is proposed and verified in both soft-switching and hard-switching scenarios. The multilevel current source gate driver provides different tuning resolutions, which improves the adaptivity to various operating conditions. Moreover, without employing the snubber circuit and the extra Miller capacitor, the high-switching-speed and low-switching-energy benefits of using GaN devices are well reserved. A series-connected GaN-based multiple pulse tester is built to validate the proposed closed-loop current source gate driver and the adaptive voltage balancing scheme. The experimental results coincide with the theoretical analysis pretty well for both soft-switching and hard-switching scenarios. With the implementation of the pro-

posed approach, the over-voltage for the switch in the stack is cut down below 10% compared with the ideal average voltage under different load and different switching speed (dv/dt) conditions.

Chapter 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

The power converters in EV applications pursue higher power ratings and lighter weight, so the progress of high power density converters is essential for future EVs development. This study investigates some of the emerging technologies which are critical for improving the power density of the power electronics converters used in EV applications.

First, to improve the power density of the magnetic components, the low-profile PCB-based magnetics are explored thoroughly. A novel core and winding structure of a planar transformer is proposed to address the challenges of high intra-winding capacitance, high inter-winding capacitance and thermal management. Meanwhile, a generalized design and optimization methodology is proposed for the planar transformer. A high-power-density 6.6 kW/500 kHz CLLC resonant converter prototype with the proposed transformer structure is built and verified. The prototype demonstrates the outstanding 97.85% peak efficiency and the 114 W/inch^3 power density.

Second, to improve the efficiency of the synchronous rectifiers (SR) and reduce the size of the heat sinks, the high-dv/dt-immune, parameter-adaptive SR driving scheme is proposed. The proposed SR driving scheme addresses the issues of over-voltage and oscillation for the controller side brought by the high voltage and high dv/dt. Meanwhile, the adaptive SR on-time tuning algorithm is utilized to eliminate the effect of the package parasitic inductance for the SRs. A 3.3 kW/500 kHz CLLC modular-designed resonant converter prototype which employs the proposed SR driving scheme

is built and verified in the lab. The prototype exhibits an outstanding power density of 130 W/inch^3 and a very high peak efficiency of 97.6%.

Last but not least, to reduce the loss of the power semiconductors and improve the operating frequency of the power converters, WBG devices should be employed. The size of the passive components can be cut down due to the increased operating frequency, and the size of the heat sinks can be reduced as well, thanks to the diminished power loss. The series-connected GaN solution is attractive due to its low-loss and fast-switching characteristics, which is promising for the future 800 V or higher dc-link EV systems. To address the dynamic voltage balancing issues of the series-connected GaN HEMTs, a novel active current source gate driver is proposed. The fast-responded and flexible current source gate driver is able to counteract the device-to-ground displacement currents and achieve fairly balanced voltage sharing among the switches in the stack without compromising the switching energy or the switching speed of the main switches. A series-connected GaN-based multiple pulse tester is built to validate the proposed current source gate driver and the voltage balancing strategies. By employing the proposed voltage balancing strategy, the series-connected GaN HEMTs exhibit less than 10% voltage difference under different load and different switching speed conditions.

5.2 Future Work

Although the investigation in the study shows promising results, there are a lot of remaining tasks to be explored in the future.

First, for the PCB-based transformers, the reduction of the inter-winding capacitance by the proposed strategy is validated. However, the quantitative analysis about the impact on the EMI filter size is lacking. Normally, the EMI filter is a large contributor to the converter's overall size. Therefore, the system power density can be

further improved if all the magnetic components are optimized at a system level.

Second, the proposed SR gate driving scheme can be used for the SiC-based SR in higher voltage level applications, such as medium voltage solid state transformers (SST). Meanwhile, the proposed bi-directional drain-to-source voltage sensing circuit can be utilized for measuring the GaN device dynamic R_{dson} or monitoring the device current.

Finally, the thermal balancing issues among the series-connected switches should be further investigated for the soft-switching power converters by using the active current source gate driver. Meanwhile, since the current source gate driver can provide the desired multilevel gate current profile, it is beneficial in the 'smart' gate driving for the single device. The multilevel gate current can be applied for different intervals (di/dt interval, dv/dt interval) during the switching transient, which can have a better trade-off between the device turn-off voltage overshoot and the switching energy. The multilevel voltage source gate driver has achieved this function in the past, and it can be achieved by the proposed multilevel current source gate driver.

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