Wide Bandgap Semiconductor Power Devices using Ga_2O_3 GaN and BN

by

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ABSTRACT

Wide bandgap semiconductors, also known as WBG semiconductors are materials which have larger bandgaps than conventional semiconductors such as Si or GaAs. They permit devices to operate at much higher voltages, frequencies and temperatures. They are the key material used to make LEDs, lasers, radio frequency applications, military applications, and power electronics. Their intrinsic qualities make them promising for next-generation devices for general semiconductor use. Their ability to handle higher power density is particularly attractive for attempts to sustain Moore's law, as conventional technologies appear to be reaching a bottleneck.

Apart from WBG materials, ultra-wide bandgap (UWBG) materials, such as Ga_2O_3, AlN, diamond, or BN, are also attractive since they have even more extreme properties. Although this field is relatively new, which still remains a lot of effort to study and investigate, people can still expect that these materials could be the main characters for more advanced applications in the near future.

In the dissertation, three topics with power devices made by WBG or UWBG semiconductors were introduced. In chapter 1, a generally background knowledge introduction is given. This helps the reader to learn current research focuses. In chapter 2, a comprehensive study of temperature-dependent characteristics of Ga_2O_3 SBDs with highly-doped substrate is demonstrated. A modified thermionic emission model over an inhomogeneous barrier with a voltage-dependent barrier height is investigated. Besides, the mechanism of surface leakage current is also discussed. These results are beneficial for future developments of low-loss β-Ga_2O_3 electronics and optoelectronics. In chapter 3,

vertical GaN Schottky barrier diodes (SBDs) with floating metal rings (FMRs) as edge termination structures on bulk GaN substrates was introduced. This work represents a useful reference for the FMR termination design for GaN power devices. In chapter 4, AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors (MISHEMTs) fabricated on Si substrates with a 10 nm boron nitride (BN) layer as gate dielectric was demonstrated. The material characterization was investigated by X-ray photoelectric spectroscopy (XPS) and UV photoelectron spectroscopy (UPS). And the gate leakage current mechanisms were also investigated by temperature-dependent current-voltage measurements.

Although still in its infancy, past and projected future progress of electronic designs will ultimately achieve this very goal that WBG and UWBG semiconductors will be indispensable for today and future's science, technologies and society.

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CHAPTER 1

INTRODUCTION

1.1 Wide Bandgap Semiconductors

Nowadays, people's daily life is encountered by a lot of electronic products, such as smart phones, computers, and home automation systems. The heart of these electronic products is the chips, and the soul of the chips are semiconductors. Over the past decades, the development of semiconductor has a dramatic improvement. However, the demand for more-efficient electronics centers on power devices, and semiconductor materials are at the vanguard of scientists focus. Silicon's low cost and wide availability enabled it to be the dominant power semiconductor material. Today, silicon is facing its bottleneck in power devices. Two higher-efficiency alternatives: silicon carbide (SiC) and gallium nitride (GaN) are now arising.

These highly promising materials are the members of wide-bandgap (WBG) semiconductor family. WBG's extraordinary physical and electrical properties make them natural candidates for meeting the performance demands of high-frequency power applications, including power and extreme-temperature requirements for faster, high-efficiency, low-loss switching in compact form factors. The expected global market size for WBGSs is estimated to be 3.7 billion USD in 2025 with a compound annual growth rate of about 30% over a 10 year period [1]. The physical and electrical properties of wide-bandgap materials determine the functional and application characteristics of the power semiconductors built with them.

From a physical aspect, solid-state materials have electrons that either are tied to the nucleus (valance band) or are free to move at a higher energy level (conduction band). The energy gap between the valence and conduction bands is a significant parameter for defining and classifying a wide-bandgap semiconductor. A wider bandgap leads to a higher breakdown electric field, higher-operating–temperature capability, and lower susceptibility to radiation.

Conventional semiconductors including silicon and gallium arsenide, has a bandgap of 1.12 eV and 1.4 eV, respectively. As to WBGSs, the bandgaps of gallium nitride and silicon carbide are about 3.4 eV and 2.86eV, respectively [2]. As the operating temperature rises, the thermal energy of the electrons in the valence band increases accordingly and passes into the conduction band. The threshold temperature required for the transition from the valence band to the conduction band of silicon is less than 200°C. This indicates at such temperature, most silicon based electronic devices will be malfunctional. However, due to their high energy bandgap, WBG semiconductors can reach much higher temperatures without the need for electrons to accumulate energy. Thus, the greater the bandgap, the higher the sustainable semiconductor operating temperature [3].

Besides, the higher electron mobility of GaN compared with silicon enables devices to operate at higher switching speeds. This indicates a lower power consumption. The reduction in energy dissipated as heat not only cuts power losses but also enables a smaller system size, which reducing the total costs compared with silicon devices. As a result, WBG semiconductors are much more efficient than silicon. In addition, the superior power

density of WBGSs allows the use of more-compact heat sinks and higher operating temperatures along with higher-frequency switching.

The increase in switching frequencies also reduces inductance and reduce the size of the requisite capacitors. A high switching frequency results in smaller component sizes and a significant reduction in noise and vibration.

Many industrial companies have already developed WBG materials in new power designs for electric vehicles, optoelectronics, and other applications that present harsh operating conditions. WBG devices also provide lower on-resistance, higher breakdown voltage, and higher short- and long-term reliability. The breakdown electric field of WBG semiconductors allows lower leakage current and higher operating voltages.

As silicon hits its application bottlenecks both in power and frequency, GaN and SiC technologies are positioned for dominance in power electronics applications, where their promising characteristics perfectly suit the requirements for compactness, light weight, high efficiency, and high-density power. However, technological challenges still persist, especially in the demands of cost reduction and total heat dissipation, which in the case of semiconductors stems from conduction and switching losses. Engineers and scientists must deal with some defects in the carbide portion of SiC and overcome more-critical issues in the manufacturing processes for gallium nitride.

Apart from WBG materials, there are a group of interesting materials that have even larger bandgaps, which is so-called ultra-wide bandgap semiconductors (UWBGSs) [4]. Common members including gallium oxide, aluminum nitride, boron nitride or diamond. Due to their even larger bandgap, they have a great potential to overwhelm the performance

of WBG semiconductors and silicon in high power and high temperature applications. Although there are plenty critical issues need to be solved first, these materials still attract a lot of attention from researchers. It is believed that in the near future, these WBG or UWBG semiconductors have a high chance to dominate several electronic application areas.

In chapter 2, a Ga_2O_3 device is introduced and investigated. In chapter 3, a vertical GaN device with advanced edge termination method is demonstrated. In chapter 4, a AlGaN/GaN based device with novel BN design is presented. The discussion in these chapters provide readers some ideas of nowadays WBG and UWBG electronic device focus and development.

1.2 The development of GaN devices

GaN is now a rising star in the power electronic industry. It has the capability to reduce the losses in power conversion circuits, which has a potential to drive a 10 percent reduction in global power consumption. Initially, the development of GaN power devices focused on a lateral geometry on a foreign substrate due to the limitation of epitaxial technique. Typically GaN were grown on Si ,SiC or sapphire substrate. This usually leads to a high dislocation density that formed during the nucleation process. The dislocation densities of these heteroepitaxial grown GaN can vary from 10^9 cm^{-2} (on sapphire substrate with 16% lattice mismatch) to 10^7 cm^{-2} (on sapphire substrate with 3.5% lattice mismatch). In addition, lateral heteroepitaxial GaN devices also limited by a mismatched coefficient of thermal expansion (CTE) which compromises both reliability and performance.

Moreover, for most lateral GaN devices such as high electron mobility transistor (HEMT), the device channel is close to the surface (in the order of a few hundred nanometers) which introduces passivation, surface defect, and cooling problems. In a lateral GaN device, the distance between drain, gate, and source determines the breakdown voltage of the device. A larger terminal distance leads to a higher breakdown performance. However, it increases the device area and channel resistance, which limits the production efficiency and the current capability.

Recently, thanks to the advanced material growth techniques, free standing bulk GaN substrates have been commercialized. The material quality of homoepitaxial GaN on the free standing GaN substrate has an obvious improvement and shows the potential for power applications. This launches a new era of vertical GaN-on-GaN devices. The

dislocation density of homoepitaxial GaN-on-GaN device can be surpassed to lower than 10^6 cm^{-2}. The advantage of vertical device compared to lateral devices includes capability of high breakdown voltage and low leakage current, reduced chip size, stable reliability, uniform electric field distribution, thermal management.

There are still some critical issues that facing vertical GaN power devices. The absence of avalanche breakdown, the realization of normally off operation, a higher rate of acceptor activation, the regrowth interface performance, and a better design for edge termination. All these topics still require further effort to be studied.

1.3 Edge termination Methods for vertical GaN devices

For vertical GaN power devices, breakdown voltage is an important parameter. Almost all investigations on vertical GaN devices are focused on improving the breakdown voltage and reducing the reverse leakage current. However, due to the electric field crowding at the edge of the junction, the depletion layer edge, or the electrode edge, premature breakdown often occurs. Therefore, to reduce the electric feld crowding of the device, several different advanced device structure designs, so-called “edge termination techniques” are developed. Varied edge termination techniques have now been applied to relax the electric feld crowding at the edge of GaN devices for a higher BV. These techniques include the field plate (FP), plasma treatment, deep mesa etching in varied angles or steps, and guard rings (GRs) [5].

The field plate is the earliest and the most widely used edge termination method in GaN-based devices for transferring the peak electric field far from the edge of the gate, anode, or junction. The merits of the field plate include a simple and compatible fabrication process, and a simultaneously deposited passivation layer for the GaN devices. However, there are still some drawbacks of this approach. The main issue is the defect during the dielectric layer deposition and interface between the dielectric and GaN, which result in carrier trapping. This reduces the stability of the device performance during long-term use. Therefore, the optimization of the deposition process of the dielectric layer must be investigated. Figure 1.1 demonstrates the GaN PN diodes with (a) a field plate with an extended passivation dielectric layer and (b) extended field plate metal contact and a passivation dielectric layer [5].

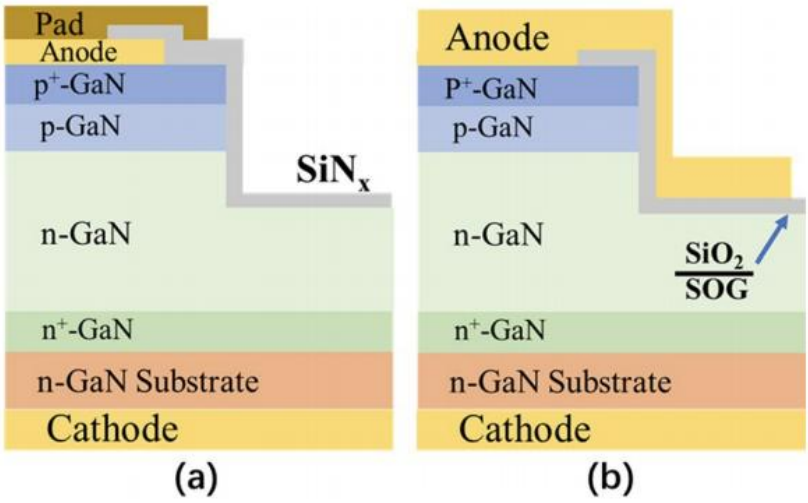

Fig 1.1 GaN PN diodes with (a) a field plate with an extended passivation dielectric layer and (b) extended field plate metal contact and a passivation dielectric layer. [5]

Mesa etching is an important step to isolate each device in the fabrication of lateral GaN-based devices. It is even more critical on vertical GaN devices since the design of mesa directly impact their breakdown performance. The ultimate target is to uniformly distribute the electric field of the power device, this approach can avoid the premature breakdown as late as possible. As shown in figure 1.2 (a) a deep mesa etching structure and (b) a two-step mesa structure was applied on the GaN devices. Figure 1.3 demonstrates the simulation results of the GaN PN diodes with various mesa etching depth [5]. When the mesa depth is not very deep, under high voltage, the peak electric field occurred at the edge of the device. When the mesa depth was increased to 10 μm, a uniform electric field distribution is presented [6].

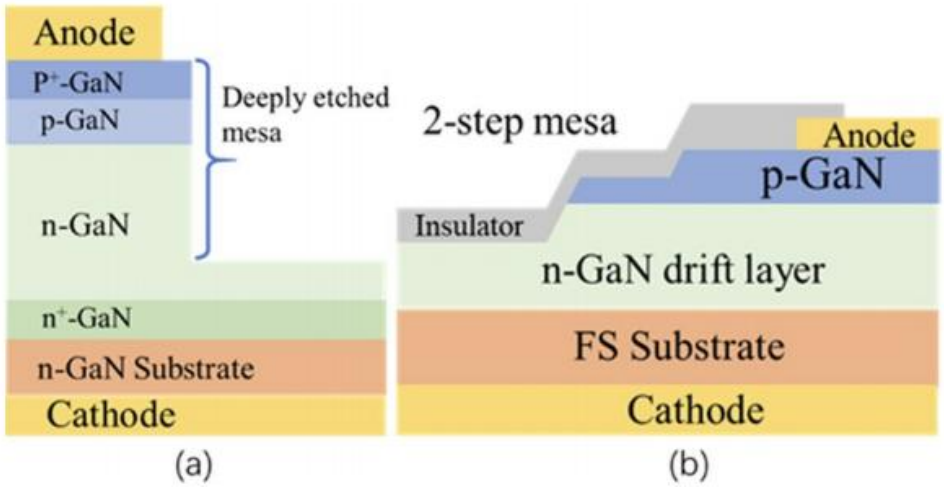

Fig 1.2 GaN PN diodes with (a) deeply etched mesa structure (b) two-step mesa structure. [5]

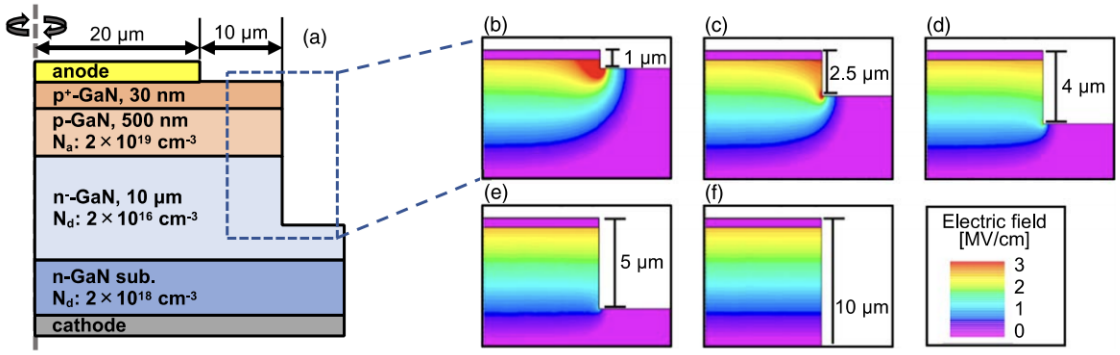

Fig 1.3 (a) Schematic cross section of the vertical GaN p–n diode used for simulation. (b) Simulated electric field distributions of the p–n diodes when a reverse bias of −800 V was applied for mesa depths of 1 μm, (c) 2.5 μm, (d) 4 μm, (e) 5 μm, and (f) 10 μm. [5,6]

The hydrogen-plasma (H-plasma) is another novel edge termination method [5]. It can reduce the conductivity of p-GaN. H-plasma treatment is an efective passivation

method to transform the conductive p-GaN into a highly resistive one because of the strong bond of Mg-H. The hydrogen-plasma treatment is appropriate for use in vertical GaN PNDs because of the low damage, low temperature, and simple operation involved. Figure 1.4 demonstrates the hydrogen plasma treatment on GaN PN diodes [5, 7, 8].

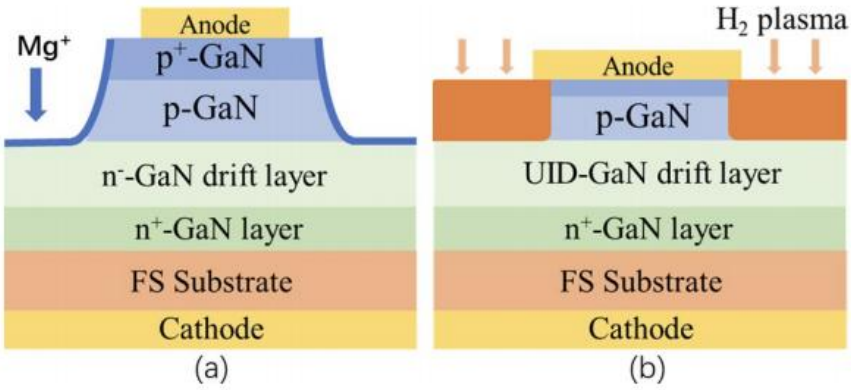

Fig 1.4. (a) A Schematic view of GaN PN diodes structure by Mg ion treatment (b) hydrogen plasma treatment. [5]

Apart from the above edge termination methods, the floating metal guard ring (FMR) is another effective approach. Further detail will be discussed in chapter 3.

CHAPTER 2

TEMPERATURE DEPENDENT ANALYSIS OF GALLIUMOXIDE SCHOTTKY BARRIER DIODES

2.1 Introduction and Motivation

III-oxide compound semiconductors hold great potential to pioneer new semiconductor-based technologies. This material system, including gallium oxide (Ga_2O_3) and aluminum oxide (Al_2O_3), has a bandgap ranging 4-8 eV. which is much larger than that of conventional semiconductors such as silicon (1.12 eV) and gallium arsenide (1.42 eV) and even wide bandgap (WBG) semiconductors such as GaN (3.4 eV) and 4H-SiC (3.25 eV). Among these III-oxide semiconductors, gallium oxide is one of the promising candidates that can push semiconductor industry into the next generation. Table 2.1 demonstrates the figure of merits table of several different semiconductor materials.

Table 2.1 Figure of merits of several semiconductors

	Conventional		WBG		UWBG	
	Si	GaAs	4H-SiC	GaN	AlN	B-Ga_2O_3
E_g (eV)	1.1	1.4	3.3	3.4	6.3	4.8
λ (W/mK)	150	50	490	130	290	13
E_c (MV/cm)	0.3	0.4	3	3.3	**12**	**8**
V_{sat} (10^7 cm/s)	1	1.2	2	2.5	1.4	1.1
μ ($cm^2/V{\cdot}s$)	1400	8000	1000	1200	300	300
ε_r	11.8	12.9	9.7	9	9	10
BFOM ($\mu\varepsilon_r E_c^3$)	1	14.8	587	870	10461	3444
JFOM ($V_{sat}E_c$)	1	1.6	20	28	56	29

Gallium oxide can form several different polymorphs, designated as α-, β-, γ-, δ-, ε-[9]. The β-form is the most common and the well-studied polymorph of gallium oxide[10]. β-Ga_2O_3 is the only stable polymorph through the whole temperature range till the melting point, whilst all other poly- morphs are metastable and transform into the β-Ga_2O_3 at temperatures above 750-900[11]. Figure 2.1 shows some different polymorphs of gallium oxide. Beta-phase Ga_2O_3 (β-Ga_2O_3) has garnered considerable attention for various optoelectronic and electronic applications[12, 13], due to its large bandgap (~ 4.8 eV) and high breakdown electric field E_{br} (~8 MV/cm)[14-16]. The large bandgap of β-phase Ga_2O_3 allows it to withstand a stronger electric field, which makes it possible to use a thinner device for a given voltage rating. This is important because the thinner the device, the lower its on-resistance, thus making it much more energy-efficient. As a result, β-Ga_2O_3 based devices are promising candidates for efficient power conversion[17, 18] application in smart grids, renewable energy, big data center power supplies, and automotive electronics.

Another advantage of β-Ga_2O_3 is the availability of cost-effective single-crystal substrates[15, 19, 20]. The edge-defined film-fed growth (EFG) method, described by Labelle and Mlavsky, is an advantageous technique for growing crystals of various materials in various shapes. The EFG method has been applied to the growth of oxides such as Al_2O_3, $LiNbO_3$, and TiO_2. It is one of the main methods to grow large-sized β-Ga_2O_3 substrates, as its relatively low cost and scalability make it aptly suited for use in mass production. Nowadays, commercialized high quality 2-inch β-Ga_2O_3 substrates grown by EFG with controllable doping concentrations ranging from $10^{16}cm^{-3}$ to $10^{19}cm^{-3}$ have also been demonstrated[19-21]. Electronic devices such as field effect transistors (FETs)[17, 18] and Schottky barrier diodes (SBDs)[15, 19, 20, 22], and optoelectronic

devices such as solar-blind photodetectors[23] fabricated on the β-Ga_2O_3 substrates have also been reported. Figure 2.2 shows (a) schematic drawing of EFG process and (b) Photograph of EFG-grown β-Ga2O3 bulk crystal with different orientation.

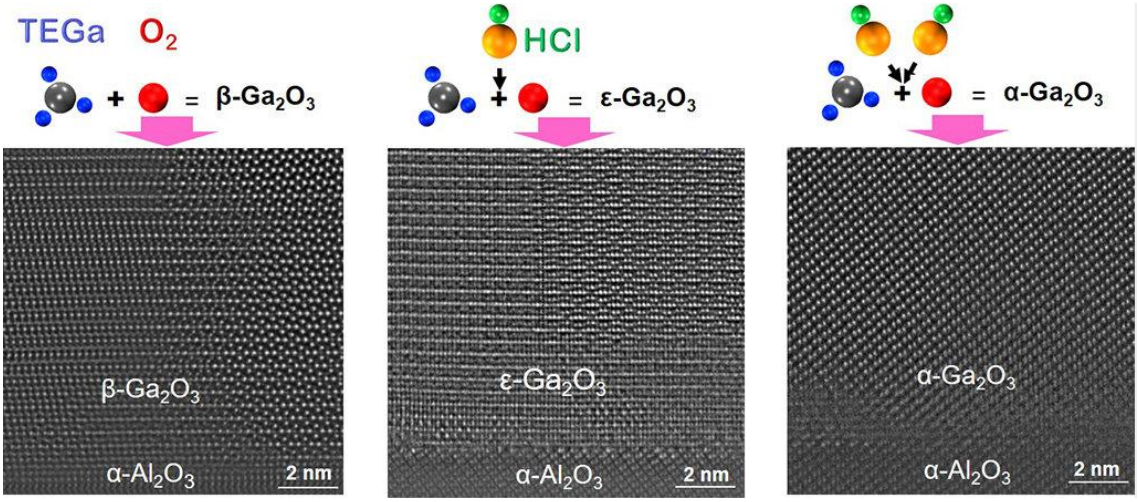

Fig 2.1. Different polymorphs of gallium oxide can be grown in a MOCVD chamber by controlling the flow of hydrogen chloride. Credit: American Chemical Society

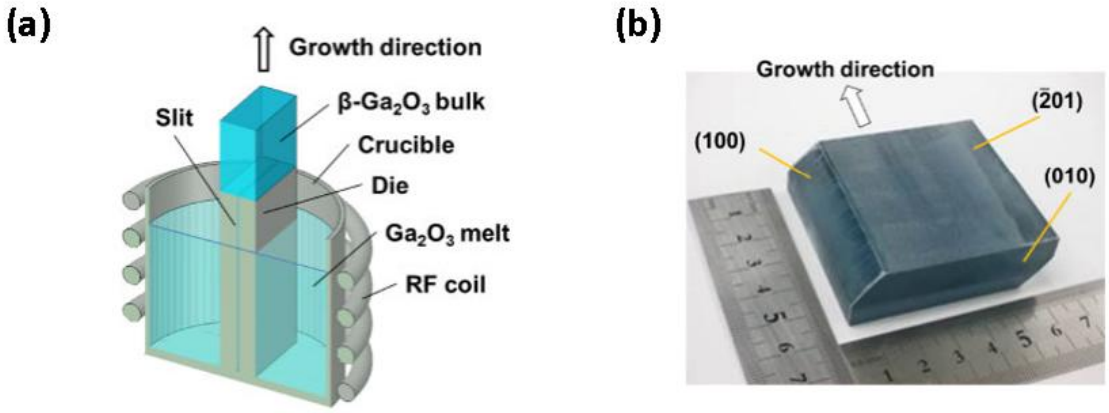

Fig 2.2. (a) Schematic drawing of EFG process and (b) Photograph of EFG-grown β-Ga2O3 bulk crystal with different orientation.

As shown in Fig. 2.3, β-Ga_2O_3 devices are capable of dramatically enhancing the efficiency of power electronics system by reducing the on-resistance. To access this low on-resistance region, high doping concentrations of β-Ga_2O_3 are needed. Currently, the majority of the β-Ga_2O_3 devices have a doping concentration below mid 10^{17} cm^{-3} range and the on-resistance is significantly higher than the theoretical limit[14, 15], resulting in large power losses. However, there are very few reports about SBDs on highly doped single-crystal β-Ga_2O_3 substrates with doping concentrations above 10^{18} cm^{-3}. Additionally, the mechanism of temperature-dependent performance of these SBDs are still not very clear. In this work, we comprehensively investigated the temperature-dependent electrical properties of $(\bar{2}01)$ β-Ga_2O_3 SBDs on highly doped (~3×10^{18} cm^{-3}) single-crystal substrates. In Section 2, we performed detailed material characterizations on the substrates and fabricated the devices. In Section 3, first, current density-voltage (J-V) and capacitance-voltage (C-V) characteristics were discussed in detail. Several important device parameters such as Schottky barrier height and ideality factor were extracted and temperature-dependent characteristics were also included. Then, the reverse leakage currents were fitted by trap-assisted tunneling model and the one-dimensional variable-range-hopping conduction (1D-VRH) model. Quantitative study of the leakage current as a function of distance was also carried out. These results represent one of first comprehensive investigations for β-Ga_2O_3 devices on highly doped substrates and is beneficial for future developments of low-loss β-Ga_2O_3 electronics and optoelectronics.

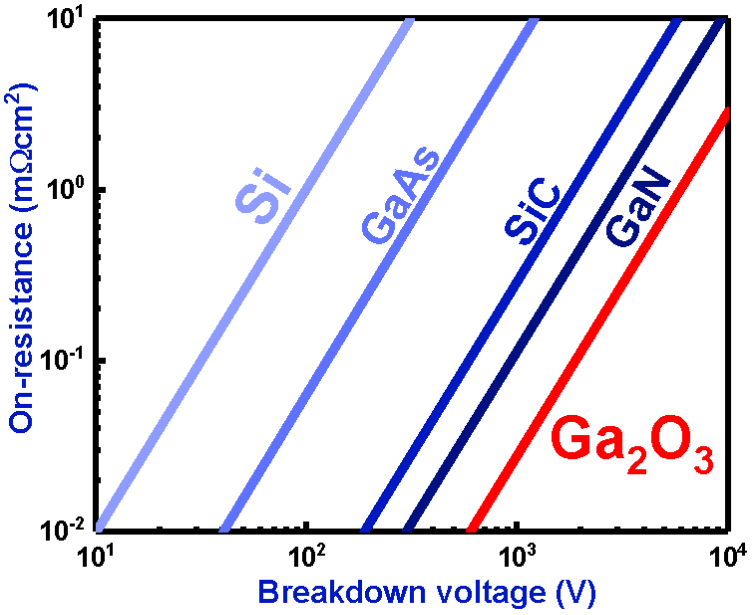

Fig 2.3. Theoretical benchmark plot of on-resistance versus breakdown voltage for power devices based on β-Ga_2O_3 and other major semiconductors.

2.2 Material Characterization

The β-Ga_2O_3 single crystal substrates were purchased from Tamura Corporation. These wafers were grown by the EFG method. Ga_2O_3 and tin oxide (SnO_2) powder were used as the source material and the precursor for n-type Sn dopants, respectively. More details about the growth process can be found elsewhere[20]. High-resolution X-ray diffraction (HRXRD) was used to characterize the crystal quality of the substrate. The setup was the PANalytical X'Pert Pro materials research X-ray diffractometer (MRD) system using Cu Kα1 radiation source with a wavelength of 1.541 Å. The incident beam optics and the diffracted beam optics were the hybrid monochromator and the triple axis module, respectively. The rocking curve (RC) for the $(\bar{2}01)$ β-Ga_2O_3 substrate is shown in Fig. 2.4(a). The full width at half maximum (FWHM) of the RC was ~ 44 arc sec. The dislocation density of the substrate was estimated to be on the order of ~ 10^6 cm^{-2} [24]. To further confirm the quality of the substrate, the surface roughness was examined by using Bruker's Multimode atomic force microscopy (AFM) as shown in Fig. 2.4(b). The root-mean-square (RMS) roughness of the scanning area of 3 μm ×3 μm is about 0.12 nm. The HRXRD and AFM results indicate that the β-Ga_2O_3 substrate has a low dislocation density and a good surface morphology.

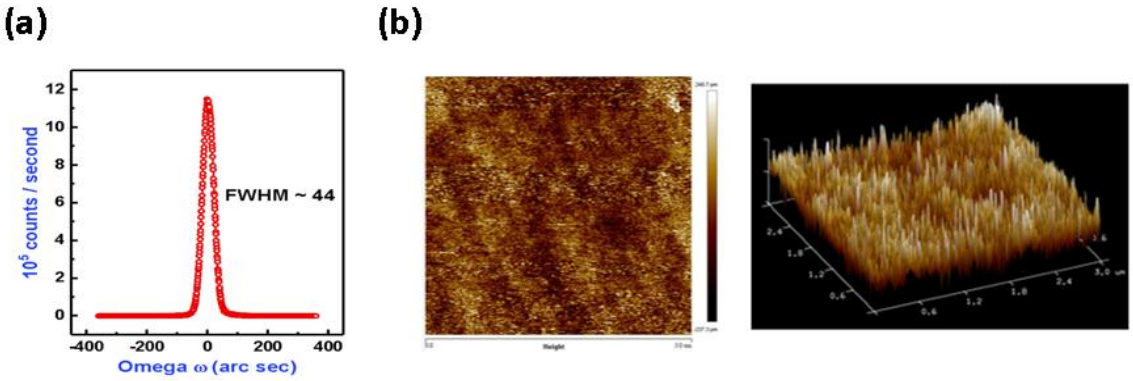

Fig 2.4. (a) The rocking curve of the β-Ga_2O_3 substrates measured by HRXRD. (b)The 2D and 3D AFM images of the surface morphology of the β-Ga_2O_3 substrates.

2.3 Device Fabrication

The SBDs were then fabricated on the β-Ga_2O_3 substrate using standard photolithography. Before the metal depositions, the sample was cleaned in acetone and isopropyl alcohol (IPA) under ultrasonic to remove possible organic contaminant on the surface. For the ohmic contacts of the SBDs, Ti/Al/Ti/Au metal stacks were deposited on the Ga_2O_3 substrate using electron beam evaporation and subsequently annealed at 470 °C for 1 minute in nitrogen ambient using rapid thermal annealing (RTA). For the Schottky contacts, Pt/Au metal stacks were deposited by electron beam evaporation. Lift-off lithography was applied to form the contacts. Figure 2.5 shows the schematic top view and cross-section view of the β-Ga_2O_3 SBDs. The diameters of the left ohmic contact and right Schottky contact are 400 μm and 200 μm, respectively. The distance between the ohmic and Schottky contacts varied from 50 μm to 500 μm. Keithley 2410 source meter and 4200-SCS parameter analyzer on a probe station with a controllable thermal chuck were used for the electrical measurement.

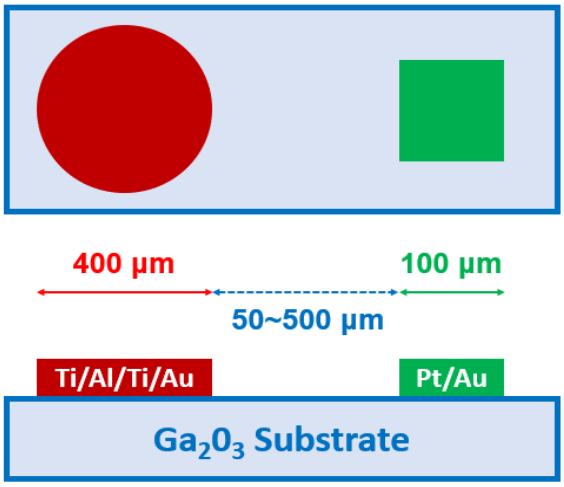

Fig 2.5. Top and cross-section view of the fabricated SBDs.

2.4 Temperature Dependent Forward J-V Characterization

Figure 2.6 shows the temperature-dependent forward I-V characteristics of the β-Ga_2O_3 SBDs from 300K to 480K (with a step of 20 degrees) in both linear scale and log scale. The upper current limit of the setup is 0.1 A. A high on/off ratio of ~10^9 was observed. To further discuss the electrical properties, on-resistance and turn-on voltage were then extracted. In Fig. 2.7(a), the on-resistance of the $(\bar{2}01)$ β-Ga_2O_3 SBD is about $0.9\text{m}\Omega \cdot \text{cm}^2$, which is lower than previous work[15, 21, 22, 25-31]. There are several factors that can influence the on-resistance such as ohmic contact, interface quality and crystalline quality[24]. In this work, the relatively low on-resistance can be attributed to the high doping concentration, which will be further discussed in the C-V measurements later. The turn-on voltage in Fig 2.7(b) gradually decreased from 0.84V to 0.64V with the temperature increasing from 300K to 480K. This is due to the generation of the high energy electrons and/or reduced bandgap at high temperature.

The current-voltage characteristics of the SBDs can be studied from the thermionic emission model[22]

$$J = A^{*}T^{2} \exp\left(-\frac{q\phi_{eff}}{kT}\right)\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (1)$$

$$J_s = A^{*}T^{2} \exp\left(-\frac{q\phi_{eff}}{kT}\right) \quad (2)$$

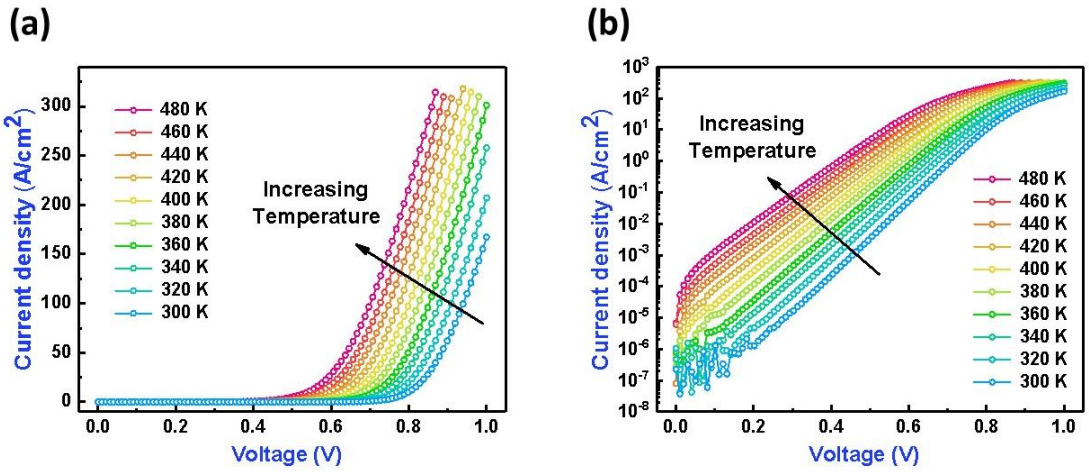

Fig 2.6. Temperature-dependent forward J-V characteristics of β-Ga_2O_3 SBDs in (a) linear scale and (b) log scale.

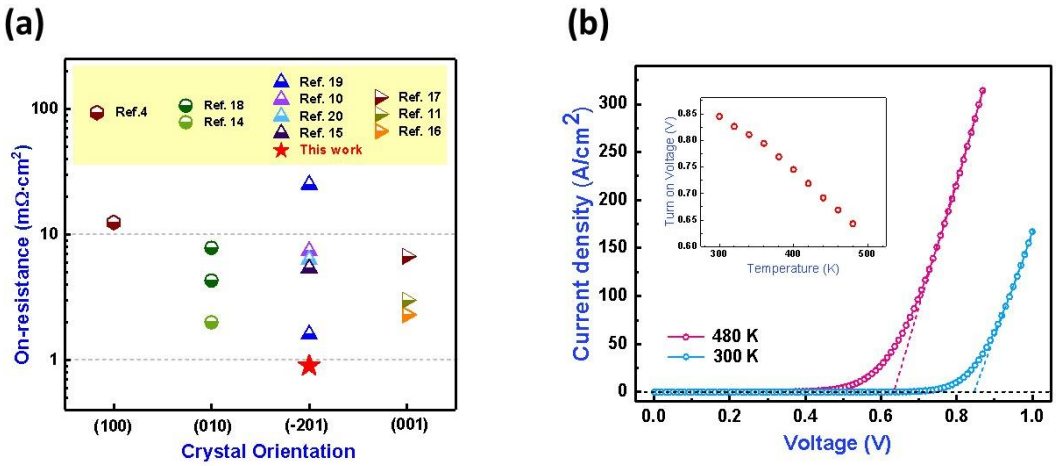

Fig 2.7. (a) Comparision of on-resistance of previously reported β-Ga_2O_3 SBDs on various crystal orientations. (b) The turn-on voltage were obtained by linear extrapolation of the linear I-V curves.

where J is the current density, A* is the Richardson constant (for β-Ga_2O_3, it is calculated to be 41.1 A/cm^{2}K^2 using an effective electron mass of 0.34 m_0 and the equation $A^* = 4\pi q k^2 m_n^*/h^3$)[29], T is temperature in kelvin, q is the electron charge, ϕ_{eff} is the

effective Schottky barrier height, k is the Boltzmann constant, n is the ideality factor, and J_s is the saturation current density. The ideality factor can be calculated as a function of temperature by applying the function[32]:

$$n = \frac{q}{kT}\frac{1}{\frac{d(\ln J)}{dV}} \tag{3}$$

Figure 2.8(a) shows the extracted ideality factor and the barrier height as a function of temperature. The values of n and J_s are extracted from measured J–V data in forward bias from 0.3 to 0.5 V. If the Schottky barrier is homogeneous and the thermionic emission model is valid, then the ϕ_{eff} should be temperature independent, ideality factor should be 1, and the y-intercept of $\ln(J_s/T^2)$ versus 1000/T graph should retrieve A*. However, the results obtained from Fig. 2.8 do not match this assumption. In Fig. 2.8(a), when the temperature is increased from 300K to 480K, the ideality factor decreased from 1.39 to 1.13, and the Schottky barrier height increased from 0.94 eV to 1.10 eV. The correlation between the ideality factor and Schottky barrier height can be further observed by a well know linear relationship[33], as shown in Fig. 2.8(b). Moreover, the blue dash line in Fig. 2.8(d) shows a fit to the Richardson plot of $\ln (J_s/T^2)$ versus 1000/T. The calculated A* value is about $3.28 \times 10^{-3} \mathrm{Acm^{-2}K^{-2}}$, which is unreasonably small compared with the theoretical value. All these non-ideal results can be explained by the thermionic emission over an inhomogeneous barrier with a voltage-dependent barrier height[34]. The spatial inhomogeneities is attributed to the defects between the metal/semiconductor interface, which may be caused by a rough interface between the Schottky electrode and the semiconductor, non-uniform metallurgy, and metal grain boundaries[35, 36]. To incorporate the barrier inhomogeneity into the thermionic emission model, it is assumed

that the Schottky barrier has a Gaussian distribution potential with a mean barrier height $\overline{\phi_b}$and a standard deviation σ, and the barrier is linearly dependent on voltage:

$$\phi_{eff} = \overline{\phi_b} - \frac{q\sigma^2}{2kT} \tag{4}$$

$$\overline{\phi_b} = \overline{\phi_{b0}} + \gamma V \tag{5}$$

$$\sigma^2 = {\sigma_0}^2 - \xi V \tag{6}$$

where ϕ_{b0} and σ_0 are the values at zero bias. The ideality factor thus becomes temperature-dependent and its value can exceed unity:

$$n^{-1} - 1 = -\gamma - \frac{q\xi}{2kT} \tag{7}$$

Figure 2.8(c) shows the linear relationship of both $n^{-1} - 1$ and ϕ_{eff} with respect to 1000/T. The coefficients γ and ξ represent the voltage-induced deformation of the Schottky barrier distribution. Note that $\gamma < 0$ and $\xi > 0$, meaning larger voltage can decrease the mean Schottky barrier height and reduce the inhomogeneity of the barrier distribution, respectively[34]. With the fitting data in Fig. 2.8(c), the extracted ϕ_{b0} is 1.34 eV and the extracted σ_0 is 0.14 eV. This potential fluctuation parameter is close to the values of some other reported SBDs with different materials, such as a-IGZO (0.13 eV)[35], ZnO (0.134 eV)[37], and a-ZTO (0.12 eV)[34] Schottky diodes.

Moreover, we can then combine the modified Schottky barrier equations (4) into the original thermionic emission equation (1) and obtain the following modified thermionic emission equation:

$$ln\left(J_s/T^2\right) - {q^2{\sigma_0}^2}/{2k^2T^2} = ln(A^*) - {q\overline{\phi_{b0}}}/{kT} \tag{8}$$

A modified Richardson plot using Eq. 8 is shown in the red line of Fig. 2.8(d). Form the fitting data (dash line), the modified Richardson constant A* is ~ 41.26 $Acm^{-2}K^{-2}$and $\overline{\phi_{b0}}$ is ~ 1.36 eV. These values are close to the theoretical A* value (41.1 $Acm^{-2}K^{-2}$) and the $\overline{\phi_{b0}}$ value extracted from the Fig. 2.8(c) (1.34 eV).

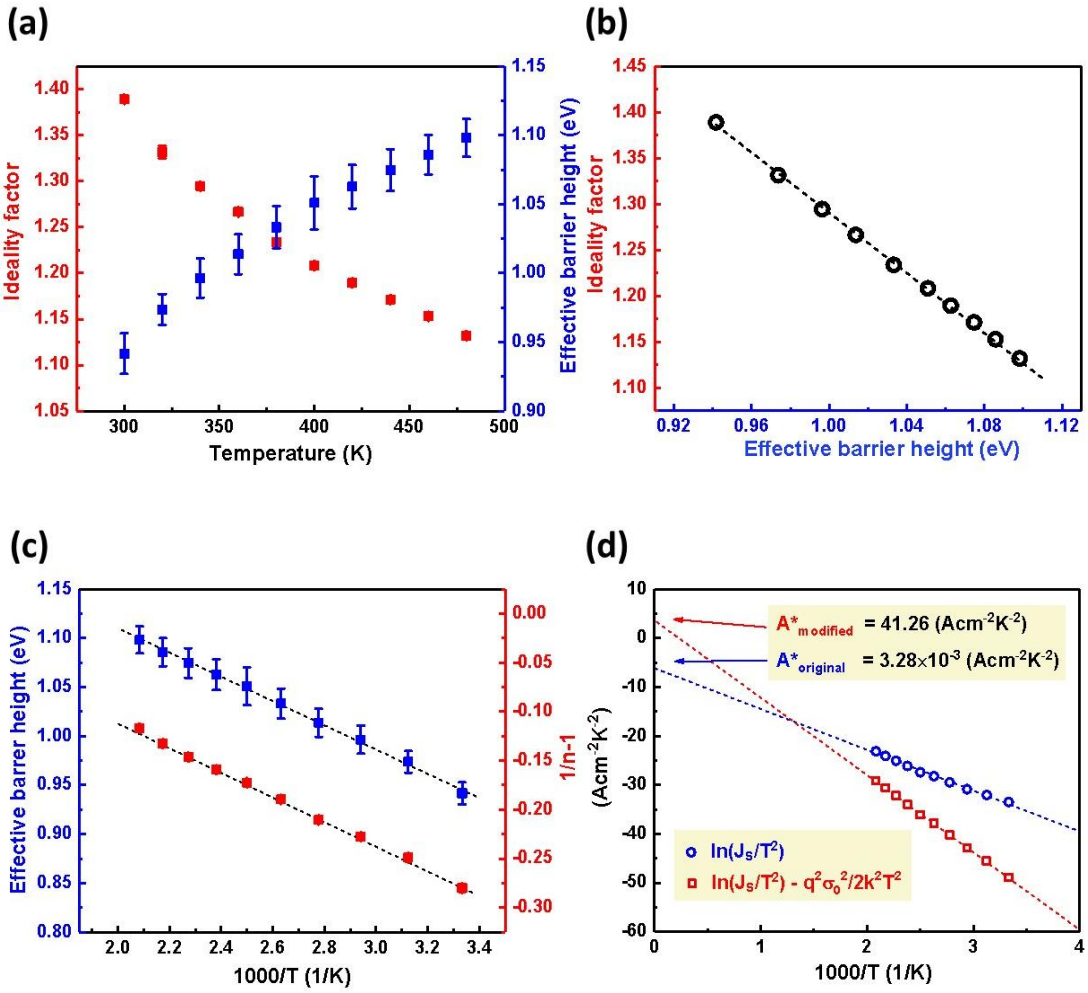

Fig 2.8.(a) Ideality factor and Schottky barrier height as a function of temperature from 300 K to 480K. (b) Ideality factor versus Schottky barrier height. (c) Plot of effective barrier height and n^{-1}-1 versus 1000/T with error bars. (d) Original and modified Richardson plot for β-Ga_2O_3 SBDs. The dash line shows the fitting curve.

2.5 Capacitance-Voltage Characterization

Figure 2.9(a) shows the C-V characteristics of the Ga_2O_3 SBDs at a frequency of 1MHz at room temperature. By plotting the $1/C^2$ vs. V in Fig. 2.9(b) and extracting the slope, the doping concentration can be calculated using the following equations[22, 38]:

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_0\varepsilon_r N_D}\left(V_{bi} - V - \frac{kT}{q}\right) \tag{9}$$

$$N_D = \frac{-2}{q\varepsilon_0\varepsilon_r\left[d\left(\frac{1}{C^2}\right)/dV\right]} \tag{10}$$

where ε_0 is vacuum permittivity, ε_r is the relative permittivity of β-Ga_2O_3, and V_{bi} is the built-in voltage. The doping concentration of the β-Ga_2O_3 substrate is about $2.9 - 3.5 \times 10^{18}$ cm^{-3}, which is a relatively high doping concentration. This result indicates that this sample is less resistive and explains the low on-resistance of the devices.

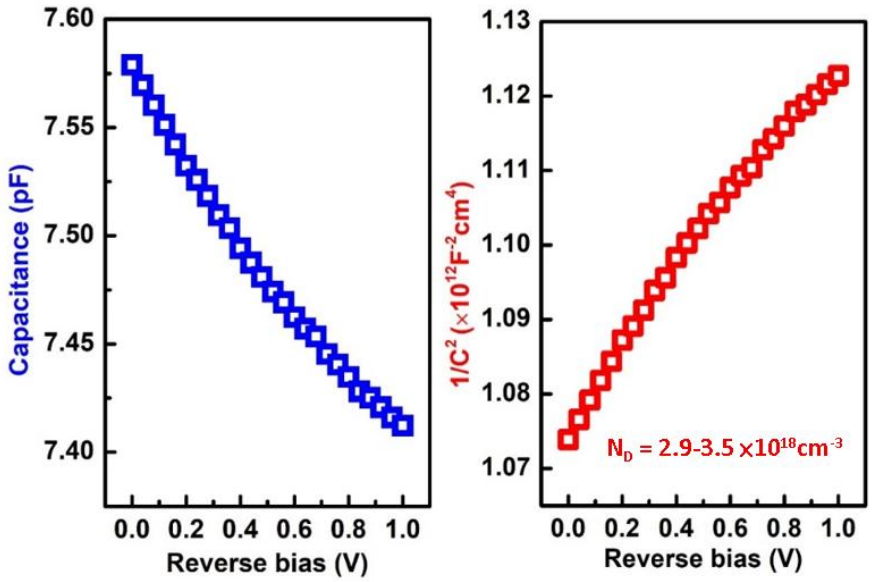

Fig 2.9. C-V characteristics for β-Ga_2O_3 SBDs at 1 MHz. The doping concentration of the devices was also extracted.

2.6 Temperature Dependent Reverse J-V Characterization

The temperature-dependent reverse J-V characteristics of the β-Ga_2O_3 SBDs is presented in Fig. 2.10. Please be noted that the breakdown voltages were relatively low due to the high doping concentration of the substrates. The reverse current increased with the temperature, increasing from 300K to 480K. Due to the ultra large bandgap of β-Ga_2O_3, the thermionic emission current over the barrier is considerably small compared to the measured current levels, hence it will be neglected in the following discussion[39]. To study the reverse leakage current mechanism, several current conduction models are proposed to characterize the reverse leakage current[39-43]. The first model is the two-step trap-assisted tunneling[39-41, 43]. In this model, an electron in the metal could be activated to a trap state at the metal-semiconductor interface and then tunnel to the semiconductor side. Figure 2.11(a) shows a typical Arrhenius plot of the current for this model at V_R = 7V and a schematic electron transport diagram in the inset. This phenomenon can be examined from the exponential temperature dependence of the reverse current. The reverse leakage current is proportional to an exponential term to the power of ($-E_A/kT$) where E_A is the activation energy. From the slope of this graph, the activation energy was extracted to be 30.5 meV. Assuming thermal activation is the rate-limiting step, the trap state would be at an energy ($q\phi_b - E_A$) below the conduction band edge of the semiconductor.

The second model is the one-dimensional variable-range-hopping conduction (1D-VRH) model[42]. The model describes a thermally activated current conduction from the metal into the semiconductor along the defect states associated with a threading dislocation near or below the Fermi level. In this model, the conductivity of the device is given by[39]

$$\sigma = \sigma_0 \exp\left[-\left(T_0/T\right)^{0.5}\right]$$

Where T_0 is a characteristic temperature. Figure 2.11(b) demonstrated the relationship of measured conductivity in log scale as a function of $T^{-0.5}$ from 300K to 480K. The good fitting between experiment data and fitting data suggests that both models play important roles in the reverse leakage mechanism. Further investigations are needed to decouple the two mechanisms and identify the primary mechanism.

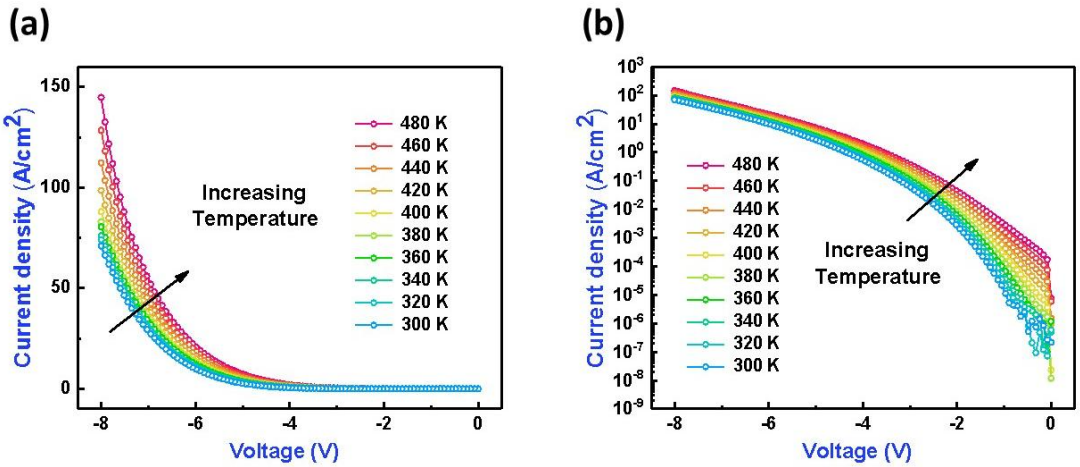

Fig 2.10. Temperature-dependent reverse J-V characteristics of the β-Ga_2O_3 SBDs in the (a) linear scale and (b) log scale.

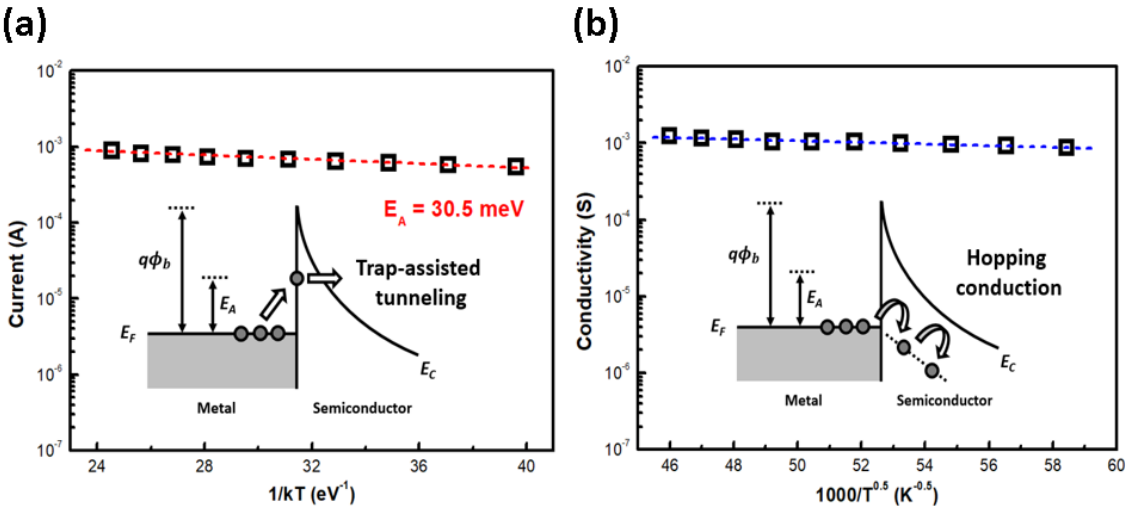

Fig. 2.11. (a) Arrhenius plot of reverse leakage currents of the β-Ga_2O_3 SBDs with the activation energy extracted. (b) Conductivity as a function of $1/T^{1/2}$ for the β-Ga_2O_3 SBDs. The inset shows the electron transport in the 1D-VRH conduction model.

2.7 Surface Leakage Current

Figure 2.12 shows the leakage current for β-Ga_2O_3 SBDs as a function of contact distance from 50 μm to 500 μm at voltages of −6V, −7V, and −8V. The reverse current decreased as the contact distance increased. This trend is opposite form the observation of some other material system such as AlN on sapphire[38, 44] and germanium on SOI[45]. The total leakage current is the sum of leakage currents through the bulk and the surface. For the cases of AlN and Ge on SOI, due to the poor material quality and the large amount of surfaces states, the leakage current is surface dominated via surface states. With shorter contact distance, there is less chance for the device to have a poor surface area between the contacts. As a result, the surface leakage current increases with the contact distance. In the case of β-Ga_2O_3 SBDs on single-crystal substrate, without the detrimental effects of poor material quality, the leakage current is dominated by the bulk. A larger contact distance results in a higher resistivity of the leakage path and a lower leakage current. With the linear fitting, the leakage currents per distance were extracted to be 0.065 mA/mm, 0.156 mA/mm, 0.361 mA/mm at −6V, −7V, and −8V, respectively. At higher reverse bias, the leakage current is increased due to a higher electric field between the contacts[46].

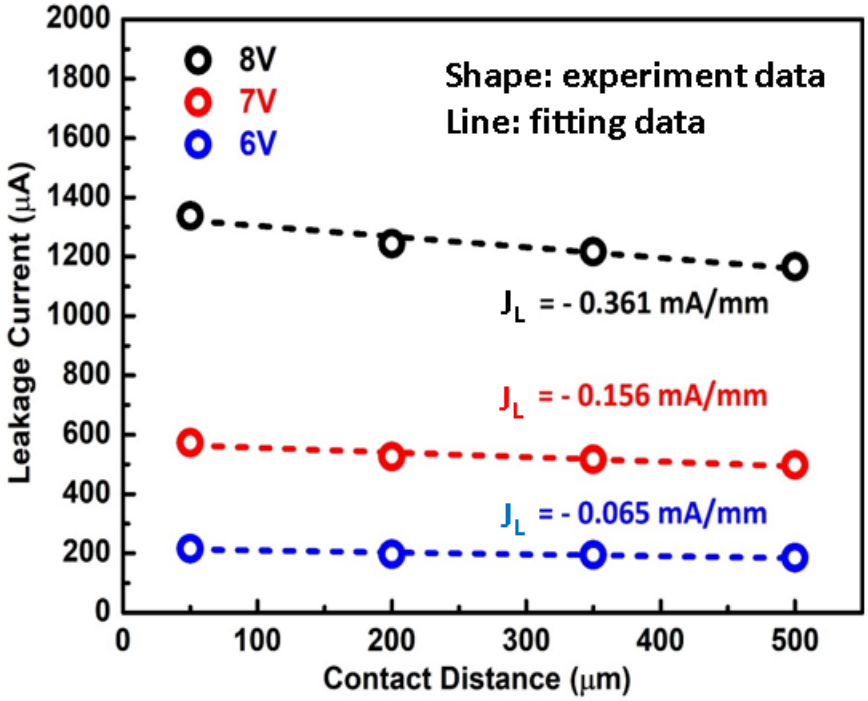

Fig. 2.12. Leakage current as a function of contact distance between ohmic and Schottky contacts at different reverse voltages.

2.8 Summary

Lateral SBDs fabricated on highly doped β-Ga_2O_3 substrates by the EFG method were presented. The temperature-dependent J-V and C-V characteristics were analyzed rigorously. The C-V measurement indicated a high doping concentration of $2.9 - 3.5 \times 10^{18}$ cm^{-3} of the β-Ga_2O_3 substrate. At the forward bias under room temperature, the SBDs exhibited a good rectifying behavior. At room temperature, the devices had a turn-on voltage of ~0.84 V, an on-resistance of ~ 0.9 $m\Omega \cdot cm^2$, an on/off ratio of ~ 10^9, an ideality factor of 1.39, and a Schottky barrier height of 0.94 eV, respectively. In addition, the ideality factor showed a negative temperature dependence, and the Schottky barrier height had a positive temperature dependence. This is due to the inhomogeneous Schottky barrier interface caused by defects. Using the modified thermionic emission with the inhomogeneous Schottky barrier considered, the modified Richardson constant was found to be ~ 41.26 $Acm^{-2}K^{-2}$ and the mean Schottky barrier height ~ 1.36 eV. At the reverse bias, the device showed a relatively low breakdown voltage because of its high doping concentration. Two models including the two-step trap-assisted model and 1D-VRH model were used to fit the reverse leakage currents. Both play important roles in the reverse leakage current mechanism. The leakage current had a distinctive negative distance dependence, indicating it is bulk leakage dominated.

CHAPTER 3

VERTICAL GAN-ON-GAN SCHOTTKY BARRIER DIODES WITH MULTI-FLOATING METAL RINGS

3.1 Introduction and Background

Gallium nitride has been widely used in both electronic and photonic devices [47-53]. It is an ideal candidate for high power and high-frequency applications due to its wide bandgap (~3.4 eV), high critical electric field (>3 MV/cm), and high Baliga's figure of merit (BFOM). Conventional lateral GaN power devices have been grown and fabricated on foreign substrates such as sapphire [54, 55] and silicon [50, 56-58], which showed limited performance. This is because lateral geometry results in surface-related issues, poor thermal dissipation, and limitations on current and voltage ratings. The second reason is related to the heteroepitaxial growth which gives rise to high defect densities and thermal coefficient mismatch. Recently, bulk GaN substrates have been commercialized that can enable vertical GaN power devices with much lower defect densities, less stringent requirements on thermal managements, better immunity to surface states and higher currents and voltages [59-65]. GaN Schottky barrier diodes have been widely investigated due to low turn-on voltages, fast switching, and lack of reverse recovery charges.

One of the key topics of GaN power diodes is to eliminate or alleviate the electric field crowding effects at the junction edge to avoid device premature breakdown, thus achieving high breakdown voltages. Several edge termination methods have been reported, such as field plates, trench structures, and deep mesa etching [66-70]. Floating metal rings (FMRs) are another effective and easy-to-implement termination method [61, 71]. It has

been shown that FMRs can effectively reduce electric field concentrations of the main Schottky junction due to the expansion of the depletion layer along the FMRs [72]. This method has also been adopted in SiC [72, 73] and Ga_2O_3 [74] Schottky barrier diodes. Another advantage of this method is that FMRs are very easy to implement. Unlike other edge termination techniques which require complicated fabrication processes, FMRs can be formed simultaneously with the Schottky contact without additional fabrication steps, simplifying device fabrication and reducing costs. In this work, we demonstrate the FMR termination structure on vertical GaN-on-GaN Schottky barrier diodes with different FMR geometry designs. The devices have similar forward characteristics and nearly ideal ideality factors. With optimized FMR structures, device breakdown performance was improved. These results can serve as helpful references for the future development of power GaN devices.

3.2 Device Fabrication

The samples were grown homoepitaxially by metalorganic chemical vapor deposition (MOCVD) on *c*-plan n^+-GaN free-standing substrates. Trimethylgallium (TMGa) and ammonia (NH_3) were used as the gallium (Ga) and nitrogen (N) sources, respectively. N-type dopants Si were incorporated by using silane (SiH_4) precursors. Figure 3.1(a) shows the structure schematic of the devices. 1-μm-thick n^+-GaN with an electron concentration of ~ $2 \times 10^{18} cm^{-3}$ were first grown on the GaN substrates, followed by 9-μm-thick n-GaN drift layer with an electron concentration of ~ $2 \times 10^{16} cm^{-3}$, which was estimated by the capacitance-voltage (C-V) method [75]. High-resolution X-ray diffraction (HRXRD) was used to characterize the crystal quality of the samples. The setup used is the PANalytical X'Pert Pro materials research X-ray diffractometer (MRD) system using Cu Kα1 radiation source with a wavelength of 1.541 Å. The incident beam optics and the diffracted beam optics are the hybrid monochromator and the triple-axis module, respectively. The full width at half maximum (FWHM) of (002) and (102) planes are 44 and 32 arcsec, respectively. The dislocation density can be calculated by using the following equation:

$$D = \frac{\beta_{(002)}{}^2}{9\overrightarrow{b_1}^2} + \frac{\beta_{(102)}{}^2}{9\overrightarrow{b_2}^2} \quad (1)$$

where β is the FWHM and $\vec{b}$ is the Burgers vector [32]. The first term represents the screw dislocation density, and the second term represents the edge dislocation density. The dislocation density was about $2.2 \times 10^6\ cm^{-2}$, indicating high material quality of the epilayers.

After the material growth, conventional photolithography was then applied to fabricate the devices. Figure 3.1(b) shows the process fabrication flow. The samples were first cleaned with ultrasonic using acetone and isopropyl alcohol, then rinsed with deionized water. Next, photolithography was used to define the pattern of the contacts. An oxygen plasma treatment was applied to remove residual photoresist, followed by 30 seconds soaking in diluted hydrochloric acid (HCl) to remove potential surface oxidization layers. The metal deposition was conducted by electron beam evaporation. Pd/Ni/Au metal stacks were first deposited on the samples to form the anodes and FMRs, followed by rapid thermal annealing (RTA) at 400 °C in a nitrogen ambient. Then Ti/Al/Ni/Au metal stacks were then deposited on the backside of the samples to form the cathodes.

Figure 3.1(c) presents the geometry of the device with FMRs. The anode has a diameter of 100 μm surrounded by multiple FMRs. The number of FMRs varied from 0, 5, 10, to 20, and the spacing between the FMRs varied from 1.5 μm to 3.5 μm with a step of 0.5 μm. The width of the FMRs is 10 μm. Forward current-voltage measurements and reverse breakdown measurements were conducted using Keithley 2400 semiconductor parameter analyzer. Figure 3.1(d) demonstrates the measurement setup. During the breakdown measurements, the devices were immersed in Fluorinert (FC-40) to avoid flash-over through the air, which may underestimate the actual breakdown voltages.

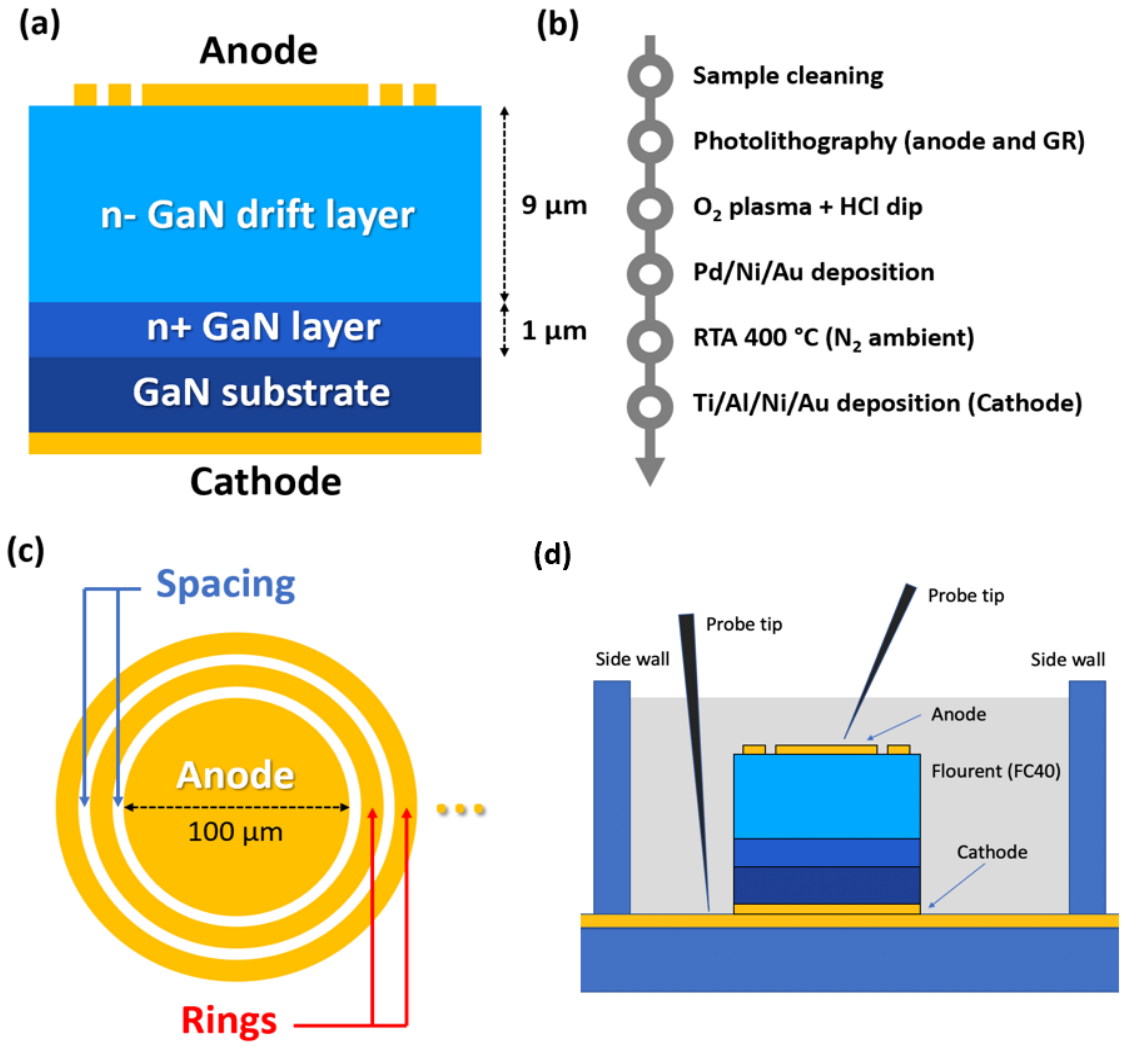

Fig 3.1. (a) Structure schematic of the vertical GaN Schottky barrier diodes with multi-floating metal ring termination structure (b) Fabrication process of the device. (c) Top view schematic diagram of the device with rings. (d) Measurement setup with the device immersed in FC40 to avoid breakdown through air.

3.3 Forward Characteristics

Figure 3.2 presents the forward current density-voltage (J-V) curves and the on resistance-voltage (R_{on}-V) curves of vertical GaN SBDs with 0, 5, 10, and 20 FMRs in a semi-log scale at room temperature. The spacings were fixed to be 2 μm. The forward voltage was applied at the anode from 0 V to 2 V with a step of 0.02 V with the cathode grounded. The current density was calculated based on the area of the anode. The maximum current densities of these 4 devices at 2 V were about 699, 761, 905, 661 A/cm^2, respectively. These devices all had a good on/off ratio of 10^9. The turn-on voltages of the four devices were extracted by linear exploration, which were about 0.96, 0.94, 0.94, 0.94 V, respectively. The specific on-resistances extracted from the curves were about 1.47, 1.37, 1.16, 1.59 mΩ·cm^2, respectively. These results indicate that the addition of FMRs doesn't significantly impact the device forward rectifying characteristics.

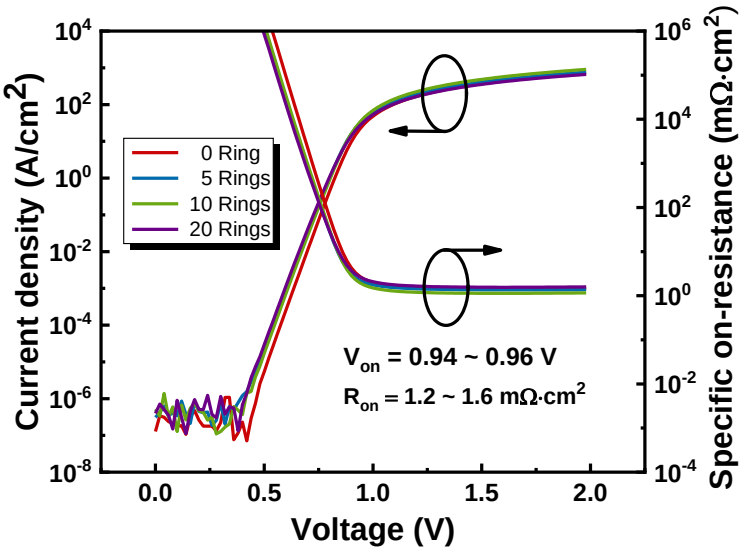

Fig 3.2. Forward current density-voltage curve (J-V) of vertical GaN Schottky barrier diodes in a semi-log scale with various floating metal rings at room temperature in a linear

scale. The on voltage is around 0.94 ~0.96 V. The specific on resistance is around 1.2~1.6 $m\Omega \cdot cm^2$. All four devices have a same spacing equal to 2 μm.

Figure 3.3 shows the forward temperature-dependent measurements of these four devices in both linear and semi-log scales. The temperature increased from 300 K to 420 K with a step of 30 K. The relationship between diode currents and voltages can be explained by the thermal emission model, which is described by the following equations [75]:

$$I = I_s \left\{ \exp[\frac{q(V - IR_s)}{nkT}] - 1 \right\} \tag{2}$$

$$I_s = AA^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \tag{3}$$

where I_s, V, R_s, n, k, T, A, A^*, ϕ_b, are the saturation current, the applied voltage, the series resistance, the ideality factor, the Boltzmann constant, the device area, the Richardson constant, and the effective Schottky barrier height, respectively. As the temperature increased, the current increased under off-state and decreased under on-state, respectively. This can be explained by the combination effect of the saturation current (I_s) and the series resistance (R_s). As the temperature increased, the saturation current increased naturally which leads to an increment in the diode current. On the contrary, as the temperature increased, the series resistance increased (due to more scattering) and hence the diode current decreased because of the $-IR_s$ term in equation (2). When the diode is off, the effect of the series resistance can be neglected since the current level is too small ($-IR_s \cong 0$). When the diode is on, this $-IR_s$ term needs to be taken into the consideration. Combine both effects, the different trends of the temperature dependence of the current under on/off

states can thus be explained. Moreover, The ideality factor and the Schottky barrier height can be calculated as a function of temperature using the following equations:

$$n = \frac{q}{kT}\frac{1}{\frac{d(lnI)}{dV}} \tag{4}$$

$$\phi_b = -\frac{kT}{q}\ln\left(\frac{I_s}{A^*T^2}\right) \tag{5}$$

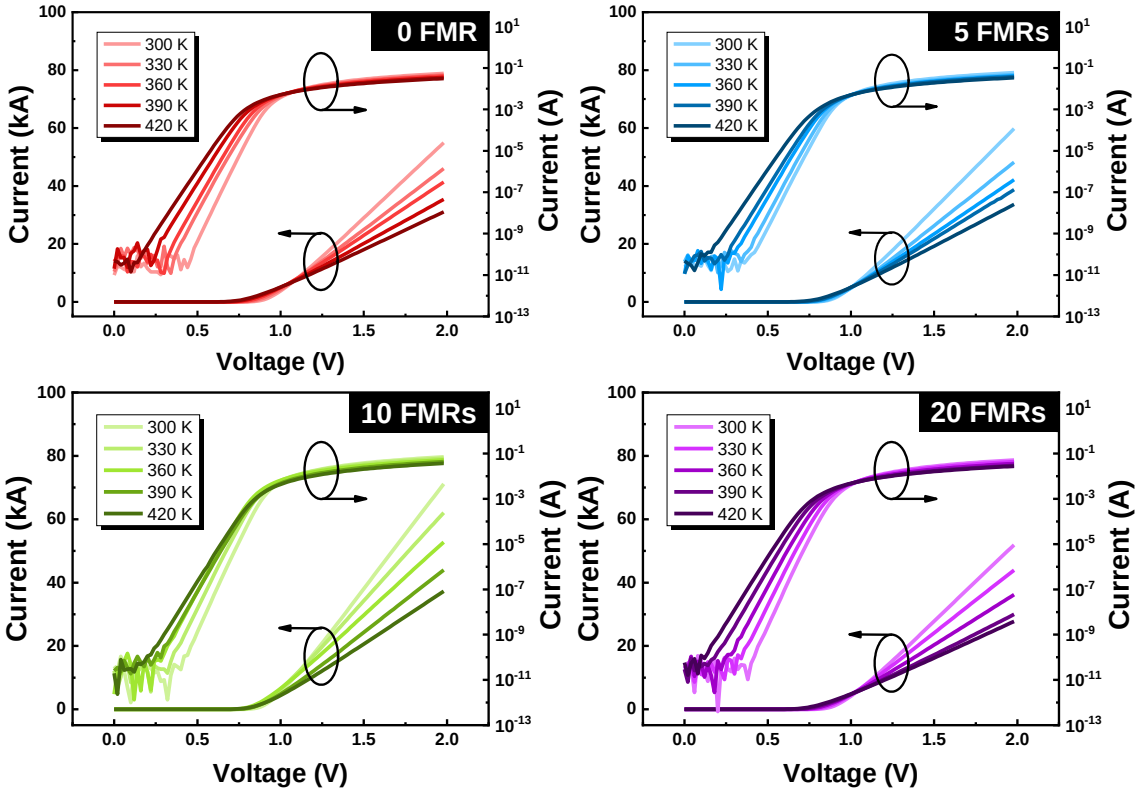

Fig. 3.3. Temperature dependent forward current-voltage (I-V) curves of devices with 0, 5, 10, 20 FMRs in both linear and semi-log scale. The temperature was increased from 300K to 420K with a step of 30 K. The four devices have identical forward electrical performance.

Figure 3.4(a) shows the extracted ideality factors and Schottky barrier heights as a function of temperature for the four devices. As the temperature increased from 300 K to 420 K, the ideality factor slightly decreased from 1.03, 1.09, 1.07, 1.09 to 1.01, 1.03, 1.03, 1.04, respectively, and the Schottky barrier height increased from 1.18, 1.12, 1.14, 1.11 eV to 1.21, 1.20, 1.26, 1.17 eV, respectively. The correlation between the ideality factor and the Schottky barrier height can be further characterized by a well know linear relationship, as shown in Fig. 3.4(b). The abnormal behavior of the device with 10 rings may stem from measurement errors. This phenomenon has been studied and reported previously in GaN [33, 76, 77] and other wide bandgap materials, such as Ga_2O_3 [75]and SiC [78]. The temperature dependence of both the ideality factor and the Schottky barrier height can be explained by the thermionic emission over an inhomogeneous Schottky barrier with a voltage-dependent barrier height. Some non-ideal condition such as rough interface between electrode and semiconductor, metal grain boundaries, and non-uniform metallurgy can lead to this spatial inhomogeneity [35, 36]. To incorporate the barrier inhomogeneity into the thermionic emission model in equation (2), it is assumed that the Schottky barrier has a Gaussian distribution potential with a mean barrier height $\overline{\phi_b}$ and a standard deviation σ, and the barrier is linearly dependent on voltage:

$$\phi_b = \overline{\phi_b} - \frac{q}{2kT}\sigma^2 \tag{6}$$

$$\overline{\phi_b} = \overline{\phi_{b0}} + \gamma V \tag{7}$$

$$\sigma^2 = {\sigma_0}^2 - \xi V \tag{8}$$

where $\overline{\phi_{b0}}$ and σ_0 are the mean barrier height and the standard deviation when V = 0. The coefficients γ and ξ represent the voltage-induced deformation of the Schottky barrier

distribution. Note that $\gamma < 0$ and $\xi > 0$, indicating larger voltage can decrease the mean Schottky barrier height and reduce the inhomogeneity of the barrier distribution, respectively [34, 75]. The ideality factor can be expressed as:

$$n^{-1} - 1 = -\gamma - \frac{q}{2kT}\xi \tag{9}$$

This explains why the experimental values of the ideality factor always exceed 1. Figure 3.4(c) shows the fitting plot of equation (7) and (9) using the average values of these devices. The extracted $\overline{\phi_{b0}}$ is about 1.41eV and the extracted σ_0 is about 0.12 eV. Previously reported SBDs on different materials showed a similar fluctuation parameter, such as Ga_2O_3 (0.14 eV) [75], α-IGZO (0.13 eV) [35], ZnO (0.134 eV) [37], and α-ZTO (0.12 eV) [34]. Moreover, this inhomogeneity modification can be applied into the original thermionic emission model:

$$ln\left(\frac{I_s}{AT^2}\right) - \frac{q^2{\sigma_0}^2}{2k^2T^2} = ln(A^*) - \frac{q\overline{\phi_{b0}}}{kT} \tag{10}$$

Figure 3.4(d) shows the original and the modified Richardson plot based on the Eqs. (3) and (10), respectively. The extracted original A^* ($3.91 \times 10^{-2}\ Acm^{-2}K^{-2}$) is unreasonably small. However, if we take the inhomogeneity barrier into consideration and use the modified model for the extraction, the value of A^* ($33.48\ Acm^{-2}K^{-2}$) is close to the theoretical value ($26\ Acm^{-2}K^{-2}$) [79]. Table 3.1 and figure 3.5 summarize the forward characteristics of the four devices. These devices have very similar forward performance, even though there are still some trivial differences due to non-uniformity of the material quality and the process fabrication skills, their forward characteristics are still similar enough for a fair comparison of the reverse breakdown performance in the next part.

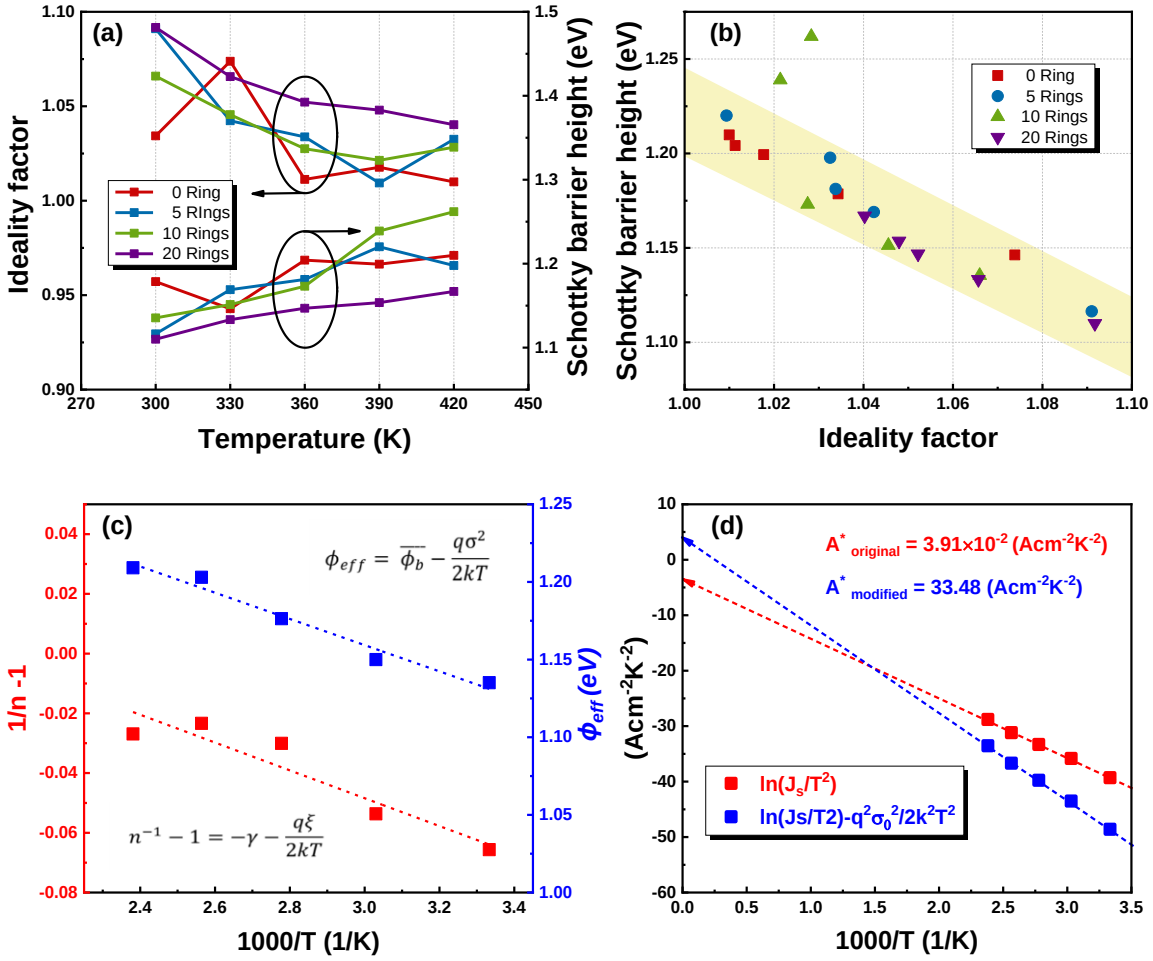

Fig 3.4. (a) Ideality factor and Schottky barrier height as a function of temperature from 300 K to 420K with a step of 30 K. (b) Ideality factor versus Schottky barrier height. (c) Plot of the average effective barrier height and n-1-1 versus 1000/T. (d) Original and modified Richardson plot for GaN SBDs. The dash line shows the fitting curve.

Fig. 3.5. Device forward characteristics for the SBDs with 0/5/10/20 FMRs. Despite the trivial differences caused by non-uniformity of the material quality and the process fabrication skills, their forward performance is similar enough for a fair comparison of the reverse breakdown measurement.

TABLE 3.1

DEVICE PARAMETERS FOR THE SBDs With Various FMRs

		0 FMR	5 FMRs	10 FMRs	20 FMRs
300 K	**Current density @ 2V (A/cm²)**	699	761	905	661
	Turn-on Voltage (V)	0.96	0.94	0.94	0.94
	Specific on-resistance (mΩ·cm²)	1.47	1.37	1.16	1.59
	Ideality factor	1.03	1.09	1.07	1.09
	Schottky barrier height (eV)	1.18	1.12	1.14	1.11
420 K	**Ideality factor**	1.01	1.03	1.03	1.04
	Schottky barrier height (eV)	1.21	1.20	1.26	1.17

3.4 Reverse Breakdown Measurement

Figure 3.6(a) presents the reverse breakdown voltage measurements of these four devices with 2 μm spacings and various numbers of FMRs. The device breakdown was edge breakdown with catastrophic damage at the contact edge as observed by optical microscopy. As the number of the FMRs increased from 0 (reference) to 5, 10, and 20, the average breakdown voltage increased from 223 to 247, 272, and 289 V, which were about 11%, 22%, 30% increment. This increase in breakdown voltages is because FMRs can be considered as depletion region extension to achieve a smooth potential contour at the device edge. More FMRs can help spread the electric field laterally at the device edge and thus significantly enhance the breakdown voltage.

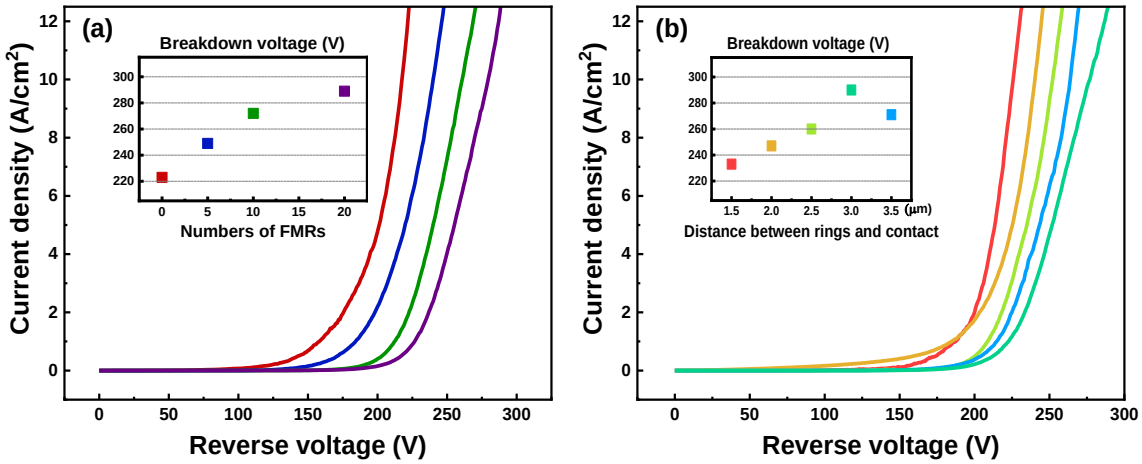

Fig 3.6. (a) Reverse breakdown voltage of GaN SBDs with 2 μm spacings and various numbers of floating metal rings (b) Reverse breakdown voltage of GaN SBDs with 5 FMRs and various distance between contact and rings.

In addition, the spacing between FMRs is also very critical since it determines the location of the peak electric field. Figure 3.6(b) shows the reverse breakdown voltage measurements of 5-ring GaN SBDs with various ring spacings from 1.5 μm to 3.5 μm with a step of 0.5 μm. As the spacing increased, the breakdown voltage increased from 233 to 247, 260, 290 and 271 V, about 4%, 11%, 17%**,** 30%, and 22% increment compared to the reference device (no ring, V_{br} = 223 V). The maximum breakdown voltage of 290 V occurred at the spacing equals to 3 μm. At this condition, the depletion region extensions can cover the spacings effectively and hence the electric field can spread widely. This helps lower the peak electric field and thus reach a higher breakdown voltage. However, when spacing equals to 3.5 μm, it is too wide for the depletion region extensions to cover the spacing effectively. As a result, the uniformity and the area of the electric field distribution decreased and hence the breakdown voltage decreased to 271 V. Furthermore, the enhancement effects in breakdown voltages by the FMRs with increasing ring spacing may also decreased afterward. Similar phenomenon happened in reference [15] and [28], too.

In short, although these devices have very similar forward performance, their reverse breakdown performance is very different. More FMRs lead to higher breakdown voltages, indicating that FMRs can effectively alleviate the electrical field crowing around the edge of the anode. In addition, the spacing of the FMRs also plays an important role in the electric field distribution of the devices.

3.5 Summary

Vertical GaN Schottky barrier diodes with various FMR structures were fabricated on bulk GaN substrates. The devices have a low R_{on} of 1.16 ~ 1.59 mΩ·cm^2, turn-on voltage of 0.96 ~ 0.94 V, and a high on-off ratio of 10^9. The ideality factor is about 1.03 ~ 1.09, which is nearly unity and the Schottky barrier height is about 1.11 ~ 1.18 eV at room temperature. As the temperature increased to 420 K, the ideality factor decreased and the Schottky barrier height increased. This phenomenon is due to the inhomogeneity of the Schottky barrier. All these devices have very similar forward characteristics, indicating the FMRs don't degrade the device rectifying performance. As the number of the FMRs increased from 0 to 5, 10, and 20, the breakdown voltage increased from 223 to 247, 272, and 289 V, respectively. This indicates more FMRs help distribute the electric field laterally at the device edge and thus enhance the breakdown voltage performance. In addition, as the spacing of the FMRs increased from 1.5 μm to 3.5 μm with a step of 0.5 μm, the breakdown voltage increased from 233, 247, 260, to 290, then drop to 271 V. The maximum occurred at 3 μm and then decreased afterward. This is because the non-effective depletion region expansion through the wider spacing. These results can serve as important references for the future design of FMR structure on power devices to obtain better breakdown performance.

3.6 Acknowledgement

The samples are provided by IQE KC, LLC. We acknowledge the use of facilities within the Eyring Materials Center at Arizona State University. The devices were fabricated at Nanofab at Arizona State University.

CHAPTER 4

ALGAN/GAN MISHEMT USING BN AS GATE DIELECTRIC

4.1 Introduction and Background

III-nitride based semiconductors have recently attracted considerable interest due to their superior high-power and high-frequency performances compared with Si, GaAs or other compound semiconductors[80, 81]. AlGaN/GaN high electron mobility transistors (HEMTs) are considered as next-generation power switching devices due to the existence of a polarization induced two-dimensional electron gas (2DEG) at the AlGaN/GaN interface[82-84]. Nevertheless, the performance of conventional Schottky-gate HEMTs has been limited by the high leakage current and low forward bias[85]. As a result, metal-insulator-semiconductor high electron mobility transistors (MISHEMTs) with gate dielectrics serve an effective solution to overcome the leakage current and surface issues of conventional Schottky-gate HEMTs[86-88]. Various dielectric materials have been investigated for the AlGaN/GaN MISHEMTs, including $SiO_{3[89]}$, $Si_3N_{4[89, 90]}$, $Al_2O_{3[88]}$, and some other high-k dielectrics[91, 92]. However, the performance of the AlGaN/GaN MISHEMTs is still far from its theoretical limitation because of strong coulomb scattering at the dielectric/AlGaN interface. Moreover, interface states and border traps result in reliability issues such as hysteresis effects in device performance[93]. It is of critical importance to seek better gate dielectric materials for AlGaN/GaN MISHEMTs.

Compared to oxide-based gate dielectric materials, nitride-based materials have significant advantages due to the lack of Ga-O related interface traps. Previous reports studied silicon nitride-based gate dielectric MISHEMTs[90, 94-96], where gate leakage,

gate swing, and interface trap density are remaining issues to be addressed. Recently, ultra-wide bandgap (UWBG) semiconductor boron nitride (BN) has garnered considerable research interests for high power and high temperature applications[97-99], due to its ultra-wide bandgap of ~5.2 eV[100], projected high breakdown electrical field of 12 MV/cm, relatively large dielectric constant of 3.76[101], and high thermal conductivity of 1300 W/Km. In addition, BN exists in various crystalline forms including a-BN (amorphous), h-BN (hexagonal), c-BN (cubic), w-BN (wurtzite). Among all these forms, hexagonal boron nitride is the most stable one. Since gallium nitride is also a hexagonal structure, if we are looking for a perfect dielectric layer for gallium nitride, then h-BN should be a more promising candidate over other nitride-based dielectric material.

BN exists in the sp3 bonded cubic phase analogous to diamond and the sp2 bonded hexagonal phase analogous to graphite or graphene. BN has also been formed in disordered films that include mixtures of sp2 and sp3 bonding[102]. Recently, some researchers demonstrated BN as gate dielectric in diamond-based or gallium oxide-based field effect transistors[103-105], where the BN thin film was transferred via mechanical exfoliation. However, there are few reports on BN as gate dielectric for AlGaN/GaN MISHEMTs[86, 106, 107]. In this work, we have demonstrated AlGaN/GaN MISHEMTs with electron cyclotron resonance microwave plasma chemical vapor deposition (ECR-MPCVD) deposited BN as gate dielectric. The ECR-MPCVD process used here is carbon free. The *in-situ* X-ray photoelectric spectroscopy (XPS) and UV photoelectron spectroscopy (UPS) are used to characterize the BN thin film structure, and the BN/GaN cap interface band offset. The transfer and output characteristics of AlGaN/GaN MISHEMTs indicate excellent switching performance with a high on/off ratio of 10^9 and a subthreshold swing

of 69.1 mV/dec. Gate leakage mechanisms under low and high electric field are also investigated.

4.2 Material Growth

The AlGaN/GaN MISHEMTs epitaxial layers were grown by metalorganic chemical deposition (MOCVD) on 6-inch Si substrates. The Al, Ga, and N sources are trimethylaluminum (TMAl), trimethylgallium (TMGa), and ammonia (NH_3), respectively. SiH_4 was used as n-type dopant and H_2 was the carrier gas. The structure consists of 3nm GaN cap layer, followed by a 28 nm AlGaN barrier layer, a 1 nm AlN interlayer, a 0.23 μm n-GaN layer, and a 3.6 μm unintentionally doped GaN buffer layer. 10 nm BN thin film layer was deposited as gate dielectric on AlGaN/GaN MISHEMTs by electron cyclotron resonance microwave plasma chemical vapor deposition (ECR-MPCVD) with a base pressure of 3×10^{-9} Torr. Before deposition, the AlGaN/GaN MISHEMTs wafer was first cleaned in the deposition chamber by flowing 35 sccm of N_2 and 20 sccm of H_2 at a pressure of 2×10^{-4} Torr under 875 °C for 60 minutes, with N_2 flow while heating and cooling. The sample surface was then characterized by *in-situ* UPS and XPS shown in Figure 4.1(c) and 4.1(a) respectively. BN was then deposited on the cleaned sample surface for 20 minutes with He of 36 sccm, Ar of 2.5 sccm, H_2 of 1 sccm, N_2 of 12.5 sccm, and BF_3 of 1 sccm. The sample was bias at –60V. The deposition temperature was 850 °C, the microwave power was 1.4 kW, and the chamber pressure was 1×10^{-4} Torr with N_2 flow while heating and cooling. The sample cleaning and BN deposition parameters in ECR-MPCVD are summarized in Table 4.1.

Table 4.1. The cleaning and deposition condition for the BN/AlGaN/GaN HEMTs.

	Clean	**Deposition**
Substrate Temperature	875 ± 25 °C	825 ± 25 °C
Chamber Pressure	2×10^{-4} Torr	2×10^{-4} Torr
Applied Bias	N/A	- 60 W
Microwave power	N/A	1400 W
Time	60 minutes	20 minutes
Gas flow (sccm)		
He	0	35
Ar	0	2.5
N_2	35	12.5
BF_3	0	1
H_2	20	1

4.3 Material Characterization

In situ XPS and UPS were used to analyze the sample surface before and after BN deposition. The X-ray source in XPS is monochromatic Al-Kα x-rays with energy of 1486 ± 0.2 eV. The UV source for UPS is a helium discharge lamp, where the He II emission line (40.8 eV) is used to measure the valence band maximum (VBM) of the clean AlGaN/GaN surface and the deposited BN layer. The chamber base pressure is 5×10^{-10} Torr monitored by a hot filament ion gauge. An Omicron Scientia R3000 spectrometer with a four-element electrostatic lens was used in a sweep mode to scan the full energy range of photoelectrons. The hemispherical analyzer has a slit size of 0.4 mm and a pass energy of 100 eV for XPS (2 eV for UPS), leading to an energy resolution of 150 meV for XPS (3 meV for UPS). It is worth noting that transition lifetime of core holes and thermal motion can cause peak broadening beyond the energy resolution. The spectrometer is calibrated using the gold 4f energy (for XPS) and the Fermi energy (for both XPS and UPS). The XPS spectra were fit with gaussian functions. Peak centers correspond to the binding energy of element core level electrons. Peak areas are used to calculate relative concentrations of elements[108], thickness of deposited layer[109], and the ratio of sp2:sp3 hybridization[110] (i.e. the ratio of hexagonal to cubic BN). The band gap of BN is measured using the boron electron energy loss peak[108, 111]. UPS spectra were fit with a linear extrapolation to determine the VBM.

Figure 4.1(a) shows the full XPS energy range before and after BN deposition. No oxygen signal (~532 eV) was observed after the cleaning process of AlGaN/GaN MISHEMTs wafer, indicating clean AlGaN/GaN surface. The presence of the Al 2p peak is consistent with a GaN cap thickness of 3 nm over the AlGaN layer, as the escape depth

of the photoelectrons in GaN are about 10 nm. After the 20-minute BN deposition, the Ga peaks were no longer visible. A small amount of fluorine is typically observed due to the residue from the boron precursor (BF_3). Figure 4.1(b) demonstrates the XPS spectrum of boron 1s core level. The faction of sp^2:sp^3 bonding was estimated using the π-plasmon : B 1s intensity ratio (green line : blue line). A reference film containing h-BN without any evidence of c-BN in Fourier transform inferred spectroscopy measurements was reported to have a π-plasmon: B 1s intensity ratio of 0.122 ±0.018. The measured ratio of the deposited BN is 0.087 ± 0.020. Indicating that the BN layer is mostly (71±17%) in the hexagonal phase. Figure 4.1(c) presents the valence band spectrum using He II photon source, the VBM for clean GaN and BN surface are 3.0 ± 0.03 eV, and 3.4 ± 0.05 eV, respectively. Figure 4.1(d) present the energy band alignment of BN deposited on GaN cap surface. The band gap of h-BN was found to be 5.0 ±0.1 eV using the onset of the core level energy loss peak.

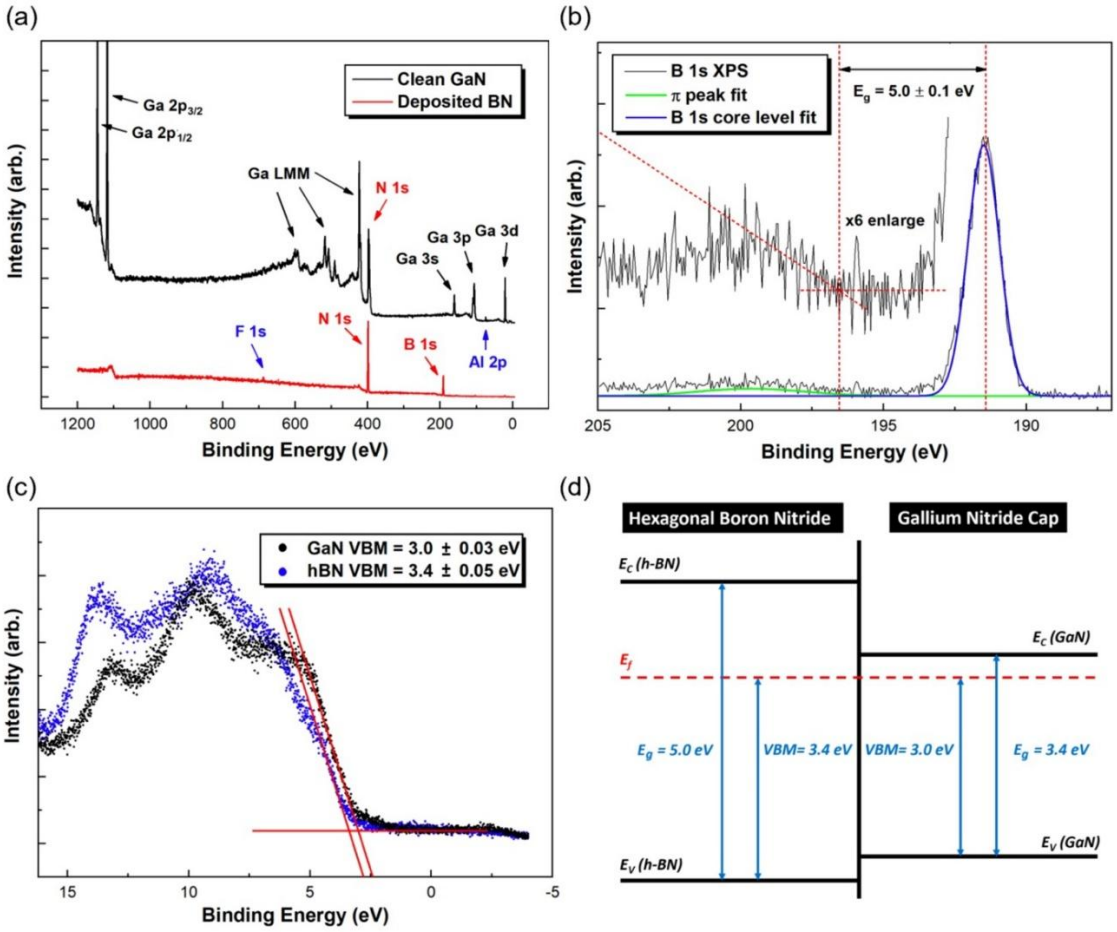

Fig 4.1. (a) Full XPS energy range before and after deposition of boron nitride. No significant signal from oxygen or carbon on the clean GaN. (b) XPS boron 1s core level (191.5eV). The π peak (green line) to core level ratio indicates the BN layer is mostly (70-80%) in the hexagonal sp2 structure. The onset of the π peak indicates a band gap of 5.0±0.1eV. Boron to Nitrogen ratio is B:N = 0.9 (c) Valence band spectrum using He II photon source. The Valence band maximum for clean GaN and BN surface is 3.0±0.03eV, and 3.4±0.05eV relative to the Fermi level, respectively. (d) Energy band alignment of BN deposited on GaN using the measure values of the VBM's and band gap of BN layer.

4.4 Device Fabrication

After the BN thin film deposition by ERC-MPCVD, conventional photolithography was utilized to fabricate the AlGaN/GaN MISHEMTs. Figure 4.2(a) shows a schematic of the AlGaN/GaN on Si sample layer structure before BN deposition, and Fig. 4.2(b)-(g) present the device fabrication process flow. The samples were first cleaned using acetone and isopropyl alcohol in an ultrasonic bath, and then rinsed with deionized water. Then the mesa was defined and etched by chlorine-based inductively coupled plasma-reactive ion etching (ICP-RIE). Next, the dielectric via hole for source and drain contacts were etched by SF_6 based ICP-RIE, which selectively etches the h-BN at a rate of 48 nm/min without reacting with the GaN underneath. It is important to use proper etching methods since over-etching BN thin film through GaN cap layer is unwanted[112]. After mesa etching, photolithography and lift-off process were used to define the source and drain contacts. A 30 second oxygen plasma treatment was applied to remove residual photoresist, followed by a 30 second soaking in diluted hydrochloric acid (HCl) to remove potential surface oxidization layers. The Ti/Al/Ni/Au (20/120/30/100 nm) metal stacks were deposited by electron beam evaporation for source and drain metal contacts, followed by a rapid thermal annealing (RTA) at 850°C in an ambient nitrogen atmosphere. Finally, after defining the gate metal pattern by photolithography, the Ni/Au gate metal stacks were deposited on BN gate dielectric by electron beam evaporation. The gate width (W_G), gate length (L_G), gate source distance (L_{GS}), and gate drain distance (L_{GD}) are 500 μm, 4 μm, 4 μm, 4 μm, respectively. A corresponding metal-insulator semiconductor (MIS) diode were also fabricated for the J_g-V_g characterization.

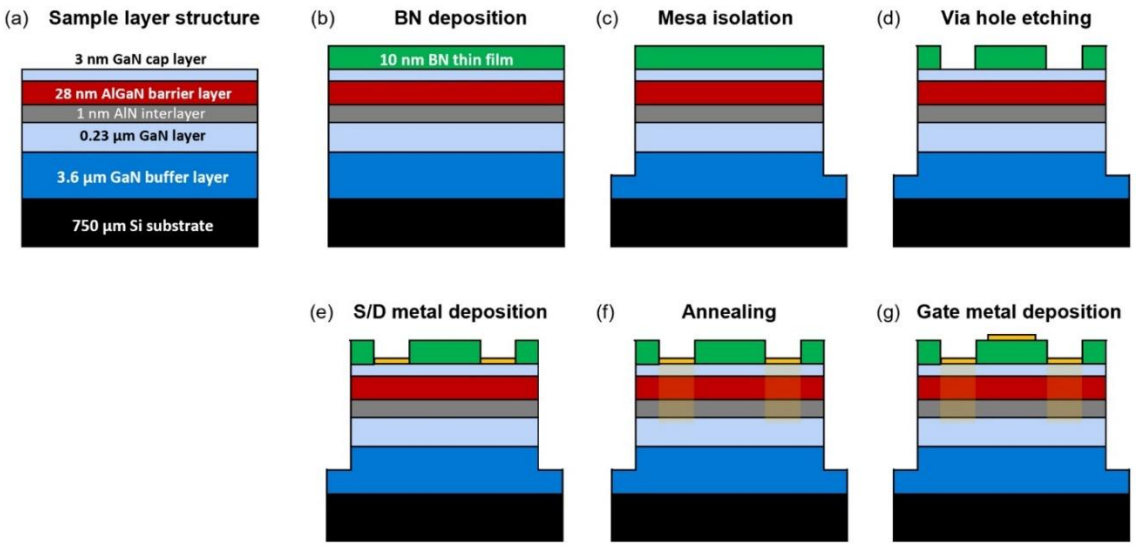

Fig 4.2. The fabrication process of the BN/AlGaN/GaN HEMTs. (a) AlGaN/GaN on Si sample layer structure. (B) 10 nm Boron nitride thin film deposition by ERC-MPCVD as gate dielectric. (c) Mesa isolation through chlorine based ICP etching. (d) Gate dielectric via hole for drain and source contact through SF6 based ICP etching. (e) Source and drain metal contact deposition by e-beam evaporation. Lift off method is applied. (f) Rapid thermal annealing for the ohmic contacts formation. (g) Gate metal contact deposition by e-beam evaporation.

4.5 Devices Forward Characteristics

The basic DC characteristics of the BN/AlGaN/GaN MISHEMTs was first investigated. Figure 4.3(a) demonstrates the transfer characteristics of the devices. The maximum drain current is about 62.6 mA/mm at V_{DS} = 1 V and V_{GS} = 0 V, and the threshold voltage is about −2.76 V. The maximum transconductance ($g_{m,\ max}$) is about 32 mS/mm when V_{DS} = 1V and V_{GS} = −2.1V. The devices exhibit a small subthreshold swing of 69.1 mV/dec and a high I_{on}/I_{off} ratio on the order of 10^9. The effective interface state density D_{it} can be estimated by the subthreshold swing equation[107]:

$$SS = \frac{kT}{q}\ln(10)\left(1 + \frac{C_s + C_{it}}{C_{ox}}\right)$$

where C_s, C_{it}, and C_{ox} are the semiconductor capacitance, interface state induced capacitance and the dielectric capacitance, respectively. While the semiconductor capacitance C_s varies non-trivially with the applied gate it is still possible to estimate the maximum D_{it} by the equation below[90]:

$$D_{it} = \frac{C_{it}}{q} < C_{ox}\left(\frac{qSS}{kTln(10)} - 1\right)$$

Since the relative dielectric constant of BN is ~3.76[101] , the maximum D_{it} can thus be calculated to be ~8.49×10^{11} $cm^{-2}eV^{-1}$. Figure 4.3(b) demonstrates output characteristics of the devices under forward sweeping and backward sweeping. The V_{DS} is swept from 0 V to 5 V (black line) and 5 V to 0 V (red dash line) with V_{GS} stepped between -2 V and 1 V with steps of 0.5 V. No obvious differences were observed in the two output curves, indicating very low hysteresis effect. The on-resistance is about 12.75 Ω·mm.

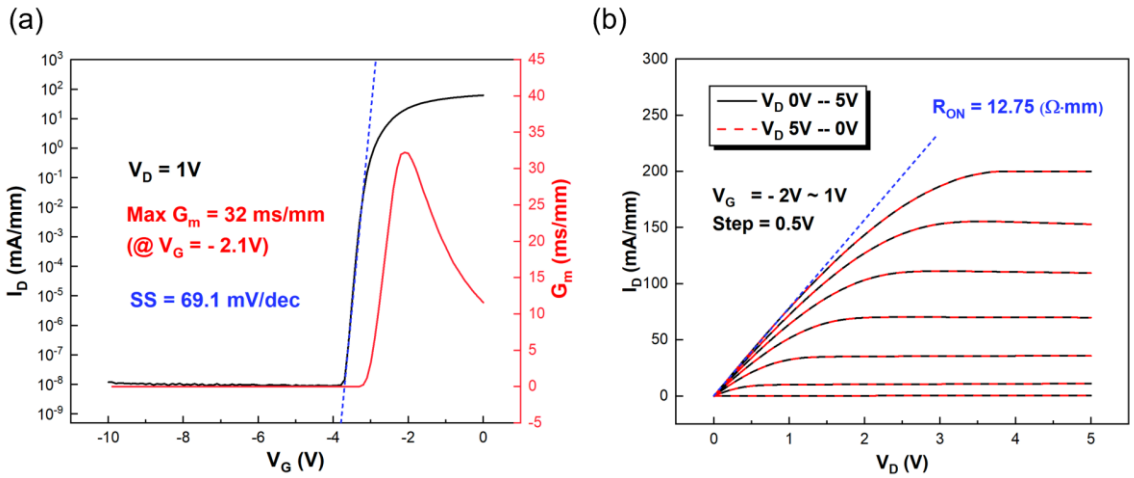

Fig 4.3. (a) [Black] Transfer curve of the BN/AlGaN/GaN MISHEMTs at V_{DS} = 1V in semi-log scale at room temperature. [Red] Transconductance of the device in linear scale at room temperature. The maximum G_m is about 161 mS/mm at V_G = -2.1V. The subthreshold swing is about 69.1 mV/dec. (b) Output characteristics of the BN/AlGaN/GaN MISHEMTs, where V_{GS} swept from -2V to 1 V with a step of 0.5 V in linear scale. The on-resistance is about 2.55 Ω·mm by linear extraction.

4.6 Gate Leakage Mechanism

In order to investigate the gate dielectric properties, gate leakage-gate voltage (I_G-V_G) curve was measured as shown in Fig. 4.4(a), where drain voltage and source voltage is set as 0 V. Very low gate leakage currents of 10^{-8} mA/mm was observed, suggesting good insulating properties of the BN gate dielectric. Due to the gate current compliance setting, the MISHEMTs were not able to be stressed to forward hard breakdown, but the corresponding electric-field maximum can still be estimated from Fig. 4.4(a) to be > 8.4 MV/cm[90]. Compared with the theoretical breakdown electric field of BN (12 MV/cm), our result shows that the ERC-MPCVD deposited BN has a very good breakdown endurance. To further investigate the gate leakage mechanism, Fig. 4.4(b) presents temperature-dependent gate current density versus gate voltage (J_G-V_G) curves of the MIS diode from 300 K to 500 K. The MIS diode has a diameter of 200 μm and an area of 3.14 × 10^{-4} cm^2. When V_G < 3.8 V, the gate leakage current is very small and below the setup lower limit (Agilent 4330). When 3.8 V < V_G < 7 V, the curves exhibit an obvious temperature-related dispersion, which indicated certain thermal emission mechanism plays an important role here. When V_G > 7 V, the curves at different temperatures began to merge again. There are some widely accepted mechanisms for the gate leakage through dielectric, such as Poole–Frenkel (PF) emission, trap-assisted tunneling, Fowler–Nordheim (FN) tunneling, and space charge limited current[113]. A more in-depth leakage mechanism analysis can be studied from the Fowler-Nordheim plot (FN plot, $ln(J_G/E_{ox})$ vs. $E_{ox}^{1/2}$). The electric field across the BN dielectric (E_{ox}) can be calculated from the below equations:

$$E_{ox} = \frac{V_{ox}}{t_{ox}}$$

$$V_{ox} = V_G + \frac{1}{q}(\Delta E_{c1} - \Delta E_{c2})$$

$$\Delta E_{c2} = \varphi_{Ni} - \chi_{ox}$$

where V_{ox}, t_{ox}, φ_{Ni}, $\chi_{ox,}$ and ΔE_{c1} are voltage across the dielectric, dielectric thickness (10 nm), Ni work function (5.15 eV)[114], dielectric electron affinity (4.5 eV), and band offset between BN/GaN interface respectively. An iterative calculation method was conducted to extract the value of ΔE_{c1}. Further detail can be found in the reference[90]. Figure 4.4(c) shows the FN plot of the devices from 300 K to 500 K. When the electric field is low ($0.15 < 1/E_{ox} < 0.3$), the curves were strongly dependent on temperature, suggesting that the PF emission is the dominant leakage mechanism. At high electric field ($1/E_{ox} < 0.15$), the curves are independent of temperature, indicating FN tunneling dominates the gate leakage. Figure 4.4(d) illustrates the schematic energy band diagram of these two dominant leakage current mechanisms. At low electric fields, when the temperature increased, the thermal excitation of electrons may emit from traps into the conduction band of the dielectric, hence the leakage current increased. At high electric fields, when the dielectric barrier is thin enough, the electron wave function may penetrate through the triangular potential barrier tunneling directly from the AlGaN to the metal.

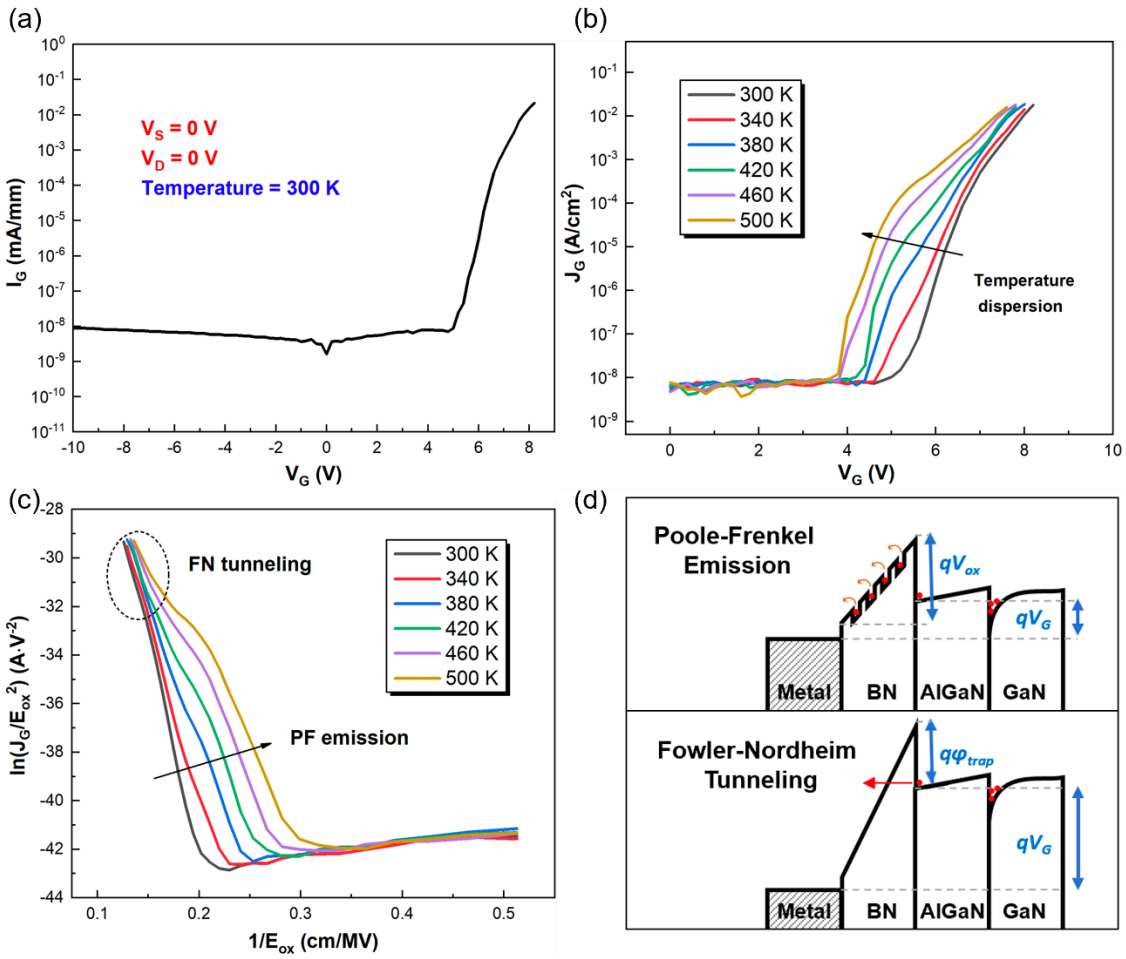

Fig 4.4. (a) I_G –V_G curve of the ERC-MPCVD-BN/AlGaN/GaN MISHEMTs. The gate leakage current is of 10^{-7} mA/mm range or less under both reverse and low forward gate voltage. (b) J_G-V_G curves of devices under various temperatures from 300 K to 500 K with a step of 40 K. (c) FN plots under various temperatures. At relatively low electric field, PF emission dominant the leakage current, results in an obvious temperature dispersion. At high electric field, FN tunneling dominants the leakage current, the curves merged again since it's no longer temperature dependent. (d) Schematic energy band diagrams of PF emission and FN tunneling.

4.7 Summary

In summary, we have demonstrated an AlGaN/GaN MISHEMT structure with ERC-MPCVD grown BN as gate dielectric. *In situ* XPS and UPS were used for comprehensive surface characterizations. The *in-situ* high temperature cleaning and deposition processes lead to high quality BN dielectric film. The devices exhibit a low off-state current of 10^{-8} mA/mm, a high on/off current ratio of 10^{9}, a stable threshold voltage of −2.76 V, a high maximum transconductance of 32 mS/mm, a nearly ideal subthreshold swing of 69.1 mV/dec, and an on-resistance of 12.75 Ω·mm. The interface state density (D_{it}) is estimated to be less than 8.49×10^{11} $cm^{-2}eV^{-1}$. The maximum breakdown electric field is no less than 8.4 MV/cm. The leakage current mechanisms were also studied by temperature-dependent measurements. Poole–Frenkel emission and Fowler–Nordheim tunneling are two dominant mechanisms for the leakage current under low and high electric field, respectively. These results can serve as important reference for future studies on BN-based gate dielectric for GaN power devices.

4.8 Acknowledgement

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CHAPTER 5

THE CHALLENGES AND OPPORTUNITIES OF WBG MATERIALS

5.1 The Challenges of WBG semiconductors

The main advantage of using WBG semiconductor power devices instead of conventional silicon power devices in low (<1.7kV) and medium (<6.5kV) voltage range including better energy efficiency, reduced size of the power devices, better field reliability, and higher operation temperature range.[115]

However, nowadays, the commercially available WBG power products still facing some challenges to fully replace the silicon power devices that dominate the past half century. These challenges including substrate size and cost, difficulty of systems integration, and the device design and cost.

Although the quality of GaN and SiC wafers is improving, the cost of producing larger-diameter wafers still needs to be reduced. Currently, to my best understanding, 8-inch SiC wafer and 6-inch GaN wafer is the largest wafer size that commercially produced. As to the system integration, WBG devices are not always suitable drop-in replacements for Si-based devices. The larger, more complex systems must be redesigned to integrate the WBG devices in ways that deliver unique capabilities. The device design and chip cost is the biggest issue. If we compare the cost of WBG power devices and silicon power devices with identical voltage and current spec, it may be possible and promising that the former has better performance on energy efficiency and robustness. However, there is still a large gap for WBG power devices to compete with silicon on the chip cost. In fact, based on the current situation, it is highly unlikely that the cost of WBG power chip has a chance

to be lower than that of silicon power chip. Several cost factors including higher starting material cost, higher epitaxial/fabrication cost, poor wafer level yield, and higher packaging cost are all the bottlenecks for WBG power devices. High cost of starting material comes from the expensive crystal growing process that require specific tool, expensive materials, high growth temperature, and long growing period. All the above difficulties still limit the speed of WBG power devices to replace traditional silicon power devices. However, as the rapid development of WBG semiconductors, no matter sooner or later, it is believed that we will eventually face the golden cross of WBG semiconductors to replace silicon in power devices.

5.2 The Opportunities of WBG semiconductors

WBG SiC and GaN electronics have a great development in the past decades. In 2015, the combined market size growing is about $210M USD per year. Recently, GaN RF devices have also been applied into commercial cellular base stations. As manufacturing capabilities improve, fabrication techniques develop, and market applications expand, costs are expected to decrease. This making WBG based devices competitive with less expensive Si-based devices. In 2018, SiC was used in Tesla's cars. In 2019, compact size GaN fast charger was developed. Significant future market growth is anticipated for WBG semiconductors, especially for power electronics applications in electronics, power grid integration systems, and electric vehicles.

Electronics: WBG materials has already been used in large, high-efficiency data centers. In addition, compact size power supplies or power chargers were developed for consumer electronics.

Grid integration: WBG-based inverters can convert the DC electricity generated from solar and wind energy into the AC electricity used in homes and businesses. Moreover, it can reduce the power loss a lot compared to silicon-based power devices.

Electric vehicles and plug-in hybrids: WBG devices have numerous applications in motor drives. These WBG devices can provide significant benefits for low-inductance motors, high-speed motors, and electric drives operating in high-temperature environment, as shown in Fig. 5.1[116].

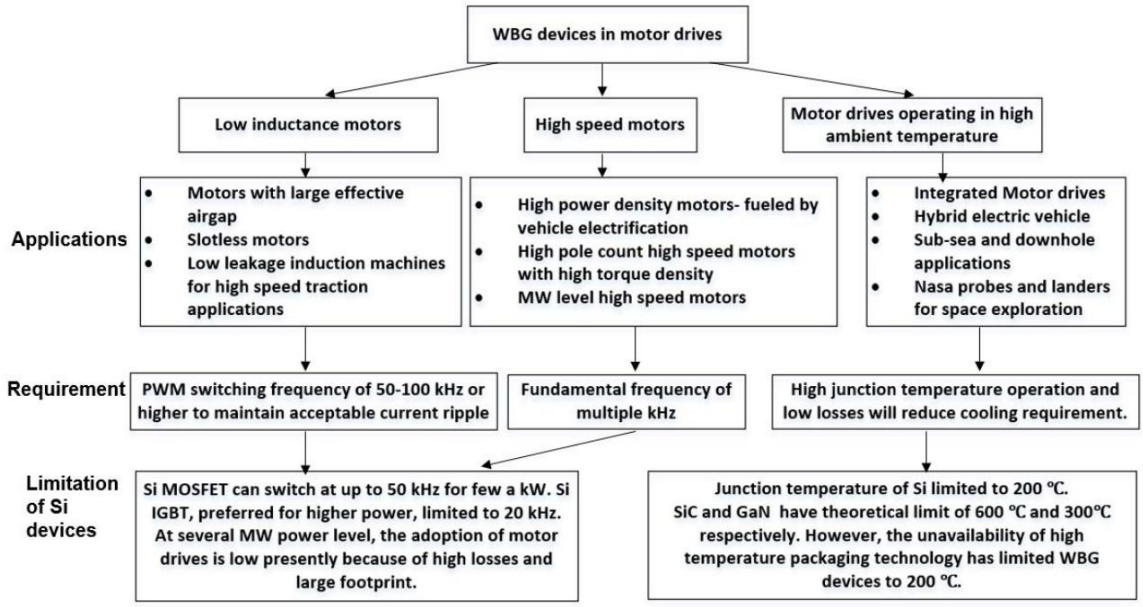

Fig. 5.1. Applications of WBG devices in ac motor drives. [116]

5.3 Possible Future Works

In conclusion to the dissertation, there are still a lot of interesting topics to be investigate on WBG and UWBG materials. For Ga_2O_3 SBDs, more physical fundamental details can be studies such as its CV and defects, and the improvement of its breakdown voltage and reduce the on resistance. For GaN-on-GaN vertical SBDs with FMRs, a comprehensive simulation would be perfect to fit the experiment data. Besides, a comparison of hydrogen plasma guard wing with FMR would be interesting. For BN MISHEMT, a detailed CV analysis and reliability test with time-dependent-dielectric-breakdown (ttbd) is important to evaluate the performance of the dielectric. In addition, a BN Trench MOSFET is also interesting. The AlN based devices are also attractive since this is a new field. No one knows how it would be. The difficulties including high growth temperature and the optimization of its ohmic contact formation.

In conclusion, I have done some works on these charming materials. There are still a lot of work to be investigated and discovered. My PhD journey is not the end of my research interest, it could be a new start. Thanks to everyone who ever helps me.

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