Two Dimensional Materials Based Memristors

for In-memory Computing and Neuromorphic Computing

by

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ABSTRACT

Modern Complementary-Metal-Oxide-Semiconductor (CMOS) technologies are facing critical challenges: scaling channel lengths below ~10 nm is hindered by significant transport degradation as bulk semiconductors (i.e., silicon) are thinned down, energy consumption is affected by short-channel effects and off-state leakage, and conventional von Neumann computing architectures face serious bottlenecks affecting performance and efficiency (energy consumption and throughput). Neuromorhic and/or in-memory computing architectures using resistive random-access memory (RRAM) crossbar arrays are promising candidates to mitigate these bottlenecks and to circumvent CMOS scaling challenges. Recently, emerging two dimensional materials (2DMs) are investigated towards ultra-scaled CMOS devices, as well as towards non-volatile memory and neuromorphic devices with potential improvements in scalability, power consumption, switching speed, and compatibility with CMOS integration.

The first part of this dissertation presents contributions towards high-yield 2DMs field-effect-transistors (FETs) fabrication using wafer-scale chemical vapor deposition (CVD) monolayer MoS_2. This work provides valuable insight about metal contact processing, including extraction of Schottky barrier heights and Fermi-level pinning effects, for next-generation integrated electronic systems based on CVD-grown 2DMs.

The second part introduces wafer-scale fabrication of memristor arrays with CVD-grown hexagonal boron nitride (h-BN) as the active switching layer. This work establishes the multi-state analog pulse programmability and presents the first experimental demonstration of dot-product computation and implementation of multi-variable stochastic linear regression on h-BN memristor hardware. This work extends beyond previous

demonstrations of non-volatile resistive switching (NVRS) behavior in isolated h-BN memristors and paves the way for more sophisticated demonstrations of machine learning applications based on 2DMs.

Finally, combining the benefits of CVD-grown 2DMs and graphene edge contacts, vertical h-BN memristors with ultra-small active areas are introduced through this research. These devices achieve low operating currents (high resistance), large R_{HRS}/R_{LRS} ratio, and enable three-dimensional (3D) integration (vertical stacking) for ultimate RRAM scalability. Moreover, they facilitate studying fundamental NVRS mechanisms of single conductive nano-filaments (CNFs) which was previously unattainable in planar devices. This way, single quantum step in conductance was experimentally observed, consistent with theorized atomically-constrained CNFs behavior associated with potential improvements in stability of NVRS operation. This is supported by measured improvements in retention of quantized conductance compared to other non-2DMs filamentary-based memristors.

DEDICATION

To “Life, Family, Friends”

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My PhD life at Arizona State University has come to an end. When I reflect on the journey at ASU in the past several years, it would not have been this meaningful and colorful without many incredible individuals I met. Here, I would like to thank the people that have supported me in various ways get to where I am today.

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CHAPTER 1

INTRODUCTION

Background

Currently, the CMOS technologies are facing some critical challenges: the scaling down of the device dimension, energy consumption, and computing architecture. In the past several decades, the number of transistors on chips has been doubled every two years based on Moore's law, which is shown in Figure 1.1 (a), to obtain high integration density, high operation speed and low cost per transistor[1]. However, it is more and more difficult to maintain the Moore's law as the transistors dimension become smaller and smaller[2]. The other issue along with Moore's law is that the energy consumption problem in current computing systems. As you can see in Figure 1.1 (b), the energy costs of data centres,

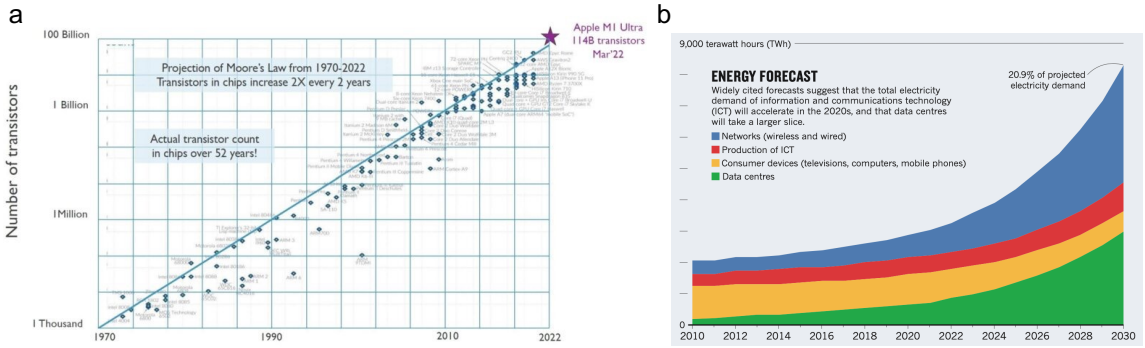

Figure 1.1 (a) Moore's law and (b) energy forecast for network, information and cummunication technology (ICT), consumer devices, and data centres

consumer devices, production of ICT (information and communication technoloogy), and networks have been increasing significantly in recent years[3].

The third issue arises from the von Neumann structure of the computing system. It includes the central processing unit (CPU), memory and input/output (I/O) components and has been widely adopted in modern computing systems. However, the problem is that the throughput rate of computer system is limited because of the relatively slow rate of data

transfer from memory compared with the frequency of the CPU, as you can see in Figure 1.2[4]. This is known as “von Neumann bottleneck”. Hence, there exists a substantial need

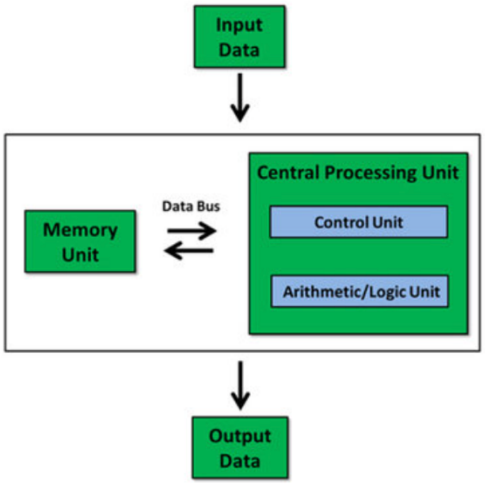

Figure 1.2 Von Neumann structure[4]

for the advancement of novel memory technologies and emerging computing systems that can facilitate high-density memory storage and efficient computational processes.

The existing conventional memory technologies include dynamic random-access memory (DRAM), static random-access memory (SRAM), and flash memory, such as NAND and NOR. The DRAM and SRAM are volatile memories, in which the data will lose once the power is disconnected, while the flash memory is non-volatile, in which the data will be retained even if the power is off. DRAM comprises of one transistor and one capacitor (1T1C). It is energy-consuming since the charge in the capacitor needs to be refreshed frequently. SRAM is fast, but the disadvantage is the large memory cell size, which limits the applications for high-density memory. Flash memory cell consists of a floating-gate MOS transistor (FG-MOSFET), which utilizes the storage of charges in different level, such as multi-level cell (MLC), in floating gate to realize multi-level storage

memory. However, flash memory requires a high voltage to charge the floating gate which requires a high energy consumption and low operation speed[5].

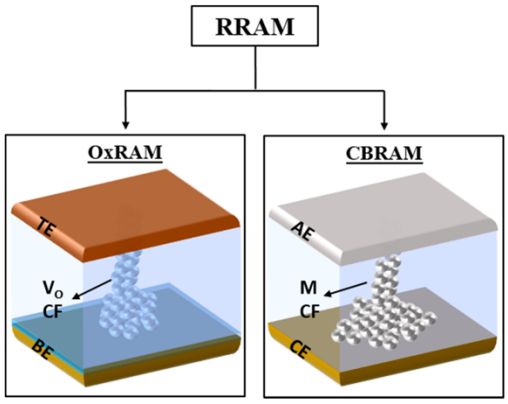

Figure 1.3 Schematic of the classification of RRAM based on different switching mechanism as metal oxide RRAM (OxRAM) and conductive bridge RAM (CBRAM)[5]

Many emerging memory technologies have been investigated recently, including phase change memory (PCM), magneto-resistive random-access memory (MRAM), and resistive random-access memory (RRAM). These emerging memories rely on the changes of resistance or conductance of the switching materials in the cells to store information rather than using the storage of charges. RRAM, also call resistive switching memory or memristor, has been widely investigated among the emerging memory technologies due to its promising properties for next-generation memory, such as fast-switching speed, high storage density, low energy consumption, non-volatility, and extremely simple device structure. It contains two planar electrodes (top electrode and bottom electrode) and a switching layer sandwiched in between, as you can see in Figure 1.3, which shows the classification of RRAM based on different switching mechanisms as metal oxide RAM (OxRAM) and conductive bridge RAM (CBRAM)[5]. In the metal oxide-based RAM, the

oxygen vacancy in the switching layer can form a conductive filament (CF) when a sweeping or pulse voltage is applied onto top electrode (TE) and grounded bottom

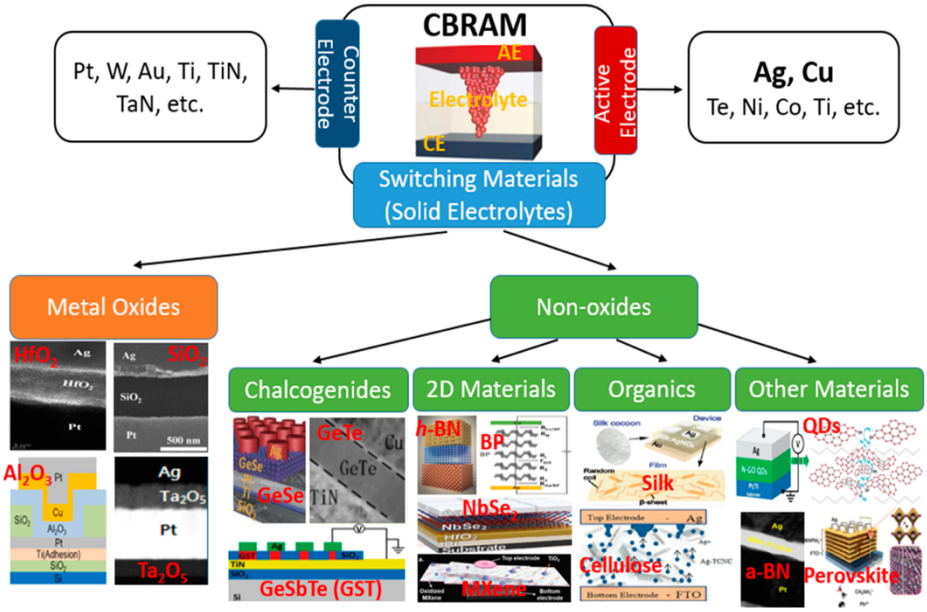

Figure 1.4 CBRAM cell with a detailed classification of the materials that are used for top electrode (TE, or active electrode, AE) and bottom electrode (BE, or counter electrode, CE), and switching medium in a CBRAM device.

electrode (BE) while for the CBRAM a metallic CN can be formed due to the mobile ions of TE or active electrode (AE) migrated into the layer sandwiched in between AE and counter electrode (CE).

Figure 1.4 shows the CBRAM cell with a detailed classification of the materials that are used for TE and BE and the different switching layers[5]. Various metal materials can be used as TE and BE. For the TE, it is usually deposited on the switching layer with electrochemically active metal, such as Ag, Cu, and Ti while the BE is typically inert metals and do not diffuse easily into the switching layer, such as Pt, Au, and W. Wide range of materials can be used as switching layer in the two-terminal MIM structure of CBRAM cell. They are categorized into metal oxides and non-oxides. In the non-oxides based CBRAM, two dimensional materials (2DMs) have attracted many attentions due to their

excellent electronic properties, especially the insulating hexagonal boron nitride (h-BN) for non-volatile memory applications.

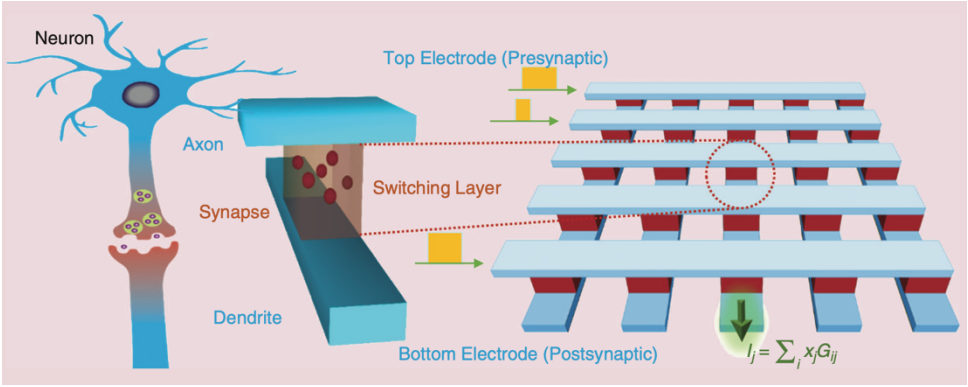

Figure 1.5 An illustration of the similarities between biological neuron and memristor-based artificial synapses and neural networks.

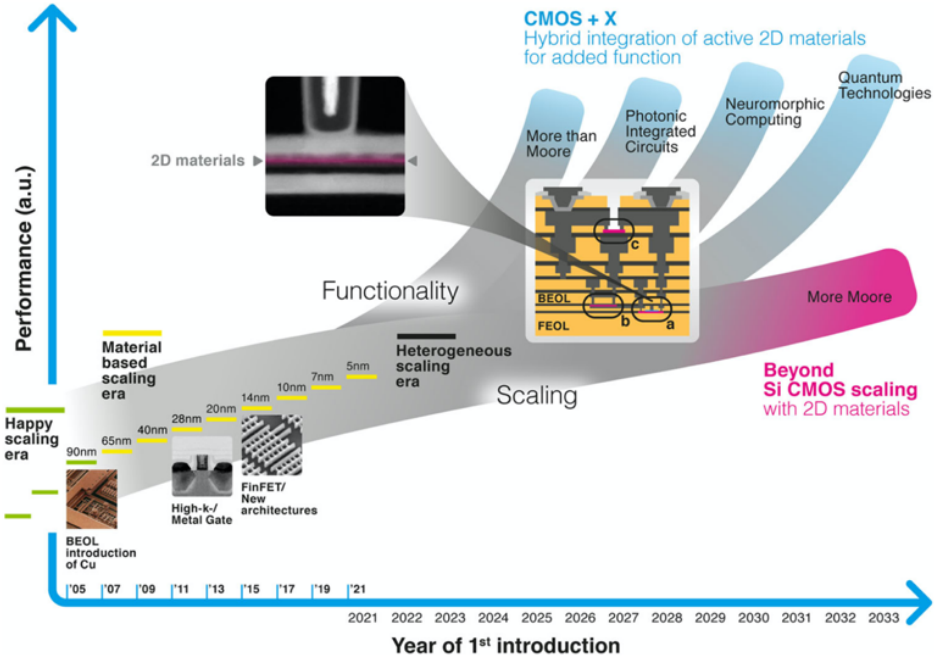

Figure 1.6 The era of geometrical scaling of silicon technology ended around the turn of the century.

To solve those issues mentioned above, one proposed solution is the neuromorphic computing with 2DMs based RRAM (2D-RRAM). There is many research exploring the neuromorphic computing system, which emulates the biological nervous system to endow

the man-made chips working in the same way as human brain. Figure 1.5 shows an illustration of the similarities between biological neuron and memristor-based artificial synapses and neural networks[6]. The two-terminal device resembles a synapse in biological neural systems, as you can see in the Figure 1.5, where the TE and BE act as axon and dendrite that connect pre-neuron and post-neuron with the conductance of the switching layer in the middle playing the role of the weight of a synapse. The crossbar structure also enables the implementation of physical mapping of the neural network in hardware and executive the parallel matrix operations directly in memory[6].

Figure 1.6 shows the co-integration of 2DMs with silicon CMOS technology. This will lead to a vast increase in chip functionality and enable the arrival of 2DMs applications in the order of their device complexity[7]. 2DMs enable further scaling of CMOS technology beyond the limits of silicon (More Moore) and memristors based on 2DMs also allow new paradigms like neuromorphic computing application (More than Moore). Therefore, neuromorphic computing based on 2D-RRAM offers a new route towards ultra-efficient computing.

Motivation for Studying 2DMs and Neuromorphic Computing

2DMs have attracted many attentions for next-generation electronic devices, optoelectronics, flexible electronics, and bioelectronics due to their unique electronic, optical, and mechanical properties[8–12]. Graphene exhibits extremely high carrier mobilities over 100,000 $cm^2V^{-1}S^{-1}$ owing to its Dirac-like linear dispersion[13–16]. Two-dimensional layered transition metal dichalcogenides (TMDs), such as MoS_2, $MoSe_2$, and WS_2, have attracted substantial attention for their use as semiconducting channel materials in switching devices[17–23]. Unlike graphene (semimetal) or TMDs (semiconductor), hexagonal

boron nitride (h-BN), which is a typical 2D-insulator material, has been used as dielectric layer material and nonvolatile switching layer in memristors due to its large band gap and outstanding thermal characteristics. Additionally, 2DMs are scalable and scalable. They can be fabricated devices with high density, as illustrated in Figure 1.7[24,25], which shows

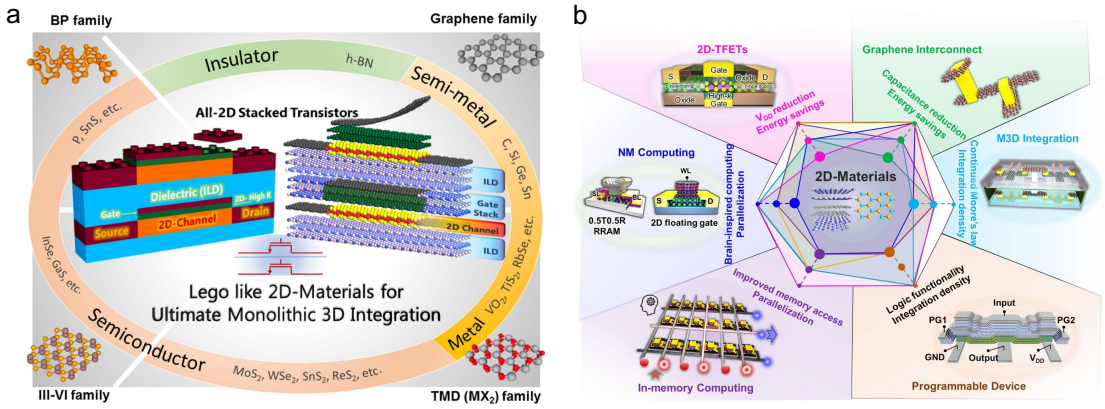

Figure 1.7 Different material properties and applications of 2DMs

the different electrical properties of different 2DMs and different applications, such as in-memory computing and neuromorphic computing.

Neuromorphic computing is the research that mimic the neural structure of human brain. Human brains consume much less energy than that of current computing system when complete a same task. Therefore, the neuromorphic computing system that emulate the working mechanism of human brains is much more energy-efficient. Neuromirphic computing promies an artificial intelligence (AI) revolution, such as self-driving cars, identifying individual's face, brain-machine interface, *et al*.

Current Status on 2DMs-based RRAM and 3D Vertical RRAM

Motivated by the high effectiveness of human brain, the AI and Internet of Things (IoTs) have been developed based on the imitation of the neural structure. Memristor crossbar is one of the important structures for neuro-inspired computing. Figure 1.8 shows some

typical research on status of memristors for memory and neuromorphic computing application. In Figure 1.8 (a-f), Pan, *et al* reported the mechanism of forming free bipolar and threshold resistive switching behavior in multilayer h-BN based memristor and developed some different strategies to tune the switching properties of the devices[26]. In Figure 1.8 (g-l), Shi, *et al*, characterized the conductive nanofilaments (CNFs) by using

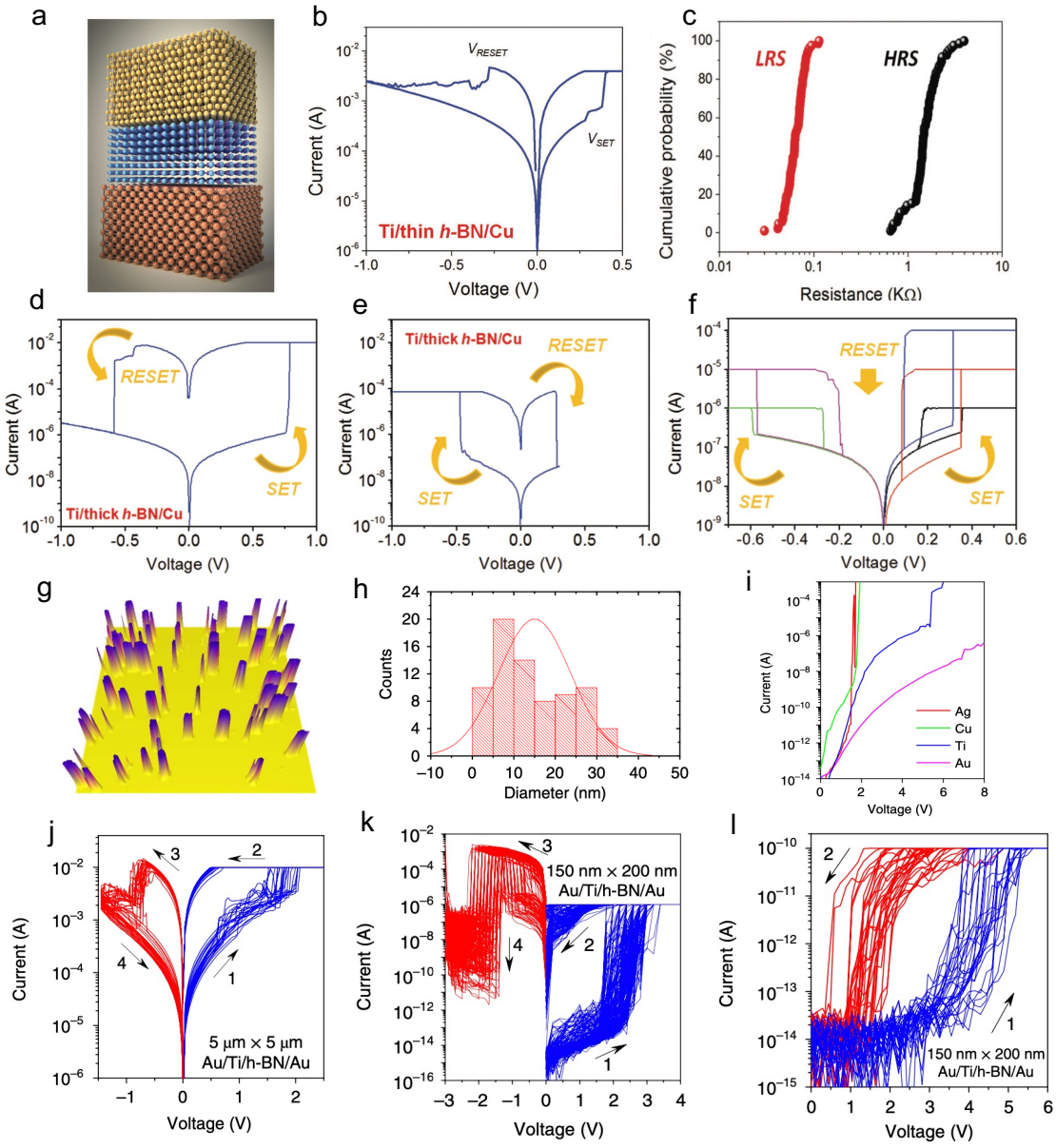

Figure 1.8 Current reearch on h-BN memristors for memory, in-memory computing and neuromorphic computing applications

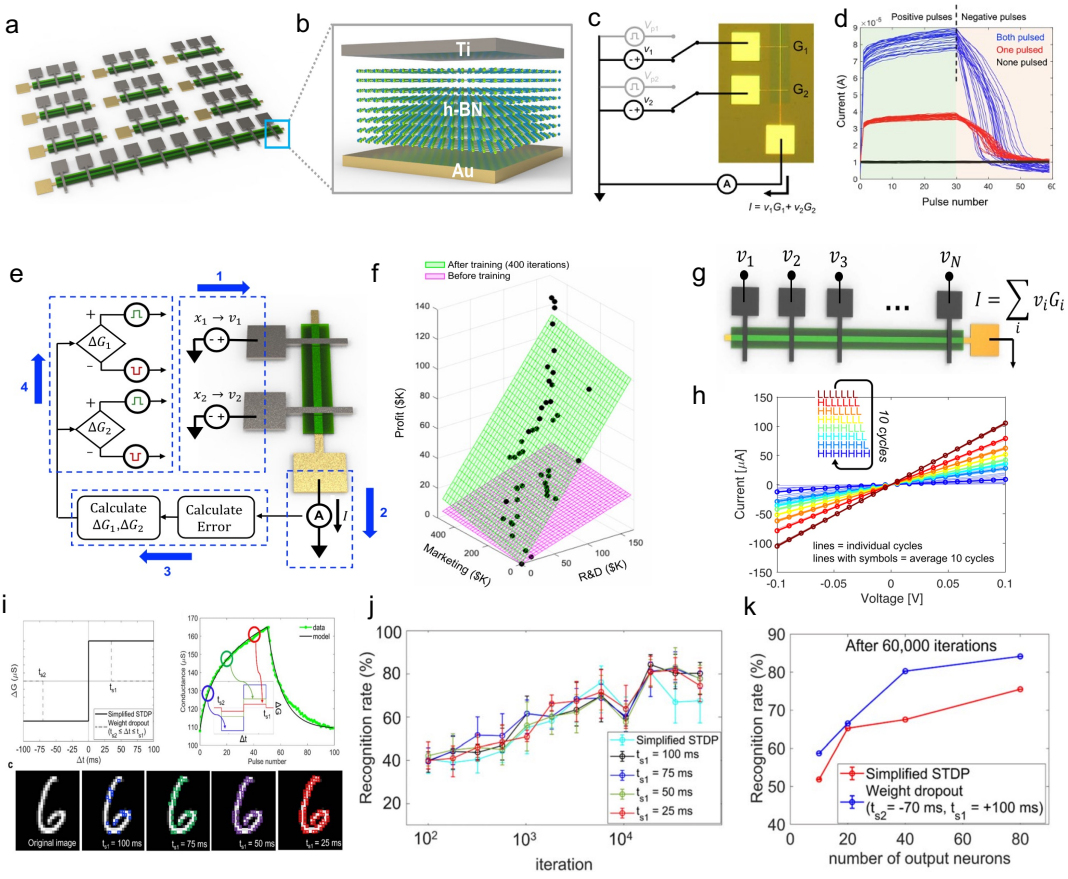

Figure 1.9 Current status of h-BN memristor crossbars for dot-product, linear regression, and logistic regression applications

conductive atomic force microscope (c-AFM) and investigated the resistive switching behavior with different metal filaments and different compliance currents to get either non-volatile or volatile switching behavior[27]. Later, based on the standalone memristor devices, more recent papers utilized these devices and constructed the crossbar structure and started to look more at the programming of the array levels and other important properties, such retention, and multi-states for machine learning and neuromorphic computing applications, as you can see in Figure 1.9, which presents parts of my research work in this dissertation. Figure 1.9 (a-d) shows the schematic of h-BN based memristor crossbars and the implementation of dot-product and linear regression with h-BN memristor crossbar. Figure

1.9 (g-h) shows the dot-product implementation in larger array (1x10) and demonstration of unsupervised spiking neural networks with h-BN memristor crossbars[28–30].

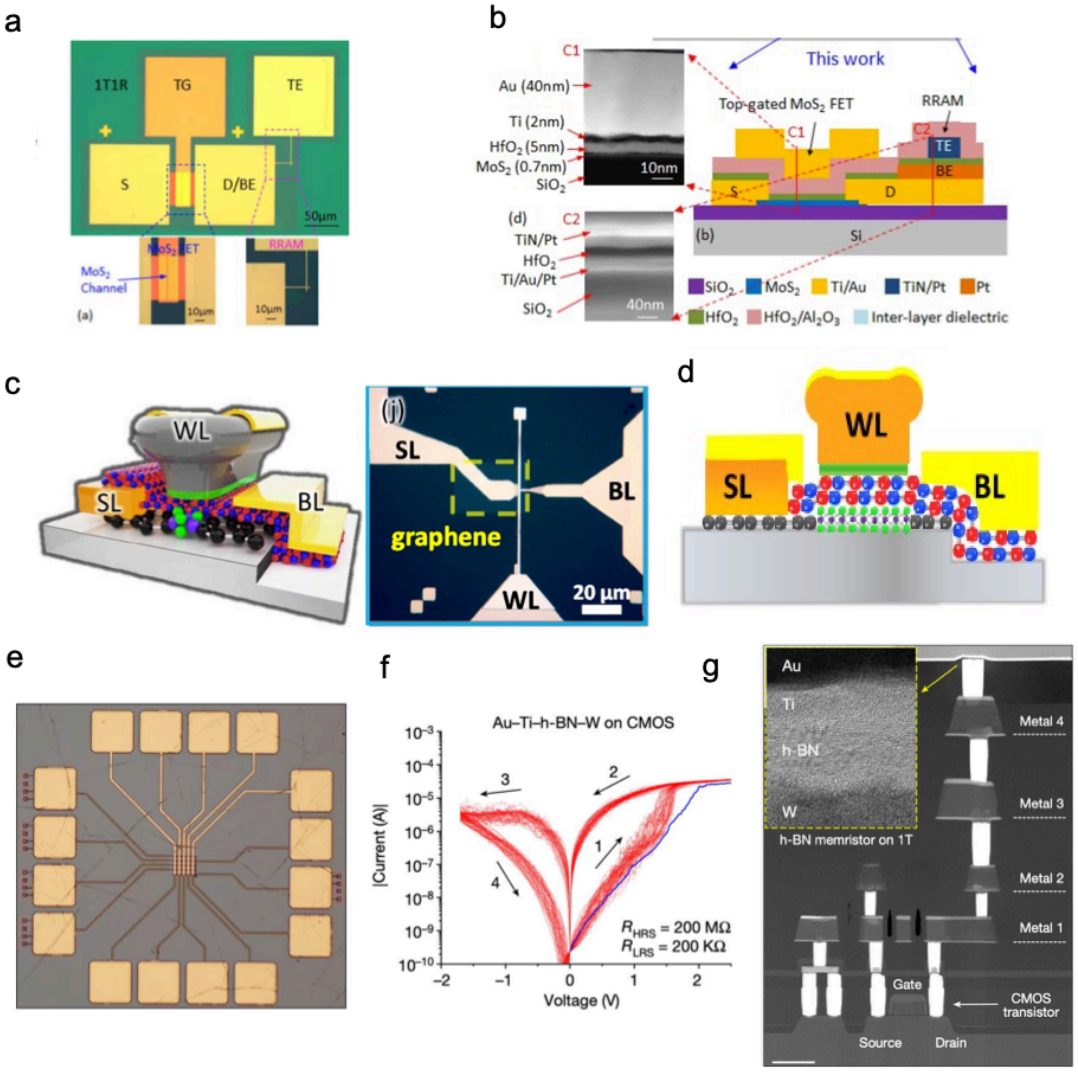

Figure 1.10 Recent research of 1T1R

Another important structure for the neuromorphic computing application is the 1T1R structure. It integrates one transistor with one memristor in series. The CMOS compatible 1T1R RRAM configuration has the capability to solve the sneak current issue in large-scale memristor crossbar array. Transistor in the combination not only plays the role of access controlling, also can use gate voltage to limit the current through pass the memristor.

In this case, it can also be used to tune the state of memristor by applying different gate voltage. Yang et al[31] used 2D MoS_2 transistor driving RRAMs with 1T1R configuration. The MoS_2 was utilized to construct the transistor channel region as well as the oxide based HfO_2 memristor was fabricated with transistor in series to build up the 1R1R structure, as illustrated in Figure 1.10 (a-b). It demonstrated the resistive switching performance of the 1R1R. Zhang *et al*[32] utilized the CVD-grown WS_2 was utilized to work as the channel region for the transistor part and the h-BN was used as the resistive switching layer of the memristor. The transistor and memristor were connected via the graphene layer. The hybrid device allows the device to be fabricated in a very small geometry. The conductance of the memristor performance was also well-controlled via the gate pulse applied to the WS_2 transistor to achieve multiple conductance states, as shown in Figure 1.10 (c-d). In 2023, Zhu *et al* transferred CVD-grown h-BN in the BEOL of commercial CMOS with 180 nm node at the fourth metal layer to fabricate 5 by 5 1T1M (one transistor one memristor), as show in Figure 1.10 (e-g)[33]. The memristors fabricated with CMOS transistors in series

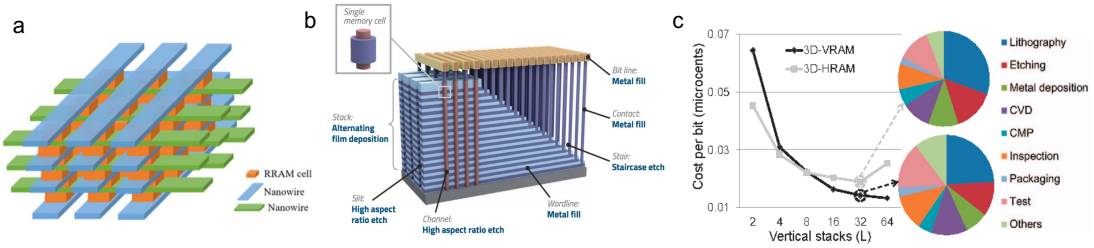

Figure 1.11 Two different 3D stacking of memristors and the cost-efficiency comparison.

show stable I-V performance for the simulation of spiking neural networks.

3D stacking of the memristors offers higher capacity, lower power consumption and cost per bit. Figure 1.11 shows two different 3D stacking structures of memristors and the comparison of cost-efficiency for two different 3D stacking structures[34,35]. One stacking

structure is called 3D horizontal structure (3D H-RRAM, as shown in Figure 1.11 a) and the other one is called 3D vertical stacking structure (3D V-RRAM, as shown in Figure 1.11 b). The memristor device area can be further reduced by stacking the memristor crossbars vertically to $4F^2/n$, where F is the minimum feature size, and n is the stacking layers. However, the cost-efficiency of these two different 3D stacking structures is different. The cost for H-RRAM increases linearly with the number of the stacked layer while the cost for V-RRAM is relatively independent of the stacking number, especially when the staking layer exceeds 32 layers, as shown in Figure 1.11 (c). Figure 1.12 shows some recent research about 3D stacking of V-RRAM with metal oxides as the switching layers. In 2014, Bai *et al* fabricated and characterized 3D vertical resistive switching memory with TaO_x as switching layer and platinum edge as the contact electrode[36]. The vertical cells show good uniformity and high performance with multi-level cell operation, as exhibited in Figure 1.12 (a-c). Later, Lee, *et al*[37], exploited the atomically thin graphene edge to assemble a resistive memory stacked in a vertical three-dimensional structure by using hafnium dioxide as the switching layer and compared the resistive switching behaviors of graphene-edge electrodes to that of the platinum electrodes, as shown in Figure 1.12 (d-i). Even though memristors with both electrodes show bipolar resistive switching behavior, the on/off ratio is small (only about two orders of magnitude). The most recent paper published in 2023 by Ren *et al*[38] reported the self-rectifying memristors based on the 3D stacking of Ta and SiO_2 as contact electrode and isolation layers respectively. TaO_2 and HfO_2 were utilized as switching layer and rectifying layer. The resistive switching behaviors are shown in Figure 1.12 (m-p). However, no work has been reported on 3D staking memristors based on h-BN.

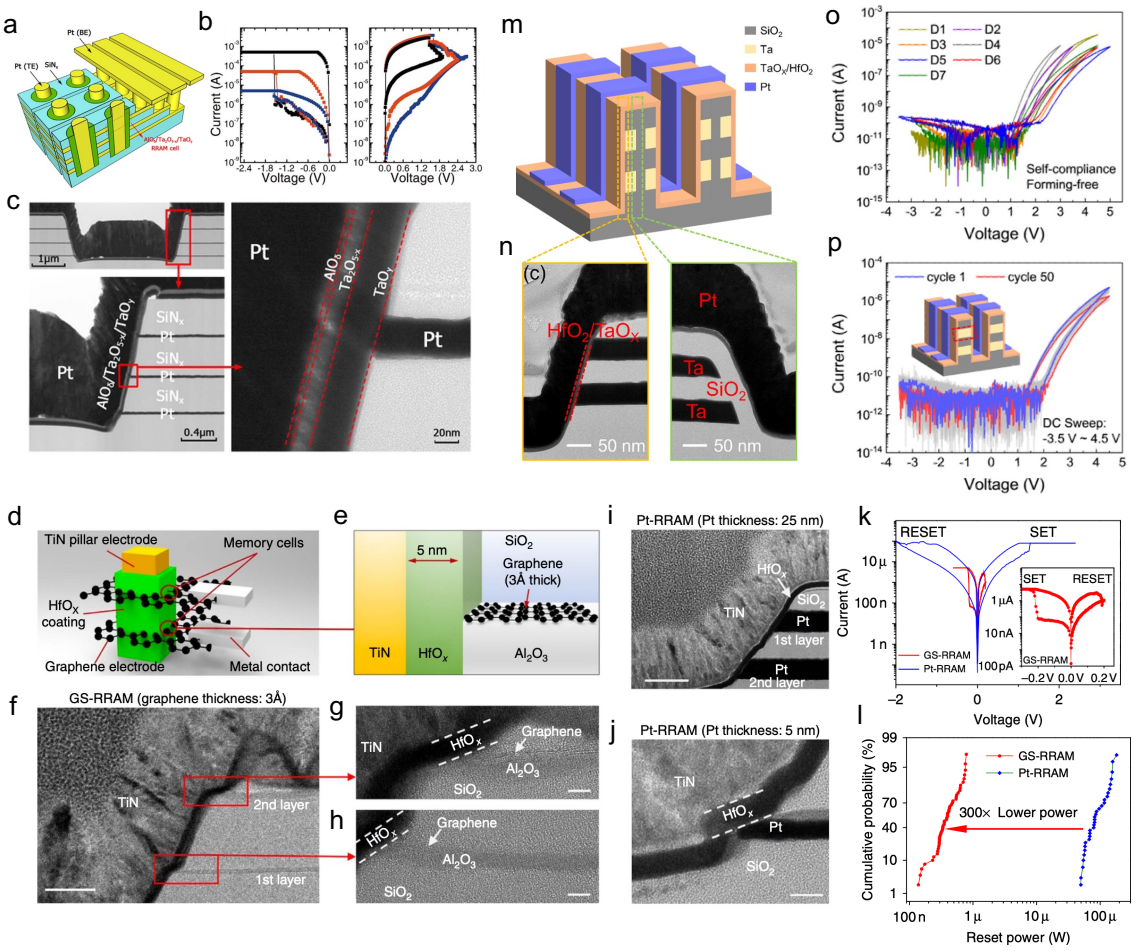

Figure 1.12 Some typical current research on 3D vertical RRAM

To investigate the resistive switching behavior in h-BN memristors with ultimate ultra-small active area, vertical h-BN memristors with graphene edge contact has been proposed as one chapter of my dissertation. Figure 1.13 (a) shows the proposed structure of vertical h-BN memristor with graphene-edge contact. The cross-sectional TEM image in Figure 1.13 (b) marks the interfaces for each component and the resistive switching behavior in Figure 1.13 (c) shows large on/off ratio about seven orders of magnitudes higher than metal oxide based vertical memristors with graphene or platinum contacts reported before. This work investigated the h-BN memristors with the smallest active area, providing new

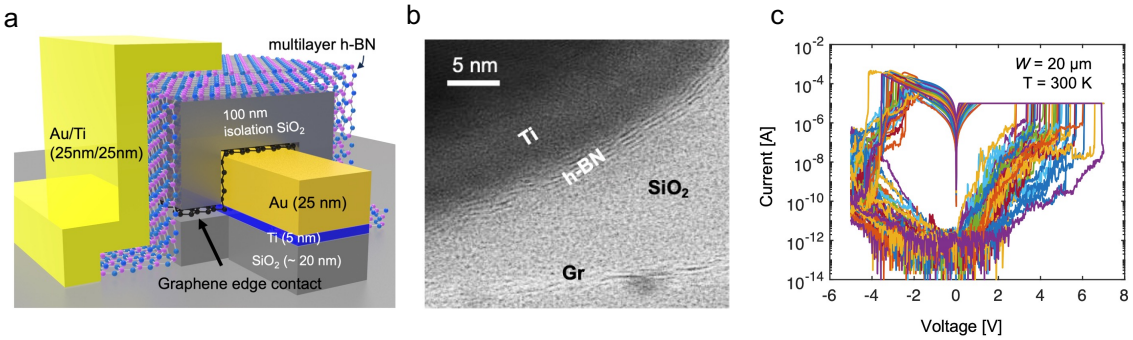

Figure 1.13 h-BN memristor with graphene-edge contact and the corresponding resistive switching behavior

opportunities for scaling down and 3D stacking of memristors. The results in Figure 1.13 will be discussed in Chapter 4 in detail.

CHAPTER 2

ANALYSIS OF SCHOTTKY BARRIER HEIGHT AND REDUCED FERMI-LEVEL PINNING IN MONOLAYER CVD-GROWN MoS_2 FIELD EFFECT TRANSISTORS

Introduction to 2DMs-based FETs

The emergence of graphene, transition metal dichalcogenides (TMD), black phosphorus, and other 2D materials has advanced basic research of monolayer (ML) crystals and has led to significant efforts towards their application in next-generation nanoscale electronic devices[21,39–45]. Molybdenum disulfide (MoS_2) is one of the most extensively studied TMD semiconductors for use as the active channel material in field-effect transistors (FETs). In addition to having a bandgap, MoS_2 provides unique properties to achieve good electrostatic control and charge transport in FETs at the scaling limit. MoS_2 FETs have been investigated using mechanically exfoliated flakes as well as CVD-grown thin films. Several studies with exfoliated MoS_2 flakes have discussed the significant role of metal contacts (i.e., the metal–semiconductor junction) on FETs operation and performance[46–50]. For example, Liu *et al* reported the properties of Ti contacts on exfoliated ML MoS_2 and discussed the importance of Schottky barriers in analyzing device performance[48]. Das *et al* studied the performance of FETs with different metal contacts on multilayered (e.g., 10 nm thick) exfoliated MoS_2 flakes[49]. They explained how the alignment of the Fermi level in the metal contacts with the bottom of the conduction band in the MoS_2 channel reduces the Schottky barrier height (SBH) enabling easier injection of carriers and improvements in on-state current. Moreover, the thickness-dependent and temperature-dependent transport properties in mechanically exfoliated ML and multilayer MoS_2 FETs were also explored extensively.[51–55]

Those studies based on exfoliated flakes have demonstrated the potential of MoS_2, but large-area methods for ML MoS_2 are needed for practical and scalable integrated technologies. Thus, CVD-grown MoS_2 coupled with conventional photolithographic patterning techniques must pave the way for more practical applications. Recently, Kwon *et al* pointed out the lack of reports for conventional photolithographic patterning of large-area ML MoS_2 and presented a study of CVD-grown ML MoS_2 FETs[56]. Similarly, Zhang *et al* synthesized and transferred CVD-grown MoS_2 to fabricate and study FETs as a function of number of layers in the MoS_2 channel[57]. In another recent study, Xu *et al* presented results on large arrays of CVD-grown MoS_2 top-gated FETs and compared two-probe versus four-probe measurements of transport parameters[58]. These studies presented statistical analysis of CVD-grown ML MoS_2 FET parameters with histograms of threshold voltage[56–58], mobility[57,58], and gate hysteresis[56], but did not analyze the effects of Schottky barriers at the contacts as done in previous studies of FETs with exfoliated MoS_2.

In this chapter, an examination of metal contacts on CVD-grown ML MoS_2 by electrical measurements of large FET arrays is present. Specially, two large FET arrays with different source/drain metal contacts (Cr/Au and Ti/Au) were fabricated (via large-area photolithography methods) and tested. SBH were extracted based on thermionic emission theory for 2D semiconductors using temperature dependent measurements. Statistically significant extractions reveal a reduction in SBH for CVD-grown ML MoS_2 compared to values extracted from FETs with exfoliated flakes. This reduction in SBH is attributed to an enhancement in the metallization of MoS_2 by hybridization between S and the metal atoms (e.g., Ti) compared to exfoliated flakes due to a larger number of defects in CVD-grown samples[48]. Moreover, the dependence of SBH (Φ_{SB}) on the metal work

function (Φ_M) indicates a reduction in Fermi level pinning (FLP) for CVD-grown samples compared to exfoliated ML MoS_2. The FLP factor ($S = |d(\Phi_{SB}) / d(\Phi_M)|$) extracted for CVD-grown samples ($S \cong 0.5$) is larger than those reported for exfoliated fakes ($S \cong 0.1$) and closer to the ideal Schottky-Mott limit ($S = 1$). Optical characterization (Raman spectroscopy) indicates a larger concentration of defects in our CVD-grown ML MoS_2 samples compared to exfoliated fakes supporting a defect-induced enhancement in the coupling between the electrodes and the channel consistent with our electrical analysis of SBH.

Method and Fabrication for CVD-grown Monolayer MoS_2

The fabrication of large-area ML MoS_2 FET arrays is illustrated in Figure 2.1. Because of weak van der Waals (vdW) interaction between the substrate and the 2D material monolayer, a strategy is needed to prevent the monolayer from peeling off, which is typically caused by a stronger cross-linking interaction between photoresist and 2D materials after the post-exposure bake in the lithography process. For example, Theofanopoulos *et al* utilized a 30 nm titanium film as sacrificial layer to protect graphene from peeling off during fabrication of devices[59]. In this work a PMMA sacrificial layer was utilized to prevent peeling of the 2D material monolayer during photolithography processing. A 1 cm-by-1 cm CVD-grown ML MoS_2 on 300 nm SiO_2/Si (Figure 2.1(a)) was ordered from SixCarbon Technology (Shenzhen) and processed directly on the original substrate. A thin PMMA layer (5000 rpm for 30 s; 100 °C for 1 min) and negative photoresist (LOR3A, 5000 rpm for 30 s, 180 °C for 2 min; AZ5214, 4000 rpm for 30 s, 95 °C for 90 s) were spun coat on top. Then, the photomask for patterning the channel regions and aligners were positioned over the substrate. After UV light exposure and post-

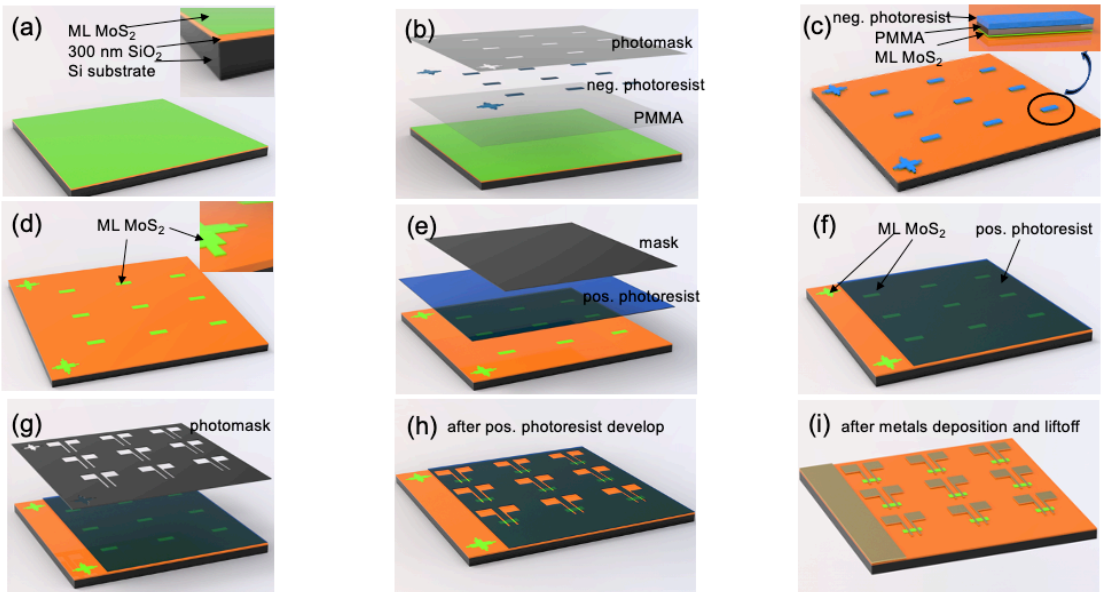

Figure 2.1 Fabrication process of CVD-grown monolayer MoS_2 FETs

exposure bake (50 mJ cm^{-2}, 115 °C for 60 s; flood exposure: 150 mJ cm^{-2}, no bake) the negative photoresist was developed by 300MIF for 1min. After developing, the photomask pattern was transferred into the negative photoresist as shown in Figure 2.1(b). Dry etching was then used to remove the unmasked regions (SF6: 20 sccm, Ar: 5 sccm, 10 mTorr, 75 W for 2 min), as shown in Figure 2.1(c). Next, the negative photoresist and PMMA were removed by Remover PG at 80 °C exposing pristine ML MoS_2 patterns as illustrated in Figure 2.1(d). Subsequently, positive photoresist (LOR3A, 5000 rpm for 30 s, 180 °C for 2 min; AZ3312, 5000 rpm for 30 s, 100 °C for 60 s) was spun coat on the patterned ML MoS_2, and a second photomask was used on the MoS_2 channel regions. After exposure and post-exposure bake (30 mJ cm^{-2}, 110 °C for 60 s), the positive photoresist was developed by 300MIF for 1 min to expose the ML MoS_2 aligners (Figure 2.1(f)). These were then used for the alignment of the source and drain metal contacts (Figure 2.1(g)). After exposure, bake, and develop, the source/drain metal contacts (5 nm Cr/35 nm Au or 5 nm Ti/35 nm Au) were deposited via electron beam evaporation (Figure 2.1(h)). Finally, the

liftoff process was performed in Remover PG at 80 °C. The final image of the fabricated CVD-grown ML MoS_2 FETs array is shown in Figure 2.1(i).

Result and Discussion for CVD-grown Monolayer MoS_2

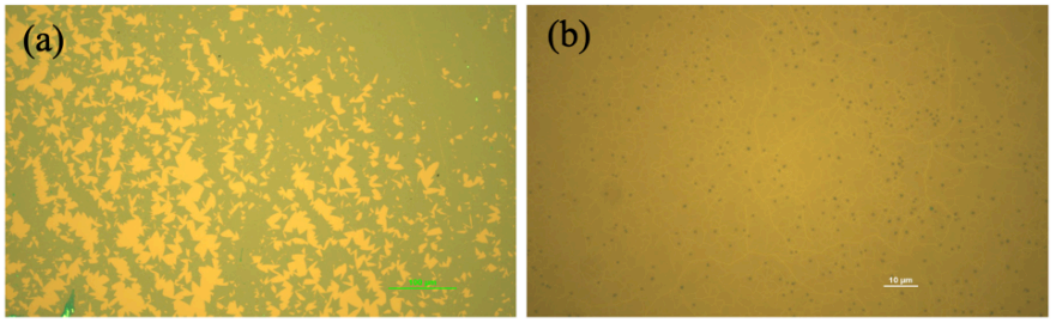

Figure 2.2 Optical images of the CVD-grown MoS_2 monolayer film. (a) Image of region near edge of the sample reveals large isolated MoS_2 monolayer grains. (b) Image of region near the middle of the sample shows uniform MoS_2 monolayer film.

Two separate arrays of ML MoS_2 FETs, each with different type of metal contacts, were fabricated and tested. The starting material is a continuous CVD-grown ML MoS_2 film, as shown in Figure 2.2 (b). Optical images near the edges of the sample reveal large crystal grains as shown in Figure 2.2(a) and Figure 2.3 (a). The AFM image of an MoS_2 crystal grain and the step height measurement are shown in Figure 2.3(b) and (c). A picture of the full FET array sample is shown in Figure 2.3(d), and a micrograph of a single MoS_2 FET is shown in Figure 2.3(e) and (f) (closer view of the FET channel region). To verify the quality and the number of MoS_2 layers, Raman spectroscopy in the channel region of five randomly selected fully fabricated FETs is conducted. Figure 2.3(g) plots the Raman spectra where the first and second peaks, centered at 385 cm^{-1} and 405 cm^{-1} respectively, correspond to the two E_{2g}^1 and A_{1g}modes, which have been demonstrated to be sensitive to the number of MoS_2 layers[60–62]. A difference in the peak positions of ~20 cm^{-1} confirms the monolayer MoS_2 channels. An AFM image of the FET and height measurement across

the channel region are shown in Figure 2.3(h) and (i) where the step observed in height includes the MoS_2 ML thickness as well as etching into the SiO_2 substrate.

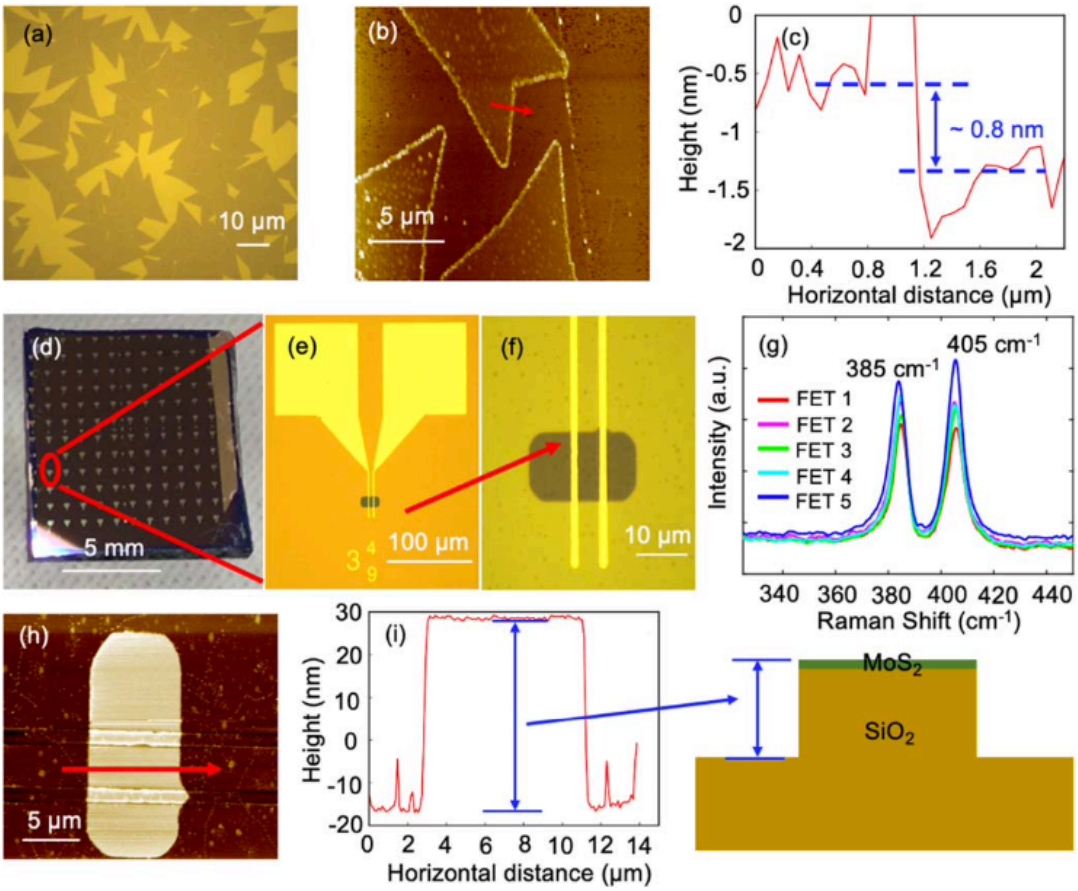

Figure 2.3 (a) Optical image of the CVD-grown MoS_2 film (image shows edge of mostly uniform film). (b) Atomic force microscopy (AFM) image of CVD-grown MoS_2 film. (c) Line scan on AFM image revels the step height on the CVD-grown MoS_2 film. (d) Picture of one sample showing the large array of MoS_2 FETs. (e) Micrograph of an MoS_2 FET. (f) Higher magnification image of the MoS_2 device. (g) Raman spectrum from the channel region of five different FETs selected randomly. (h) AFM image of the fabricated ML MoS_2 FETs. (i) AFM heigh profile across the channel region of the MoS_2 FET (step includes etching of SiO_2 as illustrated by the schematic).

The fabricated arrays include FETs with various channel widths (W) and lengths (L). Typical drain current (I_d) versus gate voltage (V_g) characteristics measured at different temperatures are shown in Figure 2.4(a) and (b) for FETs with Cr/ Au and Ti/Au contacts respectively (more I_d-V_g measurements at different temperatures are shown in Figure 2.5).

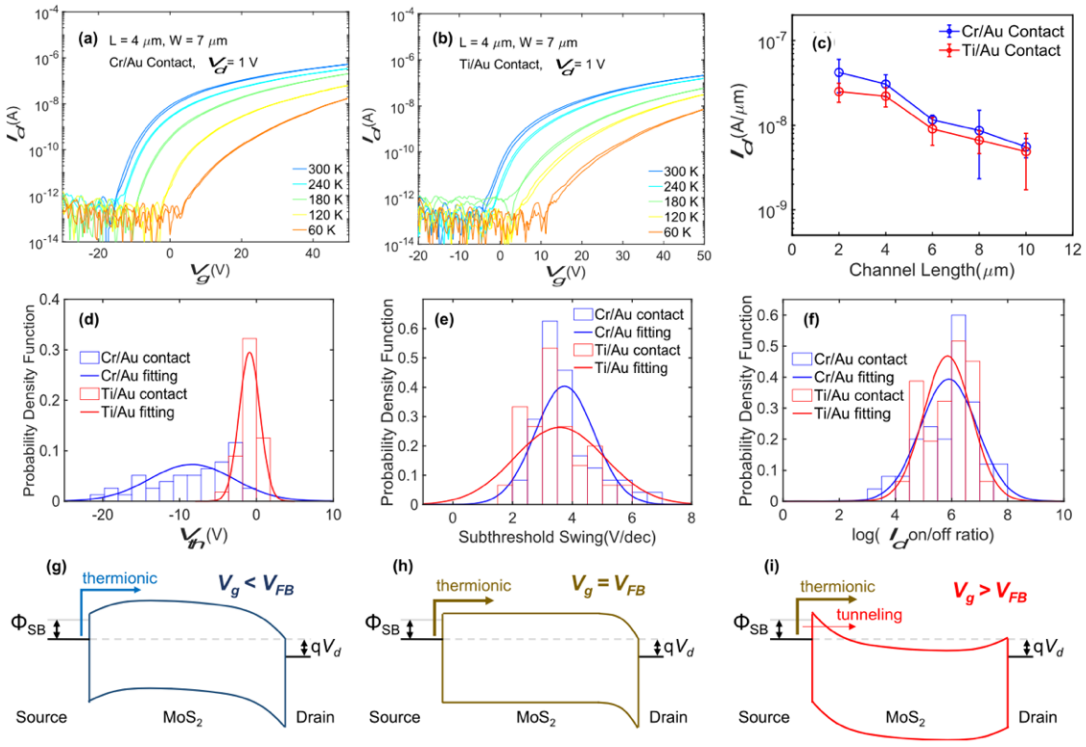

Figure 2.4 Transfer characteristics at different temperatures for CVD-grown ML MoS_2 FETs with (a) Cr/Au contacts and (b) Ti/Au contacts (both devices have channel width W = 7 μm and length L = 4 μm). (c) L-dependence of current for Cr/Au and Ti/Au FETs (symbols are mean, error bars are standard deviation from over 100 devices tested). (d)–(f) Histograms of threshold voltage, subthreshold swing, and on/ off ratio for both Cr/Au and Ti/Au FETs at room temperature and V_d = 1 V (over 100 devices tested). (g)–(i) Energy band diagram for the MoS_2 FETs for different biasing conditions.

Dual V_g sweeps show negligible hysteresis at all temperatures indicating minor contribution from near interfacial traps and adsorbates on the surface of the MoS_2 channel[63–66] (samples were annealed in situ at 375 K under high vacuum ~3E-7 Torr for 24 h, see Figure 2.6). For the range of V_g in Figure 2.4(a) and (b), I_d goes down with decreasing temperature consistent with charge transport limited by thermionic emission over the Schottky barriers at the interface between metal contacts and the MoS_2 channel. In Figure 2.4(c) it plots I_d at V_g = 50 V (normalized by W) as a function of L for both Cr/Au and Ti/Au FETs. These results shown correspond to mean values (symbols) and standard

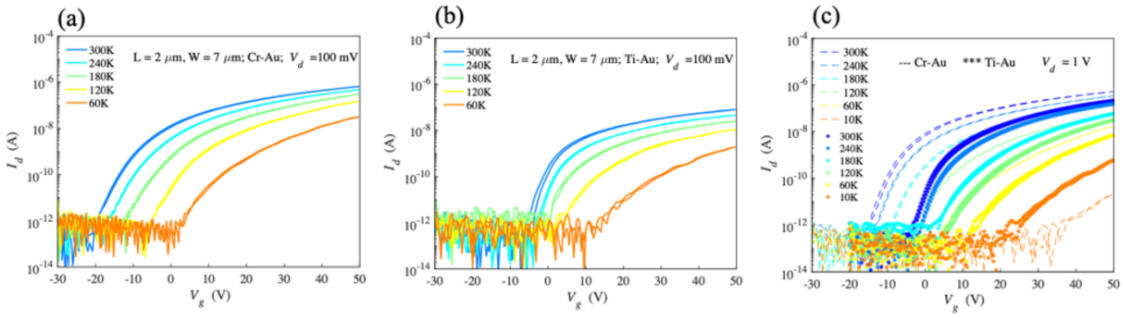

Figure 2.5 I_d-V_g characteristics measured at different temperatures using V_d = 100 mV for FETs with (a) Cr/Au and (b) Ti/Au contacts. (c) Comparison of I-V measurements from FETs with Cr/Au and Ti/Au contacts at different temperatures.

deviation (error bars) from over 20 FETs tested for each L (>100 FETs tested overall). It is worth noting that except for a few devices that failed during liftoff in the fabrication process, over 80% of the devices showed good field-effect characteristics (I_d-V_d characteristics were also verified, see Figure 2.7 and Figure 2.8). Further statistical analysis is provided with histograms of important FET electrical parameters for both Cr/Au and Ti/Au devices. These include threshold voltage (Figure 2.4(d)), subthreshold swing (Figure 2.4(e)), and on/off ratio (Figure 2.4(f)). Similar distributions of the parameters are observed for Cr/Au and Ti/Au samples, except for a wider distribution of threshold voltages (Vth) in Cr/Au devices. This may be attributed to variation in fixed oxide charge. The Cr/Au and Ti/Au FET arrays were fabricated on different CVD-grown samples on Si/SiO_2 wafers with different distributions of oxide charge. For back-gated FETs with thick SiO_2 gate oxides (300 nm in this case) small changes in fixed oxide charge can lead to large threshold shifts (e.g., a difference of ~7×10^{11} cm^{-2} can result in ~10 V shift in threshold voltage). The large values for subthreshold swing (SS) are also due to a having a thick gate dielectric. It is well established in the literature that to achieve a near-ideal SS of 60 mV/dec the effective oxide thickness (EOT) must be scaled down to a few nanometers[67].

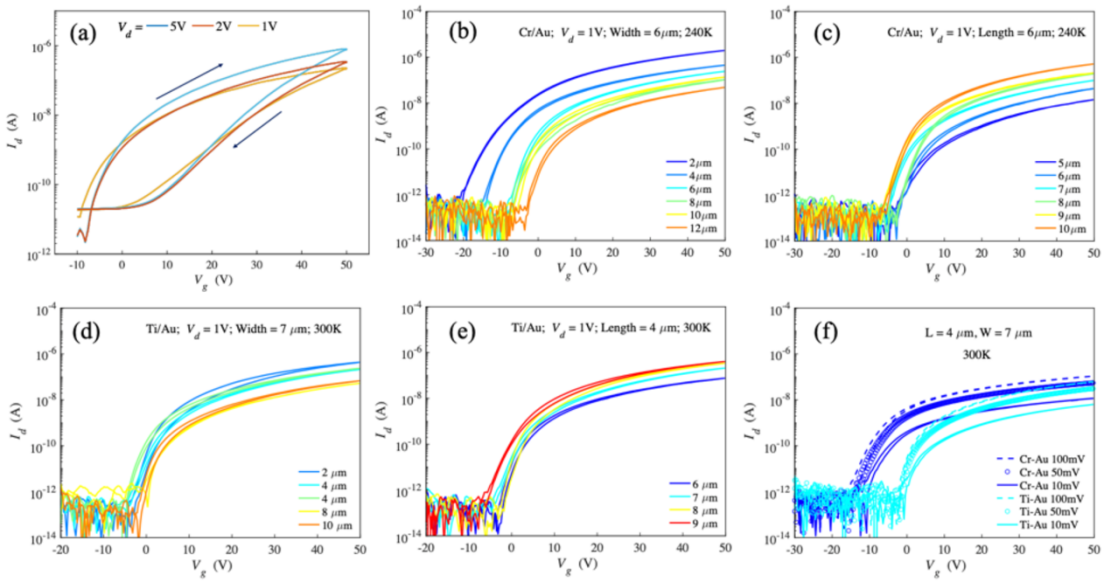

Figure 2.6 (a) I_d-V_g characteristics (dual gate voltage sweep) before in-situ anneal show large hysteresis. After in- situ annealing the gate hysteresis is successfully eliminated, significantly improving the measured I-V characteristics. (b) and (c) are I_d-V_g measurements after in-situ anneal for FETs with Cr/Au contacts and with different channel lengths and widths. (d) and (e) are I_d-V_g measurements after in-situ anneal for FETs with Ti/Au contacts and with different channel lengths and widths. (f) Comparison of typical I_d-V_g characteristics of FETs with Cr/Au vs. Ti/Au contacts at different drain voltages.

The energy band diagrams in Figure 2.4 (g-i) illustrate the charge transport mechanisms of Schottky-barrier MOSFETs (SB-MOSFETs) similar to the MoS_2 devices reported in this work. The band diagrams are shown for a positive drain-to-source voltage (V_{ds}) and correspond respectively to biasing conditions with V_g below the flat band voltage (V_{FB}), $V_g = V_{FB}$, and $V_g > V_{FB}$. For $V_g < V_{FB}$ a large (wide) energy barrier between the contacts and the channel limits the injection of carriers to thermionic emission processes. As V_g increases towards V_{FB}, the energy bands in the channel are pulled down in energy reducing the barrier height for electron injection from the source into the channel. At the flat band condition ($V_g = V_{FB}$) the energy barrier height for electron injection from source to channel is equivalent to the Schottky barrier (labeled as Φ_{SB}). Further increase in V_g will not change

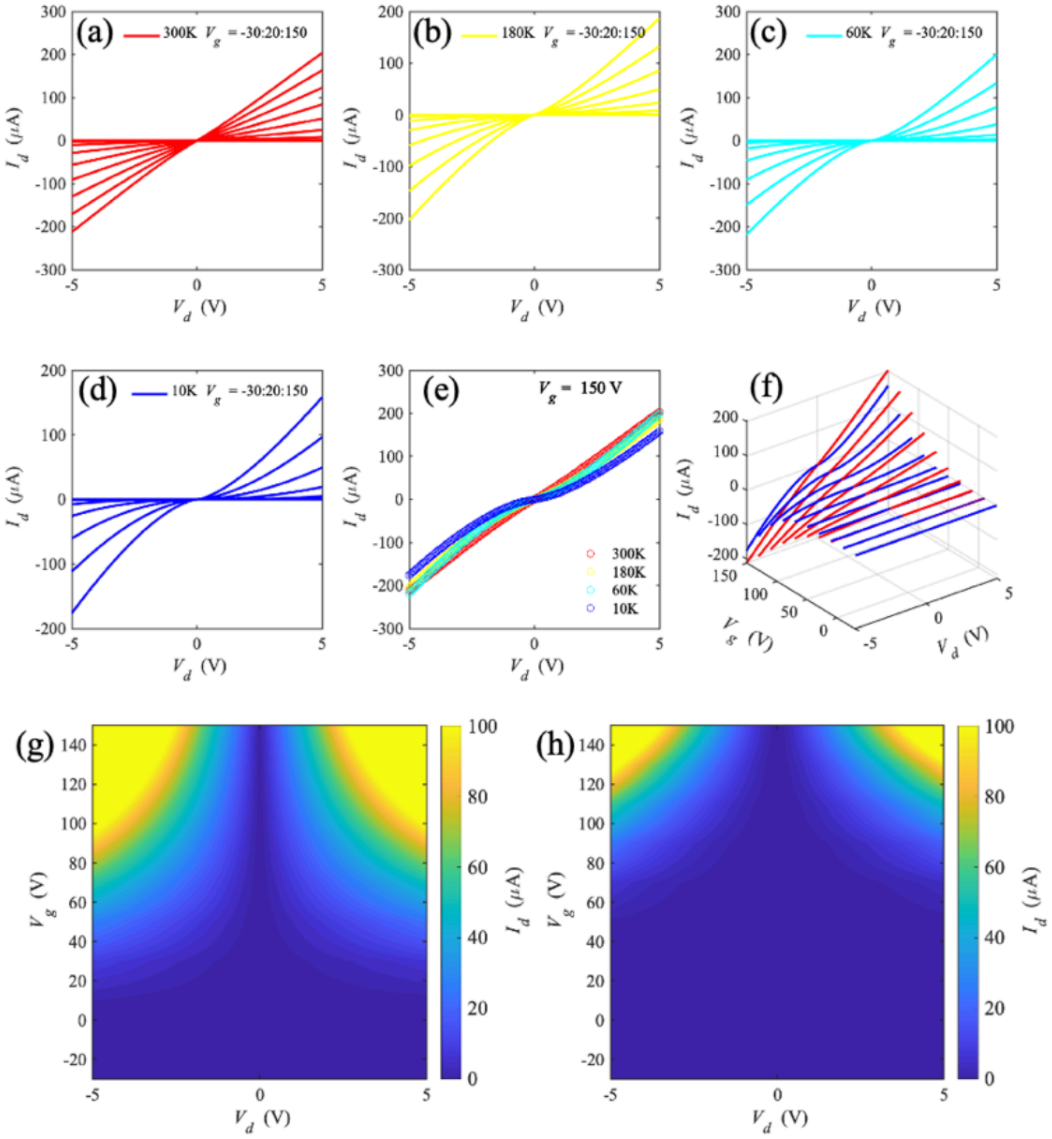

Figure 2.7 I_d-V_d characteristics for FETs with Cr/Au contacts for various V_g ranging from -30 to 150 V and at different temperatures: (a) 300 K, (b) 180 K, (c) 60 K, (d) 10 K. (e) I_d-V_d characteristics at V_g = 150 V for all four different temperatures. (f) Three-dimensional (3-D) I_d-V_d plot for various V_g comparing 300 K (solid red lines) and 10 K (solid blue lines). (g) and (h) are contours plot of I_d as a function of V_g and V_d for temperatures of 300 K and 10 K respectively.

the Schottky barrier height. However, as V_g increases above V_{FB} the barrier becomes triangular its width decreases with increasing V_g. As a result, thermally assisted tunneling of electrons through the barrier sets in for $V_g > V_{FB}$. In a device with good electrostatics,

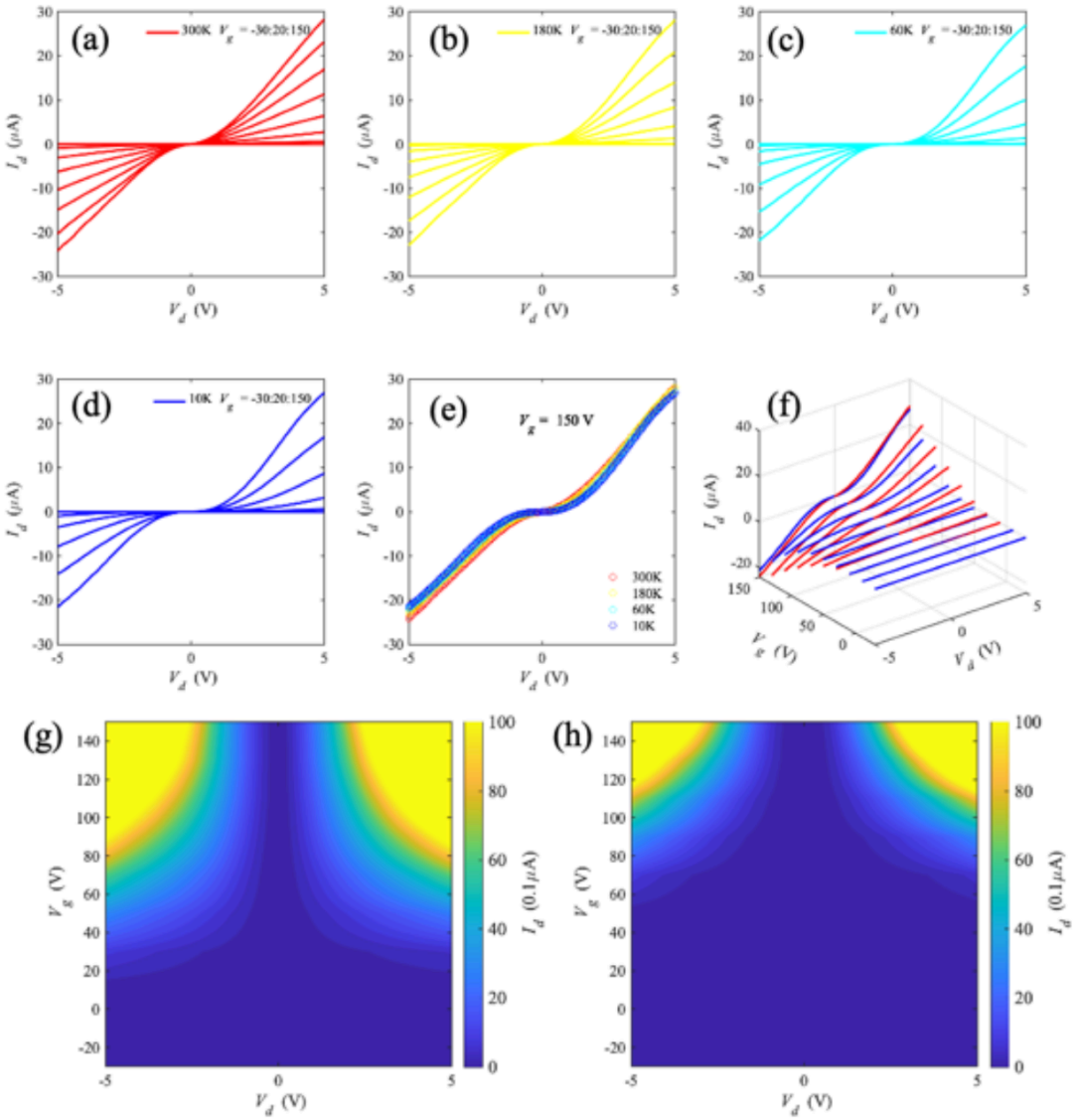

Figure 2.8 I_d-V_d characteristics for FETs with Ti/Au contacts for various V_g at different temperatures: (a-d) 300 K to 10 K. (e) I_d-V_d characteristics at V_g = 150 V for all four different temperatures. (f) Three-dimensional (3-D) I_d-V_d plot for various V_g comparing 300 K (solid red lines) and 10 K (solid blue lines). (g) and (h) are contours plot of I_d as a function of V_g and V_d for temperatures of 300 K and 10 K respectively.

increasing V_g significantly above V_{FB} would result in narrow Schottky barriers that would allow efficient electron tunneling. As explained by Illarionov *et al*[67], strongly scaled insulators enhance gate control over the channel, thereby reducing the impact of the Schottky barriers. When this is true, the limiting charge transport mechanism becomes the

scattering effects in the channel rather than thermionic emission at the contacts. When current flow is limited by charge scattering in the channel, the FET mobility can be extracted to characterize the transport properties and quality of the MoS_2 channel. The devices studied in this work do not have strongly scaled insulators (these are back-gated FETs with 300 nm SiO_2 gate dielectrics) so the limiting transport mechanism must be verified.

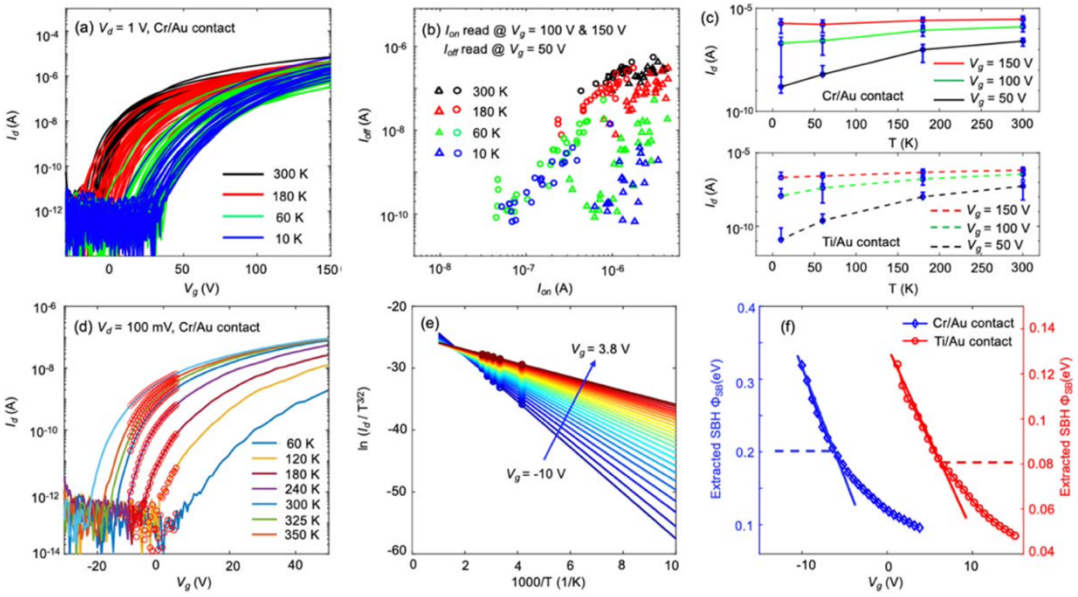

Figure 2.9 (a) Transfer characteristics for the ML MoS_2 FETs with Cr/Au contacts for V_d = 1 V and for different temperatures. (b) Scattered plot for I_{off} (I_d at V_g = 50 V) versus I_{on} (circles: I_d at V_g = 100 V; triangles: I_d at V_g = 150 V). (c) Drain current as a function of temperature for various V_g (circles are mean values, error bars are standard deviations). (d) Example of transfer characteristics used to extract barrier height. (e) Arrhenius plot for extraction of barrier height; (f) barrier height versus V_g, and extractions of Schottky barrier height (dashed lines) for FETs with Cr/Au (diamonds) and Ti/Au (circles) contacts.

To better investigate the transport properties in the MoS_2 FETs a subset of the samples was remeasured at different temperatures and sweeping V_g to higher voltages. Figure 2.9(a) plots the transfer characteristics for several FETs with Cr/Au contacts at different temperatures ranging from 10 K up to 300 K and V_g swept up to 150 V (similar results for

FETs with Ti/Au contacts are shown in Figure 2.10). For a fixed V_g, the temperature dependence of I_d is a good indicator of the limiting charge transport mechanism[68]. I_d increasing with temperature is indicative of thermionic emission (dominated by the contacts), while I_d decreasing with temperature is indicative of scattering (dominated by the channel). Figure 2.9(b) and (c) take a closer look at the statistics of I_d temperature dependence. Figure 2.9(b) plots the scattered data of I_{off} (I_d at V_g = 50 V) versus I_{on} (I_d at V_g = 100 V) for each temperature (circles). The scattered data shows more overlap in I_{on} compared to I_{off} between the different temperatures. The overlap is more pronounced when plotting the case of I_{on} corresponding to V_g = 150 V (triangles). The same trend can be observed by plotting drain current as a function of temperature for different V_g as shown in Figure 2.9(c). The top panel is for FETs with Cr/Au contacts, and the bottom panel is for FETs with Ti/Au contacts. At the lower gate voltages I_d clearly increases with temperature (i.e., consistent with thermal activation of carriers). As V_g increases the dependence of I_d begins to transition, but even at V_g = 150 V a full transition cannot be seen (I_d does not decrease with temperature). Hence, for back-gated FETs with thick gate oxides the gate control over the channel is not sufficient to render the Schottky barriers negligible. Therefore, extractions of mobility are not useful as the transport properties of the FETs are affected by the contacts even for large V_g. Instead, this work focuses on the properties of the Schottky barriers and metal contacts to the CVD-grown monolayer MoS_2 and compare these to exfoliated MoS_2.

A statistical analysis of Schottky barrier height (SBH) from the off-state measurements (e.g., for V_g < 50 V) is performed. Previous works on exfoliated MoS_2[48,49,69] (both monolayer and multilayer) as well as a study on CVD-grown multilayer MoS_2[70] have

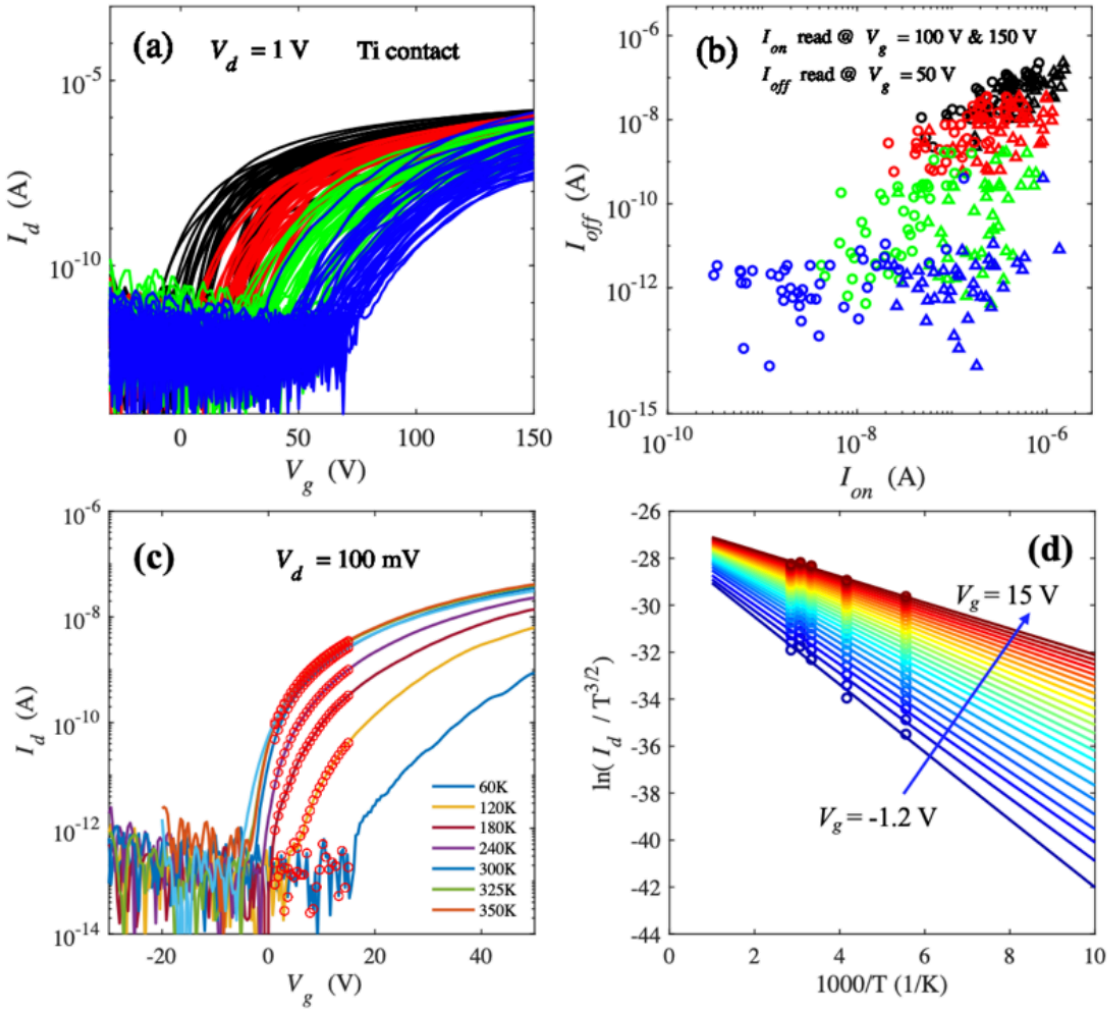

Figure 2.10 (a) Transfer characteristics for the ML MoS_2 FETs with Ti/Au contacts for V_d = 1 V and for different temperatures (300 K, 180K, 60K, 10K). (b) Scattered plot for I_{off} (I_d at V_g = 50 V) vs. I_{on} (circles: I_d at V_g = 100 V; triangles: I_d at V_g = 150 V). (c) Example of transfer characteristics used to extract barrier height. (d) Arrhenius plot for extraction of barrier height at different V_g.

reported on the extractions of SBH, but to the best of our knowledge no reports have been published on the statistics of SBH from CVD-grown ML MoS_2 devices. Since density of states, crystallinity, surface roughness, defect density, and other physical properties are different between exfoliated and CVD-grown MoS_2[57,68,71,72], it is important to analyze the statistics of SBH at the interface between metal contacts (Cr and Ti in this paper) and ML

CVD-grown MoS_2. From thermionic emission theory for 2D semiconductors the (reverse-bias) Schottky junction current is given by

$$I = WA_{2D}T^{3/2}\exp(-q\Phi_{SB}/k_BT)$$

where W is the channel width, q is the electron charge, k_B is the Boltzmann constant, Φ_{SB} is the Schottky barrier height, $A_{2D} = q(8\pi k_B^3 m^*)^{1/2}/h^2$ is the Richardson's constant for 2D[47,48,73]. For a fixed V_g, I_d at different temperatures is extracted, as shown in Figure 2.9(d) and construct an Arrhenius plot like the one shown in Figure 2.9(e). Using the thermionic emission current equation, this work extracts barrier height as a function of V_g from the slope of the Arrhenius plot. The SBH (Φ_{SB}) corresponds to the barrier extracted at the flat band condition, which can be identified from the plot of extracted barrier height as a function of V_g (Figure 2.9(f)) as the point where the extraction deviates from a linear dependence. In Figure 2.9(f) it shows examples of extracted SBHs for MoS_2 FETs with Cr/Au and Ti/Au contacts (more examples of SBH extractions are shown in Figure 2.12 and Figure 2.13). The extracted SBH is approximately 0.2 eV for the Cr/Au device and 0.08 eV for Ti/Au (statistics in Figure 2.11).

Figure 2.11(a) plots histograms of extracted SBHs for Cr/Au and Ti/Au devices. The mean and standard deviation of SBH extracted on ML MoS_2 FETs with Cr/Au contacts were respectively μ_{Cr} = 0.19 eV and σ_{Cr}= 0.05, while for FETs with Ti/Au contacts μ_{Ti} = 0.09 eV and σ_{Ti} = 0.02. The extracted SBH for Cr contact is higher than that of Ti contact due to the larger work function of Cr. The extracted SBH for CVD-grown ML MoS_2 FETs with Ti/Au contacts in this paper is smaller than those of exfoliated ML MoS_2 FETs reported earlier[48,74]. A possible explanation is enhancement in metallization of MoS_2 resulting from hybridization between S and the metal atoms (e.g., Ti) compared to

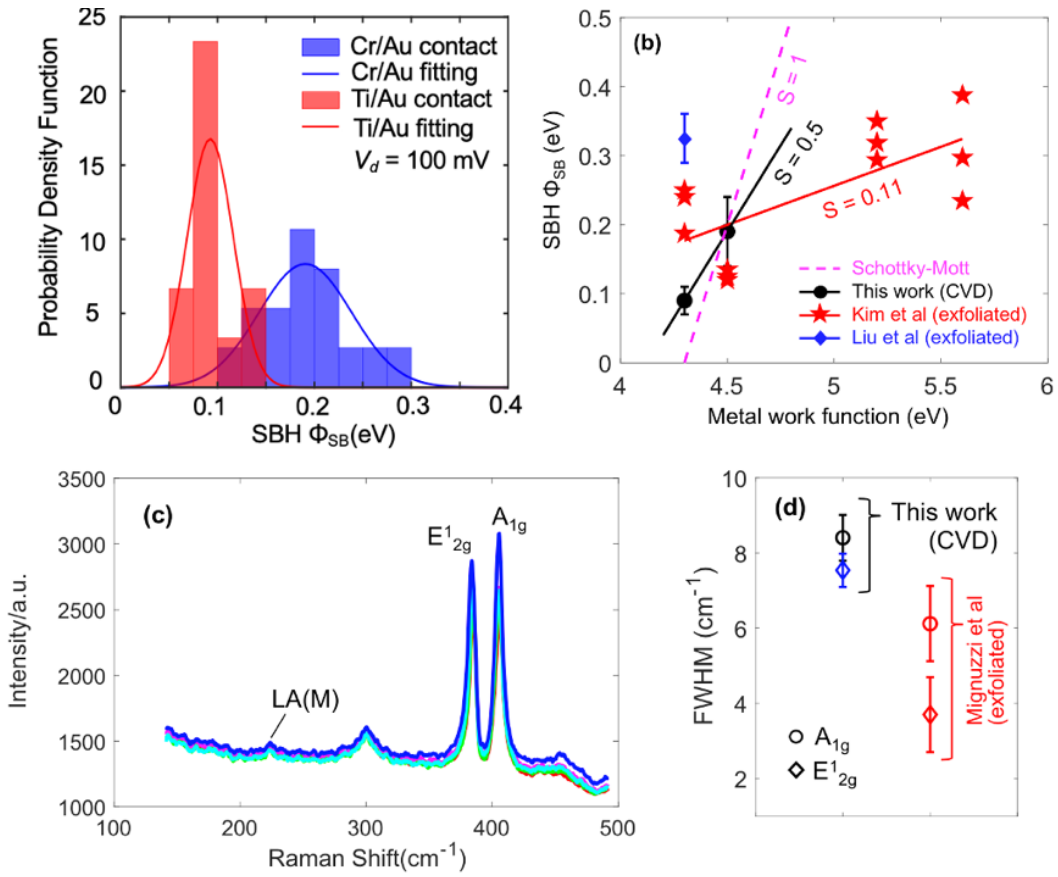

Figure 2.11 (a) Histograms of extracted SBH. (b) SBH plotted as a function of metal work function for CVD-grown ML MoS_2 samples from this work and for exfoliated samples. (c) Room temperature Raman spectra from the channel region of 5 randomly selected FET samples from this work (d) extracted full width half maximum (FWHM) for both MoS_2 prominent Raman peaks from the CVD-grown ML samples (this work) compared to pristine exfoliated flakes.

exfoliated flakes due to having more lattice defects in CVD-grown samples[48]. In Figure 2.11(b) it plots the extracted SBH for CVD-grown monolayer MoS_2 (this work) as a function of the metal (contact) work function and compare it against previous works on exfoliated monolayer MoS_2. Interestingly, an improvement (reduction) in FLP is observed for CVD-grown samples compared to exfoliated ML MoS_2. The FLP factor ($S = |d(\Phi_{SB}) /d(\Phi_M)|$) for CVD-grown samples ($S \cong 0.5$) is larger than those reported for exfoliated flakes ($S \cong 0.1$) and closer to the ideal Schottky–Mott limit ($S = 1$). The enhanced

metallization of CVD-grown MoS_2 likely mitigates the effects of gap (interface) states known to be introduced during material synthesis and/or device fabrication[74,75]. To confirm the relation between our observations of SBH in CVD-grown versus exfoliated MoS_2 and defect density this work uses optical characterization. Figure 2.11(c) plots the room temperature Raman spectra from the channel region of 5 different CVD-grown ML MoS_2 FETs. Firstly, the appearance of a defect-induced peak at ~225 cm^{-1} is not observed in pristine exfoliated samples[76]. Secondly, the full width half maximum (FWHM) for both MoS_2 prominent peaks (E^1_{2g} and A_{1g}) are extracted and plotted. The FWHM are plotted in Figure 2.11(d) and compared against typical results obtained for pristine exfoliated samples. A larger FWHM (broadened peak) indicates a larger defect density. This effect can be attributed to defect assisted broadening around the Gamma symmetry point of the phonon dispersion spectra. As such, increasing defect density leads to broader Raman FWHM. As shown, the CVD-grown ML MoS_2 samples contain a larger defect density compared to exfoliated flakes as evidenced by the larger FWHM. This supports a defect-induced enhancement in metallization of CVD-grown MoS_2, leading to improved coupling between the electrodes and the channel, as a possible explanation for our SBH observations based on the electrical analysis of CVD-grown ML MoS_2 FETs.

The importance of defect on MoS_2 contact properties were studied earlier on exfoliated samples[77]. More recently, Pelella *et al*[17] reported a defect-induced lowering of contact resistance by electron beam irradiation of exfoliated samples, and Chee *et al*[78] reported the metallization of defect- containing CVD-grown MoS_2 using x-ray photoelectric spectroscopy (XPS) leading to reduced SBH and contact resistance.

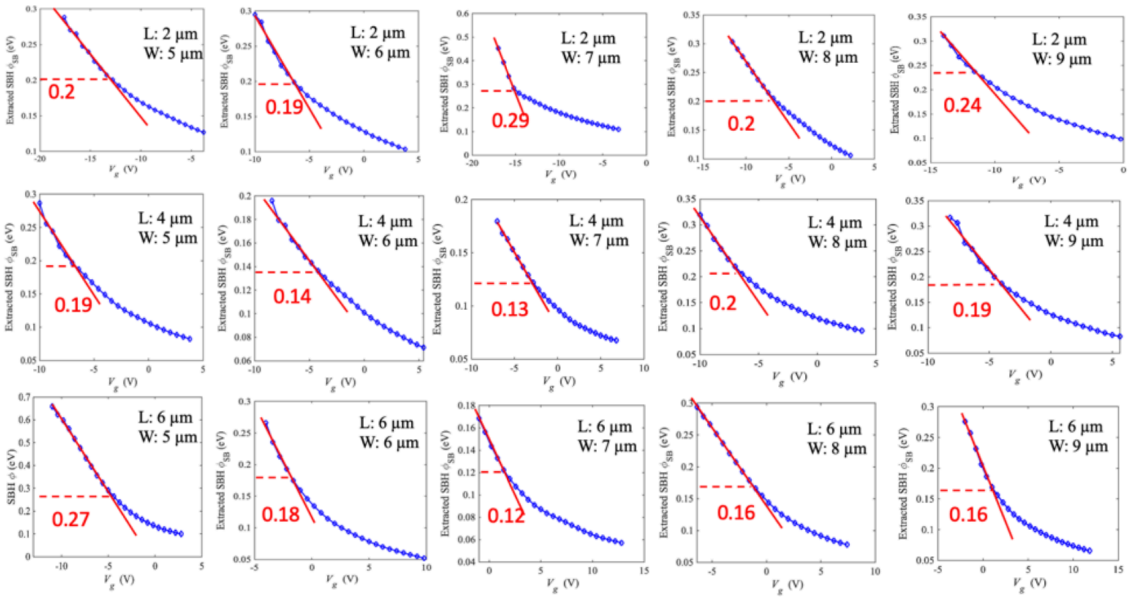

Figure 2.12 Extraction of SBH for various FETs with Cr/Au contacts.

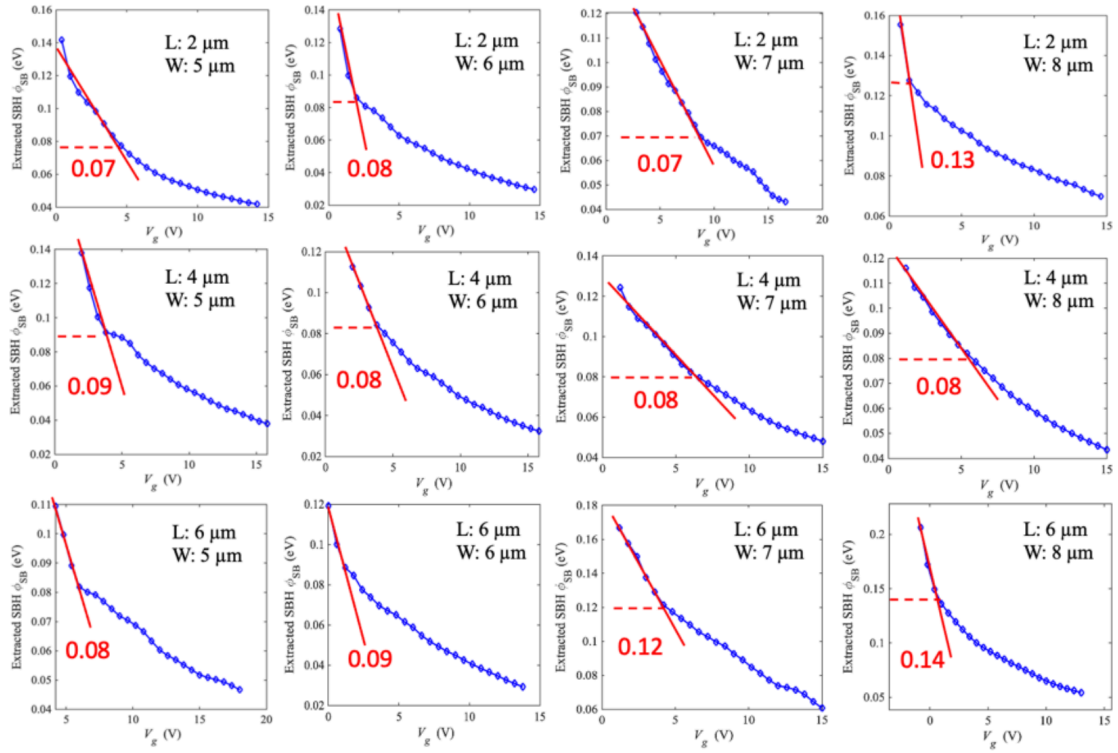

Figure 2.13 Extraction of SBH for various FETs with Ti/Au contacts.

Conclusion

In this chapter it demonstrates a high-yield fabrication process for 2D semiconductors that is compatible with high-throughput material synthesis and with wafer-scale fabrication techniques. Based on this process, large-area CVD-grown ML MoS_2 FET arrays with Cr/Au and Ti/Au contacts were fabricated. The devices were inspected by optical images, Raman spectrum, and AFM measurements. In terms of electrical characterization and analysis, a significant advantage of this process is the ability to test multiple device samples and obtain statistics for key FET parameters (e.g., threshold voltage, on/off ratio, subthreshold swing, mobility, and Schottky barrier height). By characterizing the temperature dependence of charge transport in device with two different metal contacts, the significant impact of Schottky barriers at the interface between the metal contacts and the monolayer MoS_2 channel was statistically verified. Our extractions of Schottky barrier heights for devices with Cr/ Au and Ti/Au contacts on CVD-grown ML MoS_2 resulted in mean values of 0.19 eV and 0.09 eV respectively. These values are smaller compared to those previously reported on FETs with exfoliated MoS_2 channels, indicating enhancement in metallization of CVD-grown MoS_2 compared to exfoliated flakes due to larger number of lattice defects. Moreover, a reduction in FLP is observed compared to exfoliated samples and indicated better coupling between metals and the channel. While FLP is not eliminated as achieved with exfoliated/transferred van der Waals (vdW) metal–semiconductor junctions, this work provides new valuable insight about metal contacts on large-area MoS_2 processes for next-generation integrated electronic systems based on CVD-grown monolayer 2D semiconductors.

CHAPTER 3

HEXAGONAL BORON NITRIDE (H-BN) MEMRISTOR ARRAYS FOR ANALOG-BASED MACHINE LEARNING HARDWARE

Introduction to CVD-grown H-BN Memristors

Two-dimensional (2D) materials have attracted significant interest for the downscaling of CMOS (complementary metal-oxide-semiconductor)[79–81], as well as for beyond-CMOS electronic applications[7,82]. Their atomic scale thicknesses and pristine (i.e., dangling-bond free) surfaces could enable ultra-dense integration for next-generation integrated electronic systems[7]. Consequently, many studies have evolved from the demonstration of isolated devices (e.g., field effect transistors or FETs) based on exfoliated flakes towards large-area methods for fabrication of integrated circuits with 2D materials[83–89]. While early device demonstrations focused predominantly on FET applications[39,49,90,91], recent studies have proposed memory and neuromorphic devices based on the non-volatile resistive-switching (NVRS) behavior observed in various 2D materials including transition metal dichalcogenides (TMDC)[92], black-phosphorus[93,94], graphene[95,96], and hexagonal boron nitride (h-BN)[27,97–104], etc. These devices are generally configured in vertical two-terminal structures, where the resistive switching layer is sandwiched between top and bottom metal electrodes. The use of 2D materials has enabled the demonstration of devices with atomically thin resistive switching layers having low voltage operation[100] and fast switching[97,98]. Chemical vapor deposition (CVD)-grown h-BN has attracted much attention for use as the resistive switching layer due to its compatibility with large-area wafer-scale fabrication, and arrays of h-BN memristors have been reported[88]. In CVD-grown h-BN

devices the resistive switching process is attributed to the formation and rupture of conductive paths via penetration of metal ions into defects at h-BN grain boundaries.

Initial studies of h-BN memristors reported on their non-volatile resistive switching behavior observed as transitions or hysteresis in measurements of DC current-voltage characteristics[97,98,100,102]. Previous work[88] has also shown the programming of multiple resistive states in h-BN memristors by the application of consecutive voltage pulses, although using significantly larger pulse widths (milliseconds) compared to what is reported here (nanoseconds). Pulsed programming is required for practical memory and neuromorphic computing applications. Moreover, the pulsed programming of multiple conductive states is critical for the implementation of synaptic plasticity (i.e., long-term potentiation and depression) in neuromorphic hardware, as well as for the analog-based implementation of machine learning functions in memristor arrays[105]. For example, most analog-based implementations of neural networks and/or machine learning hardware based on memristor crossbars rely on dot-product (i.e., multiply-accumulate) operations[106–108]. Here, the accumulated currents at the outputs of the arrays result from the product of input voltage signals (input vector) and the conductance of the memristor arrays (column vectors). Nevertheless, this basic function has not been reported in arrays of h-BN memristors.

This chapter presents the wafer-scale fabrication of memristor arrays using on CVD-grown h-BN resistive switching layers, and their multi-state analog programmability. It focuses on the experimental demonstration of dot-product operation on h-BN memristor arrays and on the hardware implementation of multi-variable stochastic linear regression. This work extends beyond existing demonstrations of NVRS behavior in isolated h-BN

memristors and paves the way for more sophisticated demonstrations of machine learning applications based on 2D materials.

Method and Fabrication for CVD-grown H-BN Memristor Arrays

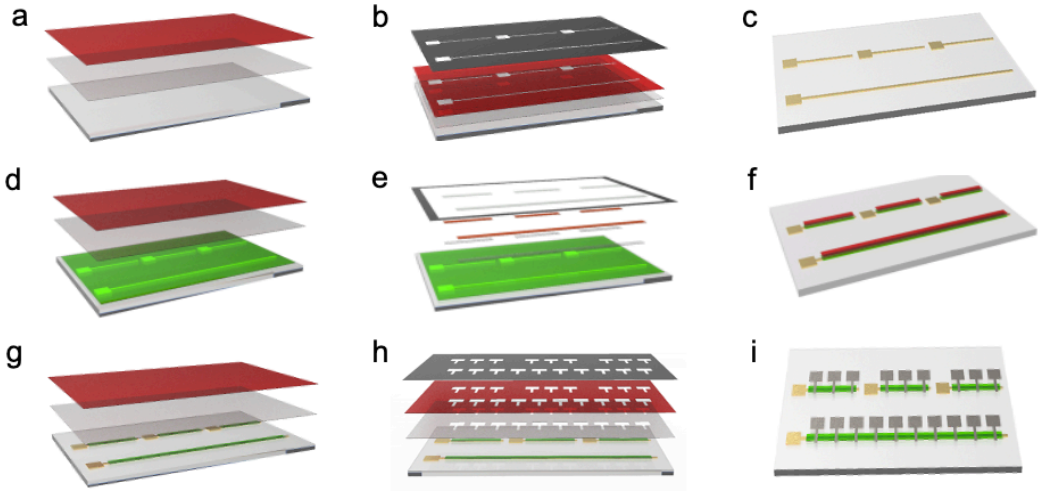

Figure 3.1 Fabrication process of h-BN memristor

The Au/h-BN/Ti memristor arrays were fabricated on a 90 nm SiO_2/Si wafer as shown in Figure 3.1(a-i). First, the bottom electrodes (5 nm Cr/35 nm Au) with 3, 20, and 50 μm width were patterned on the substrate via photolithography and e-beam evaporation methods. Second, CVD-grown multilayer h-BN on copper from Graphene Supermarket was transferred onto the prepared SiO_2/Si substrate by wet transfer method. Third, h-BN film was patterned to expose the 100 μm by 100 μm bottom electrodes pads using oxygen plasma. Finally, the top electrodes (70 nm Ti) were patterned with the same electrode width and the same methods as that of the bottom electrodes. The top electrodes are exposed to air and a thin surface layer may be oxidized over time. This oxidized layer can be easily penetrated with probe needles during measurements, and its impact on the resistive switching behavior has been ruled out by comparing against devices with Au-capped top electrodes that show very similar characteristics (see Figure 3.6)

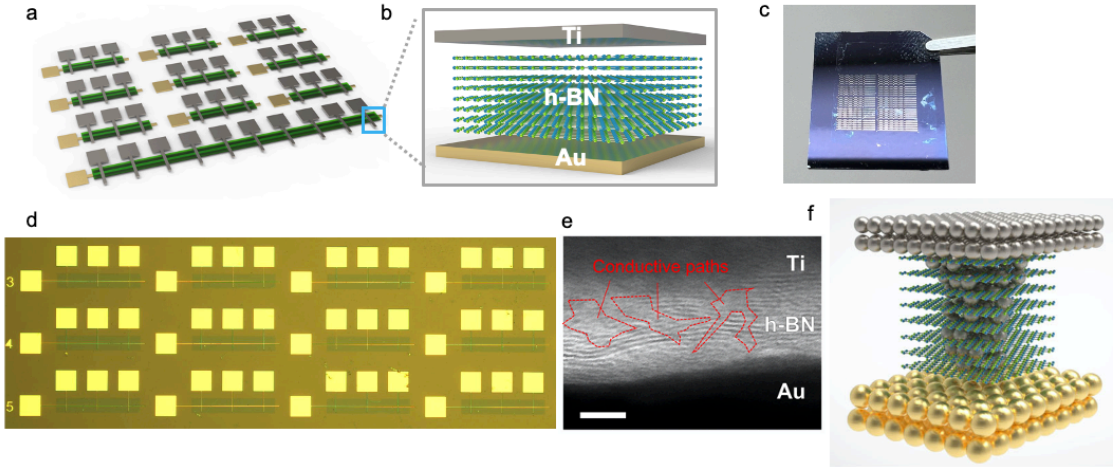

Figure 3.2 hexagonal Boron Nitride (h-BN) memristor arrays. a Schematic of the Au/h-BN/Ti memristor arrays and b cross-sectional schematic of single memristor c Photograph of Au/h-BN/Ti memristor arrays on 90 nm SiO_2/Si wafer under ambient light, and d micrograph of arrays with 3 μm × 3 μm active areas. e Cross-sectional TEM image of the Au/h-BN/Ti memristor indicating local defects responsible for the formation of conductive paths. Scale bar, 5 nm. f A representation of conductive nanofilaments on the Au/h-BN/Ti memristors.

Figure 3.2(a) shows a schematic of the fabricated Au/h-BN/Ti memristors arrays where the Au bottom electrode (BE) is shared across various devices each having an independent Ti top electrode (TE) (1 × 3 and 1 × 10 arrays are shown). Figure 3.2(b) illustrates the cross-section of the Au/ h-BN/Ti memristor. Figure 3.2(c) is a photograph of the memristor arrays on a 2cm-by-2cm SiO_2/Si wafer. A micrograph of the fabricated h-BN memristor arrays shown in Figure 3.2(d) corroborates the dimensions of the 100 μm × 100 μm squared pads and the electrodes with 3 μm × 3 μm active areas (see Figure 3.3 for 20 μm × 20 μm and 50 μm × 50 μm). Figure 3.2(e) shows a cross-section transmission electron microscopy (TEM) image of a typical Au/h-BN/Ti memristor. From the TEM image it confirms the thickness of the CVD-grown multilayer h-BN film (~8–10 nm) corresponding to approximately 15–20 atomic layers. Moreover, local defects can be observed that facilitate

metallic penetration from the top electrode (Ti) to form conductive paths (i.e., conductive nanofilaments) responsible for the resistive switching behavior in the h-BN memristors.

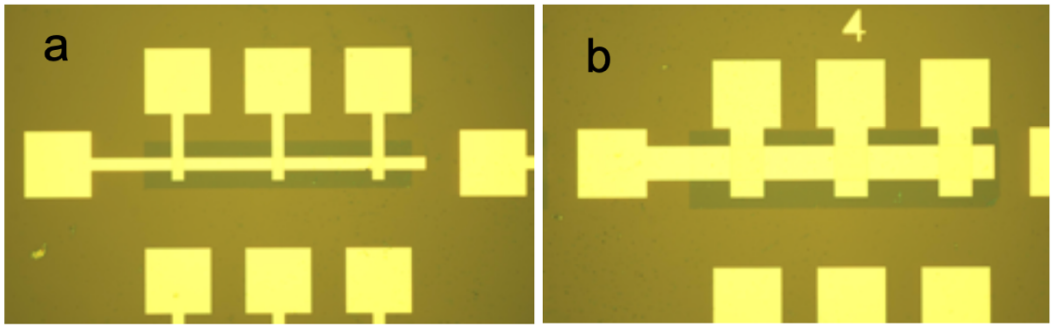

Figure 3.3 Optical images of Au/h-BN/Ti memristor crossbars with different active areas: (a) 20 μm and (b) 50 μm.

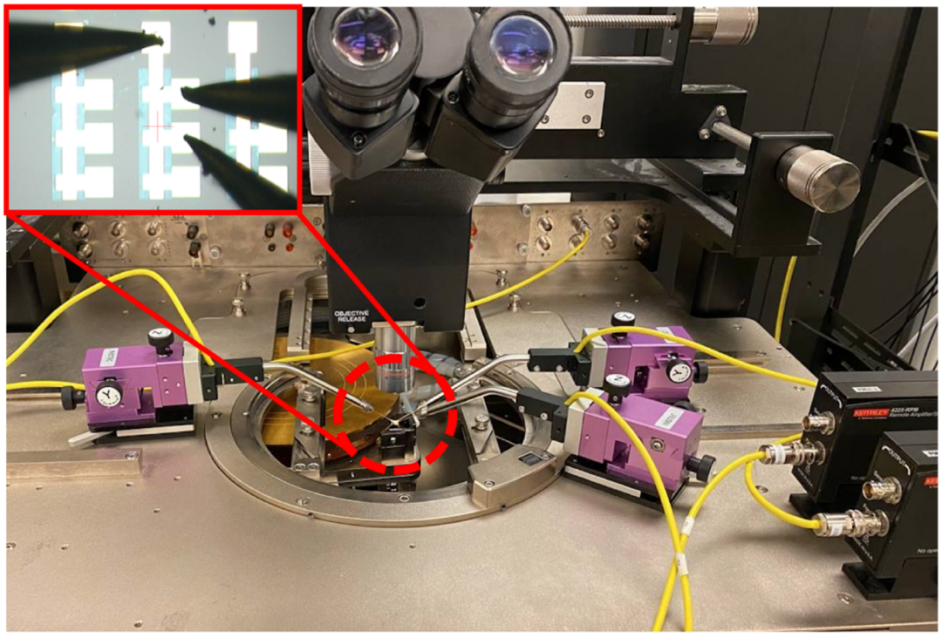

Figure 3.4 The h-BN memristor arrays under the microscope in the probe station and experimental configuration used for electrical testing. Probe connections made on the h-BN memristor array pads (connecting electrically to the top and bottom electrodes) shown on the inset are routed with triaxial cables through the Keithley remote amplifier/switch (RPM) where I can automatically connect pulse or source/measure units (PMU or SMU).

The electrical characterization was conducted on a Cascade semi-automatic probe station using a Keithley 4200 semiconductor characterization system. The DC I–V measurements were performed using source measure units (SMUs), while the pulse

programming experiments used a combination of pulse measure units (PMU, model 4225) for programming pulses and SMUs for reading currents. In the pulse programming experiments it was switched between PMU and SMU automatically using a Keithley remote amplifier/switch (4225-RPM). Figure 3.4 shows the experimental setup.

Result and Discussion for CVD-grown H-BN Memristor Arrays

Resistive Switching Properties

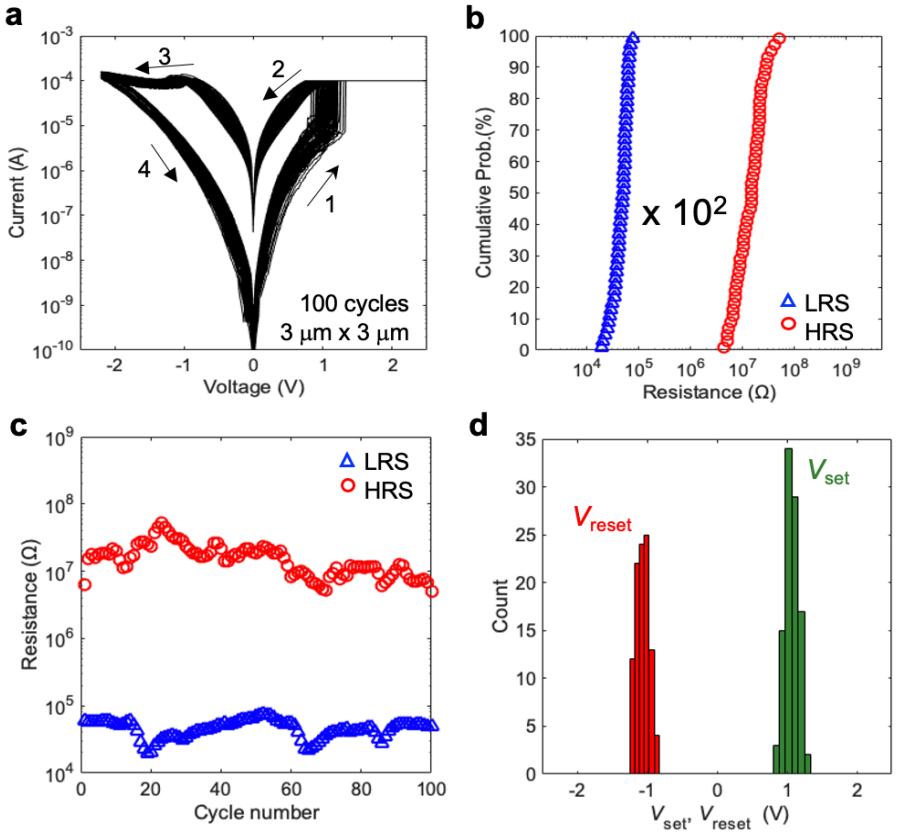

Figure 3.5 Resistive switching characteristics of h-BN memristors. (a) Representative I–V characteristics measured during 100 cycles in one single 3 μm × 3 μm Au/h-BN/Ti memristor with 0.1 and 1 mA compliance respectively for the positive and negative sides of the sweep. (b) Cumulative probability distribution of the HRS and LRS (read at 0.1V). (c) resistance vs cycle number plot, and (d) histogram of set and reset voltages.

Individual h-BN memristors from the arrays were measured electrically to evaluate their resistive-switching properties. Current–voltage (I–V) characteristics were obtained

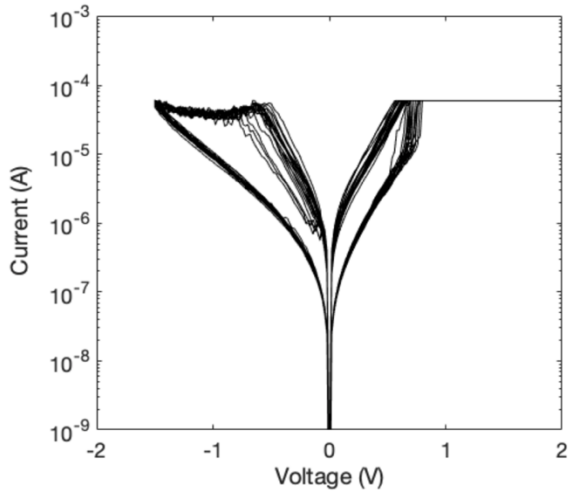

Figure 3.6 Typical resistive-switching I-V characteristics (multiple cycles) of a 3 μm × 3 μm Au/h-BN/Ti/Au memristor (i.e., the Ti top electrode is capped with Au).

by sweeping a voltage across the top and bottom electrodes while measuring current. Figure 3.5(a) plots 100 consecutive cycles of I–V measurements on an Au/h-BN/Ti memristor with a 3 μm × 3 μm active area. A compliance of 0.1 mA was activated for positive applied voltages. The numbered labels indicate the sweeping process during the I–V measurement. As shown, clear transitions occur between resistive states, evidence of a forming-free bipolar resistive-switching (RS) operation with low cycle-to-cycle resistance variability and low set and reset voltages (approximately 1 and −1 V). The cumulative distribution plot of the resistive states extracted at a read voltage of 0.1 V from all 100 cycles is shown in Figure 3.5(b). Two distinct states labeled as HRS (high resistance states) and LRS (low resistance state) are easily observed as their distributions are separated by approximately two orders of magnitude. Another illustration of the HRS and LRS distributions is provided in Figure 3.5(c) where the resistances are plotted as a function of the cycle number. A histogram of the set and reset voltages corresponding to

transitions between HRS and LRS is shown in Figure 3.5(d). All results indicate a stable and reliable RS bipolar operation.

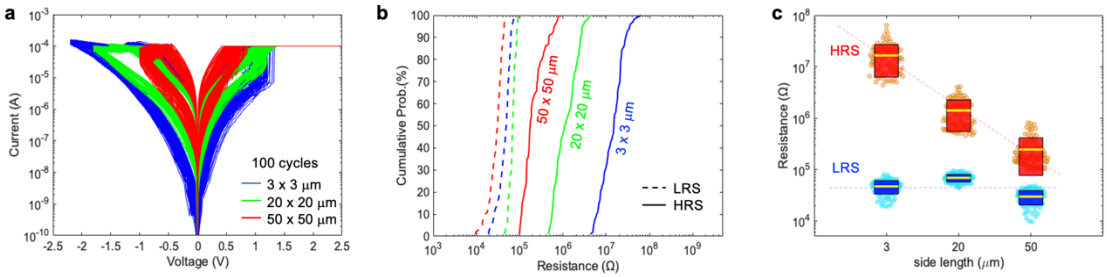

Figure 3.7 Dependence of the I–V characteristics and of the HRS and LRS statistics on h-BN memristor active area. (a) Comparison of 100 I–V cycles from Au/h-BN/Ti memristors with different active areas. (b) Cumulative probability distribution of the HRS and LRS (read at 0.1 V) and (c) statistical analysis of resistance (HRS, LRS) as a function of the active area side length.

This work also explored the dependence of the I–V characteristics and of the HRS and LRS statistics on h-BN memristor active area. In Figure 3.7(a) it compares the I–V characteristics from devices with 3 μm × 3 μm, 20 μm × 20 μm, and 50 μm × 50 μm active areas. All devices were measured for 100 cycles and the results show good repeatability with limited cycle-to-cycle variation. The difference in active area has a larger effect on the HRS and this is easier to identify in the cumulative distribution plot shown in Figure 3.7(b). Here, the HRS an LRS resistances are shown for the three devices (all 100 cycles) extracted at a read voltage of 0.1 V. While distributions of LRS are only minimally affected by active area, a clear trend in HRS. The HRS resistance goes down with increasing the active area. This trend in HRS and LRS with active area has been previously reported for different filamentary-based RS memory[109,110]. Figure 3.7(c) is a box plot showing the distribution of HRS and LRS as a function of cell area side length (3, 20, and 50 μm). The plot includes the raw data (circles), the standard deviation (size of box), and the mean values (solid horizontal lines). While cycle-to-cycle variability is comparable to previous

resistive-switching technologies (e.g., oxide-based RRAM[111]), device-to-device variability remains large, likely due to nonuniformity of the h-BN film and may be improved by optimizing the synthesis and transfer methods.

3.3.2 Multistate non-volatile pulse programmability

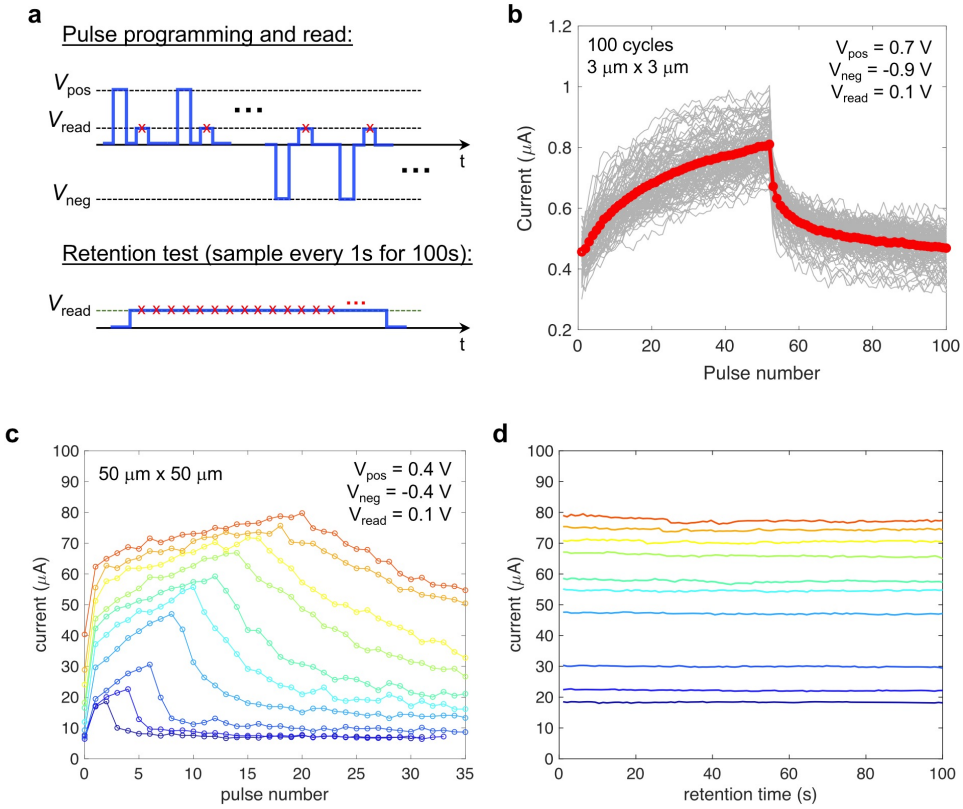

Figure 3.8 Multi-state non-volatile pulse programming of h-BN memristors. (a) Diagram of the pulsed measurements and retention test. (b) 100 cycles of pulse programming for Au/h-BN/Ti memristor with 3 μm × 3 μm active area (50 positive pulses, followed by 50 negative pulses for each cycle). Gray lines show 100 individual cycles, and the red line shows the average. (c) Pulse measurement cycles with increasing number of positive pulses. Deep blue to red colored curves corresponds to increasing the number of positive pulses from 2 up to 20. (d) Retention tests measured immediately after the last positive pulse for each cycle using a read voltage of V_{read} = 0.1 V. The color of the curves in d match the color of the corresponding cycle in (c).

Achieving multiple conductive states through the application of programming pulses is critical for the implementation of neuromorphic hardware and for the analog-based implementation of machine learning functions in memristor arrays. This work investigates

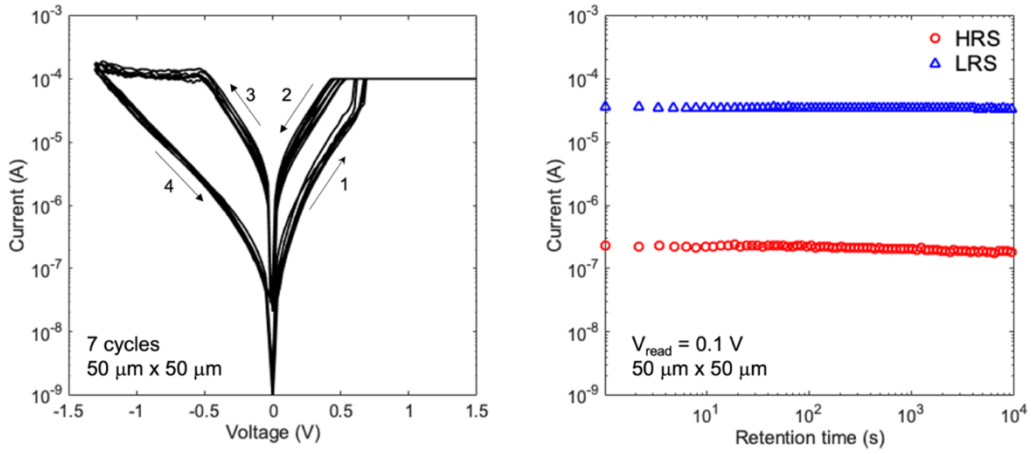

Figure 3.9 (left) Resistive-switching I-V characteristics, and (right) retention test up to 10,000 seconds showing stable LRS and HRS at room temperature (V_{read} = 0.1 V).

the multistate pulse programmability of the Au/h-BN/Ti memristors by applying a sequence of positive/negative voltage pulses (pulse width is 500 ns, amplitudes indicated in Figure 3.8). After each pulse a small read of 0.1 V is applied to read the current (conductive state) of the device (see Figure 3.8a top panel). The results are shown in Figure 3.8, where 100 cycles of 50 positive pulses followed by 50 negative pulses were applied. The gray lines are the results from each individual cycle and the solid red line with circles is the average from all 100 cycles. The results show a gradual change in conductance (from ~4 to 10 µS) indicating good analog (i.e., multistate) programmability. Due to the fast-switching behavior (nanoseconds), a low energy consumption per programming pulse of $E_{pulse} = (I)(V)(t_{pulse}) \cong 125$ fJ is achieved. This can be further reduced to aJ/pulse by applying a low compliance current as previously reported on h-BN memristors[88]. The non-volatile property of the conductive states is also demonstrated by retention tests where current is sampled over 100 s (read voltage 0.1 V) following the application of the programming pulses (Figure 3.8c, d). Figure 3.8c plots current for different programming cycles where

the number of positive pulses was varied from two up to twenty. Immediately after the last positive pulse, a 0.1 V read voltage was applied and held and sample current every second for 100 s (see Figure 3.8a bottom panel). After the retention test the negative pulses are applied and it then proceeds to the next cycle. The results from the retention test are shown in Figure 3.8d where the current is plotted as a function of the retention time. Longer retention tests up to 10^4 s confirming a stable, non-volatile response are shown in Figure 3.9(right). The results confirm the endurance and robustness of the conductive filaments and demonstrate the multistate non-volatile pulse programmability of Au/h-BN/Ti memristors.

Dot Product with H-BN Memristor Arrays

The dot-product operation is crucial for neuromorphic computing and machine learning hardware. For example, a dot-product operation is typically used in neural networks implemented on memristor crossbar arrays to accumulate currents at the outputs (i.e., the post-synaptic neurons). Here, the product of the input voltage signals (the input vector, v) multiply the conductances of the memristor arrays (the column vector, G) to accumulate an output current (I). This is achieved in hardware due to Ohm's and Kirchhoff's laws as given by $I = \sum vG$. This dot-product operation has been previously reported on oxide-based memristors[107,112], but not on recently developed h-BN memristor arrays. Here it demonstrates the most basic implementation of dot-product on an array of two h-BN memristors where the accumulated current is given by $I = \sum v1G1 + \sum v2G2$. The experimental setup is illustrated in Figure 3.10a. As shown, for each memristor it can be switched between a pulse source (used to program the memristor conductances G_1 and G_2)

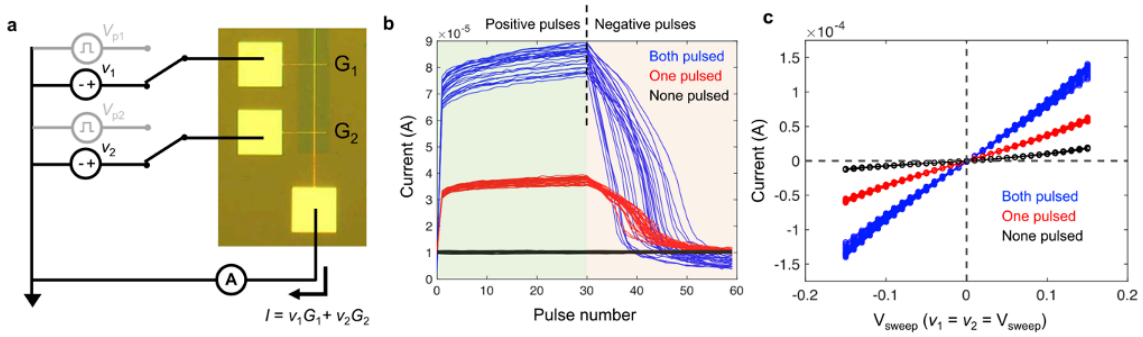

Figure 3.10 Dot-product operation with h-BN memristor arrays. (a) Schematic of the experimental setup for demonstration of basic dot-product operation. (b) Three different cases of pulse programming the memristor arrays: a read voltage of V_{read} = 0.1 V used to measure current after each pulse. (c) For each cycle in part (b) I also sweep the read voltage V_{sweep} between −0.15 and +0.15 and measure total current to show the linearity and repeatability of the dot-product operation. The sweeps are done after the 30 positive pulses for each cycle.

and a voltage source to apply the read voltage on the memristors (v_1 and v_2). During the read operation it measures the output current through the shared bottom electrode. Figure 3.10b plots the total current measured with a read voltage of 0.1 V (v_1 = v_2 = 0.1 V) following the application of consecutive programming pulses (positive then negative). It shows the case with both memristors pulsed (i.e., both are programmed with voltage pulses), the case with only one of the memristors pulsed, and with none pulsed (20 cycles shown for each case). For each cycle it also sweeps the read voltage (v_1 = v_2 = V_{read}) between −0.15 and +0.15 V and measure the total current after all 30 positive programming pulses. The results from these voltage sweeps are shown in Figure 3.10c. For the case where both memristor were pulsed (blue lines), the conductances G_1 and G_2 are both high (LRS) and therefore the current is the largest. When none of the memristors are pulsed (black lines), both G_1 and G_2 are low (HRS), and the current is the lowest. When only one memristor is pulsed, its conductance is high (LRS) while the other memristor's

conductance is low (HRS), and the magnitude of the current is between the first two cases. The results in Figure 3.10c indicate good linear behavior of the memristor I–V characteristics (needed for reliable dot-product operation)[113] and show good repeatability (small cycle-to-cycle variation).

Implementation of Linear Regression

The experimental demonstration was done with a Keithley 4200 SCS using a custom test script developed in the Keithley user library tool (KULT) and executed in the Keithley interactive testing environment (KITE). The input parameters to the test script are the minimum and maximum conductance values for each memristor (predetermined based on pulse measurements, used to normalize output currents from the array), the initial values for the programming pulse amplitudes, the constant value for the width of the programming pulses, and the number of iterations. The test script loads the training data and normalizes the independent variables (in this case marketing and R&D investments in thousands of dollars) to voltages between 0 and 0.15 V. I also subtract a constant offset (y-intercept) from the dependent variable (profit) so that the model is based only on two regression coefficients (model parameters represented by the memristor conductances). The script then goes into a loop where it randomly selects a sample for the data set and apply the read voltages (v_1 and v_2) that correspond to the independent variables of that sample. The current by $I = \sum v1G1 + \sum v2G2$ is read at the output of the h-BN memristor array (shared bottom electrode) and is translated from Amps to dollars to be compared against the training sample. This read operation is conducted with the Keithley SMUs. It then calculates the error (δ) in the prediction as well as the required update for each model parameter (i.e., ΔG_1 and ΔG_2). From the minimization of the cost function (i.e., $\delta^2/2$) the updates are

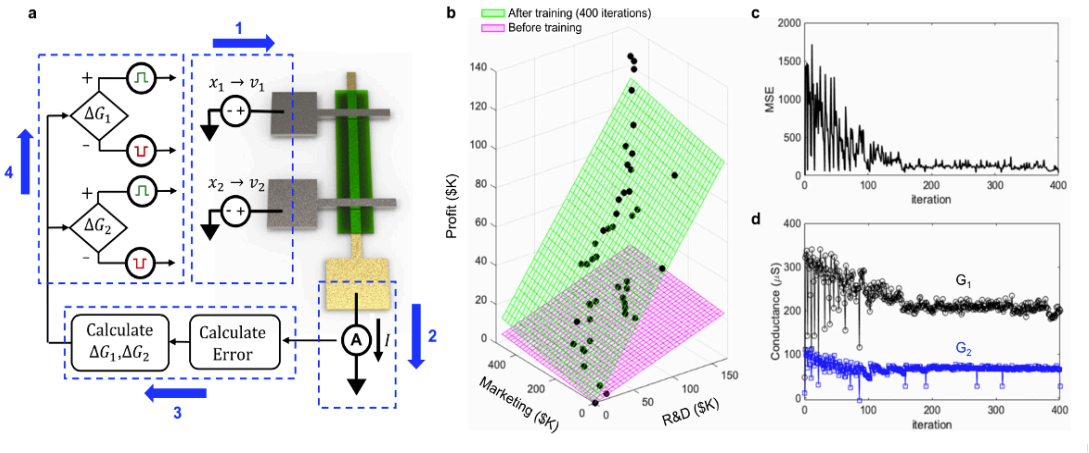

Figure 3.11 Implementation of stochastic multivariable linear regression on h-BN memristor arrays. (a) Flow diagram for stochastic multivariable linear regression: In step 1, the inputs (independent variables) are translated to DC voltages and applied to the array (top electrodes). In step 2, the total output current (the model prediction) is measured at the shared bottom electrode. In step 3, the prediction error is calculated by comparing against the training sample, and model parameter updates are obtained (ΔG_1 and ΔG_2). In step 4, a single programming pulse is applied to each memristor. Good convergence of the implementation is verified by (b) model prediction fit to training data before (magenta plane) and after (green plane) training. (c) Evolution of mean squared error (MSE) with training, and d evolution of h-BN memristor conductances (model parameters) with training step (iterations) reaching stable values that minimize prediction error.

calculated as $\Delta G = -\delta v$. Here it proposes a simplified hardware-compatible regression approach where the memristor conductances (i.e., the model parameters) are updated through the application of a single programming pulse, and the polarity of the pulse is determined by the sign of the corresponding ΔG. The programming pulses are applied using the Keithley's 4225 PMU (pulse width is fixed to 500ns). Gradient descent algorithms typically use learning rate decay to improve convergence, where model parameter updates are weighted by a learning rate (α) that is reduced gradually as training advances. In the hardware demonstration I introduce learning rate decay by gradually reducing the amplitude of the programming pulses (I have reduced the amplitude of the programming pulses by 0.1% after each iteration).

The implementation of stochastic multi-variable linear regression on an h-BN memristor array. In this implementation I use an h-BN memristor array to predict the profit of startup companies given their investment in marketing and in research and development (R&D). Our model is trained using a dataset from 50 startup companies available online[114]. In this implementation, the memristor conductances (G_1 and G_2) are the model parameters. The training process is illustrated in Figure 3.11a. For each training step a single sample from the dataset is randomly selected (the sample includes profit, marketing, and R&D in \$K). The input variables (marketing and R&D) are translated (normalized) to voltages between 0 and 0.15 V. These voltages are applied to the h-BN memristors (v_1 and v_2). I have previously confirmed that for this range of read voltages the I–V response is linear, and the dot-product operation is reliable (see Figure 3.10c). This is important for the implementation of linear regression as the prediction (h) is determined from the output current of the h-BN memristor array given by the dot product as

$$I = v^{\mathrm{T}} G \,, v = \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}, G = \begin{bmatrix} G_1 \\ G_2 \end{bmatrix}. \qquad (1)$$

The prediction is then compared against the training sample (y = profit) from which I determine the error and the required update for each of the model parameters (ΔG_1 and ΔG_2). Here I use a hardware-compatible approach to update the model parameters whereby a single programming pulse is applied to each memristor[115–117], and the polarity of the pulse is determined by the sign of ΔG_1 and ΔG_2. This programming pulse will slightly adjust the conductances to ultimately minimize the error in the prediction. To achieve good convergence, stochastic regression algorithms typically limit the parameter updates with a learning rate that is gradually reduced with training number[115,116,118]. In our experiments the learning rate is implemented by gradually reducing the amplitude of the programming

pulses. I reduce the amplitude of the programming pulses by 0.1% after each iteration (starting with ±1 V, the pulse amplitude will be reduced to ±0.67 V after 400 training steps). The width of positive and negative programming pulses is kept fixed at 500 ns throughout the training process.

Figure 3.11b–d show the results of the stochastic linear regression implementation. In Figure 3.11b it plots the training data (black dots) as well as the model prediction before (magenta plane) and after 400 training steps (green plane). As shown, the trained model clearly predicts the profit of startup companies based on their investments in marketing and R&D much better than the before training. A more quantitative result is shown in Figure 3.11c where it plots the mean squared error (MSE) as a function of the training step (i.e., iteration) as given by MSE $= (1/N)\sum_i \delta_i^2$ where N is the sample size (50 in this case) and $\delta_i = h_i - y_i$ is the error in the prediction. As shown, the MSE reduces with training indicating good convergence of the algorithm. Figure 3.11d shows the change in conductances G_1 and G_2 (the model parameters) during the training process. The mean

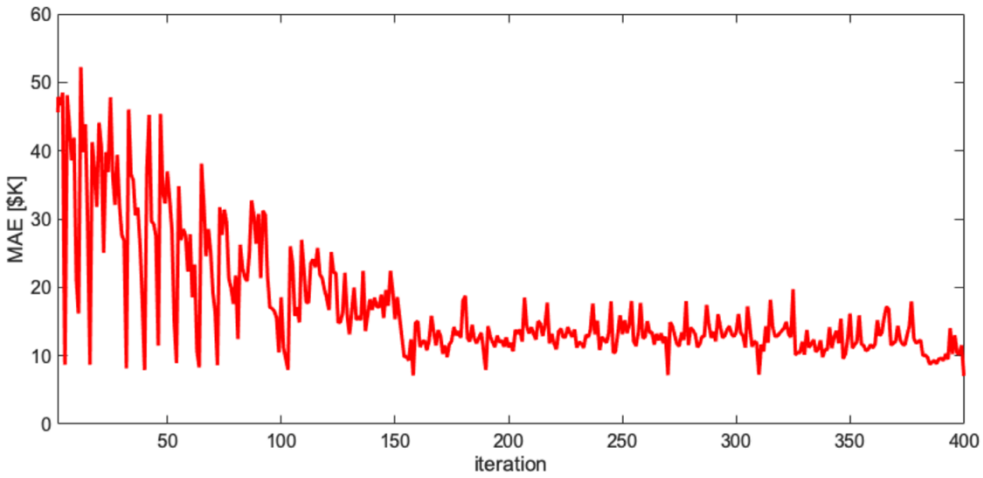

Figure 3.12 Mean absolute error MAE = $(1/N)\sum_i |\delta_i|$ as a function of iteration (training step) for the demonstration of stochastic multivariable linear regression implemented on the h-BN memristor array.

absolute error (MAE) was also calculated and is shown in Figure 3.12. I see larger updates and fluctuations in the conductances during the initial training steps, and eventually convergence to the optimal values for the model parameters.

Conclusion

In this chapter, I have reported the fabrication and characterization of Au/h-BN/Ti memristor arrays. I have presented statistics for the nonvolatile resistive switching behavior of h-BN memristors, including the effects of cell active area. I have then focused on establishing the non-volatile multistate pulse programmability of the h-BN memristors based on multiple cycles of consecutive programming pulses, and retention tests. Our results show successful multistate programming of conductive states with good stability. Moreover, I have presented the implementation of the dot-product operations on h-BN memristor arrays, and show good linearity and repeatability, which is crucial for machine learning hardware. Finally, I have demonstrated the hardware implementation of stochastic multivariable linear regression on an h-BN memristor array. Our hardware-compatible implementation shows good convergence and represents an important milestone in advancing the research and implementation of 2D materials for machine learning hardware. It also paves the way for more sophisticated demonstrations of machine learning algorithms using 2D materials, devices, and circuits.

CHAPTER 4

VERTICAL HEXAGONAL BORON NITRIDE MEMRISORS WITH GRAPHENE-EDGE CONTACTS

Introduction to Vertical H-BN Memristors

Resistive-switching random access memory (RRAM) is considered one of the most promising emerging candidates for non-volatile embedded memory, with applications in neuromorphic and in-memory computing (IMC) architectures for artificial intelligence (AI), machine learning (ML), and Internet of Things (IoT)[119–121]. It provides good scalability, low-power consumption, and fast-switching speeds[121–123]. Conventional RRAM cells (or memristors) consist of two-terminal devices in a metal-insulator-metal (MIM) configuration where the active material (insulating switching layer) is sandwiched between top and bottom metal electrodes[26,27,97,124,125]. A simple and compact structure and compatibility with back-end-of-line (BEOL) processing makes RRAM a viable candidate for CMOS+X paradigms (integration of CMOS with X = emerging technologies)[7,125,126]. The working principle of RRAM relies on the dependence of the internal resistive state on the history of the applied voltage and/or current[127]. Among the various physical mechanism responsible for non-volatile resistive switching (NVRS), formation and dissolution of filamentary conductive pathways is one of the most commonly employed[128]. Recently, 2DMs have attracted significant interest for RRAM due to promising NVRS characteristics[28,88,129–131], even with atomically-thin active layers (e.g., 0.3 nm h-BN monolayers)[92,98,132]. Specifically, 2DMs-based RRAM are sought not just for their ultimate scalability, but also for their experimentally demonstrated ultralow write currents (fA) and

programming energies (zJ)[88,133], high thermal reliability and long-term retention, ultrafast switching speeds (ps)[133–135], reduced temporal and spatial variation[88,136,137], etc.

In 2DMs-based RRAM, large-area CVD-grown films are desirable for wafer-scale integration. Here, h-BN has attracted significant interest because of its BEOL processing compatibility and excellent insulating properties[138]. However, native lattice defects (e.g., vacancies, grain boundaries) in CVD-grown films promote the penetration of metallic ions originating from the electrodes to form conductive nanofilaments (CNF). In fact, the formation and dissolution of CNF in CVD-grown (polycrystalline) h-BN films is what enables its NVRS behavior, but a significant defect density can lead to many conductive paths within the active region of a single device. Thus, existing h-BN memristor demonstrations using planar MIM configurations have many paths which are difficult to control in number, location, and conductive state (on, off, or partial formed CNF). Previous work on planar CVD-grown h-BN memristors estimates that >150 filamentary paths can be involved in NVRS of a single device[139]. Moreover, some of the CNFs cannot be turned off and remain active, so the current through the memristor cannot be lowered below a certain level. In other words, the resistance in the off-state / high resistance state (HRS) is severely limited. Granted, reducing the active area of the device would reduce the number of conductive pathways. However, scaling down the active area of CMOS-integrated memristors is limited by the resolution of lithography dictated by BEOL processing for a given technology node. For example, a recent demonstration[33] of h-BN memristors integrated in the BEOL of a CMOS 180 nm node at the fourth metal layer with via contact diameters of 260 nm achieved a minimum active area of 53,000 nm^2. To realize higher

integration density and improvement in power consumption (lower operating currents) a smaller active area is needed.

The edge of atomically-thin (0.3 nm thick) graphene has been used as a contact for different electronic devices[32,140,141], including previous work on metal-oxide-based RRAM[142]. Using graphene edge contacts, the active area of a memristor can be significantly reduced in a vertical memristor configuration (switching layer is integrated vertically, see Figure 4.1). For example, a 100 nm graphene edge contact (thickness of 0.3 nm) can achieve an ultrasmall active area of 30 nm^2, which is orders of magnitude smaller than previous demonstrations. Whereas numerous studies have focused on NVRS behavior of planar h-BN memristors[28,30,33,88,100,133], no reports have discussed NVRS and scaling properties of vertical h-BN memristors. In this work, combining the benefits of CVD-grown 2DMs and graphene edge contacts, it reports vertical h-BN memristors with ultrasmall active areas, low operating currents (high resistance) and large R_{HRS}/R_{LRS} ratio. Moreover, the proposed structure enables 3D integration (vertical stacking) for ultimate scalability and facilitates studying fundamental NVRS mechanisms of single CNFs in CVD-grown 2DMs which was previously unattainable in planar devices. It reports single quantum step in conductance consistent with theorized atomically-constrained nanofilament behavior in CVD-grown 2DMs-based memristors[30,143,144] associated with potential improvements in stability of CNF and NVRS behavior. It shows improvements in retention of quantized conductance compared to other non-2DMs filamentary-based memristors.

Method and Fabrication for Vertical H-BN Memristors with Graphene-edge Contacts

Au/Ti/h-BN/Gr(E) memristors fabrication.

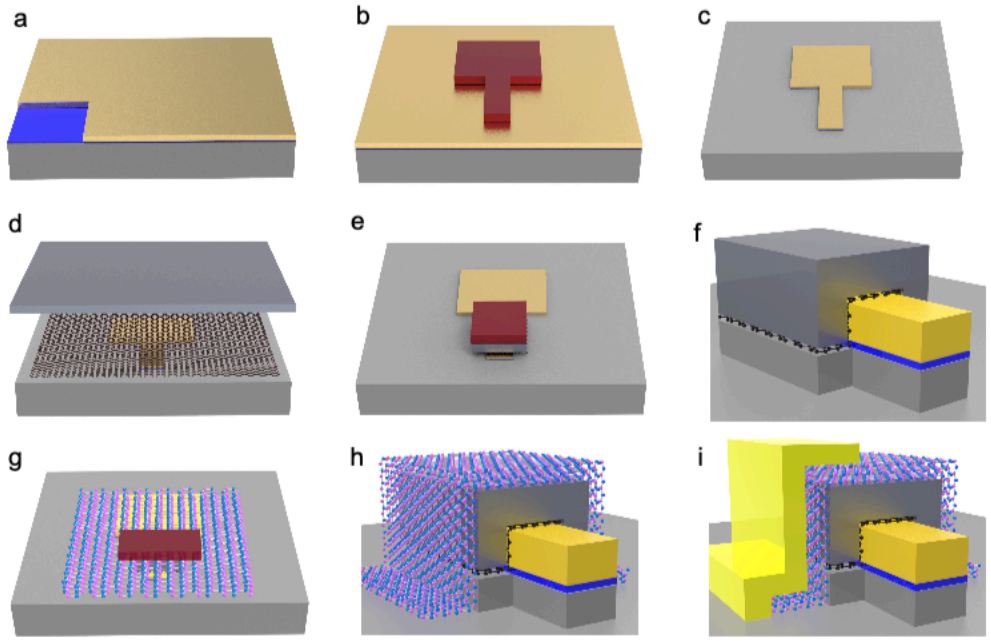

Figure 4.1 Fabrication steps of the vertical h-BN memristor with graphene edge contacts.

The Au/Ti/h-BN/Gr(E) memristors were fabricated on a 90 nm SiO_2/Si wafer. First, the initial 90 nm SiO_2/Si wafer was cleaned by piranha solution and mixture of DI water, hydrochloric caid, and hydrogen peroxide (5:1:1). Then, 5 nm Ti and 25 nm Au thin films were deposited on the blank wafer via e-beam evaporation method, as shown in Figure 4.1a. Second, photoresist was spin-coated on the wafer surface and patterned by Heidelberg MLA-150 (Figure 4.1b). The pattern of the photoresist was transferred onto Au/Ti pad and electrode by Ar sputtering and Ti dry etch process. After removal of the photoresist, the bottom electrode was complete, as shown in Figure 4.1c. Subsequently, CVD-grown graphene ordered from Grolltex was transferred by wet transfer method, then 100 nm SiO_2 was deposited as isolation layer onto the graphene via e-beam deposition (Figure 4.1d). To pattern the graphene and isolation SiO_2, the photoresist was spin-coated again and

patterned via Heidelberg MLA-150. The SiO_2 and graphene patterns were etched by SF6/Ar plasma (Figure 4.1e). The 90 nm SiO_2 on the substrate was also recessed by ~30 nm to expose the graphene edges on the side wall of the SiO_2 film (Figure 4.1f). Afterwards, CVD-grown multilayer h-BN on copper foil ordered from Six Carbon Technology, Shenzhen, was transferred onto the substrate via wet transfer. Another lithography step was used to pattern the h-BN film (Figure 4.1g-h) over the SiO_2 sidewall and graphene edges. Finally, photoresist was spin-coated and patterned for 25 nm Ti/25 nm Au top electrode deposition. After liftoff process, the close-up at the electrode of the fully fabricated Au/Ti/h-BN/Gr(E) memristor is shown in Figure 4.1i.

Wet Transfer Method

I transfer 1 cm by 1 cm samples of 2D materials (graphene and h-BN) onto a pre-patterned Si/SiO_2 wafer using a wet-transfer method: First, the 2D material on copper foil was spin-coated with a thin layer of poly(methyl-methacrylate) (PMMA). Second, I put the PMMA/2D material/copper foil stack into copper etcher (Sigma-Aldrich). After about 20 min, the Cu foil was etched and the PMMA/2D material stack floated on the surface. Third, the resulting PMMA/2D material stack was transferred with a clean blank wafer and cleaned in DI water for 1 h. Fourth, the stack was picked up and transferred into hydrochloric acid (HCl, 2 wt%) for 30 min and DI water for 1 h. After that, it was further cleaned in DI water for 3 times and picked up and transferred onto the target substrate. Fifth, the PMMA/2D material stack on the target wafer was dried naturally in the air and blown up with inert gas gun for 3 min, and then left in the vacuum chamber for 3 h. Finally, the substrate was immersed in acetone overnight to remove the PMMA.

ADF-STEM

To study the vertical memristor, 0.7 μm of carbon film and 2 μm-thick ion-beam induced Pt film were deposited for preventing FIB damage and charging. An electron transparent lamella was prepared with the ThermoScientific Scios DualBeam system. Annular dark field scanning transmission electron microscopy (ADF-STEM) images were acquired using a JEOL NEOARM equipped with a probe corrector for STEM and an EDS. An accelerating voltage of 200kV was used to acquire the images. Figure 4.3a-c show the sample SEM before FIB, the targeted device after FIB, and the ADF-STEM cross-sectional image of the vertical h-BN memristor with graphene edge contact.

Current sweeping method

In the current sweeping method, I sweep current across the device (vertical h-BN memristor) while measuring voltage. Figure 4.5 shows the measured voltage as a function of the sweep current (top) and the extracted conductance as a function of sweeping current (bottom) for several test devices. A sharp transition in voltage translates to a sharp transition in conductance.

Result and Discussion for Vertical H-BN Memristors with Graphene-edge Contacts

The Au/Ti/h-BN/Gr(E) vertical memristors were fabricated on a Si/SiO_2 wafer. First, the bottom Ti/Au electrodes/pads were fabricated using conventional lithography and etching processes. Then, CVD-grown graphene was transferred followed by deposition of 100 nm SiO_2 (isolation). I then patterned and etched the top SiO_2 isolation layer as well as the graphene contacts with ~30 nm recessed SiO_2 substrate to expose the graphene edge in the newly formed SiO_2 sidewall. Subsequently, CVD-grown h-BN (multi-layered) was transferred and patterned to extend over the SiO_2 isolation layer and sidewall with the exposed graphene edge contacts. Finally, I deposited 25 nm Ti and 25 nm Au patterned as

the top electrode using standard lithography/evaporation/lift-off process. Figure 4.2a shows an optical micrograph of the sample with a fully-fabricated array of vertical h-BN memristors with graphene edge contacts. The inset shows a close-up view of one device with active area width (W) of 10 µm. A cross-sectional schematic of the vertical h-BN memristor with graphene edge contacts is shown in Figure 4.2b. Annular dark field scanning transmission electron microscopy (ADF-STEM) images in Figure 4.2c-e reveal the critical h-BN switching layers as well as the graphene (Gr) edge contact. Additional images are provided as shown in Figure 4.3

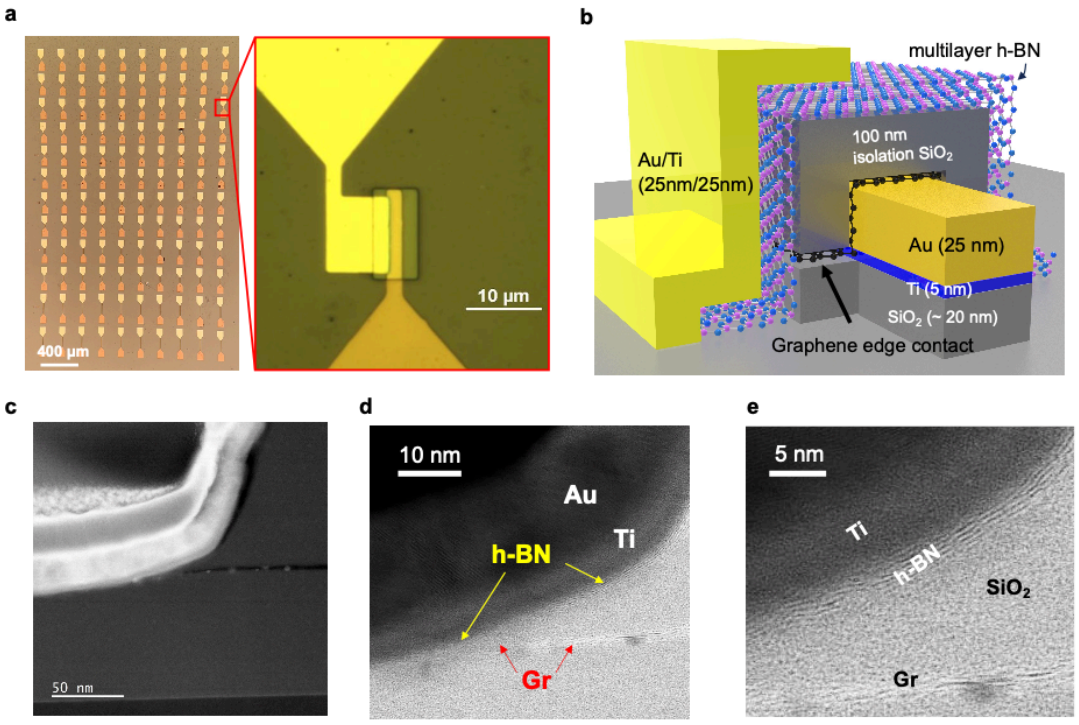

Figure 4.2(a) Optical micrograph of fully fabricated devices array with different active widths. The insert in red box shows the single device with active width equals to 10 µm. (b) Schematic of the vertical h-BN memristor with graphene-edge contact. (c) Annular dark field and bright field (d, e) scanning transmission electron microscope (ADF-STEM and ABF-STEM) images at different magnification levels revels.

To investigate the resistive switching (RS) behavior of vertical h-BN memristor with graphene edge contact, standard dual-sweep current-voltage (I-V) measurements were

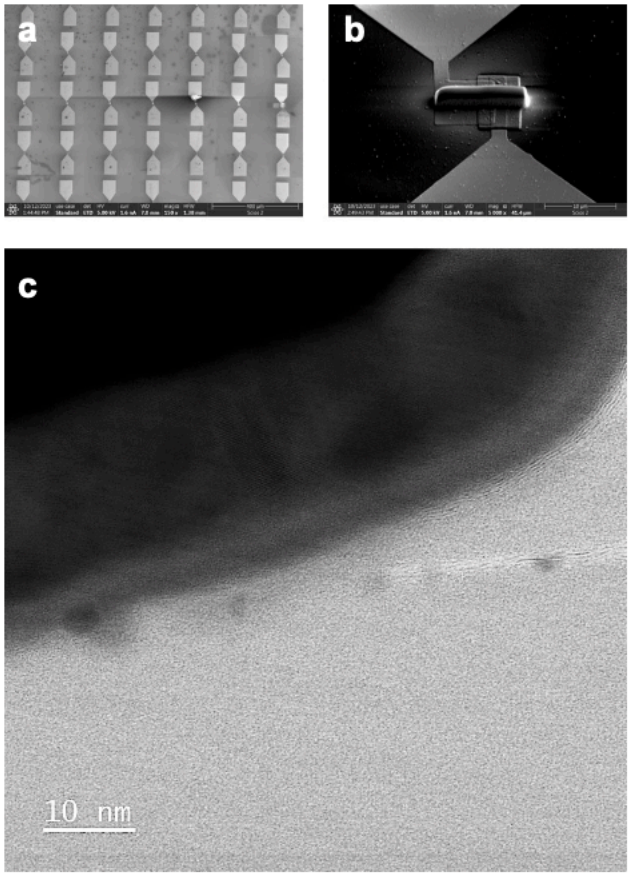

Figure 4.3 Sample preparation (FIB) and annular dark field scanning transmission electron microscopy (ADF-STEM) images of the vertical h-BN memristor with graphene edge contact.

conducted. In these measurements, the bottom electrode is grounded while the top electrode is swept in positive and negative directions while measuring current across the device. Typical dual-sweep I-V characteristics are shown in Figure 4.4a over multiple (45) cycles measured at room temperature (300 K) for a vertical h-BN memristor with active region W = 20 μm. A current compliance (CC) was used to limit the current during the positive side of the voltage sweep held at I_{CC} = 10 μA. The measurements reveal forming-free bipolar NVRS behavior with extremely low off-state (HRS) current in the pico-ampere (read at 0.1 V) range. This observation confirms negligible leakage attributed to atomically

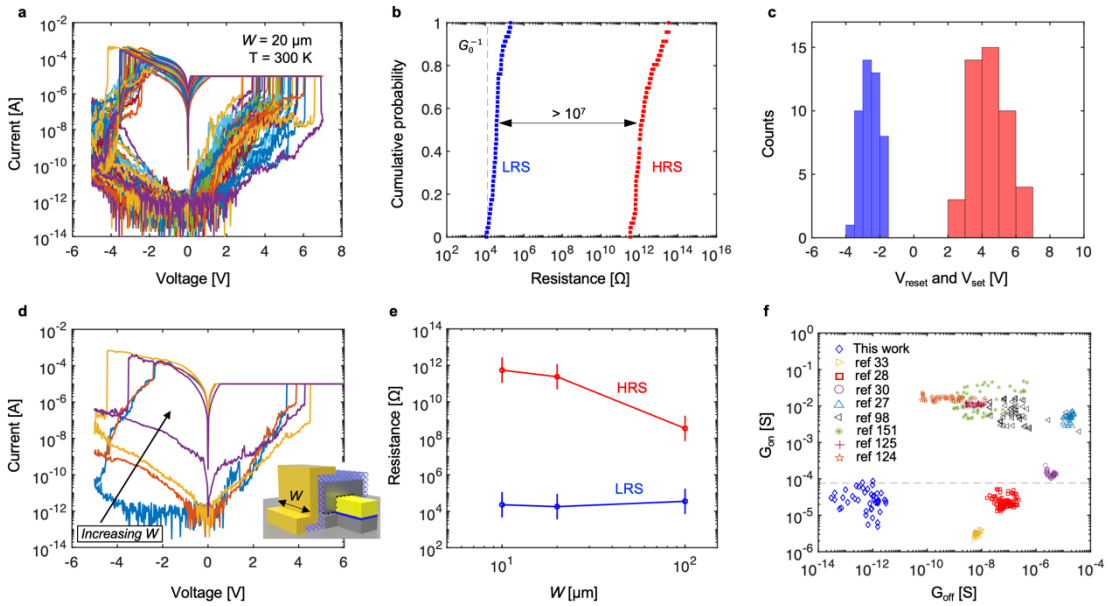

Figure 4.4 (a) Representative 45 consecutive I-V curves showing bipolar RS in Au/Ti/h-BN/GrEdge memristor with W = 20 μm and CC = 10 μA. (b) Cumulative probability distribution of HRS and LRS (read at 0.1 V). (c) Histogram of set and reset voltages. (d) I-V curves of Au/Ti/h-BN/GrEdge memristor showing the HRS trend with increasing the W. The inset show the device structure with W indicated on the schematic. (e) Statistical analysis of HRS and LRS as a function of W. (f) G_{on} versus G_{off} comparison for h-BN memristors.

thin graphene edge contact and ultrasmall active area for vertical h-BN memristors. A closer look at the (cycle-to-cycle) statistical behavior is provided in Figures 4.4b-c. Cumulative distributions of resistance in the high-resistance state (HRS) and low-resistance state (LRS) from all 45 dual-sweep I-V cycles are plotted in Figure 4.4b. These values are extracted at a read voltage of 0.1 V. The cumulative distributions indicate a large on/off ratio > 10^7, which is significantly larger than what is typically obtained in planar h-BN memristors[97], but also much larger than what is typically reported on oxide-based vertical RRAM[145,146]. A large HRS/LRS ratio (memory window) is desirable for stability, capacity, and reliable crossbar array implementation[147,148]. The dispersion in each of the distributions (HRS and LRS) is only slightly over a decade in resistance, which is a much smaller range compared to the memory window. Also indicated in Figure 4.4b (dashed line)

is the value for the quantum resistance $G_0^{-1} = (2q^2/h)^{-1} \approx 12.9$ kΩ, where q is the electronic charge and h is Planck's constant. The fact that LRS resistance is near G_0^{-1} indicates atomic-scale CNF operation with single or few conductive paths in effect (small active area). Instead, earlier work on planar h-BN memristors show HRS resistance near G_0^{-1} (and HRS/LRS ratios ~ 10-1000) because of incomplete control over CNFs with many existing paths over large active areas[149]. Figure 4.4c are histograms of set and reset voltages obtained from all 45 cycles of I-V measurements on the vertical h-BN memristors. The histograms show an average set voltage of approximately V_{set} = 4 V, and average reset voltage of approximately V_{reset} = –2.5 V. While V_{set} distribution is slightly wider than V_{reset} a sufficient voltage range (~ $\pm$2V) is available for read or IMC operations without disturbing the cell. These V_{set}/V_{reset} values are larger than those in memristors with planar sandwiched structures. As previously reported[97], set and reset voltages can increase as active areas are shrunk down due to reduced number of active native defects for CNF behavior. In this work I study NVRS in ultrasmall active areas using atomically thin graphene edge contact as the bottom electrode, so it is reasonable that V_{set}/V_{reset} voltages are slightly higher.

Figures 4.4d-e provide more evidence of filamentary NVRS behavior. Figure 4.4d shows dual-sweep I-V measurements from vertical h-BN memristors with increasing active area width (W). Increasing W results in more current in the HRS (easier to observe for negative voltages), but LRS is mostly unaffected. This is confirmed in Figure 4.4e where it plots extractions of HRS and LRS resistance (extracted at V_{read} = –1 V), and plot them as a function of W. The error bars account for device-to-device variation (~ 1 decade in resistance) based on measurements of identical devices. As shown, HRS resistance

increased with reducing the active area (W), but LRS resistance is mostly unaffected, indicative of filamentary NVRS[150]. Figure 4.4f compares HRS and LRS conductance (G_{on} and G_{off} for LRS and HRS respectively) from vertical h-BN memristors reported in this work against previous reports from planar h-BN memristors[27,28,30,33,98,124,125,151]. Clearly, our vertical h-BN memristors with graphene edge contacts achieve the smallest G_{off} because of the ultrasmall active area. It also achieves one of the smallest G_{on} (at or slightly below G_0) as conductive paths are better isolated to single of few atomic-scale CNFs. The smaller G_{on} reported by Zhu *et al*[33] is due to a one-transistor one-memristor (1T1M) configuration where the transistor acts as a current limit (i.e., limits LRS conductance).

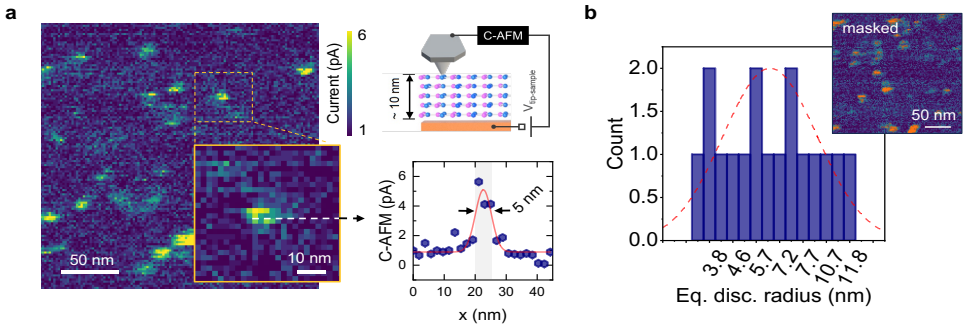

Figure 4.5(a) Conductive map of the h-BN sample obtained by conductive atomic force microscopy (c-AFM). The signal is collected with the probe grounded and the bias (6 V) applied to the sample's bottom electrode as depicted in the inset (top). Detailed view of a conductive spot is reported (inset bottom) to show actual size of the defect size. (b) The statistical distribution of spot sizes is obtained from the 2D c-AFM map shown in the inset.

To better understand NVRS behavior resulting from atomic-scale CNF operation in vertical h-BN memristors with graphene edge contacts, I use a current sweeping method. In this method, instead of sweeping voltage and measuring current I sweep the current across the device while monitoring the voltage. The current sweeping mode can suppress the effect of current overshoot, thereby enabling a self-compliant set process[152] to better observe formation of atomic-scale CNFs and corresponding quantized steps in

conductance. This method was previously employed in other (amorphous) material systems with filamentary NVRS behavior to characterize quantized conductance steps as a function of current[152,153]. In those devices, the current sweeping method allows gradual thickening of CNFs (because of limiting current overshoot) resulting in quantized steps of the conductance (multiple steps in units of G_0)[152–155]. Here, the switching material is polycrystalline CVD-grown h-BN (multi-layered) where CNFs are formed at the location of native defects (e.g., grain boundaries) that are surrounded by insulating regions of crystalline h-BN[30,143,144]. Thus, in CVD-grown h-BN memristors, the CNFs are already limited in thickness to atomically-constrained native defect. To estimate the lateral dimensions of conductive defects sites in h-BN, I used high sensitivity conductive atomic force microscopy (c-AFM). Here, a nanosized conductive (Pt coated) AFM probe is scanned in direct contact with the h-BN surface while a voltage is applied to the tip-sample system (inset Figure 4.5a). Figure 4.5a shows multiple conductive spots that are natively present on the h-BN surface. The size of the spots is reported in Figure 4.5b where it shows the distribution of the spots size obtained for a 500 x 500 nm^2 region. Although the shape of the conductive spots is not perfectly circular, for the sake of simplicity, I extract for each spot the equivalent disc radius as shown in Figure 4.5b. It is worth noting that actual spots size is slightly smaller than the measured values. The reason for this overestimation can be found in a non-negligible lateral tip-sample electronic leakage that occurs while the moving tip is approaching the conductive spots. This is considered to introduce ~1 nm overestimation on the electrical convolution of the spots (i.e., h-BN defect sites).

Based on our c-AFM observations, Figure 4.6a depicts the atomically-constrained CNF behavior in CVD-grown h-BN with a cross-sectional schematic diagram (top-view) of the

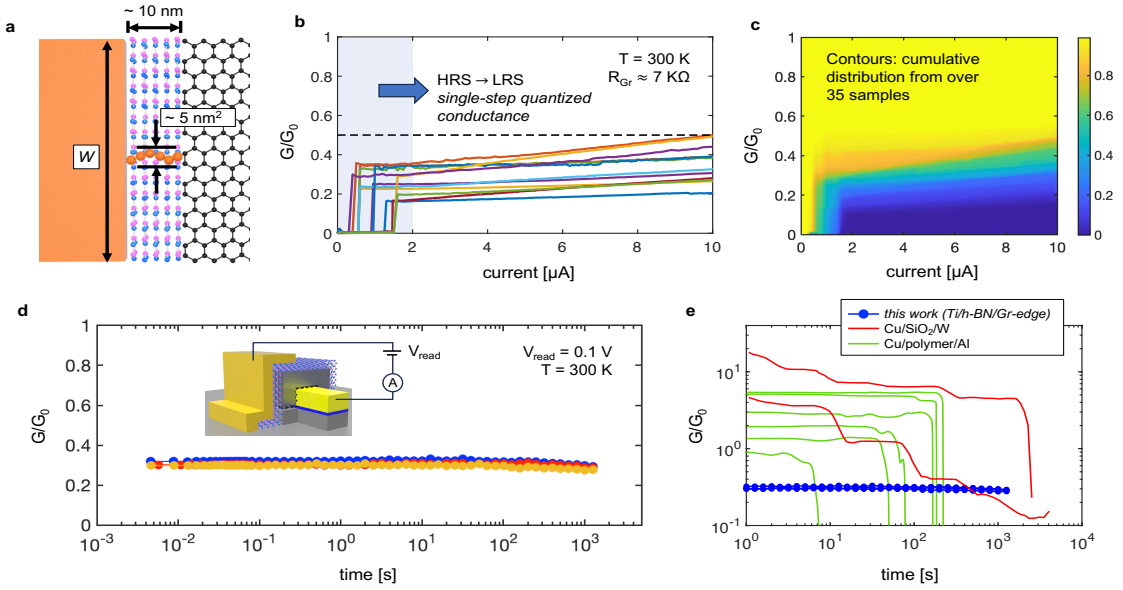

Figure 4.6(a) Schematic of the device from top view showing the formation of the conductive path in h-BN from Ti to graphene. (b) Single-step conductance change of Au/Ti/h-BN/Gr-edge vertical devices based on current sweep measurements. (c) Contours plot of conductance cumulative distribution vs current from over 35 samples. (d) Conductance retention measurements at room temperature with V_{read} = 0.1 V. (e) Comparison of vertical h-BN memristors retention with planar devices with amorphous switching layers.

active region where the graphene edge contacts h-BN. Considering the thickness of the graphene contact and the typical area of conductive regions in CVD-grown h-BN (Figure 4.5) I estimate CNF cross-sectional areas limited to a few nm^2. Figure 4.6b plots the conductance (in units of G_0) obtained as a function of sweep current for multiple devices with various *W*. A few interesting observations are made. *Firstly*, a single step in conductance is measured occurring at small programming currents (< 2 μA) with no additional steps with increasing current. This contrasts what was observed on amorphous materials where multiple steps in conductance at similar intervals in programming current were obtained as filament becomes thicker consistent with quantum point contact (QPC) theory[154]. I attribute the existence of a single step to the unique atomically-constrained CNF behavior of CVD-grown h-BN (similar behavior expected in other CVD-grown 2D layered

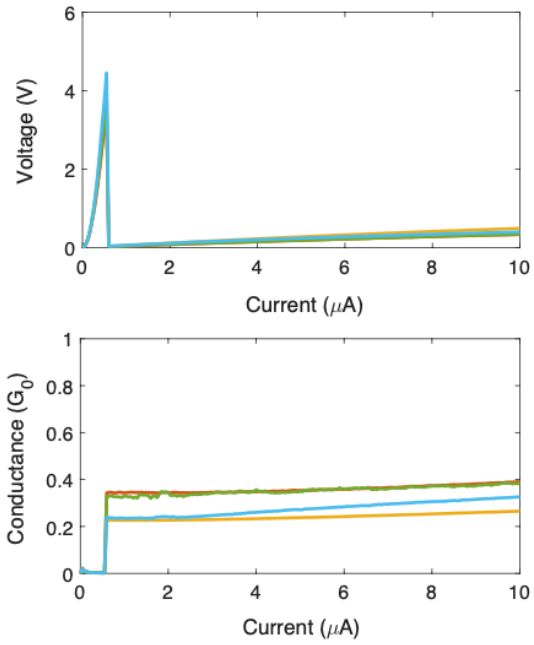

Figure 4.7 The current sweeping method

materials like TMDs), which limits the thickness of the conductive paths. However, I consider that this behavior is only attainable in the vertical h-BN memristors (as opposed to planar h-BN memristors) due to the ultrasmall active area which allows isolating single CNFs. *Secondly*, similar behavior is observed for devices with different *W* ranging from 10 μm up to 100 μm. Although this may not be surprising given the filamentary behavior of the device. I speculate that even in devices with different *W* only a single CNF is formed during the current sweep. Once formed (at the transition of conductance) I observe a sharp drop in the measured voltage to sustain the same amount of current, as you can see in Figure 4.7. *Thirdly*, the measured step in conductance is only a fraction of G_0. Previous work has reported "subquantum" conductance in devices with semiconducting materials used to form the conductive paths[156]. Here, I attribute the sub-G_0 conductance in h-BN memristors to quasi-ballistic transport resulting from scattering in metallic CNFs (in this case Ti CNFs) formed across the defect-rich ~5 nm h-BN thickness. I account for an estimated graphene

contact resistance of approximately 7 kΩ considering that significant current crowding effects may exist as the conductive path is limited to single CNF in the h-BN layers. A different visualization of the device-to-device variability in current-sweep programming is provided in Figure 4.6c where it plots contours of conductance as a function of programming current from over 35 devices.

Finally, I study the robustness of atomically-constrained CNFs in vertical h-BN memristors with graphene edge contacts by measurements of retention in quantized conductance. Previous work[30,143,144] has proposed that the unique NVRS behavior in CVD-grown h-BN, where CNFs are formed in pre-existing defective regions surrounded by insulating crystalline h-BN grains, could enhance robustness compared to amorphous materials where filaments are more susceptible to naturally dissolve. Indeed, devices with amorphous switching layers have shown the effect of naturally dissolving filaments as a spontaneous decay towards HRS in quantized conductance steps[152,153]. Here, the retention tests were conducted on a few vertical h-BN memristors immediately after programming to LRS with the current sweeping method. In the retention test I apply a fixed small read voltage of 0.1 V and sample current in logarithmic steps to cover a wide time range from approximately 5 ms up to 12.5 ks. The results are shown in Figure 4.6d where it plots conductance (units of G_0) vs time showing negligible drift (inset shows the test biasing conditions). To compare against other metal-ion based resistive switching devices (i.e., Cu/SiO_2/W and Cu/polymer/Al) it replots conductance vs time in Figure 4.6e including the measurements from these two other technologies. For each case, there are a few different retention measurements from devices programmed to different values of conductance near G_0. The comparison indicates that the vertical h-BN memristors can achieve better

retention (even at lower G, which typically limits retention) compared to the other devices with amorphous switching layers where spontaneous decay is observed.

Conclusion

In conclusion, I have introduced, fabricated, and characterized vertical h-BN memristors with graphene edge contacts. In this configuration, the proposed structure delivers ultralow power by isolating single conductive nanofilaments (CNFs) in ultrasmall active areas having negligible leakage. Statistics for the NVRS behavior of vertical h-BN memristors with graphene edge contacts are presented, as well as the dependence on graphene edge contact width (W). The measured devices achieve orders-of-magnitude improvements in on/off ratio and low current operation compared to planar h-BN memristors. Moreover, the ultrasmall active area facilitates studying quantum behavior of atomically-constrained CNF operation in CVD-grown h-BN switching layers. Here, single-step subquantum conductance is observed and analyzed, and the robustness of atomically-constrained CNFs is tested by retention measurements. Compared against other metal-ion based resistive switching devices, the vertical h-BN memristors show better stability. This is attributed to the unique NVRS behavior in CVD-grown h-BN, where CNFs are formed in pre-existing defective regions surrounded by highly-stable insulating crystalline h-BN grains. The proposed vertical h-BN memristor technology is promising for future 3D integrated (vertically stacked) 2D-material-based ultralow power RRAM.

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

Summary of Contributions

This dissertation focuses on addressing and elucidating the issues of scaling down devices and current computing system and exploring 2DMs based RRAM as possible solution through innovation in device materials and structures.

Chapter 2 focuses on CVD-grown ML MoS_2 FETs. In this part, CVD-grown ML MoS_2 was utilized to fabricate FET arrays. Two different types of metal contacts were used to analyze the temperature-dependent electrical characteristics and their corresponding Schottky barrier characteristics. Statistical analysis provides new insight about the properties of metal contacts on CVD-grown MoS_2 compared to exfoliated samples. Reduced Schottky barrier heights are obtained compared to exfoliated flakes, attributed to a defect-induced enhancement in metallization of CVD-grown samples. Moreover, the dependence of SBH on metal work function indicates a reduction in Fermi level pinning compared to exfoliated flakes, moving towards the Schottky-Mott limit. Optical characterization reveals higher defect concentrations in CVD-grown samples supporting a defect-induced metallization enhancement effect consistent with the electrical SHB experiments.

Chapter 3 focuses on CVD-grown h-BN memristors with planar structure for dot-product implementation and linear regression. Multilayer CVD-grown h-BN memristor arrays were fabricated and characterized. Statistics for the non-volatile resistive switching behavior of h-BN memristors, including effects of cell active areas, were presented. It then focuses on the non-volatile multi-state pulse programmability of the h-BN memristors

based on multiple cycles of consecutive programming pulses, and retention tests. The implementation of the dot-product operation on h-BN memristor arrays were also demonstrated, which shows good linearity and repeatability. Moreover, I have demonstrated the hardware implementation of stochastic multi-variable linear regression on the h-BN memristor array. This linear regression shows good convergence and represents an important milestone in advancing the research and implementation of 2DMs for machine learning hardware.

Chapter 4 focuses on vertical CVD-grown h-BN memristors with graphene edge contacts. In this part, I introduced, fabricated, and characterized vertical h-BN memristors with graphene edge contacts to achieve atomic-level miniaturization. The proposed vertical structure delivers ultralow power by isolating single conductive nanofilaments in ultrasmall active areas having negligible leakage. I presented statistics for the non-volatile resistive switching behavior of vertical h-BN memristors. The measured devices achieve orders-of-magnitude improvements in on/off ratio and low current at HRS compared to planar h-BN memristors. Moreover, the ultrasmall active area facilitates studying quantum behavior of atomically-constrained CNFs operation in CVD-grown h-BN switching layers. The single-step subquantum conductance is observed and analyzed as well as the robustness of the atomically-constrained CNFs are tested via retention measurements. The unique non-volatile resistive switching behavior in CVD-grown h-BN, where CNFs are formed in pre-existing defective regions surrounded by high-stable insulating crystalline h-BN grains, provides the vertical h-BN memristors with better stability compared against other metal-ion based resistive switching devices. The proposed vertical h-BN memristor technology is promising for future 3D integration of 2DMs-based ultralow power RRAM.

Future Works

Plasma-Enhanced CVD (PECVD) H-BN for Memristors

Since the emergence of 2DMs, various synthetic protocols for h-BN have been developed, such as mechanical exfoliation, solution exfoliation, and chemical vapor deposition (CVD), etc. However, these methods have some disadvantages that impede the practical applications of h-BN based memristors. Mechanically exfoliated h-BN flakes from bulk, while it exhibits remarkable properties such as excellent electrical insulation and high thermal conductivity, face significant limitations when it comes to large-scale fabrication. Additionally, inherently good crystallinity of mechanically exfoliated h-BN flakes, characterized by fewer vacancies and grain boundaries, is unfavorable for the formation of conductive filaments under applied stress-voltage, resulting in limited switching cycles, reduced reliability, or even hard breakdown of the h-BN flakes.

Currently, chemical vapor deposition (CVD) is widely used and regarded as the most effective method for h-BN thin film synthesis for memristive electronic applications, yielding both large-scale and high-quality results. However, CVD technique often necessitates the use of catalyst metals, such as Cu, Ni, or Pt for the synthesis of h-BN thin film. This requirement results in the post-synthesis wet transfer process instead of direct growth of h-BN thin films on the target surfaces, which leads to increased cost and the potential for introducing contaminations, breakage, wrinkles, and non-conformity, especially for features with high aspect ratio, to the transferred h-BN thin films on the pre-patterned substrates. Moreover, the high operating temperature of CVD technique, approximately 1000 °C, is not energy-efficient, nor is it compatible with the back-end-of-line (BEOL) CMOS integration processes, which is typically limited to lower temperatures

(around 400 °C) to avoid damage to the already-formed delicate features and interconnections.

Plasma-enhanced chemical vapor deposition (PECVD) is an attractive technology in that high-energy plasma can decompose precursors into highly reactive species at temperatures ranging from 200 °C to 400 °C lower than conventional CVD, making it energy-efficient, low cost, and compatible with industrial microelectronics[157]. Furthermore, PECVD technique enables the catalyst-free growth of h-BN thin films directly on various noncatalytic substrates, such as SiO_2/Si, which achieves transfer-free preparation of h-BN thin films on target substrates with clean surfaces. Finally, h-BN thin films directly deposited by PECVD method are highly conformal, which facilitates the applications of h-BN in the 3D stacking memristors with high aspect ratio[158]. Till now, there has been no instance of catalyst-free deposition of h-BN thin film onto a pre-patterned target substrate using the PECVD method for the purpose of memristor applications. Based on the ideas mentioned above, h-BN thin film grown by PECVD method directly on pre-patterned substrate for memristor applications will be further explored in the future.

Vertical H-BN Memristors Based Crossbar Arrays

The exponential growth of data poses significant challenges to traditional CMOS-based memory technology due to Moore's law approaching its limits and the accompanying high energy consumption, as well as to the traditional von Neumann computing system, which incurs high costs from frequent data movement between processor and memory[159,160]. Innovative memory storage techniques and computing architectures are essential to satisfy the ever-growing demand for data storage and information processing. Neuromorphic

computing, or brain-inspired computing, which emulates the structure and working mechanisms of the human brain, has emerged as an innovative computing paradigm to address these challenges. One popular approach, focused on collocating memory and computing functions, uses beyond-CMOS technology to overcome the challenges associated with traditional computing architectures[6,159,160]. This approach facilitates in-memory computing, where massive amounts of data are processed in parallel, potentially minimizing the need for extensive data movement and thereby offering a promising solution for current and future computing demands[6,160]. To achieve efficient neuromorphic computing, the memristor crossbar array (MCBA) offers high-density integration and capabilities of parallel vector-matrix multiplication with ultra-low energy in in-memory computing. As one of the promising 2DMs, h-BN has attracted much attention for various electronic applications. Recently, h-BN-based MCBAs have been widely investigated owing to the unique properties of h-BN that contribute to resistive switching behavior. To the best of my knowledge, the reported work on h-BN based MCBA primarily involves a planar metal-insulator-metal (MIM) structure, wherein the CVD-grown 2D h-BN is transferred and sandwiched between top and bottom electrodes. However, significant challenges in achieving large-scale and efficient MCBA are the sneak path current issue, which reduces the reliability of MCBA by introducing errors when programming or reading the resistance state of the memristors[161], as well as limited HRS resistance (large OFF-state leakage current). On the other hand, scaling down the active area of each memristor in the crossbar array is limited by the resolution of lithography, as mentioned in the introduction of Chapter 4. This limitation hinders the ultimate high-density integration

of the MCBA and potentially exposes additional paths within the active area for sneak currents through the non-target memristors in high resistance states.

Thanks to one of the unique properties of 2DMs with the capability to scale down to atomically-thin thickness (i.e., 0.3 nm of single layer graphene), vertical h-BN memristors with graphene-edge contact (h-BN/GrE) provide new opportunities for MCBA towards in-memory and neuromorphic computing. Firstly, the large ratio between ON state (low resistance state, LRS) and OFF state (high resistance state, HRS) achieved by h-BN/GrE (discussed in Chapter 4) enables easier differentiation between the two states, which is crucial in the MCBA to ensure accurate data readout. Secondly, the extremely low current in HRS of h-BN/GrE memristor is essential to minimize leakage and potential sneak path conduction, which occur when current inadvertently flows through unintended paths. By combining these two properties, h-BN/GrE memristors are expected to increase energy efficiency and data readout accuracy for large-scale MCBA, as opposed to arrays made with memristors that have planar electrode contacts. Therefore, h-BN/GrE based MCBA shows promise for use in in-memory and neuromorphic computing applications and should be further investigated. This future work is a straightforward continuation of my research on vertical h-BN memristor with graphene-edge contact detailed in Chapter 4.

3D Stacking of H-BN-based Memristors

With the rapid development of emerging technologies such as artificial intelligence (AI), Internet of Things (IoT), and big data, the ever-growing demand for massive data storage as well as Moore's law approaching its limit impose significant challenges to conventional charge-based CMOS memory technology such as NAND flash memory,

which is currently widely used in smartphones and solid-state drives (SSDs)[162]. As the pressures of lateral scaling increase in two-dimensional (2D) planar NAND, the industry has shifted to vertical stacking of memory cells in the third dimension (3D) to achieve ultra-high bit density, transforming the 2D planar design into a 3D 'skyscraper' on the wafer (i.e., 3D vertical NAND). In addition to lateral and vertical scaling, multi-level cell programming strategy and error-correction algorithms have been developed to expand and ensure the storage capacity. Similarly, to compete with 3D vertical NAND technology, 3D memristor (also called RRAM) needs to be investigated and developed owing to its excellent properties in feature size scaling, simple fabrication, low per-bit cost, better endurance and retention, fast operating speed, and lower energy consumption for next-generation non-volatile memory[36]. In addition to the applications on memory technology, 3D memristors could also be integrated towards computing circuits for massive connections and efficient communications required to unleash the full potential of neuromorphic computing[163]. In terms of architecture, 3D memristor can be categorized as 3D horizontal memristor (3D H-RRAM) and 3D vertical memristor (3D V-RRAM)[34,162]. However, 3D V-RRAM outperforms 3D H-RRAM in terms of cost due to its fewer lithography processes, while the number of critical lithography masks required for 3D H-RRAM increases linearly with the number of stacked layers, particularly when the layer count exceeds 32[34,162].

From material perspective, hexagonal boron nitride (h-BN) is a promising candidate for 3D RRAM technology. Firstly, due to the unique property, the conductive filaments can form along the grain boundaries surrounded by stable 2D-layered crystalline h-BN, which facilitates stable resistive switching behavior and enhances retention robustness.

Secondly, CMOS-compatible, PECVD-grown h-BN thin film, which can be directly deposited onto the pre-patterned substrates without transfer processes, offers lower synthesis temperature, reduced energy-consumption, contaminant-free, and highly conformal contact to vertical trenches with high aspect ratios in 3D vertical RRAM. From structure perspective, as previously mentioned, vertical h-BN/GrE memristors offer a large memory window, potentially providing good conductance programmability across a wide range of operating currents for multi-level cell applications[30]. Therefore, 3D vertical RRAM based on PECVD-grown h-BN/GrE memristors shows many potential opportunities for the future work.

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