Load-Sharing Low-Dropout Linear Regulators and Time-Domain Switching Regulators

by

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ABSTRACT

The development of portable electronic systems has been a fundamental factor to the emergence of new applications including ubiquitous smart devices, self-driving vehicles. Power-Management Integrated Circuits (PMICs) which are a key component of such systems must maintain high efficiency and reliability for the final system to be appealing from a size and cost perspective. As technology advances, such portable systems require high output currents at low voltages from their PMICs leading to thermal reliability concerns. The reliability and power integrity of PMICs in such systems also degrades when operated in harsh environments. This dissertation presents solutions to solve two such reliability problems.

The first part of this work presents a scalable, daisy-chain solution to parallelize multiple low-dropout linear (LDO) regulators to increase the total output current at low voltages. This printed circuit board (PCB) friendly approach achieves output current sharing without the need for any off-chip active or passive components or matched PCB traces thus reducing the overall system cost. Fully integrated current sensing based on dynamic element matching eliminates the need for any off-chip current sensing components. A current sharing accuracy of 2.613% and 2.789% for output voltages of 3V and 1V respectively and an output current of 2A per LDO are measured for the parallel LDO system implemented in a 0.18μm process. Thermal images demonstrate that the parallel LDO system achieves thermal equilibrium and stable reliable operation.

The remainder of the thesis deals with time-domain switching regulators for high-reliability applications. A time-domain based buck and boost controller with time as the processing variable is developed for use in harsh environments. The controller features adaptive on-time / off-time generation for quasi-constant switching frequency and a time-domain comparator to implement current-mode hysteretic control. A triple redundant

bandgap reference is also developed to mitigate the effects of radiation. Measurement results are showcased for a buck and boost converter with a common controller IC implemented in a 0.18μm process and an external power stage. The converter achieves a peak efficiency of 92.22% as a buck for an output current of 5A and an output voltage of 5V. Similarly, the converter achieves an efficiency of 95.97% as a boost for an output current of 1.25A and an output voltage of 30.4V.

DEDICATION

To my inspiring dad, loving mom, my amazing brother, and my dear friends,

without whom none of my success would be possible!

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I wish to express my sincerest gratitude to my advisor, Prof. Bertan Bakkaloglu for his continual unwavering support throughout my masters and doctoral studies. His guidance towards my professional and personal development has been invaluable. His constant motivation at each phase in this journey has been a key driving factors throughout my research and his compassionate and humble attitude has been invaluable.

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TABLE OF CONTENTS

Page

CHAPTER Page

LIST OF TABLES

LIST OF FIGURES

Figure Page

Figure Page

Figure Page

CHAPTER 1

INTRODUCTION

The growth and influence of electronics on our everyday life over the last decade has increased exponentially. Sophisticated portable electronic systems have found diverse applications recently from smart home devices, self-driving vehicles, space rockets to health care, medical instrumentation. Power Management ICs (PMICs) are one of the major electronic components that define the performance of such electronic systems.

The main challenge of power management ICs is to increase provide high quality, reliable power to support such sophisticated devices. The exploding number of features on electronics systems especially employed in high performance portable applications is rapidly adding to the amount of processing power. As a result, devices are getting more power thirsty to an extent that power consumption and thermal issues become major limiting factors. The power management of such handheld battery-powered devices is thus becoming increasingly vital.

1.1 Need for Highly Reliable PMICs

Consider a battery-powered PMIC application as shown in Figure 1.1. [1-3] It provides power to various functions such as charging, cellular, bluetooth, processing, display, etc. As shown in Figure 1.2, a typical implementation of a PMIC is consists multiple switching regulators (buck, buck-boost), linear regulators (LDOs) and a central power manager. As device sizes get smaller in accordance with Moore's law and advancements in technology, the absolute voltage levels for these PMICs has dropped radically. However, the power required by these functions has rather increased, leading to higher requirements of output current.

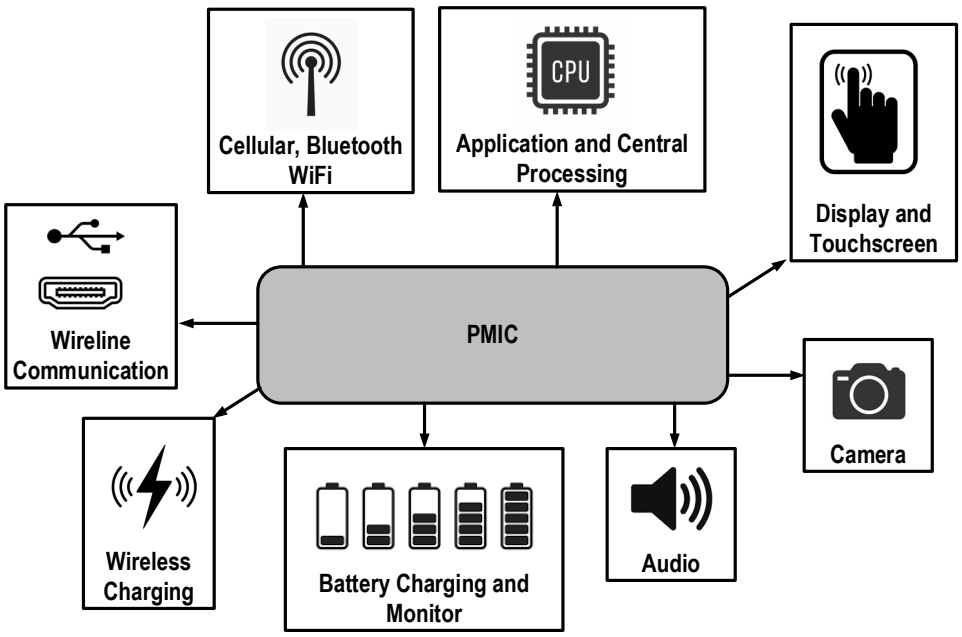
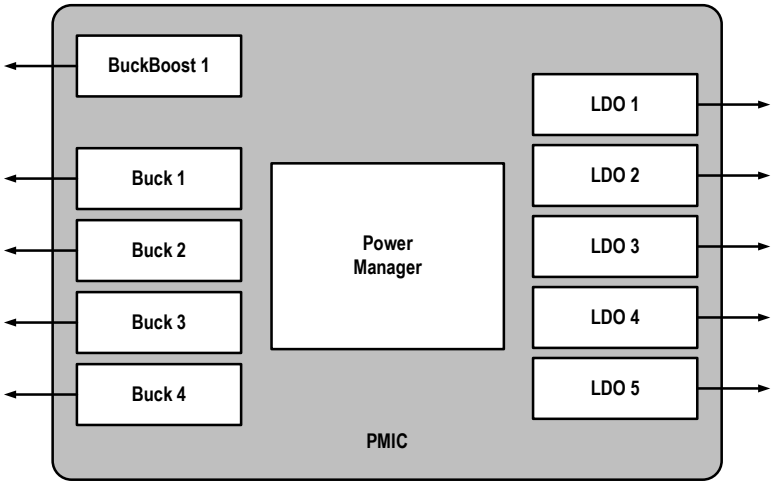


Figure 1.1. Typical PMIC application



with high output currents at low voltages. The reliability of PMICs used in such applications is a challenge to overcome.

1.2 Linear Low-Dropout and Switching Regulators Basics

DC-DC converters form the basis for most of the converters in a typical PMIC application as shown in Figure 1.2. DC-DC converters can be conventionally split as linear or switching regulators.

Linear regulators employ a linear element like a bipolar junction transistor (BJT) or metal-oxide semiconductor transistor (MOS) to regulate the output voltage. They can only be stepped down in voltage levels. A linear regulator has few external parts, low noise, however, dissipates a lot of heat thereby leading to poor efficiency. A low-dropout regulator (LDO) is a type of linear regulator where, the voltage between the V_{IN} and V_{OUT} can be dropped to low values. This leads to reduced energy loss and heat as compared to a conventional linear regulator. A conventional LDO is shown in Figure 1.3. Based on negative feedback, the output voltage of this LDO can thus be written as in Equation (1.1).

$$V_{OUT} = V_{REF}\left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \tag{1.1}$$

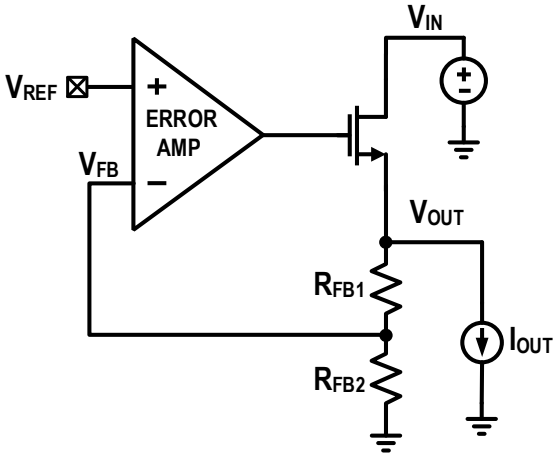


Figure 1.3. Conventional LDO structure

A switching regulator or a switcher employs a switching element to convert a DC voltage to another DC voltage. Switching regulators can be stepped down (buck) or stepped up (boost) in voltage levels and have excellent efficiency. However, switching regulators have a lot of external components, and the more noise on the output due to the switching activity. A basic buck converter is shown in Figure 1.4 where D is the duty cycle of the drive signal to the gate of the switching FET. Based on volt-sec balance, the output voltage of this buck converter is shown in Equation (1.2). Similarly, a basic boost converter is shown in Figure 1.5. Based on volt-sec balance, the output voltage of this boost converter is shown in Equation (1.3).

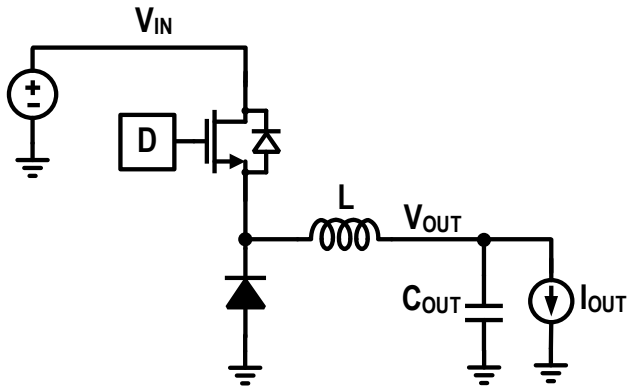
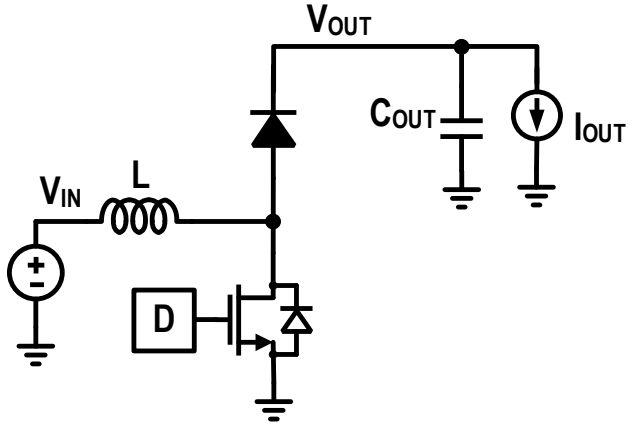


Figure 1.4. Basic buck converter



$$V_{OUT} = V_{IN} * D = V_{IN} * \frac{T_{ON}}{T_S} \qquad (Buck) \qquad (1.2)$$

$$V_{OUT} = \frac{V_{IN}}{1 - D} = V_{IN} * \frac{T_S}{T_{OFF}} \qquad (Boost) \qquad (1.3)$$

1.3 Organization of Thesis

This thesis presents solutions to two reliability problems faced by PMICs – thermal management of a parallel system of low-dropout linear regulators and performance of buck / boost time-domain switching regulators in radiation environments. The thesis is organized as follows.

Chapter 2 discusses the daisy-chain approach to parallelize multiple LDO ICs. The challenges associated with parallelizing regulators and prior art is reviewed. The PCB-friendly approach to parallelize LDO ICs is then presented along with the implementation details. Measurement results of the scalable parallel system and a comparison with prior art is then showcased to conclude the chapter.

Chapter 3 focuses on the design and performance of time-domain switching regulators in high-reliability environments. The basic theory of time-domain processing is first introduced with some prior art. The design and implementation details of the time-domain switching regulator are then discussed. Measurement results of a buck and boost converter using the developed time-domain control are presented to conclude the chapter.

Chapter 4 provide concluding remarks for the two solutions presented in the thesis and suggests future research work in these areas.

CHAPTER 2

LOAD-SHARING LOW-DROPOUT LINEAR REGULATORS

2.1 Introduction and Motivation

The growing demand for high performance and power hungry portable electronic devices has resulted in alarmingly serious thermal concerns in recent times. The power management system of such devices has thus become increasingly more vital. An integral component of this system is a Low-Dropout Linear Regulator (LDO) which inherently generates a low-noise power supply. Such power supplies are crucial for noise sensitive analog blocks like analog-to-digital converters, phase locked loops, and radio-frequency circuits. The efficiency (η) and power loss of a conventional NMOS LDO as shown in Figure 2.1 can be calculated as shown in the Equations (2.1) and (2.2) respectively.

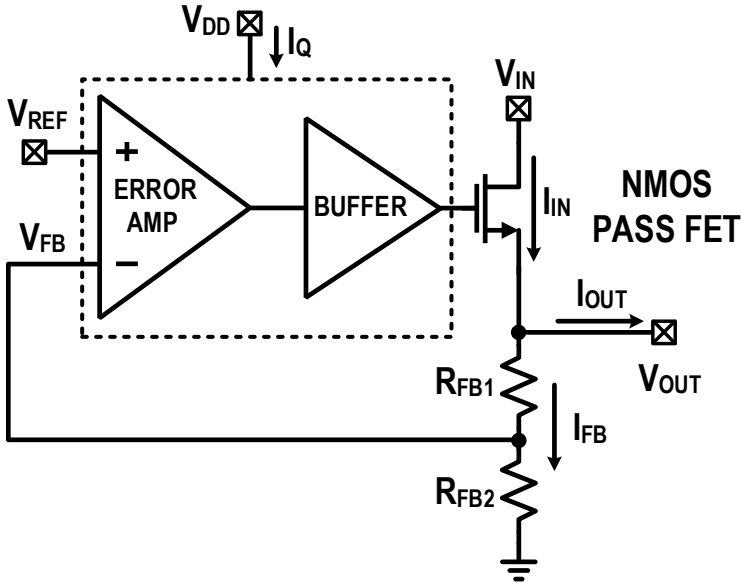


Figure 2.1. Conventional NMOS LDO

$$\eta = \frac{P_{OUT}}{P_{IN} + P_Q} = \frac{V_{OUT} * I_{OUT}}{(V_{IN} * I_{IN}) + (V_{DD} * I_Q)} = \frac{V_{OUT} * I_{OUT}}{(V_{IN} * (I_{OUT} + I_{FB})) + (V_{DD} * I_Q)} \quad (2.1)$$

$$P_{LOSS} = (V_{OUT} - V_{IN}) * I_{IN} + V_{DD} * I_Q \quad (2.2)$$

The efficiency of an ideal LDO can be calculated by neglecting I_{FB} and I_Q as they are small compared to I_{OUT}. With these assumptions for an ideal LDO, almost all the lost power is dissipated in the form of heat in the pass FET. From Equation 2.4, it can be summarized that at higher output power, a single LDO suffers from increased heat dissipation potentially leading to thermal issues.

$$\eta \approx \frac{V_{OUT}}{V_{IN}} \tag{2.3}$$

$$P_{LOSS} \approx (V_{OUT} - V_{IN}) * I_{OUT} \tag{2.4}$$

One solution to circumvent the high heat dissipation and thermal issue of a single LDO supplying high output current is to operate multiple parallel LDOs.

2.2 Prior Art

Parallelizing regulators to equally share and increase the total output current of the system have been shown [4-9] [13] [20-22]. These solutions introduce various control techniques which result in a stable parallel system with improved performance for higher load currents. However, the most compelling challenge with any parallel system is to ensure stable operation with equal distribution for each individual member of the system.

Stable parallel operation can be accomplished by placing all the parallel regulators on a single die [4] [5] [20-22] . The output current is equally shared while preserving stability of the system. This also spread the dissipated heat uniformly across the parallel regulators. For switching regulators, multi-phase control techniques have been discussed specially to improve their output voltage ripple and light load efficiency [4]. LDO regulators have also been paralleled on a single die to increase their output current [5] [20-22] for better transient response. However, such parallel regulators placed on a single die suffer from limited output current from each regulator and thus cannot be scaled for higher load current requirements.

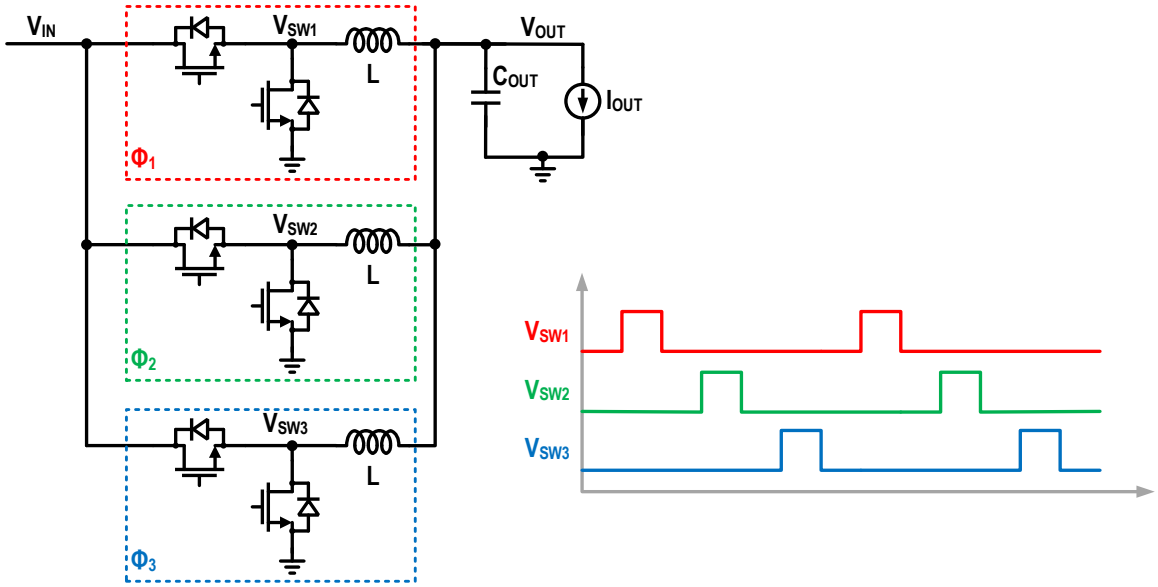


Figure 2.2. Parallel Multi-Phase Switching Regulators

Parallelizing multiple LDO ICs discretely on a PCB instead of on a single die not only provides an opportunity to scale the output current but also distribute the dissipated thermal heat uniformly across the parallel LDOs. The challenge in such a parallel LDO IC system is to equate the output current of each LDO without the loss of stability and regulation.

As shown in Figure 2.3, the simple parallelization of two LDO ICs is a not a trivial solution. LDO-1 and LDO-2 are the same models, however there are variations between the internal components of these LDOs. Advanced manufacturing processes seek to minimize these variations. However, these subtle variations cannot be erased completely. These subtle manufacturing variations both on-chip and off-chip among the parallelized LDOs can cause competition between the parallel LDOs. Even with a common set of feedback resistors, the individual LDOs may regulate at slightly different output voltages. The LDO with the slightly higher output voltage will dominate over the other LDO. This can eventually cause the dominant LDO to deliver majority of the load current [6-9]. These

competing parallel LDOs can induce current limit and thermal shutdown resulting in instability and loss of regulation.

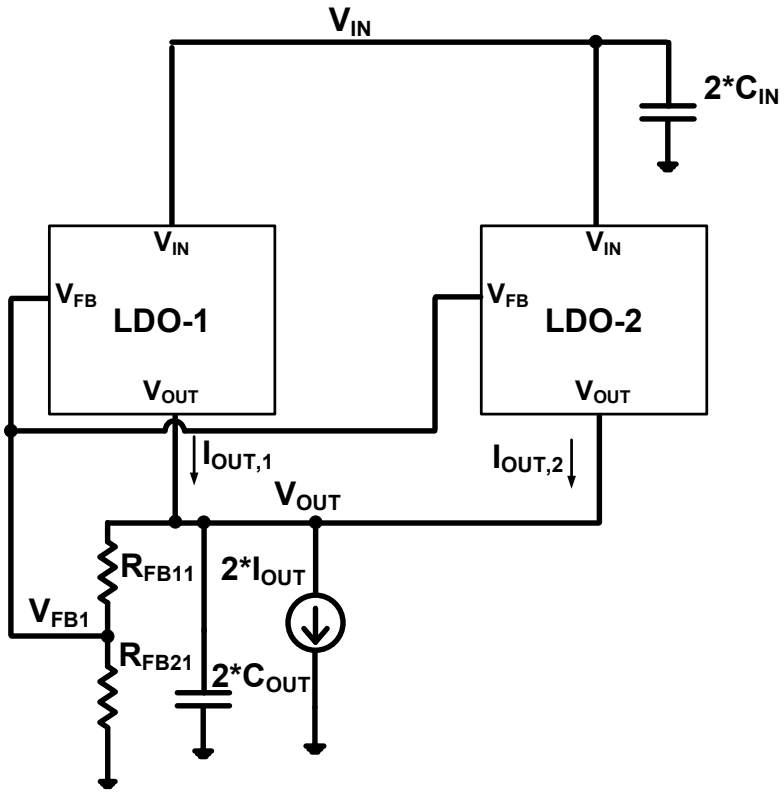


Figure 2.3. Simple Parallelization of LDOs

Discrete LDO ICs have been parallelized by introducing a range of external active and passive PCB components as shown in Figure 2.4. These include ballast resistors, current-sense resistors and amplifiers and employ a master-slave approach for control. In [8], ballast resistors are used in series with the individual LDO outputs to limit the current for stable operation. Three LDOs are parallelized with one TPS7B6750-Q1 acting as the master LDO and two TPS7B4253-Q1 as the slave LDOs for a total output current of 900mA. [9] also presents a solution to parallelize two current reference based LDOs LT3081 for a total load current of 3A with ballast resistors on the output for stable operation and current balancing.

In [6], current-sense resistors are added in series with the input of two TPS74401 LDOs to sense the individual load current of each LDO. A high-precision amplifier OPA333 measures the difference in the sensed currents and modulates the feedback voltage of one of the LDOs to distribute the current equally. Similarly, the solution presented in [9] parallelizes two LT3065 LDOs with the help of a high-precision amplifier LT1637 to supply a total load current of 1A.

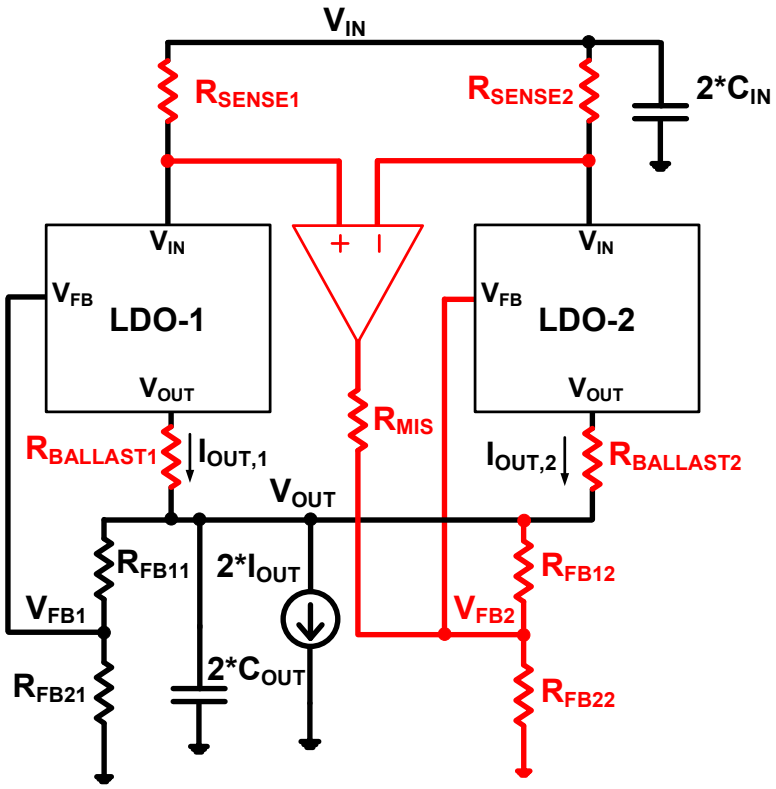


Figure 2.4. Prior Art to Parallelization of LDOs

2.3 Objectives

The prior approaches address the concerns of stability and thermal heat dissipation for a system of parallel LDO ICs. However, they achieve stable parallel operation albeit with the help of additional external active and passive PCB components. These additional PCB components not only limit the scalability of the system to higher

output currents, but also result in a higher system cost. Furthermore, the current sharing accuracy of this approach is purely dependent on the matching of these external off-chip components and the PCB traces themselves. This necessitates the use of high-precision components with tight tolerances for accurate current sharing.

The primary objective of this research topic is to develop a stable system of parallel LDO ICs without the leverage of any external high-precision active or passive components. Moreover, a system that is easily scalable for a higher range of output currents with minimal impact on the total system cost is desired. The final objective is to achieve a current sharing accuracy independent of the matching of external components or PCB traces.

2.4 Daisy-Chain Approach to Parallelize LDOs

2.4.1 Parallel LDO System

Figure 2.5 shows the developed system of parallel LDO ICs with the research objectives discussed in the earlier section. As shown, N similar LDO ICs are paralleled with their respective input voltages and output voltages shorted with each LDO's output current is $I_{OUT,N}$ for a total output current of $N*I_{OUT}$. Correspondingly the input and output capacitance of the entire system is set at $N*C_{IN}$ and $N*C_{OUT}$ respectively.

Each LDO IC in the parallel system has two extra pins for current sensing and monitoring namely I_{SENSE} and I_{MON}. The system features a daisy-chain approach to parallelize multiple LDO ICs. This can be visualized by following the red paths of the sensed and monitored current of each LDO as shown in Figure 2.5. Thus, the sensed current of each LDO is passed to the next LDO in the daisy-chain and the daisy-chain is completed by passing the sensed current of the last LDO in the chain back to the first. As

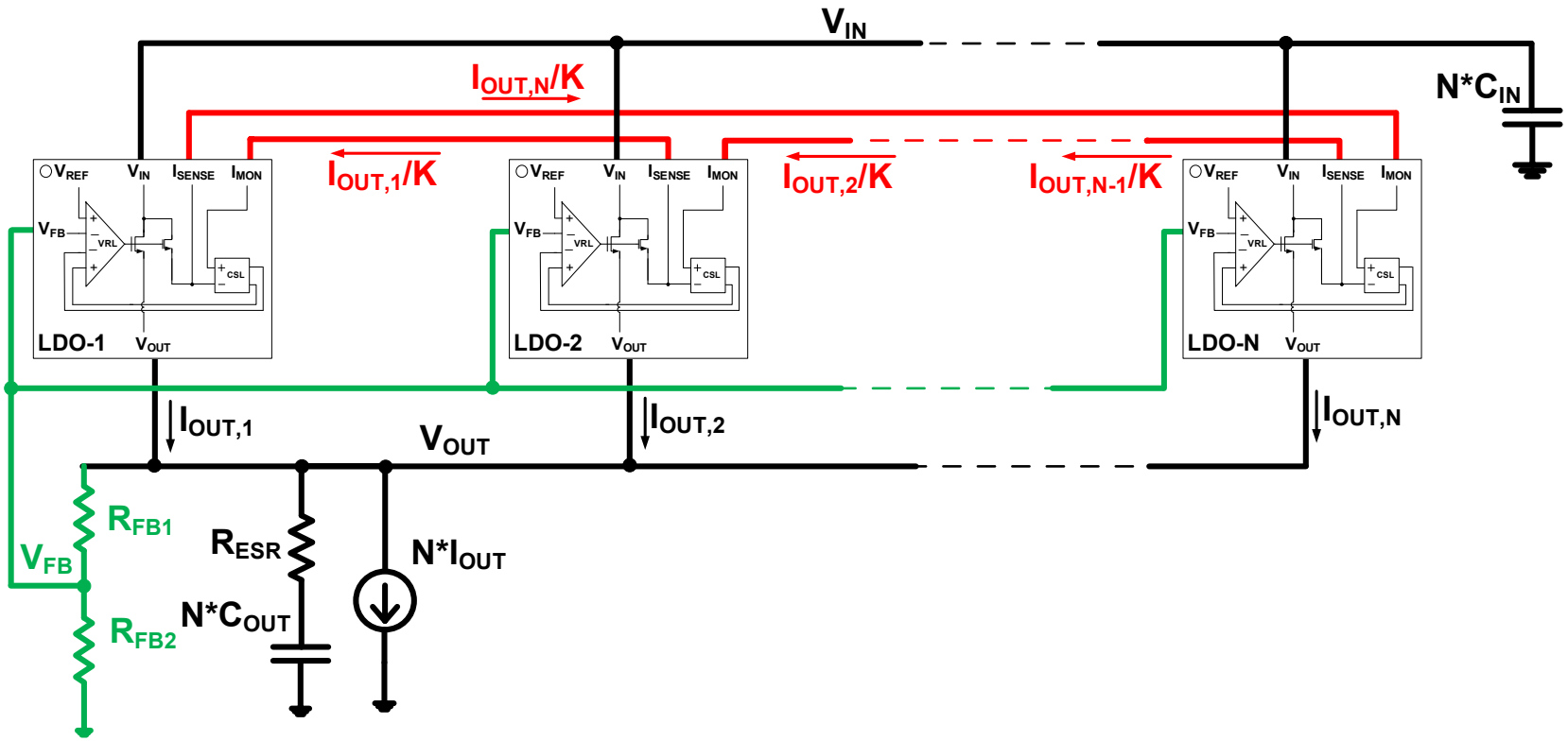


Figure 2.5. Daisy-Chain Approach to Parallelize LDOs

the system relies on a daisy-chain approach, it can be theoretically expanded to any number of parallel LDOs. However, practical considerations of bandwidth and stability of the daisy-chain loop of sensed and monitored currents limits the scalability of the system.

The presented architecture also eliminates the need for any external active or passive components to achieve stable parallel operation. Moreover, this parallel system also utilizes only one set of feedback resistors for all the parallel LDOs therefore reducing the overall size of the system considerably. These features of the presented system result in a considerably reduced cost and size as compared to prior art thus making it extremely PCB-friendly.

Each LDO IC also employs a fully-integrated high-accuracy current sensing which based on dynamic element matching. This approach eliminates the need for any off-chip current sensing resistors further reducing the external component count. The current-based approach to achieve equal output currents eliminates the need for any matched PCB traces for current sharing. Thus, the current sharing accuracy of the presented system of parallel LDOs is dependent on on-chip and not off-chip components. Moreover, employing better and efficient layout techniques coupled with advancements in manufacturing processes have led to better matching of on-chip structures. This results in an overall higher current sharing accuracy as compared to prior art.

2.4.2 Individual LDO

As shown in Figure 2.6, each individual LDO IC in the daisy-chain is the same and its implementation consist of three major blocks namely the core voltage regulation loop (VRL), the auxiliary current servo loop (CSL), and the integrated current sensing based on DEM. The target specifications for each individual LDO IC in the daisy chain are shown in Table 2.1.

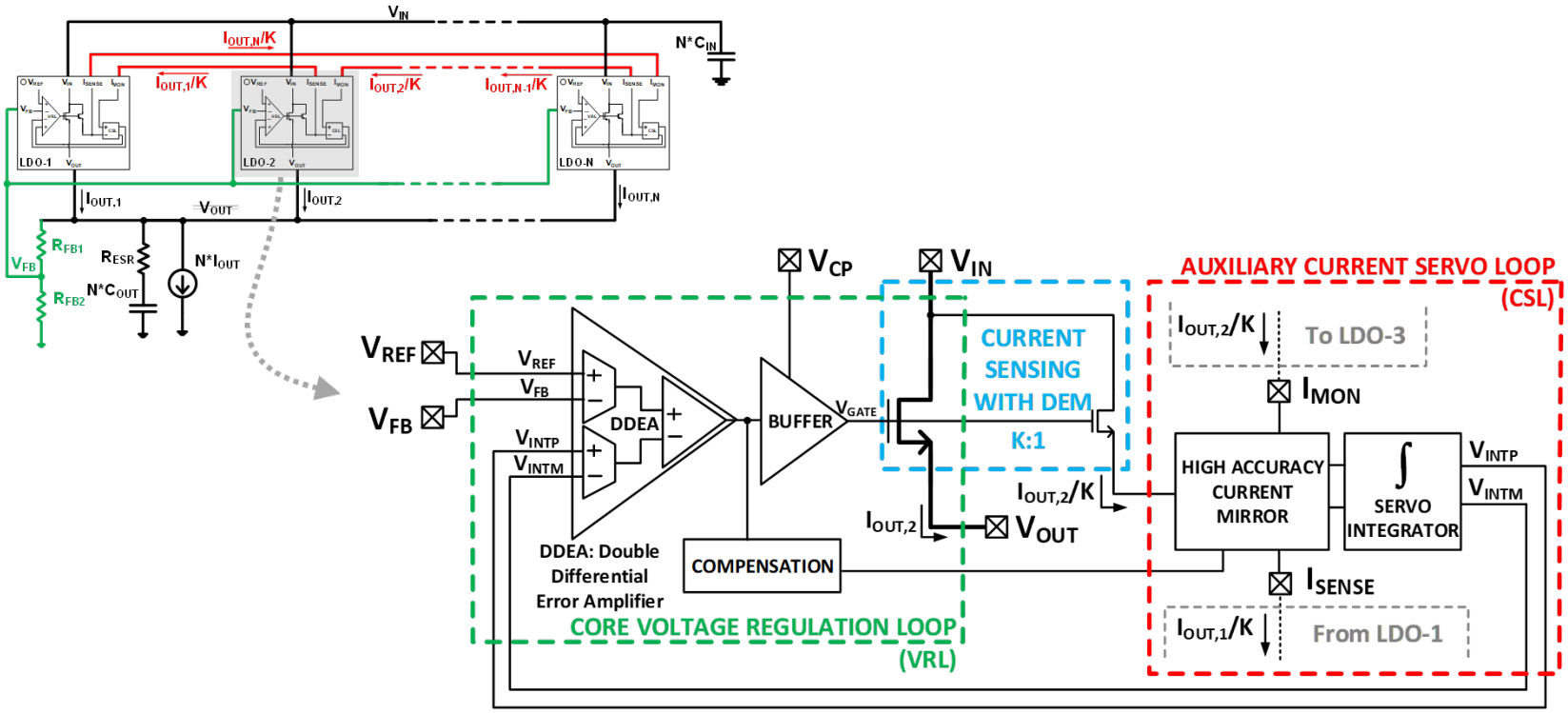


Figure 2.6. Implementation of individual LDO IC in the daisy chain

Parameter	Specification
I_{OUT}	0 to 2A
V_{OUT}	1V to 3V
$V_{DROPOUT}$	300mV
C_{OUT}	22µF
C_{IN}	10µF

Table 2.1. Target specification for individual LDO

2.4.3 Auxiliary Current Servo Loop

The goal of the auxiliary current servo loop is to equate the output currents of each LDO IC in the system and thus facilitate stable parallel operation with high current sharing accuracy. As shown in Figure 2.7, the current servo loop primarily consists of a high accuracy current mirror and a servo integrator.

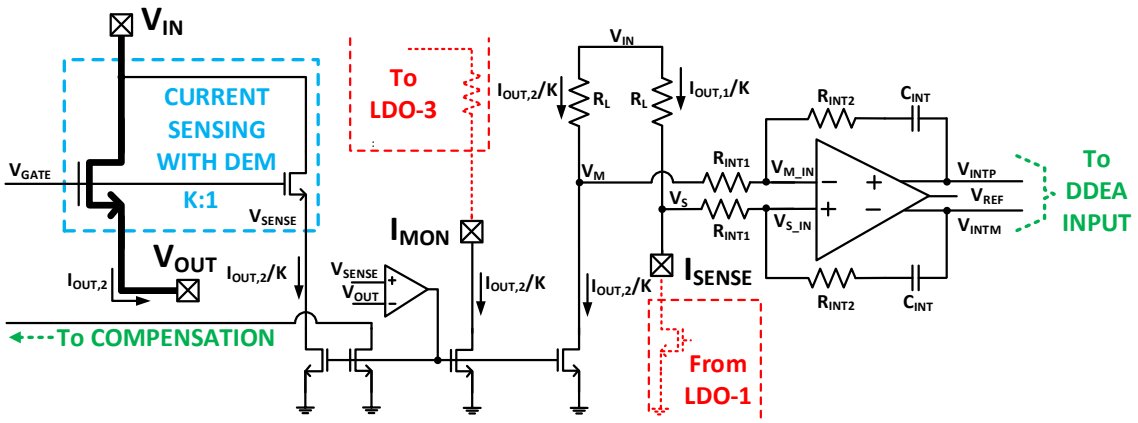


Figure 2.7. Auxiliary current servo loop for load sharing

Consider the LDO-2 in the daisy-chain. LDO-2 receives the sensed output current ($I_{OUT,1}/K$) from the preceding adjacent LDO, LDO-1 in the daisy chain through I_{SENSE}. Simultaneously, it forwards it on its own sensed output current ($I_{OUT,2}/K$) to the

subsequent adjacent LDO, LDO-3 in the daisy-chain through I_{MON}. K refers to the current sensing ratio which is discussed in a later section in detail.

A fully differential servo integrator along with a pair of pull-up resistors accumulates the error between the sensed output currents of LDO-1 and LDO-2. As shown in Figure 2.7, the fully-differential servo integrator is implemented as an active-RC integrator with a fully-differential high-gain amplifier and passive capacitor (C_{INT}) and resistors (R_{INT1}, R_{INT2}). As shown in Figure 2.8, the fully-differential high gain-amplifier is implemented using a high gain folded cascode amplifier with common-mode feedback [23]. The common-mode feedback reference voltage is set to V_{REF} which is the reference voltage for the LDO's core voltage regulation loop.

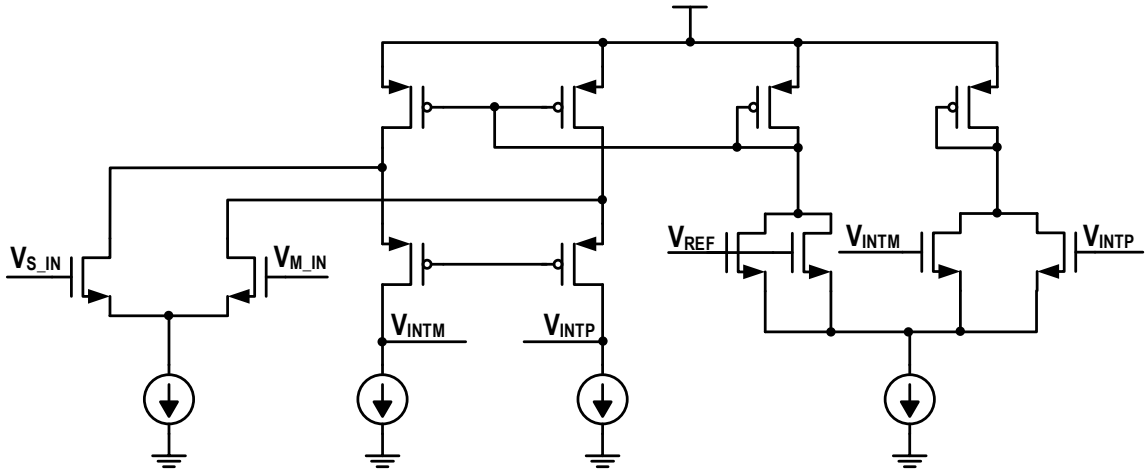


Figure 2.8. Implementation of full-differential amplifier in auxiliary current servo loop

The accumulated error at the output of the servo integrator ($V_{INTP} - V_{INTM}$) is then passed differentially to the second set of inputs of the double differential error amplifier in the core voltage regulation loop as depicted in the top-level implementation diagram in Figure 2.6. If the sensed output currents are not matched, the accumulated error at the second set of inputs of the DDEA forces a change in the individual I_{OUT} of the LDO. If the sensed output currents are matched, the common-mode feedback loop of the fully-

differential servo integrator sets the output voltages of the integrator, V_{INTP} and V_{INTM} to the reference voltage V_{REF}.

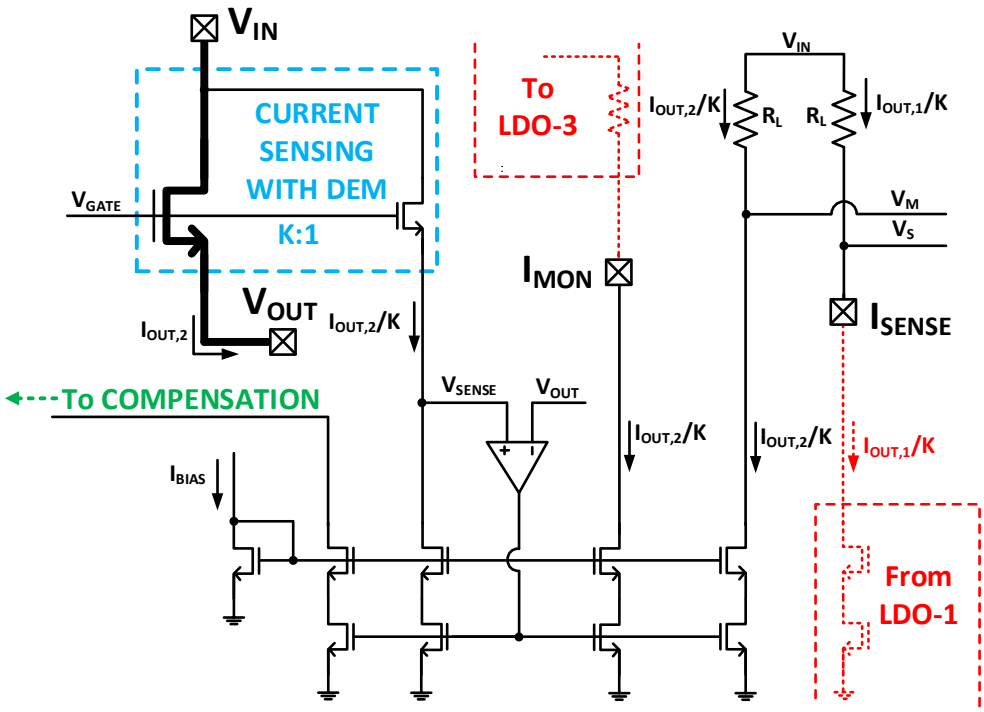


Figure 2.9. Gain boosted current mirror in the auxiliary current servo loop

A gain-boosted cascode current mirror shown in Figure 2.9 further facilitates the operation of this loop. As this approach relies on sensed output currents for current sharing, the requirement for matched PCB traces is eliminated. Moreover, this approach also results in fast transient response.

The various sources of mismatch for current sharing are shown in Figure 2.10. The typical statistical design targets for these mismatch sources are shown in Table 2.2. Output current sensing is the largest contributor to current mismatch among LDOs. Considering typical statistical mismatch variations and root mean square of all these target values, the current sharing accuracy target is set to be 2.05% as per Equation (2.5).

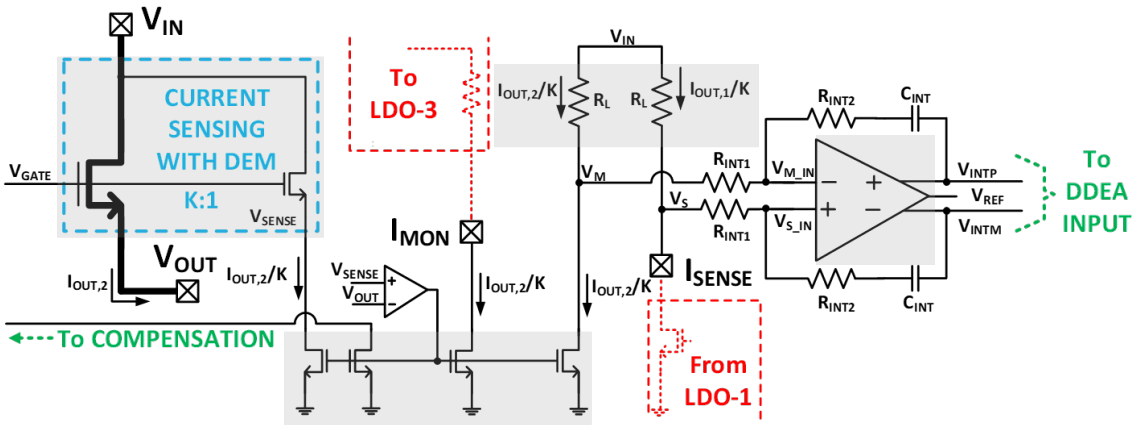


Figure 2.10. Sources of mismatch in auxiliary current servo loop

Source of Mismatch	Mismatch Target (σ)
Current sensing with DEM	1.3%
Gain boosted current mirror in CSL	0.5%
Pull-up resistors in CSL	0.5%
Integrator amplifier gain in CSL	1%
Input offset of DDEA / V_{REF}	1%

Table 2.2. Mismatch sources and target in auxiliary current servo loop

$$Current\ Sharing\ Accuracy\ Target = \sqrt{\sum_{N=1}^{5} \sigma_N^2} = 2.05\% \tag{2.5}$$

2.4.4 Core Voltage Regulation Loop and Compensation

The objective of the core voltage regulation loop is to maintain the output voltage of the LDO at all specified loads. As shown in Figure 2.11, the voltage regulation loop comprises of a double differential error amplifier (DDEA) followed by a source-follower-based buffer to drive the gate of the large NMOS pass field-effect transistor (FET) and the compensation network.

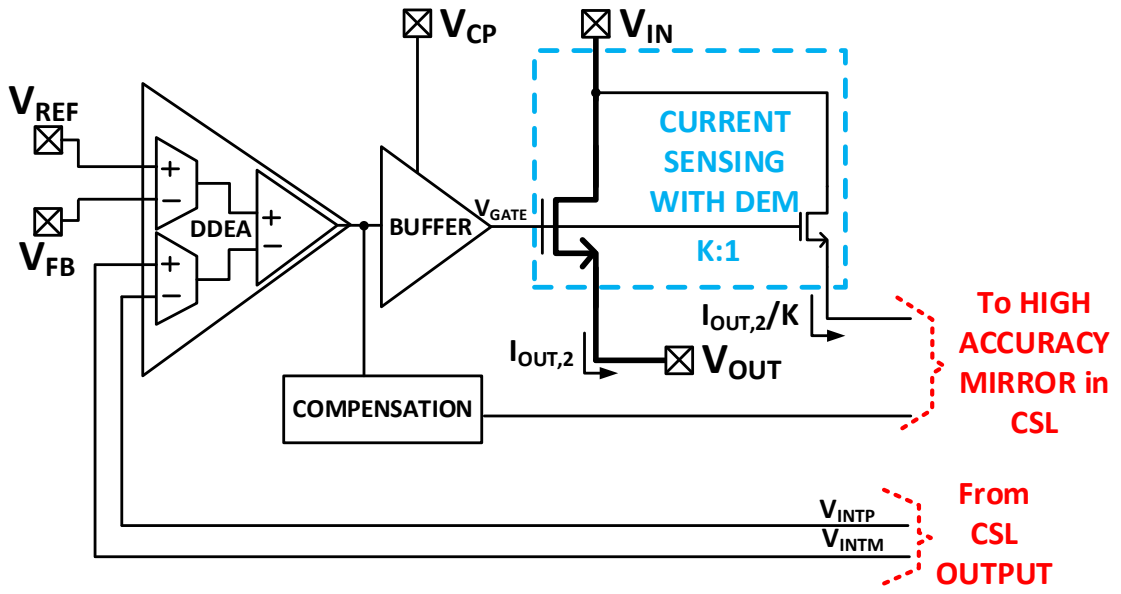


Figure 2.11. Core voltage regulation loop

The output voltage is scaled down to generate the feedback voltage VFB using a set of external resistors R_{FB1} and R_{FB2}. By using negative feedback approach, this feedback voltage V_{FB} is compared to a reference voltage V_{REF} through a high gain loop. This approach forces a change on the gate of the NMOS pass FET thereby achieving regulation. This loop is designed to regulate the output voltage to either 3V or 1V at a dropout voltage of 300mV while supplying a maximum output current of 2A.

The double differential error amplifier has two sets of differential inputs with their outputs folding into a cascode load stage to form the folded cascode structure as shown in Figure 2.12. The first set of inputs comprising of V_{REF} and V_{FB} provides the path for output voltage regulation. The second set of inputs comprising of V_{INTP} and V_{INTM}, the differential outputs of the servo integrator facilitates the equal sharing of output current of each LDO. At regulated V_{OUT}, V_{FB} tends to be equal to V_{REF}, thereby providing no differential current to the load stage. Similarly, at equal output currents of each LDO, V_{INTP} and V_{INTM} tend to

be equal to V_{REF}, thus providing no differential current to the load stage. hence, at steady state, all the four inputs of the double differential error amplifier are at V_{REF}. The input gain of the voltage regulation path was designed to be four times the input gain of the auxiliary current sharing path for stable operation. This was implemented by maintaining the bias current of the voltage regulation inputs four times that of the current sharing inputs.

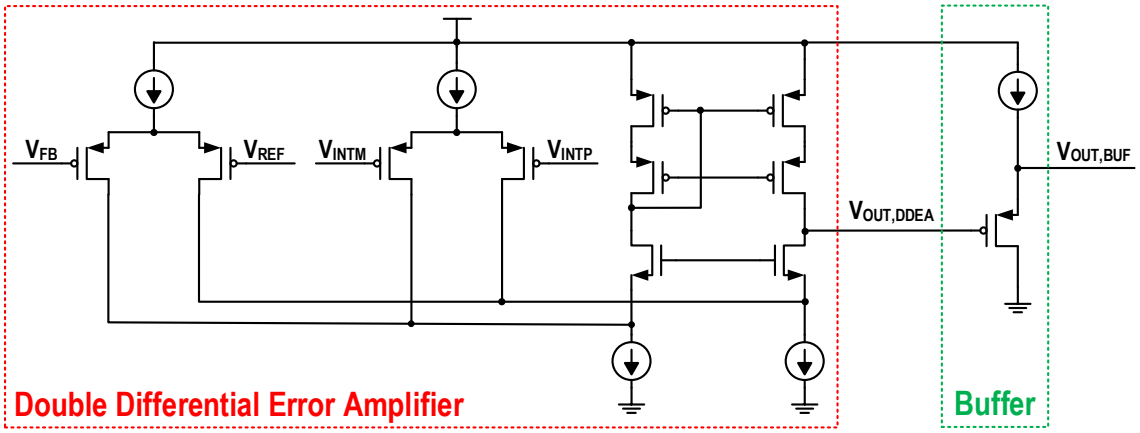


Figure 2.12. Double differential error amplifier and source-follower based buffer

A single-ended source-follower based buffer is designed for a low output impedance to drive the large gate capacitance of the NMOS pass FET. Its implementation is also shown in Figure 2.12. The pass device is sized for the specifications of maximum output current and the dropout voltage. The pass device was chosen to a NMOS as they offer significant area advantages over PMOS pass devices. NMOS pass devices however offer no additional loop gain and suffer from body effect if the bulk is not tied to the source. The NMOS pass device was sized to maintain a dropout voltage of 300mV at 2A of output current at worst corner. As the pass FET is a n-channel device, a higher power supply is required to drive the gate of the pass FET. Realistically, this can be provided by a few ways including charge pumps and other techniques. The current research project reduces the

design complexity in this regard by employing an external voltage (V_{CP}) to power the buffer.

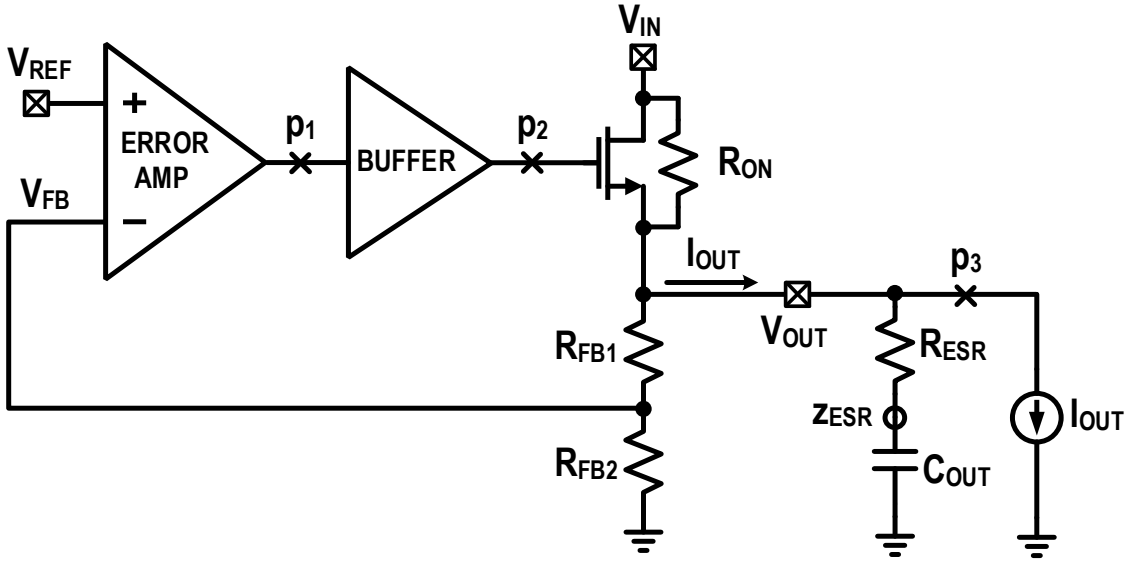


Figure 2.13. Pole-zero locations of a conventional LDO

As shown in Figure 2.13, a conventional LDO with a buffer is a three pole, one zero system inherently. The three poles are at the output of the double differential error amplifier (p_1), the gate of the NMOS pass FET (p_2) and the output of the LDO itself (p_3). The one zero is formed from by the output capacitor and its equivalent series resistance (ESR) (z_{ESR}). With low output impedance of the buffer, p_2 is designed to be beyond the unity gain bandwidth (UGB) of the LDO at all loads. Similarly, z_{ESR} is also ensured to be beyond the UGB of the LDO at all loads. However, typical design specifications keep both p_1 and p_3 within the UGB. This system is thus unstable without compensation at all loads. The frequency of the poles and zeros can be approximately quantified as follows.

$$p_1 \approx \frac{1}{R_{out,DDEA} * C_{in,BUF}} \approx constant \tag{2.6}$$

$$p_2 \approx \frac{1}{R_{out,BUF} * C_{gate,passFET}} \approx constant \tag{2.7}$$

$$p_3 \approx \frac{1}{R_{ON,passFET} * C_{OUT}} \propto I_{OUT} \tag{2.8}$$

$$z_{ESR} = \frac{1}{R_{ESR} * C_{OUT}} \approx constant \tag{2.9}$$

As shown in Figure 2.14, an extra intentional compensation zero z_C is thus added at the output of the DDEA to compensate this system. This compensation zero is formed by a constant capacitor C_C and resistor R_{CC} in series with a variable resistor R_{CV}. The variable resistor R_{CV} is implemented as the output cascode resistance from the high-accuracy gain-boosted current mirror in the current sharing servo loop. This ensures that R_{CV} is inversely proportional to I_{OUT} of the LDO. The compensation zero z_C is thus directly proportional to I_{OUT} as shown in Equation (2.10).

$$C_C,\ R_{CC} = constant$$

$$R_{CV} \propto \frac{1}{I_{OUT}}$$

$$z_C \approx \frac{1}{C_C(R_{CC} + R_{CV})} \propto I_{OUT} \tag{2.10}$$

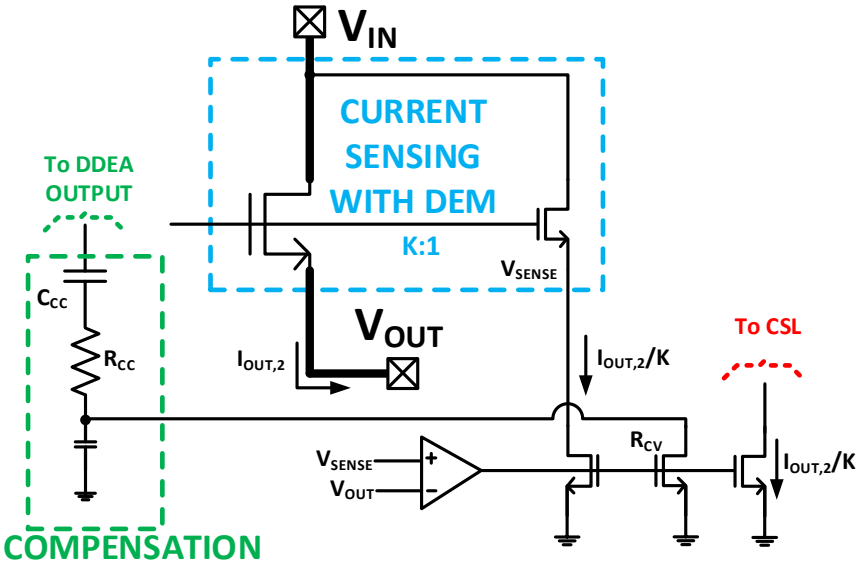


Figure 2.14. Compensation network

Thus, both z_C and p_3 are directly proportional to I_{OUT} of the LDO realizing a stable operating system across all load currents. The variation of the poles and zeros of the system and their variation with I_{OUT} are summarized in Table 2.3.

Pole / Zero	**Location**	**Variation with I_{OUT}**	
p_1	DDEA output	≈ constant	Dominant pole at I_{OUT} > 100mA
p_2	Buffer output	≈ constant	Beyond unity gain bandwidth
p_3	LDO output	∝ I_{OUT}	Dominant pole at I_{OUT} < 100mA
z_{ESR}	LDO output	≈ constant	Beyond unity gain bandwidth
z_C	DDEA output	∝ I_{OUT}	Increases at all I_{OUT}

Table 2.3. Pole zero locations of the individual LDO

The simulated loop responses for the design along with the phase margin and the DC gain of the core voltage regulation loop for various I_{OUT} are shown in Figure 2.15. The system is designed to ensure a phase margin of above 60° at all load currents.

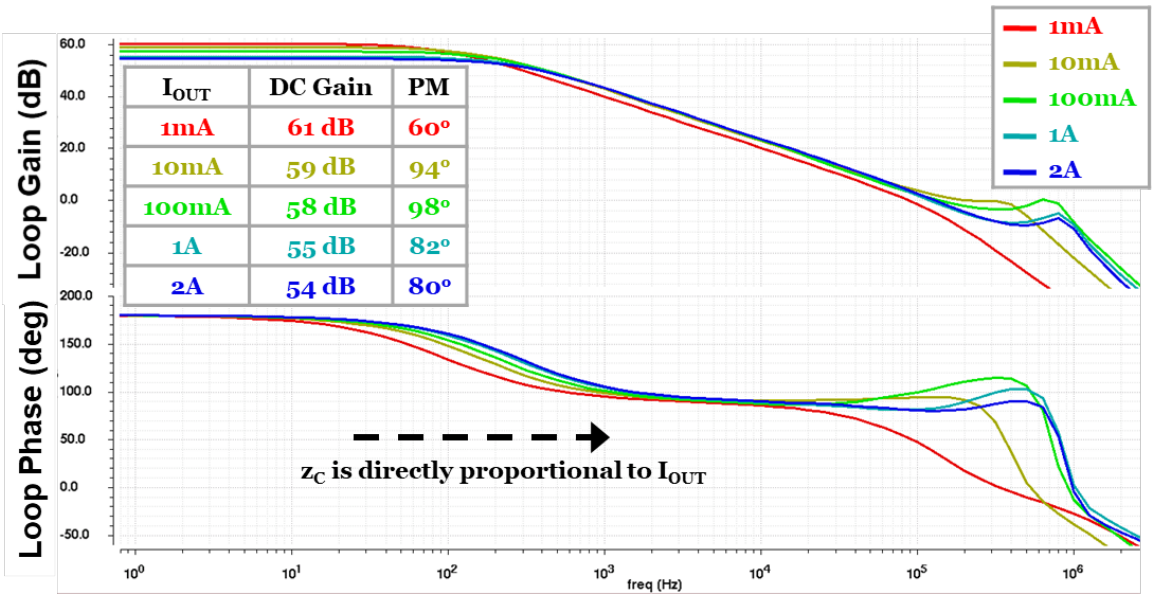


Figure 2.15. Simulated loop gain and phase response

2.4.5 Loop Analysis

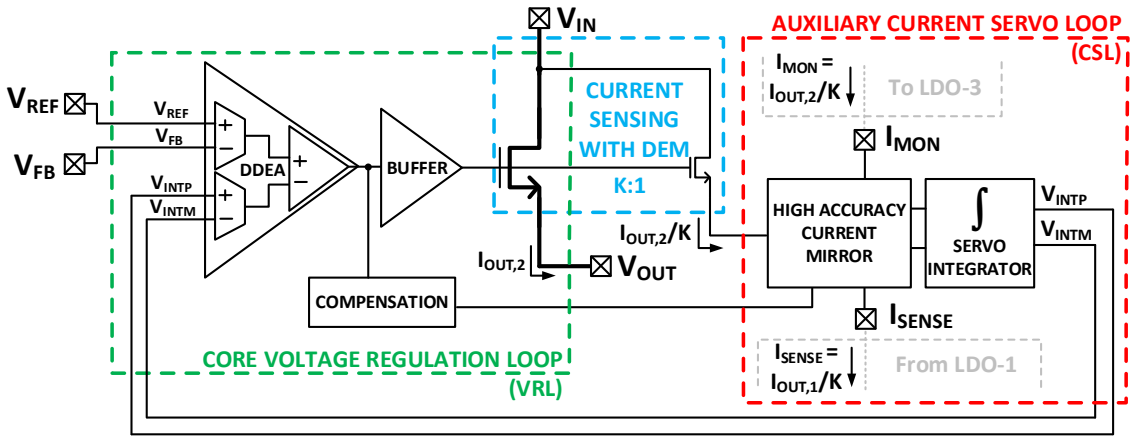


Figure 2.16. Loop analysis for current sharing

As per Figure 2.16, the overall transfer function for current sharing can be defined below.

$$H_{LOOP}(s) = \frac{I_{MON}}{I_{SENSE}} \tag{2.11}$$

I_{MON} is defined through the core voltage regulation loop transfer function as below, where ΔV_{INT} is the differential output voltage of the fully-differential servo integrator.

$$I_{MON} = H_{VRL}(s) * [(V_{REF} - V_{FB}) + \Delta V_{INT}]$$

To visualize current sharing accuracy alone, it can be assumed that the LDO regulates the output voltage, thus $V_{FB} = V_{REF}$.

$$I_{MON} = H_{VRL}(s) * \Delta V_{INT} \tag{2.12}$$

The servo integrator accumulates the error between I_{SENSE} and I_{MON} through the auxiliary current servo loop.

$$\Delta V_{INT} = H_{CSL}(s) * (I_{SENSE} - I_{MON}) \tag{2.13}$$

On simplifying Equations (2.11), (2.12) and (2.13), the overall loop transfer function for current sharing can be obtained as follows,

$$H_{LOOP}(s) = \frac{I_{MON}}{I_{SENSE}} = \frac{H_{VRL}(s) * H_{CSL}(s)}{1 + H_{VRL}(s) * H_{CSL}(s)} \tag{2.14}$$

2.4.6 Integrated Current Sensing

Current sensing for LDOs can be performed both off-chip and on-chip. Some of these techniques are described in [7] [9] [19]. The sensed output current of the LDO can be used for compensation, adaptive biasing, transient detection and more. In this LDO, integrated current sensing is primarily employed for compensation and current sharing. This is done fully on-chip without the need for any external components thereby reducing the size of the overall parallel LDO system. The accuracy of current sensing comprises of two major components namely the systematic component arising from the inherent nature of the sensing architecture, and the statistical component arising due to the random variations.

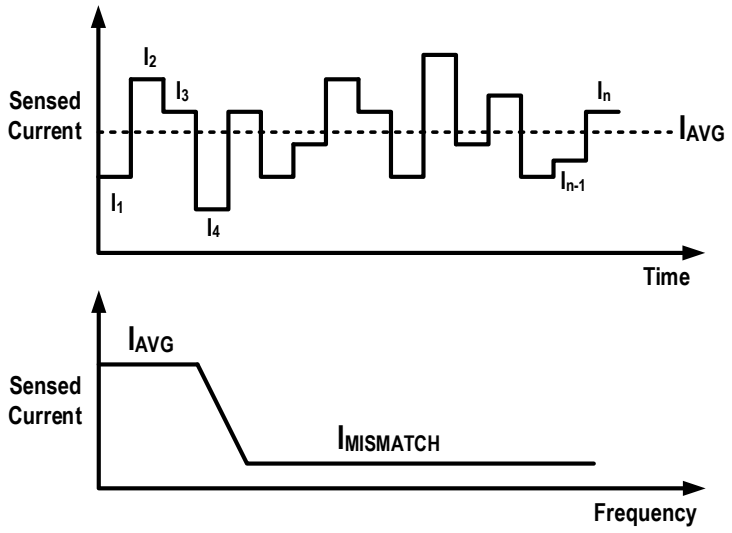


Figure 2.17. Sensed Current vs Time and Frequency

In each individual LDO, dynamic element matching (DEM) is utilized to increase the statistical accuracy of the integrated current sensing architecture multi-fold. Dynamic Element Matching (DEM) is a technique used commonly in data converters to match elements to a resolution finer than their statistical mismatch limit [16-18]. DEM reduces

this statistical mismatch by a factor of the square root of number of elements as shown in Equation (2.15).

$$\sigma_{effective} = \frac{\sigma_{original}}{\sqrt{N_{elements}}} \tag{2.15}$$

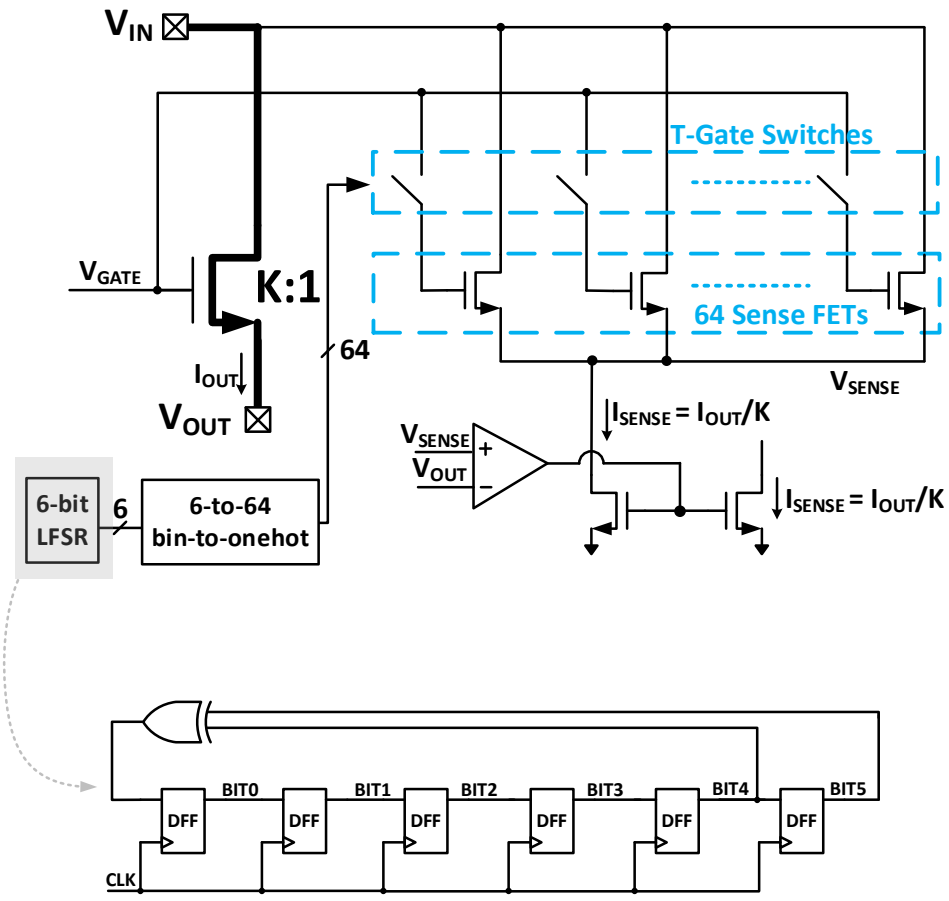


Figure 2.18. Dynamic element matching for integrated current sensing

As shown in Figure 2.18, DEM for current sensing is implemented by placing 64 sense FETs throughout the NMOS pass FET. A random sequence is generated to randomly choose only 1 of the 64 sense FETs. The statistical mismatch component of the current sensing can thus be reduced by a factor of 8 as 64 sense FETs are used. The total number

of random sense FETs was chosen to be 64 for an appropriate balance of current sensing accuracy target and design complexity.

To implement DEM for current sensing, a 6-bit pseudo-random binary sequence (PRBS) is generated. This is based on a linear feedback shift register clocked on an on-chip current controlled relaxation oscillator. The single sense FET selection is enabled by a 6bit-to-64bit binary-to-one-hot encoder. The various implementations for all these blocks are shown in Figure 2.18. Single sense FET selection is achieved by transmission-gate switches on the gate of the sense FETs. Switches for selection on the drain of the sense FETs are avoided to reduce leakage mismatch and ripple on the sensed voltage node V_{SENSE}. The gate of the single selected sense FET is connected to the gate of the NMOS pass FET, V_{GATE}. The gates of the unselected sense FETs are pulled to V_{OUT} thereby reducing their gate-to-source voltage to zero.

Overall, a current sensing ratio 'K' of 1:40,000 is maintained between the sensed current I_{SENSE} and the output current I_{OUT}. A current sensing amplifier maintains the high open loop gain in the current sensing loop. This ensures the systematic mismatch component of current sensing is reduced by a factor of this loop gain as shown in Figure 2.18.

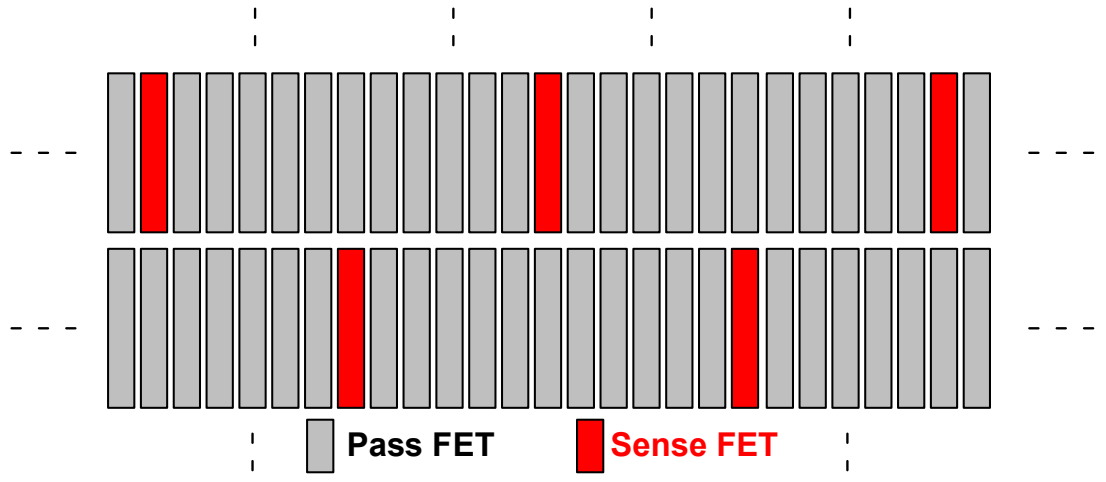


Figure 2.19. Radially and evenly spaced placement of sense FETs across pass FET

As shown in Figure 2.19, the sense FETs are radially and evenly spaced throughout the large NMOS pass FET. This enables to suppress the impact of any spatial thermal gradient over the large NMOS pass FET.

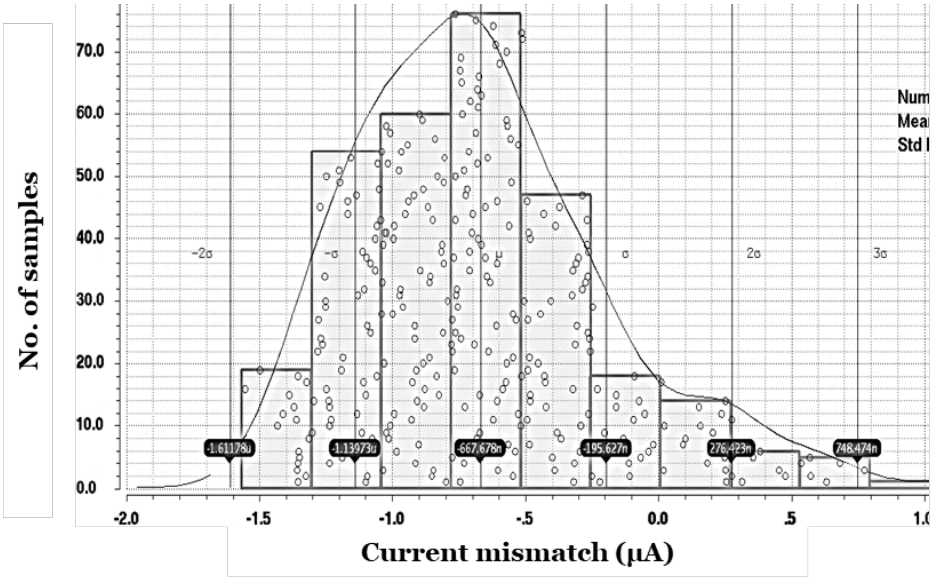


Figure 2.20. Monte-carlo simulation results of sensed current mismatch for 300 runs

$$\sigma_{I_{SENSE}} = \frac{472nA}{50\mu A} = 0.94\%$$

Monte-Carlo simulation results for 300 runs yield an expected mismatch of 0.94% for current sensing at 2A of I_{OUT} and is below the current sensing mismatch target of 1.3% as shown in Figure 2.20.

2.5 Measurement Results

The LDO is designed and fabricated on a 180nm High-Voltage (HV) Bi-CMOS-Diode (BCD) process. Figure 2.21 shows the die micrograph for an individual LDO IC in the parallel system. However, devices with a minimum length of 500nm were employed in the design to support the design specifications especially those of output voltage of 3V.

Moreover, only regular V_{TH} devices were used to showcase this approach as a generic approach expandable to all other processes. The total area of the LDO is 1.8225 mm² of which the NMOS pass FET occupies 1.02 mm². The core voltage regulation loop occupies an area of 0.33 mm², the additional auxiliary current sharing servo loop occupies an area of 0.4 mm² and the testing interface area is 0.06 mm². The layout of the NMOS pass FET is optimized to ensure equal current density in each finger of the FET including the sense FETs [4].

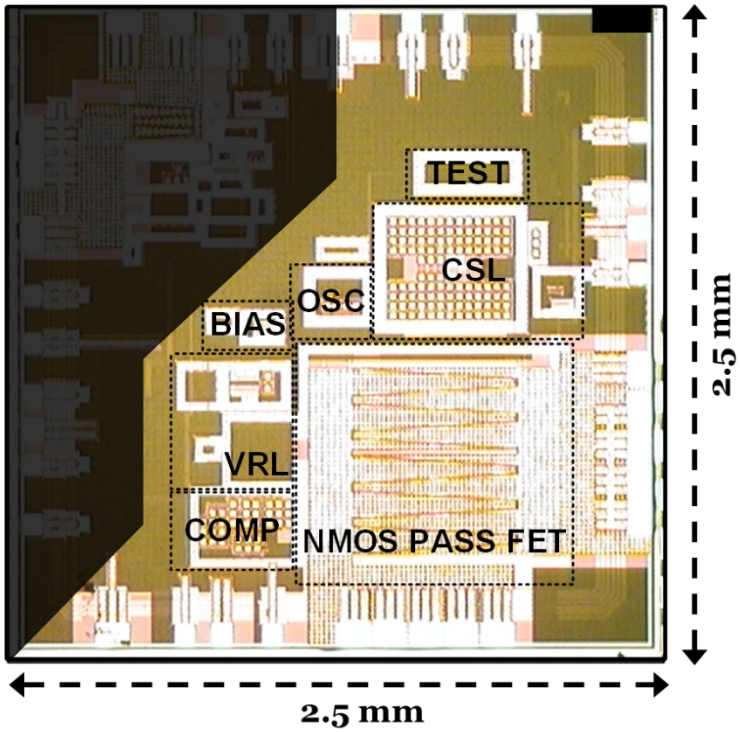


Figure 2.21. Die micrograph of individual LDO IC

The nominal input and output voltages of the LDO are 3.3V and 3V respectively, and 1.5V and 1V respectively for a maximum load current of 2A per LDO. The typical output capacitance of 10µF and the LDO is not dependent on the ESR for stability. The entire system a single set of feedback resistors for all the parallel LDOs in the daisy chain.

The reference voltage for V_{OUT} of 3V is set at 1.2V, thereby setting the feedback resistor R_{FB1} and R_{FB2} to be 360kΩ and 240kΩ respectively. Similarly, the reference voltage for V_{OUT} of 1V is set at 800mV, thereby setting the feedback resistor R_{FB1} and R_{FB2} to be 40kΩ and 160kΩ respectively. Kelvin connection is adopted to ensure that drops due to parasitic inductance and resistance have minimum effect on the performance of the LDO [14].

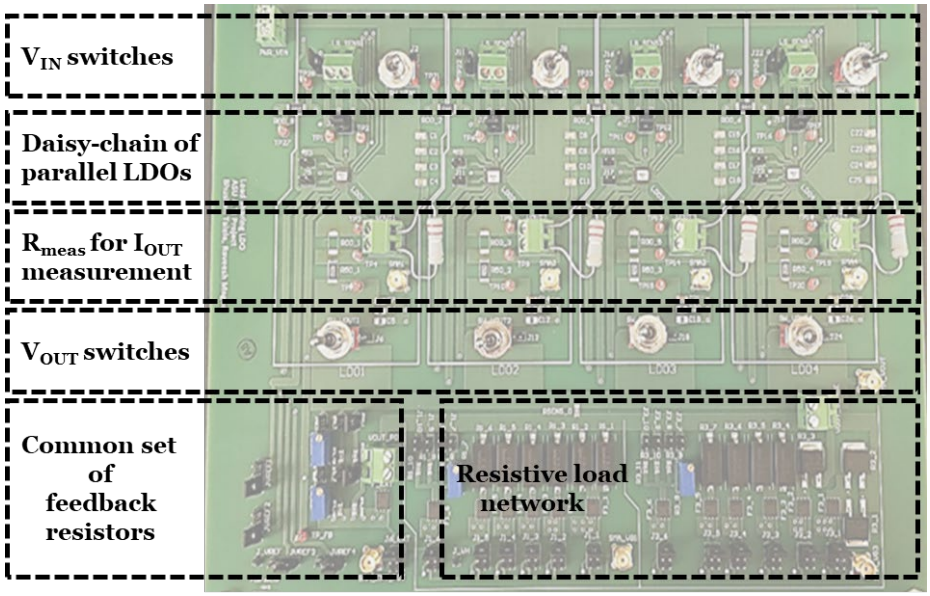


Figure 2.22. Evaluation board for parallel system of LDO ICs

Figure 2.22 shows the evaluation board for testing the designed parallel LDO system. The evaluation board consists of a system of 4 parallel LDO ICs connected in a daisy chain as per the presented idea. The evaluation board can be scaled for 1, 2, 3 or 4 LDOs in parallel. Switches on V_{IN} and V_{OUT} enable the scalable nature of this approach. The board also features a common set of feedback resistors for all the parallel LDOs and can be selected for either 3V or 1V output voltage. Also, the resistive load network can be configured for wither 3V or 1V V_{OUT}. The load transient is introduced by either the FET-slammer [15] based method connecting to a high wattage resistor along with option to have an external electronic load. Trimming and programmability is enabled through SPI

interface. The SPI data and clock signals are generated using the MCP 2210 module with an USB interface. Figure 2.23 shows the measurement setup for the parallel LDO system.

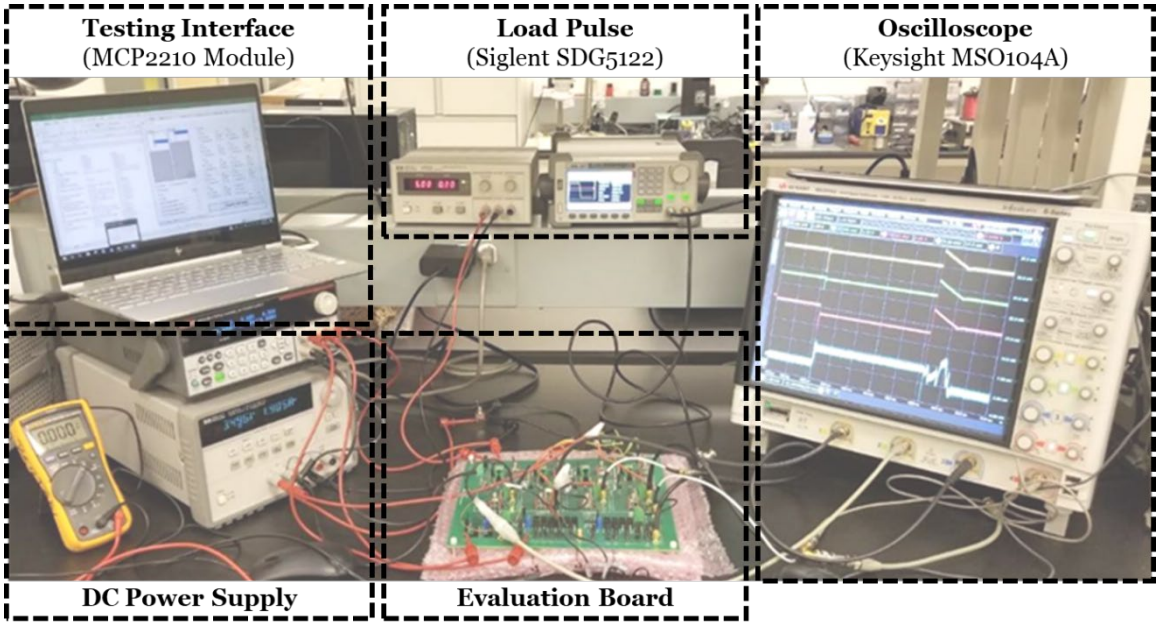


Figure 2.23. Measurement setup of parallel system of LDO ICs

2.5.1 Current Sensing Mismatch

Figure 2.24 shows the setup for measuring current sensing mismatch of the LDO. Considering only LDO-1 in the chain, the sensed current through the sensing pin I_{SENSE} is looped back into the monitoring pin I_{MON}. A high-precision resistor $R_{SENSE,test}$ (2kΩ) measures the sensed voltage $V_{SENSE,test}$ which is proportional to the sensed current $I_{SENSE,test}$. The current sensing mismatch of a single standalone LDO is then measured for a DC load transient of 10mA to 2A to 10mA at a rate of 1A/µs. For a load current of 2A, and a current sensing ratio of K (1:40,000), the ideal value of sensed current is 50µA. The current sensing mismatch (%) can thus be calculated by Equation (2.16).

$$Current\ Sensing\ Mismatch\ (\%) = \frac{I_{SENSE,test} - I_{SENSE,ideal}}{I_{SENSE,ideal}} * 100 \qquad (2.16)$$

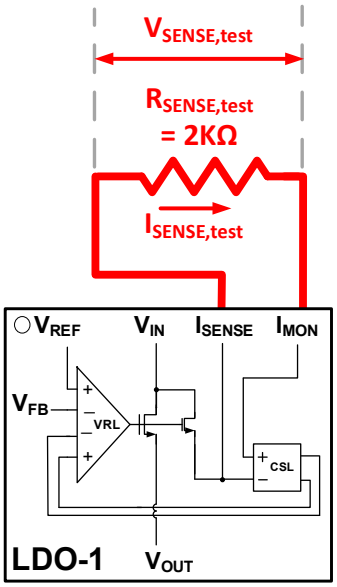


Figure 2.24. Measuring current sensing mismatch

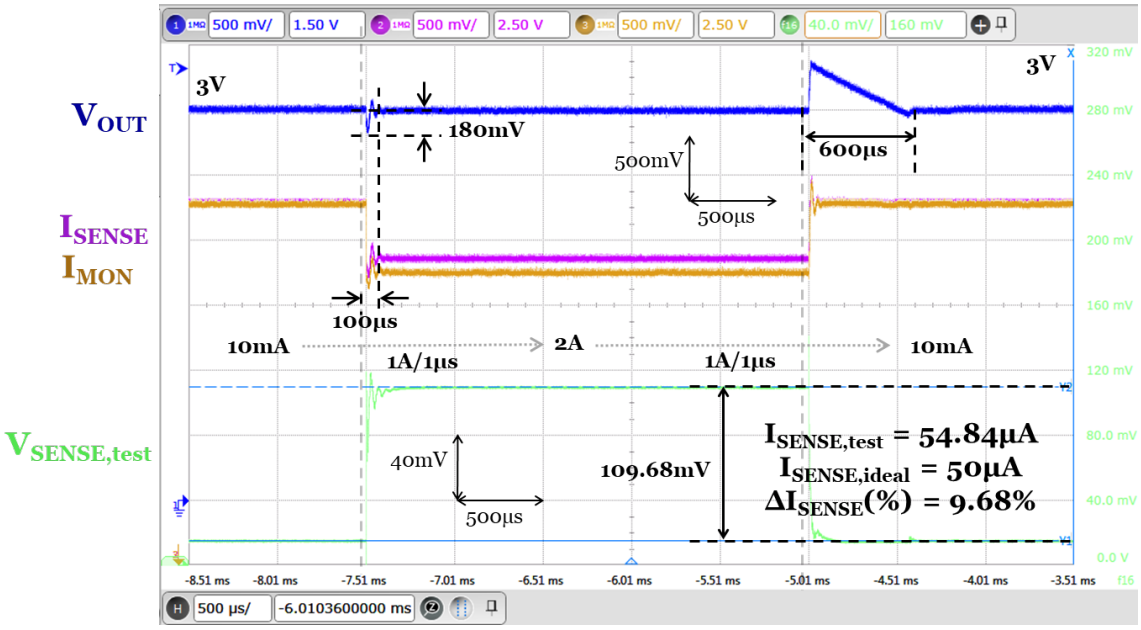


Figure 2.25. Measured current sensing mismatch with DEM disabled

With dynamic element matching disabled, the mismatch in current sensing at an output voltage of 3V and load current of 2A is measured to be 9.68% as shown in Figure

2.25. As shown in Figure 2.26, the current sensing mismatch reduces by a factor of almost 8 to 1.22% once dynamic element matching is enabled as per Equation (2.15) with the number of sense elements to be 64.

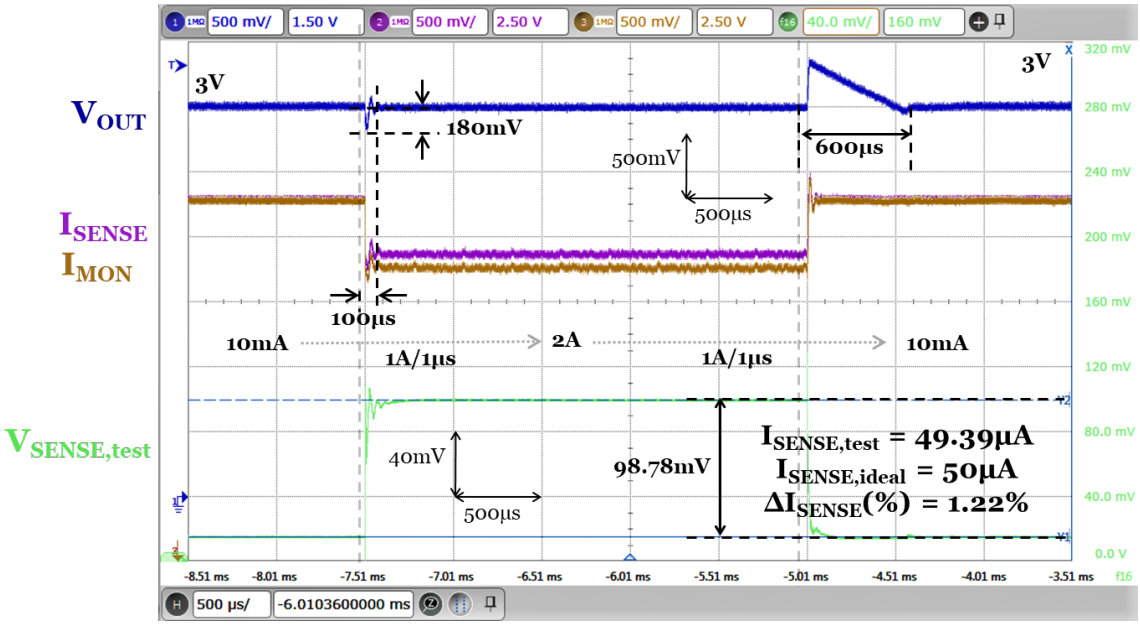


Figure 2.26. Measured current sensing mismatch with DEM enabled

2.5.2 Current Sharing Accuracy

Figure 2.27 shows the setup for measuring current sharing accuracy. Consider LDO-1 and LDO-2 connected in a parallel daisy-chain approach. High-precision resistors R_{meas} (200mΩ) are added on the output of each LDO. The difference in the output voltages of each individual LDO (ΔV_{OUT}) can thus quantify the current sharing accuracy (%) of the parallel system as shown in Equation (2.17).

$$\Delta I_{OUT} = I_1 - I_2 = \frac{V_{OUT1} - V_{OUT2}}{R_{meas}} = \frac{\Delta V_{OUT}}{R_{meas}}$$

$$Current\ Sharing\ Accuracy\ (\%) = \frac{\Delta I_{OUT}}{I_{OUT}} * 100 = \frac{\Delta V_{OUT}}{I_{OUT} * R_{meas}} * 100 \qquad (2.17)$$

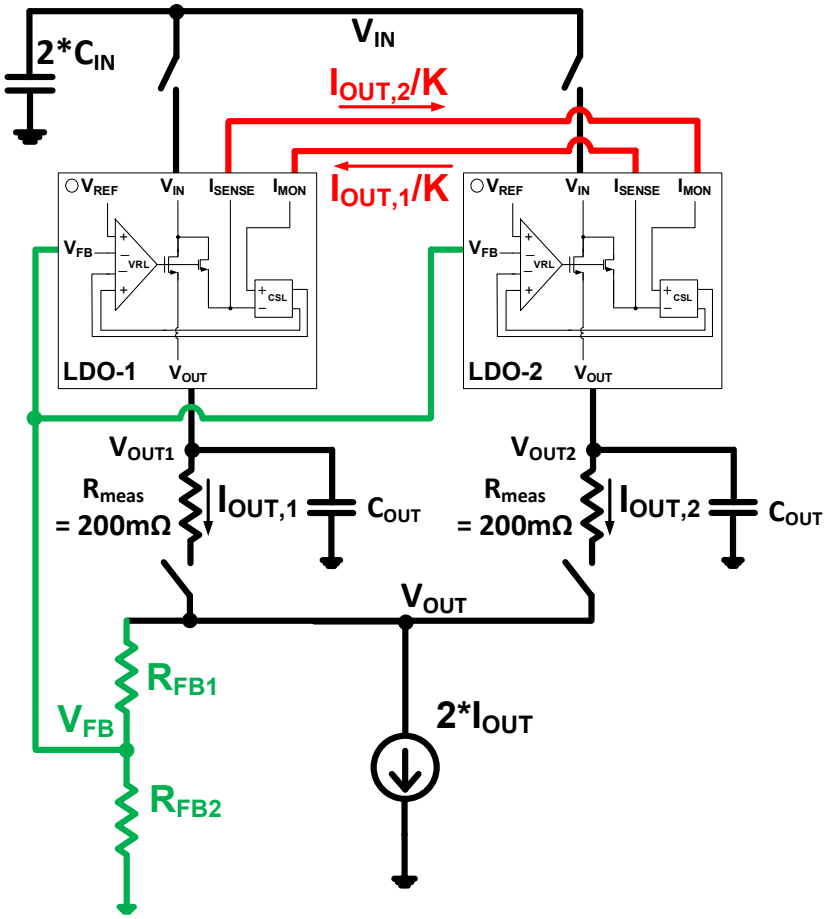
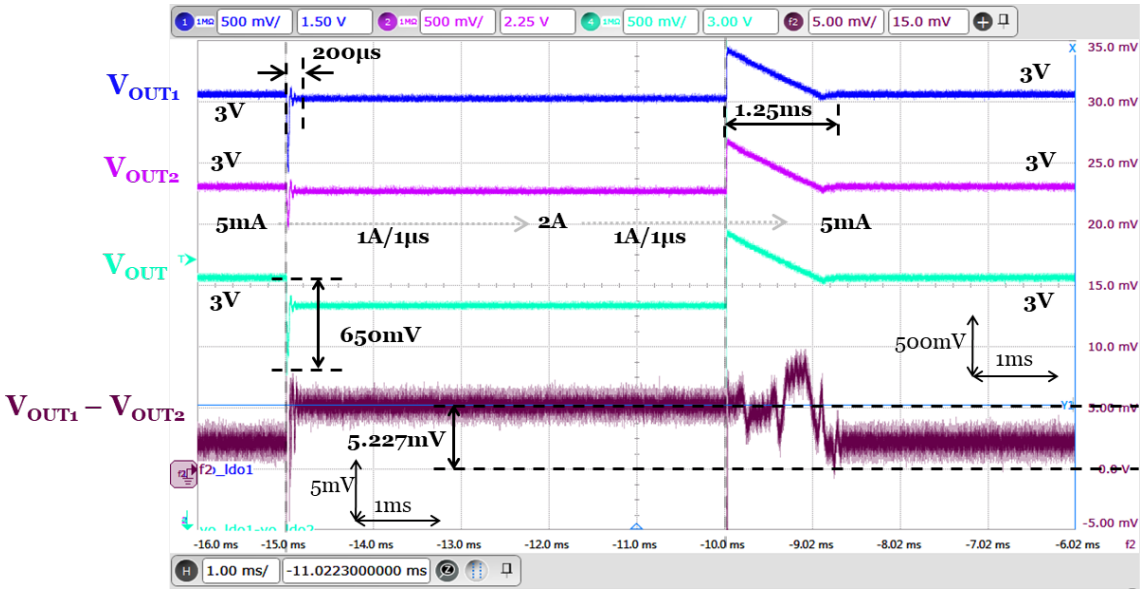


Figure 2.27. Measuring current sharing accuracy

The load regulation measurement result for the 2-parallel LDO combination for an output voltage of 3V of LDO-1 and LDO-3 is shown in Figure 2.28. A load transient of 5mA to 2A to 5mA per LDO at a rate of 1A/µs is then introduced for a total output load transient of 10mA to 4A to 10mA for the parallel system of LDOs. The average value of difference of individual output voltages at 2A of I_{OUT} per LDO is measured to be 5.227mV. This translates to a current sharing accuracy of 2.613% for V_{OUT} of 3V at I_{OUT} of 2A per LDO.

A thermal image of the board was captured during this load transient using the FLIR ONE Pro Thermal Imaging Camera to validate thermal equilibrium. As shown in Figure 2.29, thermal image of the board illustrates both the LDOs are at the same

temperature, ensuring that a thermal equilibrium is also achieved by this approach to parallelize LDOs.



V_{OUT} = 3V, I_{OUT} = 5mA*2 → 2A*2 → 5mA*2

ΔV_{OUT} = 5.227mV → ΔI_{OUT} = 2.613%

Figure 2.28. Measured load regulation for 2 parallel LDOs at V_{OUT} = 3V

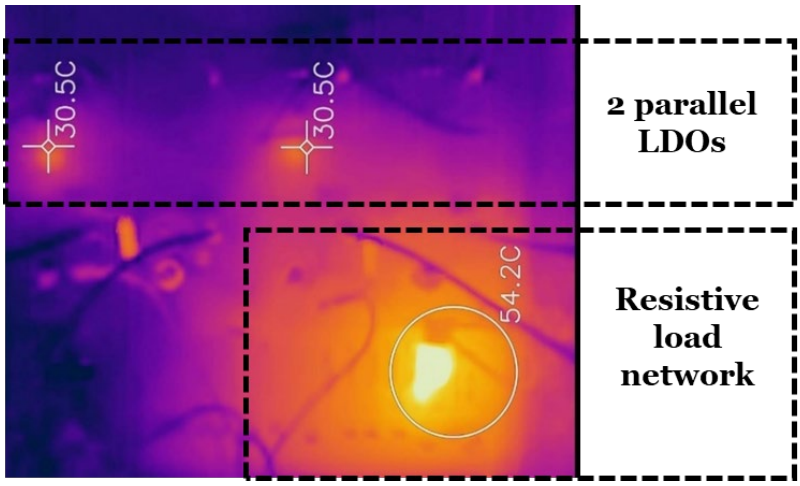
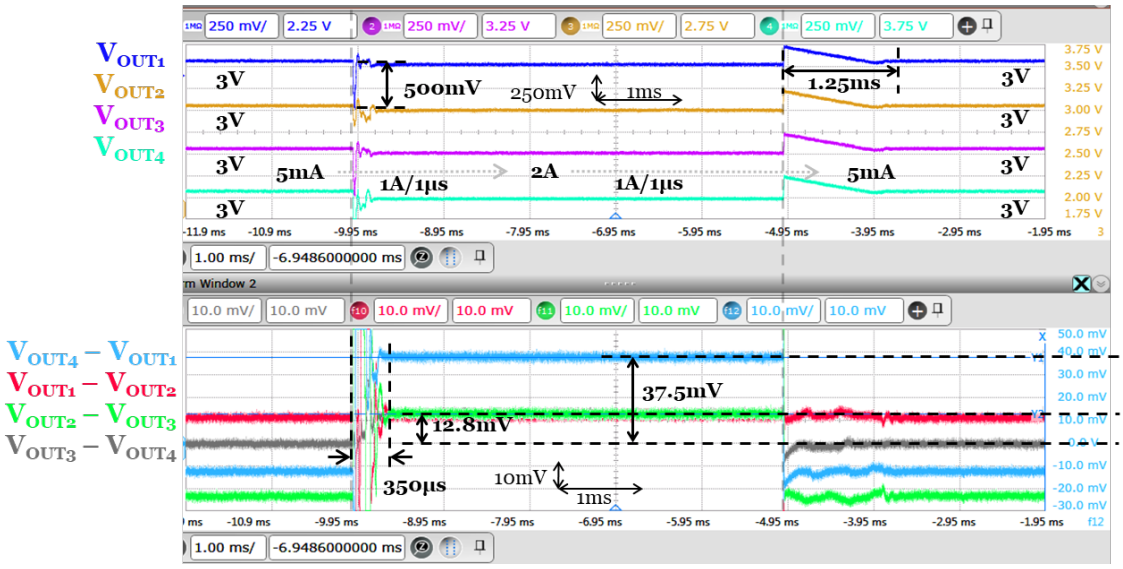


Figure 2.29. Thermal image for 2 parallel LDOs at V_{OUT} = 3V



V_{OUT} = 3V, I_{OUT} = 5mA*4 → 2A*4 → 5mA*4

ΔV_{OUT12} = 12.8mV → ΔI_{OUT12} = 6.4%

ΔV_{OUT23} = 12.8mV → ΔI_{OUT23} = 6.4%

ΔV_{OUT34} = 12.8mV → ΔI_{OUT34} = 6.4%

ΔV_{OUT41} = 37.5mV → ΔI_{OUT41} = 18.75%

Figure 2.30. Measured load regulation for 4 parallel LDOs at V_{OUT} = 3V

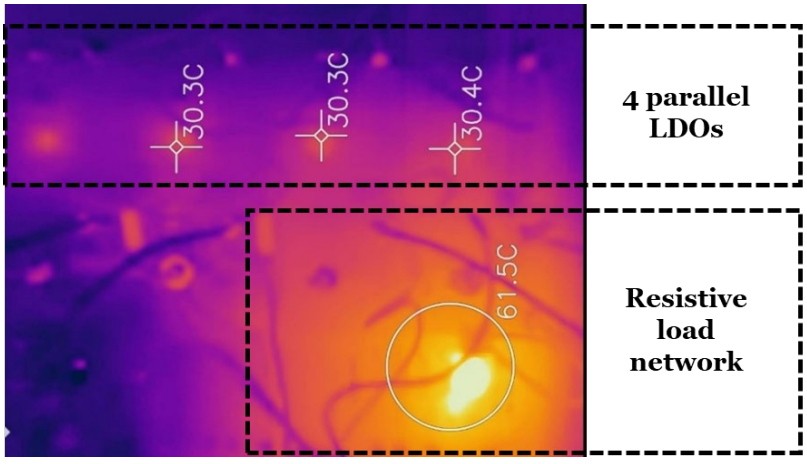
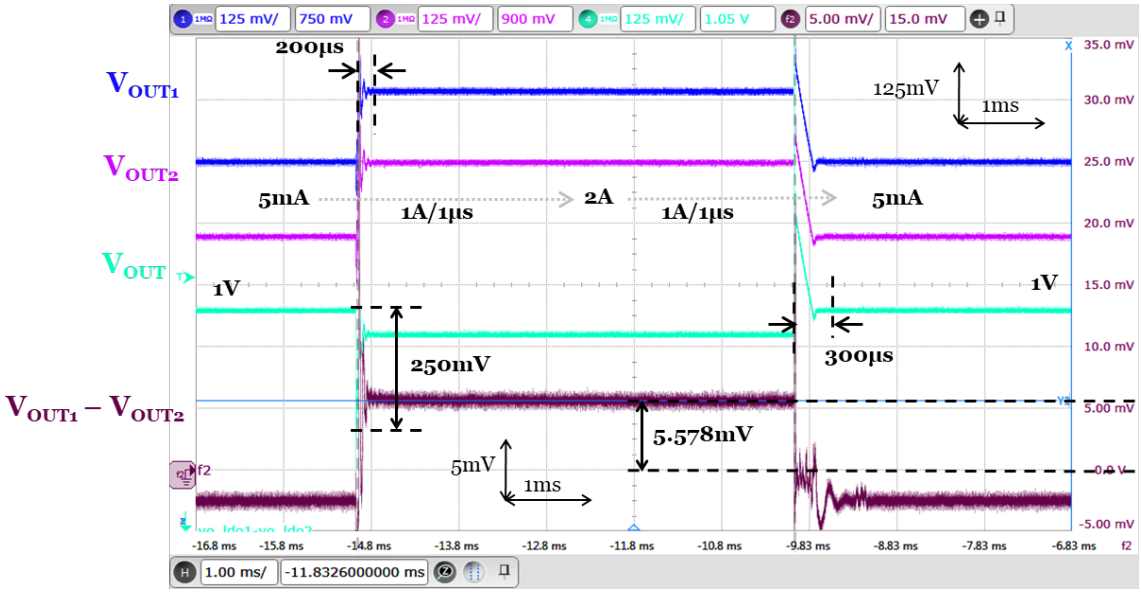


Figure 2.31. Measured load regulation for 4 parallel LDOs at V_{OUT} = 3V

The scalable nature of this approach is demonstrated by the parallel operation for all the 4-parallel LDOs on the evaluation board for an output voltage of 3V as shown in Figure 2.30. Similarly, a load transient of 5mA to 2A to 5mA per LDO at a rate of 1A/µs is then introduced for a total output load transient of 20mA to 8A to 20mA for the parallel system of 4 LDOs. The average value of difference of output voltages is measured to determine the current sharing accuracy. Current sharing accuracy of 6.4% is achieved for 3 pairs of the LDOs whereas 1 of the pair of the LDOs achieves a higher current sharing accuracy of 18.75%.

As shown in Figure 2.31, a thermal image of the board during this load transient illustrates all the 4 LDOs are almost at the same temperature and thus operating in thermal equilibrium.



V_{OUT} = 1V, I_{OUT} = 5mA*2 → 2A*2 → 5mA*2

ΔV_{OUT} = 5.578mV → ΔI_{OUT} = 2.789%

Figure 2.32. Measured load regulation for 2 parallel LDOs at V_{OUT} = 1V

Similarly, the load regulation measurement result for the 2-parallel LDO combination for an output voltage of 1V of LDO-1 and LDO-2 is shown in Figure 2.32. A load transient of 5mA to 2A to 5mA per LDO at a rate of 1A/µs is then introduced for a total output load transient of 10mA to 4A to 10mA for the parallel system of LDOs. The average value of difference of individual output voltages at 2A of I_{OUT} per LDO is measured to be 5.578mV. This translates to a current sharing accuracy of 2.789% for V_{OUT} of 1V at I_{OUT} of 2A per LDO.

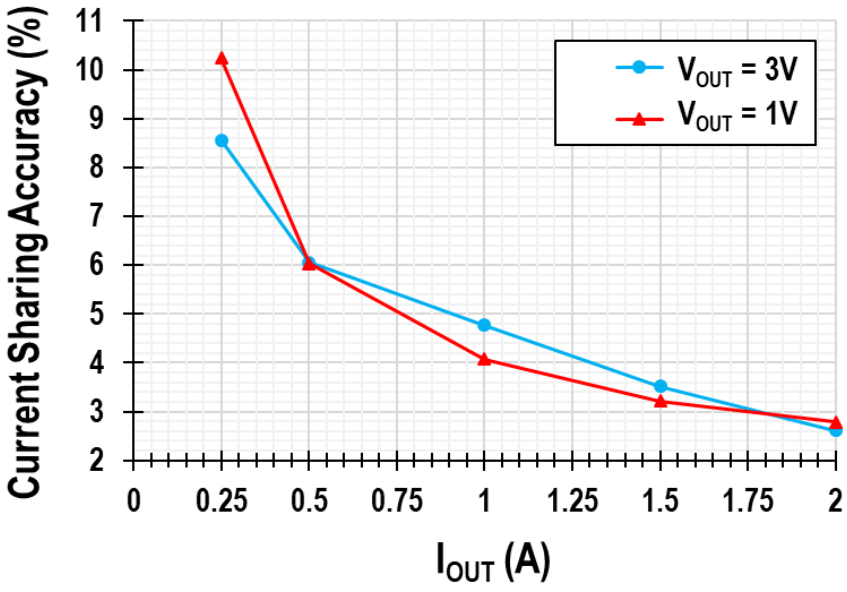


Figure 2.33. Current sharing accuracy vs output current

Figure 2.33 shows the variation of current sharing accuracy for a range of output currents from 250mA to 2A per LDO for V_{OUT} of 3V and 1V. It can be observed that current sharing accuracy is better at higher output currents as compared to lower output currents. This can be attributed to the absolute value of the sensed current being higher at higher output currents. Higher absolute values of sensed currents lead to better error correction between the sensed currents thereby leading to better current sharing accuracy.

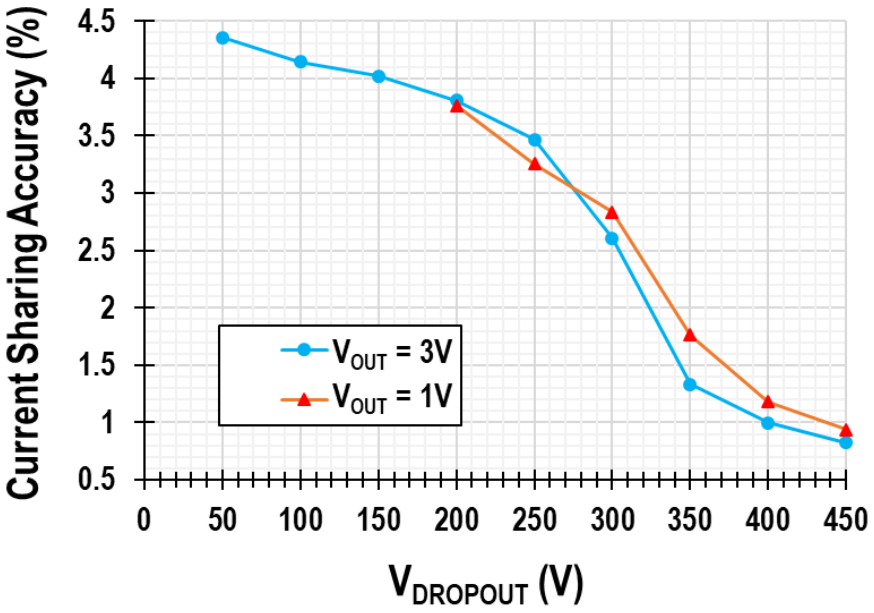


Figure 2.34. Current sharing accuracy vs dropout voltage

The variation of measured current sharing accuracy for the same parallel LDO system with dropout voltage is shown in Figure 2.34. At lower dropout voltages, the NMOS pass FET is unable to regulate the output voltage and the system stability is lost. This is the prime reason for the increased current sharing accuracy observed at reduced dropout voltages.

2.5.3 Comparison Summary

Table 2.4 showcases the PCB size of this approach comparing it with prior implementations. To implement current sharing, this work does not require any external passive or active components, such as sense/ballast resistors, amplifiers or mismatch resistors. Additionally, only a single set of feedback resistors is required as compared to multiple sets in other solutions.

Consider a routing overhead of 30% over the total component size as an estimation for PCB size. The PCB size of this work for 2 parallel LDOs supplying a total of 4A of output current is 13.312mm^2 without accounting for the LDO ICs themselves, which is 70.4% lower than its closest competitor. This work also achieves 300.48 mA/mm^2 of PCB current density without considering the LDO ICs which is 225% higher than its closest competitor.

As showcased in Table 2.5, the daisy-chain approach of this system is unique compared to the conventional master-slave approach implemented by many other prior state-of-art solutions. This work achieves on-par current sharing accuracy of 2.613% for a system of 2 parallel LDOs or regulators. Each LDO IC is designed for a V_{OUT} of 3V or 1V and maximum I_{OUT} of 2A per LDO at a dropout voltage of 300mV. Moreover, this system eliminates the need for any external active or passive components or matched PCB traces for current sharing.

		This Work		[6] Texas Instruments TIDU421 2014		[7] Analog Devices AN-1421 2016		[8] Texas Instruments TIDUB16A 2016	
		Qty.	**Size**	**Qty.**	**Size**	**Qty.**	**Size**	**Qty.**	**Size**
I_{OUT}		**2 X 2A**		2 X 3A		2 X 2.5A		3 X 300mA	
LDO IC		**2**	**5mm X 5mm (Shared Die)**	2	3.5mm X 3.5mm	2	3mm X 3mm	3	6.4mm X 6.3mm
Feedback Resistors	R_{FB1}	**1**	**3.2mm X 1.6mm**	2	1.6mm X 0.8mm	2	(1.6mm X 0.8mm)*	3	(1.6mm X 0.8mm)
	R_{FB2}	**1**	**3.2mm X 1.6mm**	2	1.55mm X 0.85mm	2	(1.55mm X 0.85mm)*	3	(1.55mm X 0.85mm)*
Current Sharing Circuitry	Sense/Ballast Resistors	**Not Required**		2	5mm X 2mm	2	(5mm X 2mm)*	3	2.5mm X 1.2mm
	Amplifier			1	2.8mm X 2.9mm	1	2.8mm X 2.9mm	Not Required	
	Mismatch Resistor			1	1.6mm X 0.8mm	1	(1.6mm X 0.8mm)*		
PCB Routing Overhead		+30%							
PCB Size (Without LDO ICs)		**13.312 mm²**		44.972 mm²		44.972 mm²		17.930 mm²	
PCB Current Density (Without LDO ICs)		**300.48 mA/mm²**		133.42 mA/mm²		111.18 mA/mm²		50.195 mA/mm²	

* Component size not mentioned; equivalent size considered for comparison

Table 2.4. Comparison of PCB size with prior art

	This Work	[4] Sun, Yang, et al. JSSC 2017	[5] Vaisband, Friedman TPEL 2016	[6] Texas Instruments TIDU421 2014	[7] Analog Devices AN-1421 2016	[8] Texas Instruments TIDUB16A 2016	[9] Linear Technology 2015
Architecture	**Daisy-chain; integrated current sensing**	Master-slave; 4-phase buck; on-chip	On-chip LDOs	Master-slave; active paralleling	Master-slave; active paralleling	Different LDO ICs; ballast resistors	Current-based reference; sense resistor
($V_{DROPOUT}$) / ($V_{IN} - V_{OUT}$)	**300mV**	400mV	300mV	500mV	300mV	500mV	500mV
V_{OUT}	**3V, 1V**	1.6V	0.7V	0.8V, 3.3V	1.5V	5V	3.3V
I_{OUT} (per Regulator)	**2A**	1.5A	131.3mA	3A	2.5A	300mA	1.5A
Current Sharing Accuracy (2 Parallel Regulators)	**2.613%**	3.6%	50% - 200%	20%	1%	N.A.	10%
External Components (for Current Sharing)	**No**	No	No	Yes	Yes	Yes	Yes
Matched PCB Trace (for Current Sharing)	**No**	No	No	Yes	Yes	Yes	No

Table 2.5. Comparison with prior art

2.6 Summary and Conclusions

Parallelizing regulators is a viable option to increase the total output current without sacrificing on performance, functionality and thermal reliability of the system. This chapter presents a daisy-chain solution to parallelize multiple LDO ICs. An auxiliary current servo loop operating in tandem with the core voltage regulation loop enables current sharing between the multiple parallel LDO ICs. A double-differential error amplifier combines both the voltage regulation error and the current sharing error thereby achieving parallel operation with a single set of feedback resistors. The presented PCB-friendly approach achieves current sharing without the need for any off-chip active or passive component or matched PCB traces thus reducing the overall system cost. Fully integrated current sensing based on dynamic element matching eliminates the need for any off-chip current sensing. 64 sense elements are used to reduce the output current sensing mismatch by a factor of 8 and validated by measurement results.

Silicon measurement results validate the high-accuracy parallel LDO operation with a measured current sharing accuracy of 2.613% and 2.789% for an output voltage of 3V and 1V respectively. The measurement results for both 2 and 4 parallel LDO IC combinations also showcase the scalable nature of the parallel system as per the end-user requirements. Thermal images as well showcase that the system achieves thermal equilibrium thereby ensuring stable reliable operation. The dependence of current sharing accuracy with output current and dropout voltage is also characterized. The comparison summary with prior art shows that this approach to parallelize LDO ICs at par current sharing accuracy with a higher current density and lower system size.

CHAPTER 3

TIME-DOMAIN SWITCHING REGULATORS

3.1 Introduction and Motivation

Space is a harsh environment to operate for all including electronic integrated circuits (ICs). Space electronics must overcome multiple hurdles compared to everyday consumer electronics to operate to function and perform efficiently. Some of these hurdles include radiation, vibration imposed during launch, temperature variance, tin whiskers, high electrostatic discharge [24]. The primary challenge of space-grade ICs is to minimize the effect of radiation events on their performance and functionality. Natural space radiation can damage ICs rendering them inoperative not only partially but also completely. Once space satellites are deployed, there is little or no way to make hard changes to their environment.

There are two primary ways radiation can affect ICs on satellites in space, namely total ionizing dose (TID) and single event effects (SEEs) [24]. TID refers to a slow long-term failure whereas SEEs are instantaneous short-term failures. TID can vary from orbital location and can affect functionality and performance over a long duration of time. Meanwhile, SEEs are caused by a single, high-energy particle passing through the IC. This can be modeled as a charge injection on a net in a circuit. Typically, SEEs can be classified as soft errors and hard errors depending on their severity. Soft SEE errors could be bit flips, changes in states of memory cells which are non-destructive, functional errors. Hard SEE errors are irreversible errors such as gate oxide rupturing that can cause permanent damage to the IC. These errors can potentially destroy the device and damage the entire IC.

3.1.1 Power Management Electronics in Space

Of the multiple subsystems on a spacecraft, the electric power and distribution subsystems primary function is to convert solar energy or any other power source such as radioisotope thermoelectric generators into electrical power [1]. As shown in Figure 3.1, this subsystem consists of multiple power management ICs (PMICs) which based on their function can be power bus converters, point-of-load (POL) converters, chargers, etc. [13].

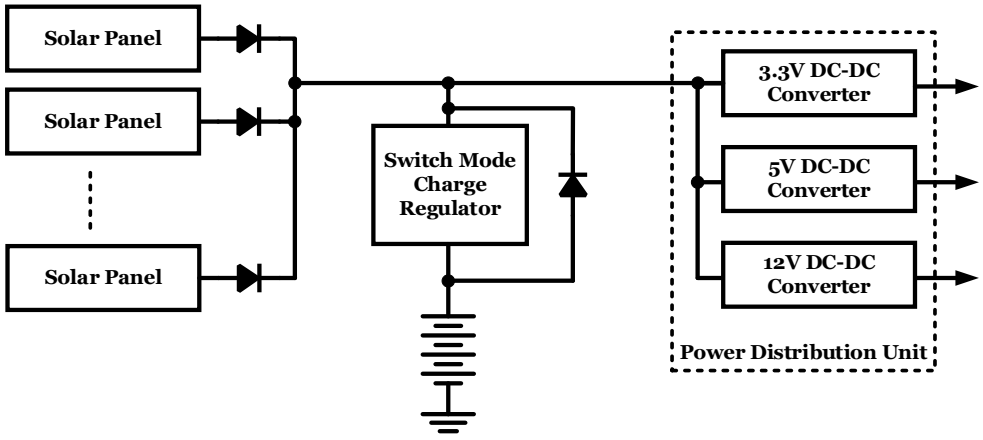


Figure 3.1. Electric power and distribution subsystem on a spacecraft

Most of these PMICs employ DC power supplies primarily and can be implemented as either linear or switching regulators depending on their application. Linear regulators are used for low-power applications less than 10W because of their simpler design, low noise and quick transient response to load changes. On the other hand, switching converters are generally used for applications for power delivery in the range of 5W to 100W. Their small size, high efficiency and ability to step-up (boost) and step-down (buck) and in some cases provide isolation are advantageous for certain applications. [30].

Conventional DC-DC switching converters employing analog control techniques as shown in Figure 3.2 are susceptible to radiation [26-33, 35]. The performance of such conventional analog converters is inhibited due to their use of classical linear control

techniques. Moreover, classical control techniques employ dominant pole and bulky on-chip / off-chip compensation which impose bandwidth limitations and limit transient performance. Moreover, TID can cause degradation of or drift of the devices on the IC affecting to accuracy and quality of voltage regulation. SEEs on the other hand can cause instantaneous violations of supply voltages and can results in unreliable operation or permanent damage.

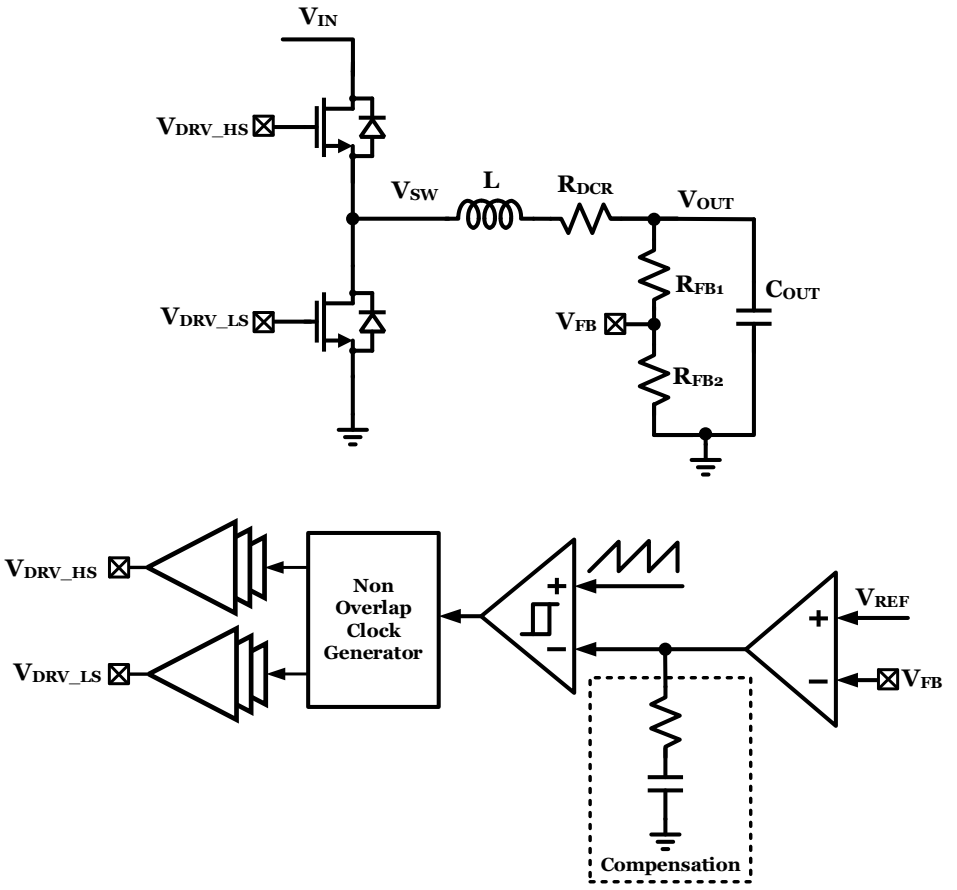


Figure 3.2. Conventional analog control for a buck converter

Digital based control techniques as shown in Figure 3.3 have considerably higher immunity to radiation over conventional analog control techniques [30] [33] [35]. A digital controller can be hardened against radiation induced errors and can offers increased functionality with potentially reduced component cost thus reducing the cost of

the system. This in-turn can lead to higher reliability. However, to ensure immunity to radiation, digital controllers must be fabricated on expensive radiation-hardened processes. Thus, conventional analog and digital controllers fabricated on largely available Bipolar-CMOS-Diode (BCD) processes are unable to mitigate the effects radiation induced errors.

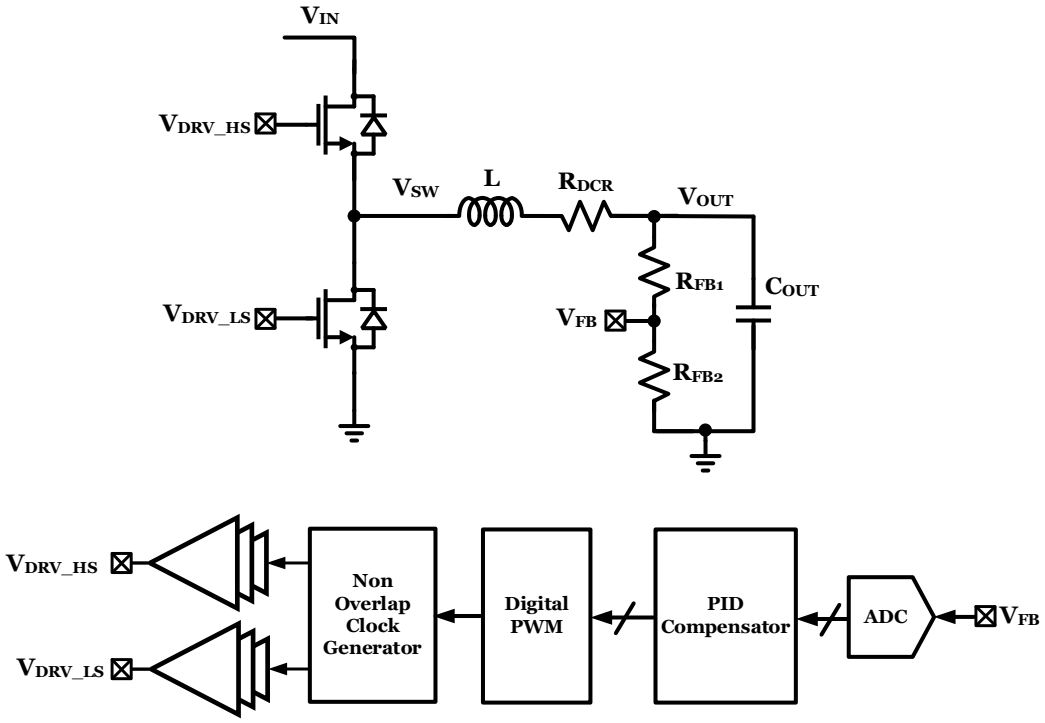


Figure 3.3. Conventional digital control for a buck converter

3.1.2 Time-Domain Control

A relatively new control approach for power converters is by using time as processing variable instead of voltage or current [37-44]. Time-domain controllers offer benefits of both digital and analog controllers. With time as the processing variable, the internal circuits can be implemented by standard digital logic gates. Thus, time-domain controllers can offer immunity to radiation events and are more resilient to process-voltage-temperature (PVT) variation just like digital controllers. Time-domain controllers

can also be scaled across process nodes similarly to digital controllers and thus be fabricated reasonable priced linear BCD processes. Moreover, time-domain based control can also eliminate the need for large passives both on-chip and off-chip. Time-domain based control can also eliminate the need for wide-bandwidth error amplifiers and PWM comparators thus resulting in reduced power consumption and silicon area. This can reduce the overall system size and cost which is crucial for any spacecraft. Time-domain control-based power converters are thus an attractive option for space applications.

Time-domain approach can be mapped to a conventional voltage-mode or current-mode approach by using the rules of thumb as shown in Figure 3.4 and Figure 3.5. An analog voltage or current can be easily converted to a time delay using a voltage-to-current (V2I) converter or transconductance stage (G_M) and a current controlled delay line (CCDL) with an input reference clock (CLK_{REF}). Considering Figure 3.4, an input voltage V_1 or an input current I_1 can be converted to with a proportional time-delay td_1 from CLK_{REF} to clock CLK_1.

$$td_1 \propto V_1 \tag{3.1}$$

$$td_1 = K_{CCDL} * V_1$$

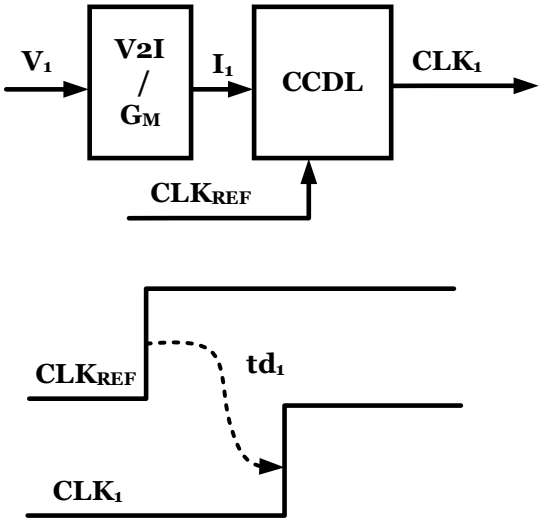
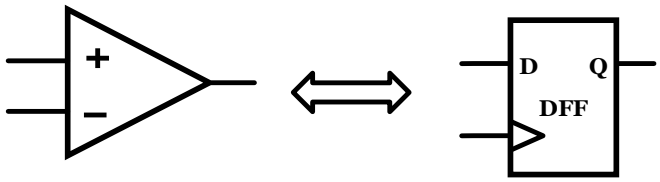


Figure 3.4. Mapping analog voltages and currents to time delays

A voltage domain comparator compares the difference of voltages between its inputs and defines the output accordingly. A time-domain comparator on the other hand compares the difference of the time-delay between its inputs and defines the output correspondingly. As shown in Figure 3.5, a rising edge triggered D flip-flop (DFF) can perfectly represent this comparator operation for a positive time-delay on the rising edge of the clock input.



Voltage Domain Comparator **Time Domain Comparator**

Figure 3.5. Mapping a voltage-domain comparator to a time-domain comparator

3.2 Prior Art

Various control techniques for power converters have been presented ever since their introduction. The prior art comprising of approaches targeted for spacecraft applications as well as converters with an emphasis on time-domain control techniques has been discussed. The control techniques are discussed in detail based on their step-down (buck) or step-up (boost converters) operation.

3.2.1 Buck Converters

The radiation tolerance of buck converters can be increased by using radiation hardened processes [25-26] [32-33]. The converter in [33] utilizes a current-mode hysteretic based control to achieve fast transient response. Moreover, a multi-phase approach is implemented to achieve high efficiency across the range of loads especially at light loads. A digital frequency synchronization circuit is also incorporated to synchronize

the switching frequency to that of an input reference frequency. The converter also incorporates an online offset calibration scheme cancels the input-referred offset of the hysteretic comparator thereby achieving high-output voltage regulation accuracy. The buck converter presented in [33] also incorporates a frequency synchronization scheme and adjustable slope, loop compensation to ensure stability and optimum performance across the specification ranges. Moreover, multiple buck converters in [32] can also be paralleled for increasing the output current of the overall system. However, these approaches employ significant analog circuits and a variety of external, off-chip components which can potentially be damaged by radiation in space.

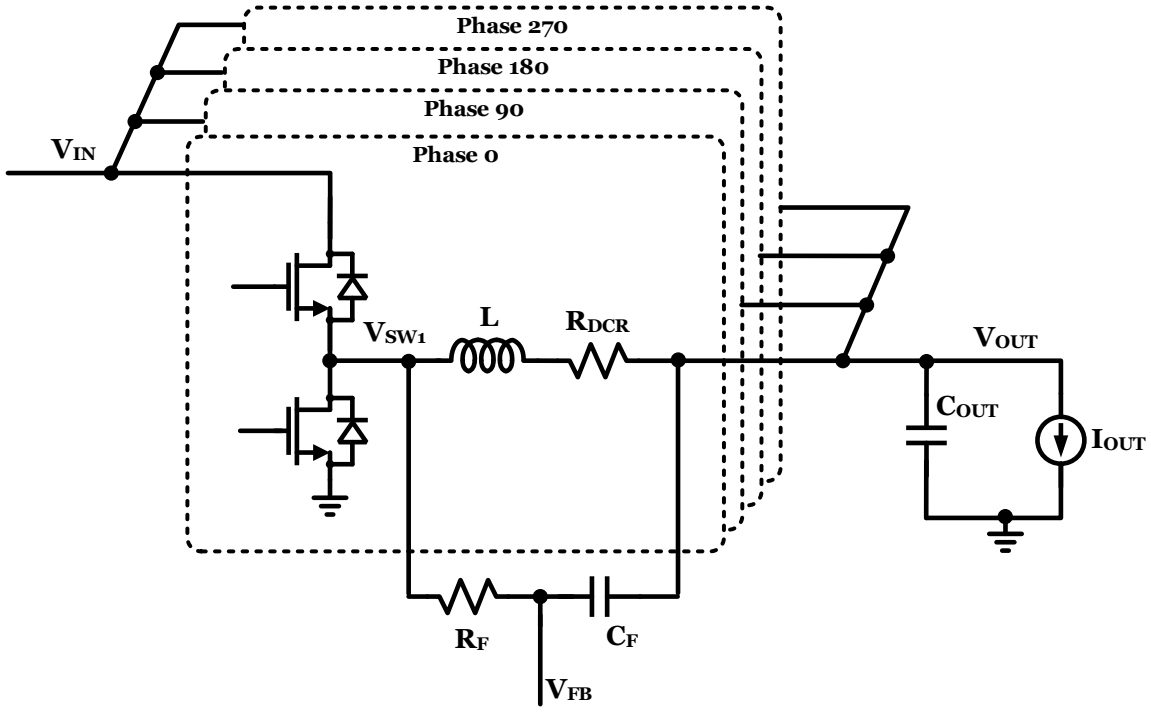


Figure 3.6. Multiphase current-mode hysteretic buck converter

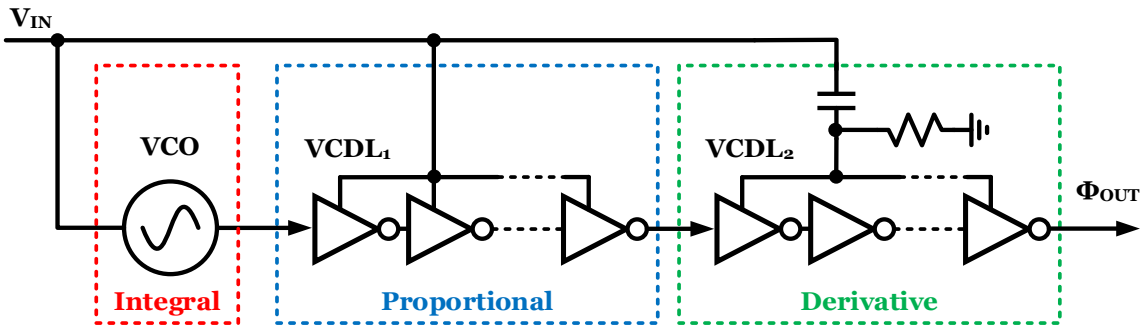


Figure 3.7. Time-domain PID compensator

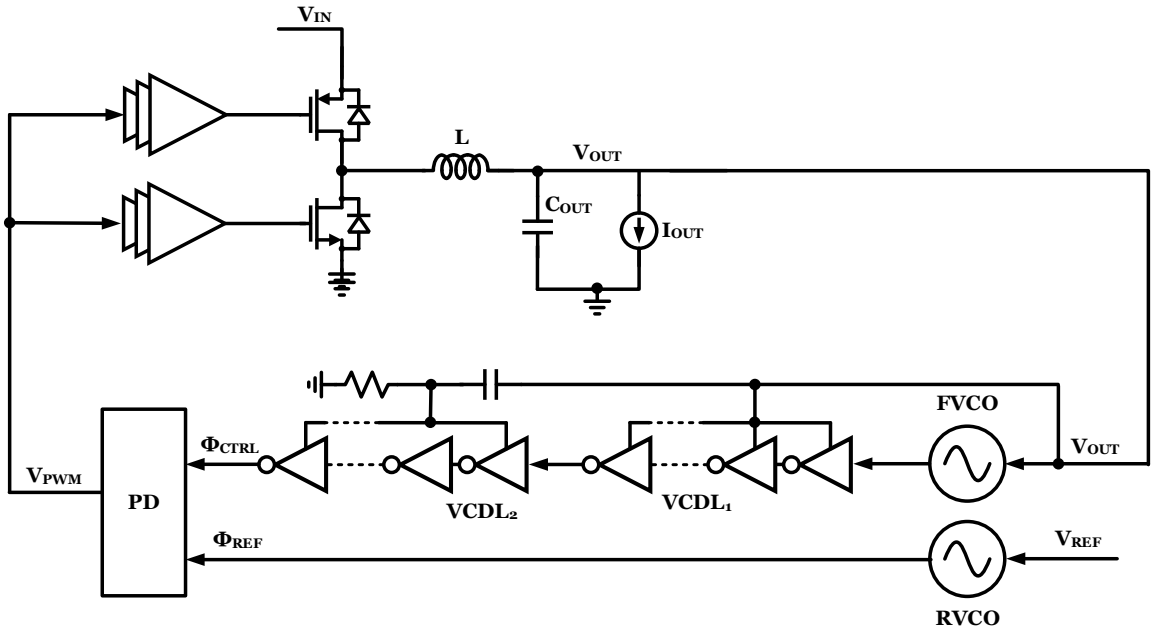


Figure 3.8. Buck converter with time-domain PID compensation

The buck converter presented in [41] introduces time-domain techniques to regulate the output voltage. The basic structure of a time-based type-III PID compensation scheme is shown in Figure 3.7 and comprises of a voltage-controlled oscillator (VCO) and voltage-controlled delay line (VCDL). This basic structure is then implemented differentially to convert a conventional voltage-mode hysteretic converter to a time-domain buck converter with standard digital logic gates as shown in Figure 3.8. The light load efficiency of such time-domain buck converters is further improved by introducing

pulse frequency modulation (PFM) operation with seamless transition between PWM and PFM modes. [39]. The time-domain buck converter shown in [38] [42] utilizes a VCO based inductor sensor and eliminates the need for slope compensation to prevent subharmonic oscillation. [37] utilizes a quasi-V^2 time-domain based hysteretic control for regulation and coupling-based inductor current emulator to support discontinuous mode conduction (DCM) operation for light loads.

3.2.2 Boost Converters

Radiation effects and radiation tolerant of boost converters have been shown in various prior art [25] [27] [29]. A radiation hardened boost converter employing classical current mode control with compensation is presented in [25]. Additional FETs are added to improve radiation tolerance of a boost converter in [29].

Boost converters with adaptive-on-time control techniques have also been discussed [47-50]. [50] employs adaptive-on-time current-mode control and a frequency locked loop that the switching frequency tracks the reference frequency. A frequency hopping scheme is also implemented to increase the efficiency at light loads and reduce EMI. In [47], a dual ramp modulation scheme is presented to solve instability of current-mode constant-on-time (COT) boost converters. An auxiliary current is added to the sensed inductor current and ensure stable and high efficiency in DCM. [48] introduces a mixed-ripple adaptive-on-time technique to use inductor current ripple in CCM and output voltage ripple in DCM for regulation. [49] utilizes an extended adaptive off-time to achieve quasi-fixed frequency for the entire range of output currents.

In a boost converter, the output and inductor are not charged during the same phases. Current-mode hysteretic approaches thus must utilize anti-phase inductor emulation to regulate the output voltage [45] [46]. As shown in Figure 3.9, the approach

in [45] utilizes three transconductance stages to algebraically add and emulate the inductor current. This approach realizes stable regulation with an inductor current ramp in-phase with the output voltage ripple. This is further simplified in [46] with a smaller design to reduce power consumption and achieve fast transient response.

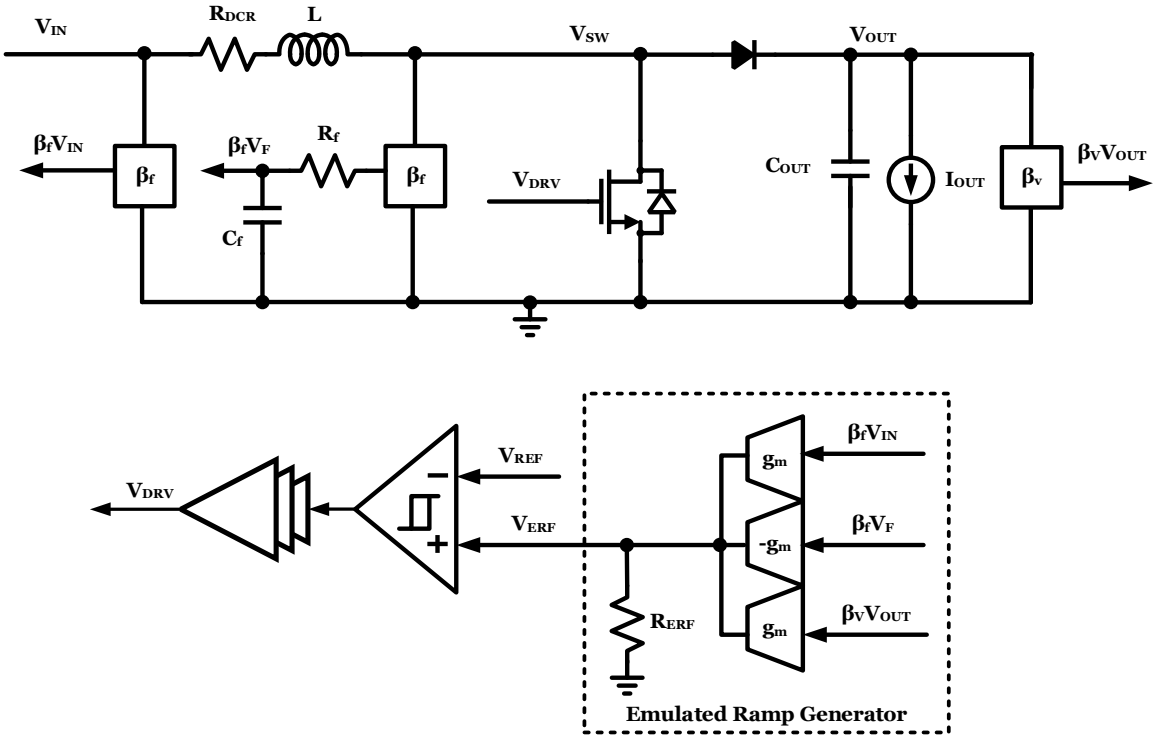


Figure 3.9. Inductor current emulation in boost converter

Most of the prior art discussed introduces various techniques to improve the performance of the boost converter. Their core regulation is based on classical current-mode or hysteretic control. However, time-domain based boost converters have not been investigated thoroughly in academic literature.

3.3 Objectives

The prior art has showcased a variety of approaches to achieve stable output voltage regulation for both buck and boost converters. State-of-art boost converters employing current mode, adaptive-on time or hysteretic control techniques for anti-phase inductor current emulation have been presented [45-50]. Buck converters employing time-domain control have been shown to eliminate subharmonic oscillations and improve their light load efficiency as well [37-42].

The primary research objective is to develop a common time-domain controller IC which can be employed for either buck or boost operation as shown in Figure 3.10 for aerospace and high-reliability applications. Each controller IC would be externally configured to operate either in buck or boost mode and would be hard-wired with an external power stage accordingly. The boost converter is designed to operate both in constant current (CC) and constant voltage (CV) modes whereas the buck converter is designed to operate in CV mode. Immunity to radiation SEEs is assured with a triple redundant bandgap reference.

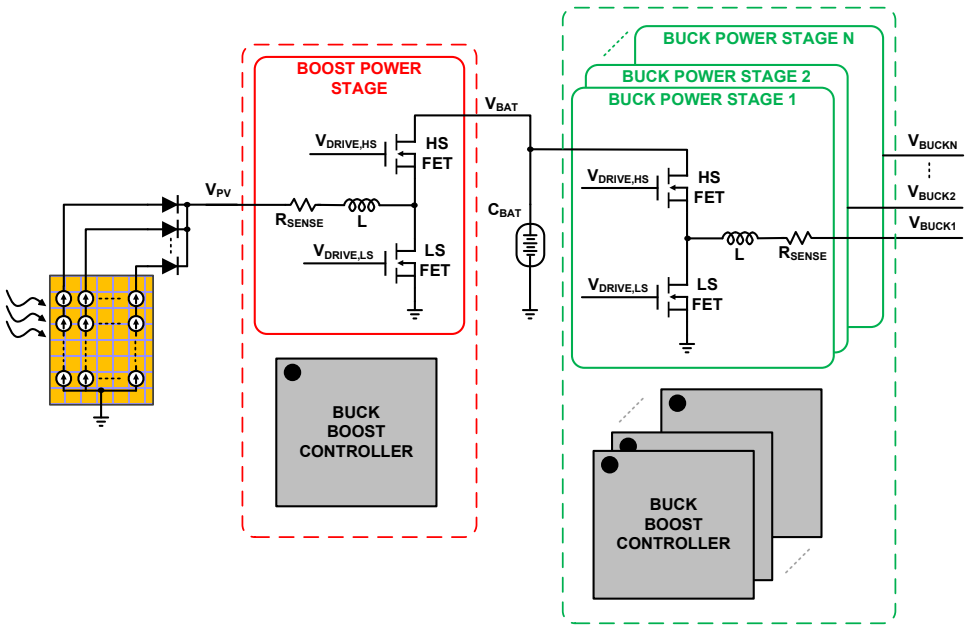


Figure 3.10. Application of the buck-boost controller IC on a spacecraft

The basic rules of thumb shown in Figure 3.4 and Figure 3.5 are utilized extensively in this research topic to implement time-domain processing. The time-delays are then processed using standard digital logic gates as per the desired operation to ensure stable regulated output for the designed buck and boost power converters.

3.4 Time-Domain Buck and Boost Converter

Figure 3.11 shows the top-level diagram for the buck-boost time-domain controller IC along with the individual buck and boost power stages. As shown, the system can be externally configured to either operate as a buck or boost converter using the SEL_{BUCK_BOOST} pin. The power stage consists of the external NMOS FETs both on high-side (HS) and low-side (LS) along with the converter filter comprising of the inductor (L) and the output capacitor (C_{OUT}). The additional external components used for inductor current emulation.

The time-domain controller IC features the time-domain based buck and boost controllers with a common driver is used to drive the external NMOS FETs. Current sensing and current limiting are implemented using an external sense resistor in series with the inductor along with stable startup sequencing for both buck and boost operational modes. A triple redundant bandgap reference for immunity to radiation and an on-chip oscillator provide the reference voltages and clocks to the system. The targeted specifications for the buck and boost operation are shown in Table 3.1.

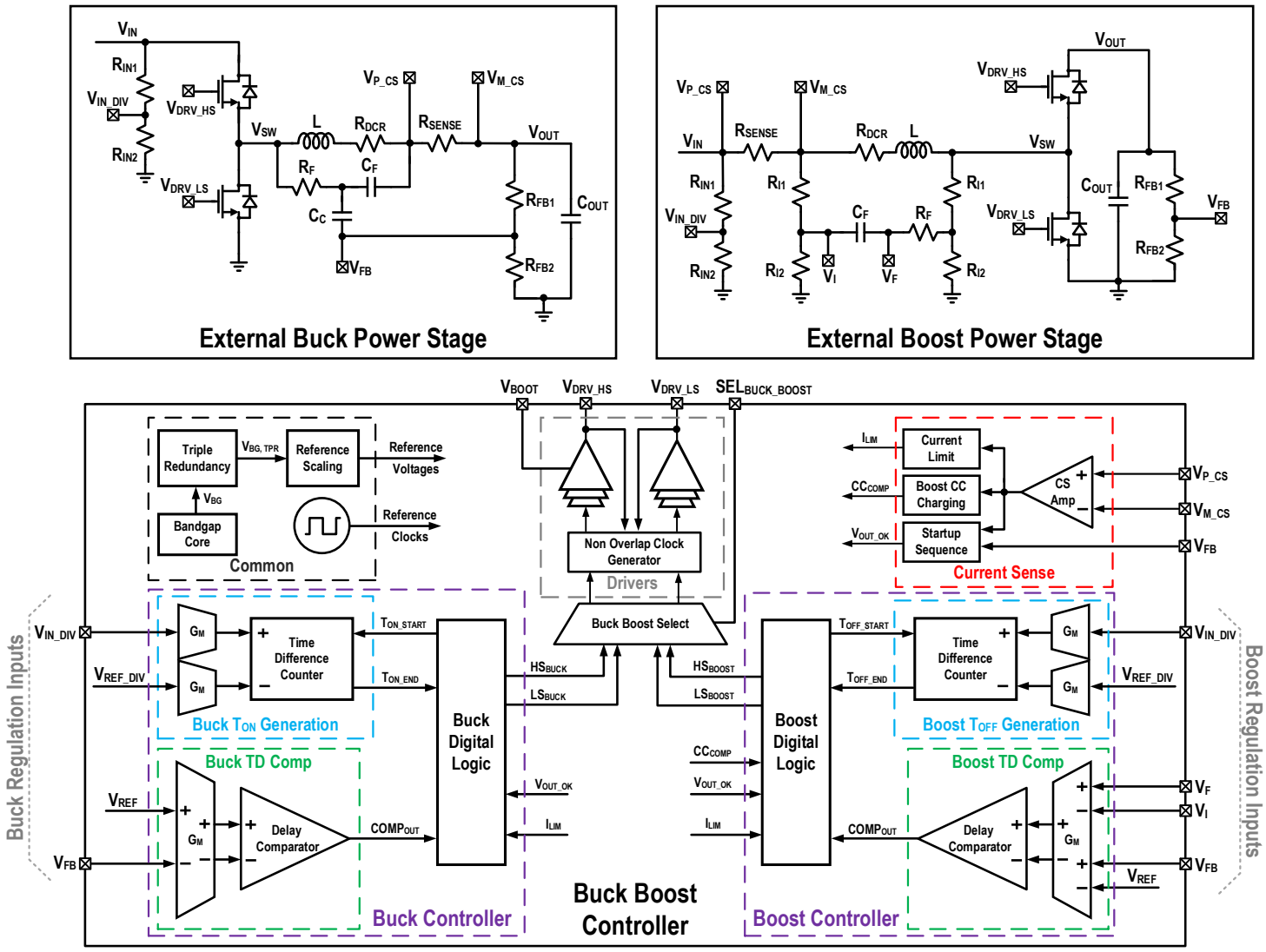


Figure 3.11. Time-domain buck-boost converter

Parameter	Specification	
	Buck Converter	**Boost Converter**
V_{IN}	26.95V – 32.8V	12.3V – 15V
V_{OUT}	3.3V, 5V	28V – 32.8V
I_{OUT}	5A	1.25A
F_{SW}	~250kHz	~250kHz
L	10µH	10µH
C_{OUT}	68µF	68µF (simulation)

Table 3.1. Buck and boost converter specifications

3.4.1 Inductor Current Emulation

As shown in Figure 3.2, classical analog control-techniques require a ramp at one of the inputs of the PWM comparator. The output of the PWM comparator determines the duty cycle (D) of the final drive signal to the switching FETs. Classical voltage-mode techniques generate the ramp internally, however current-mode techniques use the sensed inductor current to generate the ramp.

As compared to classical analog control techniques, hysteretic control techniques provide fast transient response, high output accuracy and efficiency. Moreover, hysteretic approaches require much less input and output filter capacitors [33]. Conventional voltage-mode hysteretic control techniques control the voltage ripple on the output. However, for current-mode hysteretic approaches, the inductor /switch must be sensed or emulated. This can be achieved by various ways. The primary way would be to use a sense resistor in series with the inductor current. A low pass passive filter formed by R_F and C_F across the inductor in parallel can also emulate the inductor current. [51] [52]. The emulated current approach in [33] is used as a base to develop the current emulation for the buck and boost converters developed in this chapter.

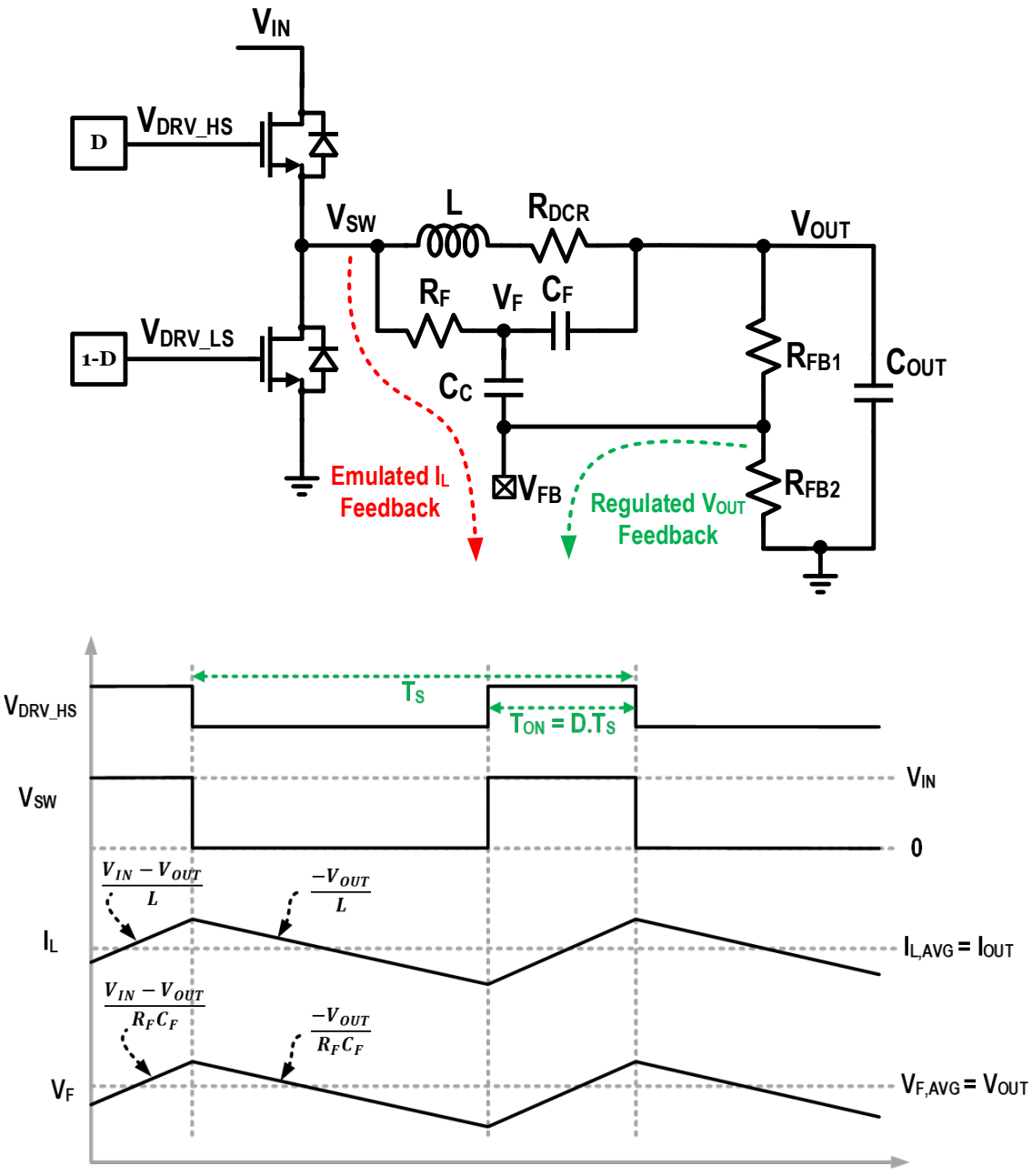


Figure 3.12. I_L emulation and waveforms in the buck converter

In buck mode, the inductor current is emulated using a passive network as shown in Figure 3.12. The ripple on the output of the passive low pass filter formed by R_F and C_F across the inductor is further coupled through C_C. The I_L ripple information is then

superimposed on the feedback voltage (V_{FB}) to be used for regulation. The green path in Figure 3.12 shows the slow path for V_{OUT} regulation whereas the red path shows the fast path for the I_L emulation. In a buck converter, I_L rises and V_{OUT} charges in the same phase. Hence, I_L ripple can be easily superimposed on V_{FB} or V_{OUT}.

$$V_F = I_L * R_{DCR}\left(\frac{\left[1 + s\frac{L}{R_{DCR}}\right]}{[1 + s\,R_F C_F]}\right) + V_{OUT} \qquad (Buck)$$

Similarly, in boost mode, the inductor current is emulated using a passive network as shown in Figure 3.13. The green path in Figure 3.13 shows the slow feedback path for V_{OUT} regulation whereas the red path shows the fast feedback path for the I_L emulation. Due to the input voltage specifications in boost mode, both V_{SW} and V_{IN} are first stepped down using a resistor divider network (R_{I1}, R_{I2}) with a feedback factor of β_F to voltage levels that can be utilized within the IC (<5V). In a boost converter however, I_L rises and V_{OUT} charges in the opposite phases. Hence, I_L ripple cannot be easily superimposed on V_{FB} or V_{OUT}. The emulated I_L inductor current is passed differentially using a low pass filter comprising of R_F and C_F through ($V_I - V_F$). As shown in Figure 3.13, (V_I- V_F) is in phase with the I_L and thus is passed on to the time-domain comparator inputs correspondingly to generate D.

$$V_F = -I_L * R_{DCR}\left(\frac{\left[1 + s\frac{L}{R_{DCR}}\right]}{[1 + s\,R_F C_F]}\right) + V_I \qquad (Boost)$$

$$V_I - V_F = I_L * R_{DCR}\left(\frac{\left[1 + s\frac{L}{R_{DCR}}\right]}{[1 + s\,R_F C_F]}\right) \qquad (Boost)$$

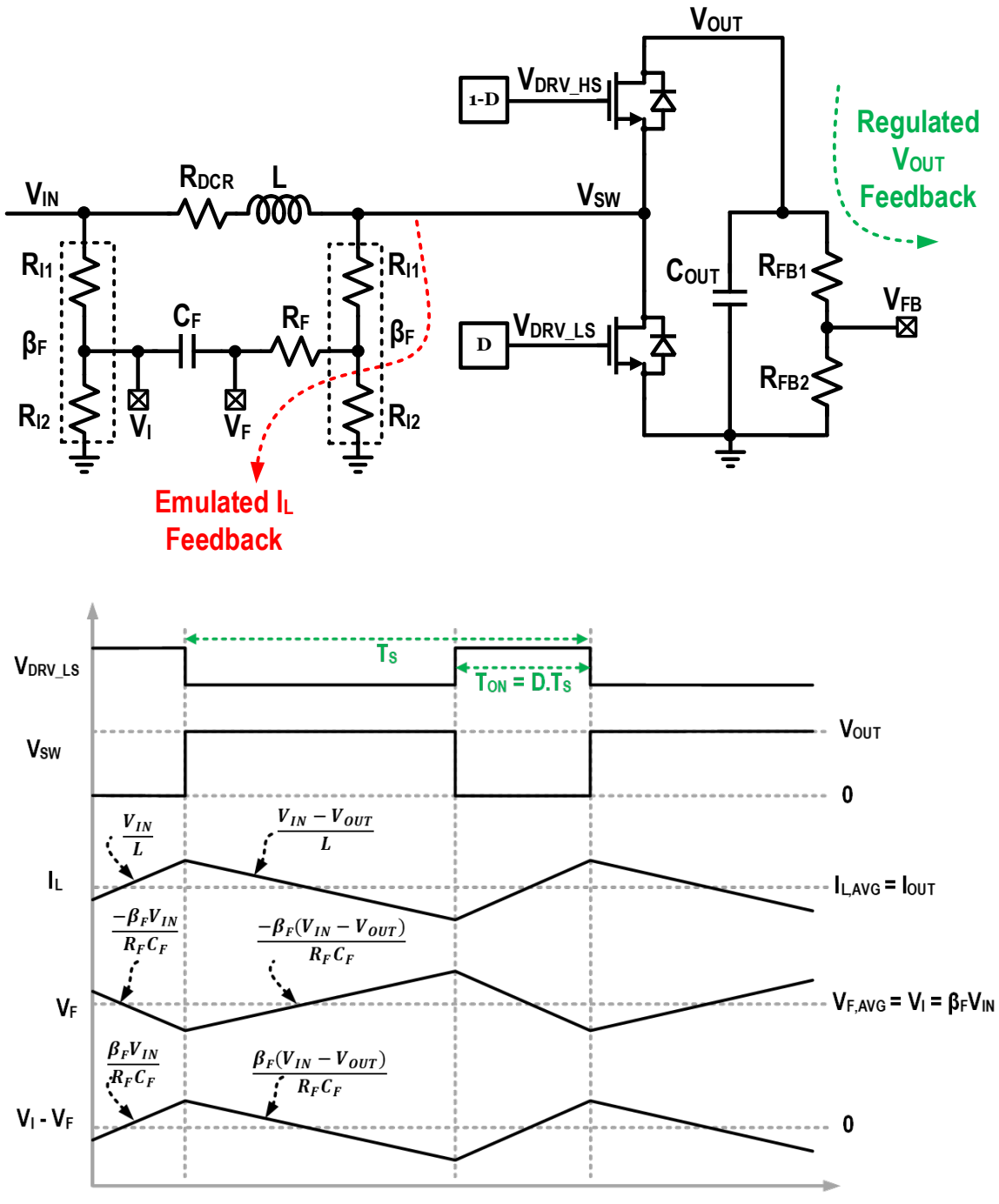


Figure 3.13. I_L emulation and waveforms in the boost converter

3.4.2 Time-Domain Comparator

Conventional hysteretic controllers employ voltage-based comparators to generate the PWM signal to drive the switches of the power stage. To improve immunity to radiation, a time-domain comparator instead of voltage comparator is employed in the presented controller IC. The time domain controller employs the basic rules of thumb developed in Figure 3.4 and Figure 3.5. As discussed in the earlier section, the inductor current is emulated in both buck and boost modes to enable current-mode hysteretic based control for fast transient response. Output voltage (V_{OUT}) is regulated with time-domain comparators (TDCOMP) for valley current-mode control in buck and peak current-mode control in boost operation.

3.4.2.1 Buck Time-Domain Comparator

As discussed in the earlier section, the emulated inductor current in buck mode is superimposed on V_{FB} and is passed to the buck TDCOMP. The implementation and waveforms for the buck TDCOMP are shown in Figure 3.14.

The buck TDCOMP compares V_{FB} with V_{REF} and converts the voltage difference into differential currents I_{P_CCDL} and I_{M_CCDL} using a fully-differential G_M stage. I_{P_CCDL} and I_{M_CCDL} are then given as inputs to a pair of CCDLs with CLK_{20M} as the common input reference frequency. The time delay between the output of the CCDLs, CLK_{P_CCDL} and CLK_{M_CCDL} is then compared by a DFF as a time-domain phase comparator. The DFF then generates a high pulse on the comparator output $COMP_{OUT}$ whenever the falling edge of V_{FB} crosses V_{REF}. This high pulse which is then latched on and passed on to the buck digital logic for processing. Thus, the valley of I_L is detected by the buck TDCOMP for valley current-mode control.

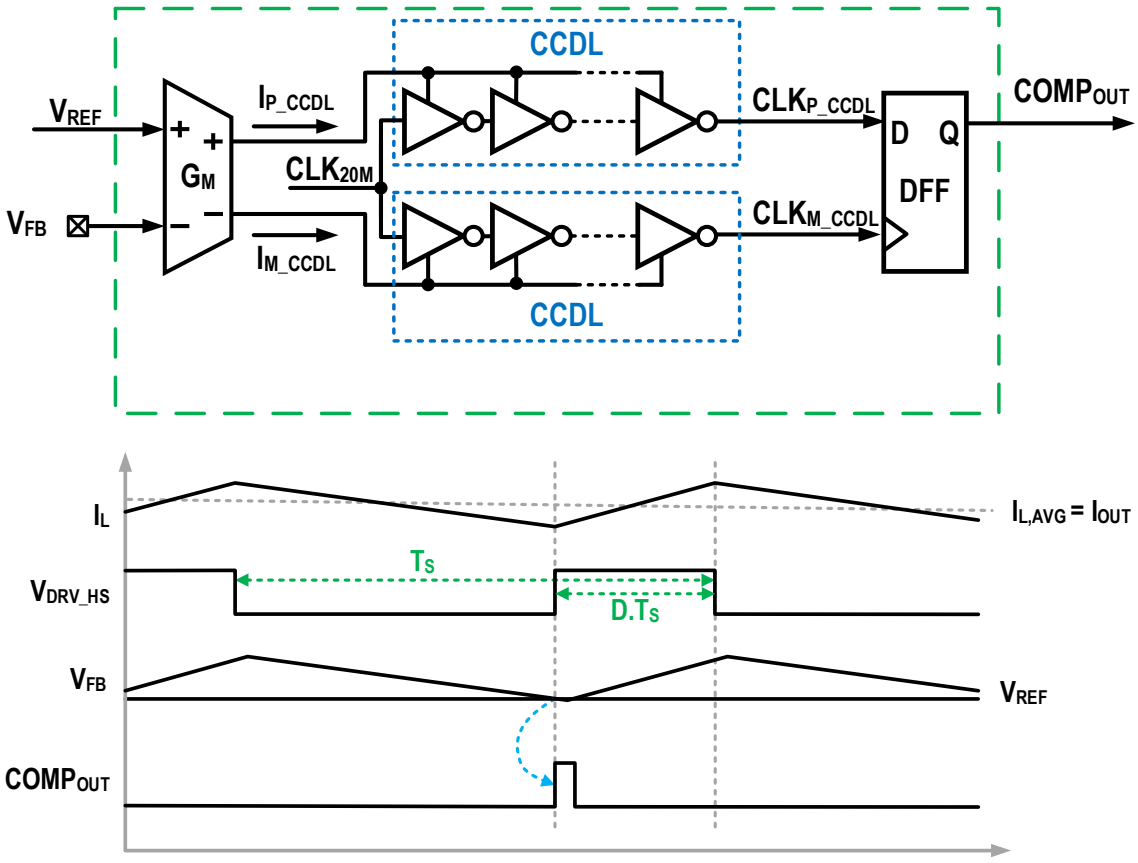


Figure 3.14. Buck TDCOMP implementation and waveforms

3.4.2.2 Boost Time-Domain Comparator

As discussed in the earlier section, the emulated inductor current in boost mode is differentially forwarded through ($V_I - V_F$) to the boost TDCOMP. The implementation and waveforms for the boost TDCOMP are shown in Figure 3.15.

The boost TDCOMP compares ((V_I - V_F) + V_{FB}) with V_{REF} and converts the voltage difference into differential currents I_{P_CCDL} and I_{M_CCDL} using a double fully-differential G_M stage. I_{P_CCDL} and I_{M_CCDL} are then given as inputs to a pair of CCDLs with CLK_{20M} as the common input reference frequency. The time delay between the output of the CCDLs, CLK_{P_CCDL} and CLK_{M_CCDL} is then compared by a DFF as a time-domain phase comparator. The DFF then generates a high pulse on the comparator output $COMP_{OUT}$ whenever the

rising edge of $((V_I - V_F) + V_{FB})$ crosses V_{REF}. This high pulse which is then latched on and passed on to the boost digital logic for processing. Thus, the peak of I_L is detected by the boost TDCOMP for peak current-mode control.

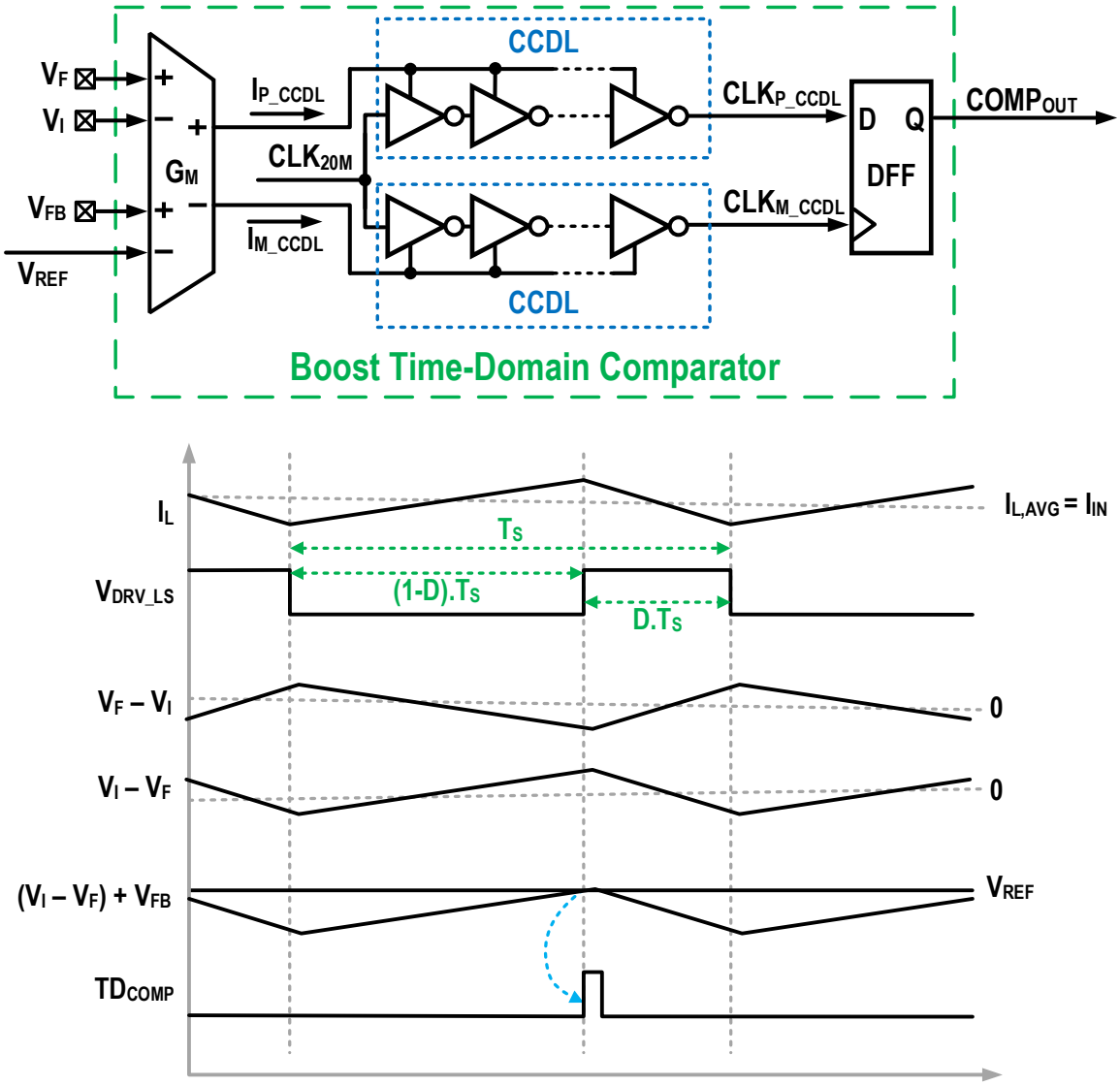


Figure 3.15. Boost TDCOMP implementation and waveforms

The G_M stage is implemented using a PMOS input pair, whereas the CCDL is implemented using a chain of current starved inverters as shown in Figure 3.16. In buck mode, the inputs V_I and V_F for the G_M stage are tied to V_{REF}.

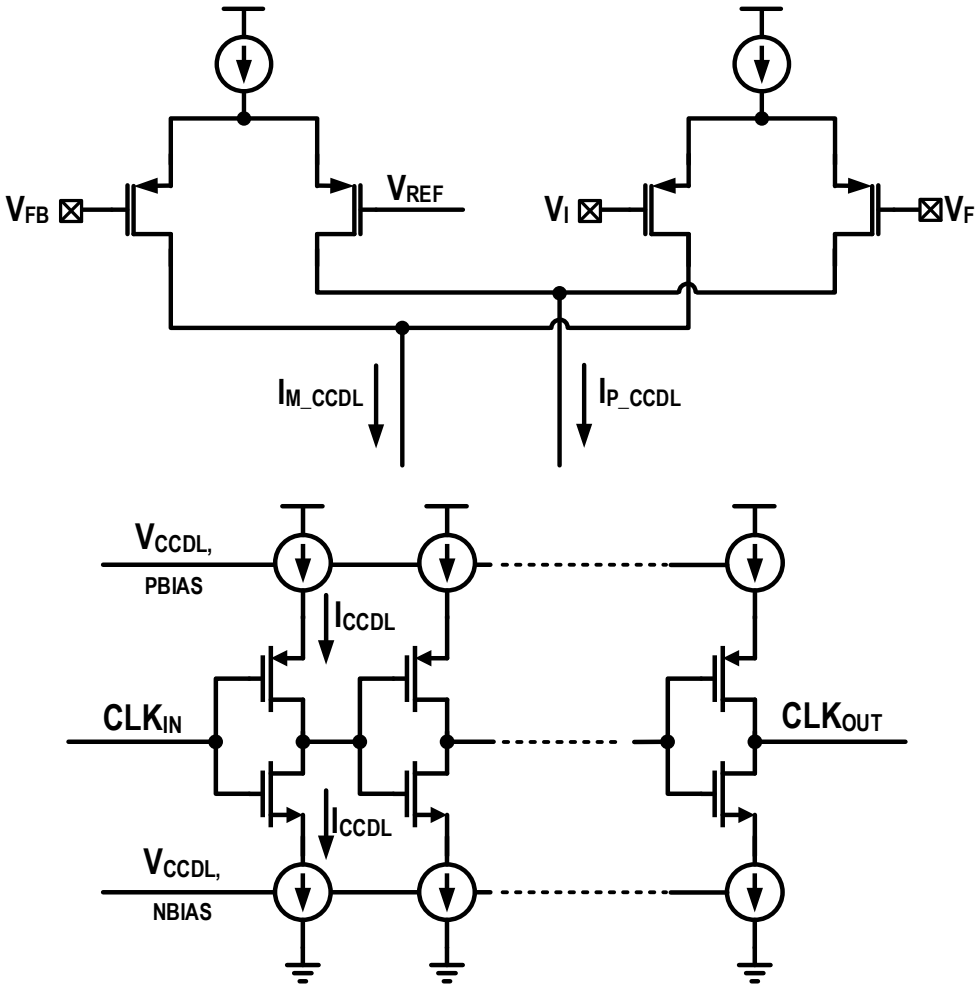


Figure 3.16. Implementation of the GM stage and CCDLs

3.4.3 Adaptive COT Time-Domain Controller

When the converter operates in discontinuous conduction mode (DCM), I_L is not always positive. This can lead to differences in the efficiency of the converter based on the operating mode of the converter. Pulse frequency modulation (PFM) is a technique where the converter operates in a boundary condition. PFM ensures low average current consumption leading to higher efficiency. However, this approach leads to variable switching frequency (F_{SW}) [53]. Alternatively, constant on-time or constant off-time (COT) operation with DCM for buck or boost operation respectively at light loads is ideal for high

current, fast transient load and fixed F_{SW}. Control loop compensation is not required with either operating mode, which reduces design time and external component count. The presented controller IC employs constant on-time or constant off-time (COT) operation with DCM for buck or boost operation respectively.

As per the volt-sec balance in steady state in Equation (1.2) and Equation (1.3), the on-time and off-time for a buck and boost converter can be written as follows.

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} * T_S \qquad (Buck)$$

$$T_{OFF} = \frac{V_{IN}}{V_{OUT}} * T_S \qquad (Boost)$$

Thus, for a constant F_{SW} or T_S, and a regulated value of V_{OUT}, T_{ON} or T_{OFF} can be made adaptive to changes in V_{IN} for a buck or boost converter respectively. For a higher V_{IN}, the T_{ON} or T_{OFF} is reduced to regulate V_{OUT} and vice versa. This adaptive nature of T_{ON} to V_{IN} is incorporated into the buck and boost time-domain controller when T_{ON} or T_{OFF} is generated and leads to better line transient.

As shown in Figure 3.17, the adaptive COT generation block for both buck and boost modes is implemented in time-domain using a pair of G_M stages, a pair of CCDLs and 10bit-counters CNT_{IN}, CNT_{REF} and CNT_{ON}.

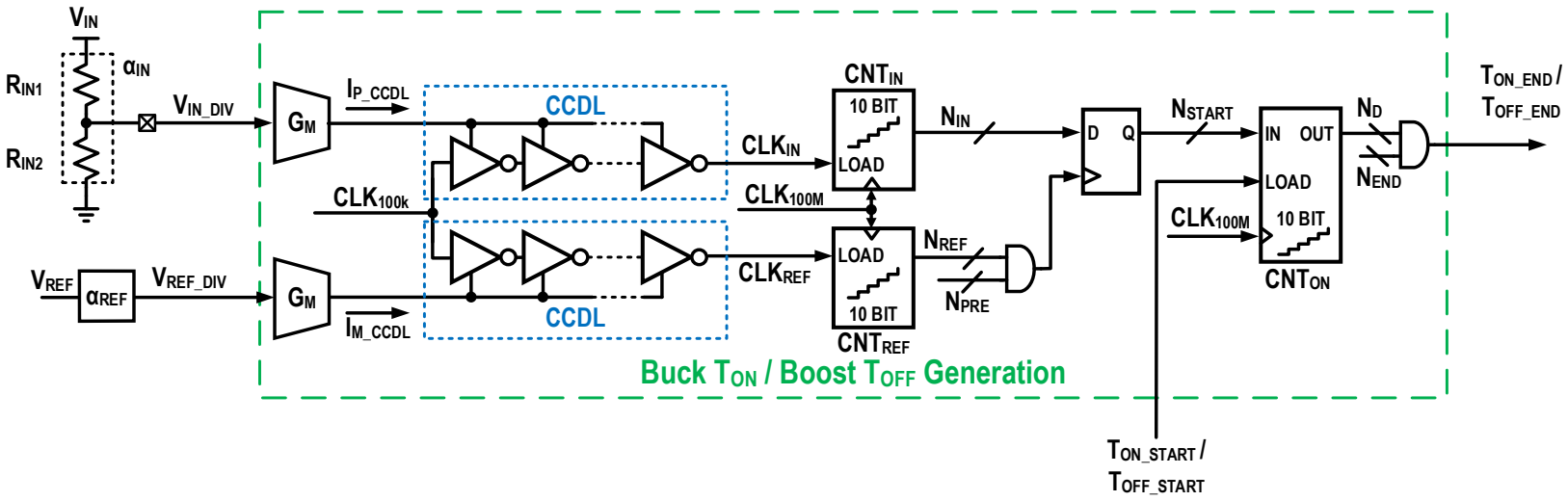


Figure 3.17. Adaptive COT generation in buck and boost time-domain controller

3.4.3.1 Buck Time-Domain Controller

Consider buck operation for now. The exact operation can be correlated to boost operation as well. It can be considered that V_{OUT} is in regulation to realize the adaptive nature of T_{ON} to V_{IN}. Thus, V_{FB} is equal to V_{REF} at regulated V_{OUT} and Equation (1.2) can be rewritten as follows,

$$\frac{T_S}{T_{ON}} = \frac{V_{IN}}{V_{OUT}} = \frac{V_{IN}}{\beta * V_{FB}} = \frac{V_{IN}}{\beta * V_{REF}}$$

Constant values α_{IN} and α_{REF} are chosen to divide V_{IN} and V_{REF} to V_{IN_DIV} and V_{REF_DIV} respectively. The constant values are chosen such that the ratio of V_{IN_DIV} to V_{REF_DIV} tends to unity at steady state for the nominal design values of V_{IN}, V_{OUT} and I_{OUT}. The voltages V_{IN_DIV} and V_{REF_DIV} are passed as inputs to a pair of GM stages, whose output currents I_{IN_CCDL} and I_{REF_CCDL} respectively are further forwarded to a pair of CCDLs. The CCDLs generate clocks CLK_{IN} and CLK_{REF} with a time delay of td_{IN} and td_{REF} proportional in reference to a CLK_{100k}. From Equation (3.1), the time delays td_{IN} and td_{REF} are thus proportional to the input voltages V_{IN_DIV} and V_{REF_DIV} respectively.

$$\frac{\alpha_{IN} V_{IN}}{\alpha_{REF} V_{REF}} = \frac{V_{IN\_DIV}}{V_{REF\_DIV}} \rightarrow 1$$

$$\frac{\alpha_{IN} V_{IN}}{\alpha_{REF} V_{REF}} = \frac{V_{IN\_DIV}}{V_{REF\_DIV}} = \frac{td_{IN}}{td_{REF}} \rightarrow 1$$

The 10-bit counters CNT_{REF} and CNT_{IN} start incrementing at the rising edge of CLK_{REF} and CLK_{IN} respectively with a frequency of 100MHz. As shown in Figure 3.17 and Figure 3.18, counter CNT_{REF} counts until N_{REF} reaches N_{PRE} at which point the value of N_{IN} is latched to N_{START}. The difference of the latched value of N_{IN} (=N_{START}) to the pre-determined value of N_{REF} (=N_{PRE}) can be corresponded to the difference of voltages between V_{IN_DIV} and V_{REF_DIV}. If $N_{START} \neq N_{PRE}$, then it can be concluded that $V_{IN\_DIV} \neq V_{REF\_DIV}$. Thus, the deviation of V_{IN_DIV} to V_{REF_DIV} from unity is thus measured by the count N_{START}. This deviation from unity indicates a change in T_{ON} required to keep the switching

frequency quasi-constant. A successive 10-bit counter CNT_{ON} is thus loaded to the count N_{START} to represent this difference.

The start of T_{ON} is determined by the assertion of $COMP_{OUT}$, the output of the TDCOMP. As shown in the timing diagram in Figure 3.18, T_{ON_START} is set high signifying the start of T_{ON} as $COMP_{OUT}$ is asserted from the TD_{COMP}. The 10-bit counter CNT_{ON} then starts counting from N_{START} at the rising edge of T_{ON_START}. As shown in the timing diagram in Figure 3.18, the time required for CNT_{ON} to count from N_{START} to N_D (=N_{END}) is the required T_{ON} for the buck converter adaptive to V_{IN_DIV}. Since N_{START} is directly proportional to $V_{IN\_DIV,}$ the value of generated T_{ON} adapts to changes in V_{IN}.

The above COT generation can be shown by the following set of equations. After the counter CNT_{IN} and CNT_{REF} and after latching N_{START} = N_{IN} at N_{REF} = N_{PRE}, the time delays can be written as follows.

$$\frac{V_{IN\_DIV}}{V_{REF\_DIV}} = \frac{td_{IN}}{td_{REF}} = \frac{\Delta N_{IN}}{\Delta N_{REF}} \rightarrow 1$$

Here, ΔN_{IN} and ΔN_{REF} refers to the difference of counts from the final count of N_{END} to the latched values of N_{IN} and N_{REF} due to time delays td_{IN} and td_{REF} respectively.

$$\frac{V_{IN\_DIV}}{V_{REF\_DIV}} = \frac{td_{IN}}{td_{REF}} = \frac{\Delta N_{IN}}{\Delta N_{REF}} = \frac{N_{END} - N_{IN}}{N_{END} - N_{REF}} \rightarrow 1$$

$$\frac{V_{IN\_DIV}}{V_{REF\_DIV}} = \frac{td_{IN}}{td_{REF}} = \frac{\Delta N_{IN}}{\Delta N_{REF}} = \frac{N_{END} - N_{START}}{N_{END} - N_{PRE}} \rightarrow 1$$

Moreover, (N_{END} – N_{START}) is the required adaptive T_{ON} as generated by the third counter CNT_{ON}. N_{END} and N_{PRE} are hard-coded into the controller as 2*$N_{TON,HC}$ and $N_{TON,HC}$ respectively.

$$\frac{N_{END} - N_{START}}{N_{END} - N_{PRE}} = \frac{N_{TON,ADAPTIVE}}{2 * N_{TON,HC} - N_{TON,HC}} = \frac{N_{TON,ADAPTIVE}}{N_{TON,HC}} \rightarrow 1$$

$$N_{TON,ADAPTIVE} = N_{END} - N_{IN} = N_{END} - N_{START} \quad \rightarrow \quad N_{TON,HC} \tag{3.2}$$

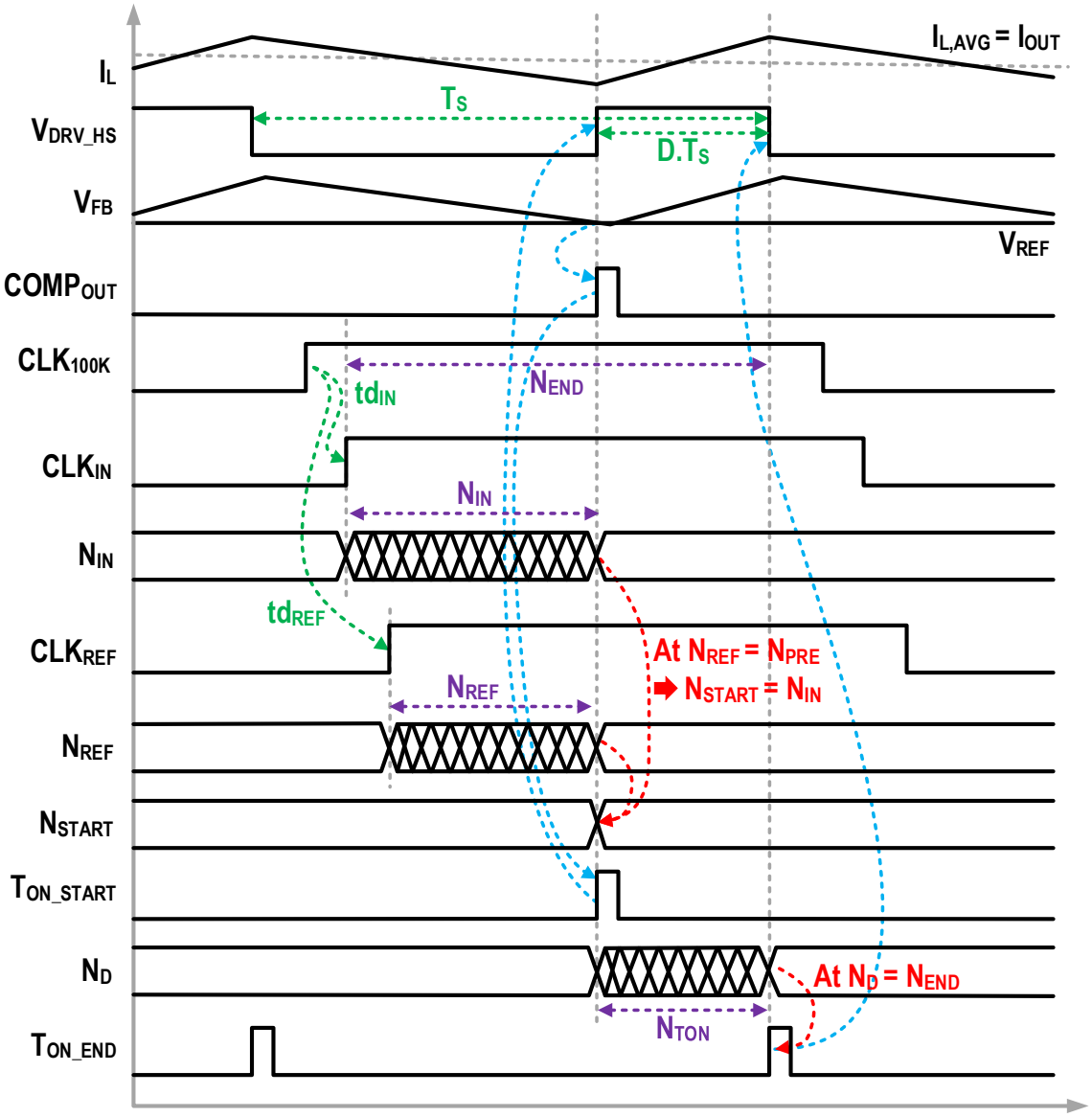


Figure 3.18. Waveforms for adaptive COT generation in buck time-domain controller

Considering the following nominal steady state values of V_{OUT} (= 5V), V_{IN} (= 28V), I_{OUT} (= 5A) and F_{SW} (= 200kHz), the ideal value of T_{ON} is calculated. Thus, the ideal number of counts required with a 100MHz clock can be calculated.

$$T_{ON,IDEAL} = \frac{V_{OUT}}{V_{IN}} * T_S = \frac{5}{28} * 5\mu s = 892.8ns$$

$$N_{TON,IDEAL} = \frac{T_{ON,IDEAL}}{10ns} \approx 89\ counts$$

However, the hardcoded value of T_{ON} is adjusted to account for various losses. Moreover, functionality is provided to hardcode these values externally.

$$N_{TON,HC} = 101\ counts$$

3.4.3.2 Boost Time-Domain Controller

The exact same algorithm used to generate the adaptive T_{ON} in the buck time-domain controller is employed to generate the adaptive T_{OFF} in the boost time-domain controller. The timing waveforms for the same are shown in Figure 3.19. With reference from Equation (3.2), the adaptive T_{OFF} is shown in Equation (3.3) as follows.

$$N_{TOFF,ADAPTIVE} = N_{END} - N_{IN} = N_{END} - N_{START} \quad \rightarrow \quad N_{TOFF,HC} \tag{3.3}$$

Considering the following nominal steady state values of V_{OUT} (= 32.8V), V_{IN} (= 12.3V), I_{OUT} (= 1.25A) and F_{SW} (= 200kHz), the ideal value of T_{OFF} is calculated. Thus, the ideal number of counts required with a 100MHz clock can be calculated.

$$T_{OFF,IDEAL} = \frac{V_{IN}}{V_{OUT}} * T_S = \frac{12.3}{32.8} * 5\mu s = 1875ns$$

$$N_{TOFF,IDEAL} = \frac{T_{OFF,IDEAL}}{10ns} \approx 187\ counts$$

However, the hardcoded value of T_{OFF} is adjusted to account for various losses. Moreover, functionality is provided to hardcode these values externally.

$$N_{TOFF,HC} = 178\ counts$$

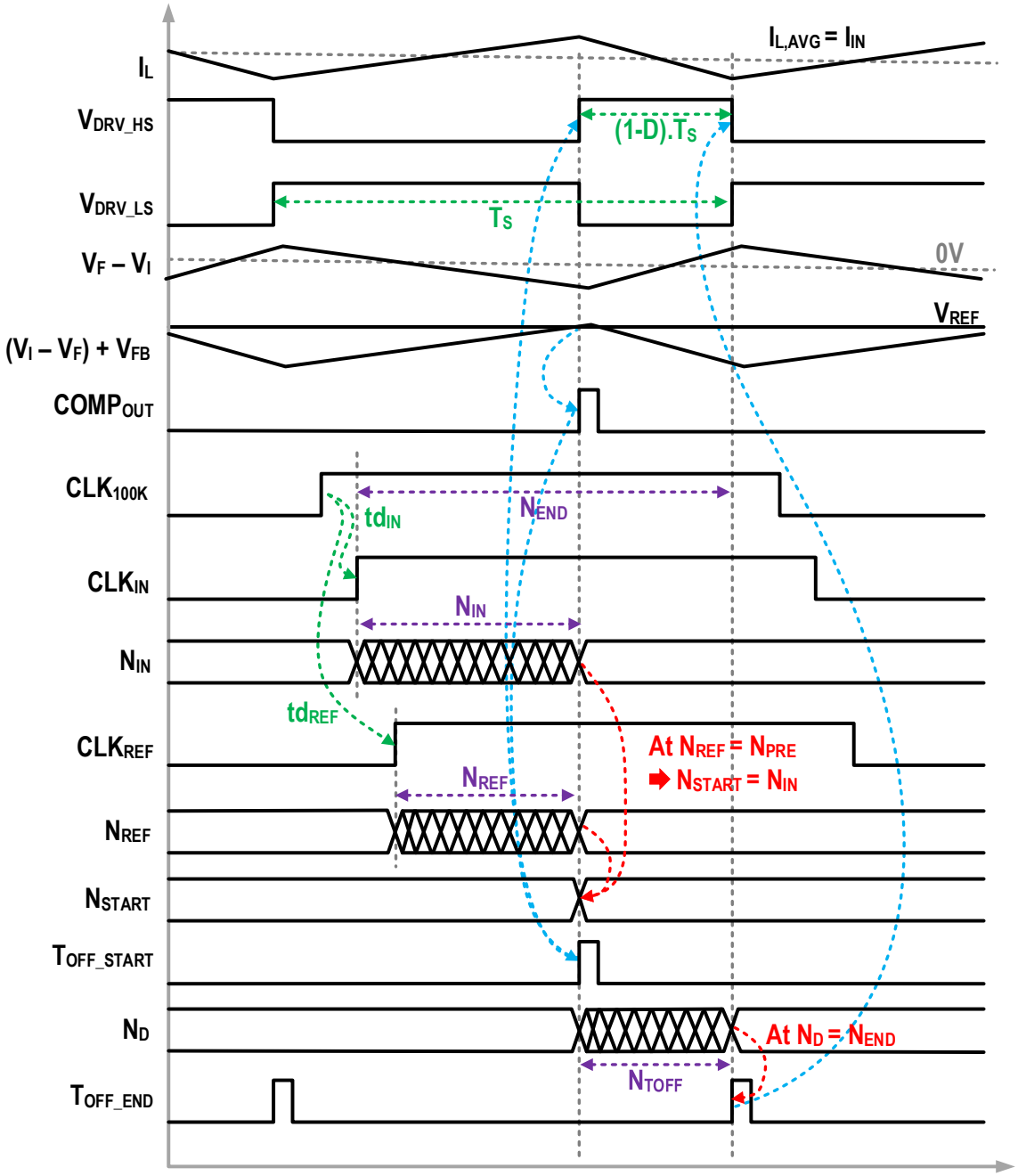


Figure 3.19. Waveforms for adaptive COT generation in boost time-domain controller

3.4.4 Driver and External Power Stage

The power stage for both buck and boost modes of operation are implemented external to the controller IC with n-channel FETs and an inductor. The same FETs and inductor are used in both buck and boost modes of operation and this proves to be advantageous in the driver design. The model number for the NMOS FET is NVMFS5C673NL which is supplied in DFN5 package by ON Semiconductor [54]. The $R_{DS,ON}$ of the FET is 11mΩ at a V_{GS} of 4.5V and I_D of 20A. Similarly, the model number for the inductor is IHLP-6767GZ-11 which is supplied by Vishay. The inductance value is 10μH with a R_{DCR} of 8.9mΩ and I_{SAT} of 17A [55].

A common driver is designed for both buck and boost modes of operation with SEL_{BUCK_BOOST} pin selecting the operational mode. If $SEL_{BUCK\_BOOST\ is\ set}$ to 0V, then buck mode is enabled, whereas setting it to 5V enables boost mode of operation. A common driver can be designed as the driving FETs in both modes of operation are the same. The implementation of the driver and power stage for buck mode is shown in Figure 3.20. The same can be extended for boost mode accordingly. The driver incorporates trimmable deadtime control to avoid shoot-through current and large current spikes during transitions. The driver for each FET also includes non-overlap control to reduce shoot through currents within the IC as well.

As the high-side FET is a NMOS device, bootstrapping is required. As shown in Figure 3.2, this is implemented by conventional methods by using an external diode D_{BOOT} and an external capacitor C_{BOOT}. Level shifters are also incorporated to bootstrap the HS_DRIVE signal from (0 to 5V) to (V_{SW} to V_{BOOT}) voltage levels and vice versa for deadtime control.

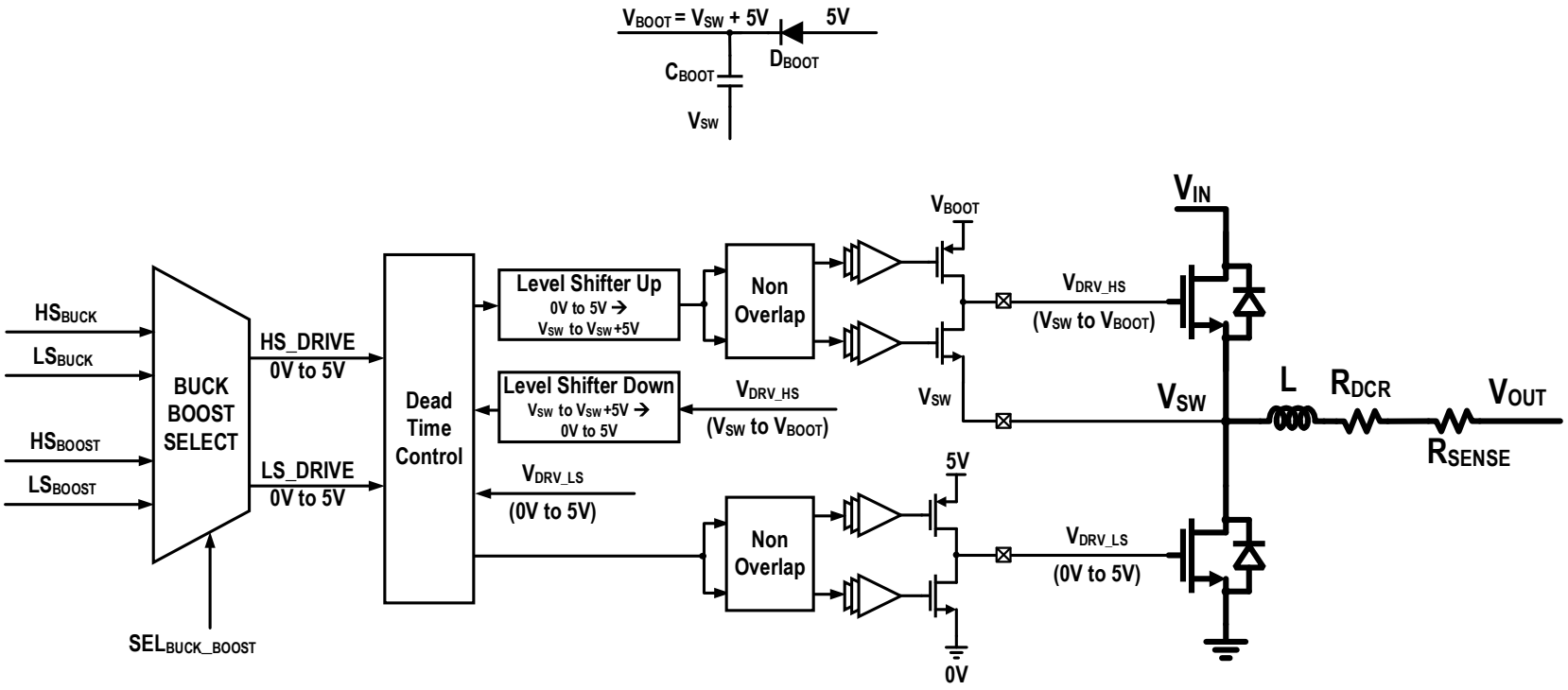


Figure 3.20. Implementation of common driver and bootstrapping

3.4.5 Current Sensing, Current Limit and Soft Start

In addition to the I_L emulation discussed in the earlier sections, I_L is additionally sensed through a high-precision sense resistor R_{SENSE} in series with the inductor. This is added to implement current limit and startup in boost mode of operation. The value of R_{SENSE} is 5mΩ with a low tolerance of 0.5% and a power rating of 5W.

A current sense amplifier (CSA) measures the voltage across the sense resistor. The implementation of the CSA for boost mode is shown in Figure 3.21. The CSA has a cascoded common-gate topology and utilizes high-voltage laterally-diffused MOS (LDMOS) to support the various specifications in both buck and boost mode. High-voltage resistors $R_{S,IN}$ and $R_{S,OUT}$ are matched to achieve a ratioed sensing gain of 0.125 V/A in buck mode and 0.250 V/A in boost mode from I_L to V_{SENSE}.

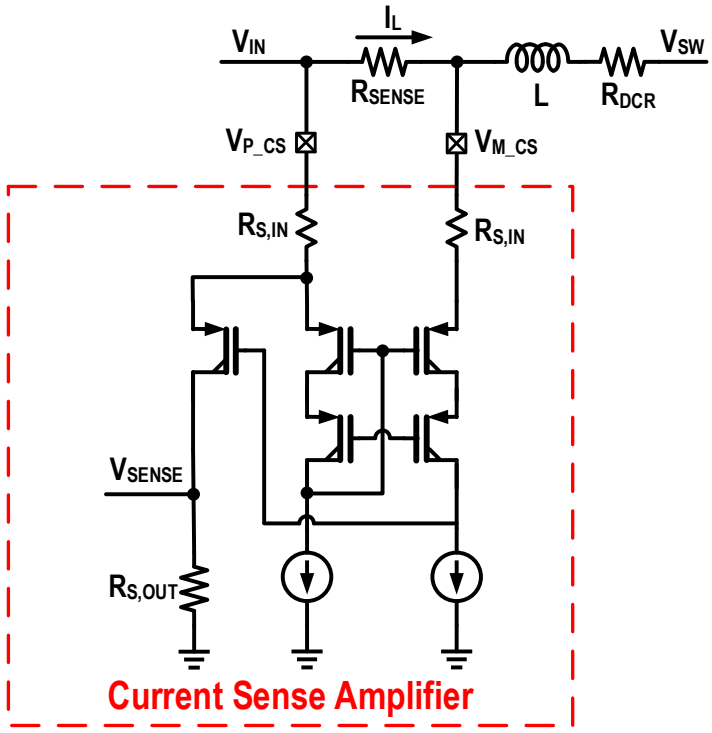


Figure 3.21. Implementation of the current sense amplifier

The output of the CSA, V_{SENSE} is compared with current limit references in both buck and boost mode using comparators to determine if the inductor has reached current limit. These reference voltages are determined based on the gain of CSA in various modes. For buck mode, the I_{LIM} was set at 14A whereas in boost mode it was set at 3A. Once the converter hits current limit, the low-side (LS) FET would be switched on, thereby discharging the inductor. This logic for current limit is implemented as part of the digital control logic for buck and boost modes.

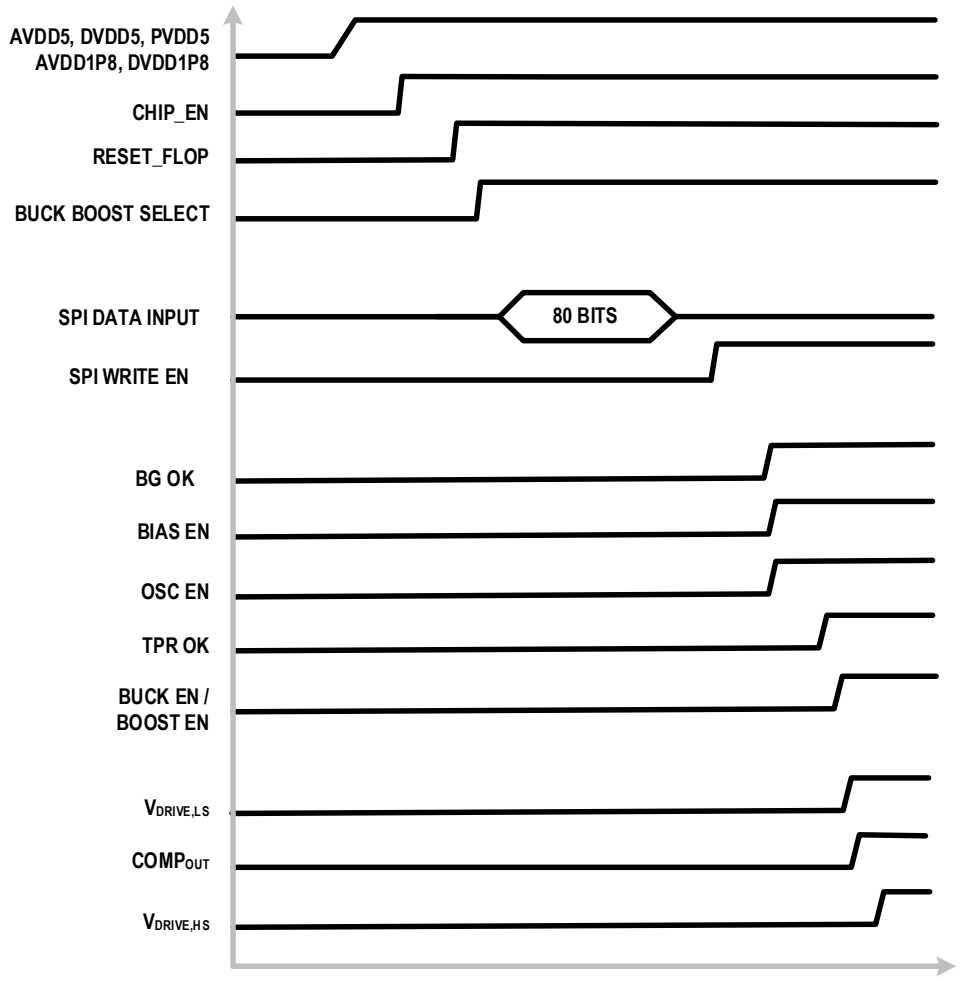


Figure 3.22. Startup sequence in buck and boost mode

Soft start is implemented by using a constant duty cycled clock (20%) charge V_{OUT} in buck mode. In boost mode however, the soft start is implemented by charging V_{OUT} in constant current (CC) mode. This is implemented by comparing V_{SENSE} to a reference voltage using a comparator. The comparator output determines the duty cycle to maintain CC startup operation. In both buck and boost modes, the time-domain control regulation loop takes over as V_{OUT} reaches a predefined reference. This is achieved by comparing V_{FB} to a reference voltage and the output of the comparator V_{OUT_OK} is set high.

In both buck and boost modes, the LS FET is first switched on to ensure that the bootstrap capacitor is properly charged before startup. This ensures V_{SW} is pulled to 0 thereby charging the bootstrap capacitor. This is implemented in the digital logic cores in both buck and boost modes. The detailed startup sequence implemented is shown in Figure 3.22.

3.4.6 Triple Redundant Bandgap Reference

A bandgap reference is incorporated in the design to generate the various voltage references for the system. A conventional bandgap reference topology was selected for its simplicity and robust performance. The bandgap reference implementation is shown in Figure 3.23. As the bandgap voltage is susceptible to SEE of radiation, triple redundancy is added on the output of the bandgap reference. Triple redundancy provides immunity from SEEs of radiation by ensuring spatial and temporal parallelism [56]. Spatial parallelism is achieved by multiple parallel sampling circuits whereas temporal parallelism is achieved by multiple phase shifted clocks. The implementation of triple redundancy is shown in Figure 3.24.

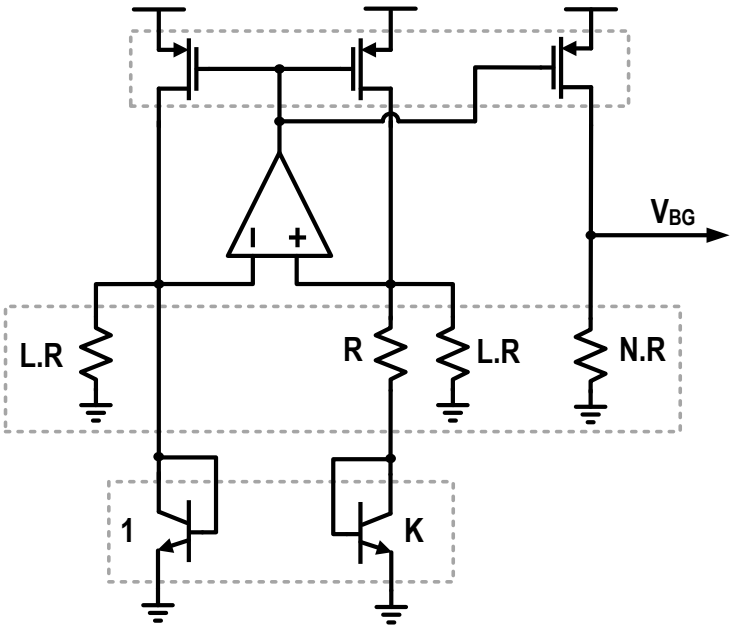


Figure 3.23 Implementation of bandgap reference

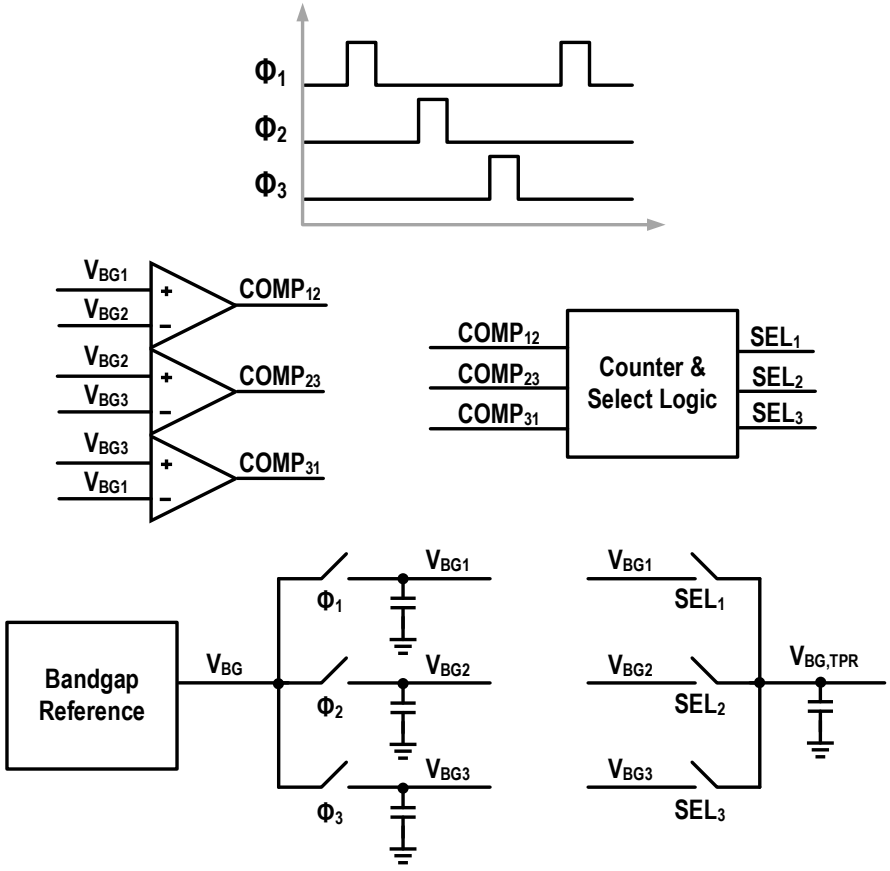


Figure 3.24 Implementation of triple redundancy for bandgap reference voltage

As shown in Figure 3.24, VBG is sampled on 3 sampling capacitors by using 3 phase-shifted clocks Φ_1, Φ_2, and Φ_3. The sampled values are compared in ascending order and the outputs of the comparators $COMP_{12}$, $COMP_{23}$ and $COMP_{31}$ are passed on to a counter and selection logic. If a SEE of radiation occurs, the corrupted V_{BG} is sampled on one of the sampling capacitors. This trips one of the comparators detecting the SEE of radiation. Selection logic then selects the earlier clean sampled V_{BG} value instead of the corrupted sampled V_{BG} value and transfers this clean sampled V_{BG} value on to the output $V_{BG,TPR}$.

A SEE can be modeled as an exponential decaying positive or negative current pulse for a very short interval. This model is used to simulate positive and negative SEE events on various nets of the bandgap reference. As shown in Figure 3.25, simulation results show that the V_{BG} is affected, however $V_{BG,TPR}$ is immune to SEE events. The zoomed-in simulation result in Figure 3.26 shows that V_{BG} drops by ~400mV however, $V_{BG,TPR}$ drops by just 193µV.

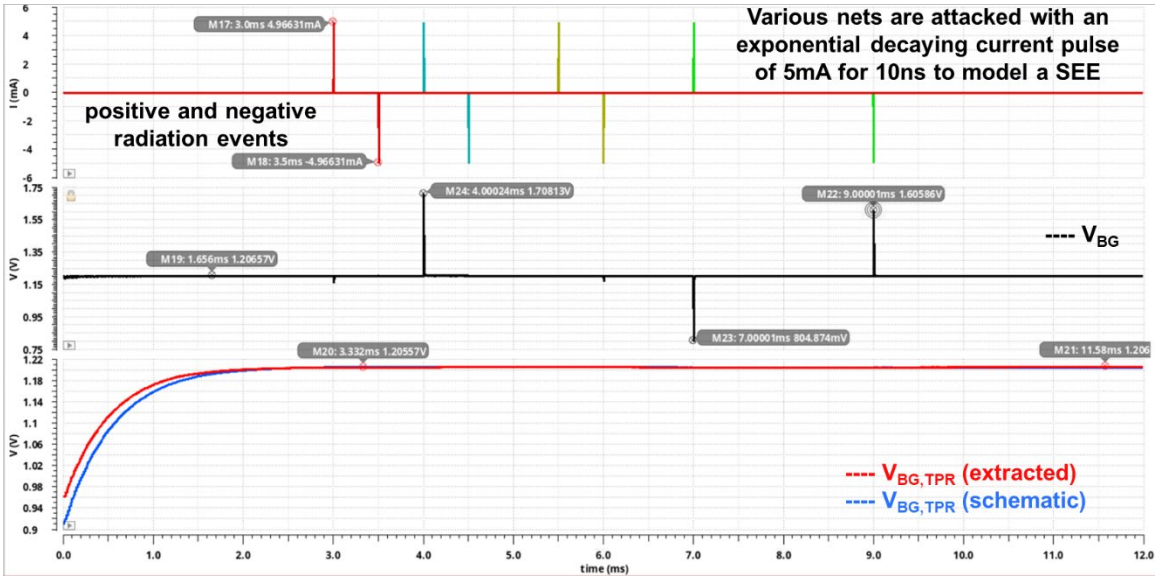


Figure 3.25. Simulation result for triple redundant bandgap reference

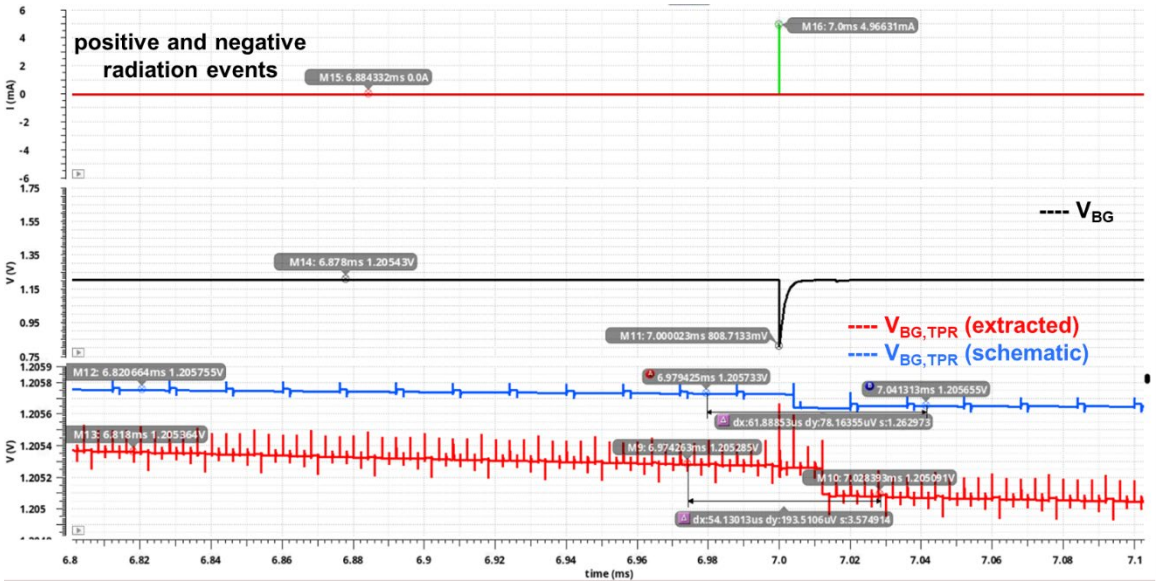


Figure 3.26. Zoomed-in simulation result triple redundant bandgap reference

3.5 Measurement Results

The controller IC is designed and fabricated on a 180nm High-Voltage (HV) Bi-CMOS-Diode (BCD) process. Figure 3.27 shows the die micrograph for the buck=boost controller IC. The total area of the controller IC is 3.38mm² of which buck and boost regulation core each occupy 0.46 mm² for a total area of 0.92 mm². Both the HS and LS drivers along with the level shifter occupy a total area of 0.6755 mm² and the bandgap reference along with triple redundancy occupies an area of 0.36mm². The layout of the driver is optimized to ensure minimum voltage drops during transitions.

The power stage for both buck and boost modes was designed nominally for the values as shown in Table 3.1. An evaluation board was designed for the testing the buck and boost converter individually. The evaluation board for testing the buck converter and boost converter is shown in Figure 3.28 and Figure 3.29 respectively. It consists of the controller IC, the power stage with the NMOS FETs, L, R_{SENSE}, C_{OUT} and C_{IN}. The board also features the I_L emulation components, and feedback resistors. The load transient can

be introduced by either an external electronic DC load or the FET-slammer [15] based method connecting to a high wattage resistor along with option to have an external electronic load. The inductor current is measured using a current probe with a wire loop in series as shown in Figure 3.28 and Figure 3.29. Trimming and programmability is enabled through SPI interface. The SPI data and clock signals are generated using the MCP 2210 module with an USB interface. Figure 3.30 shows the measurement setup.

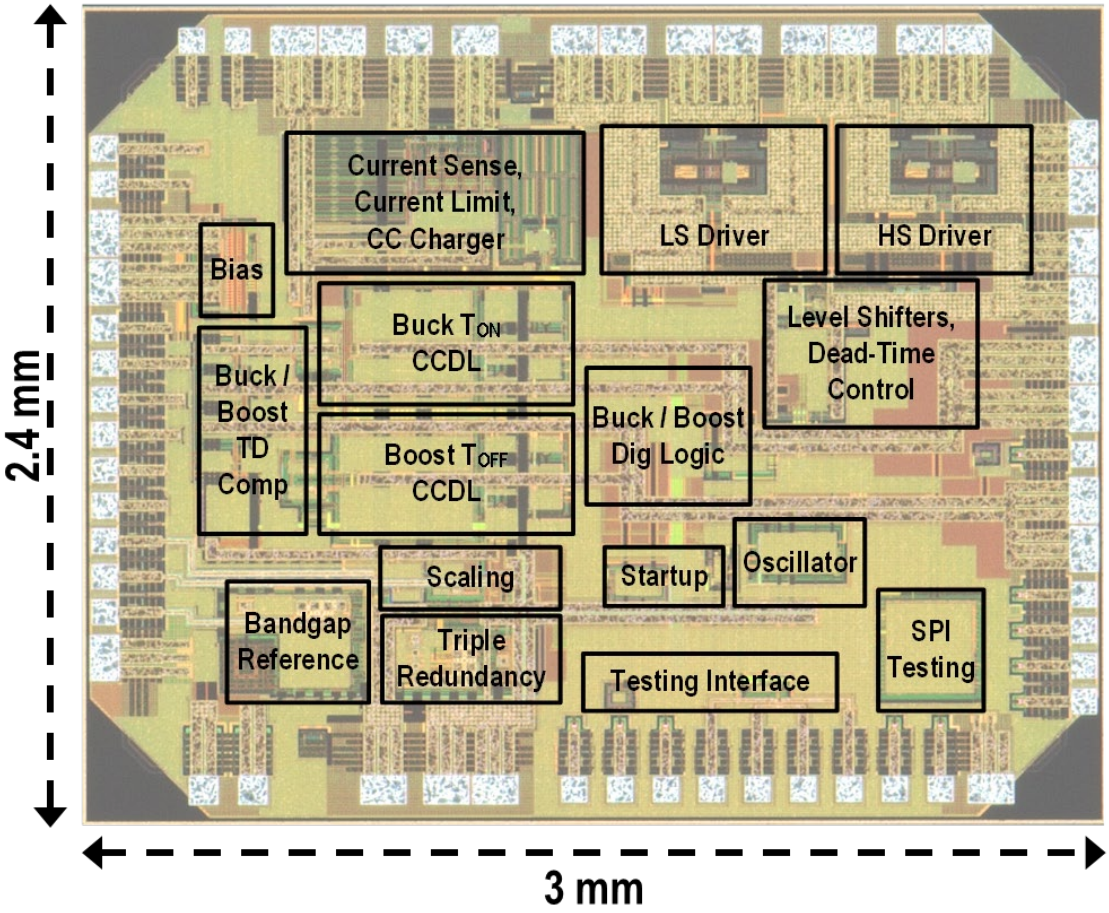


Figure 3.27. Die micrograph of the buck-boost controller IC

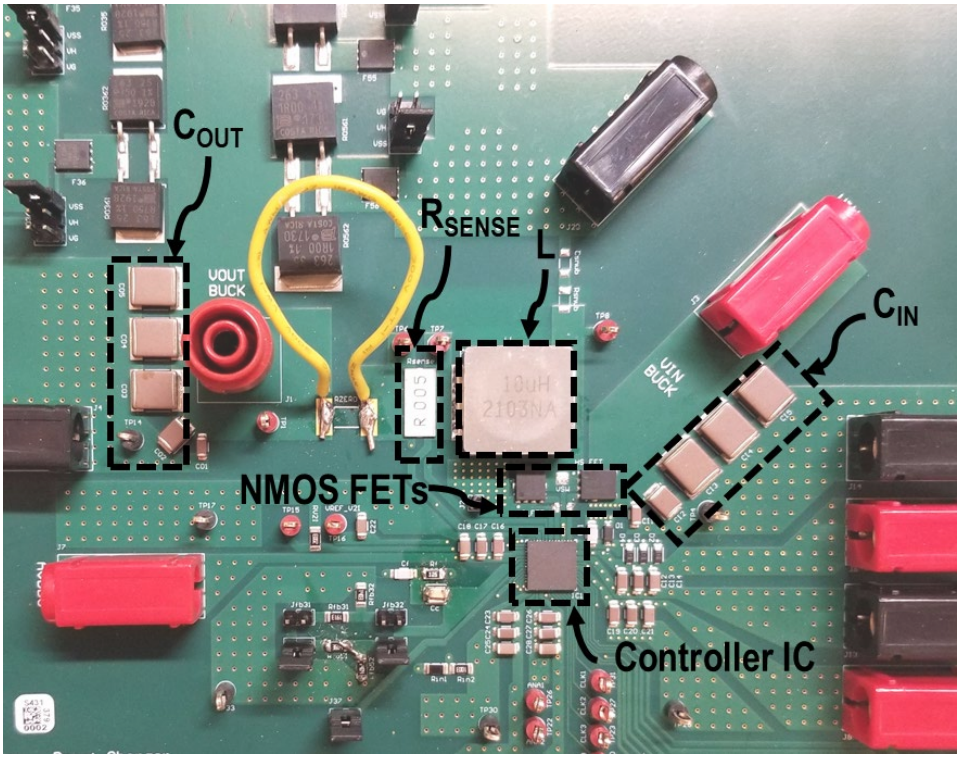


Figure 3.28. Evaluation board for buck converter

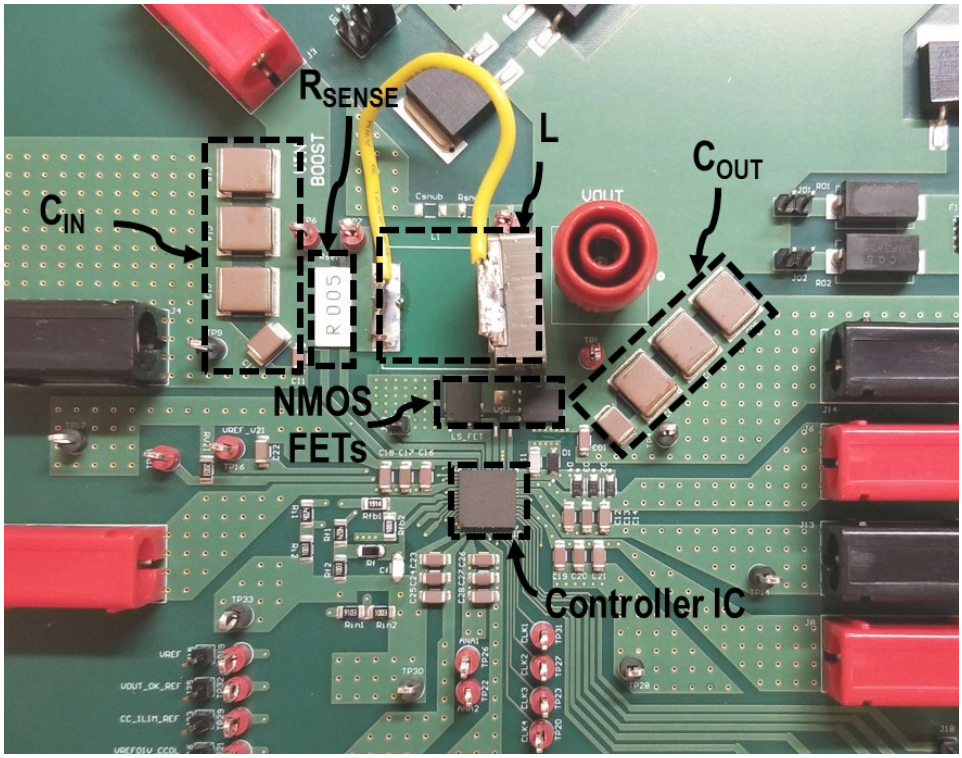


Figure 3.29. Evaluation board for boost converter

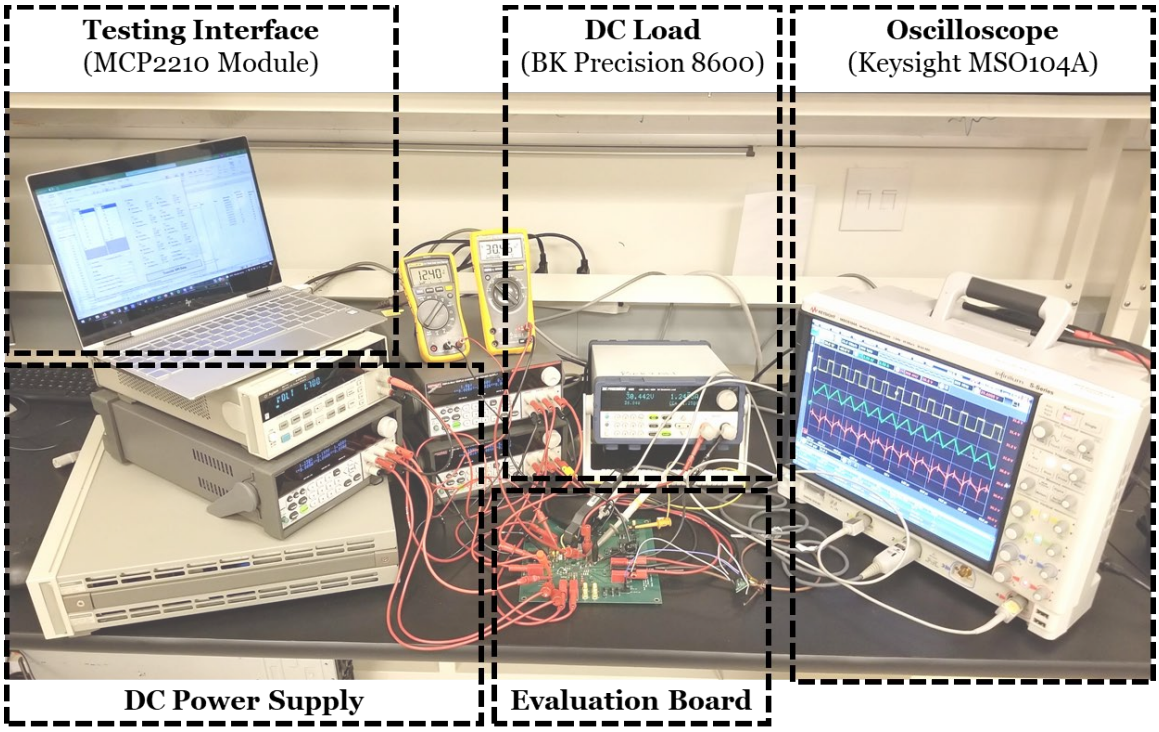
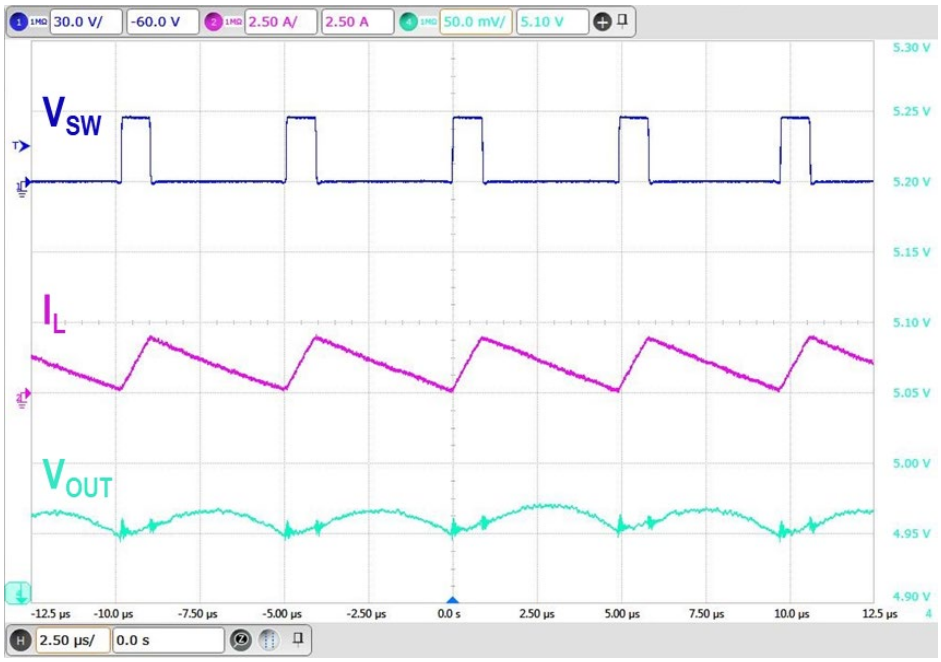


Figure 3.30. Measurement setup for time-domain switching converters

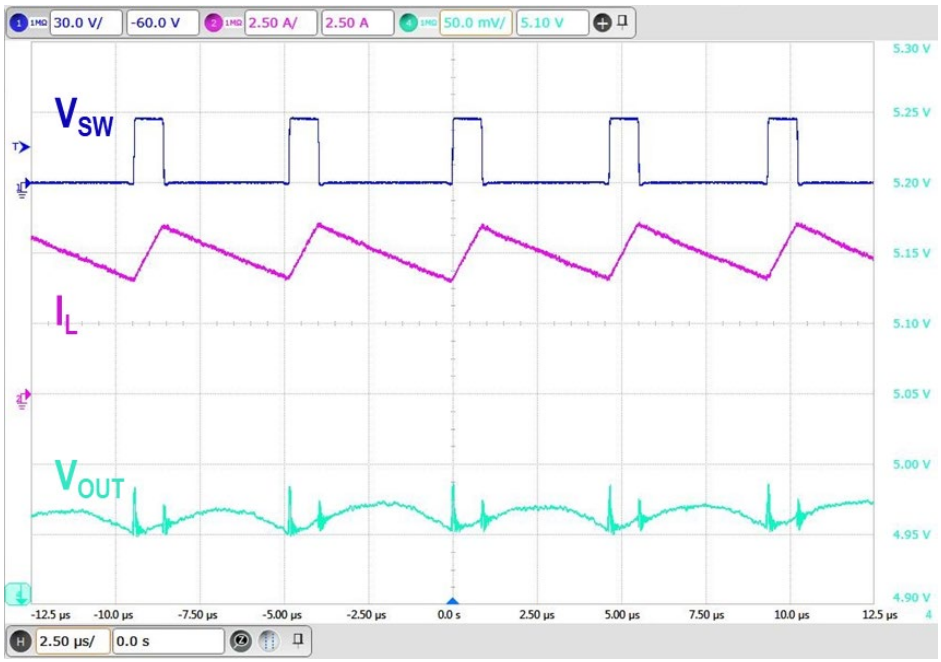
3.5.1 Buck Converter Measurement Results

Figure 3.31 shows the measured switching waveforms of V_{SW}, I_L and V_{OUT} for the buck converter in steady state at I_{OUT} of 1A and 5A for a V_{IN} of 28V and V_{OUT} of 5V. The F_{SW} is almost equal for both the steady state waveforms.

The variation of measured F_{SW} vs I_{OUT} for different V_{IN} is shown in Figure 3.32. Due to the adaptive T_{ON} approach of the controller, FSW remains relatively constant for entire range of I_{OUT}. Similarly, the measured regulated DC value of V_{OUT} vs I_{OUT} for different V_{IN} is also shown in Figure 3.32. The above results validate that the adaptive time-domain based controller achieves stable regulated output for buck conversion.



V_{IN} = 28V, V_{OUT} = 5V, I_{OUT} = 1A, F_{SW} = 196.15kHz



V_{IN} = 28V, V_{OUT} = 5V, I_{OUT} = 5A, F_{SW} = 204.27kHz

Figure 3.31. Steady-state waveforms for the buck converter

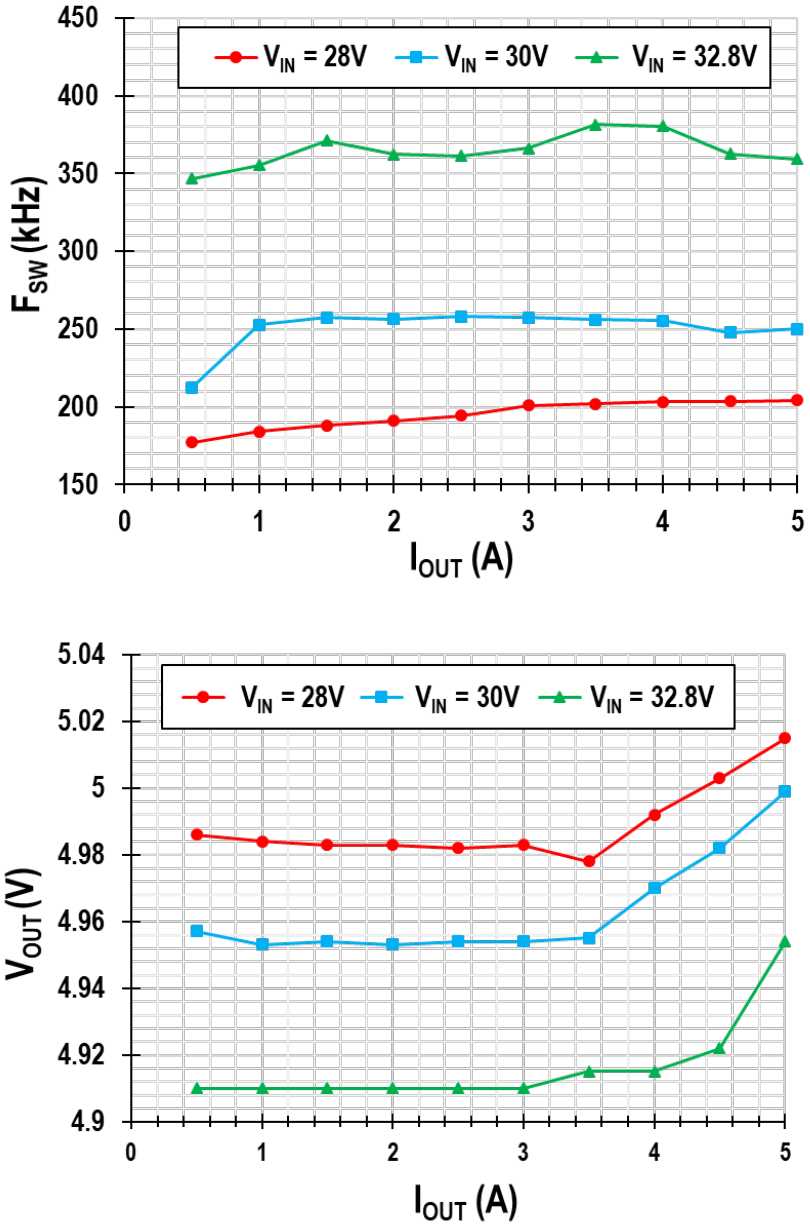
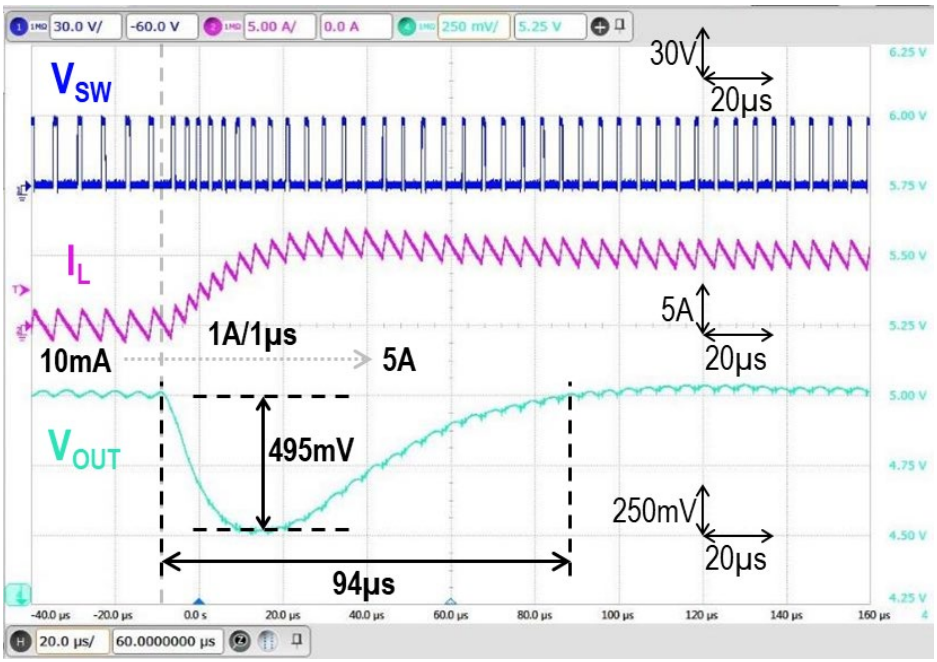
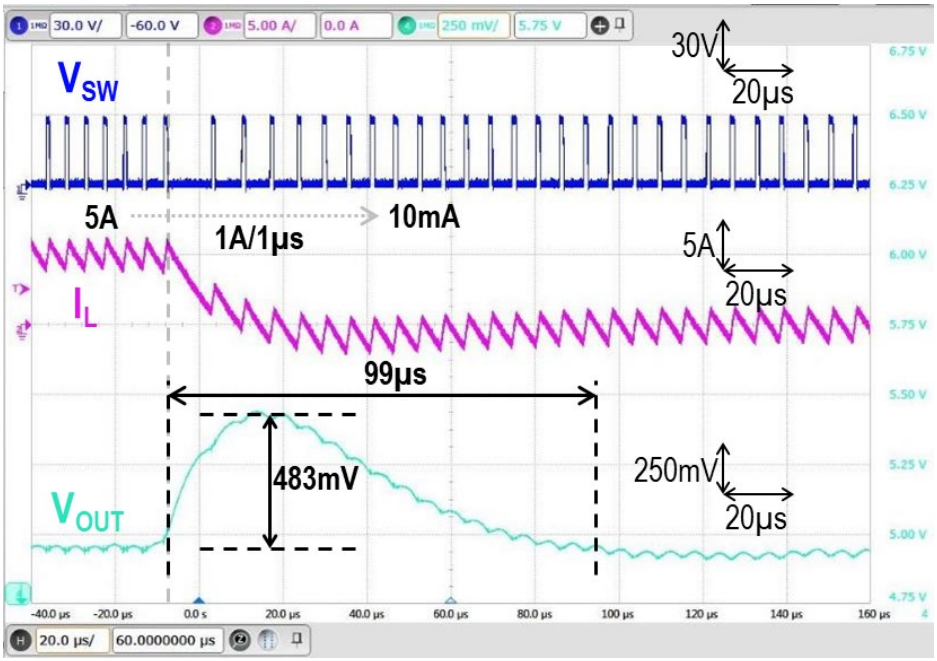


Figure 3.32. F_{SW} and V_{OUT} vs I_{OUT} for different V_{IN} in buck converter

The buck converter's measured load transient waveforms of V_{SW}, I_L and V_{OUT} for an I_{OUT} from 10mA → 5A → 10mA is at a rate of 1A/µs is shown in Figure 3.33. The controller promptly and responds to the change in I_{OUT} due to I_L emulation and feedback without any stability concerns.



V_{IN} = 28V, V_{OUT} = 5V, I_{OUT} = 10mA → 5A



V_{IN} = 28V, V_{OUT} = 5V, I_{OUT} = 5A → 10mA

Figure 3.33. Measured load transient response of buck converter

The efficiency of the entire buck converter along with the controller IC is calculated by measuring the current and voltage from all the power supplies and input and output. The variation of measured efficiency vs I_{OUT} for different V_{IN} is shown in Figure 3.34. The buck converter achieves a peak efficiency of 92.22% at an I_{OUT} of 4A.

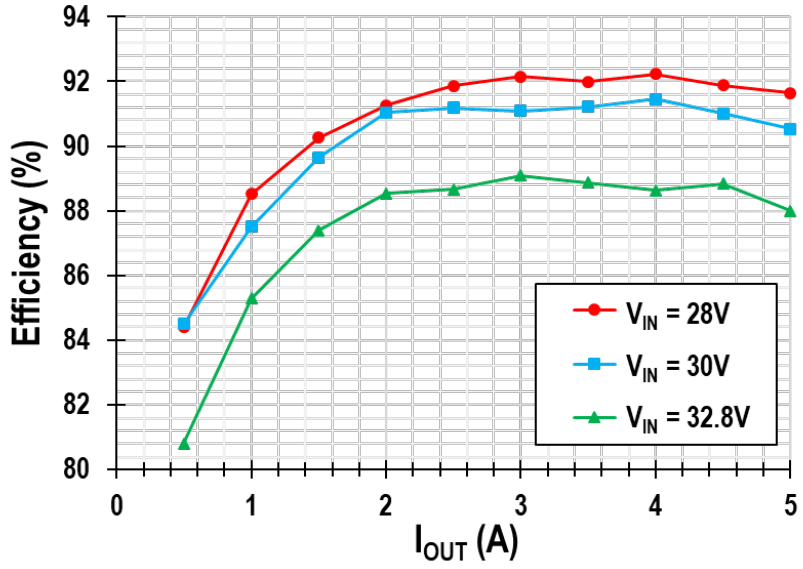


Figure 3.34. Buck converter efficiency

The measured soft-start of the buck converter is shown in Figure 3.35. Soft-start is achieved by starting the buck converter with a constant 20% duty cycled clock. The controller hands over startup control to the regulation loop once $V_{OUT,OK}$ is asserted. As shown in Figure 3.35, the buck converter takes 98µs to startup and achieve voltage regulation for the nominal design specifications.

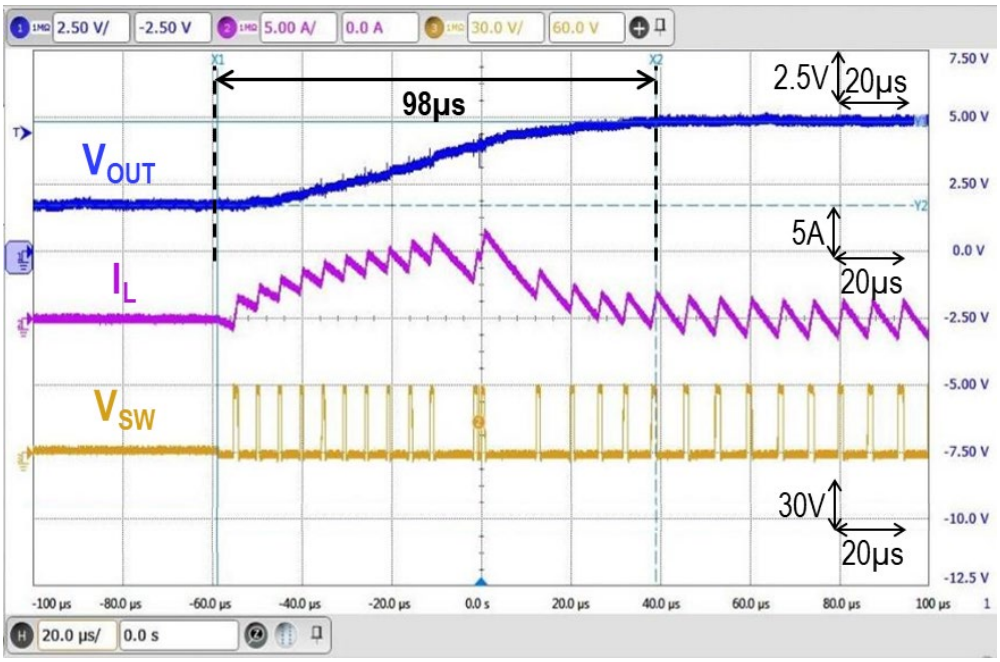
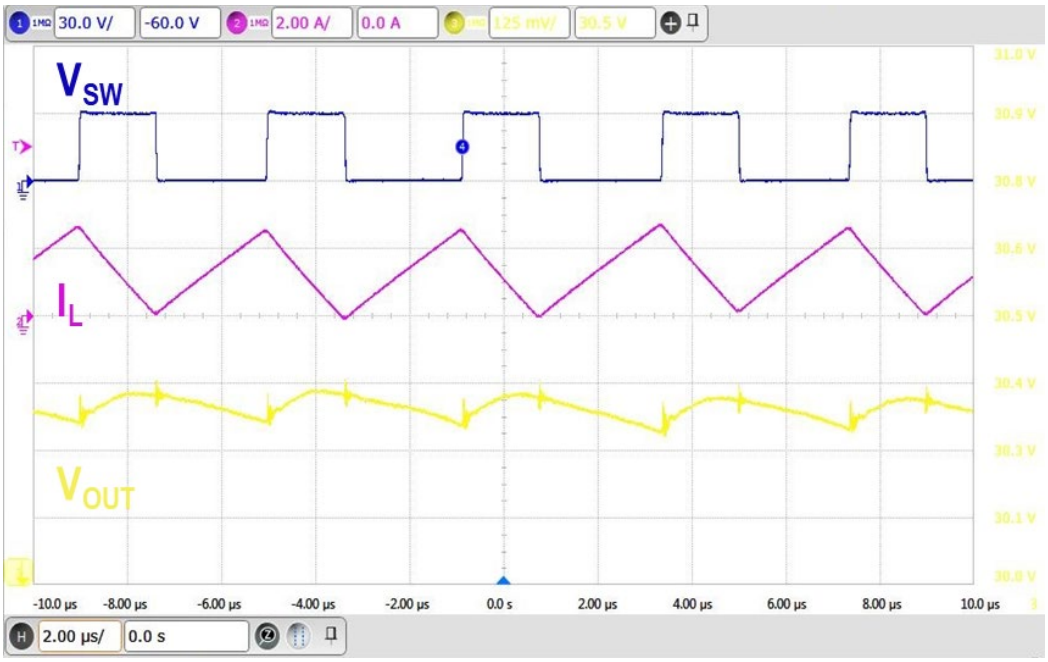


Figure 3.35. Measured startup response of buck converter

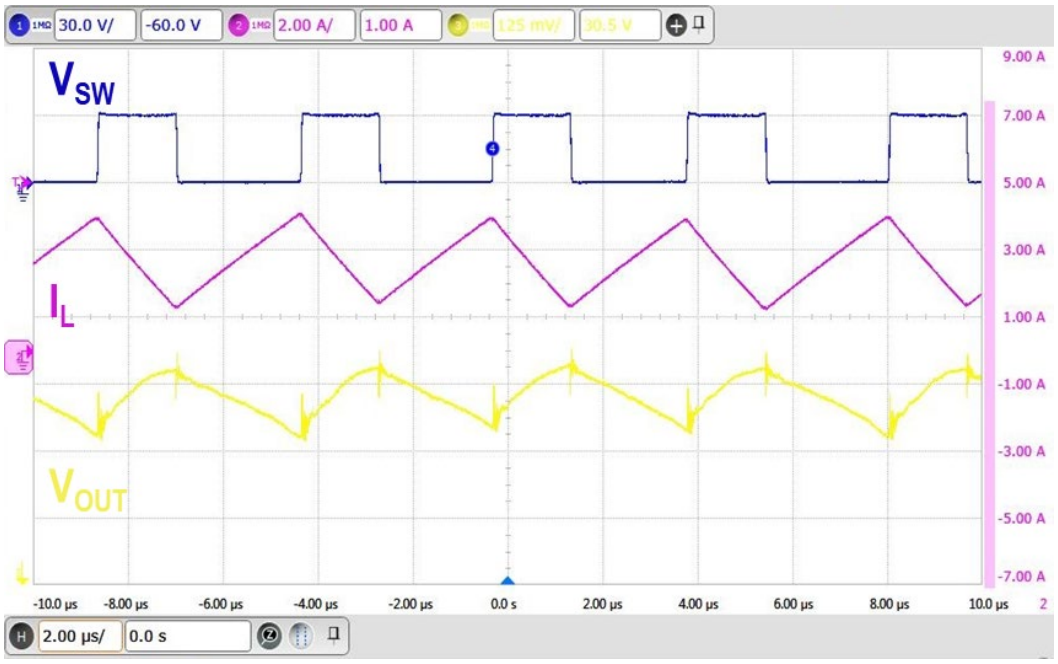
3.5.2 Boost Converter Measurement Results

Figure 3.36 shows the measured switching waveforms of V_{SW}, I_L and V_{OUT} for the buck converter in steady state at I_{OUT} of 500mA and 1.25A for a V_{IN} of 12.5V and V_{OUT} of 30.4V. The F_{SW} is almost equal for both the steady state waveforms.

The variation of measured F_{SW} vs I_{OUT} for different V_{IN} is shown in Figure 3.37. Due to the adaptive T_{ON} approach of the controller, FSW remains relatively constant for entire range of I_{OUT}. Similarly, the measured regulated DC value of V_{OUT} vs I_{OUT} for different V_{IN} is also shown in Figure 3.37. The above results validate that the adaptive time-domain based controller achieves stable regulated output for boost conversion.



V_{IN} = 12.5V, V_{OUT} = 30.4V, I_{OUT} = 500mA, F_{SW} = 252.41kHz



V_{IN} = 12.5V, V_{OUT} = 30.4V, I_{OUT} = 1.25A, F_{SW} = 247.40kHz

Figure 3.36 Steady-state waveforms for the boost converter

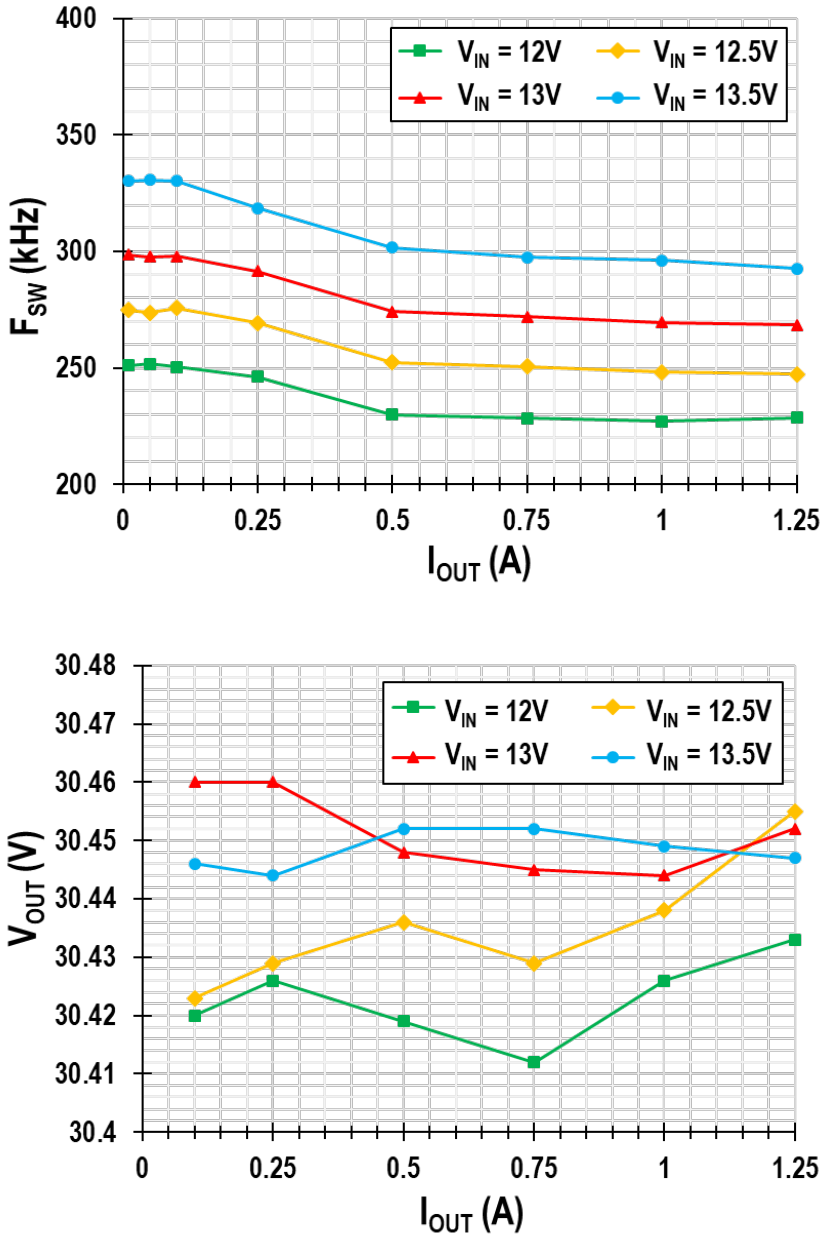
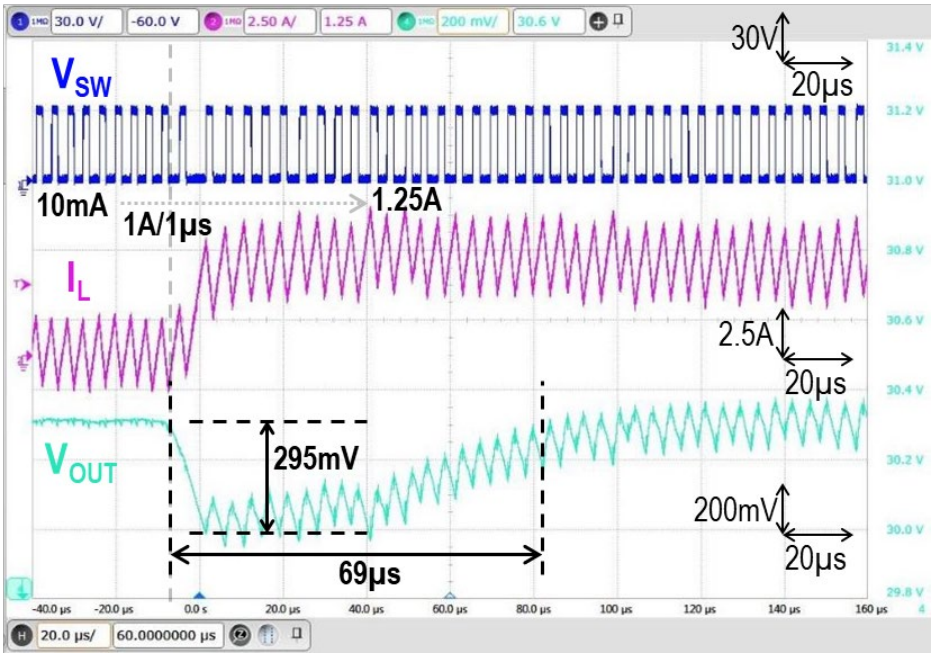
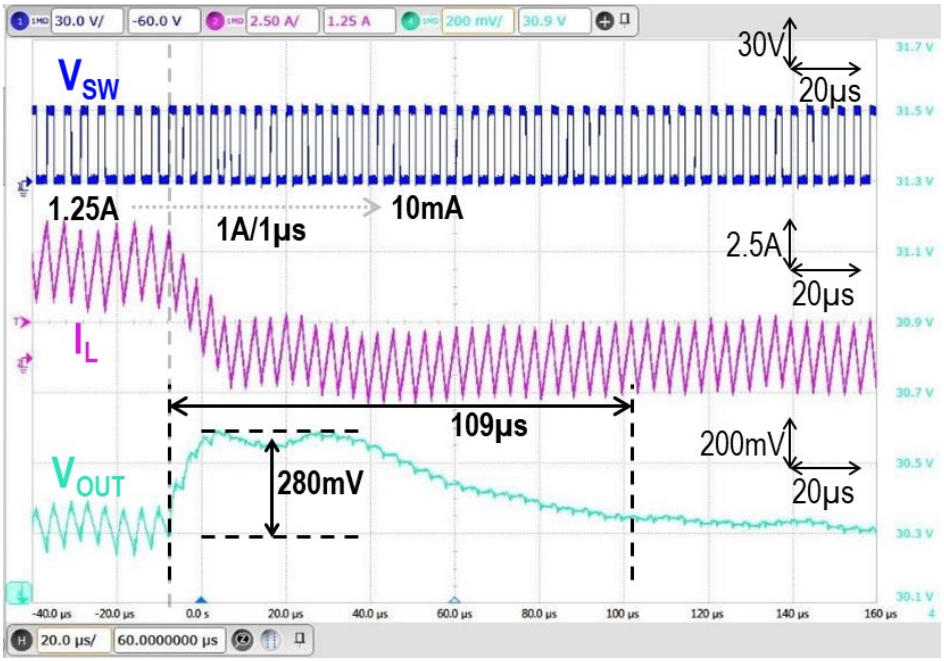


Figure 3.37. F_{SW} and V_{OUT} vs I_{OUT} for different V_{IN} in boost converter

The boost converter's measured load transient waveforms of V_{SW}, I_L and V_{OUT} for an I_{OUT} from 10mA → 1.25A → 10mA is at a rate of 1A/µs is shown in Figure 3.38. The controller promptly and responds to the change in I_{OUT} due to I_L emulation and feedback without any stability concerns.



V_{IN} = 12.5V, V_{OUT} = 30.4V, I_{OUT} = 10mA → 1.25A



V_{IN} = 12.5V, V_{OUT} = 30.4V, I_{OUT} = 1.25A → 10mA

Figure 3.38. Measured load transient response of boost converter

The efficiency of the entire boost converter along with the controller IC is calculated by measuring the current and voltage from all the power supplies and input and output. The variation of measured efficiency vs I_{OUT} for different V_{IN} is shown in Figure 3.39. The boost converter achieves a peak efficiency of 95.97% at an I_{OUT} of 1.25A.

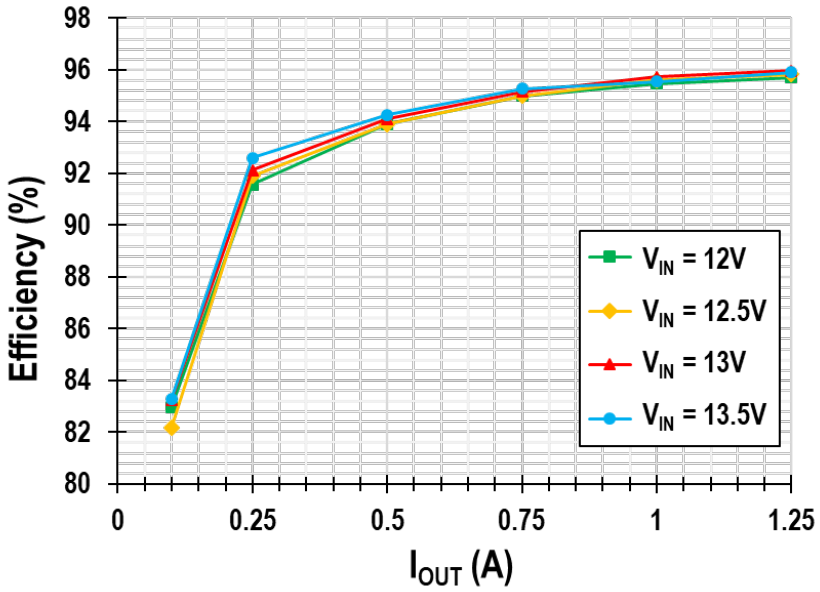


Figure 3.39. Boost converter efficiency

The measured soft-start of the boost converter is shown in Figure 3.40. Soft-start is achieved by starting the boost converter in CC mode. CC mode operation is enabled by a comparator sensing the output of the CSA V_{SENSE}. The boost controller seamlessly hands over startup control from CC loop to the CV regulation loop once $V_{OUT,OK}$ is asserted. As shown in Figure 3.40, the boost converter takes 1.108ms to startup and achieve voltage regulation for the nominal design specifications.

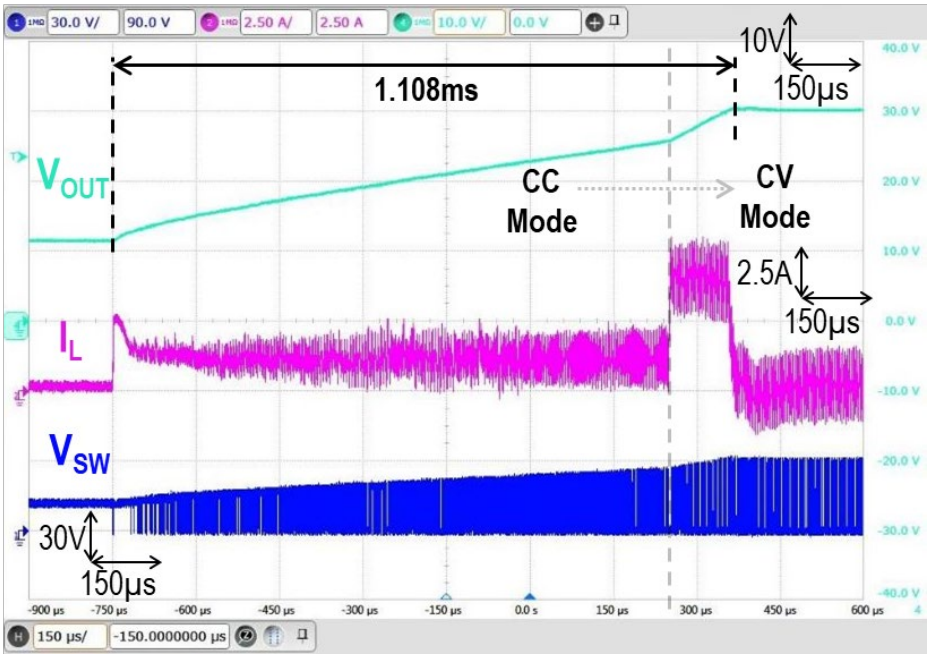


Figure 3.40. Measured startup response of boost converter

3.5.3 Comparison Summary

Table 3.2 showcases the comparison summary of this converter with prior art. The presented current-mode time-domain controller achieves stable voltage regulation for both buck and boost mode operation.

Compared to other prior approaches, the buck and boost converter is designed for higher output power thus requiring the need for external NMOS power FETs. The measured F_{SW} of the converter in buck or boost configurations is quasi-constant due to the adaptive approach for generation of T_{ON} or T_{OFF} respectively. The converter achieves an F_{SW} of 250kHz for the nominal design specifications for both buck and boost modes of operation.

The absolute value for undershoot, overshoot and settling time is higher than the prior art as the load transient step is also considerably higher. The converter also achieves on-par or higher efficiency than the prior art.

	Buck Converter				Boost Converter			
	This Work	D-H Jung, et. al, JSSC 2018 [37]	J-G Kang, et al, ISSCC 2018 [38]	S. Kim, et. al, JSSC 2018 [39]	**This Work**	C Huang, et al, JSSC 2018 [48]	W Qu, et. al, ESSCIRC 2019 [46]	W Hong, et. al JSSC 2021 [47]
Process	**180nm BCD**	350nm CMOS	65nm CMOS	65nm CMOS	**180nm BCD**	180nm CMOS	180nm CMOS	180nm CMOS
Control	**Time-Domain Current-Mode**	Time-Domain Quasi-V^2	Time-Domain Current Mode	T-PID PWM/ PFM	**Time-Domain Current-Mode**	Current-Mode AOT	Current-Mode Hysteretic	Current-Mode AOT
V_{IN} (V)	**28 – 32.8**	3.3	1.8	1.8	**12.3 – 15**	0.8 – 1.4	2.7 – 4.5	1.8 – 3.3
V_{OUT} (V)	**3.3 – 5**	1.5 – 1.8	0.15 – 1.69	0.5 – 1.5	**28 – 32.8**	1.8	5	3.0 – 4.5
$I_{OUT, max}$ (mA)	**5000**	25 – 700	600	1000	**1250**	400	400	700
L(µH) / C_{OUT}(µF)	**10 / 68**	2.2 / 4.7	0.22 / 4.7	0.22 / 4.7	**10 / 68**	1 / 6.8	- / -	0.3 / 6.6
F_{SW}	**~250 kHz**	2 MHz	10 MHz	10 MHz	**~250 kHz**	800 kHz	600 kHz	10 MHz
Settling Time (µs)	**94 / 99 (10mA - 5A)**	2.5 / 2.6 (0.17A - 0.68A)	3.5 / 3.5 (0.1A - 0.58A)	1.8 / 3* (20mA - 0.42A)	**69 / 109 (10mA - 1.25A)**	14 / 46 (10mA - 0.4A)	124 / 104 (0 - 0.3A)	4 / 27 (10mA - 0.5A)
Undershoot / Overshoot (mV)	**495 / 483 (10mA - 5A)**	38 / 20 (0.17A - 0.68A)	100* / 100* (0.1A - 0.58A)	40 / 40 (20mA - 0.42A)	**295 / 280 (10mA - 1.25A)**	126 / 150 (10mA - 0.4A)	42 / 38 (0 - 0.3A)	125 / 135 (10mA - 0.5A)
Efficiency (%)	**92.22**	92	94.9	90	**95.97**	92.4	95.3	94.5

* Estimated from results

Table 3.2. Performance comparison with prior art

3.6 Conclusion

Time-domain control can afford advantages of both analog and digital controllers. An externally configurable controller IC is designed for both buck and boost operation using basic time-domain control elements.

The boost converter is designed to operate both in CC and CV modes whereas the buck converter is designed to operate in CV mode. The controller incorporates I_L emulation to implement current-mode control both in buck and boost modes. This enables the system to achieve fast load transient response for large steps. A time-domain comparator is used to determine the peak of I_L in boost mode and the valley of I_L in buck mode. T_{ON}/T_{OFF} is generated using time-domain processing and is made adaptive to changes in V_{IN} for better line response. This also results in quasi-constant F_{SW} for the entire range of I_{OUT}.

With an external NMOS FET based power stage, bootstrapping is added to drive the HS FET. The driver is designed with deadtime control to avoid shoot-through current and gradual rise/fall time to avoid sharp current spikes. Current sensing is implemented by using R_{SENSE} in series with the inductor. The output of CSA is used to detect current limit and implement CC mode of the boost converter. Soft-start is also incorporated in the controller to ensure the converter starts gracefully without affecting reliability. In addition to a time-domain based controller core, a triple redundant bandgap further makes this controller architecture an attractive option for high-reliability space applications potentially.

The controller IC designed on a 180nm BCD process is validated with silicon measurement results as shown in the earlier section. The peak efficiency of the buck converter is 92.22% whereas the boost converter achieves a peak efficiency of 95.97%.

CHAPTER 4

CONCLUSION AND FUTURE WORK

The reliability and robustness of power-management integrated circuits (PMICs) continues to be a major hurdle in increasing performance and functionality of portable electronic systems. Most applications where reliability is a key parameter are applications with high output currents at low voltages or their usage in unique settings. This dissertation presents solutions to two such reliability problems – thermal management of a parallel system of low-dropout linear regulators and performance of buck / boost time-domain switching regulators in radiation environments. A brief overview of each of these solutions is described below.

4.1 Load-Sharing Low-Dropout Linear Regulators

A daisy-chain solution to parallelize multiple LDO ICs to increase the total output current without sacrificing on performance, functionality and thermal reliability of the system is presented. An auxiliary current servo loop operating in tandem with the core voltage regulation loop enables current sharing between the multiple parallel LDO ICs. A double-differential error amplifier combines both the voltage regulation error and the current sharing error thereby achieving parallel operation with a single set of feedback resistors. The presented PCB-friendly, low-cost approach achieves current sharing without the need for any off-chip active or passive component or matched PCB traces thus reducing the overall system cost. Fully integrated current sensing based on dynamic element matching eliminates the need for any off-chip current sensing.

Silicon measurement results validate the high-accuracy parallel LDO operation with a measured current sharing accuracy of 2.613% and 2.789% for an output voltage of

3V and 1V respectively. The measurement results for both 2 and 4 parallel LDO IC combinations also showcase the scalable nature of the parallel system as per the end-user requirements. Thermal images as well showcase that the system achieves thermal equilibrium thereby ensuring stable reliable operation. The dependence of current sharing accuracy with output current and dropout voltage is also characterized. The comparison summary with prior art shows that this approach to parallelize LDO ICs at par current sharing accuracy with a higher current density and lower system size.

Future Work:

1) Performance of parallel LDOs at ultra-light loads
2) BJTs instead of MOS in current mirrors
3) Current-input, current output servo integrator topology
4) I_{LIM} implementation
5) R_{meas} at V_{IN} instead of V_{OUT}

4.2 Time-Domain Switching Regulators

A time-domain based buck and boost controller IC with time as the processing variable and combining the benefits of both analog and digital controllers is presented. The controller is designed to operate in either constant-current and constant-voltage mode as a boost converter and purely constant-voltage mode as a buck converter. Current-mode feedback for fast transient response is implemented by passive inductor current emulation path in both buck and boost modes. A time-domain comparator supports valley current-mode control in buck and peak current-mode control in boost. A quasi-constant switching frequency across the range of output current is realized by generating on-time/off-time adaptively to changes in the input voltage for better line response. Current

sensing is also implemented to detect current limit and realize constant-current startup in boost mode. Using time-domain control for regulation and triple redundancy on the bandgap output voltage can thus make this controller architecture immune to single-event effects of radiation.

Silicon measurement results of the time-domain controller with an external power stage for buck and boost modes validate the controller architecture. Stable output voltage regulation is measured with a quasi-constant switching frequency. As compared to prior art, both the buck and boost converters achieve on-par or higher efficiency than the prior art. The peak efficiency of the buck converter is 92.22% at 5A of output current whereas the boost converter achieves a peak efficiency of 95.97% at 1.25A of output current.

Future Work:

1) Time-domain comparators for I_{LIM}, DCM, $V_{OUT, OK}$
2) Adapt hard-coded value of T_{ON}/T_{OFF} as per V_{OUT}
3) Triple redundancy on all analog sensed voltages (V_{FB}, V_F, V_I)
4) Scaling amplifier before triple redundancy
5) Implementation of DCM for better efficiency at light loads

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