Development of Diamond Devices for High Power, RF and Harsh Environments

by

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ABSTRACT

Diamond as a wide-bandgap (WBG) semiconductor material has distinct advantages for power electronics applications over Si and other WBG materials due to its high critical electric field (> 10 MV/cm), high electron and hole mobility (μ_n=4500 cm^2/V-s, μ_p=3800 cm^2/V-s), high thermal conductivity (~22 W/cm-K) and large bandgap (5.47 eV). Owing to its remarkable properties, the application space of WBG materials has widened into areas requiring very high current, operating voltage and temperature. Remarkable progress has been made in demonstrating high breakdown voltage (>10 kV), ultra-high current density (> 100 kA/cm^2) and ultra-high temperature (~1000^{o}C) diamond devices, giving further evidence of diamond's huge potential. However, despite the great success, fabricated diamond devices have not yet delivered diamond's true potential. Some of the main reasons are high dopant activation energies, substantial bulk defect and trap densities, high contact resistance, and high leakage currents. A lack of complete understanding of the diamond specific device physics also impedes the progress in correct design approaches. The main three research focuses of this work are high power, high frequency and high temperature. Through the design, fabrication, testing, analysis and modeling of diamond *p-i-n* and Schottky diodes a milestone in diamond research is achieved and gain important theoretical understanding. In particular, a record highest current density in diamond diodes of ~116 kA/cm^2 is demonstrated, RF characterization of diamond diodes is performed from 0.1 GHz to 25 GHz and diamond diodes are successfully tested in extreme environments of 500^{o}C and ~93 bar of CO_2 pressure. Theoretical models are constructed analytically and in

Silvaco ATLAS including incomplete ionization and hopping mobility to explain space charge limited current phenomenon, effects of traps and Mott-Gurney dominated diode R_{ON}. A new interpretation of the Baliga figure of merit for WBG materials is also formulated and a new cubic relationship between R_{ON} and breakdown voltage is established. Through Silvaco ATLAS modeling, predictions on the power limitation of diamond diodes in receiver-protector circuits is made and a range of self-heating effects is established. Poole-Frenkel emission and hopping conduction models are also utilized to analyze high temperature (500^{o}C) leakage behavior of diamond diodes. Finally, diamond JFET simulations are performed and designs are proposed for high temperature – extreme environment applications.

DEDICATION

To all those who seek the light

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CHAPTER 1

INTRODUCTION AND MOTIVATION

1.1 Motivation

Electricity consumption is predicted to increase more than 50% worldwide and 40% in the U.S. in the next 25 years [1.1] - [1.3]. By 2030, approximately 80% of electricity consumed is predicted to be transferred through some form of power electronics [1.2]. The European Commission proposed to reduce the greenhouse gas emission to at least 55% compared to levels in 1990 by 2030 [1.4]. To cope with the ever-increasing consumption and conversion of electricity by power electronics and to combat climate change at the same time, one of the ways predicted is to improve power conversion efficiency of power converters by 32.5% [1.4]. If the energy conversion efficiency is increased even by 5%, the burden on renewable energy sources reduces by 7.5% [1.5]. Based on the emerging applications of power converters such flexible AC transmission systems (FACTS), battery energy storage systems (BESS), EV charging systems etc. some of the key requirements for power converters identified by Ballestín-Fuertes *et. al*. [1.5] are:

- Breakdown voltage >1200 V
- Compact designs to reduce or remove completely the cooling systems
- Higher switching frequencies (>10^5 Hz) to reduce the size of passive components
- Power devices should be able to sustain high working temperatures (>125^{o}C) and have high thermal conductivities
- Reduced conduction and switching losses to improve efficiency

- Manufacturable in high volume to bring down cost and increased reliability

Si-based power converters have started to reach their theoretical limits in terms of on-state efficiencies and face several important limitations [1.3] as follows:

- high on-state losses when large critical thicknesses are required to accommodate Si's low critical field (0.3 MV/cm)
- relatively long minority carrier lifetime in Si IGBTs and high losses in large area power MOSFETs at high switching speeds causes limitations on the maximum operating frequency
- relatively low bandgap of Si causes high leakage current levels at high temperatures reducing the gain in power devices such as IGBTs

Electric power conversion through power converters can be either continuous or pulsed. In continuous power conversion, electricity is either switched, routed or converted in stationary applications such as transformers on the electrical grid, motor drivers in electric vehicles, DC-AC converters on aircrafts or spacecrafts, solar photovoltaic installations etc. In such applications, reduction in size and weight and increase in power density are the key driving components for technology. On the other hand, in pulsed power applications, a large amount of energy is delivered in a very short period of time, thus outputting a huge peak power in the duration of the pulse. Some pulse power applications involve electromagnetic railguns, high power pulsed lasers, pulsed microwave sources etc. for which some of the key requirements from the semiconductor materials are high peak power, high repetition rate and low form factor.

Wide bandgap (WBG) semiconductor materials such as silicon carbide (SiC), gallium nitride (GaN), gallium oxide (Ga_2O_3), aluminium nitride (AlN), boron nitride (BN) and diamond have emerged over the past few decades and show promising properties that meet all the afore mentioned power converter requirements. For example, their high electric field breakdown enables greater blocking voltage capabilities, thinner layers and deeper doping concentrations, resulting in lower on-state resistance and lower conduction losses. Accordingly, smaller area WBGs will be required for the same on-resistance and therefore providing smaller capacitance. Smaller capacitance and high saturation velocities allow for high switching speeds and low switching losses. Additionally, high bandgap implies ultra-low intrinsic carrier concentration resulting in very low leakage currents and thereby robust high-temperature performance. Fig. 1.1 shows how the WBG material properties translate ultimately to benefits through improved efficiencies, decreased power losses through heat, reduced form factor and cost [1.5].

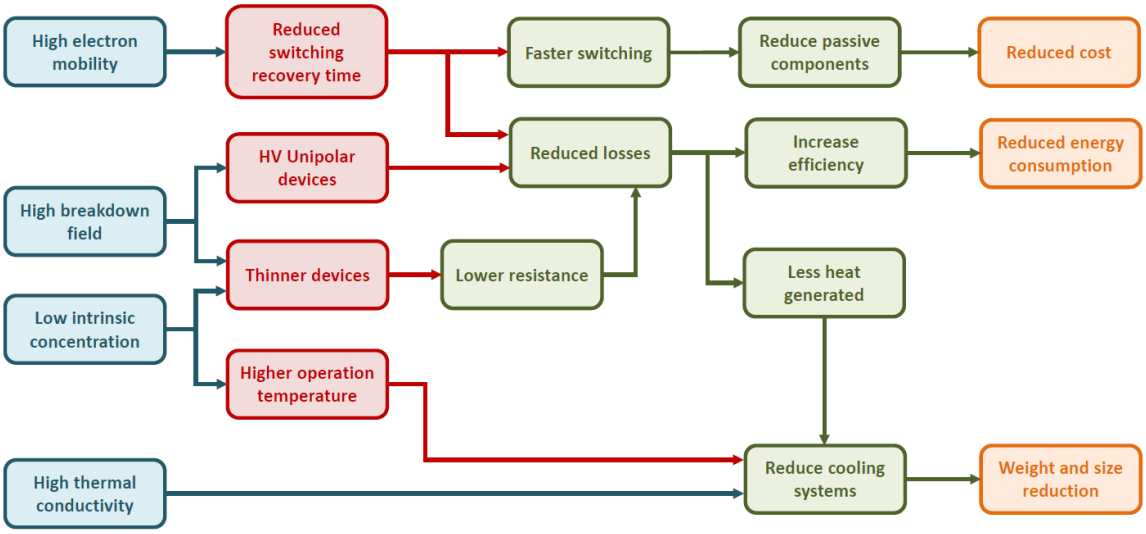

Fig. 1.1 Flowchart indicating how WBG properties translate to advantages in power converters and provide ultimate benefits [1.5]

Owing to the excellent power handling and switching properties, the anticipated application range of WBGs is wide. Fig. 1.4 shows the use of different WBG power devices in various high-power applications [1.9]. Due to its high breakdown field, large thermal conductivity and high carrier mobility, diamond can be anticipated to push the current application space towards higher power and higher frequency as shown.

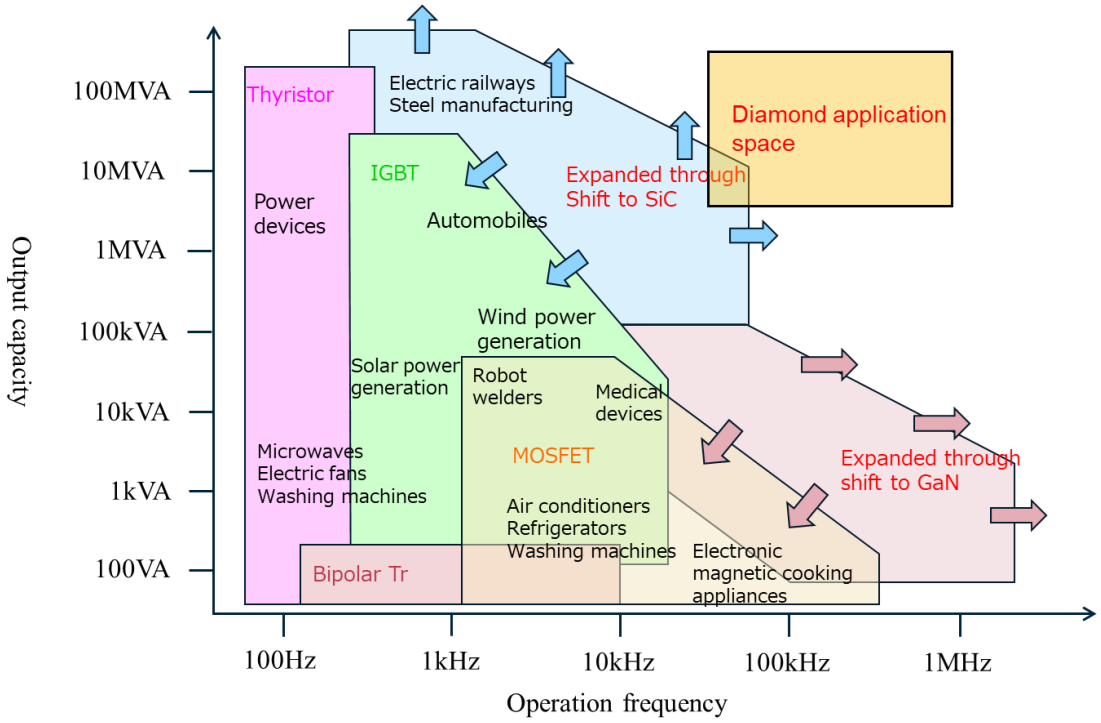

Fig. 1.2 Application space of WBG materials corresponding to their properties [1.9]. Due to its high critical breakdown field and mobility, diamond can be thought to push the boundaries of the application space

1.2 Diamond as a WBG Semiconductor

Diamond outperforms all other WBG materials in terms of its physical properties. In comparison to other WBG materials (Fig. 1.4), diamond has a high critical electric field of ~10 MV/cm [1.6], high carrier mobilities of μ_n=4500 cm^2/V-s, μ_p=3800 cm^2/V-s [1.7], high saturated drift velocities (v_{nsat}=2.5x10^7 cm/s, v_{psat}=1.4x10^7 cm/s) and high thermal conductivity (22 – 24 W/cm-K) [1.8]. Owing to the high carrier saturation velocities and mobilities, diamond-based devices can be expected to considerably reduce switching and conduction losses for high power and high temperature applications (Fig. 1.2). Owing to the large thermal conductivity and critical breakdown electric field, diamond is perfectly

suited for applications such as high-power generators, industrial motors, trunk lines etc. [1.10], as shown in Fig. 1.3.

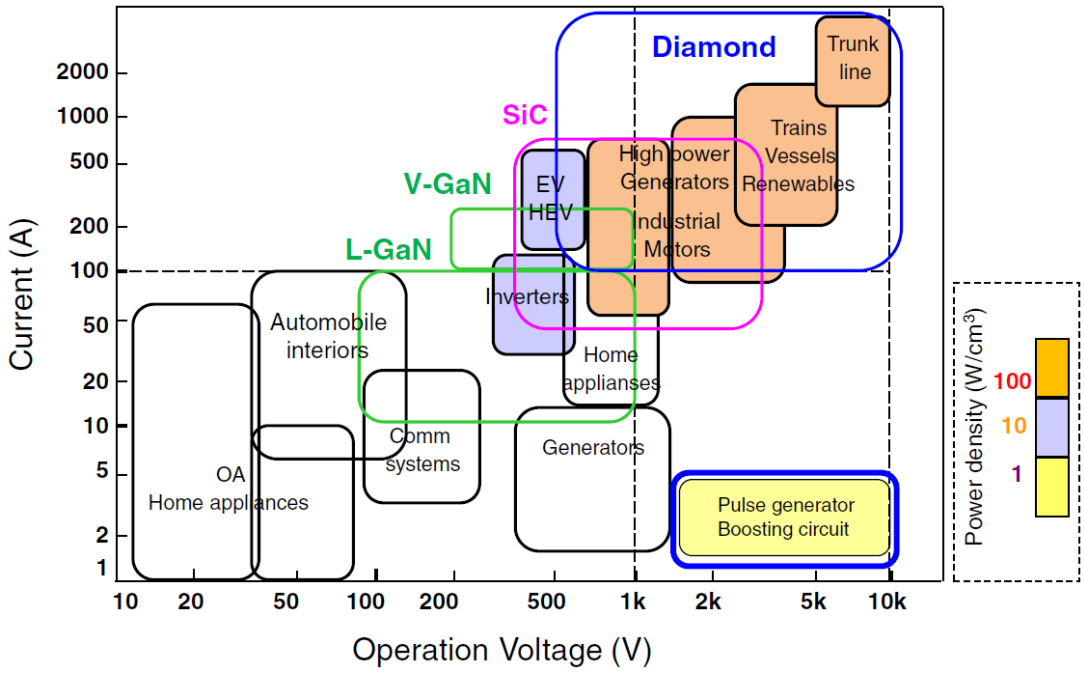

Fig. 1.3 Application space of diamond and other WBG materials in high current – high voltage areas

Lab-grown diamond synthesis was first documented by William G. Eversole of Union Carbide [1.11] and the microwave plasma CVD (MPCVD) and plasma enhanced CVD (PECVD) techniques were developed to produce diamond single crystals since the 2000s with pioneering efforts by Yan et al. [1.12]. Substitutional doping by incorporation of B dopants during the diamond CVD growth was developed in 1994 [1.13] and since then substantial progress in incorporating substitutional dopants like P, N, O, Cu etc. have seen varying success [1.14], [1.15]. Out of all the substitutional dopants, B and P have been the most successful in obtaining *p*- and *n*-type doped diamond.

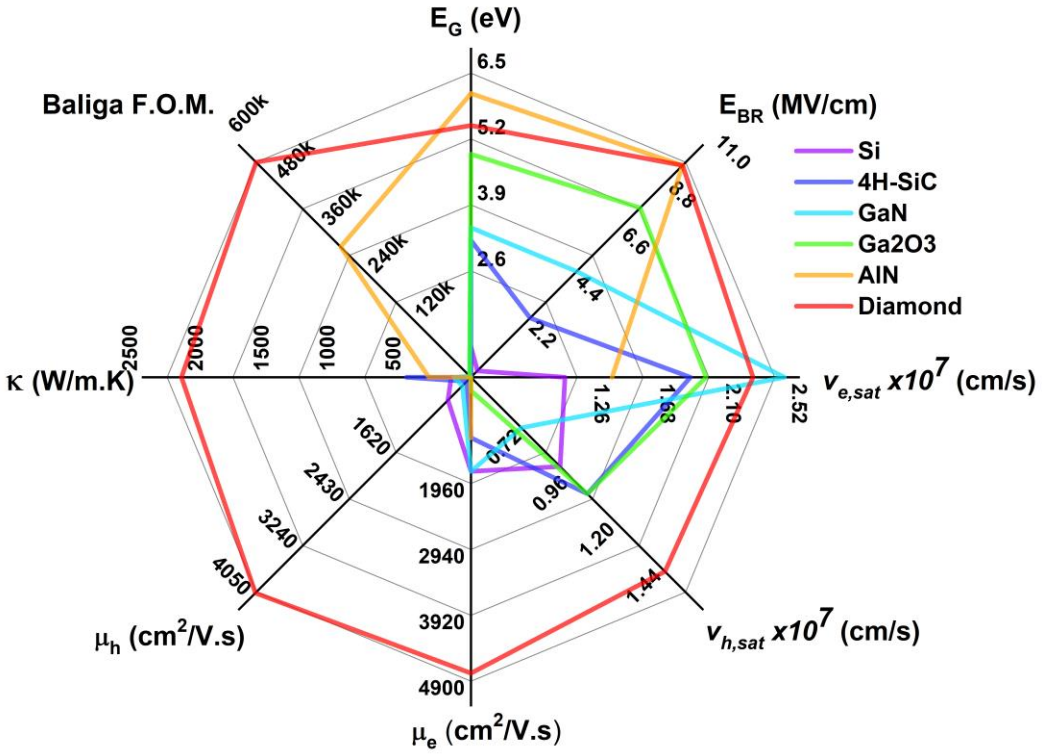

Fig. 1.4 Material and electrical properties of diamond as a semiconductor in comparison to other ultra-wide bandgap materials

Over the past two decades, there has been a substantial increase in diamond power device research with various successes such as diamond Schottky barrier diodes with a breakdown voltage of 12.4 kV [1.16], diamond bipolar junction transistor with breakdown voltage of 1 kV [1.17] and a diamond MOSFET with 4 MV/cm breakdown field [1.18]. However, despite the promising progress in diamond device performance due to homoepitaxial growth and doping techniques, the CVD growth and diamond processing techniques are still in the nascent stages of research. Improved diamond growth quality with lower defect densities, threading dislocations etc. and new growth and doping techniques such as selective area growth and ion implantation are needed to compete with

existing SiC and GaN power devices. Considerable improvements in diamond fabrication and processing in terms of defect free etching, edge-terminated devices, contacts etc. also need to be made. Moreover, deeper understanding of diamond device physics in the areas of interface and defect structures, charge transport under space charge limited conditions, impact ionization and avalanche breakdown, phonon coupling for improving thermal conductivity etc. is equally important to make advancements in diamond power applications.

In this research, the high-power handling capacity, high breakdown field, large thermal conductivity, low switching losses at high frequencies and high temperature properties of diamond as a semiconductor have been exploited and studied to develop diamond devices through various projects such as the NASA High Operating Temperature Technology (HOTTech) program, RF project and the Ultra Materials for a Resilient, Smart Electricity Grid Energy Frontier Research Center (Ultra EFRC). The main three application areas of diamond explored in this research are high power, high frequency and extreme environment through Chapters 3, 4 and 5, respectively. The following sub-sections provide a brief summary of the motivations, challenges and progress in each of the three application areas explored in this research.

1.2.1 Diamond Devices for High Power Applications

As discussed in Section 1.1, high efficiency power converters with low losses are necessary and can be made possible with WBG materials. Huge strides have been made in SiC and GaN power devices over the past few decades and are now available commercially

while diamond power devices are still in early research phase. However, just in the past two decades, several milestones in diamond diodes have been achieved in terms of maximum current, current density, blocking voltage and critical breakdown field. Table 1.1 shows some of the outstanding progress made in diamond diodes up till now.

Some of the objectives of the Ultra EFRC program were to demonstrate a 100+ kA/cm^2 and 10 kV power devices. In order to achieve this goal, along with improving diamond device fabrication techniques, a deeper understanding of the space charge limited (SCL) current phenomenon is required. The SCL conduction also affects the diode on-state resistance R_{ON} and therefore the R_{ON} vs. breakdown voltage (BV) relation also changes. Therefore, a new interpretation of the Baliga figure-of-merit, that links the on-state and off-state performance, is required for WBG materials and especially diamond. Moreover, defect levels also severely limit the current carrying capacity and need to be studied in depth. High current carrying capacity inherently requires understanding of the heat generation and dissipation in the power device. Although diamond theoretically has very high thermal conductivity, practically the value might be a lot smaller due to varying growth quality. Therefore, in order to better estimate the feasibility of diamond power devices, self-heating models need to account for the poor thermal properties as well.

Ref.	**Current (A)**	**Diode Type**
[1.22]	5	Schottky barrier diodes (SBD)
[1.21]	10	SBD
[1.20]	20	SBD
Ref.	**Current Density (A/cm2)**	**Diode Type**
[1.24]	4000	Schottky *p*-*i*-n diode (SPIND)
[1.26]	7570	SBD
[1.23]	15000	*p*-*i*-n diode (PIND)

[1.25]	60000	Schottky *p*-n diode (SPND)
Ref.	**Breakdown Voltage (V)**	**Diode Type**
[1.27]	920	PIND
[1.32]	1000	SPIND
[1.30]	1600	SBD
[1.31]	2500	SBD
[1.28]	6700	SBD
[1.29]	10000	SBD
Ref.	**Breakdown Electric Field (MV/cm)**	**Diode Type**
[1.27]	2.3	PIND
[1.33]	3	SBD
[1.34]	3.1	SBD
[1.26]	4.2	SBD
[1.36]	5	SBD
[1.29]	7.7	SBD
[1.35]	7.7	SBD

Table 1.1 Highlights in diamond diode progress made in the past two decades with emphasis on maximum forward current, current density, breakdown voltage and breakdown electric field

1.2.2 Diamond Devices for RF Applications

Radar and radio receivers process small signals using very sensitive electronic components by amplifying the RF signal. These sensitive components can be easily damaged if a large RF signal is directly incident on them. Therefore, receiver protection limiter circuits are employed to protect the receivers from large input signals and allow the sensitive RF circuit to function normally when large signals are not present, for example low-noise amplifiers and downconverter mixers. Both of these circuit blocks can be damaged by even a small portion of the large transmitter signal if coupled to the receiver input. Therefore, active (FETs) or passive (diodes) RF power limiters are necessary. The main requirements for RF power limiters are the operating frequency and power handling

capability. A large amount of power can get dissipated in the power limiter devices. WBG material like diamond is very well suited for RF power limiter applications owing to its high carrier saturation velocity, carrier mobility and large thermal conductivity.

1.2.3 Diamond Devices for Extreme Environments

Venus and Earth are considered "twin planets" owing to their nearly identical size and densities and they stand out as being considerably more massive than other terrestrial planetary bodies. Venus has been revealed through past exploration missions to be extremely hot, devoid of oceans, apparently lacking plate tectonics, and bathed in a thick, reactive atmosphere, very much in contrast to Earth. Studying and exploring Venusian atmosphere and tectonic activity is important in understanding some important goals set by NASA's future exploration of Venus such as

a) Understand atmospheric formation, evolution, and climate history on Venus.
b) Determine the evolution of the surface and interior of Venus.
c) Understand the nature of interior-surface-atmosphere interactions over time, including whether liquid water was ever present.

Until now, ten Soviet landers (and two NASA atmospheric probes) have successfully reached the surface, but the longest operational duration on the surface, by the Soviet Venera-13, was barely more than 2 hours. The longevity and scope of proposed missions to the surface of Venus are currently limited by the challenge of developing electronics that can survive the ~460°C, ~92 bar corrosive environment [1.37], [1.38]. Despite the use of cooling measures, data transmission from previous Venus landers lasted only two hours

due to failure of the Si electronics [1.38]. Long term missions (beyond 2 months) to the surface of Venus are needed to make seismic observations, determine detailed mineralogy, and characterize atmosphere-surface interactions over an extended duration. This data can illuminate the origin and diversity of terrestrial bodies (e.g., how Venus and Earth diverged in climate and geology), as well as the factors that determine the evolution of life on some planets and not others. Moreover, a surface study of the runaway greenhouse gas effect on Venus can increase our understanding of the processes that control climate on Earthlike planets [1.37], [1.39], [1.40]. After a hiatus of nearly 30 years, NASA has selected 2 new Discovery-class missions to Venus. The VERITAS (Venus Emissivity, Radio Science, InSAR, Topography, and Spectroscopy) mission will focus on the surface and interior properties of Venus, including tectonic and impact history, gravity and geochemistry. The DAVINCI+ (Deep Atmosphere Venus Investigation of Noble gases, Chemistry, and Imaging, Plus) will send both an orbiter and a descent probe to study the chemical composition of the Venusian atmosphere down to the surface. The '+' refers to cameras on the descent probe that will map surface geology.

High temperature diamond electronics are relevant to the NASA HOTTech program as a means to reduce risk in future high-operating temperature mission opportunities, including a long-duration Venus lander, probes on the surface of Mercury, and deep probes of the atmospheres of the gas giant planets. Long duration operation is defined to be > 60 days at 500 °C, conditions for which stable operation of diamond electronic devices is entirely achievable. The need for long duration landers is especially

acute for direct measurements of seismological activity and interior structure on Venus but is also useful for understanding long-term meteorological and chemical trends in the near-surface atmosphere. The HOTTech program specifically cites the need for technologies related to power electronics. WBG materials such as diamond are perfectly suited for these extreme temperatures and environments because of their very low intrinsic carrier concentrations which lead to low leakage currents during normal operation. Several high temperature diamond diodes have been demonstrated previously in the literature as shown in Table 1.2 with a temperature as high as 1000^{o}C. For the HOTTech objective, not only do diamond diodes need to be designed for long term high temperature operation, high temperature packaging and testing also needs to be developed.

Ref.	Temperature (^{o}C)	Diode On-Off Ratio
[1.42]	400	$4x10^{4}$
[1.43]	500	10^{6}
[1.42]	700	33
[1.43]	1000	30

Table 1.2 High temperature operation highlights of diamond diodes from literature

1.3 This Work

This research is arranged in the following chapters:

- Chapter 2: Diamond growth and fabrication methods are discussed. The diamond fabrication involves niche techniques that are in contrast to standard Si processing techniques. Optimization of diamond etching, small sample lithography, metal deposition and lift-off processes and diamond surface cleaning procedures are discussed in detail. An example of a complete diamond process is also given.

- Chapter 3: Characterization of ultra-high current density diamond diodes is demonstrated and analyzed. Analytical models including thermionic emission and SCL current, as well as numerical simulation using Silvaco ATLAS models including carrier drift-diffusion, SRH recombination, incomplete ionization, hole hopping mobility, trap levels and carrier velocity saturation are constructed to reproduce experimental high current density results to high degree of accuracy. The SCL effects on the diode R_{ON} are discussed and a new interpretation of the Baliga figure-of-merit is proposed. Thus, a new R_{ON} vs. breakdown voltage curve is constructed for diamond. Other high current effects such as the self-heating in diode is also studied. Silvaco ATLAS simulations are performed to estimate the self-heating temperature as a function of on-state power conducted through the diamond diodes.
- Chapter 4: RF characterization of fabricated diamond diodes is performed. A small-signal model of a diamond diode in shunt configuration is constructed to reproduce the experimental S-parameters and impedance values to a high degree of accuracy. To improve the cut-off frequency (F_{CO}) figure-of-merit, Silvaco ATLAS simulations of various diamond diode designs are performed and an optimized structure is obtained for both diamond *p*-*i*-n and Schottky diodes. Using the optimized structures, transient mixed-mode Silvaco simulations of diamond *p*-*i*-*n* and Schottky diode-based receiver-protector (RP) circuits were performed. The power rejection performance of single-stage and two-stage RP circuits was

evaluated through the simulations. An assessment of the self-heating of diamond diodes under continuous-wave operation was also done. A design for high-frequency diamond MESFETs was also proposed and a ballpark estimate of the F_{Tmax} figure-of-merit was obtained.

- Chapter 5: High temperature characteristics of diamond material and diamond diodes is analyzed. Diamond diodes are fabricated and tested in extreme environments for an extended period of time. Several diamond diode samples were also prepared for the GEER test at the NASA facility. Analysis of the forward bias characteristics of diamond diodes at high temperatures was performed. Analytical models were also constructed to faithfully reproduce the high temperature reverse bias leakage currents and threading dislocation characteristics were evaluated.

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CHAPTER 2

DIAMOND GROWTH AND DEVICE FABRICATION

2.1 Introduction

Lab-grown diamond synthesis was first documented by William G. Eversole of Union Carbide [2.1], and since then a significant number of chemical vapor deposition (CVD) techniques were explored [2.2] to produce polycrystalline diamond films and coatings for various applications including cutting tools [2.4], heat dissipators [2.6] and mechanical seals for pumps [2.7]. In the early stages of progress, the CVD growth single crystal particles, polycrystalline and epitaxial films was thick (>10 μm) and non-transparent [2.8]. By 1992, General Electric (GE) demonstrated 50 μm thick transparent polycrystalline CVD diamond films with a growth rate of 1 μm in hydrogen and methane atmosphere at temperatures below 1000^{o}C. However, the mechanical, optical and electrical properties of such polycrystalline diamond were far inferior to the theoretically predicted properties of natural single crystal diamond due to grain boundaries containing sp^2 bonded carbon. High pressure, high temperature (HPHT) methods of synthesizing diamond were then developed in order to produce single crystals and have been since optimized [2.10], [2.11]. However, HPHT synthesis restricts the size and quality of diamond single crystals and its cost effectiveness is also poor. Therefore, over the past few decades, the microwave plasma CVD (MPCVD) and plasma enhanced CVD (PECVD) techniques were developed to produce diamond single crystals with pioneering efforts by Yan et al. [1.12] at the NSF Center for High Pressure Research at the Carnegie Institution. Since then, several efforts

have been made to advance MPCVD and PECVD diamond single crystal growth in terms of high quality, high growth rate and thicker films [2.13] - [2.16].

Doping of diamond for semiconductor applications has historically been challenging. Due to its lattice structure and material strength, high-energy ion implantation produces only shallow doping profiles and is often fraught with difficulties like irreversible radiation damage and graphitization [2.17]. Thermal diffusion doping of diamond has been recently studied with some success [2.19], but is a long way from becoming a reliable method of diamond doping. Substitutional doping by incorporation of dopants during the diamond CVD growth has been the most successful amongst all the doping techniques [1.13]. Among the substitutional dopants like B, P, N, O, Cu etc., B and P doping in diamond have seen the most success. Low concentrations of boron (B) ($\sim 10^{15}$ /cm^3) can be incorporated relatively easily in (100) oriented diamond single crystals as compared to high concentrations ($> 10^{20}$ /cm^3) where there is a high chance of loss of crystallinity. Phosphorus doping concentrations of $\sim 10^{19}$ /cm^3 have been successfully incorporated during the CVD growth. However, the P-doping of diamond is mostly successful in (111) oriented diamond single crystals and it is challenging to control the epitaxial growth. Despite the doping and growth challenges, progress in developing diamond devices has been promising and steadily increasing in the past few decades.

Due to the challenges in CVD growth of doped diamond layers and its cost effectiveness, reliable and high-quality diamond epitaxy can only be achieved on very small diamond plates/wafers, typically 3x3 mm to 10x10 mm in size. This size limitation

poses considerable challenges in the fabrication and processing of diamond devices. Diamond processing cannot follow most fabrication recipes optimized for 4-inch Si wafers, and therefore new techniques and recipes need to be developed specifically for small diamond wafers. The small wafer sizes also limit the number of devices that can be fabricated on a single wafer area and therefore special care needs to be taken while designing the wafer layout.

The following sub-sections give a brief overview of the diamond growth process developed at ASU and describe the diamond fabrication process developed in the ASU NanoFab.

2.2 Diamond PECVD Growth

Type IIb high-pressure, high-temperature (HPHT) 3x3 mm square diamond wafers from New Diamond Technology with (111) and (100) orientations were used throughout this research. Diamond wafers used for all diode growth were heavily doped with B ($\sim 2 \times 10^{20}/\mathrm{cm}^3$). The diamond growth on these HPHT Type IIb substrates is done in Prof. Nemanich's diamond growth lab at ASU and as described in [2.25] is a PECVD system based on an ASTeX AX5250 reactor with a customized water-cooled sample stage (Fig. 2.1(a)). Prior to any diamond growth, the HPHT substrates are cleaned in heated acid and base piranha solutions. The heated acid piranha solution treatment involves boiling the sample in H_2SO_4:H_2O_2:H_2O in a ratio of 3:1:1 at 220^{o}C for 15 min. followed by an HF bath for 5 min. The heated base piranha solution, following the heated acid piranha treatment, involves boiling the sample in NH_4OH:H_2O_2:H_2O in a 1:1:5 ratio at 75^{o}C for 15 min. The

diamond substrate is rinsed with DI water after each step of the cleaning. Once the diamond substrate is cleaned, it is loaded into the PECVD chamber that is held at a base pressure of 10^{-8} Torr using a turbo-pump backed by a dry-roots pump. For the growth of a p-i-n diamond diode, first an intrinsic diamond is grown on top of the heavy B doped HPHT substrate. During the i-layer diamond growth, a gas flow of 393 sccm of hydrogen (H_2), 7 sccm of methane (CH_4) and 0.75 sccm of oxygen (O_2) is maintained at a chamber pressure of $\sim$60 Torr and a microwave power of 1100 W and a growth temperature of $750^{o}C - 850^{o}C$ monitored by a dual-wavelength optical pyrometer. The optical pyrometer is also used for monitoring the intrinsic layer thickness using interference oscillations.

The n-type diamond growth is performed using a 200 ppm trimethlyphosphine in hydrogen (TMP/H_2) gas mixture as the phosphorus source. Before the n-layer growth, the intrinsic surface is primed with a 5 min hydrogen plasma with a hydrogen flow rate of 400 sccm in a chamber pressure of 65 Torr and a microwave power of 1500 W resulting in a temperature of $\sim 750^{o}C$. The phosphorus doped diamond growth is then performed at the flow rates of H2 at 349 sccm thereby establishing the CH_4 flow rate at 0.25 sccm combined with a 200 ppm TMP in a H_2 flow rate of 50 sccm.

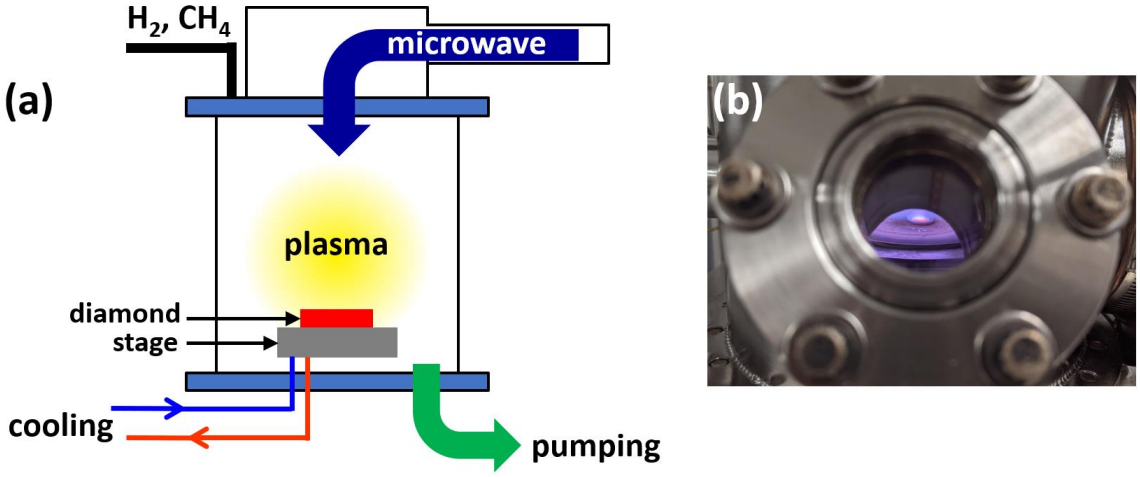


Fig. 2.1 (a) Schematic of a typical ASTeX AX5250 PECVD diamond reactor (b) Diamond growth in the PECVD diamond reactor

In some cases, a highly nitrogen (N) doped nanocrystalline diamond (NCD) has been grown as a contact layer on top of the n-layer in a p-i-n diamond diode. The highly N-doped NCD was grown in 5 sccm H_2, 20 sccm CH_4, 100 sccm N_2 and 10 sccm Ar gas mixture in a chamber pressure of 20 Torr and a microwave power of 900 W leading to a substrate temperature of $\sim 900^{o}C$. The highly nitrogen doped NCD or nano-carbon (nanoC) layer provides a highly conductive diamond layer and is used in certain diamond diode samples to reduce contact resistance [2.26].

A typical doping profile of the growth stack in a nanoC-p-i-n diamond diode obtained from a SIMS analysis is shown in Fig. 2.2. Here, the nanoC layer here is 300 nm thick while the phosphorus doped n-layer is ~ 500 nm and the i-layer is ~ 200 nm thick.

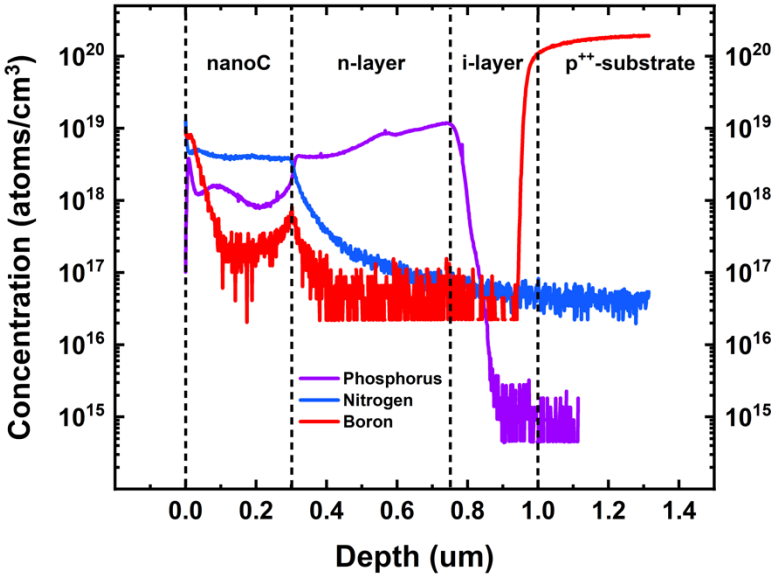


Fig. 2.2 Typical doping profile of P, N and B doping concentrations in a nanoC-p-i-n diamond diode obtained from SIMS analysis

2.3 Diamond Fabrication and Processing

Fabrication techniques were specifically designed for small diamond samples of 2x2 mm to 5x5 mm squares. Some of the processing challenges of fabricating devices on such small area wafers are photoresist edge-beads, mask alignment during contact lithography, variation of plasma density over the surface area during reactive ion etching (RIE) and CVD and sample mounting and spin coating. The following sub-sections describe certain workarounds and optimizations to minimize previously described processing issues in the diamond device fabrication and detail a typical complete diamond diode fabrication process.

2.3.1 Spin Coating

One of the main challenges in spin coating photoresist onto a 3x3mm diamond wafer is to minimize the edge beads. Edge beading causes the photoresist thickness to be uneven and increasingly large towards the wafer edges, as shown in Fig. 2.3(a). This causes uneven photoresist development after patterned UV exposure and eventually an unsuccessful photolithography. Using conventional recipes described for MSDS photoresist result in large edge beads. The relatively slow spin coater rotational speeds described in standard recipes for various photoresists on a 3x3mm diamond wafer cause the photoresist to pile up near the wafer edge and dry off within the spin cycle. Therefore, the conventional recipes were modified by adding a short "snap-spin" step prior to the main longer time spin coating step. Prior to spin coating the photoresist, the diamond surface is cleaned with 1 min sonication baths of acetone and IPA followed by de-hydration bake on a hot plate at 180^{o}C for 5min. As shown in Fig. 2.3(b), the sample is then mounted on a 2" chuck of a Brewer Science CEE 200CBX spin coater. The chuck is covered with a cleanroom compatible "blue-tape" covering its vacuum ports and a small vacuum hole is pierced through the center of the blue-tape covered chuck to limit the vacuum only below the sample. Limiting the vacuum to a small area below the sample helps securing the sample thoroughly and slows down the drying of the photoresist. To further reduce the photoresist drying during the spin, the spin coating bowl is dispersed with extra photoresist around the chuck while the lid of the spin-coater is kept closed as much as possible. This causes the solvent in the photoresist (propylene glycol monomethyl ether acetate (PGMEA)

and ethyl lactate in most AZ photoresist series and cyclopentanone in most LOR photoresists) to evaporate and create a solvent rich atmosphere in the bowl (Fig. 2.3(c)). The solvents of respective photoresists can also be sprayed with a mist sprayer in the spin coating bowl to enrichen the solvent content in its atmosphere.

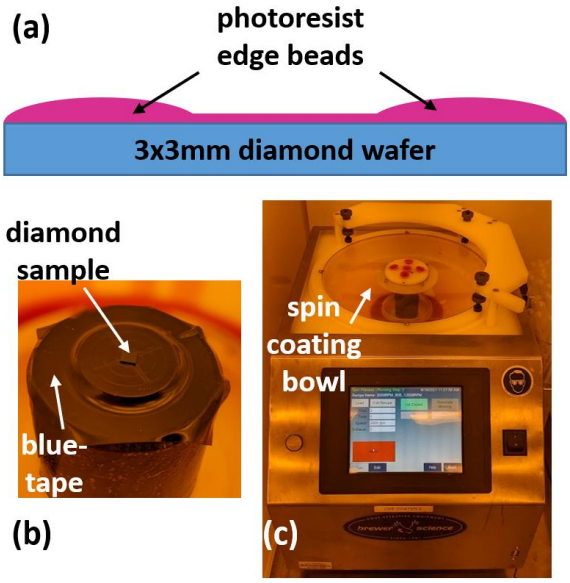


Fig. 2.3 (a) Photoresist edge-bead formation on the edges of a 3x3mm diamond sample (b) Spin coater chuck with blue-tape and sample in middle (c) CEE 200CBX spin coater with a solvent rich atmosphere bowl

The photoresists are disbursed onto the sample area with a pipette and the spin coating recipe is started immediately. The spin coating recipe starts with a snap-spin which is a burst of high-speed rotation of the spin coater at 12000 RPM for the initial 4 seconds. This high-speed burst causes large centrifugal force that disburses the photoresist evenly on the sample area and prevents the formation of thick edge beads. The snap-spin is followed by a relatively low speed (depending on the photoresist) rotation for a longer time. The resulting unevenness of the photoresist due to small unavoidable edge-beads is limited

within 200 μm from the wafer edges and constitutes a maximum of ~26% of the 3x3 mm diamond wafer (in comparison to roughly 80% to 90% with standard photoresist recipes). The photoresists are baked at their respective optimized baking temperatures and time (detailed in Table 2.2) and are ready for patterned UV exposure.

2.3.2 Mask Design and UV Exposure

Due to the small wafer size of the diamond samples, special care must be taken while designing the mask layer alignment marks in a CAD design. Several iterations of the alignment mark design were made to obtain the best possible accuracy in mask layer alignment during lithography. Fig. 2.4 shows the alignment mark obtained after several design versions. The alignment mark shown here aligns the metal contact layer (shaded red) to the underlying mesa isolation layer (solid blue). The x and y vernier scales with 8 μm wide legs, 8 μm pitch and total length of 180 μm help in aligning the two layers with an accuracy of ~3 μm on a 3x3 mm diamond wafer. Additional structures enveloped within the x and y vernier scales provide visual guidance during alignment. An OAI 808 Mask Aligner contact lithography system is used for patterning of the photoresist layer on a 3x3 mm diamond sample. UV exposure times are optimized depending on the type of photoresist and are detailed in Table 2.2. Once the mask pattern is exposed onto the diamond wafer, a post-exposure bake is performed depending on the photoresist used. The UV exposed photoresist is then developed in AZ-300-MIF photoresist developer for an optimized time (given in Table 2.2) and then rinsed with water for 1.5 min. The AZ-300-MIF developer is a metal-ion free photoresist developer with 2.38% by weight high purity

tetramethyl ammonium hydroxide (TMAH) in water. In diamond device fabrication, the patterned photoresist pattern is then used either for metal deposition or as a hard mask for etching the dielectric underneath, with additional steps in between.

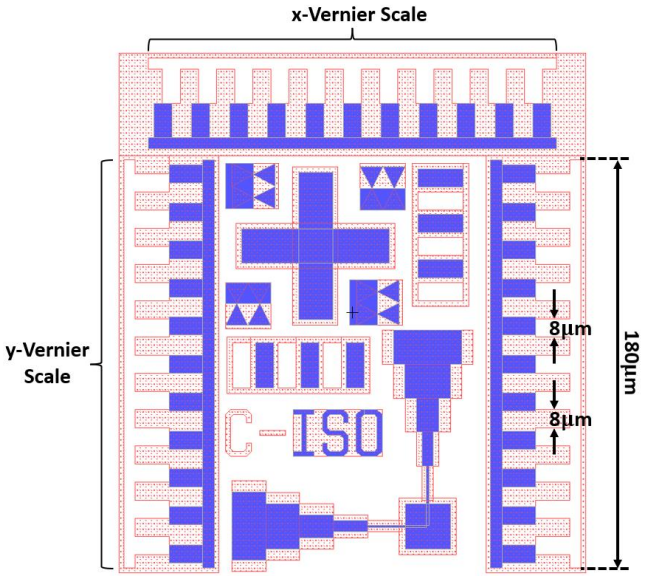


Fig. 2.4 Alignment marks with x and y vernier scales for accurate alignment

2.3.3 Double Layer Photolithography

For patterning of the device metal contacts with e-beam deposition and lift-off, a double layer process is used. The double layer photolithography consists of a lift-off resist (LOR3A) followed by an exposable g-line photoresist such as AZ3312 or AZ4330. AZ3312 is a crossover positive tone photoresist with a typical film thickness of 1µm and used for defining features greater than 1µm and is used all diamond metal contact lithography. A successful metal deposition lift-off is ensured by a successful double layer photolithography. Successful development of a double layer photoresist pattern should

have an inverted T cross-section with the bottom LOR3A layer developed more than the exposable AZ3312/AZ4330 top photoresist layer, as shown in Fig. 2.5(a).

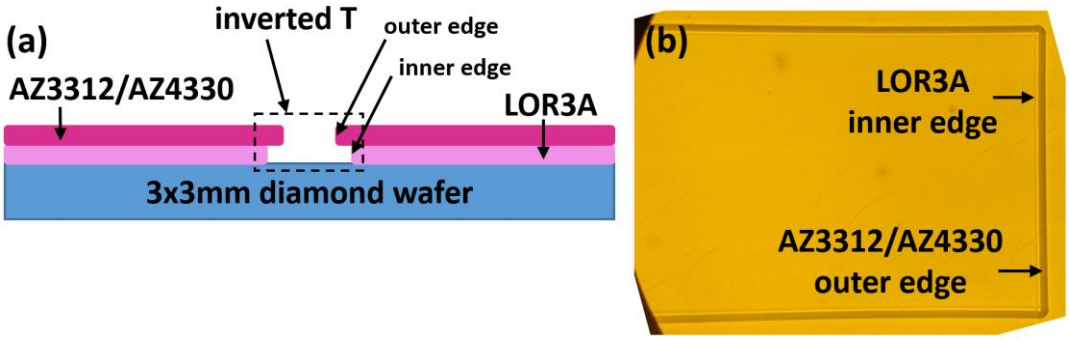


Fig. 2.5 (a) Cross-section of a successful double layer photoresist after patterned UV exposure and development with an inverted T formed between LOR3A and AZ3312/AZ4330 photoresist which can be verified by a (b) yellow light microscope image consisting of the LOR3A inner edge and AZ3312/AZ4330 outer edge

The inverted T cross-section of the double layer photoresist can be verified by observing the top view for an "inner edge" of the LOR3A and an "outer edge" of the AZ3312/AZ4330 under the highest magnification of a yellow light microscope, as shown in Fig. 2.5(b).

2.3.4 Single Layer Photolithography

For patterning of a dielectric hard mask or a surface passivation, single layer photolithography is used typically with the AZ4330 photoresist. AZ4330 is positive tone photoresist with higher viscosity than AZ3312 and is typically used for high aspect ratio lithography features. In the diamond fabrication process, AZ4330 is used as a hard mask for patterning SiO_2, which itself is used as a hard mask for pattern etching diamond. The spin coating methodology and UV lithography with AZ4330 is same as mentioned previously with the specific details as given in Table 2.2. Once the AZ4330 is patterned

after developing in AZ-300-MIF, it is hard baked at 120°C for 30 min in a conventional oven. This improves the selectivity of AZ4330 to SiO_2 (or Si_3N_4) to 2:1 during RIE. Fig. 2.6 shows a resulting surface profilometry of the patterned AZ4330 after the hard bake. A typical thickness of ~2 μm is expected.

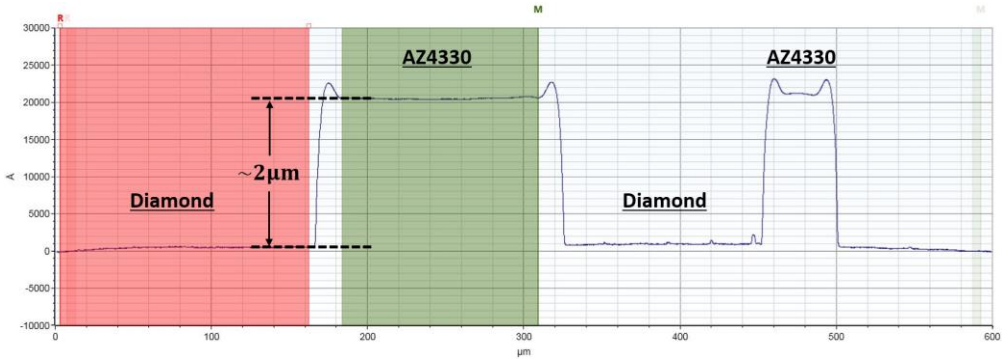


Fig. 2.6 Surface profilometry of a patterned AZ4330 using a Bruker Dektak XT profilometer

2.3.5 Dielectric Deposition for Surface Passivation and Hard Mask

SiO_2 has been used as a hard mask for etching diamond in this fabrication process. SiO_2 is preferred over metal hard mask such as Al or Ni to avoid metal impurities over the diamond surface. Other dielectrics such as Si_3N_4 and Al_2O_3, along with SiO_2, have also been used for surface passivation of etched diamond sidewalls and help in reducing side-wall leakage current. Deposition of SiO_2 and Si_3N_4 is done using an Oxford Plasmalab System 100 PECVD. The SiO_2 PECVD is done using a gas mixture of SiH_4 at a flow rate of 170 sccm and N_2O at 710 sccm in a chamber pressure of 1000 mTorr at a microwave power of 20 W and a temperature of 350°C. Due to the small size of the diamond wafers, the plasma non-uniformity due to edge effects of the wafer is large enough to cause non-

uniformity in the deposited film thickness over the entire 3x3 mm wafer area. Therefore, to minimize the plasma non-uniformity on the diamond wafer surface, a special silicon carrier wafer is made. The silicon carrier wafer is a 4 inch 750 μm thick Si wafer with several 3x3x0.3 mm etched pockets, as shown in Fig. 2.7. The surfaces of the 3x3 mm diamond wafers placed into the 3x3x0.3 mm pockets flush with the Si surface and the Si carrier wafer is loaded into the PECVD chamber for dielectric deposition. The two flushed surfaces help reduce plasma non-uniformity and give a more uniform dielectric thickness over the diamond surface area.

The Al_2O_3 deposition is done in a Cambridge NanoTech S100 atomic layer deposition (ALD) chamber. The Al_2O_3 ALD is a TMA metal-precursor based deposition with a growth rate of 1 Å per cycle. Both PECVD and ALD deposition details are specified in Table 2.2.

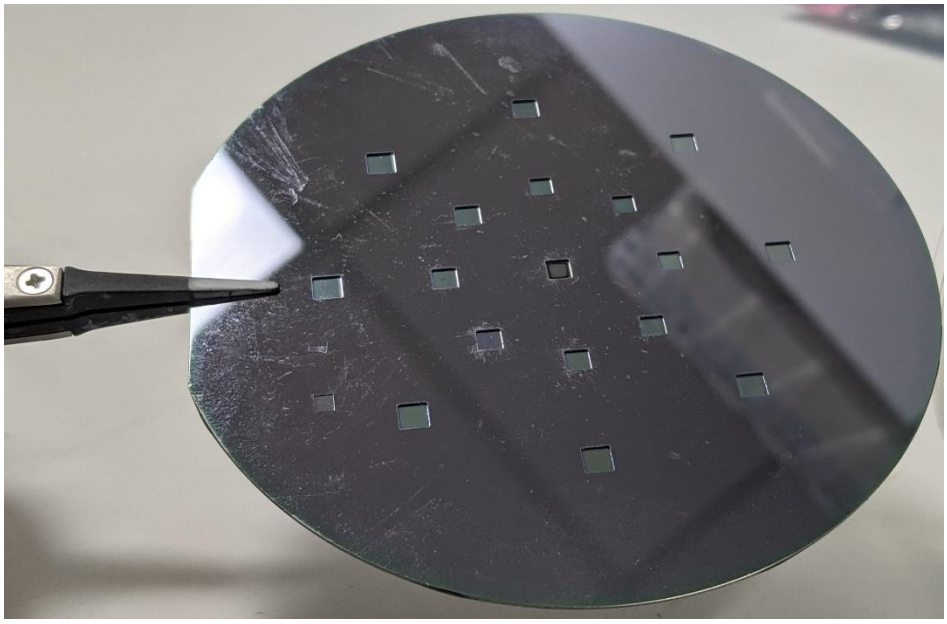


Fig. 2.7 Thick Si carrier wafer with 3x3x0.3 mm deep etched pockets for loading 3x3mm diamond wafers in the PECVD chamber.

2.3.6 Etching of Diamond and Dielectrics

Partial mesa etching of diamond is done during every diamond fabrication process to define and isolate individual diode regions. Diamond etching is done in a PlasmaLab M80+ reactive ion etching (RIE) chamber with a gas mixture of SF_6:O_2 at a gas flow rate of 2:38 sccm, respectively, maintaining a 15 mT chamber pressure and a microwave power of 300 W. The etching was optimized for an etch rate of $\sim 24\ \mathrm{nm/min}$ and minimum post-etching surface roughness. The diamond etching is more due to physical bombardment of O_2^- radicals in the chamber than the chemical etching in the presence of oxygen in the chamber. As a result, the diamond surface heats up during the etching. This can vary the etch rate during the etching. Therefore, the etching recipe is divided into 5 min etching and 5 min cooling steps. The microwave power is turned on and off during the etching and

cooling steps, respectively. As mentioned previously, SiO_2 is used as a hard mask to etch a mask pattern into diamond and has an etch rate of $\sim 20\ \mathrm{nm/min}$ in the diamond etching recipe providing a selectivity of ~ 1.2 of diamond over SiO_2.

Etching of SiO_2 (for its use as a hard mask or a sidewall passivation) is also done in the PlasmaLab M80+ chamber with a gas mixture of Ar:CHF_3 with gas flow rates of 25:25 sccm, respectively, while maintaining a chamber pressure of 30 mTorr and a microwave power of 200 W. An etch rate of $\sim 44\ \mathrm{nm/min}$ was optimized. As mentioned in section 2.3.4, AZ4330 single layer photoresist is used as a hard mask for pattern etching SiO_2. Again, to avoid plasma heating of sample surface, the etching is done in 5 min etching and 5 min cooling steps. During the etching, hydrocarbons from the photoresist may deposit back on to the sample surface, therefore the SiO_2 etching recipe is finished by performing a photoresist clean step using an O_2 plasma at 45 sccm gas flow in a chamber pressure of 350 mTorr and a microwave power of 25 W. The etch rate of AZ4330 in the SiO_2 etch recipe is $\sim 20\ \mathrm{nm/min}$.

Si_3N_4 etching is done in the PlasmaLab M80+ chamber using a high etch rate recipe in a gas environment of 20 sccm NH_3, 440 sccm of SiH_4 and 600 sccm of N_2 under a chamber pressure of 650 mT and a microwave power of 20 W.

Al_2O_3 etching is done in a PlasmaLab M80+ chamber with a gas environment of BCl_3 under a pressure of 15 mT and microwave power of 200 W. A typical etch rate of $\sim 8\ \mathrm{nm/min}$ is achieved.

2.3.7 Diamond Surface Cleaning and Oxygen Termination

Diamond surface cleaning and oxygen termination is an important step during the fabrication process to remove organo-metallic and other surface contaminations and remove any surface conduction. Table 2.1 lists the heated acid and base chemicals used in the diamond surface cleaning and oxygen termination process and details the cleaning procedure. This procedure is similar to the one described in [2.28].

Chemicals				
A]	**Heated Acid Piranha**		**Ratio**	**Quantity**
	1	Sulfuric Acid (H_2SO_4)	3	150ml
	2	Hydrogen Peroxide (H_2O_2)	1	50ml
	3	Water (H_2O)	1	50ml
B]	**Hydrogen Fluoride (%48) (HF)**			150ml
C]	**Heated Base Piranha**			
	1	Ammonium Hydroxide	1	50ml
	2	Hydrogen Peroxide (H_2O_2)	1	50ml
	3	Water (H_2O)	5	250ml
D]	**Oxygen Termination**			
	1	Sulfuric Acid (H_2SO_4)	3	150 ml
	2	Nitric Acid (HNO_3)	1	50 ml
Procedure				
1	Diamond sample is boiled in an acid piranha mixture ($H_2SO_4/H_2O_2/H_2O$, 3:1:1) at 220 °C for 15 min to remove organic and metallic surface contamination			
2	Rinse with DI water			
3	HF bath for 10 min to remove SiO_2 and metallic contamination			
4	Rinse with DI water			
5	Diamond is boiled base piranha mixture ($NH_4OH/H_2O_2/H_2O$, 1:1:5) at 75 °C for 15 min to remove the organic contamination			
6	Rinse with DI water			

7	Diamond is boiled in sulfuric (H_2SO_4) + nitric (HNO_3) acid mixture at 220^oC for 30 min
8	Rinse diamond samples with DI water for 1 min each

Table 2.1 Chemicals used and procedure for diamond surface cleaning and oxygen termination

2.3.8 Photoresist Descum

Surface termination is important especially for diamond diode metal contacts. Surface Fermi level pinning determines the Schottky barrier height of the Schottky metal (Ti) to n-layer diamond. Therefore, to ensure consistent surface conditions for all diamond diodes, the exposed diamond contact areas just after photoresist development are treated with oxygen plasma for 1 min 30 sec in a PlasmaTherm 790 RIE chamber under 10 mT pressure and with a 100 W of microwave power.

2.3.9 Metal Deposition and Lift-off

Contact metal deposition is done in a Lesker PVD-75 e-beam deposition chamber. Fabmate Graphite crucibles are used to carry the deposition metals. For most of the diamond diode contacts (anode and cathode), a metal stack of Ti:Ni:Au or Ti:Pt:Au with thicknesses of 50 nm: 50 nm: 300 nm is deposited. Ti forms TiC with the diamond surface and improves adhesion and also forms a Schottky contact with the n-type diamond. Ni or Pt acts as an inter-metallic diffusion barrier between Ti and Au. The thick Au layer helps prevent oxidation of the underlying Ti or Ni and provides good contact for electrical probing. On average lower tensile stress metals are preferred to be used as contact metals, especially at high temperatures. Fig. 2.8 shows various tensile and compressive stress of

different 100 nm thick metal thin films deposited by sputtering or e-beam evaporation on a 6" Si wafer in the ASU nanofab. As can be seen from Fig. 2.8, Ni (e-beam) has a tensile stress approximately $2/3$ that of Pt (e-beam). Therefore, Ni is preferred over Pt as an inter-metallic diffusion barrier metal for contacts on diamond diodes.

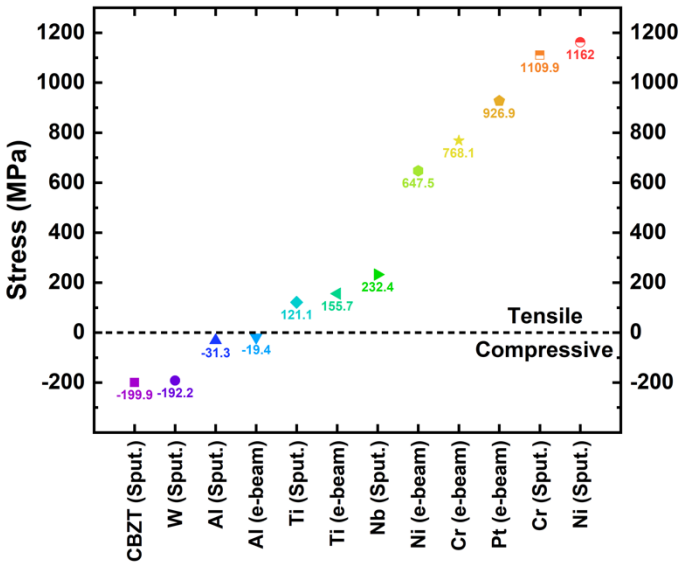


Fig. 2.8 Stress of different 100 nm thick metal thin films deposited by either sputtering or e-beam evaporation tested on a 6" Si wafer.

After the metal deposition, lift-off process is performed to define the metal contacts. The metal deposited samples are soaked in a $150^{o}C$ heated AZ400T photoresist stripper solution for at least 30 min for all the metal to lift-off. AZ400T is a tetramethylammonium hydroxide (TMAH) based photoresist stripper. Often a few minutes of sonication is needed to cleanly lift-off any residual metal.

2.3.10 Complete Diamond Processing Steps

Following Table 2.2 and Fig. 2.9 detail an example of a complete diamond fabrication.

Step	Tool	Procedure Details						
1	**Soft Clean**							
	Sonicator	1	Acetone sonication, 1min					
		2	IPA sonication, 1min					
2	**PECVD SiO_2 Deposition (hard mask)**							
	Oxford Plasmalab System 100 PECVD	**Gas**	**Flow (sccm)**	**Pressure (mT)**	**Power (W)**	**T_C (°C)**	**Time**	**Thk. (nm)**
		SiH4: N2O	170: 710	1000	20	350	22min 17sec	1500
3	**Soft Clean + Dehydration Bake**							
	Sonicator	1	Acetone sonication, 1min					
		2	IPA sonication, 1min					
	Hot plate	3	180°C for 5 min					
4	**Isolation Photolithography (single layer)**							
	1 Brewer Science CEE 200CBX spin coater	1	AZ4330; r.p.m. = 12k:3k; time = 4sec:45sec					
		2	Photoresist bake = 105°C, 2 min					
	2 OAI 808 Mask Aligner	ISO layer, Exposure time: 18 sec						
	3 Hot plate	Post-exposure bake: 105°C, 1 min						
	4 AZ-300-MIF	Development time = 75 sec						
5	**Photoresist Hard bake**							
	Conventional oven	120°C, 30 min						
6	**SiO2 (hard mask) etch**							
	PlasmaLab M80+ RIE	**Gas**	**Flow rate (sccm)**	**Pressure (mT)**	**Power (W)**	**Time (min)**		
		$Ar:CHF_3$	25:25	30	200	34		
7	**Photoresist Strip**							
	AZ400T	150°C, 15 min						
8	**Diamond Etch**							
	PlasmaLab M80+ RIE	**Gas**	**Flow rate (sccm)**	**Pressure (mT)**	**Power (W)**	**Time (min)**		
		$SF_6:O_2$	2:38	15	300	20		

9	**SiO_2 Strip**							
	Hydrofluoric Acid (%48) (HF)	30 min dip						
11	**PECVD SiO_2 Deposition (hard mask)**							
	Oxford Plasmalab System 100 PECVD	**Gas**	**Flow (sccm)**	**Pressure (mT)**	**Power (W)**	**T_C (°C)**	**Time**	**Thk. (nm)**
		SiH_4: N_2O	170: 710	1000	20	350	22min 17sec	1500
12	**Soft Clean + Dehydration Bake**							
	Sonicator	1	Acetone sonication, 1min					
		2	IPA sonication, 1min					
	Hot plate	3	180°C for 5 min					
13	**Top p-contact Photolithography (single layer)**							
	1	Brewer Science CEE 200CBX spin coater	**1**	AZ4330; r.p.m. = 12k:3k; time = 4sec:45sec				
			2	Photoresist bake = 105°C, 2 min				
	2	OAI 808 Mask Aligner	Top p-contact layer, Exposure time: 18 sec					
	3	Hot plate	Post-exposure bake: 105°C, 1 min					
	4	AZ-300-MIF	Development time = 75 sec					
14	**Photoresist Hard bake**							
	Conventional oven	120°C, 30 min						
15	**SiO2 (hard mask) etch**							
	PlasmaLab M80+ RIE	**Gas**	**Flow rate (sccm)**	**Pressure (mT)**	**Power (W)**	**Time (min)**		
		$Ar:CHF_3$	25:25	30	200	34		
16	**Photoresist Strip**							
	AZ400T	150°C, 15 min						
17	**Diamond Etch**							
	PlasmaLab M80+ RIE	**Gas**	**Flow rate (sccm)**	**Pressure (mT)**	**Power (W)**	**Time (min)**		
		$SF_6:O_2$	2:38	15	300	20		
18	**SiO_2 Strip**							
	Hydrofluoric Acid (HF)	30 min dip						
19	**Diamond Surface Cleaning and Oxygen Termination (as detailed in Table 2.1)**							
20	**PECVD SiO_2 Deposition (surface passivation)**							
	Oxford Plasmalab System 100 PECVD	**Gas**	**Flow (sccm)**	**Pressure (mT)**	**Power (W)**	**T_C (°C)**	**Time**	**Thk. (nm)**
		SiH4: N2O	170: 710	1000	20	350	7 min	200

21	**Soft Clean + Dehydration Bake**						
	Sonicator		1	Acetone sonication, 1min			
			2	IPA sonication, 1min			
	Hot plate		3	180^{o}C for 5 min			
22	**Passivation Via Photolithography (single layer)**						
	1	Brewer Science CEE 200CBX spin coater	1	AZ4330; r.p.m. = 12k:3k; time = 4sec:45sec			
			2	Photoresist bake = 105^{o}C, 2 min			
	2	OAI 808 Mask Aligner	Via layer, Exposure time: 17 sec				
	3	Hot plate	Post-exposure bake: 105^{o}C, 1 min				
	4	AZ-300-MIF	Development time = 75 sec				
23	**Photoresist Hard bake**						
	Conventional oven		120^{o}C, 30 min				
24	**SiO2 (surface passivation) via etch**						
	PlasmaLab M80+ RIE		**Gas**	**Flow rate (sccm)**	**Pressure (mT)**	**Power (W)**	**Time (min)**
			$Ar:CHF_3$	25:25	30	200	3
25	**Photoresist Strip**						
	AZ400T		150^{o}C, 15 min				
26	**Soft Clean + Dehydration Bake**						
	Sonicator		1	Acetone sonication, 1min			
			2	IPA sonication, 1min			
	Hot plate		3	180^{o}C for 5 min			
27	**Contact Photolithography**						
	1	Brewer Science CEE 200CBX spin coater	1	LOR3A; r.p.m. = 12k:3k; time = 4sec:45sec			
			2	Photoresist bake = 180^{o}C, 5 min			
			3	AZ3312; r.p.m. = 12k:3k; time = 4sec:45sec			
			4	Photoresist bake = 105^{o}C, 2 min			
	2	OAI 808 Mask Aligner	Contact layer, Exposure time: 5.7 sec				
	3	Hot plate	Post-exposure bake: 105^{o}C, 1 min				
	4	AZ-300-MIF	Development time = 75 sec				
28	**Photoresist Descum**						
	PlasmaTherm PT790 RIE		**Gas**	**Flow rate (sccm)**	**Pressure (mT)**	**Power (W)**	**Time (min)**
			O_2	20	10	100	1 min 30 sec
29	**Top contact metal deposition**						
	Lesker PVD-75		Ti:Ni:Au :: 50 nm: 50 nm: 300 nm				
30	**Metal lift-off**						
	1	AZ400T	Soak at 150^{o}C for 30 min				

	2	Sonicator	Sonicate for ~1 min
31	**Bottom contact metal deposition**		
	Lesker PVD-75		Ti:Ni:Au :: 50 nm: 50 nm: 300 nm

Table 2.2 Example of complete diamond diode fabrication processing steps

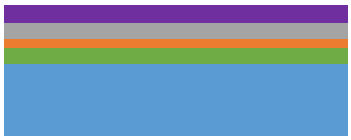
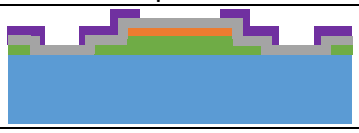
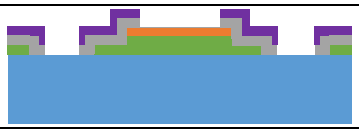
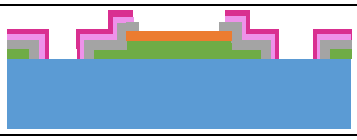
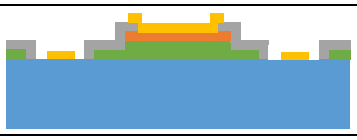
[1] AZ4330 spin coating on PECVD SiO_2 deposited diamond	[2] Patterning of AZ4330 with UV photolithography and hard baking AZ4330	[3] SiO_2 etching in RIE
		
[4] AZ4330 strip and partial mesa diamond etching in RIE	[5] SiO_2 strip and top p-contact SiO_2 hard mask PECVD deposition	[6] Top p-contact single layer photolithography with AZ4330
		
[7] Hard bake and top p-contact SiO_2 etching in RIE	[8] Top p-contact diamond etching in RIE	[9] Photoresist strip, SiO_2 strip, acid clean, surface oxygen termination
		
[10] Surface passivation SiO_2 PECVD deposition	[11] Single layer photolithography with AZ4330 of passivation via	[12] Etching vias into surface passivation SiO_2 in RIE
		
[13] Double layer contact photolithography with LOR3A and AZ3312	[14] Metal deposition and lift-off	[15] Backside contact metal deposition
		

Fig. 2.9 Schematics of sequential diamond diode processing steps

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CHAPTER 3

DIAMOND DIODES FOR HIGH POWER APPLICATIONS

3.1 Introduction

High power applications of diamond such as motor drivers, high power supplies, electric vehicle charging, photovoltaics etc. require devices to perform equally well in the high current (forward bias) and blocking voltage (reverse bias) regimes. An ideal device would offer very low on-resistance and very high blocking voltage. Theoretically, diamond offers large advantages in both the regimes owing to its very high thermal conductivity ($\kappa = 22 - 24\ \mathrm{W/cm.K}$) that can handle large amounts of current with minimal or no heatsinks and high breakdown field ($10 - 20\ \mathrm{MV/cm}$), as is summarized in [3.1]. However, the diamond technology maturity is still nascent and practical difficulties in material quality, processing, growth and space charge limited current limits pose big challenges. The following sub-sections address high current, breakdown, self-heating and current transient analysis of diamond diodes.

3.2 High Current Analysis

Practical challenges in diamond growth, material quality, processing and doping have been some of the main reasons for diamond's under-performance in comparison to its potential. One of the important metrics for on-state efficiency is the specific on-state resistance $R_{ON}S$ as given by [3.2],

$$R_{ON}S = \frac{L_{Drift}}{q(\mu_p p)} \tag{3.1}$$

where L_{Drift} is the drift region and p is the free carrier concentration, in this case for holes. Fig. 3.1.5 in [3.3] indicates that the experimental values of $R_{ON}S$ of diamond Schottky diodes are about 1-2 orders higher than expected theoretical values. This increased value of on-state resistance increases switching losses and therefore reduces power conversion efficiency. As such, it is important to investigate the factors affecting $R_{ON}S$ in diamond diodes in order to optimize device design and diamond growth.

Makino et. al [3.4] demonstrated the highest reported diamond diode forward current density prior to the current work ($> 60\ kA/cm^2$ at 6 V), and argued that diamond Schottky PN diodes (SPNDs) can be designed with a drift layer thickness for a desired blocking voltage V_{block} without having to compromise $R_{ON}S$. However, Hitchcock and Chow [3.5] show that the drift layer cannot be arbitrarily increased to achieve a suitable V_{block} since increasing the drift layer thickness causes the buildup of a space charge layer in the drift region and inhibits injection of holes from the p^+ layer i.e., space charge limited conduction, degrading the performance of SPNDs. Although Hitchcock and Chow aptly reason the practical limiting factor for the diamond diode forward current, they did not include in their modeling the more complex physics in real devices, which also affect the diode current. To fully understand the limitations on the forward characteristics of a real diamond device, practical considerations of the real material properties of diamond and other physical effects need to be considered. Maréchal et. al [3.6] have attempted reproducing

experimental I-V characteristics with such practical considerations, however a poor fit to the low injection current regime is shown and an emphasis on tuning SRH carrier lifetimes and Auger recombination parameters is applied rather than modelling the effects of e.g., multiple trap levels.

The research work in the present dissertation demonstrates the highest reported current density of $\sim 116\,\mathrm{kA/cm^2}$ at $\sim 16\,\mathrm{V}$ forward bias in a diamond Schottky P-I-N diode (SPIND) and is compared to both analytical models and TCAD (Technology Computer Aided Design) simulation with realistic material properties to accurately reproduce the measured diamond diode *J-V* characteristics and elucidate the limiting factors in figures of merit such as the on-state resistance. In the following, Sections 3.2.1 and 3.2.2 present the diamond SPIND growth, fabrication and experimental measurement results. Section 3.2.3 builds the analytical model and formulates all the physics models used in the Silvaco ATLAS TCAD simulations. Physical effects such as trapping of charge carriers at multiple single level traps within the bandgap, field dependent hopping mobility, incomplete ionization of doping impurities and bulk and contact resistances are considered in the combined theoretical analysis (analytical and TCAD models) and a space charge limited current is analyzed. Section 3.2.4 reports on the comparison of the experimental J-V characteristics with the theoretical models and their fit. The effects of different trap configurations – shallow trap, deep trap, two single level traps and three single level traps, on the J-V characteristics, turn on voltage V_T, space charge limited conduction and specific on-resistance $R_{ON}S$ are explored in detail in this section. We also establish theoretical limits

of an ideal diamond SPIND diode with a Mott-Gurney space charge limit. Conclusions and further investigations are proposed in Section 3.5.

3.2.1 Growth and Diode Fabrication

Phosphorus doped n-layers and an undoped intrinsic i-layers with target thicknesses of 50 nm and 300 nm were grown on a thick p-type <111> high-pressure, high-temperature (HPHT) 3x3 mm diamond substrate, constituting a *p*-*i*-*n* diode structure. The p-type HPHT diamond is heavily doped with boron (B) ($\sim 3 \times 10^{20}/cm^3$) and is 300 µm in thickness. The phosphorus doping concentration in the n-layer is typically $\sim 3 \times 10^{17}/cm^3$ whereas a background p-type doping of $\sim 4 \times 10^{14}/cm^3$ and background n-type doping of $\sim 10^{14}\ /cm^3$ is expected in the intrinsic layer. 50 µm diameter circular diodes were then patterned on the *p*-*i*-*n* growth stack by partially etching into the *i*-layer diamond. The partial mesa etch ensures electrical isolation between diodes by leaving a highly insulating i-layer on the surface between them, as shown in Fig. 3.1. $38\ \mu m$ wide circular cathode contacts to the n-layer are defined by patterning a Ti/Pt/Au (50 nm/50 nm/300 nm) metal stack on to the isolated diode mesa. Top anode contacts to the p^{++}-layer were made by additionally etching trenches to the sides of the mesa etch and depositing a Ti/Pt/Au patterned metal stack separated by $90\ \mu m$ from the cathode contact. The same metal stack forms a Schottky cathode and an ohmic anode due to a near-metallic doping of the p^{++}-layer. Diamond CVD growth and fabrication methods are as detailed in Chapter 2. Fig. 3.1(a) shows a cross-section of the diamond SPIN diode pseudo-vertical diode structure and Fig. 3.1(b) shows the fabricated diamond SPIND device.

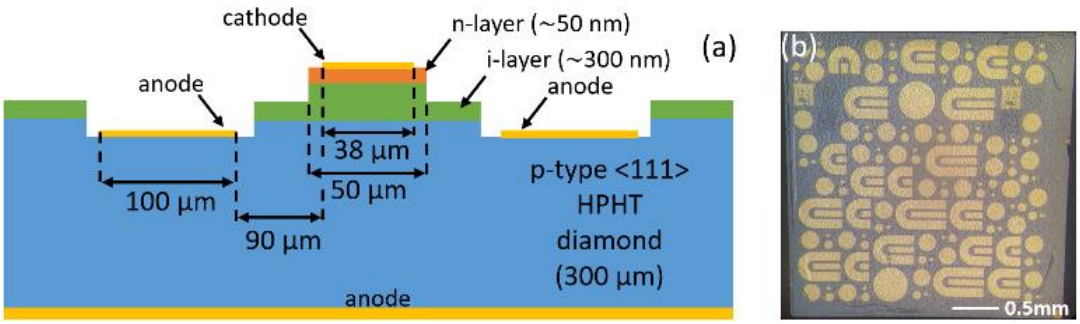


Fig. 3.1 (a) Cross-section of diamond SPIN diode (b) Microscope top-view of the fabricated diamond SPIN diode sample

3.2.2 DC and Pulsed Characterization

High resolution low noise dc J-V characteristics of diamond SPINDs were measured using an Agilent 4156b semiconductor parameter analyzer. The 4156b instrument has a current limit of 100 mA and therefore for higher current levels, pulsed J-V measurements were performed using an Agilent E3615A high current source meter controlled by the pulse sweep mode of the 4156b. The low and high power two-probe measurement system is as shown in Fig. 3.2. Pulsed J-V measurements at high currents are purposely done to reduce diode self-heating as much as possible. A pulse width of 10 msec and a period of 1 sec is maintained during the pulsed J-V measurements to give a duty cycle of ~1% while a medium integration time of 20 msec is maintained during the dc J-V characterization.

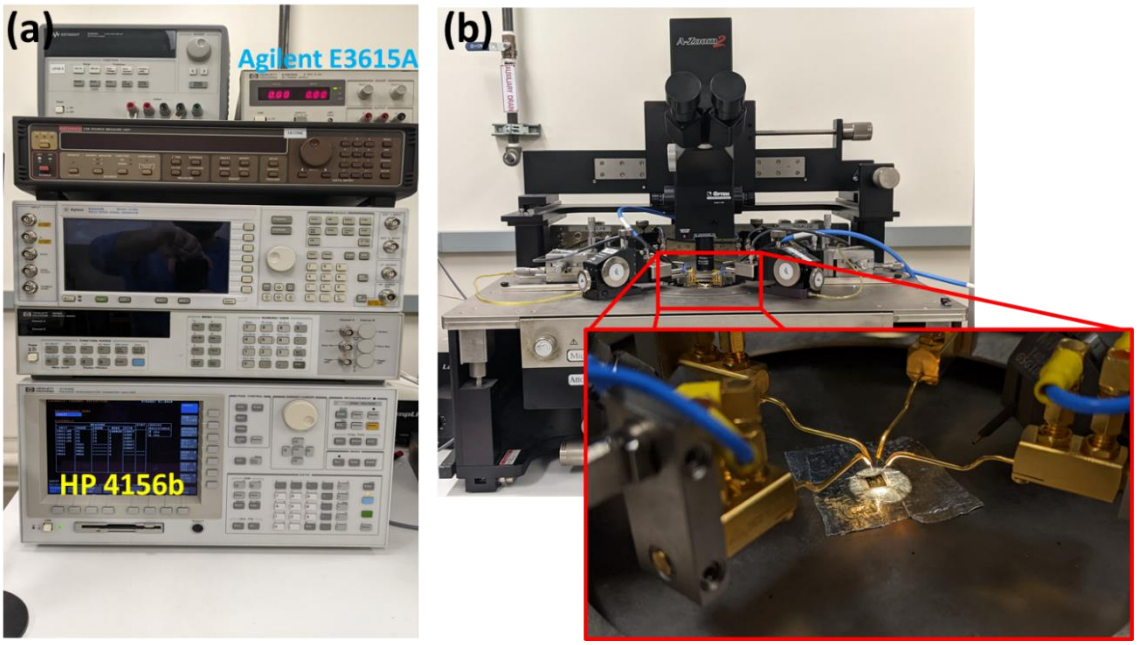
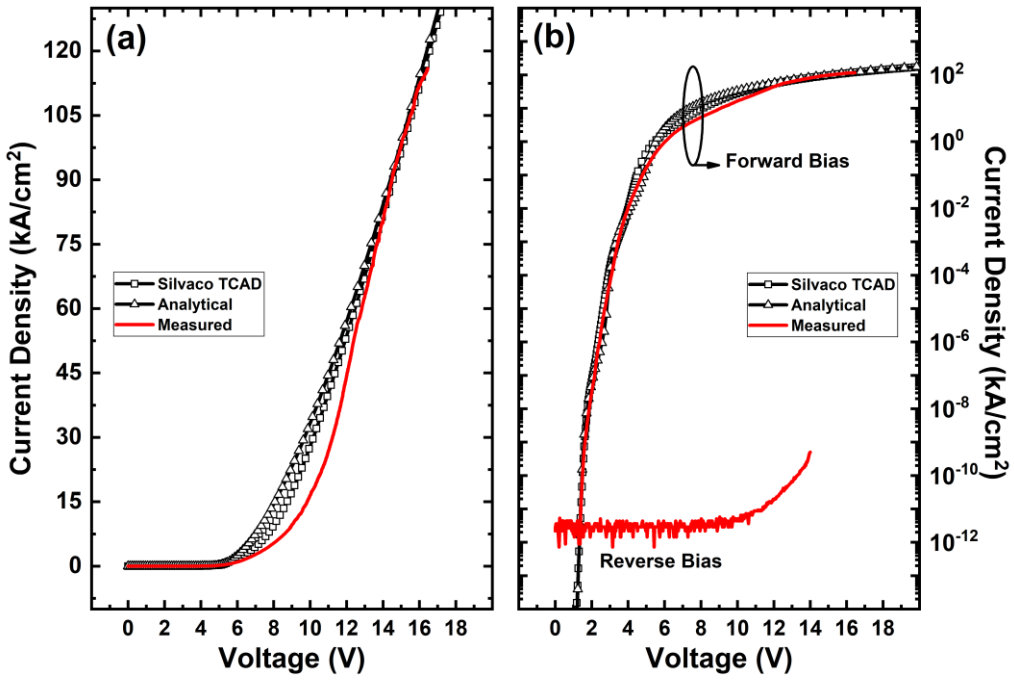


Fig. 3.2 (a) 4156b low noise DC semiconductor parametric analyzer and Agilent E3615A high current source meter (b) Two-probe Cascade probe station

The pulsed J-V measurements have a higher noise floor at low voltages and are therefore meshed with the low noise dc J-V measurements to give low to high voltage J-V characteristics as shown in Fig. 3.3, compared to theory as discussed later. Both dc and pulsed J-V characteristics were measured at room temperature. A series parasitic resistance of 1.54Ω between the probe wires was also measured and compensated for in the diode measurements. As seen in Fig. 3.3, a current density of $\sim 116\ \mathrm{kA/cm^2}$ is measured at the cathode contact ($\phi = 38\ \mu m$) at $16.4\ V$ forward bias, the highest value reported to date to our knowledge. The reverse leakage current density (Fig. 3.3(b) and Fig. 3.3(c)) is extremely low and is limited by the instrument noise floor up to $11\ V$ reverse bias, after

which the leakage current starts increasing. Therefore, an on-off rectification ratio of $> 5.7 \times 10^{12}$ is obtained at $\pm$ 10 V. Other diodes on this sample showed a breakdown voltage of ~47 V or a breakdown field of ~1.6 MV/cm. This field is small compared to the theoretical value of 10 MV/cm [3.1]. However, the diamond diode fabricated in this research is optimized for forward bias operation. Experimental results are further analyzed in detail in Section 3.2.4.



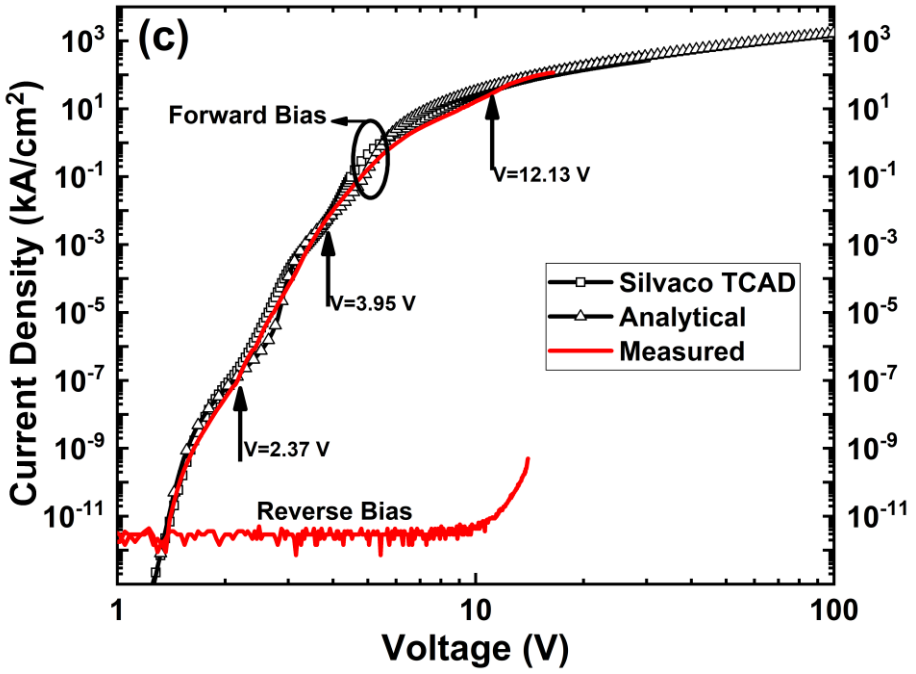


Fig. 3.3 Experimental forward and reverse linear (a) and logarithmic (b) J-V characteristics of diamond SPIND and forward bias curve-fits from both Silvaco ATLAS simulations and the analytical model. The arrows in log-log plot (c) indicate voltages at which the current jumps.

3.2.3 Theoretical Modelling

An analytical model including thermionic emission and space-charge limited current as well as numerical TCAD based Silvaco ATLAS simulations are used for the combined theoretical analysis of diamond SPINDs. The analytical model is important to provide a physical understanding of the dominant mechanism affecting the different regimes of the current – voltage characteristics, while ATLAS simulation provides a more exact model of charge transport in the diode including additional physics based on the inclusion of real material parameters for diamond diodes in the theoretical modelling. The entire scope of physical models used in this research is detailed in the following subsections.

3.2.3.1 Trap Levels in Diamond

Diamond growth and processing is still in the early stages of development and is not as mature as GaN or SiC. Hence defects and traps in CVD grown diamond are expected. Trap levels within the bandgap are particularly detrimental to diode operation because a fraction of the carriers is trapped, leading to an increase in the diode turn-on voltage, V_T, and on-state resistance as shown later. The effect of trap levels on the diamond SPIND J-V characteristics is discussed in more detail in Section 3.2.4. An exhaustive research on diamond defects, however, has not been reported, and therefore a consolidated view of defect associated trap levels within the diamond bandgap is hard to establish. Table 3.1 summarizes a few sources from the literature that describe trap activation levels, trap densities and other trap associated parameters typically found in synthetic lab-grown un-doped diamond.

Ref.	**Trap/ Activation Energy Level (eV)**	**Trap Density (cm^{-3})**	**Trap Energy Density ($cm^{-3}eV^{-1}$)**	**Trap level cross-section (cm^2)**
[3.9]	0.39	-	-	-
[3.10]	0.2	-	10^{14} to 10^{17}	-
[3.11]	0.31	-	-	-
[3.12]	0.78, 0.6, 0.2	$\sim 10^{15}$	-	$1.2 - 5 \times 10^{-22}$
[3.13]	1.7 to 2	-	-	10^{-13} to 10^{-15}
[3.14]	1.23, 1.14, 0.39	10^{16}	-	4×10^{-13}, 9.5×10^{-14}, 0.32×10^{-19}

Table 3.1 Summary of trap level parameters in synthetic diamond found in literature

As can be seen from Table 3.1, trap energy levels range from 0.2 eV to 1.7 eV with typical trap densities of the order of $10^{16}/cm^3$. In the n-layer, the phosphorus (P) activation energy level is 0.43 eV to 0.63 eV [3.8]. Due to this high activation energy level, the P doping is incompletely ionized and can act as trapping centers. In our theoretical modeling, we assume donor trap energy levels (hole traps) within a 0.2 eV to 1.7 eV energy range and with trap densities from 10^{15} $/cm^3$ to $10^{17}/cm^3$ with uniform distribution throughout the n and i layers. These trap levels are "donor-like" in the sense that they are positively charged when un-occupied by electrons (or occupied by holes) and neutral when occupied by electrons (or un-occupied by holes). Specifics of the adopted multiple trap energy levels are summarized in Table 3.2 and will be discussed in detail in Section 3.2.4.

3.2.3.2 Analytical Model

The analytical modelling in the case of diamond diodes is based on charge continuity between the thermionic emission current of holes injected over the *p-i* junction barrier and space charge limited (SCL) currents in the *n* and *i* regions. The following sub-sections build the analytical model in detail.

3.2.3.2.a Space Charge Limited Condition in Diamond

In an intrinsic semiconductor region, such as the i-layer of a diamond p-i-n diode, the free carrier charge concentration due to thermionic emission is extremely low. Therefore, when a charge is injected into such a region, Poisson's equation can be written completely in relation to the injected charge as,

$$\frac{dF(x)}{dx} = \frac{qp(x)}{\epsilon} \tag{3. 2}$$

and current density may be written as,

$$J = q\mu p(x)F(x) \tag{3. 3}$$

where $p(x)$ is given as $p(x) = N_v \exp(-E_{Fp}/k_B T)$, where N_v is the valence band density of states, $F(x)$ is the electric field across the semiconductor region of width d, E_{Fp} is the Fermi level in the semiconductor region, k_B is the Boltzmann constant and T is the lattice temperature. Multiplying both sides of (3. 2) by $F(x)$ and substituting (3. 3) we obtain,

$$2F(x)\frac{dF(x)}{dx} = \frac{d[f(x)]^2}{dx} = \frac{2J}{\epsilon\mu} \tag{3. 4}$$

Integrating (3. 4) and using the boundary condition $V = \int_0^d F(x)dx$ we obtain,

$$J = \frac{9}{8}\epsilon\mu\frac{V^2}{d^3} \tag{3. 5}$$

which is the well-known Mott and Gurney square-law relation [3.16].

In the presence of doping and therefore thermally generated carriers in the semiconductor region, the space charge limited condition is established depending on the amount of injected charge, p_{inj}, in relation to the charge present, p_0, in the drift or space charge region and the transit time, t_t, of the injected charge in relation to the dielectric relaxation time, τ_d. For low levels of injection, $p_{inj} \ll p_0$ i.e., at low bias across the semiconductor region, the current conduction is predominantly Ohmic. The transit time given by the integration of charge carrier velocity $v(x)$ over the drift region of length d

i.e., $t_t = \int_0^d v^{-1}(x)\,dx$, is greater than the dielectric relaxation time $\tau_d = \epsilon/\sigma$, where ϵ is the relative permittivity and σ is the material conductivity. The injected charge has enough time to quickly redistribute and the charge neutrality is not disturbed. This means that p_0 is not altered by the injection of p_{inj} because the unbalanced charge that gives rise to and electric field is neutralized by the adjacent electrons. The net effect is a flow of injected holes into the semiconductor region from the injecting contact replacing the holes flowing out of the collecting contact and thereby causing no appreciable change in the hole concentration anywhere in the semiconductor region. Therefore, the following continuity equation is possible

$$q\frac{\partial(p_{inj}+p_0)}{\partial t} = -\nabla.J \tag{3. 6}$$

where the current density J can be given by

$$J = q(p_{inj}+p_0)\mu F - qD_p\nabla(p_{inj}+p_0) \tag{3. 7}$$

where F is the electric field generated by the injected carrier, p_{inj}, and D_p is the diffusion constant. Substituting (3. 2) into (3. 7) and (3. 6) and ignoring second-order terms involving $p_{inj}F$, we obtain

$$\frac{\partial p_{inj}}{\partial t} = -\left(\frac{qp_{inj}\mu}{\epsilon}\right)p_{inj} + D_p\nabla^2 p_{inj} \tag{3. 8}$$

If $p_{inj} < p_0$, the injected charge spreads over the semiconductor region within the dielectric relaxation time τ_d. Therefore, integrating (3. 8) we obtain the solution as

$$p_{inj}(t) = p_{inj}(t=0)\exp\left(-\frac{t}{\tau_d}\right) \tag{3. 9}$$

Therefore, for $t_t > \tau_d$, negligible space charge would be present in the semiconductor region.

However, at higher biases when the injected charge is significantly more than the charge present in the drift region i.e., $p_{inj} \gg p_0$, t_t becomes very small and the $D_p\nabla^2 p_{inj}$ term in (3. 8) can no longer be neglected. Although, τ_d also decreases with increased conductivity because of the injected charge, in situations where $t_t < \tau_d$, there is not enough time for the charge to redistribute and charge neutrality is greatly disturbed in the drift region. This can be seen from Fig. 3.5 where t_t becomes increasingly smaller than τ_d with bias across a semiconductor region at a given level of injection. τ_d decreases for higher levels of the free carriers, p_0, present in the semiconductor, thereby delaying the space charge limited condition to larger applied bias.

The onset of the SCL conduction as it departs from an Ohmic conduction can be seen from the voltage at which the Ohmic and SCL currents become equal i.e.,

$$qp_0\mu\frac{V}{d} = \frac{9}{8}\epsilon\mu\frac{V^2}{d^3} \tag{3. 10}$$

$$\therefore V_\Omega = \frac{8}{9}\left(\frac{qp_0d^2}{\epsilon}\right)$$

This can be qualitatively seen from Fig. where the current transitions between the two regions, as has been shown in [3.15].

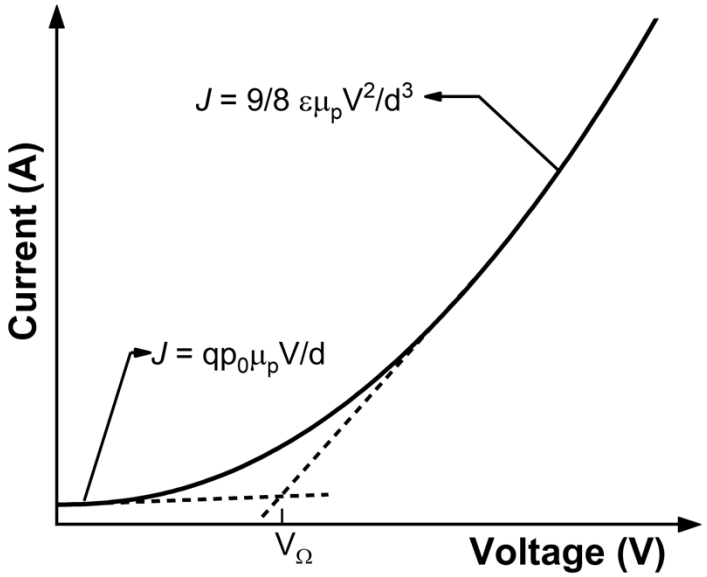


Fig. 3.4 Transition from Ohmic to Mott-Gurney SCL conduction

In the case of a diamond SPIND i-region, the intrinsic carrier concentration is extremely low ($\sim 10^{-27}\ /cm^3$) and a p-type background doping of $\sim 4 \times 10^{14}\ /cm^3$ in the i-region with an incomplete ionization of B (E_A = 0.413 eV [3.17]) produces $\sim 10^{13}\ /cm^3$ free holes. Therefore, the charge present in the i-layer is very low, and very soon after holes are thermionically emitted over the p-i junction barrier, charge accumulation in the i-region increases and the electric field in the drift region is no longer uniform.

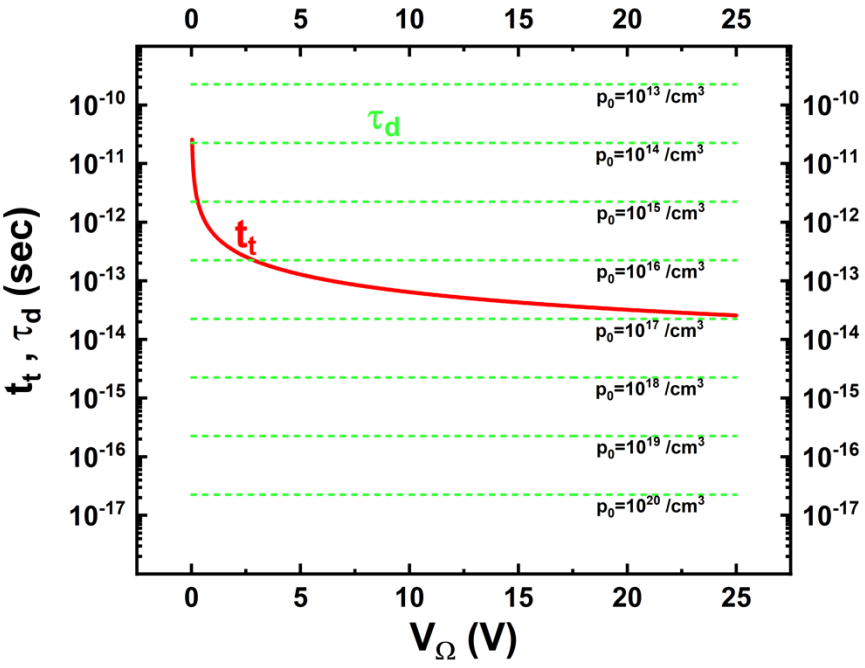


Fig. 3.5 Transit time t_t as a function of bias applied V_Ω across a semiconductor region in comparison to varying dielectric relaxation time τ_d for different levels of free carriers p_0 present in the semiconductor

3.2.3.2.b SCL Current Numerical Model

The current – voltage characteristics limited by SCL conduction are non-linear and non-exponential as given by the Mott-Gurney square law in (3. 5). However, the presence of traps modifies the simple SCL current description of the Mott-Gurney equation. For an exponential distribution of traps (e.g., a band tail), the Mark and Helfrich [3.18] equation gives the SCL current for holes as

$$J = \frac{\mu_p N_v}{q^{l-1}} \left(\frac{2l+1}{l+1}\right)^{l+1} \left(\frac{l}{l+1}\frac{\epsilon\epsilon_0}{H_b}\right)^{l} \left(\frac{V^{l+1}}{d^{2l+1}}\right) \tag{3.11}$$

where N_v is the density of states in the valence band, $l = k_B T_C / k_B T$ where T_C is the characteristic temperature of trap distribution and H_b is the trap density of states parameter.

The Mark-Helfrich equation (3.11) is a simplified form of the total current density assuming the trapped charge p_t is always greater than the injected charge p. In diamond SPINDs, $p < p_t$ is true only for low voltages and the assumption does not hold for higher voltages where the hole injection levels are comparable or greater than the trapped charges. Therefore, we follow the method adopted by Jain et. al [3.19] for multiple discrete trap levels. Here we consider three single level traps (corresponding to the three 'jumps' in the log J – log V curve in Fig. 3.3(c)), with H_1, H_2 and H_3 trap densities and E_{t_1}, E_{t_2} and E_{t_3} trap energy levels respectively distributed uniformly in the *n* and *i* regions (i.e. total drift region) of the diamond SPIND. Poisson's equation with both trapped and free holes is given by

$$\frac{dF(x)}{dx} = \frac{q[p(x) + p_t(x)]}{\epsilon} = \frac{\rho}{\epsilon} \tag{3.12}$$

The trap distribution in energy can be given as

$$h(E) = H_1 \delta(E - E_{t1}) + H_2 \delta(E - E_{t2}) + H_3 \delta(E - E_{t3}) \tag{3. 13}$$

where δ is the Dirac-delta function. The number of filled traps at a given voltage can be obtained by

$$p_t(x) = \int_{-\infty}^{\infty} \frac{H_1\delta(E - E_{t1}) + H_2\delta(E - E_{t2}) + H_3\delta(E - E_{t3})}{1 + \exp\left(\frac{E_f(x) - E}{k_B T}\right)} dE \tag{3. 14}$$

where $E_f(x)$ is the difference between the valence band and Fermi level and depends on x due to band bending. (3.17) can be simplified to

$$p_t(x) \approx \frac{H_1}{1 + \exp\left(\frac{E_f(x) - E_{t1}}{k_B T}\right)} + \frac{H_2}{1 + \exp\left(\frac{E_f(x) - E_{t2}}{k_B T}\right)} + \frac{H_3}{1 + \exp\left(\frac{E_f(x) - E_{t3}}{k_B T}\right)} \tag{3. 15}$$

Substituting for $p(x)$ from (3. 3) and equation (3.19) in the Poisson equation (3.12), we get

$$\frac{dF(x)}{dx} = \frac{J}{q\mu_p F} + \frac{H_1}{1 + \frac{\theta_1 q\mu_p F}{J}} + \frac{H_2}{1 + \frac{\theta_2 q\mu_p F}{J}} + \frac{H_3}{1 + \frac{\theta_3 q\mu_p F}{J}} \tag{3. 16}$$

where $\theta_n = N_v \exp(-E_{t_n}/(k_B T))$. Therefore, the electric field $F(x)$ can be integrated over the drift region extending from $x = 0$ to $x = d$, to obtain

$$\int_0^d dx = \int_{F_{x=0}}^{F_{x=d}} \left(\frac{J}{q\mu_p F} + \frac{H_1}{1 + \frac{\theta_1 q\mu_p F}{J}} + \frac{H_2}{1 + \frac{\theta_2 q\mu_p F}{J}} + \frac{H_3}{1 + \frac{\theta_3 q\mu_p F}{J}} \right)^{-1} dF(x) \tag{3.17}$$

where k_B is the Boltzmann constant, μ_p is the hole mobility, J is the current density given by continuity equation $J = q\mu p(x)F(x)$ and $F_{x=0}$ and $F_{x=d}$ is the electric field at the p^+ edge and Schottky contact, respectively. Assuming $F_{x=0} = 0$, the J-V characteristics can be obtained by numerically integrating (3.17) to solve for $F_{x=d}$ and using the boundary condition

$$V_{SCL} = \int_0^d F(x)dx \tag{3.18}$$

where, V_{SCL} is the voltage across the space charge limited portion of the device, as illustrated in Fig. 3.6. Determining E_t and H for each trap level requires additional experimental methods like photoluminescence or electroluminescence which are beyond the scope of this paper. Attempts were made to employ the "differential" method proposed by Nešpůrek [3.20] for characterizing trap energy levels and density by analyzing experimental and modeled diamond SPIND J-V characteristics, but all attempts were unsuccessful. However, following the analysis in [3.19], we determined the number of single trap levels by observing the number of "jumps" in the log-log plot of measured J-V characteristics as indicated in Fig. 3.3(c). We observe three points in the measured log-log J-V characteristics where the current jumps or changes slope suddenly and conclude the number of single trap levels to be three. As discussed in Section 3.2.4, using three single trap energy levels in the range 0.2 eV to 1.7 eV and trap densities between 10^{14} –

10^{17} $/cm^3$ as obtained from literature discussed in Section 3.2.3.1, J-V characteristics are reproduced from theoretical models to match the measured characteristics with a high degree of accuracy.

3.2.3.2.c Thermionic Emission Current and Bisectional Algorithm

The caveat to using the analysis in [3.19] for reproducing the measured J-V characteristics of diamond SPINDs is that the thermionic emission (TE) of holes over the p-i-n junction barrier needs to be considered in conjugation with the SCL conduction, i.e. one or the other limits the current, as well as ultimately contact resistance. As shown later in Fig. 3.9, the barrier for hole injection into the n-layer and eventually to the cathode contact is about 2.1 eV at zero bias thermal equilibrium. At sufficiently high forward bias, hole injection into the i and n layers is sufficiently large that SCL conditions are established, and the current becomes limited by this mechanism. Therefore, we model the TE current as being in series to the SCL current as shown in Fig. 3.6, where the TE current is given by

$$J_{TE} = A^* T^2 \exp\left(\frac{-\phi}{\eta k_B T}\right)\left((\exp\left(\frac{V_{TE}}{\eta k_B T}\right) - 1\right) \tag{3.19}$$

where A^* is the Richardson's constant, T is lattice temperature, ϕ is the hole injection barrier, η is the diode ideality factor and V_{TE} is voltage drop across the thermionic emission region as shown in Fig. 3.6. The voltage drop across each of the two series "current sources" is not the same as current has to be conserved. To obtain the total J-V characteristics, we employ a bisectional algorithm by finding roots (corresponding

voltages) to the continuous function of current. A specific contact resistance R_{ser} ($\Omega.cm^2$) is also added in series to the two current sources, as shown in Fig. 3.6. R_{ser} accounts for both contact and p^{++} layer bulk resistances. The ideality factor η in (3.19) corresponds only to the thermionic emission part of the total current and is set equal to 1 assuming only hole injection over the p-i-n junction. The ideality factor of the total current, however is larger and depends on the trap levels and densities as will be seen in Section 3.2.4.

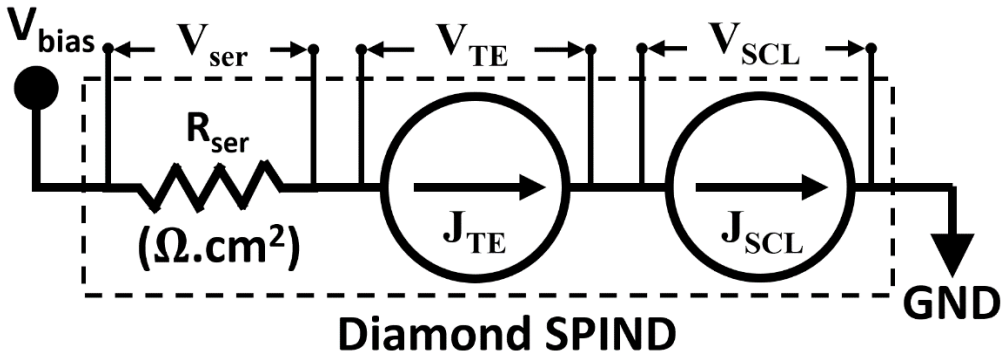


Fig. 3.6 Analytical equivalent circuit model of the diamond SPIND which is solved by a bisectional algorithm

3.2.3.3 Silvaco ATLAS TCAD Model

Silvaco ATLAS TCAD simulations were performed to gain deeper understanding of transport in diamond SPINDs. The advantage to TCAD simulations is that they numerically solve the coupled field and semiconductor (self-consistent Poisson and drift-diffusion) equations using finite elements methods over a 2D domain inclusive of thermionic emission, SCL currents, and series resistance effects, without the simplifying 1D domain decomposition of the problem shown in the analytical model of Fig. 3.6. Further, physical models of incomplete ionization, hopping mobility, field-dependence of mobility, carrier

velocity saturation and effect of traps can be implemented and the charge transport can be studied in detail by observing spatial distribution of hole injection levels, mobility variations, field variations etc. throughout the diode structure at different bias points.

The ATLAS device structure was constructed according to the diamond SPIND cross-section shown in Fig. 3.1(a). A metal work function ϕ_m of 4.5 eV (Ti ≈ 4.33eV) was assumed at the cathode contact, creating a Schottky contact to the n-layer. Phosphorus doping in the n-layer is set at $3 \times 10^{17}/cm^3$ while a background n-type doping of $10^{14}/cm^3$ and p-type doping of $4 \times 10^{14}/cm^3$ is assumed in both *n* and *i* layers. The $50\ nm$ thick n-layer in the SPIND structure is completely depleted by the Schottky contact on one side and the p-i-n junction depletion from the other side. The SPIND i and n thicknesses were fixed following the low-voltage SPND design principles stated in [3.5]. Fig. 3.9 shows a band diagram of the simulated diamond SPIND under various bias conditions, discussed in more detail later. The following subsections give brief descriptions of all the physical models used in the ATLAS simulations.

3.2.3.3.a Incomplete Ionization

P and B impurities in diamond have high activation energies and are therefore expected to be incompletely ionized at room temperature. At thermal equilibrium, the Fermi level is constant and the Poisson equation in a charge neutral semiconductor region can be written as

$$n + N_A^- = p + N_D^- \tag{3. 20}$$

The intrinsic carrier concentration can be related to the n and p thermally generated free charge carriers as

$$n_i^2 = n.p \tag{3. 21}$$

or

$$n_i^2 = N_C N_V \exp\left(-\frac{E_g}{k_B T}\right) \tag{3. 22}$$

i.e.,

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{E_g}{2k_B T}\right) \tag{3. 23}$$

Substituting (3. 21) in (3. 20), the n concentration in a n-type material can be obtained as

$$n = \frac{1}{2}\left[N_D^+ - N_A^- + \sqrt{(N_D^+ - N_A^-)^2 - 4n_i^2}\right] \tag{3. 24}$$

and similarly, the p concentration in a p-type material can be obtained as

$$p = \frac{1}{2}\left[N_A^- - N_D^+ + \sqrt{(N_D^+ - N_A^-)^2 - 4n_i^2}\right] \tag{3. 25}$$

The ionized impurity concentration is given by the steady-state Gibbs distribution as,

$$N_D^+ = \frac{N_D}{1 + g_D \frac{n}{n_D}} \text{ where } n_D = N_C \exp\left(-\frac{E_C - E_D}{k_B T}\right) \tag{3. 26}$$

and

$$N_A^- = \frac{N_A}{1 + g_A \frac{p}{p_A}} \text{ where } p_A = N_V \exp\left(-\frac{E_A - E_V}{k_B T}\right) \quad (3.27)$$

where p,n are free carrier hole and electron concentrations, N_A and N_D are acceptor and donor concentrations, $g_A = 4$ and $g_D = 0.5$ are valence band (E_V) and conduction band (E_C) degeneracy factors and E_A and E_D are acceptor and donor activation energies. Therefore, an incomplete ionization ratio η can be obtained from (3. 24) or (3. 25) as

$$\eta_D = \frac{N_D^-}{N_D} = \frac{\left(-n_D + \sqrt{n_D^2 + 4N_D n_D}\right)}{2N_D} \quad (3.28)$$

and

$$\eta_A = \frac{N_A^-}{N_A} = \frac{\left(-p_A + \sqrt{\mathrm{p_A^2} + 4N_A p_A}\right)}{2N_A} \quad (3.29)$$

The activation energy of P is fixed at 0.57 eV [3.21], [3.22] while a Pearson and Bardeen model [3.23] of the doping dependent activation energy has been adopted for B, given as

$$E_A = 0.416 - 5.4329 \times 10^{-8} N_A^{\frac{1}{3}} \quad (3.30)$$

This gives an activation energy of 0.41 eV for $N_A = 4 \times 10^{14}/cm^3$ (background *n* and *i*-layer doping), 0.362 eV for $N_A = 1 \times 10^{18}/cm^3$, 0.052 eV for $N_A = 3 \times 10^{20}/cm^3$ and approaches zero at metallic-insulator transition of $N_A = 4.5 \times 10^{20}/cm^3$. Therefore, the incomplete ionization ratio for B doping η_A becomes a function of the doping concentration shown as follows

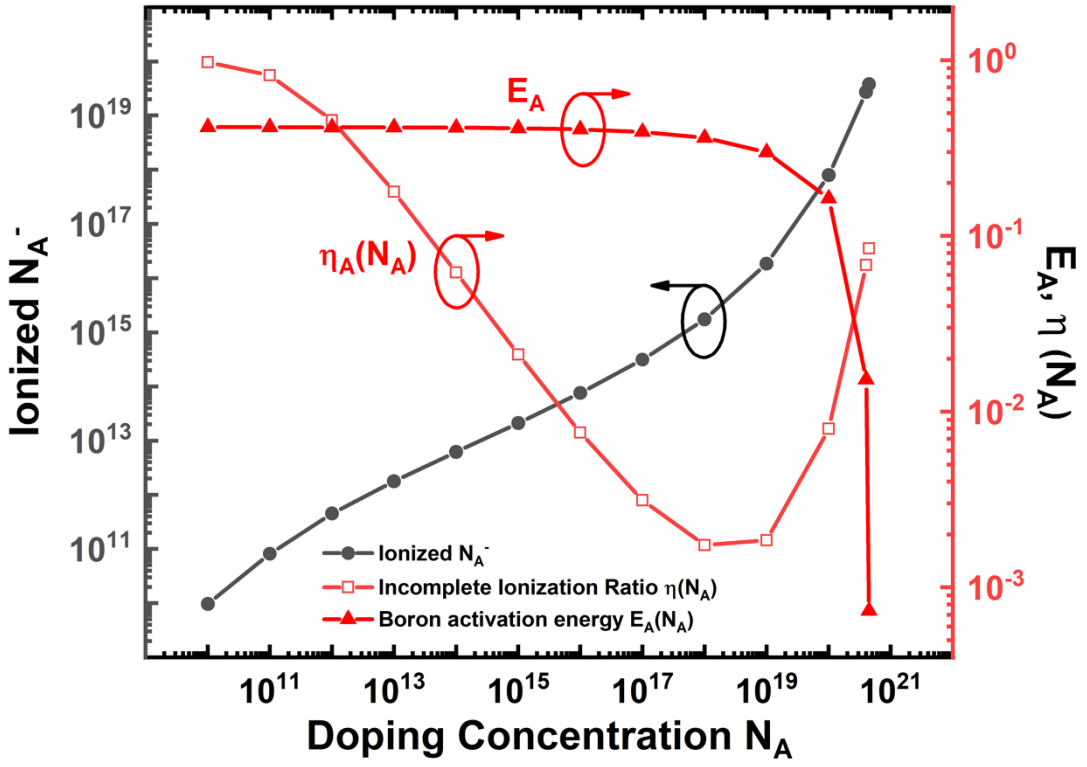


Fig. 3.7 Ionized B concentration N_A^-, doping dependent B activation energy E_A and doping concentration dependent B incomplete ionization ratio $\eta_A(N_A)$ as a function of B doping concentration

3.2.3.3.b Hopping Mobility

Considering heavy B doping in p^+ layer and expected high levels of hole injection into the drift layer (i + n layer) at high forward biases, variable range hopping (VRH) mobility was implemented following VRH formulation done in [3.6], [3.17], [3.24]. The equivalent hole mobility $\mu_{p,eq}$ is a combination of an empirical temperature and concentration dependent mobility $\mu_T(T, N)$ and VRH mobility (μ_{VRH}) given as follows,

$$\mu_{p,eq} = \mu_T(T, N_{imp}) + \left(\frac{p_{hop}}{p}\right)\mu_{VRH} \tag{3.31}$$

$$\mu_{VRH} = \frac{qR_{1/4}^2}{k_B T} v_{ph} \exp\left[-\left(\frac{T_{1/4}}{T}\right)^{1/4}\right] \tag{3.32}$$

$$\mu_{VRH} = \frac{qR_{1/4}^2}{k_B T} v_{ph} \exp\left[-\left(\frac{T_{1/4}}{T}\right)^{1/4}\right] \tag{3.33}$$

$$R_{1/4} = \left(\frac{9}{8\pi\alpha k_B T g_F}\right)^{1/2} \tag{3.34}$$

$$R_{1/4} = \left(\frac{9}{8\pi\alpha k_B T g_F}\right)^{1/2} \tag{3.35}$$

$$T_{1/4} = \frac{\beta\alpha^3}{g_F k_B} \tag{3.36}$$

$$g_F = \frac{\kappa}{q^2}\left(\frac{3N_A}{4\pi}\right)^{1/3} \tag{3.37}$$

where $N_{imp} = N_A + N_D$, $p_{hop} = N_A - p$ is the hopping hole concentration, $\alpha^{-1} = 1\ nm$ (assumed for acceptor impurities), $\beta = 7.6$ [3.34], $v_{ph} = 2 \times 10^{13}\ s^{-1}$ and $\kappa = 5.7$ is the dielectric constant for diamond. The empirical mobility μ_T is given by,

$$\mu_T(T, N_{imp}) = \mu(300, N_{imp}) \times \left(\frac{T}{300}\right)^{-\beta(N_{imp})} \tag{3.38}$$

$$\beta(N_{imp}) = \beta_{min} + \frac{\beta_{max} + \beta_{min}}{1 + \left(\frac{N_{imp}}{N_\beta}\right)^{\gamma_\beta}} \tag{3.39}$$

$$\mu(300, N_{imp}) = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_{imp}}{N_{\mu}}\right)^{\gamma_{\mu}}} \tag{3.40}$$

where $\beta_{min} = 0$, $\beta_{max} = 3.11$, $N_{\beta} = 4.1 \times 10^{18}\ cm^{-3}$, $\gamma_{\beta} = 0.617$, $N_{\mu} = 3.25 \times 10^{17}\ cm^{-3}$, $\gamma_{\mu} = 0.73$ and $\mu_{min} = 0\ cm^2/V.s$. A maximum mobility of $\mu_{max} = 2100\ cm^2/V.s$ [3.1] is implemented to give an equivalent mobility μ_{eq} of $\sim 14\ cm^2/V - s$ at $N_A = 3 \times 10^{20}\ cm^{-3}$ in the p^+ region and $\sim 2082\ cm^2/V.s$ in the i region where $N_A = \sim 4 \times 10^{14}/cm^3$ and $N_D = \sim 10^{14}/cm^3$. Hole mobility in the n region is maximum at $2100\ cm^2/V - s$.

Although diamond SPIND is mostly unipolar hole conduction, equivalent electron mobility is implemented in a similar fashion by combining $\mu_T(T, N)$ and nearest neighbor hopping (NNH) mobility given as

$$\mu_{n,eq} = \mu_T(T, N_{imp}) + \left(\frac{n_{hop}}{n}\right)\mu_{hop,NNH} \tag{3. 41}$$

$$\mu_{hop,NNH} = \frac{qR_{hop}^2}{6k_B} v_{ph} \exp\left(-2\alpha R_{hop} - \frac{qW_{hop}}{k_B T}\right) \tag{3. 42}$$

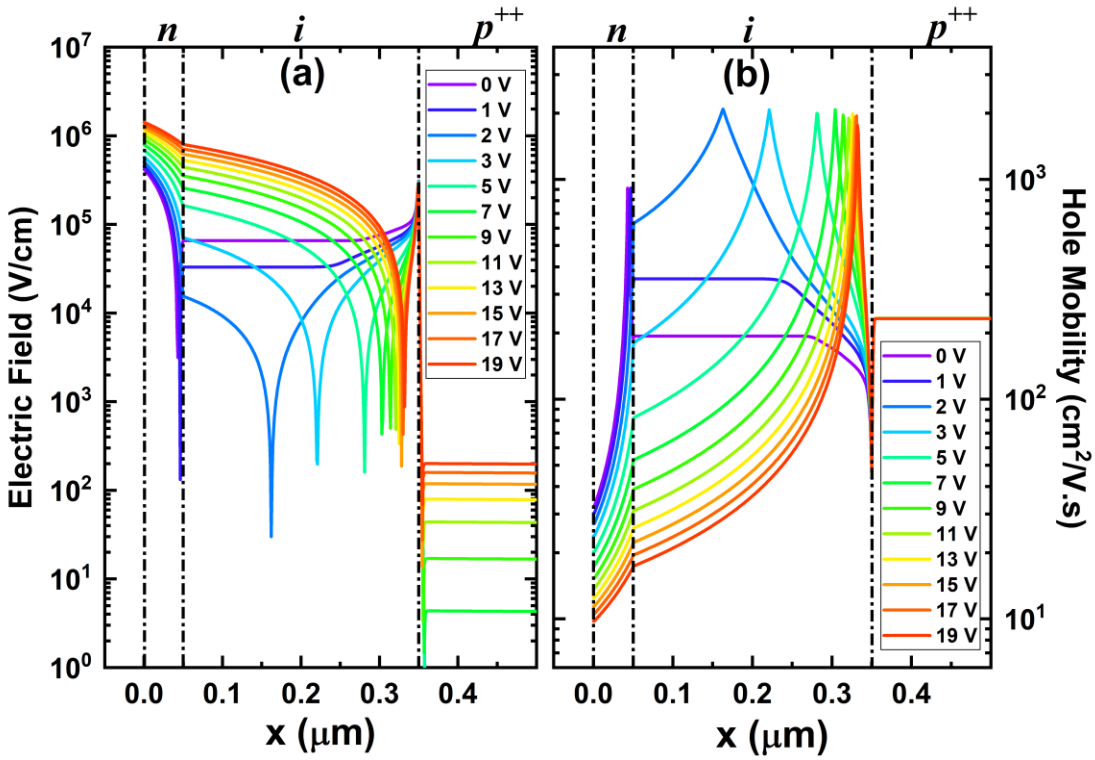
where $\mu_{hop,NNH}$ is the NNH mobility for electrons and n_{hop} is the hopping carrier concentration given by $n_{hop} = N_D - n$ where n is the free electron charge concentration. The localization length of the wave function α^{-1} is 1.8 nm for n-type doping [3.6] while $W_{hop} = 51\ meV$ is the thermal activation energy for the hoping process, $R_{hop} = N_D^{-\frac{1}{3}}$ is the average distance between n-type impurities and $v_{ph} = 2 \times 10^{11} s^{-1}$ is the phonon

frequency factor [3.17]. Maximum electron mobility is $1060\ \mathrm{cm^2/V-s}$. Both hole and electron equivalent mobilities are implemented in Silvaco ATLAS with a C-language interpreter function.

3.2.3.3.c Field-dependent Hole Mobility

At zero bias, high electric fields exist in the fully depleted *n* and *i* layers. As the diode is forward biased, the Schottky – n-region diode becomes increasingly reverse biased. Therefore, with increasing forward bias, the peak electric field increases at the Schottky contact and increases the width of the drift region (i + n layers) over which the Schottky induced electric field is high (Fig. 3.8(a)). The p-i depletion associated peak electric field and its spread in the i-layer decreases as the diode is increasingly forward bias. As a result, the hole velocity saturates in the depletion area where the electric field is high (Fig. 3.8(c)). Consequently, the area over which the hole mobility drops to low levels increases, as shown in Fig. 3.8(b). The model for the field-dependence of the mobility is described in Silvaco ATLAS based on the well-known Caughey and Thomas expression [3.26], given as

$$\mu_p(E) = \mu_{p0}\left[\frac{1}{1+\left(\frac{\mu_{p0}E}{v_{sat}}\right)^{1/\beta_p}}\right]^{1/\beta_p} \tag{3.43}$$


n
i
p++
(a)
(b)
Electric Field (V/cm)
Hole Mobility (cm²/V.s)
x (μm)
0 V
1 V
2 V
3 V
5 V
7 V
9 V
11 V
13 V
15 V
17 V
19 V

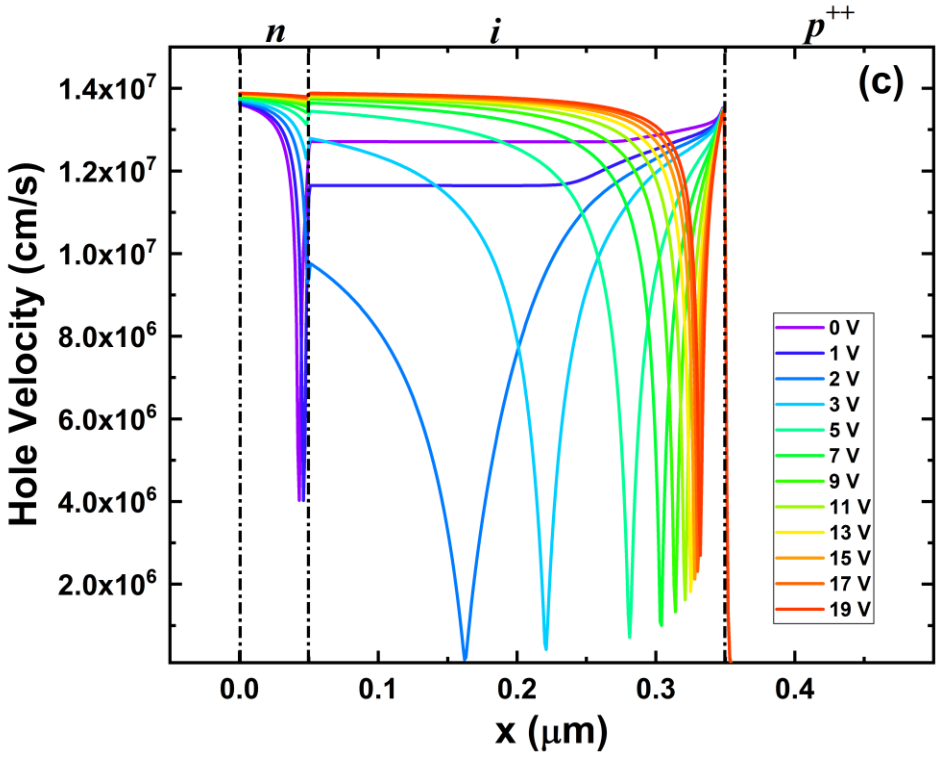


Fig. 3.8 Spatial distribution of (a) electric field, (b) hole mobility and (c) hole velocity throughout the n and i layers of the ATLAS simulated SPIND as a function of increasing forward bias

$\mu_{p,eq}$ as described in equation (3.38) is assumed to be the low-field mobility while $v_{sat} = 1.4 \times 10^7\ cm/s$ [3.1] is the hole saturation velocity. The effect of field-dependence of hole mobility on diamond SPIND J-V characteristics will be examined in Section 3.2.6.

3.2.3.3.d Trap Parameters and Shockley-Reed-Hall Recombination

As discussed in Section 3.2.3.2.b and as will be examined in Section 3.2.4, three single level traps were implemented with a uniform density throughout the drift layer constituting of both the n and i layers. Trap levels in the bandgap greatly affect carrier dynamics because of added recombination processes that can be described by unipolar Shockley-

Read-Hall (SRH) statistics in the presence of multiple donor-like traps given by the total recombination term described in [3.27], [3.28], [3.29], given as

$$R = \sum_{\alpha=1}^{l} R_{D_\alpha} \tag{3.44}$$

where $l = 3$ is the number of donor-like traps and the recombination term R_{D_α} is given by,

$$R_{D_\alpha} = \frac{(pn - n_i^2)}{\tau_n \left[p + g n_i \exp\left(\frac{E_i - E_{t_\alpha}}{k_B T}\right)\right] + \tau_p \left[n + \frac{1}{g} n_i \exp\left(\frac{E_{t_\alpha} - E_i}{k_B T}\right)\right]} \tag{3.45}$$

where n_i is the intrinsic carrier concentration of diamond with a value of [$\sim 10^{-27}$], p and n are free hole and electron concentrations respectively, E_{t_α} is the respective trap energy level, $g = 1$ is the trap degeneracy factor and the electron and hole lifetimes τ_n and τ_p are related to the carrier capture cross sections α_n and α_p through equations $\tau_n = 1/(\alpha_n v_n H_\alpha)$ and $\tau_p = 1/(\alpha_p v_p H_\alpha)$, where H_n is the trap density and v_n, v_p are electron and hole thermal velocities calculated as $v_n = 3k_B T/(m_n^* m_0)^{1/2}$ and $v_p = 3k_B T/(m_h^* m_0)^{1/2}$, respectively. m_n^* and m_h^* are electron and hole effective masses with values 0.55 and 0.908 [3.32], [3.33], respectively.

Table 3.2 compares the trap levels and densities used in both the analytical model and TCAD simulations. For best curve-fitting to measured data, the trap levels remain the same for both models but the analytical model fits to slightly different trap densities.

Parameter	Analytical	Silvaco ATLAS TCAD
E_{t1}, E_{t2}, E_{t3} (eV)	0.7, 0.45, 0.25	0.7, 0.45, 0.25
H_1, H_2, H_3 $(/cm^3)$	8.6×10^{15}, 1.5×10^{16}, 6×10^{16}	1.25×10^{16}, 8×10^{15}, 2.2×10^{16}
α_p (cm^2)	-	10^{-19}
Trap degeneracy factor	-	1
v_{psat} (cm/s)	-	1.4×10^7

Table 3.2 Parameters used in analytical and Silvaco ATLAS TCAD simulations

3.2.4 Analytical and Silvaco ATLAS Curve-Fitting

Logarithmic and linear plots of the experimental J-V measurements are shown in Fig. 3.3 along with both the analytical and ATLAS J-V characteristics in forward bias, which are both in good agreement with the measured data. The values of all three trap energy levels E_{t1}, E_{t2} and E_{t3} and their trap densities H_1, H_2 and H_3 respectively along with their associated parameters in both the analytical and ATLAS models are varied to curve-fit the simulated J-V characteristics to measured data and are summarized in Table 3.2. There are slight discrepancies in the curve-fitting results, especially when the measured current is lower than the simulated current. These discrepancies can possibly be attributed to trapping – de-trapping within the pulse-width duration during pulsed J-V measurements. Transient effects are not considered in the theoretical modeling. Fig. 3.3(c) shows the log-log plots of both the measured and modeled J-V characteristics. The arrows in Fig. 3.3(c) indicate three distinct places where the current “jumps” or changes slope suddenly. The

approximate corresponding voltages to these jumps are at $V_1 = 2.37\ V$, $V_2 = 3.95\ V$ and $V_3 = 12.13\ V$. As discussed earlier, these jumps in current indicate three distinct trap levels in the bandgap.

Fig. 3.9(a) shows the ATLAS simulated band diagram including the trap and Fermi levels. At zero bias, all hole trap levels at E_{t1}, E_{t2} and E_{t3} are empty over most of the drift region. As the forward bias is increased beyond 2.37 V to $V_{fb} = 2.5\ V$, the deepest trap level $E_{t1} = 0.75\ eV$ is just filled as the hole quasi-Fermi level dips below it (Fig. 3.9(b)). At voltages just prior to 2.37 V, part of the holes injected over the p-i junction are used to fill all the trap density of states at 0.7 eV.

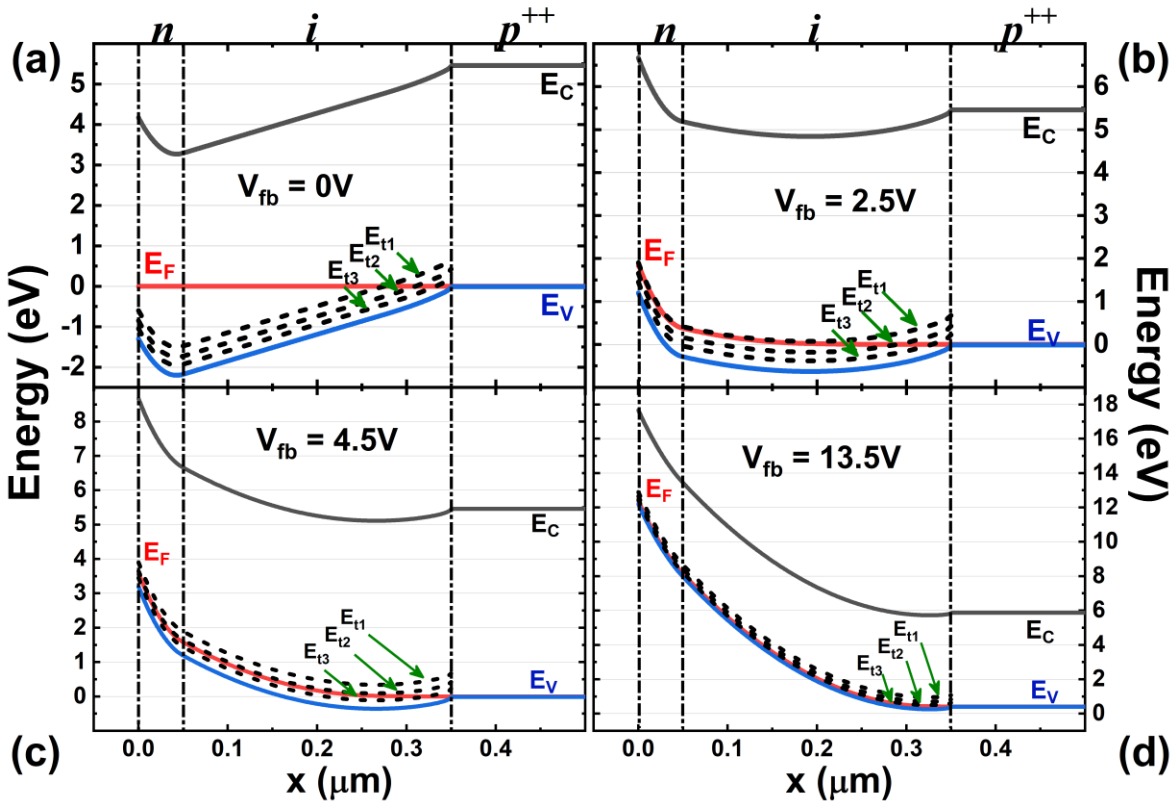


Fig. 3.9 Silvaco ATLAS simulated band diagrams of the diamond SPIND at different forward biases (a) through (d) show the Fermi level E_F dipping just below each trap level E_{t1}, E_{t2} and E_{t3} at voltages just above V_1, V_2 and V_3, respectively.

Once all the trap density of states are filled at 0.7 eV, all the injected holes are available for conduction, and we see a sudden jump in current. Similarly, we see jumps in current when the hole quasi-Fermi level dips below $E_{t2} = 0.45\ eV$ and $E_{t3} = 0.25\ eV$ as shown in Fig. 3.9(c) and Fig. 3.9(d), where the applied forward biases are 4.5 V and 13.5 V, respectively. Based on ATLAS simulations, the following observations are made.

3.2.5 SCL Condition and Hole Injection

The analytical model allows us to observe individual components of the forward

current i.e., thermionic emission current and SCL current with and without traps. In a diamond SPIND, due to the extremely low intrinsic carrier concentration and low background charge, the transition in voltage from thermionic to SCL conduction occurs without an intermediate regime of Ohmic conduction. The SCL condition is established within a few volts after TE emission of holes over the p-i junction barrier. This can be observed from ATLAS simulation plots of the injected hole concentration levels shown in Fig. 3.10(a) and normalized charge concentration (normalized remnant charge from the charge neutrality $p - N_A + N_D - n$) in the i-layer from Fig. 3.10(b).

The charge accumulation increases exponentially from $1\,V$ to $2\,V$ as the holes are thermionically emitted over the junction barrier (Fig. 3.10(a)). Beyond $\sim 2\,V$ forward bias, the charge increases proportional to V^m where $m \geq 1$. For a trap-free case, we can see current – voltage characteristics starting to deviate from the TE exponential relation towards a space charge limited Mott – Gurney relation in Fig. 3.12(a) at a forward bias of $\sim 1.8\,V$. In the case of traps, part of the thermally generated hole concentration is trapped and therefore the transition from thermionic emission to space charge limited occurs even sooner in voltage, especially for deep level traps.

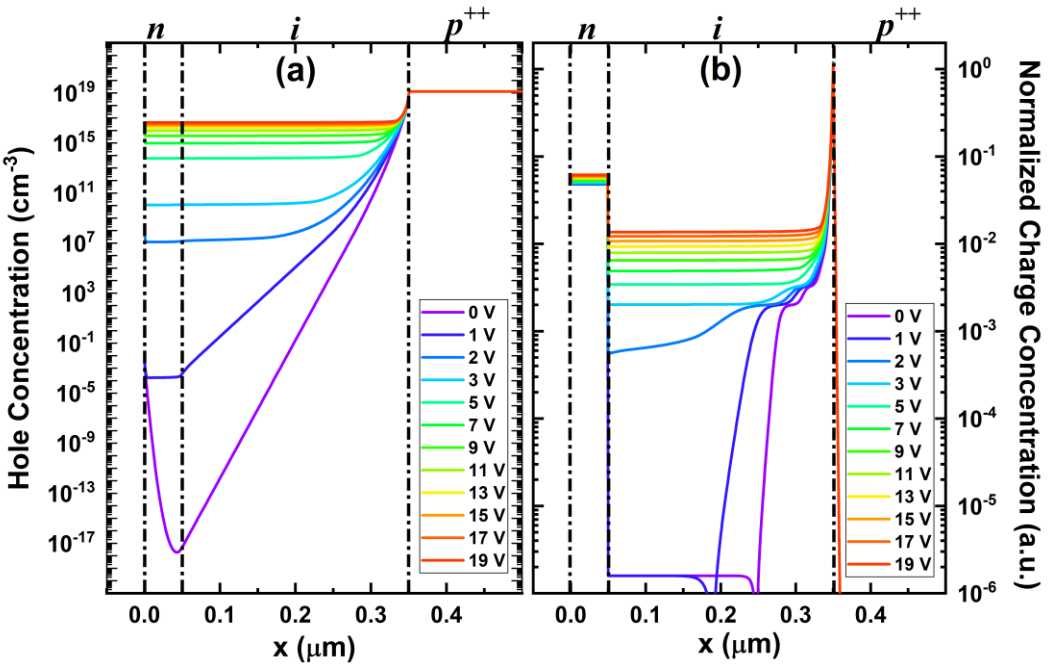


Fig. 3.10 (a) Hole concentration and (b) normalized charge concentration as obtained from diamond SPIND TCAD simulations at increasing forward bias. The sudden increase in charge concentration from 1 V to 2 V is accounted by the TE emission.

3.2.6 Velocity Saturation

With increasing forward bias, the Schottky – n-layer diode becomes more reverse biased and the Schottky depletion region spreads further into the i-layer. This can also be observed from the gradual change of band levels from discontinuous to continuous between the *n* and *i* layers with increasing forward bias voltage as shown in Fig. 3.9(a) through Fig. 3.9(d). As a result of the increasing Schottky – n-layer depletion region, an increasing area of the i-layer is under high electric field when the diode is in forward bias. This leads to the saturation of the hole velocity over an increasingly large area of the i-layer which in turn reduces the overall average mobility, as shown in Fig. 3.8. The overall effect of hole

velocity saturation in a diamond SPIND is the reduction of total diode current at a given forward bias, as shown in Fig. 3.11.

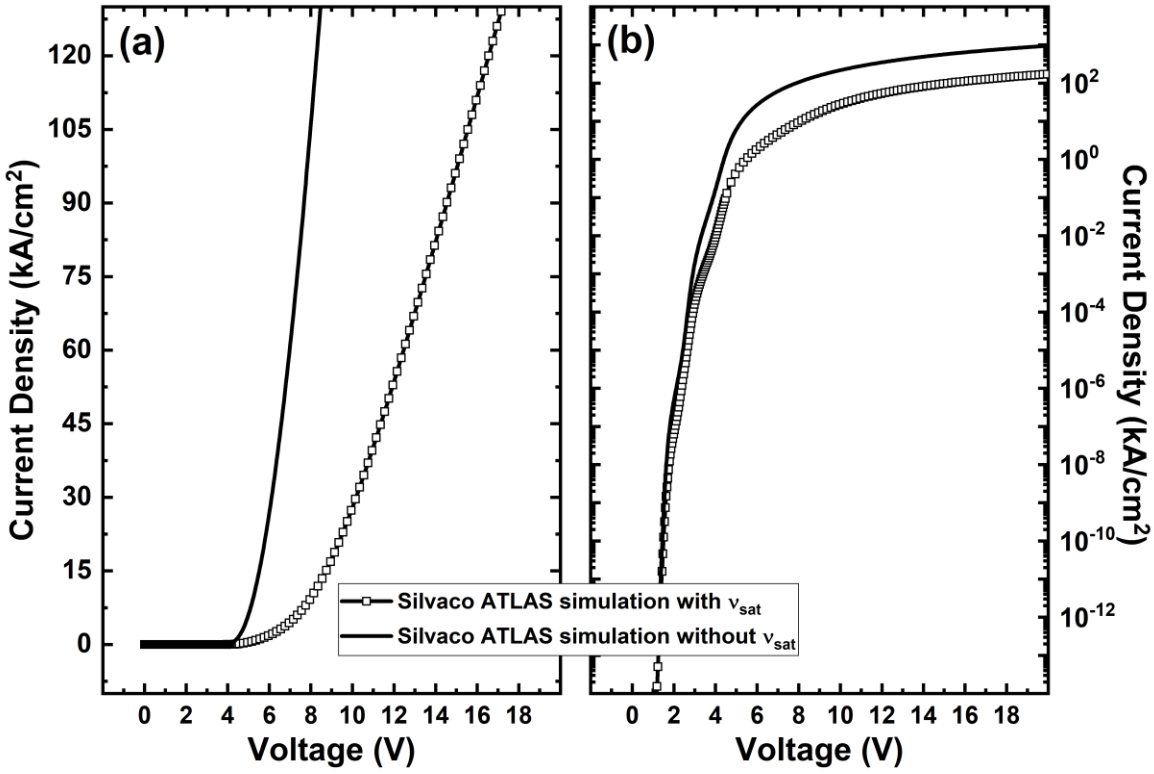


Fig. 3.11 (a) Linear and (b) logarithmic J-V comparison of Silvaco ATLAS simulations with and without field dependent saturation velocity

Since an electric field dependence of mobility is not accounted for in the analytical model but only in the ATLAS simulation model, we observe the discrepancies in trap densities between the two models (Table 3.2).

3.2.7 SPIND Turn-On Voltage V_T

Trap levels affect both low and high voltage characteristics. Using different configurations of trap levels in both the analytical and TCAD models, we can observe the

change in the overall diode turn-on voltage V_T with shallow to deep trap levels. Figures Fig. 3.12 through Fig. 3.14 show J-V, slope – voltage and $R_{ON}S$ characteristics of trap-free T.E. + Mott-Gurney configuration (plot A) and the same with R_{ser} (plot B) and with trap energy levels at 0.25 eV (plot C), 0.45 eV (plot D), 0.7 eV (plot E) and with two trap level configurations with trap levels at 0.45 eV and 0.25 eV (plot G) and the same with a R_{ser} (plot F) and lastly the three trap levels configuration curve-fit (plot H) with R_{ser}, as shown previously. In general, deeper trap levels reduce the forward bias diode current and increase the diode turn-on voltage V_T. Deep trap levels inhibit hole injection at lower voltages allowing lower current to flow through the diode as the diode transitions from TE to space charge limited Mott-Gurney current, and thereby increasing the voltage beyond which the current rapidly increases i.e., the turn-on voltage, V_T. This can be observed from plots C, D and E where the trap energy level increases as $0.25\ eV$ to $0.7\ eV$ and the current at low voltages decreases by an order of 7 (Fig. 3.12(a)) while increasing V_T from $\sim 4\ V$ to $\sim 5\ V$ (Fig. 3.12(b)).

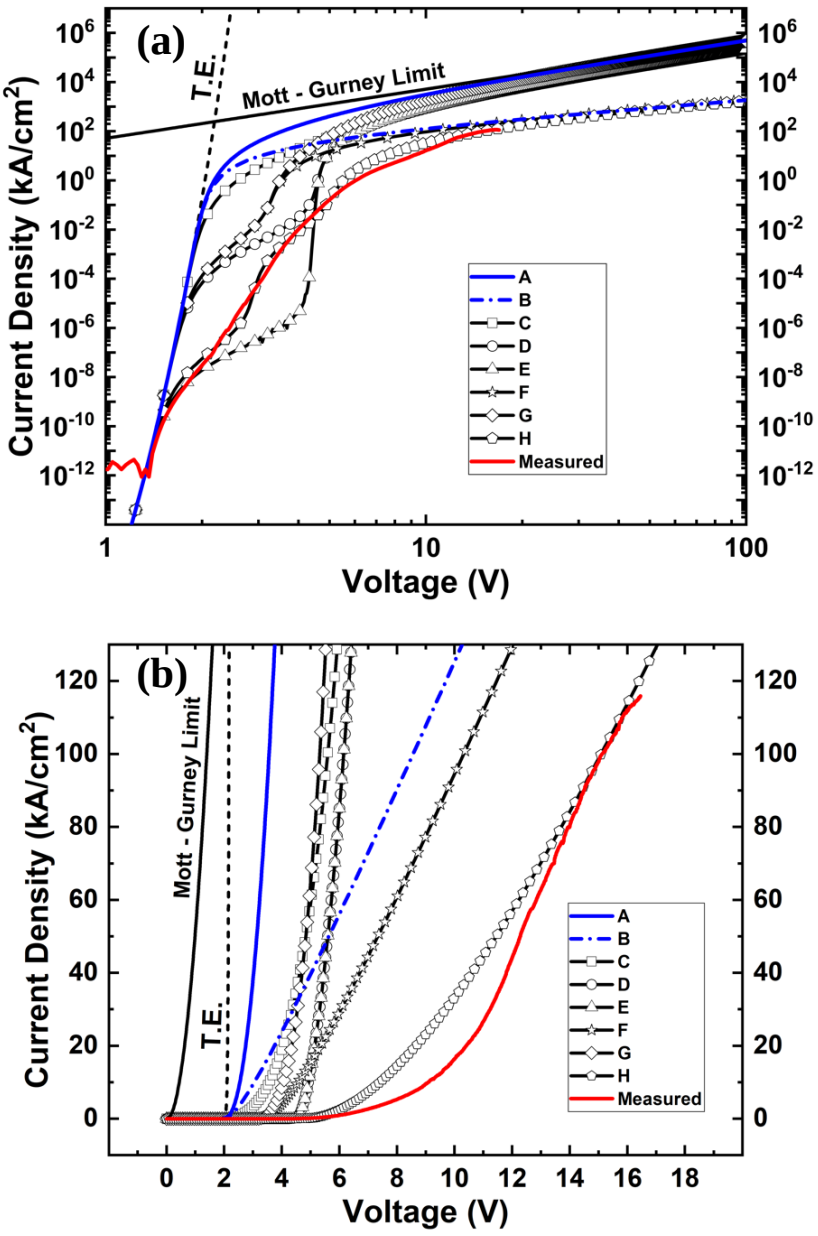


Fig. 3.12 Log-log (a) and linear (b) J-V characteristics from the analytical model show plots for different trap configurations – plot A of trap-free T.E + Mott-Gurney, plot B of trap-free T.E. + Mott-Gurney with R_{ser} in series, plot C of $E_{t3} = 0.25$ eV, plot D of $E_{t2} = 0.45$ eV, plot E of $E_{t1} = 0.7$ eV, plot F of $E_{t2} = 0.45$ eV, $E_{t3} = 0.25$ eV with R_{ser} in series, plot G of $E_{t2} = 0.45$ eV, $E_{t3} = 0.25$ eV, plot H with curve-fit of $E_{t1} = 0.7$ eV, $E_{t2} = 0.45$ eV, $E_{t3} = 0.25$ eV with R_{ser} to measured data.

The inclusion of two trap levels, $E_{t3} = 0.25\,eV$ and $E_{t2} = 0.45\,eV$ (plot G), also increases V_T to ~4.5 V in comparison to a shallow level trap (plot C) $V_T \cong 4\,V$, as can be seen from Fig. 3.12(b). However, it is interesting to note that the V_T for a two-level trap, $E_{t3} = 0.25\,eV$ and $E_{t2} = 0.45\,eV$ (plot G) is smaller in comparison to a single-level trap at $E_{t2} = 0.45\,eV$. To normalize comparison, trap density for all trap levels is fixed at $10^{16}/cm^3$.

In all the configurations, once all trap levels are filled, the current increases parallel to the Mott-Gurney limit. In practical cases, the current is limited by the bulk p^{++} layer and contact resistance R_{ser} soon after its transition from TE to space charge limited conduction. This can be observed from plot F where the two-trap level configuration has an added R_{ser} in series. The current – voltage relation diverges from the Mott-Gurney limit and tends back towards unity. The current therefore gradually transitions from exponential to Mott-Gurney and then to resistance limited. This phenomenon can also be observed by plotting the slope $m = \partial\, log\, J\, /\partial\, log\, V$ as shown in Fig. 3.13.

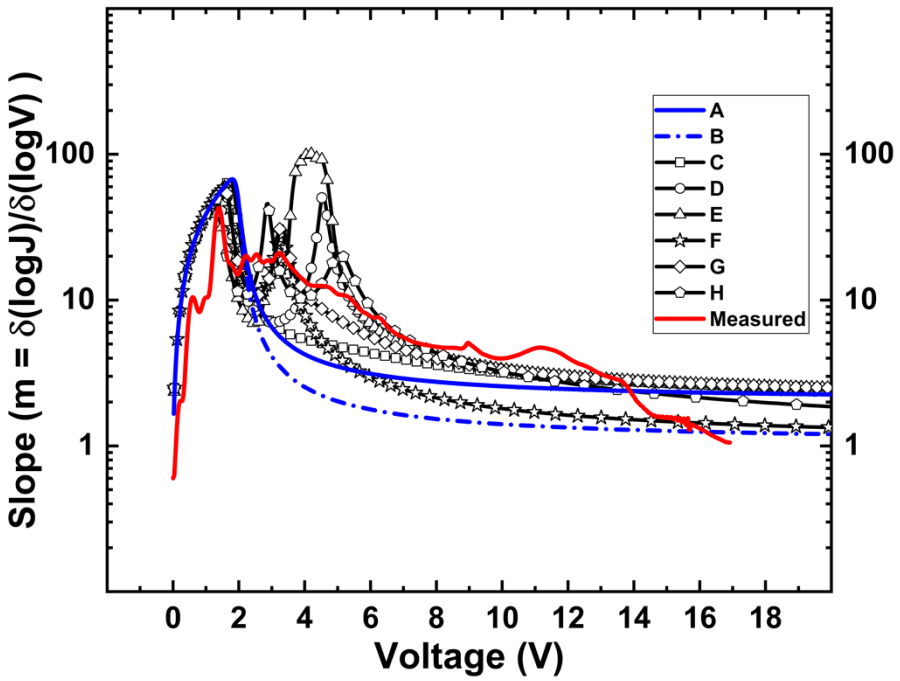


Fig. 3.13 Slope of diamond SPIND J-V characteristics for different trap configurations and thermionic emission (T.E.) and Mott-Gurney (M.G.) with and without R_{ser}

The range of voltage in which the current spends transitioning from exponential to Mott-Gurney varies as the trap configuration i.e., for deeper traps or more trap levels, the longer the transition. It can also be observed that the slope value of plot A (TE + Mott-Gurney (M.G.)) in Fig. 3.13 gradually approaches to a value of 2 i.e., $J \propto V^2$ while plot B (TE + M.G. with R_{ser}) quickly transitions from exponential to Mott-Gurney to resistance limited value of 1 i.e., $J \propto V$. The experimentally measured slope – voltage characteristic also shows a transitioning from exponential to Mott-Gurney to resistance limited conduction.

3.2.8 Specific ON-Resistance $R_{ON}S$

Diamond SPIND high power and RF performance depends on the value of diode specific on-resistance $R_{ON}S$ ($\Omega - cm^2$). Fig. 3.14 shows a minimum experimental value of

diamond SPIND $R_{ON}S$ at $0.05\ m\Omega - cm^2$ at 14.5 V forward bias. Considering a 90 μm p^{++} diamond layer with incomplete ionization that gives a free carrier (hole) concentration of $1.28 \times 10^{19}/cm^{-3}$ (Fig. 5(a)) and mobility of $233\ cm^2/V - s$, the resistivity of p^{++}-layer is $\sim 0.018\ m\Omega - cm^2$. Therefore, the experimental $R_{ON}S$ of $0.05\ m\Omega - cm^2$ is a combination of the bulk p^{++}- layer and contact resistance. The contact resistance can then be assumed to be approx. $\sim 0.035\ m\Omega - cm^2$. As discussed earlier, the analytical model accounts for both contact and bulk resistances by adding R_{ser} in series with J_{TE} and J_{SCL}. A value of $0.05\ m\Omega - cm^2$ for R_{ser} was extracted by fitting the J-V characteristics to the measured data. In the ATLAS simulations, a contact resistance R_C of $0.035\ m\Omega.cm^2$ is added at the cathode contact. The bulk resistance p^{++} layer is accounted for on its own from the 90 μm separation between cathode and top anode contacts. Fig. 3.14 also shows the analytical on-resistance values for all the trap configurations. Ideally in a trap-free diode, $R_{ON}S = 4d^3/(9\epsilon\mu_p V)$, which can be derived by taking a derivative of (3. 5), keeps on decreasing with increasing voltage as the current conduction asymptotically approaches Mott-Gurney limit, as seen from plot A in Fig. 3.14. The addition of trap levels increases the on-resistance at low voltages, which causes $R_{ON}S$ to start asymptotically approaching the trap-free limit at higher voltage. The deeper and the higher number of trap levels, the higher the voltage required to asymptotically approach the trap-free limit.

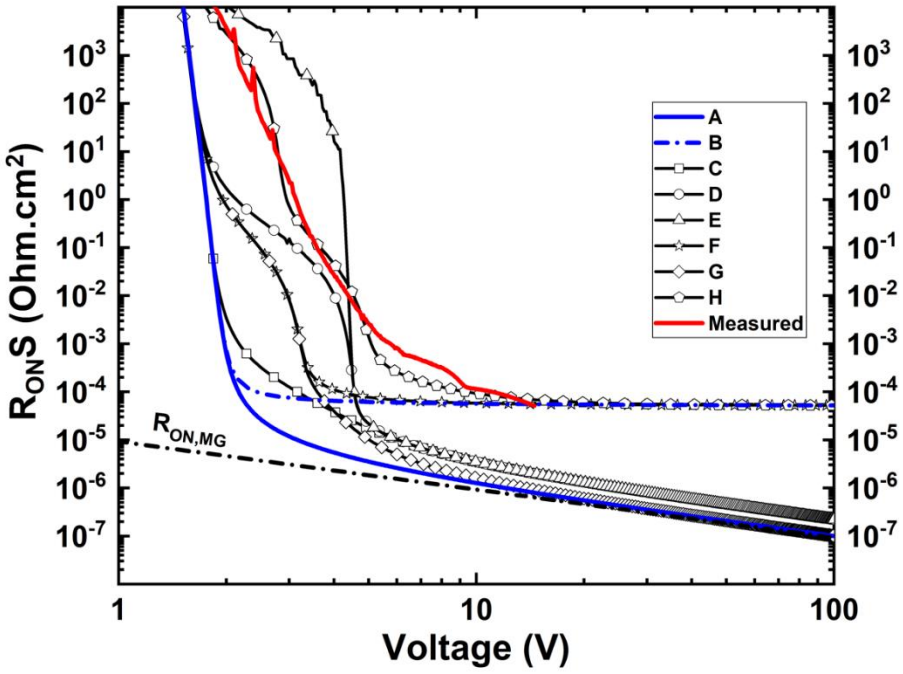


Fig. 3.14 Specific on-resistance $R_{ON}S$ of different trap configurations without a R_{ser} in series asymptotically approach the trap-free case (plot A). The trap configurations with R_{ser} in series, plots B, F, H and measured show $R_{ON}S$ saturated at R_{ser}, as is the case in a real diode.

Therefore, at a given forward operating voltage, deep traps are particularly detrimental for diode performance. In a practical case, where the current is limited by bulk and contact resistances, $R_{ON}S$ saturates to R_{ser} as seen from plot F and H where both the trap configurations are resistance limited. Therefore, the practical limitation to diamond SPIND high power and RF performance is the contact and bulk resistance as demonstrated in [3.30]. Both the contact and bulk resistances can be decreased with increasing the n-layer and p^{++}-layer doping, respectively.

It is clear from the analysis that trap levels, especially deep traps, are detrimental for diamond SPIND performance, particularly in terms of the turn-on voltage. Although single

level traps are considered here, practically the trap distribution is smeared in energy with either a Gaussian or an exponential distribution. Since diamond growth and processing are still in early stages of maturity, dislocations and grain boundaries are possible within a single crystal growth, which introduce exponential trap distributions [3.31]. Therefore, improvements to both the analytical and TCAD models can be made by accounting for exponential and gaussian trap distributions. Further improvements can also be made by accounting for Poole-Frenkel barrier lowering of trap energy levels.

3.3 Reverse Breakdown Characteristics

One of the main connections between material properties and system level performance are so-called Figures of Merit (FOMs), which incorporate performance metrics such as the breakdown voltage, on-resistance, and switching speed into a single metric encapsulating system performance for particular applications. Such FOMs are often used in comparing different material technologies for different application spaces. One such widely used one is the Baliga FOM (BFOM) formulated in 1989 [3.36] related to the on-state resistance and the maximum breakdown voltage of a device based on fundamental material properties, given by

$$BFOM = \frac{V_B^2}{R_{ON,sp}} \tag{3. 46}$$

where $R_{ON,sp}$ is the specific on-state resistance and V_B is the avalanche breakdown voltage based on impact ionization. The prediction of a 200 BFOM and later experimental measurement of BFOM>1000 [3.35] for SiC led to development of SiC power devices in

the following few decades culminating to commercial products by 2003. However, since the formulation of such FOMs, research in WBG device physics has revealed new on-state conduction and off-state breakdown mechanisms, which directly influence the parameters used in the FOM equations. As discussed in the previous sections, one such on-state conduction mechanism is space charge limited conduction (SCLC) current, given by the Mott-Gurney square law [3.16], which dominates in intrinsic or low doped WBG semiconductors [[3.37] - [3.40]]. As we showed in the previous section, the ultimate theoretical limit to the forward current is the Mott-Gurney square law [3.41]. This current-voltage relation in the on-state directly affects how the $R_{ON,sp}$ is calculated and necessitates corrections to the BFOM.

Here, we show that inclusion of space charge limited current leads analytically to a change of slope of $R_{ON,sp}$ versus V_B in the traditional BFOM plot due to the square law dependence of the current on forward voltage in diamond punch through (PT) diodes. The analytical model is verified with Silvaco ATLAS simulations of the same structures, which also show that even non-punch through (NPT) diodes are limited by Mott-Gurney behavior for low doping. Due to the non-shallow nature of acceptors and donors in diamond, we also consider the effect of incomplete ionization on the Baliga plot, which has a strong effect on $R_{ON,sp}$ in the usual Ohmic model, but little effect in terms of the Mott-Gurney limited current.

3.3.1 Space Charge Limited $R_{ON,sp}$ vs Ohmic $R_{ON,sp}$

The formulation of the unipolar BFOM is based on a Schottky diode with a moderately doped drift region and a highly doped substrate with the Schottky contact to the drift region, as shown in Fig. 1 [13]. Traditionally, the $R_{ON,sp}$ for such a Schottky diode is calculated assuming that the drift region is equal to the maximum depletion width obtained at the breakdown voltage and is given as

$$R_{ON,sp} = \frac{d}{q\mu(N_A^-)N_A^-} \tag{3. 47}$$

where d is the thickness of the drift region, $\mu(N_A^-)$ is the doping dependent carrier mobility, N_A^- is the ionized doping concentration in the drift region and q is charge of an electron [3.42]. This is predicated on the assumption that the on-state current conduction is ohmic through the drift region. However, for low drift layer doping, the ohmic conduction based on (3. 47) is not consistent with $R_{ON,sp}$ values reported in the literature (0.1 mΩ-cm^2 [3.46], 0.03 mΩ-cm^2 [3.4], 0.05 mΩ-cm^2 [3.30]). The current conduction in low to moderately doped diamond Schottky diodes is entirely through charge carriers injected by thermionic emission (TE) over the substrate to drift region junction barrier. However, charge injected over the junction barrier via TE from the highly doped substrate is larger than the free carrier density in the drift region. As the injected charge increases with increasing on-state voltage, the charge neutrality is greatly disturbed as the injected charge carriers do not relax into the material quickly enough and thereby start accumulating in the drift region [3.15].

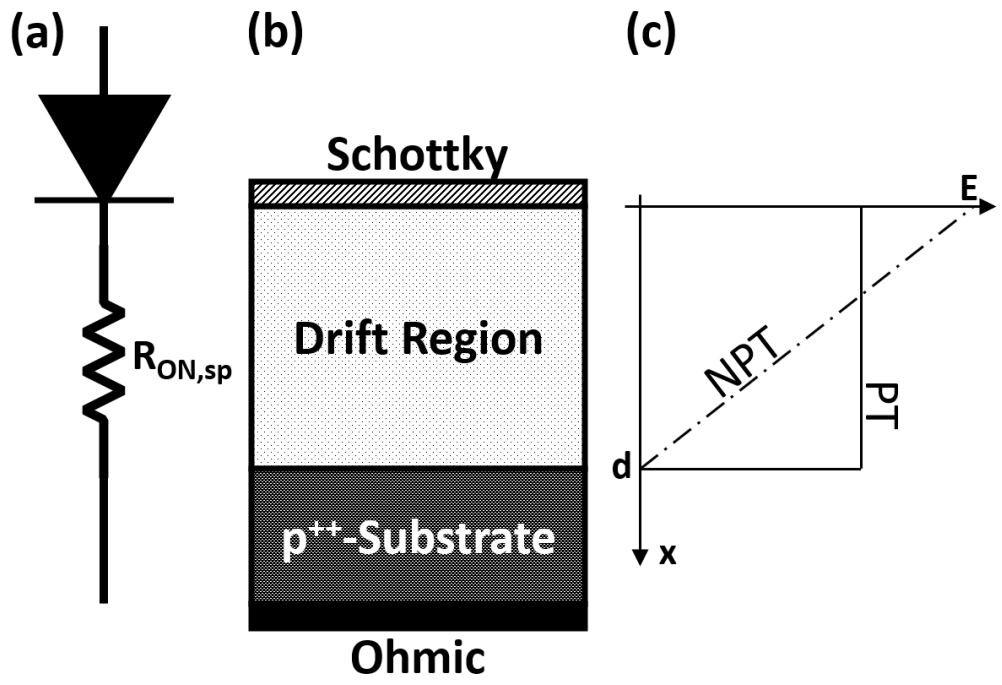


Fig. 3.15 (a) Equivalent Schottky diode model with an on-state specific resistance $R_{ON,sp}$, (b) diode structure used in SIlvaco ATLAS simulations and (c) Non-punch-through (NPT) and punch-through (PT) electric field profiles in the drift region.

This causes the current – voltage relation to transition from exponential (due to TE) to a space charge limited conduction (SCLC) case.

The SCLC current due to injected charge is well established by the Mott-Gurney square law [3.16] given as

$$J = \frac{9}{8}\epsilon_r \epsilon_0 \mu \frac{V^2}{d^3} \tag{3. 48}$$

where ϵ_r is the material's relative dielectric permittivity, ϵ_0 is the permittivity of free space, V is the voltage across the drift region of width d. The $R_{ON,sp}$ can then be calculated by taking the derivative of equation (3. 48), which gives

$$R_{ON,sp,MG} = \frac{4}{9\epsilon_r\epsilon_0\mu}\frac{d^3}{V} \quad (3.\ 49)$$

As can be seen from equation (3. 49), the $R_{ON,sp,MG}$ reduces with on-state voltage across the drift region and has a cubic dependence on the drift layer thickness.

3.3.2 Punch Through vs. Non-Punch-Through

Traditionally the BFOM was evaluated for an abrupt junction in a parallel-plane configuration [3.42]. The solution to the Poisson's equation in the drift region with a known uniform doping concentration leads to a triangular electric field with the electric field reaching a maximum E_M value at the Schottky end and then gradually decreasing towards the abrupt junction i.e., a non-punch-through (NPT) configuration, as shown in Fig. 3.15(c). The breakdown voltage (V_B) and maximum depletion width (W_d) was then determined by the maximum electric field E_M reaching the critical electric field E_C of the semiconductor material i.e., $V_B = W_d E_C/2$. In the original definition of the BFOM, the drift layer width d is made equal to the maximum depletion width W_d, which is what we use in the present paper, although this does not in fact correspond to the maximum BFOM [3.47]. Here the depletion width W_d is dependent on the total doping concentration N_A because in reverse bias (and at breakdown voltage) the depletion charge constitutes the total dopants uncovered (or ionized) by the Fermi level going below (or above) the dopant level.

In a WBG semiconductor like diamond, dopants like P and B have large activation energies (0.57 eV [3.43] and 0.413 eV [3.44], respectively) and produce incompletely

ionized dopants at room temperature. An incomplete ionization ratio η obtained from the positive root of the quadratic equation of charge neutrality (Sze and Ng [3.45]) as shown in section 3.2.3.3.a, as

$$\eta = \frac{N_A^-}{N_A} = \frac{\left(-N_\alpha + \sqrt{N_\alpha^2 + 4N_A N_\alpha}\right)}{2N_A} \tag{3. 50}$$

$$N_\alpha = \frac{N_{V,C}}{g} exp\left(-\frac{\Delta E_A}{k_B T}\right) \tag{3. 51}$$

where N_A^- is the incompletely ionized dopant concentration, g is the degeneracy factor ($g = 6$ for holes, $g = 0.5$ for electrons in diamond [3.17]), k_B is the Boltzmann constant, T is the lattice temperature, $N_{V,C}$ is the effective valence (or conduction) band density of states ($N_V = 2.16 \times 10^{19}/cm^3$ and $N_C = 1.02 \times 10^{19}/cm^3$ for diamond), ΔE_A is the dopant activation energy in relation either to the valence band or conduction band energy levels for donor and acceptor impurities, respectively. The B activation energy in diamond is dependent on the doping concentration N_A as $\Delta E_A = 0.416 - 5.4329 \times 10^{-8} N_A^{1/3}$ [3.17] and a ΔE_A= 0.362 eV for N_A = 1×10^{18} /cm^3 and ΔE_A = 0 eV at the metal-insulator transition of N_A = 4.5×10^{20} /cm^3 is obtained. Therefore, the incomplete ionization η becomes a non-linear function of the doping concentration i.e., $\eta(N_A)$, as shown in the Fig. 3.7.

Therefore, Poisson's equation in the depletion region gives $E_M = qN_A W_d/\epsilon_r\epsilon_0$ and the total doping N_A can be related to V_B as $N_A = \epsilon_r\epsilon_0 E_C^2/2qV_B$, which in combination with equation (3. 47) gives

$$R_{ON,sp} = \frac{4V_B^2}{\eta(N_A)\mu(N_A^-)\epsilon_r\epsilon_0 E_C^3} \tag{3. 52}$$

where $\eta(N_A)$is the ionization ratio, N_A^-/N_A. Therefore, an incomplete ionization modified BFOM similar to the one shown in [3.48] can then be written as

$$BFOM = \frac{V_B^2}{R_{ON,sp}} = \frac{1}{4}\,\eta(N_A)\mu(N_A^-)\epsilon_r\epsilon_0 E_C^3 \tag{3. 53}$$

which gives a ratio of the losses in on-state to the off-state power.

In the case of WBG semiconductor unipolar devices with low or zero doping, e.g., a Schottky diode, the depletion region extends across the drift layer and the electric field is constant throughout, leading to a punch-through (PT) electric field configuration shown in Fig. 3.15. The breakdown voltage for a drift layer width of d can then be determined by $V_B = d \times E_C$. Therefore, for a critical electric field of E_C and for the same breakdown voltage, V_B only half as much of the drift layer width is required in a PT configuration in comparison to an NPT configuration [3.49]. Consequently, to obtain a $R_{ON,sp,MG}$ vs. V_B relationship, the drift layer thickness d can be substituted in equation (3. 49) to obtain

$$R_{ON,sp,MG} = \frac{4V_B^3}{9\epsilon_r\epsilon_0\mu V E_C^3} \tag{3. 54}$$

As is evident from the relation, $R_{ON,sp,MG}$ has a cubic relation with V_B as compared to a square law in the traditional BFOM case. Fig. 3.16 compares $R_{ON,sp}$ vs. V_B calculated by the traditional Baliga FOM from equation (3. 52) assuming complete ionization (black curve) and including incomplete ionization (green curve) to the SCLC $R_{ON,sp,MG}$ vs. V_B

calculated from equation (3. 54) (blue curve) for a forward voltage of 20 V. Here a constant mobility of 2100 cm^2/V-s and a constant critical electric field, E_C, of 10 MV/cm was assumed for holes. As can be seen, the SCLC case has a significantly steeper slope than the traditional BFOM due to the stronger V_B dependence, and the crossing point depends on the forward bias assumed. This implies that in the SCLC case, the FOM is better at low breakdown voltages where $R_{ON,sp,MG}$ is smaller, and worse for high breakdown voltages.

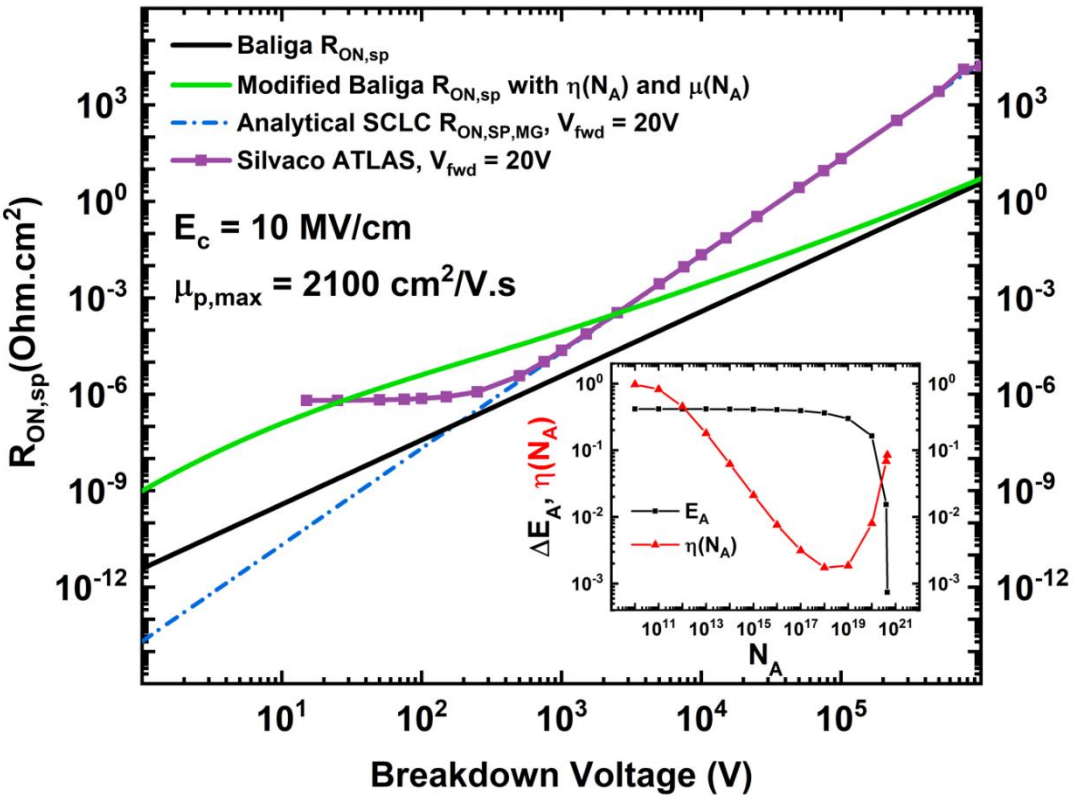


Fig. 3.16 Comparison of traditional Baliga $R_{ON,sp}$ assuming complete ionization, the modified Baliga $R_{ON,sp}$ with $\eta(N_A)$ and $\mu(N_A)$ dependence, the analytical SCLC $R_{ON,sp,MG}$ and Silvaco ATLAS simulations for an intrinsic drift layer at an on-state voltage Vfwd = 20V, for a diamond Schottky pin diode as described in Fig. 3.15.

3.3.3 Silvaco ATLAS On and Off State Simulations

Silvaco ATLAS TCAD simulations as discussed in the previous section were also performed using the Schottky diode structure shown in Fig. 3.15 with an intrinsic drift layer. Physical models such as a doping dependent effective hopping mobility, incomplete ionization, SRH recombination and thermionic emission over a Schottky barrier height are included in the simulations and are detailed in [3.30].

ATLAS simulations of $R_{ON,sp}$versus V_B agree well with the analytical $R_{ON,sp,MG}$ versus V_B calculated from (3. 54) as shown in Fig. 3.16 by the purple data points. Here $V_B = d \times E_C$ was assumed for both curves for simplicity. This agreement strongly supports the supposition of Mott-Gurney behavior limiting the current in forward bias. The divergence of the two curves at lower breakdown voltage is due to the finite on-resistance of the p^{++} substrate (here assumed to be 1 μm thick), which is fully accounted for in the ATLAS simulations.

Fig. 3.17 shows a comparison of the simulated $R_{ON,sp}$ with the analytical $R_{ON,sp,MG}$ (3. 49) variation with drift layer thickness (black curves) for an on-state voltage of 20 V and the variation, as well as the variation with on-state voltage (red) for a constant drift layer thickness of 1 μm, where the agreement between the numerical and analytical models is quite good, again emphasizing the dominant role of Mott-Gurney behavior. In the traditional BFOM from equation (3. 53), some degree of optimization is done by varying the drift layer doping and fixing d equal to the depletion width for a low ohmic $R_{ON,sp}$. However, the assumption of ohmic $R_{ON,sp}$ is not necessarily valid, even in the case of NPT

diodes. An analysis of the slope $m = \partial \log J / \partial \log V$ of the on-state characteristics reveals the dominant current – voltage relationship; a slope of ~2 indicates space charge limited Mott-Gurney conduction while a slope of ~1 indicates ohmic conduction through the drift layer. For a given doping concentration of the drift layer N_A, the slope *m* can be calculated from Silvaco ATLAS on-state simulations for different drift layer thicknesses, as shown in Fig. 3.18. For space charge limited current to dominate, the excess charge injected into the drift region must be swept out by the electric field before it can relax via dielectric relaxation to establish charge neutrality. Assuming a charge carrier velocity v and a uniform on-state potential *V* across a drift layer of thickness d, the carrier transit time across the drift layer can be given as $t_t = \int_0^d v^{-1} x \, dx = d^2/\mu V$.

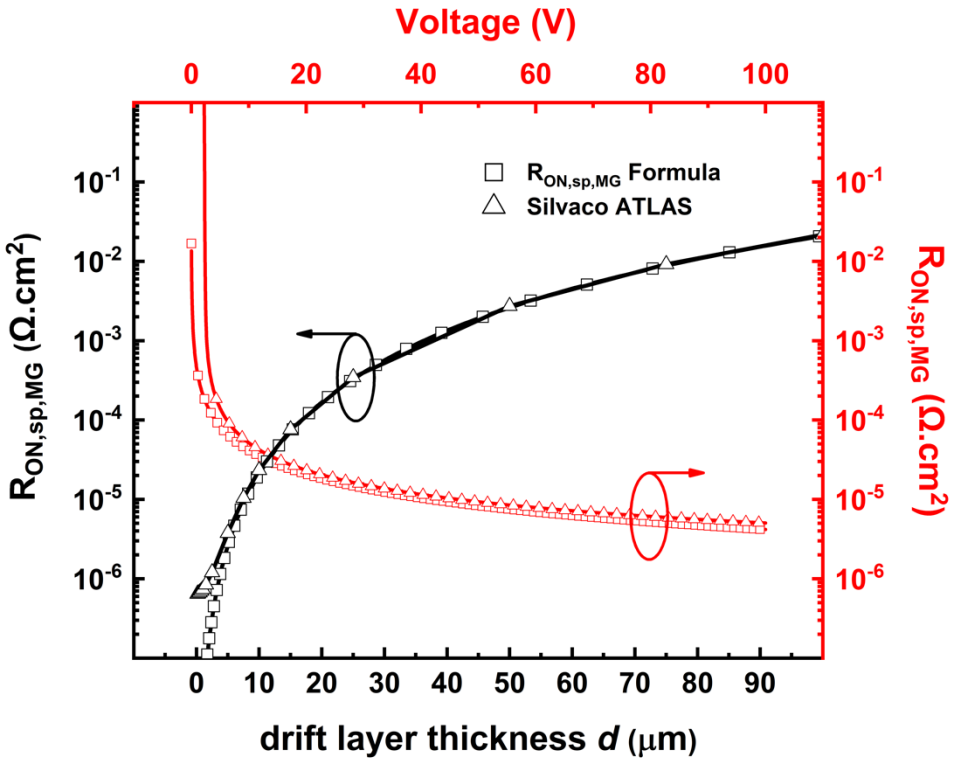


Fig. 3.17 $R_{ON,sp,MG}$ evaluated from equation (3. 49) (squares) and Silvaco ATLAS simulations (triangles) as a function of drift layer thickness (bottom x-axis) and on-state voltage (top x-axis). The $R_{ON,sp,MG}$ vs. drift layer thickness graphs are plotted for an on-state voltage of 20 V whereas the $R_{ON,sp,MG}$ vs voltage graphs are plotted for a drift layer thickness of 1 μm.

The dielectric relaxation time, assuming a thermally generated free carrier concentration p_0, can be given as $\tau_d = \epsilon/\sigma = \epsilon/qp_0\mu$. The current conduction transition from ohmic to SCLC occurs when $t_t \approx \tau_d$. The d at which the transition occurs can therefore be given as $d = \sqrt{\epsilon V/qp_0}$. For low to moderate N_A and d, $t_t \leq \tau_d$, and therefore space charge limited current dominates with a slope m of 2. However, for large d, t_t becomes comparable or larger than τ_d () and the injected carriers have enough time to relax into the dielectric material thereby reverting the dominant slope m back to 1 i.e., ohmic conduction. For very

small d, the forward current becomes dominated by the ohmic resistance of the substrate, and the slope also goes back to 1, as shown by the behavior in Fig. 3.18(a).

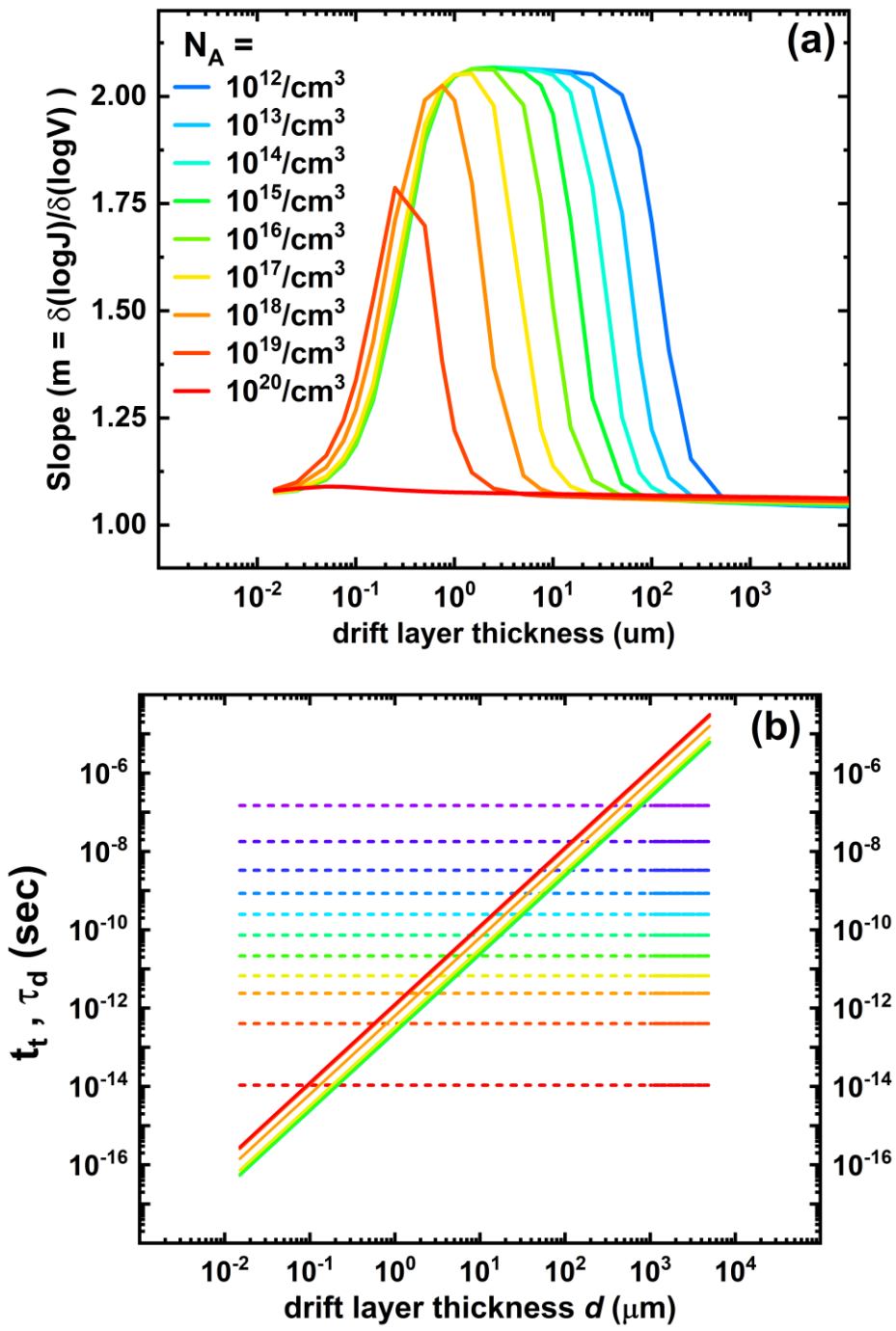


Fig. 3.18 (a) Slope $m = \partial \log J / \partial \log V$ of on-state current – voltage characteristics and (b) t_t (solid lines) and τ_d (dashed lines) vs. drift layer thicknesses for varying drift layer doping N_A of the Schottky diode

The take away from Fig. 3.18(a) is that over a wide range of doping and drift region thicknesses, the on-resistance in NPT Schottky diodes may be dominated by Mott-Gurney behavior with a different $R_{ON,sp}$ than the usually ohmic conduction used in the traditional BFOM plot, which requires different optimization than the Ohmic model used in e.g. [3.47], which will be the subject of future work.

3.3.4 Impact Ionization Silvaco ATLAS Simulations

Although Fig. 3.17 and the modified BFOM of equation (3. 54) provide a correct value of the $R_{ON,sp}$ vs BV characteristics for a diamond Schottky diode with an intrinsic drift layer, practically the drift layer usually has an inevitable background B doping due to the PECVD chamber's memory effect during diamond growth. The reverse leakage current in practical devices is also several orders of magnitude higher than the theoretically simulations. Therefore, for a more realistic realization of the breakdown characteristics including drift layer doping effects and leakage current mechanisms needs to be analyzed. Schottky diode breakdown simulations with varying drift layer doping and with impact ionization were performed as a function of drift layer thickness. Following subsections detail some of the physics models used in the simulations and provides $R_{ON,sp}$ vs BV simulation results for the same.

3.3.4.1 Impact Ionization Model

Impact ionization is a three-particle process where the carriers gain high energies while traveling through high field regions and undergo scattering events with valence band electrons or holes. The energy is transferred from the high energy carriers to the valence

band carriers and lifts them into the conduction band creating an electron-hole pair. This generated electron-hole pair can have high energy as well that can knock out more electrons or holes and thereby creating a cascading effect known as an avalanche effect. The avalanche effect increases the carrier density rapidly and gives a sharp rise in current. Increasing currents can also lead to large self-heating effects and ultimately to device failure through thermal runaway.

In drift-diffusion simulations, the carrier multiplication is expressed in terms of the impact ionization coefficients α_n and α_p, which describe the number of electron-hole pair generated per unit distance traveled by a high energy carrier between collisions [3.45]. Considering only holes generated by holes,

$$\alpha_p = \frac{1}{p}\frac{dp}{d(tv_p)} = \frac{1}{pv_p}\frac{dp}{dt} \tag{3. 55}$$

where v_p is the hole velocity and $dp/d(tv_p)$ is the carrier generation rate per distance, p is the hole concentration and dp/dt is the hole generation rate. Also accounting for electrons generated by impact ionization multiplication, the generation rate can be written as

$$G^{II} = \frac{dp}{dt} = \frac{dn}{dt} = \alpha_p p v_p + \alpha_n n v_n = \alpha_p \frac{J_p}{q} + \alpha_n \frac{J_n}{q} \tag{3. 56}$$

In Silvaco ATLAS simulations, the ionization rate proposed by Selberherr [3.50] is used. The α_p and α_n coefficients in the Selberherr model are defined as

$$\alpha_p = \mathrm{AP}\exp\left(-\left(\frac{\mathrm{BP}}{\mathrm{E}}\right)^{\beta_p}\right) \tag{3. 57}$$

$$\alpha_n = \mathrm{AN}\exp\left(-\left(\frac{\mathrm{BN}}{\mathrm{E}}\right)^{\beta_n}\right) \tag{3. 58}$$

where E is the electric field in the direction of current flow at a particular position in the structure mesh in the simulation and the AP, BP, β_p, AN, BN and β_n are simulation parameters defined as

$$AP = AP_{1,2}\left(1 + A.PT\left[\left(\frac{T_L}{300}\right)^{M.APT} - 1\right]\right) \tag{3. 59}$$

$$AN = AN_{1,2}\left(1 + A.NT\left[\left(\frac{T_L}{300}\right)^{M.ANT} - 1\right]\right) \tag{3. 60}$$

$$BP = BP_{1,2}\left(1 + B.PT\left[\left(\frac{T_L}{300}\right)^{M.BPT} - 1\right]\right) \tag{3. 61}$$

$$BN = BN_{1,2}\left(1 + B.NT\left[\left(\frac{T_L}{300}\right)^{M.BNT} - 1\right]\right) \tag{3. 62}$$

The parameters in equations (3. 59) to (3. 62) are defined in

Parameter	**Value**	**Parameter**	**Value**
AN_1	$6.56 \times 10^7\ /cm$	β_n	1
AN_2	$6.56 \times 10^7\ /cm$	$A.NT$	0.588
BN_1	$7.14 \times 10^7\ V/cm$	$A.PT$	0.588
BN_2	$7.14 \times 10^7\ V/cm$	$B.NT$	0.248
AP_1	$6.56 \times 10^7\ /cm$	$B.PT$	0.248

AP_2	$6.56 \times 10^7\ /cm$	$M.ANT$	1
BP_1	$7.14 \times 10^7\ V/cm$	$M.APT$	1
BP_2	$7.14 \times 10^7\ V/cm$	$M.BNT$	1
β_p	1	$M.BPT$	1

Table 3.3 and have been evaluated from first principal calculations [3.51]. The carrier multiplication coefficient is then defined as

$$M_p = \frac{1}{1 - \int_0^L \alpha_p \exp\left(-\int_0^x \left(dx'(\alpha_p - \alpha_n)\right)\right)} \tag{3. 63}$$

where L is the distance between the two electrodes of the diamond Schottky diode. The hole current resulting due to this impact ionization multiplication is evaluated as

$$J_p(x) = J \exp\left(\int_0^x (\alpha_p - \alpha_n)dx\right)\left[\int_0^x \alpha_n \exp\left(-\int_0^x (\alpha_p - \alpha_n)dx'\right)dx + \frac{1}{M_p}\right] \tag{3. 64}$$

The avalanche breakdown occurs when the multiplication factor M_p approaches infinity, therefore, the relation between the depletion width ($= d$ in case of PT configuration) and the ionization coefficients becomes

$$1 = \int_0^d \alpha_p \exp\left(-\int_0^x (\alpha_p - \alpha_n)dx'\right)dx \tag{3. 65}$$

Parameter	**Value**	**Parameter**	**Value**
AN_1	$6.56 \times 10^7\ /cm$	β_n	1
AN_2	$6.56 \times 10^7\ /cm$	$A.NT$	0.588

BN_1	$7.14 \times 10^7\ V/cm$	$A.PT$	0.588
BN_2	$7.14 \times 10^7\ V/cm$	$B.NT$	0.248
AP_1	$6.56 \times 10^7\ /cm$	$B.PT$	0.248
AP_2	$6.56 \times 10^7\ /cm$	$M.ANT$	1
BP_1	$7.14 \times 10^7\ V/cm$	$M.APT$	1
BP_2	$7.14 \times 10^7\ V/cm$	$M.BNT$	1
β_p	1	$M.BPT$	1

Table 3.3 Impact ionization parameters used in diamond Schottky diode simulations

3.3.4.2 Tsu-Esaki Tunneling Model

For all reverse bias simulations, the probability of band-to-band tunneling increases with high reverse electric fields contributing to one of the sources for reverse leakage current. For this purpose, the Tsu-Esaki tunneling model is implemented during the breakdown simulations. The hole (or electron) tunneling current given by the Tsu-Esaki model at the cathode contact is given as

$$J_{tp,n} = -\frac{4\pi q m^* m_0 k_B T}{h^3} \int_0^{\phi_{bp,n}} P(E_Z) N(E_Z) dE_Z \tag{3. 66}$$

where $\phi_{bp,n}$ is the hole (or electron) Schottky barrier height at the cathode contact, m^* is the relative effective mass of holes (0.8 for diamond) or electrons (0.48 for diamond), m_0 is the rest mass of an electron, h is the Planck's constant and $N(E_Z)$ is the supply function given by

$$N(E_Z) = \ln\left\{\frac{\left(1 + exp\left(\frac{E_F - E_Z}{k_B T}\right)\right)}{1 + exp\left(\frac{E_F - E_Z - qV}{k_B T}\right)}\right\} \tag{3. 67}$$

The transmission probability $P(E_Z)$ is given by the WKB approximation for a triangular barrier as

$$P(E_Z) = \exp\left(\frac{-8\pi(2m^*)^{\frac{1}{2}}\left(\phi_{bp,n} - E_Z\right)^{\frac{3}{2}}}{3qhE}\right) \tag{3. 68}$$

Fig. 3.19 shows the reverse leakage current of a diamond Schottky diode with a drift layer thickness of 3 μm with and without Tsu-Esaki tunneling current model. The breakdown voltage does not differ with and without the Tsu-Esaki model implementation, however the leakage current increases significantly with tunneling.

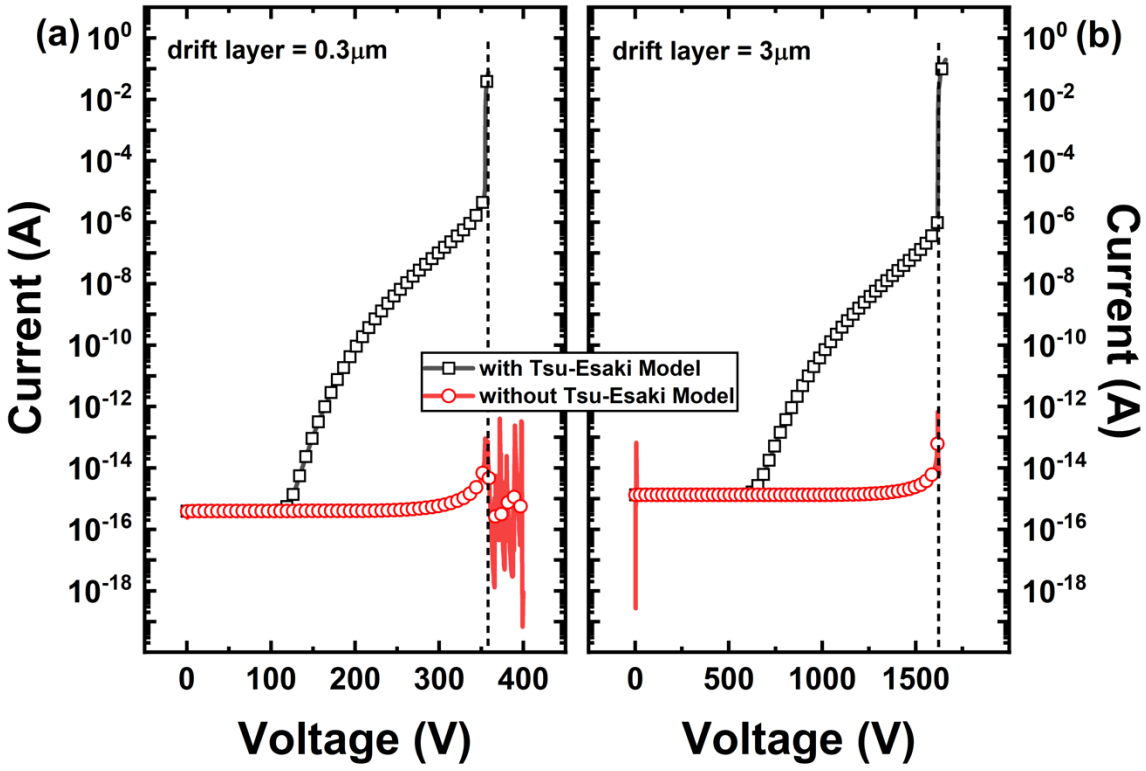


Fig. 3.19 Reverse bias breakdown characteristics of diamond Schottky diode from Silvaco ATLAS simulations with and without the Tsu-Esaki tunneling model for drift layer of (a) 0.3 μm and (b) 3 μm

3.3.4.3 $R_{ON,sp}$ vs. BV for Doped Drift Layers

Drift layers with finite doping in wide bandgap diodes influence the $R_{ON,sp}$ vs. BV relation even more. The depletion width in a doped drift layer is no longer in a PT configuration where extends beyond the drift layer thickness but has a finite value dependent on the doping level. Higher values of doping levels lead to smaller depletion layer widths in the p^{++} – substrate drift layer abrupt junction, which can be given as

$$W_D = \sqrt{\frac{2\epsilon_s(\Psi_{bi} + V_{off})}{qN_A}} \tag{3. 69}$$

where Ψ_{bi} is the built-in voltage between the p^{++} – substrate and the drift layer and V_{off} is the off-state bias. The maximum BV value for doped drift layers is dependent on N_A and is calculated from the impact ionization integral as shown in section 3.3.4.1. Therefore, for drift layer thicknesses larger than the depletion widths for a given N_A and at the maximum BV, the breakdown voltage remains constant whereas the $R_{ON,sp}$ increases because of the increasing drift layer thickness. This leads to the $R_{ON,sp}$ vs. BV relation to increase vertically after a certain BV value, as shown in Fig. 3.20 for $N_A = 10^{14}/cm^3$, $10^{15}/cm^3$ and $10^{16}/cm^3$. The slope of the $R_{ON,sp}$ vs. BV plot following a proportionality of $R_{ON,sp,MG} \propto V_B^3$ changes gradually to $R_{ON,sp} \propto V_B^2$ for all the three N_A. This can be attributed to the gradual change of conduction mechanism from space charge limited or Mott-Gurney to Ohmic, as was shown in section 3.3.3.

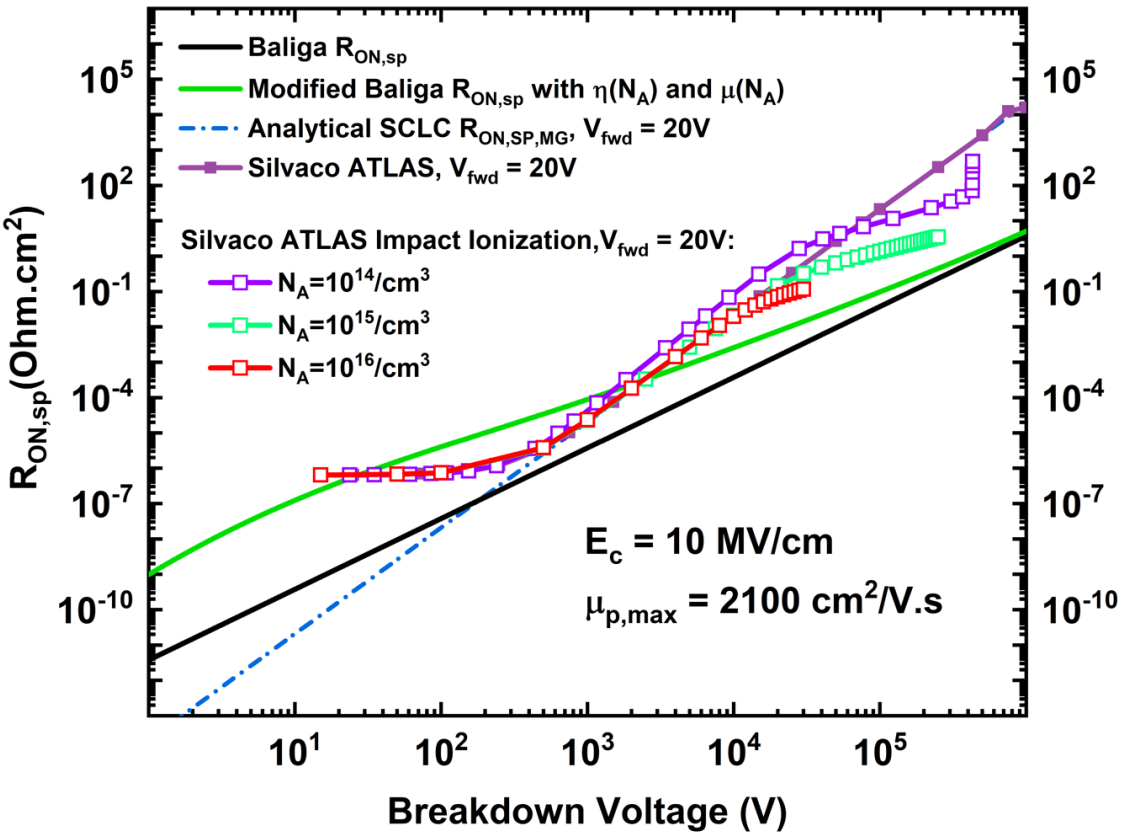


Fig. 3.20 Comparison of traditional Baliga $R_{ON,sp}$ assuming complete ionization, the modified Baliga $R_{ON,sp}$ with $\eta(N_A)$ and $\mu(N_A)$ dependence, the analytical SCLC $R_{ON,sp,MG}$, Silvaco ATLAS simulations for an intrinsic drift layer and for $N_A = 10^{14}/cm^3$, $10^{15}/cm^3$ and $10^{16}/cm^3$ at an on-state voltage Vfwd = 20V, for a diamond Schottky pin diode as described in Fig. 3.15.

Fig. 3.21 shows the depletion layer width W_D as a function of V_{off} for varying N_A. The intersection between the stars and lines in Fig. 3.21 indicate the maximum breakdown voltage (i.e., maximum off-state voltage) for a particular doping N_A obtained from Silvaco ATLAS impact ionization simulations and the maximum drift layer thickness corresponding to the maximum W_D at the breakdown voltage. Increasing the drift layer thickness beyond the max. W_D will only increase the $R_{ON,sp}$ without increasing the BV

value. Therefore, an optimization of the $R_{ON,sp}$ and BV trade-off for wide bandgap materials such as diamond with doped drift layers can be done by fixing the drift layer thickness equal to the maximum W_D.

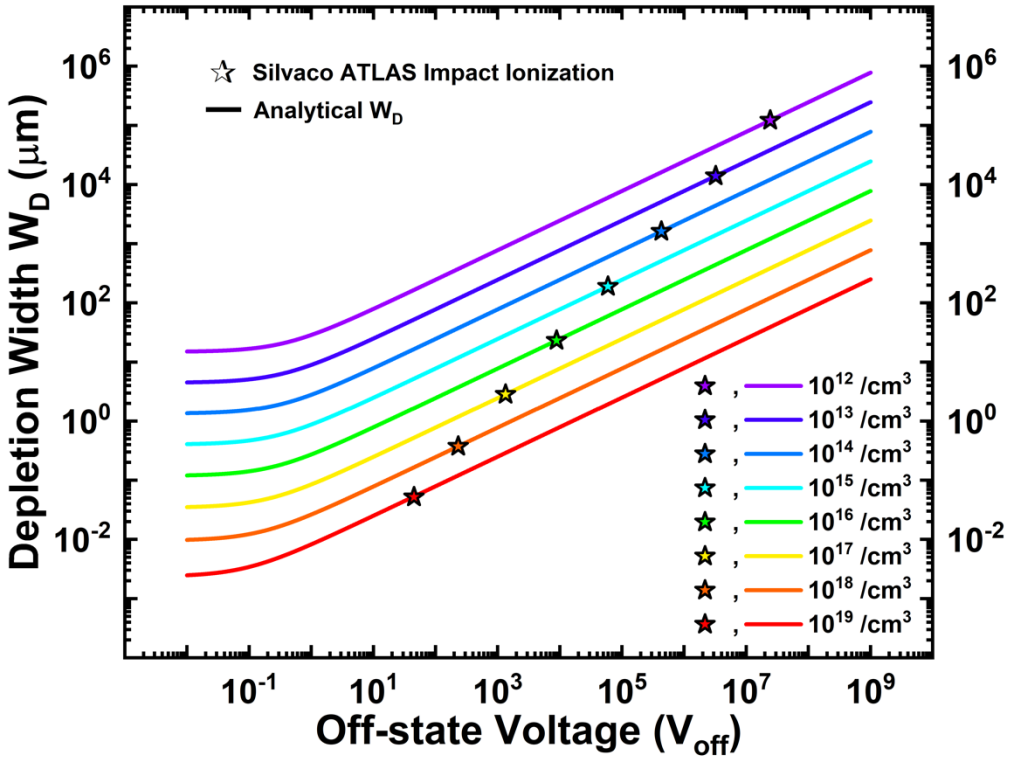


Fig. 3.21 Depletion width as a function of the off-state voltage applied on the diamond SPIND shown in Fig. 3.15 with varying drift layer doping N_A. The solid lines are W_D calculated from equation (3. 69) and are intersected by the max. W_D at the breakdown voltage obtained from Silvaco ATLAS impact ionization simulations.

3.3.5 Experimental Destructive Breakdown of Diamond Diodes

Several diamond SPINDs of a sample with targeted n-layer doping of $5 \times 10^{18}/cm^3$ and *n*- and *i*-layer thicknesses of 200 nm and 750 nm, respectively, were tested for their breakdown characteristics, as shown by the forward and reverse I-V characteristics in Fig. 3.22. The breakdown characteristics were tested using a Keithley 2657A with a layer of

Florinet F40 to prevent air dielectric breakdown. Destructive breakdown which resulted in evaporation of the material was observed at the breakdown voltages, as shown in Fig. 3.23. A cavity of ~720 nm is induced with the destructive breakdown, as shown from the Dektak Profilometer in Fig. 3.23(c).

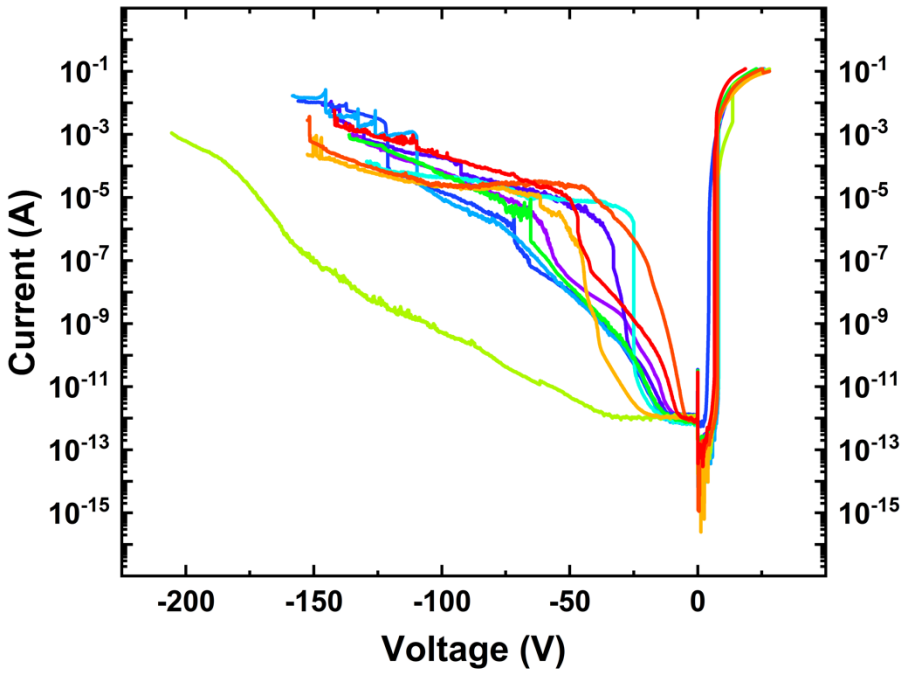


Fig. 3.22 I-V and breakdown characteristics of a diamond SPIND with targeted n-layer doping of $5 \times 10^{18}/cm^3$ and n- and i-layer thicknesses of 200 nm and 750 nm, respectively.

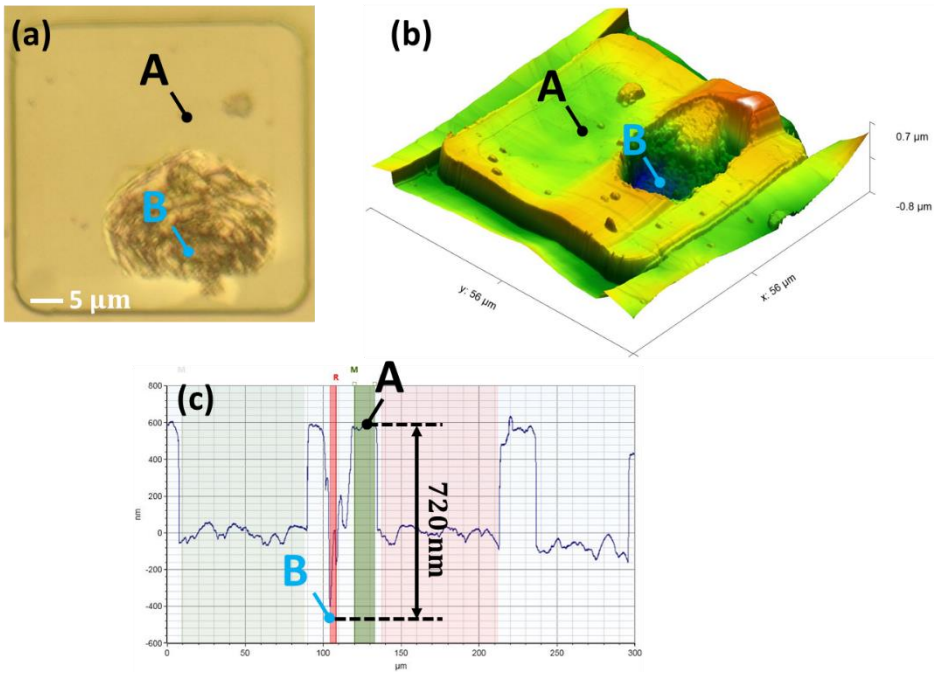


Fig. 3.23 (a) Microscope, (b) AFM and (c) profilometer profile of the destructive breakdown of the diamond SPIND. A ~720 nm cavity is induced during the destructive breakdown.

3.4 Self-Heating Effect in Diamond Diodes

An electric current flowing through a semiconductor region of finite conductivity causes a rise in the lattice temperature by the conversion of electric energy to heat through resistive losses in the material. Heat is generated on the microscale by the conduction electrons or holes transfer energy to the surrounding molecules/atoms in the lattice through collisions. This process of self-heating of the semiconductor lattice is called Joule heating. Self-heating in semiconductor devices is mostly undesirable due to its degrading consequences such as thermal breakdown, material degradation and reliability issues. Among all the semiconducting materials, diamond has one of the highest thermal conductivities, $\kappa = 22\, W/cm - K$. Therefore, ideally the heat generated due to joule

heating can be very quickly extracted to the environment through the diamond bulk and thereby preventing exacerbation of its degrading effects. However, practically, the material quality and interface thermal resistances may pose hindrances to the efficient extraction of heat. Here, through Silvaco ATLAS simulations, we provide a ballpark estimation of the self-heating effects (SHE) in diamond diodes. Following sub-sections detail the simulation methodology and provide insights into SHE in diamond diodes. Several simulations were done to establish a range of SHE in diamond diodes ranging from idealistic high thermal conductivity and low thermal boundary resistance (R_{th}) to practical values of low thermal conductivity and high R_{th}. The diamond SPIND structure shown in Fig. 3.1(a) was used to perform the Silvaco ATLAS simulations with SHE.

3.4.1 Wachutka Lattice Heating Model in Silvaco ATLAS

The GIGA self-heating simulator in Silvaco ATLAS implements the Wachutka lattice heating model [3.52], which accounts for Joule heating, heating and cooling due to carrier generation and recombination (GR heating-cooling) and the Peltier and Thomson effects. Here we consider only the Joule heating and GR heating-cooling effects. The primary heat flow equation used in ATLAS GIGA simulations is

$$C\frac{\partial T_L}{\partial t} = \nabla(\kappa \nabla T_L) + H \tag{3. 70}$$

where C is the heat capacitance per unit volume, κ is the thermal conductivity, H is the heat generation and T_L is the local lattice temperature. The heat capacitance is expressed as $C = \rho C_p$ where C_p is the specific heat capacity and ρ is the density of the material. A

temperature dependent thermal conductivity $\kappa(T_L) = \kappa_C\ (T_L/300)$ is used here, where κ_C is the thermal conductivity at 300 K equal to 22 W/cm.K.

The heat generation term H in (3. 70) in the drift-diffusion approximation considering Joule heating and GR heating-cooling is given as

$$H = \frac{\overrightarrow{|J_n|}^2}{q\mu_n n} + \frac{\overrightarrow{|J_p|}^2}{q\mu_p p} + q(R-G)\left[T_L\left(\frac{\partial \phi_n}{\partial T_{n,p}}\right) - \phi_n - T_L\left(\frac{\partial \phi_p}{\partial T_{n,p}}\right) - \phi_p\right] - T_L\left[\left(\frac{\partial \phi_n}{\partial T}\right)_{n,p} + P_n\right] divJ_n - T_L\left[\left(\frac{\partial \phi_p}{\partial T}\right)_{n,p} + P_p\right] divJ_p \quad (3.\ 71)$$

where the first two terms are the Joule heating terms and the last two terms are the GR heating-cooling terms. The $J_{n,p}$ is the electron or hole current density, $\phi_{n,p}$ is the local electron or hole Fermi potential, n, p are the local electron and hole concentrations and $P_{n,p}$ are the absolute thermoelectric powers for electrons and holes calculated as

$$P_n = \frac{k_B}{Q}\left(\frac{5}{2} + \ln\left(\frac{N_C}{n}\right) + KSN + \zeta_n\right) \quad (3.\ 72)$$

$$P_p = \frac{k_B}{Q}\left(\frac{5}{2} + \ln\left(\frac{N_V}{p}\right) + KSP + \zeta_p\right) \quad (3.\ 73)$$

where KSN and KSP are the exponents in the power law relationship between relaxation time (or mobility) and carrier temperature, ζ_n and ζ_p are the phonon drag contribution to the thermopower (relevant only for low temperature simulations) and N_C and N_V are the temperature dependent conduction and valence band density of states given as

$$N_C = \left(\frac{2\pi m_e^* k_B T_L}{h^2}\right)^{\frac{3}{2}} \quad (3.\ 74)$$

$$N_V = \left(\frac{2\pi m_h^* k_B T_L}{h^2}\right)^{\frac{3}{2}} \quad (3.\ 75)$$

where m_e^* and m_h^* are the relative electron and hole masses in diamond. The electron and hole current densities are modified to account for spatially varying lattice temperatures as

$$\overrightarrow{J_n} = -q\mu_n n(\nabla\phi_n + P_n \nabla T_L) \quad (3.\ 76)$$

$$\overrightarrow{J_p} = -q\mu_p p(\nabla\phi_p + P_p \nabla T_L) \quad (3.\ 77)$$

For transient simulations, the specific heat capacity as a function of the lattice temperature is modeled as

$$C = A_{cV} + B_{cV} T_L + C_{cV} T_L^2 + \frac{D_{cV}}{T_L^2} \quad (3.\ 78)$$

The values of the simulation parameters A_{cV}, B_{cV}, C_{cV} and D_{cV} are taken from literature [3.53] and are given in Table 3.4.

SHE Simulation Parameter	**Value**
$A_{cV}\ (J/cm^3K)$	0.4
$B_{cV}\ (J/cm^3K^2)$	0.011
$C_{cV}\ (J/cm^3K^3)$	-4×10^{-6}
$D_{cV}\ (J.K/cm^3)$	-1.1×10^5
$\kappa\ (W/cm.K)$ [3.1]	22
m_e^*	0.48
m_h^*	0.8

Table 3.4 SHE simulation parameter values taken from literature [3.53] and used in self-heating simulations in Silvaco ATLAS

3.4.2 Thermal Boundary Conditions

Thermal contacts are setup at the cathode and anode metals and at the top diamond surface. The thermal contacts are assumed to have a Dirichlet boundary condition, where the external temperature at the thermal contact is assumed to be a fixed value (300 K). A high value of thermal conductance i.e., $\alpha = 20\ \mathrm{kW/cm^2}K$ [3.54] is assumed at the metal contacts whereas a value of $\alpha = 2\ \mathrm{kW/cm^2K}$ is set for the diamond to air interface. The sides of the simulation space are defaulted to a Neumann boundary condition where the heat flux is continuous. The general heat flow equation at the thermal boundaries is given as

$$\overrightarrow{J_{tot}^{u}}.\vec{s} = \alpha(T_L - T_{ext}) \tag{3. 79}$$

where $\overrightarrow{J_{tot}^{u}}$ is the total energy flux, $\vec{s}$ is the unit external normal of the boundary and T_{ext} is the external temperature set to 300 K. Fig. 3.24 shows all the thermal boundary conditions set in the diamond SPIND structure.

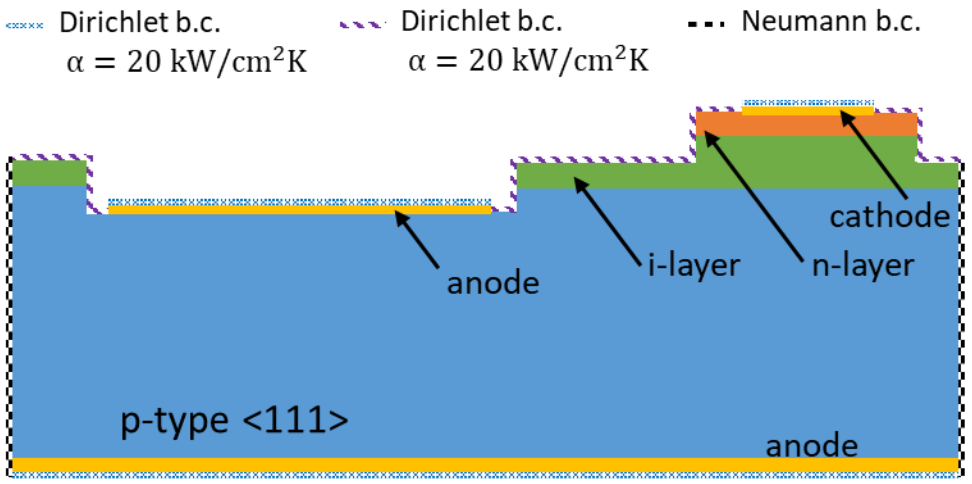


Fig. 3.24 Thermal boundary conditions setup during the Silvaco ATLAS simulations for diamond SPIND with SHE

3.4.3 Diamond Diode Simulations with Self-Heating Effects

Figures Fig. 3.25(a) and Fig. 3.25(b) show and maximum lattice temperature and on-state current vs. on-state voltage plots, respectively, for different Silvaco ATLAS simulations with diamond SPIND with multiple single level traps at a $\kappa = 22\ \mathrm{W/cm-K}$ and $\kappa = 10\ \mathrm{W/cm-K}$, diamond SPIND with no traps at $\kappa = 22\ \mathrm{W/cm.K}$ and $\kappa = 10\ \mathrm{W/cm-K}$ and finally diamond SPIND at $\kappa = 22\ \mathrm{W/cm-K}$ and with the thermal conductance at the contacts $\sigma_C \sim \infty\ \mathrm{W/cm^2-K}$ i.e. an idealistic scenario of zero thermal resistance to an infinite temperature sink. As seen from Fig. 3.25(a), at 20 V on-state bias, the self-heating temperature ranges from 555 K (or a 255 K rise) for $\kappa = 10\ \mathrm{W/cm-K}$ and $\alpha_C = 20\ \mathrm{kW/cm^2-K}$ to 331 K (or a 31 K rise) for the idealistic scenario of $\kappa = 22\ \mathrm{W/cm-K}$ and $\alpha_C = \infty\ \mathrm{MW/cm^2-K}$. The current density increases for higher temperature rise due to increase in hole concentration because of the increase in ionization

of Boron dopants in the p-layer, as can be seen by comparing the simulations with SHE with no SHE in Fig. 3.25(b). The increase in self-heating temperature causes a bigger 'jump' in the current – voltage characteristics of the simulations with the multiple single-level trap energy levels. This is due to the sudden charging of trap energy levels by the increase in free hole concentrations due to the rise in temperature. This effect can be qualitatively observed from practical measurements of a $50\,\mu m$ diameter diamond SPINDs, as shown in Fig. 3.26. Fig. 3.25(c) shows a plot of the lattice temperature as a function of the electric power in the diamond SPINDs and compares it with the simulation results of a p-type diamond demonstrated by Lambert et. al. [3.53]. The idealistic simulations of at $\kappa = 22\ \mathrm{W/cm-K}$ and $\sigma_C \sim \infty\ \mathrm{W/cm^2-K}$ in this research match well with the simulation results of Lambert et. al. [3.53].

Fig. 3.27 and Fig. 3.28 show the simulated current density and corresponding lattice temperature profile over the device area for $\kappa = 22\ \mathrm{W/cm-K}$ and $\alpha_C = 20\ \mathrm{kW/cm^2-K}$ at an on-state bias of 20 V applied on the diamond SPIND. The current density and corresponding lattice temperature 'hot-spots' are in the p^{++}–substrate parallel to the cathode contact edges. The heat generated in the bulk of the diode flows towards the cathode and anode contacts as well as to the diamond surface, where it dissipates to the surrounding air. Due to the finite thermal resistance between the diamond – contact and diamond – air interface, a rise in temperature is expected at both these interfaces.

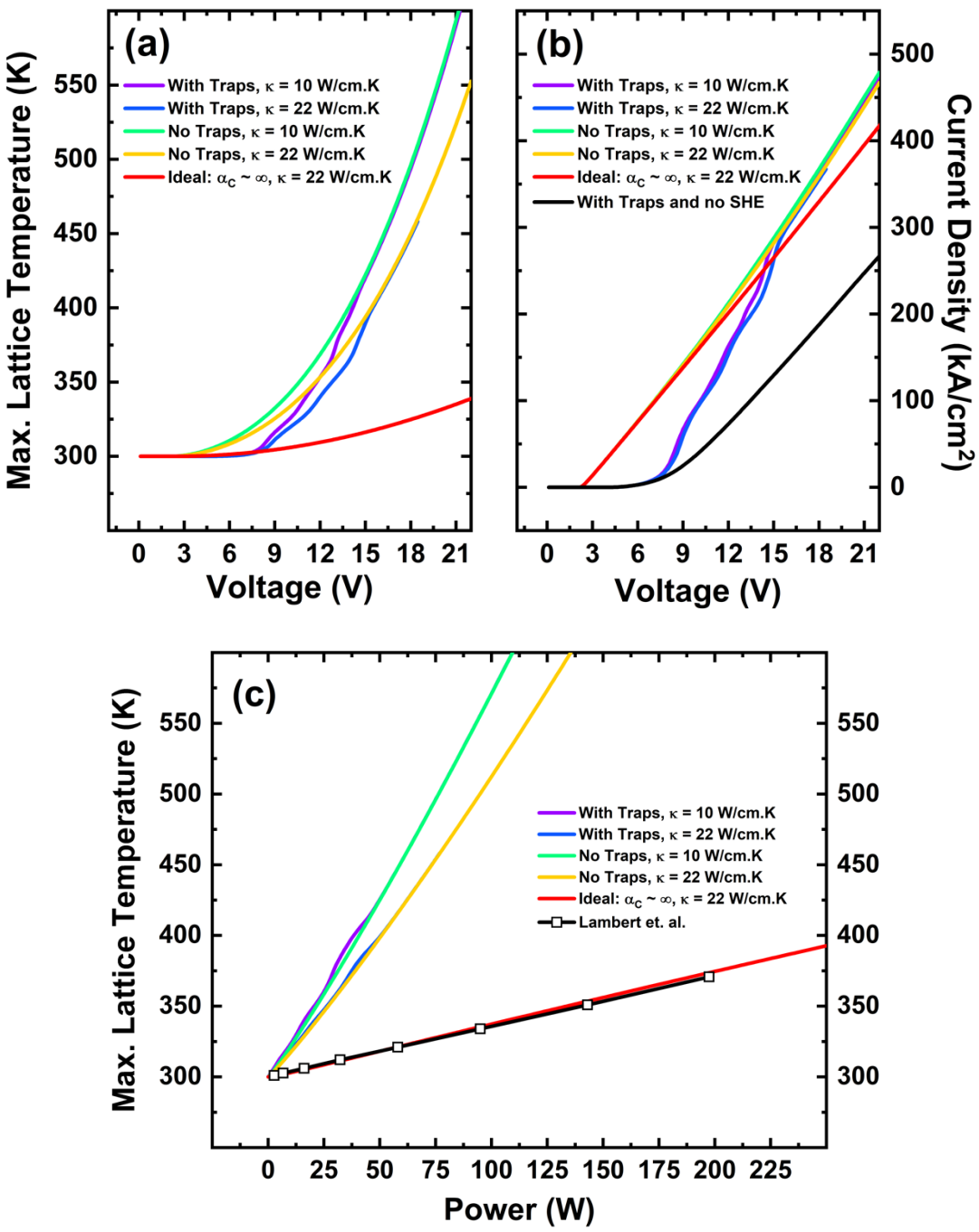


Fig. 3.25 (a) Current Density and (b) lattice temperature vs on-state of a diamond SPIND with multiple single-level traps at $\kappa = 22\ \mathrm{W/cm-K}$ and $\kappa = 10\ \mathrm{W/cm-K}$, diamond SPIND with no traps at $\kappa = 22\ \mathrm{W/cm-K}$ and $\kappa = 10\ \mathrm{W/cm-K}$ and an idealistic scenario with $\kappa = 22\ \mathrm{W/cm-K}$ and $\sigma_C \sim \infty\ \mathrm{W/cm^2-K}$

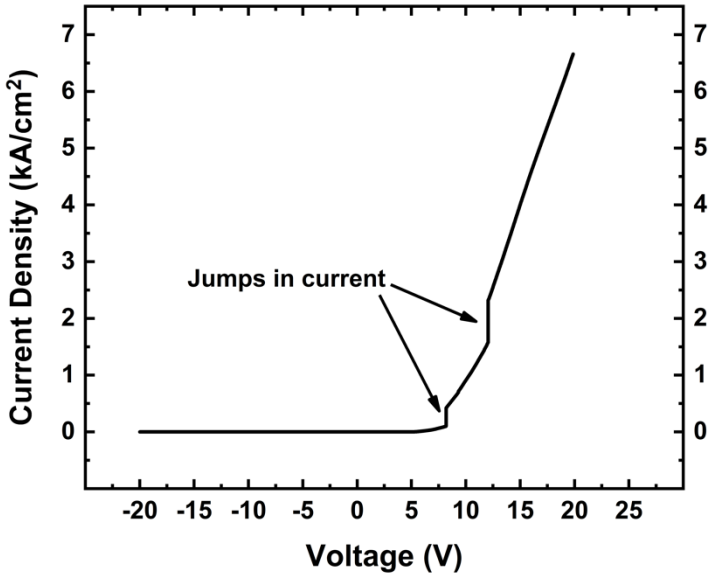


Fig. 3.26 J-V characteristics of experimental 50 μm diameter diamond SPIND indicating large 'jumps' in current due to self-heating effect

3.4.4 Experimental Dark Lock-In Thermography of Diamond SPIND

Dark lock-in thermography (LIT) measurements of an experimental 800μm diameter diamond SPIND at various forward bias voltages V_{FB} and increasing levels of current were performed using a Thermo Sensorik TS130 LIT system with a InSb 640 SM infrared camera. Although a proper calibration of the DLIT system could not be done to quantitatively asses the self-heating temperature rise during the forward operation of the diamond SPIND, an excellent qualitative match between the current and temperature profile obtained from the Silvaco ATLAS SHE simulations shown in Fig. 3.27 and Fig. 3.28 and the DLIT top-view measurements was obtained, as shown in Fig. 3.29. Comparing all the infrared images Fig. 3.29, the "hot-spot" profile changed from being concentrated at the edges of the metal contact at lower V_{FB} and current values to gradually

spreading over the entire contact area at higher V_{FB} and current values. Therefore, it can be said that at higher current values the entire contact area conducts current and therefore heats up uniformly.

The criterion for thermal breakdown of a material due to self-heating proposed by Melchior and Strutt [3.55] is an 'intrinsic' temperature T_i at which the intrinsic carrier concentration n_i is equal to the majority (or background) carrier concentration. For diamond, because of the ultra-high bandgap of 5.47 eV, $n_i \approx 3 \times 10^{-27}/cm^3$ at 300 K. Therefore, for a typical background doping of $10^{14}/cm^3$, the intrinsic temperature at which $n_i \approx 10^{14}/cm^3$ would be ~ 2700 K which is extremely large compared to T_i for other semiconductor materials like Si ($T_i \sim 550$ K), SiC ($T_i \sim 1200\ K$) and GaN ($T_i \sim 1700\ K$). Therefore, theoretically, diamond has a huge potential in high power and high temperature applications without thermal degradation.

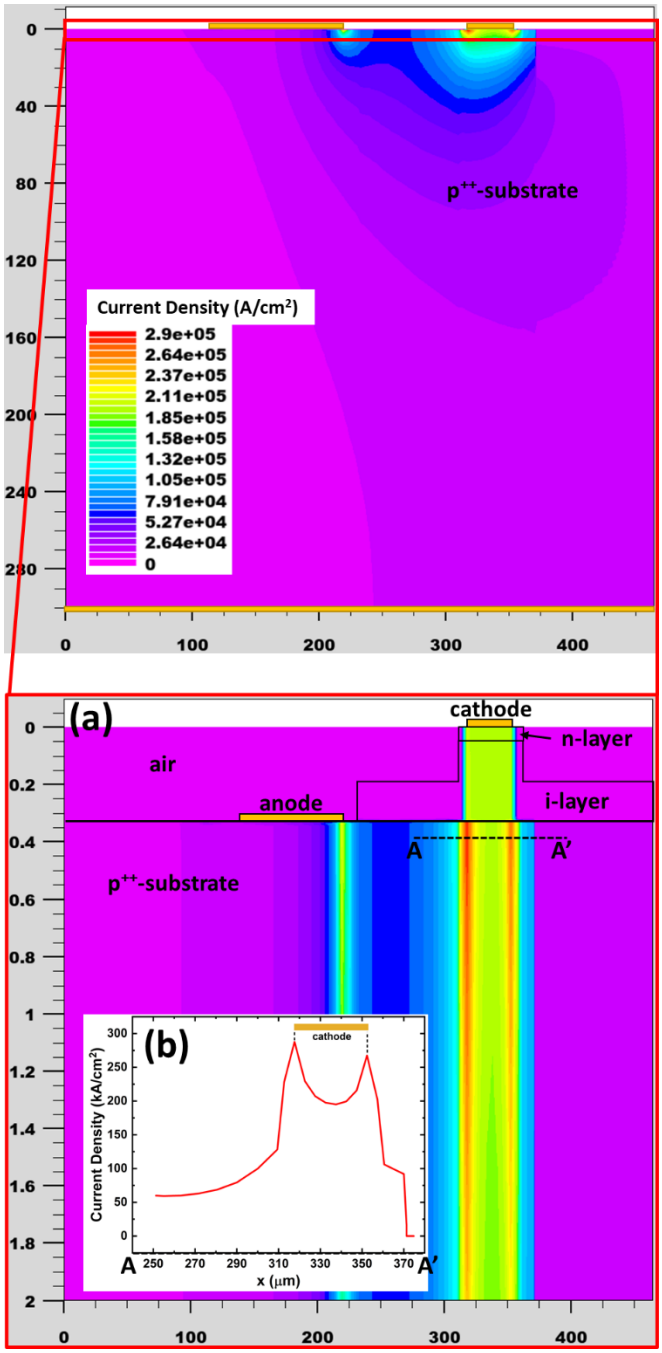


Fig. 3.27 Current density profile at an on-state bias of 20 V on a diamond SPIND without traps and for a $\kappa = 22\ \mathrm{W/cm-K}$ and $\alpha_C = 20\ \mathrm{kW/cm^2-K}$. The current density 'hot spots' are located in the p++–substrate parallel to the cathode edges, as shown in the inset (b).

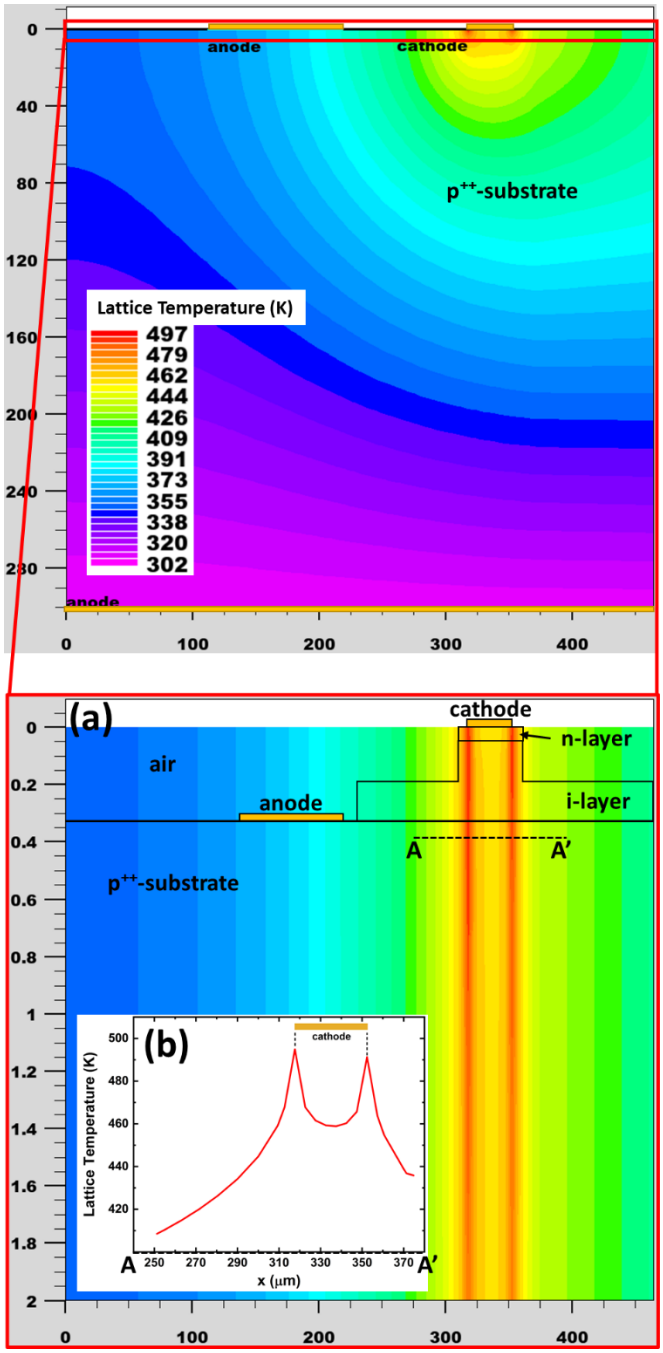


Fig. 3.28 Lattice Temperature profile over the diamond SPIND area indicating the n-layer, i-layer and p^{++}-substrate. The inset (b) shows the temperature profile along the cut-line A-A'. The thermal 'hot-spots' are concentrated in the p^{++}-substrate parallel to the cathode edges where the current density is maximum, as shown in Fig. 3.27.

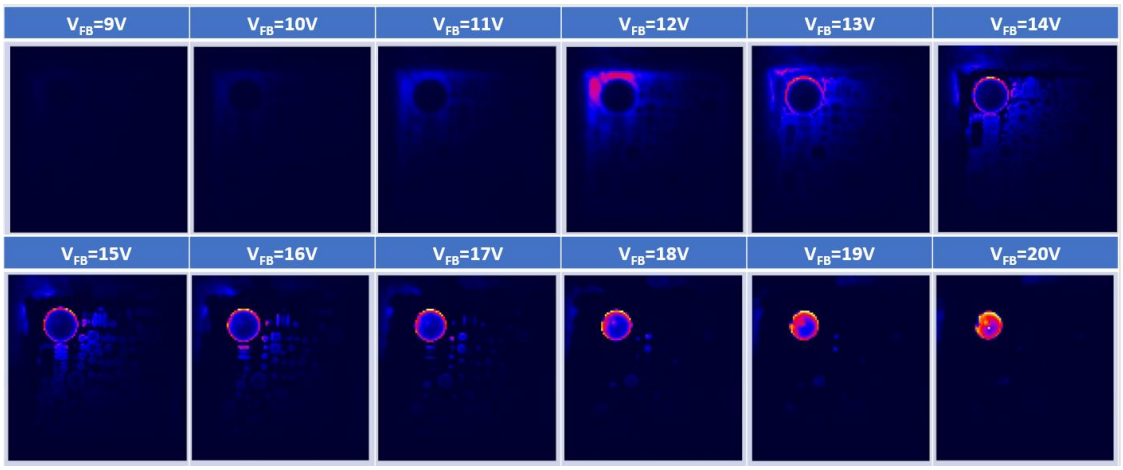


Fig. 3.29 Top-view DLIT infrared images at increasing forward biases V_{FB} and increasing current passing through an 800µm dimaeter diamond SPIND. The current (and temperature) "hot-spot" changes from being concentrated at the edges of the metal contact for lower V_{FB} to spread across the entire contact area at higher V_{FB}

3.5 Conclusion

Diamond pseudo-vertical Schottky PIN diodes have been practically demonstrated with the highest reported forward current density of $\sim 116\ kA/cm^2$ and a rectification ratio of $> 5.7 \times 10^{12}$. Analytical models are developed combined with ATLAS TCAD simulations to understand the measured hole conduction including the presence of trap levels and space charge limited conduction. From the analysis using both models, we also establish that in real diamond diodes, increasing trap levels increase the turn-on voltage V_T and decrease the current at a given forward bias thereby limiting the power handling capacity of a diamond diode while the series contact and bulk resistances are the major limiting factors for designing low $R_{ON}S$ diamond diodes. We also conclude that the ultimate performance limit in an ultra-wide bandgap material like diamond is the trap-free Mott-Gurney limit and that the $R_{ON}S$ keeps on decreasing with increasing forward bias.

The traditional BFOM based on an ohmic $R_{ON,sp}$ cannot be used for wide bandgap devices if the dominant current – voltage relationship is space charge limited, following the Mott-Gurney square law. Here, a new interpretation of the BFOM based on the Mott-Gurney square law is derived and compared to the traditional ohmic based BFOM. Silvaco ATLAS simulations are performed and are in excellent agreement with the analytically derived Mott-Gurney law based $R_{ON,sp,MG}$ for low-doped PT diodes, validating the assertion that SCLC dominates. Based on the Mott-Gurney BFOM, we also propose that the optimization of wide bandgap power devices in terms of on-state and off-state losses should be done based on the drift layer width, on-state operating voltage, and drift layer doping, with consideration of $R_{ON,sp}$ dominated by Mott-Gurney behavior. Silvaco ATLAS impact ionization simulations with Tsu-Esaki tunneling models were also performed for different drift layer doping levels and their effect on the $R_{ON,sp}$ vs. BV relation was compared to the traditionally calculated ohmic case.

Another aspect of high-power applications of diamond in terms of self-heating was also explored. Silvaco ATLAS simulations with Joule-heating and generation-recombination heating-cooling were performed with and without traps and at idealistic thermal interface resistance to establish a ~250 K range of lattice temperature rise due to self-heating. Dark lock-in thermography measurements were also performed on diamond SPINDs to qualitatively observe the current and temperature profile in practical devices.

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CHAPTER 4

DIAMOND DIODES FOR RF APPLICATIONS

4.1 Introduction

Radar and RF communication circuits such as the one shown in Fig. 4.1 [4.1], often employ power limiter circuits to protect the low noise amplifiers [4.2] and other sensitive components from unwanted high power high frequency signals. Historically, vacuum tubes, ferrite limiters, multipactors and diode limiters have comprised some of the passive RF power limiting components, whereas high frequency transistors such as MESFETs have been the active RF power limiters [4.22].

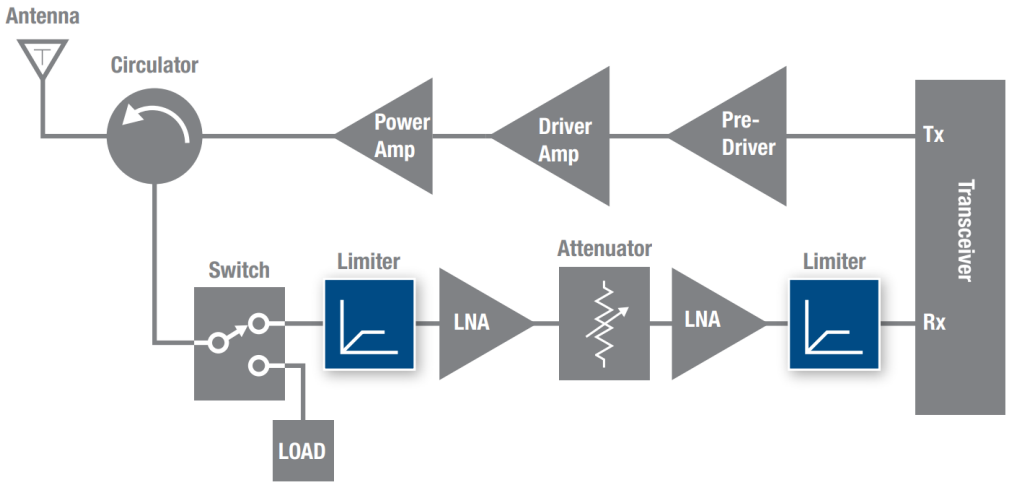


Fig. 4.1 Typical RF transceiver circuit with power limiters [4.1]

Diode limiters offer a controllable short-time-constant attenuation, noise resistance functions, and fast recovery time with no operating life limitation. The most important factor limiting the use of diodes as RF power limiters is the power handling capacity.

In a RF receiver-protector (RP) circuit with diode limiters, the diode is in a shunt configuration, as shown in Fig. 4.2(a). For low power (amplitude) modulation signals, the diodes remain off since the input signal strength is not sufficient to turn-on the diodes (Fig. 4.2(b)). The off capacitance C_{off} contributes to the insertion loss and adds directly to the noise figure of the receiver thereby limiting the bandwidth of the entire RF circuit.

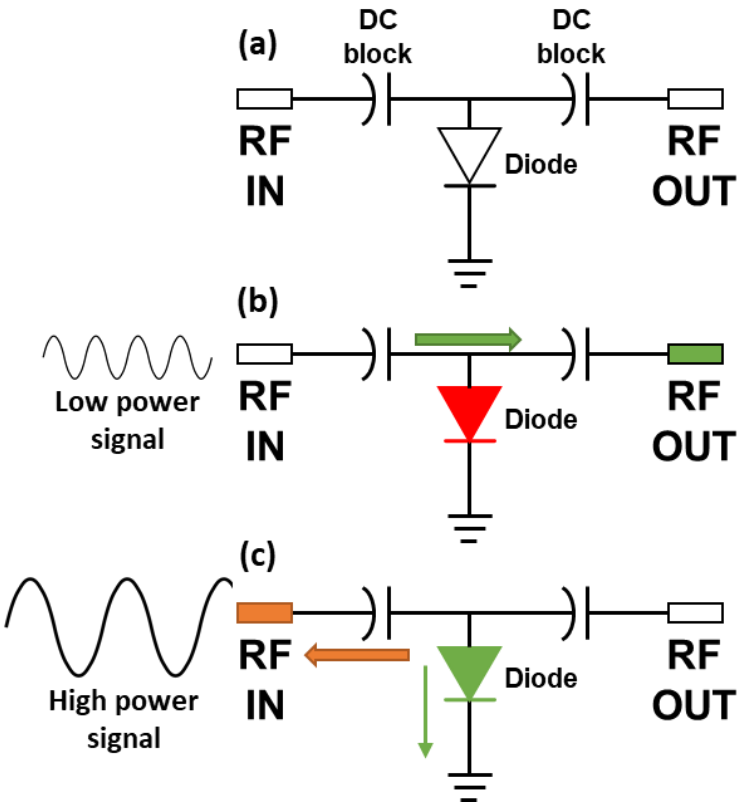


Fig. 4.2 (a) Single-stage diode power limiter in a shunt configuration with the transmission line coupled between the RF in and out ports with DC blocking capacitors. (b) The diode has high impedance at lower power input signals and almost all of the input signal is transmitted to RF out. (c) The high-power input signal turns-on the diode putting it into low impedance state and thereby reflecting most of the power back to the RF-in with a small portion being dissipated in the diode.

When high power RF signals are incident upon the RF input, the diode turns on and provides low impedance to the input port and thereby providing an impedance mismatch which reflects most of the power while absorbing part of the remaining and only allowing a small portion to be transmitted to the output port, protecting the RF circuitry beyond the power limiter (Fig. 4.2(c)).

A commonly used figure of merit for RP is,

$$F_{oc} = \frac{1}{2\pi R_{on} C_{off}} \tag{4. 1}$$

where C_{off}, is the off-state capacitance, and R_{on} is the on-state resistance. Low values of C_{off} are required to minimize insertion loss while low R_{on} ensures that the input signal is maximally reflected. Inevitably, input power will be dissipated in the receiver protector diodes and the ability to disperse the associated heat via the RP substrate is important for high power systems. As dissipated power converts to heat, the thermal impedance and temperature resilience of the limiter diode becomes the primary factor determining device lifetime, reliability, and power handling. Si and GaAs-based p-i-n and Schottky diodes and even SiC-based Schottky diodes suffer non-recoverable thermal overload with excess power dissipation. Diamond, by contrast, offers superior thermal conductivity ($\kappa = 22\ W/m - K$) and temperature resilience. Diamond also provides good charge carrier mobility and high electric breakdown field making it an ideal material for next generation high power RF limiters.

RF RP circuits are typically realized in their most fundamental form through either a single-stage PIN diode limiter with an RF choke in shunt configuration [4.3], [4.4] (Fig. 4.3(a)) or through two Schottky diodes anti-parallel to each other in shunt to the transmission line (Fig. 4.3(b)) also known as a clipper circuit [4.4], [4.5]. The single-stage PIN diode RP circuit works as described previously – by variation of the diode impedance at small and large signals and therefore causing impedance mismatch. In the clipper circuit with two anti-parallel Schottky diodes, the negative and positive peak voltages of the input signal are limited or "clipped" beyond a certain cut-in value depending on the Schottky turn-on voltage, thereby limiting the RMS power delivered to the output. In both cases, the RF insertion losses in the small-signal operation depend on the total diode impedance. Therefore, it is important to minimize C_{OFF} to maximize the total reactance $X = 1/2\pi f C_{OFF}$, which can be achieved by a thicker i-layer. On the other hand, to maximize reflection loss at large-signal RF input by maximizing the impedance mismatch and to minimize the diode power dissipation, R_{ON} needs to be minimized, which can be achieved by a thinner *n* and *i*-layer in case of a PIND or a thinner p^--layer in case of a Schottky diode. Therefore, a trade-off exists between minimizing R_{ON} and maximizing C_{OFF} at the same time. Additional stages in the RP circuit (Fig. 4.3(c)) with added anti-parallel pairs of Schottky diodes help in providing a trade-off between high power attenuation, diode power distribution and circuit complexity.

To realize diamond diodes as receiver protectors, diamond Schottky p-i-n diodes (SPINDs) were fabricated and tested at high frequencies in a shunt configuration. An

analytical high frequency model of a diode was developed to faithfully reproduce the experimental RF characteristics. Silvaco ATLAS TCAD models of diamond diodes are then developed to optimize F_{CO} for small-signal performance. Based on the optimized diode designs, RP circuits are modeled through the mixed-mode simulations in Silvaco ATLAS and performance limits of diamond diodes as RF power limiters are established. The details of RF characterization, modeling and optimization are divided into small-signal and large-signal characterization and analysis in the following sections.

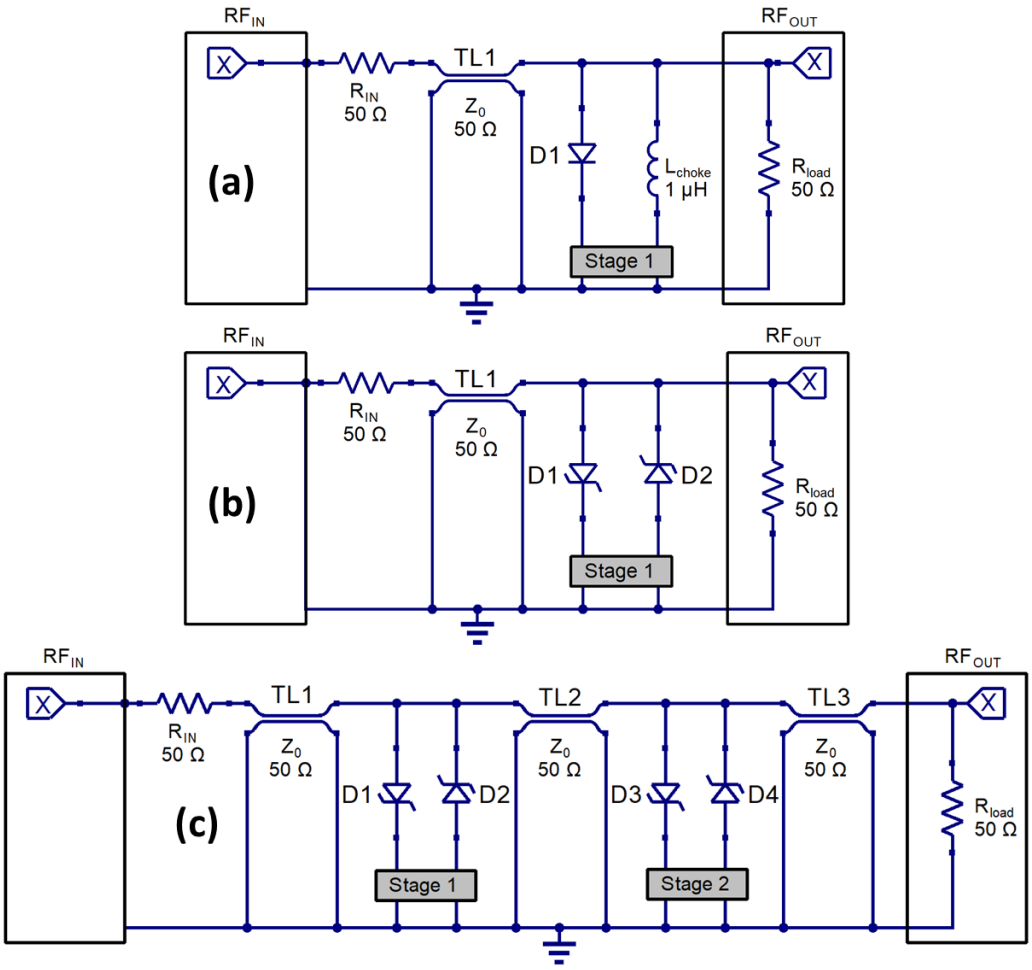


Fig. 4.3 (a) Single-stage PIND RF power limiter with RF choke (b) Single-stage clipper circuit with two anti-parallel Schottky diodes (c) Two-stage clipper circuit with two pairs of anti-parallel Schottky diodes

4.2 Small-signal Characterization and Analysis

To characterize diamond diodes at high frequencies, we first experimentally study the RF characteristics of a single diamond SPIND as a shunt element between a co-planar stripline waveguide. The shunt configuration of the diamond SPIND in a co-planar stripline is similar to a single stage transmitter – receiver protector.

4.2.1 Experimental Small-Signal Analysis

The experimental diamond SPIND's n-layer growth configuration (doping and thickness) is such that the n-layer is fully depleted by the top metal contact and it operates as a high-speed Schottky rectifier. Two port RF measurements are performed from 1 to 25 GHz at increasing diode forward bias voltages in order to observe the co-planar stripline S-parameters as a function of the decreasing diode impedance. A lumped-element model of the SPIND in shunt configuration, consisting of a diode resistance r_d in parallel with a junction capacitance which in turn are in series with a bias independent contact resistance R_C, is used to extract the diode impedance from the 1-port S-parameter measurements. Two port S-parameters are then reconstructed from the extracted diode impedance and are shown to faithfully fit with the measured S-parameters, thus providing confidence to further understand the diamond SPIND in a transmitter-receiver protection circuit. The following subsections detail the diamond SPIND, S-parameter measurements, small-signal analysis and diode lumped-element modeling.

4.2.1.1 Diamond SPIND Growth and Fabrication

The starting point for the SPIN diode growth was a high-pressure, high-temperature (HPHT) <111> diamond substrate, doped p-type with boron to a concentration of $\sim 2 \times 10^{20}\ cm^{-3}$. As described in Chapter 2, section 2.3.10, the diamond substrates were obtained from New Diamond Technology [4.14] and had dimensions of 3 mm x 3 mm with a thickness of $\sim 300\ \mu m$. Plasma enhanced chemical vapor deposition (PECVD) was used to deposit the intrinsic, and n-type diamond layers. The intrinsic i-layer had a target

thickness of $50\ nm$ and while nominally undoped the boron background concentration is typically $\sim 1 \times 10^{13}\ cm^{-3}$. After growth of the i-layer was complete a phosphorus doped n-layer with a target thickness of $300\ nm$ was deposited. The target phosphorus concentration in the n-layer is $\sim 3 \times 10^{17}\ cm^{-3}$.

Diode shunted co-planar striplines were fabricated on the surface of the PECVD coated diamond substrate. The same metal stack (Ti:Ni:Au :: 50 nm: 50 nm: 300 nm) forms a Schottky contact on the n-layer and an ohmic contact to the p-layer because of the high boron doping in the substrate.

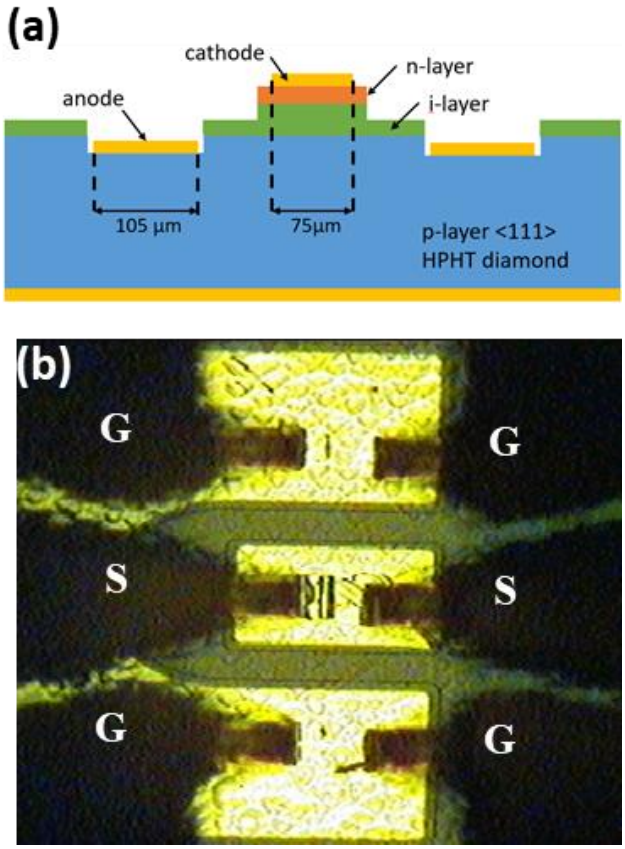


Fig. 4.4 (a) Cross-section of the diamond Schottky PIN diode. (b) GSG probe arrangement on the co-planar stripline showing the signal (S) and ground (G) probe configuration.

The cathode area of the Schottky PIN diode is $110\ \mu m \times 75\ \mu m$ and a schematic cross-section of the device is shown in Fig. 4.4(a). The surface contacts to the device form the co-planar waveguide that can be probed directly using ground-signal-ground (GSG) RF probes with a 100 µm pitch as shown in Fig. 4.4(b).

4.2.1.2 Experimental Small-Signal Parameter Extraction

The co-planar waveguides were mounted on a probe station for DC and RF measurements. The logarithmic and linear DC current-voltage (*I-V*) characteristics are

shown in Fig. 4.5(a) and Fig. 4.5(a) inset, respectively. The differential resistance, R_{ON}, is as shown in Fig. 4.5(b). The instrumentation has a noise floor of a few pA and can supply a maximum current of $1\ A$. The diode current begins to grow exponentially at a forward bias threshold of $\sim 1\ V$, similar to other diamond Schottky PIN diodes [4.7], [4.8], [4.11], [4.13]. The diode reaches the $1\ A$ current compliance at a forward bias of $9.2\ V$, corresponding to a current density of $12.1\ kA/cm^2$ which is ten orders of magnitude above the DC noise floor when the diode is in the off state. Component parameters for the small-signal model of the Schottky PIN diode shown in Fig. 4.6 have been extracted from 1-port S-parameter measurements of the shunted co-planar striplines in the frequency range $1 - 25\ GHz$. RF probes from MPI Corp. [4.16] with a ground-signal-ground (GSG) configuration were calibrated with an impedance substrate standard to establish the measurement planes at the input and output of the co-planar striplines.

The one-port reflection coefficient, S_{11}, was recorded for bias voltages in the range $0\ V$ to $7.6\ V$,as shown in Fig. 4.7, then converted to the diode impedance, Z_d, using the standard formula

$$Z_d = Z_o \frac{1 + S_{11}}{1 - S_{11}} \qquad (4.2)$$

for a waveguide with characteristic impedance Z_o. The magnitude of Z_d is shown in Fig. 4.8 for a range of forward bias voltages. A lumped-element model for a PN junction diode consists of a parallel combination of the bias-dependent diode resistance, R_d, and junction capacitance, C_d. These in turn are in series with a bias independent contact resistance, R_C,

as shown in Fig. 4.6. The resulting impedance due to the shunt connected diode can therefore be expressed according to (4. 3)

$$Z_d = R_C + \frac{R_d}{1 + j\omega R_d C_d} \tag{4. 3}$$

The data in Fig. 4.8 have been fitted to (4. 3) and used to extract the diode parameters R_C, R_d, and C_d. The solid lines in Fig. 4.8 were obtained using $R_C = 3\ \Omega$ for all bias voltages as expected for bias independent contact resistances. This value of R_C corresponds to a specific contact resistance of $0.25\ m\Omega - cm^2$. An excellent fit to the measured Z_d is obtained using a constant diode capacitance of $C_d = 1.44\ pF$, equivalent to $17.5\ nF/cm^2$. Assuming a junction capacitance $C_d = \epsilon A/T_d$ gives a depletion layer thickness, T_d, of $0.29\ \mu m$, consistent with the target thickness of $\sim 0.3\ \mu m$ The diode resistance, R_d, varies with applied bias and the extracted values (including the contribution from the 3 Ω contact resistance) are shown as open circles in Fig. 4.8.

The good agreement between the diode resistance determined from the DC *IV* curves and from the RF measurements, along with the excellent fit to the Z_{11} data, suggest that the extracted Schottky PIN diode model is adequate for application simulations up to $25\ GHz$.

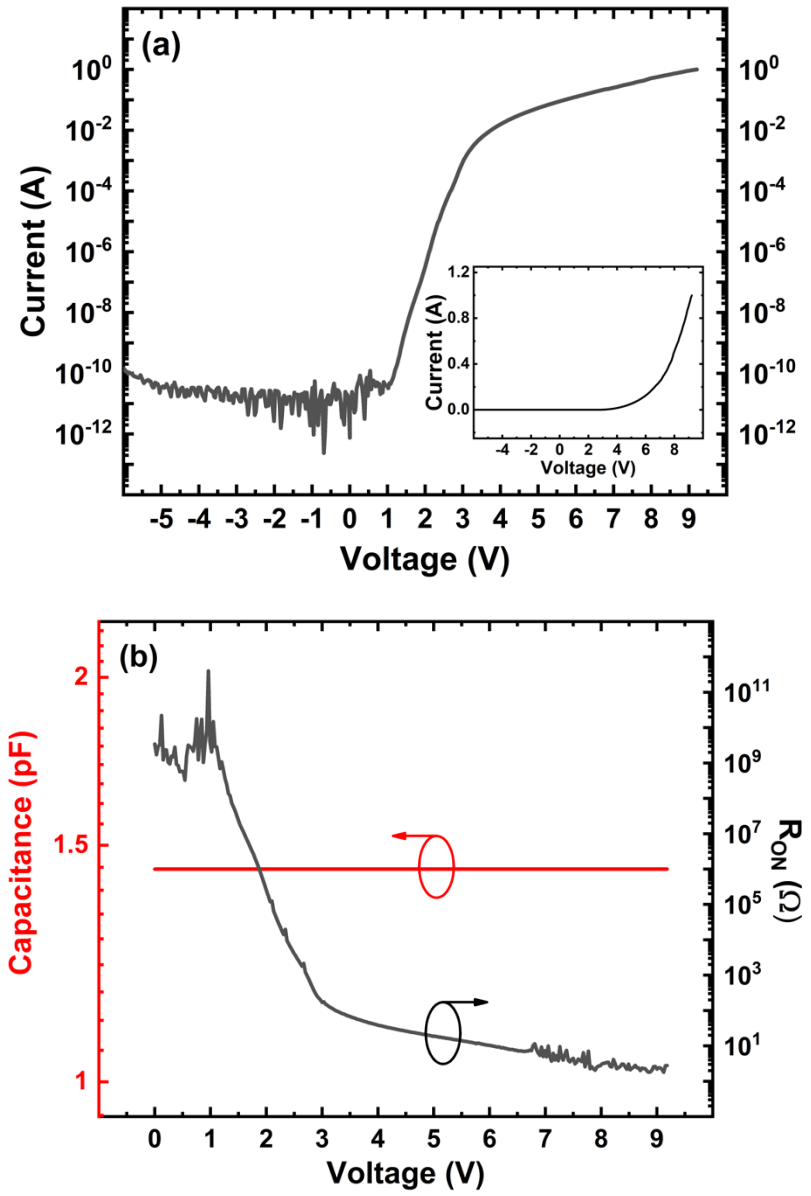


Fig. 4.5 (a) DC logarithmic and linear (inset) I-V characteristics and (b) differential resistance (black) along with the capacitance (red) extracted from the RF s-parameters of a diamond Schottky PIN diode with an area of 110 µm x 75 µm

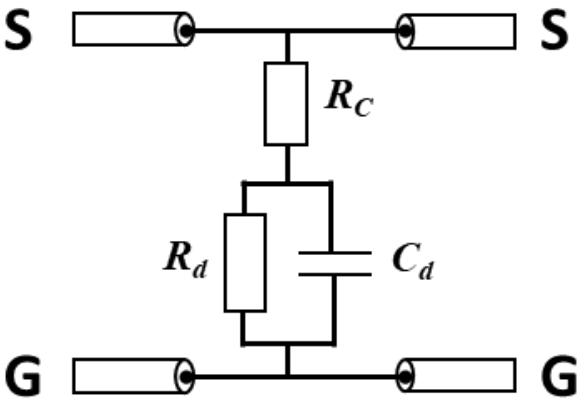


Fig. 4.6 Small signal model of diamond SPIND with signal (S) and ground (G) ports, contact resistance R_C, diode differential resistance R_d and a junction capacitance C_d

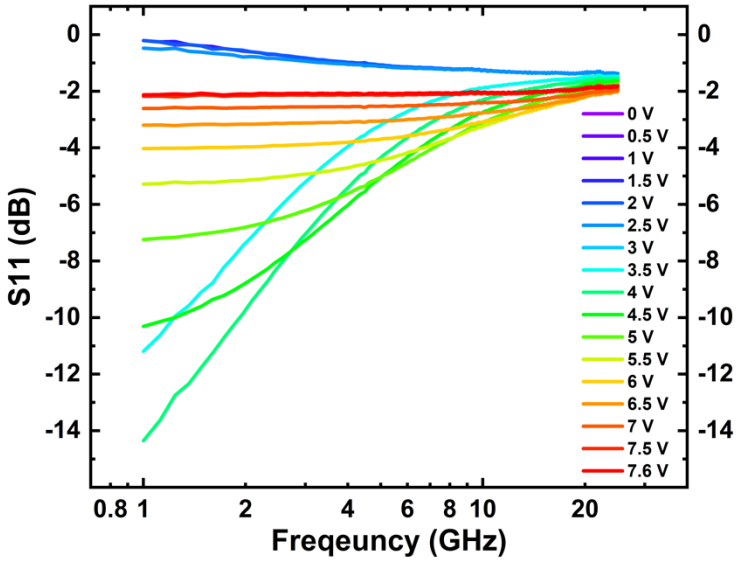


Fig. 4.7 1-port S11 characteristics of the diamond Schottky PIN diode for frequencies ranging from 1 GHz to 25 GHz

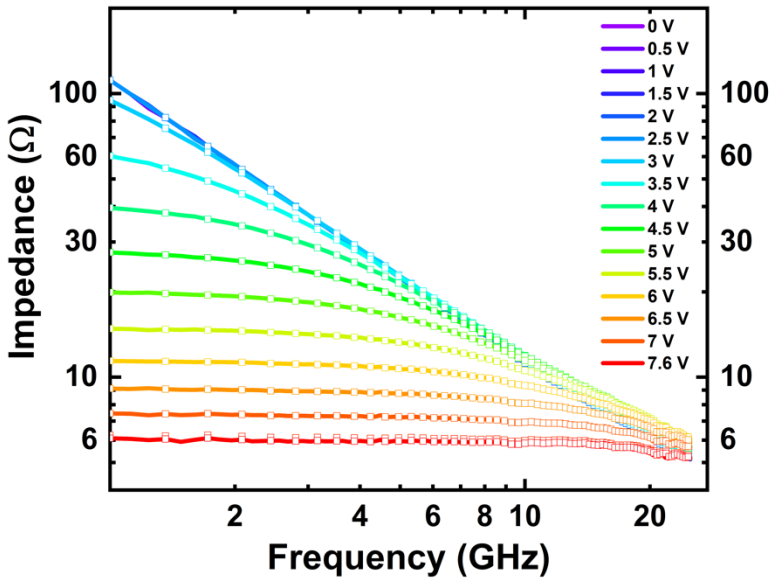


Fig. 4.8 Magnitude of the diode impedance extracted from 1-port s-parameter measurements (open squares) for various bias voltages. The solid lines are the fit to the data used to extract the small-signal parameters of the lumped-element model shown in Fig. 4.4(c)

4.2.1.3 Two-Port Measurements with Diamond SPIND in Shunt

The diode shunted co-planar waveguide was configured for two-port RF measurements as shown in the photograph of Fig. 4.4(b). The forward transmission, S_{21}, and the input reflection, S_{11}, were recorded from $1 - 25\ GHz$ with bias voltages of $0 - 7.8\ V$ applied to the diode. The measured data is shown as open symbols in Fig. 4.10 along with simulated values of S_{21} and S_{11} using the extracted diode impedance in equations (4. 4) and (4. 5) below.

$$S_{11} = \frac{Z_0 // Z_d - Z_o}{Z_0 // Z_d + Z_o} \tag{4. 4}$$

$$S_{21} = \frac{2Z_0//Z_d}{Z_0//Z_d + Z_o} \quad (4.5)$$

At zero bias the measured insertion loss from the diamond diode shunt is $0.3\,dB$ and increases to $14\,dB$ at a forward bias of $7.6\,V$, as shown in Fig. 4.9.

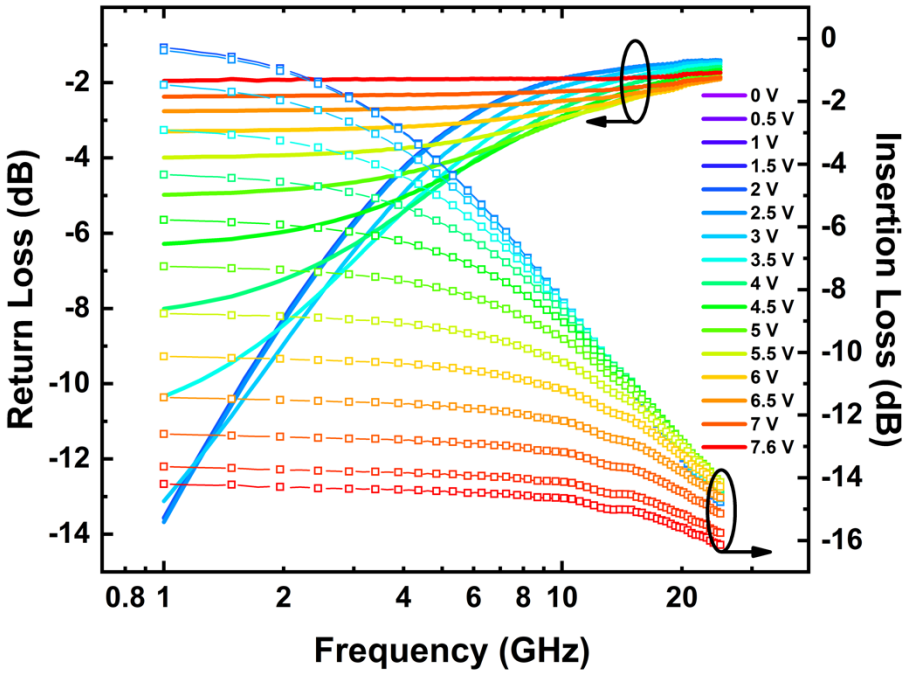


Fig. 4.9 Return and insertion losses measured from the 2-port s-parameter measurements of the diamond SPIND

For these diodes with a contact resistance of 3 Ω, the simulated forward transmission in the on-state suggests that the maximum return loss is 19 dB with a corresponding S_{11} of -1 dB. To achieve a return loss of 30 dB, as shown by the dashed line in Fig. 4.10, the contact resistance would have to be reduced to 1 Ω or less, corresponding to a specific contact resistance of $8.3 \times 10^{-5}\ \Omega - cm^2$. Diamond Schottky PIN diodes with specific on-

resistance of $< 5 \times 10^{-5}\ \Omega - cm^2$ have been demonstrated [[4.8], [4.12]] suggesting that with further optimization the shunt on-resistance can be reduced below 0.6 Ω.

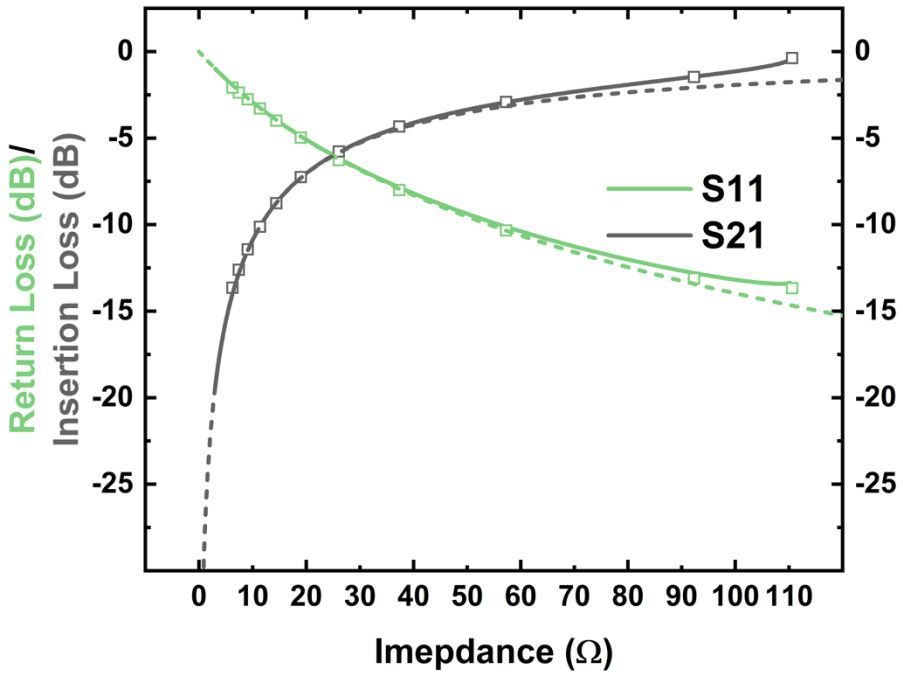


Fig. 4.10 Two-port measurements at 1 GHz (open symbols) of the forward transmission, S_{21}, and the input reflection, S_{11}, of the co-planar waveguide as a function of the impedance of the Schottky PIN diode shunt. As the diode bias is increased from 0 V to 7.6 V the diode impedance falls to 4.3 Ω and the insertion loss increases from 0.3 dB to 14 dB. The solid lines are the fit to the data using the lumped-element diode model with a contact resistance of 3 Ω and diode capacitance of 1.44 pF. If the diode resistance in the on-state is reduced to 1 Ω the return loss increases to 30 dB, dashed line.

At 1 GHz the off-state insertion loss of 0.3 dB is adequate for most receiver protector applications. However, at higher frequencies such as S-band ($2 - 4\ GHz$) the relatively high capacitance of 1.4 pF leads to an insertion loss approaching 3 dB which is unacceptable. At 4 GHz a capacitance C_d of 0.35 pF is required to recover the forward transmission and input reflection shown in Fig. 4.10. A four-fold reduction in C_d could be achieved with the current device PIN layer structure by a corresponding reduction in its

area. However, this would increase the contact-resistance, R_C, to $12\ \Omega$ and substantially reduce the input reflection in the on-state. Alternatively, the value of C_d can be reduced to $0.35\ pF$ by increasing the diode intrinsic layer thickness from $0.29\ \mu m$ to $1.16\ \mu m$. If this can be done whilst also reducing the specific contact resistance to $\sim 5 \times 10^{-5}\ \Omega - cm^2$ diamond Schottky PIN diodes may have useful applications as high-power receiver protectors at S-band frequencies.

4.2.2 Parameter Optimization with Silvaco ATLAS

As discussed in the previous section, to achieve lower insertion losses at higher frequencies and low power, the impedance needs to be lowered by reducing the contact resistance, R_C, the diode resistance, R_d, or the diode capacitance, C_d. R_C can easily be eliminated in the simulations, as it is a more of a diamond-metal interface and fabrication process dependent parameter. Silvaco ATLAS simulations of different epitaxial thicknesses of n and i-layers were therefore performed to optimize R_d and C_d. Mainly, two structures of diamond diodes are simulated i.e., diamond PIN diode (PIND) with a highly doped ($5 \times 10^{19}/cm^3$) n-layer with ohmic contacts to both cathode and anode terminals and second, a diamond Schottky $- p^- - p^{++}$ (SpPD) diode with a p^- drift layer of low doping ($10^{17}/cm^3$) and a Schottky cathode contact. Different values of C_{off} and R_{ON} are obtained by varying the n and i-layer in the PIND and p^--layer in the SpPD. Following sub-sections detail this optimization process and provide the ideal limits of diamond diodes at high frequency.

4.2.2.1 Diode Capacitance

Space charge limited (SCL) conduction plays an important part in determining the carrier transport in the on-state of a diamond diode, as was established in chapter 2. The standard C-V Shockley model based on the depletion approximation of a diode is the sum of depletion and diffusion capacitances which dominate at low and high currents, respectively [4.17]. The depletion capacitance C_{dep} is derived from the depletion approximation while the diffusion capacitance depends on the diffusion length and minority carrier concentrations and also exponentially on the forward bias voltage, as shown in

$$\begin{aligned} C_D &= C_{dep} + C_{diff} \\ &= A\sqrt{\frac{q\epsilon N_A N_D}{2(N_A+N_D)\phi_{bi}}} \cdot \sqrt{\frac{\phi_{bi}}{\phi_{bi}-V}} + \frac{qA}{2\phi_T}\exp\left(\frac{V}{\phi_T}\right)\left(L_n n_p + L_p p_n\right) \end{aligned} \quad (4.6)$$

where A is the diode area, ϵ is the diamond material permittivity, N_A and N_D are the ionized p-type and n-type doping concentrations, respectively, ϕ_{bi} is the built-in voltage, $\phi_T = k_B T/q$ is the thermal voltage, V is the applied voltage on the diode, n_p and p_n are the electron and hole minority carrier concentrations, respectively and L_n and L_p are the electron and hole diffusion lengths, respectively. However, due to the SCL nature of the injected carriers during the on-state of the diodes, the diffusion lengths are no longer constants and are in fact a function of the on-state voltage [4.18]. As the diode is increasingly forward biased, the diffusion capacitance rises due to the diffusion of the injected carriers over the thermionic emission (TE) barrier. The increasing diffusion

capacitance eventually gives way to a downward trend due to the drift dominated SCL regime where the charge neutrality is disturbed as the transit time of the injected charges decreases more than the dielectric relaxation time. Therefore, a peak in capacitance can be observed both experimentally and from Silvaco ATLAS drift-diffusion simulations, as shown in Fig. 4.11. The competing drift and diffusion mechanisms can be observed from the drift and diffusion currents from the simulations, as shown in Fig. 4.12. Initially, for $V_{ON} < V_{peak} = 5.7\ V$ (for simulations, Fig. 4.11), the diffusion current is dominant in the n and i-layers. Beyond 5.7 V, the drift current dominates the carrier transport and thereby transient time effects come in place.

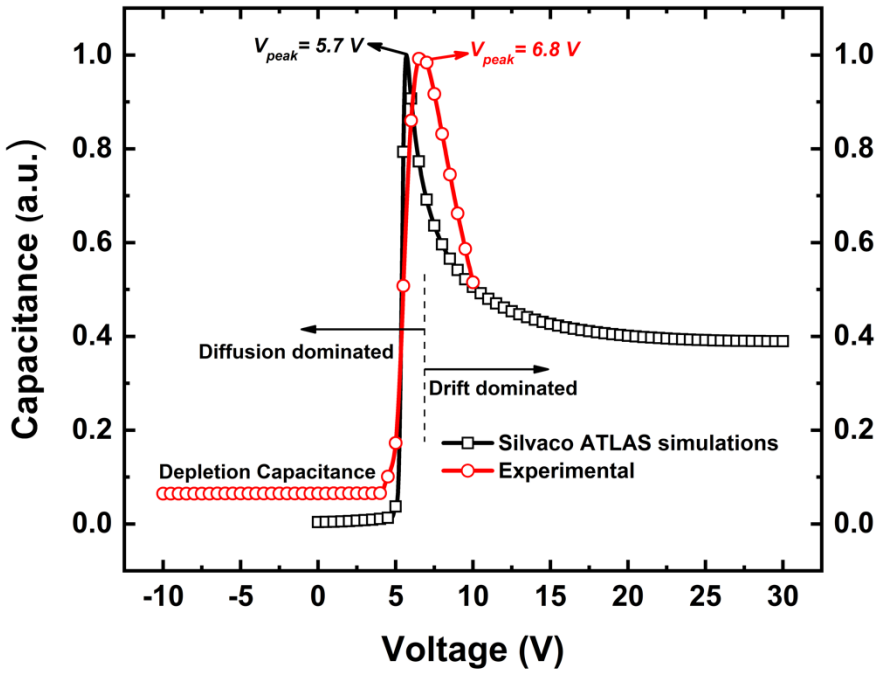


Fig. 4.11 C-V characteristics of diamond SPINDs observed from Silvaco ATLAS simulations and experimental measurements

The diffusion length can no longer be derived from the standard Einstein relation and the dielectric relaxation of the injected charge needs to be taken into account while formulating the C-V relationship, $C = AdQ/dV$. Tripathi et. al. [4.18] have proposed a $C^{-2/3} - V$ relationship (equation (4. 7)) whereas Boukredimi [4.19] has formulated a more complex proportionality.

$$C_{diff} = \frac{qAp_0 d}{2}\left(\frac{k_B T}{q}\right)^{1/2}(V - V_{bi})^{-3/2} \tag{4. 7}$$

where p_0 is the carrier concentration in the drift layer of width d and A is the diode area.

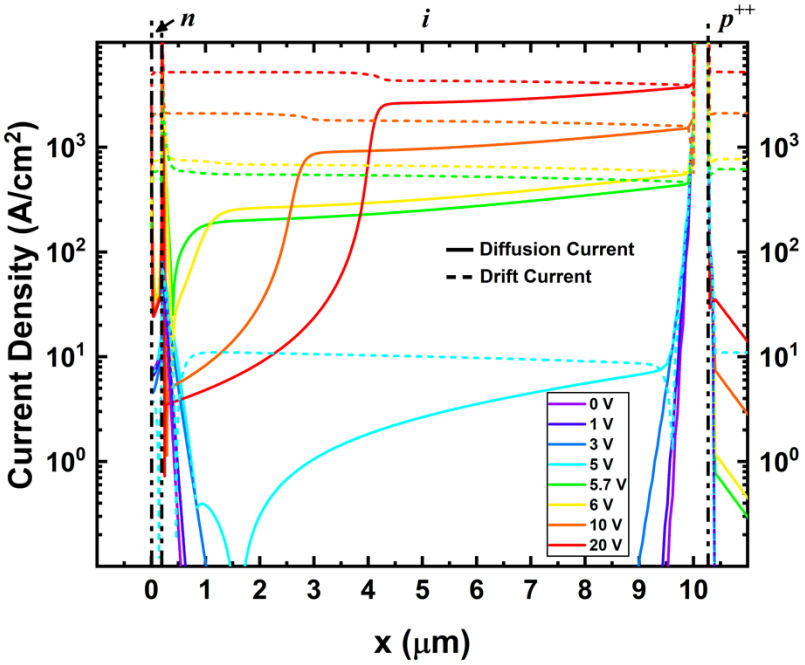


Fig. 4.12 Drift and diffusion currents at 1 GHz for varying on-state voltages in a diamond PIND

However, both formulations explicitly show the drift-diffusion components of the capacitance separated by $V_{peak} \sim V_{bi}$, where V_{bi} is the built-in voltage. In the case of a

diamond PIND V_{bi}, and therefore the V_{peak}, is the bandgap of diamond $\sim 5.47\ V$ whereas for the case of a diamond SpPD, V_{bi} is dependent on the *i*-layer thickness. For higher frequencies where the change in AC voltage is comparable to the transit time of carriers, the diffusion length is proportional to the changes in the transit time of the drifting carriers. Therefore, as formulated by Tripathi [4.18], the diffusion length becomes

$$\partial L_{n,p} = \sqrt{\frac{k_B T}{q} \frac{d^2}{V_{bi} - V}} \tag{4. 8}$$

In the RF RP circuits, the insertion loss at low power levels needs to be minimized by minimizing the C_{off}.

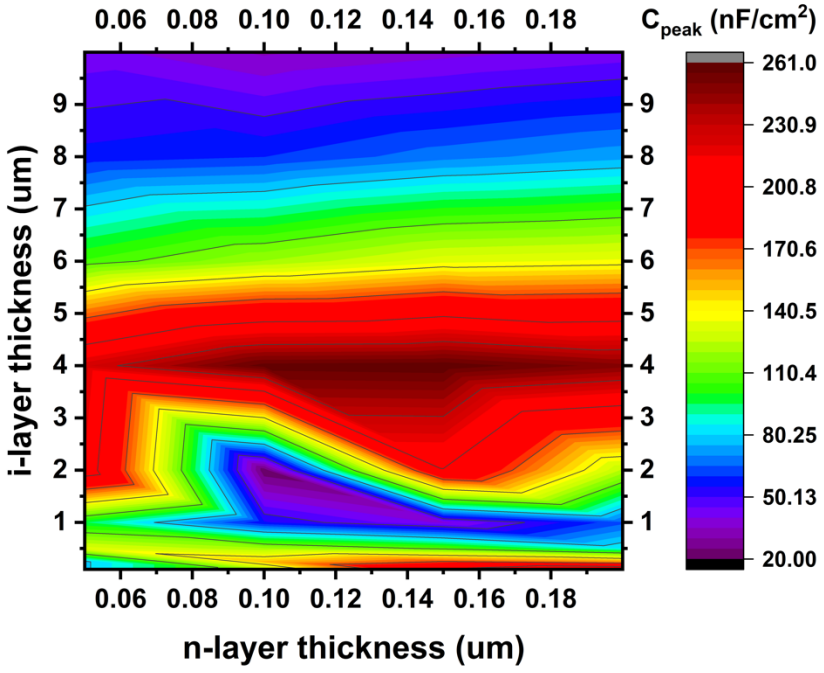


Fig. 4.13 C_{peak} variation with *n* and *i*-layer thicknesses in a diamond PIND at 1 GHz

Since the low power levels would correspond to r.m.s. voltages near the V_{bi} of the shunt diodes, the peak diffusion capacitance is minimized through different structural simulations of the diamond PINDs and SpPDs. Fig. 4.13 shows a contour plot of the Silvaco ATLAS simulated capacitance (nF/cm^2) for a diamond PIND with different *n* and *i*-layer thicknesses. A minimum capacitance of $\sim 20\ nF/cm^2$ is observed for an n-layer of $\sim 0.1\ \mu m$ and an *i*-layer of $\sim 2\ \mu m$ of the PIND. In the case of a diamond SpPD, the capacitance is a decreasing function of the p^--layer thickness, as shown in Fig. 4.14. A minimum value of 6.92 nF/cm^2 for a p^--layer thickness of 10 µm.

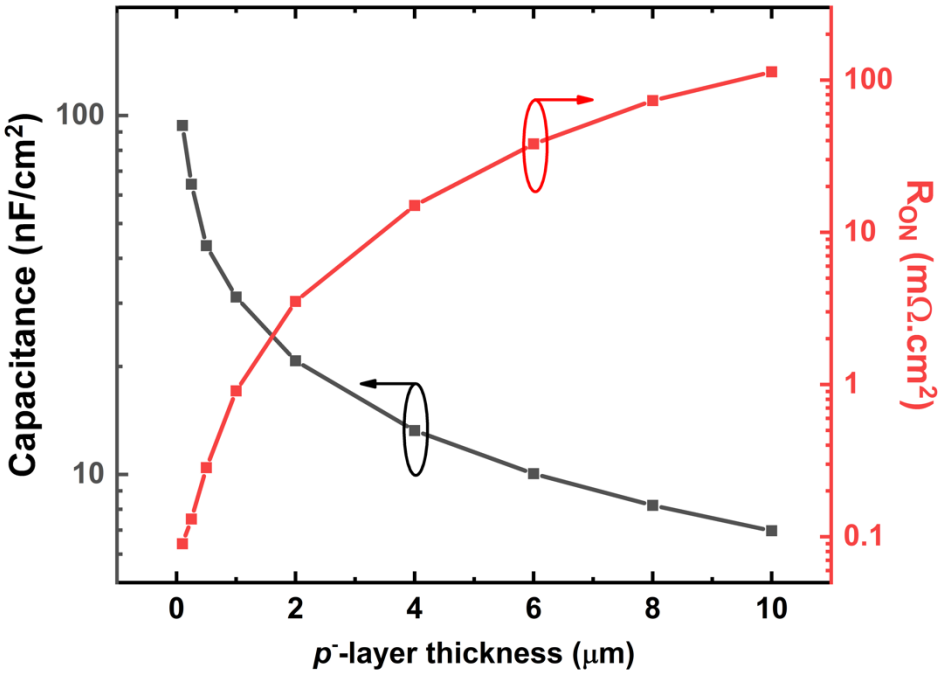


Fig. 4.14 C_{peak} and R_{ON} variation of a diamond SpPD for varying p^--layer thickness at 1 GHz

4.2.2.2 Differential ON-resistance

For high power levels which correspond to on-state voltages well into the SCL drift dominated I-V region, similar structural optimization was done to find the minimum R_{ON}. As established in chapter 3, the space charge limited current (SCLC) dominates for higher on-state voltages and the R_{ON} is a decreasing function of voltage i.e.,

$$R_{ON,sp,MG} = \frac{4}{9\epsilon_r\epsilon_0\mu}\frac{d^3}{V} \tag{4. 9}$$

However, with a finite p^{++}- substrate resistivity the R_{ON} saturates to a constant value dictated by the p^{++}-layer thickness. Fig. 4.15 shows a contour plot of R_{ON} variation with *n* and *i*-layer thicknesses for a diamond PIND.

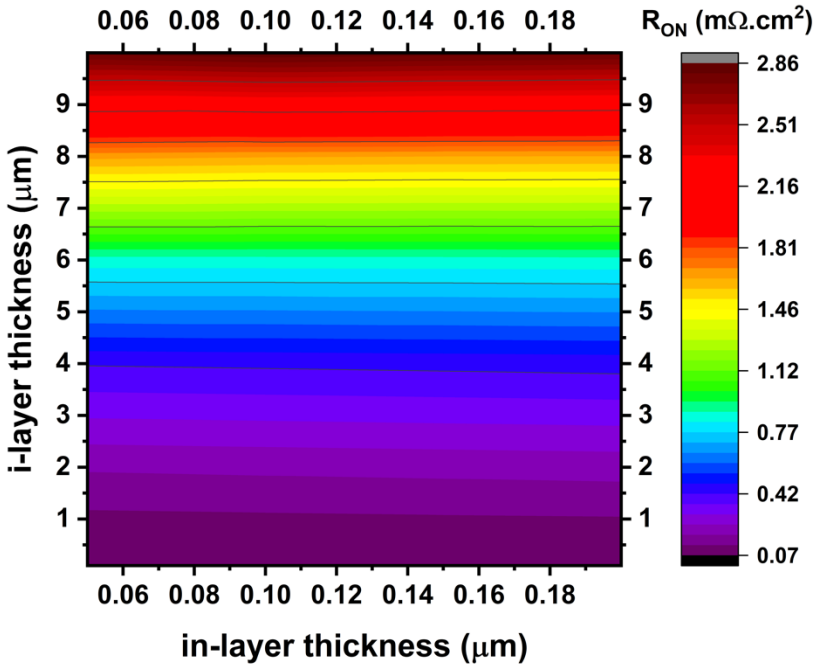


Fig. 4.15 R_{ON} variation of a diamond PIND with n and i-layer thicknesses at 1 GHz.

As can be seen, the R_{ON} monotonously increases with i-layer thickness whereas the n-layer thickness has no effect, with a minimum value of 0.07 mΩ − cm^2 observed at an i-layer thickness of 0.1 µm. In the case of a diamond SpPD, the R_{ON} minimum value of 0.09 mΩ − cm^2 is achieved at a p^--layer thickness of 0.1 µm, as shown in Fig. 4.14 .

4.2.2.3 F_{CO} Figure of Merit

The F_{CO} figure of merit from equation (4. 1) is calculated for both diamond PIND and SpPD, as shown in Fig. 4.16 and Fig. 4.17. For diamond PINDs a maximum F_{CO} value of 38.2 GHz is obtained for an n-layer of $\sim 0.1\ \mu m$ and an i-layer of $\sim 2\ \mu m$ whereas for the diamond SpPD a maximum value of 18.9 GHz is obtained at a p^--layer thickness of 0.1 µm.

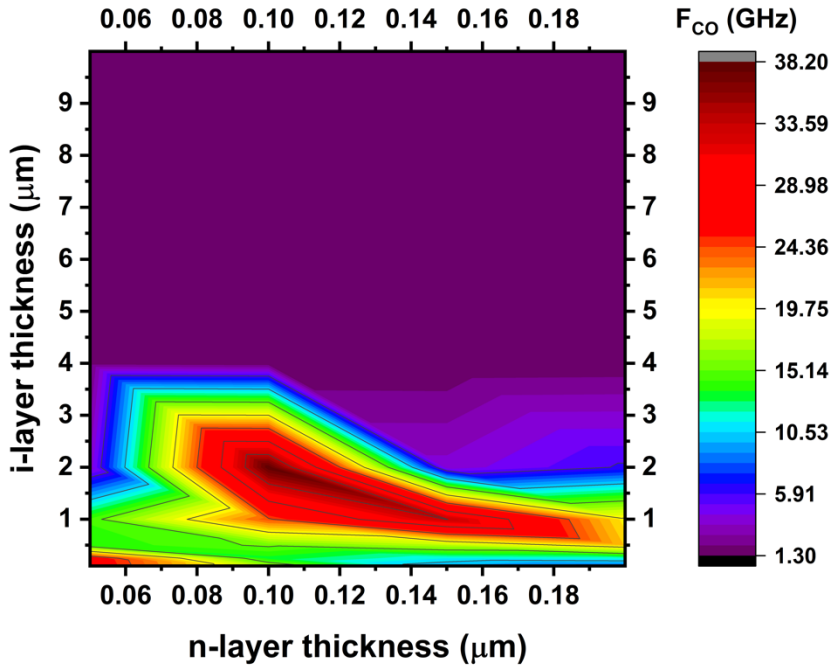


Fig. 4.16 F_{CO} variation of a diamond PIND with n and i-layer thicknesses at 1 GHz.

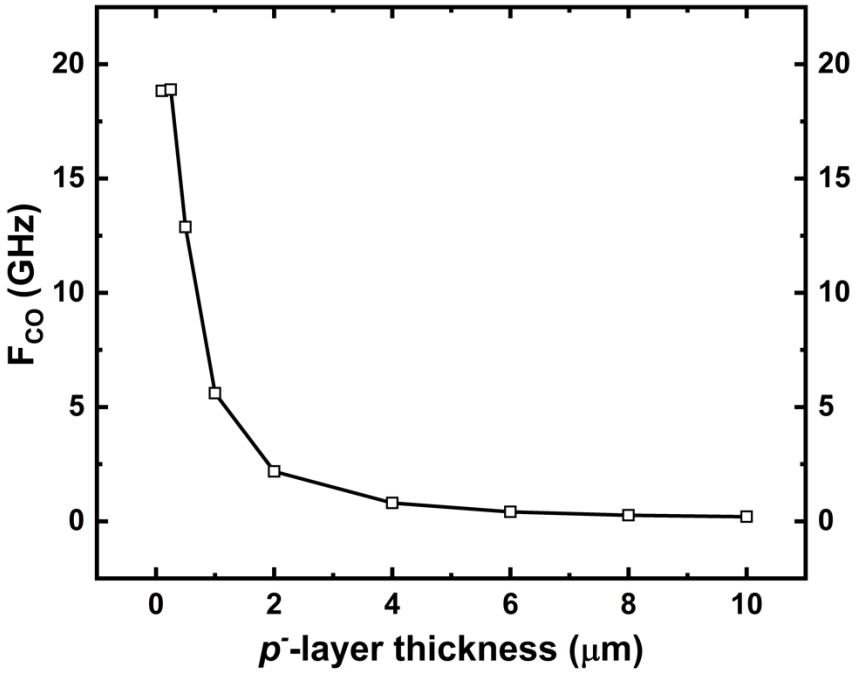


Fig. 4.17 F_{CO} variation of a diamond SpPD with p^--layer thickness at 1 GHz

It can therefore be observed from figures Fig. 4.13 to Fig. 4.17 that for a diamond PIND with bipolar current conduction, the C_{peak} or C_{OFF} is the dominant factor for maximizing F_{CO} whereas for a diamond SpPD with unipolar current conduction. R_{ON} is the dominant factor. This is expected since the charge retention capability of a bipolar diamond PIND in the i-layer is considerably higher than the diamond SpPD, owing to both electron and hole minority carrier concentrations. In diamond SpPDs, a fast recovery of charges is expected as the unipolar charge (holes) are quickly swept away from the drift region. Therefore, diamond PIND are suitable for a diode limiter RP whereas diamond SpPD are suitable for an anti-parallel clipper power limiter RP.

4.3 Large-signal Analysis and RF Reiver Protectors

Full RP circuits at 1 GHz were analyzed through large-signal mixed-mode Silvaco ATLAS simulations. The optimized configuration of the diamond PIND used for the RP circuits is with an n-layer of 0.1 μm thickness and $5 \times 10^{19}/\text{cm}^3$ of P doping, an i-layer of 2 μm and a 90 μm thick p^{++}- substrate with $2 \times 10^{20}/\text{cm}^3$ B doping whereas the optimized SpPD design is with a p^{-}- layer of 0.1 μm thickness and $10^{17}/\text{cm}^3$ B doping. For comparison purposes two different diode diameters, 200 μm amd 2100 μm, were simulated for the diamond PIND in the RP test circuits. The RP test circuits with SpPDs were simulated with a 200 μm diode diameter. In total, the following four RP test configurations were simulated and compared:

a) 1 stage with a single transmission line (TL) of characteristic impedance Z_0 of 50 Ω, a load resistance R_{Load} of 50 Ω and with 1 PIND (Fig. 4.3(a)) with n-layer thickness of 0.1 μm and doping of $5 \times 10^{19}/\text{cm}^3$, an i-layer thickness of 2 μm, a p^{++}-substrate of 90 μm and with a circular cathode diameter of 200 μm or "1x1-200 μm-PIND"

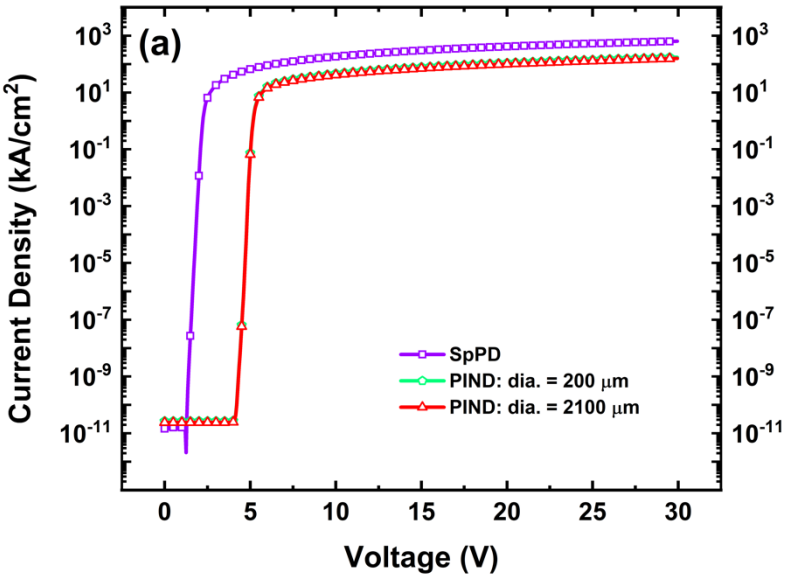
b) 1 stage with a single TL of Z_0 of 50 Ω, a load resistance R_{Load} of 50 Ω and with 1 PIND (Fig. 4.3(a)) with n-layer thickness of 0.1 μm and doping of $5 \times 10^{19}/\text{cm}^3$, an i-layer thickness of 2 μm, a p^{++}-substrate of 90 μm thickness and with a circular cathode diameter of 2100 μm or "1x1-2100μm-PIND"

c) 1 stage with a single TL of Z_0 of 50 Ω, a load resistance R_{Load} of 50 Ω and with 2 anti-parallel SpPDs Fig. 4.3(b) with p^{-} drift layer of 0.1 μm and $10^{17}/\text{cm}^3$ doping, a p^{++}-substrate of 90 μm and with a circular cathode diameter of 200 μm or "1x2-SpPD"

d) 2 stages with two TLs of Z_0 of 50 Ω each, a load resistance R_{Load} of 50 Ω and with 4 anti-parallel SpPDs Fig. 4.3(c) with p^- drift layer of 0.1 µm and $10^{17}/\text{cm}^3$ doping, a p^{++}-substrate of 90 µm and with a circular cathode diameter of 200 µm or "2x4-SpPD"

4.3.1 DC Characteristics of Optimized PIND and SpPD

The DC J-V characteristics of all the optimized diamond diodes used in the simulations are as shown in Fig. 4.18. Fig. 4.18(b) shows the differential R_{ON} for all the three diodes. Saturated R_{ON} values of 0.04 mΩ − cm^2 (0.14 Ω), 0.15 mΩ − cm^2 (0.5 Ω) and 0.17 mΩ − cm^2 (0.04 Ω) are obtained for the SpPD, 200 µm and 2100 µm PIND, respectively.



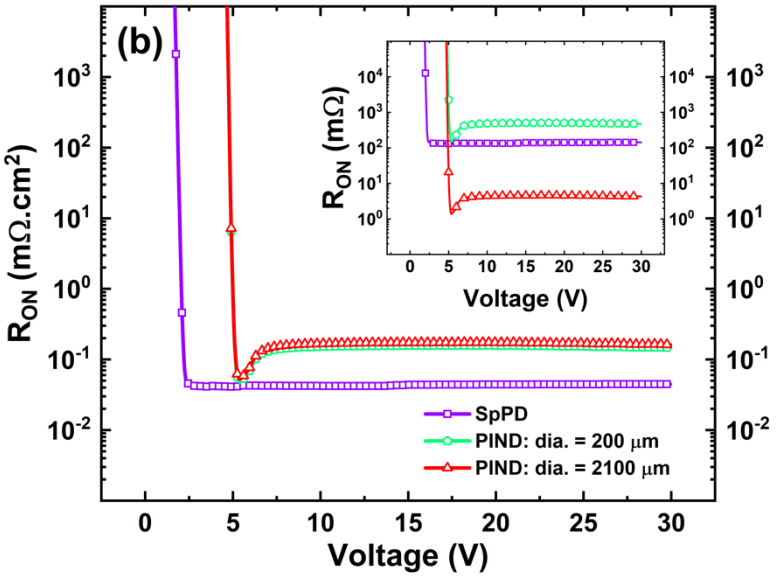


Fig. 4.18 Silvaco ATLAS simulated (a) DC J-V characteristics and (b) R_{ON} (mΩ − cm^2) and R_{ON}(Ω) (inset) vs voltage characteristics of the SpPD, 200 μm and 2100 μm PIND

4.3.2 Spike Leakage, Flat Leakage and Reverse Recovery Time

Initially, when the large RF signal burst is incident upon the RF-in, the diode limiters are still in their high impedance state. In the diodes, a finite transit time is required for the charge carriers to travel across the i-layer of the diode thereby allowing a small portion of the large incident power to propagate to the output terminal for a very short duration. This "spike" in the output power is termed as the spike leakage power of the diode limiter circuit, as shown in Fig. 4.19. When the diode is fully turned on and the diode has reached its low impedance state, a small portion of the input signal does not reflect back to its source. Some of this energy propagates past the limiter stage to the limiter circuit's load, which is termed as flat leakage Fig. 4.19. The diode dissipates the balance of the input energy, through joule heating. An RF signal level forces the series resistance of the limiter PIND to its minimum

value. If the input-signal amplitude increases further, the output power from the limiter also increases on a decibel-for-decibel basis, because the finite, nonzero minimum impedance of the diode remains fixed at approximately some saturation impedance R_{SAT} that can comprise of the diode's contact and series resistance in combination with the circuit series resistance. Consequently, the reflection loss caused by the impedance mismatch also remains constant. The isolation produced by the attenuation of input power can be given as

$$\text{Isolation} = 20\log\left(\frac{Z_0}{2R_{ON}}\right) \tag{4. 10}$$

where Z_0 is the characteristics impedance of the RF-in to RF-out transmission line and R_{ON} is the diode on-resistance. Isolation ratios of 51, 40 and 61 can be expected from the SpPD, 200 μm PIND and 2100 μm PIND, respectively.

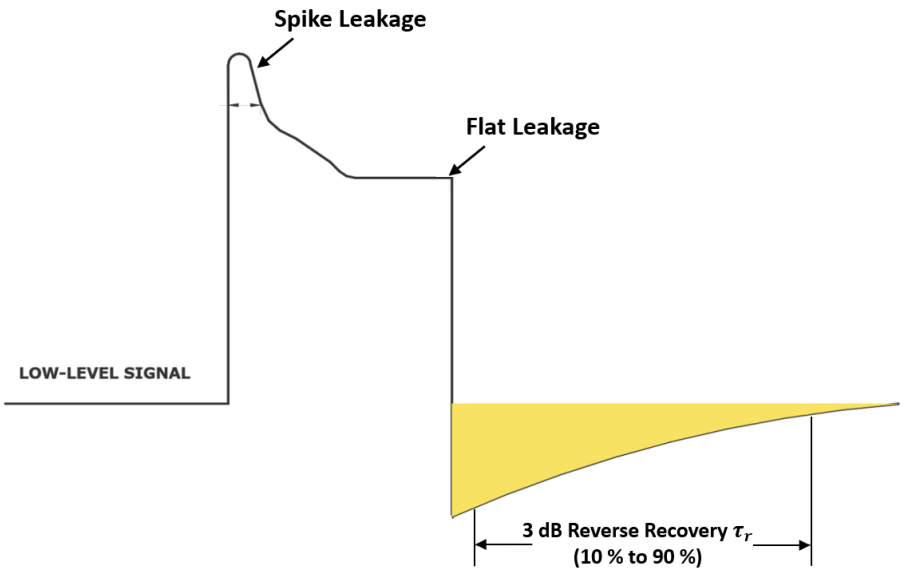


Fig. 4.19 Large signal RF spike leakage, flat leakage and reverse recovery through a RF power limiter circuit

At the end of the RF-input-signal burst and briefly afterward, free charge carriers are present in the diode *i*-layer, so its impedance remains low. During this interval, the limiter is still operating in its isolation state. In a radar transceiver, therefore, the receiver is essentially "blind" during this interval, even though the transmitter is no longer producing its high-power RF burst. The sensitivity of the receiver temporarily degrades during this interval because the mismatch loss of the diode's low impedance would attenuate reflected signals that might arrive from a target during this interval. After completion of the RF burst, no externally applied electric field exists to force these charge carriers to be conducted from the *i*-layer. Therefore, the only mechanism to eliminate them and thereby allow the diode to revert to its high-impedance, low-insertion-loss state is recombination of the charge carriers. The time that this process requires is proportional to the minority carrier lifetime of the diode. In the Silvaco ATLAS simulations an average value of 6 ns is

assumed for both electron and hole carrier lifetimes [4.20]. The time required for the diode to regain its high impedance state is termed as reverse recovery time τ_{rr} which is measured as the time required for the output power to decrease from 10 % to 90 % of its maximum off power, as shown in Fig. 4.19.

It is important to select a limiter diode such that the energy that propagates past the limiter during the output spike is sufficiently small that no damage to the following stages occurs. For a practical limiter, the RF currents in the limiter diode operating in its saturated mode can approach or exceed the value that damages the diode.

Spike leakage, flat leakage and reverse recovery time for all RF RP test configurations are calculated from transient mixed-mode Silvaco ATLAS simulations. A rectangular pulse with a rise and fall time of 5 ps, a pulse width of 1 ns and a period of 50 ns was used for the simulations. The RF-out time dependent current and voltage signals were observed and the leakage powers were calculated, as shown in Fig. 4.20. The spike leakage for the 1x1-200 μm-PIND test configuration is much larger than its corresponding flat leakage (Fig. 4.20(a)). This can be attributed to the R_{ON} value of the 200 μm diameter diode at the starting of the RF burst signal not being sufficiently low enough to cause mismatch and reflection of the RF burst signal. Therefore, a large instantaneous power gets transmitted to the RF-out during the starting of the RF burst signal. The flat leakage saturates to a ~25 dBm level beyond the ~30 dBm input power level. In comparison, the same single stage RP circuit with a larger diode with 2100 μm cathode diameter exhibits low enough diode R_{ON} at the starting of the RF burst signal and a limited spike leakage

current level is transmitted to the RF-out. C_{off} is also reduced more than 110 times, thereby further reducing the shunt diode reactance. The spike and flat leakage power levels of the 1x1-2110-PIND test configuration saturate to a $\sim$25 dBm value beyond $\sim$30 dBm and $\sim$45 dBm input power levels, respectively. The 1x2-SpPD and 2x4-SpPD RP test configurations both exhibit excellent spike leakage tolerance due to low R_{ON} values of the SpPDs. The spike and flat leakages for both the test configurations is limited to $\sim$25 dBm beyond $\sim$30 dBm of the incident RF burst power level.

The SpPDs are unipolar majority carrier current dominated diodes and are therefore faster in exhibiting low R_{ON} values in comparison to the bipolar minority carrier current dominated PINDs. This can also be seen from the reverse recovery time τ_{rr} values extracted from the Silvaco ATLAS simulations for all the RP test configurations, shown in Fig. 4.21. Both the 1x2-SpPD and 2x4-SpPD test configurations exhibit a fast reverse recovery with an average τ_{rr} of $\sim$2 ns for RF burst power levels as high as 60 dBm or 1 kW. The PIND test configurations, on the other hand exhibit increasing τ_{rr} values with increasing input RF burst power levels. The 1x1-200 μm-PIND test configuration with a smaller PIND of 200 μm diameter exhibits a maximum of 8 nsec τ_{rr} at a 55 dBm power level while the 1x1-2100 μm-PIND configuration with a larger 2100 μm diode exhibits a maximum of $\sim$20 ns τ_{rr} at a power level of 57 dBm. Therefore, the RP circuit is "blind" towards the incoming low-power RF-in signals for τ_{rr} duration after the RF burst in the 1x1-2100 μm-PIND test configurations.

A deterioration of the reverse recovery performance in terms of increased τ_{rr} can be expected with large RF-burst power levels due to self-heating effects described in chapter 3 section 3.4. The trap-free SRH recombination rate given by

$$R_{SRH} = \frac{n.p - n_i^2}{\tau_p n + \tau_n p} \tag{4. 11}$$

is inversely proportional to the electron and hole carrier lifetimes τ_n and τ_p, respectively. Both τ_n and τ_p are dependent on the lattice temperature T_L as

$$\tau_{n,p} = \tau_{n0,p0}\left(\frac{T_L}{300}\right) \tag{4. 12}$$

Therefore, an increased T_L due to self-heating effects can cause a reduction in the recombination rate and thereby increasing the reverse recovery time.

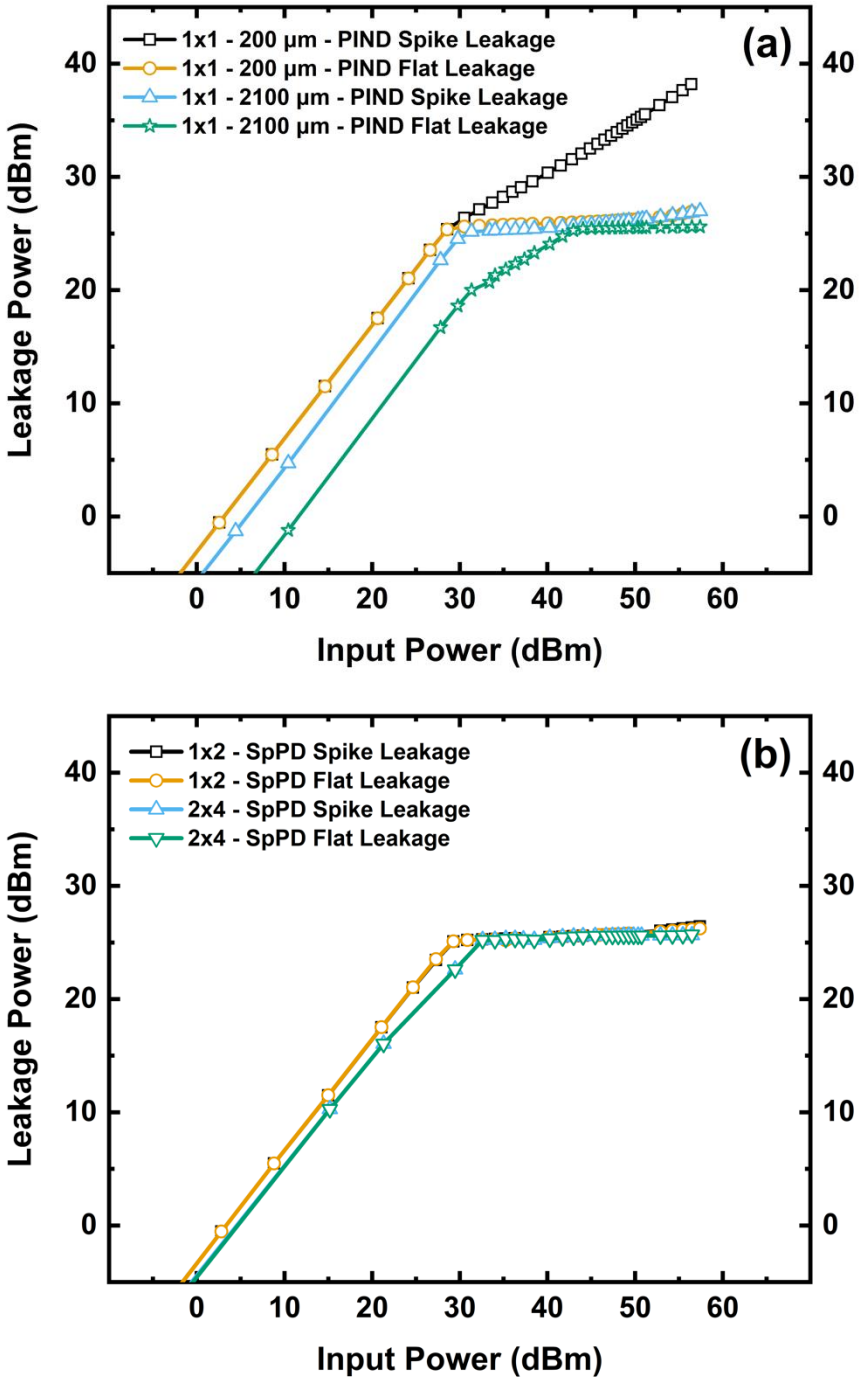


Fig. 4.20 Spike and flat leakage powers for (a) 1x1-200 µm-PIND, 1x1-2100 µm-PIND and (b) 1x2-SpPD, 2x4-SpPD.

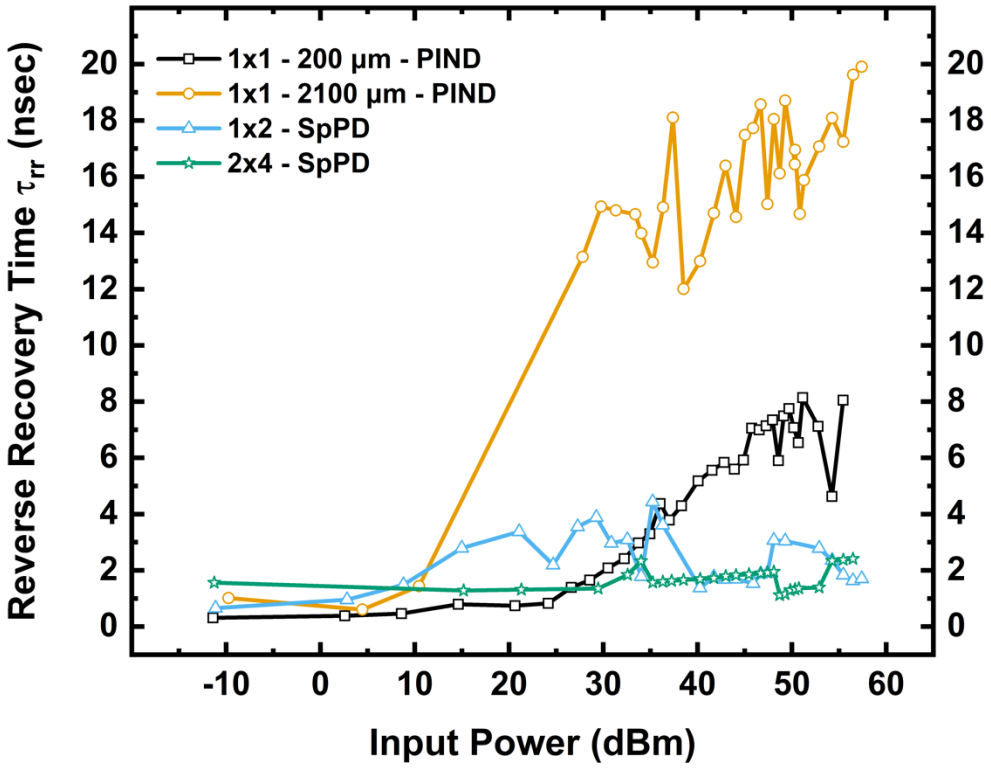


Fig. 4.21 Reverse recovery time τ_{rr} of 1x1-200 µm-PIND, 1x1-2100 µm-PIND, 1x2-SpPD and 2x4-SpPD test configurations simulated at 1 GHz

4.3.3 RF Power Limiting

Transient mixed-mode Silvaco ATLAS simulations were performed on all the four RP test configurations. Low to high power RF signals were implemented by simulating a sinusoidal wave with varying amplitudes at 1 GHz at the RF-in port. Fig. 4.22 through Fig. 4.25 show the voltage and current signals at the RF-in, across the D1 PIND and across the load R_{Load} for both the PIND test configurations – 1x1-200 µm-PIND and 1x1-2100 µm-PIND at different input power P_{IN} levels. In both cases, the load current is clipped in the positive cycle and attenuated in the negative cycle of V_{IN} (or I_{IN}). During the positive cycle of V_{IN}, the shunt PIND gets increasingly forward biased with increasing P_{IN} levels, thereby

driving the PIND further into a highly conductive or low-impedance state. The impedance offered by the shunt diode is smaller for a larger area PIND, as shown in Fig. 4.18. Therefore, the impedance mismatch at the RF-in also increases with decreasing PIND impedance. Therefore, the clipping of I_{Load} in positive V_{IN} cycle of the 1x1-2100 μm-PIND is larger (i.e., smaller I_{Load}) than the 1x1-200 μm-PIND test configuration. Moreover, the 2100 μm diameter PIND needs longer time τ_{rr} to switch from highly conducting or low-impedance state in the positive V_{IN} cycle to a highly resistive or high-impedance state in the negative V_{IN} cycle. Therefore, the 2100 μm diameter diode offers a lower shunt impedance over almost the entirety of the negative V_{IN} cycle, as shown in Fig. 4.25. In comparison, the 200 μm PIND carries a smaller charge in its *i*-layer from the positive V_{IN} cycle and can therefore switch to a highly resistive or high-impedance state within half of the negative V_{IN} cycle, as shown in Fig. 4.24. The overall effect of having a larger area shunt PIND in the single stage RP circuit is increased overall attenuation level of the RF-in signal. This can be seen from the P_{IN} - P_{OUT} relationship through both the test configurations as shown in Fig. 4.26. The power delivered to R_{Load} starts decreasing beyond a P_{IN} level of ~10 dBm in the case of 1x1-200 μm-PIND (Fig. 4.26(a)). A P_{Load} of 45 dBm (31 W) is delivered to R_{Load} for an input P_{IN} of 55 dBm (316 W). An approximate ~49 dBm (~80 W) is dissipated in the D1 diode through its on-state impedance while the remainder power ~53 dBm (200 W) is reflected back to the RF-in port. In comparison, the 1x1-2100 μm-PIND RP test configuration only allows a total P_{Load} of ~25 dBm (0.31 W) for a P_{IN} of 55 dBm (316 W) while dissipating ~40 dBm (10 W) in the D1

PIND and reflecting 54 dBm (251 W) (Fig. 4.26(b)). However, the 1x1-2100 µm-PIND also attenuates the low-power input signal as well, reducing the RP circuit's low-power sensitivity. Therefore, the diode design should be done taking the power rejection requirement and signal sensitivity into consideration.

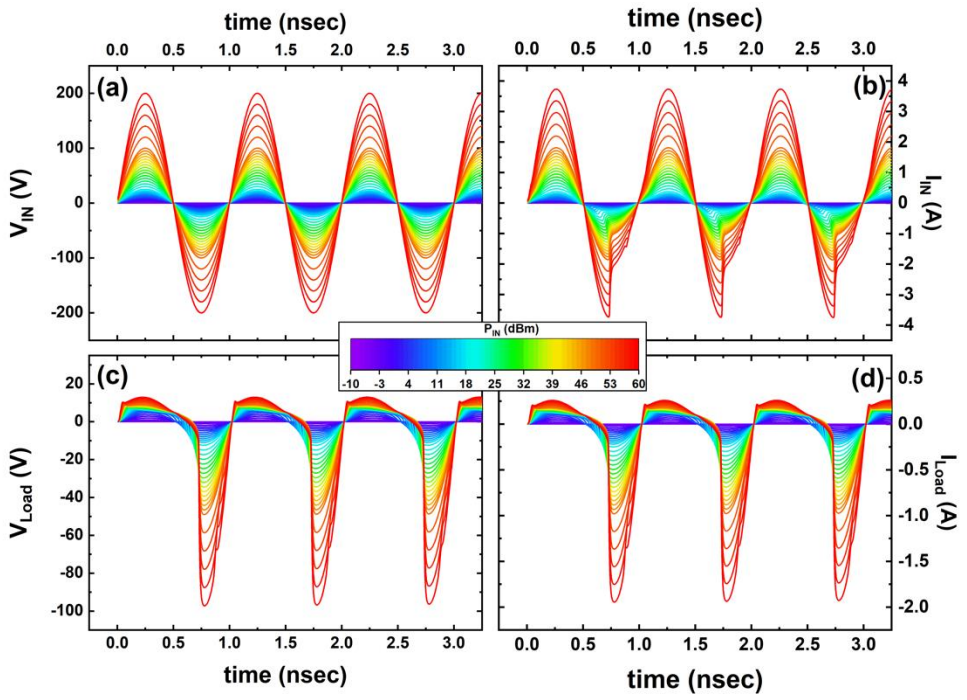


Fig. 4.22 (a) V_{IN}, (b) I_{IN} signal at RF-in and (c) V_{Load}, (d) I_{Load} signals at RF-out from the 1x1-200 µm-PIND RP test configuration

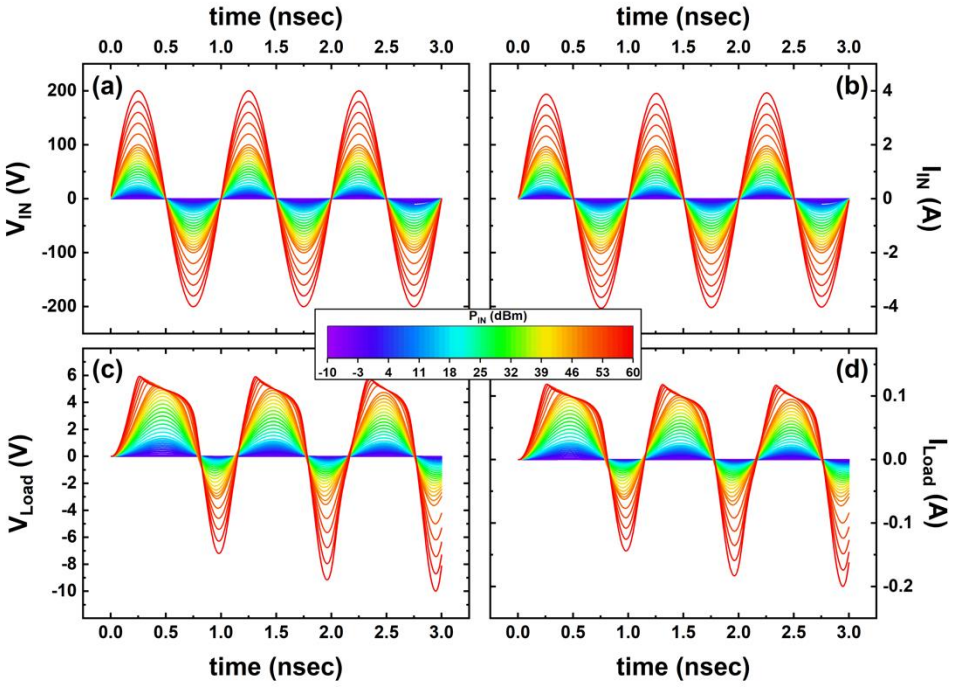


Fig. 4.23 (a) V_{IN}, (b) I_{IN} signal at RF-in and (c) V_{Load}, (d) I_{Load} signals at RF-out from the 1x1-2100 µm-PIND RP test configuration

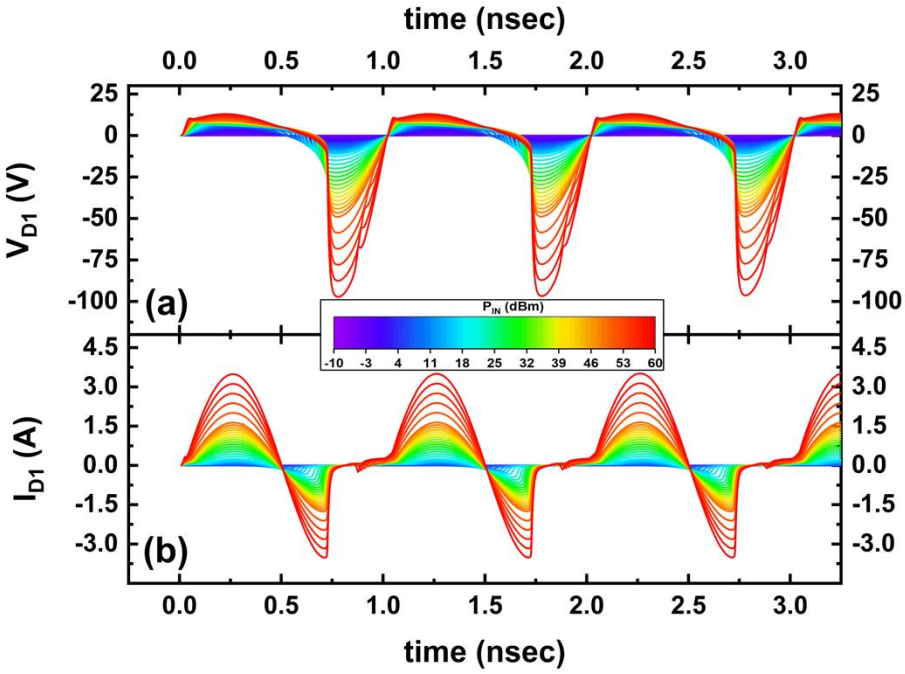


Fig. 4.24 (a) V_{D1} and (b) I_{D1} signals of the D1 PIND in the 1x1-200 µm-PIND for varying P_{IN} levels

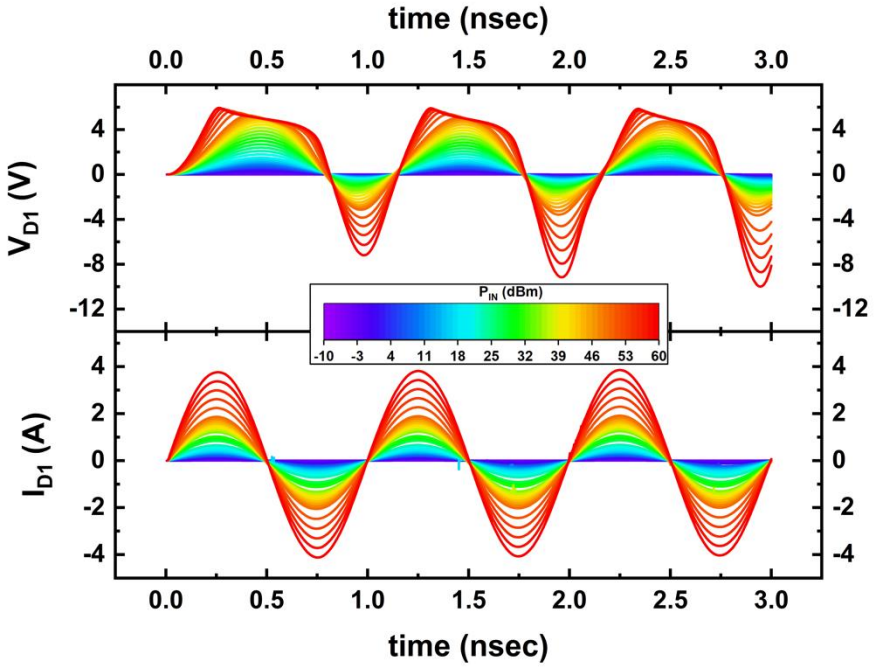


Fig. 4.25 (a) V_{D1} and (b) I_{D1} signals of the D1 PIND in the 1x1-2100 μm-PIND for varying P_{IN} levels

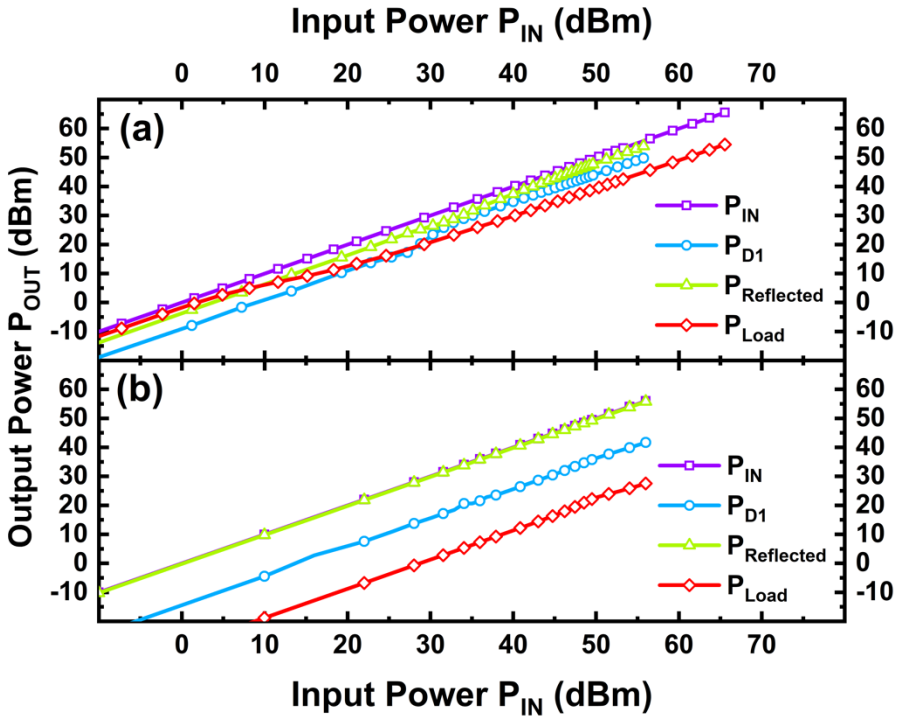


Fig. 4.26 Input P_{IN} and output P_{OUT} power relationship through (a) 1x1-200 µm-PIND and (b) 1x1-2100 µm-PIND test configurations.

The RP power limiter performances from the two SpPD based test configurations – 1x2-SpPD and 2x4-SpPD are also evaluated. Fig. 4.27 through Fig. 4.31 show the voltage and current signals at RF-in, across the anti-parallel SpPDs in shunt and across the R_{Load} for both the test configurations. A clear distinction can be readily seen comparing the PIND based RP test configurations with one diode in shunt and the SpPD RP test configurations with anti-parallel diodes – the V_{Load} and I_{Load} signals are clipped in both the positive and negative V_{IN} cycles in the case of the SpPD based RP test configurations. In the case of the 1x2-SpPD, the anti-parallel SpPDs turn-on in the positive and negative V_{IN} cycles one after the other and provide a shunted low-impedance and thereby a continuous impedance

mismatch after a certain P_{IN} level enough to turn the SpPDs on. This is evident from the alternating I_{D1} and I_{D2} signals shown in Fig. 4.29. The unipolar majority current dominated SpPDs have faster switching speeds than the PINDs and can quickly switch from highly conductive or low-impedance on-state to highly resistive or high-impedance off-state. However, as seen in Fig. 4.29 at the end of each time period of 1 ns, for a brief period (~0.15 ns) some overlap between the two anti-parallel SpPDs exists where both the diodes are in relatively low-impedance state. This may cause high power dissipation in the diodes in a short time and care needs to be taken to avoid overheating of diodes. As shown in the P_{IN} - P_{OUT} relationship from Fig. 4.32(a), the power P_{Load} delivered to R_{Load} is limited to 24 dBm (0.25 W) beyond a P_{IN} level of 33 dBm (~2 W). Therefore, even at a P_{IN} level of 55 dBm (316 W) the P_{Load} is limited to 24 dBm while a total of 41 dBm being dissipated in the SpPDs combined and nearly all the incident power is reflected i.e., $P_{\text{Reflected}}$ = 54.7 dBm (295 W). Therefore, the 1x2-SpPD provides an excellent RF power rejection at 1 GHz beyond 33 dBm.

In comparison, the 2x4-SpPD provides almost equivalent power rejection to the 1x2-SpPD test configuration. However, the main difference is the total power dissipated in the diodes is now distributed in all the four SpPDs instead of two SpPDs. This can be seen from Fig. 4.32 by comparing the average diode power dissipation in 1x2-SpPD – P_{D1}, P_{D2} ≈ 37 dBm (5 W) to average power dissipation in 2x4-SpPD - P_{D1}, P_{D2}, P_{D3} and P_{D4} ≈ 34 dBm (2.5 W). This is further evidenced by the alternating I_{D1}, I_{D2} and I_{D3}, I_{D4} current

signals across D1, D2 and D3, D4, from Fig. 4.30 and Fig. 4.31, respectively. Therefore, the 2x4-SpPD is a more efficient RP circuit for lower diode power dissipation.

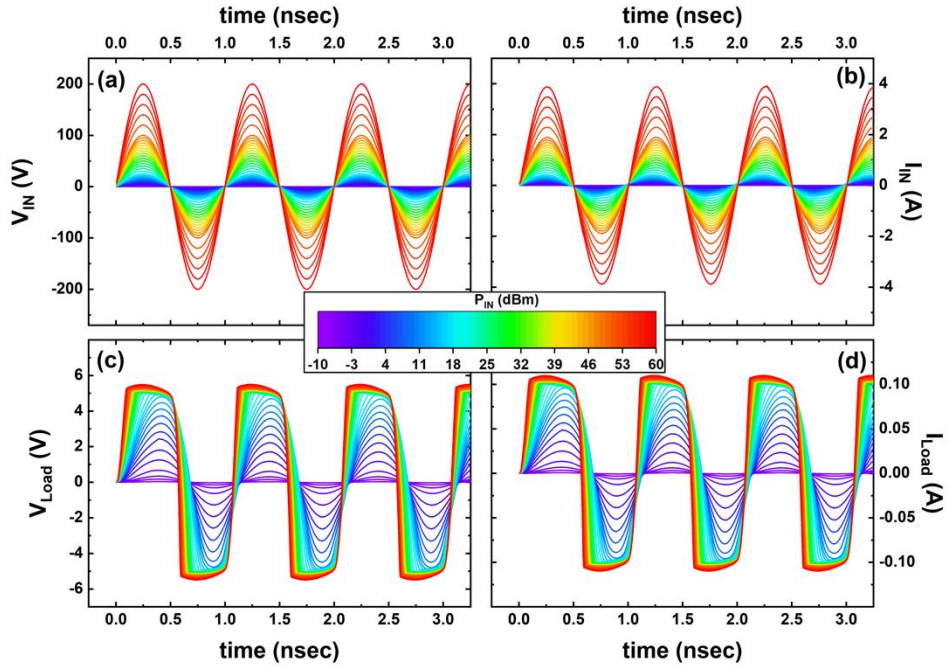


Fig. 4.27 (a) V_{IN}, (b) I_{IN} signal at RF-in and (c) V_{Load}, (d) I_{Load} signals at RF-out from the 1x2-SpPD RP test configuration

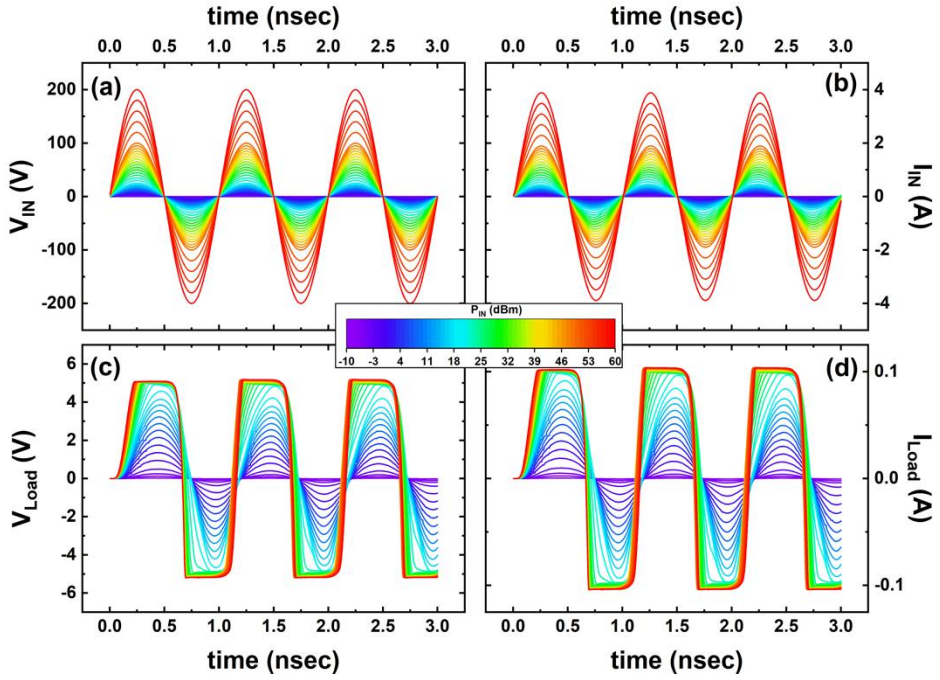


Fig. 4.28 (a) V_{IN}, (b) I_{IN} signal at RF-in and (c) V_{Load}, (d) I_{Load} signals at RF-out from the 2x4-SpPD RP test configuration

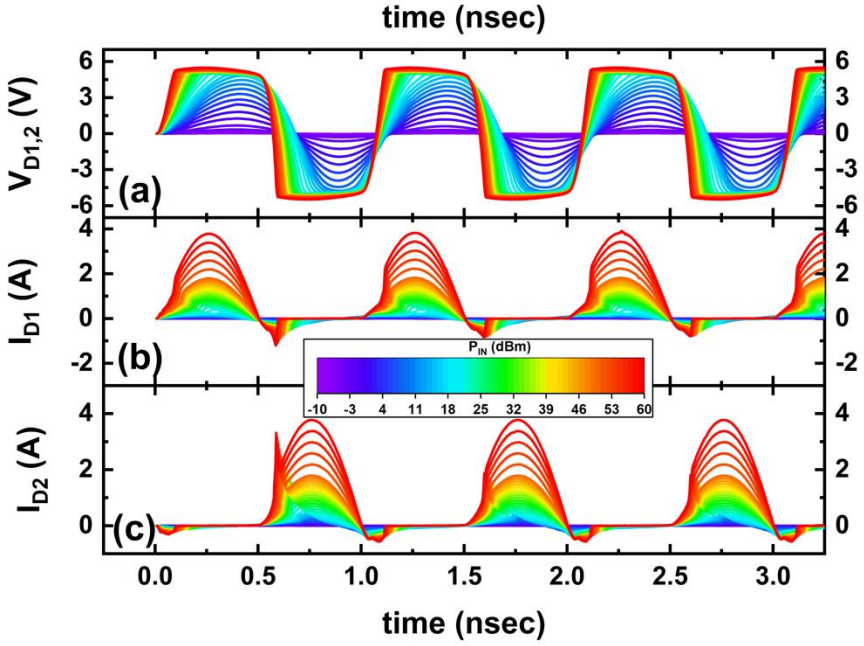


Fig. 4.29 (a) $V_{D1,2}$, (b) I_{D1} and (b) I_{D2} signals through the D1 and D2 SpPDs in the 1x2-SpPD test configuration at varying P_{IN} levels

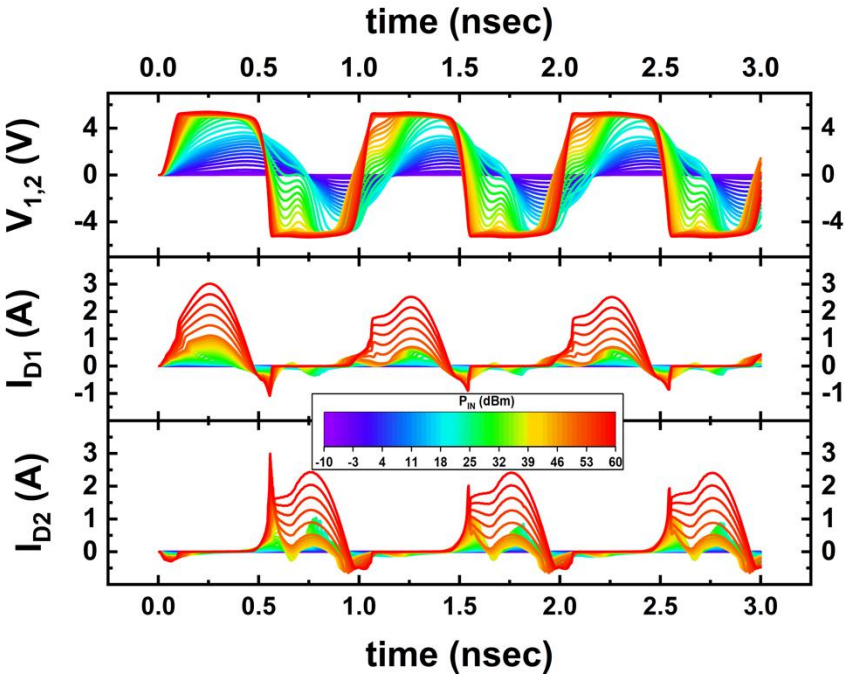


Fig. 4.30 (a) $V_{D1,2}$, (b) I_{D1} and (c) I_{D2} signals through the D1 and D2 SpPDs in the 2x4-SpPD test configuration at varying P_{IN} levels

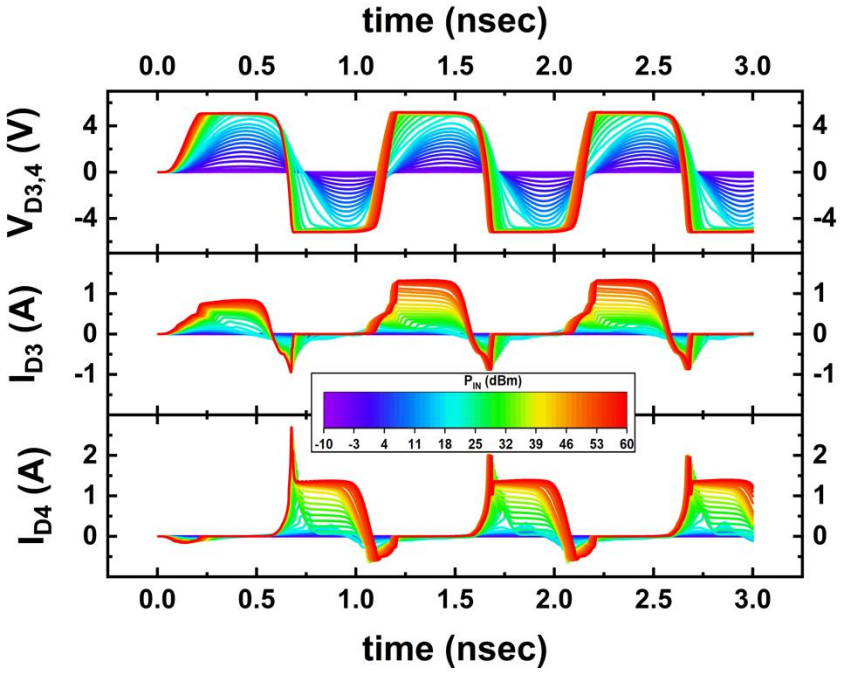


Fig. 4.31 (a) $V_{D3,4}$, (b) I_{D3} and (c) I_{D4} signals through the D3 and D4 SpPDs in the 2x4-SpPD test configuration at varying P_{IN} levels

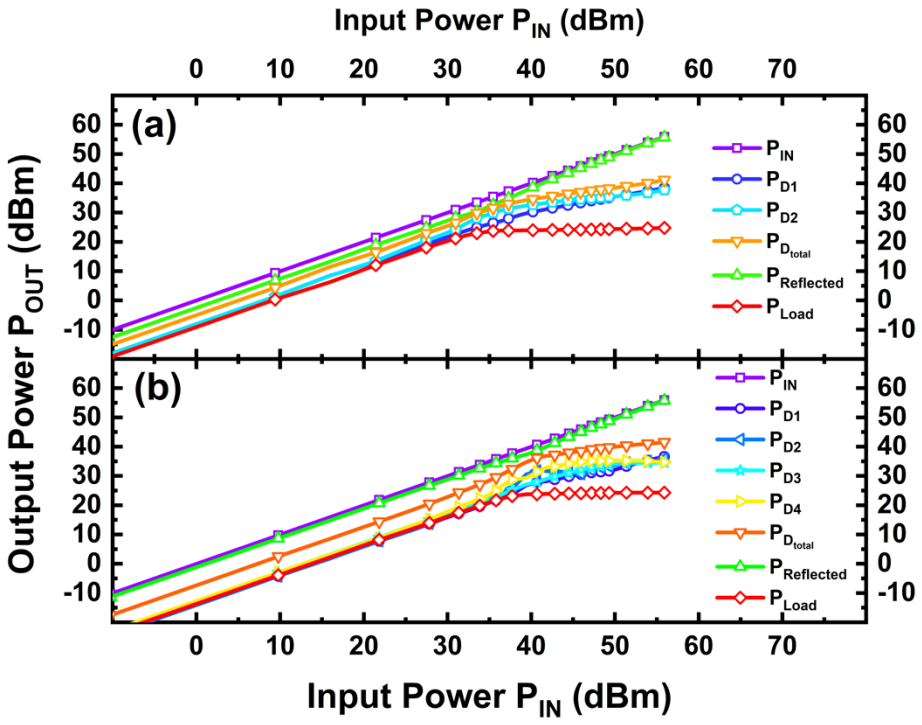


Fig. 4.32 Input P_{IN} and output P_{OUT} power relationship through (a) 1x2-SpPD and (b) 2x4-SpPD test configurations

It should be noted that the I_{Load} and V_{Load} signals at the R_{Load} of all the four test configurations are distorted sinusoidal or rectangular signals and therefore the RMS power cannot be simply calculated by

$$P_{RMS} = V_{RMS} \times I_{RMS} = \frac{V_{pp}}{2\sqrt{2}} \times \frac{I_{pp}}{2\sqrt{2}} \tag{4. 13}$$

where V_{pp} and I_{pp} are peak-to-peak voltage and current, respectively. Since the V_{Load} and I_{Load} signals are distorted, their powers are distributed over a frequency spread. A Fourier

transform is therefore calculated. The spectral power distribution for varying P_{IN} levels for the 2x4-SpPD RP test configuration is shown in Fig. 4.33.

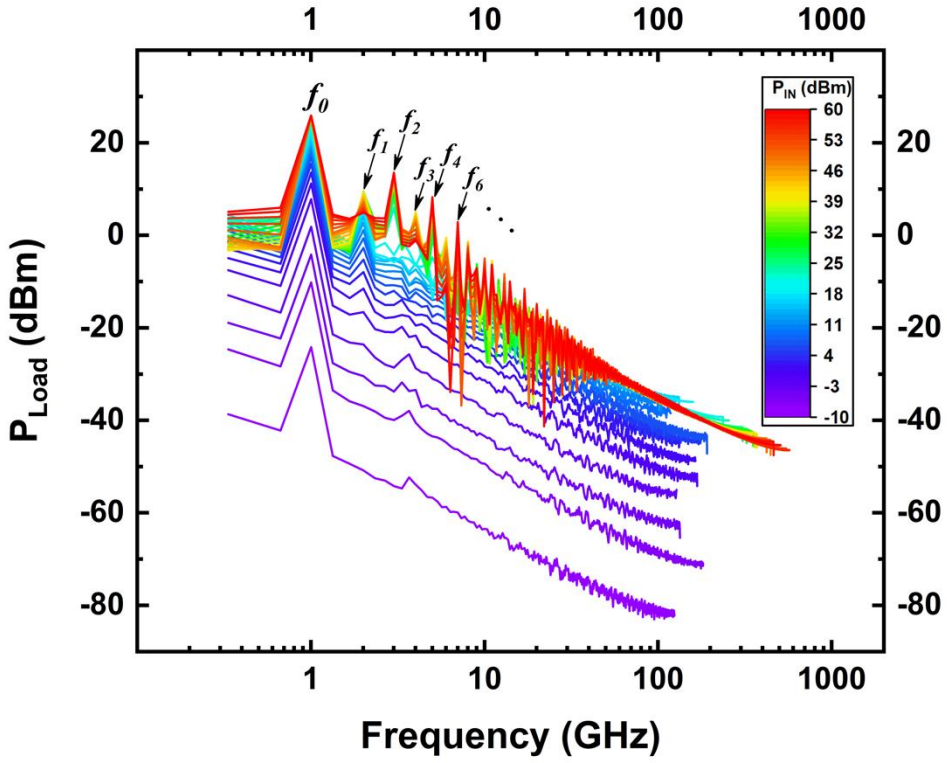


Fig. 4.33 Spectral power spread of P_{Load} in the 2x4-SpPD RP test configuration

As can be observed from Fig. 4.33, the majority of the power is contained at 1 GHz (f_0) while the remaining power is distributed throughout the spectrum with the odd frequency harmonics (f_2=3 GHz, f_4=5 GHz, …) containing diminishing local peaks of RF power. According to Parseval's theorem [4.28], the power of a signal in time domain is equal to its power in frequency domain i.e.,

$$\frac{1}{R_{Load}} \int_{-\infty}^{\infty} V_{Load}(t)^2 dt = \frac{1}{R_{Load}} \sum_{n=-\infty}^{\infty} V_{Load}(f_n)^2 \qquad (4.\ 14)$$

where $V_{Load}(t)$ is the time dependent V_{Load} signal as shown in Fig. 4.28(c) and $V_{Load}(f_n)$ are the discrete Fourier components of the V_{Load}'s Fourier transform. The total power can therefore be calculated by the summation of squares all the re-normalized frequency components of V_{Load} (or I_{Load}) divided (or multiplied) by R_{Load} i.e.,

$$P_{total} = \frac{1}{R_{Load}} \sum_{n=-\infty}^{\infty} V_{Load}(f_n)^2 \qquad (4.\ 15)$$

All the P_{OUT} powers shown in Fig. 4.26 and Fig. 4.32 are calculated using equation (4. 15).

4.3.4 Experimental Single-stage Diamond SPIND Power Limiter

The experimental diode fabricated and RF characterized in section 4.2.1 was measured in a single-stage shunt configuration for large-signal RF inputs at 1 GHz using a N9010A Keysight Signal Analyzer. Fig. 4.34 shows the experimental P_{IN} - P_{OUT} relationship obtained by varying the RF input power P_{IN} from 0 dBm to 30 dBm. For a maximum P_{IN} of ~30 dBm (1 W) a P_{Load} of ~29 dBm (0.8 W) was obtained. Although the power rejection ratio of the experimental diamond SPIND is not significant, these results are promising for further research.

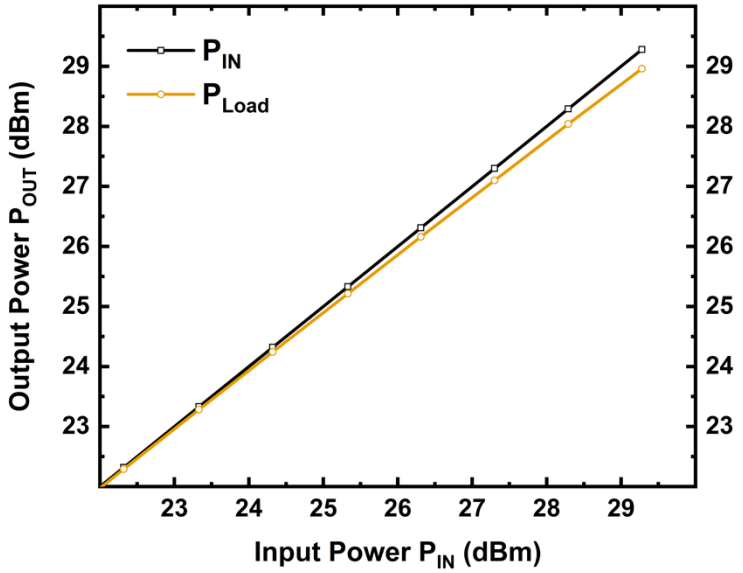


Fig. 4.34 Experimental large-signal analysis of a diamond SPIND in a single stage shunt RP configurations

4.4 Diamond RF Power Handling and Self-Heating

As discussed in section 4.3.3, depending on the RP test circuit, the power dissipated in the diamond shunt diodes varies between a maximum of ~80 W in the 200 µm PINDs to a minimum of 2.5 W in the SpPDs. As established in Chapter 3 Section 3.4.3, the static power dissipation in diamond diodes can produce self-heating effects resulting in a local temperature rise of approximately ~215 K for the worst case of $\kappa = 10\ W/cm - K$. However, a finite period of time is required for the heat generated locally to flow out of the diode during which the temperature of the diode increases as the heat propagates from the diode junction to the thermal interface to the heatsink. To estimate the diode junction temperature over time a thermal time constant can be calculated as follows [4.1],

$$\tau_{thermal} = \theta_J \times C_{thermal} \quad (4.16)$$

where θ_J is the diode junction to heatsink thermal resistance and $C_{thermal}$ is the thermal capacitance. Assuming an interface thermal conductance of 20 kW/cm^2-K [3.54], the θ_J can be calculated for the 200 μm diameter PIND as 0.16 K/W. The thermal capacitance can be calculated as [4.1]

$$C_{thermal} = S \times \frac{\rho}{V} \quad (4.17)$$

where S is the specific heat of diamond (0.68 J/gK [4.30]), ρ is the density of diamond (3.53 g/cm^3) and V is the volume. Considering the 0.1 μm thick *n*-layer, 2 μm thick *i*-layer and 90 μm p^{++}- substrate, the total volume of the 200 μm diameter PIND can be calculated as approx. equal to $2.86 \times 10^{-6}/\text{cm}^3$. Therefore, the total thermal capacitance $C_{thermal}$ is $\sim$839 kJ/K. Owing to this large $C_{thermal}$ of diamond, the thermal time is approx. equal to 1.34×10^5 sec. This thermal time is extremely large for the diamond PIND to reach maximum static power temperature (of 515 K). The high-power RF-burst signals are usually short lived and therefore maximum static power temperatures will mostly likely be never reached. Fig. 4.35 shows the lattice temperature rise as a function of time during the 1x1-200 μm-PIND RP simulation for a P_{IN} of 55 dBm (316 W) while dissipating ~80 W in the 200 μm diamond PIND at 1 GHz. Here a diamond thermal conductivity $\kappa = 10\ W/cm-K$ and the cathode contact diamond-metal interface thermal conductance $\alpha = 20\ kW/cm^2-K$ is assumed with the self-heating models implemented in chapter 3

section 3.4. Even after 100 CW cycles of P_{IN} at 55 dBm, the maximum lattice temperature rise in the diamond PIND is ~ 2.5 K.

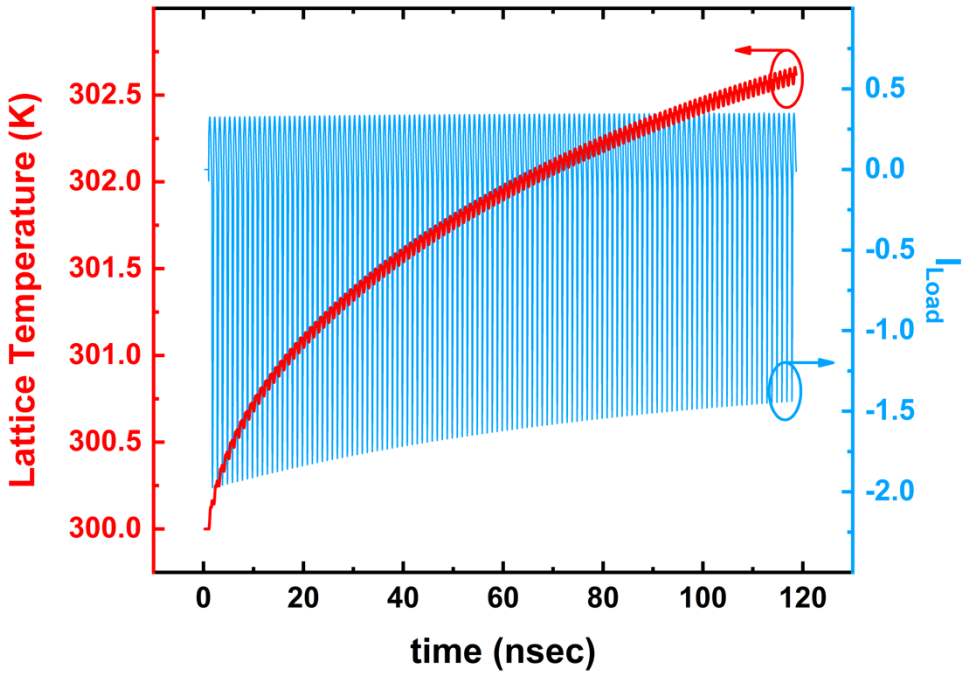


Fig. 4.35 Rise in the lattice temperature T_C of a 200 µm PIND in the 1x1-200 µm-PIND RP test configuration with a CW power P_{IN} at 55 dBm (316 W) over 100 cycles

4.5 Diamond High-Frequency MESFETs

The large signal RF power handling performance of diamond diodes is promising and can be used as a springboard to design high power diamond transistors. Accordingly, Silvaco ATLAS simulations were performed to assess the high frequency RF limits of an n-channel diamond MESFET. The simulated MESFET structure is as shown in Fig. 4.36. Incomplete ionization, hopping mobility and velocity saturation models used in Chapter 3 Sections 3.2.3.3.a, 3.2.3.3.b and 3.2.3.3.c, respectively, have been implemented in the n-channel MESFET simulations. The gate to source length L_{GS}, gate to drain length L_{GD} and

gate length L_{Gate} are all assumed to be 1 μm. The n-channel doping is set at $1.5 \times 10^{19}/\text{cm}^3$ concentration of P. Here an optimistic P activation energy E_D of 0.46 eV [4.31] is assumed. The n-channel thickness is optimized to about 50 nm with an underlying insulting intrinsic diamond substrate. A Schottky contact with a metal work-function ϕ_{MS} of 4.55 eV, equivalent to Ti work-function, is assumed. Due to the incomplete ionization of the n-type P doping in the n-channel, the free charge carrier concentration, i.e. electrons, in the n-channel is approximately only $\sim 10^{15}/\text{cm}^3$ or 0.009%. However, the depletion charge is made up of the total doping concentration since while depleting the channel, the Fermi level goes above the P donor level and all the dopant concentration is uncovered. This is evident from the simulated ionized P doping concentration N_D^- and electron concentration levels n shown in Fig. 4.37. Therefore, on one-hand a higher channel doping concentration is needed to improve total drain current density by increasing the free electron concentration but on the other hand increasing the channel doping concentration makes depleting the channel harder and thereby requiring larger V_{GS} channel turn-off voltages. This results in a normally-on n-channel MESFET. The room temperature (r.t.) DC $I_D - V_D$ characteristics of the n-channel MESFET are as shown in Fig. 4.38(a). A maximum r.t. drain current I_D of ~13.5 mA/mm is obtained at $V_{GS} = -4\,V$ and $V_{DS} = +30\,V$. The cut-off V_{GS} voltage is -52 V.

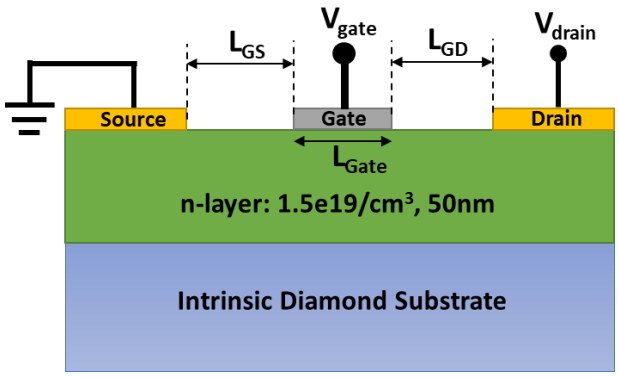


Fig. 4.36 Diamond n-channel MESFET structure for RF applications

$I_D - V_G$ characteristics were also simulated for varying V_{DS} values, as shown in Fig. 4.38(b). Consequently, the room temperature transconductance g_m as a function of V_{GS} is derived from the $I_D - V_G$ plots using the equation (4. 18) and is shown in Fig. 4.39(a). A maximum g_m of 0.95 mS/mm is obtained at a V_{GS} of -45 V.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \tag{4. 18}$$

In order to evaluate the maximum transitionary frequency at which the current gain goes to unity i.e., $f_{T_{max}}$, the gate to source capacitance C_{GS} was also simulated (Fig. 4.39(b)) and $f_{T_{max}}$ was calculated by

$$f_{T_{max}} = \frac{g_m}{2\pi C_{GS}} \tag{4. 19}$$

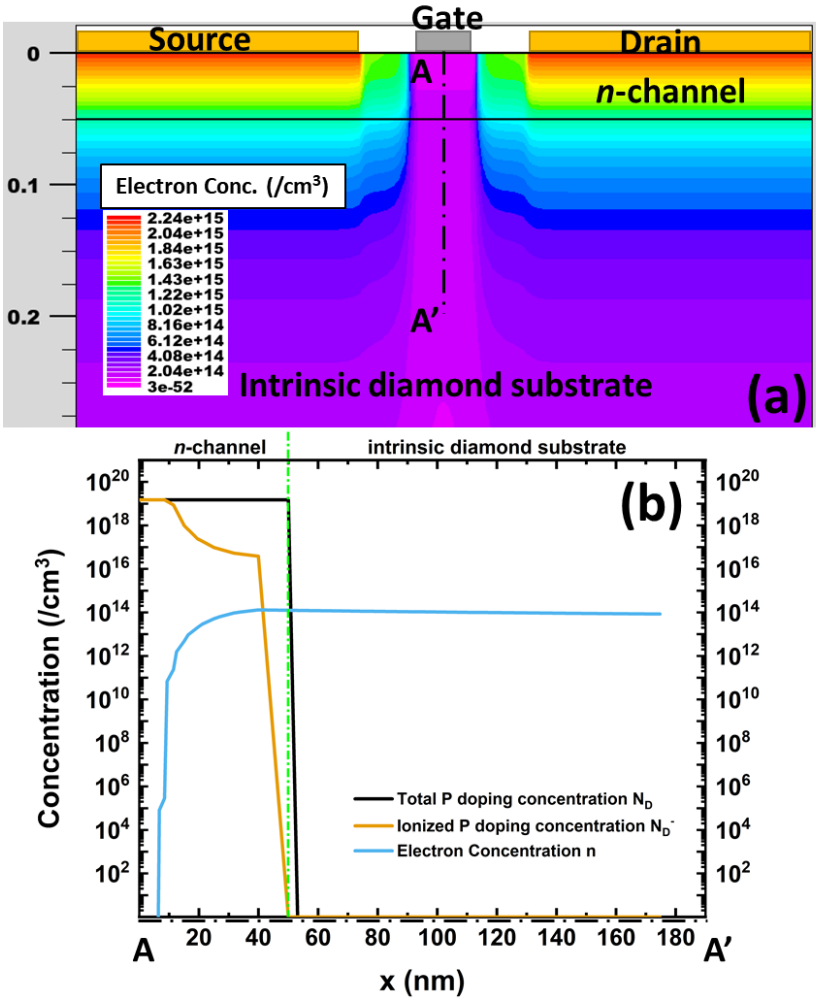


Fig. 4.37 (a) Contour plot of electron concentration across the MESFET area with a A-A' cut-line across the channel depletion region indicating the (b) total P doping concentration N_D, ionized doping concentration N_D^- and electron concentration n at $V_{GS} = V_{DS} = 0\ V$

With increasing lattice temperature, the ionization of P increases and more free electrons are available for conduction in the n-channel. This improves the transconductance and thereby increasing the $f_{T_{max}}$, as shown in Fig. 4.41. However, the temperature dependent electron hopping mobility, as established in Chapter 3 Section 3.2.3.3.b,

decreases with increasing temperature. Therefore, a trade-off exists between the increasing transconductance and decreasing drain current due to decreasing electron mobility and a peak $f_{T_{max}}$ of ~70 GHz is achieved for 400°C.

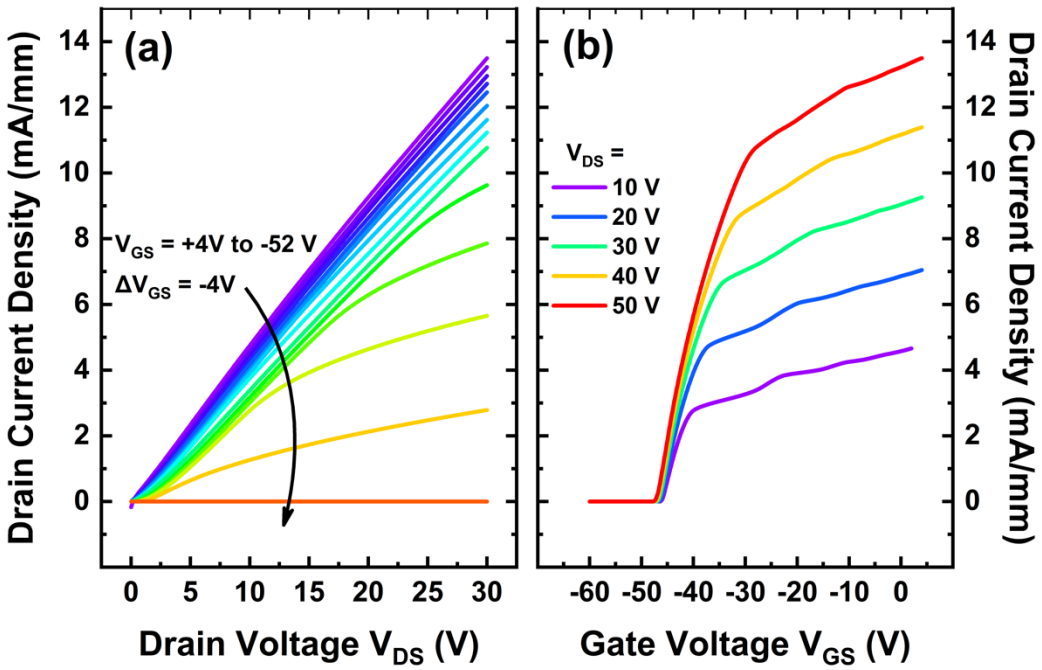


Fig. 4.38 DC (a) $I_D - V_{DS}$ and (b) $I_D - V_{GS}$ characteristics of diamond n-channel MESFET for V_{GS} values ranging from +4 V to a cut-off V_{GS} of -52 V

As shown in Fig. 4.40, a maximum $f_{T_{max}}$ figure-of-merit of ~9.5 GHz is obtained at $V_{DS} = 30\ V$.

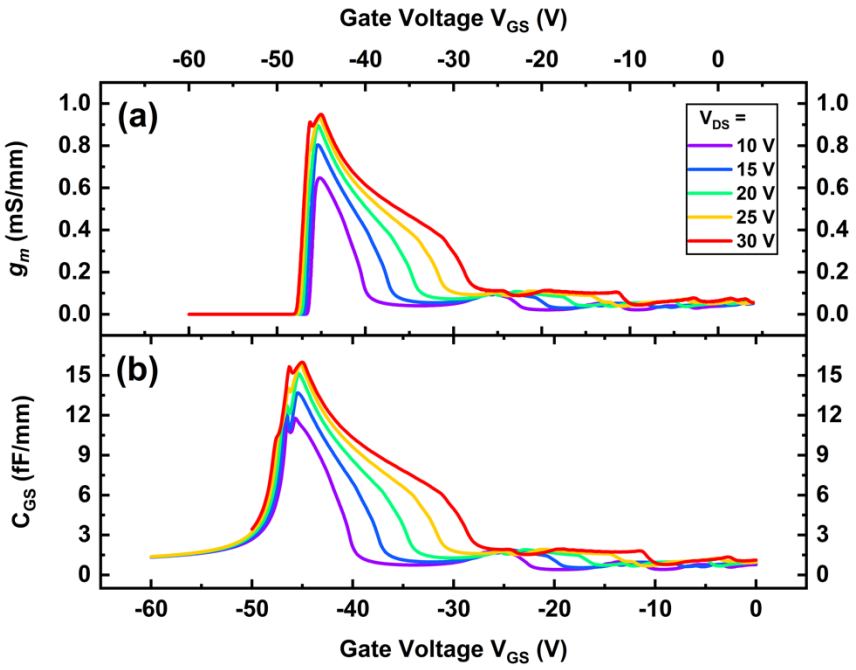


Fig. 4.39 Room temperature (a) transconductance g_m and (b) C_{GS} vs V_{GS} characteristics of diamond n-channel MESFET

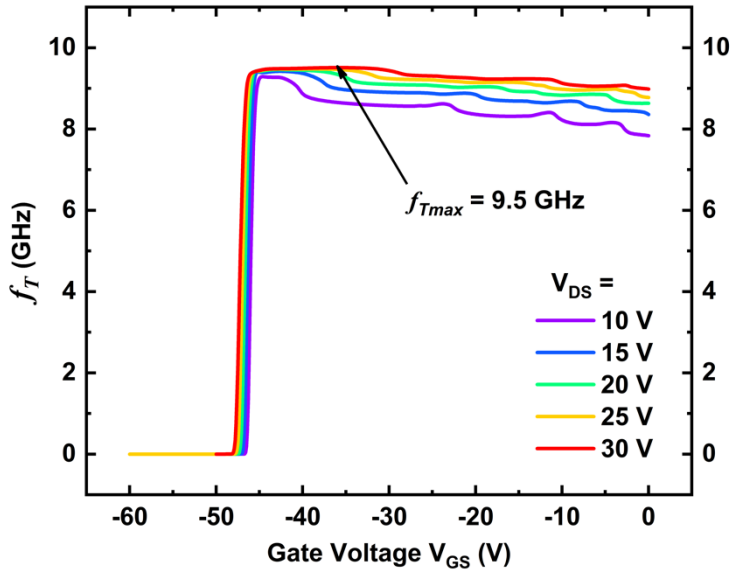


Fig. 4.40 f_T figure-of-merit vs. V_{GS} of a diamond n-channel MESFET

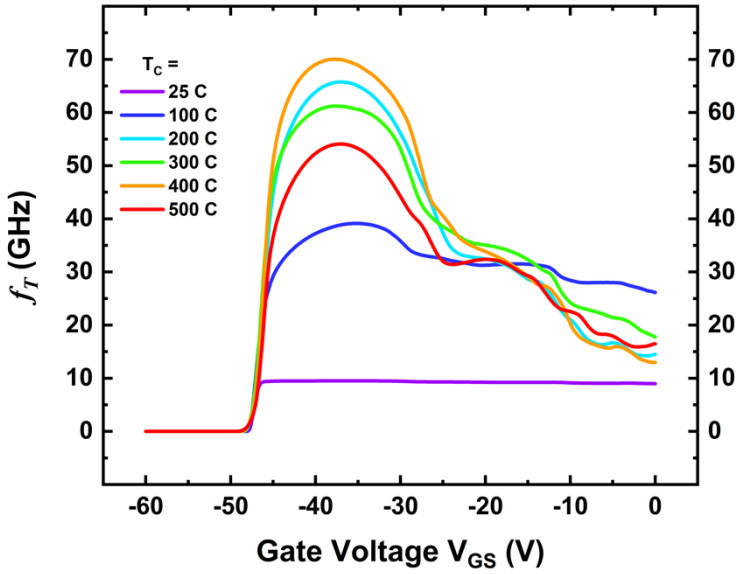


Fig. 4.41 f_T vs V_{GS} for increasing T_C of a diamond n-channel MESFET

4.6 Conclusion

Diamond p-i-n and Schottky diodes were fabricated and characterized at high frequencies from 0.1 GHz to 25 GHz as shunt impedances in co-planar striplines. Small-signal parameters for a lumped-element Spice model have been extracted and demonstrate good agreement with measured impedance parameters in the frequency range 1-25 GHz. Two-port measurements of the co-planar striplines show the diode shunt has an off-state insertion loss of 0.3 dB at 1 GHz with a power rejection ratio of 14 dB in the on-state. Using Silvaco ATLAS simulations, to maximize F_{OC}, the diode R_{ON} and C_{Off} values are optimized by varying the epitaxial thicknesses of *n*, *i* and p^- layers in both diamond *p-i-n* and Schottky diodes. A drift-diffusion based diode capacitance model is also proposed. To establish the usefulness of diamond diodes as high-power RF limiters, mixed-mode transient Silvaco ATLAS simulations were performed on single and two stage receiver-

protector circuits with diamond *p-i-n* and Schottky diodes as shunt impedances. An excellent load power limitation to a maximum of 24 dBm or 0.25 W is achieved for incident CW RF burst powers beyond 33 dBm or ~2W and up to 55 dBm or 316 W in RP circuits using diamond Schottky diodes. A maximum of 25 dBm or 0.31 W load power limitation is also achieved through diamond *p-i-n* based RP circuits, however, the low-power sensitivity is compromised. For the worst-case scenario of ~80 W being dissipated in the diamond diodes during CW operation at 1 GHz, self-heating effects were also simulated and a maximum ball-park value of lattice temperature rise of 2.5 K is shown at the end of 100 cycles. Silvaco ATLAS simulations of an n-channel diamond MESFETs were also performed and a $f_{T_{max}}$ figure-of-merit of ~9.5 GHz at room temperature and ~70 GHz at $400^{o}C$ was demonstrated. Therefore, the potential of diamond as an excellent candidate for high-frequency and high-power applications is established through experimental and theoretical evidence.

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CHAPTER 5

DIAMOND DIODES FOR HARSH ENVIRONMENTS

5.1 Introduction

Wide band-gap semiconductors such as SiC, GaN, Ga_2O_3 and Diamond have much lower intrinsic carrier concentrations than Si, and ideally the leakage currents are orders of magnitude smaller than Si, provided that junctions are realized in crystals of adequate structural quality. Therefore, wide bandgap semiconductor devices are capable of much higher temperature operation with respect to this fundamental limitation, in excess of 600^oC. Diamond has a large bandgap of $5.47\ eV$ and the intrinsic carrier concentration at room temperature is extremely small on the orders of $10^{-70}/cm^3$. Therefore, diamond is naturally a suitable candidate for high temperature electronics.

One of the main project goals was to prepare working diamond diodes and test them at NASA's Glenn Extreme Environment Rig (GEER) test run scheduled sometime in March 2022. In order to develop diamond diodes for extreme environments, we simulate and analyze effects of high temperature on incomplete ionization, hopping mobility and space charge limited conduction, develop high temperature contacts, fabricate, test and analyze diamond diodes for high temperature (500^oC) operation, stress test at continuous high temperature and high currents and collaboratively develop packaging and automatic data acquisition for the NASA GEER run. We also simulate and show a potential design for a high temperature diamond JFET and its application in a power converter. The following

sections detail the high temperature analysis and development of diamond diodes towards the NASA GEER run.

5.2 High Temperature Effects on Diamond

Silvaco ATLAS TCAD simulations and in-house analytical models are used to theoretically analyze the effect of high temperatures on the reverse and forward current – voltage characteristics of diamond diodes. The three major effects of temperature on diamond diode characteristics are through incomplete ionization, hopping mobility and space charge limited (SCL) conduction. Following sub-sections analyze these effects.

5.2.1 Temperature Dependent Incomplete Ionization

As established in Chapter 3 Section 3.2.3.3.a and as shown in Fig. 3.7, the incomplete ionization ratio η_A of a B doped p-type diamond semiconductor is dependent on the doping concentration, N_A, since the activation energy, E_A, is a function of N_A. Moreover, both η_D and η_A are a function of temperature as given by equations (3.28) and (3.29), respectively. The diamond bandgap is also a function of temperature and has been formulated by O'Donnell *et. al.* [5.1] as

$$E_g(T_C) = E_g(300) - S\langle h\omega\rangle\left[coth\left(\frac{\langle h\omega\rangle}{2k_BT_C} - 1\right)\right] \quad (5.1)$$

where $E_g(300)$ is the bandgap at 300 K equal to 5.47 eV, S is a dimensionless coupling constant equal to 2.31 for C and ⟨hω⟩ is an average phonon energy equal to 0.094 eV for C. The temperature dependent conduction and valence band density of states are as follows

$$N_{C,V} = N_{C,V}(300)\left(\frac{T_C}{300}\right)^{3/2} \quad (5.\ 2)$$

where $N_{C,V}(300)$ are the conduction and valence band density of states at 300 K equal to $1.021 \times 10^{19}/cm^3$ and $2.166 \times 10^{19}/cm^3$, respectively [5.1]. The intrinsic carrier concentration therefore also depends on the temperature as given by

$$n_i(T_C) = \sqrt{N_C(T_C)N_V(T_C)}\exp\left(-\frac{E_g(T_C)}{2k_BT_C}\right) \quad (5.\ 3)$$

The dependence of $n_i(T_C)$ and $E_g(T_C)$ on temperature is as shown in Fig. 5.1.

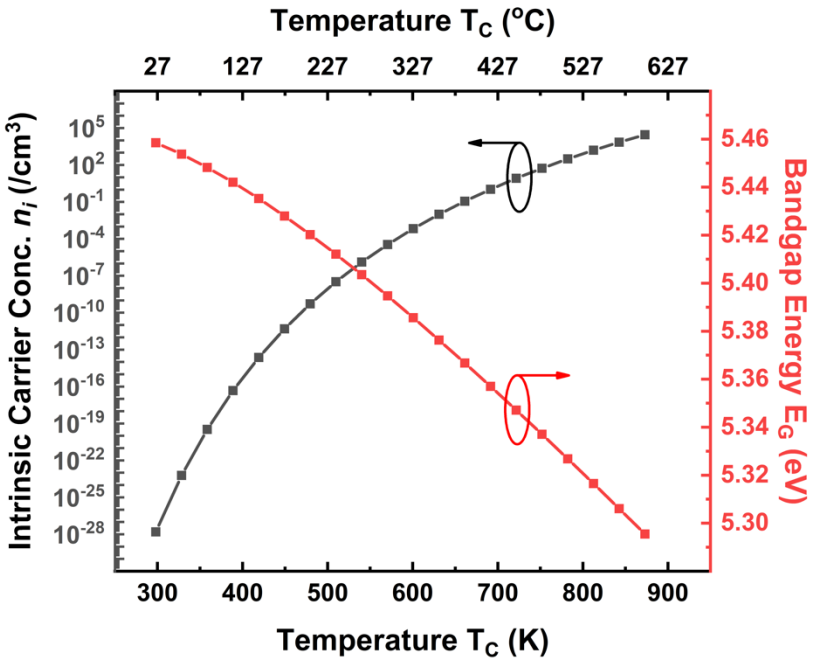

Fig. 5.1 Temperature dependence of intrinsic carrier concentration $n_i(T_C)$ and material bandgap $E_g(T_C)$ of diamond

Therefore, the η_D and η_A as a function of the total doping concentrations N_D and N_A and the lattice temperature T_C are as shown in Fig. 5.2(a) and Fig. 5.2(b). The doping dependent

B activation energy assumed here is as given in equation (3.30) while a constant P activation energy of 0.57 eV is assumed here.

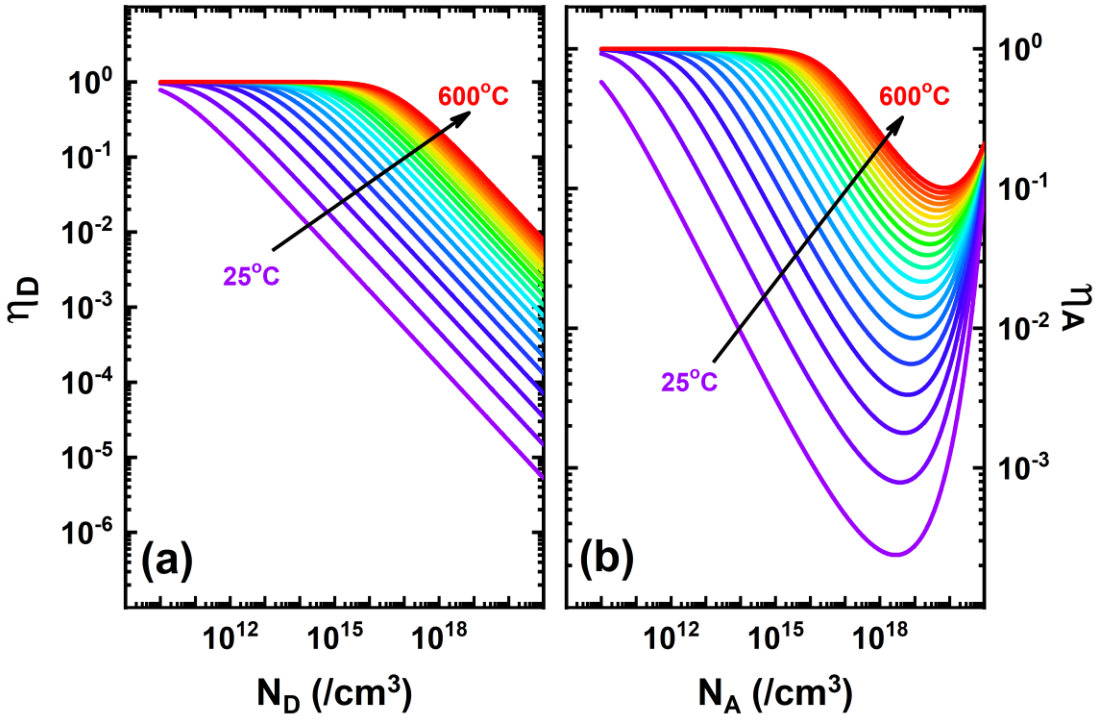

Fig. 5.2 Temperature dependence of (a) P incomplete ionization ratio η_D and (b) B incomplete ionization ratio η_A as a function of N_D and N_A respectively.

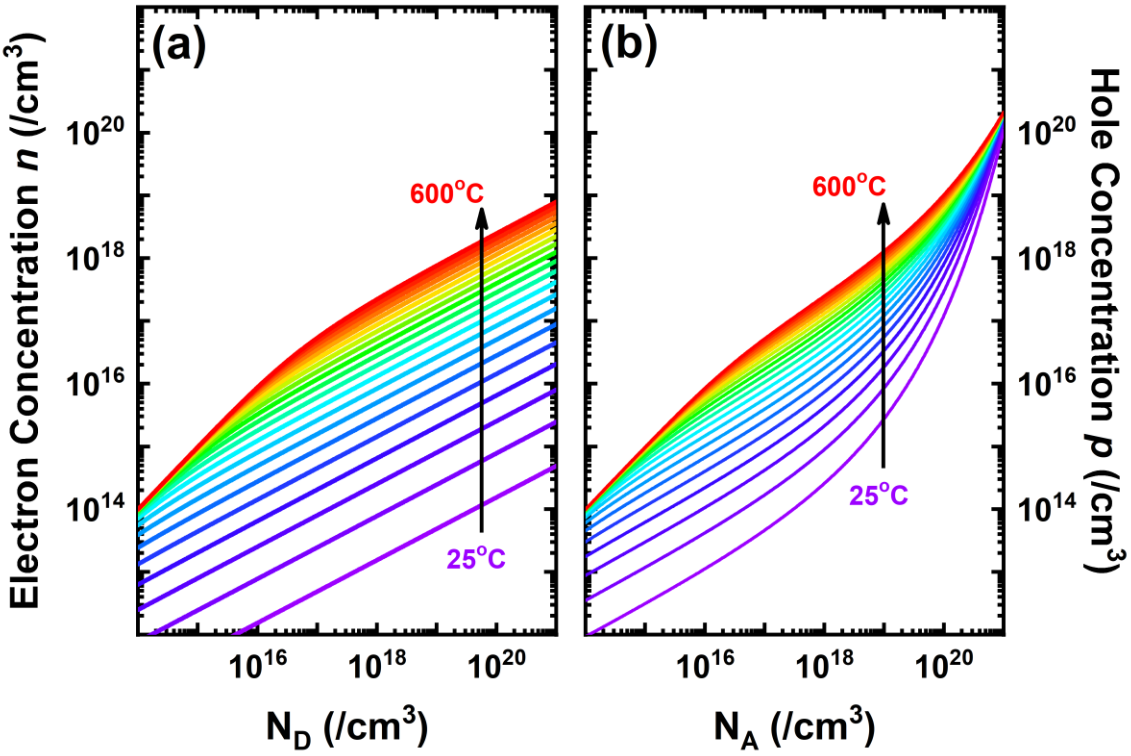

Fig. 5.3 Temperature dependence of (a) electron concentration n as a function of N_D and (b) hole concentration p as a function of N_A

5.2.2 Temperature Dependent Hopping Mobility

Effective variable-range hopping (VRH) and nearest-neighbor hopping (NNH) mobilities implemented for holes and electrons in diamond, respectively, have been formulated in Chapter 3 Section 3.2.3.3.b through equations (3.31) to (3.42). Both of the VRH and NNH mobilities have strong dependence on the temperature. Considering a maximum and minimum electron and hole mobility of $\mu_{nmax} = 1030\ cm^2/V-s$, $\mu_{nmin} = 10\ cm^2/V-s$, $\mu_{pmax} = 2100\ cm^2/V-s$ and $\mu_{pmin} = 20\ cm^2/V-s$ [5.3], the temperature dependent $\mu_n(T_C)$ and $\mu_p(T_C)$ as a function of N_D and N_A is as shown in Fig. 5.4. The range over which the hopping mobilities (VRH or NNH) are dominant is also indicated in Fig.

5.4. The NNH hopping mobility of electrons increases considerably with increasing N_D concentration beyond $10^{19}/cm^3$. $\mu_p(T_C)$ decreases monotonously with increasing temperature. On the other hand, for the $\mu_n(T_C)$, a temperature dominated decrease over hopping conduction dominated increase occurs with increasing temperature, as shown in Fig. 5.4(a).

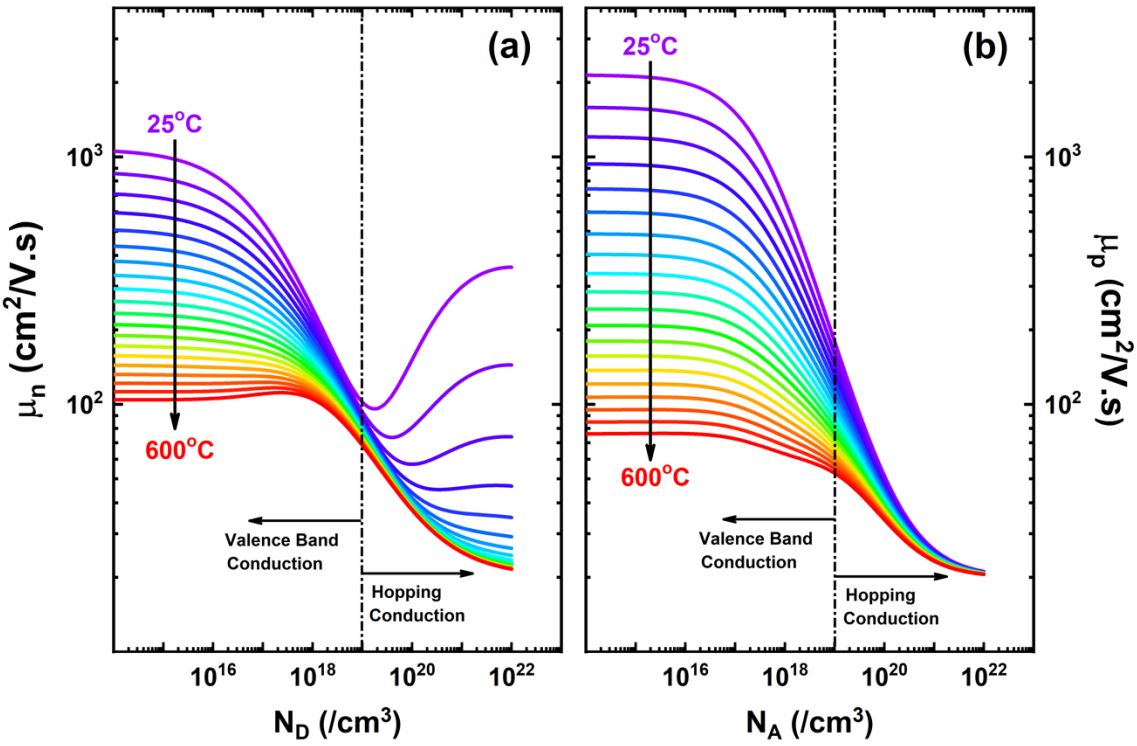

Fig. 5.4 Temperature dependence of (a) electron and (b) hole hopping mobilities as a function of N_D and N_A, respectively, in diamond.

5.2.3 Temperature Dependent Resistivity

Combining the temperature dependent incomplete ionization ratios and mobilities shown in the previous sections, a temperature dependent resistivity for both P doped n-type diamond and B doped p-type diamond can be calculated by

$$R_n = \frac{1}{q\left(n_D \mu_{nT}(T_C) + n_{Hopp} \mu_{nHopp}(T_C)\right)} \tag{5. 4}$$

$$R_p = \frac{1}{q\left(p_A \mu_{pT}(T_C) + p_{Hopp} \mu_{pHopp}(T_C)\right)} \tag{5. 5}$$

where $\mu_{nT}(T_C)$ and $\mu_{pT}(T_C)$ are the empirical temperature dependent electron and hole mobilities, respectively, given by equation (3.38), $n_{Hopp} = N_D - n_D$, $p_{Hopp} = N_A - p_A$ and $\mu_{nHopp}(T_C)$ and $\mu_{pHopp}(T_C)$ are electron NNH and hole VRH temperature dependent mobilities, describe by equations (3.42) and (3.32), respectively. Fig. 5.5 shows the temperature dependence of R_n and R_p as a function of N_D and N_A, respectively.

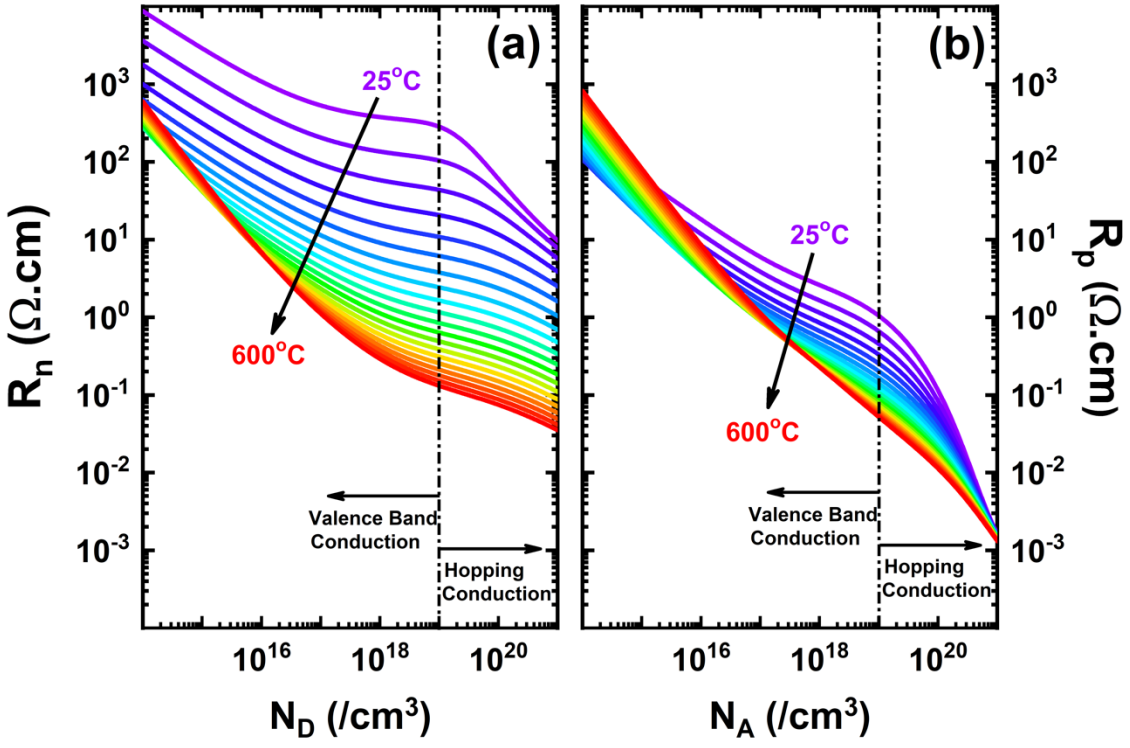

Fig. 5.5 Temperature dependence of (a) R_n and (b) R_p as a function of N_D and N_A, respectively, in diamond

The hopping dominated regions for both R_n and R_p are for N_D and N_A concentrations beyond $10^{19}/cm^3$ and are shown in Fig. 5.5. For a N_D of $10^{20}/cm^3$, R_n exhibits a broad swing over temperature with a maximum value of $\sim 59\ \Omega - \text{cm}$ at r.t. and a minimum of $\sim 0.074\ \Omega - \text{cm}$ at $T_C = 600^{\text{o}}\text{C}$. On the other hand, the R_p exhibits a smaller swing over temperature with a maximum value of $0.11\ \Omega - \text{cm}$ at r.t. and a minimum of $\sim 0.011\ \Omega - \text{cm}$ at $600^{\text{o}}C$. The difference in swing with temperature for electron and hole resistivities can be attributed to the fact that P activation energy is higher and constant with doping in comparison to B activation energy, therefore free electrons available for conduction are several orders of magnitude smaller than free holes, over the entire temperature range Fig. 5.3.

5.3 High Temperature Characterization

In order to prepare for the GEER chamber test run, diamond diodes were progressively developed for the chamber's extreme environment. Several diamond diode samples were prepared for the GEER test run, out of which one "active" sample was selected for *in-situ* measurements. Following sub-sections detail the extreme environment characterization of diamond diodes developed *a priori* to the main GEER diodes and long thermal and current stress measurements on diamond diodes for assessing their stability and reliability.

5.3.1 UARK Venus Atmosphere Emulation Run

Prior to the main GEER test, several diamond diodes were tested for extreme environment performance at the Venus emulation chamber at the University of Arkansas (UARK) Center for Space and Planetary Science in collaboration with Dr. Simon Ang's research group. The UARK Venus emulation chamber is a 500 mL capacity stainless steel pressure vessel and was pumped down to $37\ \mathrm{mbar}$ at room temperature and flushed with CO_2 at $\sim 4\ \mathrm{bar}$ to remove residual gas in the chamber. More CO_2 was introduced into the chamber until the desired starting pressure, calculated using the ideal gas law, was reached. The chamber was sealed and the heating sleeve was set. The chamber took ~45 minutes to reach the temperature setpoint of $460°C$ and shortly afterwards the pressure stabilized to $\sim 96\ bar$. Under these conditions, the CO_2 is in a supercritical state. During the 100-hour run, the temperature and pressure were monitored and remained stable at 460°C ± 0.5% and 96 *bar* ± 2%.

In total, four diamond samples, 19-104, 19-105, 19-106 and 19-108, were tested in the UARK emulation chamber. All four samples were grown on a type IIb <111> oriented, heavily B doped, 3x3x0.3 mm diamond plate using the CVD growth procedure detailed in Chapter 1, Section 2.2. All samples had an n-layer of ~300 nm and a targeted P doping of $10^{18}/cm^3$. The target i-layer thickness of the 19-105, 19-106 and 19-108 samples was ~300 nm whereas that of the 19-104 sample was ~750 nm. An additional ~135 nm nano-carbon layer was deposited on top of the n-layer of the 19-108 sample. Diamond SPINDs were fabricated on all the four samples using the procedure described Chapter 1, Section

2.3. Samples 19-104, 19-105 and 19-108 were mounted on an alumina PCB with gold pads using Ferro Material 8835 gold cement while the 19-106 sample was packaged in a molded ceramic chip carrier with kovar alloy contact pads, as shown in Fig. 5.6. An insulating adhesive was also applied on the 19-106 sample in order to secure the wire bonds in place and protect the surface of the diamond during the Venus simulation run.

The samples were subjected to 100 hours of extreme environment in the UARK Venus emulation chamber. The diode $J - V$ characteristics of all samples were compared before and after the UARK test run. Fig. 5.7 shows the $J - V$ characteristics of the 19-104 sample pre- and post- UARK test run. The diode turn-on voltage increases from $13.4\ V$ to $14.6\ V$ and a small increase in the leakage current is observed. The metal contacts on the 19-108 sample with a nano-carbon layer on top of the n-layer de-laminated during the UARK test run and therefore could not be characterized post-UARK test run.

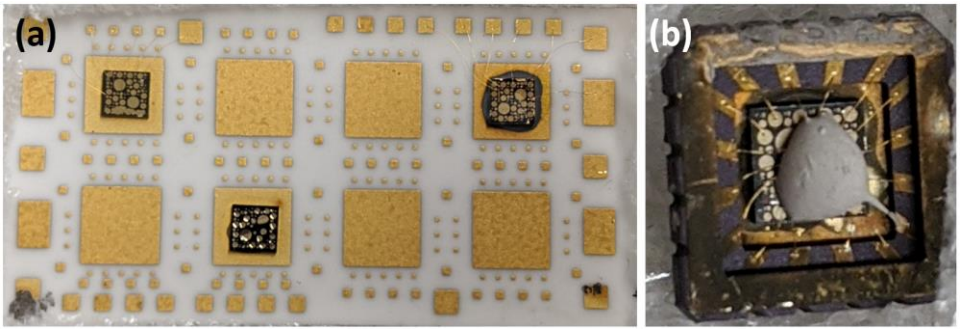

Fig. 5.6 (a) 19-104, 19-105, 19-108 samples mounted on an alumina substrate and wire-bonded to gold pads (b) 19-106 sample packaged in a molded ceramic package with Kovar alloy contact pads. An insulating adhesive is applied partially over the sample surface area

The survival of diamond diodes under ~92 bar CO_2 atmosphere and ~460°C temperature for 100 hours provided confidence on the survivability of diamond diodes in the GEER chamber.

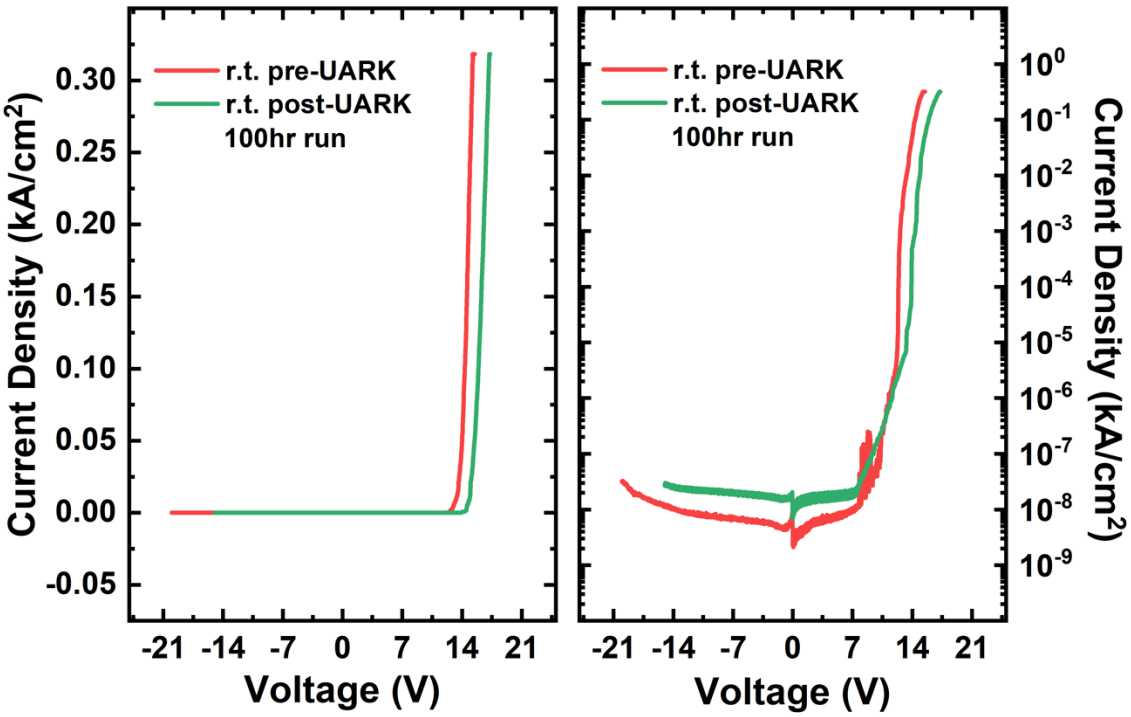

Fig. 5.7 (a) Linear and (b) logarithmic $J-V$ characteristics of 19-104 sample pre and post UARK emulation chamber test run

5.3.2 Temperature and Current Stressing of Diamond Diodes

The diamond diodes are required to be stable and reliable under thermal stress in the Venusian atmosphere, as well as handle continuous current and voltage operation. Therefore, preliminary thermal and current stress measurements were performed on fabricated diamond diodes for more than 100-hour cycles. Fig. 5.8 shows the thermal

stressing at room temperature and 460°C for 100+ hours at a constant reverse bias V_{rev} of -10 V and continuous I-V sweeps for 26 hours on diamond SPINDs. The diamond SPIND remains very stable at room temperature for 100+ hours with very little deviation in the leakage current. At 460°C, the leakage current is inherently larger due to increased temperature and is only stable for 65 hours, beyond which, the current increases by 3 orders of magnitudes. A continuous I-V sweep was also performed and the degradation of the diamond diode was assessed over time, shown in Fig. 5.8(b). Over 26 hours the diamond diode degrades and the leakage current increases significantly to the point where the diode is shorted. The instability and increase in leakage current is possibly due to increased defects and threading dislocations due to current induced stress in the diamond bulk or on the etched surface sidewalls of the diode structure, where graphitization can occur. Further research needs to be done to ascertain the source of the degradation and improve the diamond growth and fabrication process.

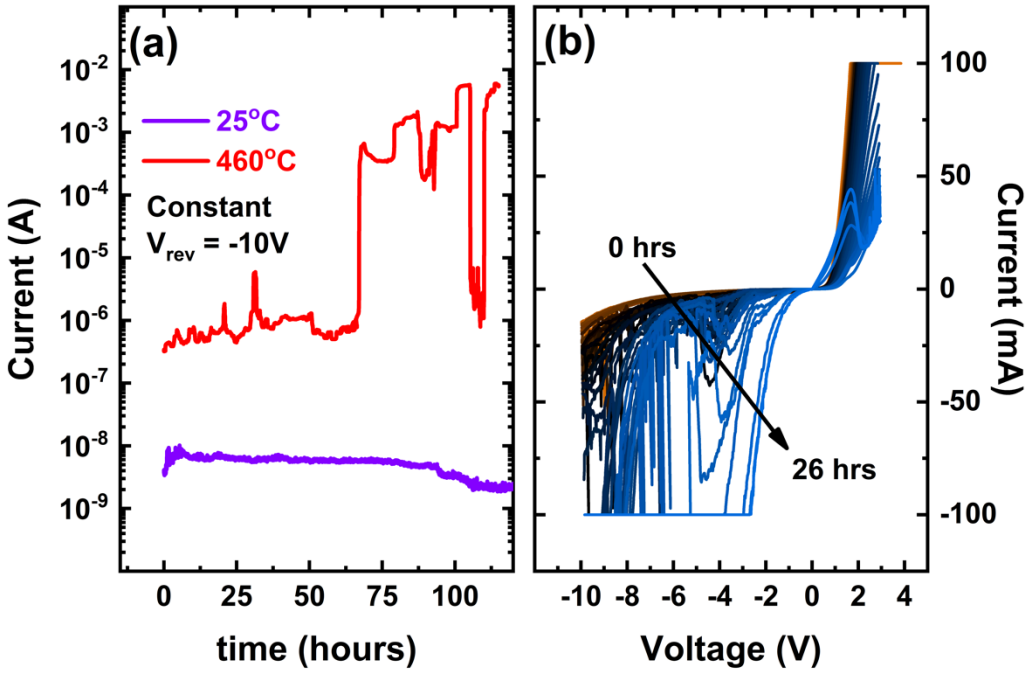

Fig. 5.8 (a) Thermal stressing at room temperature and 460°C for 100+ hours at a constant reverse bias of -10 V and (b) continuous I-V sweeps for 26 hours on diamond SPINDs

5.4 Glen Extreme Environment Rig (GEER) Test Chamber

The GEER apparatus consists of an 800-liter cylindrical shaped stainless-steel pressure vessel outfitted with three internal AC-phase controlled electric heaters and automated gas injection and gas analyzer systems. The GEER test chamber can reproduce the Venusian surface conditions of 467°C, ~ 1330 psi (92 bar) pressure consisting of CO_2 (~96.5%) and N_2 (~3.4%) as well as traces of SO_2 (130 ppm), H_2O (30 ppm), CO (15 ppm), COS (27 ppm), HCl (0.5 ppm), HF (5 ppb), H_2S (3 ppm) and NO (5.5 ppb) [5.4]. A high sensitivity quadrupole mass spectrometer analyzes the gas mixture by sampling aliquots from the GEER chamber at regular intervals. A Raman spectrometer is also present to provide

complementary information based on the vibrational symmetry of the chemical species present in the chamber.

The GEER test chamber is brought to very low pressures $\sim 10^{-6}$ Torr at ambient temperature and is then filled with the Venusian gas mixture. Liquid water is weighed and then added through a fill port on the vessel. All other gas constituents are delivered to the chamber in gas phase using high accuracy mass flow controllers at approximately 34 atm (500 psi). The chamber is heated at $7^{o}\mathrm{C/hr}$ that takes to ~2.5 days to reach the final $460^{o}\mathrm{C}$ temperature and ~92 bar pressure. The temperature is controlled within $1^{o}\mathrm{C}$ and pressure is monitored continuously throughout the experiment. Once a total 10 day of experimentation at the full Venusian atmosphere is performed, the chamber will be cooled in the Venusian atmosphere itself till $300^{o}\mathrm{C}$ and then followed by a cool down in N_2 atmosphere. The active sample in-situ testing will be carried out throughout the span of the GEER test run. Electrical connections to the active devices made through the chamber will be used to continuously monitor the current at a given voltage on the diamond diodes. Every 4 hours a forward and reverse bias I-V sweep will also be performed on the active diamond diode. The data is collected through an automated data acquisition system whose details are described in section 5.5.7. A laptop is used for data logging and is kept outside the GEER chamber room connected by ~80 ft of GPIB cables. A schematic of the GEER chamber operation is as shown in Fig. 5.9 [5.4].

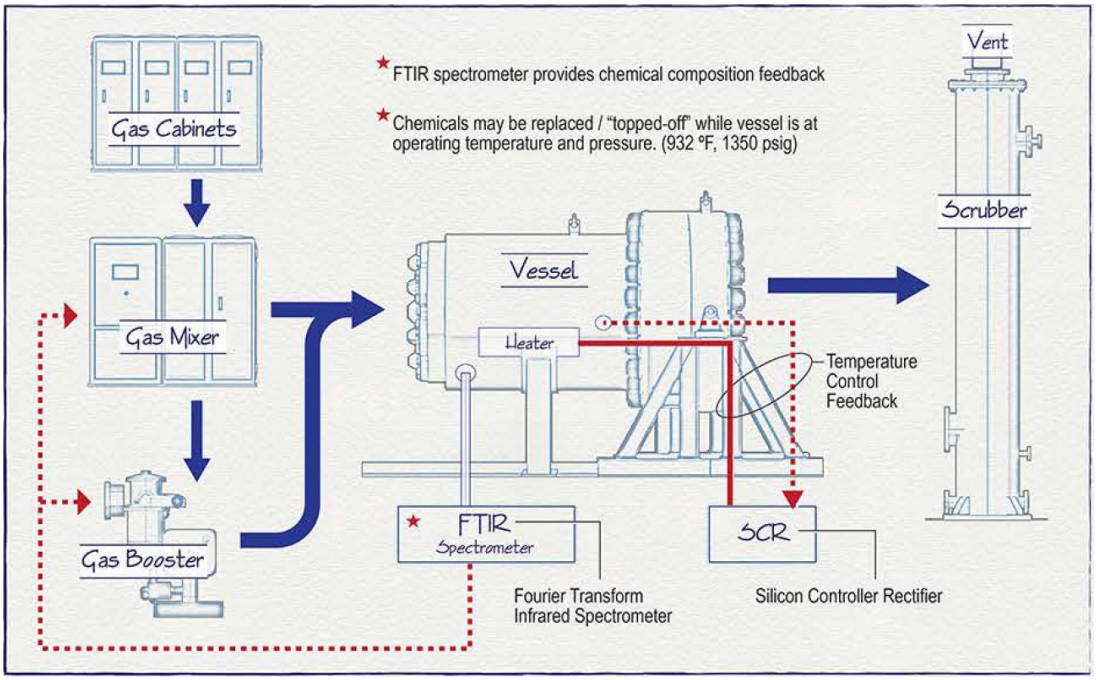

Fig. 5.9 Schematic of the GEER test chamber operation [5.4]

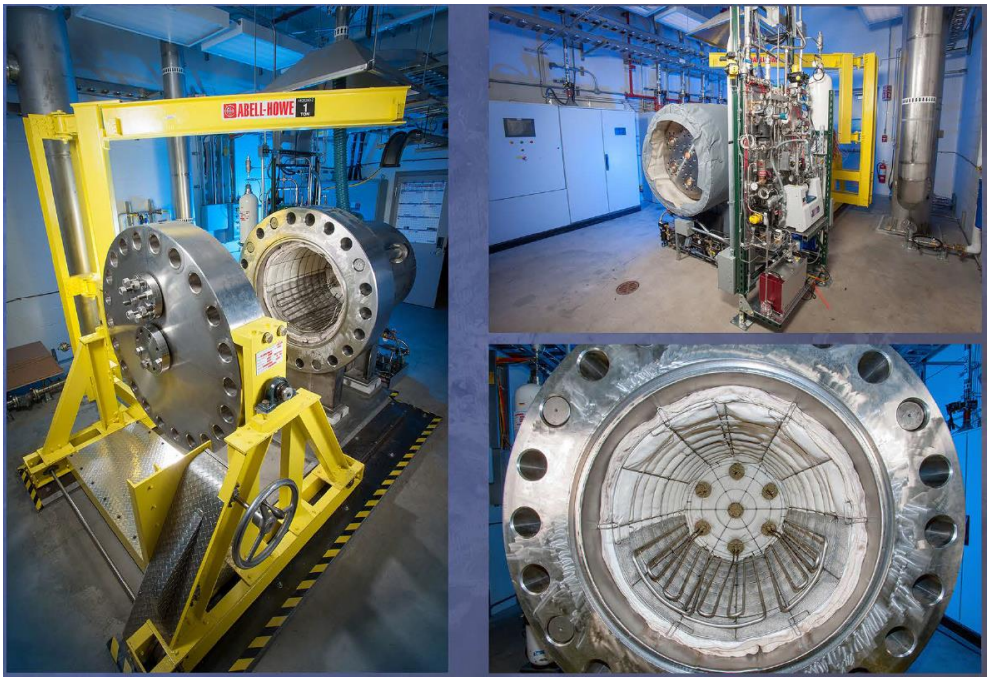

Fig. 5.10 GEER test chamber at the NASA Glenn Research Center, Ohio.

5.5 GEER Sample Preparation and pre-GEER Characterization

In total eight samples were prepared for GEER run out of which five were with patterned diodes and the remaining three un-patterned but with different passivations on the sample surface. Out of the five pattered samples, one (17-050) was selected for active in-situ measurements during the GEER test run. The fabrication process used for the patterned sample is as detailed in chapter 2, section 2.3.

Sample Name	Details	Target n-layer thickness and doping	Target i-layer thickness	Passivation
17-050 (patterned) *Active*	Type IIb, [111] orientation, SPIND	600 nm, $\sim 4 \times 10^{19}/\mathrm{cm}^3$	~1 µm	200 nm SiO_2
20-054 (patterned) *Passive*	Type IIb, [111] orientation, SPIND	200 nm, $\sim 1 \times 10^{19}/\mathrm{cm}^3$	~750 nm	200 nm Al_2O_3
20-055 (patterned) *Passive*	Type IIb, [111] orientation, SPIND	200 nm, $\sim 1 \times 10^{19}/\mathrm{cm}^3$	~750 nm	Un-passivated
20-058 (patterned) *Passive*	Type IIb, [111] orientation, SPIND	200 nm, $\sim 1 \times 10^{19}/\mathrm{cm}^3$	~750 nm	200 nm Si_3N_4
20-059 (patterned) *Passive*	Type IIb, [100] orientation, Schottky	-	~750 nm	Un-passivated
1b p^+ *Passive*	Type IIb, [100] orientation	-	-	200 nm Al_2O_3
1b p^+ *Passive*	Type IIb, [100] orientation	-	-	200 nm Si_3N_4
1b p^+ *Passive*	Type IIb, [100] orientation	-	-	Un-passivated

Table 5.1 Details of samples prepared for GEER test run

Table 5.1 details a list of samples prepared for the GEER test. A SIMS analysis was also done on the 17-050 active sample and the P and B doping profiles were extracted, as shown in Fig. 5.11.

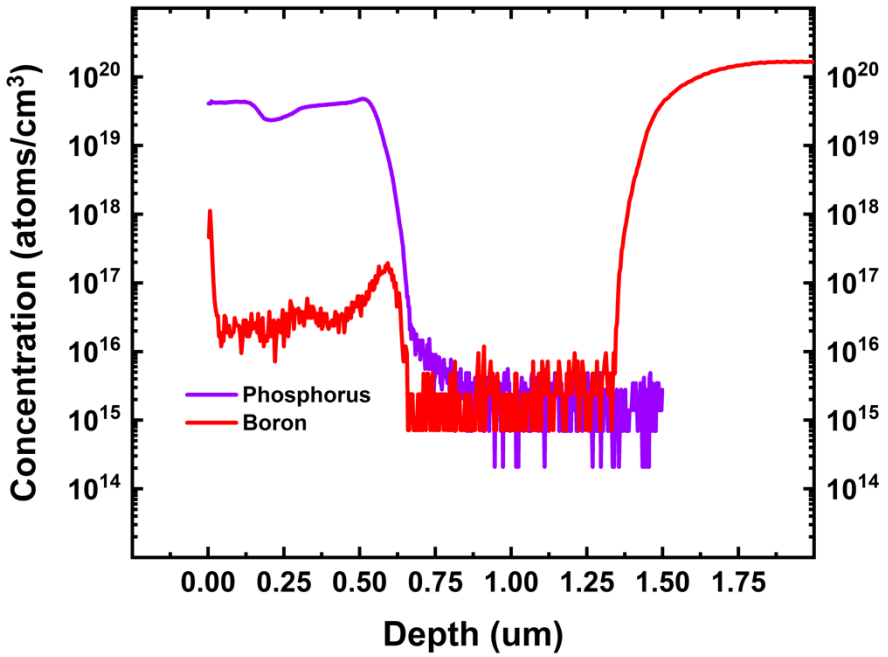

Fig. 5.11 SIMS analysis profile of the 17-050 active sample with P and B doping concentration profiles.

The patterned samples have a total number of 282 diodes each with diode diameters ranging from $10\,\mu m$ to $800\,\mu m$. Fig. 5.12 shows microscope images of the PIND representative 17-050 active sample and Schottky 20-059 sample.

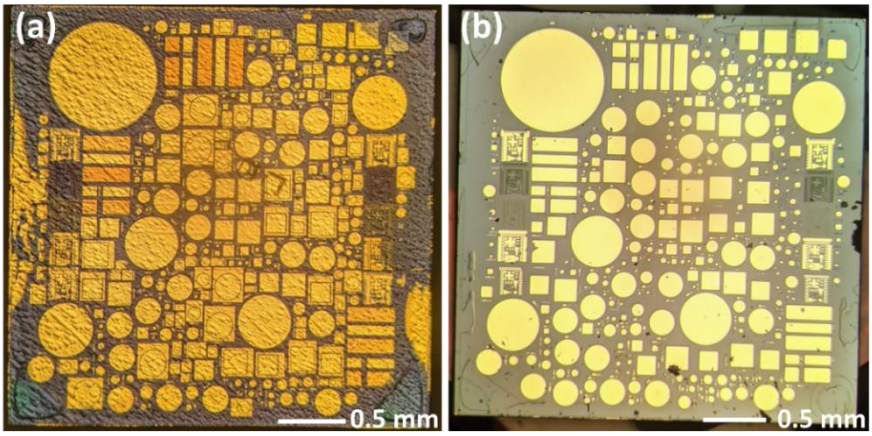

Fig. 5.12 Microscope images of patterned (a) 17-050 PIND and (b) 20-059 Schottky diode samples

All diodes on the patterned samples were characterized at room temperature by *I-V* measurements. Several other measurements were also performed to fully characterize the samples before subjecting them to harsh environments during the GEER testing. All the passive samples are mounted on a 4x2 cm alumina PCB while the active sample is mounted on a ceramic PCB. The following sub-sections detail the pre-GEER measurements and packaging.

5.5.1 Room Temperature I-V Characterization

All 282 diodes on each patterned GEER sample (17-050, 20-054, 20-055, 20-058 and 20-059) were measured for their dc $I-V$ characteristics. Fig. 5.13 shows the $I-V$ characteristics of diodes ranging in diameter from $25\ \mu m$ to $800\ \mu m$ for the 17-050 PIND and 20-059 Schottky diode samples. A high on-off ratio of 3×10^{14} and 4×10^{15} is obtained for 17-050 and 20-059 samples, respectively. Both samples show excellent ultra-low leakage current characteristics in the reverse bias. An in-house Python driver program

was written for a Keithley 2461 high current source meter and was used to perform the $I-V$ measurements and data acquisition. An averaging time of 200 msec was maintained for all the dc IV measurements.

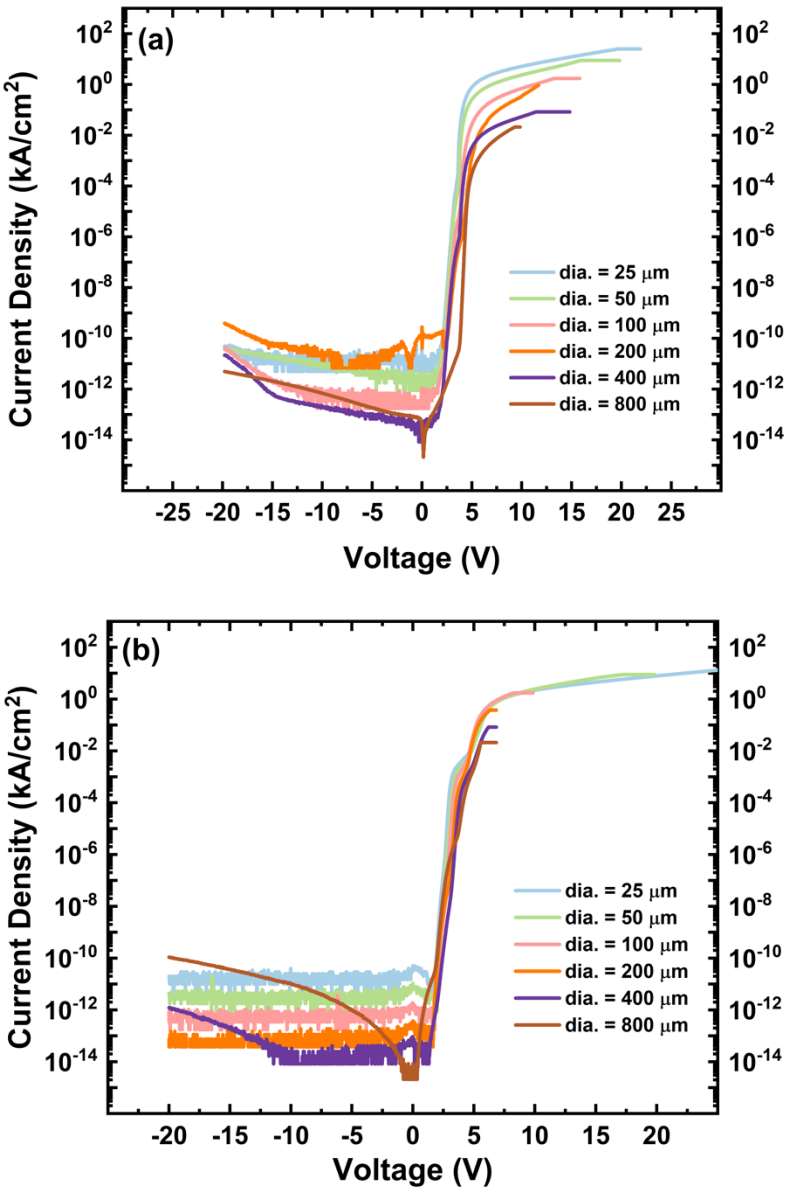

Fig. 5.13 Room temperature I-V characteristics of (a) 17-050 SPIND and (b) 20-059 Schottky diode samples with varying diode diameters on each sample.

A Python program was also written to parse all the $I-V$ data using Pandas dataframe library modules. Wafer maps of maximum measured current density, leakage current at 20 V reverse bias and the current on-off ratio were created for all the samples. Fig. 5.14 shows representative wafer maps of the 20-059 Schottky sample. A similar assessment of wafer maps will be created post-GEER test run and comparison of diode performance and survivability will be made.

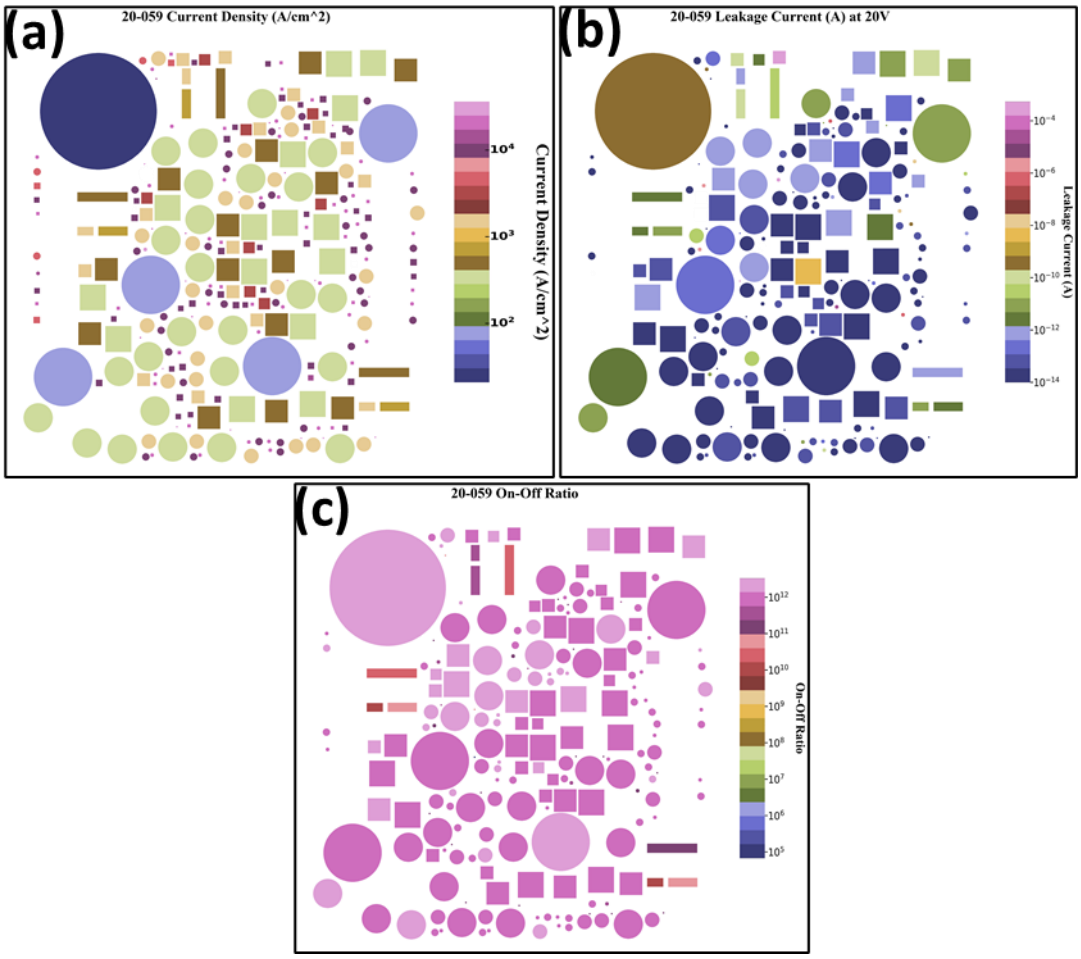

Fig. 5.14 Wafer maps of (a) current density at 20 V forward bias, (b) leakage current density at -20 V reverse bias and (c) maximum current on-off ratio of the 20-059 Schottky diode sample

5.5.2 Leakage Current and Surface Passivation

The leakage current data at $20\,V$ reverse bias for all samples was collected and analyzed. Fig. 5.15 shows the spread of leakage current levels for diodes with diameters ranging from 25 μm to 400 μm for all the patterned samples: 20-054, 20-055, 20-058, 20-059 and 17-050 with Al_2O_3, none, Si_3N_4, none and SiO_2 surface passivations, respectively.

A clear trend in surface passivation and leakage current cannot be established and a sample-to-sample variation is seen with the 20-059 Schottky diode showing the lowest current leakage. However, these surface passivations are useful in suppressing leakage current through sidewalls of the partially etched mesa diodes on all patterned samples.

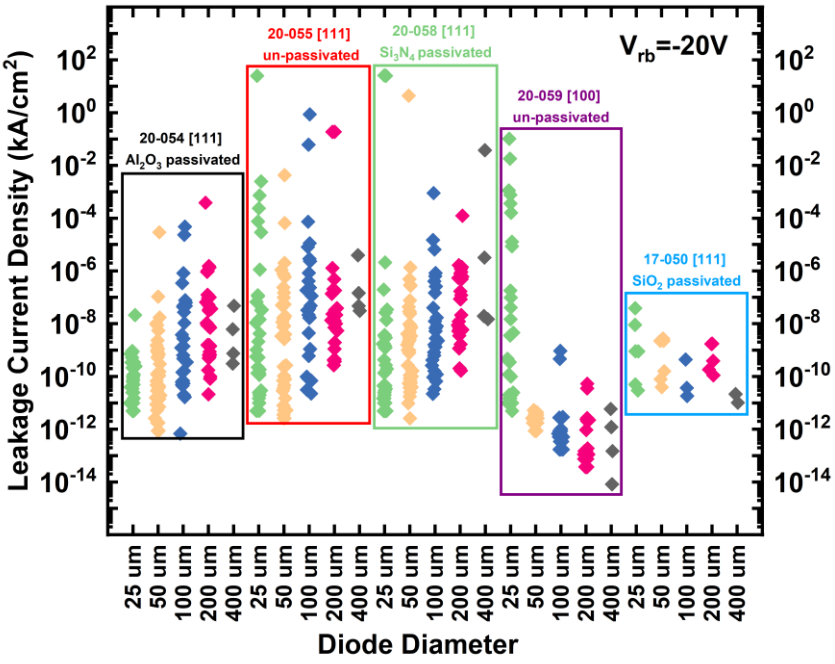

Fig. 5.15 Leakage current density comparison of 20-054, 20-055, 20-058, 20-059 and 17-050 samples with Al_2O_3, none, Si_3N_4, none and SiO_2 surface passivations, respectively.

5.5.3 High Temperature I-V characteristics

High temperature performance of all patterned GEER test samples was evaluated from room temperature to 500^oC. A Linkam THMS600 hot stage with computer control was used to ramp through increasing temperature cycles. Fig. 5.16 shows the logarithmic and linear (inset) high temperature J-V characteristics of the 17-050 active sample from room temperature to 500^oC. Following sub-sections provide detailed forward and reverse bias

analysis and useful insights into the high temperature performance of the 17-050 active sample.

5.5.3.1 High Temperature Forward Bias Analysis

A forward current density of 20 A/cm^2 is obtained at ~10 V at 25^oC and at ~5.5 V at 500^oC. The diode turn-on voltage decreases from ~7.9 V at room temperature to ~4.7 V at 500^oC, as shown in Fig. 5.18. The ideality factor (Fig. 5.18) non-linearly rises from a near ideal ~2.2, indicating ohmic contacts to a two-carrier (electrons and holes) current conduction at room temperature to ~3.8 at 500^oC, indicating non-idealities caused by interface states, barrier inhomogeneities and image force effect. The ideality factor also decreases suddenly at 225^oC to a value of ~2.1 possibly due to contact annealing effects during temperature cycling.

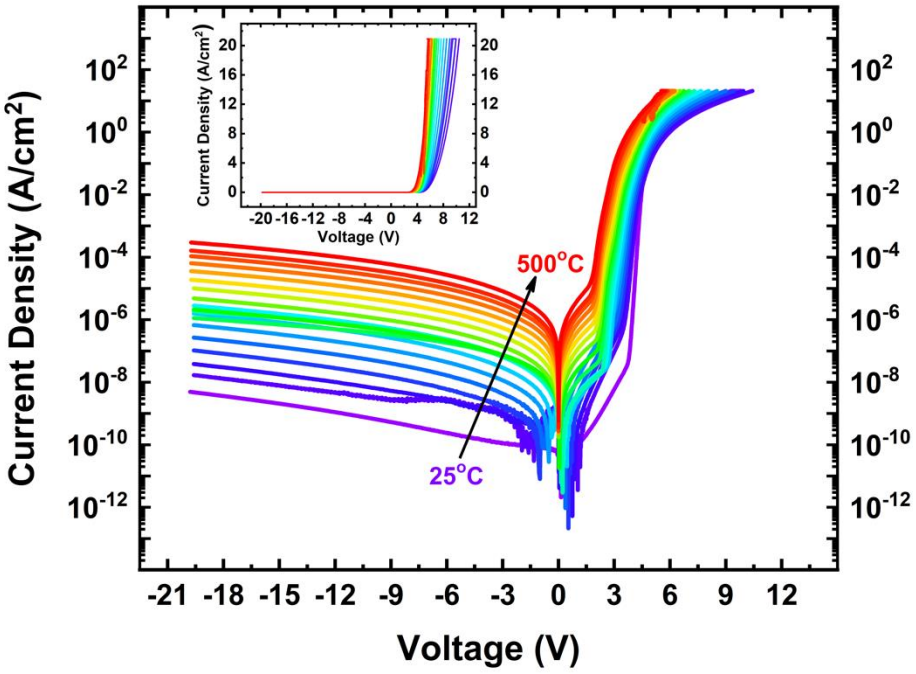

Fig. 5.16 High temperature logarithmic and (inset) linear J-V characteristics of the 17-050 active diamond SPIND sample

The 17-050 SPIND consists of a *p*-*i*-*n* junction barrier and a Schottky barrier at the metal cathode to *n*-layer diamond interface. During the forward bias operation, the *p*-*i*-*n* junction barrier, E_{PN}, reduces with increasing forward voltage V_{FWD} while the Schottky barrier at the cathode, E_{CD}, gets reverse biased. With a Ti metal contact work-function $\phi_M = \sim 4.55$ eV, a Schottky barrier to electrons is formed at the interface with the Fermi level pinned to a certain level determined by the interface states. Therefore, with increasing V_{FWD}, the barrier for electrons to diffuse across the *i*-layer into the p^{++}-layer to form an electron minority charge current and the barrier for holes to diffuse across the *i*-layer into the *n*-layer to form a hole minority charge current decreases with decreasing E_{PN}. This was verified using Silvaco ATLAS simulations of the 17-050 SPIND sample using P and B

doping profile obtained experimentally from SIMS analysis shown in Fig. 5.11. As seen by the band diagram at increasing V_{FWD} in Fig. 5.17, the E_{PN}, measured from the conduction band energy E_{CB} in the p^{++}-layer to the E_{CB} in the *n*-layer, decreases while the E_{CD}, measured from the E_{CB} edge at the cathode Schottky contact to the E_{CB} in the *n*-layer, increases. Therefore, the total barrier height experienced by the electrons depends on the dominant barrier height i.e., E_{CD} or E_{PN}, at a given forward bias. This can be seen from Fig. 5.19. Due to the electron Schottky barrier at the cathode, the electron injection is reduced significantly in comparison to the hole injection from the p^{++}-layer. Practically, however, the Fermi pinning level is observed to decrease with increasing temperature and thereby reducing the electron Schottky barrier height (SBH) at the cathode, as shown by Fig. 5.21. The barrier height, ϕ_B, vs. V_{FWD} was obtained by calculating the slope of Arrhenius plots - $\ln(I/T^2)\ vs.\ (1000/T)$, at different T_C and V_{FWD} values, as given by equation (5. 6) and shown in Fig. 5.20.

$$\phi_B = \frac{V_{FWD}}{n} - \frac{2.3k_B}{q}\frac{\partial(\ln(I/T^2))}{\partial(1/T)} \tag{5. 6}$$

The decreasing Fermi pinning with temperature could not be realized from the Silvaco ATLAS simulations. However, an excellent qualitative comparison can be made from Fig. 5.19 and Fig. 5.21.

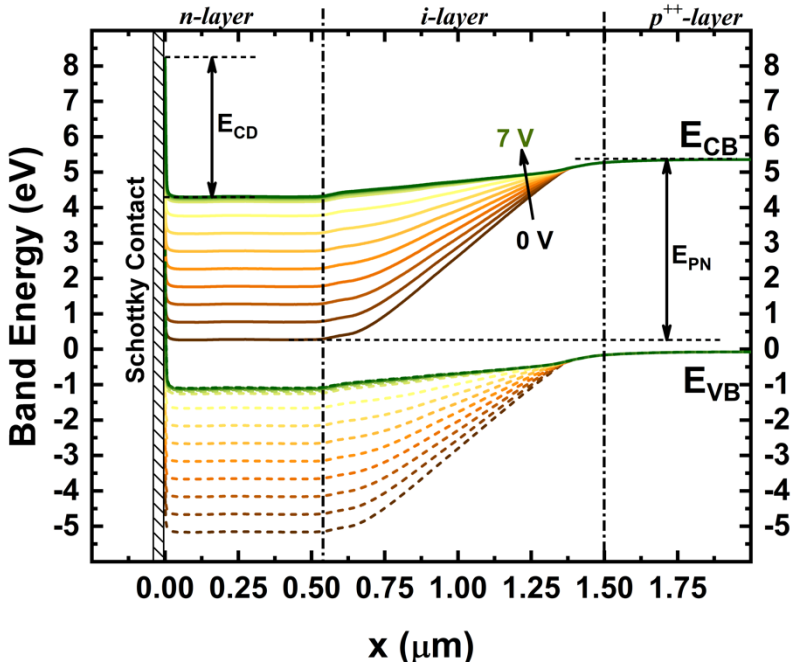

Fig. 5.17 Energy band diagram along the 17-050 SPIND sample at increasing forward bias voltages. The electron Schottky barrier, E_{CD}, at the cathode to *n*-layer interface is measured from the top of the conduction band (E_{CB}) edge at the cathode to the E_{CB} value in the *n*-layer, for all V_{FWD}. The *p*-*i*-*n* junction barrier is measured from the E_{CB} in the p^{++}-layer to the E_{CB} in the *n*-layer.

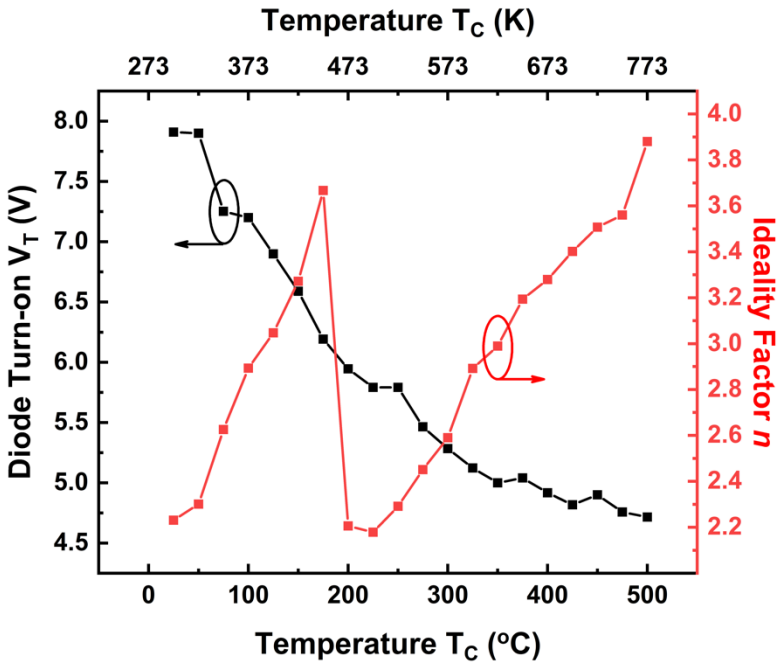

Fig. 5.18 Diode turn-on voltage V_T and ideality factor n as a function of increasing temperature T_C in the 17-050 SPIND sample

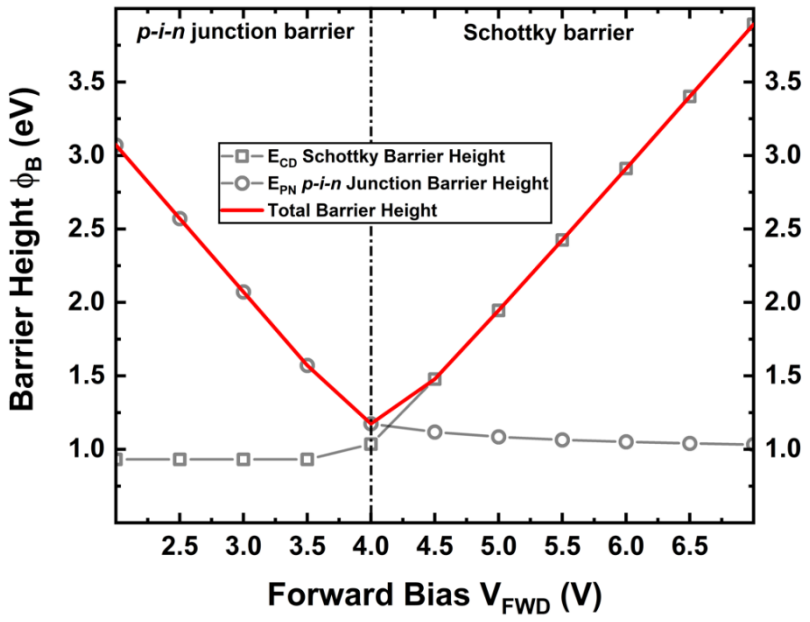

Fig. 5.19 The cathode Schottky barrier height E_{CD}, *p-i-n* junction barrier height and the total electron barrier height obtained from 17-050 SPIND Silvaco ATLAS simulations.

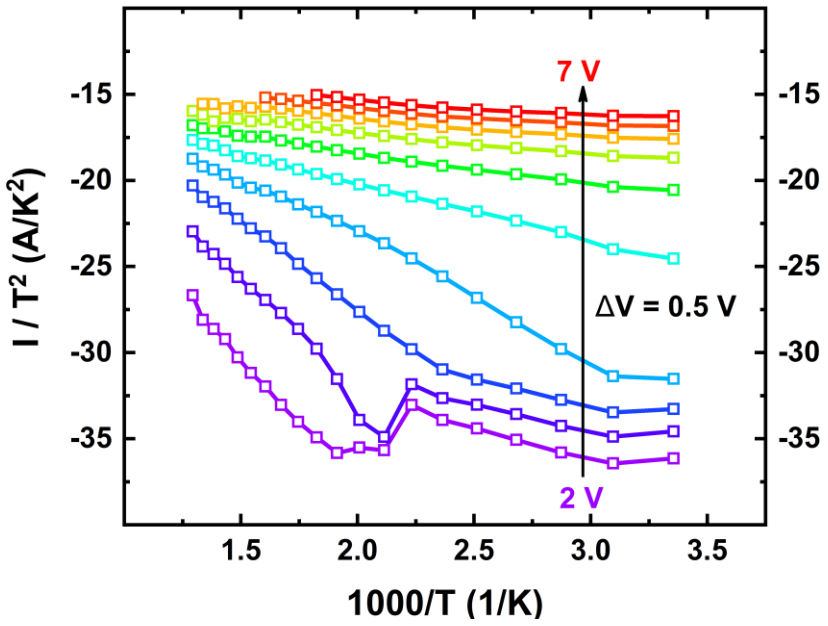

Fig. 5.20 Arrhenius plot - $\ln(I/T^2)$ $vs.$ $(1000/T)$, from experimental 17-050 SPIND I-V measurements at increasing temperature T_C

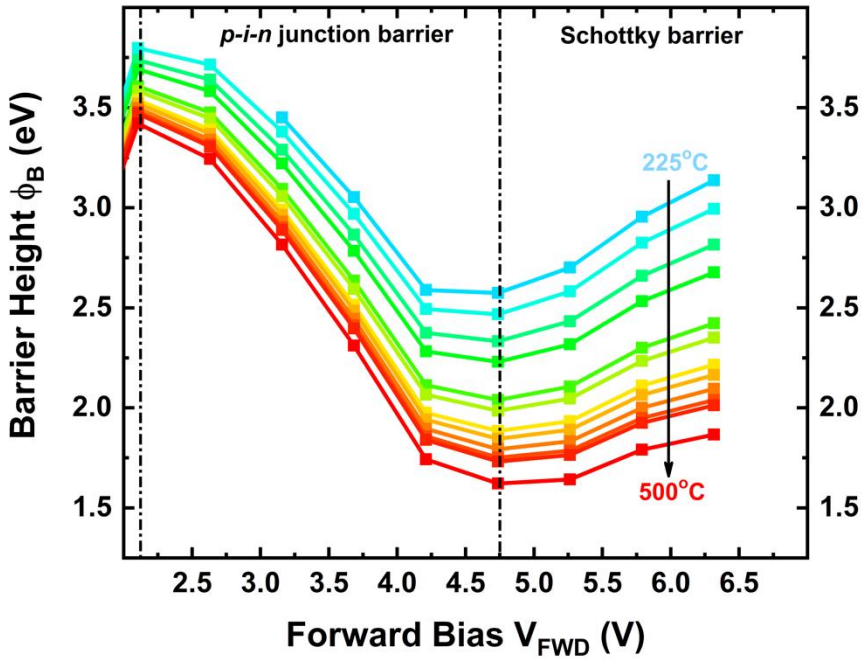

Fig. 5.21 Barrier height ϕ_B as a function of increasing forward bias V_{FWD} at varying temperatures T_C obtained from the Arrhenius plots of 17-050 SPIND sample

Due to the decrease in the electron SBH at high temperatures, the electron minority current increases in the diamond SPIND forward bias conduction. This is corroborated experimentally by brighter light emission from the 17-050 SPIND at $500^{o}C$, indicating the presence of increased electron-hole recombination, as shown in Fig. 5.22.

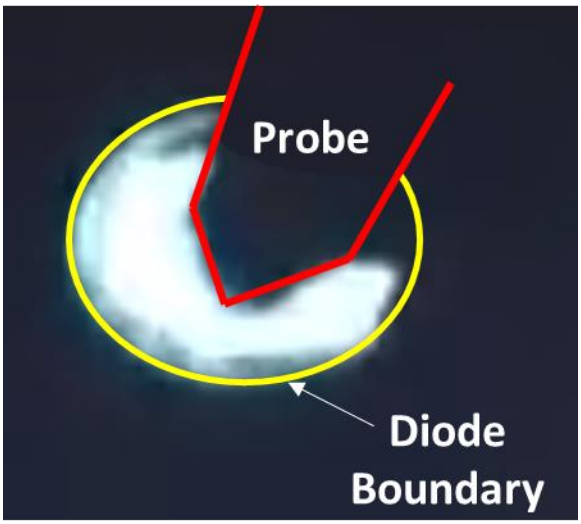

Fig. 5.22 Light emission at $500^{o}C$ from 17-050 SPIND

5.5.3.2 High Temperature Reverse Bias Analysis

Threading dislocations (TDs) and defects in diamond have been shown to cause leakage currents [[5.5] - [5.8]] through multiple parallel paths as shown in [5.8]. These parallel leakage paths degrade the high temperature diode reverse bias performance through increased leakage current. At low electric field or low reverse bias voltages, hopping conduction, through localized states in the bandgap, is the dominant conduction mechanism while Poole-Frenkel Emission (PFE), between Coulombic potentials in the

bandgap, dominates at high electric fields or increased reverse bias voltages. The current associated with PFE can be given by [[5.9], [5.10]],

$$I = \frac{A\sigma}{t}\, V \exp\left(-\frac{q\phi_b}{k_B T}\right) \exp\left(\frac{q}{k_B T}\sqrt{\frac{qV}{\pi\epsilon t}}\right) \tag{5. 7}$$

where A is the total cross-section area, t is the thickness over which the TDs are active, ϕ_b is the barrier height for carrier emission from trapped states, V is the applied voltage and ϵ is the diamond optical permittivity [5.8]. The PFE conductivity σ through the continuum states is assumed to be

$$\sigma = \frac{q\mu N_{TD}}{t} \tag{5. 8}$$

where N_{TD} is the threading dislocation density ($/cm^2$) and $\mu(T)$ is the temperature dependent conductivity of diamond given by equation (3.38). With increasing V, the barrier for carrier tunneling is lowered increasing the probability of hopping from/to threading dislocation sites. On the other hand, hopping conduction through thermally assisted tunneling of carriers can be modeled as

$$I = \frac{Aq\alpha N_{TD} v}{t} \exp\left(-\frac{qE_a}{k_B T}\right)\left\{\exp\left(\frac{q\alpha V}{t k_B T}\right) - 1\right\} \tag{5. 9}$$

where α is the hopping distance, v is the thermal vibration frequency of holes at the trap sites and E_a is the activation energy of the traps.

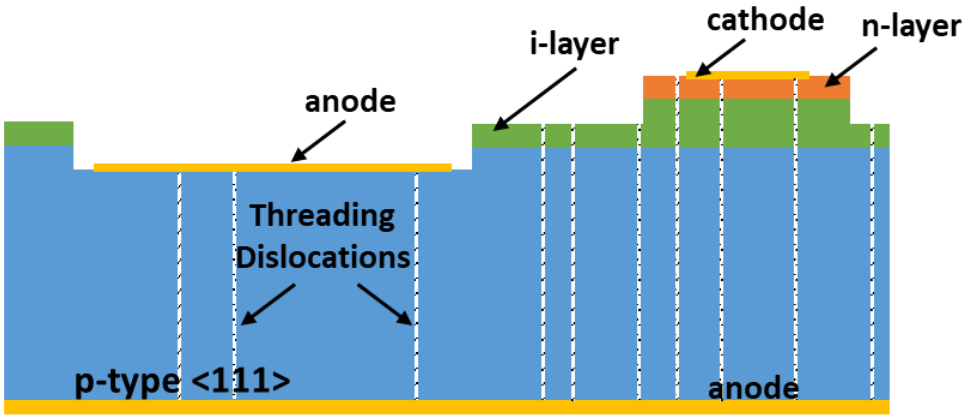

Fig. 5.23 Schematic of diamond SPIND with threading dislocations

The threading dislocation thickness t can be extracted from the experimental reverse bias J-V characteristics of 17-050 sample at different temperatures (Fig. 5.16), by rewriting equation (5. 7) as

$$\ln\left(\frac{I}{V}\right) = b(T) + m(T)\sqrt{V} \tag{5. 10}$$

where,

$$m(T) = \frac{q}{k_B T}\sqrt{\frac{q}{\pi \epsilon t}} \tag{5. 11}$$

$$b(T) = \ln\left(\frac{A\sigma}{t}\right) - \frac{q\phi_b}{k_B T} \tag{5. 12}$$

After obtaining t, N_{TD} and ϕ_b can be obtained by curve-fitting equation (5. 10) to experimental $\ln(I/V)$ vs. $\sqrt{V}$ plot, as shown in Fig. 5.24. An average N_{TD} of $\sim 1.2 \times 10^5\ /cm^2$ is obtained, as shown in Fig. 5.25. The average N_{TD} is in good agreement with values reported in literature $5 \times 10^4 /cm^2$ [5.11], [5.12]. The threading dislocation thickness t varies from a maximum of $\sim$1.36 µm to a minimum of $\sim$0.65 µm, which is in

excellent agreement between the 17-050 sample's *i*-layer thickness ($\sim$1.2 μm) and *n*-layer thickness ($\sim$600 nm), as can be seen from Fig. 5.11. The change in t may be attributed to the annealing/modification of TDs with temperature. The extracted PFE carrier emission energy ϕ_b has an average value of 0.375 eV as shown in Fig. 5.26.

It can be observed from the Fig. 5.24 that the PFE fits very well at high reverse bias voltage V values for the entire temperature range. For low reverse bias voltages, the hopping activation energy is extracted by curve-fitting the hopping current from equation (5. 9) to the measured 17-050 SPIND characteristics at different temperatures. An average E_a of 0.535 eV is extracted, as shown in Fig. 5.26. Fig. 5.27 shows an excellent total analytical fit to the experimental temperature dependent I-V characteristics of 17-050 SPIND.

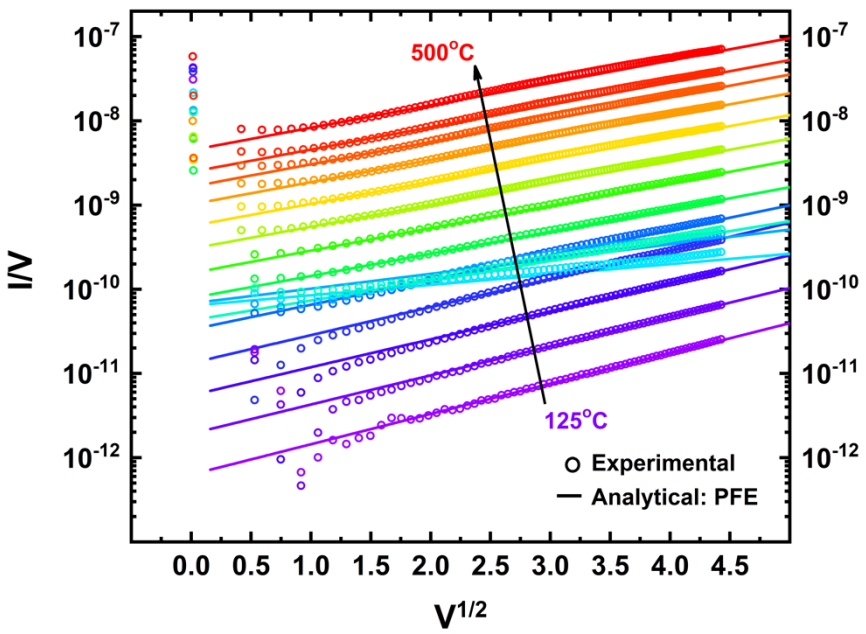

Fig. 5.24 $\ln(I/V)$ vs. $\sqrt{V}$ plot of 17-050 SPIND experimental data (circles) and analytical PFE curve-fit (lines)

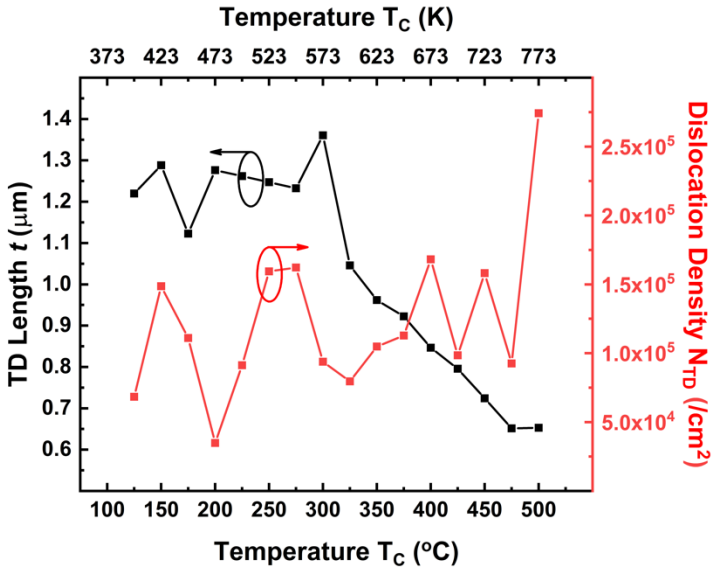

Fig. 5.25 Threading dislocation thickness t and density N_{TD} as a function of temperature T_C obtained from curve-fitting to experimental 17-050 SPIND sample data

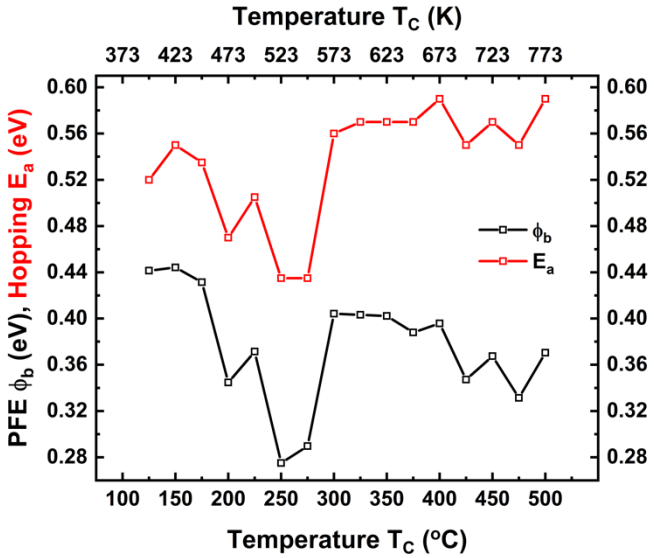

Fig. 5.26 PFE trap state carrier emission barrier ϕ_b and hopping activation energy of state E_a extracted from curve-fitting to 17-050 SPIND temperature dependent characteristics

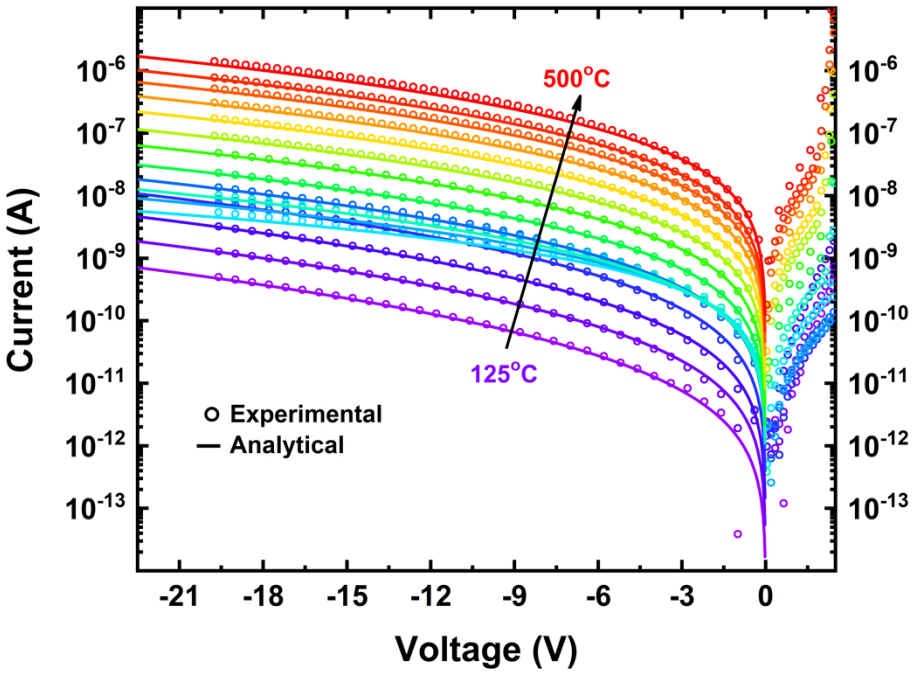

Fig. 5.27 Analytical PFE and hopping leakage current curve-fit to experimental temperature dependent I-V characteristics of 17-050 SPIND

5.5.4 Diode Breakdown Characterization

Diode breakdown measurements were performed on several diodes from the 20-054 and 20-055 samples in order to establish a baseline of material quality of diamond pre-GEER test run. Fig. 5.28 compares the breakdown voltages of several diodes from both the samples. The Al_2O_3 sidewall passivation on the 20-054 sample does not show to improve the breakdown field of the diamond. Changes in diode breakdown measurements post-GEER test run will indicate effects of thermal stress on the diamond bulk material.

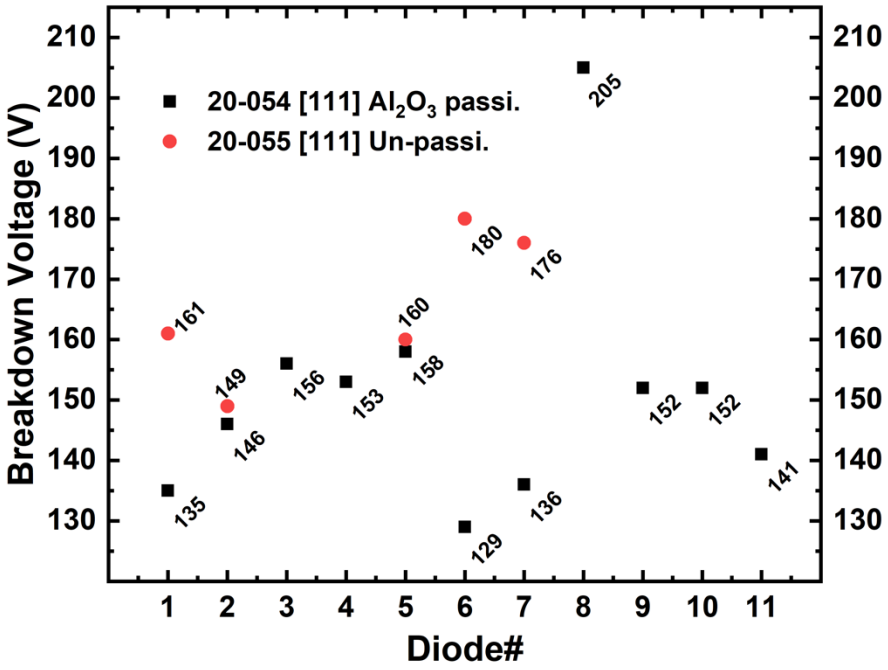

Fig. 5.28 Breakdown voltage of several diodes from 20-054 and 20-055 samples

5.5.5 Scanning Electron Microscopy

Scanning electron microscope (SEM) images were obtained from the surface of several patterned samples as shown in Fig. 5.29. The sample surface topology, including the

diamond surface, metal contacts and surface passivation, is expected to undergo changes due to the thermal and toxic environment stress during the GEER test run. Neudeck *et. al*. [5.13] have observed the growth of PtS "fibers" and Au/PtS "boulders" due reaction with the Sulphur in the GEER chamber environment over the 60-day GEER run time on SiC samples. A post-GEER assessment of the surface topology will be made on all the diamond samples.

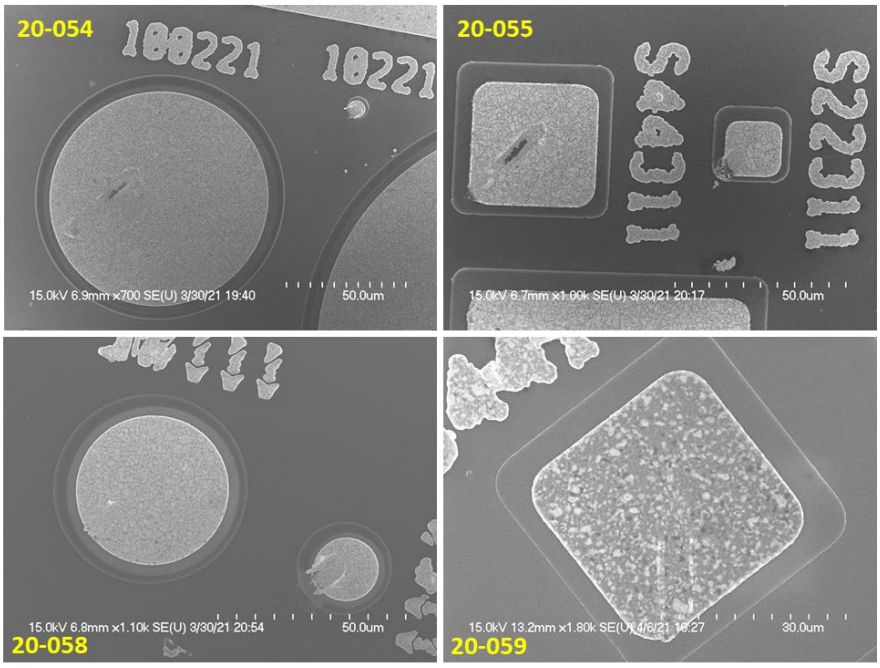

Fig. 5.29 SEM images of 20-054, 20-055, 20-058 and 20-059 patterned GEER samples pre-GEER test run

5.5.6 High Temperature Packaging

All passive GEER samples as detailed in Table 5.1 are mounted on an alumina pcb with gold pads using the 8835 Gold Cement high temperature adhesive, as shown in Fig. 5.30. A thermal cycling at $580^{o}C$ for 1 hour was done to secure the diamond samples to

the gold pads. The active sample (17-050) was also mounted on a ceramic chip carrier. The cathode metal contact of a 800 μm diameter diode on the 17-050 sample was wire bonded to the gold pads on the ceramic chip carrier as shown in Fig. 5.31. Ground connections to the diode were also wire bonded to the top and bottom p^{++}-layer anode contact. All high temperature packaging of diamond samples was done in collaboration with Makel Engineering.

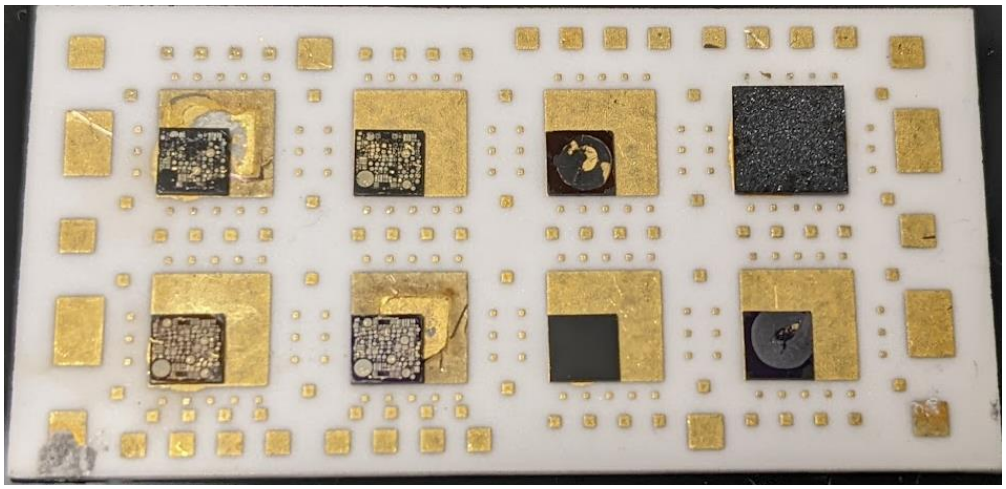

Fig. 5.30 Passive samples mounted on an alumina PCB using a high temperature adhesive

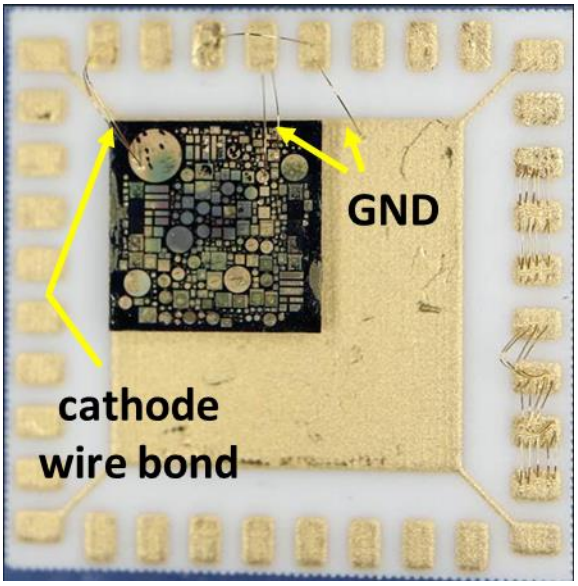

Fig. 5.31 Active 17-050 wire bonded to ceramic chip carrier

5.5.7 Data Acquisition System for In-Situ GEER Measurements

As established earlier, the 17-050 SPIND sample is planned for active in-situ characterization during the operation of the 10-day GEER test run. An automated data acquisition system has been developed in collaboration with ASU, Stanford and MIT. In total 3 devices have been mounted on the ceramic chip carrier and are being in-situ tested during the GEER test run. The data acquisition system is programmed to switch between the 3 devices to acquire data simultaneously. The data acquisition system consists of components listed in Table 5.2. An overall view of the data acquisition system is shown by the schematic in Fig. 5.32.

	Component	Purpose
1	Agilent B2902A SMU	Supply current and voltage and acquire data
2	Computer controlled Keysight U2751A switching matrix	Switch between the 3 devices based on the computer instructions

3	Breakout board	Connects the wire connections from the ceramic chip carrier to the switching matrix
4	USB to ethernet adaptor	Connects the laptop to the switching matrix and SMU via a USB to ethernet connection
5	Laptop	A Python program with a data acquisition and auto-switching algorithm controls the SMU switching matrix
6	80 ft USB and ethernet cables	Long USB and ethernet cables to connect from outside of the GEER room to the inside

Table 5.2 Components of the data acquisition system used for in-situ measurements during the GEER test run

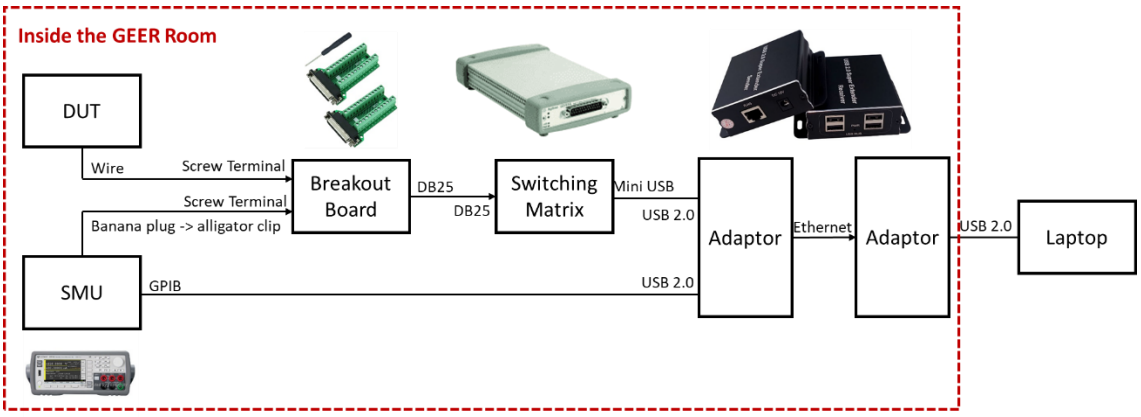

Fig. 5.32 Schematic of the data acquisition system developed in collaboration with ASU, Stanford and MIT for in-situ measurements during the GEER test run.

The 17-050 SPIND active sample is programmed to be continuously measured for current at a reverse bias of -10 V and a full reverse to forward I-V characterization every 4 hours. An additional “resistor” consisting of two shorted gold pads on the ceramic chip carrier is will also be monitored to assess the wire resistance of other device connections during the GEER test run.

5.6 Diamond JFET for High Temperature Power Converters

To achieve functional robotics on board of surface landers on Venus, the electronic components need to be designed for the Venusian atmospheric conditions i.e., for 460°C and 92 *bar* pressure of toxic environment. By demonstrating $500^{o}\mathrm{C}$ operable diamond *p*-*n* junction diodes with high current carrying capacities, we propose diamond Junction Field Effect Transistors (JFETs) for high temperature power converters. Two JFET designs were developed and simulated in Silvaco ATLAS TCAD viz. lateral and vertical JFETs. The design of a *p*-channel lateral JFET is as shown in Fig. 5.33. A gate to source length L_{GS}, gate to drain length L_{GD} and gate length L_G of 1μm are simulated. The *p*-channel is B doped at $10^{18}/\mathrm{cm}^3$ concentration and is 175 nm thick. A 400 nm thick $10^{20}/\mathrm{cm}^3$ doped n^{++}-doped diamond layer of 400 nm thickness is added in between the *p*-channel and the intrinsic or N doped diamond substrate. The n^{++}-layer prevents leakage current through the substrate by creating a depletion layer below the *p*-channel. The gate also consists of a $10^{20}/\mathrm{cm}^3$ doped n^{++} diamond and controls the channel width by modulating the depletion region below the gate, as shown by the current density contour plot in Fig. 5.34. Fig. 5.35(a) shows the normally-on I_D-V_D characteristics of the *p*-channel lateral JFET. A maximum of 0.1 mA/mm current density is achieved at a gate voltage V_G of 0 V and V_{DS} of 50 V. A cut-off V_G threshold is of ~16 V. However, the JFET is much more efficient at high temperature due to the increased free hole charge carrier density in the incompletely ionized p-channel. In comparison, the maximum current density at $500^{o}\mathrm{C}$ is ~200 mA/mm at 0 V V_G and V_{DS}

of 50 V i.e., a 2000x increase. Therefore, to obtain current capacity of 1 A at 500°C, a total of 5 mm channel length of the JFET can be designed.

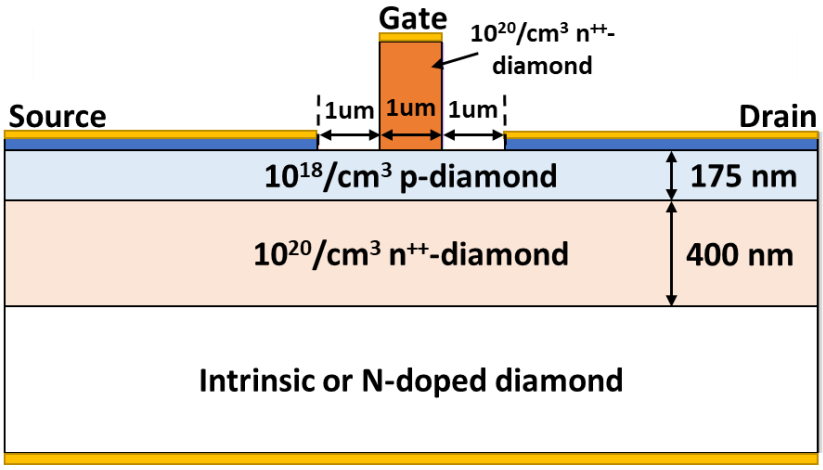

Fig. 5.33 Diamond lateral JFET with a 175 nm thick p-channel on a highly doped n^{++} diamond layer

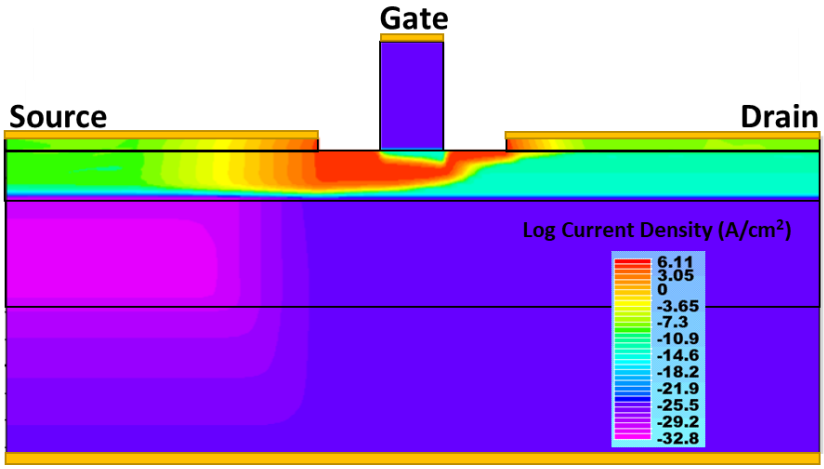

Fig. 5.34 Current density contour plot of an operation p-channel lateral JFET obtained from Silvaco ATLAS simulations

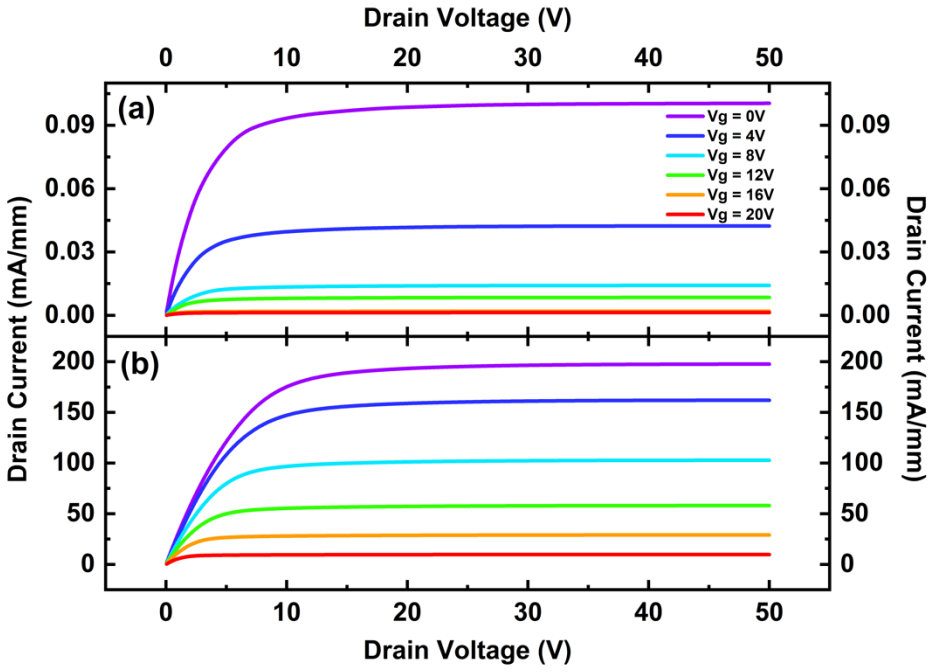

Fig. 5.35 $I_D - V_D$ characteristics of the lateral *p*-channel diamond JFET at (a) room temperature and at (b) 500°C

To achieve a more robust design in terms of both high current and high breakdown voltage, p-channel vertical JFET design is also proposed. As shown in Fig. 5.36(a), the *p*-channel vertical JFET designs consists of an 850 nm wide *p*-channel aperture with two current blocking n^{++}-layers on each side. The *p*-channel is $10^{16}/\text{cm}^3$ B doped and 3 µm thick out of which 1 µm consists of the channel aperture. A highly doped p^+ source of $5 \times 10^{19}/cm^3$ B doping is added below the source contact. The *p*-channel rests on a highly doped ($2 \times 10^{20}/\text{cm}^3$) p^{++} substrate that is connected to the drain contact. The vertical JFET is designed to achieve normally off operation. This is achieved by the depletion of the *p*-channel aperture being depleted from both sides by the n^{++} blocking layers connected to the gate contact. When the channel is formed, current flows vertically from

the source contact to the drain contact, as shown in Fig. 5.36(b). Non-ideal I_D-V_D characteristics are achieved at room temperature due to incomplete ionization with a maximum current density of 50 mA/mm at V_G of -4.5 V and V_{DS} of 50 V, as shown in Fig. 5.37. However, the vertical JFET performs much more efficiently at 500°C with a maximum current density of ~500 mA/mm at V_G of -4.5 V and V_{DS} of 50 V i.e., a ~100x increase. The breakdown characteristics were also simulated using the impact ionization parameters described in Chapter 3, Section 3.3.4. Excellent breakdown characteristics are achieved with ~ 550 V blocking voltage for a V_G of 30 V, as shown in Fig. 5.38.

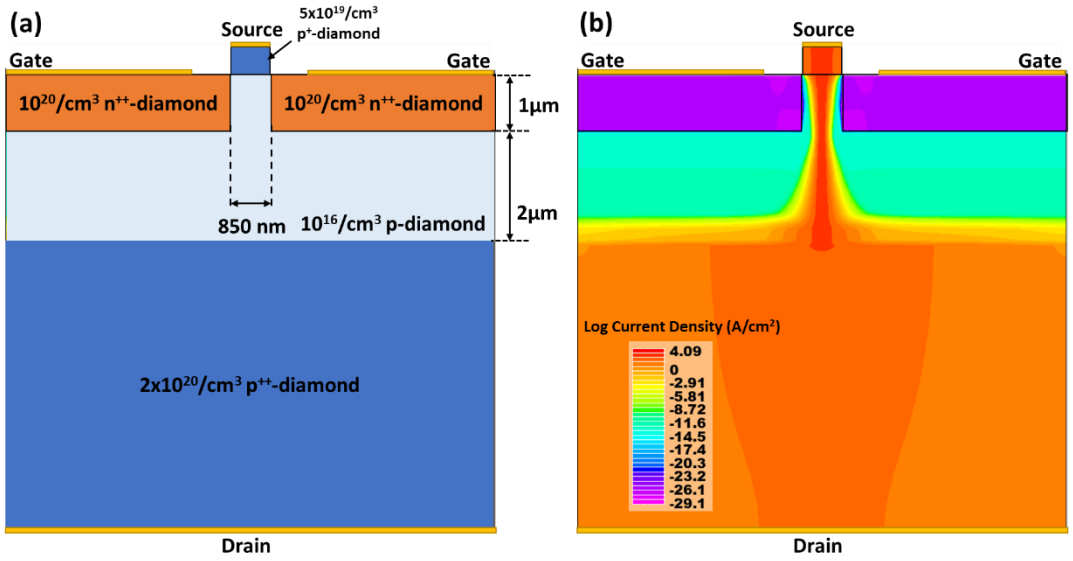

Fig. 5.36 (a) Vertical *p*-channel JFET design (b) Current density contour plot indicating the vertical current flow in the *p*-channel vertical diamond JFET simulated in Silvaco ATLAS

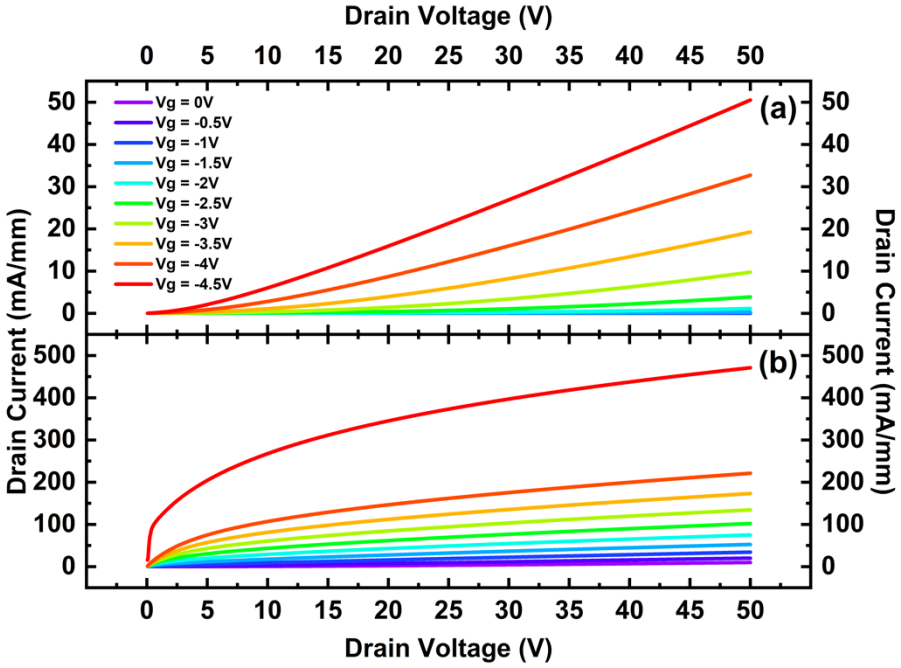

Fig. 5.37 $I_D - V_D$ characteristics of the vertical *p*-channel diamond JFET at (a) room temperature and at (b) 500°C

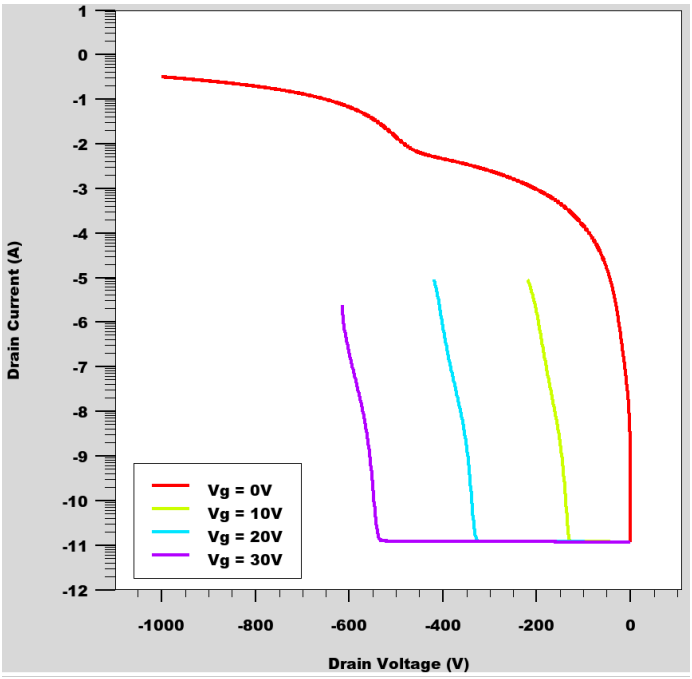

Fig. 5.38 Breakdown characteristics of vertical p-channel JFET with increasing V_G. A ~550 V blocking voltage is achieved for a V_G of 30 V.

To demonstrate the capability of the vertical JFET at high temperature, a DC-DC buck power converter circuit was also simulated. The buck converter is based on pulse width modulation in which the DC input voltage is sampled and reduced or increased based on the sampling period. The buck converter circuit consists of a diode, a 1 mH inductor and a 10 µF capacitor required to take the modulated waveform and convert back to a DC voltage at the resistive load of 10 kΩ. The switching device in this case is the vertical JFET in Fig. 5.36 with the I-V characteristics of Fig. 5.37(b) at 500°C. The diode is a high temperature diamond Schottky-PIN diode which has large breakdown voltage and low R_{ON}. Fig. 5.40 shows the transient waveforms from the output of the buck converter circuit operated in the down converting mode. The load voltage V_{Load} is down converted to -3 V

from the input voltage V_d of -50 V by modulating the vertical JFET to turn on and off using a pulsing gate voltage V_G. Negligible ripple is observed at the load.

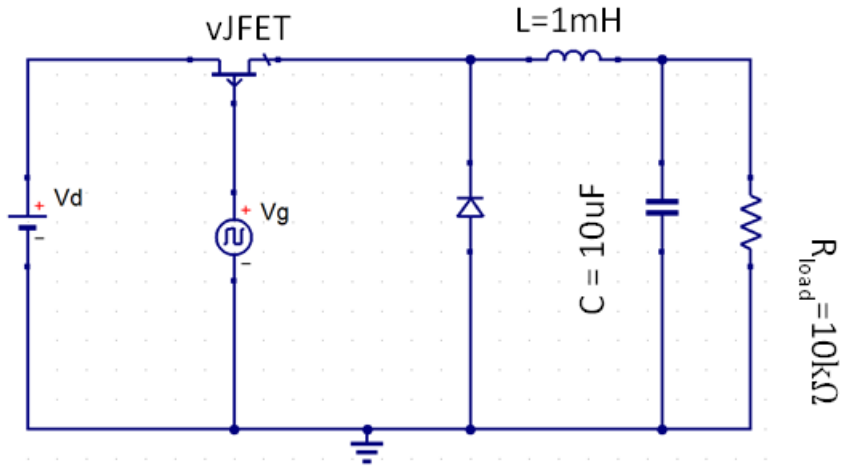

Fig. 5.39 DC-DC buck power converter circuit using the vertical p-channel diamond JFET

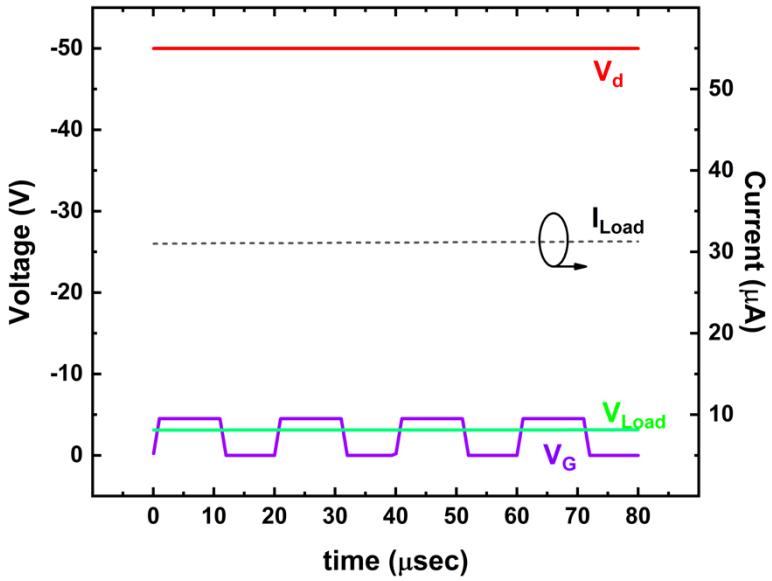

Fig. 5.40 Transient waveforms of the down converted load current and voltage and the pulsing gate voltage V_G

5.7 Conclusion

Diamond diodes were fabricated, tested and analyzed at high temperatures (500^{o}C) and high pressure (~92 atm) in CO2 for 100 hours at the UARK facility. Very small increase in leakage current and small change in forward current – voltage characteristics was observed post-UARK run. Based on these preliminary testing, 5 diamond diode samples and additional 3 diamond samples are prepared to be tested at the NASA GEER test chamber in Venusian atmosphere for 10 days. All the diamond diodes have been thoroughly characterized electrically at room and high temperatures. Excellent on-off ratios are achieved even at 500^{o}C with low leakage currents. Analysis was also done on the high temperature forward and reverse bias characteristics of the diamond diodes. A combined *p-i-n* junction and cathode Schottky barrier was extracted from Arrhenius plots and verified through Silvaco ATLAS simulations. An analytical current – voltage model was built based on hopping conduction and PFE and excellent fit to the high temperature reverse leakage current of experimental diamond diode measurements was achieved. An average $1.2 \times 10^{5}/\mathrm{cm}^{2}$ threading dislocation density was extracted from the analytical fitting. The passive diamond samples for GEER test run were packaged onto an alumina pcb while the active sample was packaged and wire bonded onto a ceramic chip carrier, in collaboration with Makel Engineering. An automated data acquisition system was also built for the in-situ GEER test measurements in a collaborative effort between ASU, Stanford an MIT. High temperature effects on the incomplete ionization, hopping mobility and resistivity were also modeled. Based on the diamond models developed in Silvaco ATLAS, designs

for high temperature lateral and vertical JFETs were also proposed in order to demonstrate a simulation of a high temperature DC-DC buck power converter.

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CHAPTER 6

CONCLUSION AND FUTURE RESEARCH

6.1 Conclusion

The research presented in this thesis demonstrates the feasibility of diamond as an excellent WBG material for high power, high frequency and high temperature applications through experimentation and modeling. Experimentally, diamond diodes with the highest reported current density of ~116 kA/cm^2 were demonstrated, RF characterization from 0.1 GHz to 25 GHz was performed on diamond diodes in a shunt configuration and diamond diodes were developed to work at 500^{o}C. Theoretically, an analytical model of a diamond diode with thermionic emission and space charge limited or Mott-Gurney current including trap levels, and a Silvaco ATLAS model with incomplete ionization, hopping mobility, velocity saturation and SRH recombination was constructed. Through curve-fitting to the ~116 kA/cm^2 current density experimental result, both the analytical and Silvaco ATLAS models explicitly show the transition from thermionic emission to space charge limited conduction in the diamond diodes. Depending on the number of trap levels and their densities, this transition is delayed in voltage and the forward current density is also reduced. The models also predict that the diode R_{ON} becomes a linear function of voltage due to the Mott-Gurney square law for trap free conduction and it saturates to a constant value in the case of a series parasitic resistance. Thus, a theoretical limit is established to the lowest R_{ON} values that can be achieved in diamond diodes. The Mott-Gurney law influenced R_{ON} also affects the Baliga Figure of Merit (BFOM), through which predictions

about diamond and other WBG materials' capabilities as high voltage semiconductors are made. We show here, that instead of the traditionally followed $R_{ON} \propto V_B^2$ relation, the correct relation in the presence of SCL current is $R_{ON} \propto V_B^3/V_{FWD}$ i.e., the R_{ON} vs. breakdown relation is cubic instead of square and also depends on the on-state voltage. This corrected formulation shows an improved BFOM over the traditional relation for diamond up to a certain breakdown voltage. Impact ionization simulations were also done on diamond diodes and it was observed that due to incomplete ionization, the Mott-Gurney R_{ON} dominates, even for drift layer doping as high as 10^{18} /cm^3. However, for very high breakdown voltages realized by large drift layers, the transit time of carriers across the drift layer becomes larger than the dielectric relaxation time, in which case the Mott-Gurney dominated R_{ON} reverts back to an ohmic R_{ON}. Silvaco ATLAS models were also employed to simulate self-heating effects in ideal and practical diamond diodes where the thermal conductivity is 22 W/cm-K and 10 W/cm-K, respectively. For a nominal on-state power of 100 W, the predicted ideal and practical self-heating temperatures are 334 K and 572 K, respectively.

The RF analytical modeling involved formulating a diode equivalent circuit with a resistance and capacitance in parallel that are in series with the contact resistance. This diode equivalent circuit reproduced the experimental small-signal RF parameters (S-parameters and impedance) to a high degree of accuracy over a frequency range of 0.1 GHz to 25 GHz. Silvaco ATLAS models were then constructed to optimize the F_{CO} figure of merit and perform transient simulations of single and two stage RF RP circuits. The single

and two stage RP circuits based on diamond Schottky diodes show excellent power limitation to a constant level of 24 dBm or 0.25 W for any input power beyond 33 dBm or 2 W. The self-heating in the diamond diodes under CW operation was also simulated and a mere ~2 K increase in temperature was observed after 100 cycles at 1 GHz, thus corroborating the high-power handling capacity of diamond diodes.

Through Silvaco ATLAS simulations, we also observed that in a diamond SPINDs, the Schottky cathode contact to the *n*-layer becomes reversed biased at increasing forward bias. This causes a reduction in the electron injection from the cathode and eventually a hole minority current dominated diode. Therefore, in order to achieve full bipolar conduction, the SBH at the n-layer contact needs to be reduced. This electron SBH is observed to reduce at increasing temperatures and a bipolar diode current is observed practically through increased light emission from the diamond diodes. High temperature reverse bias conduction was also modeled through hopping and Poole-Frenkel Emission current models. An excellent fit to the experimental data was achieved and an average of $\sim 1.2 \times 10^5/\text{cm}^3$ threading dislocation density was extracted.

6.2 Future Work

One of the prime limitations in experimental diamond devices in the present stage are contacts to the *n*-type diamond. Due to interface states and Fermi pinning, an electron SBH is formed along with increased contact resistance. Therefore, bipolar conduction is difficult at room temperature, limiting the diamond diodes to unipolar Schottky diodes.

Contacts to the n-layer can be improved through nano-carbon [6.1] or graphite [6.2] formation below the contact metal.

Another major limiting factor in the present state of diamond technology is the presence of defects and trap levels that severely limit the diamond device performance. Although reducing defect density through improved growth is a longer and more difficult albeit necessary task, improvements in diamond etching is comparatively easier. The present diamond etching process through O_2 RIE is more of a physical etching process (compared to a chemical etching process), which may introduce significant damage related defects on the sidewalls. These defects can be responsible to increased leakage currents, suppression of forward current and lower breakdown. Improvement in diamond etching may be done through novel etching processes such anisotropic wet etching through thermochemical reaction between Ni and diamond in high-temperature water vapor [6.3].

Through the RF application research in Chapter 4, it can be seen from the simulations that even with the present stage of diamond growth and fabrication, anti-parallel Schottky barrier diamond diodes will be able to handle large RF power through them without being damaged. A selective area growth can be done to grow standalone *p-i-n* diodes and on-chip single-stage or multi-stage RP circuits can be built. It was also shown through the power-frequency spectrum analysis, that the RF power can be distributed throughout multiples of the main frequency. Therefore, diamond diodes can also be used for high power - high frequency multipliers and mixers.

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