Advanced Control of Distributed Energy Resource (DER) Inverters and Electric Vehicle (EV) Traction Drives

by

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ABSTRACT

Voltage Source Converters (VSCs) have been widely used in grid-connected applications with Distributed Energy Resource (DER) and Electric Vehicle (EV) applications. Replacement of traditional thyristors with Silicon/Silicon-Carbide based active switches provides full control capability to the converters and allows bidirectional power flow between the source and active loads. In this study, advanced control strategies for DER inverters and EV traction inverters will be explored.

Chapter 1 gives a brief introduction to State-of-the-Art of VSC control strategies and summarizes the existing challenges in different applications. Chapter 2 presents multiple advanced control strategies of grid-connected DER inverters. Various grid support functions have been implemented in simulations and hardware experiments under both normal and abnormal operating conditions. Chapter 3 proposes an automated design and optimization process of a robust H-infinity controller to address the stability issue of grid-connected inverters caused by grid impedance variation. The principle of the controller synthesis is to select appropriate weighting functions to shape the systems closed-loop transfer function and to achieve robust stability and robust performance. An optimal controller will be selected by using a 2-Dimensional Pareto Front. Chapter 4 proposes a high-performance 4-layer communication architecture to facilitate the control of a large distribution network with high Photovoltaic (PV) penetration. Multiple strategies have been implemented to address the challenges of coordination between communication and system control and between different communication protocols, which leads to a boost in the communication efficiency and makes the architecture highly scalable, adaptive, and robust. Chapter 5 presents the control strategies of a traditional Modular Multilevel Converter (MMC) and a novel Modular Isolated Multilevel Converter (MIMC) in grid-connected and variable

speed drive applications. The proposed MIMC is able to achieve great size reduction for the submodule capacitors since the fundamental and double-line frequency voltage ripple has been cancelled. Chapter 6 shows a detailed hardware and controller design for a 48 V Belt-driven Starter Generator (BSG) inverter using automotive gate driver ICs and microcontroller. The inverter prototype has reached a power density of 333 W/inch^3, up to 200 A phase current and 600 Hz output frequency.

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Chapter 1

INTRODUCTION

1.1 Background

Voltage Source Converters (VSCs) have drawn much attention in modern power system due to the rising demand of renewable energy applications such as Photovoltaic (PV) and off-shore wind farms [1]. The use of VSCs makes it possible to provide electric energy to the 60 Hz power grid from these intermittent energy sources. However, the problem of system stability and controllability arises when more and more VSCs are connected to the main grid. Fast changes in the power output of the renewable energy sources due to their intermittency have placed challenges on system stability. The power quality in terms of current Total Harmonic Distortion (THD) should be maintained due to the Pulse Width Modulation (PWM) in the VSCs. Especially in recent years, traditional Si-based Insulated Gate Bipolar Transistors (IGBTs) have been replaced by high-speed Si or SiC Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs). High-frequency harmonics must be suppressed due to higher PWM frequency. Grid-connected VSCs should be able to achieve stable operation regardless of the type of feeder to which it connects and the location of inverter interconnection. Traditional Proportional-Integral (PI) and Proportional-Resonant (PR) controllers have limited stability margin under a large variation of the grid impedance. A robust controller should be implemented by taking the grid impedance uncertainty into consideration. IEEE 1547 Standard sets certain requirements for grid-connected converters even under abnormal conditions. When unintentional islanding happens, grid-connected converters should be able to detect it and cease to energize the system.

The challenge of this task is to detect islanding in the Non-Detection Zone (NDZ) where the power provided by the converter exactly matches the power absorbed by the load. In this case, the inverter will not experience any voltage and current change at output terminals, which is hard to tell whether the main grid is still present or not. Another function of grid-connected converters is Low-Voltage Ride-Through (LVRT) where the converters should be able to continue operating when one phase or three phases of the grid voltage becomes low. For inverters which are connected in close proximity under standalone condition, it is necessary to apply droop control strategies to ensure power sharing. However, it will cause the voltage and frequency to drift from their rated values.

Multi-layer communication is essential to control a large number of grid-connected converters in a distribution system. The communication architecture development in such a system faces two major challenges. The first challenge is the coordination between communication and system control. The reason can be explained in the following three aspects. Firstly, if the control and the communication programs are both carried out in the Enhanced Pulse Width Modulator (ePWM) interrupt inside the Digital Signal Processor (DSP), the total time consumption of both programs should be less than the switching period otherwise the PWM output will be affected. In this case, the communication interacts with the control algorithm. For instance, if most of the switching period is assigned to the control program, the amount of data that can be exchanged is greatly limited. If the communication takes up too much time, and the control algorithm cannot be completed within the remaining time, the DER normal operation will be affected. Secondly, in a multi-layer architecture, communication between different layers should take place at different frequencies based on the specific control tasks. For example, if the control task happens once every second in the upper supervisory layer, it is inappropriate to conduct the associated

communication every switching cycle. Thirdly, the communication error also affects the control performance. For example, abnormal communication caused by hardware interference may generate incorrect monitoring data and commands, which poses a threat to the system normal operation. The second challenge is the coordination of communication between different layers. The reason is explained in the following two aspects. Firstly, communication between different layers should be independent with each other especially when there is communication being carried out inside the ePWM interrupt. The communication outside of the interrupt should not interfere with the one inside. Otherwise, the DER inverter operation will be influenced. Secondly, the relationship between the amount of data transmitted and the time consumed is different for different communication protocols. For example, the time consumption for Serial Peripheral Interface (SPI) communication is proportional to the number of words exchanged. However, in Modbus communication, the time consumption for transmitting one register and 120 registers is almost the same. This requires coordination between these two protocols in order to improve communication efficiency.

Modular Multilevel Converters (MMCs) are a special type of VSCs. They have been widely used in High Voltage Direct Current (HVDC) and medium voltage drive applications. Compared with a traditional two-level converter, MMC shows advantages in the following aspects. Firstly, the size of the passive filter at converter output could be reduced considerably due to multi-level output voltage and lower harmonic component. Secondly, in HVDC applications, the voltage stress of the active switch is greatly reduced since each device only takes VDC/N where VDC is the entire DC bus and N is the number of modules used in each arm of the converter. In addition, the system reliability is also improved due to the modular topology. However, modular topologies also inherent some drawbacks. First, the value and the size of the DC link capacitor in each submodule is hard to reduce due to the inherent fundamental and

2nd order circulating current in each module. The capacitor must be large enough to keep the voltage ripple under a certain limit. Secondly, in a Variable Speed Drive (VSD) application, since the voltage ripple is inversely proportional to the fundamental frequency of the output voltage and current, it is difficult for a conventional MMC to start from zero frequency without additional control.

VSCs are also widely used in Electric Vehicle (EV)/Hybrid Electric Vehicle (HEV). For a 48 V Belt-Driven Starter Generator system, a three-phase inverter is an essential component to drive the Interior Permanent Magnetic Synchronous Machine (IPMSM). The power supply is 48 V DC. The peak power can go up to 12 kW and lasts for several seconds. The peak output current can be up to 300 A. More than 550 W power loss will be generated. The challenge on the hardware design is to get 3 key performance which are well-balanced current in paralleled MOSFETs, low drain-source voltage spike at switching-off, and small thermal resistance of the heatsink system. With respect to the control algorithm, it should be able to achieve stable and robust field-weakening operation of the machine by carefully controlling the stator winding currents. Otherwise, the inverter may experience over modulation or even fall into instability.

1.2 Research Overview

This dissertation is aimed at providing effective and advanced solutions to address the aforementioned challenges of VSCs. For grid-connected DER inverters, PV cells, batteries, and supercapacitors are firstly modeled in PLECS. A novel control strategy has been proposed to smooth the intermittent PV output power by separating the current reference into low and high frequency components for respective energy storage devices. Various grid support functions have been integrated and implemented based on the requirements of IEEE Standard 1547. A unified P control for the

DC/DC stage has been implemented for both grid-connected and standalone operations. For the DC/AC stage, a repetitive controller has been implemented in addition to the traditional Proportional-Resonant (PR) controller in order to eliminate harmonic current caused by deadtime in the gate driving signals of the active switches and the harmonic voltages in the grid. A robust H-infinity controller is proposed to replace the traditional PR controller to maintain a stable operation of the PV inverter under different grid impedance values. The synthesized controller is able to achieve the robust stability and robust performance simultaneously. A 2-D Pareto Front optimization process has been implemented to find an optimal controller in terms of stability margin and steady-state error/3^{rd} order harmonic suppression capability. For three-phase DER inverters, a Second-Order-Generalized-Integrator (SOGI) based Sequence Separation Method (SSM) is used to decompose the unbalanced voltage and current into positive sequence, negative sequence, and zero sequence. A Low-Voltage-Ride-Through (LVRT) control strategy based on SOGI-SSM has been implemented to independently control different sequences in the grid current. A novel active islanding detection method based on SOGI and harmonic injection has been proposed for both single-phase and three-phase inverters in order to prevent unintentional islanding per IEEE 1547 requirements. Finally, if multiple paralleled inverters are operating in standalone mode, power sharing is achieved using traditional droop control. In order to prevent drift of the grid voltage and frequency, a supervisory control has been implemented to modify the staring points of the per-unit droop curves so that the voltage and frequency can be brought back to their rated values. Simulation and hardware verification are provided.

A high-performance 4-layer communication architecture to facilitate the control of a large number of PV inverters in a distribution grid through a centralized cloud platform has been proposed. This multi-layer architecture consists of multiple DER

inverters with PV and battery channels capable of advanced grid supportive and grid forming functions in the Process layer, Raspberry Pi computers in the Interface layer, several customized Edge Intelligent Device (EID) in the Substation layer, and an end-to-end solar energy optimization platform (e-SEOP) in the Supervisory layer. The Raspberry Pi serves as a communication interface that communicates with the DER inverter using Serial Peripheral Interface (SPI) communication and talks to the EID using Modbus TCP/IP protocol. In this work, a convenient and comprehensive solution to SPI and Modbus TCP/IP communication implementation in a distribution grid will be firstly provided. Multiple strategies have been implemented to address the challenges of coordination between communication and system control and between different communication protocols, which leads to a boost in the communication efficiency and makes the architecture highly scalable, adaptive, and robust. The proposed communication architecture has been validated through hardware experiments using an actual 2 kVA DER inverter, a Raspberry Pi and an EID. The results indicate a reliable and efficient communication among different layers, which facilitates large-scale status monitoring of edge devices and coordinated control of the entire system.

Control strategies of a conventional Modular Multilevel Converters (MMCs) is firstly introduced. The control consists of three outer energy loops and four inner current loops. An equation based switching mode MMC simulation has been performed in PLECS in order to speed up simulation process when the number of modules becomes large. An MMC based medium voltage Variable Speed Drive (VSD) has been simulated using a pump-back system. In order to reduce the DC link capacitor size in each submodule, a new topology named Modular Isolated Multilevel Inverter (MIMC) has been proposed. The fundamental and double-line frequency current ripple in each submodule has been eliminated by connecting three submodules on the same

level from each phase through additional DC/DC converters. As a result, MIMC is perfect for zero frequency start-up in the medium voltage VSD applications and integrating energy storage devices into each SM. Compared with control strategies of an MMC, no circulating current control is needed since the phase energy and arm energy are naturally balanced. A MIMC based VSD simulation has been performed using the same pump-back topology.

VSCs also become essential components in a 48V Belt-driven Starter Generator (BSG) system for HEV applications which have gained more attention in recent years. A 48V BSG system is featured with high output current, high starting torque, and highly efficient thermal management. Hardware design considerations of a high power density three-phase BSG inverter have been elaborated to address the challenges of even current distribution among paralleled MOSFETs, small drain-source voltage spike and good thermal dissipation. In order to satisfy the high-current requirement, a careful selection of MOSFET device with high-current rating and low on-resistance has been presented. In order to suppress circulating current among paralleled devices, individual gate resistors and common-mode chokes have been placed in the gate loop of each MOSFET. In order to provide good thermal dissipation, an Insulated Metal Substrate (IMS) board and single-layer layout technique have been implemented. Multiple low-profile electrolytic capacitors are used to increase the power density of the prototype. Moreover, the use of automotive gate driver IC TLE9180 and micro-controller TC1782 makes the prototype more readily accepted by industry. An improved Interior Permanent Magnet Synchronous Machine (IPMSM) control strategy and a pump-back system have been implemented in the designed inverter to facilitate the validation of the prototype under rated condition without using a real machine. The control algorithm automatically adjusts the onset of field-weakening by using an additional inverter voltage loop and takes into account the nonlinearity of

the stator flux linkage by using curve fitting technique, which makes the motor drive adaptive to machine parameter changes as well as DC bus voltage fluctuation. A 12 kW three-phase BSG inverter prototype has been built and tested. The prototype power density has reached 333 W/inch^3. Both PLECS simulations and hardware experiments show a continuous and stable operation with up to 200 A peak phase current and up to 600 Hz output frequency.

1.3 Dissertation Outline

Chapter 2 focuses on the control strategies of grid-connected DER inverters with energy storage (supercapacitors and batteries). An automated robust H-infinity controller design using Pareto Front optimization for a single-phase grid-connected inverter is presented in Chapter 3. Chapter 4 introduces a high-performance multi-layer communication architecture using SPI and Modbus TCP/IP protocols. Chapter 5 shows the control strategy of a conventional MMC and proposes a novel MIMC to overcome the drawbacks of MMCs. Chapter 6 presents a detailed hardware design of a high current high power density 48 V BSG inverter and a robust IPM control strategy to achieve automatic field-weakening operation.

Chapter 2

CONTROL OF GRID-CONNECTED DER INVERTERS WITH ENERGY STORAGE

2.1 Introduction

Literature [2] shows that consumption of fossil fuels becomes the most significant cause of air pollution in the United States and they account for 66.9% of electricity generation. Greenhouse gases produced from fossil fuel combustion are the primary issue concerning global warming, which urges the government to further cut the emissions and improve energy efficiency [3]. One popular solution that is gaining more and more attention is to integrate renewables as DERs into the traditional power grid in order to meet the emission-reduction targets [4–6]. Unlike traditional large synchronous generators which produce 60 Hz three-phase AC voltages and currents, most currently available renewable energy resources such as Photovoltaic (PV) panels and fuel cells only generate DC output voltage and current. In this case, VSCs provide an interface to convert energy from DC to AC quantities with some control strategies. In addition, due to the intermittency of renewable supply, big fluctuation in the bus voltage magnitude and frequency becomes a major problem as the penetration rate of renewable energy increases. Therefore, the power grid puts additional requirements to VSCs which connect DERs to the main system to guarantee the power quality [7]. As a result, additional control methods must be applied to VSCs. In terms of renewable power supply, energy storage devices are considered a promising approach to improve the balancing of power demand and supply in the grid with increasing penetration of renewables [8, 9]. Energy storage devices are required to compensate for the power

difference between the source and the load. However, characteristics of different type of energy storage devices must be taken into consideration for compensating power in order to avoid sacrificing their lifetime. In terms of interfacing with grid using VSCs, each power electronic converter is required to comply with IEEE 1547 standard for interconnection and interoperability of DERs with associated electric power systems interfaces [10]. A brief summary of IEEE 1547 standard for grid-connected converters under both normal and abnormal operations are shown in Table 2.1. In terms of power quality, IEEE 1547 also sets different limits for both even and odd harmonic currents as shown in Table 2.2 where h represents the harmonic order and I_{rated} represents the rated current. As a result, output current of the converters should be well regulated as well. Another important topic of grid-connected VSCs is Anti-Islanding Detection (AID). Islanding refers to a situation where DERs continue to power partial local load with the absence of the main grid. Unintentional islanding can be dangerous to utility workers and other electric components that are no longer controllable by the main utility. In addition, islanding may cause power line asynchronization with respect to the grid. Large inrush current can occur when reclosing under such circumstance [11]. As a results, IEEE 1547 requires the inverter to step energizing the grid and to trip within 2 seconds. Droop control provides the VSCs with virtual inertial to improve system stability under load step changes in standalone operation. Even power sharing can only be achieved if the output characteristics of the paralleled DER inverters are controlled to follow the same per-unit droop curve and the grid impedance is inversely proportional to the inverter rating, which is not common. In addition, traditional droop control will make the system voltage and frequency of the system deviate from rated values if the load step change is large.

In this chapter, modeling of PV, supercapacitor, and battery will be discussed in Section 2.2. A novel strategy to compensate power difference between the source

Table 2.1: IEEE 1547 Standard For High Penetration Category Grid-connected Converters

Normal Operations		**Abnormal Operations**	
Operation Modes	Requirements	Abnormal Conditions	Requirements
Mode 1: Constant Power Factor Mode	To follow a constant power factor command with limited reactive power injected or obsorbed	Mode 1: Voltage Ride-Through	To remain connected under both low and high voltage ride-through and to follow specific real and reactive power commands [12]
Mode 2: Voltage-Reactive Power (Volt-Var) Mode	To change the reactive power command based on the grid voltage feedback		
Mode 3: Constant Reactive Power Mode	To follow a constant reactive power command with limitation	Mode 2: Frequency Ride-Through	To remain connected under both low and high-frequency ride-through and to change the active power command according to frequency (Frequency-Droop operation)
Mode 4: Active Power-Reactive Power (Watt-Var) Mode	To change the reactive power command according to the active power feedback		
Mode 5: Voltage-Active Power Mode	To change the active power command based on the grid voltage feedback		

and load using energy storage devices by decomposing the current reference into low- and high-frequency components is also proposed in this section. The rest of this

Table 2.2: IEEE 1547 Requirements For Harmonic Current Injected By Grid-connected Converters

Even harmonic current limit	**Odd harmonic current limit**
If $h = 2$, $I_h < 1\%$ of I_{rated}	If $h \leq 11$, $I_h < 4\%$ of I_{rated}
If $h = 4$, $I_h < 2\%$ of I_{rated}	If $11 \leq h \leq 17$, $I_h < 2\%$ of I_{rated}
If $h = 6$, $I_h < 3\%$ of I_{rated}	If $17 \leq h \leq 23$, $I_h < 1.5\%$ of I_{rated}
If $8 \leq h \leq 50$, same limit as odd harmonic current	If $23 \leq h \leq 35$, $I_h < 0.6\%$ of I_{rated}
	If $35 \leq h \leq 50$, $I_h < 0.3\%$ of I_{rated}
Total current distortion $< 5\%$	

chapter focuses on multiple grid support functions provided by the DER inverter per IEEE 1547 requirements. In Section 2.3, a novel P control has been implemented for the DC/DC stage of the DER inverter so that the DC bus voltage is controlled by the DC/AC stage regardless of grid-connected or standalone operation. For the DC/AC stage, a repetitive controller has been implemented for lower current THD. Analysis of each controller parameter and a highly efficient digital implementation of the repetitive controller have been provided. The controller has been verified through PLECS simulation and hardware experiments. A novel Second-Order-Generalized-Integrator (SOGI) based active anti-islanding detection method has been proposed in Section 2.4. This approach is able to easily extract the harmonic voltage at Point of Common Coupling (PCC) without using Fast Fourier Transform (FFT) which saves resources of the digital controller. The proposed technique has been verified using PLECS simulation and Hardware-In-Loop (HIL) simulation. Section 2.5 uses a SOGI based Sequence Separation Method (SSM) to separate positive and negative sequence components of the grid voltage and current. The DER inverter is able to independently control each current component to ride through the low voltage

abnormal condition under unbalanced three-phase grid voltage. Section 2.6 talks about the control strategies for paralleled inverters in standalone operation. In order to achieve power sharing, each inverter has been controlled such that the output voltage and frequency follow the same per-unit droop curve. Supervisory control has been added on top of the droop control so that the grid voltage and frequency will be brought back to rated values. Simulation results have been provided in this section as well. Conclusions and future work are provided in Section 5.5.

2.2 Modeling and Control of DERs

2.2.1 Modeling of PV

Solar energy, which is one of the most commonly accessible renewable energy, has been considerably studied and deployed in the current energy industry. The output voltage and current of a PV panel are DC, which requires an inverter to connect PV panels to an AC bus. Also, the DC output voltage is relatively low, and the number of PV panels connected in series is limited. One solution is to use a DC/DC, either isolated or non-isolated, boost converter to generate a high voltage DC link for the inverter. A typical three-phase PV inverter is shown in Fig. 2.1. The output I-V characteristic of TSM-245 PA05.08 is provided in Fig. 2.2 [13]. The detailed PV model is shown in 2.3 and can be found in PLECS demo simulation. The model consists of two controlled current sources where I_{ph} represents the photon current generated by sunlight, and I_d is diode current which can be described by the following equation,

$$I_d = I_o(e^{\frac{qV_d}{akT}} - 1) \tag{2.1}$$

In (2.1), I_o is the reverse saturation current of the diode at temperature T. q is the charges of an electron. V_d is the voltage across the diode (in this case, the voltage

across the controlled current source). a is ideality factor and is a measure of the material quality. Series resistance R_s models the combined resistances of contacts, metal grids, and p and n layers while shunt resistance R_{sh} models the leakage current of p-n junction [14]. All these parameters can be derived from the I-V curves shown in Fig. 2.2 and the product datasheet by the method introduced in the literature [14].

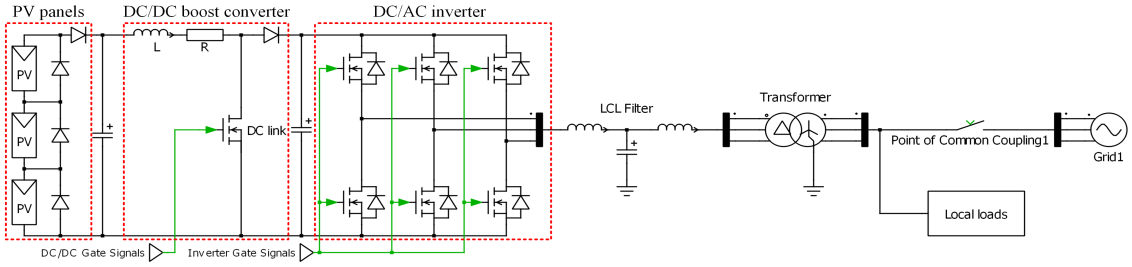


Figure 2.1: A Typical Three-phase PV Inverter Topology

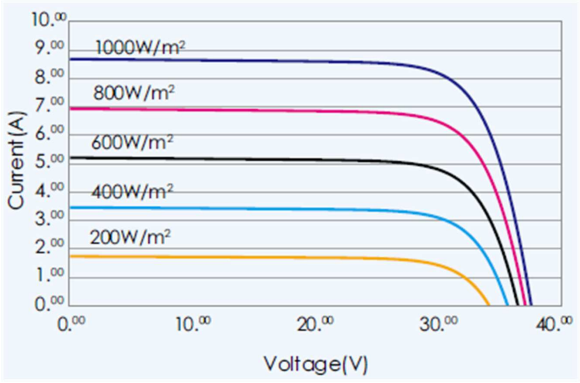


Figure 2.2: Output I-V Characteristic Of TSM-245 PA05.08

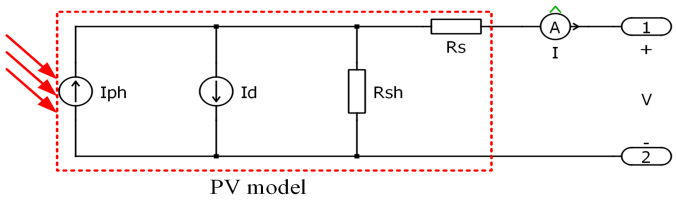


Figure 2.3: The Simulation Model Of A PV Panel

2.2.2 Modeling of Supercapacitors and Batteries

Two types of energy storage devices, supercapacitors and batteries, will be discussed in this section. These energy storage devices are connected to an inverter through a DC/DC boost converter to create a high voltage DC link because of the low voltage rating of each supercapacitor and battery cell. A typical DER inverter with energy storage is shown in Fig. 2.4 where a common DC bus is shared among the DER and energy storage devices. Supercapacitors have high power densities and possess a long life cycle with fast response for charging or discharging [15, 16]. As a result, supercapacitors can only take high-frequency current component. The model which is to be used in the simulations is called frequency-dependent model provided by PLECS. It is a three-stage RC network, and the parameters are based on experimental measurements. The model itself and its resistance characteristic concerning operating frequency are shown in Fig. 2.5(a) and 2.5(b) [17], respectively.

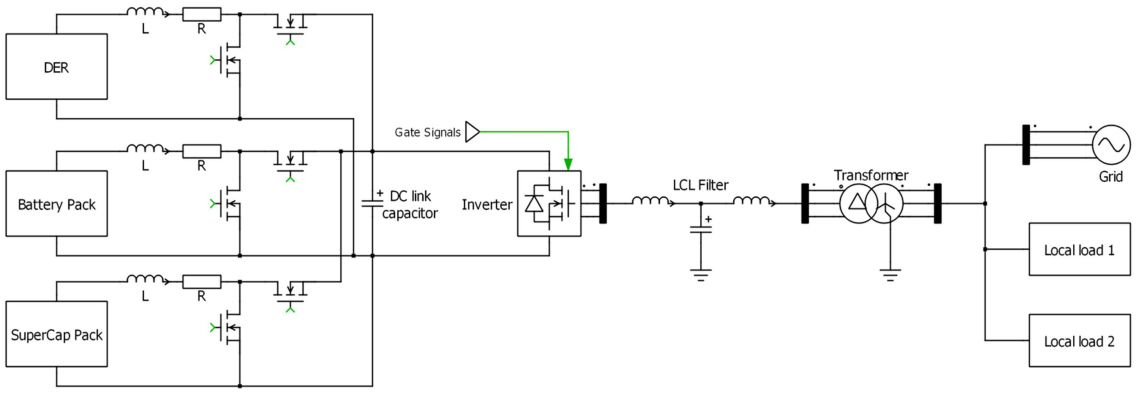
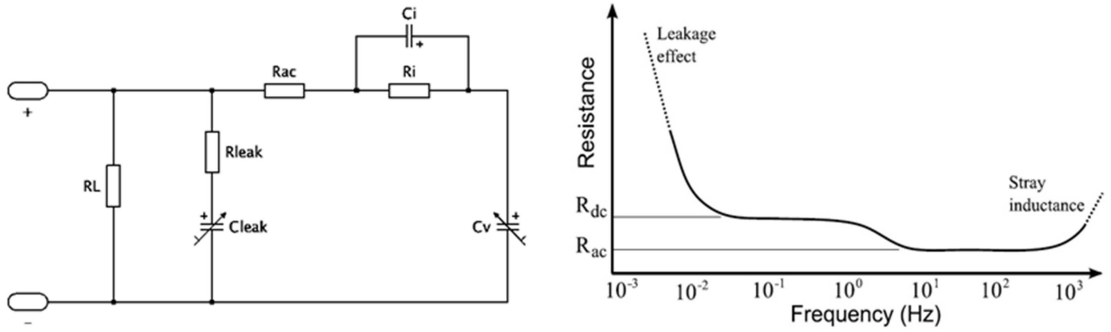


Figure 2.4: A Typical DER Inverter With Energy Storage

Unlike supercapacitors, batteries have high energy densities and are able to provide necessary energy in the long term. Hence, they can only take low-frequency current components [18]. The model of the batteries is also from PLECS and is based on look-up tables. The data comes from CGR18650CG 3.6V 2250mAh Panasonic cell



(a) (b)

Figure 2.5: (a)Supercapacitor Model From PLECS; (b)Supercapacitor Resistance Characteristic With Respect To Operating Frequency

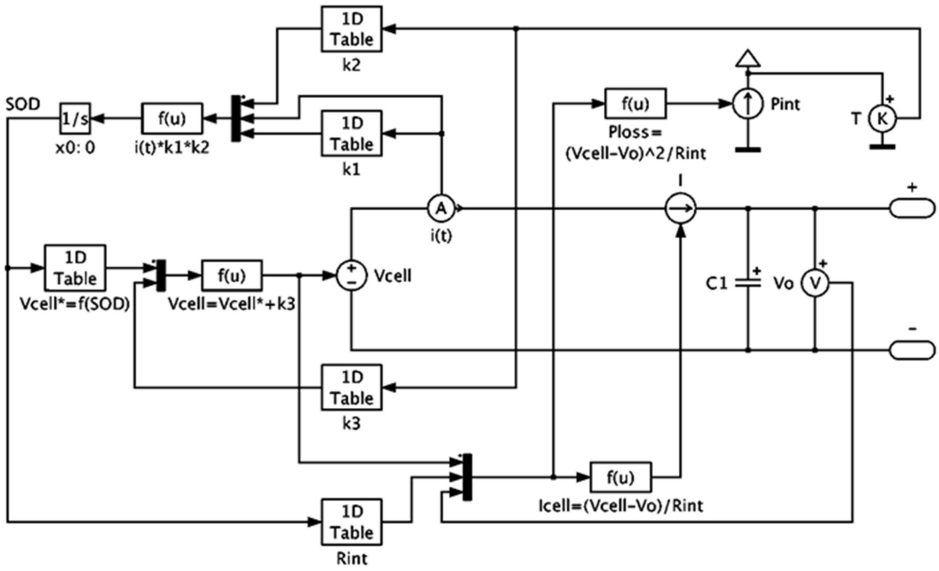


Figure 2.6: Look-up Table Based Battery Model From PLECS

[19]. The detailed model of a battery cell is shown in Fig. 2.6.

2.2.3 Power Compensation Using Energy Storage

Energy storage can be used to smooth the intermittent PV output power caused by solar radiation or ambient temperature. Especially in a standalone operation mode where there is power unbalance between the source and the load, the supercapacitors and batteries should be controlled to compensate the power difference. In a

standalone scenario, the DC link voltage is controlled by DC/DC stage instead of DC/AC inverter. The control diagram is shown in Fig. 2.7 where the DER connected DC/DC boost converter has been omitted. The PV is assumed to operate under Maximum Power Point Tracking (MPPT). From the control diagram, the output of the DC link voltage regulator is the sum of the battery and supercapacitor current references. The sum of the two current references represents the power that is required to be compensated by energy storage devices. In order to separate the high- and low-frequency components, a low-pass filter is used to get low-frequency current reference for batteries and high-frequency current reference for supercapacitors. Feedforward is implemented for each PI regulator to help them reach steady state much faster.

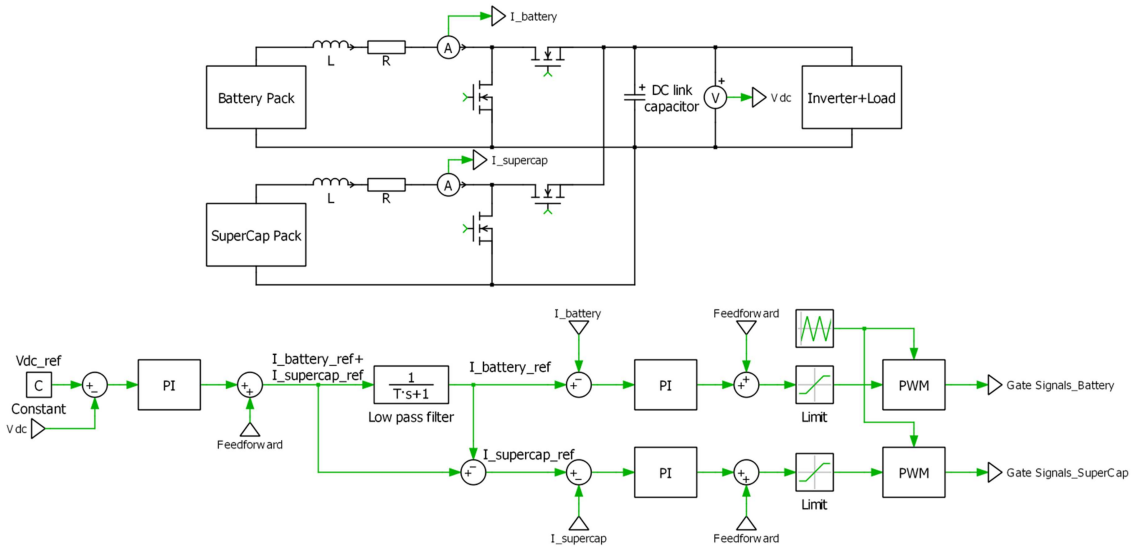


Figure 2.7: Control Diagram Of Energy Storage Connected DC/DC Boost Converter In Standalone Mode

PLECS simulation verification has been performed. In the simulation, the PV output power is intentionally changed while the load remains constant in order to create power difference between the load and source. The energy storage devices will be able to provide or absorb extra power to stabilize the system. Fig. 2.8 shows the

PV output power variation by changing the radiation intensity in the PV modules. Fig. 2.9 shows the DC link current for the energy storage devices and current reference for supercapacitors (green line) and batteries (red line). It is obvious that the DC link current is different at different time intervals since the amount of power that needs to be compensated is different. The current direction of the energy storage devices can be either positive and negative since they are able to provide and absorb extra power. The simulation results show that the current reference has been decomposed to high- and low- frequency components. The supercapacitors and batteries will only respond to high-frequency and low-frequency current command, respectively.

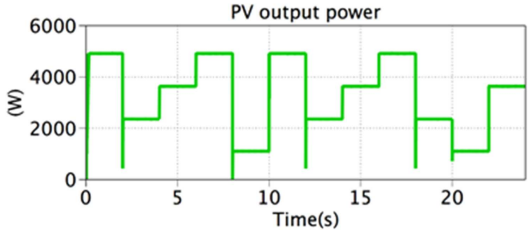


Figure 2.8: Simulation Results Of PV Output Power

2.3 Normal Operation

From Table 2.1 in Section 6.1, only reactive power command is given in some cases (Mode 1 to 4 under normal operation) while others require certain real power as well. For PV applications, MPPT should be implemented when active power is not specified. However, PV should not operate at MPPT if the inverters are required to generate certain amount of active power assigned by system operators. This is also the case when PV inverters are in standalone operation. Traditionally, the control strategies for PV inverters need to change from one to another as shown in Fig. 2.10. In this scenario, only battery is considered as the energy storage. In case of not having an active power command, the PV inverters implement MPPT for the

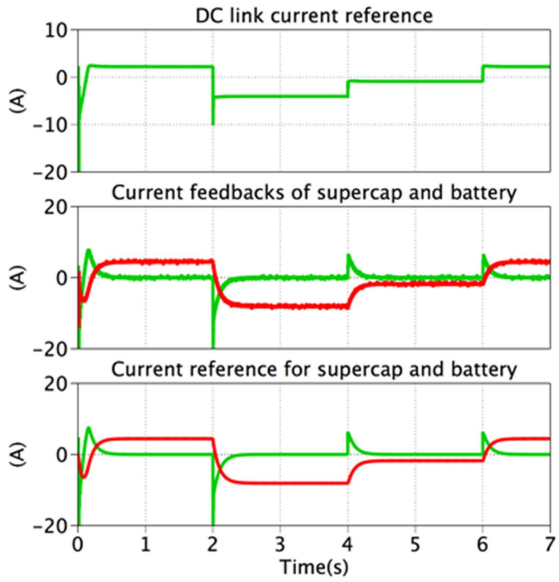


Figure 2.9: Simulation Results Of DC Link Current For Energy Storage Devices, Current References And Feedbacks For Supercapacitors (Green Line) And Batteries (Red Line)

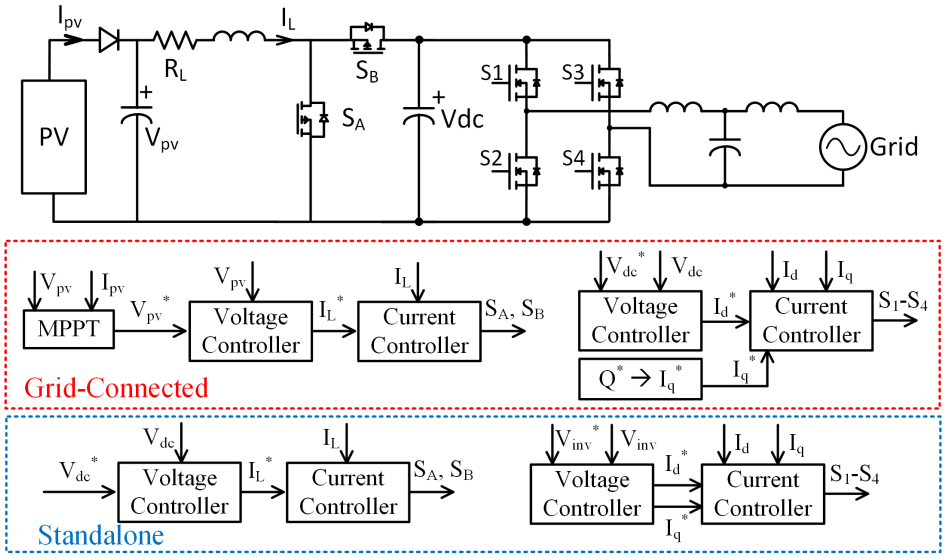


Figure 2.10: Traditional Control Strategy Of A Single-phase PV Inverter

DC/DC stage and decoupled current control for the inverter stage. When active power command is specified either by system operators or load conditions in standalone system, the DC/DC converter controls DC bus voltage and inverter controls output

voltage. Obviously, control object changes for DC/DC stage PI regulators under different operating conditions and PI parameters need to be tuned accordingly. The proposed advanced DER control is a unified control strategy for PV inverters even with energy storage system under all cases. For the DC/DC stage, P control is proposed where a double loop structure consisting of an outer PV voltage loop and an inner inductor current loop is implemented. The inverter is under current control under both grid-connected and standalone conditions. P Control is also flexible for energy storage control implementation. Take battery systems as an example, direct battery current control is used under both grid-connected and standalone situations.

2.3.1 A Novel P Control for the DC/DC Stage

The proposed control scheme for a single-phase PV inverter with battery system under grid-connected and standalone operations are illustrated in Fig. 2.11 and 2.12, respectively. P^* and Q^* are real and reactive power commands, respectively. All variables with * represent the reference or command. Variables without * represent the actual feedback. As can be seen from the two figures, P control is universal for the DC/DC stage under both operating conditions. For the inverter stage, direct grid current control is implemented in grid-connected mode with current reference coming from IEEE 1547 for different mode. As for standalone operation, only an extra outer capacitor voltage loop is added, and gird current control becomes an inner loop. Under this proposed universal control, the DC/DC stage PI parameters are not required to change during transition from one to another operating condition. Detailed control strategies are discussed in the following subsections.

P control literally means that real power command is used to control the whole DC/DC stage. In this study, Perturb and Observe (P&O) has been chosen to perform MPPT for PV cells. Traditional P&O only looks for the point where derivative of PV

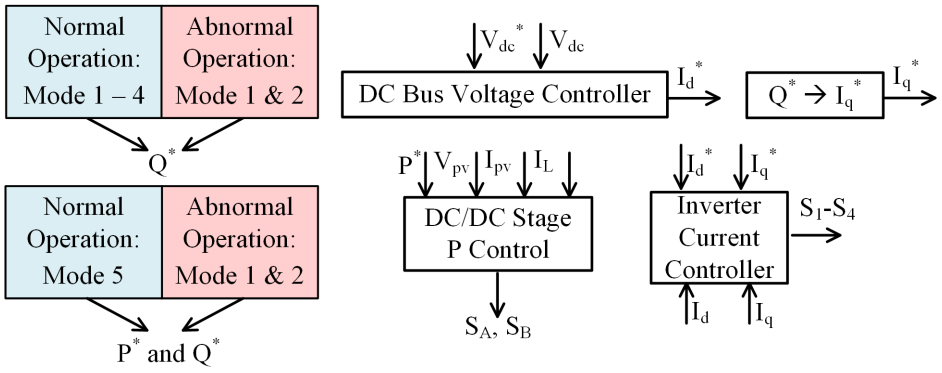


Figure 2.11: Proposed Unified DER Control Under Grid-connected Operation

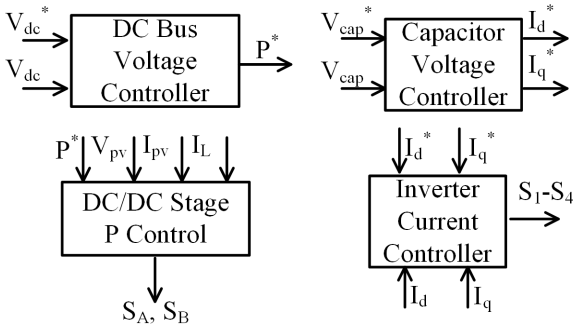


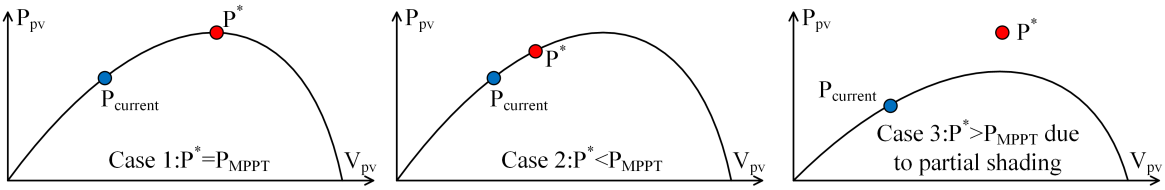
Figure 2.12: Proposed Unified DER Control Under Standalone Operation

output power with respect to its terminal voltage equals 0 as the maximum power point. However, P&O has been modified as shown in Fig. 2.13 to find a point producing either maximum power or power equal to the command. In the figure, the power error ΔP is calculated using the following equation.

$$\Delta P = P^* - P_{current} \tag{2.2}$$

$$\frac{dP_{PV}}{dV_{PV}} = \frac{P_{current} - P_{previous}}{V_{current} - V_{previous}} \tag{2.3}$$

In (2.2), $P_{current}$ is the measured PV output power at current instant (switching cycle). $P_{previous}$ in (2.3) represents the measured PV power at the previous switching



Scenarios	$\Delta P > 0$, $dP_{pv}/dV_{pv} > 0$	$\Delta P < 0$, $dP_{pv}/dV_{pv} > 0$	$\Delta P > 0$, $dP_{pv}/dV_{pv} < 0$	$\Delta P < 0$, $dP_{pv}/dV_{pv} < 0$
PV Voltage Change	Increase V_{pv}	Decrease V_{pv}	Decrease V_{pv}	Increase V_{pv}

Figure 2.13: Proposed P Control With Modified P&O Method

cycle. The advantage of this method is highlighted when partial shading happens and the power command is greater than PV maximum available output power. The maximum power point on P-V curve can be automatically achieved since P&O will find the point with dP_{PV}/dV_{PV} equal to 0 automatically even when ΔP is positive. The power difference can be compensated by the battery system. As Mode 1 through 4 in normal operation will not specify a P command, a P reference with maximum allowable real power which is determined by inverter rating will be sent to PV. However, under Mode 5 in normal operation and Mode 1 & 2 in abnormal operation, P reference is equal to the command required by IEEE 1547. Therefore, PV will try to provide the required power as much as possible. The energy storage will be controlled by the power difference between the power command and actual PV output power. The DC/DC boost converter which is connected to PV uses a double-loop control strategy with an outer PV voltage loop and an inner boost inductor current loop. For battery connected boost converter, direct inductor current control is performed. The control diagram is shown in Fig. 2.14. In the standalone operation, P command comes from DC bus voltage control so that the unified control strategy for the D-C/DC stage can be realized and all PI parameters for the DC/DC boost converters can be kept unchanged between different operation modes. If the power command is negative which means the DER is required to absorb energy from the grid, only

battery will work since PV does not have energy absorption capability.

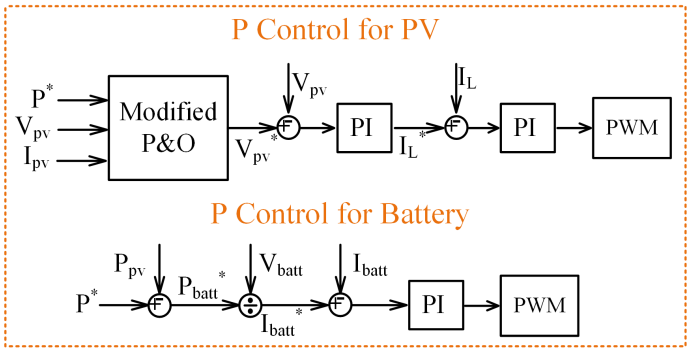


Figure 2.14: Detailed P Control Diagram For The DC/DC Stage

2.3.2 Current THD Improvement Using a Repetitive Controller for the DC/AC Stage

The control target of the inverter is the grid side current I_g. In grid-connected mode including both normal and abnormal conditions, d-axis current reference comes from DC bus voltage control, and q-axis current reference is generated from the reactive power command Q^*. However, in standalone operation, the inverter is required to control its output voltage. An extra outer voltage loop will be added. [20] shows that the system damping effect is improved if capacitor current is chosen as the inner loop control target. Therefore, the capacitor current reference will be generated by the voltage controller. In order to keep the gains of the PI controller the same as those in grid-connected mode, a grid side current reference has been reconstructed by subtracting capacitor current reference from inverter output current feedback. The control strategy is presented in Fig. 2.15. As a result, PI gains for the inner current controller do not change under different operating conditions.

As mentioned in Section 6.1, the power quality of the grid can be deteriorated because of more electronic sources and loads. Previous literatures analyzed and pro-

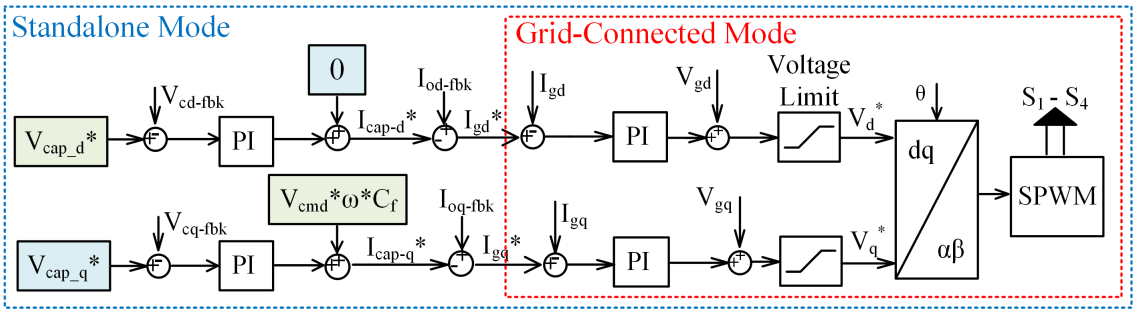


Figure 2.15: Detailed Inverter Current Control Under Both Grid-Connected And Standalone Operations

posed several approaches to mitigate the harmonic current brought by power electronic converters [21, 22]. However, many papers only focus on one reason that causes harmonic current. [23, 24] proposed different harmonic current controllers, among which repetitive controllers seemed promising due to its simple transfer function and easy digital implementation. [24] introduced a repetitive controller with added low-pass filter and phase-lead compensator for better stability performance. However, the analysis of each controller parameters was missing. This section provides a thorough analysis on the harmonic current generation in a single-phase inverter system.

(a) **Harmonic current analysis:** The mechanism of harmonic current generation in a single-phase voltage source grid-tied inverter is presented in this section.

(i) Harmonic current can be generated if the grid voltage is distorted possibly due to grid fault, sudden load change, etc. A little grid distortion will result in substantial harmonic current due to small grid impedance.

(ii) Common-mode/leakage current also contributes towards harmonics at inverter output due to the parasitic capacitance between the output of each half-bridge and the real ground. [25] used H-5 topology only to reduce the common-mode voltage.

(iii) Dead-time is widely implemented in power electronic converters to prevent shoot-through of the power electronic devices. The distorted inverter voltage caused by dead-time generates harmonic current which is influenced by the duration of the dead-time. Different open-loop dead-time compensation strategies have been proposed. [26] introduced a constant voltage compensation and [27] adopted a compensation voltage which is proportional to the inverter output current.

(iv) Different modulation methods, such as unipolar and bipolar modulation, and different carrier waveforms, such as triangular and sawtooth waveforms, will have an impact on the injected harmonic current.

(v) An LC or LCL filter is typically used at the inverter output to attenuate current ripples around switching frequency. Low-order harmonics are still retained. The corner frequency of the designed filter also affects current THD.

(vi) Also, there is a 1.5 switching cycle delay in digital control where, Delta-Sigma based ADC contribute 0.5 switching cycle delay and PWM control results in another 1.0 switching cycle delay. These delays in digital control also affect the injected harmonic current. Harmonic current cannot be eliminated merely by open-loop compensations. Additional closed-loop current controller is needed to actively regulate harmonic current.

(b) **Principles of a repetitive controller:** PR controller based harmonic current compensation has been widely used for single-phase inverters [23]. A PR controller with a center frequency of 60 Hz is used to control the fundamental component of the grid current to achieve required power output. Several PR controllers with center frequencies of 3^{rd}, 5^{th}, 7^{th}, 9^{th}, and 11^{th} order will be

paralleled to the fundamental PR controller to eliminate low-order harmonics. The corresponding control diagram is shown in Fig. 2.16. Even though the PR controller eliminates the input error at the center frequency, it will push the harmonics to higher order thus challenging system instability. Multiple PR controllers also take up much memory space in the DSP and will add more computational burden to the processor. The repetitive controller introduced in [24] is shown in Fig. 2.17, the fundamental component is still regulated by a PR controller while the harmonics will be taken care of by a single repetitive controller. k_{rc} is the proportional gain of the repetitive controller. $e^{-T_0 s}$ represents a fundamental cycle delay where T_0 equals to the fundamental cycle. $Q(s)$ is a low-pass filter, and $G_f(s)$ is a phase-lead compensator. $Q(s)$ and $G_f(s)$ are added to improve system stability.

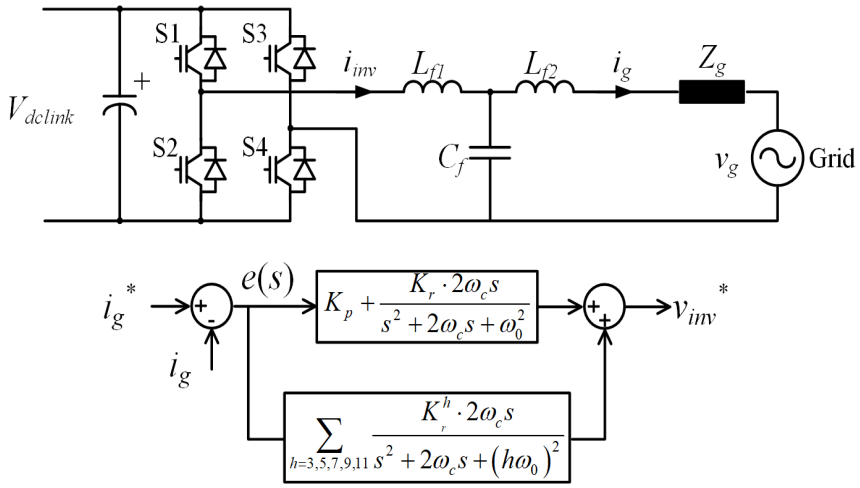


Figure 2.16: Schematic Of A Single-phase Inverter And Grid Current Control Strategy Using Multiple PR Controllers

(i) Tracking performance of the repetitive controller. Assume that k_{rc}, $Q(s)$ and $G_f(s)$ are all equal to 1, the closed-loop transfer function of the RC is

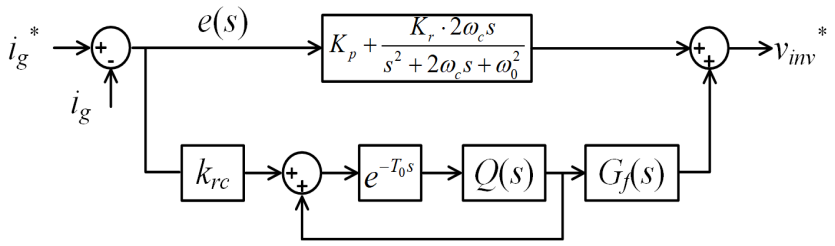


Figure 2.17: Grid Current Control Diagram Using A Fundamental PR Controller And A Repetitive Controller

expressed as

$$G_{rc} = \frac{e^{-T_0 s}}{1 - e^{-T_0 s}} \tag{2.4}$$

The corresponding bode plot is shown in Fig. 2.18. From the bode plot, we can see that the RC has a very high gain at each harmonic frequency, which leads to almost zero tracking error for all harmonics.

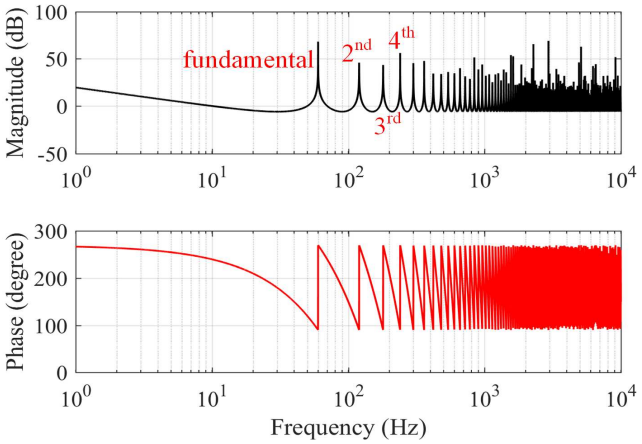


Figure 2.18: Bode Plot Of An Ideal Repetitive Controller With k_{rc}, $Q(s)$, And $G_f(s)$ Equal To 1

(ii) Stability improvement. The low-pass filter, $Q(s)$, is used to prevent the controller to respond to high-frequency harmonic errors. High-frequency harmonic current is already very small since most of them has been attenuated by inverter output filter. If the controller is not generating a proper

voltage that exactly compensates the high frequency harmonics, excessive harmonics might be induced, and adding RC might be counterproductive. However, the low-pass filter induces delay in the control loop which may deteriorate system stability. Therefore, a phase-lead compensator, $G_f(s)$, has been added. $G_f(s)$ has unity magnitude but an advanced phase angle. This compensator will not affect the magnitude of the original transfer function, but it will lift the system phase characteristic to provide more stability margin. Note that harmonic current at different frequencies has identical control gains so that the harmonics cannot be regulated separately.

(c) **Digital implementation of the repetitive controller:**

(i) Discretization of the transfer function. The discretization of the transfer function from s-domain to z-domain is shown in Fig. 2.19. z^{-N} shows the fundamental cycle delay where the integer N equals to T_0/T_s (T_s represents the sampling frequency). The low-pass filter is chosen in the z-domain as [28]

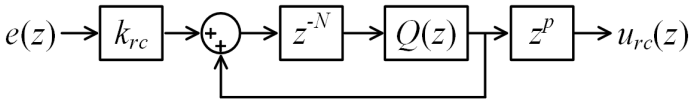


Figure 2.19: Control Diagram Of A Repetitive Controller In z-domain

$$Q(z) = \alpha_1 z + \alpha_0 + \alpha_1 z^{-1} \tag{2.5}$$

where $2\alpha_1 + \alpha_0 = 1$, $\alpha_0 > 0$, and $\alpha_1 > 0$. This is not a classical low-pass filter but with a phase-lead term to compensate the phase delay resulted by z^{-1}. z_p is the phase-lead compensator where p is an integer that represents

the phase-lead steps ($p \ll N$). The corresponding closed-loop transfer function is expressed as,

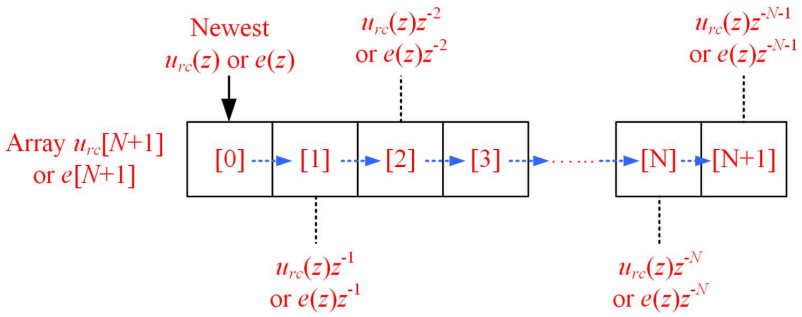
$$G_{rc}(z) = \frac{u_{rc}(z)}{e(z)} = k_{rc}\frac{\alpha_1 z^{-N+p+1} + \alpha_0 z^{-N+p} + \alpha_1 z^{-N+p-1}}{1 - \alpha_1 z^{-N+1} - \alpha_0 z^{-N} - \alpha_1 z^{-N-1}} \tag{2.6}$$

$$\begin{aligned} &u_{rc}(z) - \alpha_1 u_{rc}(z) z^{-N+1} - \alpha_0 u_{rc}(z) z^{-N} - \alpha_1 u_{rc}(z) z^{-N-1} \\ &= k_{rc}(\alpha_1 e(z) z^{-N+p+1} + \alpha_0 e(z) z^{-N+p} + \alpha_1 e(z) z^{-N+p-1}) \end{aligned} \tag{2.7}$$

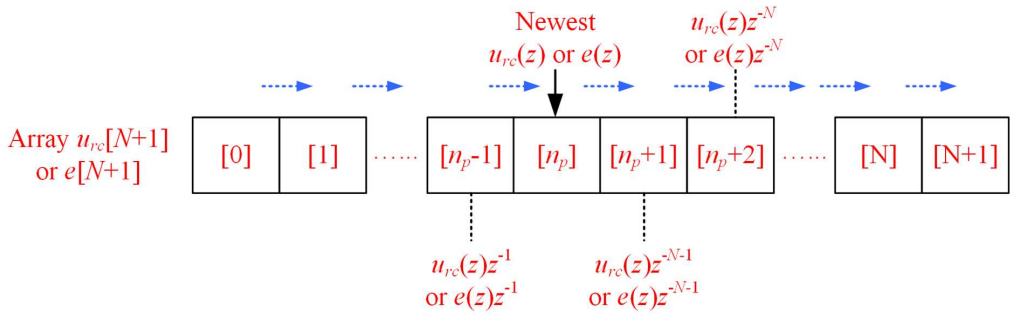
Where $u_{rc}(z)$ represents the controller output voltage and $e(z)$ is the input current error.

(ii) Digital implementation of the repetitive controller. From (2.7), the output of the repetitive controller is simply an algebraic equation using historic data of $u_{rc}(z)$ and $e(z)$. Particularly, we are using $u_{rc}(z)$ that has a delay of $N-1$, N, and $N+1$ switching cycles, respectively. We are also using e(z) that has a delay of $N-p-1$, $N-p$, and $N-p+1$ switching cycles, respectively. The maximum delay step in the transfer function is $N+1$. Therefore, we created two arrays, each has $N+2$ elements (one more element for the current switching cycle), to store all historic values of $u_{rc}(z)$ and $e(z)$, respectively. Fig. 2.20(a) shows a traditional implementation method for a repetitive controller. Each box represents an element and the number in the brackets represents the index of the element. During each switching cycle, all the elements in the array will be shifted right by one position. Then, $u_{rc}(z)$ and $e(z)$ from the current switching cycle will be stored in the element with index of 0. In this way, the last element, which has an index of $N+1$, represent $u_{rc}(z)$ and $e(z)$ with a delay of $N+1$ switching cycles. This method is straightforward

since the index of each element is equal to the delay step. However, the disadvantage of this technique is also obvious. In every switching cycle, N elements will be moved once, which takes a lot of time since N is usually around 200 to 400 in such applications. Using this traditional method consumes much time and will make the ePWM interruption time exceed the switching period limit. Fig. 2.20(b) shows an alternative approach to implement the repetitive controller. $u_{rc}(z)$ and $e(z)$ from each switching will be stored in different elements instead of a fixed one. For example, $u_{rc}(z)$ and $e(z)$ from the 1^{st} switching cycle will be stored in the index 0 elements. In the 2^{nd} cycle, the updated $u_{rc}(z)$ and $e(z)$ will be stored in the index 1 elements. In the 3^{rd} cycle, the data will be stored in the index 3 elements. This pattern is followed for the rest switching cycles. If the index reaches $N+1$, then it goes back to 0 for the next switching cycle. The index of the element which stores the newest data, denoted as n_p ($0 \leq np \leq N+1$), will repeat from 0 to $N+1$ continuously. The required historic data in (2.7) can be easily found based on n_p, and this is shown in Table 2.3. In the alternative method, no elements will be moved. The only thing that changes every switching cycle is the storage position of the newest $u_{rc}(z)$ and $e(z)$. The efficiency of the modified algorithm has been greatly improved. For example, assume the switching frequency of the inverter is 18 kHz, and the traditional method takes about 40 μs which is 72% of the entire switching period. However, it only takes 1 μs for the proposed approach.



(a)



(b)

Figure 2.20: (a)Traditional Digital Implementation Of A Repetitive Controller; (b)Proposed Digital Implementation Of A Repetitive Controller

Table 2.3: The Historic Data of $u_{rc}(z)$ And $e(z)$ With Required Number Of Delay Steps And Their Corresponding Index Numbers In The Array Under Two Different Impelemtation Methods

Historic data	**Corresponding index for the traditional method**	**Corresponding index for the alternative method**
$u_{rc}(z)z^{-N-1}$	$N+1$	n_p+1
$u_{rc}(z)z^{-N}$	N	n_p+2
$u_{rc}(z)z^{-N+1}$	$N-1$	n_p+3
$e(z)z^{-N+p-1}$	$N-p+1$	n_p+p+1
$e(z)z^{-N+p}$	$N-p$	n_p+p+2
$e(z)z^{-N+p+1}$	$N-p-1$	n_p+p+3

2.3.3 Simulation Results of Normal and Abnormal Operations of the DER Inverters

The proposed P control and inverter current control have been verified through PLECS simulation under both normal and abnormal operating conditions. Five operation modes defined as normal operation in IEEE 1547 have been simulated. Fig. 2.21 shows the simulation results. The P, Q feedbacks tracks the P, Q commands perfectly and are complying with the IEEE 1547 standard. Fig. 2.22 shows power distribution between two PVs and one battery system using the proposed P control for the DC/DC stage. Power rating for each PV is 1 kW and battery is rated at 1.5 kW in this scenario. From the simulation results, the PVs try to output their maximum power when the power command is beyond their power capability. The power difference is compensated by battery, and when the inverter is required to absorb active power, only battery responds to the command. PV cells will not generate any real power.

Two fault ride-throughs defined as abnormal operation in IEEE 1547 have been simulated. Fig. 2.23 shows the simulation results. Inverter output P and Q, as well as frequency and output voltage fulfill the 1547 standard. In addition, frequency-droop is included in the frequency ride-though operation as well.

2.3.4 Experimental Results of DER Operation with a Repetitive Controller

A 3 kVA single phase inverter has been built to test the controller performance of the harmonic current elimination and the proposed digital implementation of the repetitive controller. Fig. 2.24 shows the hardware picture of the inverter. The inverter has three DC/DC input channels in total. One channel is connected to PV

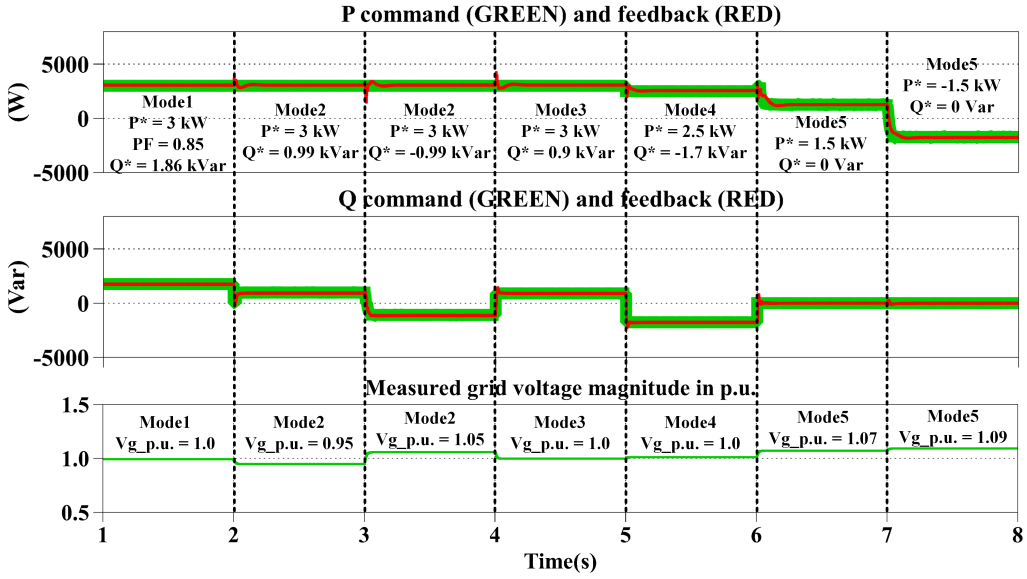


Figure 2.21: Simulation Results Of Real Power Command And Feedback, Reactive Power Command And Feedback, And Grid Voltage Magnitude Under Normal Operations

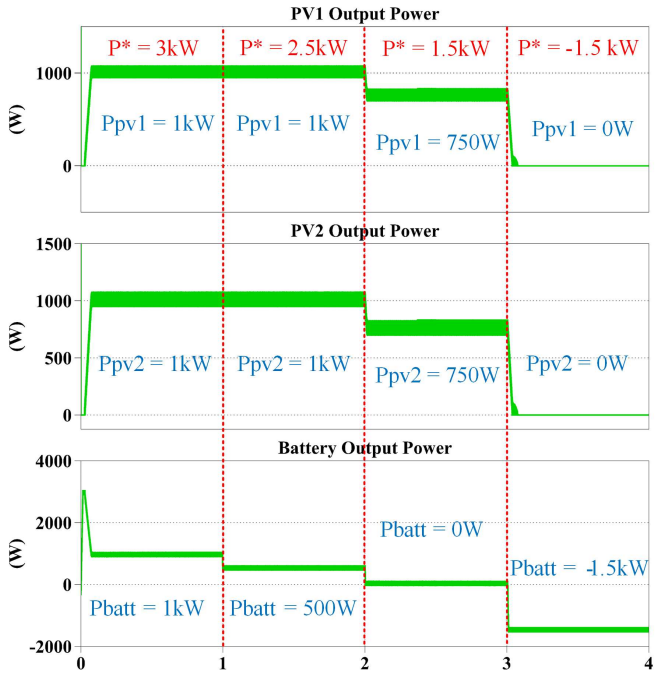


Figure 2.22: Simulation Results Of Power Distribution Among Different Types Of DERs

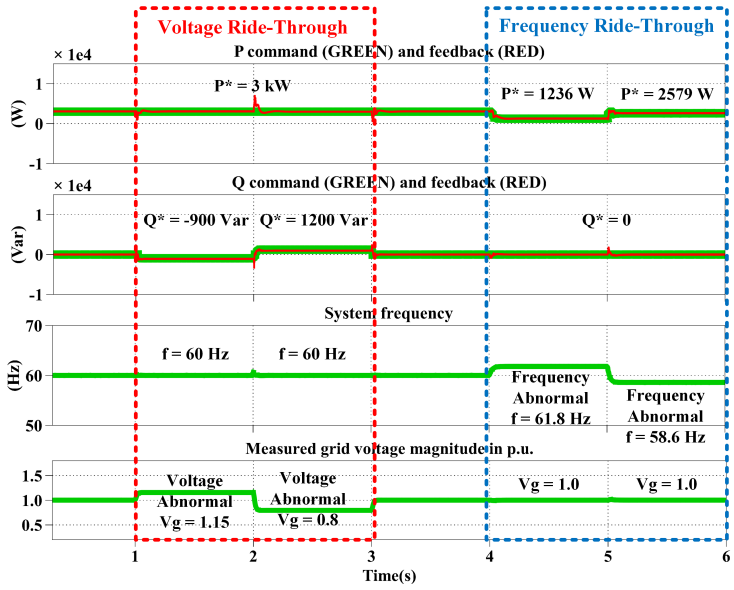


Figure 2.23: Simulation Results Of Real Power Command And Feedback, Reactive Power Command And Feedback, Grid Frequency, And Grid Voltage Magnitude Under Abnormal Operations

and other two are connected to batteries. Table 2.4 shows the devices and parameters of the inverter hardware. Fig. 2.25 shows the grid voltage and current waveforms with only open-loop dead-time compensation method proposed in [26]. The current THD is over 10% which is still high. Fig. 2.26(a) shows the experimental results of the designed DER inverter under grid-connected operation with unity power factor, and 3^{rd}, 5^{th}, 7^{th}, 9^{th}, and 11^{th} PR controllers are used to eliminate the harmonic current. Fig. 2.26(b) shows the results with a single repetitive controller. Note that the fundamental current is always controlled by a 60 Hz PR controller. The current THD under non-unity power factor conditions are also shown in Table 2.5 for both PR controller and repetitive controller approaches. The results show that the repetitive controller gives a better current THD than multiple PR controllers do even under distorted grid voltage (THD_V =2.68%).

Figure 2.24: Hardware Picture Of The Designed 3 kVA Inverter

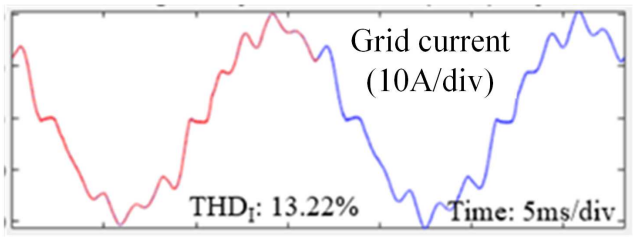
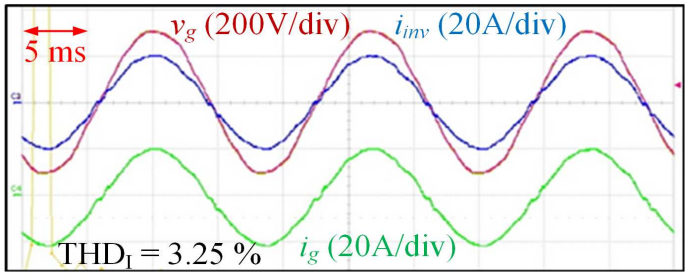
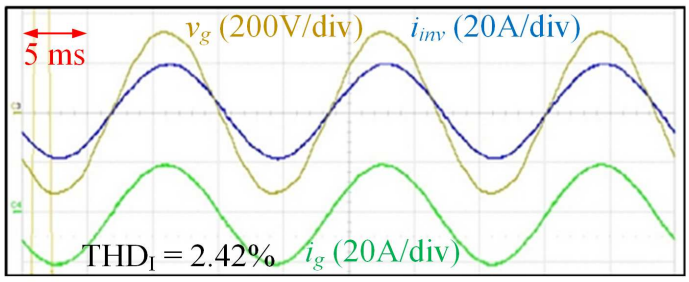


Figure 2.25: Experimental Results Using Only Open-loop Dead-time Compensation



(a)



(b)

Figure 2.26: (a)Experimental Results Using Multiple PR Controllers To Compensate Harmonic Current Under Unity Power Factor; (b)Experimental Results Using A Repetitive Controller To Compensate Harmonic Current Under Unity Power Factor

Table 2.4: Devices And Key Parameters Used In The Experiments

Devices/Parameters	**Values**
Power modules	FS35R12W1T4(1200V/35A)
Digital Signal Processor	TMS320F28379D
Gate driver ICs	1ED020I12-F2
DC link voltage	400 V
Grid voltage	208 V_{RMS}
Switching frequency	18 kHz
Dead-time	1.0 μs

Table 2.5: Grid Current THD Comparison Between PR Controllers And Repetitive Controllers (RCs)

Power factor	**THD_I(PR controllers)**	**THD_I(RCs)**
1.0	3.25%	2.42%
0.7 lagging	4.53%	2.48%
0.7 leading	4.03%	2.27%

2.4 SOGI Based Active Anti-islanding Detection

2.4.1 Challenges and Motivations

Due to an increasing penetration rate of distributed renewable energy resources in the power system, islanding becomes one of the most important safety issues for microgrids. Islanding refers to a situation where Distributed Generators (DGs) continue to power partial local load with the absence of the main grid. Unintentional islanding can be dangerous to utility workers and other electric components that are no longer controllable by the main utility [29]. In additional, islanding may cause

power line asynchronization with respect to the grid. Large inrush current can occur when reclosing under such circumstance [30]. As a result, all DGs should be equipped with Anti-Islanding Protection (AIP) unit to detect islanding event within the time requirement specified by different international standards such as IEEE 1547. Different AIP methods have been explored during the last decade. They can be classified into three categories [31–33] which are Passive method, Active method, and Communication based method. Communication based method is the least desirable option, even though it is effective and reliable, due to its high cost for transferring data between each DGs and controllers. Passive method usually measures system parameters, such as voltage and frequency at Point of Common Coupling (PCC), to monitor the change before and after an islanding event happens [34]. Under/Over voltage (UVP/OVP) and Under/Over frequency protection (UFP/OFP) are the most straightforward passive methods which generate an islanding signal when the PCC voltage and frequency variation exceed pre-defined limits [35]. Rate of change of frequency (ROCOF) and Rate of change of power (ROCOP) can also be measured to detect islanding [36]. [37] introduced a method by measuring the change in the amplitude of the 5th harmonic in PCC voltage to detect islanding, which requires special equipment to analyze the frequency spectrum of the PCC voltage. However, the main disadvantage of most passive methods is their large Non-Detection Zone (NDZ). In this case, the voltage and frequency variation at PCC will be too small to be identified, which leads to failure of the AIP methods [38]. [39] claims its passive AIP has no NDZ. Nevertheless, the presented control loop for each inverter includes a low-pass filter which introduces a huge delay. Active method relies on the change of disturbance on the terminal of each DG by intentionally inject small perturbation. The change can be significantly after the grid is disconnected even when the power mismatch between DGs and load is small [40]. Therefore, active methods can achieve

zero NDZ. The popular active techniques are: Slip-Mode frequency Shift method [41], Active Frequency Drift method [42], and PLL based active method [43]. However, the power quality will be affected due to the injection of disturbance. Moreover, the controller performance will be greatly affected by traditional PLL under weak grid condition. This section proposes a novel active AIP method which is based on sinusoidal reactive power injection and SOGI. A small amount of 40 Hz reactive power command will be intentionally added to the q-axis of the control system, under which the harmonic power with corresponding frequency will be either injected into the grid when the grid is connected or injected to the load when the grid is disconnected. If the grid is connected, the PCC voltage is clamped by the stiff grid voltage; however, if the grid is disconnected, this injected harmonic will be revealed on the PCC voltage. The proposed method tries to extract this low-amplitude 40 Hz component from the large-amplitude main frequency component of the PCC voltages by using SOGIs in dq-frame instead of traditional PLL to identify islanding.

2.4.2 Proposed AIP Method

A typical anti-islanding test configuration can be represented by Fig. 2.27. An inverter is connected to an RLC load through an LC filter. The grid is connected to this system through a controllable breaker S. The RLC parallel load is designed to resonate at 60 Hz so that it only consumes real power when the system is operating at resonant frequency. The value of each component of the RLC load can be determined by the following equations.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{2.8}$$

$$R = \frac{V^2}{P} \tag{2.9}$$

$$L = \frac{V^2}{2\pi f Q_f P} \tag{2.10}$$

$$C = \frac{Q_f P}{2\pi f V^2} \tag{2.11}$$

In the above equations, P is the real power absorbed by R and Q_f is the quality factor. V represents the line-to-line RMS voltage of the system. The proposed AIP method must be tested under the worst case where the inverter is controlled to provide the exact amount of real power that the RLC load needs, which leads to a negligible amount of real and reactive power exchange with the grid. After disconnecting the grid by opening the breaker S, the inverter continues to operate, and cannot tell if the grid is gone. The proposed AIP method can be summarized in the following four steps.

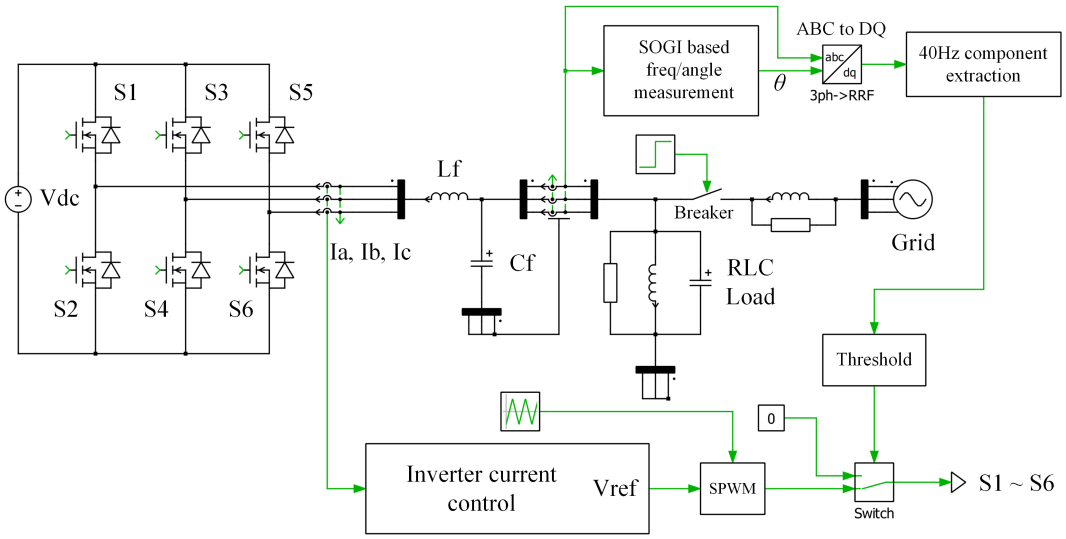


Figure 2.27: A Typical AIP Test System Configuration

(a) **Reactive power injection:** A 40 Hz sinusoidal reactive power (1.25% of the rated power, adjustable) will be added to reactive power command on q-axis, which is equivalent to adding 40 Hz sinusoidal harmonic to the current references

on q-axis. The equations showing the relationship between real and reactive power command and dq current reference are

$$i_{dref} = \frac{P_{cmd}}{1.5V_{mag}} \tag{2.12}$$

$$i_{qref} = -\frac{Q_{cmd}}{1.5V_{mag}} \tag{2.13}$$

where V_{mag} is the magnitude of the line-to-neutral grid voltage. P_{cmd} and Q_{cmd} are real and reactive power commands, respectively. i_{dref} and i_{qref} are current references on d-axis and q-axis, respectively.

(b) **Frequency/Angle measurement using SOGI:** The PCC voltage frequency and angle can be measured by using SOGIs with a center frequency of 60 Hz. The dq rotating angle can be calculated by the 60 Hz voltage components in Alpha-Beta frame after eliminating the negative sequence components. The angle will be used in ABC to dq and dq to ABC transformations of the grid currents and voltages in order to perform inverter current control.

(c) **40 Hz component extraction using a Double-SOGI topology:** The 40 Hz harmonic from PCC voltages in dq frame will be extracted by using a proposed Double-SOGI based topology.

(d) **Threshold comparison:** If the amplitude of the 40 Hz harmonic is below the pre-defined threshold, it can be judged that the inverter is still operating in grid-connected mode. Otherwise, the inverter is considered islanded and will be shut down by disabling all the gate signals. The injected 40 Hz reactive power ripple will be absorbed by the stiff voltage source when the grid is present since the grid impedance is be much smaller than the RLC load. However, when the grid is disconnected, this 40 Hz reactive power has nowhere to go but the

RLC load which leads to a large variation in 40 Hz harmonic amplitude in grid voltage.

2.4.3 Advantages of the Proposed AIP Method

The proposed AIP method eliminates the delay in measuring the PCC frequency/angle by using SOGI instead of traditional PLL and successfully achieved 40 Hz harmonic extraction without doing complex Fourier Analysis, which greatly improves the calculation efficiency and performance. The detailed description of each benefit will be presented as follows.

(a) **Frequency/Angle measurement using SOGI:** Fig. 2.28 shows the configuration of a SOGI. From the figure, it is easy to derive the two transfer functions as follows,

$$H_{sin}(s) = \frac{\text{Sin\_out}}{\text{Input}} = \frac{k\omega_o s}{s^2 + k\omega_o s + \omega_o^2} \tag{2.14}$$

$$H_{cos}(s) = \frac{\text{Cos\_out}}{\text{Input}} = \frac{k\omega_o^2}{s^2 + k\omega_o s + \omega_o^2} \tag{2.15}$$

In the transfer functions, ω_o is known as the center frequency, and k is a constant. The bode plots of the two transfer functions are also presented in Fig. 2.29 with a center frequency of 60 Hz. It is obvious that the Sin_out of a SOGI performs as a band pass filter which extracts the center frequency component with zero phase delay. The constant k affects the width of the band as well as the transient response of the SOGI. Fig. 2.30 shows the SOGI-based topology implemented in the AIP method to measure the frequency and angle of the PCC voltages. The basic idea is to do arctan function between the alpha and beta voltages. However, the frequency and angle of the PCC should be calculated only from the positive sequence alpha-beta voltage. Therefore, the negative

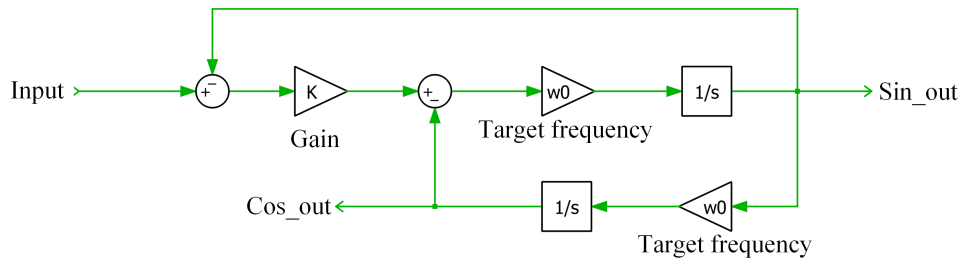


Figure 2.28: A Simple SOGI Configuration

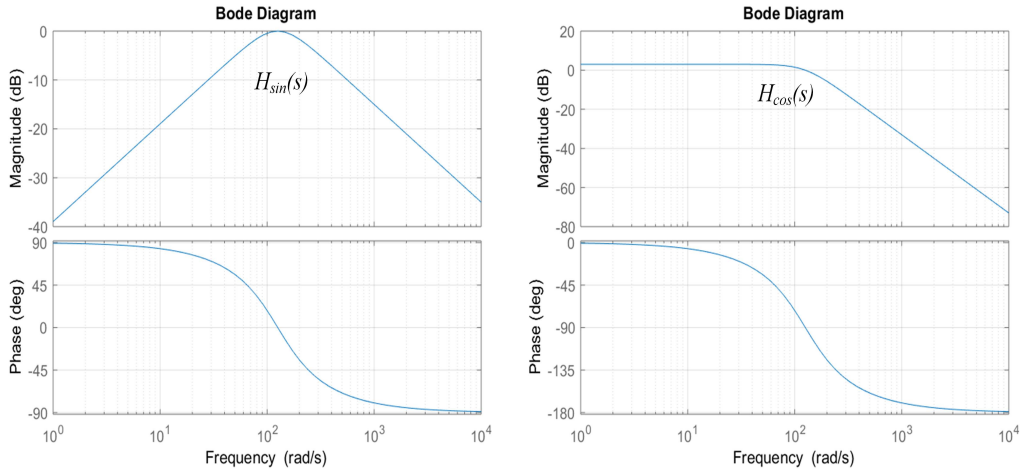


Figure 2.29: Bode Plots Of SOGI Outputs

sequence components in the voltage need to be separated from the positive sequence. In the proposed method, SOGI is employed on both Alpha-axis voltage and Beta-axis voltage to get the sin output which is in phase with the input and the cos output which is 90-degree phase shifted from the input. Both sin and cos components on Alpha-axis contains not only the positive sequence but also negative sequence alpha-beta voltages. The same thing happens on Beta-axis. By building up their relationship and solve the equations, the positive sequence Alpha-Beta voltages can be easily separated from the negative sequence Alpha-Beta voltages [44]. In Fig. 2.30, Valpha+ and Vbeta+ represent the positive sequence component of the PCC voltage in $\alpha\beta$ frame, respectively. Valpha- and

Vbeta- represent the negative sequence component of the PCC voltage in $\alpha\beta$ frame, respectively. The angle of the PCC voltage can be computed by using the arctan function involving only positive sequence components. As a result, the angular frequency of the PCC voltage can be easily calculated by a DSP according to the following equation.

$$\omega_{system} = \frac{\theta - \theta_{pre}}{T_s} \tag{2.16}$$

In the equation, θ and θ_{pre} are angles coming from SOGI from current step and last step, respectively. And T_s is the sampling time of the DSP. Compared with traditional PLL, this topology eliminates the PI controller. In addition, SOGI has the advantages of better dynamic response, higher tracking accuracy, and faster detection of reference signal under varying grid conditions [44]. Fig. 2.31 shows that SOGI has a faster transient response compared with traditional PLL with the same step change.

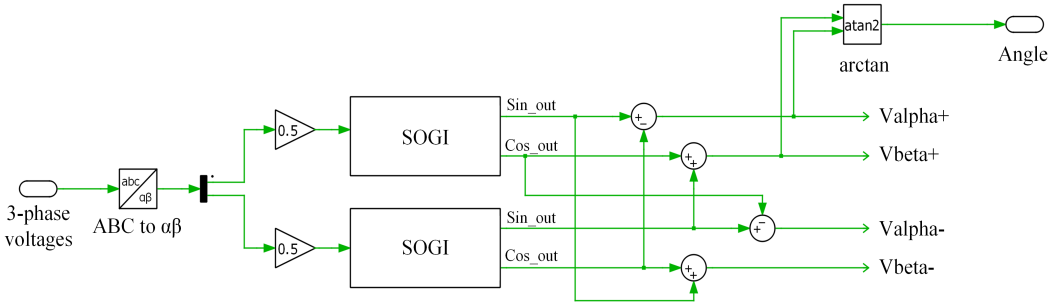


Figure 2.30: SOGI Based Frequency/Angle Measurement At PCC

(b) **40 Hz reactive power injection:** Speaking of reactive power injection, two questions must be taken into considerations: How much reactive power and what frequency of the reactive power should be injected. The amount of reactive power injected into the grid cannot be too large in order to avoid transformer saturation and system malfunction. On the other hand, the level of injected

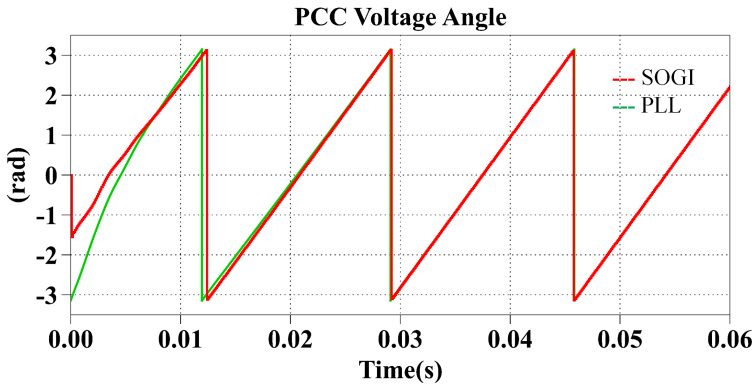


Figure 2.31: PCC Voltage Angle Measured By SOGI And Traditional PLL

reactive power cannot be too low in case that the variation in harmonic amplitude is too small to be detected. Since the sinusoidal reactive power is injected in dq-frame, the voltage and current in ABC frame contain multiple harmonic frequencies based on Park Transformation. For instance, if a q-axis signal contains a sinusoidal component with frequency of f_1, and the dq-frame is rotating at the speed of f_2, the resulting ABC signals will see the following frequency components: $f_2 - f_1,\ f_2,\ f_2 + f_1$. In the proposed method, since the 3-phase voltage at PCC will be used to get its frequency and angle by setting the center frequency of the SOGIs as 60 Hz, the harmonic frequency components should have adequate distance from 60 Hz to have larger attenuation in SOGI output and not distort the extraction of the 60Hz components. Larger attenuation means less harmonic in the SOGI output and higher accuracy in frequency and angle measurement. Table 2.6 shows the SOGI attenuation percentage in ABC frame when injecting harmonics with different frequencies in q-axis. In the proposed method, 40 Hz has been chosen as the injected harmonic frequency and the amount of reactive power injected is designed to be 1.25% of the rated power. In this way, the volt-second of the low frequency component (20 Hz) in ABC frame is small so that the transformer saturation can be avoided. It is worth

Table 2.6: SOGI Attenuation Percentage In ABC Frame When Injecting Harmonics With Different Frequencies In q-axis

Injected frequency	**Attenuation percentage**	
20 Hz	40 Hz: 13.8% reduction	80 Hz: 7.6% reduction
30 Hz	30 Hz: 31.2% reduction	90 Hz: 13.8% reduction
40 Hz	20 Hz: 53.2% reduction	100 Hz: 20.2% reduction
50 Hz	10 Hz: 76.7% reduction	110 Hz: 26.1% reduction

noting that the harmonic frequency selection is also affected by the RLC load, which will be described in the next section.

(c) **RLC load design:** The RLC load design equations are listed in Section 2.4.2. Once the system specifications are determined, the load resistance is fixed. However, the load inductance and capacitance vary with different quality factors. Based on the fact that the injected reactive power has to be absorbed by the main grid when the breaker is closed, the impedance of the RLC load at the injected harmonic frequency should be much larger than the grid impedance. Fig. 2.32 shows the impedance curve of an RLC load with different quality factors as well as grid impedance. In this case, the grid impedance is 4.7% in per unit. The ratio between load impedance and grid impedance at harmonic frequency is related to both quality factors and the distance between the harmonic frequency and 60 Hz. Fig. 2.32 indicates that the ratio of load impedance over grid impedance increases when quality factor goes down at a fixed frequency. Therefore, a large ratio requires a small quality factor. In addition, under a fixed quality factor, the impedance ratio reaches its maximum at 60 Hz and becomes smaller when the frequency moves away from 60 Hz, so a large ratio requires a harmonic frequency close to 60 Hz. In order to ensure proper operation when

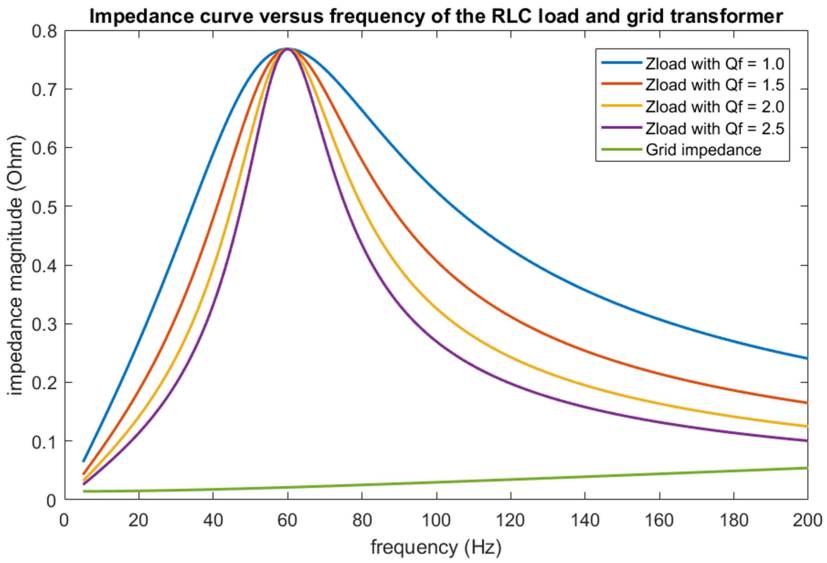


Figure 2.32: Impedance Curve Of The RLC Load With Different Quality Factors

the breaker is not open, the ratio of load impedance over grid impedance should be as large as possible so that most injected reactive power flows to the grid. Therefore, smaller quality factor and harmonic frequency which is close to 60 Hz can be selected. On the other hand, the needs to extract the 60 Hz components from the PCC voltage for angle calculation requires that the harmonic frequencies in ABC frame cannot not be too close to 60 Hz. As a result, 40 Hz is selected as the injected harmonic frequency and quality factor of the RLC load is selected as 1.0.

(d) **40 Hz component extraction:** In order to detect islanding condition, the 40 Hz harmonic ripple must be extracted from the PCC voltage in dq frame. One existing solution of harmonic extraction is Fourier Transformation which requires high complexity of computation and large memory from computers. To overcome this disadvantage, a new Double-SOGI based harmonic extraction method is presented in Fig. 2.33. The magnitude of a sinusoidal waveform can

be calculated by the following equation if its orthogonal signal with the same amplitude and frequency is known.

$$\text{Mag} = \sqrt{(Asin(\omega t))^2 + (Acos(\omega t))^2} \tag{2.17}$$

As shown in Fig. 2.33, if the center frequency of SOGIs is selected at 40 Hz, Sin_out of the first SOGI will only contain the 40 Hz harmonic sinusoidal signal without any DC component. The second SOGI is used to generate an orthogonal signal by taking its Cos_out. Therefore, the magnitude of the 40 Hz harmonic ripple in d-axis voltage can be easily calculated by using (2.17). The same method can be implemented in q-axis. The reasons why the extraction is not

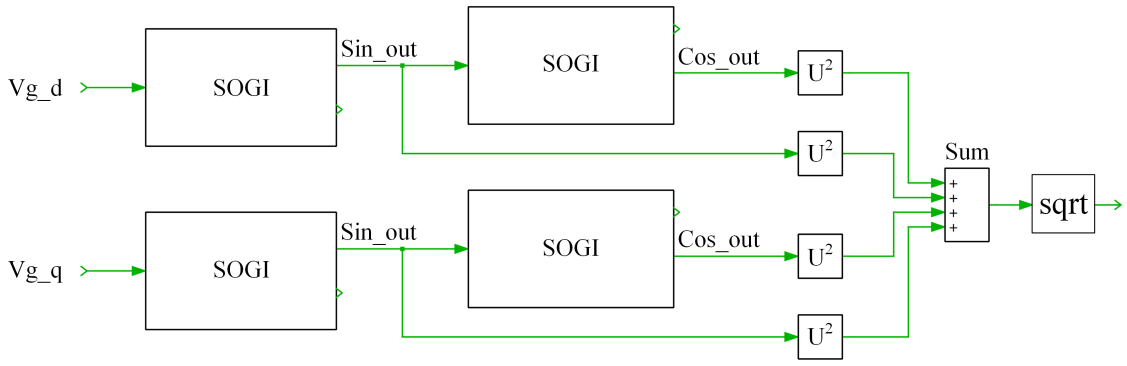


Figure 2.33: A Double-SOGI Based 40 Hz Harmonic Extraction Method

performed in ABC frame can be summarized as follows. Firstly, the ABC frame voltage contains multiple harmonic frequencies (i.e. 20 Hz and 100 Hz). At least two SOGIs with different center frequencies must be used. However, the grid voltage in dq frame only contains DC component and 40 Hz harmonics. Secondly, 60 Hz is the main frequency component (around 98%) of the 3-phase voltage at PCC, and the harmonic frequencies is not very far away from 60 Hz. It is difficult to extract harmonic frequencies due to limited attenuation at 60 Hz of SOGIs. However, the dq frame only contains harmonics and DC

components. Sin_out of a SOGI is able to completely remove DC component of its input according to the big attenuation at zero frequency shown in the Bode plot of $H_{sin}(s)$. Therefore, performing harmonic extraction in dq frame results in simpler topology as well as higher accuracy.

2.4.4 Simulation Verification

(a) **PLECS simulation results:** A PLECS simulation verifying the effectiveness of the proposed AIP method has been conducted with the system parameters shown in Table 2.7. The breaker S opens at t = 0.35 second. Fig. 2.34 shows

Table 2.7: System Specification For PLECS Simulations

System parameters	Values
Grid line-toline-voltage (RMS)	480 V
System frequency	60 Hz
Injected reactive power frequency	40 Hz
Injected reactive power amplitude	3750 Var
RLC load power at resonant frequency	300 kW
RLC load resistance	0.768 Ω
RLC load inductance	2.0372 mH
RLC load capacitance	3453.8833 μF

that the inverter output voltage and current have little change before and after 0.35s, which indicates that the inverter feels nothing different after grid disconnection and it is difficult to tell whether the grid is still present. Fig. 2.35 displays the grid voltage and current. The current before 0.35 s is small due to little power exchange between the grid and the RLC load. After 0.35 s, the grid is disconnected, and the current becomes zero. The ripple in the grid current

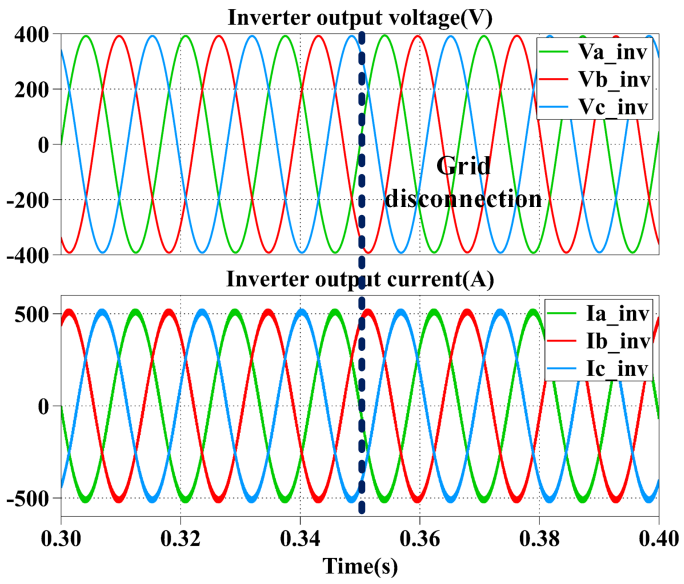


Figure 2.34: Simulation Results Of The Inverter Output Phase Voltage And Current After The LC Filter

is due to the reactive injection and the frequency is a mix of 20 Hz and 100 Hz (40 Hz is injected in *dq* frame) and it has very small amplitude compared with normal load current. Fig. 2.36 shows the measured system frequency at PCC

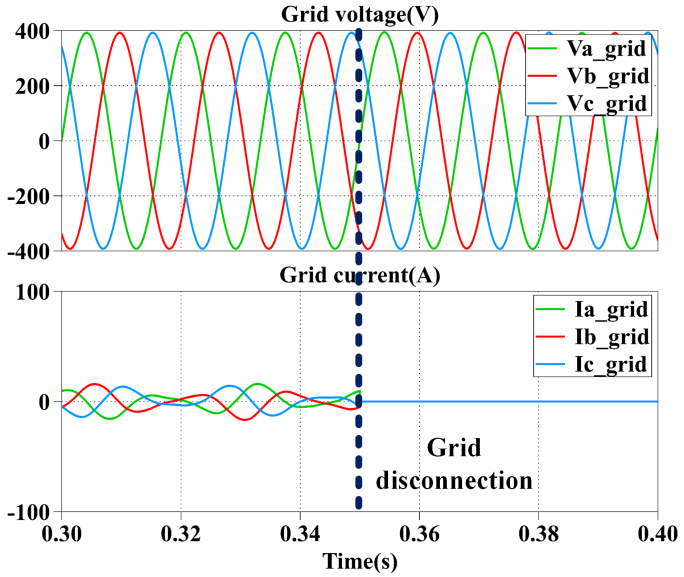


Figure 2.35: Simulation Results Of The Grid Phase Voltage And Current

before and after the breaker is open. It reveals that the system frequency also has variation after the grid is disconnected since the SOGIs used to measure this frequency cannot completely remove 20 Hz and 100 Hz ripple. As a result, the frequency will still contain some 40 Hz ripple. Fig. 2.37 shows the measured 40 Hz harmonic amplitude using the proposed Double-SOGI topology before and after the breaker is open. The amplitude of the 40 Hz component rapidly increases after 0.35 s. As a result, the threshold in this case can be set to 1.5. In addition, the measured harmonic amplitude reaches steady state only after one fundamental cycle which means SOGI has a very good transient response.

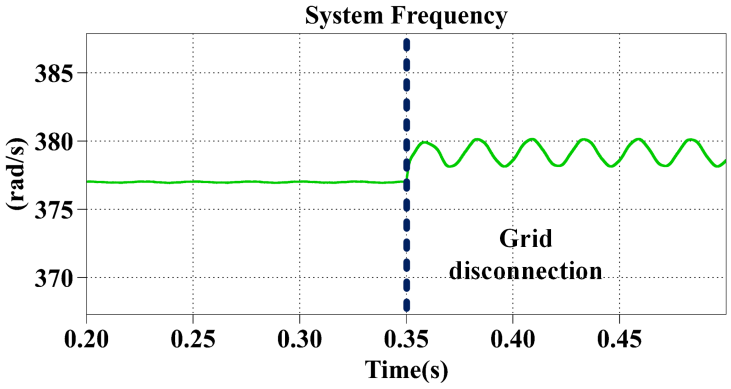


Figure 2.36: Simulation Results Of The Measured System Angular Frequency

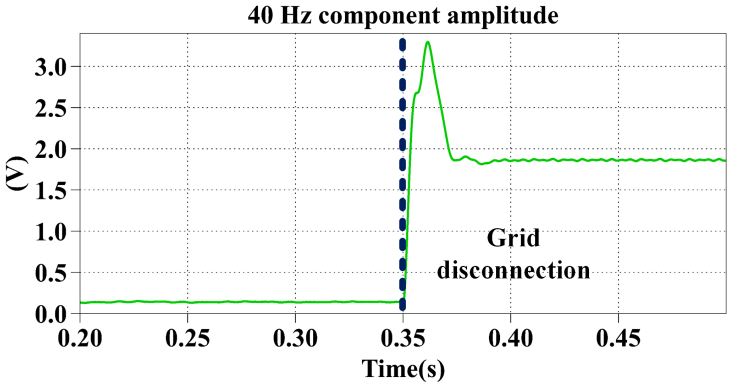
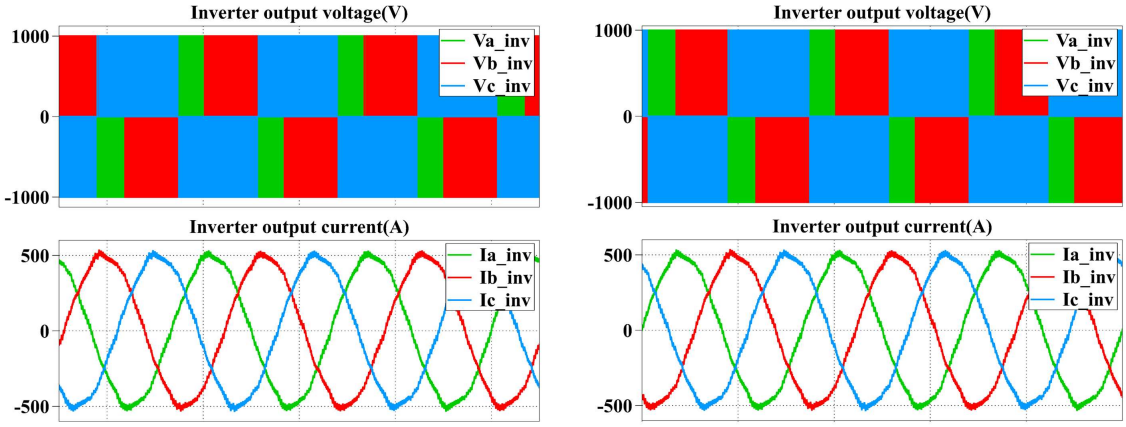


Figure 2.37: Simulation Results Of The Amplitude Of The 40 Hz Component

(b) **Hardware-In-Loop (HIL) simulation results:** A HIL simulation using the PLECS RT-box has also been carried out. The simulation step is fixed at 1 μs. Fig. 2.38 shows the inverter output voltage and current before and after the breaker is opened, and Fig. 2.39 shows the grid voltage and current before and after the breaker is opened. These figures indicate that the inverter output voltage remain almost unchanged before and after the breaker changes its state. Fig. 2.40 shows the 40 Hz component amplitude before and after the breaker is



(a) (b)

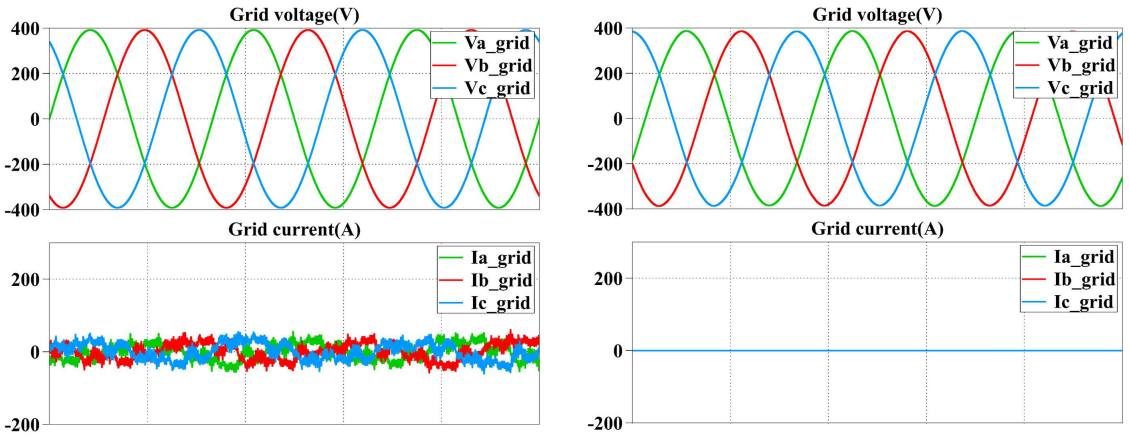
Figure 2.38: (a)Inverter Output Voltage And Current Before The Breaker Opens; (b)Inverter Output Voltage And Current After The Breaker Opens

open using HIL simulation. From both figures, the proposed harmonic injection and SOGI based AIP method has been proved to be effective.

2.5 Low-Voltage-Ride-Through (LVRT) Control Under Unbalanced Grid Voltage

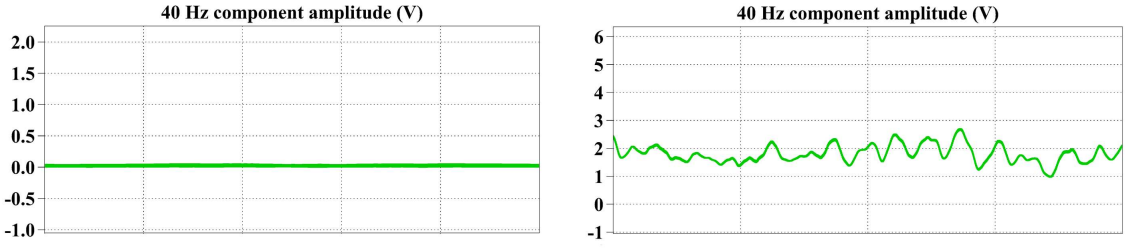
2.5.1 LVRT Control Strategies

IEEE standards require inverters to remain online and to provide the required amount of real and reactive power when the grid is under the fault condition. Among



(a) (b)

Figure 2.39: (a)Grid Voltage And Current Before The Breaker Opens; (b)Grid Voltage And Current After The Breaker Opens



(a) (b)

Figure 2.40: (a)40 Hz Component Amplitude Before the Breaker Opens; (b)40 Hz Component Amplitude After the Breaker Opens

transmission line faults, roughly 5% are symmetric [45]. Most commonly seen faults are asymmetric, such as a line to ground fault, a line to line fault and so forth. In this section, LVRT control under asymmetric faults will be discussed.

For symmetric faults, the normal grid current control is still valid. During LVRT operation, the DC link voltage will be controlled by the front DC/DC stage and be regulated to follow the change of grid voltage to maintain a high modulation ratio so that the high-frequency harmonics injected into the grid can be attenuated significantly [46]. The inverter output current reference will be determined by required real and reactive power commands. Under an asymmetric fault condition, the three-

phase grid voltage becomes unbalanced. As a result, both positive and negative sequence components exist in the system and should be controlled by the inverter. The control diagram is shown in Fig. 2.41.

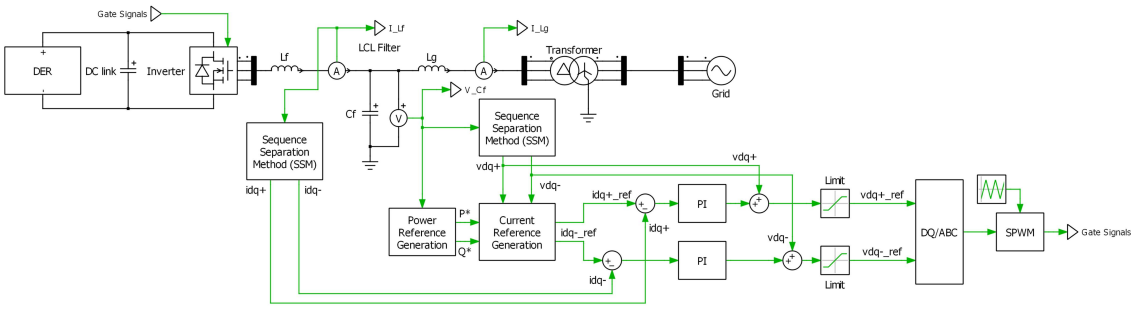


Figure 2.41: Control Diagram Of LVRT Using Positive And Negative Sequence Current Control

Firstly, the objective of the Sequence Separation Method (SSM) block is to retrieve positive and negative sequence components in the dq frame (4 quantities). Multiple advanced SSMs are introduced in many papers such as delayed signal cancellation method [47] and SOGI based SSM [48]. The SOGI based SSM has the advantages of small signal delay and good frequency adaptation capability. The system configuration is shown in Fig. 2.42. For a single SOGI, it is equivalent to a PR controller which only filters out the signal with selected frequency. By using two identical SOGIs, the positive and negative voltage components are separated under $\alpha\beta$ frame. The angle of the voltage can be directly calculated by using the positive sequence components as shown in Fig. 2.42. The angle can be used to generate positive and negative sequence components under dq frame.

Secondly, the Power Reference Generation block is used to provide real and reactive power commands based on grid standards. An example of desired active and reactive power commands (represented as P^* and Q^*) is shown in the following equations. The amount of reactive power is determined by the lowest grid voltage in per unit (represented as $V_{gp.u.}$), and the total apparent power cannot exceed inverter

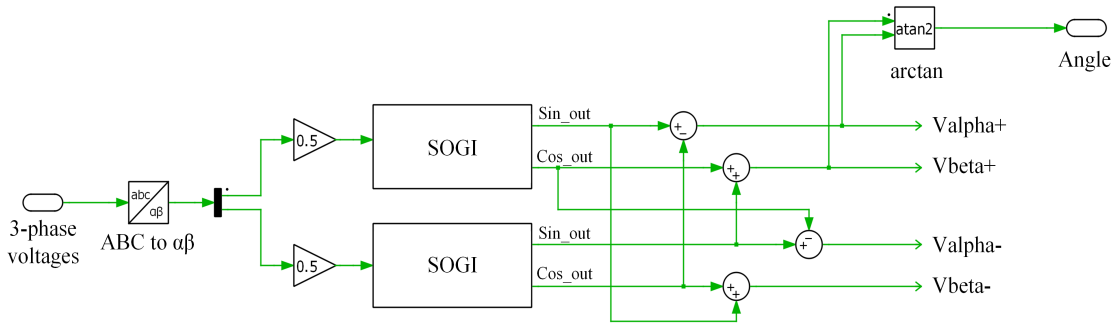


Figure 2.42: Configuration Of SOGI Based SSM

power rating [12].

$$0.0 \leq V_{gp.u.} \leq 0.5 \begin{cases} P^* = 0 \\ Q^* = P_{max} \end{cases} \tag{2.18}$$

$$0.5 \leq V_{gp.u.} \leq 0.9 \begin{cases} P^* = \sqrt{P_{max}^2 - Q^{*2}} \\ Q^* = 2(1 - V_{gp.u.})P_{max} \end{cases} \tag{2.19}$$

$$0.9 \leq V_{gp.u.} \leq 1.0 \begin{cases} P^* = P_{max} \\ Q^* = 0 \end{cases} \tag{2.20}$$

Finally, the Current Reference Generation block generates the four current references including positive and negative sequence components in the dq frame. The current references can be calculated from the following equations [12]. These current references will be sent to the four current regulators to generate corresponding voltage commands.

$$\begin{bmatrix} i_d^{+*} \\ i_q^{+*} \\ i_d^{-*} \\ i_q^{-*} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} v_d^+ & v_q^+ & v_d^- & v_q^- \\ v_q^+ & -v_d^+ & v_q^- & -v_d^- \\ v_q^- & -v_d^- & -v_q^+ & v_d^+ \\ v_d^- & v_q^- & v_d^+ & v_q^+ \end{bmatrix}^{-1} \begin{bmatrix} P^* \\ Q^* \\ 0 \\ 0 \end{bmatrix} \tag{2.21}$$

2.5.2 Simulation Results of the LVRT Control

The proposed LVRT control strategy has been simulated using PLECS. In order to unbalanced three-phase voltages, the Phase A voltage is intentionally changed to 0.8 per unit from 0.5 s to 1.5 s. The grid phase voltage and current are shown in Fig. 2.43, and inverter output current reference and feedback in the *dq* frame in terms of positive and negative sequence components are shown in Fig. 2.44. Fig. 2.45(a) shows the measured real and reactive power of the system while (b) is a zoom-in version of (a) at around t = 0.5 s. It is shown in Fig. 2.43 that the low voltage fault happens at t = 0.5 s, and the grid voltage becomes unbalanced. In order to regulate the real and reactive power, the inverter output current must be controlled in both positive and negative sequence. Fig. 2.44 shows that the four current regulators successfully control the inverter output current to follow the command. Fig. 2.45 shows the measured real and reactive power of the system. The real power is controlled to follow the command and has no oscillation while the reactive power will oscillate but with a controlled average value.

2.6 Control of DER Inverters in Standalone Mode

2.6.1 Droop and Supervisory Control

Droop control and supervisory control have been brought to attention under the circumstance that multiple inverters with different power ratings are connected in

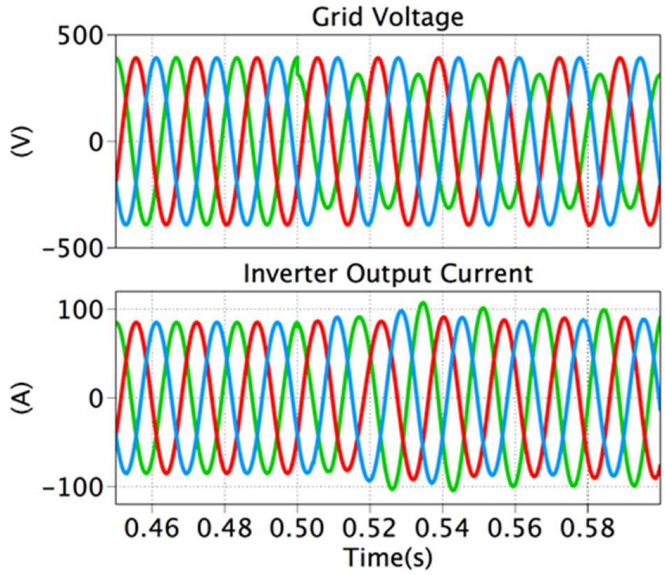


Figure 2.43: Simulation Results Of Grid Phase Voltage And Current In LVRT

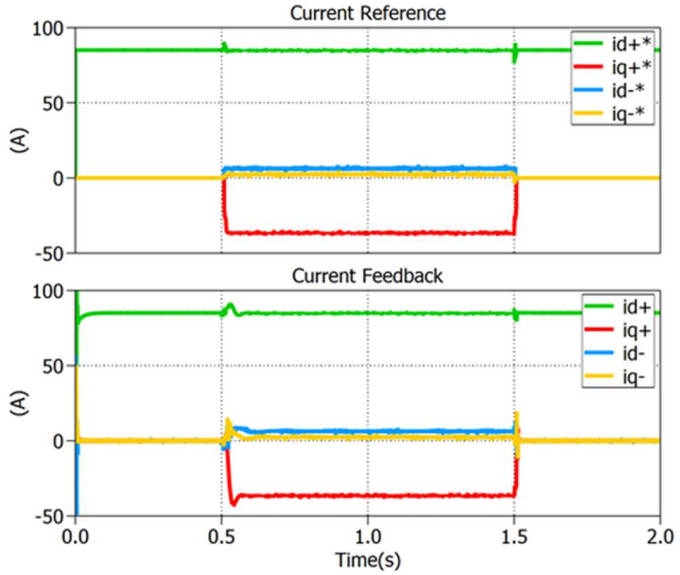
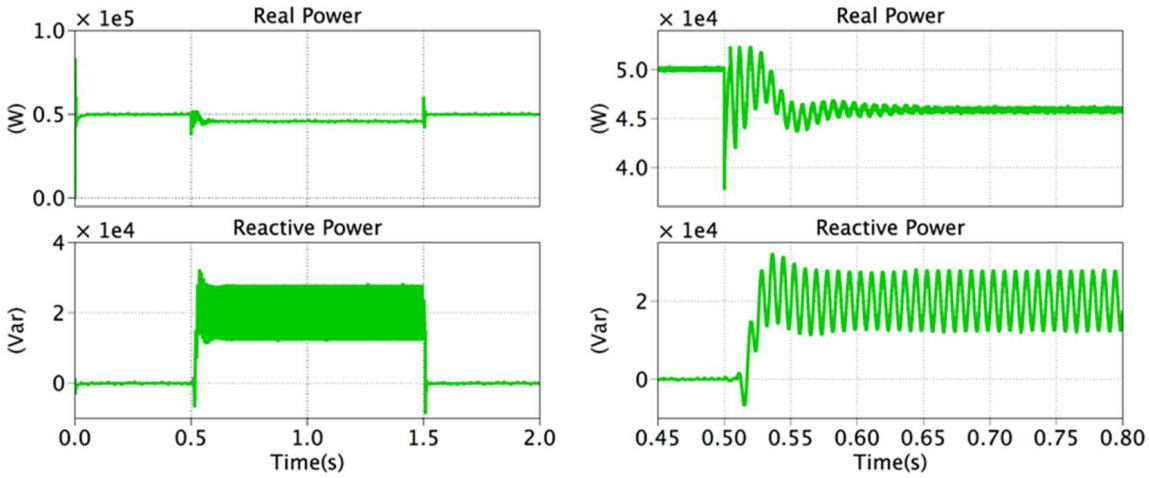


Figure 2.44: Inverter Output Current Reference And Feedback In The dq Frame In Terms Of Positive And Negative Sequence Components

parallel in a standalone situation, and no energy storage devices have been installed. In a traditional power grid, the voltage amplitude and frequency will change slowly based on the generators' droop curves when there is a load step change. This is because of the presence of large synchronous generators which have large inertia.



(a) (b)

Figure 2.45: (a)Real And Reactive Power Of The System; (b)Real And Reactive Power At Around t = 0.5 s

However, it is not the case in an inverter-based microgrid. Inverters have a high control bandwidth which means they can respond to load change very fast, which imposes threats to grid stability. One solution is to control the inverter outputs to follow the droop curves. The droops are coordinated to make sure each inverter supplies active and reactive power in proportion to its rating and share the load if the droop curves are designed in per unit sense. One advantage of the traditional droop method is that each inverter can operate independently, and no additional interconnection among the inverters is required [49]. Traditional droop equations are expressed as follows. ω and ω_{ref} represent the actual and the nominal angular frequency command of the inverter, respectively. V and V_{ref} represent the actual and nominal voltage magnitude command of the inverter, respectively. m and n are the droop coefficients for the $P-f$ and $Q-V$ curves, respectively. P and P_{ref} are the actual real power feedback and the nominal real power operating point, respectively. Q and Q_{ref} are the actual reactive power feedback and the nominal reactive power operating point, respectively.

$$\omega = \omega_{ref} + m(P - P_{ref}) \tag{2.22}$$

$$V = V_{ref} + n(Q - Q_{ref}) \tag{2.23}$$

Supervisory control introduced in [50] shows good performance in bringing grid frequency and voltage magnitude back to their rated values. The principle of supervisory control is illustrated in Fig. 2.46. For example, under no load condition, it is assumed that the grid frequency and voltage amplitude are at their predetermined rated values. When an arbitrary load has been connected, the grid frequency and voltage amplitude are supposed to drop based on the black droop curves in Fig. 2.46. The supervisory control measures real-time grid frequency and voltage amplitude to calculate the frequency and voltage error between the rated values and feedbacks. Then the error will be added to the starting points of droop curves, which is equivalent to lift the curves by the amount of error (the red droop curves). The final stable operating point will have the rated frequency and voltage amplitude. The implementation of droop and supervisory control is shown in Fig. 2.47.

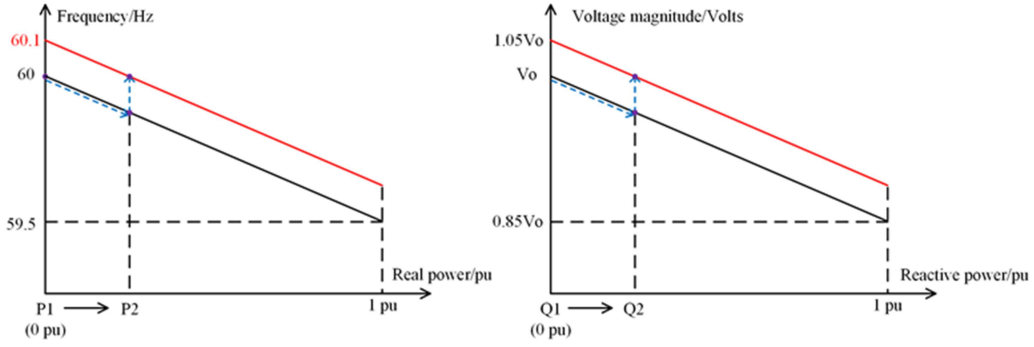


Figure 2.46: Illustration Of Supervisory Control Principle

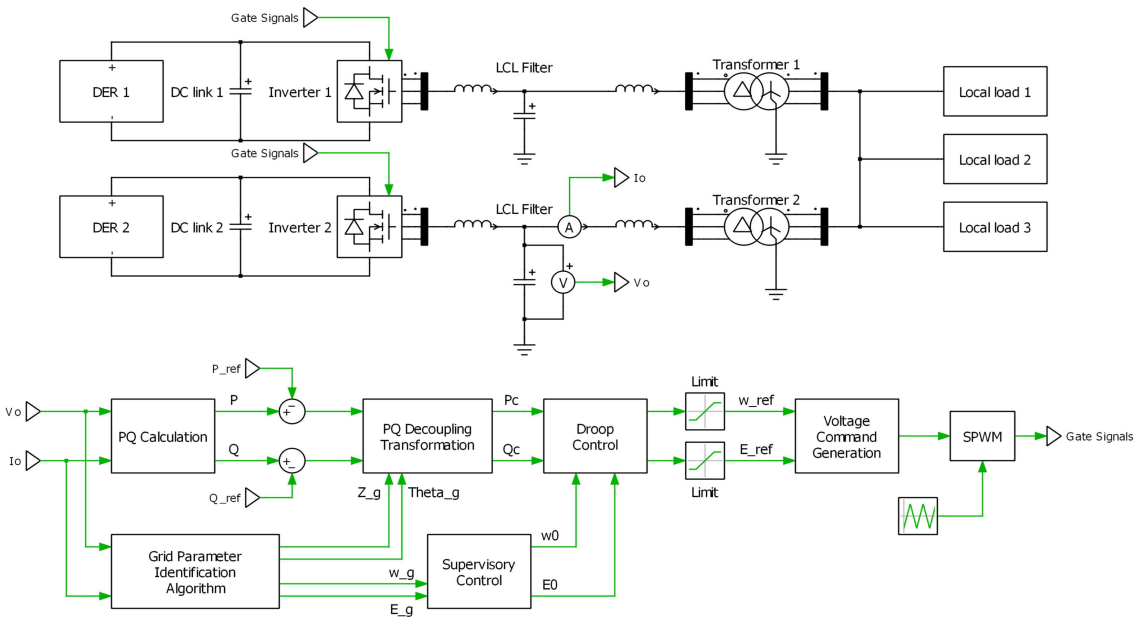


Figure 2.47: Implementation Of Droop and Supervisory Control

For each inverter, the instantaneous output real and reactive power will be firstly calculated by using the three-phase output voltage and current. The actual real power P_m and reactive power Q_m after the filter will be used to calculate frequency and voltage commands based on predefined droop equations. At the same time, the grid voltage and frequency will be measured using a PLL. The supervisory control will modify the starting point of the droop curve by adding the difference between the feedback and its rated value on top of the rated value. As a result, the final voltage and frequency will return to their nominal values.

2.6.2 Simulation Results of the Droop and Supervisory Control

The simulation of droop and supervisory control consists of three inverters with different power ratings connected in parallel. The system experiences a load step change at t = 0 s when all the load is connected to the AC bus and t = 2.0 s when an additional load has been added to the bus. Fig. 2.48 shows the grid (bus) phase

voltage and current. Fig. 2.49 shows the power-sharing among the three inverters. Fig. 2.50 and 2.51 show the grid frequency and voltage amplitude, respectively.

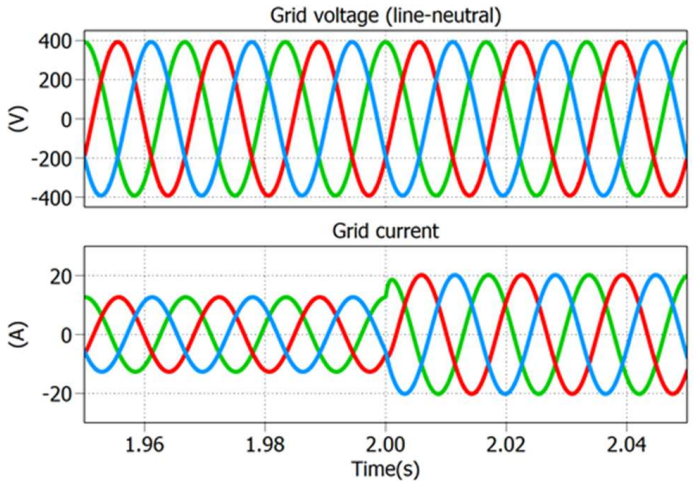


Figure 2.48: Simulation Results Of Grid Phase Voltage And Current

In Fig. 2.48, the grid current amplitude becomes larger at t = 2.0 s due to a load increase while the voltage experiences little fluctuation which shows the effectiveness of the droop and supervisory control. It is clear in Fig. 2.49 that the three inverters share the same per unit amount of real and reactive power all the time due to the implementation of the droop control. In Fig. 2.50 and 2.51, the grid frequency and voltage amplitude have been brought back to their rated value even after a load step change because of the supervisory control. The simulations results indicate that the droop and supervisory control are good candidates for reducing grid frequency and voltage fluctuation.

2.6.3 Advanced Droop Control with Active Slope Change

The aforementioned droop and supervisory control can achieve even power sharing without requiring the information of the rest inverters in the area only when the grid-impedance is inversely proportional to the rating of the respective inverter. When

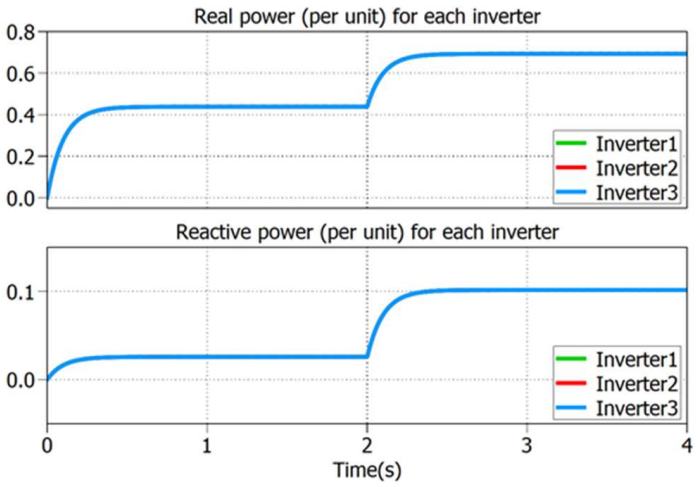
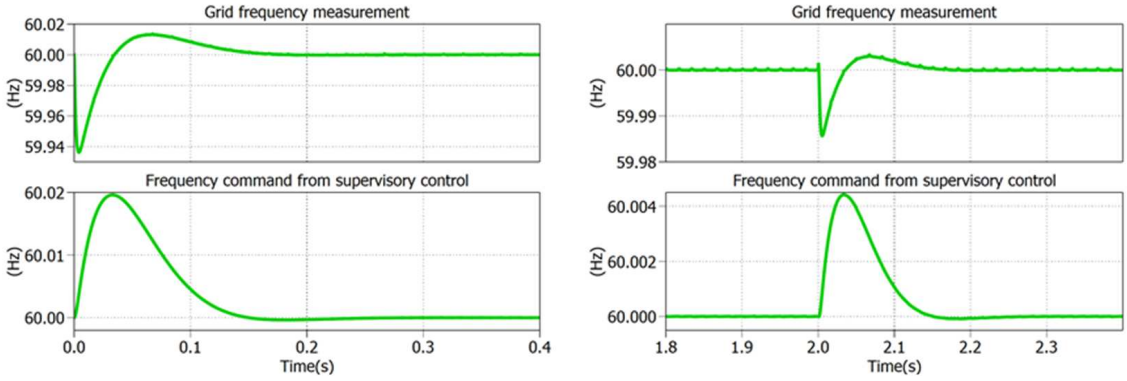


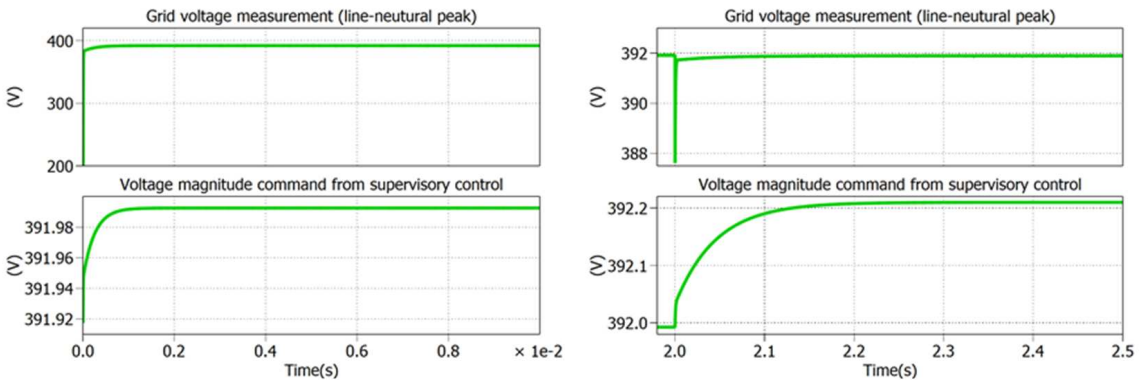
Figure 2.49: Real And Reactive Power Sharing Of The Three Paralleled Inverters



(a) (b)

Figure 2.50: Simulation Results Of Grid Frequency And Frequency Command From The Supervisory Control At Around (a) t = 0 s And (b) t = 2 s

this condition is not satisfied, reactive power is not properly shared. If a central communication system is existing, we are able to adjust the slope of the $Q-V$ droop curve for each inverter based on the reactive power feedback of the rest inverters. The advanced droop control block diagram is shown in Fig. 2.52. The averaged reactive power feedback of all the inverters will be sent to each inverter using the communictaion channel provided by an Edge Intelligent Device (EID). A closed-loop PI controller is used to tune the slope of the $Q-V$ droop curve. The slope of the $P-f$ droop curve remains unchanged since the main frequency is the same for all



(a) (b)

Figure 2.51: Simulation Results Of Grid Voltage And Voltage Command From The Supervisory Control At Around (a) t = 0 s And (b) t = 2 s

inverters.

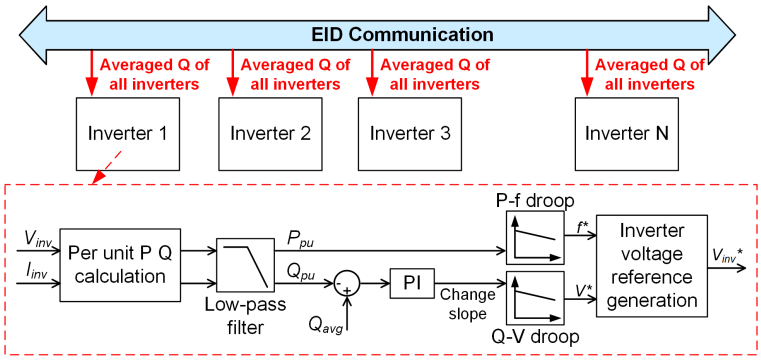


Figure 2.52: Control Diagram Of The Proposed Advanced Droop Control

A PLECS simulation has been conducted and the simulation circuit is shown in Fig. 2.53 where 5 PV inverters with the same power rating are connected through different grid impedances. The local load is simulated by some arbitrary RL load. Traditional droop control is firstly implemented and the advanced droop control is activated when the simulation time is equal to 6 seconds. Simulation results are shown in Fig. 2.54. The reactive power is not equally shared by each inverter when traditional droop is implemented. The power difference can be as large as 10% of the inverter rating. When the advanced droop control is implemented, the reactive power generated from each inverter becomes the same by adjusting the slope of individual

$Q - V$ droop curve.

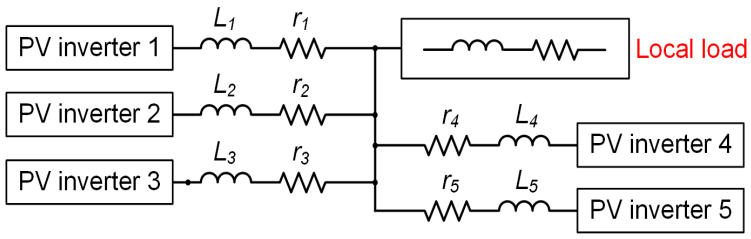


Figure 2.53: Simulation Circuit For Advanced Droop Control Verification In Island Operation

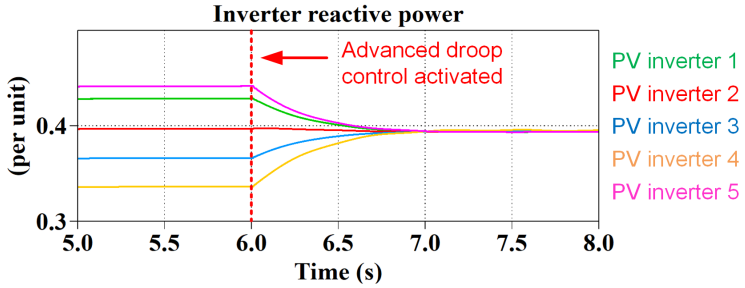


Figure 2.54: Simulation Results Of Reactive Power Among 5 Inverters With Advanced Droop Control Activated

The proposed advanced droop control has also been implemented in a realistic large feeder network. A large utility feeder model is partitioned into 5 different zones with respect to their geological position. An island network is generated in Zone-3. The distribution line parameters, inverter specifications and load details are imported from OpenDSS data into the PLECS simulation. Distribution line parameters include the line impedance of different transformer connections at the primary side as well as the secondary side. Each transformer secondary is connected to the residential loads and inverters. Fig. 2.55 shows the OpenDSS screenshot of the selected island in the utility feeder. PLECS simulation results with the selected 22 inverters and 5 distribution transformers are shown in Fig. 2.56. Due to the different to-grid impedances, the reactive power was not shared equally. The reactive power difference

among the 22 inverters can be as large as 1 kVAr. The proposed advanced droop control by changing the slope of $Q - V$ droop curve has been activated as shown by the red dash line. The reactive power of each inverter finally reaches the same per unit value.

Figure 2.55: Screenshot Of Zone-3 Subsection Of Utility Feeder With Islanded Network

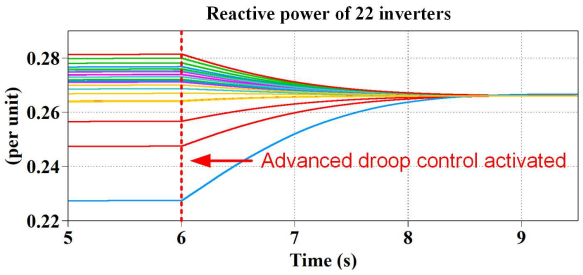


Figure 2.56: Simulation Results Of Reactive Power Among 22 Inverters With Advanced Droop Control Activated

2.7 Conclusions

In this chapter, PV and energy storage devices have been modeled for simulation purposes. In order to smooth PV output power, energy storage devices have been implemented to compensate the power different between the source and the load. The supercapacitors and batteries have been controlled to respond to only high-frequency current command and low-frequency command, respectively. The control strategies for grid-connected DER inverter have been designed according to the requirements

from IEEE 1547 Standard. Under normal operation, a unified P control is proposed so that the DC bus voltage is always controlled by the DC/AC stage under either grid-connected or standalone operation. The current controllers in the DC/AC stage can also be kept the same. To meet the current THD requirement for grid-connection, a repetitive controller has been implemented to suppress harmonic currents from all orders. Under large variation of grid impedance, traditional PI and PR controllers experience limit stability margin. Grid-connected DER inverters should be able to detect unintentional islanding and cease to energize the system. A SOGI based active anti-islanding protection method has been proposed such that islanding can be detected even in the NDZ. A simple LVRT control strategy has been realized for a three-phase unbalanced system. Both positive and negative sequency currents are controlled independently. For paralleled DER inverters in standalone operation, it turns out that the supervisory control is able to bring the grid frequency and voltage back to their rated value even after a load step change. The droop control is able to automatically achieve power sharing among different inverters. With the help of system communication, an advanced droop control is capable of tunning the slope of the Q-V droop curve in order to achieve reactive power sharing even when the grid impedance is not inversely proportional to the rating of the respective inverter.

Chapter 3

AN AUTOMATED ROBUST H-INFINITY CONTROLLER DESIGN USING PARETO FRONT OPTIMIZATION FOR A SINGLE-PHASE GRID-CONNECTED INVERTER

3.1 Introduction

Grid-connected power electronic converters are increasingly required to provide a wide range of voltage and frequency support for modern power systems [51, 52]. However, the complex control loops and the output filters of the power converters bring more complicated dynamics in a wide frequency range to the grid, which adds more challenges to the stability of the power system [53]. For example, grid-connected inverters are required to inject stable and high-quality current at the Point of Common-Coupling (PCC) under different grid impedances. The variable grid impedance can be due to different feeder types of the network and different locations of inverter interconnection. A significant grid impedance variation will have a big impact on the performance of the current control in terms of stability [54–59]. The unstable operation brought by this impedance uncertainty must be mitigated by designing a current controller which is not only robust to the grid impedance variation but also capable of meeting the requirements of power regulation and high power quality.

A PI controller is commonly used in grid-connected applications due to its simplicity and easy implementation [54, 60, 61]. However, it is not a good candidate for single-phase systems because of the large steady-state error at 60 Hz when the proportional gain is low and the small stability margin when the gain is increased. A PR controller is usually used in single-phase as well as three-phase systems, and

it can achieve a small steady-state error at 60 Hz due to the large resonant peak at the same frequency [62–65]. However, it is challenging to design a PR controller with enough stability margin and good dynamic performance under a large grid impedance variation [55]. H-infinity controllers were proposed to address the stability problem caused by model uncertainty [66]. A prespecified degree of robustness and tracking error to model uncertainty can be ensured by shaping the systems closed-loop transfer function with appropriate weighting functions [67–70]. Designing a robust H-infinity controller then becomes a problem in choosing loop-shaping weighting functions. The synthesized H-infinity controller is able to provide tolerance on the predefined model uncertainty as large as possible.

The robust H-infinity control concept has been implemented in various publications. [71, 72] implemented an H-infinity robust control scheme to regulate inverter output voltage in islanded micro-grids. However, only a simple L filter was considered at the inverter output. The high-frequency instability will not be indicated in this situation. [51] proposed an H-infinity controller for grid-connected converters with LCL output filters. However, the proposed control strategy was trying to regulate the inverter output current instead of the grid current. In this way, the control plant became a simple 1st order system. However, from the system point of view, a parallel resonant path was created by the filter capacitor and the grid side inductor. High-frequency oscillation could be induced in the grid current if the harmonics from inverter output were close to the resonant frequency [54]. [73, 74] implemented a robust H-infinity controller to multimachine power systems such as distributed synchronous generators and asynchronous motors in electric trains. The analysis was based on the linearization of the model around different operating points. The modeling error due to this approximation was considered to be the perturbation that would be compensated by the designed H-infinity controller. [75] extended this concept to a three-phase voltage

source converter. However, system parameter variation was not considered as the disturbance to the controller, and only simulation results were provided. [67] proposed a robust H-infinity loop-shaping voltage controller for single-phase UPS inverters. The designed controller was able to keep stable and low THD output voltage under load variation. In [54], the grid impedance uncertainty was taken care of by a robust H-infinity controller. The results showed superior performance of the H-infinity controller over the conventional PI controller for a three-phase grid-connected voltage source converter. However, the weighting functions used in [54, 67] were directly given without further explaining why the authors selected those coefficients. Especially in [67], the weighting function that was used to shape the systems closed-loop transfer function had a tight bound over the model uncertainty and low magnitude at high-frequency. This would lead to insufficient attenuation for high-frequency noise. [54] implemented an order reduction for easier digital implementation after the original controller was synthesized. Revalidation of the stability and disturbance rejection capability using the new controller was missing. Furthermore, [54] only showed the results under two different grid impedances, and the variation range was relatively small.

This chapter aims to, firstly, provide a deep understanding of the design objectives for a robust H-infinity controller. Instead of deriving tedious matrix equations as in the previous literature, a geometric representation of the robust stability is presented in this study, and the robust performance is explained using a frequency-dependent constraint. Secondly, an automated design procedure is proposed to intelligently select the weighting function coefficients for controller synthesis. Thirdly, instead of randomly choosing the controller as shown in the previous work, the Pareto Front technique has been implemented in this work to select an optimal controller among all the candidates. The multiobjective optimization using Pareto Front has been

introduced in [76–78]. The advantage of this method is that it does not need to weight the optimization objectives in advance [79]. This technique is suitable for this grid-connected application where a small steady-state error and a large phase margin are simultaneously desired, but the priority of the two objectives is not known. Last but not least, the proposed automated H-infinity controller design and Pareto Front based optimization process are generalized methodologies and can be applied to other applications where model uncertainty needs to be considered.

The remainder of the chapter is organized as follows: Section 3.2 reviews and explains the two design objectives of an H-infinity controller, namely the robust stability and robust performance. The detailed H-infinity controller design process including the weighting function selection is provided in Section 3.3. Section 3.4 presents the controller optimization process using Pareto Front. PLECS simulation results and hardware experimental results are shown in Section 6.6 and 6.7, respectively.

3.2 Review of H-infinity Robust Control Design Objectives

3.2.1 Introduction

In order to evaluate the controller performance in terms of stability, steady-state error and disturbance rejection, various transfer functions such as the closed-loop transfer function and the error to output transfer function of the system need to be derived using the system model. Fig. 3.1 shows a typical feedback control system configuration, including the process disturbance and measurement noise. The system model is represented by a nominal plant and a multiplicative uncertainty. $R(s)$ represents the reference. $E(s)$ is the error between the reference and feedback signals. $U(s)$ is the controller output. $\Delta G(s)$ is the multiplicative plant uncertainty. $G_N(s)$ is the nominal plant. $G(s)$ represents the entire plant transfer function. $D(s)$ is the

process disturbance. $Y(s)$ is the system output. $N(s)$ is the measurement noise. As a result, the system output $Y(s)$ and error $E(s)$ can be derived as,

$$Y(s) = \frac{G(s)C(s)}{1 + G(s)C(s)}(R(s) - N(s)) + \frac{1}{1 + G(s)C(s)}D(s) \tag{3.1}$$

$$E(s) = \frac{1}{1 + G(s)C(s)}(R(s) - D(s)) + \frac{G(s)C(s)}{1 + G(s)C(s)}N(s) \tag{3.2}$$

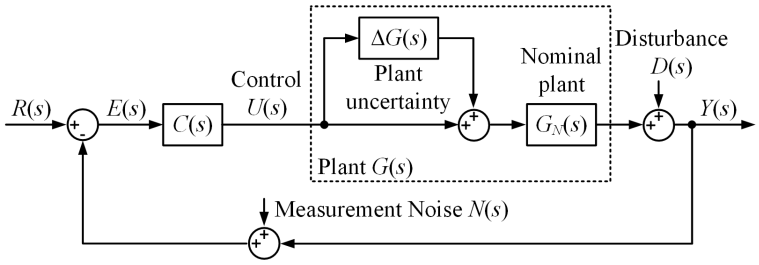


Figure 3.1: A Typical Feedback Control System Configuration

The sensitivity function $S(s)$ and complementary sensitivity function $T(s)$ are defined as follows,

$$S(s) = \frac{1}{1 + G(s)C(s)} \tag{3.3}$$

$$T(s) = \frac{G(s)C(s)}{1 + G(s)C(s)} \tag{3.4}$$

It is obvious that the following relationship holds true for the entire frequency range.

$$S(s) + T(s) = 1 \tag{3.5}$$

By substituting (3.3) and (3.4) into (3.1) and (3.2), we have

$$Y(s) = T(s)(R(s) - N(s)) + S(s)D(s) \tag{3.6}$$

$$E(s) = S(s)(R(s) - D(s)) + T(s)N(s) \tag{3.7}$$

The following conclusions can be made based on (3.6) and (3.7). Firstly, in order to have a small steady-state error, $S(s)$ should be close to 0 at the frequency of interest since $S(s)$ is the reference-to-error transfer function. Based on (3.5), $T(s)$ will be close to 1, which provides the system with a good tracking performance since $T(s)$ is the reference-to-output transfer function. Secondly, $S(s)$ should be close to 0 to reject process disturbance at the frequency of interest since $S(s)$ is also the disturbance-to-output transfer function. Thirdly, $T(s)$ should be close to 0 to attenuate noise at the frequency of interest since $T(s)$ is also the noise-to-output transfer function. These three conclusions help us to define the overall shape of the two sensitivity functions. Take the grid-connected application as an example. The injected grid current is required to be controlled to have a small steady-state error at the fundamental frequency. The disturbance is assumed to be from the grid side and is mainly at 60 Hz. However, the noise is concentrated primarily in the high-frequency range. As a result, $S(s)$ should be close to 0 at 60 Hz to have a small steady-state error and good disturbance rejection capability at 60 Hz. $T(s)$ should be close to 0 at high frequency to attenuate the noise. Note that $S(s)$ and $T(s)$ are always constrained by (3.5). Then $S(s)$ will be close to 1 at high frequency, and $T(s)$ will be close to 1 at 60 Hz.

The loop-shaping based robust H-infinity controller design needs to achieve two

design objectives by selecting appropriate weighting functions to shape $S(s)$ and $T(s)$ such that they have desired gains at different frequencies.

3.2.2 Design Objective 1: Robust Stability

The robust stability requires that the system can achieve stable operation under all uncertainty. In this section, the robust stability criterion will be derived using a geometric method and the Nyquist plot of the open-loop transfer function. There will be multiple stability criteria considering system parameter uncertainty. However, a weighting function which covers all model uncertainty can be used so that a single criterion can be derived.

Recall the multiplicative plant uncertainty shown in Fig. 3.1. It is a normalized uncertainty and can be expressed as

$$\Delta G(s) = \frac{G(s) - G_N(s)}{G_N(s)} \tag{3.8}$$

The robust stability design objective will be explained by using the Nyquist plot. Assume we select a weighting function $W_T(s)$ that bounds all the system uncertainty. Then the following relationship holds true.

$$|W_T(s)| > \left| \frac{G(s) - G_N(s)}{G_N(s)} \right| \tag{3.9}$$

By multiplying the controller transfer function $C(s)$ to both the numerator and denominator on the right-hand side of (3.9), we have

$$|W_T(s)| > \left| \frac{C(s)G(s) - C(s)G_N(s)}{C(s)G_N(s)} \right| \tag{3.10}$$

The product of controller and plant transfer functions is the systems open-loop transfer function assuming a unity feedback loop. Let $G_{op}(s)$ and $G_{opN}(s)$ be the actual open-loop transfer function and the nominal open-loop transfer function, respectively. (3.10) can be rewritten as

$$|G_{opN}(s) \cdot W_T(s)| > |G_{op}(s) - G_{opN}(s)| \tag{3.11}$$

The Nyquist plot is drawn based on the systems open-loop transfer function. As shown in Fig. 3.2, when the plant parameter changes, $|G_{op}(s) - G_{opN}(s)|$ represents the distance between the point on the actual system Nyquist plot and the point on the nominal system Nyquist plot. Since $W_T(s)$ bounds all system variation, regardless of the system parameter change, the actual Nyquist plot will always be within the circle with a center of $G_{opN}(s)$ and a radius of $|G_{opN}(s) \cdot W_T(s)|$. The robust stability requires that the point (-1, 0) is always on the left-hand side of the Nyquist contour. As shown in Fig. 3.3, after mapping all the Right-Half-Plane (RHP) points (represented by the green dashed lines in Fig. 3.3(a)) to the Nyquist plane, these points are always on the right-hand side of the contour (represented by the green dashed lines in Fig. 3.3(b)). Then all the Left-Half-Plane (LHP) points are mapped to the left-hand side of the contour as represented by the red dashed lines in Fig. 3.3(a) and (b). If the point (-1, 0) is in the green area, this means that there is a RHP solution making the open-loop transfer function equal to -1, which makes the system unstable. Therefore, the point (-1, 0) must always be in the red area, as shown in Fig. 3.3(b).

This criterion can be guaranteed as long as the dashed circle in Fig. 3.2 does not include the point (-1, 0). From a geometric point of view, the robust stability criterion is equivalent to that the distance between (-1, 0) and the center of the circle should be greater than the radius. As shown in Fig. 3.2, the following relationship

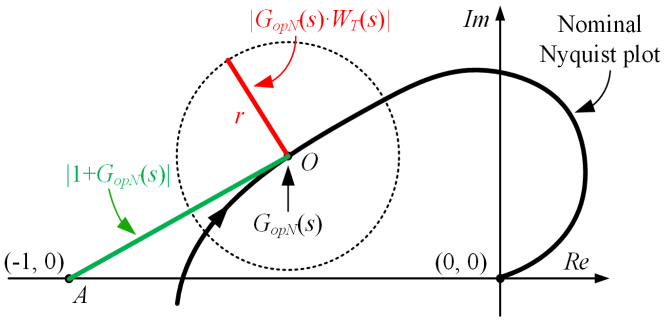
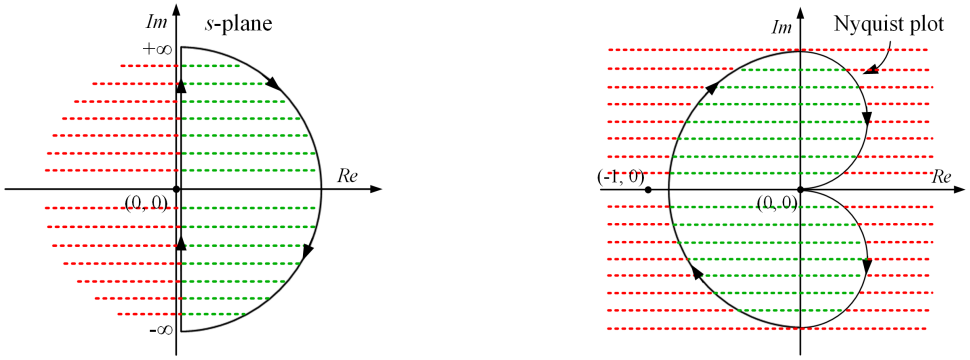


Figure 3.2: Geometric Representation Of The Robust Stability Criterion For H-infinity Controller Design



(a) (b)

Figure 3.3: Geometric Representation Of The Nyquist Stability Criterion: (a) s-plane; (b) Nyquist Plot

must be satisfied.

$$r < |OA| \tag{3.12}$$

As a result,

$$|G_{opN}(s) \cdot W_T(s)| < |1 + G_{opN}(s)| \tag{3.13}$$

$$\left| \frac{G_{opN}(s)}{1 + G_{opN}(s)} \cdot W_T(s) \right| < 1 \tag{3.14}$$

Define a nominal complementary sensitivity function $T_N(s)$ as

$$T_N(s) = \frac{G_{opN}(s)}{1 + G_{opN}(s)} \tag{3.15}$$

Then 3.14 can be rewritten as

$$|T_N(s) \cdot W_T(s)| < 1 \tag{3.16}$$

(3.16) is the robust stability criterion for the H-infinity controller design.

3.2.3 Design Objective 2: Robust Performance

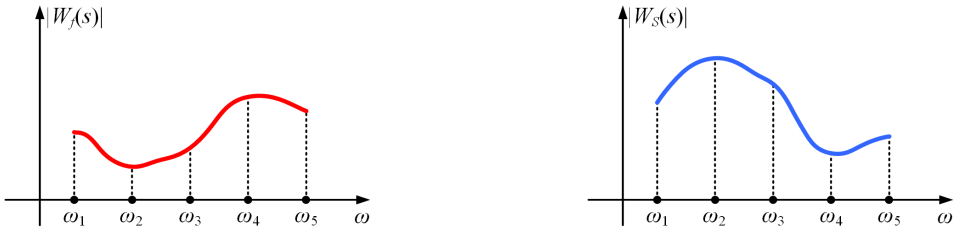
The robust performance requires that the error to output gain is less than a certain value under respective frequencies for all system parameter variations. As a result, the sensitivity function $S(s)$ needs to have desired gains at different frequency intervals, which can be represented as

$$|S(s)| < |W_f(s)| \tag{3.17}$$

where $W_f(s)$ is a frequency-dependent constraint and limits the gain of the sensitivity function at important intervals of the frequency spectrum, as shown in Fig. 3.4(a) [66]. Clearly, $W_f(s)$ puts a performance boundary on the sensitivity function. In order to uniform the design objectives, the above relationship can be reorganized as

$$|S(s) \cdot W_S(s)| < 1 \tag{3.18}$$

where $W_S(s)$ is just a weighting function representing the reciprocal of $W_f(s)$, as shown in Fig. 3.4(b). (3.18) is the robust performance criterion for the H-infinity controller design. In general, the sensitivity function $S(s)$ should have a small gain at the corresponding frequency to reach a small steady-state error and to have a small gain at disturbance frequencies. Therefore, the weighting function $W_S(s)$ should have a sufficient gain at these frequencies based on (3.18).



(a) (b)

Figure 3.4: (a) An Example Of The Performance Bound Function $W_f(s)$; (b) An Example Of The Robust Performance Weighting Function $W_S(s)$

3.2.4 Summary

The robust H-infinity controller design principle can be performed after understanding the aforementioned design objectives. The basic idea is to select proper weighting functions, $W_T(s)$ and $W_S(s)$, to shape the sensitivity function $S(s)$ and the complementary sensitivity function $T(s)$ such that (3.16) and (3.18) are satisfied.

3.3 Automated H-infinity Controller Design For A Single-phase Grid-connected Inverter

3.3.1 System Modeling

Fig. 3.5 shows the circuit topology of a single-phase H-bridge voltage source inverter. S_1, S_2, S_3, and S_4 are the four IGBT switches. L_{f1} and L_{f2} are the two inductors of the LCL filter at the inverter output. C_f is the capacitor of the LCL

filter. L_g and r_g represents the grid impedance. V_{DC} represents the DC bus voltage. i_{Lf} and i_g are the inverter output current and grid current, respectively. v_{cf} is the voltage across the filter capacitor C_f. v_g is the voltage at PCC and is considered as the measured grid voltage. Table 3.1 shows the key parameters of the inverter. Grid impedance variation is considered as the perturbation that needs to be compensated by the robust H-infinity controller. The nominal impedance value is based on a realistic feeder model provided by a local utility company. The variation range is assumed to be from 0.1 per unit to 10 per unit. Fig. 3.6 shows the corresponding control block diagram. i_g^* is the grid current reference. e is the current error input of the controller. $K_{H\infty}(s)$ represents the H-infinity controller transfer function. v_{inv}^* is the inverter output voltage reference. The plant transfer function is 3^{rd} order since the grid current is chosen as the control object. A repetitive controller can be implemented in parallel with the robust H-infinity controller to mitigate the harmonic current induced by the deadtime in the PWM switching, as presented in [24, 80, 81].

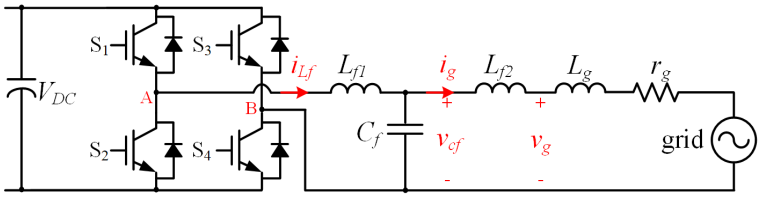


Figure 3.5: A Single-phase H-bridge Voltage Source Inverter

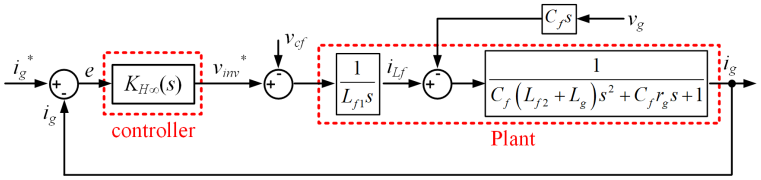


Figure 3.6: The Control Block Diagram Of The Proposed Robust H-infinity Control

Table 3.1: Key Parameters Of The Single-phase Inverter System

Parameters	**Values**
Grid voltage	240 V_{RMS}
DC link voltage	400 V
Grid frequency	60 Hz
Filter inductance L_{f1}	2.24 mH
Filter capacitance C_f	9.4 μF
Filter inductance L_{f2}	116 μH
Nominal grid inductance L_g	80 μH
Nominal grid resistance r_g	22.5 mΩ
L_g variation range	[8, 800] μH
r_g variation range	[2.25, 225] mΩ
Switching frequency	18 kHz
Deadtime	1 μs

3.3.2 Weighting Function Selection

Two basic rules should be considered before selecting individual weighting functions. Firstly, all the weighting functions must be proper transfer functions, which means the degree of the numerator does not exceed the degree of the denominator. Otherwise, errors will occur during controller synthesis in MATLAB. Secondly, we should keep the order of the weighting functions as low as possible. The order of the controller is the sum of the order of the plant and all the weighting functions. The order of the resulting controller is usually greater than 6. Then controller order reduction is required to reduce the dependency on the controller parameter accuracy. The original controller should be kept as low-order as possible so that the difference brought by the order reduction can be minimized.

(a) **Selection of $W_T(s)$** The weighting function $W_T(s)$ determines the robust stability as well as high-frequency noise rejection capability. As mentioned in the previous section, $W_T(s)$ should be able to bound all system uncertainty in order to ensure the robust stability. Based on (3.8), the singular value of the model uncertainty has been plotted in Fig. 3.7 for the entire grid impedance variation range. The red dashed curve shows the upper envelope of all uncertainty curves. As a result, $W_T(s)$ must be chosen such that its singular value is always higher than the envelope. The shape of a satisfying $W_T(s)$ is also shown in Fig. 3.7. The transfer function of the weighting function can be automatically generated using the MATLAB function makeweight which is specifically designed for creating weighting functions with a monotonic gain profile in the robust controller design process. The following key parameters must be specified when using this

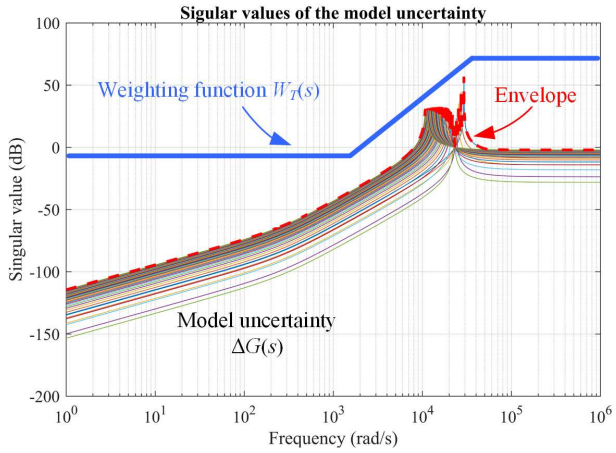


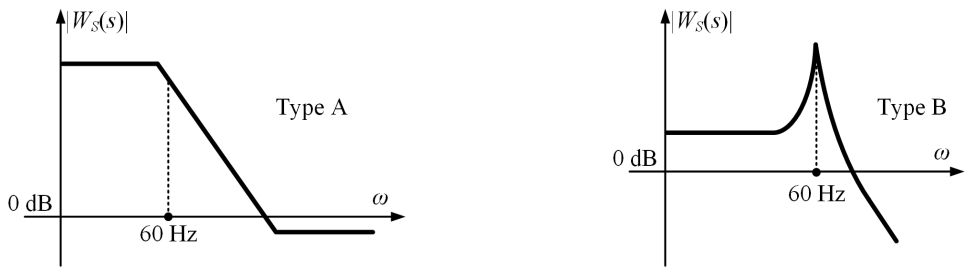
Figure 3.7: The Singular Values Of The Model Uncertainty Over The Entire Grid Impedance Variation Range

function. **(i) Low-frequency gain:** The singular value of $W_T(s)$ at low frequency should be less than 0 dB. From (3.16), it is easy to derive the following relationship.

$$|T_N(s)| < |W_T(s)|^{-1} \tag{3.19}$$

That is to say, the magnitude of the nominal complementary sensitivity function is always below that of the reciprocal of $W_T(s)$. A positive low-frequency gain of $W_T(s)$ leads to a negative gain of $W_T^{-1}(s)$. Therefore, $T_N(s)$ will have a more negative gain. Recall that $T_N(s)$ needs to be close to 0 dB at low frequencies in order to have a good tracking performance. This is only achievable when $W_T(s)$ has a negative low-frequency gain. In this design, we select a small gain of 0.1 (-20 dB) for $W_T(s)$. **(ii) Crossover frequency:** As shown in Fig. 3.7, the crossover frequency of $W_T(s)$ should be smaller than that of the uncertainty envelope to ensure that $W_T(s)$ bounds all model uncertainty. In this automated design, the crossover frequency varies from 0.1 times to 0.6 times the crossover frequency of the uncertainty envelope. **(iii) High-frequency gain:** The magnitude of $W_T(s)$ at high frequency should be very large, which is equivalent to a very small high-frequency gain of $T_N(s)$. In this way, the high-frequency noise can be effectively attenuated. In this design, the high-frequency gain is selected as 200, which is way higher than the peak of the envelope. **(iv) Order of the weighting function:** Only 2^{nd} order and 3^{rd} order weighting functions will be considered in order to keep a low controller order.

(b) **Selection of** $W_S(s)$ The weighting function $W_S(s)$ determines the steady-state error and disturbance rejection capability. In this particular design, $W_S(s)$ needs to have a large gain at the fundamental frequency to achieve a small steady-state error and to reject 60 Hz disturbance. In addition, it should have some positive gain at DC so that DC offset can be eliminated in the single-phase system. Two possible shapes of $W_S(s)$ are shown in Fig. 3.8. Since Type A weighting function has a monotonic profile, the MATLAB function makeweight can also be used to get its transfer function. Two characteristics of Type A



(a) (b)

Figure 3.8: Two Possible Shapes Of The Weighting Function $W_S(s)$

weighting function $W_S(s)$ should be pointed out. The first is that a high DC gain is automatically guaranteed since the gain at 60 Hz is forced to be high. The second is that the high-frequency gain should be less than 0 dB such that the sensitivity function $S(s)$ is able to be close to 1 at high-frequency based on the following relationship.

$$|S(s)| < |W_S(s)|^{-1} \tag{3.20}$$

As a result, the magnitude of $T(s)$ is forced to be low so that high-frequency noise can be attenuated.

The expression for a Type B weighting function is

$$W_S(s) = \frac{k\omega_0^2}{s^2 + 2\xi\omega_0 s + \omega_0^2} \tag{3.21}$$

From Fig. 3.8(b), the weighting function has a large resonant peak at resonant frequency ω_0. In this design, ω_0 is selected to be 377 rad/s, which ensures a small steady-state error and enough 60-Hz disturbance rejection capability. Also, a positive k will give us some positive DC gain and provide some DC offset suppression capability.

Another important point must be taken into consideration when selecting the weighting function $W_S(s)$. The crossover frequency of $W_S(s)$ must be lower

than that of $W_T(s)$. This can be easily explained by using Fig. 3.9 where ω_{cS} and ω_{cT} are the crossover frequencies of $S(s)$ and $T(s)$, respectively. If ω_{cS} is less than ω_{cT}, (3.5) can be easily achieved between the two crossover frequencies since both $S(s)$ and $T(s)$ can be either small or large. However, if ω_{cS} is larger than ω_{cT}, as shown in Fig. 3.9(b), both $S(s)$ and $T(s)$ can only have small values between the two frequencies. Then (3.5) will be violated. As a result, the weighting function $W_S(s)$ should have a low crossover frequency as much as possible. Based on this criterion, Type B weighting function is more suitable since the crossover frequency can be easily brought down by the resonant peak, and the order of this weighting function is only 2. In order to reach the same low crossover frequency, the order of Type A function would be very high, which does not satisfy the basic rules introduced at the beginning of this section.

In this automated design, we would like to have the steady-state error of the grid current to be less than 1%. As a result, $W_S(s)$ should be greater than or equal to 100 at 60 Hz. This leads to

$$\frac{k}{2\xi} = 100 \tag{3.22}$$

In addition, the coefficient k should be positive so that we can have some DC offset suppression capability. k is then selected to vary between 1 and 10. The detailed automated weighting function selection has been presented in the flow chart, as shown in Fig. 3.10.

3.3.3 Controller Synthesis

As shown in Fig. 3.10, there are three steps to generate the desired H-infinity controller. The first step is to use the MATLAB function mixsyn to synthesize a high-order H-infinity controller. The function needs four inputs which are the nominal

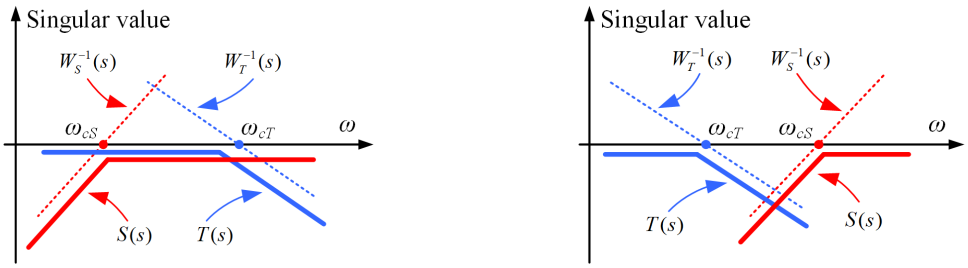


Figure 3.9: Examples Of The Two Weighting Functions And The Associated Sensitivity Functions

plant transfer function, $W_T(s)$, $W_S(s)$, and a weighting function $W_C(s)$ representing the control effort. A small constant is assigned to $W_C(s)$ to ensure that the D_{12} matrix of the augmented plant is of full rank [54]. In the design process, we assume that $W_C(s)$ is between 0 and 1. After the controller is created, the second step is to reduce the order of the transfer function to 3 using the MATLAB function reduce for easier and more reliable digital implementation. The third step is to check the robust stability and robust performance using the new controller, which is one of the major contributions of the proposed automated design procedure and is missing in the previous literature. For the robust stability, it is easy to use MATLAB functions to solve for zeros of the systems closed-loop transfer function for all grid impedances since the controller transfer function is already known. For the robust performance, the new controller should satisfy (3.18) for all grid impedances.

In the automated design, the aforementioned 3 steps will be executed as long as the weighting function parameter changes. As a result, multiple satisfying controllers can be generated. In order to select an optimal controller, optimization must be implemented based on different targets for different applications.

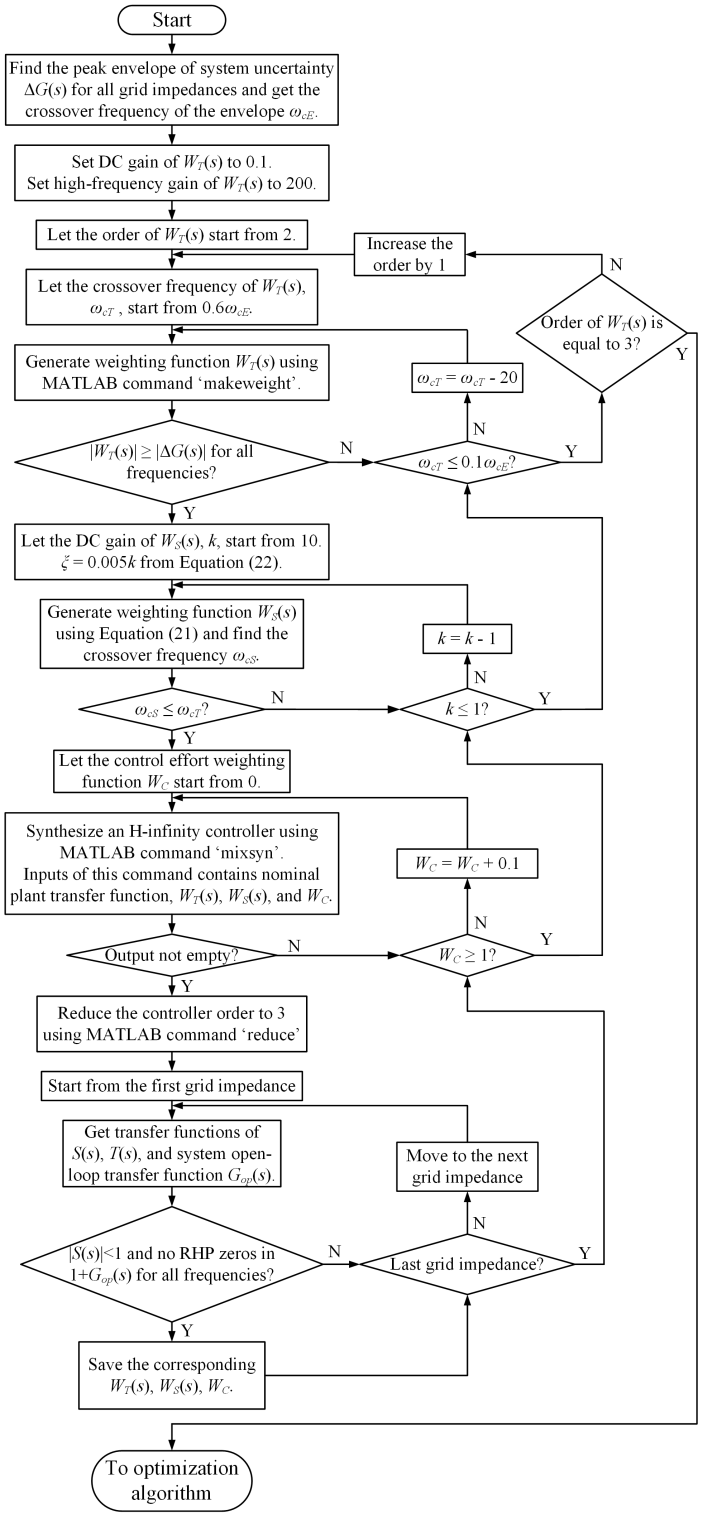


Figure 3.10: The Flow Chart Of The Proposed Automated H-infinity Controller Design Process

3.4 Controller Optimization Using Pareto Front

A straightforward optimization method using Pareto Front has been implemented in this design. The Pareto Front optimization is based on a Design-Space concept, and the priority of the optimization targets does not have to be known in advance. The detailed optimization procedure is shown in Fig. 3.11.

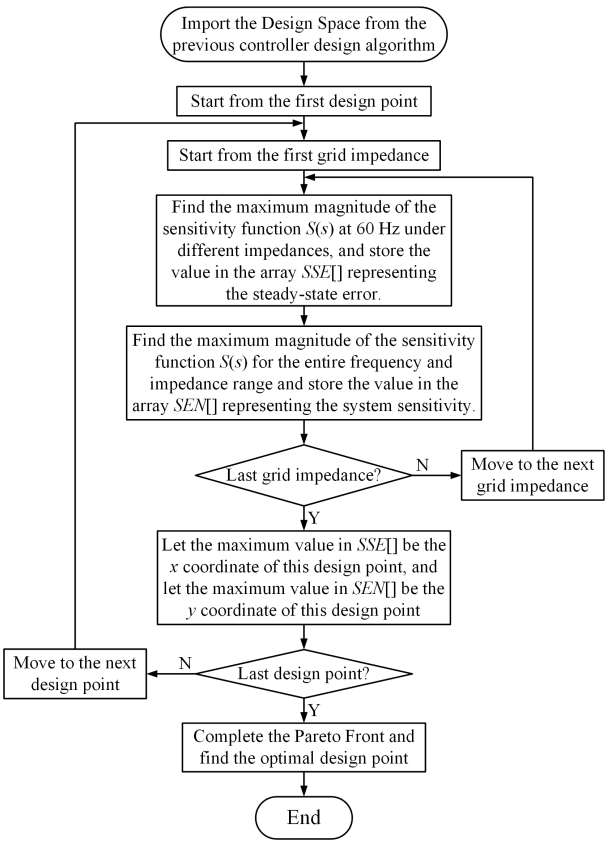


Figure 3.11: The Flow Chart Of The Pareto Front Optimization Process

The first step is to define the Design Space by selecting all satisfying candidates that meet all the design requirements. In this particular design, a two-stage selection has been implemented already in the previous Section 3.3. Stage I is to generate an H-infinity controller for each combination of the three weighting functions where each weighting function has been given at least one variable coefficient. Only the

weighting functions that satisfy both the robust stability and robust performance will be considered. Stage II is to select those controllers which can still fulfill the two design objectives after order reduction. This will exclude some combinations of the weighting functions from Stage I. All the controllers and the associated weighting functions after the two-stage selection are considered as the Design Space.

The second step is to plot the Pareto Front for the selected Design Space and to find an optimal design point. For simplicity, a 2-D Pareto Front will be implemented in this design. As a design example, we have selected the steady-state error at the fundamental frequency and the system sensitivity as the two optimization targets. Let the x-axis be the steady-state error. Then the magnitude of the sensitivity function $S(s)$ at 60 Hz for each H-infinity controller in the Design Space will be calculated for different grid impedances. The maximum value will be plotted in the 2-D Pareto Front. Let the y-axis be the system sensitivity. The distance between the system Nyquist contour and the point (-1, 0) indicates the easiness of becoming unstable and can be expressed as

$$|1 + G_{op}(s)| \tag{3.23}$$

The reciprocal of the above equation is exactly the magnitude of the sensitivity function $S(s)$. A larger sensitivity means a shorter distance to (-1, 0), and the system is more likely to become unstable when unpredictable perturbation occurs. As a result, for each controller in the Design Space, the sensitivity will be computed for the entire grid impedance variation range, and the maximum value will be plotted in the 2-D Pareto Front. The generated Pareto Front is shown in Fig. 3.12. For each controller, when the grid impedance varies, the steady-state error and system sensitivity will always be lower than the values indicated by the corresponding x and

y coordinates, respectively. In Fig. 3.12, the Pareto Front is represented by the thick orange line. For any given steady-state error requirement, the points on the Pareto Front will always have the smallest sensitivity. For any given sensitivity requirement, the points on the Pareto Front will always have the smallest steady-state error. The final design point is selected as shown in Fig. 3.12.

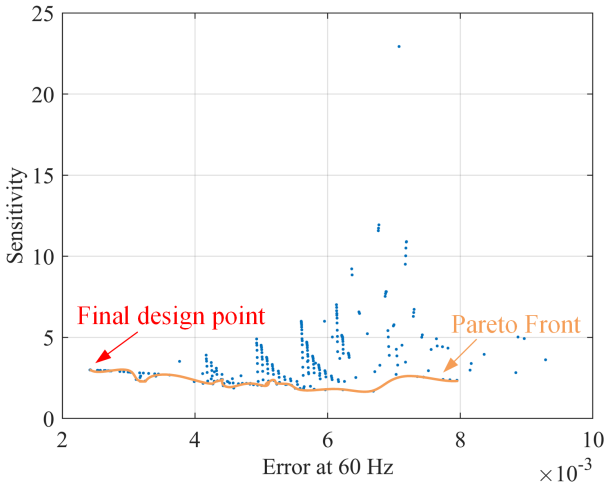


Figure 3.12: The 2-D Pareto Front Plot Considering The Steady-state Error At 60 Hz And The Sensitivity

The transfer function of the H-infinity controller for the selected optimal design point after order reduction is shown below.

$$C(s) = \frac{2664s^2 + 3.510 \times 10^5 s + 6.970 \times 10^7}{s^3 + 563.4s^2 + 1.442 \times 10^5 s + 7.953 \times 10^7} \tag{3.24}$$

Fig. 3.13 shows the singular value of the original H-infinity controller as well as the 3^{rd}-order controller. The resonant peak at 60 Hz has been preserved, whereas the negative peak at high frequency is lost in the low-order controller. Fig. 3.14 shows the singular value of $W_T(s)$, $W_S(s)$, $T(s)$, and $S(s)$ with the 3^{rd}-order controller under the nominal grid impedance. The sensitivity function $S(s)$ has a large negative peak at 60 Hz, ensuring a small steady-state error in the grid current. At the same

frequency, $T(s)$ is equal to 0 dB, which indicates that the grid current output is equal to its reference. In addition, $T(s)$ has a very low gain as frequency increases, which ensures high-frequency noise attenuation capability. Due to the missing negative peak in the original high-order controller, the attenuation at the resonant frequency is not sufficient, and a small resonant peak can still be observed at around 23300 rad/s (3708 Hz).

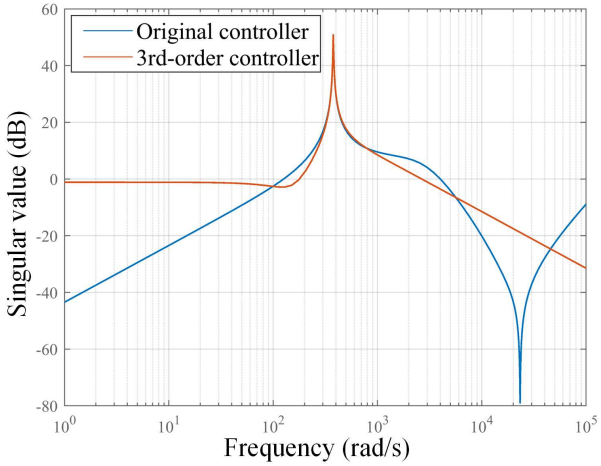


Figure 3.13: The Singular Value Of The Synthesized High-order H-infinity Controller And The Simplified 3^{rd}-order Controller

3.5 Simulation Results

PLECS simulations have been conducted to validate the robust stability of the selected optimal H-infinity controller. In addition, the comparison between the conventional PR controller and the robust H-infinity controller is also presented in this section. The control algorithm is implemented in the "C-script" block in PLECS and will be executed once every switching cycle, which makes the simulation more practical. The controller needs to be discretized as below in order to be implemented digitally.

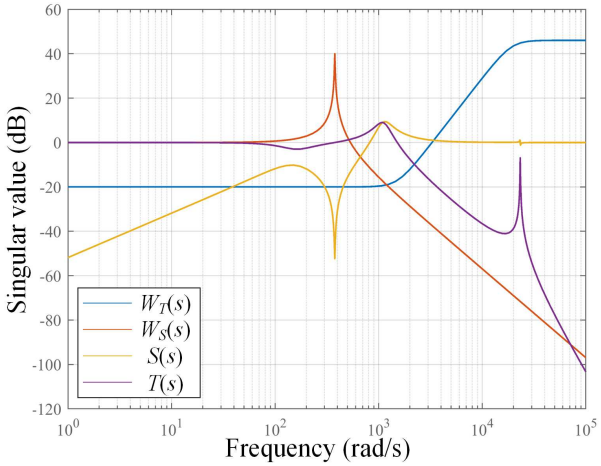


Figure 3.14: The Singular Value Of The Selected Weighting Functions $W_T(s)$ And $W_S(s)$, The Sensitivity Function $S(s)$ And The Complementary Sensitivity Function $T(s)$ Using The 3^{rd}-order Controller And Nominal Grid Impedance

$$C_{re}(z) = \frac{0.0731 - 0.0762z^{-1} - 0.0731z^{-2} + 0.0762z^{-3}}{1 - 2.9687z^{-1} + 2.9379z^{-2} - 0.9692z^{-3}} \tag{3.25}$$

3.5.1 Comparison Between the H-infinity Controller and Traditional PR Controller

The gains for the conventional PR controller are selected as $K_p = 20$ and $K_r = 150$ to get optimal performance in terms of the steady-state error and dynamic response. Fig. 3.15 shows the steady-state error of the grid current for the two controllers under different grid impedances. When the impedance is less than 7 p.u., both controllers have almost the same steady-state error. However, as the impedance increases, the PR controller is not able to keep the system stable. As shown in Fig. 3.16, high-frequency resonance is observed in the grid current waveform for the selected PR controller when the grid impedance increases to 7 p.u.. However, the H-infinity controller is able to stabilize the grid current even under the largest grid impedance (10 p.u.). The Bode plot of the systems open-loop transfer function has been plotted for both controllers

under different grid impedances, as shown in Fig. 3.17 and 3.18. An overall picture is that, compared with the traditional PR controller, the H-infinity controller has more significant attenuation at high frequency, making the high-frequency resonant peak below 0 dB. Then the stability can be verified by looking at the phase angle at the crossover frequency as represented by the red dashed line in Fig. 3.17. However, the Bode plot for the traditional PR controller has multiple crossover frequencies, which makes it difficult to determine the stability. Again, the Nyquist plot is used to verify the stability of the system.

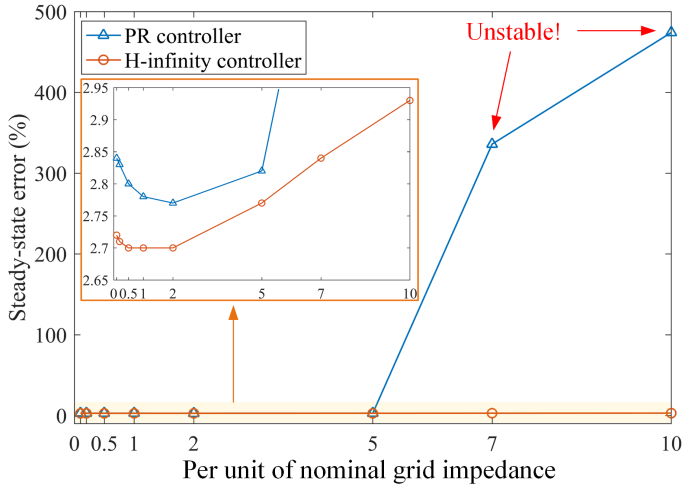


Figure 3.15: The Stead-state Error Of The Grid Current Under Different Grid Impedances Using The H-infinity And PR Controllers

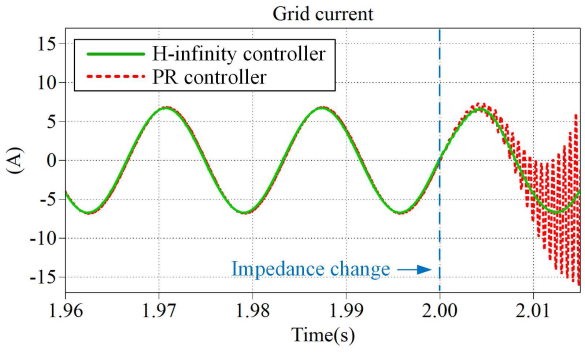


Figure 3.16: Simulated Waveform Of The Grid Current For Both PR And H-infinity Controllers When The Grid Impedance Changes To 7 p.u.

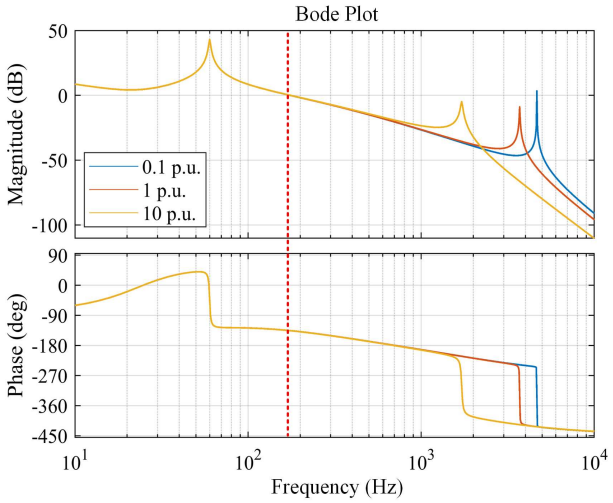


Figure 3.17: The Bode Plot Of The Open-loop Transfer Function Using The Robust H-infinity Controller Under 3 Different Grid Impedances: 0.1 p.u., 1 p.u., And 10 p.u.

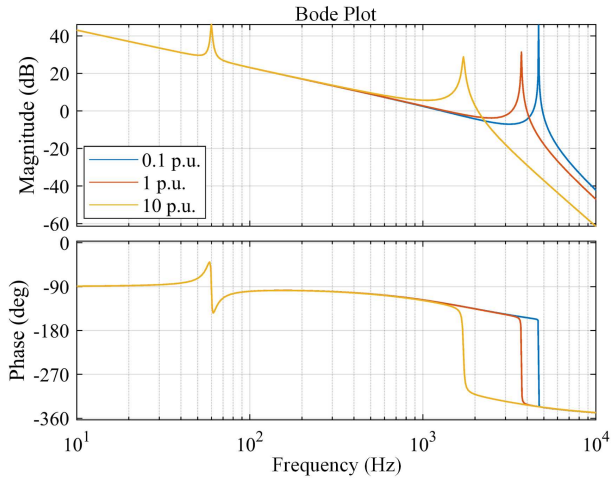


Figure 3.18: The Bode Plot Of The Open-loop Transfer Function Using The Traditional PR Controller Under 3 Different Grid Impedances: 0.1 p.u., 1p.u., And 10 p.u.

The Nyquist plot for each controller under different grid impedances has been constructed to verify system stability. Fig. 3.19 shows the Nyquist plot when using the PR controller under 1 p.u. and 10 p.u. grid impedance, respectively. Fig. 3.20 shows the Nyquist plot when using the proposed H-infinity controller under 1 p.u. and 10 p.u. grid impedance, respectively. For the conventional PR controller, the

(-1, 0) point moves towards the right-hand side of the Nyquist contour when the grid impedance increases, leading to instability of the system. However, for the proposed H-infinity controller, the (-1, 0) point is always on the left-hand side of the contour even under the largest grid impedance, which proves the robust stability of the H-infinity controller.

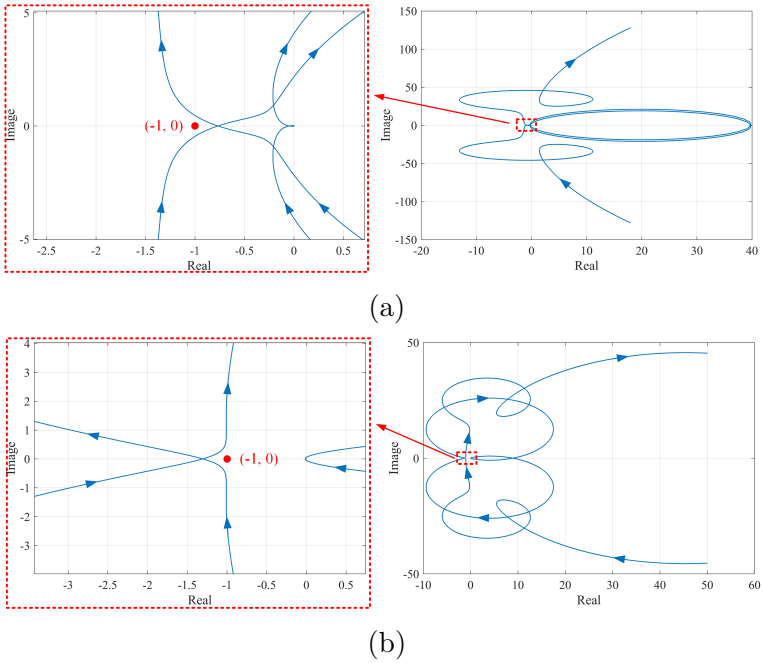
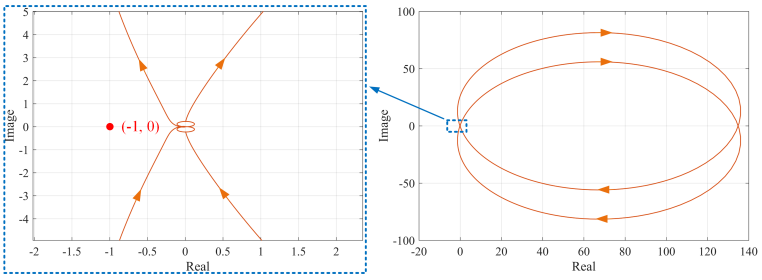
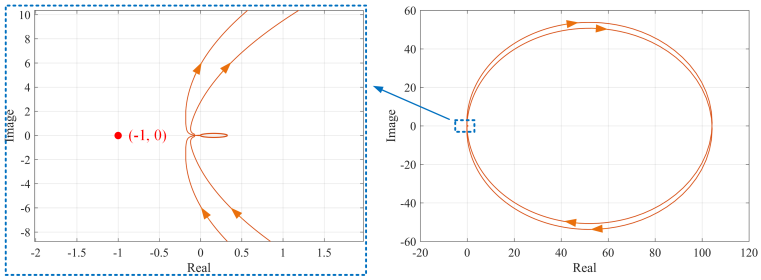


Figure 3.19: The Nyquist Plot When Using A Conventional PR Controller (K_p = 20 and K_r = 150) Under The Grid Impedance Of (a) 1 p.u. And (b) 10 p.u.

It is also possible to make the PR controller stable even under the largest grid impedance by reducing the proportional gain. The proportional gain has been reduced to 1.5 to achieve almost the same sensitivity as the H-infinity controller, as shown in Fig. 3.21. Fig. 3.22 compares the steady-state error between the H-infinity controller and the new PR controller. Even though the PR controller still has a slightly higher error, stability is achieved even at the highest grid impedance. Most importantly, the PR controller with a lower proportional gain leads to a lower bandwidth, which can result in a slower dynamic response compared with the H-infinity controller. The



(a)



(b)

Figure 3.20: The Nyquist Plot When Using The Proposed H-infinity Controller Under The Grid Impedance Of (a) 1 p.u. And (b) 10 p.u.

Bode Plot of the closed-loop transfer function for the two controllers is shown in Fig. 3.23. The bandwidth (the frequency at -3 dB) of the H-infinity controller system is almost 100 Hz higher than that of the PR controller system. Fig. 3.24 shows the PLECS simulation waveform of the grid current at start-up. When the low-gain PR controller is used, the current reaches the steady-state about a fundamental cycle slower than the H-infinity controller.

Another difference between the two closed-loop transfer functions is the noise rejection capability. Note that the closed-loop transfer function is also the noise-to-output transfer function. Additional PLECS simulations have been conducted to evaluate the noise rejection capability of the two controllers at different frequencies. The same amount of noise has been added to the feedback loop simulating the measurement noise. Table 3.2 shows the grid current THD for both controllers under the measurement noise with different frequencies. Fig. 3.25 shows the output current

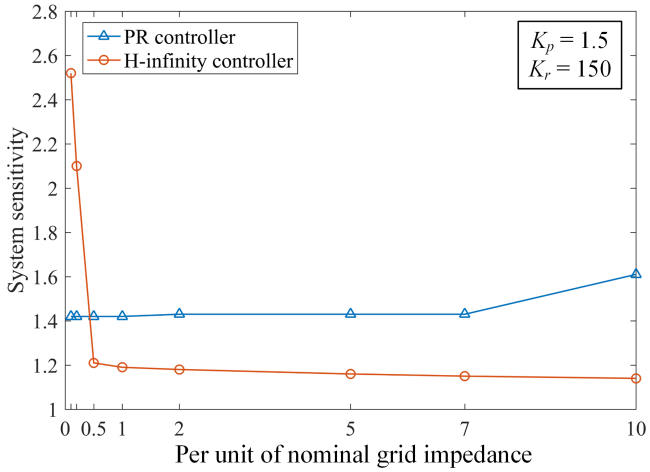


Figure 3.21: The System Sensitivity Comparison Between The H-infinity Controller And The PR Controller With A Lower Proportional Gain Under Different Grid Impedances

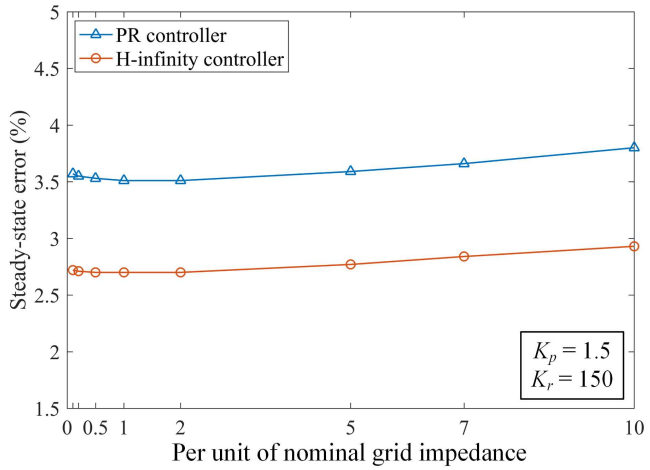


Figure 3.22: The Steady-state Error Comparison Between The H-infinity Controller And The PR Controller With A Lower Proportional Gain Under Different Grid Impedances

waveform of the PR controller and the H-infinity controller when the noise is at 2 kHz. As expected, the H-infinity controller has a better noise rejection compared with the PR controller.

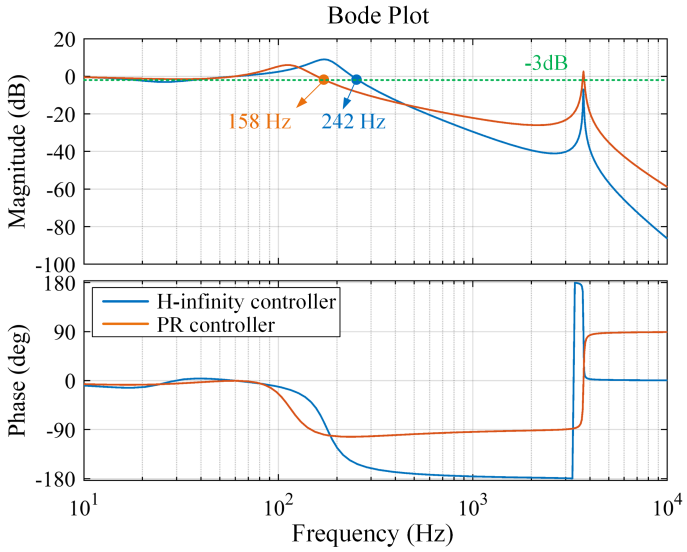


Figure 3.23: The Bode Plot Of The Closed-loop Transfer Function For Both The H-infinity Controller And The PR Controller With Low Proportional Gain

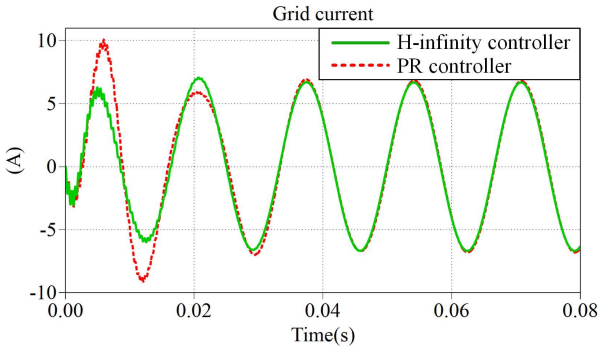


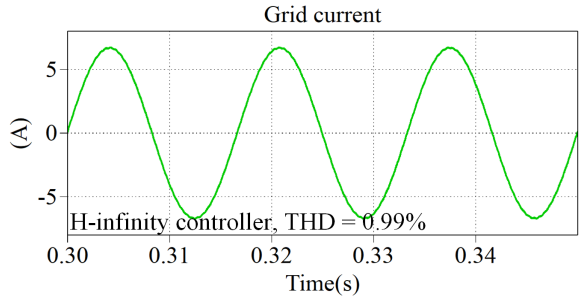
Figure 3.24: Simulated Waveform Of The Grid Current At Start-up For Both The H-infinity Controller And The PR Controller With Low Proportional Gain

3.5.2 Stability Analysis Of The Phase Locked Loop

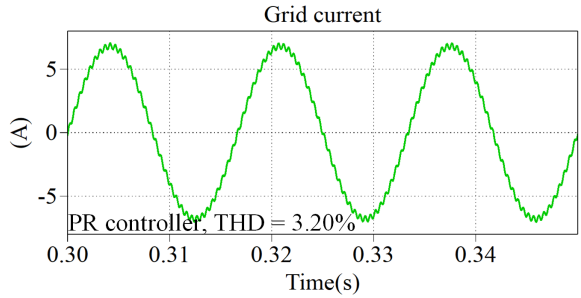
It is important to make sure that the instability after the grid impedance change is not caused by the synchronization block which is known as the Phase-Locked Loop (PLL). When the grid impedance is large enough to form a weak grid, PLL becomes a problem due to the increased coupling between the inverter and grid dynamics which can result in harmonic resonance or even instability [82, 83]. A Second-Order Gen-

Table 3.2: Comparison Of Noise Rejection Capability Between The H-infinity Controller And The PR Controller With A Low Proportional Gain

Frequency of the injected noise	**THD of the grid current**	
	H-infinity controller	PR controller (with low K_p)
1000 Hz	2.37%	5.26%
2000 Hz	0.99%	3.20%
3000 Hz	0.88%	3.70%



(a)



(b)

Figure 3.25: Comparison Of The Noise Rejection Capability At 2 kHz Between The PR Controller With A Low Proportional Gain And The H-infinity Controller: (a) Current Waveform Of The H-infinity Controller; (b) Current Waveform Of The PR Controller

eralized Integrator (SOGI)-PLL has been implemented in this single-phase system. The PLL structure is shown in Fig. 3.26. Fig. 3.27 shows the simulation results of the implemented SOGI-PLL when the PR current controller becomes unstable after the grid impedance increases to 7 times the nominal value at the time of 2.0 s. The

results show that the current loop becomes unstable and high frequency resonance is observed in both grid current and measured grid voltage. However, the implemented SOGI-PLL is stable and the virtual q-axis voltage only has a small ripple (0.8%) due to the filtering capability of the SOGI block as shown in Fig. 3.26. As a result, the instability is caused by the PR current controller instead of PLL. Another straightforward method to extract the angle from the SOGI block is based on the following equation.

$$\theta_{arctan} = arctan(\frac{v_\beta}{v_\alpha}) \tag{3.26}$$

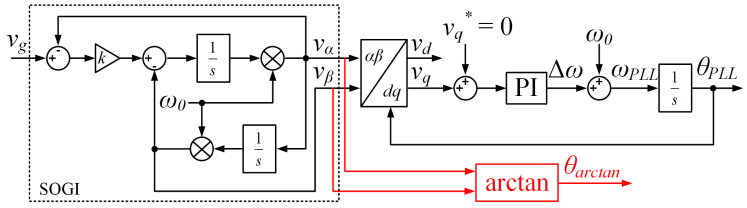


Figure 3.26: Structure Of A Single-phase SOGI-PLL

However, eliminating the PI controller makes this method very sensitive to harmonic voltage. As shown in Fig. 3.28(a), 50% 5^{th} order harmonic has been injected to the input voltage of the PLL. A larger harmonic ripple is observed in the angle from the arctan block compared with that from the PI controller as shown in Fig. 3.28(b). The output angle from the PI controller is almost overlapped with the actual angle of the fundamental voltage. Table 3.3 shows the peak-to-peak angle ripple of the two angle extraction methods under different amount of injected harmonic voltage. It shows that the PI controller is still necessary due to the limited filtering capability of the SOGI block especially on the low-order harmonics. A recent literature [84] has performed a comparative study on 7 different single-phase PLL approaches under different grid conditions including voltage sag, phase angle jump, and distorted

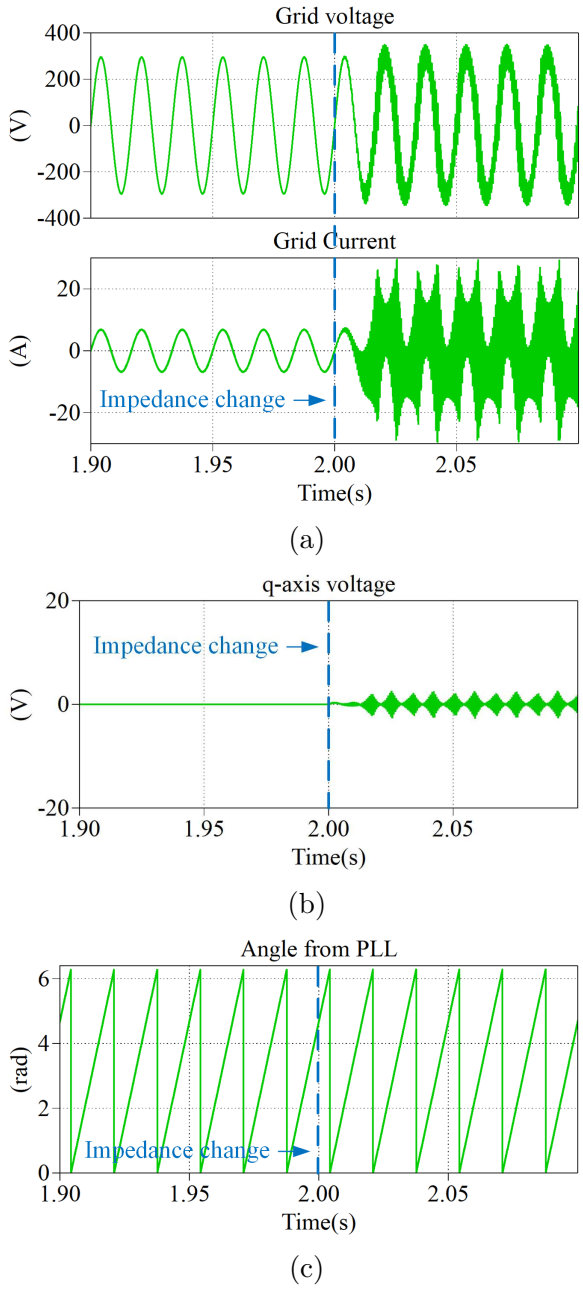
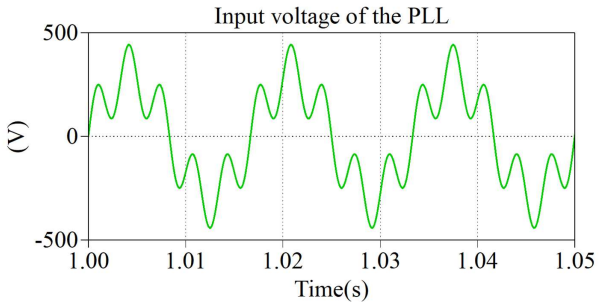


Figure 3.27: Simulation Results Of The Implemented SOGI-PLL: (a) Waveform Of The Measured Grid Voltage And Current; (b) The Virtual q-axis Voltage; (c) Output Angle From The PLL

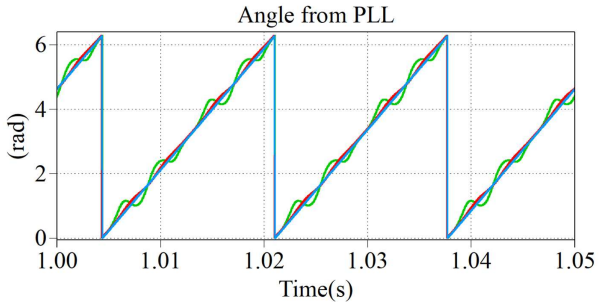
grid voltage (3^{rd} order harmonic injection). It has concluded that the SOGI-PLL has the most satisfactory performance in terms of dynamic response, harmonic rejection, algorithm simplicity, and robustness in a weak grid.

Table 3.3: Comparison Of The Peak-to-peak Angle Ripple Between The Two Angle Extraction Methods Under Different Amount Of Injected Harmonic Voltage

Amount of injected 5^{th} order harmonic	**Peak-to-peak angle ripple (rad)**	
	From arctan	From PI controller
10%	0.24	0.10
20%	0.34	0.16
50%	0.68	0.22



(a)



(b)

Figure 3.28: Comparison Between The Two Angle Extraction Methods. (a) Waveform Of The PLL Input Voltage With 50% 5^{th} Order Harmonic Injected; (b) The Actual Angle Of The Fundamental Voltage (Blue Curve) And The Output Angle From The Arctan Block (Green Curve) And The PI Controller (Red Curve)

3.5.3 Comparison Between the H-infinity Controllers Generated by Different Pareto Fronts

The Pareto Front optimization targets can be changed based on specific applications. In case that harmonic suppression is more critical than steady-state error, the x-axis of the previous Pareto Front plot can be replaced by the error at the harmonic frequency. For example, the harmonic frequency can be selected at 180 Hz which is the primary harmonic frequency due to the deadtime in the PWM switching. As shown in Fig. 3.29, a new Pareto Front has been generated, and the final design point has been selected. The steady-state error and grid current THD have been compared for the two H-infinity controllers. H-infinity controller A is optimized for the steady-state error and H-infinity controller B is optimized for the 3^{rd} order harmonic suppression. Fig. 3.30 shows the steady-state error comparison for the two controllers. H-infinity controller A is selected in terms of the lowest sensitivity and the smallest steady-state error at 60 Hz. H-infinity controller B is selected in terms of the lowest sensitivity and the smallest error at 180 Hz. Both controllers achieve almost the same steady-state error under different grid impedances. This is probably because the error at 60 Hz has already been limited to a very small range using the selected weighting function $W_S(s)$. However, there is a large difference in power quality performance for the two controllers. In the simulation, a 1 μs deadtime is added, and no harmonic compensation method is used in order to observe the 3^{rd} order harmonic suppression capability of the two controllers. As shown in Fig. 3.31, the H-infinity controller B has a much lower THD compared with controller A, which indicates a stronger harmonic attenuation capability of the H-infinity controller B. The result shows that the selected H-infinity controller has a better performance in terms of the respective Pareto Front optimization target.

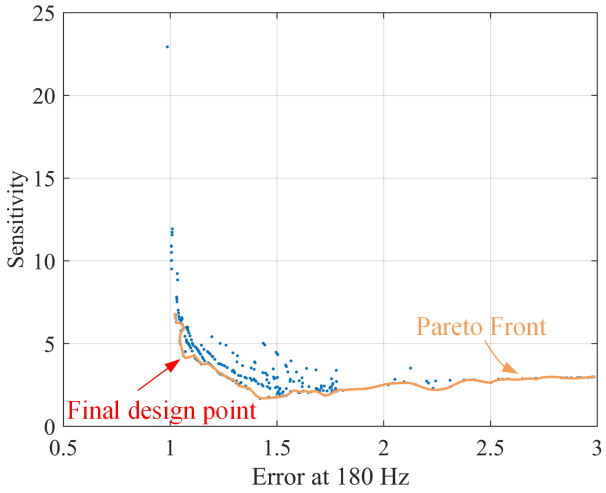


Figure 3.29: The New 2-D Pareto Front Plot Considering The 3^{rd} Order Harmonic Suppression As One Of The Optimization Targets

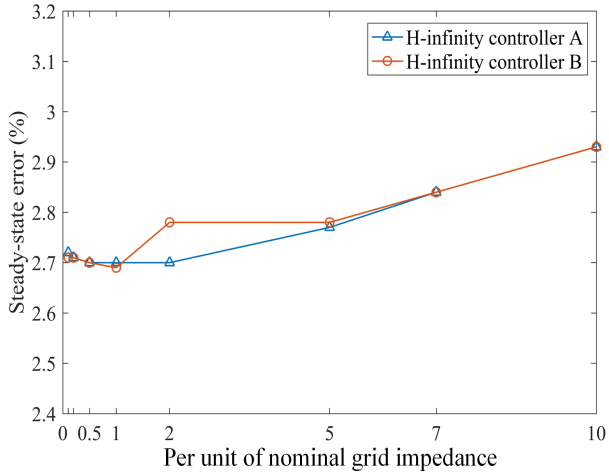


Figure 3.30: Comparison Of The Steady-state Error Between The Two H-infinity Controllers Generated By Different Pareto Fronts Through PLECS Simulations

3.6 Experimental Results

The proposed H-infinity controller has been implemented in a 3 kVA single-phase voltage-source inverter. The inverter output is connected to a Chroma 61800 Series Regenerative Grid Simulator through different inductors and resistors representing the variable grid impedance. Fig. 3.32 shows the inverter prototype. 1 shows the

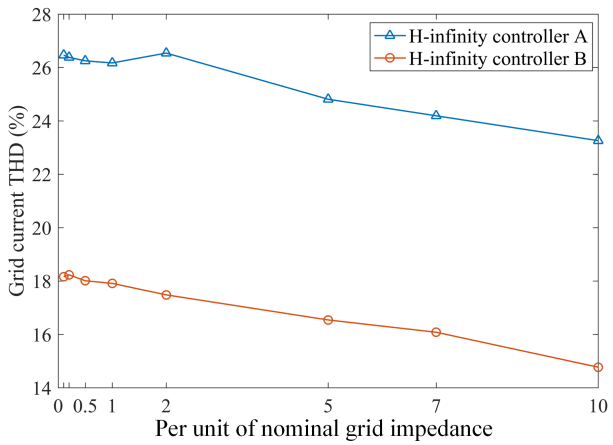


Figure 3.31: Comparison Of The Grid Current THD Between The Two H-infinity Controllers Generated By Different Pareto Fronts Through PLECS Simulations

DC/DC input stage including the DC EMI filters; 2 shows the DC bus; 3 shows the gate driver daughter-boards and the IGBT power modules (on the back); 4 shows the AC output LCL filters; 5 shows the AC EMI filters; 6 shows the DSP board. Both the PR and the H-infinity controllers have been tested under 1 kW unity power factor operating conditions.

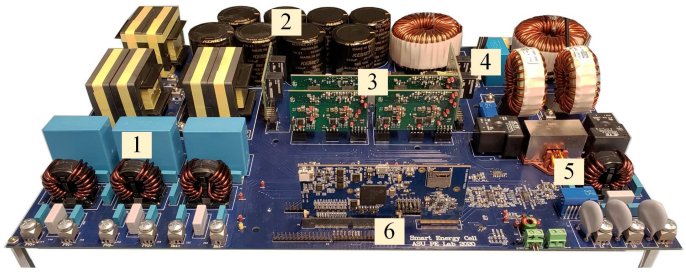
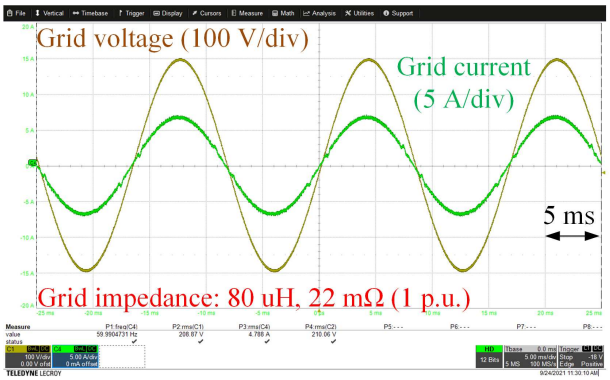


Figure 3.32: A 3 kVA Single-phase Voltage-Source Inverter Prototype

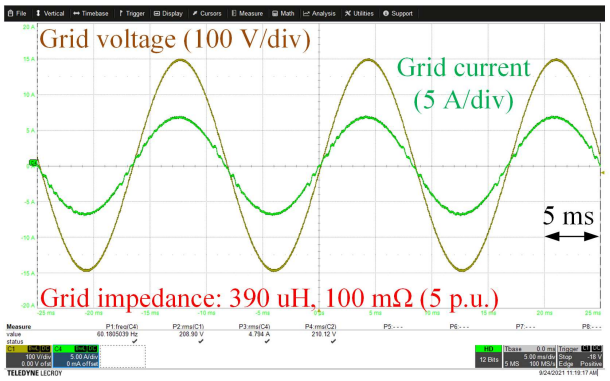
3.6.1 Comparison Between the H-infinity Controller and Traditional PR Controller

Fig. 3.33 shows the experimental results when a PR controller has been implemented. The controller gains are $K_p = 20$ and $K_r = 150$. The grid current is stable

when the grid impedance is less than 7 p.u.. However, as shown in Fig. 3.34(a), the grid current envelope does not converge when the impedance reaches 7 p.u.. High-frequency resonance can be observed in Fig. 3.34(b). Note that the grid voltage is measured before the grid impedance, which explains why the resonance also exists in the voltage waveform.



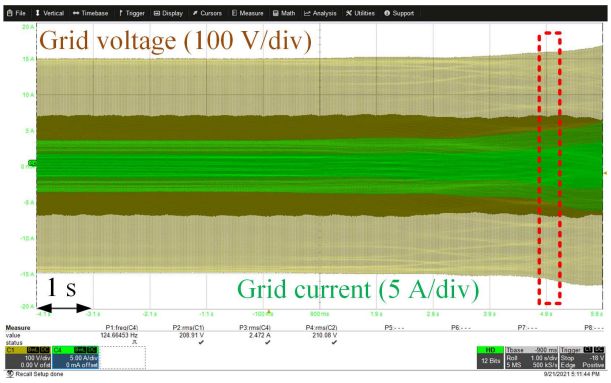
(a)



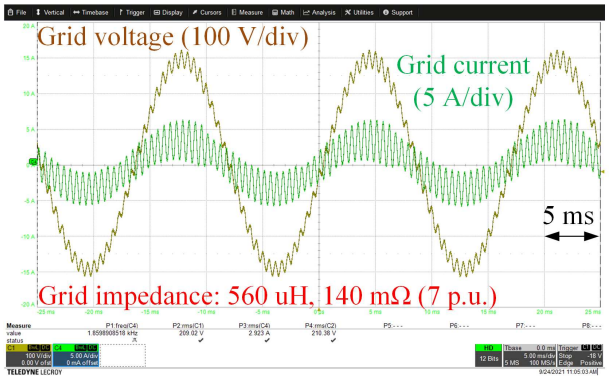
(b)

Figure 3.33: Experimental Waveforms For The PR Controller Under Different Grid Impedances

However, the grid current can be kept stable for the entire grid impedance variation with the selected H-infinity controller. Fig. 3.35 shows the experimental waveforms for the H-infinity controller under 4 different grid impedances. Table 3.4 shows the grid current THD comparison between the two controllers under different grid impedances. The THD is measured using a YOKOGAWA WT500 Series Power An-



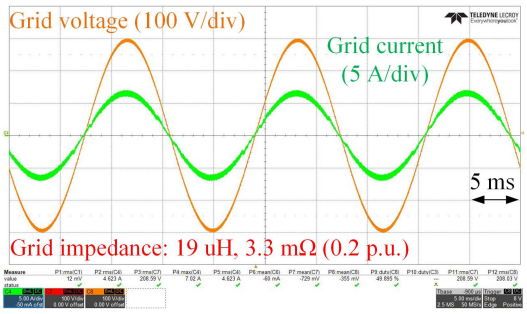
(a)



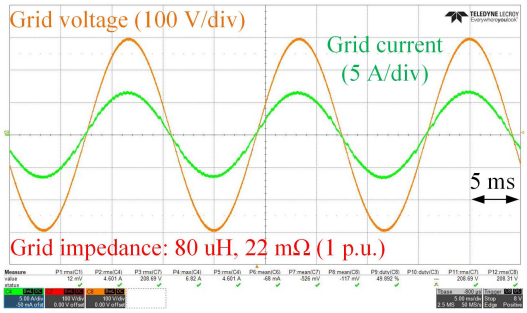
(b)

Figure 3.34: Experimental Waveforms For The PR Controller When The Grid Impedance Is 7 p.u. (a) Zoom-out Waveform Showing The Divergent Grid Voltage And Current; (b) Zoom-in Waveform Showing The High-frequency Resonance In The Grid Current

alyzer. The THD is always below 4% for the H-infinity controller, which fulfills the power quality requirement from the IEEE 1547 Standard [10].



(a)



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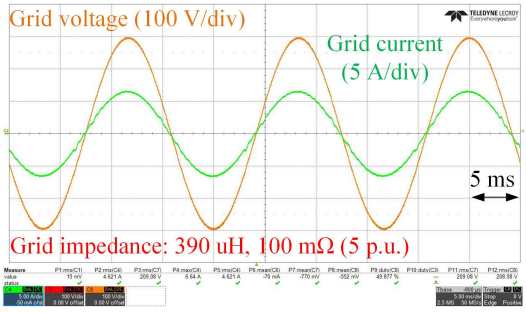

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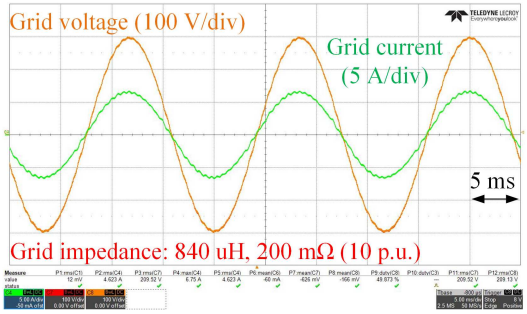


(d)

Figure 3.35: Experimental Waveforms For The H-infinity Controller Under Different Grid Impedances

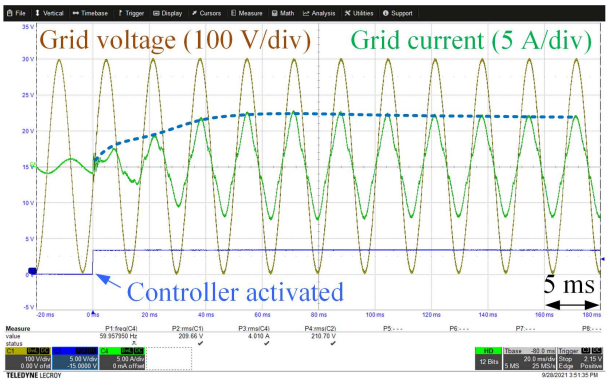
Table 3.4: Grid Current THD Comparison Between The H-infinity COntroller And The PR Controller Under Different Grid Impedances

Grid impedance	**THD (H-infinity controller)**	**THD (PR controller)**
19 μH, 3.3 mΩ (0.2 p.u.)	1.4%	1.3%
29 μH, 5 mΩ (0.3 p.u.)	1.4%	1.3%
58 μH, 10 mΩ (0.5 p.u.)	1.4%	1.4%
80 μH, 20 mΩ (1 p.u.)	1.5%	1.4%
174 μH, 30 mΩ (2 p.u.)	1.6%	1.5%
280 μH, 70 mΩ (3.5 p.u.)	1.8%	1.7%
390 μH, 100 mΩ (5 p.u.)	1.7%	1.8%
560 μH, 140 mΩ (7 p.u.)	1.7%	unstable
730 μH, 180 mΩ (9 p.u.)	2.5%	unstable
840 μH, 200 mΩ (10 p.u.)	2.2%	unstable

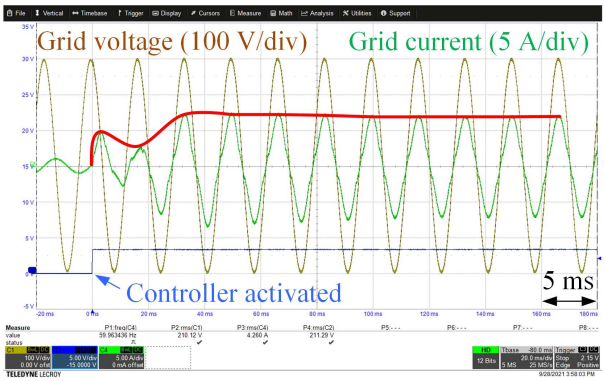
Additional experiments have been performed using a PR controller with a low proportional gain of 1.5. The resonant gain is still equal to 150. Fig. 3.36(a) shows that the PR controller can also keep the grid current stable under the largest grid impedance. The blue dashed curve represents the current envelope for the PR controller. The red solid curve represents the current envelope for the H-infinity controller. However, compared with the H-infinity controller, the dynamic response to a current reference step-change of such a low-gain PR controller is slower. As shown in Fig. 3.37, the current envelope of both controllers has been plotted in the same figure. It is clear that when the H-infinity controller is used, the grid current reaches the steady-state almost 16.67 ms earlier than the PR controller with a low proportional gain. From both the simulation and experimental results, we can see that when the PR controller has a relatively large proportional gain, both controllers can achieve similar steady-state error and grid current THD only for small grid impedances. The PR controller loses its stability when the impedance continues to increase. When the PR controller gain has been reduced, stability can be maintained for all impedance variations. At the same time, both controllers can achieve similar steady-state error and stability margin. However, the dynamic response of the PR controller becomes slower than that of the H-infinity controller due to the lower bandwidth. As a result, the proposed H-infinity has an overall satisfactory performance in terms of stability, steady-state error, and dynamic performance compared with the traditional PR controller.

3.6.2 THD Comparison Between The H-infinity Controllers Generated By Different Pareto Fronts Without Harmonic Compensation

Different H-infinity controllers have been implemented in the hardware testbed as well. The same two H-infinity controllers used in the simulations have been pro-



(a)



(b)

Figure 3.36: Experimental Start-up Waveforms For (a) The H-infinity Controller And (b) The PR Controller With Low Proportional Gain Under 10 p.u. Grid Impedance

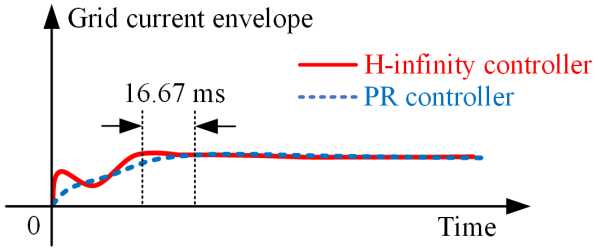
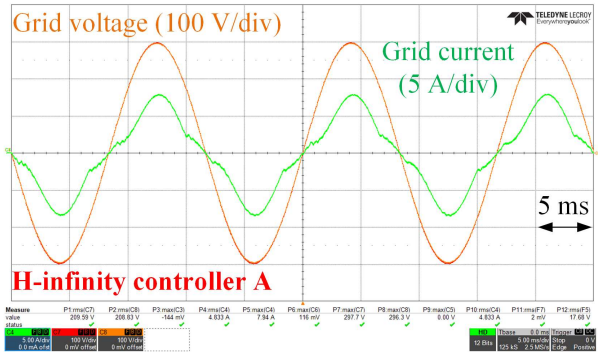


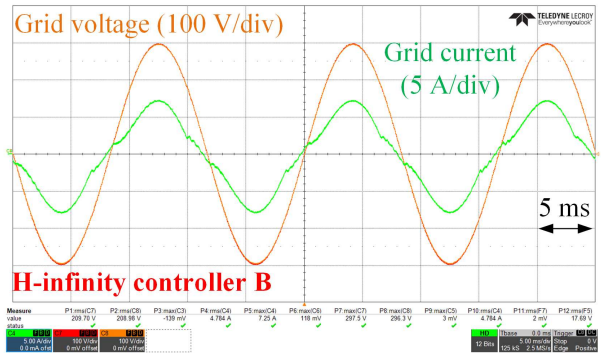
Figure 3.37: Comparison Of The Dynamic Response Between The H-infinity Controller And The PR Controller With A Low Proportional Gain

grammed into the DSP in the experiments. The repetitive controller based harmonic compensation has been intentionally removed in order to compare the 3^{rd} order harmonic suppression capability of the two H-infinity controllers. Fig. 3.38 shows the

experimental waveforms of the two controllers under the nominal grid impedance and 1 kW unity power factor operating condition. Fig. 3.39 shows the measured grid current THD of the two H-infinity controllers for all grid impedances. We can see that the H-infinity controller B, which takes the error at 180 Hz as an optimization target, achieves a much lower THD compared with controller A. This result is consistent with the simulation results provided in the previous section.



(a)



(b)

Figure 3.38: Experimental Waveforms For Different H-infinity Controllers Without Additional Harmonic Compensation Controllers Under The Nominal Grid Impedance. (a) H-infinity Controller A Is Selected In Terms Of The Lowest Sensitivity And The Smallest Steady-state Error At 60 Hz. (b) H-infinity Controller B Is Selected In Terms Of The Lowest Sensitivity And The Smallest Error At 180 Hz.

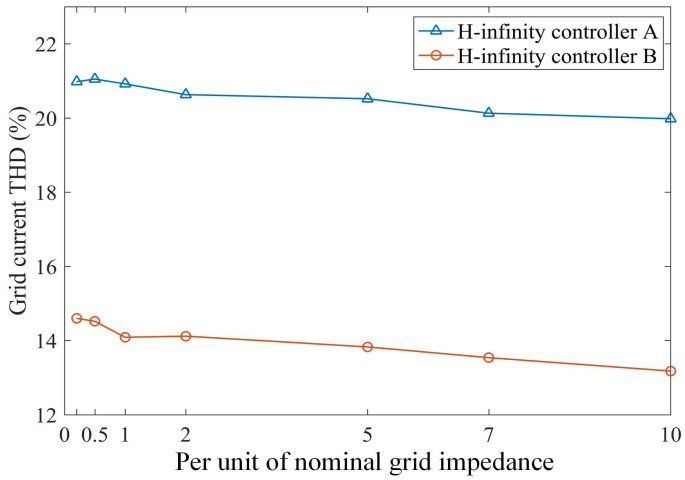


Figure 3.39: Comparison Of The Grid Current THD Between The Two H-infinity Controllers Generated By Different Pareto Fronts Through Experiments

3.7 Conclusion and Future Work

A large variation of the grid impedance can cause an unstable grid current in grid-connected inverters. A robust H-infinity controller has been implemented to address this stability issue. This chapter firstly explains the two important design objectives for the H-infinity controller synthesis, namely the robust stability and robust performance, by using a geometric representation and a frequency-dependent constraint. In order to achieve the above design objectives, an automated design process has been proposed to generate a cluster of satisfying H-infinity controllers by intelligently selecting the weighting functions based on a predefined grid impedance uncertainty and by actively shaping the systems closed-loop transfer function. The constraints on each weighting function have been elaborated, and the generated controller will be reduced to 3^{rd} order for easier digital implementation in the DSP. As a result, the design objectives need to be revalidated using the reduced-order controller to ensure that the robust stability and performance are retained. Another significant contribution of this study is that the selection of the final H-infinity controller is

based on a 2-D Pareto Front optimization technique in terms of stability margin and steady-state error, while the existing literature randomly chooses the controller. The performance of the conventional PR controller and the proposed H-infinity controller has been evaluated through PLECS simulations as well as hardware experiments. The result shows that when the proportional gain of the PR controller is high, both the controllers have similar steady-state error only for low grid impedances. The PR controller loses its stability when the impedance goes large. A PR controller with low proportional gain can keep the grid current stable under larger impedances and achieve almost the same stability margin as the H-infinity controller. However, the dynamic response becomes slow due to the lower bandwidth. In conclusion, the selected optimal H-infinity controller has an overall satisfactory performance in terms of stability, steady-state error, and dynamic response compared with the traditional PR controller. The comparison between different H-infinity controllers generated by different Pareto Fronts has been conducted through PLECS simulations and hardware experiments. The result indicates that the selected H-infinity controllers have a better performance in terms of the respective optimization targets. Last but not least, the proposed automated design methodology can also be applied to other applications where model uncertainty needs to be considered. A repetitive controller has been implemented in the experiments in order to compensate for the harmonic current induced by deadtime in the SPWM switching. The effect of the repetitive controller on the system stability has not been evaluated in the manuscript, which will be the future work of this study.

Chapter 4

A MULTILAYER COMMUNICATION ARCHITECTURE ASSISTING CONTROL OF DERS IN A DISTRIBUTION NETWORK WITH HIGH PENETRATION

4.1 Introduction

The continuously rising demands for clean and economic sources of electricity generation promotes the use of distributed renewable energy resources which is a promising alternative to fossil fuel based resources [85]. A micro-grid concept was introduced where the loads in such a grid was energized by multiple interconnected Distributed Energy Resources (DERs) and energy storage devices. A micro-grid can also interact with the main grid to provide energy management and economic dispatch [86]. However, the operation of the distribution system will be impacted by the micro-grid with high penetration of DERs [87]. As a result, a communication architecture is necessary for micro-grids and even for distribution systems in order to monitor and control the installed DERs [88].

In traditional power systems, analog variables explain all the phenomenon. The implementation of digital devices provides the power system with new forms of remote monitoring and control, which provides smartness to the system. Remote monitoring is achieved by communicating with the DER systems by using digital variables. The development of digital control is beneficial to all actors and specifically to end users in the modern power system. One important step towards the digitalization of the power system was the introduction of the Intelligent Electronic Device (IED), allowing direct conversion of analog inputs, like voltages and currents, into digital variables

and calculated results. Such devices are implemented with appropriate protocols combined with communication and computing systems [89]. Protocols such as Modbus TCP/IP and Distributed Network Protocol 3 (DNP3) are widely used in commercial DER inverters to facilitate communication with supervisory devices [90]. IEC 61850 standard provides a universal communication solution to solve the problems of interoperability among devices from different vendors. In order to provide control capability in smart micro-grids, a multi-layer structure is commonly implemented, which makes it possible to decentralize systems intelligence by reorganizing management tasks and reallocating them in different layers. And this, in turn, permits the control system to have different levels of autonomy [91], [92]. Different control tasks are assigned to different layers based on their time sensitivity and the amount of data that can be handled by each layer. For instance, grid current control and power control will be handled by individual DERs since the inverters need to respond to their power command promptly. However, tasks such as energy management and power flow control can be assigned to the upper supervisory level.

The communication architecture development in such a multi-layer based smart micro-grid system faces two major challenges. The first challenge is the coordination between communication and system control. The reason can be explained in the following three aspects. Firstly, if the control and the communication programs are both carried out in the Enhanced Pulse Width Modulator (ePWM) interrupt inside the Digital Signal Processor (DSP), the total time consumption of both programs should be less than the switching period otherwise the PWM output will be affected. In this case, the communication interacts with the control algorithm. For instance, if most of the switching period is assigned to the control program, the amount of data that can be exchanged is greatly limited. If the communication takes up too much time, and the control algorithm cannot be completed within the remaining time, the

DER normal operation will be affected. Secondly, in a multi-layer architecture, communication between different layers should take place at different frequencies based on the specific control tasks. For example, if the control task happens once every second in the upper supervisory layer, it is inappropriate to conduct the associated communication every switching cycle. Thirdly, the communication error also affects the control performance. For example, abnormal communication caused by hardware interference may generate incorrect monitoring data and commands, which poses a threat to the system normal operation. The second challenge is the coordination of communication between different layers. The reason is explained in the following two aspects. Firstly, communication between different layers should be independent with each other especially when there is communication being carried out inside the ePWM interrupt. The communication outside of the interrupt should not interfere with the one inside. Otherwise, the DER inverter operation will be influenced. Secondly, the relationship between the amount of data transmitted and the time consumed is different for different communication protocols. For example, the time consumption for Serial Peripheral Interface (SPI) communication is proportional to the number of words exchanged. However, in Modbus communication, the time consumption for transmitting one register and 120 registers is almost the same. This requires coordination between these two protocols in order to improve communication efficiency.

Various micro-grid testbeds have been proposed in existing literature. In [93], a private micro-grid system with multiple DERs was built, and an IED prototype was proposed using a CompactRIO from National Instruments (NI), an integrated LabView real-time processor, and a Field-Programmable Gate Array (FPGA). The communication between the IED and supervisory controller was based on ethernet. However, the results presented in this paper only included system variables monitoring. No control functionality has been implemented and tested. [94] [95] proposed

a three-layer automation system for a 200 kVA utility-connected low-voltage micro-grid based on peer-to-peer and plug-and-play concepts at The Catalonia Institute for Energy Research (IREC). The top layer is the remote management unit. The middle layer is responsible for real and reactive power command generation. The bottom layer consists of multiple DERs which keep the real and reactive power equal to the reference. [96] also proposed a three-level automation architecture for a smart micro-grid to achieve bidirectional communication between the supervisory controller and DERs. The station level includes a supervisory controller which receives system variables and sends control commands to the Bay level using IEC-61850 standard. The Bay level uses a Raspberry Pi to collect analog variables from the DER inverters and to send power and voltage commands to DERs using SPI communication. The implementation of SPI communication and IEC-61850 was discussed in the paper. However, the DERs used in both projects were emulators instead of real inverter hardware. Even though [96] presented SPI and IEC-61850 implementation details, coordination between system control and communication and coordination between the two communication protocols have not been discussed. The communication speed of IEC-61850 in [96] is much slower than Modbus TCP/IP which is implemented in this paper. In addition, the work presented here is highly scalable and designed for applications in actual, large distribution systems with high PV penetration compared to a relatively limited laboratory scale demonstration in the literature.

Many universities and institutes have developed their own micro-grid testbeds with integrated communication architecture. University of Los Andes presented an interactive real-time distribution network which used a CompactRIO [97]. The distribution system has been modeled by using LabView and OpenDSS. Oak Ridge National Laboratory (ORNL) also proposed a Hardware-In-Loop (HIL) based micro-grid testbed which was composed of a Real-Time Digital Simulator (RTDS) for modeling

of the microgrid, multiple CompactRIOs, a prototype Energy Management System (EMS), and a Supervisory Control and Data Acquisition system (SCADA) [98]. The communication protocol used between the IED controller and the EMS is Modbus TCP/IP. However, both [97] and [98] used HIL setup instead of real hardware inverters, and no Modbus TCP/IP protocol implementation details were provided in [98]. Lehigh University leaded the development of a power converter based Advanced Experimental Platform [99]. The system is consisted of one OPAL-RT RTDS, two one-bus microgrid testbeds, one modular multilevel converter (MMC), one cascaded multilevel converter (CMC), and one multiagent system (MAS). Aalborg University has developed a microgrid prototype consisting of a DC power supply, linear loads, a dSPACE controller, and DER converters (Battery, wind turbine and PV) [100–104]. A 35 kW micro-grid test bench developed at the Energy Systems Research Laboratory, Florida International University includes a generator station, different renewable energy sources (wind emulator, PV panels, fuel cells emulators) and electronic load [105]. The communication between different types of Data Acquisition systems (DAQs) and local/supervisor controllers is through Ethernet or LAN. The University of Tennessee-Knoxville proposed a 15 kVA microgrid system with emulated generator, load, wind turbine, and PV panels using power electronic converters [106]. The communication between the IED and LabView is through ethernet. CAN bus is used to exchange data between the CompactRIO and the DSP in each emulator. [99–106] did not include strategies to address the challenges in the communication architecture in terms of the coordination between the control and communication as well as the coordination between different protocols.

The main contribution of this study compared with existing references is to provide a fast, convenient, and comprehensive communication solution for a smart micro-grid system and to provide validation through actual hardware instead of emulators. Mul-

tiple strategies have been proposed to address the aforementioned challenges so that the system is well optimized, highly scalable and adaptive. In order to coordinate communication and system control, two dual-core DSPs are used in the architecture where one DSP is responsible for control and another DSP is used for communication. In such arrangement, the Control DSP only needs to exchange a small amount of data with external devices, which greatly reduces the communication time. In addition, the communication will be performed in conjunction with a simple feedforward control in only one switching cycle during each fundamental period, which minimizes the interaction between the control and communication programs. At the same time, by adopting a separate DSP which is specifically responsible for data collection, processing, and transmission, the amount of data that can be transferred has been increased to a large extent. Time scales have been adjusted for different types of communication between different layers by taking into consideration the time sensitivity of different control tasks. In addition, certain software protection mechanism has been introduced in the proposed architecture in order to protect the control program from being affected by communication failure. In order to coordinate different communication protocols, parallel computing has been adopted to minimize the dependency between different protocols. Moreover, communication efficiency has been improved by taking into account the features of different protocols. For example, the data transmitted through multiple SPI communications in every 6 fundamental cycles will be grouped into a larger data package for one-time Modbus communication. Finally, all the hardware prototypes are built with off-the-shelf components, which makes the architecture ready for industrial applications in a large distribution system with high renewable penetration.

In this chapter, a 4-layer communication architecture in a smart micro-grid system will be firstly presented in Section 4.2. The hardware design consideration of the

customized Edge Intelligent Device (EID) will be briefly presented in Section 4.3. The communication architecture for this test bench involves SPI communication, Modbus TCP/IP communication, and Wireless communication. Implementation of both SPI and Modbus communication will be illustrated by using a flow chart in Section 4.4. Multiple strategies have been proposed in Section 4.5 in order to mitigate the aforementioned challenges so that the system performance and communication efficiency can be improved. Experimental results are presented in Section 4.6 to show the effectiveness of the proposed architecture.

4.2 Description of the Testbed

4.2.1 The 4-layer Structure

A 4-layer structure has been proposed for the smart micro-grid testbed with the advanced communication architecture. An overview of the architecture is shown in Fig. 4.1, and the tasks of each device in different layers are presented in Fig. 4.2.

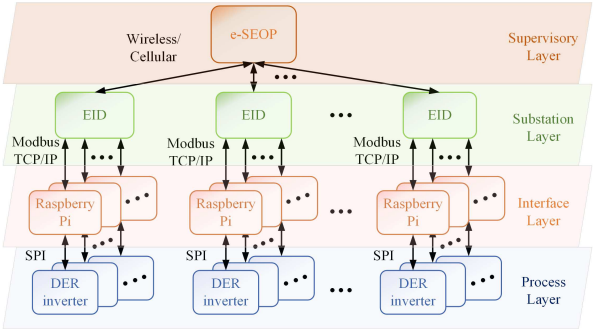


Figure 4.1: An Overall Structure Of The Proposed Multi-layer Communication Architecture

(a) **The Process Layer:** The Process Layer consists of customized DER inverters, and each inverter is equipped with two DSPs. One DSP is used for controlling the DER inverter and another is specifically for communication. The inverter

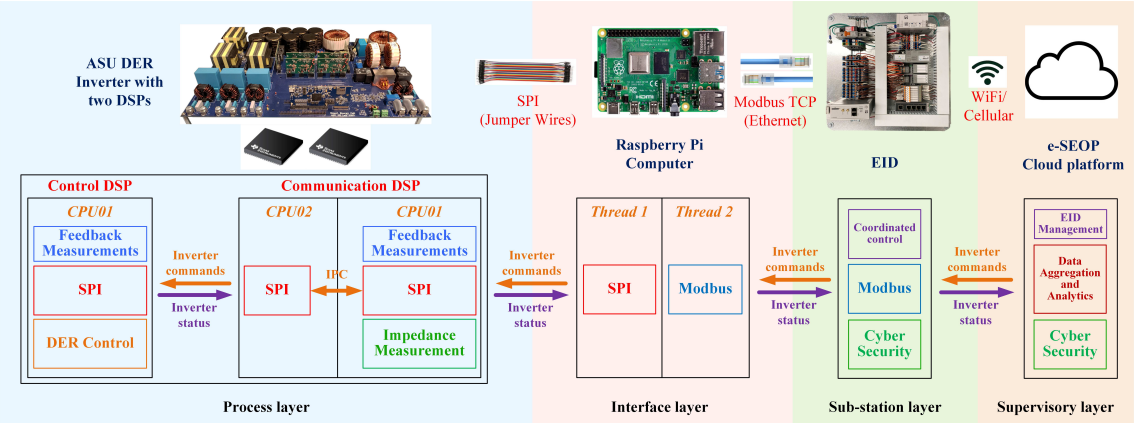


Figure 4.2: Detailed Communication And Control Tasks For Each Component In The Proposed Multi-layer Architecture

analog feedback will be directly fed into the Analog-to-Digital (ADC) channels of both the DSPs. The Control DSP will use the feedback information to carry out Maximum Power Point Tracking (MPPT) control for both PV channels, State-of-Charge control for the battery channel, DC bus voltage control, and grid current control following IEEE 1547 standard in grid connected condition. The Control DSP will also implement droop control for power sharing in standalone condition. Besides the control functions, the Control DSP also receives real and reactive power commands from the Communication DSP. There are two CPU cores in the Communication DSP. One core is responsible for sending all the inverter analog measurement, such as voltages and currents, to the upper Interface layer (Raspberry Pi) using SPI communication. Simultaneously, this core receives inverter commands, such as real and reactive power commands, inverter operation mode, and operation curves, from the Interface layer. The final real and reactive power commands will be calculated in this core based on the received operation mode and curve settings and shared with the 2nd CPU. The 2nd CPU of the Communication DSP will be responsible for sending the final real and reactive power commands to the Control DSP and receiving

inverter operation status (such as operation mode or fault status, etc.) from the Control DSP through SPI. As a result, a large amount of data exchange between the Process layer and the Interface layer will be handled by the Communication DSP. The Control DSP will just involve a small amount of communication.

(b) **The Interface Layer:** Raspberry Pi computers are used in the Interface Layer. It serves as a communication interface between the Process and Sub-station layers. Each Raspberry Pi is connected to a single inverter. The Raspberry Pi collects the analog feedback measurements from the Communication DSP using SPI and sends them to the upper Sub-station layer using Modbus TCP/IP protocol. At the same time, it receives the inverter commands and customized settings from the Sub-station layer using Modbus TCP/IP and sends them back to the Process layer using SPI communication. The SPI communication frequency is determined by the Communication DSP while the Modbus communication frequency is controlled by the EID in the Sub-station layer. Two reasons have been taken into consideration when choosing Modbus instead of IEC 61850 as the communication protocol. Firstly, most commercial DER inverters such as ABB and SMA solar inverters support Modbus protocol. Such off-the-shelf converters can be easily added to the developed micro-grid system to increase the system capacity. Secondly, IEC-61850 is a complete standard for Distribution Automation System (DAS) while Modbus is just a communication protocol. Modbus allows data and commands to pass between the two devices without requiring the knowledge of how data is processed or how outside communication is implemented [98]. As a result, Modbus is more suitable for rapid system development.

(c) **The Substation Layer:** A customized EID is used in the Sub-station layer.

A Substation Layer can have multiple EIDs, and each EID can be connected to multiple Raspberry Pis which are in the same Area Electric Power System (AEPS). The EID will receive all the DER inverter feedback signals from the Raspberry Pi and send inverter commands and settings to the Raspberry Pi through Modbus TCP/IP communication. At the same time, the EID will upload inverter feedback variables to the upper Supervisory layer and receive inverter commands from the Supervisory layer through cellular or wireless (WiFi) communication. Besides the communication function, the EID is also responsible for DER management through coordinated control. Since the EID will be exposed to the public network, cyber security feature is a must.

(d) **The Supervisory Layer:** The Supervisory Layer consists of a customized end-to-end solar energy optimization platform (e-SEOP). The e-SEOP will be connected to multiple EIDs to form a larger AEPS, and it is responsible for EID management. Data aggregation and data analytics will be handled by the platform as well. Finally, a dashboard will be created to serve as a Graphical User Interface (GUI) so that both the customers and the system operators will have a better understanding of the system status. Cyber security is also integrated in e-SEOP to protect user data and the system from cyber-attacks [107].

4.2.2 Description of the Hardware

(a) **The Process Layer:** The Process Layer consists of multiple DER inverters, and each one includes both DC/DC and DC/AC power stages. The circuit schematic of the customized DER inverter is shown in Fig. 4.3. The DER inverter is rated at 2 kVA and has a 0.75 power factor capability. The DC/DC stage contains three independent channels which are two PV channels and one

battery channel. As a result, the DER hardware is able to generate as well as absorb real power. The DC/AC stage is a conventional single-phase voltage-source inverter. The switches used are IGBT power modules from Infineon Technology, and the part number is FS35R12W1T4 [108]. The control stage of the inverter contains two C2000 series dule-core DSPs from Texas Instruments, and the part number is TMS320F28379D [109].

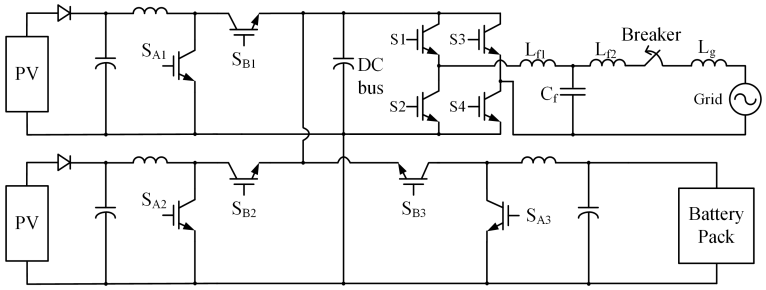


Figure 4.3: Circuit Topology Of The Customized DER Inverter

(b) **The Interface Layer:** The Raspberry Pi 4B is used in the Interface Layer as shown in Fig. 4.2. It is a small-sized computer that runs Linux Operating System. It features high processor speed, outstanding multimedia performance, large memory, and easy connectivity [110]. The Raspberry Pi also supports different hardware communication protocols such as SPI and Modbus TCP/IP. The hardware connection between the Raspberry Pi and the Communication DSP is through jumper wires while the connection between the Raspberry Pi and the EID is through ethernet cables.

(c) **The Substation Layer:**: A customized EID designed by one of the project partners, POUNDRA, LLC [111], is used here in the Substation Layer. The EID hardware information will be provided separately in Section 4.3.

(d) **The Supervisory Layer:** The e-SEOP is designed by one of the project part-

ners, Hitachi America, Ltd., and further details on this platform is beyond the scope of this study.

4.2.3 Description of the Software

(a) **The Process Layer:** The coding of the two DSPs adopted in the Process layer is implemented in the Code Composer Studio (CCS) using C language.

(b) **The Interface Layer:** The coding environment in the Raspberry Pi is called Geany which is a pre-installed application. For SPI communication, an open-source and third-party library called WiringPi [112] is used. It configures the hardware pins on the Raspberry Pi board and initiates SPI communication by calling predefined functions. For Modbus TCP/IP communication, an open-source and third-party library called libmodbus [113] is used. It also has customized functions for both the client and server in Modbus. Both the libraries are based on C language.

(c) **The Substation Layer:**: The coding of the Modbus TCP/IP communication in the customized EID is based on structured text which is a high-level language supported by IEC 61131-3 standard and is specifically designed for Programmable Logic Controllers (PLCs).

(d) **The Supervisory Layer:** The proposed e-SEOP platform is developed using a web-based language.

4.2.4 Advantages of the Proposed Architecture

System flexibility and scalability can be greatly improved using the proposed 4-layer structured communication architecture. In terms of hardware, even though each inverter is equipped with a Raspberry Pi, a single EID can manage several Raspberry

Pis at a time. Since most of the commercial DER inverters support Modbus communication, and since the Raspberry Pi supports both SPI and Modbus protocols, it is flexible to add either customized or commercial inverters to the testbed by connecting the EID and DER inverter through an individual Raspberry Pi. In addition, the e-SEOP uses the wireless or cellular network which makes it possible to control multiple distant EIDs. In terms of software, the customized coding structure in the Communication DSP, the Raspberry Pi, and the EID makes it adaptive to different number of analog feedback signals, different number of DER inverters connected, data format, and switching frequencies. As a result, the proposed architecture is highly scalable and can be applied to a large distribution system with high renewable penetration.

4.3 Hardware Design of the Customized EID

To meet the control and communication requirements of the proposed communication architecture, the EID needs the following capabilities: (1) The EID is equipped with hardware interface with downstream end device using Modbus TCP or DNP3 TCP protocol; (2) The EID is able to interface with at least two end devices; (3) The EID is allowed to communicate with adjacent EIDs through Machine-to-Machine (M2M) communication; (4) The EID is capable of automatic time setting using Network Time Protocol (NTP) or Simple Network Time Protocol (SNTP); (5) The EID can connect to the private or public cloud through Message Queuing Telemetry Transport (MQTT) or JavaScript Object Notation (JSON) for e-SEOP integration through its communication channel hardware. The following five hardware platforms were evaluated, and two platforms were selected for the prototypes.

(a) FC6APlus® from IDEC [114]

(b) PLCNext® from Phoenix Contact [115]

(c) iQ® from Mitsubishi [116]

(d) CR1000X® from Campbell Scientific [117]

(e) cRIO® and LabView® from National Instruments [118]

The EID should be built with only Commercial-Off-The-Shelf (COTS) components to avoid developing custom hardware and need for hardware certification. The EID can then be more readily accepted by utilities. Two platforms demonstrate that the EIDs are platform independent and reduce the risk of implementing new features developed in this project. The hardware platforms were designed to meet UL508A Standard for Safety, Industrial Control Panel (ICP). Open box hardware is developed for the prototype, which will allow changes to be made before getting a UL508A listing.

Fig. 4.4 shows the completed PLCNext and cRIO based EID prototypes.

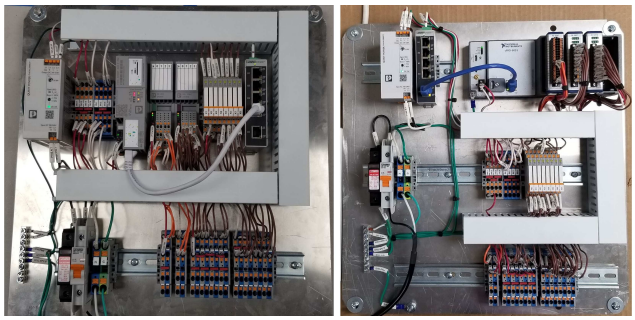


Figure 4.4: EID Prototypes: PLCNext EID Prototype (Left) And cRIO EID Prototype (Right)

4.4 SPI and Modbus TCP/IP Communication Implementation

4.4.1 SPI Communication

SPI is a synchronous serial communication interface specification used for short-distance communication [119]. One feature of SPI communication is that data transmission and reception happen within the same SPI clock. Therefore, the master and slave will send and receive data simultaneously. The speed of data transfer is depen-

dent on SPI clock frequency. There are four different clock schemes in both the DSP F28379D and Raspberry Pi which decides when the slave/master sends and receives data bits. Both devices should be configured to the same clock scheme.

As shown in Fig. 4.2, two dual-core DSPs will be used in this communication architecture. CPU01 of the Communication DSP will handle the SPI communication to the Raspberry Pi, while the SPI between the two DSPs will be assigned to CPU02 of the Communication DSP and CPU01 of the Control DSP. Inter-Processor-Communication (IPC) is in the Communication DSP to share data between the two cores [119].

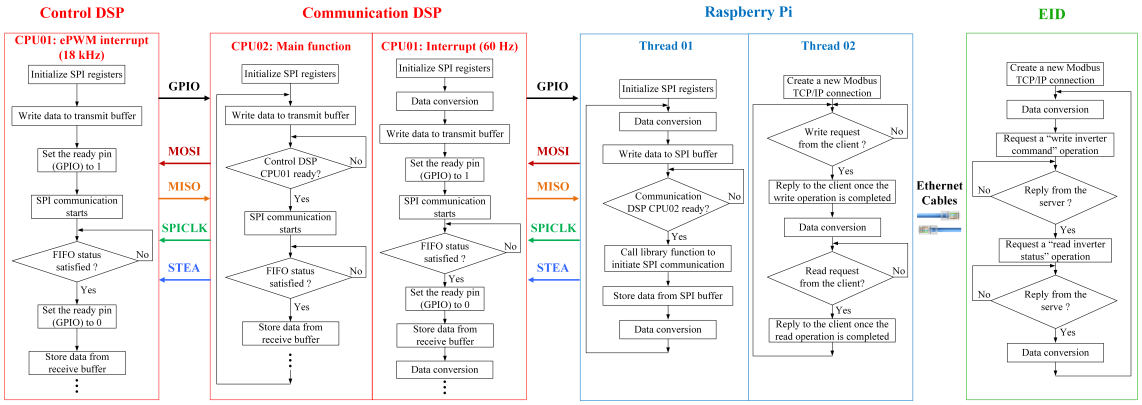


Figure 4.5: Program Routine For SPI And Modbus TCP/IP Communication In The Proposed Architecture

(a) **SPI communication between the Communication DSP and Raspberry Pi:** The CPU01 of the Communication DSP and the Raspberry Pi will be configured as a slave and a master, respectively. Pin connection between the two devices is shown in Fig. 4.5. For the DSP F28379D, the number of bits in each word transmitted can be flexibly configured from 0 to 16. There are two First-In-First-Out (FIFO) buffers in the DSP for transmitting and receiving words from external devices. For the Raspberry Pi, the number of bits per word is fixed at 8. There is only one data buffer in the Raspberry Pi, and the data

in the buffer will be automatically covered by the bits received from the MISO bus. The SPI clock frequency of the Raspberry Pi can vary from 5 MHz to 32 MHz. However, the F28379D has an upper limit for the SPI clock frequency when it is configured as a slave [119]. Hence, the maximum clock frequency is 12.5 MHz.

The program routine for the SPI communication between the Communication DSP and Raspberry Pi is shown in Fig. 4.5. Before initiating SPI communication, both the Communication DSP and the Raspberry Pi need to perform data conversion so that different types of data can be represented by multiple bytes. Then the transmitted data will be written to the transmit buffer in the DSP and to the SPI buffer in the Raspberry Pi. SPI communication between the Communication DSP and the Raspberry Pi is controlled to happen once every fundamental cycle. Firstly, the SPI code will be placed in a DSP interrupt function with a 60 Hz timer. Secondly, a GPIO pin from the DSP will be used as an SPI ready indicator. If the pin is pulled high, that means the DSP is ready for SPI communication. Then the Raspberry Pi can call its library function to send out SPI clocks and initiate the communication. Once the communication is completed, the ready pin will be pulled low so that the second communication will be avoided in the same interrupt. Therefore, the Communication DSP determines the pace of SPI communication in this scenario. The completion of the communication depends on the FIFO status of the receiving buffer in the DSP. For example, if there are 8 words being exchanged in the process, the code will be in a while loop until the FIFO status changes from 0 to 8, which indicates the slave has received all the words.

(b) **SPI communication between the Communication DSP and Control**

DSP: In this scenario, the CPU02 of the Communication DSP and the CPU01 of the Control DSP will be configured as a master and a slave, respectively. Pin connection between the two DSPs is shown in Fig. 4.5. One of the major difference between this SPI communication and the previous one is that the number of bits per word transferred can be configured to 16 bits. As a result, no additional data conversion to bytes is needed. The SPI frequency is still limited to 12.5 MHz.

The program routine for the SPI communication between the two DSPs is shown in Fig. 4.5. The basic steps for communication are very similar to the previous SPI communication. However, the SPI code of the Control DSP is placed in its ePWM interrupt function, and the SPI code of the Communication DSP CPU 02 is written in its main function. A dedicated GPIO pin is used as an indicator, which means the pace of SPI communication is determined by the Control DSP. As a result, the SPI communication happens once in a switching cycle. In addition, complicated interrupt nesting is avoided since no SPI interrupt is involved.

4.4.2 Modbus TCP/IP Communication

Modbus is an application-layer communication protocol, positioned at level 7 of the OSI model. It provides client/server communication between devices connected on different types of buses or networks [120]. Modbus TCP/IP uses TCP/IP as its electrical interface, and it uses the existing ethernet network equipment which makes communication very fast and cost effective. There are four types of data that Modbus TCP/IP can deal with, and the detailed information is shown in Table 4.1. Since the data exchanged between the EID and DSP is usually integers or floating points, only input registers and holding registers will be used in the program. The major difference

between the Modbus TCP/IP and SPI communication is that the data transmission and reception does not happen simultaneously in Modbus TCP/IP. Only the client has the authority to perform read and write operations.

Table 4.1: Data Types In Modbus TCP/IP Communication

Data types	**Number of bits**	**Operation**
Coils	1	Read or Write
Discrete inputs	1	Read only
Input registers	16	Read only
Holding registers	16	Read or Write

In the proposed communication architecture, the Raspberry Pi is configured as the server, and the EID is configured as the client. In the Raspberry Pi, a Modbus TCP/IP context must be generated using its IP address before trying to create a connection to the EID. Before receiving and sending data, the Raspberry Pi will create a register map for all four data types with desired size, and the map for each data type has a starting address of 0. Since the server cannot perform read or write operations in Modbus TCP/IP protocol, it only accepts read or write requests from the client and replies a message to the client once the operation has been completed. The program routine of the Modbus communication can be seen in Fig. 4.5.

All the variables that need to be exchanged between the Raspberry Pi and the EID must be converted to 16-bit data since only holding registers and input registers will be used. The adopted approach is described as follows, each variable, regardless of integer or floating point, will be represented by 2 registers. The first register indicates the sign of the variable. For example, 0 means positive and 1 means negative. The second register stores the absolute value of the variable. It is easy to convert integer

variables to such format. For floating points, they can be converted to integers just by multiplying the absolute value by 100 in order to preserve 2 decimals. In this way, the precision of the data can be easily adjusted based on either EID requirement or data size restriction placed by the Modbus register. Of course, both the Raspberry Pi and the EID are aware of the actual data format for each Modbus register.

4.5 Strategies to Improve Communication Performance

One major contribution of this study is that multiple strategies have been proposed to optimize the 4-layer communication architecture so that the efficiency and adaptiveness can be greatly enhanced.

4.5.1 Use of Two Dual-Core DSPs

The analog feedback signals of the inverter will be connected to the ADC channels of both the Communication and Control DSPs so that the monitoring data does not have to be transmitted from the Control DSP to the Communication DSP. The benefits of using two DSPs include a boost of data transmission capacity and a reduction of the impact of communication on the inverter control. The conventional single-DSP approach requires each SPI communication to be finished within one switching cycle, which limits the amount of data being transferred. In the proposed architecture with two DSPs, since the Communication DSP does not need to run at switching frequency, it can transmit a large amount of real-time measured data to the Raspberry Pi at a much lower frequency. The time consumed in the SPI communication is positively correlated to the amount of data being exchanged. Therefore, in order to reduce the influence of the communication on the Control DSP, the amount of data transferred between the two DSPs needs to be minimized. This is achieved by using the Communication DSP to process both the instruction data and monitoring data.

IEEE 1547 standard defines 5 normal operation modes for a DER inverter in the grid connected condition [10]. For the case of constant reactive power mode, the Communication DSP will directly transfer the reactive power commands which are received from the EID. Similarly, for constant power factor mode, the Communication DSP will calculate the required reactive power command given by the desired power factor and real power measurement from its own ADC channels. In the Volt Var, Volt Watt, and Watt Var modes, the Communication DSP will construct three curves based on the set points received from the EID and calculate the corresponding real or reactive power command based on the measured analog feedback (such as voltages, active power, etc.). As a result, the instruction data will be pre-processed in the Communication DSP, and only real and reactive power commands will be transmitted to the Control DSP using SPI protocol. On the other hand, the computational processing, such as average and RMS value estimation of the analog feedback of the inverter, can also be done in the Communication DSP using its own ADC channels. As a result, the Control DSP will only transmit the inverter operation status (such as operation mode, fault mode, etc.) to the Communication DSP. Compared with the single-DSP approach where the DSP needs to handle all the instruction and monitoring data, the proposed two-DSP architecture greatly reduces the communication burden of the Control DSP. Therefore, the data transmission capacity is expanded, and the influence of communication on inverter control is minimized. Hence, the Control DSP will have more resource to implement complex control algorithms.

In addition, the DSP used in this application is featured with dual-core which further enhances the processing power of the Control and the Communication DSPs. The entire system becomes an equivalent quad-core environment. The Communication DSP can undertake not only communication tasks but also some control tasks that do not require high real-time performance but need heavy data processing. For

example, the implementation of network impedance measurement using Fast Fourier Transformation (FFT) analysis requires a large amount of calculation. However, this measurement does not need to be performed every switching cycle. Instead, the network impedance only needs to be measured every hour or every few hours in a day. Such tasks can be assigned to the Communication DSP. Parallel computing happens naturally in this quad-core configuration. Furthermore, if the computing power of the DSP increases, the switching frequency can be further increased because the time spent on each core has reduced as the tasks being allocated to different cores.

4.5.2 Communication Time Scales

Fig. 4.6 shows different time intervals for communication between different layers and the time restriction for each communication. The communication between different hardware have various time scales. The SPI communication between the two DSPs needs to be finished in one switching cycle. In order to save more time for the DER control algorithm, the SPI communication will only be performed in one switching cycle during each fundamental period, and that switching cycle only has a very simple feedforward control for the DER inverter. Since this happens only once in every fundamental cycle, it will not have much impact on the control, which has been proved by experimental results in Section 4.6. Between the two DSPs, the Control DSP determines the pace of the SPI communication, and the frequency of the communication is once every fundamental cycle. Therefore, the time interval between two SPI communications is 16.7 ms. The SPI communication between the Communication DSP and the Raspberry Pi is also implemented once every fundamental cycle. However, the time consumption of this communication is not limited to one switching period. It can use the entire 16.7 ms for transferring data. Therefore, the number of data that can be exchanged is significantly increased, which fulfils the

communication requirement of the system. The Modbus communication frequency between the Raspberry Pi and the EID is once every 100ms. This is because that the time consumed for transmitting a large data package is almost the same as the time consumed for transmitting a few registers using Modbus protocol. Therefore, the data from the Communication DSP through SPI will be grouped in the Raspberry Pi and sent to the EID every 100 ms or every 6 fundamental cycles. The communication frequency between the EID and the e-SEOP is once every second. This is limited by the communication capability of the cloud platform.

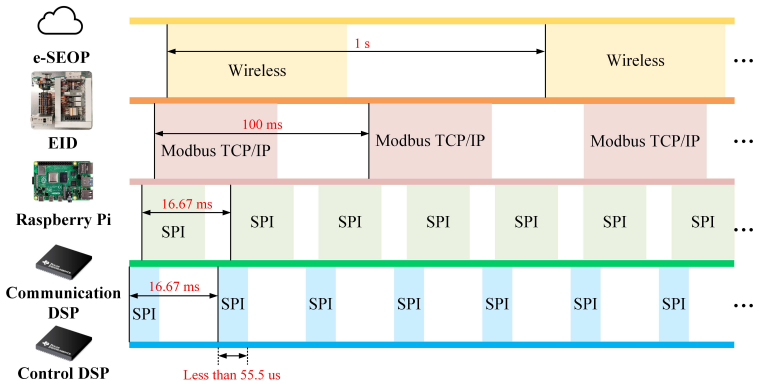


Figure 4.6: Time Scales For Communication Between Different Layers In The Proposed Architecture

4.5.3 Parallel Computing in the Raspberry Pi

The Raspberry Pi, as the communication interface between the Process layer and the Sub-station layer, is responsible for transmitting the information collected in the lower Process layer to the upper Sub-station layer using both SPI and Modbus communication. The Raspberry Pi can work in both serial and parallel computing modes. Serial computing means that the Raspberry Pi sends data to the EID only after it receives the data from the Communication DSP. Similarly, in order to send data to the Communication DSP, the Raspberry Pi needs to wait until it receives the EID

data. It can be seen that in the serial mode, the SPI and Modbus communication are coupled, and the DER inverter control will be negatively affected. The Modbus read and write operations usually take hundreds of microseconds while the switching cycle is usually tens of microseconds. It is impossible for the SPI communication to complete within one switching cycle if serial computing is implemented in a single-DSP architecture. In addition, the number of data transferred through SPI communication in one switching cycle is still small. Performing Modbus communication in series with SPI does not fully utilize its advantage of transmitting a large amount of data.

In order to improve communication efficiency, a parallel computing technique is used here. That is, SPI communication and Modbus communications are carried out independently. In the Raspberry Pi, parallel computing is realized by the multi-threading technique. Two threads will be created for the SPI and Modbus communication, respectively. The Raspberry Pi will run the two threads concurrently. The program routine for multi-threading is also presented in Fig. 4.5 where Thread 01 represents SPI communication and Thread 02 represents Modbus communication. As a result, both SPI and Modbus can have independent transmission frequencies, and the amount of data transmitted each time can be different. This is specifically useful in the single-DSP configuration where the SPI communication has to be completed within one switching cycle. Table 4.2 shows the time consumption of the SPI communication in both serial and parallel computing scenarios. As can be seen in the table, multi-threading helps reduce the time consumption of the SPI communication so that it satisfies the switching period restriction (The switching frequency is assumed to be 18 kHz).

Table 4.2: Time Consumption Of SPI Communication For Both Serial And Parallel Computing In A Single-DSP Configuration

Operating conditions	Time consumption
Serial computing	478 μs
Parallel computing	15 μs

4.5.4 Protection of Shared Variables in the Raspberry Pi

It is important to protect shared variables from being modified by two threads at the same time in the Raspberry Pi.

A mutual-exclusion (mutex) approach is used in the multi-threading technique, which serves as a safety lock to all the shared variables for both SPI and Modbus threads in the Raspberry Pi. Use of mutex includes a pair of lock and unlock operations. Before reading or modifying a variable in either of the threads, mutex will put a lock to the variable if it is not being used by another thread. So that the variable is only accessible to the current thread. After the read or write operation is completed, mutex will release the access to this variable by unlocking it, and other threads will be able to read or modify its value. This ensures each variable can be modified by only one thread at any time.

As a result, if a thread is trying to access a variable that is currently being locked by another thread, it has to wait until the variable accessibility is released. This increases the execution time of a thread because of another thread, which introduces the dependency between the two threads. This is not desirable in parallel computing. However, the dependency between the SPI and Modbus threads can be minimized by reducing the code length between the lock and unlock commands.

4.5.5 Large Data Package and Contiguous Register Mapping for the Modbus Communication

Modbus is especially suitable for transferring a large amount of data. As shown in Table 4.3, the read and write operations of Modbus take almost the same time for different number of registers. In order to take advantage of this feature, the Modbus communication between the Raspberry Pi and the EID is intentionally programmed to occur every 100 ms or every 6 fundamental cycles. During each of this 100 ms, the feedback measurement sent from the Communication DSP will be grouped into a large circular buffer, and the EID will only perform the Modbus read operation once to accept all the data in the buffer. Compared with the communication solution proposed in [96], Modbus is much faster than IEC-61850. From the results shown in [96], it took 3.71 ms for IEC-61850 to send a variable whereas Modbus takes only 135 us to transmit 120 variables.

Table 4.3: Time Consumption Of Modbus TCP/IP Communication For Transmitting Different Number Of Registers

Number of registers operated	**Modbus operation type**	**Time consumption**
1	Read	134 μs
	Write	128 μs
2	Read	135 μs
	Write	134 μs
30	Read	139 μs
	Write	133 μs
120	Read	136 μs
	Write	135 μs

As mentioned in the previous section, any transmission of floating point data needs extra data conversion since either holding registers or input registers consists of only 16 bits. To implement the data conversion, the floating points will be expressed using two 16-bit registers. The first register represents the sign, and the second register equals to its absolute value multiplied by 10/100/1000 based on how many decimals need to be preserved. As a result, the proposed communication solution has the ability to adjust data precision.

Another feature of the Modbus communication is that it prefers a contiguous register map instead of several register map segments. A starting address and the number of registers the client wants to access must be specified in the Modbus read and write functions. Only one single read or write operation is needed if the register map is contiguous. However, if the map is not contiguous, which is the case in some commercial DER inverters such as SMA and ABB, multiple Modbus operations are required. As shown in Fig. 4.7, the time consumption for reading all the registers in a contiguous map is much less than that in a non-contiguous map. If the EID wants to read all the 120 registers in a contiguous map, it only needs to call the Modbus read function once which will take around 135 μs based on Table 4.3. However, if the register map has three separate segments, the EID need to perform Modbus read operation three times, and the time consumption will be tripled. In the proposed architecture, a contiguous register map which contains all the analog feedback variables and control parameters has be created in the Raspberry Pi for convenient and efficient Modbus communication.

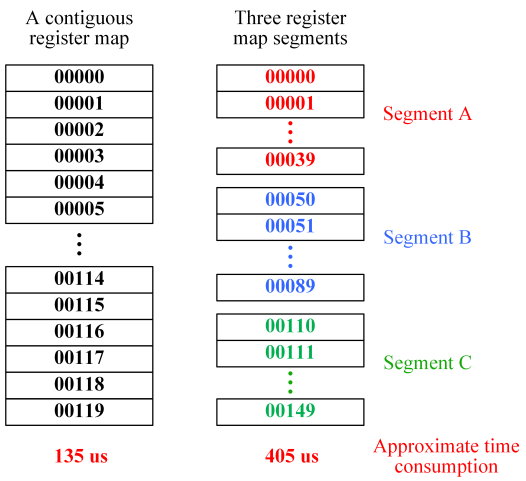


Figure 4.7: Modbus Time Consumption Comparison Between A Contiguous Register Map And A Discontinuous Map Where Both Maps Contain 120 Registers

4.5.6 Advanced Coordination Between the SPI Communication and the Control Algorithm

Since the control program of the DER inverter is written in the ePWM interrupt which runs once every switching cycle in the DSP, a natural idea is to program the SPI communication in the ePWM interrupt instead of using a separate SPI interrupt to avoid interrupt nesting. However, SPI takes considerable amount time as it involves waiting for the flag bit and data conversion. All the coding written in the ePWM interrupt must be completed within one switching cycle, otherwise it will affect the normal PWM output. Therefore, the addition of the SPI program reduces the time that the control algorithm can utilize. Moreover, this time restriction also limits the amount of data that can be transferred because the time spent by SPI communication is proportional to the number of words transmitted. According to the measurement, the control algorithm already occupies over 90% of the switching cycle, which greatly reduces the amount of data that can be exchanged. As a result, this traditional method is not suitable for applications which requires a large amount

of data transmission. An alternative solution proposed here is to evenly distribute the SPI communication into several switching cycles, as shown in Fig. 4.8. In these selected switching cycles, the control command is generated using a simple predictive feed-forward approach. It is assumed that the difference between the output voltage command in the current cycle and the previous cycle is almost equal to the difference between the previous cycle and the cycle before that. This predictive algorithm is based on the observation of adjacent output voltage commands. This technique greatly reduces the time consumption of the control algorithm, and most of the remaining time in this switching cycle can be used for the SPI communication.

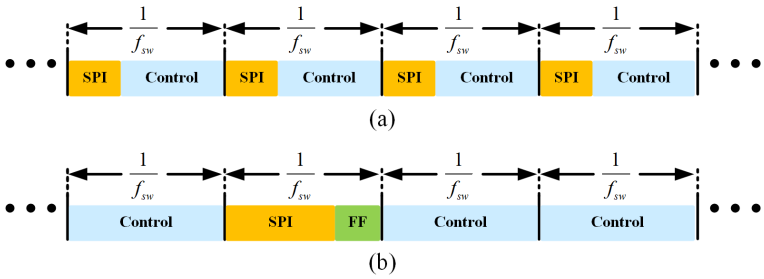


Figure 4.8: Comparison Between Conventional And The Proposed SPI Implementation Methods Where f_{sw} Represents The Switching Frequency And FF Represents A Feed-forward Control. (a) Conventional Method: SPI Communication In Each Switching Cycle; (b) Proposed Method: SPI Communication Only In Specific Switching Cycles Where A Feed-forward (FF) Is Used To Simplify The Control.

Of course, the number of selected switching cycles should be minimized to provide least impact on the normal control. Therefore, as much data as possible should be transmitted during these selected switching cycles. Simulation results show that if this feed-forward method is used only for a limited number of times in a fundamental period, it will hardly affect the control output. However, the output harmonics will increase if there is too much interference. Fortunately, the proposed architecture with two dual-core DSPs has reduced the communication task of the Control DSP. Now it only needs to receive real and reactive power commands (two 16-bit words)

from the Communication DSP and send the real-time inverter operating mode (one 16-bit word) to the Communication DSP. Based on the experimental results, all data transmission can be completed within one switching cycle. As a result, only one switching cycle in every fundamental period will be used for the SPI communication, and a feed-forward approach will be used as the control command in this switching cycle. Experimental results in Section 4.6 have shown that this strategy has little impact on the output waveforms.

This approach is adaptive to different number of variables by adjusting the number of selected switching cycles. But the number of such special switching cycles should be limited. The waveforms in Section 4.6 show that the DER inverter output will be affected if there are too many switching cycles being selected for SPI communication.

4.5.7 Software Protection of the SPI Communication

The software protection proposed in this part includes detection of incorrect data using Cyclic-Redundancy-Check (CRC) and prevention of self-lock of the SPI program.

The first software protection aims to improve the communication reliability. In the experiments, it is found that the SPI communication between the Raspberry Pi and Communication DSP and between the Communication and Control DSP can be interfered by the EMI generated in the power circuit. In order to ensure that the data transmitted through SPI is correct, additional CRC bits will be added to the data package so that the program can determine whether the data received is correct or not. CRC is commonly used in the industry for SPI communication.

In the SPI communication implementation, a GPIO pin serves as a flag to indicate the master whether the slave is ready for data transmission. The master will wait until the flag has been pulled high by the slave and then starts to send out SPI

clock signals to initiate communication. This is achieved by using a while loop in the master program. The master code will not jump out of the while loop until the flag is triggered. However, the flag may not be correctly set due to some interference noise in the circuit. In that case, the master code will be locked in the infinite loop, and the SPI clock will never be sent out to the slave, which disturbs the normal operation of both master and slave. Especially in the Control DSP, the SPI communication is included in the ePWM interrupt which must finishes within one switching cycle. The PWM output errors will occur if such situation happens. Therefore, a software protection approach is adopted for the master. The principle is that if the time consumed for the while loop exceeds an upper limit, the program will break the loop and directly move to the control algorithm without running the rest of the communication code. This protection ensures that the PWM output is not disturbed by the unintentional noise. The same protection strategy should be applied to the program where both the slave and the master use a while loop to check the status of the receiving FIFO register to determine whether the SPI communication has completed. If the number of received words, which is indicated by the FIFO status bit, is lower than the preset value due to abnormal interference in the circuit, the protection mechanism will intentionally break the while loop to avoid the impact on the control algorithm. Verification of the proposed software protection mechanism has be elaborated in Section 4.6.

4.6 Validations of the Proposed Communication Architecture

4.6.1 Advantages of the Proposed SPI Implementation Method in the DSP

Two test scenarios will be compared in this part. Both the scenarios will use only one DSP. The first scenario will implement the SPI communication in each switching

cycle while in the second scenario, the SPI communication will be carried out only in several selected switching cycles.

In the first scenario, since SPI communication is implemented in each ePWM interrupt along with the control algorithm, the time restriction for SPI is determined by the switching period and the time consumption of the control code. Table 4.4 shows the time consumption for each control function in the DSP.

Table 4.4: Time Consumption For Each Control Function In The DSP

Control function description	**Time consumption**
ADC feedback measurement	2.78 μs
Second-Order-Generalized-Integrator (SOGI)	5.7 μs
$\alpha\beta$-to-dq transformation	1.7 μs
PLL controller	2.0 μs
PR controller	5.7 μs
Command generation based on IEEE 1547	2.88 μs
DC/DC stage control (for all 3 channels)	20 μs
Grid impedance measurement	6.0 μs
Robust grid current control using H-infinity	3.44 μs
Total	**50.20 μs**

Assume that the switching frequency is 18 kHz which means the switching period is 55.55 us. The maximum SPI clock frequency for the DSP (as a slave) is 12.5 MHz. Therefore, the time consumed for transferring one 8-bit word is calculated using the following equation.

$$T_{8bits} = \frac{8}{12.5 \times 10^6} = 0.64\mu s \tag{4.1}$$

Hence, by considering approximately 5 us as a safety margin, the remaining time in

each switching cycle is only enough to transmit 1 word. For the entire fundamental cycle which contains 300 switching periods, the maximum number of 8-bit words that can be transmitted is 300.

In the second scenario, several switching cycles will be selected specifically for SPI communication. In such switching cycles, a single feed-forward will be used as the inverter output voltage command, and its time consumption is negligible. As a result, the entire 50 us can be used for the SPI communication considering a 5 us margin. Using the same SPI clock frequency, the number of 8-bit words that can be transmitted within such a switching cycle is 80. Fig. 4.9 shows the inverter output voltage (measured across the filter capacitor at inverter output) and the grid current obtained from PLECS simulations when 25 and 30 switching cycles are selected for such a combination of SPI communication and feed-forward control, respectively. It clearly shows that when the number of selected switching cycles is under a certain limit, the feed-forward control still yields a low THD in the grid current. The maximum number of words that can be transmitted without affecting the inverter output in this scenario (for the case of 25 switching cycles) is 2000 which is much more than that in the first case. Note that some harmonic voltage is intentionally added to the grid in order to test the harmonic compensation algorithm.

4.6.2 Advantages of the Proposed Two-DSP Architecture and the Improved Time Scales

When implementing the proposed communication architecture with two dual-core DSPs, all the real-time feedback measurements will be transmitted from the Communication DSP instead of the Control DSP, and the SPI communication can fully utilize the entire fundamental cycle. Assume that the SPI clock frequency is still configured as 12.5 MHz. The number of 8-bit words that can be exchanged between

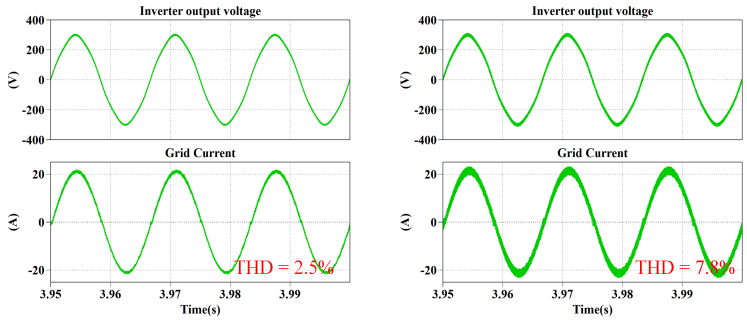


Figure 4.9: PLECS Simulation Results Of Inverter Output Voltage And Current With Different Number Of Switching Cycles Being Selected For The SPI Communication. Left: 25 Cycles From Each Fundamental Period Are Selected; Right: 30 Cycles From Each Fundamental Period Are Selected.

the Communication DSP and Raspberry Pi is

$$N_{8bits} = \frac{T_{60Hz}}{T_{8bits}} = \frac{16.7ms}{0.64\mu s} = 26093 \tag{4.2}$$

where T_{60Hz} represents the fundamental period. It can be seen that the number of words is even much larger than that in the second scenario of Section 4.6.1 where only a single DSP was implemented, and SPI communication is performed only in selected switching cycles. Table 4.5 summarizes the number of words exchanged through SPI in a fundamental period under different architectures. As a result, the proposed dual-DSP architecture is very suitable for applications which requires a large amount of data transmission. Between the Control DSP and Communication DSP, only one switching cycle during every fundamental period is selected for SPI since only real and reactive power commands need to be transferred. And the time consumption for transmitting these two variables is way less than the 55.55 us (switching period).

4.6.3 Software Protection of the SPI Communication

Fig. 4.10 shows the time measurement of the ePWM interrupt in the DSP when an abnormal condition happens. A GPIO will be pulled high when the interrupt starts and pulled low at the end of the interrupt. As a result, the pulse width of

Table 4.5: Number Of Words That Can Be Exchanged With Raspberry Pi Through SPI In A Fundamental Period In Different Architectures

Test Scenarios	**Number of 8-bit words**
· Single-DSP architecture · SPI communication is initiated every switching cycle	300
· Single-DSP architecture · SPI communication is initiated only in limited number of switching cycles · Feedforward control is used in those selected cycles	2000
· Dual-DSP architecture · SPI communication in the Communication DSP uses full fundamental period · SPI communication in the Control DSP initiates only in one switching cycle · Feedforward control is used in the select cycle	26093

the GPIO signal represents the time consumed for each interrupt. In Fig. 4.10, the SPI communication was impacted by some unintentional interference so that the status of the receiving FIFO register in the slave DSP never reaches the predefined threshold. The program will be locked in the while loop, and the interrupt takes infinite time. Therefore, the GPIO signal is always high. This poses a threat to the control algorithm and the PWM output. By adopting the proposed software protection strategy, the while loop will be forcibly broken, and the program will continue with the control algorithm. As shown in Fig. 4.11, the time spent by each ePWM interrupt is successfully limited within the switching period.

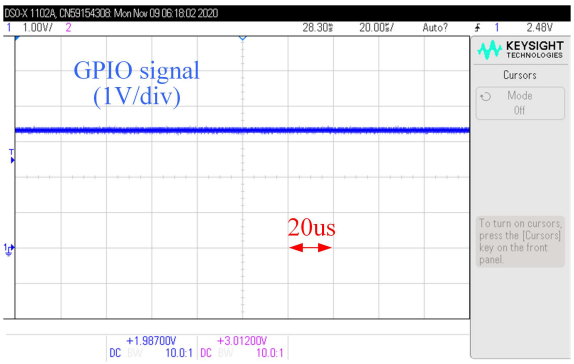


Figure 4.10: EPWM Interrupt Time Measurement When The SPI Communication Is Impacted By Unintentional Interference, And No Protection Method Is Implemented

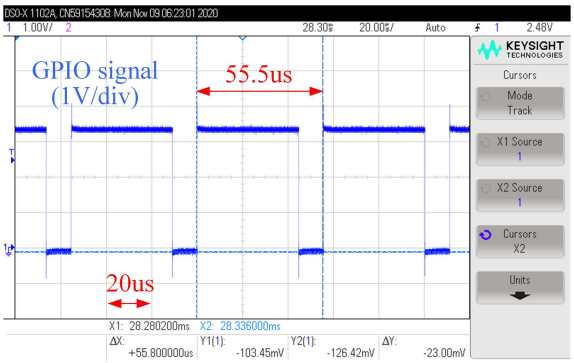


Figure 4.11: EPWM Interrupt Time Measurement When The SPI Communication Is Impacted By Unintentional Interference, And The Proposed Protection Method Is Implemented

4.6.4 Experimental Verification of the DER Inverter Operating under Control Commands Sent from the EID

Test Case 1: Constant Power Factor and Constant Reactive Power Modes

As per IEEE 1547 standards, constant power factor and constant reactive power factor modes require a direct command from the Sub-station layer. Therefore, the EID will send a specific power factor and reactive power command to the Raspberry Pi using Modbus. For the case of constant reactive power mode, the Communication DSP does not need to process the command received from the Raspberry Pi and will

directly pass it along to the Control DSP using SPI. For the case of constant power factor mode, the Communication DSP will calculate corresponding reactive power reference using the power factor command as well as the feedback signals from its own ADC channels. Fig. 4.12 and 4.13 show the experimental waveforms of the grid voltage and grid current for each mode. A screenshot of the power analyzer (Part number: YOKOGAWA WT500) is also presented for each mode showing the detailed real-time power measurement. Table 4.6 shows the commands sent from the EID for each mode.

Table 4.6: Commands Specified By The EID For Constant Power Factor And Constant Reactive Power Mode Operation

Operation mode	Command values
Constant power factor mode	1.0
Constant reactive power mode	1.5 kVar

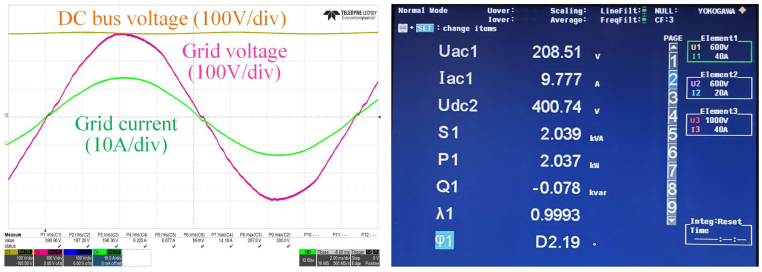


Figure 4.12: Experimental Results Of Constant Power Factor Mode. Left: Measured DC Bus Voltage, Grid Voltage And Grid Current; Right: Real-time Power Measurement From The Power Analyzer

Among the notations of the parameters presented in the power analyzer result, Uac1 represents the RMS voltage after the breaker as shown in Fig. 4.3. As a result, this voltage includes the actual grid voltage and the voltage drop across the grid impedance. Iac1 represents the grid current which is after the filter capacitor. Udc2 is the DC bus voltage. S1 is the apparent power. A positive P1 represents the real

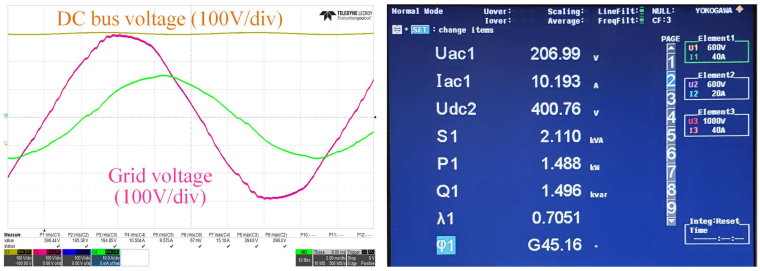


Figure 4.13: Experimental Results Of Constant Reactive Power Mode. Left: Measured DC Bus Voltage, Grid Voltage And Grid Current; Right: Real-time Power Measurement From The Power Analyzer

power generated by the DER inverter. A positive Q1 represents the reactive power generated by the DER inverter. $\lambda 1$ stands for the instantaneous power factor. $\phi 1$ stands for the phase difference between the voltage and the current. The term D before the number means the current is leading the voltage, while the term G means the current is lagging the voltage. Fig. 4.12 shows that the inverter exactly follows the 1.0 power factor command. The Q1 in Fig. 4.13 is 1.496 kVar which is very close to the 1.5 kVar command.

Test Case 2: Volt Var and Volt Watt Modes

In Voltage Reactive power mode, the reactive power actively changes with the grid voltage. The relationship between the two quantities is represented by a Q-V curve which is shown in Fig. 4.14. The EID will firstly transmit several set points to the Communication DSP through the Raspberry Pi so that the Communication DSP is able to calculate the expressions of the Q-V curve. Since the Communication DSP has its own ADC feedback measurement, the instantaneous grid voltage magnitude will be used to calculate the required reactive power command based on the equations. Then this command will be sent to the Control DSP. Similarly, in Voltage Active power mode, the Communication DSP will pre-process the command based on the P-V curve as well as the instantaneous grid voltage feedback and send the final active power command to the Control DSP. Fig. 4.15 and 4.16 show the grid voltage and

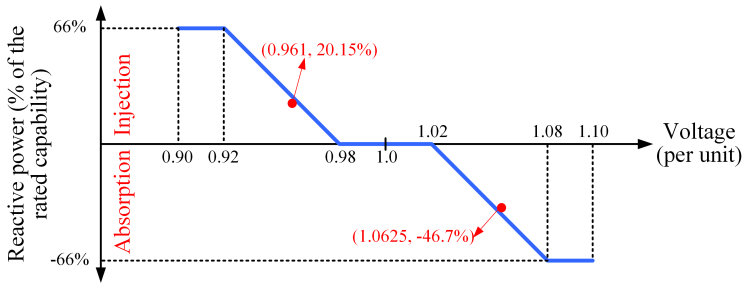


Figure 4.14: The Volt Var Curve Used In The Experiment

grid current waveforms as well as the results from the power analyzer of two operating points in the Volt Var mode. Each point is also plotted on the per unit Q-V curve as the red dot shown in Fig. 14. Note that all the per unit values in the figures are based on 208 V and 2 kVA rated condition. The two operating points closely follow the pre-defined curve. Fig. 4.17 and 4.18 show the grid voltage and grid current waveforms as well as the results from the power analyzer of two operating points in the Volt Watt mode. The points are also plotted on the per unit P-V curve as shown in Fig. 4.19. The real power in Fig. 4.18 is negative which indicates the battery channel of the DC/DC stage is taking power from the grid.

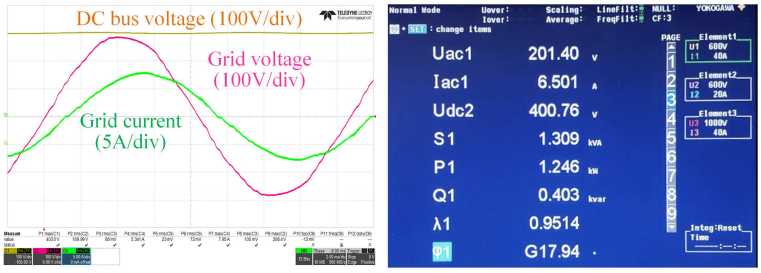


Figure 4.15: Experimental Results Of Volt Var Mode When The Grid Voltage Is Equal To 0.961 Per Unit. The Reactive Power Injected By The DER Is 20.15%. Left: Measured DC Bus Voltage, Grid Voltage And Grid Current; Right: Real-time Power Measurement From The Power Analyzer. The Grid Voltage Is Slightly Increased Due To Reactive Power Injection From The Inverter.

Test Case 3: Volt Var Operation with Different Q-V Curves

Fig. 4.20 and 4.21 show the experimental results when the Q-V curve is changed

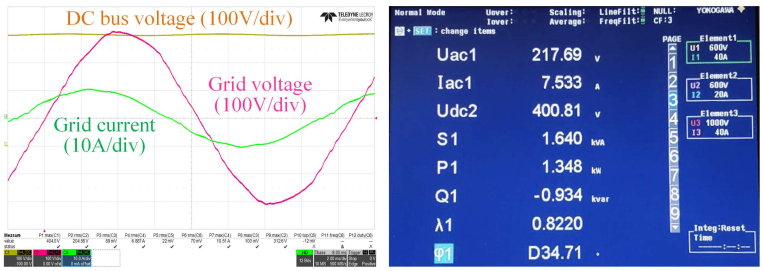


Figure 4.16: Experimental Results Of Volt Var Mode When The Grid Voltage Is Equal To 1.0625 Per Unit. The Reactive Power Absorbed By The DER Is 46.7%. Left: Measured DC Bus Voltage, Grid Voltage And Grid Current; Right: Real-time Power Measurement From The Power Analyzer. The Grid Voltage Is Slightly Decreased Due To Reactive Power Absorption By The Inverter.

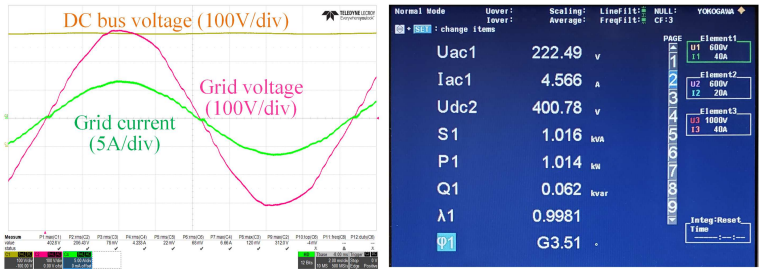


Figure 4.17: Experimental Results Of Volt Watt Mode When The Grid Voltage Is Equal To 1.07 Per Unit. The Real Power Generated By The DER Is 50.7%. Left: Measured DC Bus Voltage, Grid Voltage And Grid Current; Right: Real-time Power Measurement From The Power Analyzer

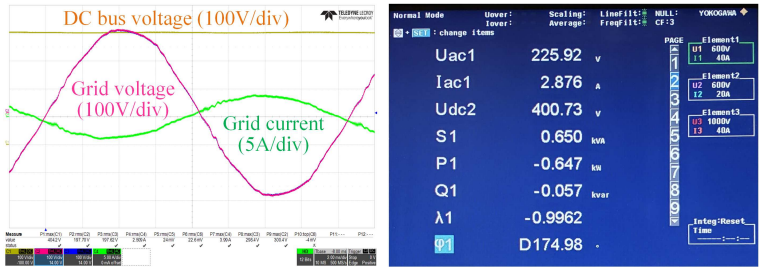


Figure 4.18: Experimental Results Of Volt Watt Mode When The Grid Voltage Is Equal To 1.086 Per Unit. The Real Power Absorbed By The DER Is 32.35%. Left: Measured DC Bus Voltage, Grid Voltage And Grid Current; Right: Real-time Power Measurement From The Power Analyzer

by the EID by modifying the set points. In the experiments, the grid voltage is kept the same as that in Test Case 1. However, the generated reactive power command is smaller in terms of magnitude due to different Q-V curves. The two operating points

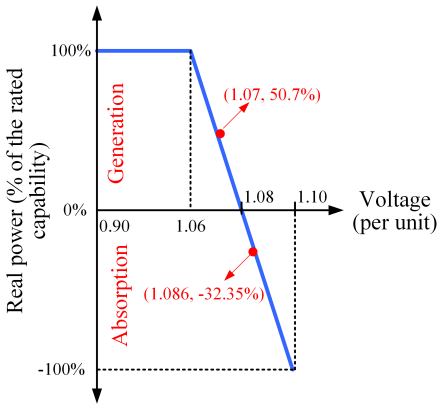


Figure 4.19: The Volt Watt Curve Used In The Experiment

are plotted on the modified Q-V curve as shown in Fig. 4.22. The results show the generated reactive power closely follows the updated curve.

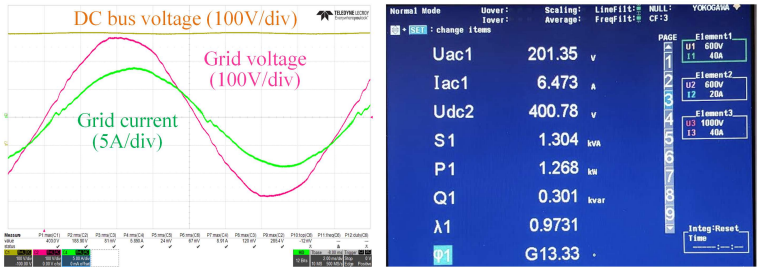


Figure 4.20: Experimental Results Of Volt Var Mode With Modified Curve When The Grid Voltage Is Equal To 0.961 Per Unit. The Reactive Power Injected By The DER Is 15.5%. Left: Measured DC Bus Voltage, Grid Voltage And Grid Current; Right: Real-time Power Measurement From The Power Analyzer. The Grid Voltage Is Slightly Increased Due To Reactive Power Injection From The Inverter.

4.7 Conclusions

This chapter firstly introduces a 4-layer architecture for a smart micro-grid testbed which includes a Process Layer, an Interface Layer, a Substation Layer, and a Supervisory Layer. A customized 2 kVA DER inverter and an EID have been constructed for hardware testing of the proposed system. The Raspberry Pi in the Interface layer serves as a communication interface which communicates with the DER inverter us-

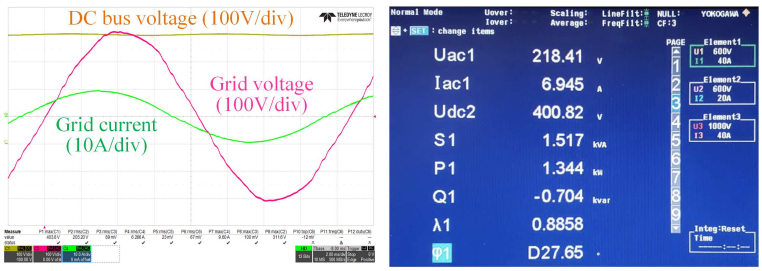


Figure 4.21: Experimental Results Of Volt Var Mode With Modified Curve When The Grid Voltage Is Equal To 1.0625 Per Unit. The Reactive Power Absorbed By The DER Is 35.2%. Left: Measured DC Bus Voltage, Grid Voltage And Grid Current; Right: Real-time Power Measurement From The Power Analyzer. The Grid Voltage Is Slightly Decreased Due To Reactive Power Absorption By The Inverter.

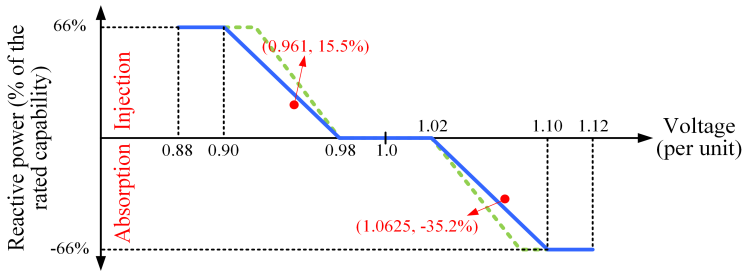


Figure 4.22: The Modified Volt Var Curve Used In The Experiment (The Green Dash Line Represents The Original Volt Var Curve In The Previous Test.)

ing SPI communication and talks to the EID using Modbus TCP/IP protocol. This study provides a convenient and comprehensive solution to SPI and Modbus protocol implementation in a multi-layer architecture. Another important contribution of the study is that it proposes multiple strategies to mitigate the existing challenges of coordination between system control and communication as well as between different communication protocols so that the communication efficiency has been greatly improved. Moreover, the proposed architecture is highly scalable and can be applied to a large distribution system with high renewable penetration. The proposed communication solution has been validated through actual hardware instead of emulators compared with existing literature. The results show a reliable and efficient communication between different layers which facilitates system monitoring and control.

Chapter 5

CONTROL OF MODULAR MULTILEVEL CONVERTERS (MMCS)

5.1 Introduction

Modular Multilevel Converters (MMCs) have been brought into great attention due to their modularity, scalability and improved power quality [121]. They have been widely used in various applications including High Voltage Direct Current (HVDC) transmission system, medium voltage drive, and grid connection of renewable energy resources.

Compared with a traditional two-level converter, MMC shows advantages in the following aspects. Firstly, the AC output voltages of an MMC are multi-level instead of PWM waveforms, which leads to much smaller passive filter (due to lower harmonics) and lower switching loss (due to lower switching frequency of each module) [122]. Secondly, in HVDC applications, the extreme high DC link voltage is a big issue due to the voltage rating of current power semiconductor devices. A well-known solution which is presented in [123] utilizes a conventional Two-Level Converter with a high number (> 100) of direct series connected IGBT devices. However, these devices must be carefully controlled such that they will be turned on and off simultaneously. Otherwise, the voltage sharing cannot be achieved, and the switches with slower turn-on speed or faster turn-off speed will experience severe over-voltage. Alternative solutions are known as Three-Level Converters to reduce undesired grid side harmonics. However, this kind of converters needs a very complex construction-hampering industrial series application and leading to a limited low number of voltage levels [124]. In addition, the system reliability is also improved due to the modular topology.

Fig. 5.1 shows a three-phase MMC configuration. Each phase of MMC consists of two arms, and each arm includes N series-connected Sub-Modules (SMs) and an arm inductor which is intended to suppress high order harmonics in arm currents. The typical structure of each SM is a half-bridge with its DC terminal connected to a capacitor. Each SM is able to output the capacitor voltage if the upper switch is closed and lower switch is open or zero if the lower switch is closed, and the upper switch is open.

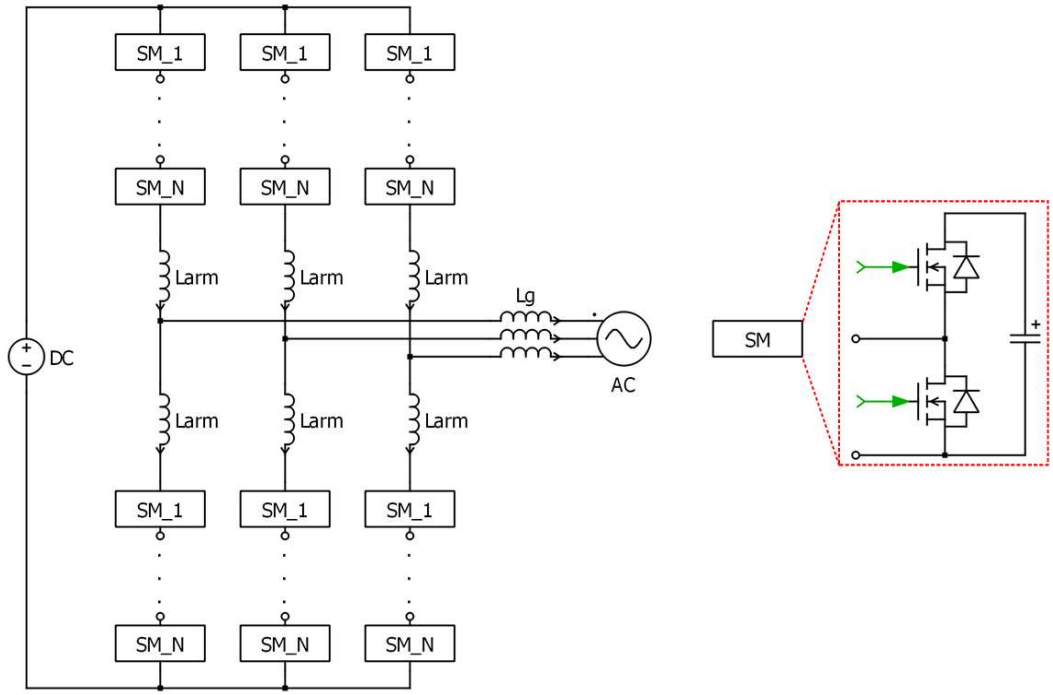


Figure 5.1: Topology Of An MMC

A typical application of the MMC is Variable Speed Drive (VSD) which is suitable for the soft start-up of induction machines. A pump-back system is usually used to test such a VSD with high voltage and high power. In a pump-back system, a motor is connected to the power grid through a VSD. And, at the same time, the motor is also connected to a generator which feeds back most of the energy back to the power grid through another VSD. A pump-back system with two brushless

induction motors has been presented in the literature [125] where analysis of both asynchronous and synchronous performance has been studied as well as the effects of machine parameters, windings, and construction. The limitation of space and cost makes it inappropriate to use real machines to test the system. Literature [126] proposes an improved version of a pump-back system to avoid interaction with real power grid so that the system will not experience high distortion and instability under weak grid condition. A hysteresis control is introduced in the literature [127] for a pump-back system, and its switching characteristic has been studied for the first time. However, the two converters used in this test configuration are traditional two-level inverters, which results in PWM voltage (square) waveforms in the virtual grid. The implementation of MMC will make the virtual grid voltage a sinusoidal waveform if the number of submodules of each arm is large enough.

For Medium Voltage Direct Current (MVDC) system used in the power system, converters with high bandwidth, high reliability, high efficiency and high power density are required. In addition, energy storage devices are preferably integrated into these converters. However, the problems lie in the difficulties of connecting supercapacitors and batteries to high voltage DC buses, and therefore additional DC/DC converters should be implemented in the system, which lowers down the system efficiency. Fortunately, modular structured topologies such as Solid State Transformer (SST), Cascaded H-Bridge (CHB) and the previous MMCs have been widely studied and turn out to be perfect candidates for such MVDC applications.

However, modular topologies also inherent some drawbacks: (1) The large fundamental and 2^{nd} harmonic current in the DC link of each SM will cause dramatic loss if supercapacitors and batteries are used in the module. As a result, the SM switches are supposed to tolerate higher current and switching loss will increase accordingly. In addition, the voltage ripple is inversely proportional to the AC output frequency.

Hence, it is unsuitable to use the traditional MMC as a VSD without controlling the voltage ripple across SM capacitors at a very low frequency. One existing solution introduced in the literature [121] is to absorb the current ripple by another film capacitor and to connect the supercapacitor/battery to the DC link through a DC/DC boost converter. The disadvantage of this method is that the additional film capacitor needs to take the full rating of the current ripple which results in a large capacitor size. Moreover, the switching frequency of the boost converter cannot be high due to hard switching which also increases system switching loss; (2) The size of the additional film capacitor mentioned in (1) will shrink by using the method proposed in GEs MEMC topology [128]. GE replaced the flying capacitors with MMC modules in a three-level flying capacitor structure. It claims 50% reduction in capacitor size. However, the forced commutation of the thyristors is the main drawback of this method, which requires more complex control strategies; (3) For variable frequency application, modular topologies have difficulties starting up from zero frequency under full torque since the voltage and energy ripples in the DC link capacitors are inversely proportional to the frequency. One solution adopted by ABB [129] is circulating current injection with high amplitude and high frequency. The issue associating with this method is the high conduction and switching loss at low-frequency operation. Another solution proposed by Siemens SINAMICS SM120 [130] is to size the capacitor at the highest frequency with variable DC link and AC voltage so that the energy ripple remains the same at a different frequency. The problem with this solution is that to create a variable DC link, DC/DC converters and diode bridges rectifiers are needed, which leads to a large number of devices and passive components.

A Modular Isolated Multilevel Converter (MIMC) has been proposed to overcome the drawbacks existing in the traditional modular structured topologies by connecting

the SM capacitors on the same level of each phase together through isolated DC/DC converters. The proposed MIMC has multiple advantages over the existing solutions in the following aspects. (1) The supercapacitors/batteries can be inserted since the low frequency current ripple in the modules capacitor has been eliminated; (2) Lower voltage supercapacitor/battery can be selected as the isolated DC/DC converter can buck the secondary voltage; (3) As long as the three phase modules on the same level are always connected, different numbers of modules can be connected in parallel on the secondary side, to create a flexible current rating for the supercapacitor/battery packs; (4) All the secondary sides can be connected in parallel to interface with the supercapacitor/battery pack. This supercapacitor/battery pack can be grounded. Therefore, the common mode voltage due to floating the supercapacitor/battery is avoided, and the common mode current caused by high dv/dt is eliminated; (5) The additional capacitor which has to be used with the supercapacitor/battery to absorb the fundamental and 2^{nd} harmonic current can be replaced by a tiny capacitor which only needs to take the switching ripple current. The size of the arm inductor is also reduced due to the elimination of the second order harmonic current in the phase leg. For the isolated DC/DC converter which is used in the proposed topologies, its size can be reduced by making the converter soft-switching at hundreds of kilo-Hertz; (6) In MIMC, the phase energy is automatically balanced by controlling the current of the DC/DC converter. The DC link current in each half bridge still needs to have the same fundamental and 2^{nd} harmonic ripple as usual, since the energy ripple in each phase still has the same form; (7) In the DC short circuit fault, the isolated DC/DC converter can prevent the discharge of the supercapacitor/battery through the diodes by stop switching the DC/DC converters.

In this chapter, a detailed control strategy of a traditional MMC which consists of outer energy loops and inner current loops will be discussed in Section 5.2. A capacitor

voltage balancing technique has been implemented to keep the average DC voltage of each SM the same. The control strategies of an MMC based VSD in a pump-back system has been presented in Section 5.3. Simulation results of the traditional MMC and the MMC based VSD are included in Section 5.2 and 5.3, respectively. Section 5.4 introduces the topology and detailed control strategies of a MIMC. A comparison between the traditional MMC and the newly proposed MIMC has also been made. In Section 5.4, multiple application scenarios have been simulated. First, normal operation of an MIMC has been observed. Since no low-frequency ripple in the SM capacitors, zero-frequency start-up is easy to achieve by using a MIMC. The MIMC based VSD in a pump-back system has been simulated as well. Finally, MIMC is able to provide a large pulse current in a short time due to the integration of supercapacitors. Conclusions and future work are presented in Section 5.5.

5.2 MMC Control Strategy

5.2.1 Outer Energy Loops

Unlike the traditional Two-Level Converters, MMCs contain a large number of capacitors in SMs which are able to absorb and provide energy when they are charged and discharged, respectively. Hence, outer energy loops are necessary to keep the capacitor voltage at the nominal value to ensure proper operation of the MMC.

(a) **Total ennergy control loop:** Total energy loop ensures the power balance between DC and AC side, and it generates DC link current reference. The control diagram of total energy loop is shown in Fig. 5.2 where E_{total_ref} is the sum of the SM capacitor energy at nominal voltage, V_{nom}. E_{total_fbk} represents the feedback of the sum of SM capacitor energy. I_{dc_nom} is the nominal value of DC link current and can be calculated from the power balance between AC side

and DC side. The generated DC link current reference, I_{dc_ref} , will be sent to DC link current control loop.

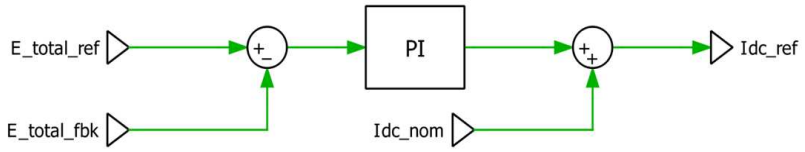


Figure 5.2: Total Energy Control Loop

(b) **Phase ennergy control loop:** As mentioned in Section 6.1, arms currents contain 2^{nd} harmonic circulating components besides fundamental components, and these circulating currents can be separated as common-mode and differential-mode components. Common-mode circulating currents share the same direction in each arm and need to be regulated through controlling phase energy. Phase energy control loop ensures the energy in three phases is balanced so that common-mode circulating currents will be eliminated. The control diagram of phase energy balance is shown in Fig. 5.3. E_{nom} is the nominal energy for a single arm. E_p and E_n represent the upper arm energy and lower arm energy in each phase, respectively. The command generated by this loop is the common-mode circulating current reference, $I_{cir\_com\_ref}$.

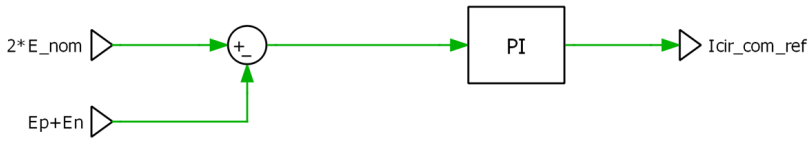


Figure 5.3: Phase Energy Control Loop

(c) **Arm ennergy control loop:** Unlike the common-mode circulating currents, the differential-mode circulating currents have the opposite directions in the upper arm and lower arm in each phase. Arm energy loop ensures the energy

in each phase is balanced so that differential-mode circulating currents will be eliminated. The control diagram of arm energy balance is shown in Fig. 5.4. The command generated in this loop is the differential-mode circulating current reference, $I_{cir\_dif\_ref}$.

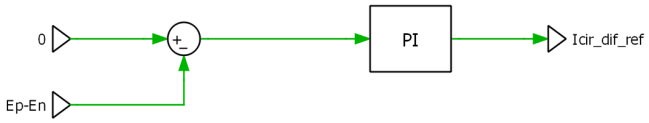


Figure 5.4: Arm Energy Control Loop

5.2.2 Inner Current Loops

In order to better illustrate MMC inner current loop controls, an equivalent circuit model is shown in Fig. 5.5. In the figure, the SMs in each arm are replaced by four controlled voltage sources. I_{dc} is the DC link current. i_a, i_b, i_c are three phase line current. i_{ap} and i_{an} represents the upper arm and lower arm current in Phase A, respectively. The same notation applies to Phase B and C. L_g is the grid inductance and L_{arm} is the arm inductance.

(a) **DC link current control loop:** The DC link current controls the DC voltage component, V_{dc_ref}, in each arm. The DC link current control diagram is shown in Fig. 5.6. The current reference comes from the total energy control loop which was introduced in the previous section. A voltage feedforward of the nominal DC bus voltage, V_{dc_nom} is implemented.

(b) **Fundamental current control loop:** The fundamental voltage component in each arm is controlled by regulating fundamental current component. The control diagram is shown in Fig. 5.7. In the figure, the fundamental currents are controlled in the dq frame. The current reference in d-axis and q-axis control the transferred real and reactive power, respectively.

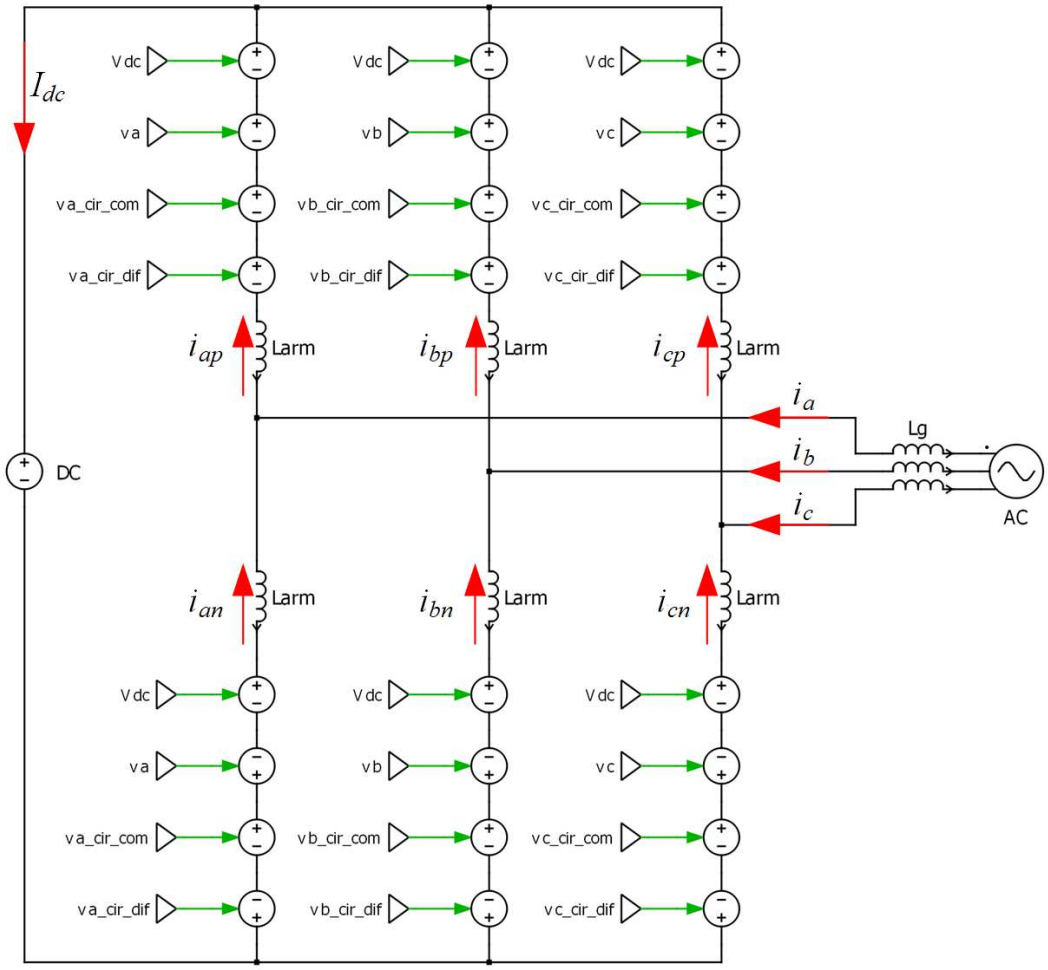


Figure 5.5: Equivalent Circuit Of An MMC

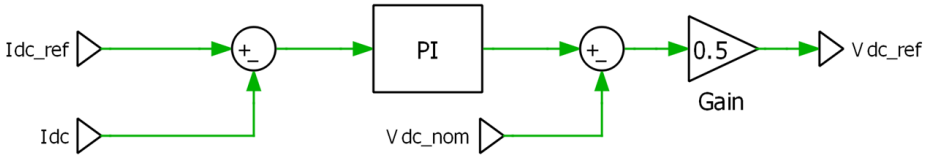


Figure 5.6: DC Link Current Control Loop

(c) **Common-mode circulating current control loop:** The common-mode circulating current is used to control the common-mode circulating voltage component in each arm. The circulating currents only affect the arm currents and have no influence on either AC side or DC side. The control diagram of Phase A common-mode circulating current is shown in Fig. 5.8, and the control of

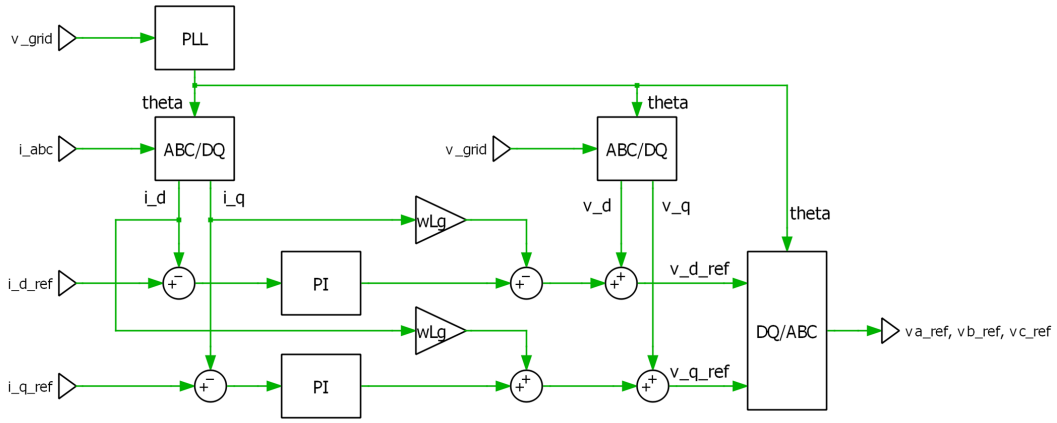


Figure 5.7: Fundamental Current Control Loop

the other two phases are similar. The Phase C voltage command can even be calculated from Phase A and B. Note that a Proportional-Resonant (PR) controller is used to control an AC signal and the selected frequency is chosen to be the double-line frequency. The common-mode circulating current reference comes from phase energy control loop. The common-mode circulating current feedback for Phase A can be calculated as

$$i_{a\_cir\_com} = \frac{1}{2}(i_{ap} + i_{an}) - \frac{1}{3}I_{dc} \tag{5.1}$$

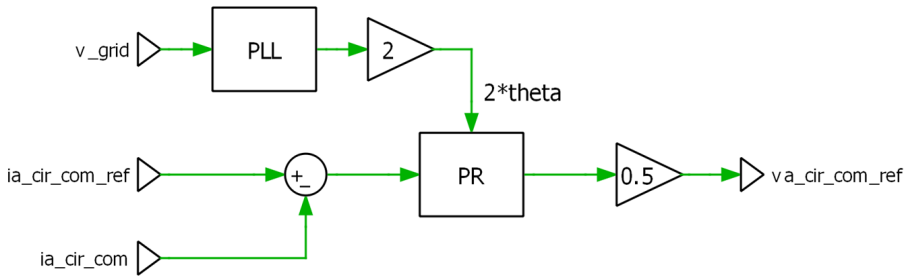


Figure 5.8: Common-mode Circulating Current Control Loop

(d) **Differential-mode circulating current control loop:** The differential-mode circulating current is used to control the differential-mode circulating voltage

component in each arm. The differential-mode circulating currents only affect the arm energy and do not affect phase energy. However, they are linked to phase currents which means they will influence the AC side. The control diagram of Phase A is shown in Fig. 5.9. Similar to the common-mode circulating current control, a PR controller is also used to filter out 2^{nd} harmonic components. The differential-mode circulating reference comes from arm energy control loop. The differential-mode circulating current reference of Phase A can be expressed as

$$i_{a\_cir\_dif} = i_{ap} - i_{an} - i_{a\_ref} \tag{5.2}$$

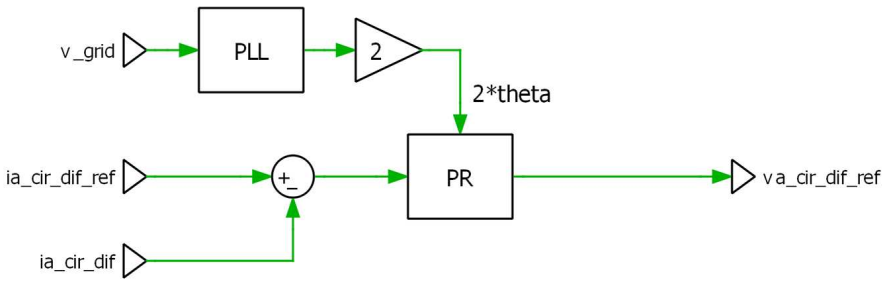


Figure 5.9: Differential-mode Circulating Current Control Loop

5.2.3 Capacitor Voltage Balancing

After completing the voltage reference generation discussed in the previous two sections, the number of SMs that is going to be connected to the circuit can be determined by dividing the arm voltage reference by the average SM capacitor voltage. The issue of capacitor voltage deviation arises when the capacitor with relatively low/high voltage continues discharging/being charged. The solution to this problem is that every time there is a new group of switching signals, sorting the SM capacitors

by their instantaneous voltages. Let the capacitor discharge/be charged if it has the higher/lower voltage.

5.2.4 Equation Based MMC Switching Mode Solution

When it comes to MMC switching mode simulation, an important issue is that the simulation speed is largely affected by the number of switches used in the topology. An effective solution will be using equivalent equations to represent the actual half-bridge switches. In general, when the input gate signal is one, the module capacitor is connected to the main circuit, and the capacitor voltage is related to the integral of the current flowing through the capacitor. The module output voltage is equal to the capacitor voltage. When the gate signal is zero, the module is bypassed, and the capacitor voltage keeps unchanged. The module output voltage is 0. By using this equation based switching mode, the simulation speed can be significantly improved.

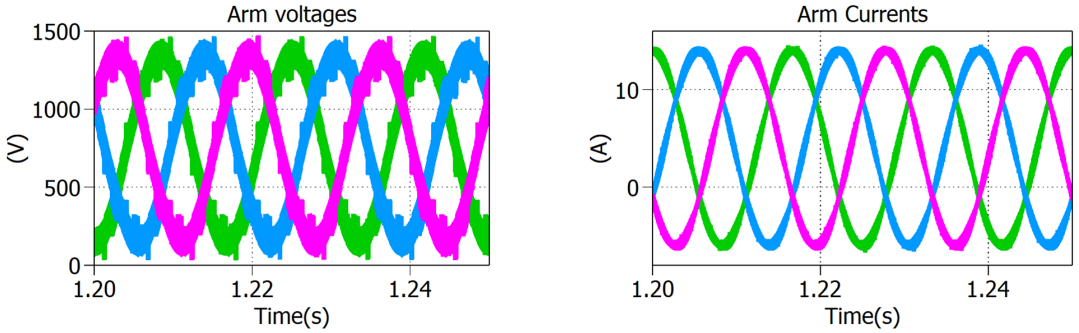
5.2.5 Simulation Results

The system parameters of a down-scaled traditional MMC are shown in Table 5.1.

Arm voltages and arm currents are shown in Fig. 5.10. SM capacitor voltages are shown in Fig. 5.11. Arm energy is shown in Fig. 5.12. From Fig. 5.10(b), it is apparent that the arm currents are almost sinusoidal and the 2^{nd} harmonic components have been eliminated due to the 2^{nd} harmonic PR controllers. Fig. 5.11(a) shows all the SM capacitor voltages while (b) only shows a zoom-in version of SM voltages of the upper arm of Phase A. The voltage differences between different SMs are slight which proves the effectiveness of the voltage balancing algorithm. Fig. 5.12(a) shows the MMC arm energy with an average value of 75 J. The arm energy before passing through the moving average is shown in Fig. 5.12(b), and fundamental and 2^{nd} harmonic energy ripple can be seen from the results.

Table 5.1: System Parameters Of A Down-scaled MMC Simulation

System parameters	Values
AC output voltage (line-neutral peak)	600 V
AC output frequency	60 Hz
DC link voltage	1.5 kV
Arm inductance	5 mH
Grid inductance	0.1 mH
SM capacitance	200 μF
Number of SMs per arm	3
Sampling frequency	20 kHz
System power rating	18 kW

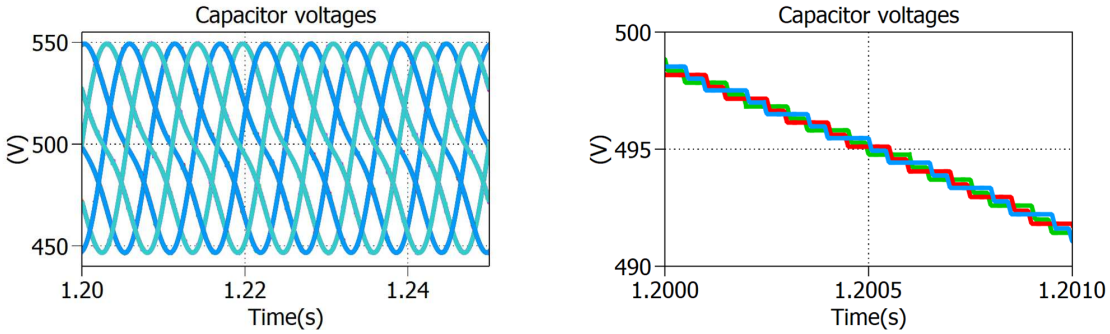


(a) (b)

Figure 5.10: (a) Simulation Results Of MMC Upper Arm Voltages Of Each Phase; (b) Simulation Results Of MMC Upper Arm Currents Of Each Phase

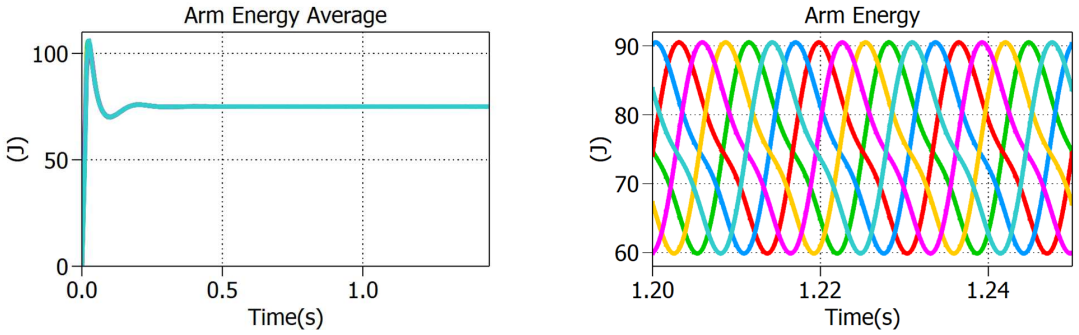
5.3 MMC Based VSD in a Pump-back System

A standard pump-back system adopted in this section is shown in Fig. 5.13 where the DC links of the two converters are tied together, and their AC sides are connected through inductors which represent the induction machine. The basic operating principle of a pump-back is that one of the MMC is controlled as a voltage source to provide a virtual grid. Another MMC is therefore controlled as a current source



(a) (b)

Figure 5.11: (a) SM Capacitor Voltages; (b) SM Capacitor Voltages Of The Upper Arm Of Phase A



(a) (b)

Figure 5.12: (a) MMC Arm Energy After Moving Average; (b) MMC Arm Energy Before Moving Average

which regulates the total power circulating in the system.

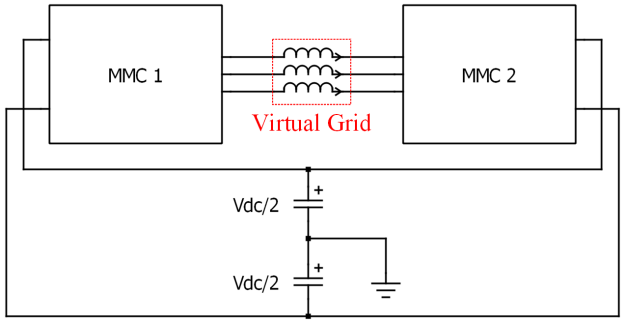
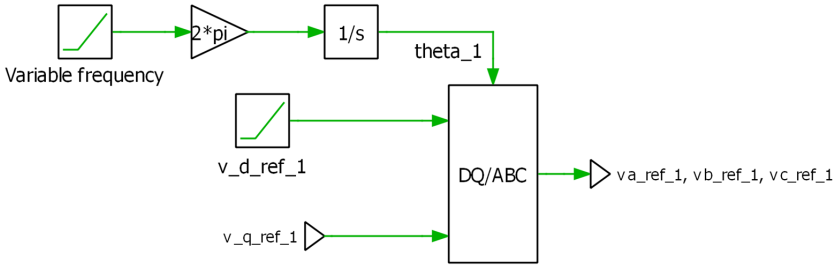


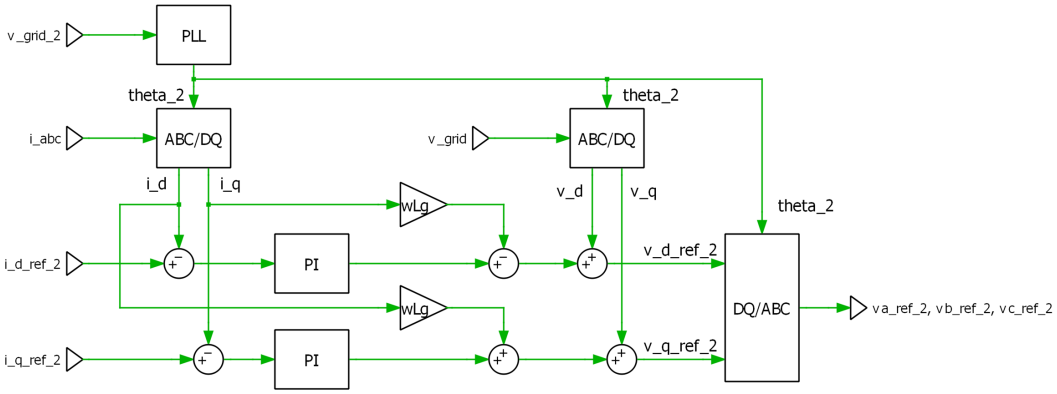
Figure 5.13: A Standard MMC Based Pump-back System Configuration

5.3.1 Control Strategies of the Two MMCs

Basically, the control of a pump-back system comes down to the control of the two converters. As mentioned in the last section, the two MMCs should implement different control strategies in order to avoid command conflict. In this case, MMC1 will be under voltage control mode while MMC2 is under current control mode. The MMC control strategy introduced in Section 5.2 is still valid here except that the fundamental current control loop of the two MMCs will be different. The control diagram of the two MMC fundamental current control loops is shown in Fig. 5.14.



(a)



(b)

Figure 5.14: (a) MMC1 Fundamental Current Control Loop; (b) MMC2 Fundamental Current Control Loop

In Fig. 5.14(a), variable frequency and variable amplitude control is used. The ramp signal represents the changing frequency and voltage amplitude where this voltage amplitude shares the same per unit value with output frequency. Fig. 5.14(b)

implements the same control strategy introduced in Section 5.2. However, since the inherent fundamental and 2^{nd} harmonic voltage ripple in SM capacitors which is inversely proportional to the operating frequency, the lowest system frequency determines capacitance. Without additional control methods, it is difficult for the pump-back system to start from zero frequency.

5.3.2 Moving Average of Capacitor Energy

As shown in Fig. 5.11(a), the capacitor voltage in each submodule will contain not only a DC value but also pulsating fundamental and 2^{nd} harmonic AC components. In order to perform the three energy loops, moving average must be used to extract the DC component of the instantaneous capacitor energy. However, the challenge is that if the output of the MMC is a variable frequency waveform, the period used to calculate the moving average is variable, which makes the control algorithm more complicated.

A new approach has been tested to achieve good performance for replacing the traditional moving average. Ideally, if ABC to $\alpha\beta$ transformation is used for three-phase sinusoidal signals with the same DC offset, the output signals will be pure AC signals without any DC offset. Then use the inverse transformation to get the AC components under ABC frame. Therefore, the average DC value can be calculated by subtracting the AC components from the original signals. In our case, the average value of SM capacitor has been kept close due to the capacitor voltage balancing algorithm. As a result, the performance of this method is good enough for the controllers. This method is illustrated in Fig. 5.15.

5.3.3 Simulation Results

The system parameters of an MMC based VSD are shown in Table 5.2.

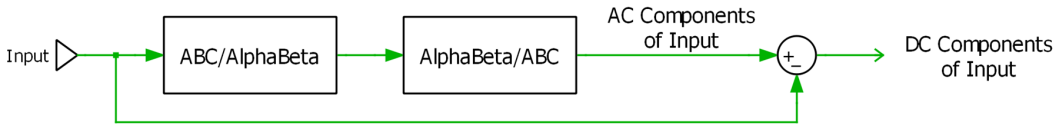


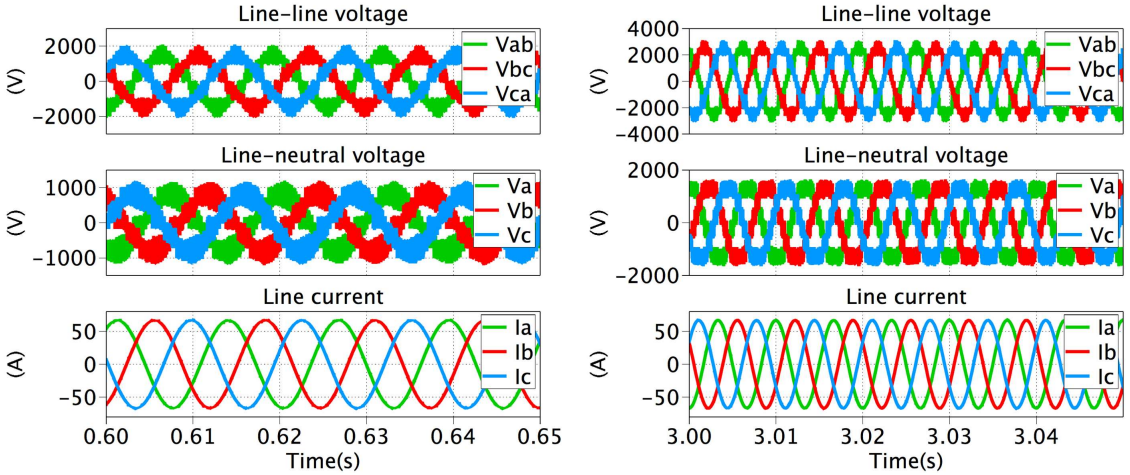
Figure 5.15: Illustration Of The Proposed Method For Moving Average

Table 5.2: System Parameters Of An MMC Based VSD In A Pump-back Simulation

System parameters	**Values**
AC output voltage (line-neutral peak)	1500 V
AC output frequency	150 Hz
DC link voltage	3 kV
Arm inductance	2 mH
Grid inductance	0.1 mH
SM capacitance	300 μF
Number of SMs per arm	3
Sampling frequency	20 kHz
System power rating	150 kW

The virtual grid voltage and current waveforms at different intervals are shown in Fig. 5.16(a) and (b). Fig. 5.16(a) shows the grid voltage and current between 0.6 and 0.65 sec while Fig. 5.16(b) shows the same voltage and current between 3 and 3.05 sec. It is apparent that the waveform frequency in Fig. 5.16(b) is higher than that in Fig. 5.16(a). Fig. 5.17 shows the DC link current flowing in each MMC and through the shared DC bus. The DC link currents in the two MMCs are close in amplitude but have opposite directions. And the amplitude is increasing when the system frequency goes up. The current on the shared DC link bus should contain only ripples, which proves that the active power is circulating between the two converters. Fig. 5.18 shows the six arm energy in MMC1. Fig. 5.18(a) shows the arm energy

waveform during the entire process with frequency going from low to its rated value. The arm energy ripple is inversely proportional to the operating frequency, and this characteristic can be clearly seen from Fig. 5.18(a). A zoom-in version of arm energy is shown in Fig. 5.18(b). The capacitor voltage waveform is shown in Fig. 5.19. The capacitor voltage ripple shares the same feature with the arm energy. And Fig. 5.19(a) shows the capacitor voltage ripple becomes smaller when the system frequency goes up. Fig. 5.19(b) is a zoom-in version of Fig. 5.19(a) with an average value of 450 J. It also indicates the effectiveness of voltage balancing algorithm implemented in the control scheme. The voltage deviation of SM capacitors in the same arm will be controlled within a small range to ensure stable operation of the system.



(a) (b)

Figure 5.16: (a) Virtual Grid Line-line, Line-neutral Voltage And Line Current Between 0.6-0.65 s; (b) Virtual Grid Line-line, Line-neutral Voltage And Line Current Between 3.0-3.05 s

5.4 Operation Principles and Control Strategies of a MIMC

5.4.1 MIMC Topology and Operation Principles

The proposed MIMC topology is shown in Fig. 5.20. The MIMC has much higher power density than the traditional MMC. It inherits the structure of MMC

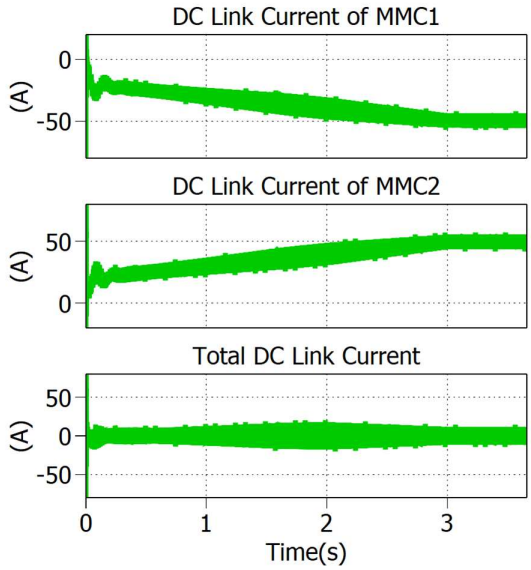
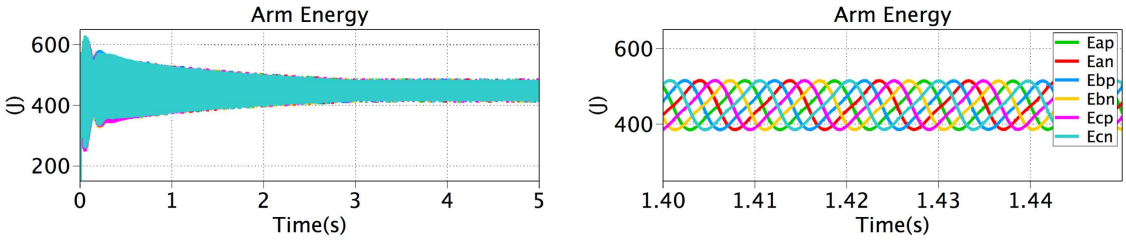
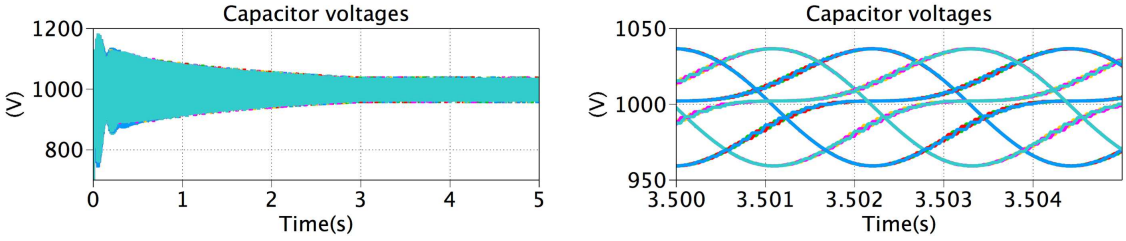


Figure 5.17: Simulation Results Of (From Top To Bottom) DC Link Current Of MMC1, DC Link Current Of MMC2, And Common DC Link Current



(a) (b)

Figure 5.18: (a) Arm Energy Of MMC1 During The Entire Operation Time; (b) ZoomED-in Arm Energy Of MMC1



(a) (b)

Figure 5.19: (a) SM Capacitor Voltages During The Entire Operation Time; (b) Zoomed-in SM Capacitor Voltages

but replaces the half-bridge modules by the new Isolated H-Bridges (IHBs). The fundamental frequency and 2^{nd} harmonic frequency current in the MMC module

capacitor have been completely eliminated through connecting the secondary sides of the IHBs at the same level together. The isolation transformer (with the insulation level equal to the full DC link voltage) in the IHB module of the MIMC enables the parallel connection. These parallel connections are not allowed in the traditional MMC due to the significant different voltage potentials of the SMs. To carry only switching frequency ripple, the module capacitance is reduced by more than ten times and its voltage waveform becomes flat. The absence of the low-frequency current also enables the replacement of the capacitor by the energy storage devices which have extremely high loss at low frequency, which makes the inverter be able to provide the contingency reserves and frequency regulations to the grid.

One of the major advantages of MIMC lies in the size reduction of DC link capacitors in each IHB due to fundamental and 2^{nd} harmonic elimination, which leads to higher power density than that of a traditional MMC. Another breakthrough is the integration of distributed energy storage devices without a high boost ratio high voltage DC/DC converter stage to achieve higher bandwidth, higher power density, higher efficiency and lower cost. The storage can provide energy and power to the ac grid without affecting the dc distribution line voltage/current and vice versa. Table 5.3 shows the quantitative metrics that compares the proposed MIMC with the traditional MMC, A theoretical 150 kW system with 1.7 V/72 A SiC MOSFET has been chosen. From this table, the following conclusions can be made based on the data: (1) The proposed MIMC has significant power density improvement compared to traditional MMC. The MIMC with supercapacitors has lower power density because of the large size of the integrated supercapacitors; (2) The efficiency of MIMC will be a slightly lower than MMC due to the additional losses of the DC/DC converter; (3) The MIMC has a larger number of devices than MMC, which could result in a slightly lower reliability and higher cost. However, this could be mitigated by simply

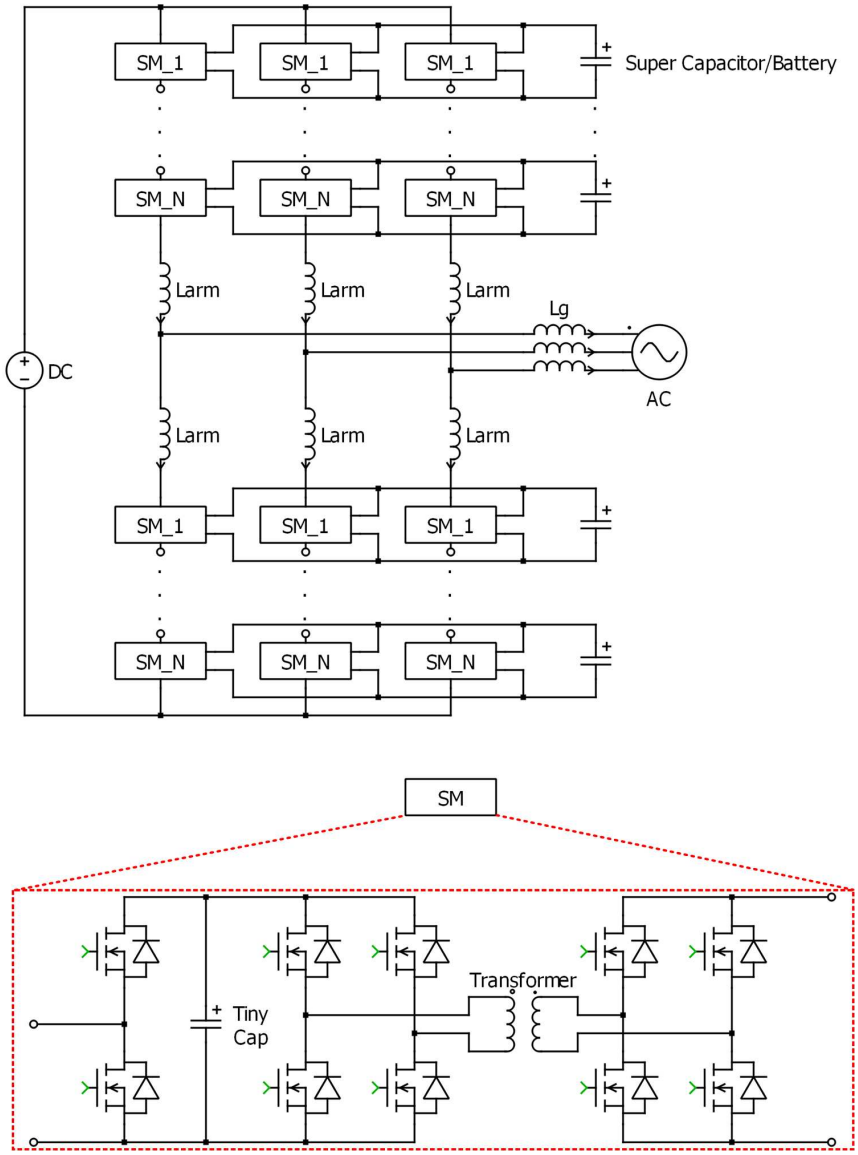


Figure 5.20: Topology Of The Proposed MIMC

increasing the number of redundancy; (4) The required arm inductor in the MIMC is smaller than that in the MMC.

Other benefits brought by the proposed topology are: (1) Lower Total Harmonic Distortion (THD) and smaller size of arm inductor due to the absence of 2^{nd} harmonic components in the arm current; (2) High reliability can be achieved when redundancy is applied; (3) The proposed topology can maximize the efficiency of the storage

Table 5.3: Quantitative Metrics Of Proposed MIMC Compared With Traditional MMC

Mtric	**MMC**	**MIMC**	**MIMC with supercapacitors**
Power	150 kW	150 kW	150 kW
Voltage	6 kV DC, 3.3 kV AC	6 kV DC, 3.3 kV AC	6 kV DC, 3.3 kV AC
Module DC link voltage	1 kV	1 kV	1 kV
Efficiency	98%	97%	96.5%
Power density	115 W/inch^3	634 W/inch^3	87 W/inch^3
Switching frequency	20 kHz	20 kHz	20 kHz
Device type and count	C2M0025170D*96	C2M0025170D*192	C2M0025170D*192
Device specs	1.7 kV, 72 A	1.7 kV, 72 A	1.7 kV, 72 A
Film cap per module	107 μF	5.4 μF	5.4 μF
Film cap type and count	1300 V/14.5 A/12 μF, B32776G1126, Quantity: 432	1300 V/5 A/2.7 μF, B32776T1275, Quantity: 96	1300 V/5 A/2.7 μF, B32776T1275, Quantity: 96
Supercap type and count	N/A	N/A	VHC2R3127QG, 300 F/2.3 V/3 A, Quantity: 2400
Supercap size	N/A	N/A	1488 inch^3
Total volume	1329 inch^3	236 inch^3	1724 inch^3

by creating a flexible interface voltage through regulating the transformer turns ratio, while still keeping the minimum number of modules to maintain the inverter simplicity, reliability and efficiency, which results in high energy storage operating efficiency; (4) The proposed topology is also able to parallel and ground partial or all the batteries/supercapacitors in order to reduce the floating voltage of the battery thus preventing the leakage current to the ground; (5) The proposed topology can prevent the high discharge current from the energy storage by turning off the DAB unit in the IHB module, during the dc bus short circuit fault.

5.4.2 Control Strategies of the MIMC

Similar to the MMC, the proposed MIMC is a six-arm inverter with cascaded modules and an inductor in each arm and is able to convert the input dc voltage into a multi-level ac voltage. At each moment, each phase has half modules being inserted and half modules being bypassed. Therefore, the control strategies of MIMC under normal operation are similar to those of MMC except that the phase and arm energy balance are automatically achieved since the fundamental and 2^{nd} harmonic components in the SM capacitor voltages have been eliminated. Hence, common-mode and differential-mode circulating current control are omitted. The total energy balance which regulates DC link current is still needed to balance the power between AC and DC side. For inner current loops, only DC link current and fundamental AC current control are retained. The capacitor voltage balance is also necessary to avoid large voltage deviation between different capacitor in different modules. Note that in the energy loop, moving average is no longer needed since the capacitor voltage is flat, which makes it convenient to control under variable frequency applications.

For MIMCs which are operating as VSDs, the control strategy is similar to that of an MMC based VSD where the per unit frequency and voltage amplitude commands

are shared between to converters. A pulse load in the DC bus is also considered in this work. Especially in the Navy application, pulse load application is commonly used to provide enough energy within a very short time. This can be realized by integrating the distributed energy storage devices, such as supercapacitors, into the MIMC. The control strategy will be the same as that of an MIMC under normal operation except that the energy between DC and AC side of MIMC are not equal. Therefore, the total energy balance is not needed. Only a DC link current command (a pulse in this case) is needed. The converter will automatically discharge energy from its SMs. Another important point is that the change in DC link current has no effect on the AC side of MIMC.

5.4.3 Simulation Results

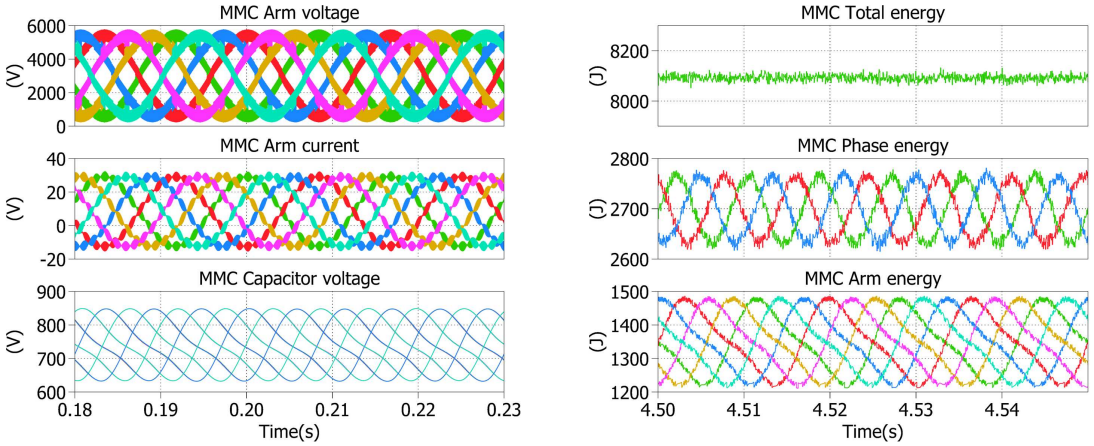
In order to show the advantages of MIMC over the traditional MMC, three simulations have been conducted which are traditional MMC simulation, MIMC simulation, MIMC with integrated supercapacitor simulation. Table 5.4 shows the system parameters used in these three simulations.

Fig. 5.21, 5.22 and 5.23 show the simulation results of MMC, MIMC, and MIMC with supercapacitors (MIMC+SC), respectively. The waveforms of each figure show the total energy of all the SM capacitors, phase energy, arm energy, arm voltage, arm current, and capacitor. The AC terminal voltage and current of the three topologies are similar. However, the capacitor voltage is different. A large fundamental and 2^{nd} harmonic component in capacitor voltage can be seen from the results of MMC while the capacitors of MIMC have a relatively flat voltage waveform even the capacitance is much smaller than that in the MMC. Flatter voltage can be observed in MIMC+SC topology. The phase energy and arm energy ripples are almost the same for MIMC and MIMC+SC topologies since the energy ripple is only dependent on the

Table 5.4: Simulation Parameters Of Traditional MMC, MIMC, And MIMC With Supercapacitors

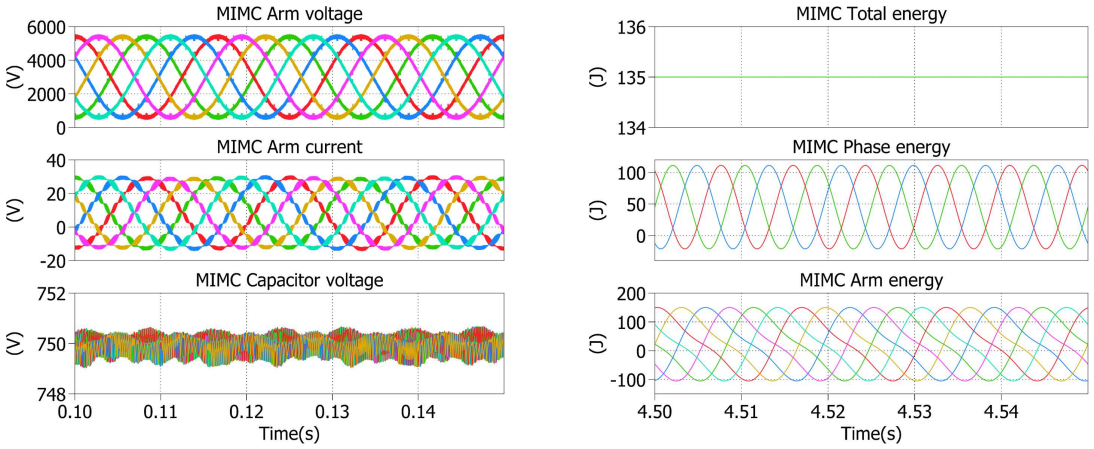
Metric	MMC	MIMC	MIMC with supercapacitors
AC output voltage (line-neutral peak)	2400 V	2400 V	2400 V
AC output frequency	60 Hz	60 Hz	60 Hz
DC link voltage	6 kV	6 kV	6 kV
Arm inductance	2 mH	2 mH	2 mH
Grid inductance	0.1 mH	0.1 mH	0.1 mH
SM capacitance	600 μF	10 μF	10 F
Number of SMs per arm	8	8	8
Sampling frequency	20 kHz	20 kHz	20 kHz
System power rating	150 kW	150 kW	150 kW

AC terminal voltage and current. However, MIMC has smaller average energy since the capacitance used in this topology is small.



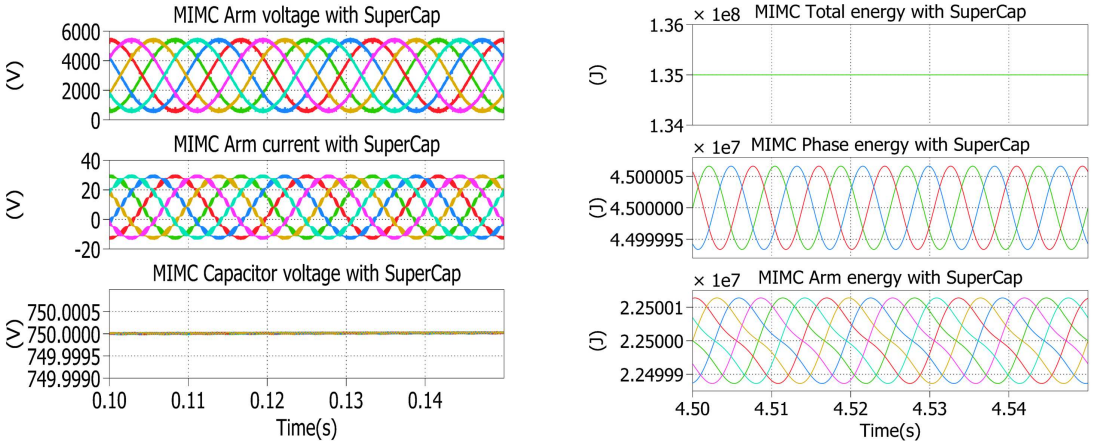
(a) (b)

Figure 5.21: (a) Arm Voltage, Arm Current And SM Capacitor Voltages Of A Traditional MMC; (b) The Total Energy, Phase Energy And Arm Energy Of A Traditional MMC



(a) (b)

Figure 5.22: (a) Arm Voltage, Arm Current And SM Capacitor Voltages Of The MIMC; (b) The Total Energy, Phase Energy And Arm Energy Of The MIMC

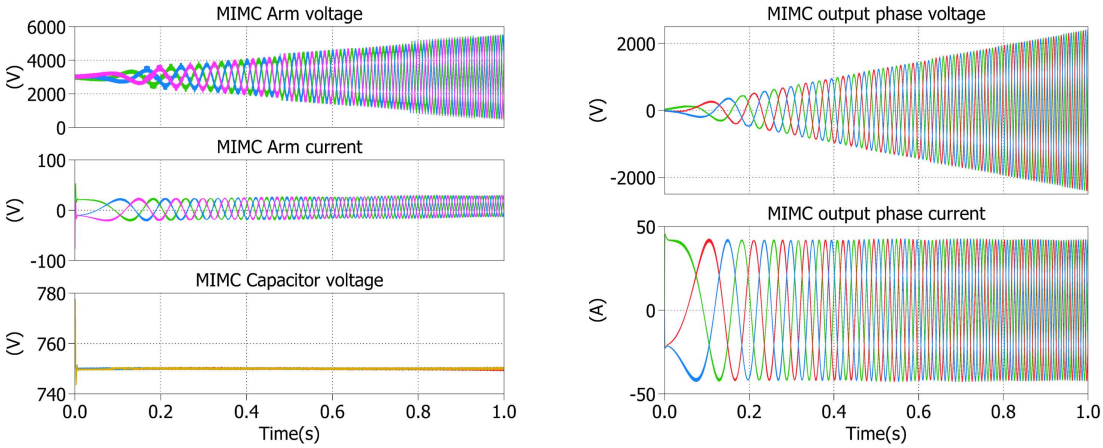


(a) (b)

Figure 5.23: (a) Arm Voltage, Arm Current And SM Capacitor Voltages Of The MIMC With Supercapacitors; (b) The Total Energy, Phase Energy And Arm Energy Of The MIMC With Supercapacitors

One important advantage of the proposed MIMC is that it is able to start from zero frequency with a small capacitance. This could be an advantage if the converter is connected to a generator and is required to operate as a turbine starter. Fig. 5.24(a) shows arm voltage, arm current and SM capacitor voltages. Fig. 5.24(b) shows the output AC voltage and current. Total energy and arm energy are presented in Fig. 5.25. It can be seen from Fig. 5.24(b) that the output AC voltage amplitude goes up

as the output frequency increases. In addition, the energy ripple decreases because it is inversely proportional to the frequency. The SM capacitor voltages remain constant even when the frequency is very low.



(a) (b)

Figure 5.24: (a) Arm Voltage, Arm Current And SM Capacitor Voltages Of The MIMC; (b) Output Phase Voltage And Current Of The MIMC

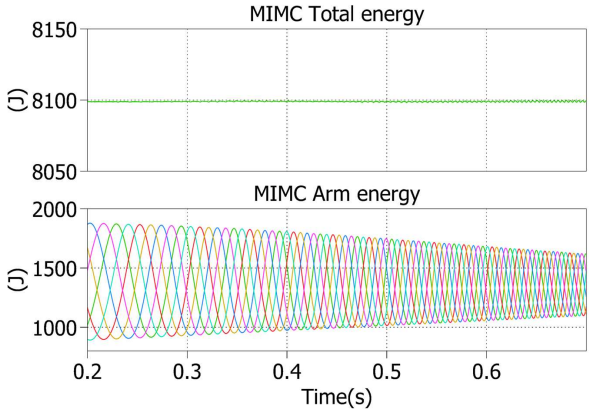
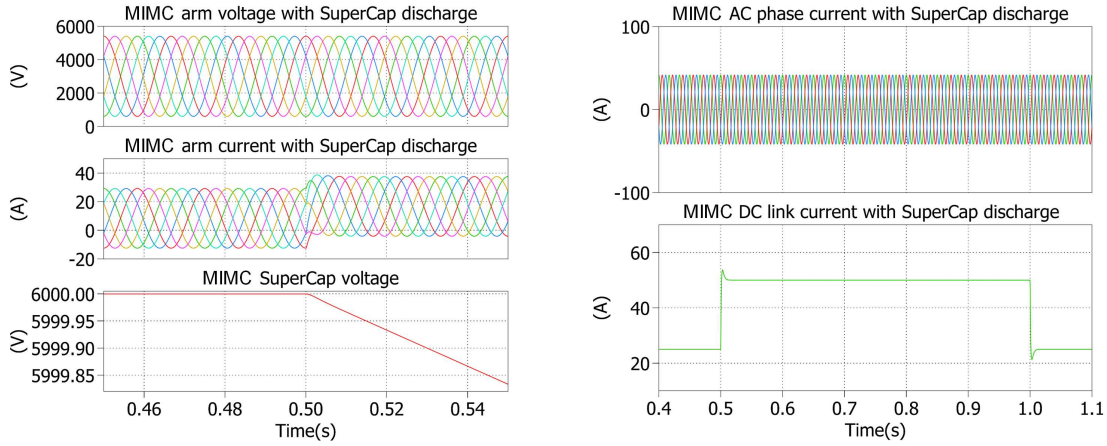


Figure 5.25: The Total Energy And Arm Energy Of The MIMC

In addition, MIMC with supercapacitors has been simulated under a pulse command in the DC link current reference. Fig. 5.26(a) shows the arm voltage, arm current and supercapacitor voltage from top to bottom. Fig. 5.26(b) shows the AC terminal current and DC link current. The pulse current command can be directly

sent to the DC control loop (without the total energy outer loop) as a command. The results show that during the pulse load, the supercapacitor voltage can keep relatively constant thus the AC side of the circuit will feel almost nothing about the DC link disturbance, thus protecting the generator and its prime-mover. In addition, the re-charging of the supercapacitor can come from either the AC or DC side.



(a) (b)

Figure 5.26: (a) Arm Voltage, Arm Current And SM Capacitor Voltages Of The MIMC With Supercapacitors Under A Pulse Load; (b) Output AC Voltage And DC Link Current Of The MIMC With Supercapacitors Under A Pulse Load

5.5 Conclusions and Future Work

In this chapter, basic MMC topology and control strategies including three outer energy loops, three inner current loops, and voltage balancing control are discussed. In order to test MMC as a variable speed motor drive, a pump-back system has been developed and simulated. To overcome the drawbacks of the traditional MMC which has large fundamental and 2^{nd} harmonic voltage ripple in SM capacitor voltages, a MIMC with SM capacitors on the same level connected has been proposed and simulated. This type of multilevel converter is able to eliminate the voltage ripple so that it is perfect for zero-frequency start-up for a VSD. In addition, MIMC operation

with integrated supercapacitors has been simulated.

Future work will focus on the control verification by using Digital Signal Processor (DSP) in both MMC and MIMC. Fig. 5.27 and 5.28 show the designed submodule prototype of a conventional MMC and a MIMC, respectively. The construction of the entire converter is in progress.

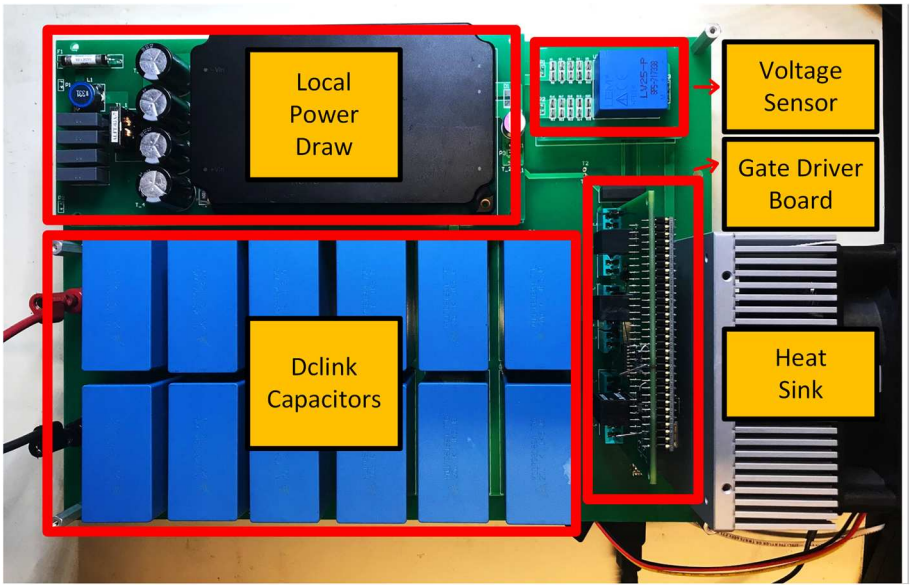


Figure 5.27: MMC Submodule Prototype

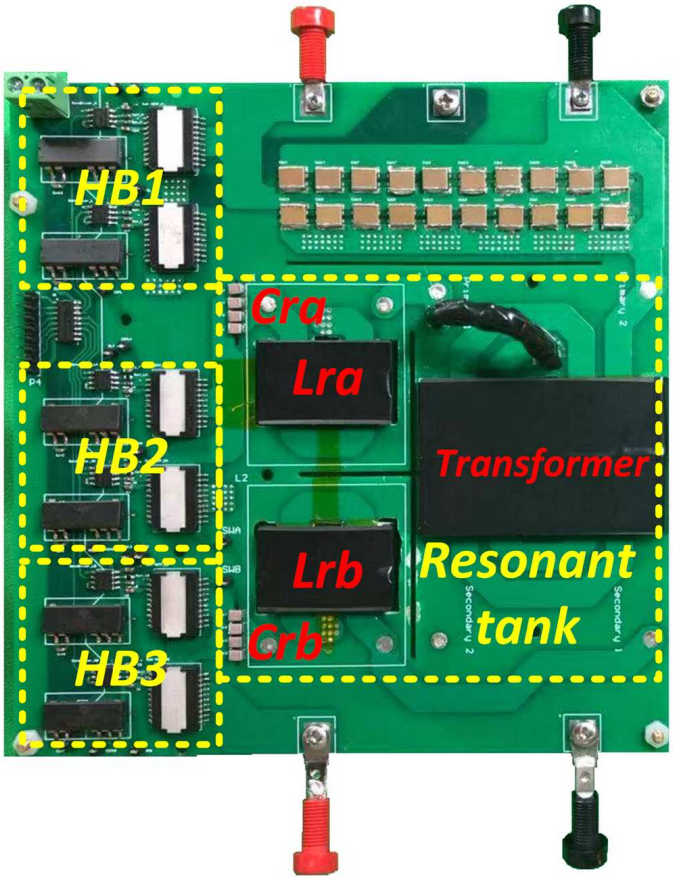


Figure 5.28: MIMC Submodule Prototype

Chapter 6

A HIGH CURRENT HIGH POWER DENSITY MOTOR DRIVE FOR A 48-VOLT BELT-DRIVEN STARTER GENERATOR (BSG) SYSTEM

6.1 Introduction

The 48 V Belt-Driven Starter Generator (BSG) system has been developed for cost-efficient mass hybridization. Its capability of advanced stop-start, coasting and electric boost can help reduce CO2 emission by up to 10%. For a mild-hybrid application, the 12 V alternator is replaced by the 48 V electric motor which is directly mounted to the engine via a belt [131]. Interior Permanent Magnet Synchronous Machines (IPMSMs) are commonly used in this BSG system due to their high efficiency, high power density, wide speed range operation, and maintenance-free characteristics [132, 133].

Inverter is an essential component which needs to be compactly integrated with the BSG motor. A typical topology of a 48 V BSG inverter is shown in Fig. 6.1. The power supply is 48 V DC. The peak power can go up to 12 kW and last for several seconds. The peak output current can be up to 300 A. The challenge on the hardware design is to achieve 3 key targets which are well-balanced current among paralleled MOSFETs, low drain-source voltage (V_{ds}) spike during turn-off transient, and small thermal resistance of the heatsink system [134]. Most of the existing literature focus on the switching characteristics of the BSG power stage. [135] presents a design and measurement of an integrated H-bridge and a compact DC/DC converter for a commercial 48 V BSG system . [136] presents a BSG inverter prototype with 6 MOSFETs connected in parallel in each arm and [137] uses 8 devices instead. Indi-

vidual gate resistor for each MOSFET is used in both papers to suppress circulating current among paralleled switches and to reduce the drain-source voltage overshoot in high-current operating conditions. Thermal behavior of the inverter is also included in [136] showing that individual gate resistor helps even current sharing. However, [136] and [137] only show switching waveforms of the MOSFETs, and no inverter operation waveforms are provided. [134] illustrates a design of 48 V BSG inverter using 4 MOSFETs in parallel in each inverter arm. Besides individual gate resistors, an Insulated Metal Substrate (IMS) board has been used to provide smaller temperature difference among paralleled devices compared with [136]. However, the power density of the prototype has been compromised due to the height of the DC link capacitors and no operational waveforms are provided.

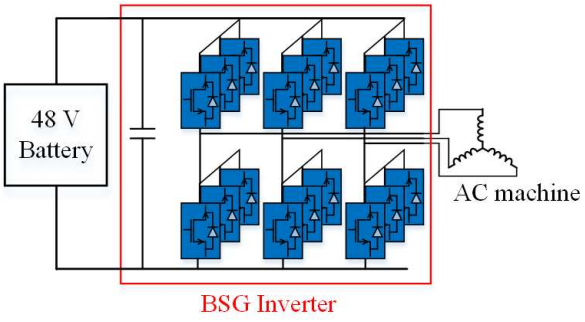


Figure 6.1: Circuit Configuration Of A 48 V BSG Inverter

In order to test the BSG inverter hardware, a simple and robust IPM control strategy should be implemented in the controller. The control algorithm should be able to achieve stable and robust field-weakening operation [138–140]. [141–143] adopt an additional DC/DC boost converter to raise the DC bus voltage so that the operating speed can be expanded. However, the additional switches and passive components lower down the power density of the inverter. In terms of current controllers, [144] directly uses equations to compute d-axis and q-axis current commands and [145] proposes to use one current regulator to decouple the two current components. [146–148]

utilize either phase current error or inverter voltage error to determine the amount of demagnetizing current in d-axis. However, the methods in [144–148] fail to take into account the nonlinearity of the stator flux linkage, which can lead to unstable operation of the controllers. The nonlinear effect can be accommodated by inserting look-up tables [149] and by using curve fitting equations based on Finite Element Analysis (FEA) results of a physical IPM machine [150–153]. However, these methods are not adaptive to machine parameter changes and DC bus voltage variation since the look-up tables and the curve fitting equations cannot be tuned online.

The research gaps have been identified and the main contributions of this study are illustrated from the following aspects. Firstly, this study provides the readers with not only a complete design guideline of a 48V BSG inverter but also an economical and feasible approach to test the designed prototype under rated operating conditions without using a real machine, which is missing in the existing literature. Secondly, improvements have been made in terms of both hardware design and IPM control strategy in order to make the prototype more reliable and robust so that it can be more readily accepted by industry. From hardware perspective, this study elaborates the hardware design considerations of a low-voltage high-current high power density three-phase 48V BSG inverter to address the challenges of even current distribution among paralleled MOSFETs, small drain-source voltage spike and good thermal dissipation. Appropriate device selection in order to satisfy the high-current requirement in such applications is missing in the existing literature. As a result, an iterative method for selecting MOSFET with an ultra-low on-state resistance (R_{dson}) has been presented. The power density of the BSG inverters in the previous literature has been compromised due to the large size of the DC link capacitors. In the proposed design, multiple low-profile electrolytic capacitors have been used so that the power density of the prototype has been increased. Moreover, none of the previously published

papers covers the topic of gate driver and microcontroller ICs which are compliant with automotive standard and specialized for electric vehicle applications. In the proposed prototype, the gate driver ICs TLE9180 and the microcontroller TC1782 which are specifically designed for electric vehicles have been implemented. From the aspect of IPM control strategy, an improved IPM control strategy and a pump-back system have been implemented, which facilitates the validation of the designed inverter hardware under rated conditions without using a real motor. The control algorithm automatically adjusts the onset of field-weakening by using an additional inverter voltage loop, which makes it adaptive to machine parameter changes and DC bus voltage fluctuation. At the same time, the nonlinearity of the stator flux linkage has been taken into consideration by using curve fitting equations so that the control accuracy is improved. In addition, the improved control scheme is suitable for both speed control and torque control. A three-phase BSG inverter prototype with a peak power of 12 kW has been built based on current industrial requirements, and the prototype power density has reached 20.3 kW/L.

The rest of the chapter is organized as follows. A detailed hardware design procedure for a 48 V BSG inverter is firstly presented in Section 6.2 including device selection, device paralleling, DC link capacitor selection, IMS board and heatsink selection, and an introduction to automotive standard gate driver ICs and microcontrollers for this application. Section 6.3 shows a brief operation analysis of an IPM machine and an optimized operation curve which not only simplifies the control but also keeps a relatively large output torque. A constant current based control method is implemented in Section 6.4. In order to test the performance of the designed inverter hardware and the improved control method, a pump-back test bench is introduced in Section 6.5 based on a virtual machine concept. PLECS simulations and hardware experiments are presented in Section 6.6 and 6.7, respectively, to show not only the

continuous operation of the prototype but also the robustness of the improved control technique under machine parameter changes and DC bus voltage variation.

6.2 Hardware Design Considerations

The three challenges for the inverter hardware design are current sharing among paralleled devices, V_{ds} spike suppression at 300 A peak current, and thermal management under 100 ℃ environment temperature. In addition, the high motor speed (600 Hz) at limited switching frequency (12 kHz) and high efficiency target also superimpose challenges to the inverter design. A three-phase motor drive inverter prototype with a peak power of 12 kW has been constructed in the lab for an industry-funded project. The system requirements and the specifications of the final design are presented in Table 6.1.

6.2.1 Power Device Selection

The power device selection includes four aspects which are drain-source voltage rating, drain current rating, on-state resistance, and device package.

(a) Device voltage rating selection

The avalanche breakdown voltage of an Infineon OptiMOS transistor is slightly higher than its voltage rating due to a typical safety margin. The voltage rating is defined at room temperature. Breakdown voltage shows a strong positive temperature coefficient in Fig. 6.2(a) [154]. Breakdown voltage at typical operation temperature of 100 120 ℃ is approximately 7% higher than its rated voltage. Another criterion for selecting the voltage rating of a MOSFET is the voltage spike. During turn-off transient, the voltage across drain and source can reach a much higher value than that in steady state due to parasitic inductance

Table 6.1: Key Parameters For A 48 V BSG System And The Final Prototype Design Specification

System requirements	
Structure	Integrated motor and inverter
Dimension	$\leq$ D155 mm $*$ L180 mm
Mass	$\leq$ 10.5 kg
Continuous torque	10 Nm
Continuous power	5 kW
Peak torque	$\geq$ 20Nm, @ 0-1500 rpm, 20 s
Peak motor power	$\geq$ 8 kW @ 48V, lasting 10 s
Peak generator power	$\geq$ 10 kW @ 48 V, lasting 10 s
Maximum mechanic speed	12000 rpm
Efficiency	$\geq$ 83%, measured at 25 ℃
Operation temperature	40 $\sim$ 100 ℃
Cooling	Forced air cooling
Specifications of the final design	
DC bus voltage	36 V $\sim$ 52 V (rated @ 48 V)
Continuous phase current	200 A peak
Peak phase current	300 A peak
Switching frequency	12 kHz
dV/dt	$\leq$ 1 V/ns
Efficiency of the inverter	98.5%
Power density of the inverter	20.3 kW/L

in the circuit. The maximum steady state voltage during turn-off should not exceed 70% to 90% of the rated voltage. In this project, a maximum junction temperature of 150 ℃ is considered for voltage rating deviation, and a 50% voltage spike is assumed based on possible dv/dt. Finally, a 100 V device is

selected in this design.

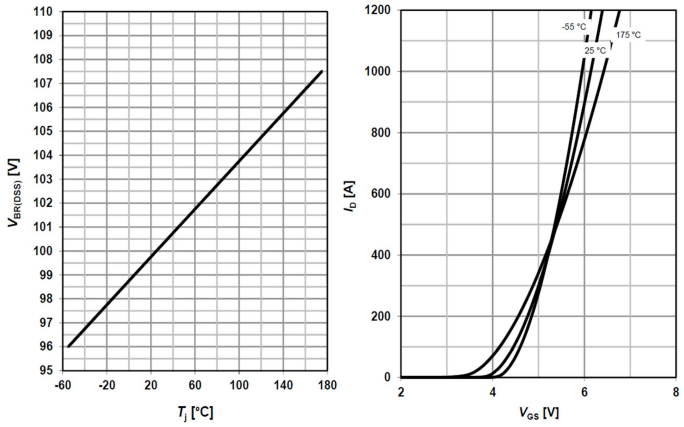


Figure 6.2: Characteristic Curves Of Infineon MOSFET IAUT300N10S5N015. Left: Breakdown Voltage As A Function Of Junction Temperature: $V_{DS} = f(T_j)$; Right: Drain Current As A Function Of Gate-Source Voltage Under Different Temperatures: $I_D = f(V_{gs})$

(b) Operating junction temperature selection

Similar reliability rules can be applied to the selection of operating junction temperature of the MOSFET. The operating junction temperature should not exceed the maximum value specified in the datasheet. Pushing the operating temperature to its maximum is not reasonable. In order to achieve high forecasted reliability, the operating temperature should be lower than the maximum value. For example, reducing the junction temperature by 30% will improve the Mean Time Between Failure of the OptiMOS by an order of magnitude. On the other hand, the Rdson increases with junction temperature. It leads to an increase in conduction power loss. For these reasons, a derating factor between 70% and 90% of the maximum junction temperature is used. In this design example, the maximum temperature of the device is 175 ℃ , and 85% of the maximum temperature, which is 150 ℃, has been chosen as the operating temperature. The highest environment temperature is 100 ℃, which means the

maximum allowable device temperature rise is 50 ℃ . It is found in the experiments that the temperature rise is only around 20 ℃. Therefore, the current and voltage rating selected based on 150 ℃ is enough for continuous operation of the inverter.

(c) Device current rating selection

In the high-current applications, the MOSFET is not being stressed up to its maximum current rating due to poor cooling conditions. Designer prefers to take advantage of low R_{dson} of the MOSFET in order to reduce power loss. Usually, a MOSFET with selected low R_{dson} has a higher current rating than needed in the application. Nevertheless, it is useful to check the Safe Operating Area of the selected MOSFET. On the other hand, gate-source voltage (V_{gs}) should be high enough to completely turn on the MOSFET. The transistor should be able to carry the maximum pulse current in the converter under all conditions. Especially during start-up or short circuit, the supply voltage for the control IC can fall close to under voltage lockout limit. Some modern control ICs have an under voltage lock out of approximately 7 V. The gate-source voltage of MOSFET can be less than 5 V, if we consider the voltage drop on the output stage of the IC. MOSFET should be able to carry the required current without an increase of drain-source voltage at a given gate-source voltage. In this design, the transfer characteristic from the datasheet (Fig. 6.2(b)) can be used to verify device current capability when V_{gs} becomes low. If the MOSFET does not meet the requirements, another transistor with higher current rating should be selected.

(d) R_{dson} selection

The most complicated task is to choose a device with the correct R_{dson}. The

selection of R_{dson} is based on the maximum allowable power dissipation of a particular application and the maximum junction temperature of the MOSFET. Here it is assumed that the switching frequency is fixed and that the space for heat sink is known which means we can estimate the thermal resistance of the heat sink (R_{sink}).

Step 1: Calculate how much power loss is allowed for a given heat sink and a specific junction temperature based on the efficiency target.

Step 2: Calculate the required R_{dson} satisfying the maximum power loss from Step 1. At this point we already know the value of the maximum allowable power dissipation. We also know the circuit topology and the drain current waveform. Therefore, we can calculate the value of R_{dson} which satisfies the maximum power loss. For the first iteration we will consider only conduction loss because we do not know the MOSFET type yet. The switching loss strongly depends on the specific MOSFET device. For this reason, the switching loss will be skipped for now and be checked in the following steps.

Step 3: Select an OptiMOS with pre-calculated R_{dson} in Step 2. Note that instead of using room temperature, the junction temperature which is specific for a particular design (usually between 110 ℃ and 120 ℃) should be used.

Step 4: Calculate the total power loss for the selected OptiMOS transistor in Step 3. Now we have enough information to calculate the total power loss for the selected OptiMOS transistor under particular operating condition. Since we know the exact transistor type, we will be able to calculate the switching loss for a given switching frequency.

Step 5: Recalculate the maximum power dissipation for the selected OptiMOS. With the junction to case thermal resistance of the selected OptiMOS device,

it is possible to make the calculation of maximum allowable power dissipation more precisely. This step can help to skip one of the iterations that will be explained in Step 6.

Step 6: Compare the total power loss calculated in Step 4 for the selected OptiMOS with the maximum allowable power dissipation from Step 5. If the total power loss from Step 4 is lower than the maximum allowable power dissipation from Step 5, then the selected OptiMOS meets the requirements. In case that the total power loss from Step 4 is higher than the maximum allowable power dissipation from Step 5, select a new device from the OptiMOS family with a lower R_{dson}. Then repeat Steps 4, 5 and 6. Another possible approach would be to adjust the heat sink. To speed up the iteration process, the drain current versus the switching frequency chart, as well as output power versus the switching frequency chart can be used as a pre-selection of the MOSFET type.

Particularly in this project, for Step 1, the designed junction temperature is 150 ℃, and the maximum environment temperature is 100 ℃. Since the system efficiency target is 98.5% and the power under continuous operation is 5 kW, the allowable system power loss is around 75 W in the worst case. The heatsink needs to have a super low thermal resistance to dissipate this high amount of power loss. Therefore, an IMS board is used instead of a normal PCB board. For Step 2, when calculating the conduction loss, R_{dson} should be considered as a function of junction temperature. When calculating the switching loss, both E_{on} and E_{off} strongly depend on the value of the drain current. E_{on} is dominated by the commutated diode instead of the MOSFET. The relationship between E_{on}, E_{off}, and the drain current can be represented as a polynomial function using curve-fitting technique. The switching energy is also a function of

gate resistor. The recharging speed of OptiMOS capacitance can be controlled by a gate resistor. It influences the switching time and correspondingly the switching loss. The E_{on}/E_{off} versus gate resistor curves are almost linear. Therefore, if the gate resistor used in the hardware is different from the value on the datasheet where E_{on} and E_{off} are claimed, a bias plus a corrective factor needs to be applied. The drain-source voltage also has an effect on the device switching behavior. The dependence of switching loss on the drain-source voltage is almost linear. In our case, when the DC link voltage varies, a bias plus a corrective factor needs to be applied to E_{on} and E_{off}.

After the six-step iteration, the Infineon Automotive OptiMOS transistor I-AUT300N10S5N015 has been selected as shown in Table 6.2. Three devices are connected in parallel to undertake a continuous current of 200 A and a peak current of 300 A at the designed junction temperature of 150 ℃. This device is featured with ultra-low R_{dson}, which is good for lowering the device loss in high-current condition, and at the same time, reducing the temperature rise. The maximum operating voltage for this BSG application is 52 V. But twice the voltage has been selected for the device to overcome the high frequency resonance ripple on V_{ds} caused by dv/dt and large current. A gate driver voltage of 12 V is selected.

6.2.2 Paralleling OptiMOS transistors

The major challenge for paralleling OptiMOS transistors is the static and dynamic unbalance in current sharing. The second challenge is the destructive high-frequency oscillation. The first problem is due to the asymmetry of R_{dson} or the difference in the gate voltages. The second problem is due to slight imbalance in gate thresholds or circuit parasitic [155]. Because the parasitic determines the high frequency current

Table 6.2: Infineon Automotive OptiMOS Transistors

Device Part NO.	V_{ds}	R_{dson}	I_{dmax}	**Operating Temp**
IAUT240N08S5N019	80 V	1.9 mΩ	240 A	-55 ~ 175 ℃
IAUT300N08S5N014	80 V	1.4 mΩ	300 A	-55 ~ 175 ℃
IAUT300N08S5N012	80 V	1.2 mΩ	300 A	-55 ~ 175 ℃
IAUT165N10S5N035	100 V	3.5 mΩ	300 A	-55 ~ 175 ℃
IAUT300N10S5N015	100 V	1.5 mΩ	300 A	-55 ~ 175 ℃

flow. For static and dynamic current sharing, matched R_{dson}, perfectly symmetrical circuit layout, and matched gate thresholds are essential. In addition, some strategies can be applied to mitigate the unbalance or oscillation effect.

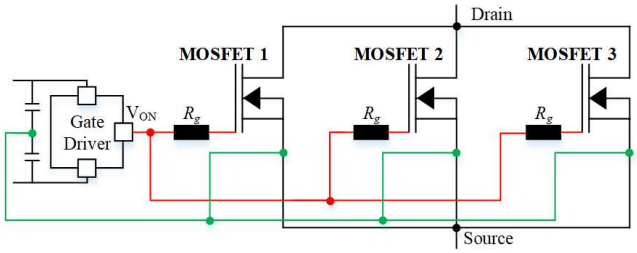


Figure 6.3: Gate Driver Output Circuitry For Three Paralleled MOSFETs In The Same Arm

Fig. 6.3 shows the gate driver output circuitry for paralleled OptiMOSs in each arm. All the gates of the paralleled devices are driven by a single gate driver IC, and each OptiMOS has its own gate resistor. Large gate resistors are chosen to suppress potential circulating current in different gate loops. The gate resistor selection is also constrained by the required dv/dt and the maximum switching loss. Fortunately, the requirement of dv/dt in this application is below 1 V/ns. And the switching loss is low as well due to the low DC voltage. Thus, a 15 Ω gate resistor can be selected. As shown in Fig. 6.5, the currents are well balanced so that the temperature difference

among the paralleled devices is within 2 ℃.

6.2.3 DC Link Capacitor Selection

55 Aluminum Electrolytic Capacitors manufactured by Panasonic (Part No. EEHZC1K470P) are connected in parallel to construct the entire DC bus. Each capacitor is 47 μF and rated at 80 V. The power density of the prototype has been greatly improved compared with [134] which uses Chemi-Con capacitors for the DC bus. Table 6.3 shows the comparison between the two types of electrolytic capacitors. The footprint taken by Panasonic capacitors is almost the same as that when Chemi-Con capacitors are used. However, the total volume has a 75% reduction when Panasonic capacitors are used, which leads to a much higher power density. Unlike the prototypes in existing literature, the height of the DC link capacitors is no longer a bottleneck of the box volume of our prototype.

Table 6.3: Comparison Between Panasonic And Chemi-Con Electrolytic Capacitors

Manufacturer	**Panasonic**	**Chemi-Con**
Product	EEHZC1K470P	EGPD101E621MM30H
Capacitance	47 μF	620 μF
RMS current of the cap	1.3 A	3.2 A
Number of caps needed	55	23
Volume of each cap	0.8 cm^3	7.63 cm^3
Total volume of capacitor	44 cm^3	175.5 cm^3
Footprint of capacitors	43.2 cm^2	46.2 cm^2

6.2.4 IMS Board and Heatsink Selection

Fig. 6.4 shows the cooling structure of the power stage. The MOSFETs are soldered on an IMS board. The IMS board has a copper layer, a dielectric layer and an aluminum layer. The IMS board has a much better thermal conductivity compared with a standard FR4 PCB board as shown in Table 6.5. The detailed parameters of the selected IMS board can be found in Table 6.4. The IMS board was mounted on a forced air cooled heatsink with a thermal pad. In the design phase, the temperature rise during steady state operation could be estimated from power loss multiplying the total thermal resistance. The junction to case thermal resistance, R_{jc}, is 0.4 K/W. The thermal resistance of the selected IMS board, R_{IMS}, is 0.11 K/W. The total thermal resistance of the thermal pad, $R_{thermal}$, and the heat sink, R_{sink}, is 0.22 K/W. The total thermal resistance, R_{total}, is estimated to be 0.73 K/W. The device power loss under continuous operation has been estimated by PLECS simulation, and the value is 25 W. As a result, the temperature rise of the MOSFETs at steady state could be estimated as

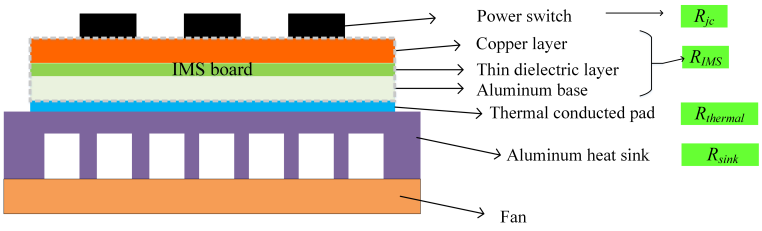


Figure 6.4: Structure Of The Proposed IMS Board

$$\Delta T = P_{loss} \cdot R_{total} = 25 \cdot 0.73 = 18.54 \tag{6.1}$$

The measured temperature rise shown in Fig. 6.5 is around 14.7 ℃, which matches with the calculation pretty well. In addition, the maximum allowable device temper-

ature rise is 50 ℃ in the worst case where the environment temperature is 100 ℃ and the maximum device junction temperature is 150 ℃. Therefore, the heatsink design meets the requirement.

Table 6.4: Parameters Of The Selected IMS Board

IMS board design parameters		**Reason for the design**
Board type	Thermal Clad HT04503	
Copper thickness	3 oz(105 μm)	Handle 500 A RMS/10mm width
Aluminum carrier thickness	2 mm	Handle dynamic thermal of 500 A RMS for 300 ms
Insulator layer thickness	76 μm	6.8 kV insulation with 80 V/μm dielectric strength
R_{IMS}	0.11 K/W	For the conductive layer

Table 6.5: Comparison Between IMS Board And Standard FR4 PCB

	IMS board	**Standard PCB**
Thermal conductivity	4.1 W/mk	0.35 W/mk
Dielectric strength	80 kV/mm	20 kV/mm

6.2.5 Automotive Standard Gate Driver Infineon TLE9180D-31QK

One important contribution of this work is that the gate driver IC and microcontroller used in the prototype are compliant with automotive standards, which makes the prototype more readily accepted by industry. The TLE9180D-31QK is an advanced gate driver IC which is dedicated to control 6 external N-channel MOSFETs

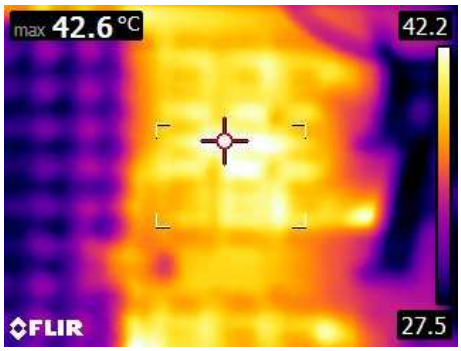


Figure 6.5: Thermal Image Of The MOSFETs In Continuous Operation

of an inverter for high-current three-phase motor drive applications in the automotive sector [156]. A sophisticated high-voltage technology allows the TLE9180D-31QK to support applications for single and mixed battery systems with battery voltages of 12 V, 24 V and 48 V even in tough automotive environments. Therefore, the pins that are related to inverter bridges, motor, and power supply can withstand voltages of up to 90 V. Motor related pins can even withstand negative voltage transients down to 15 V without damage. All low- and high-side output stages are based on a floating concept, and the driver strength of the IC is enough to drive MOSFETs with the lowest R_{dson} on the market. The suggested schematic is shown in Fig. 6.6 and external circuitry parameters can be found in [156]. Each arm consists of three paralleled MOSFETs. C_{boot} is the bootstrap capacitor which is connected to BH, and R_g is the gate driver for each switch. GHa and SHa represent the high-side gate output and source output pins of the gate driver IC, respectively. GLa and SLa represent the low-side gate output and source output pins of the gate driver IC, respectively

An integrated SPI interface is used to configure the TLE9180D-31QK. After successful power-up, parameters can be adjusted by SPI. Monitoring data, configuration and error registers can be read by external controllers. Cyclic-Redundancy-Check (CRC) over data and address bits ensures safe communication and data integrity.

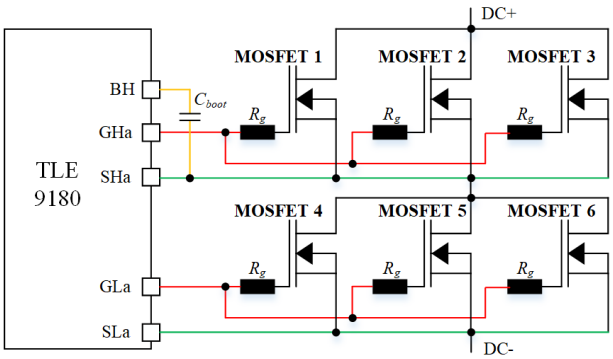


Figure 6.6: Schematic Of Gate Driver TLE9810D-31QK Output Section For Phase A

Specifically, CRC8 has been implemented in this IC. Bridge currents can be measured by the 3 integrated current sense amplifiers. The output of the current sense amplifiers is compatible with 5 V Analog-to-Digital (AD) converters, and the robust inputs can withstand negative transients down to 10 V without damage. The proportional gain and zero current offset can be adjusted by SPI, and the offset can be calibrated as well. Diagnostic coverage and redundancy have increased steadily in recent years in automotive applications. The TLE9180D-31QK also offers a wide range of diagnostic features, like monitoring of power supply voltage as well as system parameters. A testability of safety relevant supervision functions has been integrated. Failure behavior, threshold voltages and filter time constants of the supervisions of the device are adjustable via SPI. The TLE9180D-31QK is integrated in a LQFP64 package with an exposed pad, which provides an excellent thermal characteristic.

6.2.6 Automotive Standard MCU Infineon TC1782

The TC1782 is a high-performance microcontroller which includes a TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor, a Direct Memory Access (DMA) controller, and several on-chip peripherals. The TC1782 is designed to meet the needs of the most demanding em-

bedded control system applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements. The TC1782 offers several versatile on-chip peripheral units such as serial controllers, timer units, and AD converters. Within the TC1782, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB) [157].

6.3 IPM Machine Operation and Optimization

This section includes a brief analysis of an IPM machine and proposes an optimized operation curve which not only simplifies the control strategy but also keeps a relatively large output torque. The operation of an IPM machine can be described using a series of equations and constraints which will be presented in the following subsections.

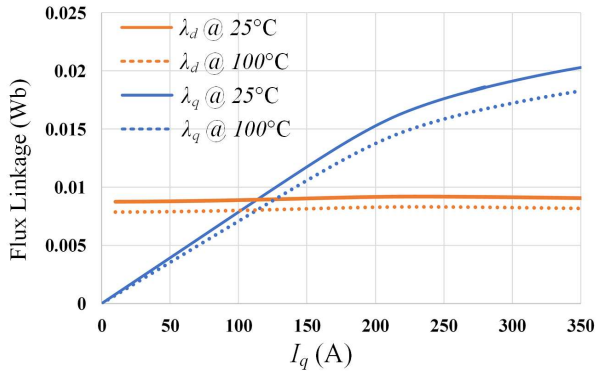
6.3.1 Equations

An FEA simulation has been performed on a physical 6-pole IPM machine. Based on Fig. 6.7 and curve fitting technique, the equations of stator flux linkage at 25 ℃ have been generated as a function of stator winding current.

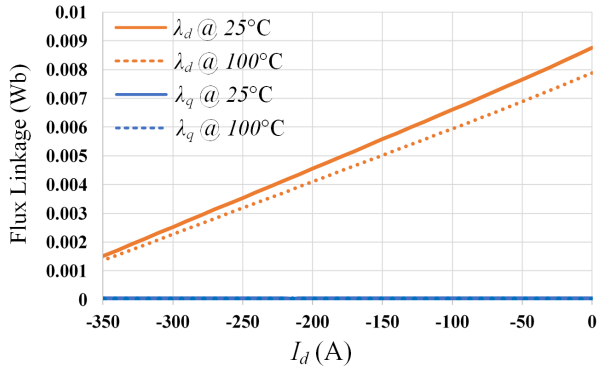
$$\begin{aligned}\lambda_d = f_1(I_d) = 6.457 \times 10^{-14} \cdot I_d^4 + 5.751 \times 10^{-11} \cdot I_d^3 \\ +1.855 \times 10^{-8} \cdot I_d^2 + 2.293 \times 10^{-5} \cdot I_d \\ +8.760 \times 10^{-3}\end{aligned} \tag{6.2}$$

$$\begin{aligned}\lambda_q = f_2(I_q) = 1.119 \times 10^{-14} \cdot |I_q|^5 - 8.327 \times 10^{-12} \cdot |I_q|^4 \\ +1.714 \times 10^{-9} \cdot |I_q|^3 - 1.255 \times 10^{-7} \cdot |I_q|^2 \\ +8.142 \times 10^{-5} \cdot |I_q| - 3.125 \times 10^{-6}\end{aligned} \tag{6.3}$$

where λ_d and λ_q are stator flux linkages in d-axis and q-axis, respectively. I_d and I_q are d-axis and q-axis stator current, respectively.



(a)



(b)

Figure 6.7: FEA Results Showing The Relationship Between Stator Flux Linkages And Winding Currents Under Different Room Temperatures: (a) Stator Flux Linkage Curves With Different q-axis Current; (b) Stator Flux Linkage Curves With Different d-axis Current

Output Electromagnetic (EM) torque is a function of stator flux linkage and winding currents as well as number of pole-pairs of the machine. It can be expressed as

$$T_e = \frac{3}{2} p(\lambda_d I_q - \lambda_q I_d) \tag{6.4}$$

where T_e is the output EM torque, and p is the number of pole-pairs.

Stator terminal voltages in the rotating reference frame can be expressed as

$$V_d = r_s I_d - \omega_e \lambda_q + \frac{d\lambda_d}{dt} \tag{6.5}$$

$$V_q = r_s I_q + \omega_e \lambda_d + \frac{d\lambda_q}{dt} \tag{6.6}$$

where V_d and V_q represent d-axis and q-axis stator terminal voltages, respectively. r_s is the stator winding resistance. ω_m and ω_e are rotor mechanical speed and electrical speed, respectively. The stator terminal phase voltage, V_t, can be expressed as

$$V_t^2 = V_d^2 + V_q^2 \tag{6.7}$$

6.3.2 Constraints

The voltage constraint is imposed by the finite DC bus voltage of the three-phase inverter and can be expressed by

$$V_d^2 + V_q^2 \leq V_{max}^2 \tag{6.8}$$

where V_{max} represents the maximum available stator terminal voltage. The current constraint can be expressed as

$$I_d^2 + I_q^2 \leq I_{max}^2 \tag{6.9}$$

where I_max represents the maximum allowable current and is determined by inverter device current rating and stator winding current rating.

6.3.3 IPM Operation Curves

The IPM operation and constraint curves are plotted in Fig. 6.8. The voltage constraint depicts an ellipse under a certain motor speed, and the ellipse shrinks as the speed increases. Fig. 6.8 shows four blue ellipses under four different electrical speeds. With fixed maximum winding current and device current rating, the current constraint can be simply represented by a circle which does not change with machine speed. Fig. 6.8 also shows a series of constant EM torque curves corresponding to different torque values varying from 0.2 to 1.0 per unit. On each torque curve, there is always an (I_d, I_q) pair yielding minimum winding current. Connecting all these (I_d, I_q) pairs from different EM torque curves produces a Maximum Torque Per Amp (MTPA) curve which is shown as the purple curve in Fig. 6.8.

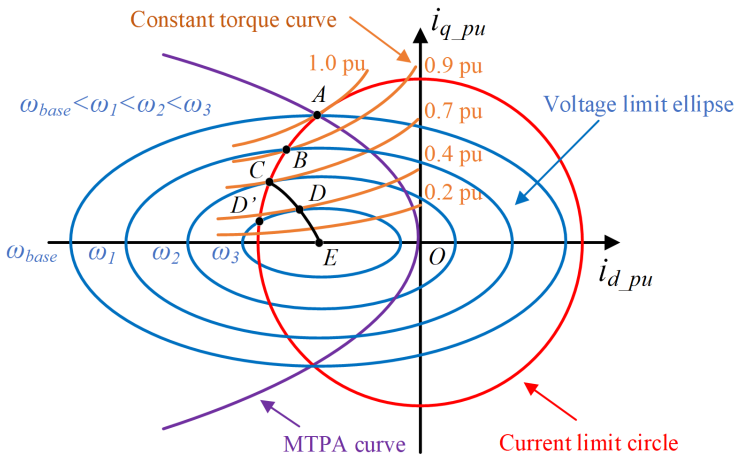


Figure 6.8: IPM Operation Curves In I_d I_q Plane

6.3.4 IPM Operation Optimization

Fig. 6.9 shows maximum output EM torque versus mechanical speed of the IPM machine used in the experiment. ω_{base} is the critical point between constant torque and field-weakening region. It can be seen that the maximum EM torque is constant

when the speed is below ω_{base}. The machine enters field-weakening when its speed goes beyond ω_{base}, and the maximum output EM torque starts to decrease. The optimization target before field-weakening is to achieve MTPA which ensures maximum acceleration and minimum winding current that produces minimum conduction loss in the inverter devices and minimum iron loss in the machine windings. Therefore, the operating point in this region is Point A. In order to calculate the value of I_d and I_q at Point A, curve fitting method is used instead of deriving the analytical expressions since the stator flux linkages are also data driven. The flow chart of the curve fitting equation generation is illustrated in Fig. 6.10. The generated equations are expressed as follows,

$$\begin{aligned} I_q = f_3(T_e) = &-4.494 \times 10^{-4} \cdot |T_e|^4 + 3.803 \times 10^{-2} \cdot |T_e|^3 \\ &-1.237 \cdot |T_e|^2 + 2.446 \times 10^{1} \cdot |T_e| + 1.098 \end{aligned} \tag{6.10}$$

$$\begin{aligned} I_d = f_4(I_q) = &-1.663 \times 10^{-8} \cdot I_q^4 + 3.350 \times 10^{-6} \cdot I_q^3 \\ &-2.841 \times 10^{-3} \cdot I_q^2 - 2.277 \times 10^{-1} \cdot I_q \\ &+1.777 \end{aligned} \tag{6.11}$$

In this way, the minimum current can be calculated using the above equations given by any torque command.

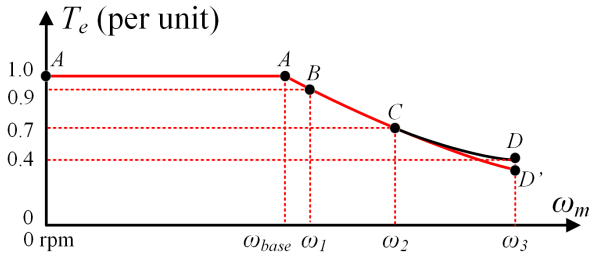


Figure 6.9: Maximum Output EM Torque Versus Mechanical Speed

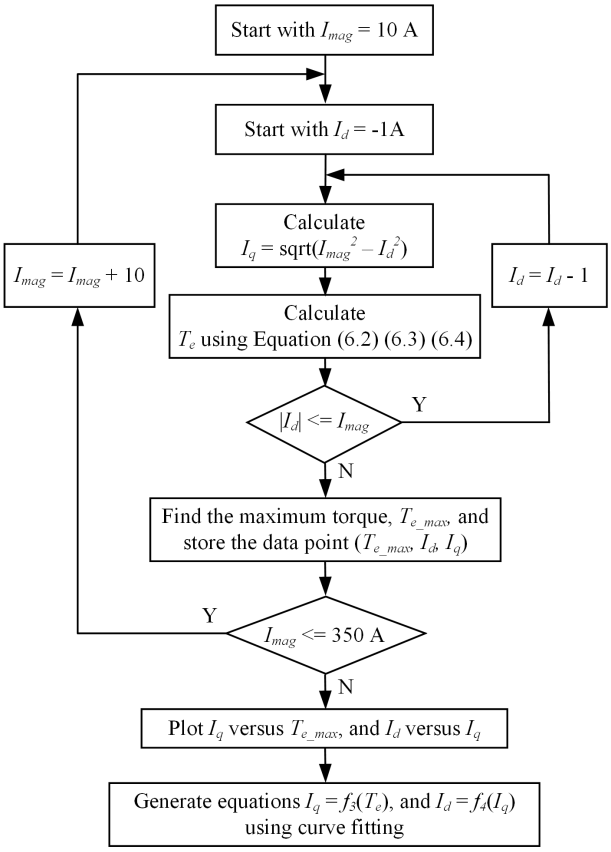


Figure 6.10: Flow Chart Of Equation Generation Of MPTA Using Curve Fitting Where I_{mag} Represents The Winding Current Magnitude

When IPM machine speed is higher than ω_{base}, the optimization target is to keep EM torque as large as possible so that the machine can reach its targeted speed as quickly as possible. From Fig. 6.8 and 6.9, operating at maximum available torque can be separated into two segments. The operating point should firstly follow along the red curve ABC when the speed is between ω_{base} and ω_2. On this curve, the output EM torque is always at its maximum. After the speed goes higher than ω_2, the operating point should follow the black curve CD. This is because the point producing maximum torque is no longer on the red circle. The equation of this black curve can be acquired using curve fitting technique that ensures MTPA from zero speed to infinity. However, these equations are not adaptive to DC bus fluctuation

and other machine parameter changes. Instead, the proposed control strategy here chooses to regulate the current vector to continue following the red curve CD' (current limit curve) instead of the black curve CD. Even though the resulting EM torque is around 10% smaller, the control strategy is much easier to be implemented. The additional voltage loop which is used to modify d-axis current reference makes the algorithm more adaptive, and the voltage limit can be fulfilled during the whole operating range.

6.4 Proposed Constant Current Control Strategy

Based on the analysis in Section 6.3, an improved IPM control strategy is illustrated in Fig. 6.11. V_{DC} represents the DC bus voltage. i_A, i_B, i_C represent the three-phase line current feedbacks. θ_m is the rotor mechanical angle while θ_e is the corresponding electrical angle. ω_m^* represents the mechanical speed command. ω_{fbk} is the motor mechanical speed feedback. T_e^* is the EM torque command. I_d^* and I_q^* are current references on d-axis and q-axis, respectively. V_d^* and V_q^* are voltage references generated from the current regulators on d-axis and q-axis, respectively. The proposed constant current control consists of the following three parts.

6.4.1 Torque Command Generation

The EM torque command is generated by a speed loop followed by an output limiter. The controller is designed such that the output will be clamped at its maximum limit when the motor speed is low compared with the pre-set reference. During this period, the PI controller is saturated, and the output torque command is 10 Nm. When the speed feedback is very close to its command, the PI controller will exit saturation region. In torque control mode, a direct torque command is used to calculate corresponding current commands based on Equation 6.10 and 6.11.

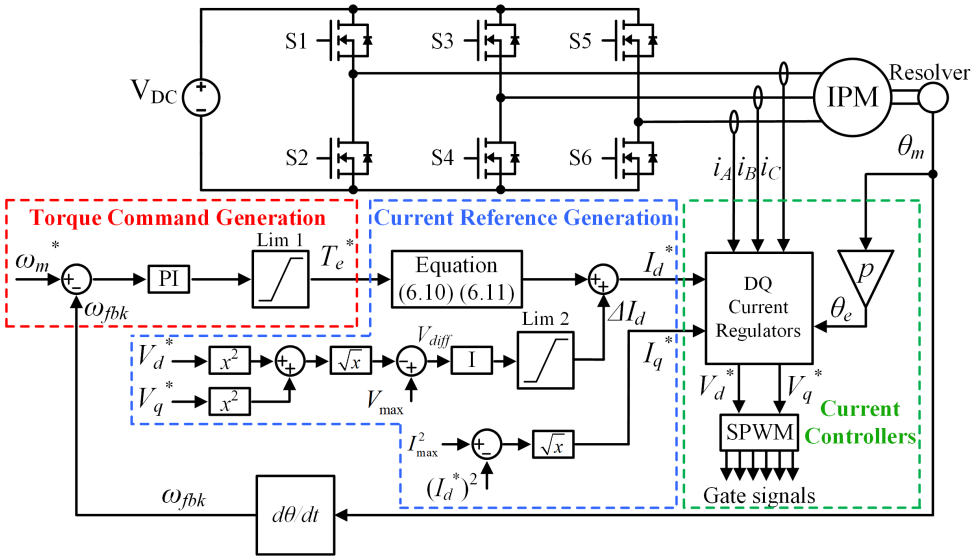


Figure 6.11: Proposed IPM Motor Drive Control Block Diagram

6.4.2 Current Reference Generation

The control loop enclosed by the blue dashed line represents the inverter current reference generation. Based on the analysis in Section 6.3, the control strategy is separated into two cases.

In order to determine whether the motor enters field-weakening region, the inverter output voltage magnitude will be computed using the two outputs of the current regulators, V_d^* and V_q^*. Since the inverter output voltage cannot exceed its maximum value V_{max} (half of V_{DC} in this case), the difference between inverter output voltage magnitude and V_{max} is used to determine motor operation region, and this voltage difference is represented by V_{diff} as shown in Fig. 6.11. If the inverter voltage is smaller than its maximum value, the current reference will follow the MTPA equations 6.10 and 6.11. When the inverter voltage is higher than its maximum value, the voltage loop will generate a negative ΔI_d to modify the original I_d^*. The I_q^* is then calculated such that the winding current magnitude is kept constant. Therefore, the operating point will drift from the purple MTPA curve in Fig. 6.8, but it still

fulfills the voltage and current constraints. In this way, field-weakening happens automatically, and the controller is capable of adjusting the starting point of field-weakening when DC bus voltage fluctuates and other machine parameter changes since V_{max} will change when DC bus voltage varies.

6.4.3 dq-frame Current Controllers

As shown in Fig. 11, two simple PI controllers are used to generate inverter output voltage reference and traditional SPWM technique is used to generate device gate signals.

6.4.4 Advantages of the Proposed Control Strategy

The proposed IPM drive control strategy has the following advantages over the existing solutions. Firstly, no look-up tables are involved in the control loops, which saves memory of the digital controller. Secondly, the proposed control strategy is adaptive to machine parameter changes caused by temperature and other operating conditions as well as DC bus voltage fluctuation, since an online regulation is implemented by the voltage integrator. Thirdly, no piecewise functions are involved in generating torque command and current references compared with [151]. In addition, Lim 2 ensures smooth change of d-axis current reference when the machine enters field-weakening. Therefore, a seamless transition can be realized from non-field-weakening to field-weakening operation. Two improvements have been made compared with [148]. Firstly, the nonlinearity of stator flux linkage has been taken into consideration, and the self-inductance is not assumed to be constant. Secondly, the proposed control scheme is suitable for not only speed control but also torque control.

6.5 Pump-back Test Bench Development

The designed power stage and the proposed IPM motor drive control strategy can be tested and verified using a pump-back system which does not need a real machine and has been implemented in literature [151, 158–161] as well.

A pump-back system contains two identical three-phase inverters. One inverter serves as the Motor Drive while another is controlled to mimic the operation of an IPM machine (called IPM Emulator). This virtual machine concept was proposed in [159] and the machine emulators in [159–161] also show excellent reaction to the motor drive under test.

The control block diagram of the proposed pump-back system is shown in Fig. 6.12. The AC terminals of the two inverters are connected through three inductors due to the PWM voltages at inverter output. The DC terminals of the two inverters are directly connected to the same DC power supply. As a result, the real power circulates between the two converters and the DC power supply only provides loss of the system. In Fig. 6.12, L_c represents the inductors linking the two inverters. I_{d_fbk} and I_{q_fbk} are current feedbacks on d-axis and q-axis, respectively. V_{d2}^* and V_{q2}^* are calculated terminal output voltages of the virtual IPM machine on d-axis and q-axis, respectively. λ_d' and λ_q' are flux linkages seen from the IPM Emulator AC terminals on d-axis and q-axis, respectively. T_e is the calculated EM torque. λ_{Lcq} and λ_{Lcq} represent the flux linkages generated in L_c on d-axis and q-axis, respectively. The control diagram on the left-hand side of the red dashed line represents the improved IPM control strategy presented in Section 6.4. The control of the second inverter (IPM Emulator) is shown on the right-hand side. Since the motor drive controls AC side current, open-loop voltage control is implemented in the IPM Emulator. Stator flux linkages on both d-axis and q-axis are firstly calculated using Equation 6.2 and

6.3 subtracted by the flux produced in L_c. Along with the mechanical speed of the motor, the machine terminal voltage can be computed using Equation 6.5 and 6.6.

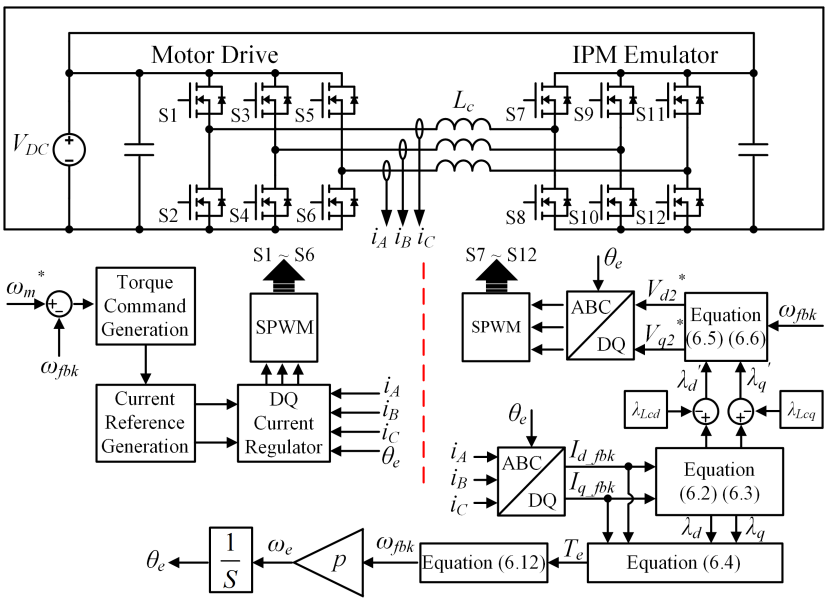


Figure 6.12: Control Block Diagram Of The Proposed Pump-back System

In order to get the information of the rotor speed and position without having a real machine and a resolver, the following equation is used.

$$\omega_{fbk} = \int \frac{1}{J}(T_e - T_{Load})dt \tag{6.12}$$

In Equation 6.12, ω_{fbk} is the mechanical speed of the machine. J is the moment of inertia of the IPM machine and can be acquired from the nameplate. The output EM torque, T_e, can be calculated using Equation 6.4. T_{Load} is the load torque and can be set as a constant in the experiment. As a result, the electrical speed is just p (number of pole-pairs) times of the mechanical speed, and the rotor electrical angle is the integral of the electrical speed. This rotor angle will be shared between the two inverters. The second issue is how to design the value of L_c. All components outside of the motor drive should be regarded as the virtual IPM machine. Therefore,

the flux produced by the AC inductors is also a part of the flux produced in the virtual machine. This is the reason why λ_{Lcd} and λ_{Lcq} should be subtracted from the calculated stator flux linkage. The inductor L_c should be designed such that the generated flux is smaller than the total flux calculated from Equation 6.2 and 6.3. In this case, L_c is designed as 20 μH.

6.6 Simulation Results

PLECS simulations have been performed to verify the effectiveness of our proposed constant current based IPM motor drive control technique, and to prove the correctness of our proposed pump-back system control algorithm. Some of the simulation parameters are listed in the following table.

Table 6.6: Simulation Parameters

Parameters	**Values**
DC bus voltage	48 V
Output frequency range	0 $\sim$ 600 Hz
Load torque	2 Nm
Switching frequency	12 kHz
Deadtime	1 μs

The first simulation was conducted using an IPM machine model provided by PLECS with a load torque of 2 Nm which has an opposite direction as the rotation. The machine parameters can be directly typed into the model or inserted as look-up tables. Fig. 6.13(a) shows the inverter output current and filtered terminal voltage before the machine enters field-weakening region (corresponding to Point A in Fig. 6.8). The current waveform indicates a constant current magnitude when the motor speed increases. However, the output terminal voltage amplitude increases with motor

speed. Fig. 6.13(b) shows the inverter current and filtered output voltage after the motor enters field-weakening region. It is obvious that the current magnitude is still kept constant. The output terminal voltage is also limited at a constant level due to the voltage integrator.

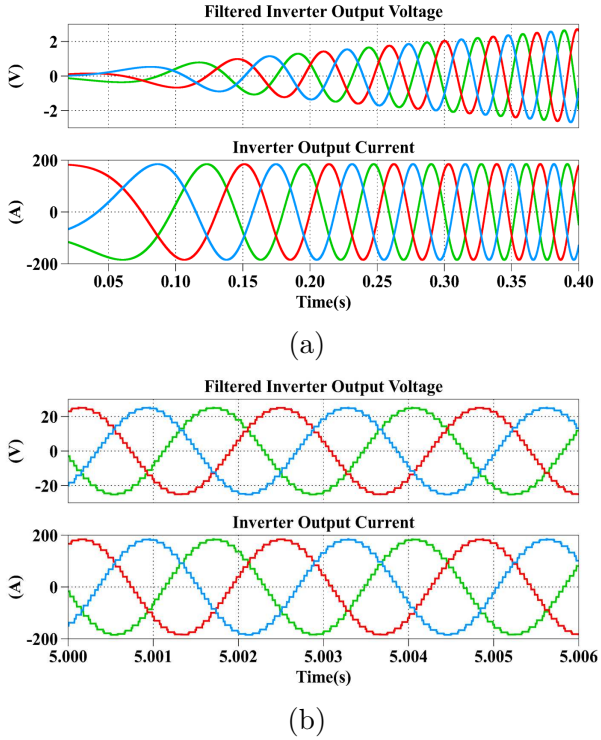


Figure 6.13: PLECS Simulation Results Of Filtered Inverter Output Voltage And Current (a) Before Entering Field-weakening Operation And (b) After Entering Field-weakening Operation

In the simulation, the IPM machine operates as a motor in the first 15 seconds and changes to generator operation after 15 seconds. The results of the entire process are shown in Fig. 6.14. Region I to III are motor operation (acceleration) while Region IV to VI represent generator operation (deceleration) of the IPM machine. The top figure shows that the current feedback perfectly tracks its reference, which validates the effectiveness of the designed current controllers. Since the speed error is very large in Region I, the speed regulator is saturated and the output has been clamped to 10 Nm. Since the EM torque is the largest in this region, the slope of the mechanical

speed, which represents the acceleration, is also the largest. Region II represents the field-weakening region of the motor. In this region, the inverter terminal voltage loop starts to play a role in d-axis current reference generation, and I_d^* becomes more negative due to a negative ΔI_d. I_q^* also decreases in order to keep the phase current magnitude constant. At the same time, the speed acceleration decreases due to smaller output EM torque. When the motor speed is close to its command, the machine enters Region III where the speed regulator retreats from saturation, and the output torque is trying match the load torque. The speed command changes from 12000 rpm to 0 at t = 15 s and the machine starts to decelerate. In Region IV, since the speed is still high, the machine operates in the field-weakening region. However, the output EM torque becomes negative and I_q changes its polarity from positive to negative. As the speed becomes even lower, the machine leaves field-weakening and enters constant torque operation. As shown in Region V, the output EM torque becomes -10 Nm. Finally, when the speed becomes very low, the output EM torque is trying to balance the load torque, and the speed loop exits the saturation region. The results show that the proposed control strategy works for both motor and generator operations.

A pump-back system simulation has also been conducted to verify the proposed control strategy. The motor drive shows the same behavior as that in the previous simulation with an IPM machine model. This also proves the equivalence between a real machine and an emulator.

6.7 Experimental Results

The constructed pump-back test bench is shown in Fig. 6.15. Top view of each component including power board, controller board, gate driver board, AC inductors, current sensors, and DC power supply have been provided. The actual hardware

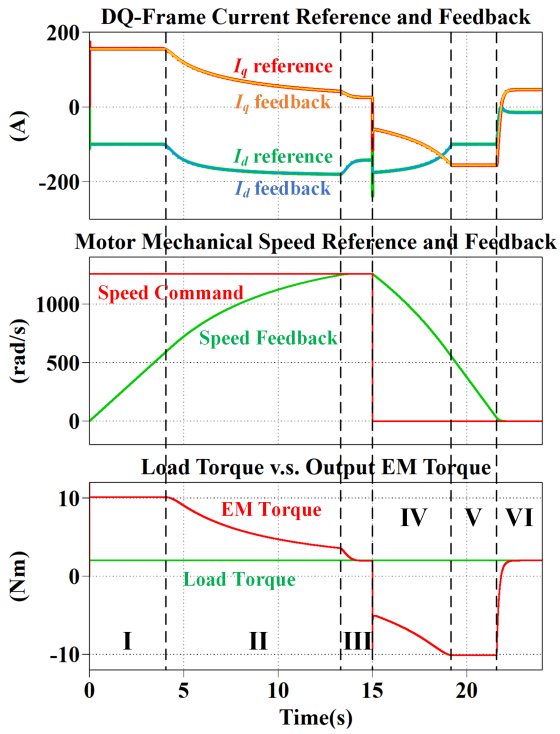


Figure 6.14: PLECS Simulation Results. Top: Stator Current reference And Feedback In dq-frame; Middle: Mechanical Speed Reference And Feedback; Bottom: Load Torque And Output EM Torque

setup is shown on top left corner of Fig. 6.15. The dimension of the power stage is shown in Fig. 6.16. The designed prototype reaches a power density of 20.3 kW/L.

6.7.1 Device dv/dt Regulation

Since the ratio of switching loss over conduction loss is very small, the major limitation of the dv/dt is on the motor side. High dv/dt of the machine terminal voltage can lead to high EMI noise and, most importantly, can create stresses that cause motor insulation to deteriorate and to fail [162]. Unlike traditional AC motor drives where mitigation of high dv/dt usually occurs at the motor end due to the long cable connection between AC drives and machines, the inverter and the motor are compactly integrated in this 48 V BSG system. As a result, reducing dv/dt at

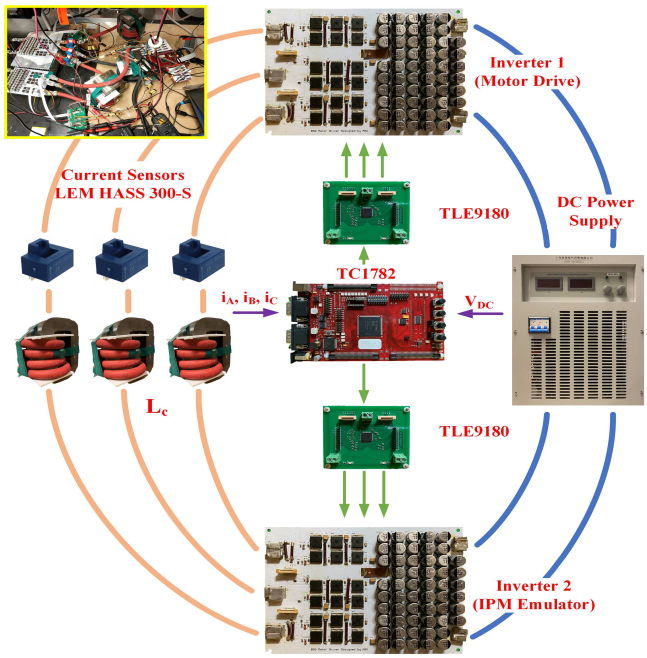


Figure 6.15: Experimental Setup Using Infineon Technologies TC1782 Microcontroller And TLE9180 Gate Driver IC

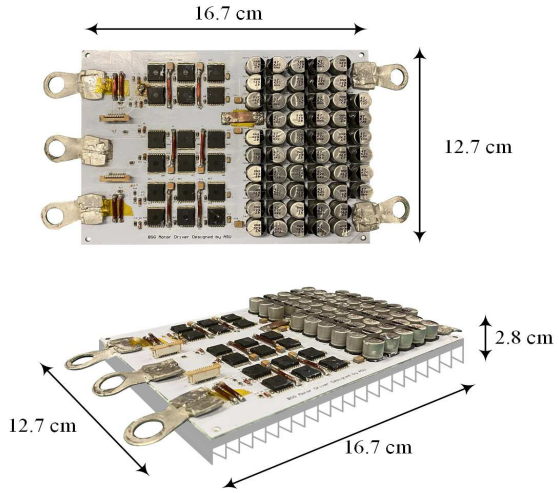


Figure 6.16: Dimension Of The Designed Power Board

the inverter output has been implemented by adding large gate resistors so that the gate-to-source current of the Si MOSFETs during turn-on and turn-off transients can be effectively limited. The final dv/dt is around 0.15 V/ns, as shown in Fig. 6.17.

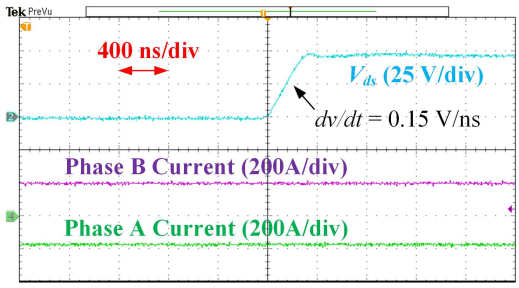


Figure 6.17: Drain-source Voltage (V_{ds}) Of The Device And dv/dt Measurement

6.7.2 Experiments of Closed-loop Current Control with RL Load

The first experiment is to achieve closed-loop current control of the inverter by using a three-phase RL load which consists of a 90 mΩ resistor and a 20 μH inductor in each phase. The closed-loop current control can be easily verified by changing the DC bus voltage. The experimental waveforms are shown in Fig. 6.18. The magnitude of the phase current has been well regulated at 186 A under different DC bus voltages.

6.7.3 Experiments of the Proposed Pump-back System

The control strategy of the proposed pump-back system has been verified using the constructed test bench. Fig. 6.19 shows the current waveforms under four different frequencies which are 60 Hz, 200 Hz, 400 Hz, and 600 Hz. Each waveform corresponds to a point on the Torque-Speed curve shown in Fig. 6.20. The test waveforms show the proposed constant current control and pump-back system control are effective. Note that the current magnitude in the 400 Hz and 600 Hz case is smaller than 186 A. The reason is that there is a large voltage drop across the inductor L_c between two inverters, and this voltage drop increases with higher current magnitude and electrical frequency. The terminal voltage of the IPM Emulator inverter can become much larger than that of the Motor Drive inverter. In order to avoid over modulation of the Emulator inverter under the same DC bus voltage, the current magnitude is

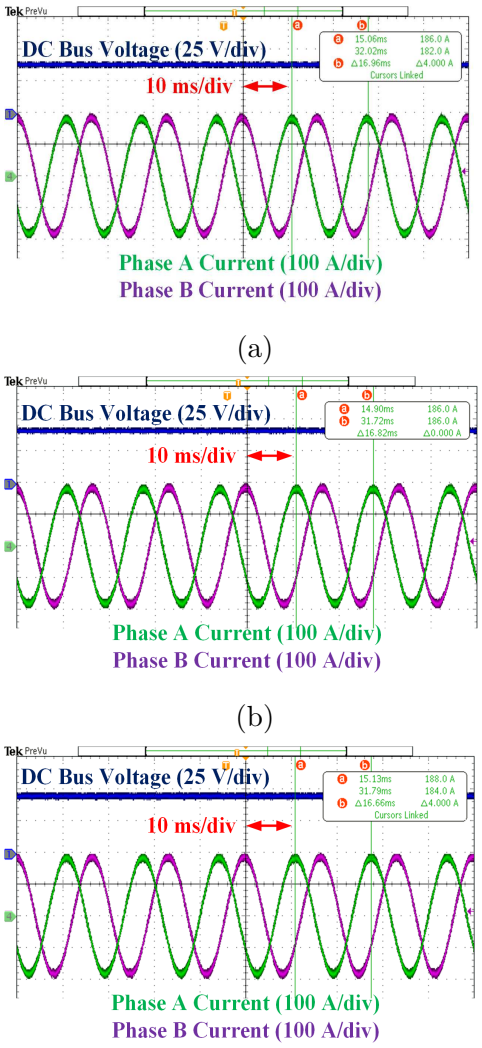
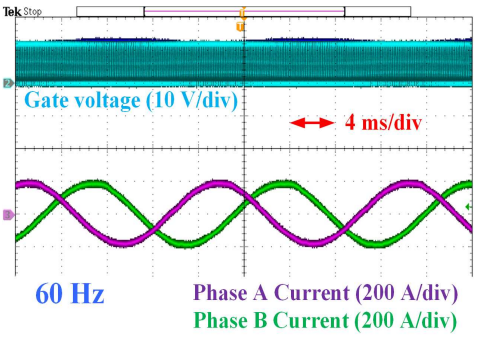
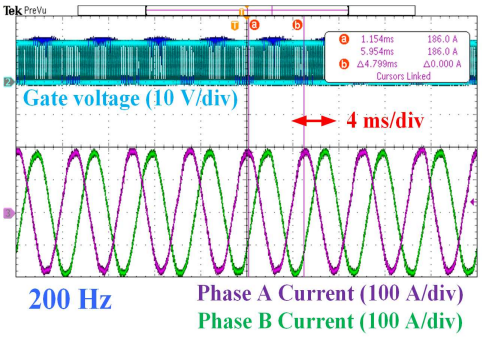


Figure 6.18: Closed-loop Current Control Experimental Results Under The DC Voltage Of (a) 39 V; (b) 42 V; (c) 46 V

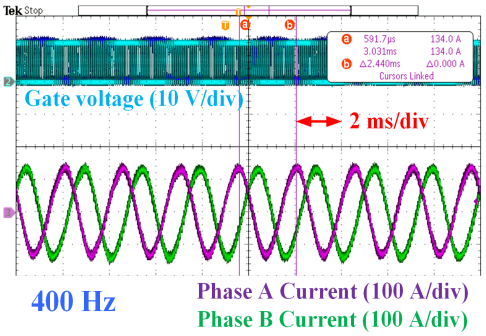
intentionally decreased. As a result, the corresponding output EM torque is also below the green curve.



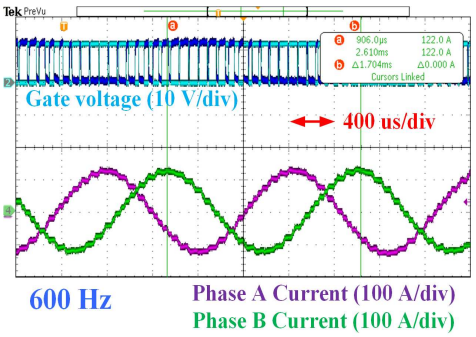
(a)



(b)



(c)



(d)

Figure 6.19: Pump-back System Experimental Results Of Phase A And B Currents With An Output Frequency Of (a) 60 Hz; (b) 200 Hz; (c) 400 Hz; (d) 600 Hz

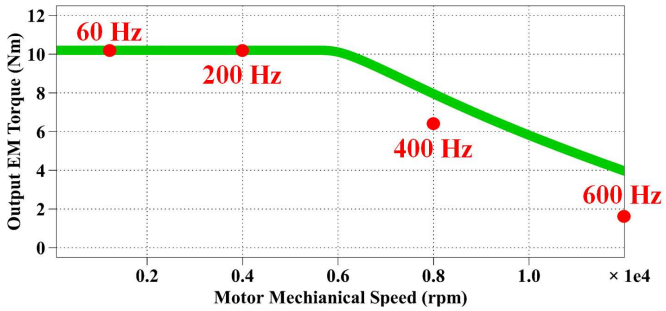


Figure 6.20: Output EM Torque Versus Motor Mechanical Speed

6.7.4 Pump-back Experiments under Machine Parameter Change Caused by Temperature

We have conducted pump-back experiments considering stator flux linkage change caused by temperature variation. In the experiments, all the equations on the Motor Drive side remain unchanged since all the equations from curve fitting can only be tuned offline. However, the flux linkage equations will be updated using the FEA data acquired at 100 ℃ on the IPM Emulator side, which represents machine parameter changes caused by temperature variation. The experimental results are shown in Fig. 6.21 and 6.22.

Fig. 6.21 shows the d-axis and q-axis current feedbacks as well as output EM torque, and Fig. 6.22 shows the measured motor mechanical speed at two different temperatures. From the top and middle figure of Fig. 6.21, it is obvious that the onset of field-weakening happens early at 25 ℃ compared with the case at 100 ℃. The EM torque at 100 ℃ is 5% smaller than that at 25 ℃ in constant torque region. Due to the difference in EM torque in two cases, the speed curves shown in Fig. 6.21 are also different. Larger torque leads to larger acceleration. As a result, the mechanical speed at 100 ℃ experiences a slightly slower increase at the beginning. During field-weakening region, the motor acceleration at 100 ℃ increases and finally

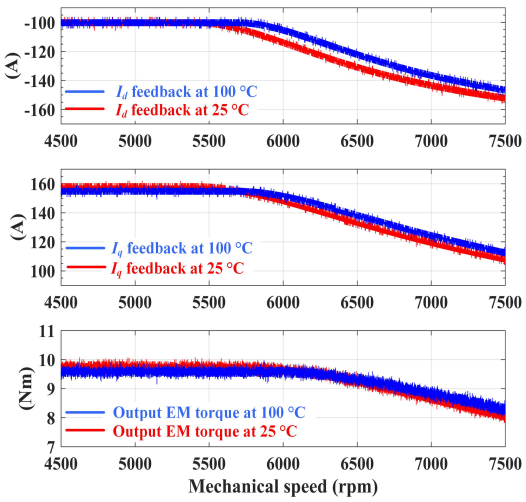


Figure 6.21: Experimental Results Using Data At 25 ℃ And 100 ℃. Top: d-axis Current Feedback; Middle: q-axis Current Feedback; Bottom: Output EM Torque

becomes larger than that at 25 ℃.

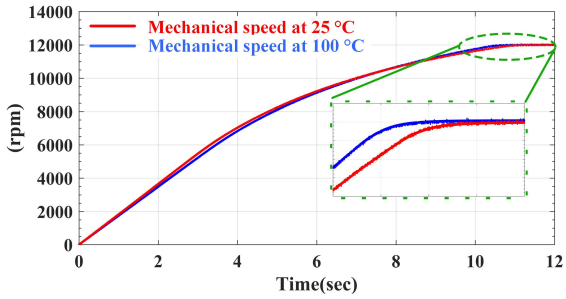


Figure 6.22: Motor Mechanical Speed Measurement At 25 ℃ And 100 ℃

The reasons for these difference can be analyzed as follows. Due to the difference in flux linkage equations at 25 ℃ and 100 ℃, the voltage constraints become different. Since higher temperature leads to smaller flux linkage, the frequency of the onset point of field-weakening operation becomes higher. This explains a late change in d-axis and q-axis current feedbacks at 100 ℃. The output EM torque is calculated using the updated flux linkage equations and winding current feedbacks, as shown in the bottom figure of Fig. 6.21. These machine parameter changes do not affect the field-weakening control algorithm due to the inverter voltage loop which is not dependent

on any machine parameters. As long as the inverter terminal voltage tries to exceed its limit, a negative ΔI_d will be added to d-axis current command in order to keep inverter voltage under limit. This machine parameter variation does not influence the speed loop as well. In the pump-back experiment, the motor mechanical speed is calculated on the IPM Emulator side with updated flux linkage equations. Therefore, the mechanical speed feedback has already taken into account the parameter changes, and the speed regulator can successfully make the motor speed equal to its reference. As shown in Fig. 6.22, both the red and blue speed curves reach 12000 rpm during steady state with small time difference. Therefore, the proposed field-weakening control is highly robust.

6.7.5 Pump-back Experiments under DC Bus Variation

Another advantage of the proposed method is the adaptation to different DC bus voltages, and it has been validated by pump-back experiments as well. The experiments are classified into two categories which are "V_{DC} decreasing (Category I)" and "V_{DC} increasing (Category II)". The nominal DC bus voltage in a BSG system is 48 V. In Category I experiments, the DC bus voltage will decrease to 45 V while in Category II case, the DC link will rise to 51 V. In each category, we have conducted experiments in three cases. The DC bus voltage change will be controlled to occur before field-weakening as well as during field-weakening. The case with unchanged DC bus voltage will also be performed for comparison purpose. The results are presented in Fig. 6.23 and Fig. 6.24.

From the top and middle figure of Fig. 6.23, an early DC bus drop leads to early onset of field-weakening operation comparing the green curve with the blue curve. If the V_{DC} drop happens during field-weakening, there will be a negative step change in d-axis and q-axis current feedbacks as shown by the red curve, and finally the red

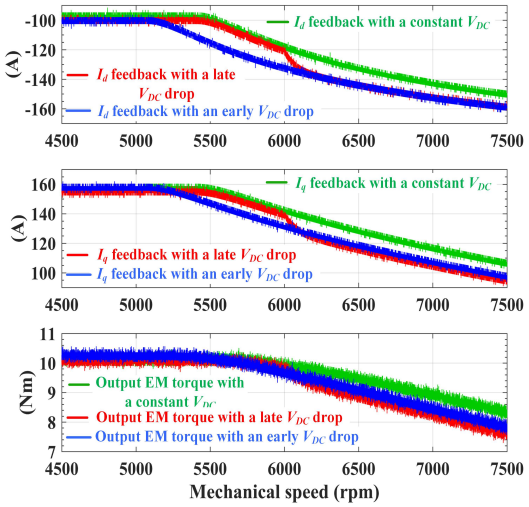


Figure 6.23: Experimental Results With A DC Bus Voltage Drop. Top: d-axis Current Feedbacks; Middle: q-axis Current Feedbacks; Bottom: Output EM Torque

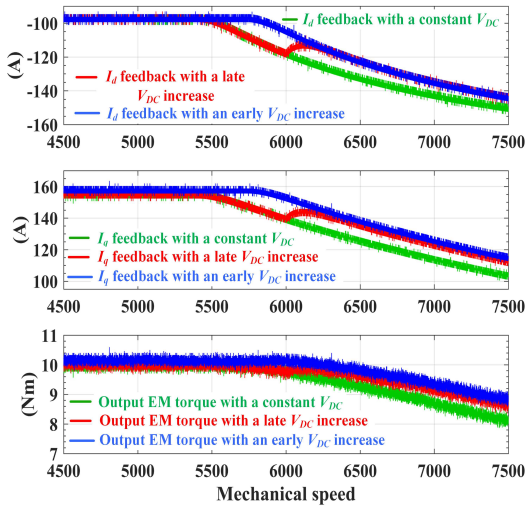


Figure 6.24: Experimental Results With A DC Bus Voltage Increase. Top: d-axis Current Feedbacks; Middle: q-axis Current Feedbacks; Bottom: Output EM Torque

curve will coincide with the blue curve. The same phenomenon can be observed in output EM torque as shown in the bottom figure of Fig. 6.23. From the top and middle figure of Fig. 6.24, an early DC bus rise leads to a late starting point of field-weakening operation comparing the green curve with the blue curve. If the V_{DC} rise happens during field-weakening, there will be a positive step change in d-axis

and q-axis current feedbacks as shown by the red curve, and finally the red curve will coincide with the blue curve. The same phenomenon can be observed in output EM torque as illustrated in the bottom figure of Fig. 6.24.

The reasons can be analyzed as follows. In Category I experiments, smaller DC bus voltage means smaller V_{max}. If the DC bus drop happens in constant torque region, the onset of field-weakening occurs at lower electrical frequency. If V_{DC} drops in field-weakening region, a more negative d-axis current is needed to reduce the terminal voltage magnitude so that no over modulation will occur. Therefore, a negative step change in d-axis and q-axis current feedbacks is expected. The output EM torque starts to decrease at lower frequency if V_{DC} drops in constant torque region since field-weakening will start at lower frequency. However, the torque experiences a negative step change when V_{DC} decreases during field-weakening because of a deeper field-weakening is expected. The same analysis applies to Category II results. Thanks to the additional voltage loop, the proposed IPM motor drive strategy is adaptive to all V_{DC} changes.

6.7.6 Comparison Between the Proposed Method and Curve Fitting Method

We have conducted additional pump-back experiments using the curve fitting based method introduced in [151] for comparison purpose. We firstly compared the performance of the two methods when machine parameter changes. Fig. 6.25 shows the inverter output current with two methods using stator flux linkage data at 100 ℃. As discussed in the previous section, smaller flux linkage leads to a late onset of field-weakening operation using the proposed method so that the DC bus voltage can be fully utilized. However, due to fixed curve fitting equations, the flux-weakening has not been delayed in the curve fitting method. In the top and middle figure of

Fig. 6.25, I_d and I_q feedbacks in the curve fitting method starts to change around the same frequency as that at 25 ℃. The proposed method generates a maximum torque of 10 Nm for longer time as shown by the blue curve in the bottom figure of Fig. 6.25. Therefore, the machine will experience a longer and larger acceleration. The comparison of the two methods with DC bus fluctuation has also been performed. Fig. 6.26 shows the inverter output current using two different methods with a DC bus voltage drop from 48 V to 45 V. Due to the voltage integrator in the proposed method, it automatically adapts to the lower DC bus voltage and regulates the inverter output voltage to be within limit. However, the curve fitting based method uses fixed equations to generate current reference during the entire operation. Therefore, the controller still assumes a 48 V DC bus voltage, which leads to over modulation and current distortion.

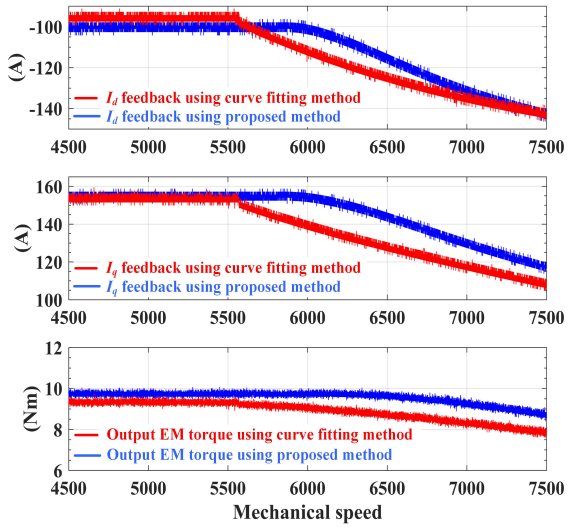


Figure 6.25: Experimental Results Comparison Between Proposed Constant Current Based Method And Original Curve Fitting Based Method Using Stator Flux Linkage Data At 100 ℃

Therefore, the proposed method can automatically adjust the onset of the field-weakening operation when machine parameter varies or DC bus voltage changes com-

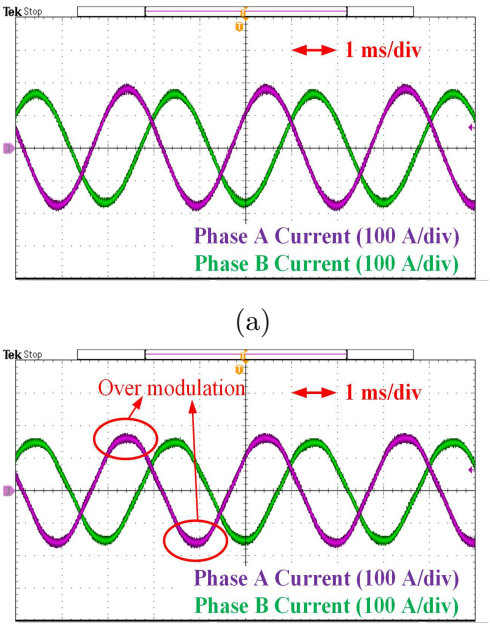


Figure 6.26: Experimental Results Of Inverter Output Current Using Proposed Constant Current Based Method: (a) And Original Curve Fitting Based Method; (b) With A DC Bus Drop From 48 V To 45 V

pared with the curve fitting method in [151].

6.7.7 Common-mode Current Suppression

As shown in Fig. 6.27, the current waveforms are distorted and contain 3^{rd} order harmonics in the pump-back system. Since the DC bus of the two inverters are directly connected, the DC link capacitors of both inverters serve as a low-impedance path for the 3^{rd} order harmonic current. A simple solution is to use a 3^{rd} order PR controller to suppress the circulating current. The result is shown in Fig. 6.28 where the 3^{rd} harmonic component reduces from 1.35 A to 0.2 A. Fortunately, this common-mode current only exists in the pump-back system. When the inverter is directly connected to an IPMSM, the common-mode current will be eliminated since it has no path.

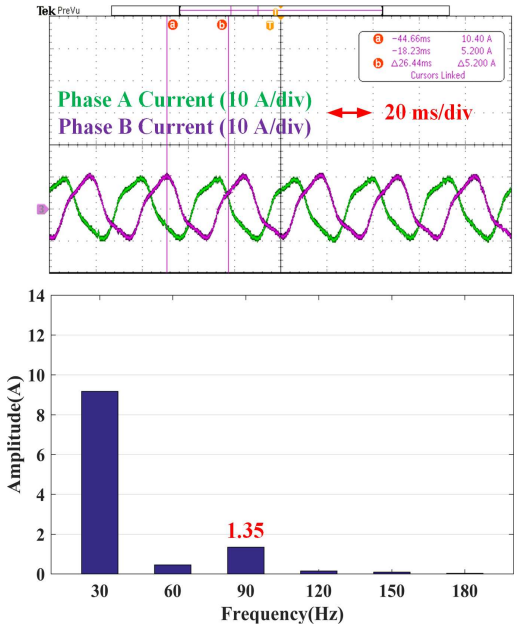


Figure 6.27: Pump-back System Experimental Results Using TC1782 And TLE9180 Without 3^{rd} Harmonic Suppression. Top: Phase A And phase B Current With A Fundamental Frequency Of 30 Hz; Bottom: FFT Analysis Of Phase A Current

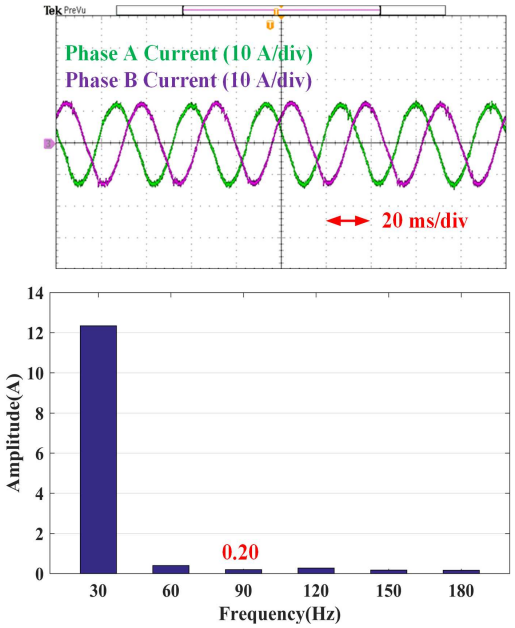


Figure 6.28: Pump-back System Experimental Results Using TC1782 And TLE9180 With 3^{rd} Harmonic Suppression. Top: Phase A And phase B Current With A Fundamental Frequency Of 30 Hz; Bottom: FFT Analysis Of Phase A Current

6.8 Conclusions

This chapter firstly elaborates hardware design considerations for a low-voltage high-current high power density three-phase motor drive inverter to address the challenges of even current distribution among paralleled MOSFETs, small drain-source voltage spike and good thermal dissipation. In order to satisfy the high-current requirement in such applications, a careful selection of MOSFET device with high-current rating and low on-resistance has been presented. In order to suppress circulating current among paralleled devices, individual gate resistors have been placed in the gate loop of each MOSFET. In order to provide good thermal dissipation, an IMS board and single-layer layout technique have been implemented. Multiple low-profile electrolytic capacitors are used so that the power density of the prototype has been increased. Moreover, the gate driver IC TLE9180 and microcontroller TC1782 used in the prototype are compliant with automotive standard, which makes the prototype more readily accepted by industry. An improved IPM control strategy and a pump-back system based on a virtual machine concept have been implemented, which facilitates the validation of the designed inverter hardware under rated condition without using a real motor. The control algorithm automatically adjusts the onset of field-weakening by using an additional inverter voltage loop and takes into account the nonlinearity of the stator flux linkage, which makes the motor drive adaptive to machine parameter changes as well as DC bus voltage fluctuation. A 12 kW three-phase BSG inverter prototype has been built and tested. The prototype power density has reached 20.3 kW/L. The experimental results show a continuous and stable operation with up to 200 A phase current and up to 600 Hz output frequency.

Chapter 7

PUBLICATIONS

7.1 Journal Papers

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