Modeling, and Application of Existing and Novel Characterization Techniques for Solar Cells with Contact Barriers

by

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ABSTRACT

Improving solar cell efficiency is an enormously powerful driver of the cost reduction of solar power. While the silicon solar cell efficiency approaches theoretical limits, many thin-film solar cell technologies fall behind. In particular, cadmium telluride (CdTe) solar cells have only reached a maximum efficiency of 22.1%. One of the challenges associated with the development of CdTe solar cells is due its high electron affinity and the difficulty of achieving heavy p-type doping. This challenge results in the formation of a Schottky barrier at the hole contact, which reduces solar cell efficiency, primarily through the reduction of open circuit voltage (Voc) and fill factor (FF). The Schottky barrier makes the characterization of the actual solar cell p-n junction through current voltage (I-V), capacitance voltage (C-V), and thermal admittance spectroscopy (TAS) more difficult and not straightforward. However, interpreted through accurate physical models and under the correct experimental conditions, these techniques can then also be used to extract the impact of the contact on device performance, chiefly through analysis of the barrier height. Additionally, characterization of the open circuit voltage as a function of the illumination intensity (Suns-Voc) and the open circuit voltage as a function of temperature [Voc(T)] offer insight into the potential impact of the contact barrier. A comprehensive review of characterization of the barrier through the above techniques is given, primarily through a two-diode model. Further, a discussion of the utility of electrochemical capacitance-voltage (ECV) profiling to recover carrier concentrations in device regions otherwise difficult to access through traditional C-V measurements is provided along with modeling to support this conclusion. A discussion of and justification for the experimental extraction of barrier height from TAS

measurements are also provided. Experimentally measured Voc(T), C-V, and Suns-Voc characteristics are presented and compared for a CdTe and a gallium arsenide (GaAs) solar cell. Experimental results indicate that the contact barriers and other possible non-idealities strongly affect the performance of the CdTe solar cell. Modeling results demonstrate the use of ECV to characterize solar cell absorbers can offer information unavailable via conventional C-V measurements.

ACKNOWLEDGMENTS

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CHAPTER 1

REVIEW OF SCHOTTKY BARRIERS AND I-V CHARACTERISTICS

The current through a Schottky diode, if limited by thermionic emission (TE), is given by [1]:

$$J_{Schottky,TE} = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right)\left(\exp\left(\frac{qV}{kT}\right) - 1\right)$$

Where A^* is the effective Richardson coefficient, T is temperature, q is the fundamental electric charge, k is Boltzmann's constant, V is the applied voltage, and ϕ_B is the barrier height. This barrier height for a hole contact is defined by:

$$\phi_B = E_{F,interface} - E_V$$

Where $E_{F,interface} - E_V$ is the energy separating the Fermi level from the valence band at the metal-semiconductor interface. This general form is best demonstrated visually:

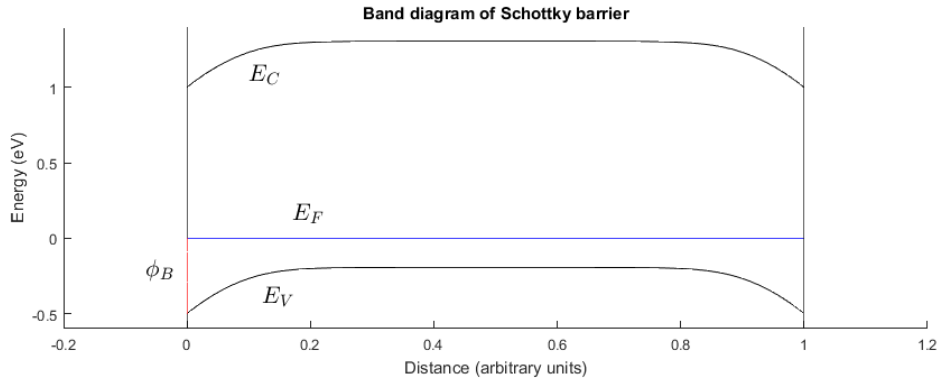

Figure 1 – Band diagram illustrating hole Schottky barrier band alignment

The above band diagram is for a symmetrical structure where a Schottky barrier for hole conduction exists at both metal-semiconductor interfaces, located at $x = 0$ and $x = 1$. Vertical lines mark these interfaces. The barrier height ϕ_B is highlighted in red – in the above sample structure it has a value of 0.5eV.

In the ideal case, absent any surface states and Fermi level pinning, and employing the Boltzmann approximation, this barrier height is given by:

$$\phi_B = \Phi_S - \Phi_M = \chi_S + E_G - \frac{kT}{q}\ln\left(\frac{N_A}{N_V}\right) - \Phi_M$$

This simpler expression illustrates the difficulty in forming a contact to p-type doped CdTe, which has a high (~4.5eV) electron affinity [2]. Metals with appropriately high work functions are unavailable. In practice, surface states can modify this band alignment, but have not been found experimentally to pin the Fermi level near or below the valence band of CdTe – as a result, the observation of a Schottky barrier to hole transport at the p-type CdTe/metal contact is expected.

Two diode models describing the I-V behavior of solar cells with a back contact barrier have been established and discussed at some length in the literature [3],[4], in particular with regards to barrier height extraction via temperature dependent I-V, also referred to as JVT (current density, voltage, temperature).

A solar cell with a contact barrier can be described by two opposite polarity diodes in series. Since the current through both diodes is the same, one can write:

$$J_{cell} = J_{0,pn}\left(\exp\left(\frac{qV_{pn}}{nkT}\right) - 1\right) = -A^*T^2\exp\left(-\frac{q\phi_B}{kT}\right)\left(\exp\left(\frac{-qV_{Sch}}{kT}\right) - 1\right)$$

This model is referred to as the two diode model and neglects shunt and series resistance for simplicity, as these parameters do not affect JVT barrier height extraction unless either junction has a low shunt resistance. A shunted back contact barrier will have a smaller impact on device performance and is therefore of less interest, but is discussed in later sections. If the barrier height is sufficiently large, the forward characteristic must saturate at:

$$J_{cell} = A^* T^2 \exp\left(-\frac{q\phi_B}{kT}\right)$$

as increasing forward voltage falls across the rear diode. This results in "rollover" in the I-V characteristic. This saturation current is an exponential function of temperature. Therefore an Arrhenius plot of $\ln\left(\frac{J_{cell}}{A^* T^2}\right)$ vs. $\frac{1}{T}$ when the current is in the "rollover" regime yields the barrier height ϕ_B, contained in the slope of the plot.

The I-V curves as a function of temperature were experimentally recorded for a CdTe sample cell. The CdTe solar cell was placed in a vacuum chamber cooled down to 78K, and stepped up in temperature to 300K in increments of 25K. The temperature was measured by a thermocouple reading from the stage. The solar cell rested upon a copper contact structure placed on to the stage, and was allowed 15 minutes to equilibrate at each temperature step. The rollover in forward bias is characteristic of a barrier significantly impeding current, though for extraction of the barrier height it is more appropriate to consider the dark characteristic such that the analysis presented above strictly holds.

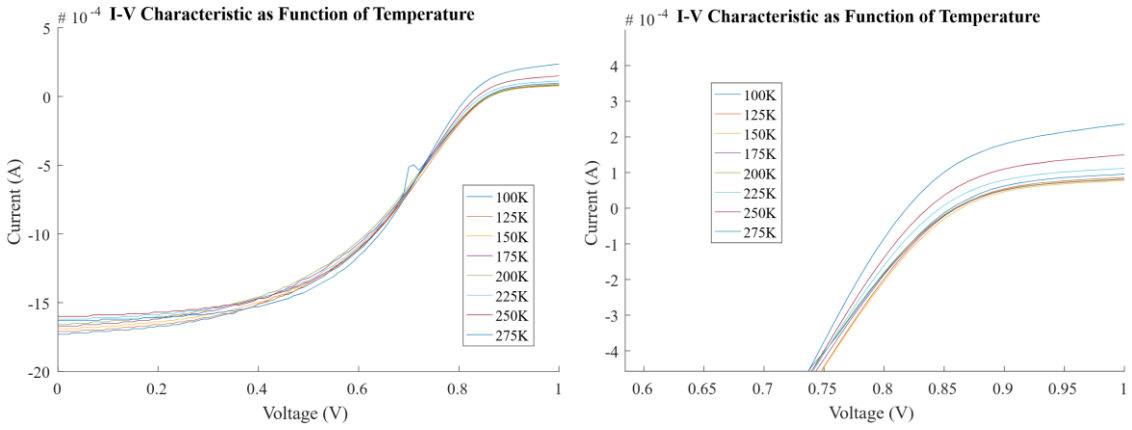

Figure 2- JVT curves for CdTe cell. Right: zooming in on forward bias

The temperature dependence is clearly visible and dictates the saturation value of the forward current. This is very strong evidence of a contact barrier that may impact solar cell performance.

CHAPTER 2

CAPACITANCE-VOLTAGE AND THERMAL ADMITTANCE SPECTROSCOPY CHARACTERIZATION

It is known that contact barriers can give rise to TAS signatures [5][6], a technique primarily utilized to capture and describe deep defect levels by observing capacitance and conductance response as a function of temperature and frequency [7]. This is also a consequence of the temperature dependence of the Schottky barrier conduction, but requires description of the C-V characterization in structures with two junctions to understand. The circuit model for a solar cell with a back contact barrier is:

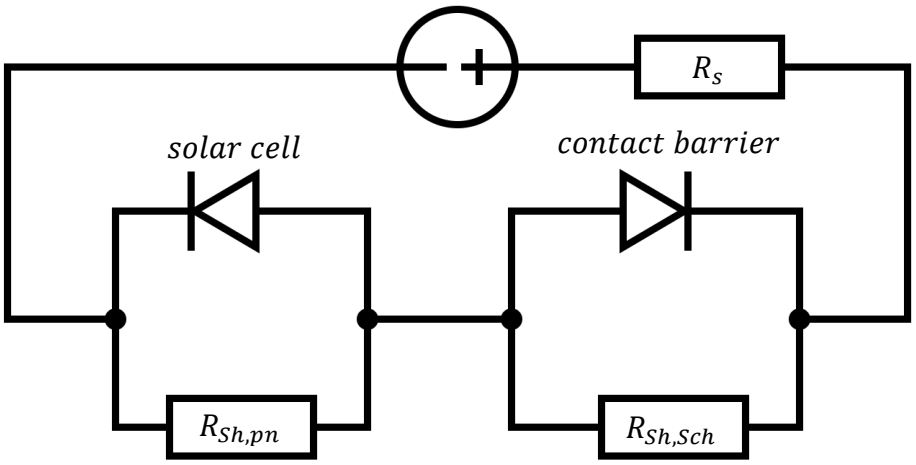

Figure 3 - Circuit diagram of 2 diode model

Where the solar cell and contact barriers have an associated shunt resistance and the circuit has a lumped series resistance. The diodes are voltage controlled capacitors and resistors, so that the circuit model can instead be represented:

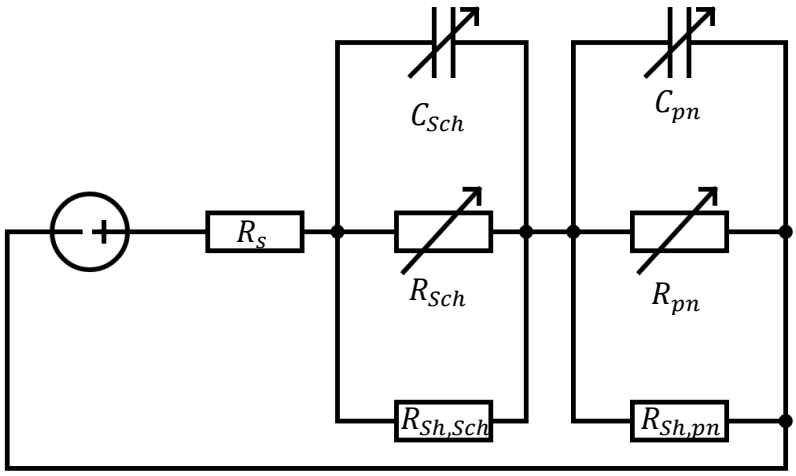

Figure 4 - Small Signal Two Diode Circuit Model

Where $R_s = R_{series}$ describes a lumped external resistance. The total impedance of this circuit is given by [8]:

$$Z = R_{series} + \frac{1}{j\omega C_{Sch} + G_{Sch} + G_{Sh,Sch}} + \frac{1}{j\omega C_{pn} + G_{pn} + G_{Sh,pn}}$$

Ignoring series resistance for the moment, let:

$$G_s = G_{Sch} + G_{Sh,Sch}, G_p = G_{pn} + G_{Sh,pn}$$

The derivation of the total capacitance and conductance of the circuit proceeds:

$$Y = \frac{1}{Z} = \frac{(j\omega C_{Sch} + G_S)(j\omega C_{pn} + G_p)}{j\omega\left(C_{Sch} + C_{pn}\right) + G_S + G_p}$$

$$Y = \frac{(-\omega^2 C_{pn}C_{Sch} + j\omega\left(C_{Sch}G_p + C_{pn}G_s\right) + G_pG_s)}{j\omega(C_{Sch} + C_{pn}) + G_s + G_p}$$

$$Y = \frac{\left[-\omega^2 C_{pn}C_{Sch} + j\omega\left(C_{Sch}G_p + C_{pn}G_s\right) + G_pG_s\right]\left[G_s + G_p - j\omega\left(C_{Sch} + C_{pn}\right)\right]}{\left(G_s + G_p\right)^2 + \omega^2\left(C_{Sch} + C_{pn}\right)^2}$$

$$Y = \frac{\left[-\omega^2 C_{pn}C_{Sch} + j\omega\left(C_{Sch}G_p + C_{pn}G_s\right) + G_pG_s\right]\left[G_s + G_p - j\omega\left(C_{Sch} + C_{pn}\right)\right]}{\left(G_s + G_p\right)^2 + \omega^2\left(C_{Sch} + C_{pn}\right)^2}$$

Separating the complex impedance yields the conductance and capacitance of the total circuit [8]:

$$G = Re(Y) = \frac{(G_p G_s)(G_s + G_p) + \omega^2 (G_p C_{Sch}^2 + G_s C_{pn}^2)}{(G_s + G_p)^2 + \omega^2 (C_{Sch} + C_{pn})^2}$$

The addition of the series resistance to the above expression is trivial and influences the total conductance of the circuit, which is important to the extent it challenges C-V characterization at various frequencies. However, it makes no difference to the relative and total capacitance contributions of each diode to the total circuit capacitance:

$$C = \frac{Im(Y)}{j\omega} = \frac{C_{Sch} G_p^2 + C_{pn} G_{Sch}^2 + \omega^2 C_{Sch} C_{pn} (C_{Sch} + C_{pn})}{(G_s + G_p)^2 + \omega^2 (C_{Sch} + C_{pn})^2}$$

Existing models describe a characteristic frequency of the two diodes [8][9]:

$$\omega_C = \frac{G_s + G_p}{C_{Sch} + C_{pn}}$$

For frequencies well below this value, the frequency independent terms dominate:

$$C = \frac{C_{Sch} G_p^2 + C_{pn} G_{Sch}^2}{(G_s + G_p)^2}$$

This reduces to C_{Sch} if $G_p \gg G_s$ and C_{pn} if $G_p \ll G_s$.

At high frequencies:

$$C = \frac{C_{Sch} C_{pn} (C_{Sch} + C_{pn})}{(C_{Sch} + C_{pn})^2} = \frac{C_{Sch} C_{pn}}{C_{Sch} + C_{pn}}$$

The measured capacitance is the usual series capacitance. This framework provides clear insight into the recovery of the barrier height from TAS measurements, as similarly to the JVT barrier height extraction, the conductance of the Schottky contact is what drives the measured response, in particular the frequency dependence of the measured admittance.

This only strongly holds if the conductance of the main diode and the capacitance of each diode are weaker functions of temperature than the conductance of the back contact barrier. In devices significantly affected by the barrier, passing only a small signal voltage, this is a reasonable assumption. If the back contact is not shunted, the characteristic frequency of the capacitance response has an effective activation energy from:

$$\omega_C = \frac{G_s + G_p}{C_{Sch} + C_{pn}}, G_s = \frac{dI}{dV}\left(J_{Schottky}\right)\Big|_{V \cong 0} \cong \frac{qA^*T}{k}\exp\left(-\frac{q\phi_B}{kT}\right)$$

This definition of a characteristic frequency, while helpful and suitably analogous to defect characteristic frequencies, is not ultimately necessary to justify the extraction of barrier height from the capacitance response – the relative dominance of the frequency dependent and frequency independent terms in the expression for total capacitance C as a function of the back contact conductance G_s is sufficient to consider.

The presence of a significant shunt of the back contact is an important nuance in these models minimally discussed in literature. Shunting of the back contact barrier can occur due to material inhomogeneities and is also sometimes proposed to explain Suns-Voc rollover in several material systems, discussed later. If this shunt is largely independent of temperature, the back contact conductance is:

$$G_s = G_{Sch}(T) + G_{Sh,Sch}$$

This defines a lower temperature limit on the expected frequency response of the barrier. For a temperature range where $G_{Sch}(T)$ lies below $G_{Sh,Sch}$ it is not possible to recover a frequency dependence suitable for extraction of the barrier height from TAS, as changes in conductance and measured capacitance are masked by the shunt leakage of the back

contact. This suggests the possibility of deliberately choosing to conduct admittance measurements, when practical, at a higher temperature and frequency range where the conductance of the back contact remains strictly temperature controlled through the barrier height. Then information about a back contact shunt with weak temperature dependence could potentially be obtained by examining the temperature range over which TAS can recover the barrier height. However, it has been theorized that the observed shunting of the back contact can be primarily the result of moderate spatial inhomogeneities in the barrier height itself, rather than pinholes or ohmic conduction channels such as trap-assisted tunneling, and modeling on this basis can accurately describe certain CdTe JVT results [4]. In this case, the temperature dependence of the back contact shunt is strong and must be accounted for in the analysis.

CHAPTER 3

ELECTROCHEMICAL CAPACITANCE-VOLTAGE APPLICATION FOR SOLAR CELLS AND CAPACITANCE-VOLTAGE MEASUREMENTS

The description of capacitance measurements in a two diode model is a helpful foundation to develop a novel application of electrochemical capacitance voltage profiling. Traditionally ECV is useful as a method to progressively etch and characterizing the doping and defect concentrations in thicker films [10]. However, the preceding discussion illuminates voltage and frequency regimes where the capacitance response of a two junction structure is associated with only one junction, i.e. only one depletion region. Capacitance-voltage profiling is known to be unreliable when junctions are driven into strong forward bias due to the minority carrier diffusion capacitance and a high conductance to capacitance ratio (low phase angle) [11]. This means that for processes and devices that result in uneven carrier concentrations it can be difficult to access information about the doping and defect concentrations close to, for example, an absorber/emitter interface.

ECV offers a means to access that information in thin film solar cells prior to deposition of a contact layer, through the introduction of an electrolyte-semiconductor contact that is fairly similar in principle to a metal-semiconductor Schottky contact. As described earlier, for suitably low frequencies and when the Schottky contact is limiting ($G_p \gg G_s$), only the contact barrier capacitance is measured by an external circuit, and by extension only charge associated with the back contact depletion region. The conductance constraint (along with chemistry considerations) guides the choice of appropriate electrolyte – here the aim is to deliberately introduce a large barrier opposite

to the main junction, such that across a large voltage range only the capacitance response of the semiconductor-electrolyte junction is measured.

Electrolytes placed into contact with semiconductors must also reach an equilibrium in accordance with the Fermi level of the semiconductor [12]. The degree of charge transfer and associated band bending is a function of the choice of redox species in the electrolyte and concentration (acidity) in accordance with the Nernst equation. For an appropriate choice of electrolyte, large barriers to hole or electron transport may be formed. Charge transport between semiconductor and electrolyte is substantially different from of a metal-semiconductor junction [13]. Electrons are transferred to the oxidized species and transferred from the reduced species, which occupy different energy distributions.

In the case of a p-type absorber in a CdTe solar cell, an appropriate choice of electrolyte results in a band diagram similar to [13]:

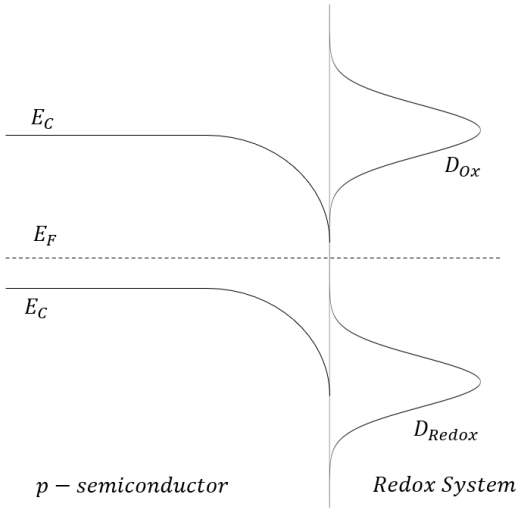

Figure 5 - Band diagram with a large barrier for p-type semiconductor

Here forward current consists of majority carrier hole transfer to the reduced species. The oxidized species cannot contribute electrons to the conduction or valence band of the semiconductor, and minority carriers are not present in sufficient numbers to constitute significant current. The energy separation between the oxidized and reduced states is termed the reorganization energy, and is difficult to approach theoretically [14]. But the potential of the electrolyte itself is easily understood, and for well-prepared semiconductor surfaces large barriers to current conduction can be created and checked experimentally.

Semiconductor-electrolyte charge transfer can be limited by charge transfer kinetics at the surface, or diffusion of the ions in the electrolyte, but this is more likely to be significant in forward bias with larger currents [13]. In the simpler case under reverse bias it instead behaves essentially as a Schottky diode, though there are additional theoretical considerations involving the formation of the Helmholtz layer, its capacitance contribution (usually negligible), and voltage drop across the Helmholtz layer itself. In any case, so long as a depletion region forms and responds to voltage over a range of interest in the expected manner and conductance is very low, characterization of the absorber is possible despite the presence of an additional junction in the device. In fact, the frequency dependence provides a very useful check on the validity of the capacitance measurement – if further reductions in frequency noticeably change the extracted capacitance over the voltage range of interest, then this can indicate that the conductance ratio or choice of frequency is inadequate to extract only the back junction capacitance. However, this potentially runs afoul of other frequency dependent capacitance elements (see TAS discussion).

Satisfying the conductance requirement in the context of C-V characterization rather than TAS characterization necessitates the definition of an appropriate voltage range, and a full consideration of Schottky barrier conductance as a function of applied voltage. Here two reverse leakage current mechanisms are evaluated: thermal generation in the depletion region and bias dependent barrier lowering due to the surface charge, commonly described in terms of the image force applied to approaching charge carriers [1]. If thermal generation current is included in the reverse characteristic, it takes the form:

$$J_{reverse} = \left(J_0^p + J_0^n\right)\left(\exp\left(\frac{qV}{kT}\right) - 1\right) - \frac{qn_i\sqrt{\frac{2\varepsilon}{qN_A}(V_{bi} - V)}}{\tau_p + \tau_n}$$

Where J_0^p and J_0^n describe the electron and hole saturation currents, n_i is the intrinsic carrier concentration, $\tau_{p,n}$ are the electron and hole bulk lifetimes, and V_{bi} is the built in voltage of the junction.

As the minority current contribution is negligible, J_0^n is discarded, resulting in a conductance:

$$G_{reverse} = \frac{qn_i\sqrt{\frac{2\varepsilon}{qN_A}}}{2(\tau_p + \tau_n)\sqrt{(V_{bi} - V)}} + \frac{d}{dV}\left[J_0^p\left(\exp\left(\frac{qV}{kT}\right) - 1\right)\right]$$

Schottky barrier lowering for a hole barrier is described by [1]:

$$J_{0,Sch} = A^*T^2\exp\left(\frac{q\phi_{B0} - \Delta\phi_B}{kT}\right) = A^*T^2\exp\left(\frac{q\phi_{B0}}{kT}\right)\exp\left(\frac{q\left(\frac{q^3N_A(V_{bi} - V)}{8\pi^2\varepsilon^3}\right)^{\frac{1}{4}}}{kT}\right)$$

Where $J_{0,Sch}$ is the saturation current of the Schottky barrier, which becomes a function of voltage if barrier height modulation is accounted for. The change in barrier height is $\Delta\phi_B$, N_A is the hole doping, and V_{bi} is the built in voltage of the junction. The barrier height can be related to the built in voltage by:

$$\phi_{B0} = V_{bi} + \frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right)$$

The conductance associated with Schottky barrier lowering is:

$$\frac{d}{dV}J_{0,Sch} = \frac{-A^*Tq^4N_A}{4 * 8k\pi^2\varepsilon^3}\left(\frac{8\pi^2\varepsilon^3}{q^3N_A(V_{bi}-V)}\right)^{\frac{3}{4}}\exp\left(-\frac{q\phi_{B0} - q\left(\frac{q^3N_A(V_{bi}-V)}{8\pi^2\varepsilon^3}\right)^{\frac{1}{4}}}{kT}\right)$$

Or, expressed more simply:

$$\frac{d}{dV}J_{0,Sch} = \frac{-q}{4kT}\left(\frac{q^3N_A}{8\pi^2\varepsilon^3}\right)^{\frac{1}{4}}\left(\frac{1}{(V_{bi}-V)}\right)^{\frac{3}{4}}J_{0,Sch}$$

The total reverse conductance, if a shunt is also present, is:

$$G_{reverse} = \frac{qn_i\sqrt{\frac{2\varepsilon}{qN_A}}}{2(\tau_p+\tau_n)\sqrt{(V_{bi}-V)}} + \frac{d}{dV}\left(J_{0,Sch}\right)\left(\exp\left(\frac{qV}{kT}\right)-1\right) + \frac{q}{kT}J_{0,Sch}\exp\left(\frac{qV}{kT}\right) + \frac{V}{R_{sh}}$$

In practice, thermal generation is negligible in comparison to barrier lowering, especially in materials with lower intrinsic carrier concentrations. Analytical evaluation of this conductance is difficult. Consideration of these equations reinforces the importance of the large built in voltage V_{bi} in suppressing leakage current and reducing conductance.

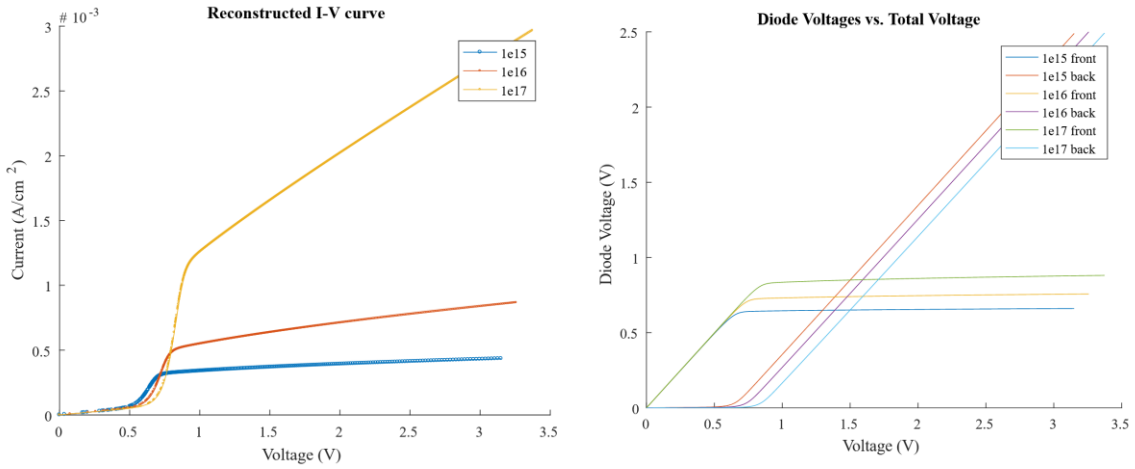

Figure 6 - I-V, V-V curves for two diodes

A similar effort to describe the forward conductance of the absorber/emitter junction in conjunction with the previous description of Schottky leakage can be fed into a numerical model to generate representative I-V and C-V characteristics for the series combination. The above characteristics in Fig. 6 are derived by assuming the doping level determines the barrier height at both junctions (ideal case, no surface pinning), resulting in the doping variation illustrated. The saturation of the reverse diode is clearly visible in the characteristic, as is the transition between voltage falling across the forward diode to voltage falling across the back diode.

The capacitance for an abrupt one sided junction is given by [11]:

$$C_{dep} = \left[\frac{qN_A\varepsilon}{2(V_{bi} - V)}\right]^{1/2}$$

Therefore the capacitance associated with each diode follows naturally from the recovered voltage falling across each one shown in Fig. 6.

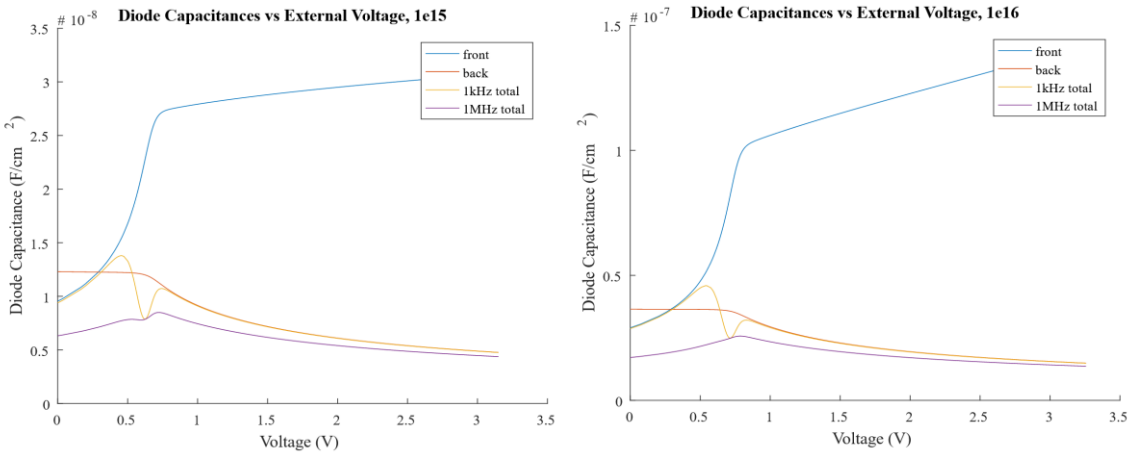

Figure 7 - Individual capacitance contributions and total high/low frequency capacitance response for external voltage

The capacitance of each diode and the total measured capacitance as a function of external applied voltage and frequency for an appropriate choice of front and back junction parameters show interesting behavior. The frequency dependence illustrated here clearly shows the recovery of the back contact capacitance (orange line) at low frequencies (yellow line), whereas at high frequencies the recovered capacitance (purple line) is more representative of the total series capacitance. Note the change in voltage ranges for which C-V extraction of the back contact is valid – these correlate with the saturation of the front contact voltage. The conductance ratio $\frac{G_p}{G_s}(V)$ describes the valid characterization regime:

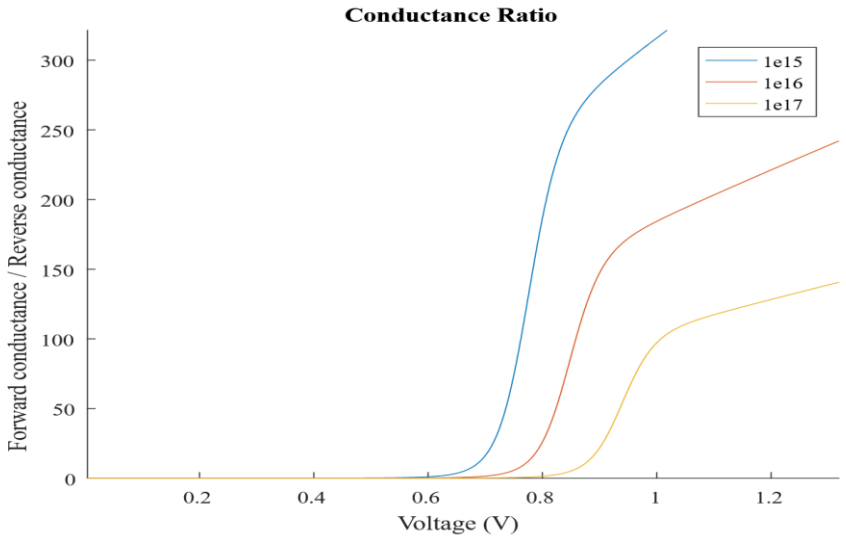

Figure 8 - Conductance ratio of diodes

These figures are illustrative of the general model, but in fact it is desirable to have a barrier height such that the front voltage saturates almost immediately, and the back contact is limiting across almost all reverse biases. The exponential dependence of the leakage current on barrier height means that even relatively small (200meV) increases result in characteristics entirely dominated by the semiconductor-electrolyte junction.

There is an important consideration with regards to ECV and the implementation of a deliberately high barrier at the semiconductor-electrolyte interface.

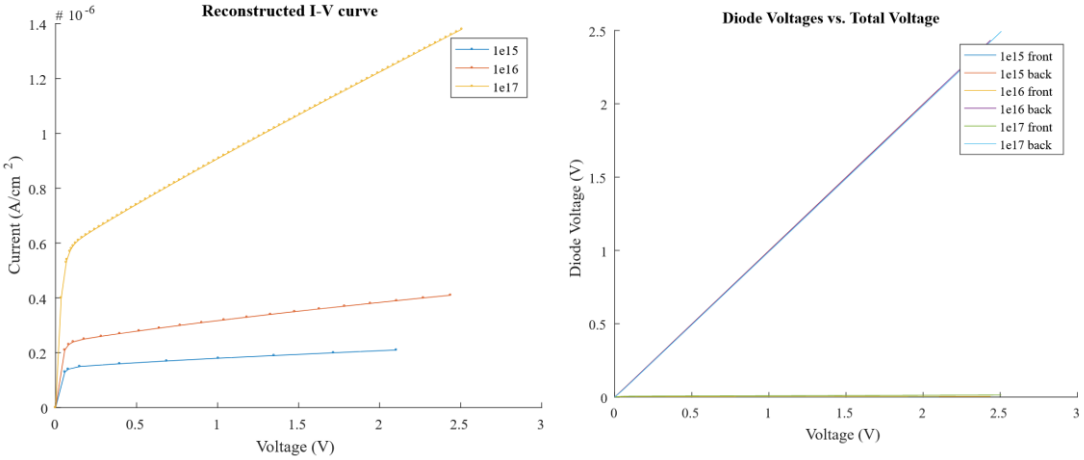

Figure 9 - I-V and V-V for high barrier

For this very high barrier the low frequency characteristic no longer entirely recovers the back contact capacitance.

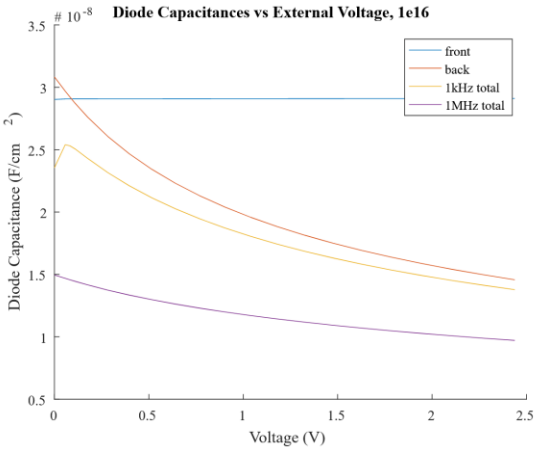

Figure 10 - Capacitance vs. voltage and frequency, high barrier

Returning to the characteristic frequency expression, restated for convenience:

$$\omega_C = \frac{G_s + G_p}{C_{Sch} + C_{pn}}$$

Here the conductance of both diodes is very low, even though the forward voltage across the structure is significant. When the back contact barrier is too limiting, the forward biased junction saturates immediately and is pinned, while the back contact conductance is very low and does not vary quickly with voltage. The consequence of this is that the recovered capacitance signal is stuck slightly towards the middle and slowly recovers towards the single junction ideal with increasing reverse voltage, resulting in an incorrect extraction of N_A. For this and other reasons deployment of ECV should be accompanied by comparison with typical C-V characterization of known uniform samples to determine the parameter range of valid measurements.

ECV of course also offers the potential to progressively etch away the absorber. In the case of p-type CdTe this is done very readily through forward biasing of the back contact barrier, or reverse biasing of the device, which depletes bonds at the surface and allows the electrolyte to attack the crystal rapidly. This results in and is evidenced by an observed hysteresis and evolution of the I-V characteristic as voltage is swept into forward bias and back repeatedly, in addition to visible sample etching post measurement. However, for inhomogeneous materials (like polycrystalline CdTe) that may more rapidly etch at grain boundaries or even for more homogenous materials this poses an additional risk in this context because the maintenance of low reverse conductance is crucial to suppress the response of the front junction. Therefore etching, which may alter the surface quality and the properties of the reverse leakage current, requires care.

The capacitance-voltage of a CdTe solar cell provided by NREL was measured at low and high frequencies to attempt to capture behavior associated with two-diode model described above:

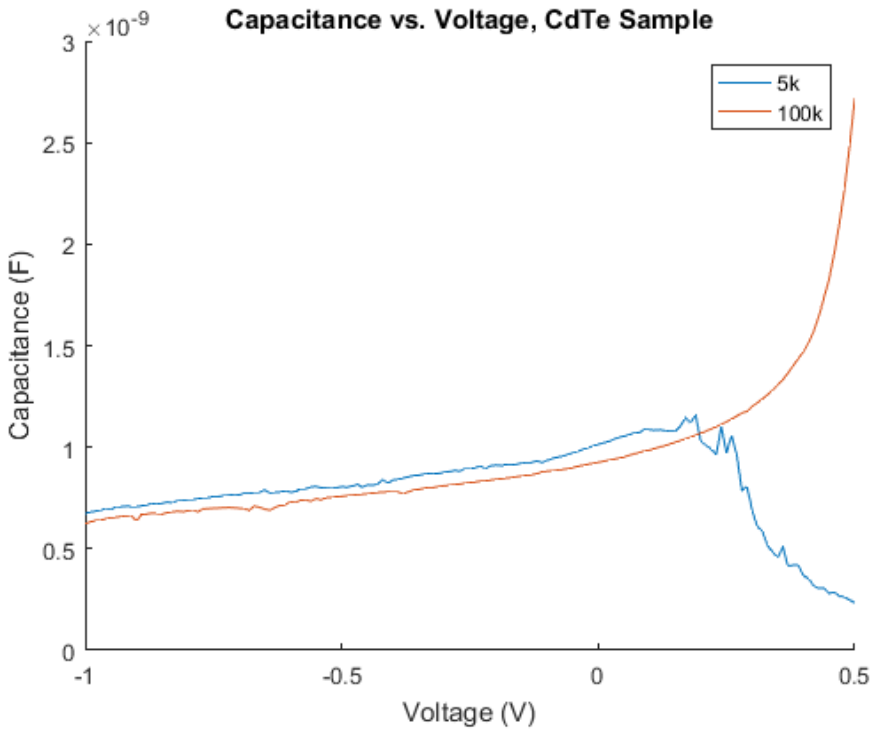

Figure 11 - Measured C-V of CdTe cell at low/high frequencies (5kHz, 100kHz)

These results do not strongly agree with the two diode model. Here the capacitance decrease of the 5kHz characteristic going into forward bias could make sense when understood in terms of voltage sharing with a back contact barrier (see Fig. 6, 1kHz characteristic), but the behavior of the 100kHz characteristic is in contrast to expected behavior – the sharp increase in forward bias specific to high frequency is hard to attribute and cannot be understood in terms of the two-diode model, nor in terms of classical descriptions of bulk defects, which should contribute capacitance responses at any frequency lower than their characteristic frequency. Instead it is more representative

of a typical pitfall of C-V forward bias characterization, namely the contribution of a minority diffusion capacitance that increases with lower frequency [11]. However, this is unlikely to be the case given the intrinsic carrier concentration and hole lifetime in polycrystalline CdTe [6], and the conductance of both measurements in the forward bias regime is similar. Further experimentation is necessary to clarify the behavior of this device. In the negative voltage regime the Schottky barrier is expected to always have high relative conductance due to its much larger saturation current, so the expected behavior is not symmetrical and a treatment of the C-V response in terms of a two diode model is of less interest.

CHAPTER 5

SUNS-VOC AND VOC(T)

Contact barriers also influence measurements of Suns-Voc and Voc(T). In Suns-Voc, it is understood that contact barriers can result in a "rollover" of the characteristic, or a decrease in the open circuit voltage as illumination intensity increases [15]. Existing literature describes this in terms of a shunted back contact operating as a solar cell with an opposite polarity [16],[17]. The argument is that increasing opposite voltage builds on the back diode with increasing intensity, and a voltage develops across the shunt faster than the voltage increase of the solar cell associated with illumination intensity, thus generating a characteristic that initially climbs and then rolls over.

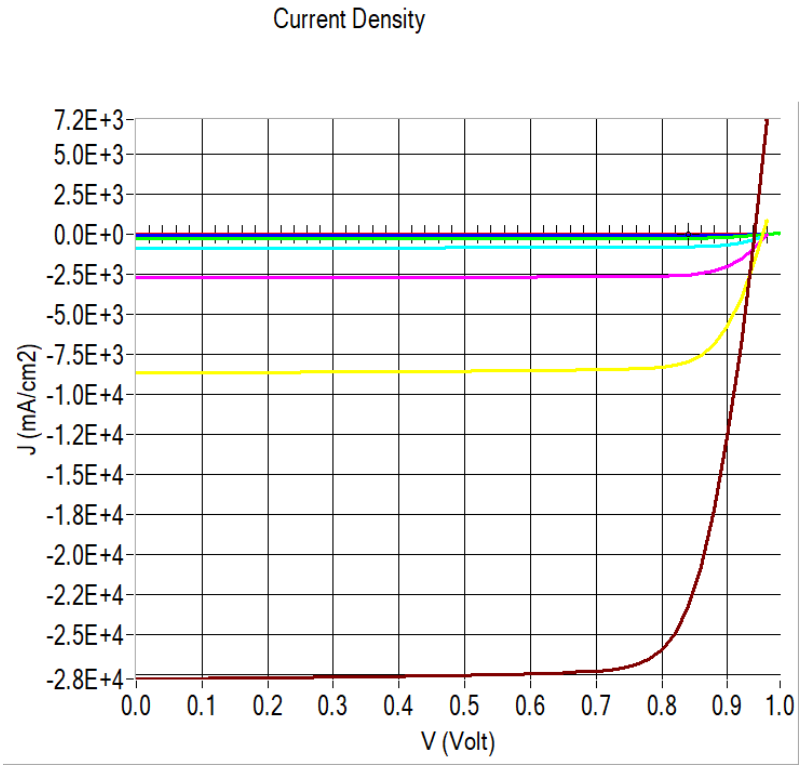

Figure 12- Simulated I-V curves Illustrating decreasing open circuit voltage with increasing illumination intensity. Illumination is increased from 1 to 1000 suns over 7 steps.

While this can be a reasonable physical model in devices with poor contact material quality and can be fit to experimental data, device physics simulations show it is entirely possible to observe Suns-Voc rollover in thin film, small area devices with even contact, and the introduction of a back contact shunt resistance is not necessary to explain the behavior. Analytical approaches generally fail because the superposition principle explicitly does not hold when Suns-Voc rollover is observed – i.e., the description of an independent photocurrent superimposed on a dark current is not accurate. This is illustrated in Fig. 11, where the open circuit voltage decreases at high illumination. A plot of the open circuit voltage points against the illumination intensity (roughly the short circuit current) yields a concave down characteristic. Computational simulation has been used to guide a qualitative description of this behavior in the context of analyzing a-Si cells [18]. Here an interpretation of Suns-Voc rollover in a particular CdTe structure is given and explored via simulation.

Simulations are carried out using SCAPS-1D, a solar cell simulation program that solves the coupled system of equations describing potential, current, and charge distribution in a one dimensional structure, developed by Marc Burgelman and collaborators at the University of Ghent. One way to conceptualize the voltage loss associated with the back contact barrier under increasing illumination intensity relates to the transport of minority carriers through the absorber to the "wrong" contact, which is related to the frequently observed "crossover" of light and dark I-V curves associated with a back contact barrier in CdTe cells [3]. This particular structure is simplified to yield an easily understood but meaningful analysis – the heterointerface at the absorber/emitter junction is defect free, and the valence band offset is prohibitive to hole

transport, such that the predominant loss mechanism is entirely recombination at the back contact. The metal contact itself has a surface recombination velocity equal to the thermal velocity of the charge carriers.

As illumination intensity increases, minority carrier concentration increases throughout the absorber, and in particular the minority carrier concentration close to and approaching the back contact increases. At open circuit voltage, an equal population of holes recombines at this back contact. The voltage associated with injecting a sufficient hole population to the back contact can be considered the open circuit voltage loss incurred by the back contact opposite polarity diode. Stated another way, the voltage necessary to drive larger electron populations from the front of the device (in the model, a heavily n-doped transparent conductive oxide layer) to the back contact decreases as illumination increases (note that illumination results in generation highest immediately adjacent to the TCO/absorber interface). Experimentally observed crossover can then also indicate a contact barrier and be explained by this framework. A heterostructure with a significant back contact barrier of 0.5eV is simulated in the dark and at short circuit 1 sun condition, yielding the following band diagrams:

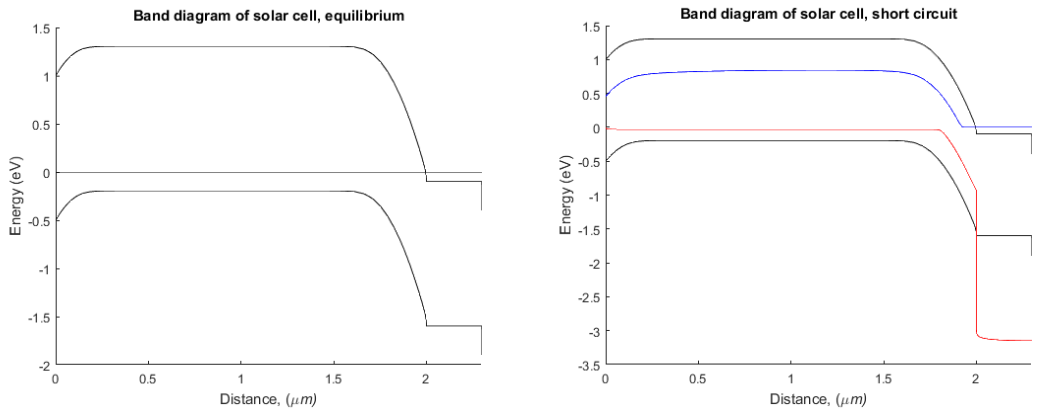

Figure 13 - Equilibrium and short circuit band diagrams

At open circuit, the carrier concentrations and band bending in the absorber are:

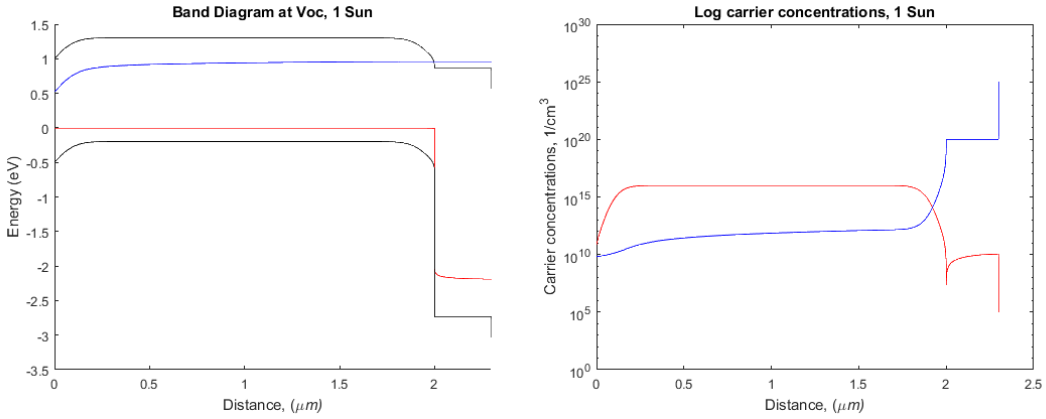

Figure 14 - Left: Band Diagram with quasi-Fermi levels. Right: Carrier concentrations

For very high illumination, at 1000 suns, the carrier concentration and band bending in the absorber very near open circuit voltage are:

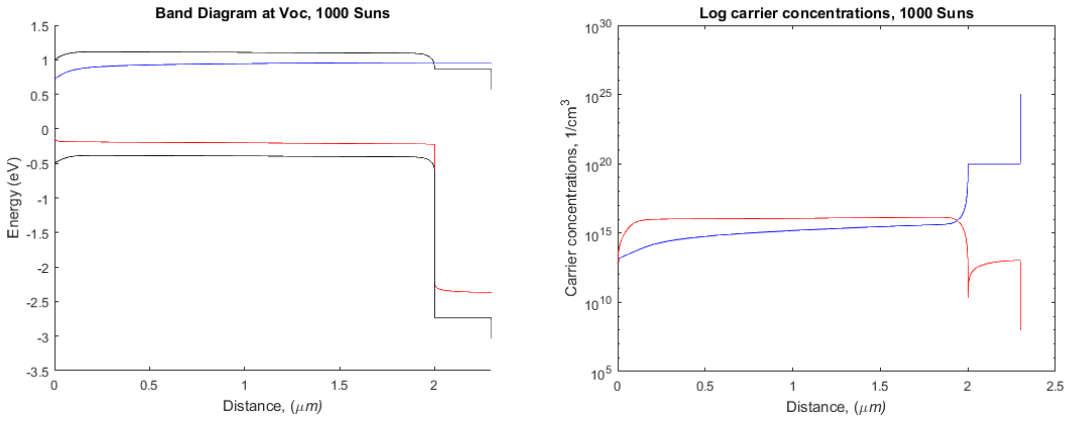

Figure 15- Left: Band Diagram with quasi-Fermi levels. Right: Carrier concentrations

While the quasi-Fermi level separation at the heterointerface strictly increases with suns, as reasonably expected, the hole-quasi Fermi level approaching the hole contact begins to collapse significantly only at higher intensities. The electron current towards the hole contact increases roughly proportionally with suns, resulting in an increasing recombination loss and opposing voltage. This demonstrates that the two diode model, while it offers a robust description of dark I-V and C-V measurements, may need some

adjustment beyond treating the back contact as a shunted, opposite polarity solar cell under illumination.

Experimental characterization of the Suns-Voc response of a GaAs and CdTe solar cell was also performed using an incident 532nm laser, a wavelength near the peak of the solar spectrum, in the hope of contrasting fairly ideal behavior against a non-ideal rollover characteristic. However, experimental limitations limited the available power density to conduct experiments, and the following Suns-Voc characteristics result:

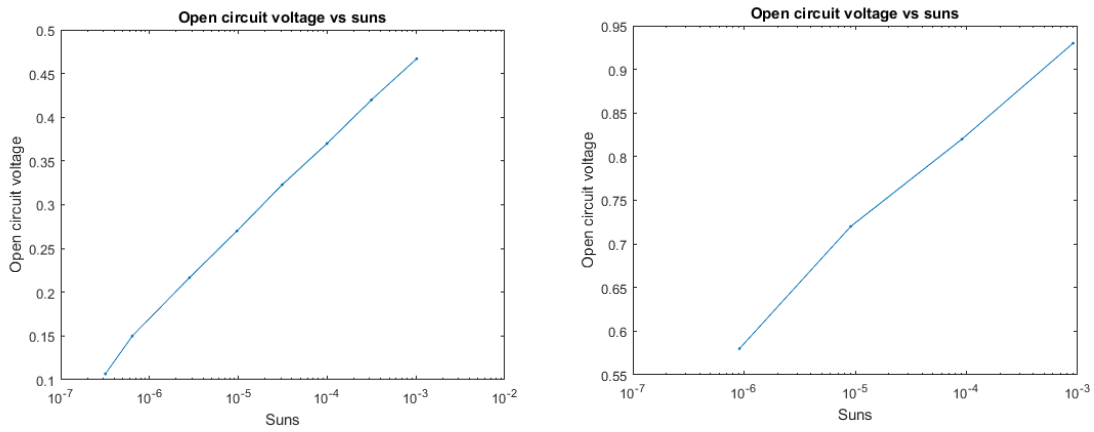

Figure 16 – Suns Voc Measurement. Left: CdTe, right: GaAs

Here no rollover can be observed even in the presence of a significant barrier because intensity is well below even 1 sun. These illumination intensities are rough approximations given the power supplied to the laser and the sample area, but are accurate within an order of magnitude. Extraction of the ideality factor from:

$$V_{oc} = \frac{nkT}{q} \ln\left(\frac{J_L}{J_0}\right)$$

Yields $n \cong 2$ for both samples, indicating the expected dominance of depletion region recombination at low intensities and forward currents.

Examination of the variance of the open circuit voltage with temperature can also give some insight into the presence of a contact barrier in the device and its impact on performance [19]. Typical Voc(T) measurement is used to extract an activation energy associated with the dominant recombination channel in the device, and more sophisticated analyses even attempt to extract the balance of recombination mechanisms [20]. In the simple ideal case for a p type absorber:

$$V_{oc} = E_{Fn} - E_{Fp} = E_g - \frac{kT}{q} \ln\left(\frac{G\tau_n N_A}{N_C N_V}\right)$$

Thus as temperature drops the open circuit voltage is expected to increase nearly linearly towards the band gap limiting the quasi-Fermi level splitting. In the case of heterostructures with interfaces providing a reduced effective band gap for recombination, or "cross recombination," Voc(T) can provide information about the relative prevalence of this recombination mechanism [21].

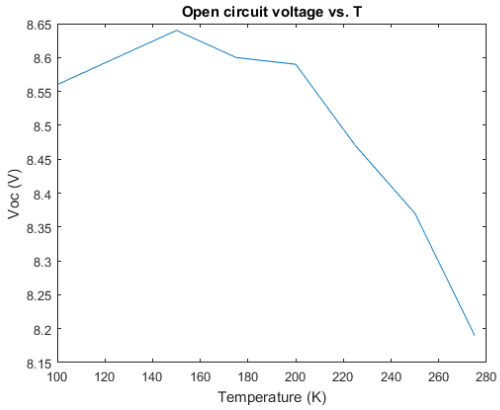

Figure 17 - Open circuit voltage rolls over and decreases at low T in measured CdTe sample

In all cases, the activation energy is extracted from a linear portion of the Voc(T) characteristic at higher temperatures. In the presence of contact barriers, the open circuit

voltage can again experience a rollover, which can also be described in terms of the voltage loss associated with pushing holes to the back contact.

Here, instead of increasing illumination driving the increasing voltage associated with driving holes over the back contact potential hill, a decrease in temperature and associated reduction in thermionic emission current can cut into or overcome the expected gain in open circuit voltage. Earlier, more severe rollover is a sign of a higher barrier due to the increasing voltage loss associated with thermionic emission current. The Voc(T) characteristic for the CdTe cell is found simply by extraction from the JVT curve family presented in Fig. 2 at zero current. The fairly minimal gain with decreasing temperature and the saturation/rollover are again indicative of the back contact barrier. Therefore for extraction of the activation energy governing the dominant recombination loss mechanism, it is necessary to extrapolate from higher temperature regimes.

In summary, a review and analysis of various experimental techniques to qualify and describe contact barriers is provided, along with experimental results utilizing several of these techniques. The temperature dependence of the thermionic emission limited current is most easily observed in the JVT curve family, but is also relevant to TAS measurements. A two diode C-V model allows the definition of regimes where C-V and ECV measurements provide meaningful information about the back contact junction and the solar cell as a complete device, and details of this model guide the experimental approach. Experimental C-V characterization suggests further investigation. A specific mechanism responsible for the Suns-Voc rollover often attributed to a general back contact shunt is provided and explored via simulation.

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