EMI Modeling and Optimized EMI Filter Design for PFC Topologies

by

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ABSTRACT

With the emergence of electric transportation and the infrastructure for electric vehicles (EVs), numerous viable approaches and topologies have emerged. In order to improve the power quality of the grid, it is essential for Onboard Battery Chargers (OBC) for electric vehicles to maintain a power factor closer to unity. This study mainly focuses on two prominent PFC topologies, Totem-pole PFC (TPFC) and H-Bridge PFC (HPFC), which are simple to implement and capable enough of providing high operating efficiency. This study elucidates the comprehensive comparison of the TPFC and HPFC converters using the comprehensive mathematical modeling approach, simulation models, and the hardware experiments. Also, the comparison of the EMI filter requirement and design of DM EMI filter for both the topologies is also extensively illustrated in this study.

Firstly, focusing the comprehensive mathematical models of TPFC and HPFC converters, which includes the mathematical formation of the duty cycle for both the converters incorporating the discretized input current controller into the mathematical model which gives more closer comparison when it is compared to simulation models and the hardware experiment model operations. The input current FFT analysis and the THD modeling are also covered in the mathematical modeling of TPFC and HPFC converters. Moreover, the EMI noise is modeled, and the corresponding EMI filter is also designed for both the PFC topologies.

Further, the simulation models of TPFC and HPFC converters are also developed and the outputs of the simulation models show an input AC current is precisely following the input AC voltage and also the output voltage of constant 400V is attained for both the

PFC converters. Similarly, for the experimental results, the constant 400V regulated DC output voltage is obtained and the input AC current is following the input AC voltage with the power factor of 0.983 for TPFC and 0.99 for HPFC converter. Moreover, the implementation of the EMI filter at the front end of the converter succinctly attenuates the EMI noise and complied within the FCC Class A limit for both TPFC and HPFC converters.

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CHAPTER 1

INTRODUCTION

1.1 Overview of Grid Infrastructure

The present grid infrastructure, also known as the electrical grid or power grid, is a complex network of interconnected power generation, transmission, and distribution systems that supply electricity to homes, businesses, and industries across the world. The grid infrastructure varies from country to country and region to region, but it generally consists of the following components:

1. Power generation facilities: These facilities use various sources such as fossil fuels (coal, oil, and natural gas), nuclear, hydropower, wind, solar, geothermal, and biomass to produce electricity.
2. Transmission lines: These high-voltage power lines transport electricity over long distances from power generation facilities to substations.
3. Substations: These facilities transform the high-voltage electricity received from the transmission lines into lower voltage electricity suitable for distribution to homes and businesses.
4. Distribution lines: These low-voltage power lines deliver electricity from substations to homes, businesses, and industries.
5. Consumers: The end-users of electricity who consume it for various purposes.

The grid infrastructure also includes various control systems, such as SCADA (Supervisory Control and Data Acquisition) systems and automatic switches, which enable grid operators to monitor and manage the flow of electricity to ensure a reliable and stable

supply of electricity to consumers [1]. The present grid infrastructure faces various challenges such as aging infrastructure, increasing demand for electricity, cybersecurity threats, and integrating renewable energy sources into the grid [2]. To address these challenges, there are ongoing efforts to modernize and upgrade the grid infrastructure by incorporating digital technologies such as advanced sensors, communication networks, and machine learning algorithms [3]. Figure 1.1 shows the present grid infrastructure which includes the integration of renewables with the conventional energy sources.

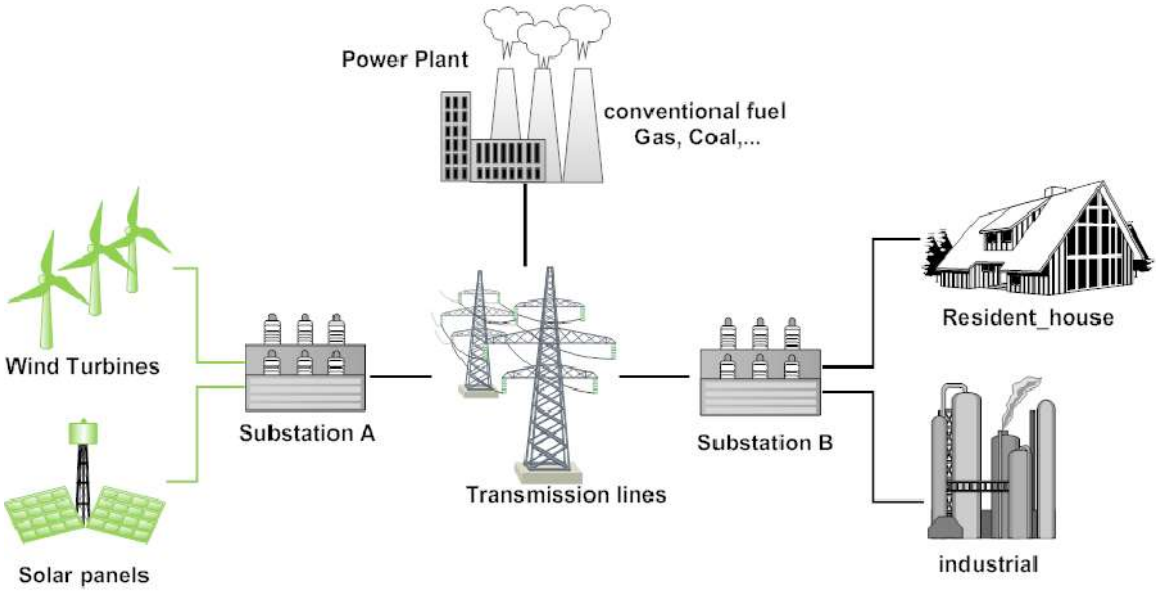

Figure 1.1: The General Structure of Integrating Renewables Energy into AC Grid [4]

With the increasing adoption of renewable energy sources such as solar PV and wind turbines, the complexity of interconnecting them has increased. This is because renewable energy sources are often distributed and intermittent in nature, which requires a more sophisticated power system infrastructure to manage. In traditional power systems, power is generated by a few large power plants and transmitted over long distances to the end-users.

However, renewable energy sources such as solar PV and wind turbines are often located in remote areas, which makes it difficult to transmit the power over long distances. As a result, renewable energy sources are typically connected to the distribution grid, which is a lower voltage level than the transmission grid. The standard and technical guidelines for the interconnection of the renewable energy sources into the Distribution grid is extensively described in [5]. The interconnection of renewable energy sources to the distribution grid requires a complex control system that can manage the variability and intermittency of these sources. This control system needs to ensure that the power quality and stability of the grid are maintained, even as the power supply from the renewable energy sources fluctuates [6,7].

One of the key challenges in interconnecting renewable energy sources to the grid is the need for power electronics to interface between the renewable energy source and the grid [8]. Power electronic converters are essential components in renewable energy systems, such as solar photovoltaic (PV) panels and wind turbines. These systems generate DC power, which needs to be converted to AC power for integration into the grid. Power electronic converters use semiconductor devices, such as transistors and diodes, to switch DC voltage on and off at high frequencies, creating a waveform that approximates AC voltage. This process is known as pulse-width modulation (PWM). The output voltage and frequency can be controlled by adjusting the timing and duration of the switching events.

1.1.1 Integration of EVs into the Smart Grid

The integration of electric vehicles (EVs) into the smart grid is becoming an increasingly important topic in the field of energy systems. EVs are a form of clean and renewable energy that can help reduce greenhouse gas emissions and improve energy efficiency. Figure 1.2 depicts how the conventional energy sources and the renewables including electric vehicles are interconnected into the smart grid.

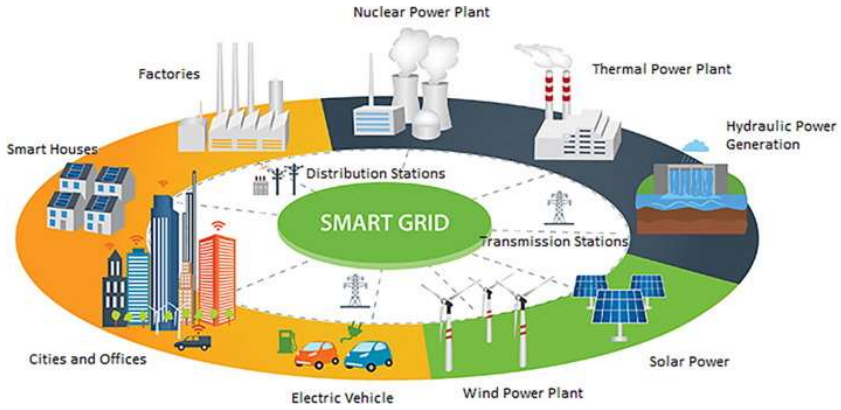

Figure 1.2: Smart Grid [9]

At the same time, the smart grid enables advanced technologies that allow for a more efficient and reliable distribution of electricity [10]. By integrating EVs into the smart grid, electric vehicle owners can use the grid as a source of energy for charging their vehicles [11]. This has the potential to provide a more stable and reliable source of electricity than relying solely on the power supplied by the local utility [12]. Furthermore, the smart grid can help manage the demand for electricity and improve the efficiency of the charging process [13].

Further, Vehicle-to-Grid (V2G) technology is a promising solution that enables electric vehicles (EVs) to participate in the power system as active demand response resources. By allowing EVs to be used as storage devices, V2G can help to reduce peak demand and improve the overall efficiency of the power system [14]. However, the

implementation of V2G technology in power systems can lead to both positive and negative effects, which are listed below. [15,16]

1. The flexibility of the load can be increased, and the grid can be balanced by charging and discharging electric vehicles according to the needs of the power system.
2. V2G can help to reduce emissions and enhance air quality by allowing EVs to be charged using renewable energy sources.
3. The stability of the power grid can be improved by providing grid services such as frequency regulation and voltage support through V2G.
4. During peak times when EVs are charging, V2G could potentially increase the demand on the power system.
5. There is a possibility of battery degradation in EVs due to frequent charging and discharging as a result of V2G.

The integration of V2G technology could potentially increase the complexity of power system management, requiring new technologies and control systems to manage the interaction between EVs and the grid [17]. The widespread adoption of electric vehicles (EVs) is considered to be a crucial step towards reducing carbon emissions and combating climate change. However, the increasing number of EVs on the roads presents a significant challenge to the power grid. As more people switch to electric vehicles, there will be a significant increase in demand for electricity, especially during peak charging periods [18,19,20]. Figure 1.3 shows the schematic of V2G power transfer schematic bidirectional power electronics converters are included which helps in charging the vehicle and transferring the power from vehicle to grid as well [21].

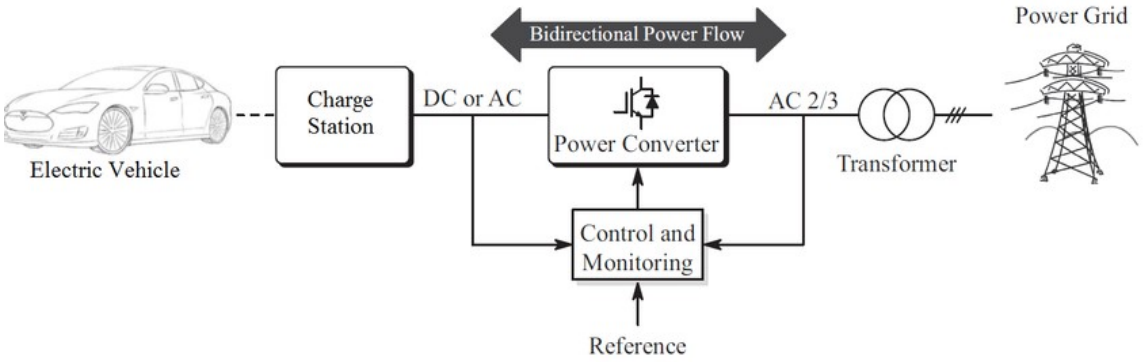

Figure 1.3: Block Diagram of V2G Structure [21]

The challenge of EV (electric vehicle) charging is multi-faceted, and requires solutions in both infrastructure and energy management. One of the key challenges is the need to expand the charging infrastructure to support the growing number of EVs on the road [21]. This includes not only public charging stations, but also charging facilities at workplaces, homes, and other locations. As more and more people switch to EVs, the demand for charging facilities will increase, and the infrastructure needs to keep pace.

The second challenge is related to the power grid. With the increased demand for electricity from charging EVs, the power grid needs to be able to handle the increased load [22]. This requires not only adding more generation capacity, but also upgrading the grid infrastructure itself to handle the increased demand. Failure to address these challenges can result in overloading of the power grid during peak charging periods, leading to power outages or other grid disturbances.

To address these challenges, a multi-pronged approach is needed. Governments and private companies need to invest in building out the charging infrastructure, with a focus on strategic locations such as major highways and urban centers. This can include providing incentives for private companies to build and operate charging stations, as well as funding for public charging facilities [23]. At the same time, efforts must be made to

upgrade the power grid to handle the increased demand for electricity. This can include the deployment of smart grid technologies to better manage and balance the load, as well as the integration of renewable energy sources such as wind and solar to provide additional generation capacity. Energy storage solutions such as batteries and pumped hydro storage can also play a role in helping to balance the load and manage peak demand [24].

The charging systems of an electric vehicle involves power electronic components such as Power Factor Correction (PFC) converters and isolated DC-DC converters. PFC converters that can be used in the EV OBCs is the focus of this study.

1.2 EV Charging Systems

EV charging systems are becoming more common as more people adopt electric vehicles. They can be found at public charging stations, in parking lots, and even in private homes. Many EV manufacturers also offer their own charging solutions, including home charging stations and access to their own network of public charging stations. Some different charging location can be seen in the Figure 1.4.

Charging at home Charging on public networks Charging at workplace

Figure 1.4: Charging Stations at Different Locations [25]

A charging system for electric vehicles (EV) is an infrastructure designed to charge the batteries of EVs. There are a variety of EV charging systems, each with its own distinct capabilities and characteristics [28]:

1. Level 1 Charging: Using a standard 120V AC household outlet, this is the most basic and sluggish method of charging. Level 1 charging can take up to eight to ten hours to fully charge a battery-powered vehicle.
2. Level 2 Charging: This type of charging requires a dedicated charging station and a 240V AC power source. Depending on the vehicle and charging station, level 2 charging can charge an electric vehicle in 3 to 4 hours.
3. Level 3 Charging: This is also known as DC fast charging. This is the quickest charging method and can charge an electric vehicle's battery to 80% capacity in 20 to 30 minutes. Level 3 charging requires specialized charging equipment and a DC power source.

In addition to that, there are different types of connectors are also used world wide for EV charging. In North America, the most common connectors that are used for Level 2 EV charging are SAE J1772 connectors. For Level 3 charging there are different types of connectors are used such as CHAdeMO, CCS (Combined Charging System). Tesla has their own charging connectors for Level 2 and Level 3 charging. The different power levels of Level 1, Level 2, and Level 3 charging systems and some other differences between them are presented in Table 1.1 [26].

Table 1.1 Power Levels of EV Charger [26]

Power Levels	**Level 1**	**Level 2**	**Level 3**
Grid Voltage	120 VAC (US) 230 VAC (EU)	240 VAC (US) 400 VAC (EU)	208-600 VAC or VDC
Power Limits (kW)	≤ 3.3	$3.3 - 20$	> 50
Charging Time (Hours)	4-36	1-6	0.2-1
Charger Placement	On-Board	On-Board	Off-Board
Phase Type	1 Phase	1 or 3 Phase	3 Phase
Charging Speed	Slow	Medium	Fast

The charging schematic of the different Levels of chargers are shown in the Figure 1.5 which mainly focuses on the power electronics circuits included in charging systems. The Level 1 and 2 requires the rectifier circuits as input power is in the form of AC and it is transferred to DC battery. On the other hand, Level 3 charging systems only requires DC-DC converters as the input supply is in the form of DC.

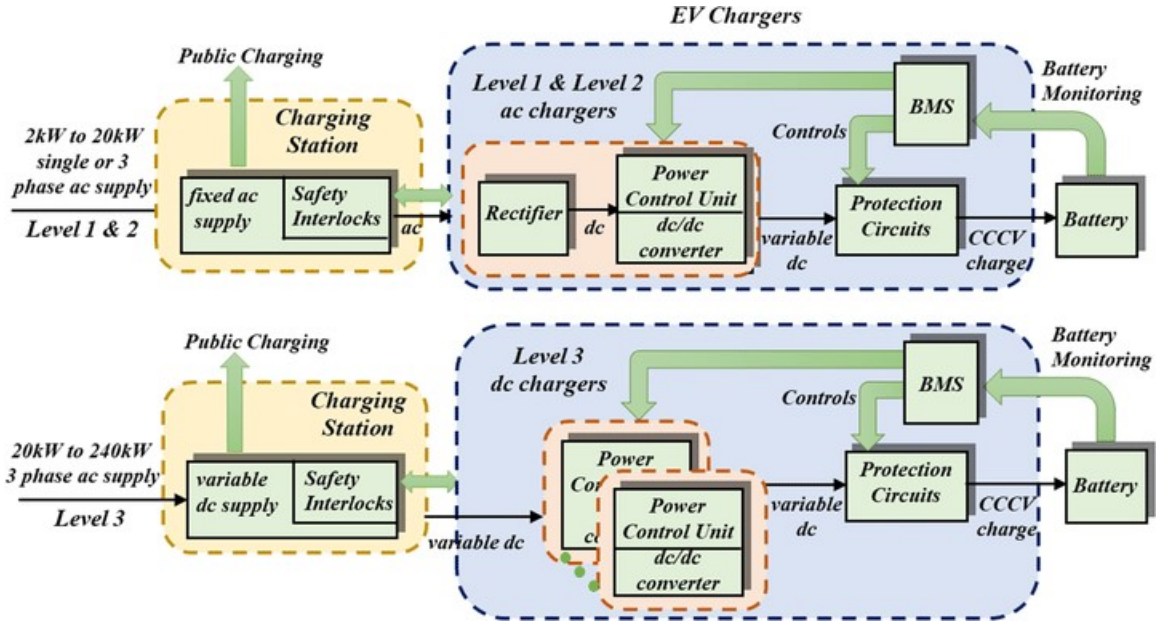

Figure 1.5: Block Diagram of the Level 1, 2 and 3 EV Charging [27]

From the Table 1.1, it can be seen that Level 1 and Level 2 charging systems can be employed as onboard battery chargers in the EVs itself. But as the Level 3 charging systems requires the high power as an input, these chargers are employed as off-board charging systems to provide regulated AC-DC conversion. Also, Level 3 chargers are not viable for the residential charging. These chargers are mainly employed in the commercial charging areas.

1.3 Power Factor Correction Converters

Ensuring compliance with rigorous power quality requirements, incorporating power factor correction at the input stage of any plug-in power electronic device designed for electric vehicular application has become essential aspect. The power factor correction (PFC) converters are more popular to be used in the EV Onboard battery chargers (OBC). There are varieties of PFC converters are popular to be used in EV OBCs. The Totem-pole PFC (TPFC) and H-Bridge PFC (HPFC) are focus in this study. There are some advantage of these two topologies of PFC over other techniques and topologies used for the rectification (AC-DC). These two topologies of PFC can be operated with high switching frequency which significantly reduce the size of the filter components. This helps in increasing he power density of the product and also leads to small size of OBC that can be employed in EVs.

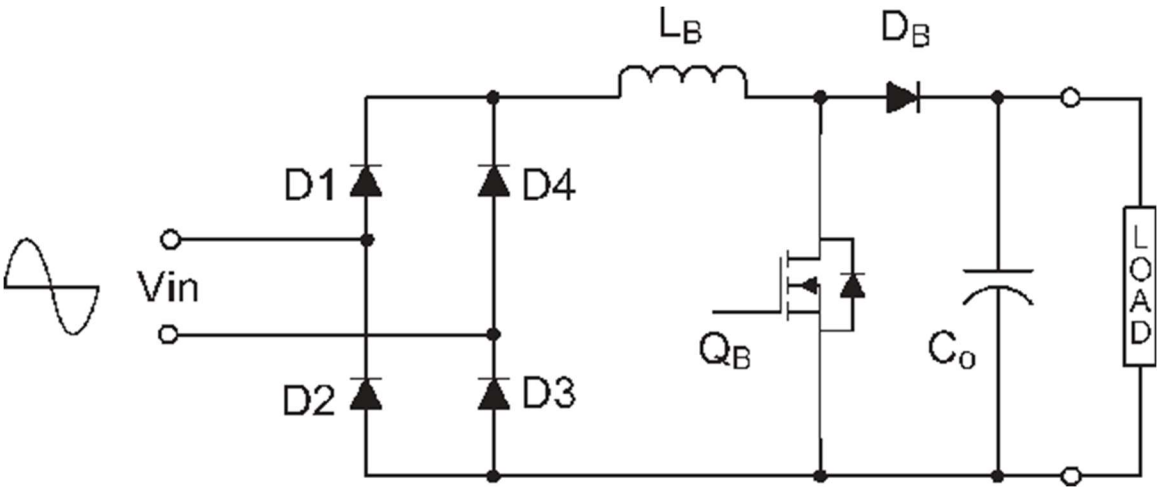

Figure 1.6: Conventional Boost PFC Converter [28]

When comparing these PFC topologies with the conventional Boost PFC converter which has a diode full bridge for rectification followed by the boost DC-DC converter as shown in the Figure 1.6, the diode bridge is eliminated from these advance PFC topologies

such as Totem-pole PFC and H-Bridge PFC converter. These PFC topologies has all active MOSFETS rather than a diode bridge which leads to lower conduction loss. An introduction of TPFC, interleaving of input side inductor to reduce the current ripple and other enhancements to reduce the overall size of the circuit have been discussed and well documented in [29,30]. Similarly, the H-Bridge PFC operation and its optimized design is exhaustively discussed and documented in [31].

In this study, the PFC topologies (i.e. Totem-pole PFC and H-Bridge PFC) are compared comprehensively and thoroughly discussed through their mathematical models, simulation models analysis, the hardware experiments.

1.4 EMI Related challenges in PFC converters

The EMI related challenges are introduced because of the high frequency switching operation of TPFC and HPFC converters. TPFC and HPFC converters usually operate at the switching frequency of several hundreds of kilohertz. An elevated switching frequency leads to a significant reduction in the volume of the input filter of the converter. But with higher operating frequency, it is essential to take care of the DM EMI noise emission. As the converter is directly connected to the grid-end in such applications, it is crucial to suppress EMI noise to comply with the FCC Class A/B standards ranging between 150kHz and 30MHz. Therefore, the EMI filter must be connected at the front end of the PFC converter. The three basic requirements that must be considered for designing DM EMI filters are as follows: (i) it should be able to suppress the EMI noise below standard level, (ii) it should not affect the power factor, and (iii) the system stability should not be impacted by the new zeros and poles introduced by the EMI filter transfer function [32]. This high frequency switching operation generated high frequency noise which can

interfere with the other electronics devices and components of the circuit which can result in the damage of some sensitive electronics components. This EMI noise generation also leads to reduced efficiency of the power electronic converters.

A practical approach in designing Mixed-Mode (MM) EMI filters for ac line powered converters is proposed in [33] where a complex design of MM EMI filter is presented when it is compared to the DM EMI filter design proposed in this study. The work done in [34] presents only about a DM EMI noise at different voltage and power levels for a boost PFC converter operating in critical conduction mode with a diode-bridge at the front-end. On the other hand, this study explains about the DM EMI noise and the EMI filter design for a more advanced PFC topology. The DM EMI filter is not discussed for such PFC design topology. In [35], the similar PFC topology as of [34] alongside its EMI compliance mechanism is discussed; however, the comprehensive design methodology while accounting for passives volume minimization and other converter constraints is absent in the discussion, which is described thoroughly in this study. The works conducted in [36] and [37] provide extensive information on the architectures of EMI filter networks and the volumetric optimization of EMI filters in three-phase PFC converters, which can be consulted to gain a better understanding of these topics.

1.5 Thesis Outline

As discussed in this chapter, the current grid infrastructure and the increasing involvement of the electric vehicles as a part of smart grid with some crucial guideline, it is essential to take care of some of the issues related to power electronics devices involved in these systems to make them more efficient and reliable to maintain the power quality of

the grid. The PFC converters are mainly discussed in this study and the comprehensive comparison of TPFC and HPFC converters is thoroughly discussed in the further chapters.

Chapter 2 elucidates the extensive comparison of TPFC and HPFC converter in terms of their mathematically modeled input current FFT analysis and THD modeling. Further, the incorporation of the discretized current controller into the analytical models of TPFC and HPFC is also discussed exhaustively in this study. Further, the analytical models of TPFC and HPFC converter are also compared with their simulations and experimental results.

Chapter 3 extensively explains the EMI modeling and the DM EMI filter design methodology for TPFC and HPFC converter. For the thorough comparison of the analytical model and hardware prototypes of TPFC and HPFC, the DM EMI filter designed considering the values obtained through the analytical models and the EMI filter having the identical parameters is employed at front end of the hardware prototype and their comparison is expressed in-depth in this chapter.

Finally, Chapter 4 makes some pertinent conclusive points and summarizes the technical findings presented in this work.

CHAPTER 2

COMPREHENSIVE COMPARISON BETWEEN TOTEM-POLE AND H-BRIDGE POWER FACTOR CORRECTION CONVERTERS

2.1 Introduction

Power factor correction (PFC) converters are widely used in modern power electronics to improve the power quality of electrical systems. Among various PFC topologies, the Totem-pole and H-bridge PFC converters have gained significant attention due to their high efficiency and low cost. As mentioned in Chapter 1, to ensure clean and stable power flow when using Electric Vehicles as energy storage systems in the smart grid, PFC topologies such as the totem-pole and H-bridge PFC converters are commonly employed in Onboard Chargers (OBC). In such application, the PFC converter is directly connected to the grid. Therefore, it is essential to avoid any instability or irregularities that may arise during integration, making the use of PFC converters crucial for reliable and efficient operation.

To design and optimize these converters, comprehensive mathematical models are essential, which can accurately capture the converter's behavior under different operating conditions. The major technical contributions of this work are as follows: (a) An input current FFT Analysis based comprehensive mathematical modeling of Totem-pole PFC (TPFC) and H-Bridge PFC (HPFC) converters, (b) A thorough correlation of the mathematically reconstructed input current of the TPFC and HPFC converters with the simulation models and hardware experiment results, (c) Comparison of the THD modeling of the mathematically reconstructed input current waveform with the simulation and

experimental results. The results of this study will help researchers and engineers to design and optimize the PFC converters for various applications.

The technical aspects discussed in this chapter are derived from the studies included in [46,47].

2.2 Totem-pole PFC Converter Topology and Modes of Operation

Figure 2.1 depicts the schematic diagram of single phase TPFC which comprises four active switches. Out of those four active switches, switches S_1 and S_2 are operating at the switching frequency (100 kHz) and the other two switches, S_3 and S_4 are operating at the grid line frequency (60 Hz). When it comes to the comparison of conventional boost PFC and TPFC, the front-end diode bridge is minimized in TPFC. The didoes usually have high forward voltage drop compared to MOSFETS which also results higher conduction loss. So, with the minimization of the diode bridge itself, the conduction loss is also minimized with the arrangement shown in the Figure 2.1.

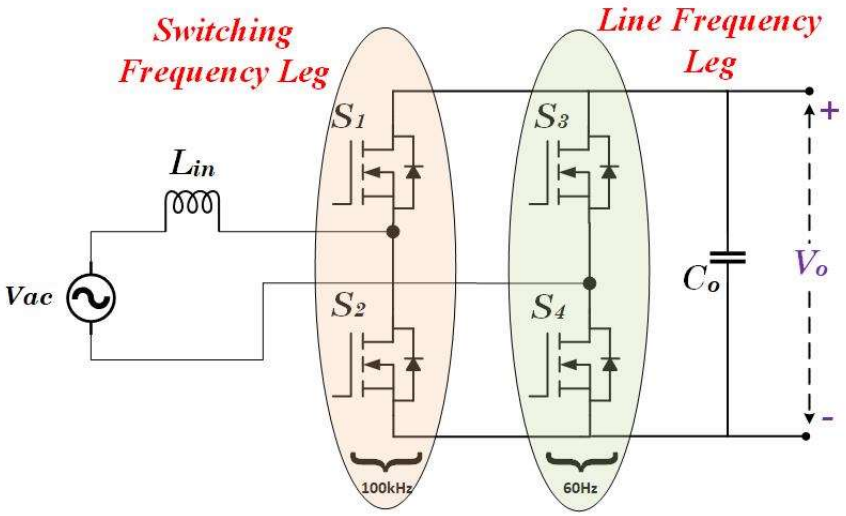

Figure 2.1: Single Phase Totem-pole PFC Converter

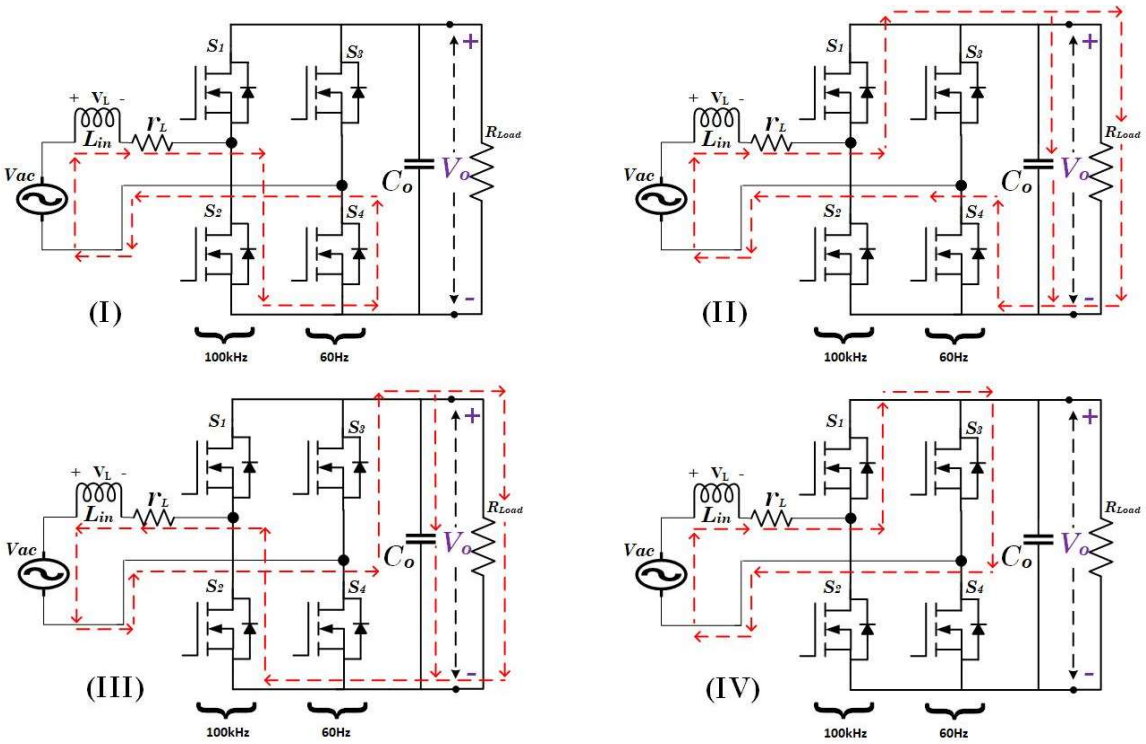

Figure 2.2 Modes of Operation of TPFC

Table 2.1: Totem-pole PFC Modes of Operation

Mode	**Input Voltage (V_{in})**	**S_1**	**S_2**	**S_3**	**S_4**	**Inductor Voltage (V_L)**
I	$V_{in} > 0$	OFF	ON	OFF	ON	$V_L(t) = V_{in}(t) - i(t) \cdot r_L$
II	$V_{in} > 0$	ON	OFF	OFF	ON	$V_L(t) = V_{in}(t) - i(t) \cdot r_L + V_o$
III	$V_{in} < 0$	OFF	ON	ON	OFF	$V_L(t) = V_{in}(t) - i(t) \cdot r_L + V_o$
IV	$V_{in} < 0$	ON	OFF	ON	OFF	$V_L(t) = V_{in}(t) - i(t) \cdot r_L$

In Figure 2.2, the modes of operation for TPFC are shown. As the switches S_3 and S_4 are controlled through the input voltage, switch S_4 conducts when $V_{in} > 0$ and switch S_3 conducts when $V_{in} < 0$. From the Figure 2.2 and the Table 2.1, the direction of the flow of current during different modes of operation can be observed. During Mode – I, the switches S_2 and S_4 are tuned on as input voltage is in its positive half cycle. As per the direction of flow of current shown in the Figure 2.2 for Mode – I, positive current $\big(i(t)\big)$ starts magnetizing the inductor which results in building a voltage across an inductor. The amount of this voltage depends on the instantaneous input AC voltage V_{in} and the voltage drop across the winding resistance $(i(t) \cdot r_L)$. Similarly for Mode – II, S_2 is turned off and S_1 is turned on keeping the S_4 in turned on condition, leading to the current flowing through the load as shown in Figure 2.2. This is when the instantaneous voltage across the inductor also comprises the output voltage component along with the voltage drop across its winding resistance of the inductor. Further, Mode – III and Mode – IV of operation comes when $V_{in} < 0$. That means for both Mode – III and Mode – IV of operation, switch S_3 remains tuned on. During Mode – III and Mode – IV, the switches S_1 and S_2 are triggered as described in Table 2.1.

From Figure 2.2 showing the modes of operation of TPFC and the switching states mentioned in Table 2.1, applying the volt-second balance across the input side inductor considering the unity power factor, the duty ratio $D(t)$ for the TPFC can be formulated as shown below.

$$D(t) = \begin{cases} 1 - \frac{V_{in}(t)}{Vo}, when\ V_{in} > 0 \\ \left|\frac{V_{in}(t)}{Vo}\right|, when\ V_{in} < 0 \end{cases} \tag{2.1}$$

Figure. 2.3 depicts the behavior of duty ratio $D(t)$ with respect to input voltage, $V_{in}(t)$. At the zero-crossing transition when the input voltage goes from its positive half cycle to its negative half cycle, there is sudden variation in the duty ratio can be observed from 0 to 1. This sudden transition of the duty ratio can cause an overlap in the switching transition which results in the zero-crossing distortion (ZCD) in the input current of Totem-pole PFC converter which is explained further in this chapter.

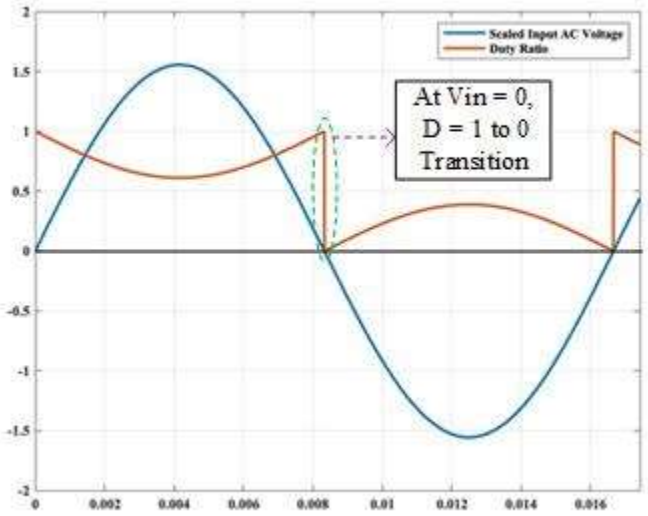

Figure 2.3: The Variation of Duty Cycle with Respect to Input Voltage in TPFC

2.3 H-Bridge PFC Converter Topology and Modes of Operation

The power circuit design of the H-Bridge PFC is identical to that of Totem-pole PFC converter. The operation of HPFC differs from TPFC as all the switches involved in the power circuit operate at switching frequency and no switch is controlled based on the instantaneous input voltage $V_{in}(t)$. Figure 2.4 presents the schematic diagram of H-Bridge PFC which comprises four active switches, out of which switches S_1 and S_4 turn on

simultaneously and same way, switches S_2 and S_3 turn on simultaneously as presented in Table 2.2, which means the bipolar PWM technique is used for HPFC converter.

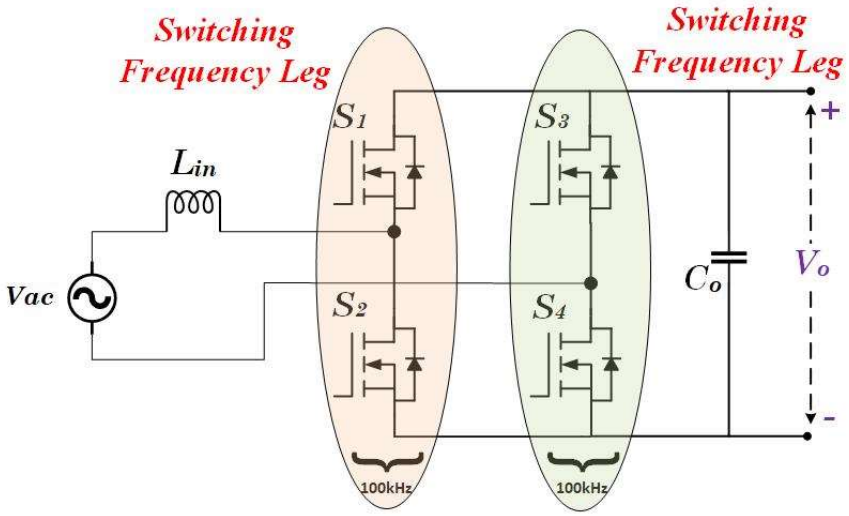

Figure 2.4: Single Phase H-Bridge PFC Converter

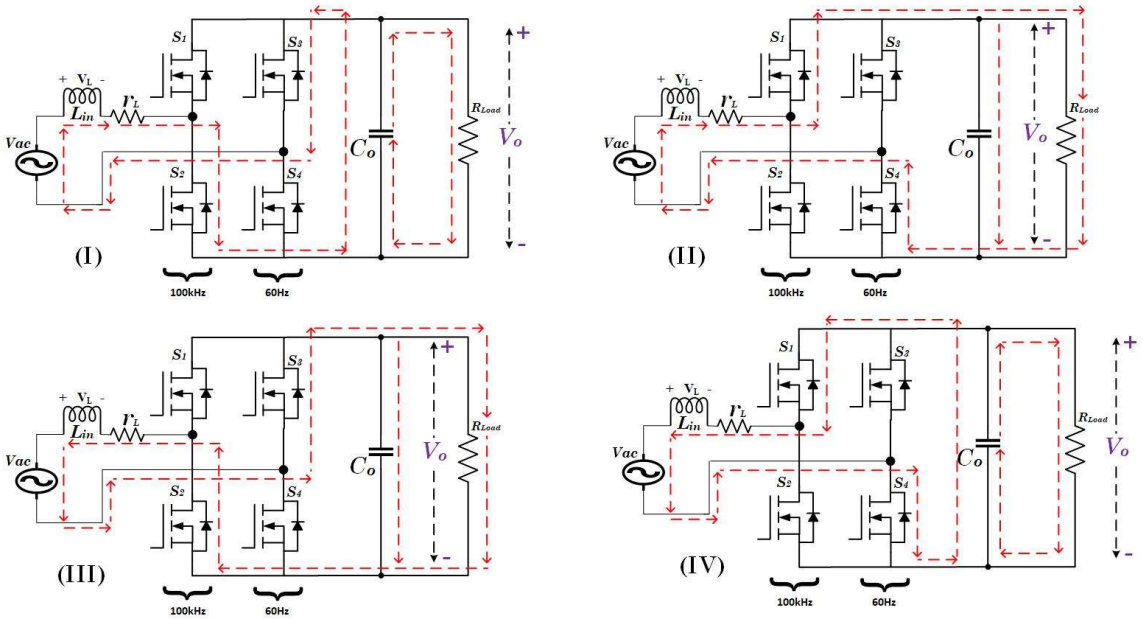

Figure 2.5: Modes of Operation of HPFC

Table 2.2: H-Bridge PFC Modes of Operation

Mode	Input Voltage (V_{in})	S_1	S_2	S_3	S_4	Inductor Voltage (V_L)
I	$V_{in} > 0$	OFF	ON	ON	OFF	$V_L(t) = V_{in}(t) - i(t) \cdot r_L - V_o$
II	$V_{in} > 0$	ON	OFF	OFF	ON	$V_L(t) = V_{in}(t) - i(t) \cdot r_L + V_o$
III	$V_{in} < 0$	OFF	ON	ON	OFF	$V_L(t) = V_{in}(t) - i(t) \cdot r_L + V_o$
IV	$V_{in} < 0$	ON	OFF	OFF	ON	$V_L(t) = V_{in}(t) - i(t) \cdot r_L - V_o$

Figure. 2.5 shows all the modes operations for H-bridge PFC based on the bipolar PWM technique which is used. As observed from Table 2.2 which shows the switching patterns in the operation of HPFC converter, the switching state of any of the four switches does not depend on the input voltage. When comparing this behavior of switches with that of TPFC converter, the output voltage is not a part of instantaneous inductor voltage for all the modes of operation in the case of TPFC converter. On the other hand, the output voltage is reflected in all the modes of operation for HPFC converter. During Mode – I and Mode – III switches S_2 and S_3 are turned on simultaneously. Therefore, the inductor current charging slope differs in both the PFC topologies. The input voltage is in its positive half cycle during Mode – I and it is in the negative half cycle during Mode – III which states the difference in the instantaneous inductor voltage for both the modes of operation. Similarly, during Mode – II and Mode – IV, switches S_1 and S_4 remain turned on and the instantaneous inductor voltage values differs for both the modes of operation because of the different input voltage polarities. The current flowing through the circuit during all the modes of operation can be analyzed from the Figure 2.5.

From these modes of operation mentioned in the Table 2.2 and the Figure 2.5, referring to the voltage-second balance across the inductor the duty ratio $D(t)$can be formulated as shown below.

$$D(t) = \frac{1}{2}\left(1 - \frac{V_{in}(t)}{Vo}\right) \tag{2.2}$$

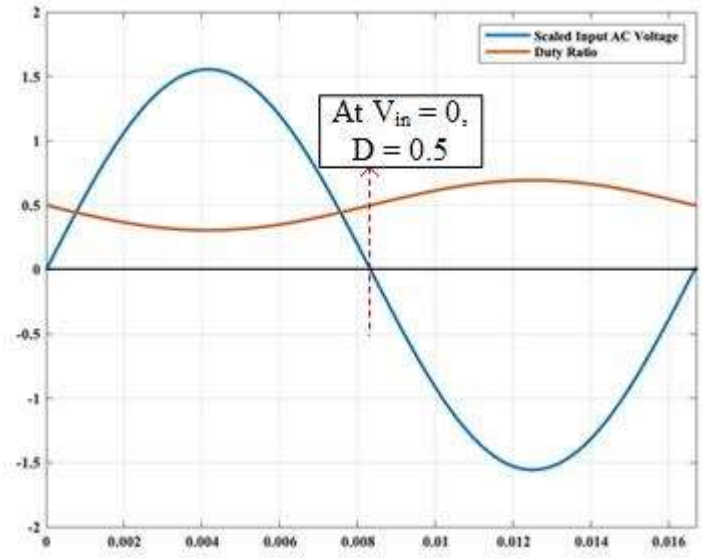

Figure 2.6: The Variation of Duty Cycle with Respect to Input Voltage in HPFC

Figure 2.6 shows the waveform of duty cycle $D(t)$ with respect to instantaneous input AC voltage $V_{in}(t)$. From Figure 2.6, it can be observed that the duty cycle is sinusoidal having the average of 0.5. When comparing the duty cycle of HPFC case with that of TPFC converter, it can be analyzed that there is not sudden transition of 0 to 1 or 1 to 0 is present. In any boost derived topologies, the maximum input current ripples occur at D = 0.5. In the case of HPFC converter, D = 0.5 occurs when the input AC voltage is transferring from positive half cycle to its negative half cycle. So, the maximum input current ripple appear at the zero-crossing in the case of HPFC converter as these are the boost derived converter topologies.

2.4 Mathematical Formulation of the Input Current Frequency Response for TPFC and HPFC Converters

This section presents the comparison between the mathematical modeling of the duty formation and the input side current FFT analysis from the simulation outcomes for the topologies under study.

2.4.1 Mathematical Modelling of the Duty Formation for TPFC and HPFC Converters

The input current can be expressed as the sum of the fundamental component and the switching frequency ripple components in any PFC topology. The equation for the input current can be written as,

$$I_{in,actual} = I_{pk}\sin(\omega_g t) + i_{in,ripple} \tag{2.3}$$

where, w_g=$2\pi f_g$ and f_g is the line frequency.

For TPFC, the equation of ripple component over a switching cycle can be expressed as,

$$i_{ripple,TP} = \begin{cases} \frac{V_{pk}\sin(wt)}{L}\cdot D\cdot T_s, & 0 < t < D\cdot T_s \\ \frac{V_o - V_{pk}\sin(wt)}{L}\cdot(1-D)\cdot T_s, & D\cdot T_s < t < T_s \end{cases} \tag{2.4}$$

Similarly, for HPFC, the equation of ripple component over a switching cycle based on the bipolar PWM technique can be formulated as,

$$i_{ripple,HB} = \begin{cases} \frac{V_O + V_{pk}\sin(wt)}{L}\cdot DT_s, & 0 < t < DT_s \\ \frac{V_o - V_{pk}\sin(wt)}{L}\cdot(1-D)T_s, & DT_s < t < T_s \end{cases} \tag{2.5}$$

where D and T_s are the duty cycle and a switching period, respectively.

The duty cycle is derived from the inner current loop controller function output, while the controller works to minimize the differential error between the measured current and current reference generated from the outer loop voltage compensator, which only consists of the fundamental component of the current.

The measured input current can be mathematically formulated as,

$$i_{in,actual} = \sum_{n=1,3,5,\ldots} a_n \sin(nw_g t) + b_n \cos(nw_g t) \tag{2.6}$$

As the duty cycle is derived from the controller, the most generalized equation for the duty cycle can be written as,

$$D(t) = K_p \left(I^* \sin(w_g \cdot t) - i_{in,actual}(t)\right) + K_i \int \left(I^* \sin(w_g \cdot t) - i_{in,actual}(t)\right) \tag{2.7}$$

where, K_p and K_i are the PI controller parameters and I^* is the transconductance reference generated from voltage loop compensator output.

Substituting the value of equation (2.6) in equation (2.7), we arrive at the following expression that establishes a relation between the duty cycle and the current loop controller coefficients, which is critical to complete the frequency response characterization of the input currents.

$$D = A_1 \sin(w_g t + \emptyset_g) + \sum_{n=1,3,5,\ldots} A_n \sin(nw_g t + \emptyset_s) \tag{2.8}$$

where, $A_1 = \sqrt{\left(K_p \cdot I^*\right)^2 + \left(\frac{(K_i \cdot I^*)}{w_g}\right)^2}$ (2.9)

$$\emptyset_g = \tan^{-1}\left(-\frac{K_i}{K_p \omega_g}\right) \tag{2.10}$$

$$A_n = \sqrt{\left(K_p a_n + \frac{K_i b_n}{w_s}\right)^2 + \left(K_p b_n + \frac{K_i a_n}{w_n}\right)^2} \tag{2.11}$$

$$\emptyset_s = \tan^{-1}\left(\frac{\left(K_p b_n + \frac{K_i a_n}{w_s}\right)}{\left(K_p a_n + \frac{K_i b_n}{w_s}\right)}\right) \tag{2.12}$$

2.4.2 Comparison of between the FFT-based mathematical model and simulation analysis for TPFC and HPFC converters

From the previously described mathematical formulations, the input current waveforms developed using MATLAB are shown in Figure 2.7 and Figure 2.8, which respectively refer to the TPFC and HPFC converters' input currents. The zoomed in portions highlighted in Figures 2.7 and 2.8 show the switching frequency ripple riding over a fundamental current waveform.

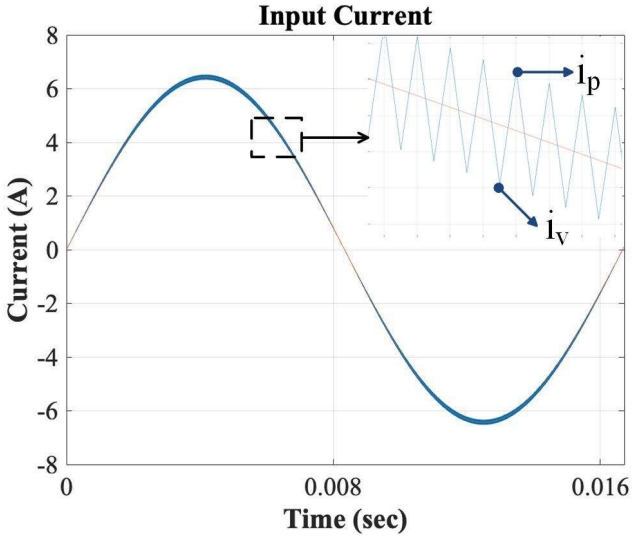

Figure 2.7: Mathematically Reconstructed Input Current Waveform for TPFC

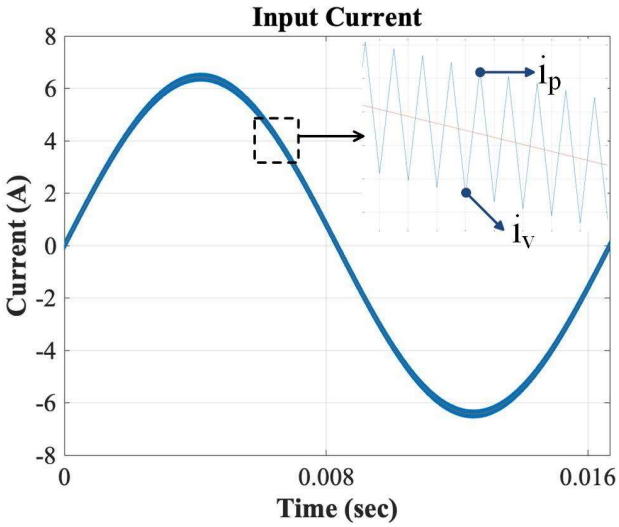

Figure 2.8: Mathematically Reconstructed Input Current Waveform for HPFC

In the switching ripples, the peak component is denoted by i_p and the valley component is be denoted by i_v. From Figures 2.7 and 2.8, it can be observed that the average of i_p and i_v is the instantaneous value of the fundamental component of the input current and its mathematical formulation is stated in equation (2.13).

$$i_v(t) + i_p(t) = 2 \cdot I_{pk} \sin(w_g t) \tag{2.13}$$

where, $I_{pk} = \frac{2P}{V_{pk}}$ and P is the Power.

The equations for the falling edge of the input current ripple are identical for both the converters topologies, which can then be verified through the equations (2.4) and (2.5). The falling segment of the input current ripple can be expressed in terms of i_p and i_v as follows.

$$i_v(t) - i_p(t) = \frac{V_o - V_{pk}\, sin(wt)}{L} \cdot (1 - D) \cdot T_s \tag{2.14}$$

Substituting the time-varying dynamics of D in the equation (2.14) and using equations (2.13) and (2.14), the values of i_p and i_v can also be calculated for any instant over a period of cycle.

Applying Fourier series on the mathematically reconstructed input current waveshape, the following can be formulated.

$$i_{in}(t) = \sum_{<n>}(a_n \sin(nw_g t) + b_n \cos(nw_g t)) \tag{2.15}$$

The values of the a_n and b_n can be determined from the following equations (2.16) and (2.17).

$$a_n = \frac{2}{T}\int_0^T i_{in}(t) \cdot cos(nw_g t)\, dt \tag{2.16}$$

$$b_n = \frac{2}{T}\int_0^T i_{in}(t) \cdot sin(nw_g t)\, dt \tag{2.17}$$

For TPFC converter, the Fourier series coefficients are expressed as follows.

$$a_n = \frac{2}{T}\sum_{n=0,1,2,\dots}\left[\int_{nT_s}^{nT_s+DT_s}\left(i_v + \frac{V_{in}}{L}t\right)\cdot cos(nw_g t)\ dt \quad + \right.$$
$$\left.\int_{nT_s+DT_s}^{(n+1)T_s}\left(i_p - \frac{V_o - V_{in}}{L}t\right)\cdot cos(nw_g t)\ dt\right] \tag{2.18}$$

$$b_n = \frac{2}{T}\sum_{n=0,1,2,\dots}\left[\int_{nT_s}^{nT_s+DT_s}\left(i_v + \frac{V_{in}}{L}t\right)\cdot sin(nw_g t)\ dt \quad + \right.$$
$$\left.\int_{nT_s+DT_s}^{(n+1)T_s}\left(i_p - \frac{V_o - V_{in}}{L}t\right)\cdot sin(nw_g t)\ dt\right] \tag{2.19}$$

Similarly, for HPFC converter, the Fourier series coefficients are expressed as follows.

$$a_n = \frac{2}{T}\sum_{n=0,1,2,\dots}\left[\int_{nT_s}^{nT_s+DT_s}\left(i_v + \frac{V_o + V_{in}}{L}t\right)\cdot cos(nw_g t)\ dt \quad + \right.$$
$$\left.\int_{nT_s+DT_s}^{(n+1)T_s}\left(i_p - \frac{V_o - V_{in}}{L}t\right)\cdot cos(nw_g t)\ dt\right] \tag{2.20}$$

$$b_n = \frac{2}{T}\sum_{n=0,1,2,\dots}\left[\int_{nT_s}^{nT_s+DT_s}\left(i_v + \frac{V_o + V_{in}}{L}t\right)\cdot sin(nw_g t)\ dt \quad + \right.$$
$$\left.\int_{nT_s+DT_s}^{(n+1)T_s}\left(i_p - \frac{V_o - V_{in}}{L}t\right)\cdot sin(nw_g t)\ dt\right] \tag{2.21}$$

The terms a_n and b_n are repeating over a cycle of every 60Hz. The current harmonic components at different frequencies can be determined using equation (2.22).

$$< i_{in} >_n = \sqrt{(a_n^2 + b_n^2)} \tag{2.22}$$

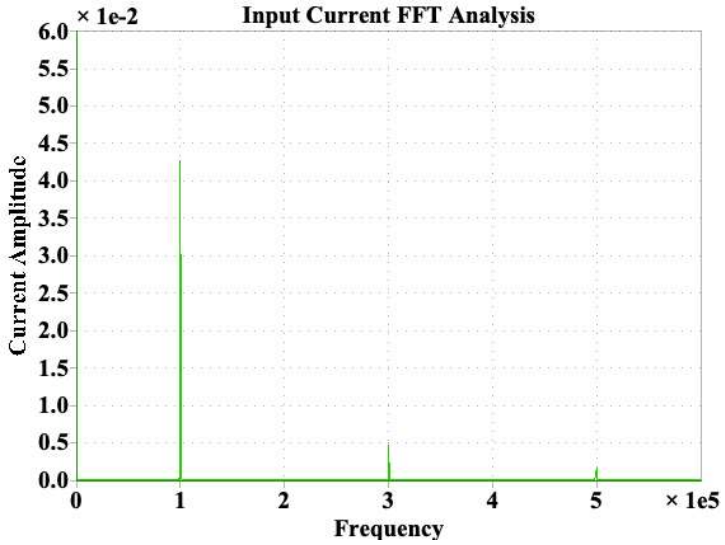

Figure 2.9: FFT Analysis of the Mathematically Reconstructed Input Current for TPFC

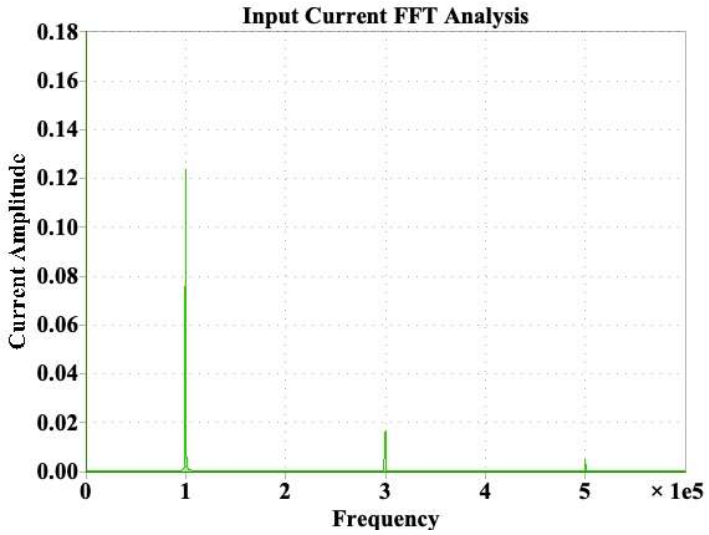

Figure 2.10: FFT Analysis of the Mathematically Reconstructed Input Current for HPFC

The FFT analyses of the mathematically reconstructed input current for TPFC and HPFC converters are presented in Figure 2.9 and Figure 2.10, respectively, which describe the harmonic components present in the input current at the switching frequency and at its odd multiples. Through this observation, it is evident that the magnitudes of the switching harmonic components are higher in HPFC compared to the TPFC despite having identical design parameters.

The simulation models of TPFC and HPFC are also developed. The bipolar PWM technique is used for HPFC converter simulation model. Figure 2.11 and Figure 2.12 refer to the input current waveforms obtained from the simulation models of TPFC and HPFC, respectively, which indicate a greater current ripple in the HPFC input current, primarily due to higher voltage applied across the boost inductor and hence a greater charging slope for HPFC $\left(of\ \frac{V_{in}+V_o}{L}\right)$ compared to the TPFC $\left(of\ \frac{V_{in}}{L}\right)$ case. As the bipolar PWM technique is used for the HPFC converter, the charging slope of the inductor current is higher. If the unipolar PWM technique was used for HPFC converter, the charging slop of the inductor current could be less compared to TPFC converter and it can results in lower harmonics present in HPFC input current. Furthermore, the zoomed in portion in Fig. 2.11 shows the presence of Zero Crossing Distortion (ZCD) in TPFC, while that is absent in HPFC candidate, primarily due to a continuous time-variant and sinusoidal profile of the duty cycle as opposed to the TPFC case with discontinuous duty cycle profile. The effect of ZCD reflects directly on the power factor deterioration, which also degrades the efficiency of the converter. However, the presence of larger switching harmonics in HPFC directly impacts the efficiency. Although the ZCD is absent in HPFC input current waveform, the zero crossing contains the switching components in relatively larger magnitude in comparison to the TPFC, primarily due to higher charging slopes of the inductor current, as evident from Figure 2.12.

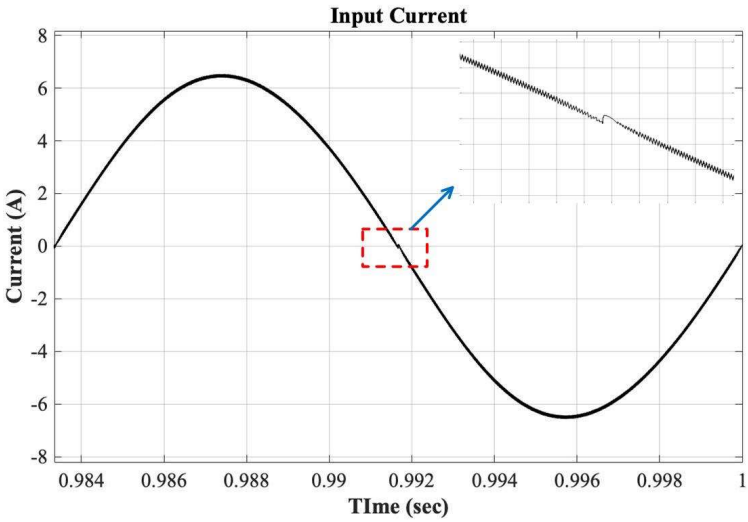

Figure 2.11: Input Current Waveform Developed through TPFC Simulations

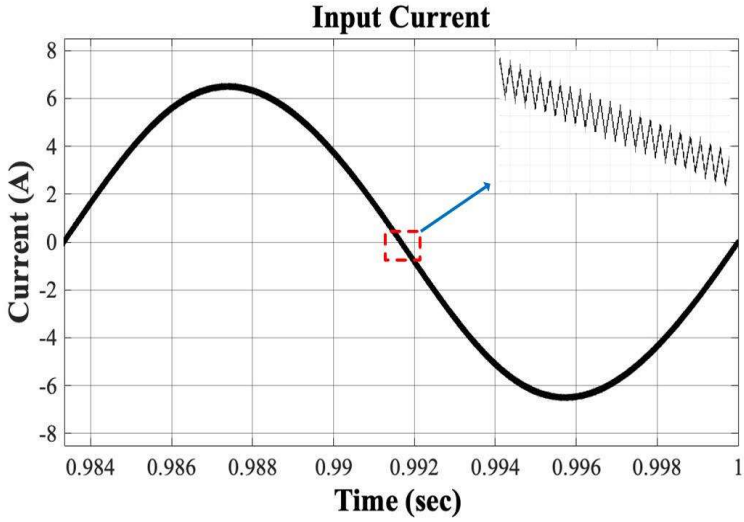

Figure 2.12: Input Current Waveform Developed through HPFC Simulations

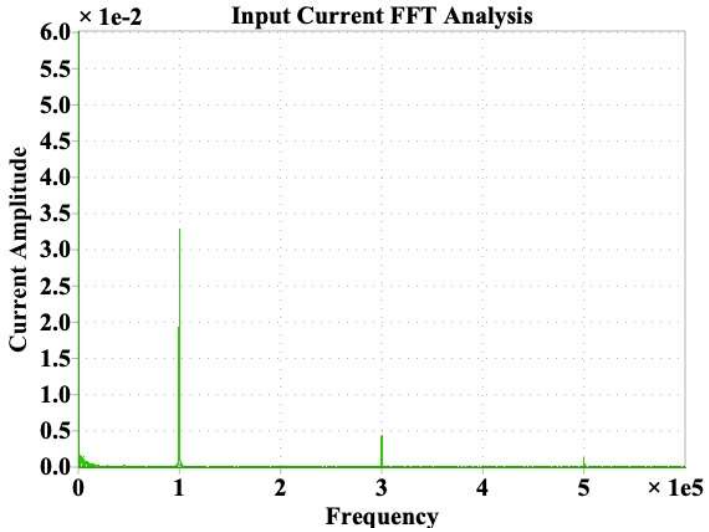

Figure 2.13: FFT Analysis of the Simulation-Based Input Current for TPFC

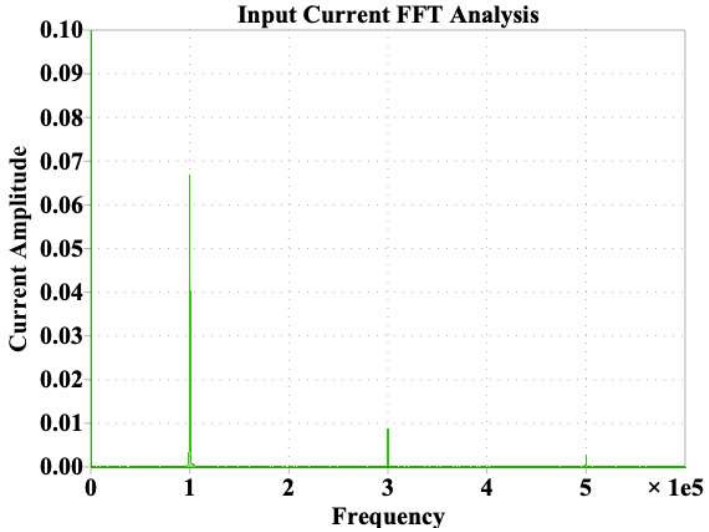

Figure 2.14: FFT Analysis of the Simulation-Based Input Current for HPFC

Further, the FFT analyses are performed on the simulation models of TPFC and HPFC (as shown in Figs. 2.13 and 2.41) for comparison against the mathematical model developed. The current amplitudes at the switching frequency and at its odd multiples obtained from the mathematically reconstructed waveshape follow a close agreement with the simulation results. The effect of these harmonic components on the THD is presented in the further sections of this study.

2.5 Formulation and Development of the Input Current THD Model

From the input current model developed in section 2.4, the Total Harmonic Distortion (THD) can be determined by computing the line frequency component of the input current and the integral multiples of the fundamental frequency component.

The harmonic components can be determined by performing FFT analysis for input current of the converter as shown in Figure 2.13 and Figure 2.14. The generalized expression to calculate the THD of the input current can be written as follows.

$$THD = \sqrt{\frac{\sum_{n=2,3,4,\ldots} {I_{in,n}}^2}{{I_{in,1}}^2}} \tag{2.23}$$

According to the FFT analysis performed in section 2.4, the harmonic components are higher for HPFC converter than that of TPFC converter corresponding to a specific output power, at which the fundamental current components for both the PFC topologies are equal. Based on this analysis, the input current in HPFC has average 1.45% higher THD compared to that of TPFC that can be observed from the values mentioned in Table 2.3.. The extensive comparison of the THD values of the input current obtained from the mathematical model, simulation model, and hardware experiments are presented in Table 2.3 for both the PFC topologies that indicate a close mutual agreement.

Table 2.3: The Compariosn of the Input Current THD for Mathematical Model, Simulation Model, and Hardware Experiment for TPFC and HPFC Converters

Power	**Model Type**	**PFC Converter Type**	**Input Voltage (V_{RMS})**	**Input Current (I_{RMS})**	**Power Factor**	**Output Voltage (V_{DC})**	**THD (%)**
500 W	Mathematical	Totem-pole	110 V	4.545 A	0.999	400 V	0.94 %
500 W	Mathematical	H-Bridge	110 V	4.545 A	0.999	400 V	2.39 %
500 W	Simulation	Totem-pole	110 V	4.545 A	0.989	400 V	1.47 %
500 W	Simulation	H-Bridge	110 V	4.545 A	0.999	400 V	2.86 %
500 W	Hardware Experiment	Totem-pole	110 V	4.896 A	0.983	400 V	1.91 %
500 W	Hardware Experiment	H-Bridge	110 V	4.546 A	0.999	400 V	3.47 %

2.6 Results and Observations

In this section, the experimental and the simulation results are presented and compared under the system parameters, mentioned in Table 2.4.

Table 2.4 Design Parameters of the TPFC and HPFC Simulation and Hardware Implementation

Parameters	Specifications
Input Voltage (V_{in})	110 V RMS, 1- Phase, 60 Hz
Rated Load (P_{out})	500W
Output Voltage (V_{out})	400V
Boost Inductor (L)	500µH
Output Capacitor (C)	1mF
Switching Frequency	100kHz
MOSFET	C3M0120065D

2.6.1 Steady State Simulation Results

Figures 2.15 and 2.16 depict the steady-state simulation waveforms for Totem-pole PFC and H-Bridge PFC converters, respectively, measured from MATLAB/Simulink under the same system parameters shown in Table 2.4.

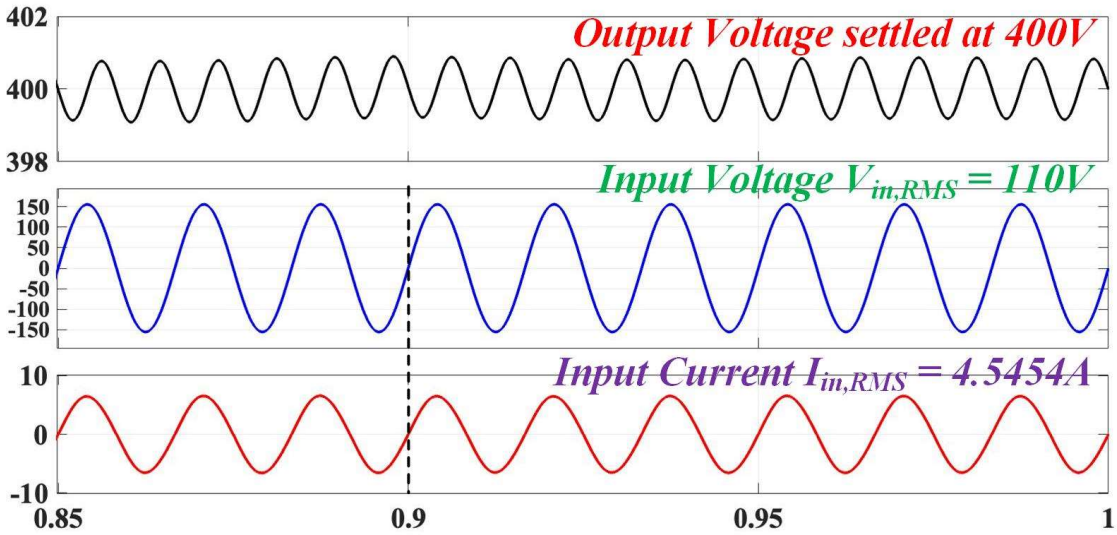

Figure 2.15: TPFC Simulation Results at Steady State: Waveforms of (i) Output Voltage (V_{out}), (ii) Input Voltage (V_{in}), and (iii) Input Current (I_{in}) at Rated Load of 500W

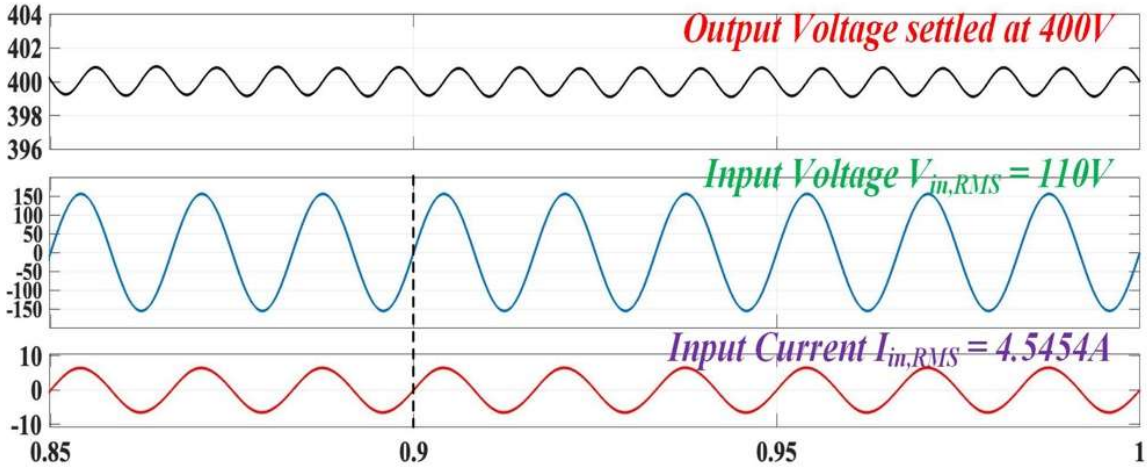

Figure 2.16: HPFC Simulation Results at Steady State: Waveforms of (i) Output Voltage (V_{out}), (ii) Input Voltage (V_{in}), and (iii) Input Current (I_{in}) at Rated Load of 500W

It is observed that the input current is precisely following the input voltage with near-zero phase angle difference for both the PFC topologies. The steady-state output voltage is regulated at constant 400 V with peak-to-peak ripples below ±5%.

2.6.2 Steady State Hardware Experiment Results

To verify the effective performance of both PFC converters, a proof-of-concept 500W converter is designed, fabricated, and experimented. For the control algorithm implementation, a single-core digital signal processor (TMS320F28335 from Texas Instruments) is used as the microcontroller. Both the converters are operated at a switching frequency of 100kHz. Figure 2.17 shows the Hardware prototype implementation and also the different components included in the hardware prototype are highlighted in the figure. The control system incorporated for the hardware experiment is composed of inner current loop converter and output voltage loop controller. The bipolar PWM technique is used for HPFC converter similar to mathematical and simulation model.

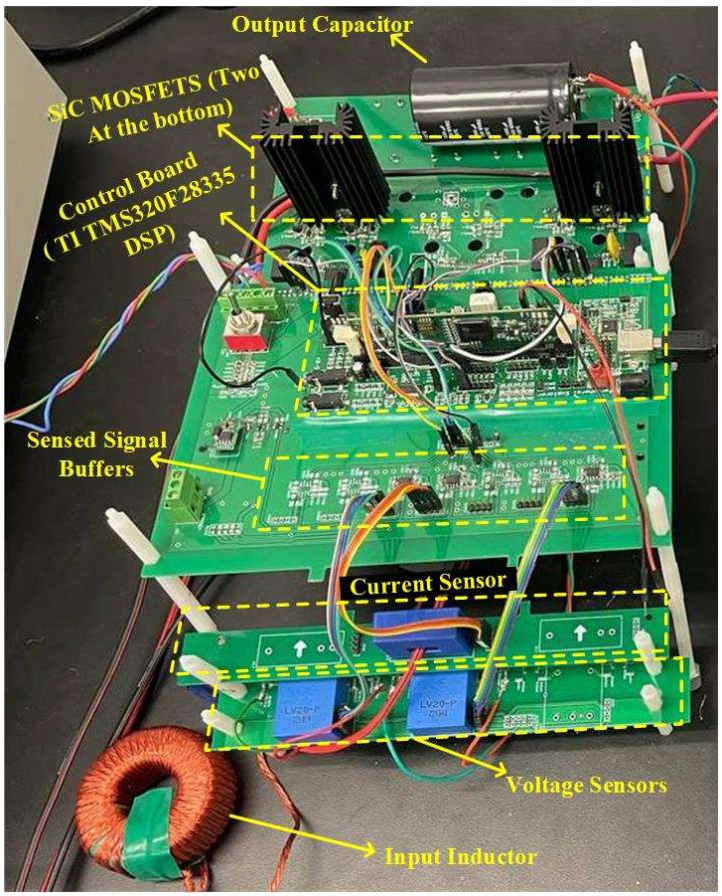

Figure 2.17: Hardware Implementation of PFC Converter

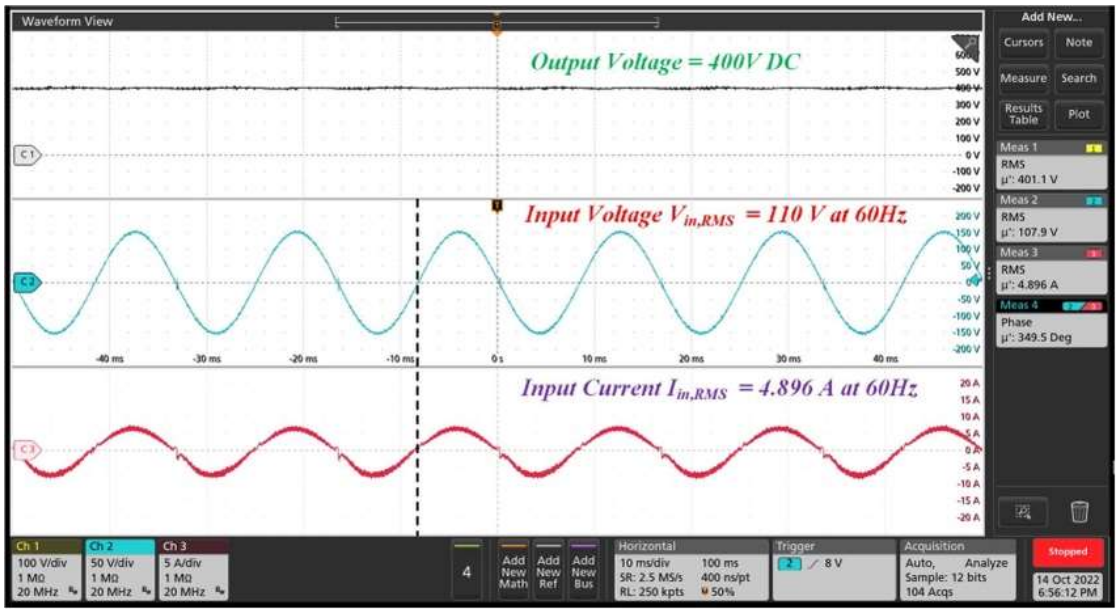

Figure 2.18: TPFC Experimental Results at Rated 500W Load Power: (i) Output Voltage (V_{out}) (ii) Input Voltage (V_{in}) and (iii) Input Current (I_{in})

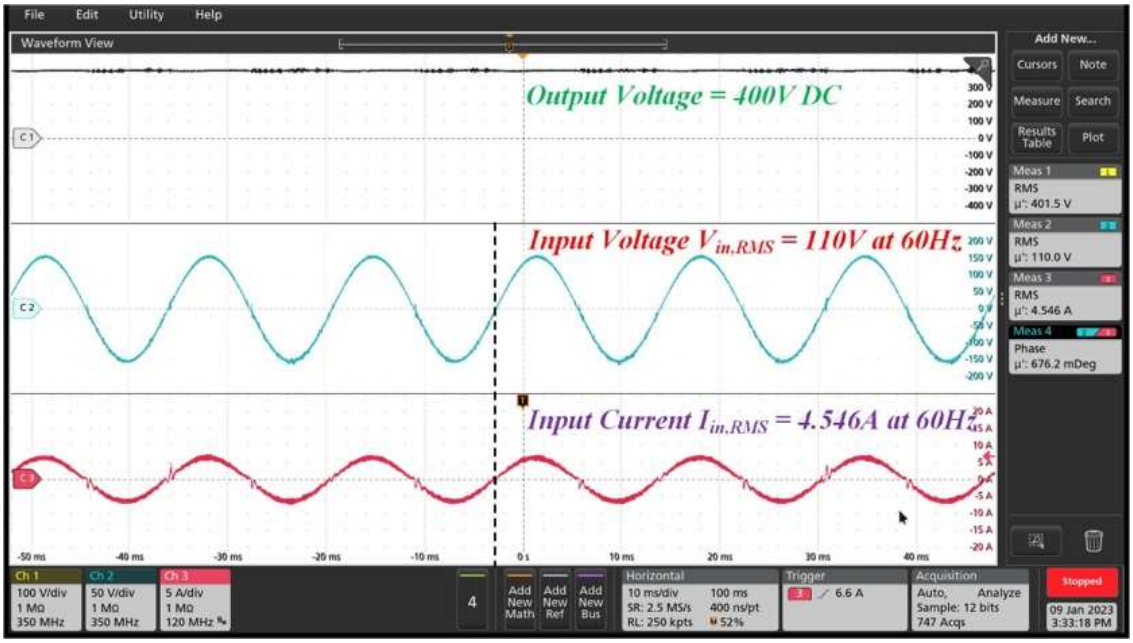

Figure 2.19: H-Bridge PFC Experimental Results at Rated 500W Load Power: (i) Output Voltage (V_{out}) (ii) Input Voltage (V_{in}) and (iii) Input Current (I_{in})

The steady state experimental results illustrated in Figure 2.17 and Figure 2.18 refer to the TPFC and HPFC, respectively. Besides of near-unity power factor and steady output voltage regulations, the observations include the absence of zero crossing distortion of the input current in H-bridge PFC converter that match with theoretical modeling. The TPFC power factor is measured to be 0.983, while the HPFC attains an improved power factor of 0.99, mainly due to the mitigation of zero crossing distortion.

2.7 Chapter Summary

The comprehensive mathematical model-based comparison of TPFC and HPFC can be summarized in different aspects.

i. Efficiency

Both the converters operate with high efficiency which is evident from the simulation and experimental results. Performing an experiment on the rated 500 W models

of both converters, the efficiency achieved for the TPFC is 98.45% and for HPFC converter is 97.86%, corresponding to a load resistance of 320Ω. As HPFC has a greater number of high-frequency switching devices compared to TPFC and results in higher switching loss, the higher switching losses badly affects the efficiency of HPFC converter.

ii Total Harmonic Distortion (THD)

In the HPFC, the switching ripples over the fundamental sine wave are approximately 80% higher than that of TPFC converter. As observed from the mathematical modeling of HPFC converter, the current ripple magnitude near the zero crossing is approximately 24% greater than the Totem-pole PFC converter primarily due to higher charging/discharging slope of the inductor current for a specific boost inductance value because of the bipolar PWM technique used for HPFC, which accounts for the higher THD in the HPFC input current. If the unipolar PWM technique was used then the harmonics present in HPFC input current could be less compared to TPFC converter.

CHAPTER 3

EMI MODELING AND OPTIMIZED DM EMI FILTER DESIGN METHODOLOGY

3.1 Introduction

EMI modeling is an essential process in the design of electronic systems to ensure reliable and safe operation. Electromagnetic interference (EMI) can cause malfunctions, noise, and other issues that can negatively impact system performance, leading to serious consequences [38]. Therefore, it is important to identify potential EMI sources during the design phase to mitigate or eliminate them.

EMI modeling involves creating a model of the power supply system, which can include the power source, power distribution network, and various electronic components such as voltage regulators, filters, and capacitors [39]. The model is then used to predict the electromagnetic emissions and susceptibility of the system to external sources of EMI.

The modeling process may involve a combination of analytical, numerical, and experimental techniques. Analytical techniques such as circuit analysis, electromagnetic theory, and statistical analysis can be used to develop mathematical models and simulations of the system. Numerical techniques such as finite element analysis (FEA) and computational electromagnetics (CEM) can be used to solve complex electromagnetic problems and predict the behavior of the system under different conditions [40-41].

Experimental techniques such as conducted and radiated emissions and susceptibility testing can also be used to validate the model and verify its accuracy [42]. The results of the modeling process can then be used to optimize the design of the system to reduce EMI and ensure reliable operation.

3.2 EMI Modeling and DM EMI Filter Design Methodology

Power factor correction (PFC) converters typically use switches that operate at high frequencies in the range of several hundred kilohertz to several megahertz [43]. These high-frequency switches can generate electromagnetic interference (EMI) noise due to their fast switching speed and high voltage and current transitions. The EMI noise generated by the PFC converter can interfere with other electronic devices and cause electromagnetic compatibility (EMC) issues [44]. This is particularly important in applications where sensitive electronic equipment is in close proximity to the PFC converter, such as in medical equipment, telecommunications, and other grid tied applications.

To mitigate the EMI noise generated by PFC converters, various techniques can be employed, such as using shielded cables, filtering components, and minimizing the parasitic capacitances and inductances in the converter circuitry. Additionally, careful design of the PCB layout and grounding scheme can also help to reduce the EMI emissions from the converter [45]. Out of all the EMI noise minimization techniques, implementing DM Emi filter is the most cost-effective technique. The EMI Filter Design methodology discussed in this chapter is derived from [46,47].

The unique DM EMI filter design methodology is extensively described in this study. The DM EMI filter, in this study, is designed from the EMI spectrum developed using the mathematically reconstructed input current waveform for TPFC and HPFC converters. The DM EMI filter having identical filter components that designed from the mathematically reconstructed model of TPFC and HPFC converters are implemented in the front end of the hardware prototypes of TPFC and HPFC which provides a close comparison of the behavior of EMI filter for both the analytical model and hardware

prototypes. This chapter describes the correlation of all the topics discussed in previous chapters with the EMI modeling and the DM EMI filter design for Totem-pole PFC and H-Bridge PFC converters. The detailed volumetric comparison of the EMI filter components requirement for TPFC and HPFC is also presented in this study.

Based on the TPFC and HPFC specifications with an input voltage of 110V and power rating of 500W, a comprehensive multi-constraint DM EMI filter design optimization process is performed. The design approach requires the EMI noise to comply with the FCC Class A EMI standard, subjected to EV charging requirements.

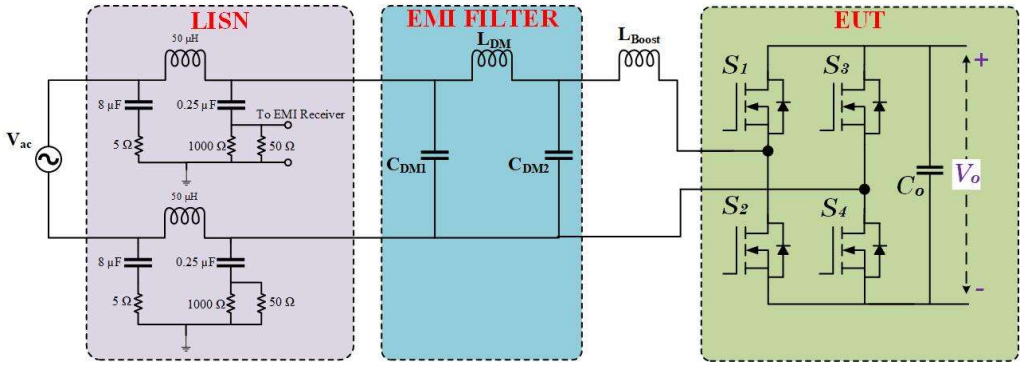

Figure 3.1: Implementation of DM EMI Filter and LISN Box at the Front End of PFC Converter

The topology of a DM EMI filter is illustrated in Figure 3.1 which consists of a DM inductor L_{DM} and DM capacitors C_{DM1} and C_{DM2}. In order to attenuate the noise originating from the high switching frequency devices of the converter and to meet the FCC class A EMI standard requirements, the filter network is placed between the AC source and the equipment under test (EUT). The Line Impedance Stabilization Network (LISN), which is connected between the AC source and EUT, is used for measuring DM EMI noise and the output of the LISN is connected to an EMI test receiver for measurement purposes across a 50Ω resistor. The LISN provides a band pass filter function to allow the high frequency noise current to flow through the RC network path. Moreover, it provides a blocking effect

to the noise generated from the AC source to ensure the EMI noise measurement is performed only from the converter side. The DM noise is composed of the multiple switching harmonics, contributed by input current ripple. From the input current frequency response analysis discussed in Chapter 2, the EMI noise measured at the LISN can be found from the following relation.

$$EMI_{noise}(dB\mu V) = 20\log\left(FFT(i_{in}(t) \cdot 50 \cdot 10^6\right) \tag{3.1}$$

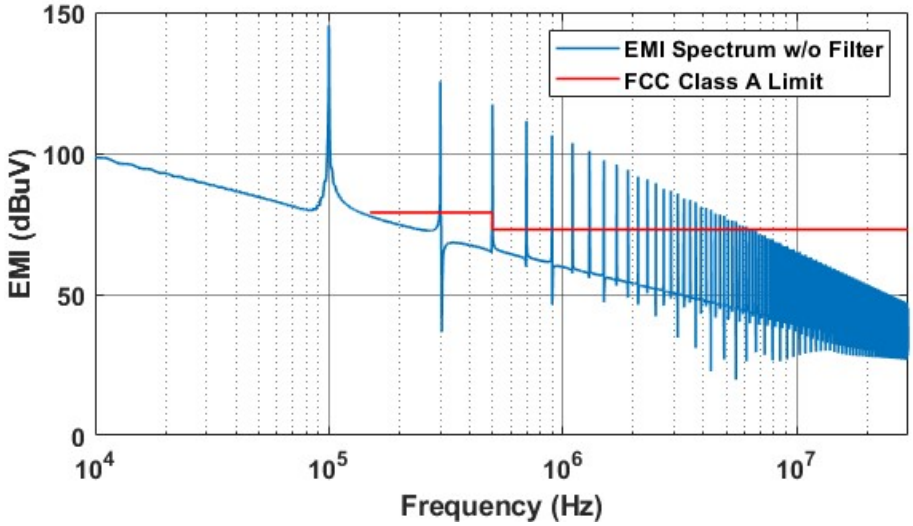

Figure 3.2: Analytical Model of the DM EMI Noise Spectrum without EMI Filter for TPFC

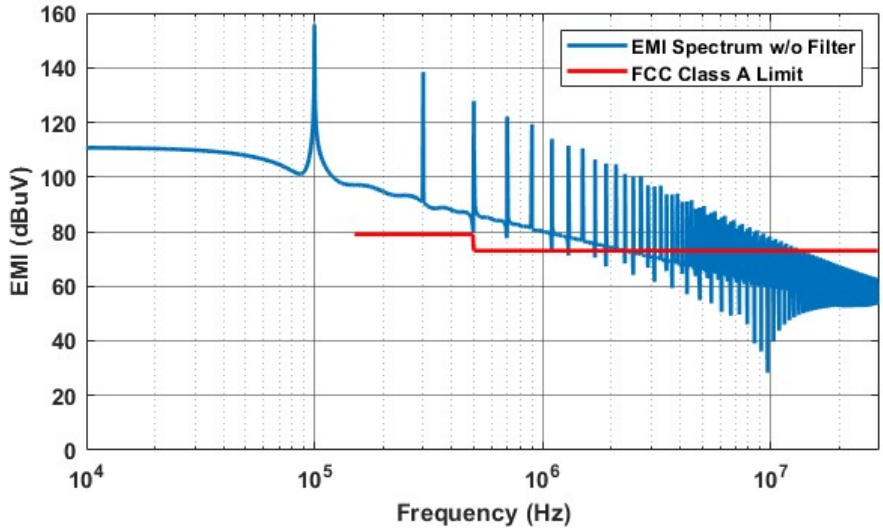

Figure 3.3: Analytical Model of the DM EMI Noise Spectrum with EMI Filter for HPFC

By performing Fourier analysis of the input current waveform, the DM EMI noise spectral characteristic is computed. Figure 3.2 and Figure 3.3 depict the analytically modeled EMI noise of the TPFC and HPFC input currents. It can be observed that the current peaks appear at the switching frequency of 100kHz and at its integral harmonics. One of the crucial steps in designing the DM EMI filter is the selection of design frequency and the attenuation requirement. To meet the required FCC Class A standard, each harmonic necessitates a unique level of attenuation. For selecting the design frequency of the EMI filter, the switching frequency harmonic that falls first within the FCC Class A standard, which starts from 150kHz is picked as the design frequency f_D. Hence, if the switching frequency is above 150kHz, the design frequency is same as the switching frequency. But if it is lower than 150kHz, the design frequency f_D can be expressed as,

$$f_D = ceil\left(\frac{150KHz}{f_s}\right) f_s \tag{3.2}$$

Where f_s is the switching frequency.

A higher switching frequency leads to a higher DM EMI noise emission and hence more stringent attenuation requirement. After determining the design frequency, the attenuation required is obtained by subtracting the EMI noise spectrum from the FCC class A EMI standard limit while keeping a safety margin of about 6dB for reliable EMI performance of the PFC converters.

Based on the attenuation requirement and design frequency, the two stage DM EMI filter is to be designed while dampening the high frequency noises and high-Q peaks in the spectrum that surpass the EMI standard limit. By keeping the attenuation requirement as a constraint, the modeling and volumetric optimization of DM EMI filter presented in [36] are used for determining the minimum LC product that is formulated as follows.

$$Att_{req}(f_D) = (2\pi f_D)^4 (L_{DM} C_{DM}\ L_{boost} C_{DM2}) \quad (3.3)$$

where, L_{boost}, L_{DM}, C_{DM1}, and C_{DM2} are the boost inductor, DM inductor, and DM capacitors, respectively.

3.3 Results and Observations after Implementation of EMI FIlter

3.3.1 Mathematical Model Based Results

To verify the effectiveness of the DM EMI filter design methodology, the comprehensive step-by-step procedure explained above is performed to select the appropriate DM filter inductor and capacitor. From the DM noise spectrum without EMI filter developed from the analytical model, the first noise peak that violates the FCC Class A standard limit by 50dB is found to be at 300kHz for TPFC candidate. Consequently, the DM filter inductors L_{boost}=500μH, L_D=100μH and DM capacitors C_{DM1}=C_{DM2}=10nF are utilized as the DM filter components that limit the DM EMI spectrum under the standard, as depicted in Figure 3.4.

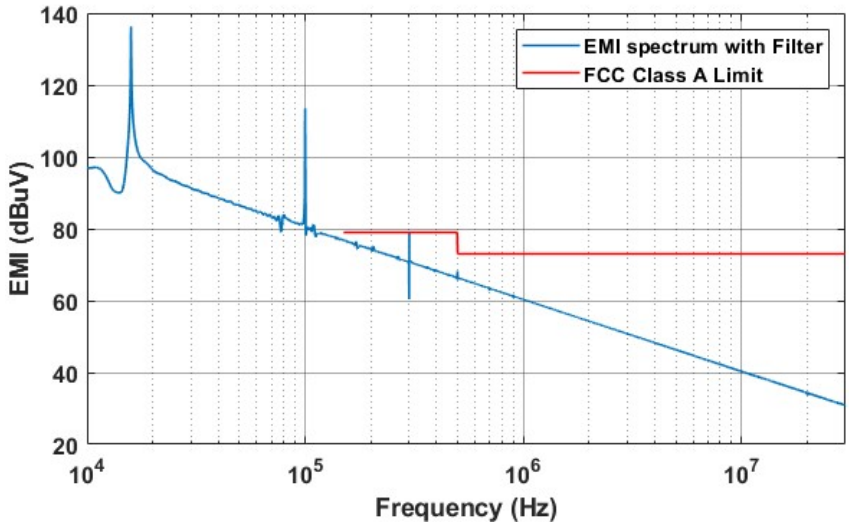

Figure 3.4: Analytical Model of the DM EMI Noise Spectrum with EMI Filter for TPFC

For performing a comparative evaluation of the DM EMI performance between the TPFC and HPFC converters, the same set of filter parameters as used for TPFC are employed in the HPFC filter network too.

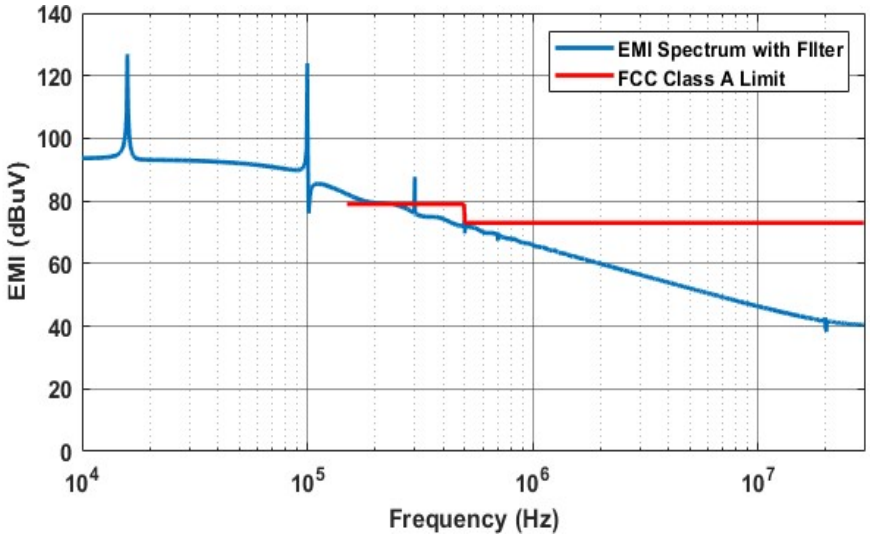

Figure 3.5: Analytical Model of the DM EMI Noise Spectrum with EMI Filter that Designed for TPFC Employed in HPFC

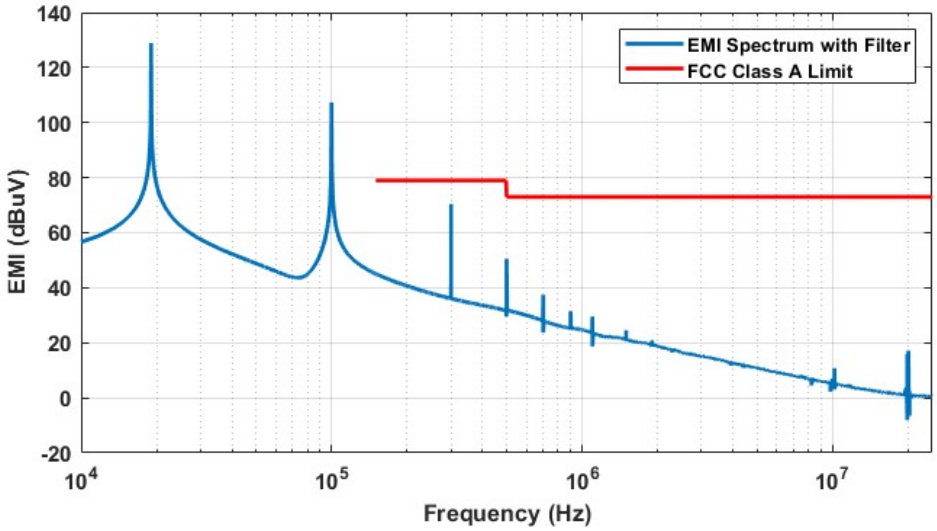

Figure 3.6: Analytical Model of the DM EMI Noise Spectrum with Extended EMI Filter for HPFC

From Figure 3.5, it can be observed that the EMI noise is suppressed below the limit only for frequencies that are greater than 300kHz. At 300kHz frequency, the EMI noise surpasses the standard EMI requirement by 11dBμV while for Totem-pole PFC, the designed EMI filter was performing in a way to comply the EMI noise within the standard requirement all throughout the conducted EMI range. Based on this analysis, in order to suppress the EMI noise peaks for HPFC, a filter inductor of 100μH and two DM capacitors of 15nF each are employed as depicted in Figure 3.6 to provide sufficient attenuation and ensure that the EMI spectrum remains lower than the standard limit, which, however, leads to 20% of increased volume of the EMI filter for HPFC. Further, the LC product is found to be 125% greater in the HPFC filter network design compared to the TPFC case.

3.3.2 Hardware Experiment Based Results

Further, the EMI spectrum of the input current from the hardware experiment is also presented. The EMI spectrum of the input current for TPFC without implementing the EMI filter at the front end is presented in Figure 3.7, which when compared with the FCC class A EMI standard shows that the input current spectrum surpasses the defined standard limit at certain frequencies. To suppress the EMI noise and to comply with the required standard, a DM EMI filter with the values of its elements obtained from the mathematical models developed earlier, is designed and implemented at the front end of the converter.

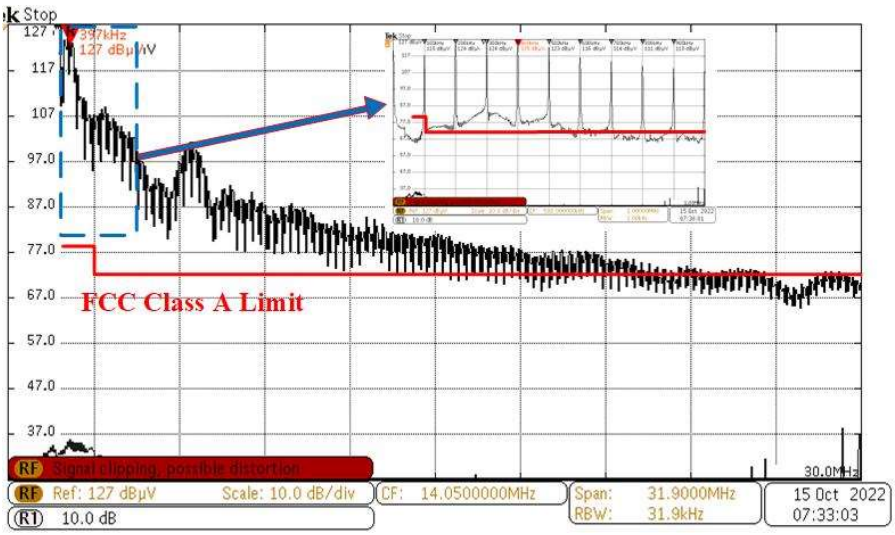

Figure 3.7: DM Noise EMI Spectrum without Implementing the EMI Filter at the Front End of TPFC

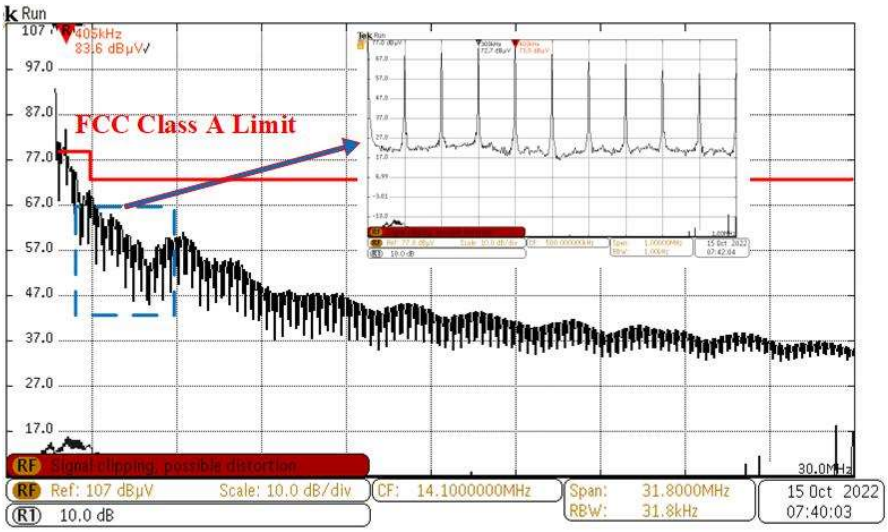

Figure 3.8: DM Noise EMI spectrum after implementation of the EMI filter at the front end of Totem-pole PFC

The filter parameters employed in the network for implementation are as follows: L_{DM}=100µH and C_{DM1}= C_{DM2}=10nF. Figure 3.8 illustrates an attenuation of the DM noise EMI spectrum by 50 dB at 300 kHz, which adheres to the FCC Class A standard throughout the frequency range of 150 kHz to 30 MHz. The zoomed-in portion shows the peaks of the input current switching harmonics up to 1 MHz, which stay well below the standard limit.

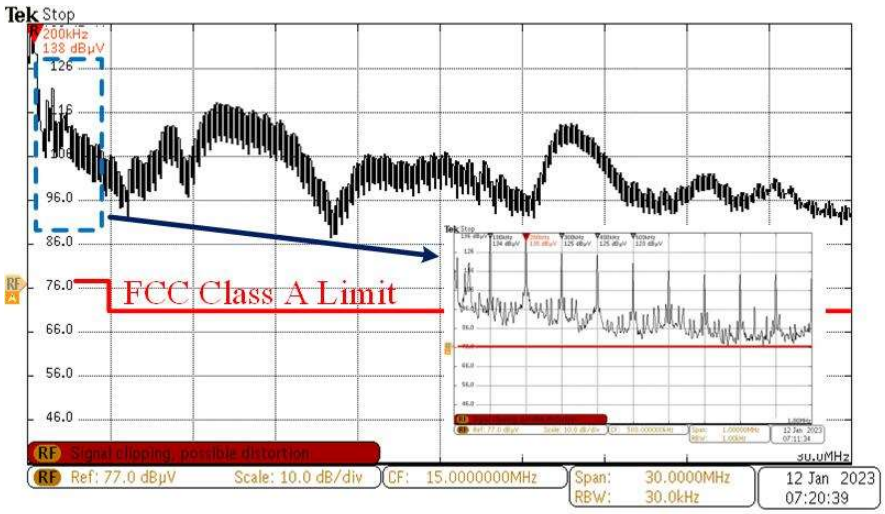

Figure 3.9: DM Noise EMI spectrum without implementing the EMI filter at the front end of the H-Bridge PFC converter

Similarly, the EMI spectrum of the input current for HPFC is shown in Figure 3.9 without the implementation of EMI filter at the front end of the converter. As discussed in section 3.2, the DM EMI noise emitted by HPFC converter is higher compared to TPFC and the corresponding EMI test performed on the hardware prototype confirms that the H-Bridge PFC requires 24 dB further attenuation at 200 kHz in comparison to the TPFC candidate.

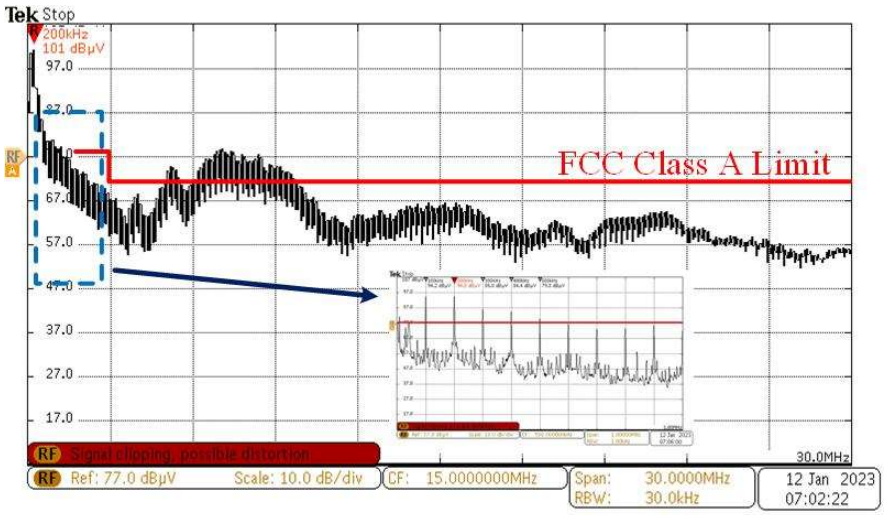

Figure 3.10 DM Noise EMI spectrum with implementing the EMI filter designed for TPFC at the front end of the HPFC converter

In the HPFC hardware prototype, the DM EMI filter designed for TPFC is first implemented specifically in order to investigate the suppression of DM EMI noise emission, as depicted in Figure 3.10. Although the EMI filter with TPFC suffices the criteria for noise emission, the HPFC necessitates further 24 dB suppression at 200kHz from the EMI filter.

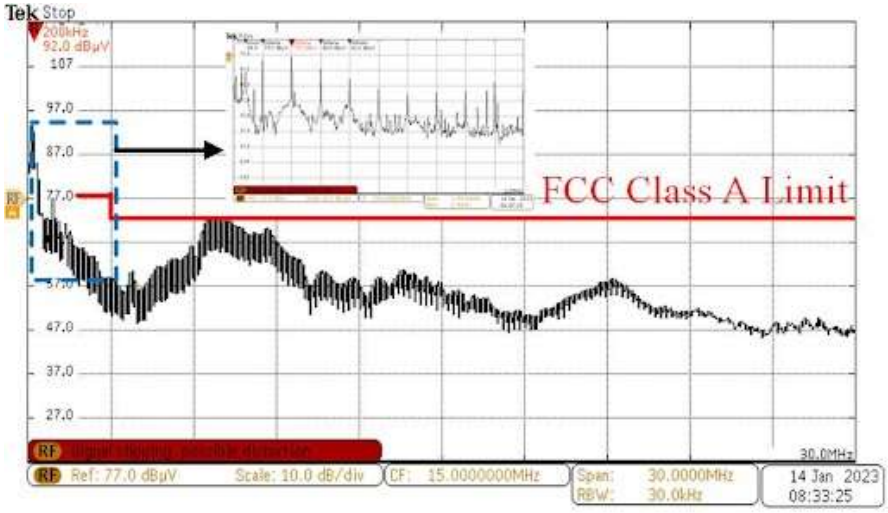

Figure 3.11 DM Noise EMI spectrum with implementing the extended EMI filter at the front end of the HPFC converter

Hence, a DM EMI filter for the HPFC is developed based on the design methodology discussed in section 3.3 above. A filter inductor of 100µH and filter capacitors C_{DM1} and C_{DM2} of 15nF are employed to implement the DM EMI filter having 125% higher LC product and 20% higher volume than that of the TPFC EMI filter. Figure 3.11 represents the input current EMI spectrum of the HPFC after employing the newly designed DM EMI filter. The compliance of the EMI spectrum with the FCC Class A standard limit validates the EMI filter design methodology to achieve the required attenuation for both the PFC converters.

3.4 Chapter Summary

Based on the input current FFT analysis of the TPFC and HPFC converters, the switching frequency components and their harmonics amplitudes for HPFC are higher compared to the same for TPFC leading to higher EMI noise emission from the switching circuit. When the EMI filter designed for TPFC is employed in HPFC, the converter fails to fulfill the attenuation requirement and an additional 11dBμV of attenuation is required at 300kHz frequency (from the section 3.2) to comply within the FCC Class A EMI standard requirements. For HPFC converter to achieve the required attenuation, the DM filter capacitor values are increased by 50% resulting in net 20% larger volume EMI filter as compared to the TPFC converter. Also, the LC product is also increased 125% compared to that designed for TPFC converter.

HAPTER 5

CONCLUSIONS

This study exclusively covers various chapters comparing the Totem-pole PFC and H-Bridge PFC converters including a concept of EMI modeling and design of DM EMI filter methodology for PFC topologies.

A detailed and accurate mathematical model of the input current characteristic is derived over a complete line cycle while taking the duty cycle variation into account. The bipolar PWM technique is used for H-Bridge PFC in this study which resulted in higher harmonic components present in HPFC input current. The input current THDs for both the PFC topologies are compared in analysis of mathematical model, simulation model, and hardware experiments which resulted in higher harmonics in the H-Bridge PFC input current.

To validate the performance of both the PFC topologies, a 500W hardware prototype is developed. The experimental results report an input power factor of 0.986 for TPFC and 0.989 for HPFC converter at the rated load condition. The achieved efficiencies at rated load of 500W operation for TPFC is 98.45% and for HPFC is 97.86%.

By utilizing the mathematical models of the input current frequency response, the EMI filters are designed for both the PFC converters. The EMI filter designed for HPFC converter is found to have 20% greater volume compared to that of the TPFC converter for ensuring the FCC class A standard compliance. Also, the EMI filter for HPFC converter has 125% higher LC product compared to that designed for TPFC.

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