A Low-Loss PWM Method to Improve the Efficiency and Dynamic Performance of Electric Vehicle Traction Inverters and Grid Connected Photovoltaic Converters

by

Haleema Qamar

A Dissertation Presented in Partial Fulfillment
of the Requirement for the Degree
Doctor of Philosophy

Approved April 2022 by the
Graduate Supervisory Committee:

Raja Ayyanar, Chair
Qin Lei
Hongbin Yu
Yang Weng

ARIZONA STATE UNIVERSITY

May 2022

ABSTRACT

Voltage Source Inverter (VSI) is an integral component that converts DC voltage to AC voltage suitable for driving the electric motor in Electric Vehicles/Hybrid Electric Vehicles (EVs/HEVs) and integration with electric grid in grid-connected photovoltaic (PV) converter. Performance of VSI is significantly impacted by the type of Pulse Width Modulation (PWM) method used.

In this work, a new PWM method called 240° Clamped Space Vector PWM (240CPWM) is studied extensively. 240CPWM method has the major advantages of clamping a phase to the positive or negative rail for 240° in a fundamental period, clamping of two phases simultaneously at any given instant, and use of only active states, completely eliminating the zero states. These characteristics lead to a significant reduction in switching losses of the inverter and lower DC link capacitor current stress as compared to Conventional Space Vector PWM. A unique six pulse dynamically varying DC link voltage is required for 240CPWM instead of constant DC link voltage to maintain sinusoidal output voltage. Voltage mode control of DC-DC stage with Smith predictor is developed for shaping the dynamic DC link voltage that meets the requirements for fast control.

Experimental results from a 10 kW hardware prototype with 10 kHz switching frequency validate the superior performance of 240CPWM in EV/HEV traction inverters focusing on loss reduction and DC link capacitor currents. Full load efficiency with the proposed 240CPWM for the DC-AC stage even with conventional Silicon devices exceeds 99%.

Performance of 240CPWM is evaluated in three phase grid-connected PV converter. It is verified experimentally that 240CPWM performs well under adverse grid conditions like sag/swell and unbalance in grid voltages, and under a wide range of power factor. Undesired low frequency harmonics in inverter currents are minimized

using the Harmonic Compensator that results in Total Harmonic Distortion (THD) of 3.5% with 240CPWM in compliance with grid interconnection standards. A new, combined performance index is proposed to compare the performance of different PWM schemes in terms of switching loss, THD, DC link current stress, Common Mode Voltage and leakage current. 240CPWM achieves the best value for this index among the PWM methods studied.

to my son, Mustafa

ACKNOWLEDGEMENTS

Throughout the course of this research I have received a great deal of support and assistance. First and foremost, I would like to express my gratitude to my advisor Dr. Raja Ayyanar whose expertise was invaluable in formulating the research questions and fostering a research environment that encouraged ideas. I am also extremely thankful to my committee members Dr. Hongbin Yu, Dr. Qin Lei, and Dr. Yang Weng for their valuable time and suggestions.

I would like to to express my sincere gratitude to my sister Hafsa Qamar who also happens to be my colleague at Power Electronics Laboratory for always supporting me during the highs and lows of life. I would like to thank my fellow Power Electronics students and scholars Nikhil Korada, Ankul Gupta, Madhura Sondharangalla and Arnab Acharya for the helpful discussions during the course of this research. I would like to thank Dr. Deliang Wu for his help and guidance in the hardware fabrication and initial testing.

I would like to express my deep thanks and gratitude to my father Dr. Qamar Mehboob who has always been a role model for me and encouraged me to pursue Ph.D. My sincere thanks to my husband Muhammad Shahrukh who has stood by me through each and every step and supported me to fulfill my dreams. I would like to especially thank my mother Saima Qamar who took care of my son Mustafa in the last year of my Ph.D. research.

Finally, I would like to acknowledge support by the Fulbright program.

TABLE OF CONTENTS

CHAPTER Page

CHAPTER Page

CHAPTER Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

Figure Page

Figure Page

Figure Page

Figure Page

Figure Page

Figure Page

Figure Page

Chapter 1

INTRODUCTION

Energy especially electricity is the backbone and driving force to meet the present level of civilization across the globe [1]. Factors like increase in population, weather conditions, growing economies, industrialization and urbanization are responsible for perpetual increase in energy demand worldwide [2], [3]. More than 70% of this energy demand is still met by fossil fuels that emit high levels of greenhouse gases [4]. On the other hand, renewable energy is clean, sustainable, and abundant. The power systems energy production sector (powered by fossil fuels) alone contributes to 75% of total carbon dioxide emissions in the world which leads to global warming [5], [6].That is why United Nations has set up Sustainable Development Goals to combat climate change that proposes the exploitation of renewable sources to meet the energy demand [7], [8]. The U.S. transportation sector alone takes up 30% of the total energy used in the country and it is responsible for 92% of petroleum based energy demand [9]. Such a huge reliance on petroleum-based fuels makes transportation sector the second highest carbon producing sector after power generation. Fig. 1.1 shows the greenhouse gas emissions in US by sector where electricity and transportation are the top two contributors [10]. The UN Framework Convention on Climate Change (UNFCC) urged to reduce the carbon dioxide emissions by at least 50% by 2050 [11]. To achieve such goals, reliance on renewable energy sources must increase instead of conventional fossil fuels.

Technologies that help to combat climate change and reduce carbon footprint without compromising the power quality are as follows:

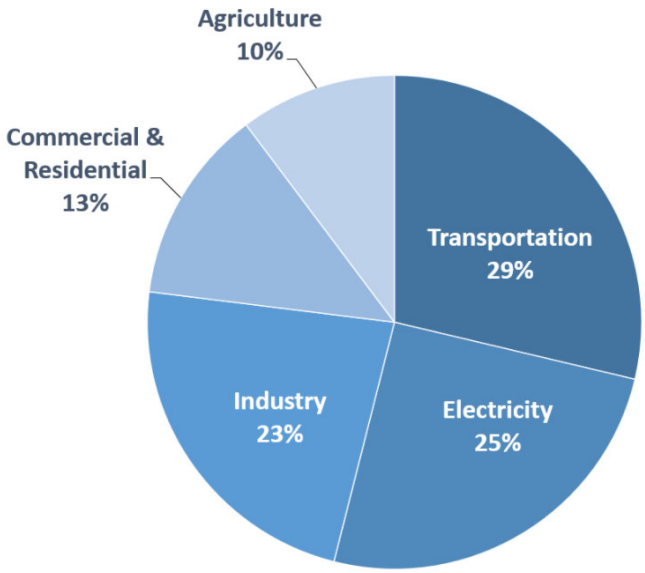

Figure 1.1: Overview of US Greenhouse Gas Emissions in 2019. Figure from [10].

1.1 Electric Vehicles (EVs) / Hybrid Electric Vehicles (HEVs)

Transportation sector is accountable for approximately a quarter of greenhouse gas (GHG) emissions globally [12]. Developed countries are promoting electrification in the transportation sector by introducing incentive based policies. More than 100 countries have deployed EVs/HEVs by the end of 2019 [13]. Despite having cost and infrastructure barriers, sales of EV/HEVs have skyrocketed over the past few years and the course seems clear for growth over the next decade [14]. Bloomberg's advanced transportation analysts predict that by 2040 EVs will contribute to 35% of the total global new car sales [15]. Fig. 1.2 shows the cumulative EV+HEV sales by market. Despite the enormous growth in sales of EVs over the past few years, they still account for only 1% of the global car stock in 2020 owing to user concerns and technical challenges [16]. EVs require low maintenance and cost of electricity required is much lower as compared to traditional combustion engine vehicles. Fig. 1.3 shows that cost saving per km is 75% using EVs as compared to gasoline based vehicle [16]. Even though EVs are gaining traction but their challenges remain. The technical

challenges of EVs compared to well established internal combustion engine vehicles include low power density, lack of charging stations, higher initial cost, degradation over time (related to batteries) and increased load on the grid (charging the electric vehicles) [17], [18].

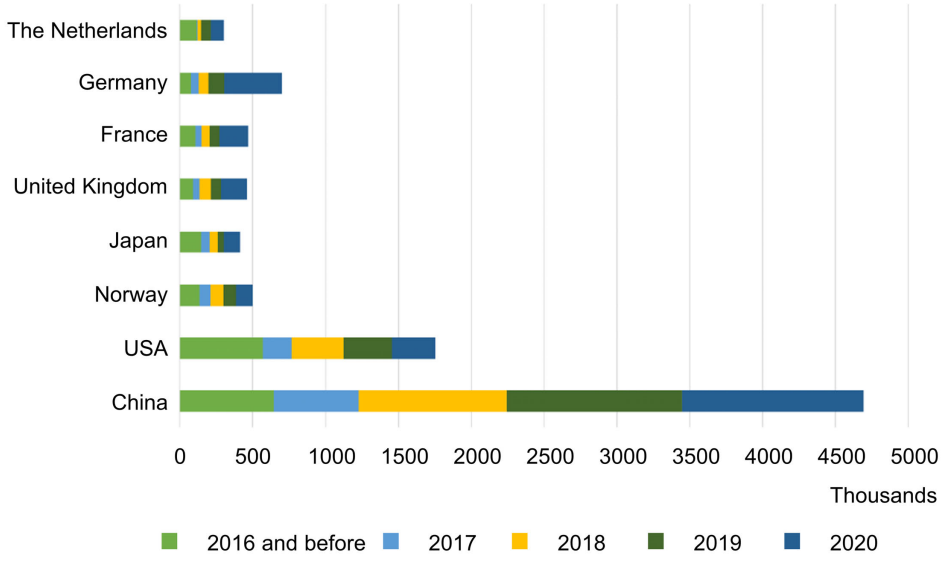

Figure 1.2: Evolution of the Number of Electric Vehicle Sales Worldwide. Figure from [16].

1.2 Photovoltaic Energy

To meet the Paris climate agreement targets, deep penetration of renewable energy sources into the electric grid is required. Fast and widespread deployment of solar PV alone can reduce carbon dioxide emissions by 4.9 gigatonnes in 2050 which represents 21% decrease in the total carbon dioxide emissions in the energy sector [19]. The International Energy Agency (IEA) targets to cut carbon dioxide emissions to less than half of 2011 levels by 2050 to combat climate change. Electricity demand is predicted to rise by 79% between 2011 and 2050. Wind, hydro and solar energy are

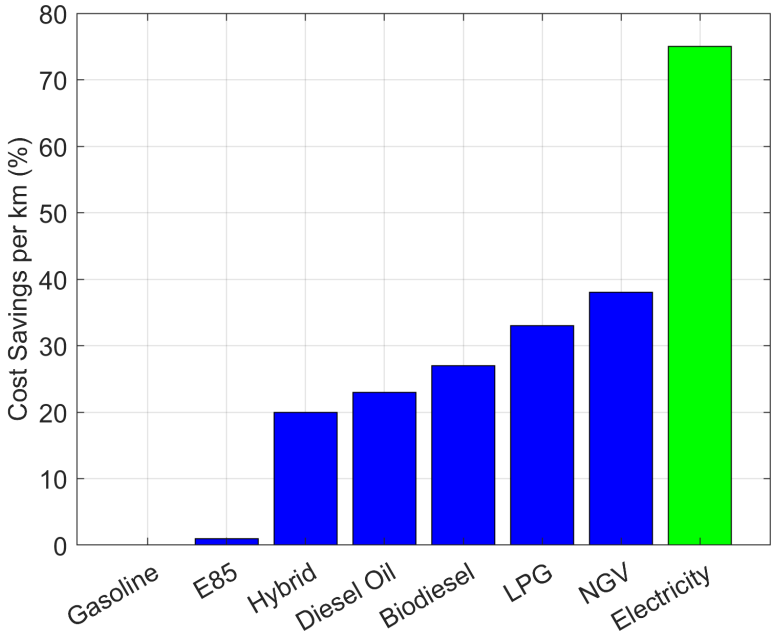

Figure 1.3: Comparison of Savings in Cost per Kilometer Offered by Vehicles Powered by Gasoline, Ethanol (E85), Hybrid, Diesel Oil, Biodiesel, Liquefied Petroleum Gas (LPG), Natural Gas Vehicle (NGV), and Electricity. Figure from [16].

predicted to supply 66% of global electricity generation in 2050, with photovoltaic alone contributing 27% [20]. Fig. 1.4 shows the annual global PV additions with historical data and future projections until 2050. It shows that PV additions were 94 GW in 2018 and they are predicted to rise to 270 GW in 2030 and 372 GW in 2050 [19]. Dramatic cost decline of solar PV in the past few decades is because of government policies supporting clean energy and research and development (R&D) in this area. Solar PV is expected to be the cheapest energy source by 2050 with costs ranging from \$0.014 to \$0.05 / kWh [21].

Continuous research and development in power electronics has transformed the transportation sector using EVs/HEVs and energy sector using solar PVs. To meet climate goals agreed in Paris, large scale deployment of EVs/HEVs and solar PV is the need of hour. To make this possible, high efficiency of system is a key requirement both in EV/HEV powertrain and solar PV. This research focuses on increasing the

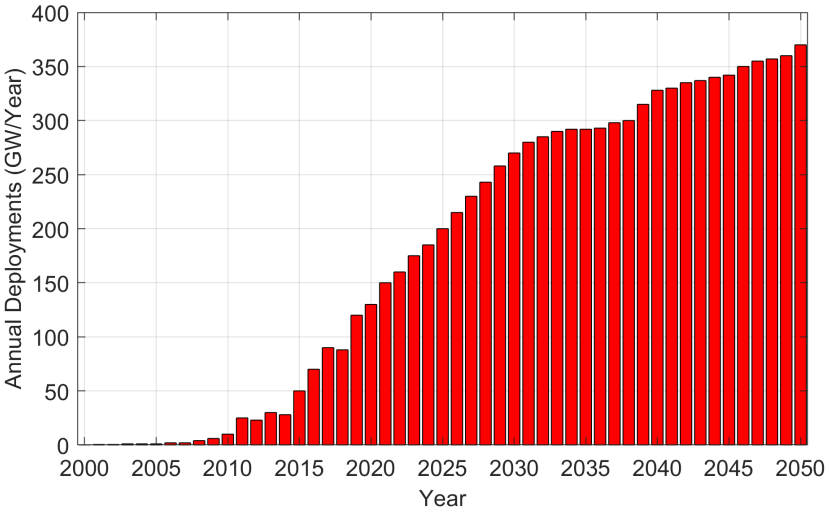

Figure 1.4: Trend of Annual Deployments of PV from 2000 to 2050. Figure from [19].

efficiency of EV/HEV powertrain and solar PV system by deploying a new Pulse Width Modulation (PWM) method in the inverter.

1.3 Challenges

Both in EV/HEV and solar PV application, one or more power electronic converters is used to interface battery with load/grid. A cascaded architecture of a DC-DC stage followed by a three-phase DC-AC stage is gaining acceptance in the traction inverters of many Hybrid Electric Vehicles and to a smaller extent in Electric vehicles shown in Fig. 1.5 [22]. However, in solar PV application (stand alone or grid connected), DC-DC converter is almost always used to perform maximum power point tracking (MPPT) [23].

To reduce the size of passive components, high switching frequency is targeted for most power electronic converters [24]. This helps to achieve high power density but there are certain challenges associated with it. Power loss in the switches increases due to high switching frequency which means compromising the efficiency. The challenges

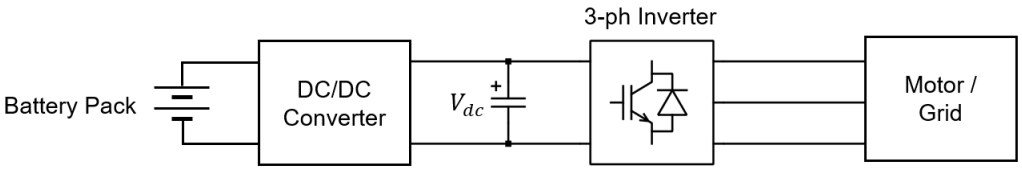

Figure 1.5: Power Conversion Stages in EV/HEV and Grid Connected Photovoltaic system.

associated to EVs/HEVs and solar PV application are listed below:

1.3.1 Efficiency

Efficiency of electric vehicle is primarily dictated by its power train. Extensive research is underway for the improvement of drive train performance and efficiency [25], [26]. Higher the drive train efficiency, lesser would be the thermal management issues and the required battery size. Thus, high power density structure which is one of the key requirements of EV drive train is made possible. EV drive train consists of battery, three phase inverter and electrical machine (Induction Machine or Permanent Magnet Synchronous Machine) and now DC/DC converter in between battery and inverter to provide variable DC-link at inverter input [27]. Fig. 1.6 below outlines power losses associated in EV drive train [27]. Power losses in electric drive system are up to 20% of the total power output lost in drives [28]. (Electric drive system constitutes inverter, motor, DC-DC converter). Even a little improvement in the efficiency of inverter would mean significant increase in the EV range and charge time [29].

In grid-connected PV converter, there are mostly no batteries, and grid replaces not just the motor but the entire mechanical energy. In grid-connected PV converter, power losses are usually associated with the wiring losses, DC-AC inverter and DC-DC converter losses. Another loss value comes into picture due to PV system availability

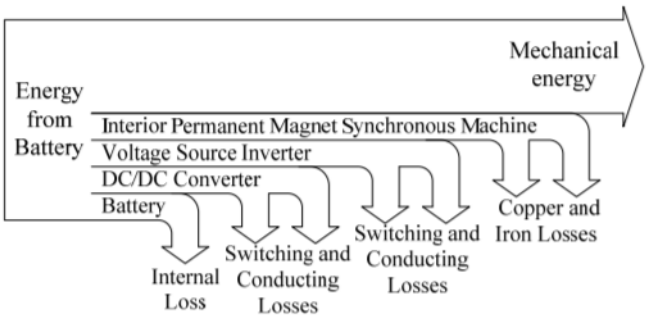

Figure 1.6: Power Losses in the Drivetrain. Figure from [27].

in such systems. It is meant to capture events that knock out the system entirely – including inverter shutdowns or failures, grid outages, or other actions that disconnect the PV system and prevent it from producing electricity [30].

1.3.2 Power Density

High power density is critical to EV/HEV design to meet the limited space and weight requirements [31], [32]. Power density targets of EV/HEV manufacturing companies are presented in [22]. These targets are always evolving due to research and development in power electronics. In 2012, US Department of Energy introduced a project called "EV Everywhere Grand Challenge" that aims to define technology roadmap for EVs that can replace internal combustion engine vehicles in future [33]. To meet the aggressive power density and vehicle drive range targets of technology roadmap, national laboratories and suppliers are working to improve power electronic systems at all levels. For example, 18% cost reduction and 87% volume reduction is targeted in 2025 goals as compared to 2020 [22]. Meeting such power density targets requires extensive research and technological breakthroughs. DC link capacitor is a crucial component because it plays a major role in dictating the power density of the EV/HEV powertrain. An optimum design of DC link capacitor is critical to achieving such goals.

Power density requirement of PV inverters is not as stringent as EV/HEV. Recently three phase string inverters have gained acceptance for utility applications. However, manufacturing cost per watt (MCPW) of string inverters is quite high. Largest commercial string inverters for low voltage grid have power rating of 40 kW to 60 kW that weigh around 60 kg to 70 kg. Increasing the power level of string inverters will help to bring down their MCPW but it will also increase their weight to such an extent that the installation and maintenance would not be very efficient [34].

1.3.3 Control System and Dynamic Performance

Seamless control is the heart of EV/HEV [35]. Control of EV/HEV is intricate because the operation parameters are always changing. For example, road conditions and traffic are highly variable. Therefore, the controller should be able to adopt to those changing conditions and provide good steady state and dynamic performance. With the advancement in computing technology such as digital signal processor (DSPs), it is possible to perform complex control to achieve optimal performance [36].

Similarly for PV application, control architecture is vital to the system performance, both in grid connected and stand-alone mode. Controls like maximum power point tracking (MPPT) is necessary in all kinds of PV inverters. Role of close loop control is even more important in grid connected PV applications where PV inverters are supposed to provide ancillary services to the grid like active and reactive power support [37].

1.3.4 Harmonic Content in Currents

Harmonic content in currents has adverse effect on EV motors which are listed as follows [34].

- Increased heating due to iron and copper losses at harmonic frequencies.
- Higher audible noise
- Harmonic currents in the rotor causing increased rotor heating and pulsating torque

In PV application, harmonic content in currents has different side effects, especially in grid connected mode. In grid connected mode, PV inverters need to meet very stringent requirements on harmonic content in current (dictated by total harmonic distortion THD) as per IEEE 1547 standard for interconnection of distributed energy resources with the grid [38].

1.3.5 Common Mode Behavior

High switching frequency is targeted for most power electronic converters which reduces the size of passive components and ensures motor operation with reasonably sinusoidal currents. High switching frequency poses other challenges like common mode voltage (CMV) and leakage currents both in EV and PV application. Leakage current causes problems in motor control due to erroneous operation of current operated circuit breakers and electromagnetic interference [39]. Leakage current may also induce shaft voltages that can damage the lubrication of motor bearings, causing the circulation of bearing currents. Bearing currents wear down the bearings causing them to fail [40].

In grid connected PV application, three phase two level transformerless voltage source inverters are commonly used. Due to lack of galvanic isolation in this topology, high frequency common mode voltage may induce undesirable leakage currents causing distortion in output currents and safety issues [41]. German safety standard VDE01261-1-1 requires the leakage current to be less than 300 mA [42].

1.4 Contributions

This thesis aims to address the challenges related to efficiency, power density and close loop control by introducing a new pulse width modulation (PWM) method that will be explained in detail in the next chapters both for EV/HEV and PV applications. New contributions of this thesis are as follows:

- Space vector based PWM method called 240° clamped PWM (240CPWM) is studied extensively for three phase voltage source inverters (VSIs) both for EV/HEV and PV applications.

- Switching loss characteristics of 240CPWM are thoroughly analyzed and compared with other PWM methods along with simulation and experimental validation.

- Detailed analysis of DC link capacitor sizing for 240CPWM is carried out and verified through simulations and experiments.

- Close loop control to shape dynamic DC link voltage is tested for 240CPWM and compared with different control strategies at maximum fundamental frequency of 300 Hz. Voltage control, current control, dual loop control and voltage control with Smith predictor are designed and experimentally verified for dynamic DC link voltage control of DC-DC stage.

- Performance of 240CPWM is compared with Advanced Bus Clamped PWM (ABCPWM) methods both with constant and variable DC link voltage control.

- Hardware results of the two-stage drive system at a power level of 10 kW with the highest DC link voltage of 800 V covering a range of fundamental frequency from 25 Hz to 150 Hz. Typical constant V/f mode of Variable Speed Drives with

constant load current is used to compare the characteristics of different PWM methods, where the fundamental voltage is proportional to the fundamental frequency.

- Performance of 240CPWM in PV inverters is also evaluated under adverse grid conditions i.e., unbalance and sag/swell in grid voltages. Harmonic Compensator (HC) is used along with PI control in grid side current control to minimize undesired low frequency harmonics in grid currents. With the designed controller, THD in grid currents is only 3.5% with 240CPWM in grid-connected mode which is in compliance with IEEE-1547 standard for interconnection of distributed energy resources with the grid [38].

- Finally, 240CPWM is applied to Transformerless Grid Connected PV Converters and its performance is compared with other PWM methods in terms of switching loss, THD, DC link current stress, CMV and leakage current. 240CPWM is selected as an ideal candidate for grid connected PV converters in terms of all round performance for each of the above metrics. A new, combined performance index is proposed to compare the performance of different PWM schemes, and it is shown that the 240CPWM achieves the best value for this index among the PWM methods studied.

1.5 List of Publications

- **H. Qamar**, H. Qamar, N. Korada and R. Ayyanar, "240-Clamped PWM Applied to Transformerless Grid Connected PV Converters with Reduced Common Mode Voltage and Superior Performance Metrics," in *IEEE Open Journal of Power Electronics*, doi: 10.1109/OJPEL.2022.3155053.

- H. Qamar, **H. Qamar** and R. Ayyanar, "Performance Analysis and Experimen-

tal Validation of 240°-Clamped Space Vector PWM to Minimize Common Mode Voltage and Leakage Current in EV/HEV Traction Drives," in *IEEE Transactions on Transportation Electrification*, vol. 8, no. 1, pp. 196-208, March 2022, doi: 10.1109/TTE.2021.3108957.

- D. Wu, H. Qamar, **H. Qamar** and R. Ayyanar, "Comprehensive Analysis and Experimental Validation of 240°-Clamped Space Vector PWM Technique Eliminating Zero States for EV Traction Inverters With Dynamic DC Link," in *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13295-13307, Dec. 2020, doi: 10.1109/TPEL.2020.2994599.

- **H. Qamar**, H. Qamar, N. Korada and R. Ayyanar, "Control and Performance of 240°-Clamped Space Vector PWM in Three Phase Grid-Connected Photovoltaic Converters under Adverse Grid Conditions," in *IEEE Transactions on Industry Applications* (Submitted).

- **H. Qamar**, H. Qamar, D. Wu and R. Ayyanar, "DC Link Capacitor Sizing for 240°-Clamped Space Vector PWM for EV Traction Inverters," 2021 *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 835-841, doi: 10.1109/APEC42165.2021.9487179.

- **H. Qamar**, H. Qamar and R. Ayyanar, "Performance Evaluation of Space Vector PWM Methods with DC Link Voltage Control for EV/HEV Powertrains," *IECON 2021 47th Annual Conference of the IEEE Industrial Electronics Society*, 2021, pp. 1-6, doi: 10.1109/IECON48115.2021.9589333.

- H. Qamar, **H. Qamar**, and R. Ayyanar, "240°-Clamped PWM in Three Phase Grid-Connected PV Converter Application," 2021 *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 340-346,

doi: 10.1109/ECCE47101.2021.9595349.

- **H. Qamar**, H. Qamar and R. Ayyanar, "Smith Predictor Control for Dynamically Varying DC Link Voltage with 240°-Clamped Space Vector PWM in Hybrid Electric Traction Drives," *2022 IEEE Transportation Electrification Conference & Expo (ITEC)*, 2022 (Accepted).

1.6 Chapter Overview

Chapter 2 discusses the space vector pulse width modulation approach. Switching sequences of well known PWM methods are discussed. Chapter 3 outlines the proposed 240° clamped PWM (240CPWM) method. It also discusses the cascaded architecture of DC-DC stage followed by three phase inverter for hybrid/electric vehicle powertrains. Switching loss characteristics of 240CPWM are thoroughly analyzed and experimentally verified. DC link capacitor sizing for 240CPWM is thoroughly analyzed in Chapter 4. Simulation and experimental results are presented to verify the analysis. Chapter 5 discusses the close loop control for dynamically varying DC link voltage required for 240CPWM. In chapter 6, performance of 240CPWM in PV inverters is evaluated under adverse grid conditions i.e., unbalance and sag/swell in grid voltages. Harmonic Compensator (HC) is used along with PI control in grid side current control to minimize undesired low frequency harmonics in grid currents. In chapter 7, performance of 240CPWM in transformerless grid-connected PV converter is studied and compared with other PWM methods in terms of switching loss, THD, DC link current stress, CMV and leakage current. 240CPWM is selected as an ideal candidate for grid connected PV converters in terms of all round performance for each of the above metrics.

Chapter 2

SPACE VECTOR APPROACH TO PWM

2.1 Introduction

Voltage source inverter (VSI) is a building block of power stage both in EV/HEV and PV application. Therefore, it is imperative to achieve highly efficient operations of VSI. Three phase VSI is realized using three single pole double throw switches. These switches can be realized using semi-conductor elements like Insulated Gate Bipolar Transistors (IGBTs), Metal Oxide Semiconductor Field Effect Transistor (MOSFET) or Bipolar Junction Transistors (BJT). The power switches need to be robust and capable of handling faults long enough until the activation of protection scheme. The switches undergo high switching stresses since inverters are typically hard switched. The switching loss in switch-mode operation is linearly dependent on switching frequency. IGBTs have become the preferred technology in such applications because of their robustness and ability to pass greater current than equivalent die size MOSFET. Also, IGBTs tend to have lower conduction losses than MOSFETs since IGBT's loss is dependent on collector current while MOSFET's loss is a function of drain current squared [43]. An undesirable trait of IGBTs is the tail current that stems from the stored charge in internal PNP transistor. Significant research in this area has led to the development of IGBTs with tail times as small as 300ns at around 20kHz. The desired switching frequency is 20kHz due to audible hearing range of human beings [44]. Another important component is the free-wheeling diode that is co-packaged with the IGBT. Free-wheeling diode is placed parallel to the IGBT to conduct reverse currents.

These semiconductor devices in the inverter need to be switched appropriately to obtain desired output voltage. The three phase voltages should be shifted by 120° with respect to each other at fundamental frequency. Simplest means to achieve switching in inverter is via square wave modulation but it results in low order harmonics resulting in torque pulsations and high copper loss. To overcome these issues, pulse width modulation (PWM) was introduced [45]. Various PWM methods have been introduced ever since to achieve several performance objectives [46], [47]. Modulation method used in the inverter dictates DC bus utilization, total harmonic distortion in line currents, inverter efficiency, common mode voltage and leakage currents [48], [49]. Fig. 2.1 shows a typical three phase two level VSI which is connected to motor in EV/HEV and to three phase grid via filter in PV application.

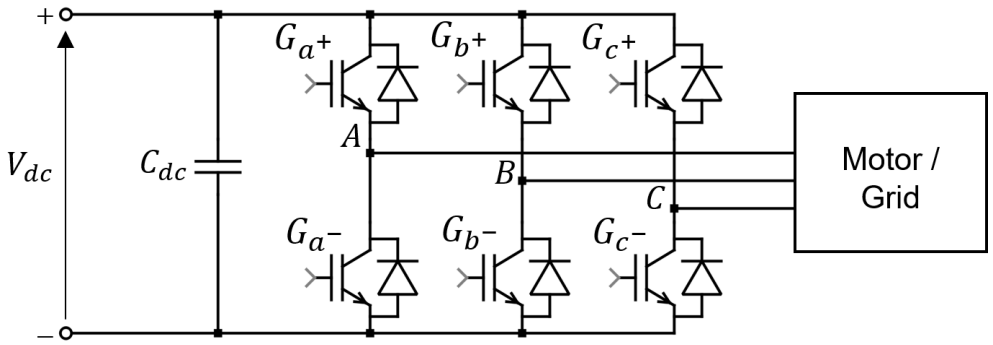

Figure 2.1: Three Phase Two Level Voltage Source Inverter.

2.2 Space Vector Pulse Width Modulation

Space Vector PWM (SVPWM) is the preferred PWM method for VSI inverters due to its benefits over Sine SPWM (SPWM) in terms of higher DC bus utilization, less distortion in line currents and flexibility in the choice of switching sequences, allowing a variety of design trade-offs [50], [51] . With the evolution of advanced DSP controllers, space vector implementation has become an industry standard.

A two-level, three-phase VSI has eight switching states as shown in Fig. 2.2. The zero or null states, 0 (– – –) and 7 (+ + +) produce voltage vectors of zero magnitude. The remaining six states (1 (+ – –), 2 (+ + –), 3 (– + –), 4 (– + +), 5 (– – +), 6 (+ – +)) produce non-zero output voltages resulting in power transfer between the DC bus and motor/grid. So, these states are called active states. The space vector plane is divided into six sectors by the six active vectors. The sectors are designated as I, II, III, IV, V and VI as shown in Fig. 2.2. Table 2.1 shows the switch state and line to line voltage corresponding to applied vectors.

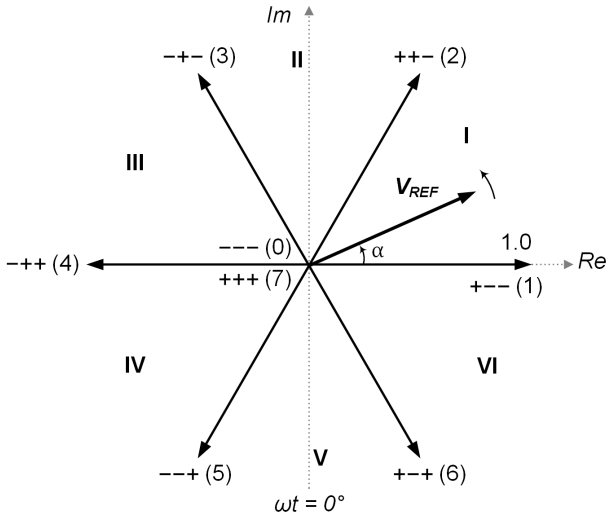

Figure 2.2: Voltage Vectors Produced by Two Level VSI.

The reference voltage vector V_{REF} is sampled once in every sub-cycle T_s. Conventionally, for V_{REF} having angle α in Sector I, the active vectors 1, 2 and zero vectors are applied for durations T_1, T_2 and T_z respectively.

$$T_1 = \frac{V_{REF}}{V_{dc}} \frac{\sin(60^\circ - \alpha)}{\sin 60^\circ} T_s \tag{2.1}$$

$$T_2 = \frac{V_{REF}}{V_{dc}} \frac{\sin \alpha}{\sin 60^\circ} T_s \tag{2.2}$$

Table 2.1: Switching States and Line to Line Voltages Corresponding to Eight Switching States

Vector	Ga^+	Gb^+	Gc^+	Ga^-	Gb^-	Gc^-	V_{AB}	V_{BC}	V_{CA}
000	OFF	OFF	OFF	ON	ON	ON	0	0	0
100	ON	OFF	OFF	OFF	ON	ON	$+V_{dc}$	0	$-V_{dc}$
110	ON	ON	OFF	OFF	OFF	ON	0	$+V_{dc}$	$-V_{dc}$
010	OFF	ON	OFF	ON	OFF	ON	$-V_{dc}$	$+V_{dc}$	0
011	OFF	ON	ON	ON	OFF	OFF	$-V_{dc}$	0	$+V_{dc}$
001	OFF	OFF	ON	ON	ON	OFF	0	$-V_{dc}$	$+V_{dc}$
101	ON	OFF	ON	OFF	ON	OFF	$+V_{dc}$	$-V_{dc}$	0
111	ON	ON	ON	OFF	OFF	OFF	0	0	0

where V_{REF} is defined as $V_{REF} = \sqrt{3}V_{LL,pk}/2$, V_{dc} is the DC link voltage and $V_{LL,pk}$ is the peak value of the reference line-to-line voltage. The angle α is defined as $\alpha = [(\omega t - 90°) \bmod 60°]$, where $\omega = 2\pi f_1$ is the angular fundamental frequency. Time duration of zero vector is given as follows:

$$T_z = 1 - T_1 - T_2 \tag{2.3}$$

2.3 Triangle Comparison Based PWM Generation

In triangle comparison method of PWM generation, three modulating signals at fundamental frequency that are 120° apart are compared against a common high frequency triangular carrier. For sine-triangle PWM (SPWM), the three modulating

signals are given by:

$$v_a(t) = V_m sin(\omega t) \tag{2.4a}$$

$$v_b(t) = V_m sin(\omega t - 2\pi/3) \tag{2.4b}$$

$$v_c(t) = V_m sin(\omega t + 2\pi/3) \tag{2.4c}$$

Where V_m is the peak value of modulating signal and ω is the angular fundamental frequency. Modulating signal for SPWM along with the triangular carrier is shown in Fig. 2.3.

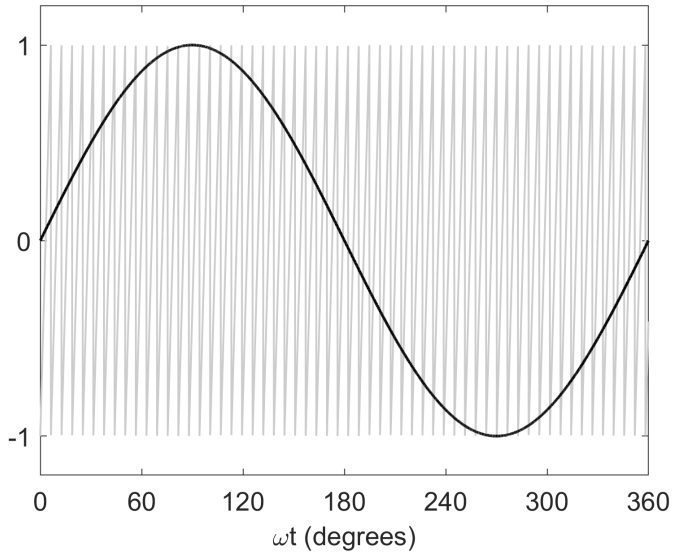

Figure 2.3: Modulating Signal of SPWM (Black) and Triangular Carrier Signal (Grey).

For other PWM methods, the modulating signal can be obtained by adding a zero-sequence signal to three phase sinusoidal signals given in (2.4). One of the most widely used PWM methods is Conventional Space Vector PWM (CSVPWM) which gives 15% higher DC bus utilization and better THD performance as compared to SPWM. The modulating signal and zero-sequence signal for CSVPWM is shown in Fig. 2.4.

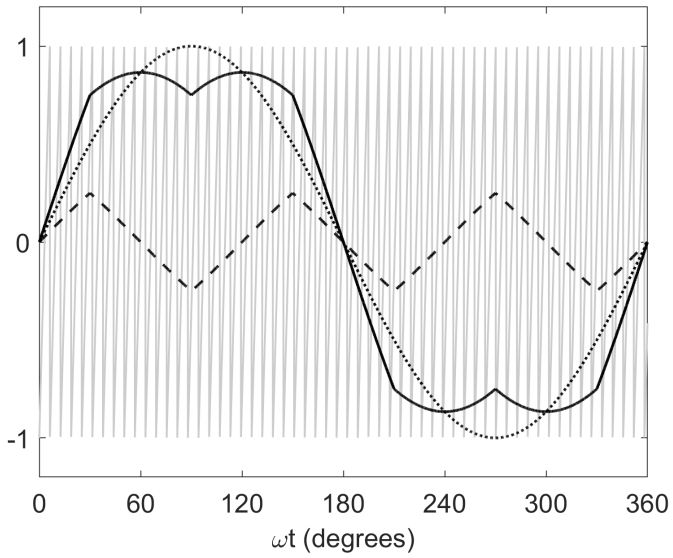

Figure 2.4: Modulating Signal of CSVPWM (Solid Black), Zero Sequence Signal (Dashed Black), Triangular Carrier Signal (Grey), and Sinusoidal Signal (Dotted Black).

In Discontinuous PWM (DPWM) methods, modulation wave of a phase has at least one segment which is clamped to positive or negative DC bus for 120° i.e., it discontinues modulation which results in saving in switching loss at the expense of THD in most cases [47]. Duration and region of clamping depends on the required performance parameters. Modulating signals of various discontinuous PWM methods and their corresponding zero-sequence signals are shown in Fig. 2.5.

2.4 Switching Sequences

Many switching sequences that maintain volt-second balance to produce a given sample in an average sense are possible but they are limited by the following constraints [52].

- Total number of switchings in a sub-cycle should not exceed three which is the number of switchings when CSVPWM is applied.
- Only one phase must switch while transitioning from one state to another. For

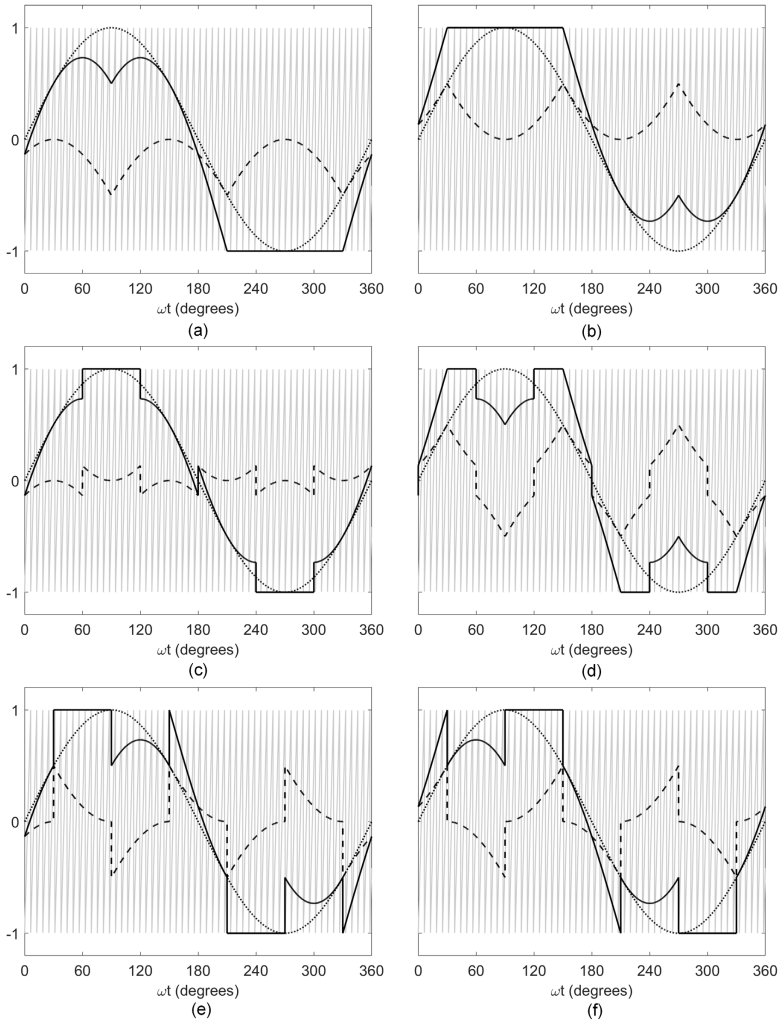

Figure 2.5: Modulating Signal of DPWM (solid black), Zero Sequence Signal (Dashed Black), Triangular Carrier Signal (Grey), and Sinusoidal Signal (Dotted Black). (a) DPWMMIN, (b) DPWMMAX, (c) DPWM1, (d) DPWM3, (e) DPWM0 and (f) DPWM2.

example, transition from state 0 (- - -) to 1 (+ - -) is allowed because only one phase is switching i.e., phase a but transition from state 0 (- - -) to 2 (+ + -) is not allowed because it leads to switching of two phases i.e., phase a and b.

Fig. 2.6 shows the possible switching sequences in Sector I meeting these constraints; 0127-7210, 012-210, 721-127, 0121-1210, 7212-2127, 1012-2101 and 2721-1272. In this figure, T_s shows the sub-cycle duration which is half of the switching

cycle duration T_{sw}.

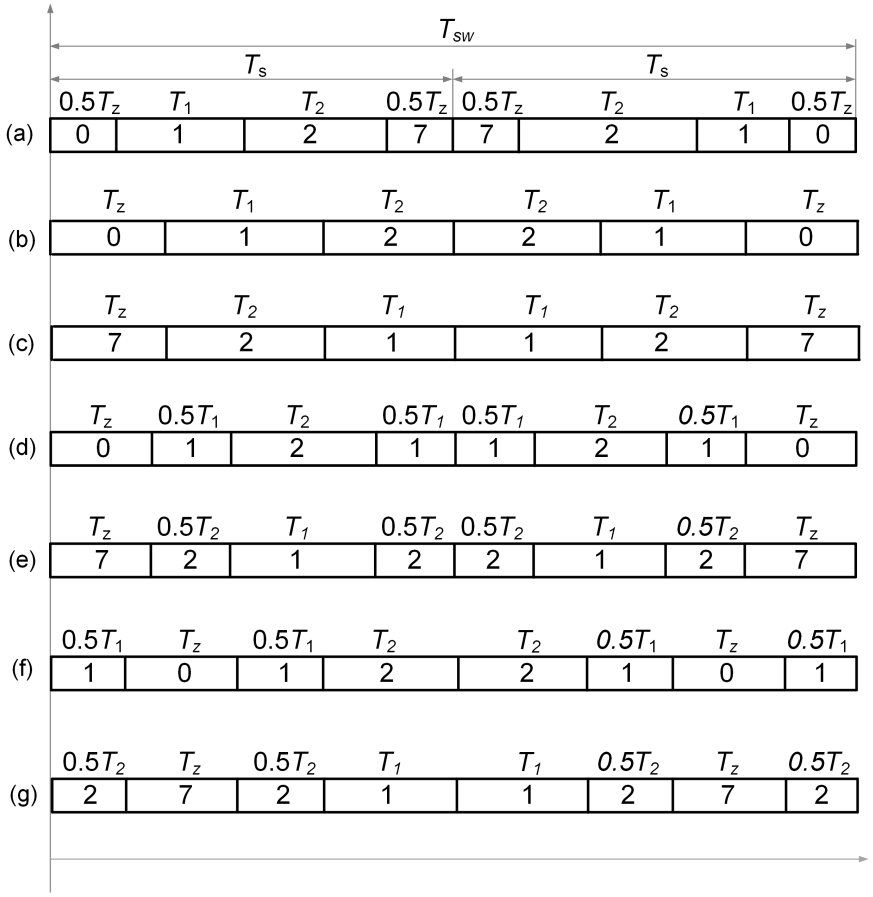

Figure 2.6: Possible Switching Sequences in Sector I (a) 0127-7210, (b) 012-210, (c) 721-127, (d) 0121-1210, (e) 7212-2127, (f) 1012-2101 and (g) 2721-1272.

2.4.1 Conventional Sequence

The switching sequence corresponding to the applied states 0127 and its reverse sequence 7210 in alternating sub-cycles in Sector I is termed as conventional sequence. The space vector plane corresponding to CSVPWM in Sector I is shown in Fig. 2.7. CSVPWM results in switching of all phases, thereby leading to three switchings in a sub-cycle. For example, applied sequence of 0 (- - -), 1 (+ - -), 2 (+ + -), 7 (+ + +) in Sector I leads to switching of phase a, b and c when transitioning from 0 to 1, 1 to 2 and 2 to 7 respectively.

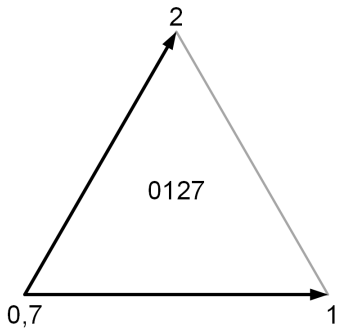

Figure 2.7: Conventional Sequence

2.4.2 Discontinuous Sequences

In discontinuous sequences, only one of the zero states (either 0 or 7) is used in a sub-cycle instead of both. This are also called clamping sequence because it leads to clamping of a phase pole either to positive or negative DC bus. For example, switching sequence 7 (+ + +), 1 (+ - -), 2 (+ + -) in Sector I leads to phase a clamped to positive DC bus and phase b and c switching. Thus, total number of switchings in a sub-cycle are two instead of three as in CSVPWM which means saving in switching loss. Total duration of clamping in a fundamental cycle is 120° degrees in these sequences i.e., a phase switches for two-thirds of the fundamental cycle and remains clamped for one-third of the fundamental cycle. Regions of clamping depend on the applied sequence which are shown in Fig. 2.8. Applied sequence 721 and 012 in Sector I are referred as DPWMMAX and DPWMMIN and they lead to continuous 120°clamping. Sequence 721 in first half sector and 012 in next half sector produce clamping of two 60° durations in a fundamental cycle which is referred as Continual Clamp PWM (CCPWM). And Sequence 012 in first half sector and 721 in next half sector generate clamping of four 30° durations in a fundamental cycle which is referred as Split Clamp PWM (SCPWM).

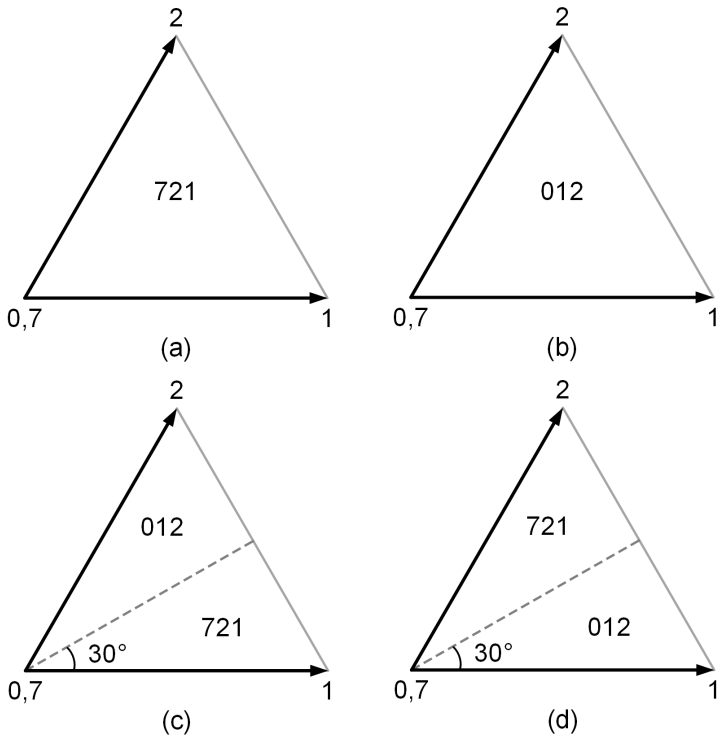

Figure 2.8: Discontinuous Sequences (a) DPWMMAX, (b) DPWMMIN, (c) CCPWM, (d) SCPWM.

2.4.3 Double Switching Clamping Sequences

Another class of PWM sequences has emerged which involves double switching and clamping also known as advanced bus clamped PWM methods (ABCPWM) [53]. They cannot be implemented using triangle comparison approach. In such sequences, one zero state is used in a sub-cycle and one of the active states is divided into two equal durations. In such sequences, one phase gets clamped, one phase switches once and one phase switches twice in a sub-cycle. For example, when 7 (+ + +), 2 (+ + -), 1 (+ - -), 2 (+ + -) is applied in first half of Sector I (Fig. 2.9 a), phase a is clamped to positive DC bus, phase b switches twice and phase c switches once. Such sequences give better THD performance as compared to conventional and discontinuous sequences at high modulation indices. Fig. 2.9 shows four double

switching clamping sequences where (a) and (b) belong to Type-I and (c) and (d) belong to Type-II sequences. Sequences in Fig. 2.9 (a) and Fig. 2.9 (b) generate Advanced Continual Clamp PWM (ACCPWM) and Advanced Split Clamp PWM (ASCPWM) respectively.

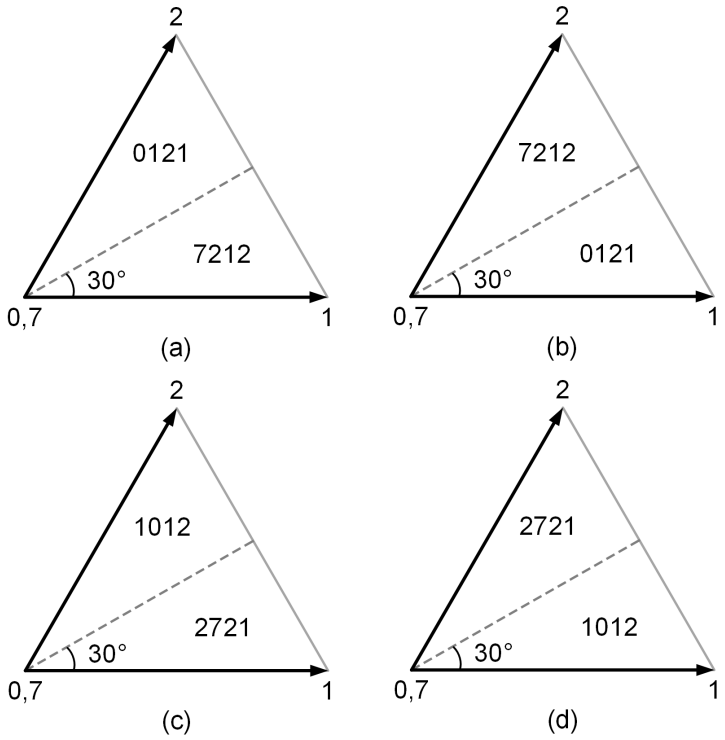

Figure 2.9: Double Switching Clamping Sequences (a) and (b) Type-I, (c) and (d) Type-II.

2.5 Conclusion

In this chapter, space vector-based approach for different PWM methods is discussed. Conventional and clamping sequences are analyzed both with triangular comparison approach and space vector approach. Then double switching clamping sequences are shown that can be implemented using space vector approach.

In this report, CSVPWM will serve as benchmark for evaluating the performance of proposed PWM method. Performance of proposed PWM method will also be com-

pared against one bus clamped PWM method i.e., DPWM1 or CCPWM and one double switching clamping sequence i.e., ACCPWM.

Chapter 3

240° CLAMPED PWM (240CPWM) CONCEPT AND ITS CHARACTERISTIC SWITCHING LOSS

3.1 Cascaded Topology and 240CPWM Concept

A cascaded architecture of a DC-DC stage followed by a three-phase DC-AC stage is gaining acceptance in the traction inverters of many Hybrid Electric Vehicles (HEVs) and to a smaller extent in Electric Vehicles (EVs) [22]. This is due to the ability to support high voltage motors and independently optimize motor and battery voltages, and improved overall system efficiency, [54] [55]. Fig. 3.1 shows the EV powertrain architecture with a DC-DC converter that interfaces a relatively low voltage battery to the inverter and the high voltage motor. This cascaded topology in EV drivetrain supports higher DC link voltages due to which the motor speed has increased from 6000 rpm to 17000 rpm over the years; reducing the size of motor and inverter thereby increasing the power density [56]. Commercial EVs particularly Hybrid Electric Vehicles (HEVs) have developed mature architecture to interface battery and inverter DC bus via bidirectional DC-DC converter [57], [58], [59], [60]. This cascaded topology is used in various commercial vehicles such as Toyota Prius [57], Lexus LS 600h [58], Toyota Camry [59] and Honda Accord Hybrid [60].

Such a system with DC-DC converter already in place lends itself very well to the implementation of the 240° clamped space vector PWM (240CPWM). The DC link voltage at the output of the DC-DC stage is controlled dynamically both in magnitude and in waveshape corresponding to the motor speed. The required DC link voltage for 240CPWM for three different speeds is also shown in Fig. 3.1 as an example.

Recently proposed PWM method with 240° clamping of a phase in a line cycle (240CPWM) gives superior performance in terms of reduced switching loss and THD [61], [62], [63]. Cascaded topology of EV powertrain under consideration that is suitable for the implementation of 240CPWM is shown in Fig. 3.1. The DC-DC converter topology used is three-phase interleaved boost converter. The DC-DC converter allows the shaping of dynamic DC link voltage that is required for 240CPWM. Voltage vectors produced by two-level Voltage Source Inverter (VSI) are shown in Fig. 2.2. A two-level, three phase VSI has eight switching states: six active states (1 to 6) and two zero states (0 and 7). The reference voltage vector V_{REF} is sampled once in every switching sub-cycle T_s. CSVPWM uses two active states and two zero states in each sub-cycle while 240CPWM does not use any zero-state resulting in clamping of two-phase poles simultaneously. With 240CPWM, each phase pole is clamped to positive DC rail or negative DC rail for a total of 240° and switches only for 120° in a fundamental cycle.

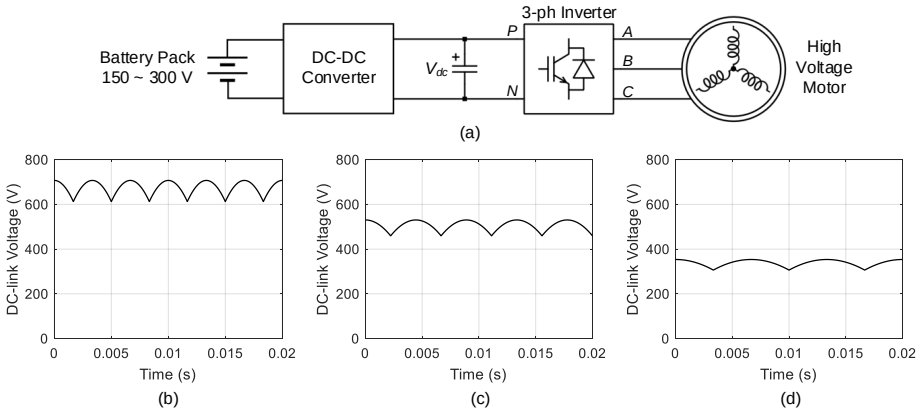

Figure 3.1: EV Powertrain Architecture. (a) Block diagram; Proposed DC-link Voltage for (b) High Speed, (c) Medium Speed, (d) Low-Speed Operation.

Conventional space vector PWM (CSVPWM) uses both the zero states (0 and 7) and divides T_z equally between them. It employs the switching sequence of 0127 (or 7210) in a sub-cycle in Sector I. The total number of switchings in a sub-cycle with

both the zero states applied is three. The discontinuous PWM (DPWM) methods employ only one zero state resulting in two switchings per sub-cycle. Several DPWM sequences have been discussed in literature [47], [53]. CSVPWM results in lower distortion in line current whereas DPWM leads to a reduction in switching loss at the expense of increased switching frequency ripple and total harmonic distortion (THD) [53], [48]. For the purpose of evaluation and comparison, we will consider the 120° clamping PWM and refer it as DPWM1, which employs sequences 721 (or 127) in the first 30° of Sector I and 012 (or 210) in the next 30° of Sector I. The switching sequence in a sub-cycle for CSVPWM, DPWM1 and 240CPWM in Sector I are shown in Fig. 3.2. The red arrows correspond to the variable magnitude of applied voltage vectors for 240CPWM.

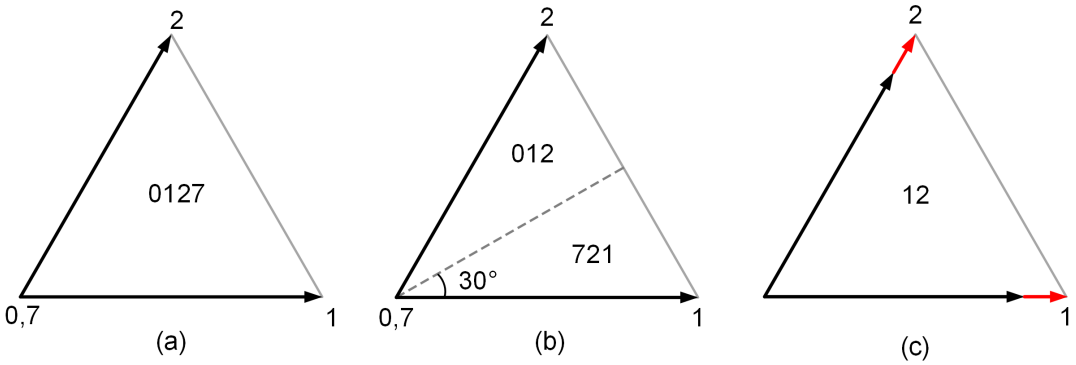

Figure 3.2: EV Powertrain Architecture. Switching Sequence of (a) CSVPWM and (b) DPWM1 (c) 240CPWM in Sector I.

Expressions of dwell times for 240CPWM are given below:

$$T_1 = \frac{V_{REF}}{V_{dc}(t)} \frac{\sin(60^\circ - \alpha)}{\sin 60^\circ} T_s \tag{3.1}$$

$$T_2 = \frac{V_{REF}}{V_{dc}(t)} \frac{\sin \alpha}{\sin 60^\circ} T_s \tag{3.2}$$

The condition for eliminating the zero states is given by

$$T_z = T_s - T_1 - T_2 = 0 \tag{3.3}$$

In these equations, V_{dc} is replaced by $V_{dc}(t)$ to incorporate the dynamic DC link voltage.

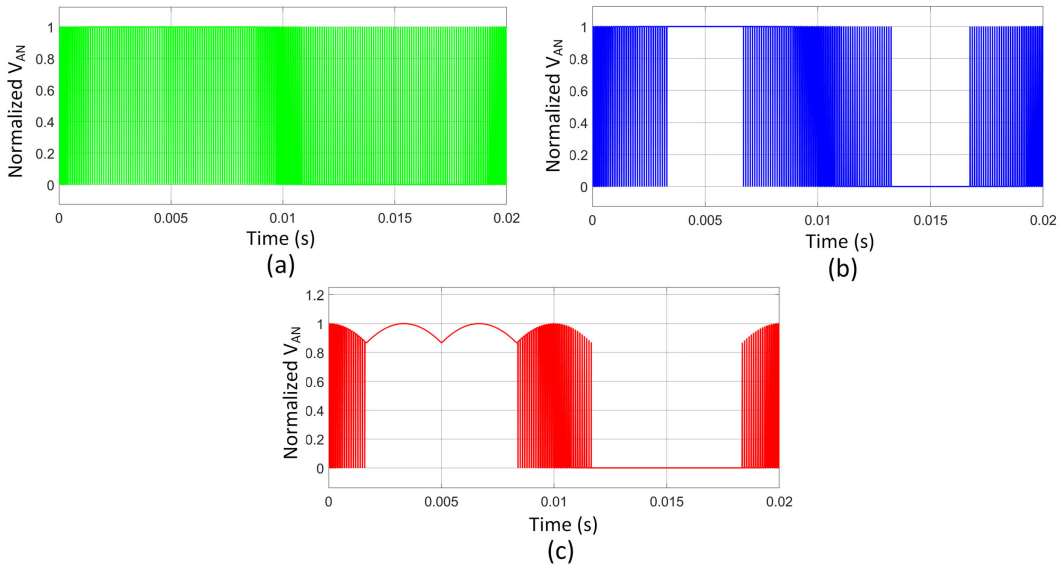

Figure 3.3: Normalized Switching Phase Voltage for (a) CSVPWM (b) DPWM1 (c) 240CPWM, Normalized with Respect to Peak Line to Line Voltage ($V_{LL,pk}$).

Fig. 3.3 shows the normalized switching phase voltage for CSVPWM, DPWM1 and 240CPWM. For CSVPWM, phase voltage is always switching. For DPWM1, clamping of 60° to positive DC bus and 60° to negative DC bus is visible that results in clamping of 120° in a line cycle. In 240CPWM, phase voltage clamps for 120° to positive DC bus and to negative bus for another 120°. Thus, total clamping duration in 240CPWM is 240° in a line cycle (name 240CPWM comes from 240° clamping).

The three phase switching signals for 240CPWM are shown in Fig. 3.4 (a) where switching of 120° and clamping of 240° of each phase in a fundamental cycle is visible. Fig. 3.4 (b) shows the average modulating signals of 240CPWM.

Fig. 3.5 shows the inverter voltage waveforms corresponding to 240CPWM. Phase voltages V_{AN}, V_{BN} and V_{CN} are shown in 3.5 (a), (b) and (c) respectively. All phase voltages along with dynamic DC link voltage are shown in Fig. 3.5 (d). Finally, Fig. 3.5 (e) shows the switching and average line to line of inverter with 240CPWM. It

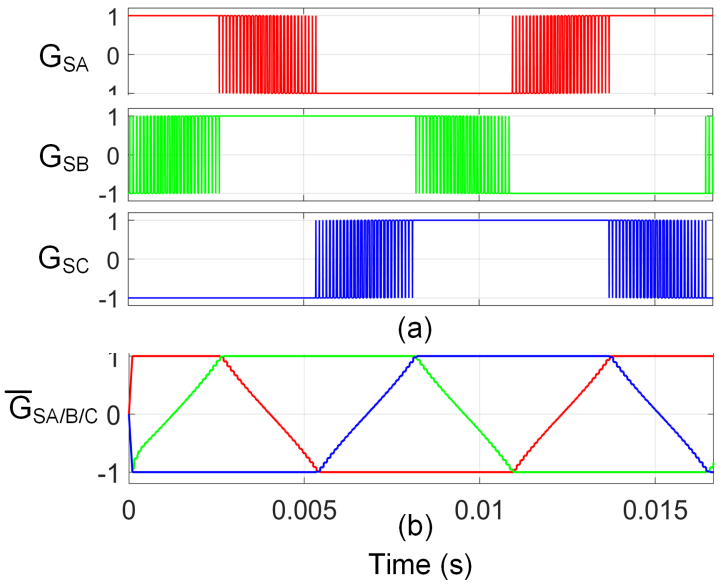

Figure 3.4: (a) Three Phase Switching Signals and (b) Average of Switching Signals for 240CPWM.

shows the dynamic DC link voltage becomes part of line to line voltage in clamped regions to ensure sinusoidal output voltage and currents. With complete elimination of zero states in 240CPWM, constant DC link voltage cannot be used. 240CPWM requires a six-pulse dynamically varying DC link voltage instead of a constant DC voltage as shown in Fig. 3.5 (d) to maintain undistorted sinusoidal output voltages and currents. Fig. 3.5 (e) shows the switching (solid) and average (dotted) line to line voltage, V_{AB}. V_{AB} is color coded to identify which switching phase voltage becomes part of line-to-line voltage. For example, switching phase B (yellow) and A (green) voltages appear in V_{AB} from 0 to 0.0026s and 0.0026s to 0.0053s respectively and it is clamped to DC link voltage (black) from 0.0053s to 0.0083s completing half fundamental cycle.

The dynamic DC link voltage is generated by the front-end DC-DC stage. The expression for the dynamic DC link voltage can be equivalently given as follows in

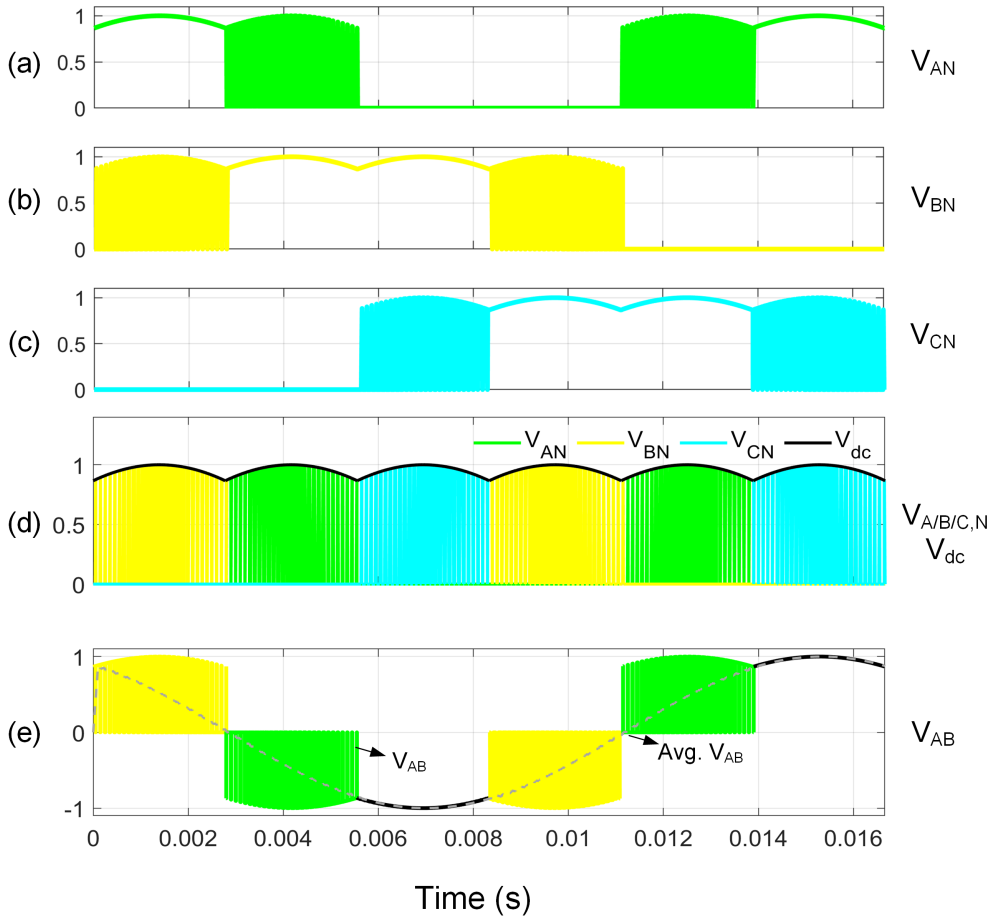

Figure 3.5: Characteristic Waveforms for 240CPWM (a) Phase A Voltage (b) Phase B Voltage (c) Phase C Voltage (d) Phase A/B/C Voltages with Dynamic DC-link Voltage (e) Switching and Average Line to Line Voltage, All Normalized with Respect to Peak Line to Line Voltage ($V_{LL,pk}$)

Sector I.

$$V_{dc}(t) = \max\{v_a, v_b, v_c\} - \min\{v_a, v_b, v_c\} \tag{3.4}$$

where v_a,v_b and v_c are the reference phase voltages.

The 240CPWM has an equivalence in carrier based PWM approach as well. In this case the modulating signals that are compared with a triangle carrier to generate

the PWM signals with required duty ratios are given by (3.5).

$$d_a = [v_a - \min\{v_a, v_b, v_c\}]/V_{dc}(t) \tag{3.5a}$$

$$d_b = [v_b - \min\{v_a, v_b, v_c\}]/V_{dc}(t) \tag{3.5b}$$

$$d_c = [v_c - \min\{v_a, v_b, v_c\}]/V_{dc}(t) \tag{3.5c}$$

3.2 Switching Loss Characteristics of 240CPWM

240CPWM results in lowest switching loss because of 240° clamping and switches only for 120° in a fundamental cycle. The total switching loss of the three-phase inverter over a line cycle can be reduced by minimizing the switching loss in every sub-cycle. Switching loss in a sub-cycle depends on DC link voltage V_{dc}, number of switchings in a phase n_{PH} and the current flowing through the switch i_{PH}. The contribution of current ripple to switching loss is ignored since it is very small. To compare different PWM methods in terms of switching loss, the simplest way is to compare the product of number of switchings in a phase, the DC link voltage and the instantaneous current flowing through the switch in each sub-cycle. Considering phase A, its fundamental current can be normalized with respect to its peak value I_m to produce normalized per phase switching loss $P_{SUB,PH}$.

$$P_{SUB,PH} = V_{dc,nom}\frac{n_{PH}|i_{PH}|}{I_m} = V_{dc,nom}n_{PH}|\sin(\omega t + \phi)| \tag{3.6}$$

where ϕ is the power factor angle and $V_{dc,nom}$ is the DC link voltage normalized to its peak value. The number of switchings in a phase depends on the specific PWM method used. For CSVPWM each phase switches once in a sub-cycle while for DPWM1 a phase either switches once or does not switch at all in a sub-cycle. Table 3.1 shows the three modulation methods under consideration in terms of number of switchings in a phase in Sector I.

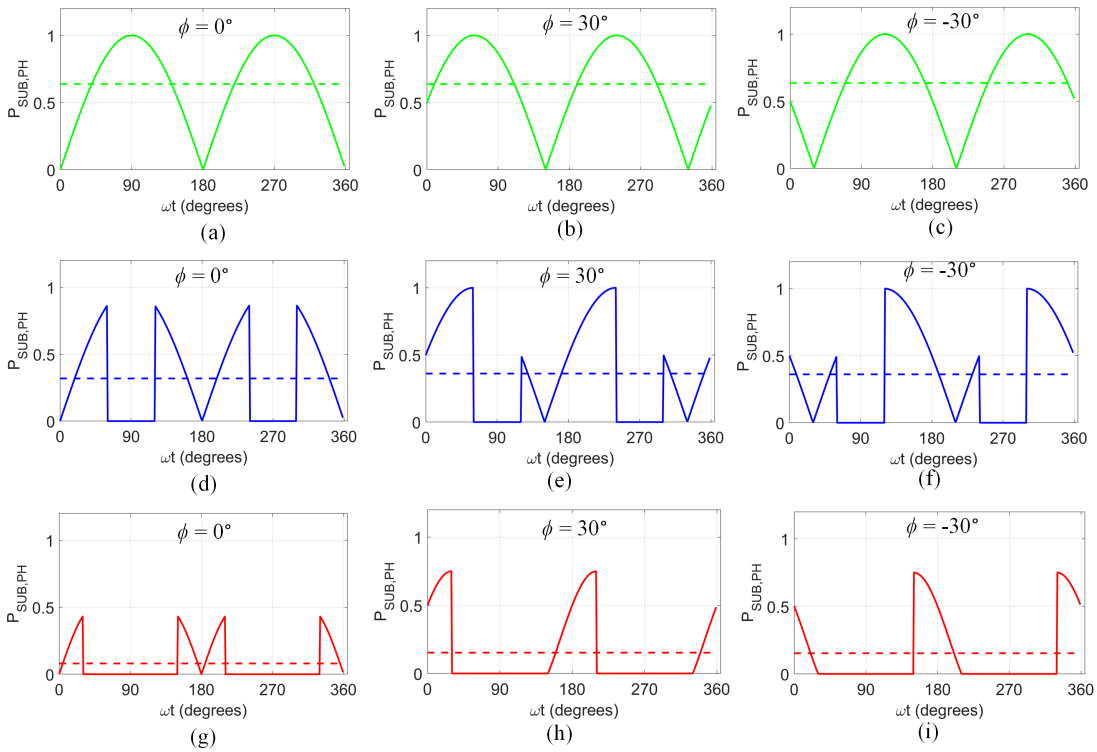

Figure 3.6: Variation of Normalized Local Switching Loss in Phase A over a Line Cycle $P_{SUB,PH}$. (a) CSVPWM, $\phi = 0°$, (b) CSVPWM, $\phi = 30°$, (c) CSVPWM, $\phi = -30°$, (d) DPWM1, $\phi = 0°$, (e) DPWM1, $\phi = 30°$, (f) DPWM1, $\phi = -30°$, (g) 240CPWM, $\phi = 0°$, (h) 240CPWM, $\phi = 30°$, (i) 240CPWM, $\phi = -30°$

Detailed analysis of $P_{SUB,PH}$ for various bus clamping techniques is carried out in [53]. Here we present the variation of $P_{SUB,PH}$ for CSVPWM, DPWM1 and 240CPWM at three different power factor angles. $P_{SUB,PH}$ for CSVPWM is just a rectified sine function of unit magnitude with average of $2/\pi$ (i.e. 0.637) in a line cycle (Fig. 3.6(a)). $P_{SUB,PH}$ for CSVPWM only shifts depending on the power factor angle, but its average remains the same (Fig. 3.6(b) and (c)). For DPWM1, a phase is clamped for $\omega t \in [60°, 120°] \cup [240°, 300°]$ which is near the current peaks for a total of 120° in line cycle at unity power factor (Fig. 3.6(d)). Thus, average of $P_{SUB,PH}$ for DPWM1 is lower than CSVPWM. At power factor angle of $-30°$ and 30°, averaged $P_{SUB,PH}$ for DPWM1 is slightly higher than that for unity power factor due to non-ideal positions of phase clamping i.e. clamping near current peaks is not there

Table 3.1: Number of Switchings in a Phase in Sector I

Technique		n_A	n_B	n_C
CSVPWM		1	1	1
DPWM1	721	0	1	1
	012	1	1	0
240CPWM		0	1	0

anymore. In fact, some switching can be seen near current peaks in 3.6 (e) and (f). It can be observed from Fig. 3.6(g), that in 240CPWM, a phase switches only for $\omega t \in [0°, 30°] \cup [150°, 210°] \cup [330°, 360°]$, which is near the zero crossings of the phase current for a total of 120° and remains clamped for the remaining 240° which happens to be the current peaks at unity power factor. This is an ideal scenario of switching to achieve minimum possible switching loss. That is why average of $P_{SUB,PH}$ for 240CPWM is only 0.08, which is around seven times lower than that of CSVPWM. Now for non-unity power factor, 240CPWM still yields savings in switching loss as compared to CSVPWM but the extent of savings is a function of power factor angle. At power factor angle of 30° lagging and 30° leading, each phase still switches near zero crossing of current and remains clamped near current peaks with 240CPWM (Fig. 3.6(h) and (i)). 240CPWM outperforms CSVPWM and other clamped sequences too because it is effectively switching, in an average sense, only at one third of the switching frequency.

$P_{SUB,PH}$ for all the three phases are added to give normalized total switching loss in a sub cycle $P_{SUB,TOT}$. $P_{SUB,TOT}$ is in fact the product of the normalized DC link voltage and the weighted sum of the absolute three phase currents, where the weights are the number of switching-transitions of each phase in a sub-cycle [48].

$$P_{SUB,TOT} = V_{dc,nom} \frac{n_A|i_A| + n_B|i_B| + n_C|i_C|}{I_m} \tag{3.7}$$

where $i_A = I_m \sin(\omega t + \phi)$, $i_B = I_m \sin(\omega t - 120° + \phi)$, $i_C = I_m \sin(\omega t - 240° + \phi)$. Variation of $P_{SUB,TOT}$ for 240CPWM along with CSVPWM and DPWM1 in Sector I is shown for different power factor angles in Fig. 3.7. As discussed before, minimum switching losses can be observed for 240CPWM at unity power factor in Fig. 3.7(a). For CSVPWM all three absolute phase currents and for DPWM1 two absolute phase currents are added to yield $P_{SUB,TOT}$ in Sector I. In 240CPWM, however, only one absolute phase current (phase B) gives $P_{SUB,TOT}$ in Sector I because phase A and C are clamped to positive and negative DC bus respectively. For non-unity power factors, weights in (3.7) remain the same as for unity power factor case, only sections of absolute currents that are being summed up shift accordingly as shown in Fig. 3.7(b), (c) and (d).

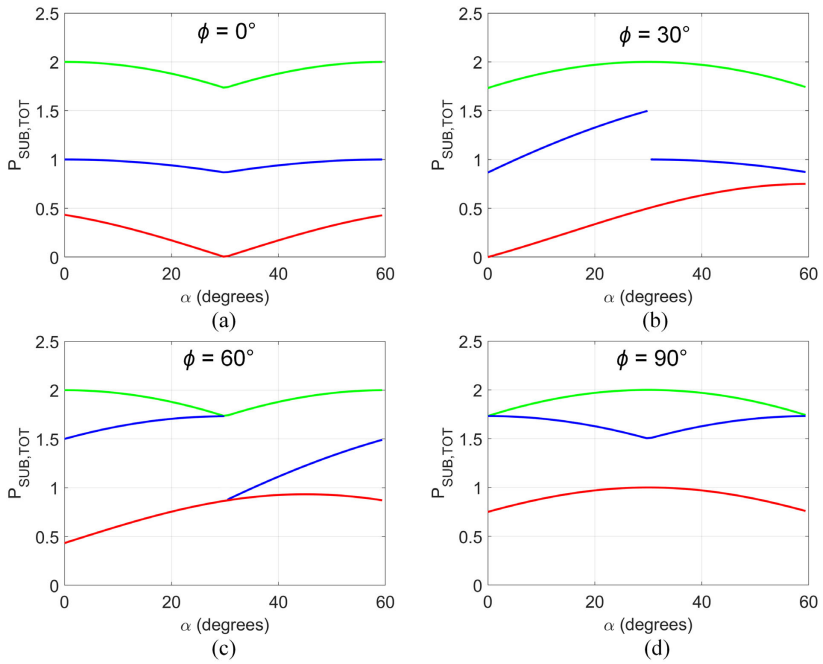

Figure 3.7: Variation of Normalized Total Switching Loss in a Sub-cycle over a Sector $P_{SUB,TOT}$ for Different PWM methods (a) $\phi = 0°$, (b) $\phi = 30°$, (c) $\phi = 60°$ and (d) $\phi = 90°$

Average value of $P_{SUB,TOT}$ for CSVPWM over a sector is $6/\pi$ at any power factor [53]. The normalized switching loss P_{SW} for a given PWM method is defined as the

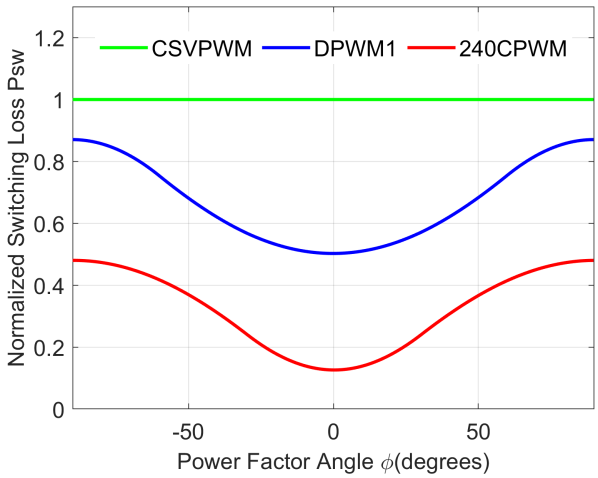

Figure 3.8: Variation of P_{SW} for all PWM Methods under Consideration Against Power Factor Angle.

ratio of averaged $P_{SUB,TOT}$ for the given PWM method over a sector to the averaged $P_{SUB,TOT}$ for CSVPWM. P_{SW} facilitates the comparative evaluation of various techniques using power losses of all three phases at different power factor angles.

$$P_{SW} = \frac{1}{2}\int_{0}^{\pi/3} P_{SUB,TOT}\ \mathrm{d}\alpha \tag{3.8}$$

Fig. 3.8 shows the variation of P_{SW} against power factor angle for CSVPWM, DPWM1 and 240CPWM. Again, 240CPWM is the lowest switching loss PWM method in the entire power factor angle range.

Now the variation of switching loss for variable speed operation will be analyzed using the constant V/f control discussed in the previous sub-section. Two scenarios of variable speed operation will be studied, one with constant V_{dc} and other with variable V_{dc}. For varying V_{dc} case, value of V_{dc} remains constant over a fundamental period but that constant value is different for different fundamental frequencies (or speeds) for CSVPWM and DPWM1. However, for 240CPWM, V_{dc} is variable both in average and instantaneous sense i.e. V_{dc} is variable even within a fundamental period. For constant V_{dc} operation, switching losses are higher since switches are switching

at fixed (high) V_{dc}, no matter how small the output voltage requirement is as governed by motor speed. Switching losses for varying V_{dc} cases are significantly lower than constant V_{dc} scenario since DC-link voltage is brought to the minimum value required to support the given line-to-line voltage using a DC-DC converter. This way the inverter switches do not have to switch at maximum V_{dc} at lower speeds, thereby reducing the switching loss considerably.

Fig. 3.9 shows the switching loss variation against fundamental frequency for CSVPWM (constant and varying V_{dc}), DPWM1 (constant and varying V_{dc}) and 240CPWM normalized with respect to the classical case of CSVPWM with constant V_{dc} at unity power factor. 240CPWM is the case of varying DC-link voltage by default. It can be observed that P_{SW} for 240CPWM is substantially lower than all the other cases. Switching loss for varying V_{dc} cases is always less than their corresponding constant V_{dc} cases. For the varying V_{dc} cases, switching loss is low at lower power and increases progressively for higher power levels. This is due to the fact that the magnitude of the line currents are kept the same while the DC link voltage magnitude is increased linearly with fundamental frequency resulting in linear increase in the switching loss.

From Fig. 3.9 it can be observed that switching loss for 240CPWM is 7.8 times lower than CSVPWM with constant DC link voltage at the maximum fundamental frequency. It is noted that the switch ratings with 240CPWM are identical to that of conventional two-level, three-phase inverters, since the DC link voltage with 240CPWM is never more than that of an inverter with conventional PWM methods. The peak current rating is equal to the peak line current, which is similar to conventional PWM methods.

The PWM methods under consideration have very different switching loss profiles depending upon the duration and location of clamping. However, their conduction

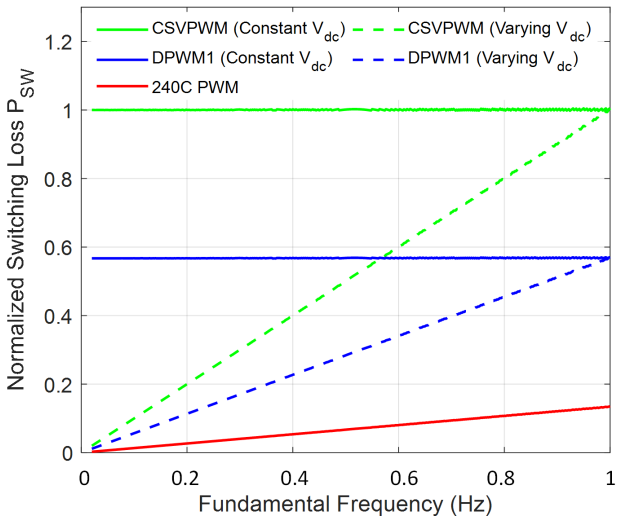

Figure 3.9: Variation of Normalized Switching Loss P_{SW} Against Normalized Fundamental Frequency for Various PWM methods (Normalized with Respect to CSVPWM) at Unity Power Factor. The Fundamental Frequency is Normalized with Respect to $f_{1,max}$.

losses are nearly same due to almost same RMS current flowing through the switches.

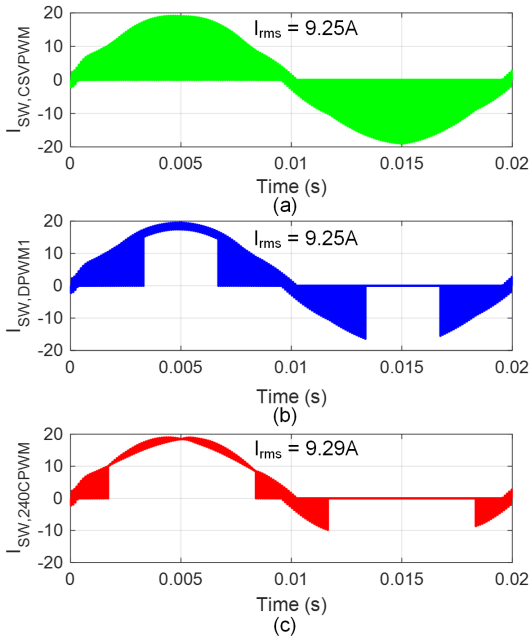

Figure 3.10: Instantaneous Switch Current with RMS Values Indicated for Each (a) CSVPWM, (b) DPWM1 and (c) 240CPWM.

3.3 Experimental Validation of Switching Loss

The experimental set-up is rated at 10 kW and is illustrated in Fig. 3.11. Fig. 3.12 shows a picture of the set-up. It is designed to test and compare the CSVPWM, DPWM1 and 240CPWM methods in terms of conversion efficiency of the DC-AC stage. Test points at three different fundamental frequencies of 25 Hz, 37.5 Hz and 50 Hz respectively are designed to test each modulation method with constant load current and constant fundamental V/f ratio. The operating conditions for different test points is summarized in Table 3.2.

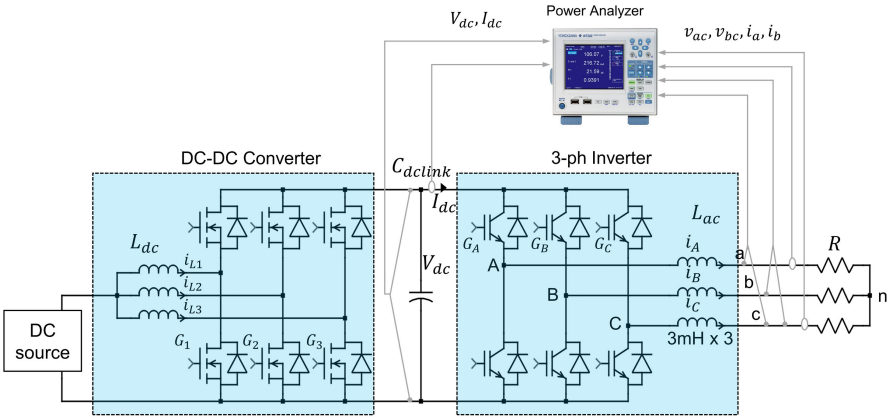

Figure 3.11: Illustration of Experimental Setup

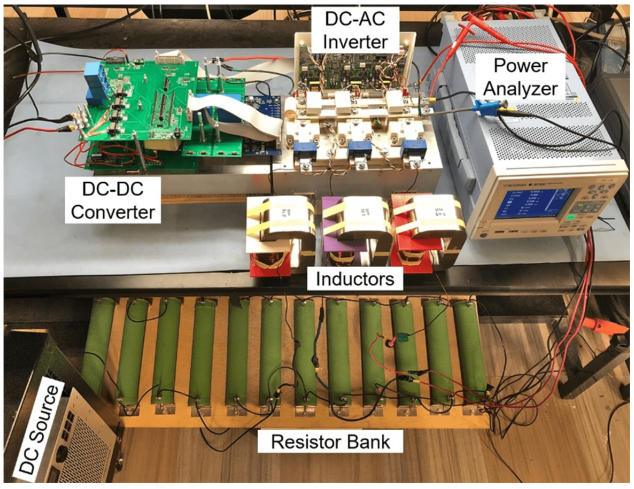

Figure 3.12: Picture of the Experimental Setup

The CSVPWM and DPWM1 methods are tested for both constant and varying DC-link voltage conditions. For the constant DC-link voltage condition, the modulation index is adjusted for different fundamental frequencies in order to keep a constant V/f ratio. For the varying DC-link voltage condition, the modulation index is fixed at $0.9M_{max}$ and the DC-link voltage is varied.

The DC-DC converter used in the experiment setup is a three-phase interleaved Buck/Boost converter. A common duty ratio is applied to all the three phases. The gate pulses of the three phases are shifted by 120 degrees with respect to each other. The reference for the DC link voltage is expressed by (3.4). Currently, open-loop control is used for the DC-DC converter and the duty ratio is calculated as follows:

$$D = 1 - \frac{V_{in}}{max\left\{v_a, v_b, v_c\right\} - min\left\{v_a, v_b, v_c\right\}} \tag{3.9}$$

The conversion efficiency of the inverter is measured by a Yokogawa WT500 power analyzer. The output current waveforms are captured by a LeCroy HDO8038 oscilloscope with 10 MHz sampling frequency with LeCroy CP030 30 A 50 MHz current probes.

Each phase leg of the Boost converter switches at 200 kHz, resulting in 600 kHz ripple in the DC-link voltage. The DC-DC and DC-AC stages are controlled by using the same reference phase angle. When implementing the 240CPWM, the same reference phase angle is used for generating the DC link voltage and the PWM, thus synchronism between the generated 6-pulse DC link voltage and the modulation of the subsequent DC-AC stage is always secured by the control system. A series-connected inductive-resistive load bank is used to emulate a motor load with unity power factor. The switching frequency of the inverter is 10 kHz. A wye-connected filter capacitor bank is connected after the inductors in order to extract the average phase voltage and line-to-line voltage waveforms.

Table 3.2: Constant V/f Operating Conditions at Three Different Fundamental Frequencies

Parameters	**Values**		
Fundamental Frequency	50 Hz	37.5 Hz	25 Hz
Output Voltage (L-L RMS)	500 V	375 V	250 V
Load Resistance	25 Ω	18.7 Ω	12.5 Ω
Load Current (RMS)	11.5 A	11.5 A	11.5 A
Load Power	10 kW	7.5 kW	5 kW
Constant V_{dc}	800 V	800 V	800 V
Varying V_{dc}	800 V	600 V	400 V
Dynamic V_{dc}	707 V pk	530 V pk	353 V pk

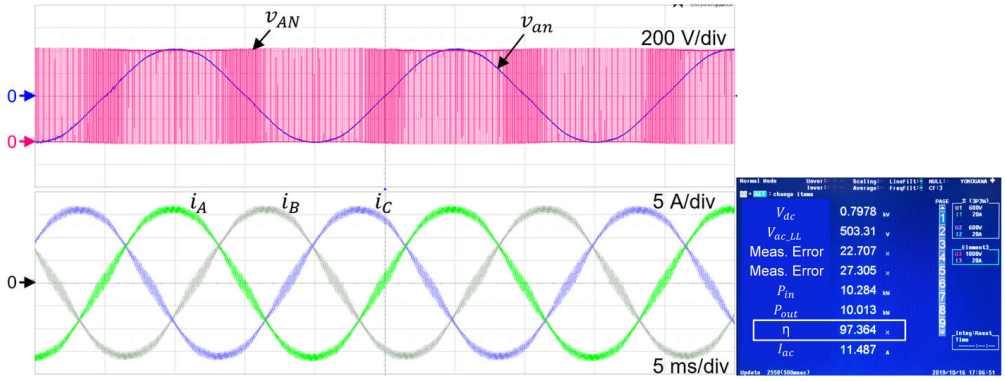

Figure 3.13: Experimental Waveforms of Phase Voltage v_{AN}, Phase Voltage after the Filter v_{an}, and Output Currents at 10 kW, 50 Hz with CSVPWM at V_{dc} = 800 V.

Fig. 3.13, 3.14 and 3.15 show the experimental results of CSVPWM, DPWM1 and 240CPWM at 10 kW, 50 Hz. Switching phase voltage v_{AN}, phase voltage after filter v_{an}, line currents i_A, i_B and i_C are shown. The power analyzer image shows the inverter efficiency of the given test. Inverter efficiency with CSVPWM, DPWM1 and 240CPWM at 10 kW is 97.364%, 98.39% and 99.1% respectively. Fig. 3.15 (b) shows the line to line voltage and dynamic DC link voltages with 240CPWM at 10 kW. Efficiency with 240CPWM is the highest because of just 120° switching in a line

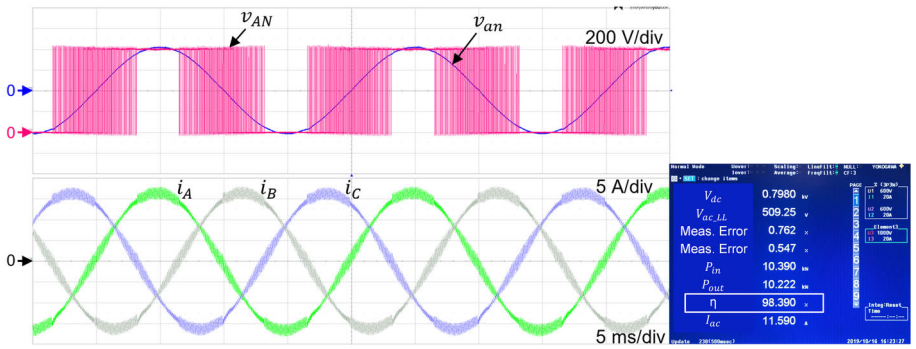

Figure 3.14: Experimental Waveforms of phase voltage v_{AN}, Phase Voltage after the Filter v_{an}, and Output Currents at 10 kW, 50 Hz with DPWM1 at $V_{dc} = 800$ V.

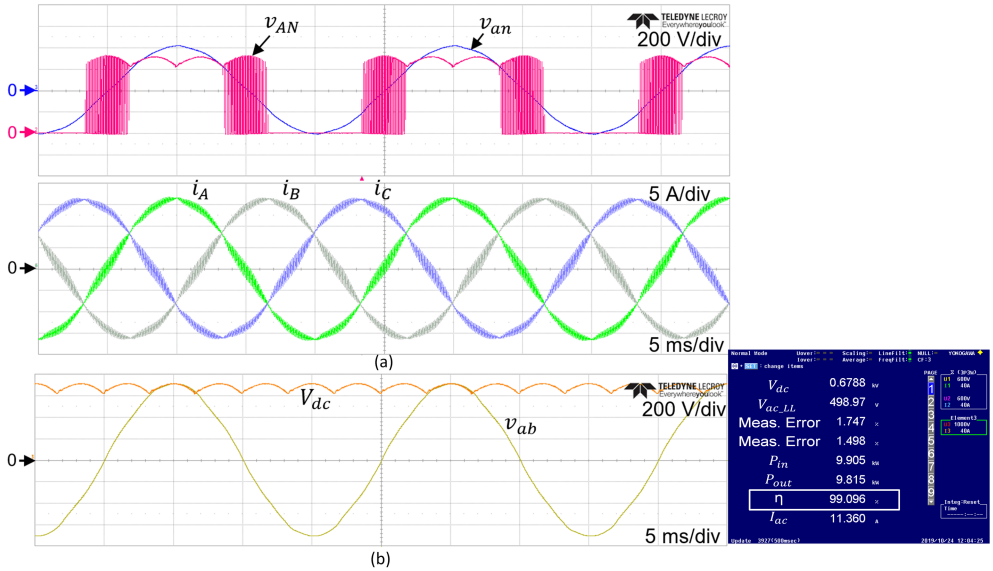

Figure 3.15: (a) Experimental Waveforms of Phase Voltage v_{AN}, Phase Voltage after the Filter v_{an}, and Output Currents at 10 kW, 50 Hz with 240CPWM (b) Dynamic DC Link Voltage $V_{dc,peak} = 720$ V and Filtered Line to Line Voltage v_{ab}

cycle (evident from the phase voltage v_{AN}). CSVPWM and DPWM1 are operated at $0.9M_{max}$ due to large dead time of Si IGBTs while 240CPWM operates at M_{max}. To compare all PWM methods at same power level, DC link voltage of 720 V is maintained for 240CPWM and 800 V for CSVPWM and DPWM1 for 10 kW. Fig. 3.16 shows the averaged phase voltage $\overline{v}_{AN}$ for all PWM methods under consideration at 10 kW.

It is evident from Fig. 3.16 that with CSVPWM the IGBTs are constantly switch-

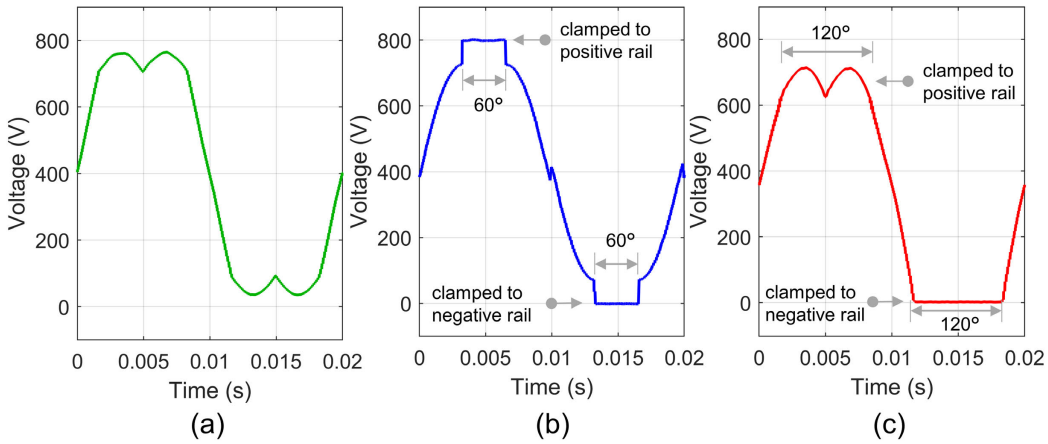

Figure 3.16: Switching-cycle Averaged Phase Voltage $\overline{v}_{AN}$ with (a) CSVPWM, (b) DPWM1 and (c) 240CPWM at 10 kW, 50 Hz, Extracted from Experimental Phase Voltage Waveform.

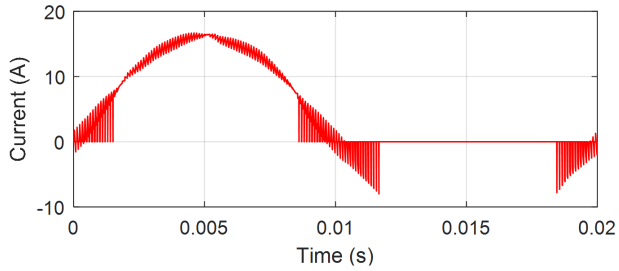

Figure 3.17: Phase A top Switch Current Waveform with 240CPWM, Derived from Measured Switch Gate Pulse and Inductor Current Waveforms.

ing in a fundamental cycle. With DPWM1, the output is clamped to the positive DC-link for 60° near the positive peak and to the negative DC-link for 60° near the negative peak, resulting in less switching actions. With 240CPWM, the output is clamped to the positive DC-link for 120° near the positive peak and to the negative DC-link for 120° near the negative peak, resulting in the lowest number of switchings.

Fig. 3.17 shows the current in the Phase A top switch (through IGBT or the anti-parallel diode) with 240CPWM, which is derived from the waveforms of the output current and the switch gate pulses. It can be seen that the IGBT only switches near the zero crossings of the output current and is kept ON during $\omega t \in [30°, 150°]$ and

kept OFF during $\omega t \in [210°, 330°]$. Due to the near-unity power factor operation, this also corresponds to switching only near the zero-crossing of the line current. Therefore, with the combination of minimum number of switchings and low magnitude of currents at the instants of switching, the switching losses are significantly lower compared to even the DPWM1 and even more so compared to CSVPWM.

Now to evaluate the performance of all PWM methods under consideration with constant V/f mode of operation, two more test points (i.e., 7.5 KW 37.5 Hz and 5 kW 25 Hz) are considered.

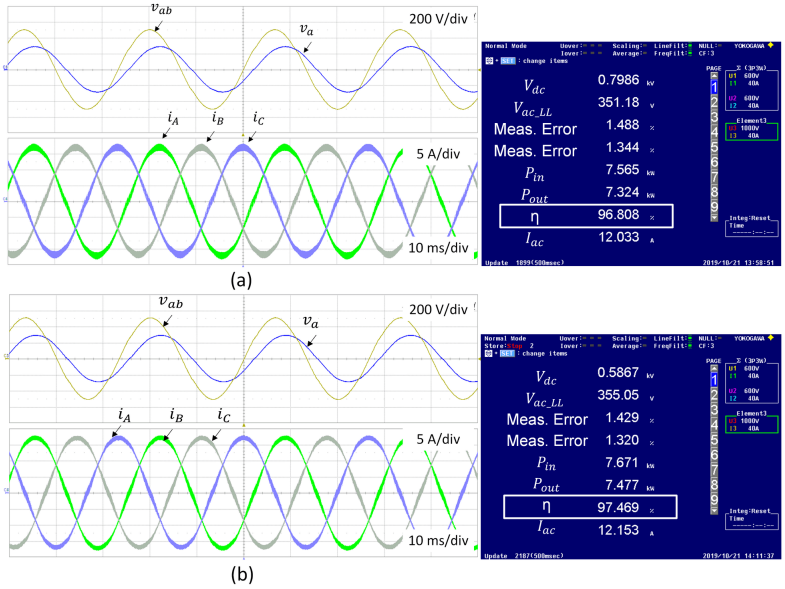

Figure 3.18: (a) Experimental Phase Voltage v_{an}, Line to Line Voltage v_{ab} after the Filter and Output Currents at 7.5 kW, 37.5 Hz with CSVPWM (a) Constant DC Link Voltage Case, $V_{dc} = 800$ V, (b) Varying DC Link Voltage Case, $V_{dc} = 600$ V

Fig. 3.18 shows the experimental waveforms with CSVPWM at 7.5 kW, 37.5 Hz both with constant V_{dc} (Fig. 3.18 (a)) and varying V_{dc} (Fig. 3.18 (b)). For constant DC link voltage case, V_{dc} remains at 800 V and modulation index is lowered to achieve lower output voltages, while for varying DC link voltage case, DC link voltage is 600 V and modulation index remains maximum. Efficiency with constant DC link voltage case is 96.8% while it is 97.5% for varying DC link voltage case with CSVPWM at 7.5

kW. The increase in efficiency with varying DC link voltage is because that inverter switches do not have to switch at 800 V, rather they switch at 600 V, thereby reducing the switching loss.

Fig. 3.19 shows the experimental waveforms with DPWM1 at 7.5 kW, 37.5 Hz both with constant V_{dc} (Fig. 3.19 (a)) and varying V_{dc} (Fig. 3.19 (b)). Efficiency with constant DC link voltage case is 97.1% while it is 98.15% for varying DC link voltage case with DPWM1 at 7.5 kW.

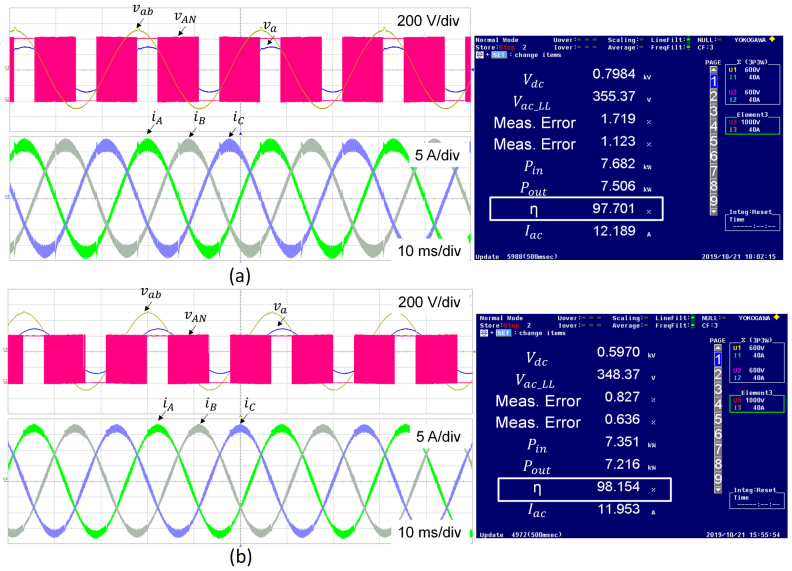

Figure 3.19: (a) Experimental Waveforms of Phase Voltage v_{AN}, Phase Voltage after the Filter v_{an}, Line to Line Voltage v_{ab} and Output Currents at 7.5 kW, 37.5 Hz with DPWM1 (a) Constant DC Link Voltage Case, $V_{dc} = 800$ V, (b) Varying DC Link Voltage Case, $V_{dc} = 600$ V

Fig. 3.20 shows the experimental results both for constant and varying DC link voltage cases with CSVPWM at 5 kW, 25 Hz. Again the efficiency of varying DC link voltage case is higher than constant DC link voltage case. The increase in efficiency is now even higher because at low power level of 5 kW, switching at high DC link voltage of 800 V incurs much more switching losses as compared to switching at just 400 V. Fig. 3.21 shows the similar set of results for DPWM1 wherein same conclusion is drawn for efficiency.

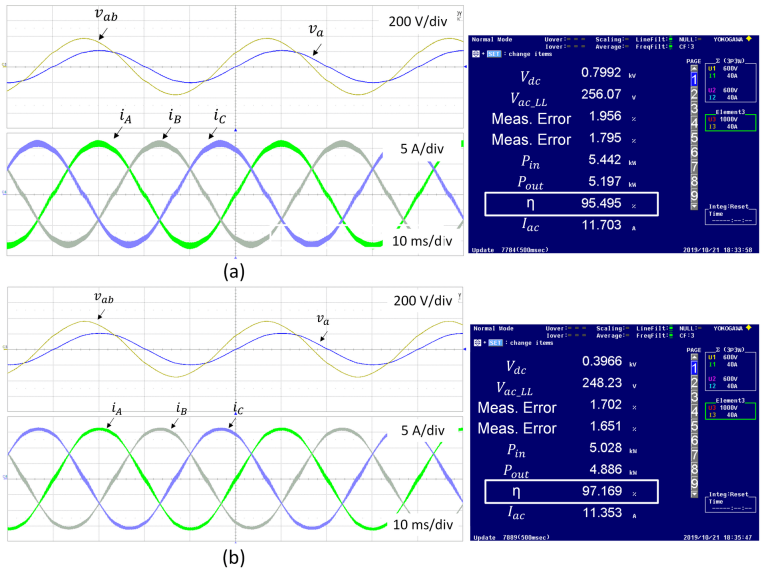

Figure 3.20: (a) Experimental Phase Voltage v_{an}, Line to Line Voltage v_{ab} after the Filter and Output Currents at 5 kW, 25 Hz with CSVPWM (a) Constant DC Link Voltage Case, $V_{dc} = 800$ V, (b) Varying DC Link Voltage Case, $V_{dc} = 400$ V

Fig. 3.22 shows the experimental results for 240CPWM at 7.5 kW, 37.5 Hz and 5 kW, 25 Hz. Efficiency of inverter with 240CPWM is the lowest for all test points. Fig. 3.23 shows the performance of 240CPWM at higher fundamental frequency of 100 Hz and 150 Hz. The dynamic DC link voltage shape is maintained decently even with open loop control of DC-DC converter at 150 Hz. Fig. 3.24 gives the loss breakdown of the inverter with CSVPWM, DPWM1 and 240CPWM at 10 kW and 5 kW. Fig. 3.25 shows the comparison of measured inverter efficiency with different modulation methods and DC-link voltage conditions. It is evident that the 240CPWM method has the highest efficiency over the tested operating range. At 10 kW, the inverter efficiency is 99.10% with 240CPWM while it is 98.39% with DPWM1 and 97.36% with CSVPWM. Since the conduction loss is influenced only marginally by the modulation method, it is the switching loss associated with different PWM methods that dictates the total loss and thus the efficiency of the drive. Switching loss for 240CPWM is 31W which is 6.8 times lower than CSVPWM with constant V_{dc} at

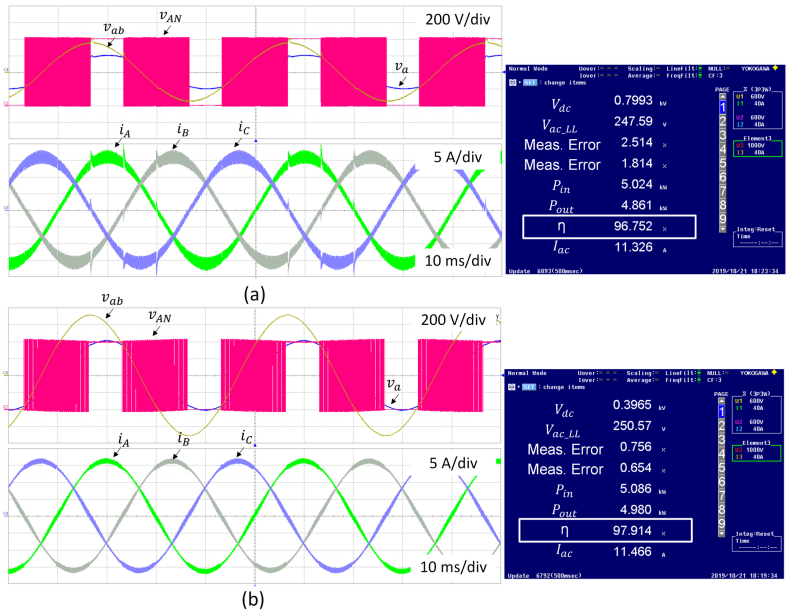

Figure 3.21: (a) Experimental Waveforms of Phase Voltage v_{AN}, Phase Voltage v_{an} and Line to Line Voltage v_{ab} after the Filter, and Output Currents at 5 kW, 25 Hz with DPWM1 (a) Constant DC Link Voltage Case, V_{dc} = 800 V, (b) Varying DC Link Voltage Case, V_{dc} = 400 V

50 Hz operation. Likewise, switching loss for 240CPWM is 12W which is 15.5 times lower than CSVPWM with constant V_{dc} at 25 Hz operation. This trend validates theoretically predicted switching loss.

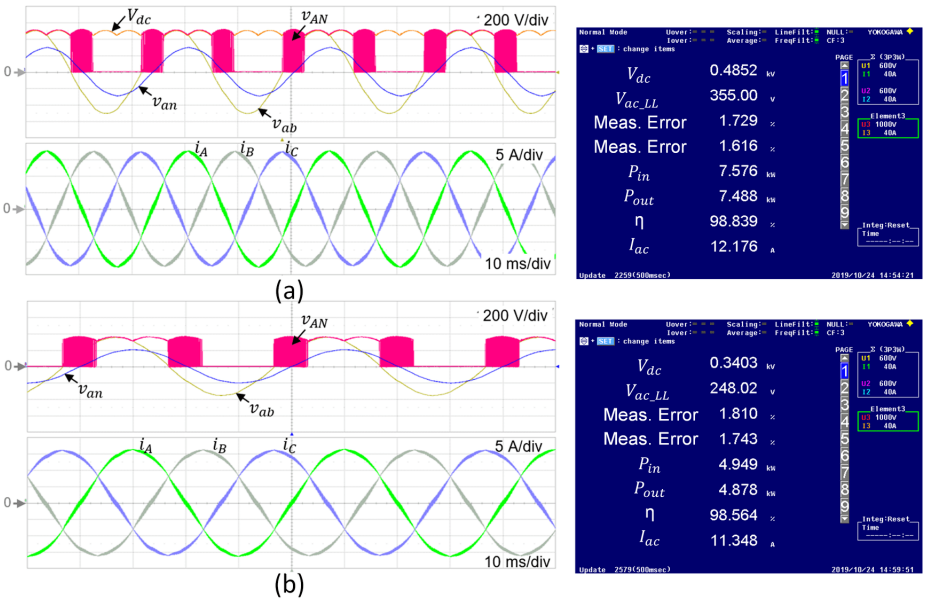

Figure 3.22: (a) Experimental Waveforms of Phase Voltage v_{AN}, Phase Voltage v_{an} and Line to Line Voltage v_{ab} after the Filter, and Output Currents (a) 7.5 kW, 37.5 Hz, (b) 5 kW, 25 Hz

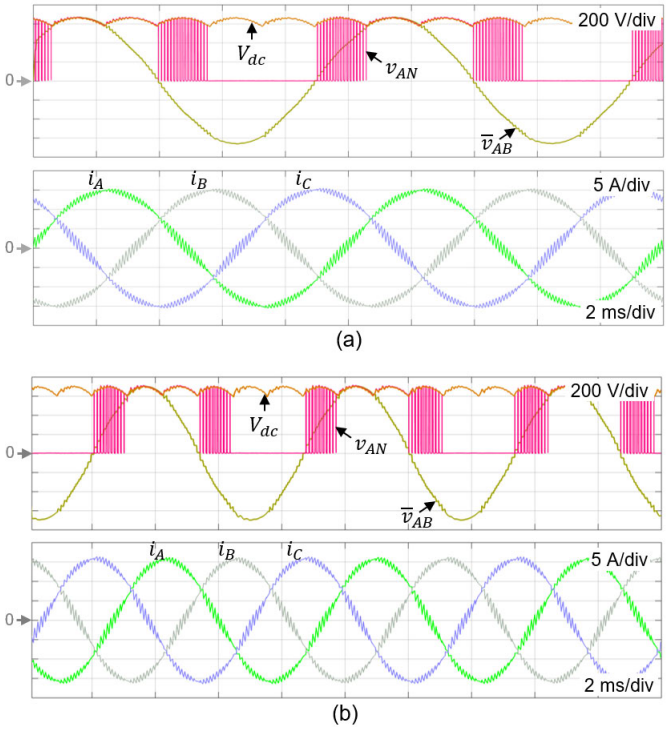

Figure 3.23: Experimental Waveforms with 240CPWM at 10 kW with Fundamental Frequency of (a) 100 Hz and (b) 150 Hz. $\overline{v}_{AB}$ Denotes the Switching cycle Average of v_{AB}.

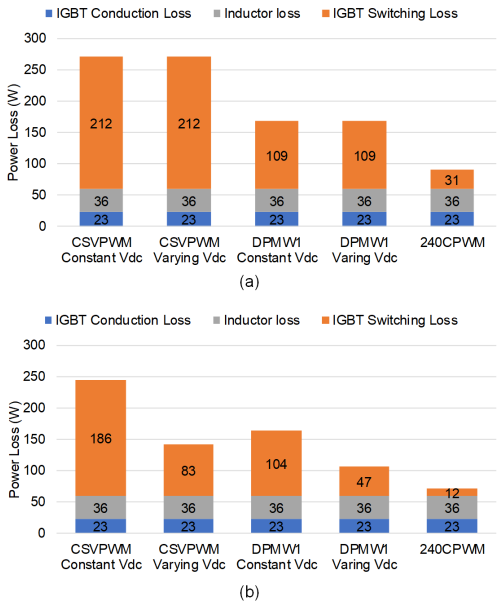

Figure 3.24: Loss Breakdown at (a) 50Hz, 10kW, (b) 25 Hz, 5kW

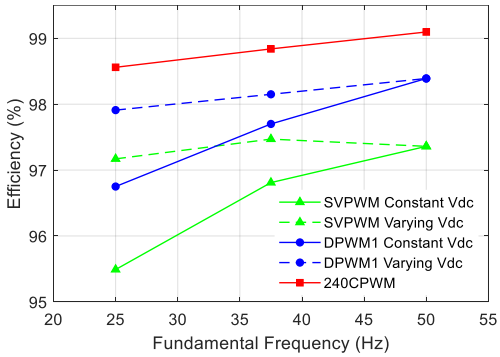

Figure 3.25: Comparison of Measured Inverter (DC-AC Stage) Efficiency under Different Modulation Methods and DC-link Voltage Conditions.

3.4 Comparison of 240CPWM with ABCPWM Methods

Advanced Bus Clamp PWM methods (ABCPWM) are the double switching and clamping sequences. In this section, ABCPWM methods are compared with 240CPWM in terms of switching loss for the sake of completeness.

3.4.1 Analysis of Switching Loss for ABCPWM Methods

Two of the most commonly used ABCPWM methods are Advanced Continual Clamp PWM (ACCPWM) and Advanced Split Clamped PWM (ASCPWM) methods shown in detail in Chapter 2. Fig. 3.26 shows the normalized switching phase voltage for ACCPWM and ASCPWM. The figure shows regions of double switching both for ACCPWM and ASCPWM.

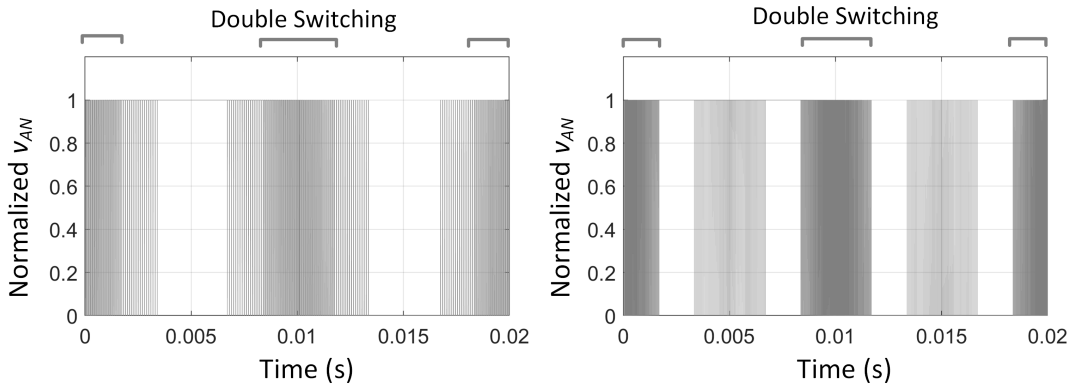

Figure 3.26: Normalized Switching Phase Voltage (a) ACCPWM and (b) ASCPWM (Normalized with respect to $V_{LL,pk}$).

The variation of $P_{SUB,PH}$ for ACCPWM and ASCPWM is presented at two different power factor angles in Fig. 3.27. For ACCPWM, the clamping is same as DPWM1, but there is a double switching of 120° in a line cycle for $\omega t \in [0°, 30°] \cup [150°, 210°] \cup [330°, 360°]$ near zero crossings of current (Fig. 3.27 (a)). Due to the double switching, averaged $P_{SUB,PH}$ for ACCPWM (i.e., 0.403) is slightly higher than DPWM1. At power factor angle of 30° (lagging), $P_{SUB,PH}$ for ACCPWM is higher than one at some instants due to double switching near current peaks (Fig. 3.27 (b)). For ASCPWM, the 120° clamping in a line cycle is for $\omega t \in [30°, 60°] \cup [120°, 150°] \cup [210°, 240°] \cup [300°, 330°]$ near current peaks while double switching is for $\omega t \in [0°, 30°] \cup [150°, 210°] \cup [330°, 360°]$ near zero crossings of current (Fig. 3.27 (c)).

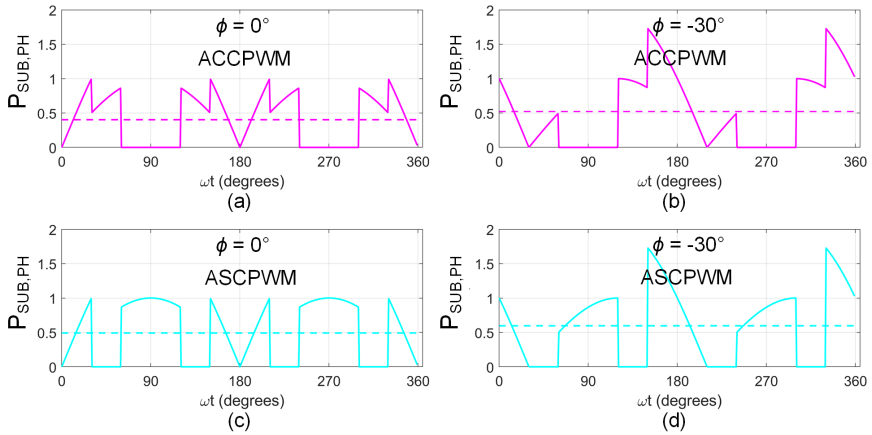

Figure 3.27: Variation of Normalized Local Switching Loss in Phase A over a Line Cycle $P_{SUB,PH}$ (a) ACCPWM, ϕ =0°, (b) ACCPWM, ϕ =-30°, (c) ASCPWM, ϕ =0°, (d) ASCPWM, ϕ =-30°

Fig. 3.28 shows the variation of $P_{SUB,TOT}$ at two different power factor angles for CSVPWM, DWPM1, ACCPWM, ASCPWM and 240CPWM. Finally, the variation of P_{SW} for all these PWM methods against fundamental frequency (for constant V/f mode of operation) is shown in Fig. 3.29. It is clear from Fig. 3.29 that switching loss for ASCPWM is higher than ACCPWM.

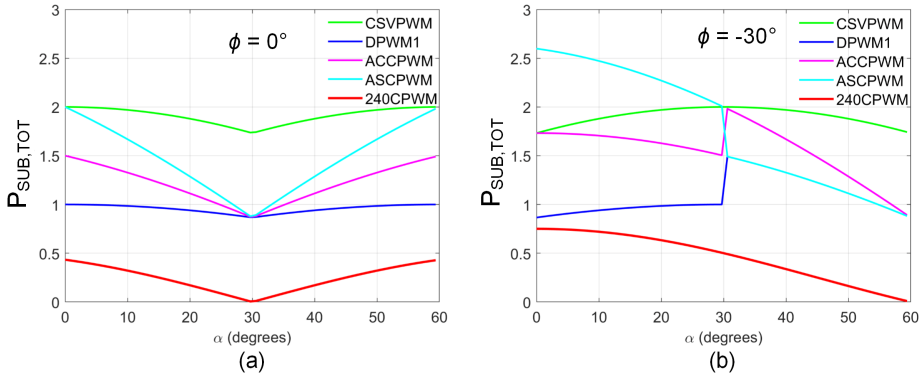

Figure 3.28: Variation of Normalized Total Switching Loss in a Sub-cycle over a Sector $P_{SUB,TOT}$ for Different PWM Methods (a) $\phi = 0°$, (b) $\phi = -30°$.

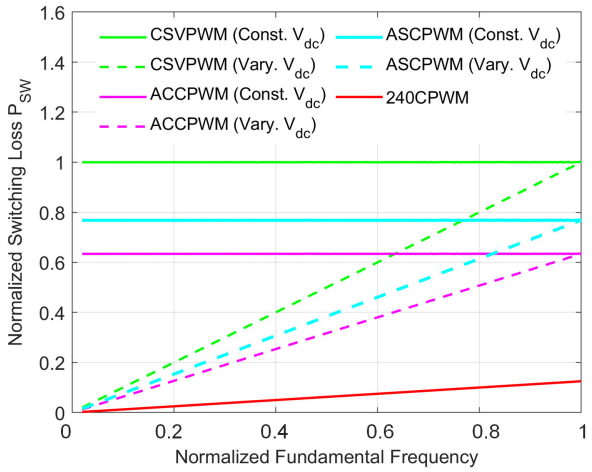

Figure 3.29: Variation of Normalized Switching Loss P_{SW} (Normalized with respect to CSVPWM) Against Normalized Fundamental Frequency (Normalized with respect to $f_{1,max}$ for Different PWM Methods at Unity Power Factor.

3.4.2 Experimental Validation of Switching Loss for ABCPWM Methods

The experimental results along with efficiency measurement at all test points will be presented for ACCPWM method only. The experimental results for ACCPWM at 10 kW, 7.5 kW and 5 kW for varying V_{dc} are presented in Fig. 3.30 (a), (b) and (c) respectively. Fig. 3.31 shows the efficiency at all test points with ACCPWM. The efficiency at 10 kW is 97.741% with ACCPWM. The results are consistent with the analytical discussions presented above.

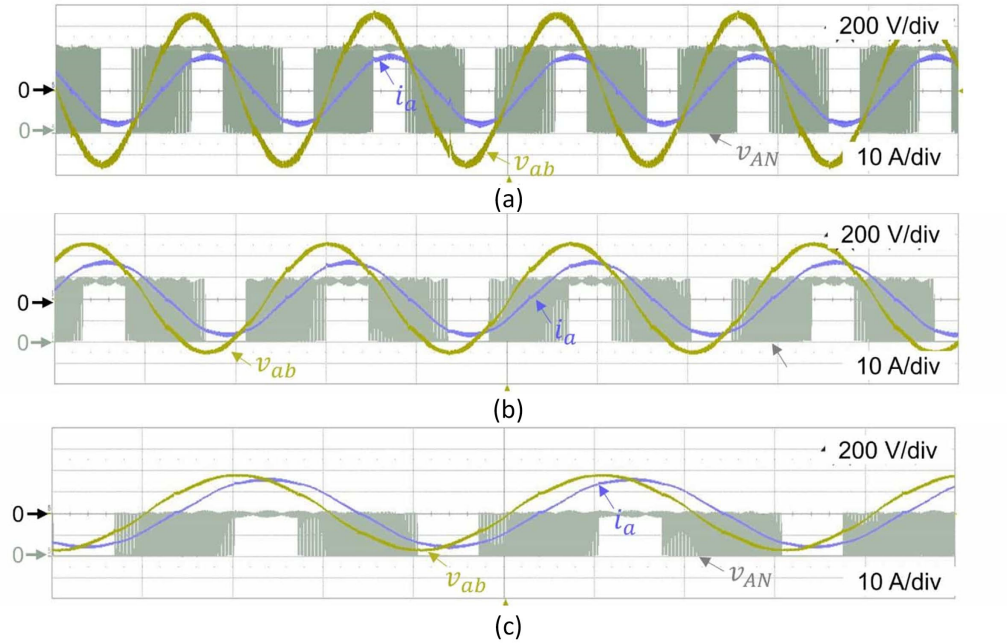

Figure 3.30: Experimental Waveforms of Phase Voltage v_{AN}, Line-to-Line Load Voltage v_{ab}, Load Current i_a for Varying V_{dc} Cases with ACCPWM (a) 10 kW, 50 Hz, (b) 7.5 kW, 37.5 Hz, (c) 25 kW, 25 Hz (time scale = 10 ms/div).

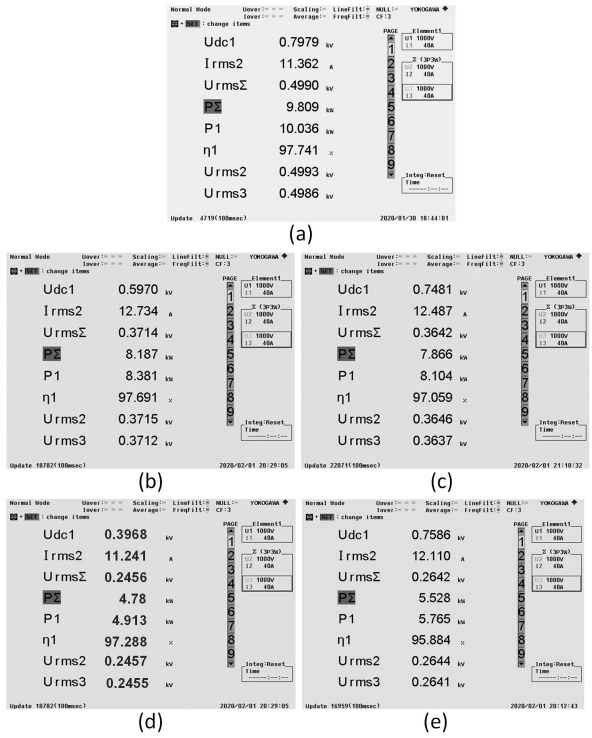

Figure 3.31: Efficiency Measurement Using Power Analyzer with ACCPWM (a) 10 kW, (b) 7.5 kW (Varying V_{dc}), (c) 7.5 kW (Constant V_{dc}), (d) 5 kW (Varying V_{dc}) and (e) 5 kW (Constant V_{dc})

Table 3.3: Efficiency Comparison from Experiments of All PWM Methods under Consideration

Power, Fund. Frequency	CSVPWM η (%)		DPWM1 η (%)		ACCPWM η (%)		240CPWM η(%)
	Const. V_{dc}	Vary. V_{dc}	Const. V_{dc}	Vary. V_{dc}	Const. V_{dc}	Vary. V_{dc}	
10 kW, 50 Hz	97.364	Same as Const. V_{dc}	98.39	Same as Const. V_{dc}	97.741	Same as Const. V_{dc}	99.1
7.5 kW, 37.5 Hz	96.8	97.469	97.7	98.154	97.059	97.691	98.839
5 kW, 25 Hz	95.495	97.169	96.752	97.914	95.884	97.288	98.564

Table 3.3 compares the efficiency results from experiments with all PWM methods under consideration at all test points. Highest efficiency of 99.1% is obtained with 240CPWM at 10 kW.

3.5 Switching Loss Analysis for Drive Cycles

Many driving cycles are available to test the performance of vehicle under different operating conditions and in different regions of the world e.g., European driving cycles, American driving cycles, Japanese driving cycles, Global harmonized driving cycle and Heavy duty test cycles etc. [64]. For this study, two American driving cycles will be used i.e., City driving cycle and Highway driving cycle shown in Fig. 3.32. The driving cycle data is obtained from Oak Ridge National Laboratory's Transportation Energy Databook [65]. These driving cycles are simulated in PLECS where the DC link voltage, fundamental frequency, and load resistance changes as per the given speed profile. In this simulation, constant V/f mode of operation is used, and load current is kept constant under all operating conditions. In PLECS simulations, time is reduced by factor of 100 because original time scale would take too long to run.

All PWM methods under consideration are analyzed for City and Highway driving cycles. The percentage saving in switching loss for 240CPWM with respect to CSVPWM are higher for city driving cycle as compared to highway driving cycle because vehicle runs at lower speeds (i.e., lower DC link voltage) for the most part in the

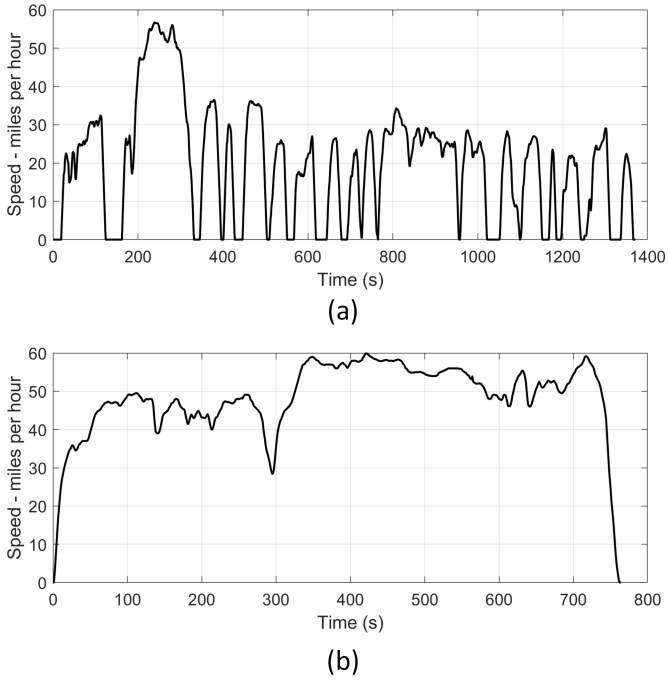

Figure 3.32: (a) City Driving Cycle, (b) Highway Driving Cycle

city as shown in Fig. 3.33. The results are summarized in Table 3.4. The percentage saving in normalized switching loss with 240CPWM as compared to CSVPWM with varying V_{dc} is 87.3% and 95.6% as compared to CSVPWM with constant V_{dc} in City driving cycle. The percentage saving in normalized switching loss with 240CPWM as compared to CSVPWM with varying V_{dc} is 87.3% and 89.7% as compared to CSVPWM with constant V_{dc} in Highway driving cycle.

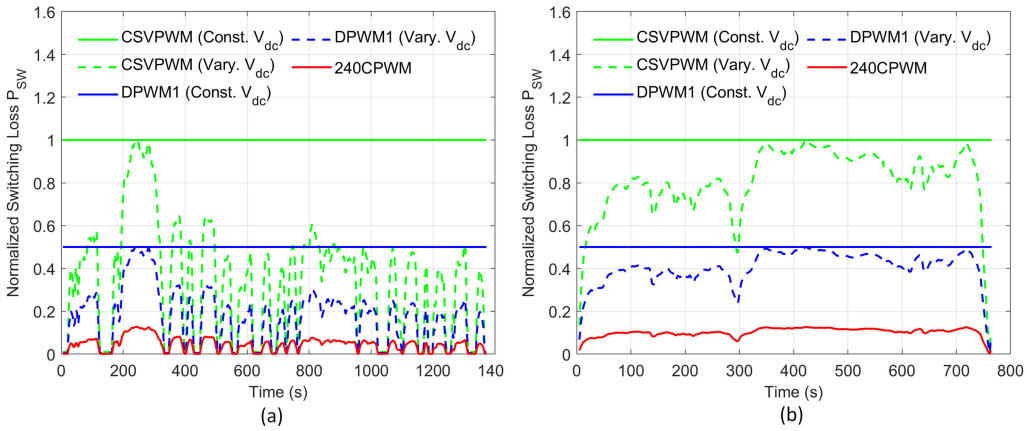

Figure 3.33: Switching Loss Analysis for all PWM Methods Under Consideration (a) City Driving Cycle and (b) Highway Driving Cycle.

Table 3.4: Switching Loss for City and Highway Driving Cycles

Driving Cycle	PWM Method (Varying V_{dc})	Normalized Switching Loss
City	CSVPWM	0.347
City	DPWM1	0.1740
City	240CPWM	0.0441
Highway	CSVPWM	0.813
Highway	DPWM1	0.4055
Highway	240CPWM	0.1029

3.6 Conclusion

240CPWM concept in cascaded architecture of DC-DC stage followed by three phase inverter is discussed in detail. Switching loss characteristics of 240CPWM are thoroughly studied and compared with CSVPWM, DPWM1 and ACCPWM both with constant and varying DC link voltage cases. Typical constant V/f mode of variable speed drives with constant load current is used to compare the characteristics

of different PWM methods, where the fundamental voltage is proportional to the fundamental frequency. Switching loss for 240CPWM is only 31 W which is 6.8 times lower than CSVPWM with constant V_{dc} at 10 kW, 50 Hz operation. Likewise, switching loss for 240CPWM is 12W which is 15.5 times lower than CSVPWM with constant V_{dc} at 5 kW, 25 Hz operation. Finally, to analyze the efficacy of 240CPWM in EV powertrains, switching loss analysis is extended for two standard driving cycles i.e., City and Highway driving cycles.

Chapter 4

DC LINK CAPACITOR SIZING FOR 240CPWM IN EV/HEV TRACTION INVERTERS

4.1 Introduction

Large DC link capacitors are used between DC-DC stage and traction inverter to deal with the following problems: (1) The ripple current due to switching of DC-DC stage and inverter stage, (2) Voltage spikes caused by leakage inductance and switching operations (3) Over voltage due to regeneration [66]. The capacitance value needed to limit the voltage ripple may not be very high, but current handling capability of the capacitor is a major concern. Electrolytic capacitors have high parasitic inductance, low RMS current handling capability and short lifetime [67]. They occupy almost 50% of the space in the traction inverter package and contribute to around 20% of its total cost [68]. Due to these reasons, use of electrolytic capacitors in newer commercial EVs is almost obsolete [69], [70], [58]. Film capacitors have emerged as the technology of choice for EVs due to low power loss, low parasitic inductance, low ESR, long life time and self-healing capability [67], [71]. Minimizing the DC link capacitance is an essential step towards meeting the ambitious power density targets of EVs and HEVs [67], [72]. For correct thermal design of the DC link capacitor, RMS value of current flowing through it i.e., I_{cap_rms} is of utmost importance. Bottleneck of capacitor's size is dictated by the current ripple requirement due to the existing capacitor manufacturing technology rather than voltage ripple requirement [73]. Various strategies have been proposed in the literature to reduce the DC link current ripple of HEV DC-DC converter and inverter systems [73]. Bang-

bang control for DC-DC converter is proposed in [74] to reduce the DC link capacitor current stress but it is not preferred because of complicated close-loop control. Reduction in DC link capacitor ripple in HEV converter inverter system is shown by optimizing the phase shift between the two carrier waveforms of dc-dc converter and inverter [75]. Optimized pulse pattern is used in four bidirectional boost converters to reduce the DC link capacitor current stress and compared with state of the art four phase interleaved boost converter [76]. Few PWM methods have been discussed in literature for AC-DC-AC systems for reducing the dc input current ripple which is the same as reducing the capacitance [77], [78]. This chapter explores the benefits of 240CPWM in terms of reducing the DC link capacitor current stress in a typical HEV/EV powertrain (shown in Fig.4.1). Analytical closed form expressions of RMS current in the DC link capacitor due to inverter stage only for CSVPWM are derived in [79] which is extended for 240CPWM in this chapter. Current drawn by the inverter is a strong function of modulation method used in the inverter which affects the DC link capacitor current inevitably.

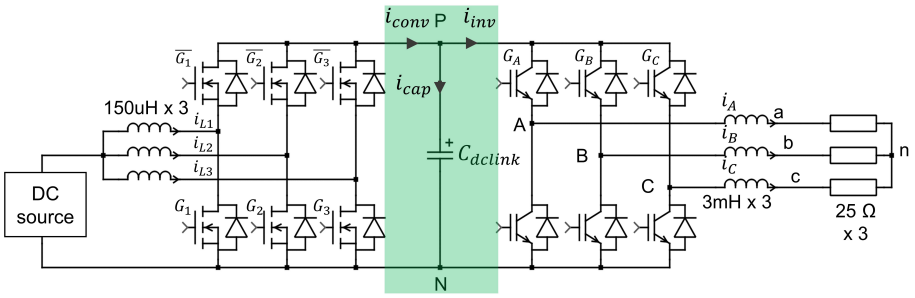

Figure 4.1: Illustration of the HEV/EV Powertrain (Cascaded Architecture) under Consideration.

4.2 Analysis of DC Link Capacitor Ripple

The DC link capacitor in cascaded topology sees current ripple both from DC-DC stage and DC-AC stage as shown in Fig. 4.1. DC link capacitor current is the

difference of current into the inverter stage (i_{inv}) from the current output of DC-DC stage (i_{conv}).

$$i_{cap} = i_{conv} - i_{inv} \tag{4.1}$$

Current ripple from DC-DC stage and DC-AC stages will be analyzed separately.

4.2.1 Current Ripple from DC-DC Stage

RMS value of current ripple in the DC link capacitor from DC-DC stage ($I_{cap\_rms\_dcdc}$) depends on duty cycle D, number of interleaved phases n, switching duration T_s, input current I_{in} and output current I_o. Variation of $I_{cap\_rms\_dcdc}$ is studied in three duty ratio intervals i.e. $0 < D < 1/n$, $1/n < D < (n-1)/n$ and $(n-1)/n < D < 1$ and the analysis is shown for these intervals in 4.2 (a), (b) and (c) respectively. When G1 is gated on and G2, G3 are gated off, $2I_{in}/3 - I_o$ flows into the DC link capacitor (time interval t_a in Fig. 4.2 (a)) and when all three switches are gated off, $I_{in} - I_o$ flows into the the DC link capacitor (time interval t_b in Fig. 4.2 (a)). So, the RMS value of ripple current in the DC link capacitor from DC-DC stage ($I_{cap\_rms\_dcdc}$) normalized with respect to output current I_o comes out to be as follows for $D < 0.333$

$$I_{cap\_rms\_dcdc} = \frac{1}{I_o}\sqrt{3(\frac{2I_{in}}{3} - I_o)^2 D + 3(I_{in} - I_o)^2(\frac{1}{3} - D)} \tag{4.2}$$

For $0.333 < D < 0.667$, when G1 and G3 are gated on, $I_{in}/3 - I_o$ flows in the DC link capacitor in time interval t_a and when G1 is gated on, $2I_{in}/3 - I_o$ flows in the DC link capacitor in time interval t_b (shown in Fig. 4.2 (b)). So, $I_{cap\_rms\_dcdc}$ in this interval is given as follows:

$$I_{cap\_rms\_dcdc} = \frac{1}{I_o}\sqrt{3(\frac{I_{in}}{3} - I_o)^2(\frac{3D-1}{3}) + 3(\frac{2I_{in}}{3} - I_o)^2(\frac{2-3D}{3})} \tag{4.3}$$

Similarly, for $D > 0.667$, when G1, G2 and G3 are gated on, $-I_o$ flows in the DC link capacitor in time interval t_a and when G1 and G3 are gated on, $I_{in}/3 - I_o$ flows in the DC link capacitor in time interval t_b (shown in Fig. 4.2 (c)). So, $I_{cap\_rms\_dcdc}$ in this interval is given as follows:

$$I_{cap\_rms\_dcdc} = \frac{1}{I_o}\sqrt{3(-I_o)^2(D - \frac{2}{3}) + 3(\frac{I_{in}}{3} - I_o)^2(1 - D)} \tag{4.4}$$

Variation of normalized $I_{cap\_rms\_dcdc}$ against duty ratio is shown in Fig. 4.3.

4.2.2 Current Ripple from DC-AC Stage

Contribution of current ripple to the DC-link capacitor from inverter stage can be evaluated by calculating the instantaneous current drawn by the inverter (i_{inv}). i_{inv} depends on the switching sequence of the inverter as well the line currents i.e.

$$i_{inv} = G_A i_A + G_B i_B + G_C i_C \tag{4.5}$$

Where G_A, G_B and G_C are the switching signals and i_A, i_B and i_C are the line currents of the inverter (defined in Fig. 4.1). i_{inv} for CSVPWM and 240CPWM is shown in Fig. 4.4 from PLECS simulation. Time durations of active states for 240CPWM (sequence 12-21 in Sector I) normalized with respect to sub-cycle duration T_s are given as follows:

$$T_1 = \frac{V_{REF}}{V_{dc}(t)} \frac{\sin(60^\circ - \alpha)}{\sin 60^\circ} T_s \tag{4.6}$$

$$T_2 = \frac{V_{REF}}{V_{dc}(t)} \frac{\sin \alpha}{\sin 60^\circ} T_s \tag{4.7}$$

where $V_{REF} = \sqrt{3}V_{LL,pk}/2$, $V_{dc}(t)$ is the dynamically varying DC link voltage, $V_{LL,pk}$ is the peak value of line to line voltage, α is the sector angle given by $\alpha = [(\omega t -$

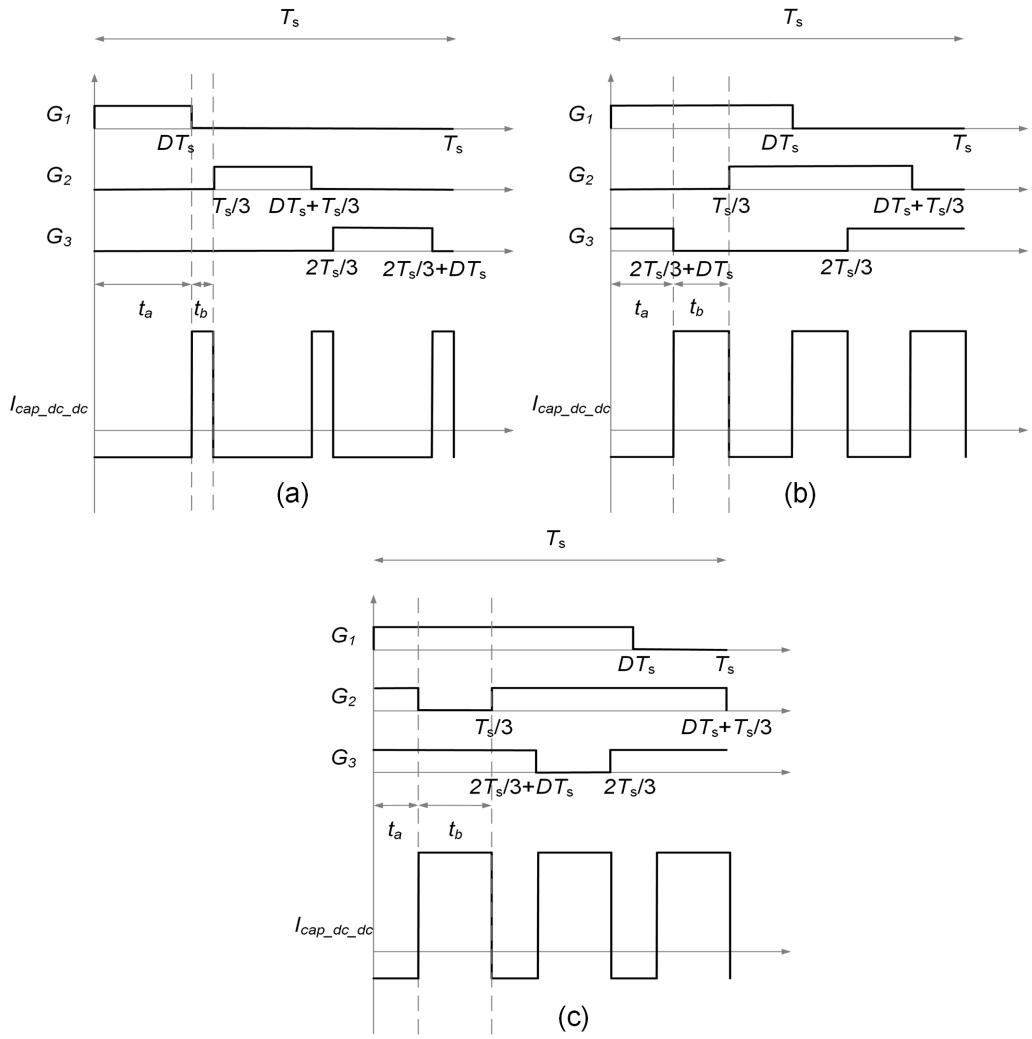

Figure 4.2: DC Link Capacitor Current Due to DC-DC stage (I_{cap_dcdc}) for (a) $D < 0.333$, (b) $0.333 < D < 0.667$, (c) $D > 0.667$.

90°) mod 60°], where $\omega = 2\pi f_1$ is the angular fundamental frequency. A zero-state duration T_z exists in CSVPWM which is given by $T_z = T_s - T_1 - T_2$ but it is nonexistent in 240CPWM.

Local RMS value of inverter input current can be expressed as:

$$i^2_{inv,rms} = \frac{2}{T_s} \int_0^{\frac{1}{2}T_s} i^2_{inv} \, \mathrm{d}t \tag{4.8}$$

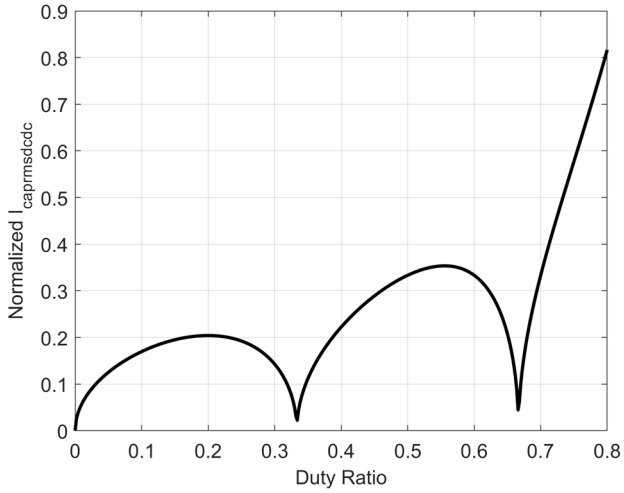

Figure 4.3: Variation of RMS Capacitor Current due to DC-DC stage ($I_{cap\_rms\_dcdc}$) Against Duty Ratio (Normalized with Respect to Output Current I_o).

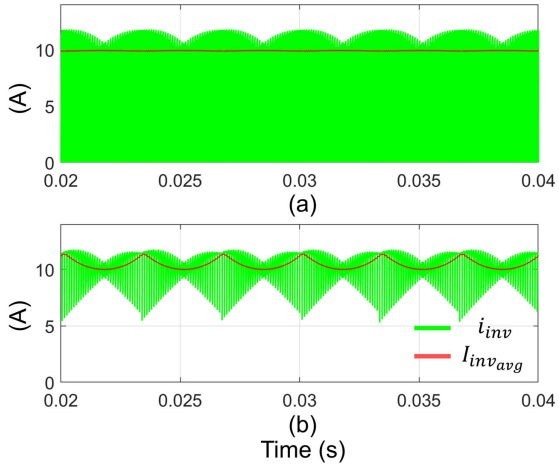

Figure 4.4: DC Link Current Drawn by the Inverter (i_{inv}) in a Fundamental Period (a) CSVPWM (b) 240CPWM

Zoomed in version of i_{inv} is shown in Fig. 4.5. RMS inverter input current can also be written as follows from Fig. 4.5, .

$$i_{inv,rms}^2 = T_1 i_A^2 + T_2 i_C^2 \tag{4.9}$$

$$I_{inv,rms}^2 = \frac{3}{\pi} \int_0^{\pi/3} i_{inv,rms}^2 \, \mathrm{d}\alpha \tag{4.10}$$

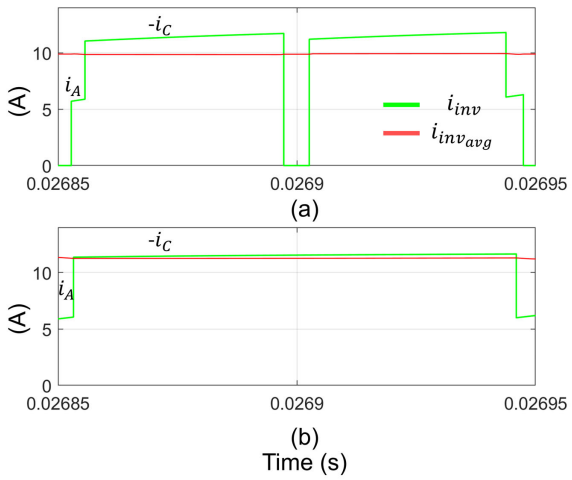

Figure 4.5: DC Link Current Drawn by the Inverter (i_{inv}) in a Switching Period (a) CSVPWM (b) 240CPWM

The local average value of inverter input current (related to pulse half period) is given by

$$i_{inv,avg} = \frac{2}{T_s} \int_0^{\frac{1}{2}T_s} i_{inv} \, \mathrm{d}t \tag{4.11}$$

which can also be expressed as

$$I_{inv,avg} = i_{inv,avg} = T_1 i_A - T_2 i_C \tag{4.12}$$

where $i_A = I_m \sin(\omega t - \phi)$, $i_B = I_m \sin(\omega t - \phi - \frac{2\pi}{3})$, $i_C = I_m \sin(\omega t - \phi + \frac{2\pi}{3})$ and I_m is the peak value of phase current and ϕ is the power factor angle.

It is shown in literature that RMS current ripple in the DC link capacitor due to inverter switching ($I_{cap\_rms\_dcac}$) is given by (4.13) [79]:

$$I_{cap\_rms\_dcac} = \sqrt{I_{inv,rms}^2 - I_{inv,avg}^2} \tag{4.13}$$

Fig. 4.6 shows the variation of normalized $I_{cap\_rms\_dcac}$ against normalized fundamental frequency. $I_{cap\_rms\_dcac}$ is normalized with respect to rms line current and fundamental frequency is normalized with respect to maximum fundamental frequency. $I_{cap\_rms\_dcac}$ remains constant for variable V_{dc} cases (both with CSVPWM

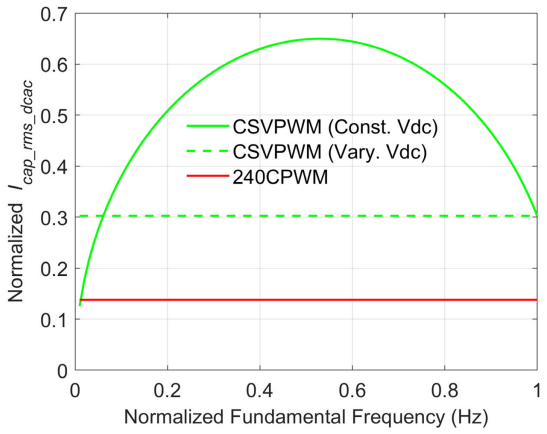

Figure 4.6: Variation of Normalized RMS Capacitor Current Due to Inverter Stage $I_{cap\_rms\_dcac}$ (Normalized with Respect to RMS Line Current. Fundamental Frequency is Normalized with Respect to Maximum Fundamental Frequency $f_{1,max}$)

and 240CPWM) because $I^2_{inv,rms}$ and $I^2_{inv,avg}$ change proportionally as per the DC link voltage. For constant V_{dc} case, average component of current drawn by the inverter i.e., $I_{inv,avg}$ increases with modulation index (or fundamental frequency). Therefore, according to (4.13), the maximum of $I_{cap\_rms\_dcac}$ occurs about in the middle of modulation range as shown in Fig. 4.6.

Finally, the total RMS DC link capacitor current due to DC-DC stage and inverter stage combined is given by

$$I_{cap\_rms} = \sqrt{I^2_{cap\_rms\_dcdc} + I^2_{cap\_rms\_dcac}} \tag{4.14}$$

Table 4.1 gives the individual current contribution to the DC link capacitor current from DC-DC stage and DC-AC stage for both PWM methods under consideration from analysis and PLECS simulation (Fig. 4.7 and 4.8).

Table 4.1: DC Link Capacitor Current Contribution from DC-DC Stage and DC-AC Stage at 500 V, 5 kW at m_{Max} from Analysis and Simulations

PWM Method	Analysis			Simulation		
	$I_{cap\_rms\_dcdc}$ (A)	$I_{cap\_rms\_dcac}$ (A)	I_{cap_rms} (A)	$I_{cap\_rms\_dcdc}$ (A)	$I_{cap\_rms\_dcac}$ (A)	I_{cap_rms} (A)
CSVPWM	2.9	2.9	4.1	2.93	2.744	4.18
240CPWM	3	1.2	3.23	2.95	1.117	3.2

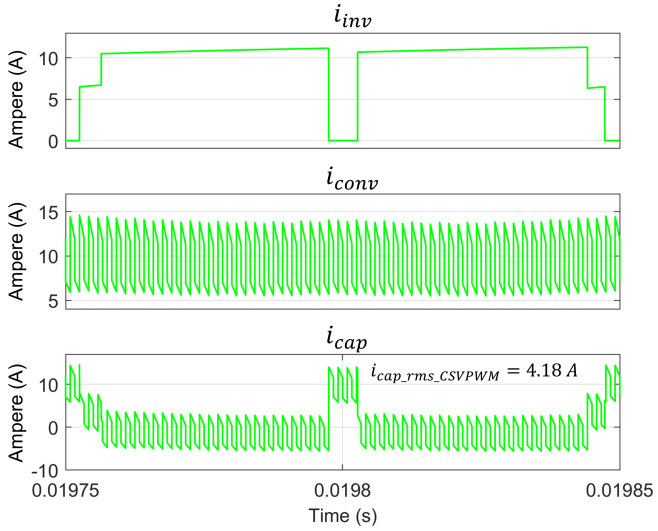

Figure 4.7: Simulation Results of DC Link Capacitor Current for CSVPWM near Peak Inverter Current at 5 kW (RMS Value Calculated over Fundamental Period).

Fig. 4.7 and 4.8 show the I_{cap_rms} (from simulation) for CSVPWM and 240CPWM under same operating conditions at 5 kW respectively. I_{cap_rms} for 240CPWM is 25% lower than CSVPWM.

4.3 Experimental Validation

The experimental setup is tested at 5 kW for CSVPWM and 240CPWM to verify the current stress on DC link capacitor. The DC-AC stage is a three-phase inverter with Si-IGBTs switching at 10 kHz. A series connected resistive-inductive load is used to emulate a motor load at nearly unity power factor. The DC-DC stage is a

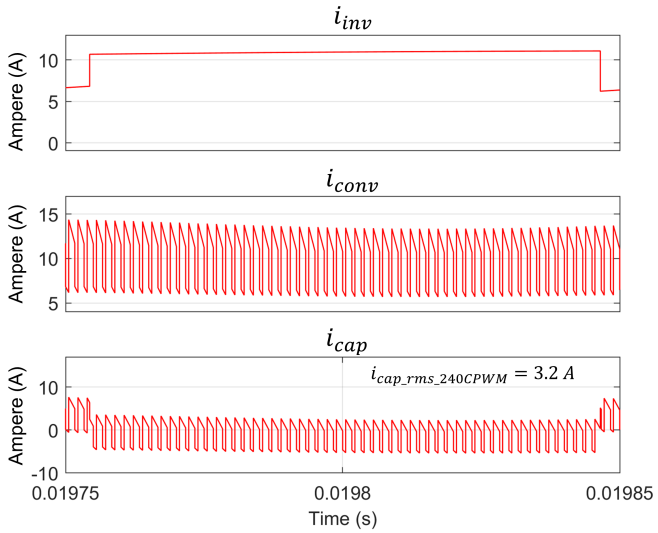

Figure 4.8: Simulation Results of DC Link Capacitor Current for 240CPWM near Peak Inverter Current at 5 kW (RMS Value Calculated over Fundamental Period).

three-phase interleaved Buck/Boost converter. The switching frequency of DC-DC stage is 200 kHz. Table 4.2 gives the specifications of hardware prototype. Direct measurement of DC link capacitor current is not possible in the current setup. First, output current of DC-DC stage i.e. i_{conv} is obtained from switching pulses of top switches and inductor currents of DC-DC stage as follows:

$$i_{conv} = \overline{G_1} i_{L1} + \overline{G_2} i_{L2} + \overline{G_3} i_{L3} \tag{4.15}$$

The current into the inverter stage i.e. i_{inv} is probed directly from the hardware setup. Then the difference of i_{inv} from i_{conv} generates the DC link capacitor current i_{cap}. The DC link capacitor currents obtained from experimental setup for CSVPWM and 240CPWM are shown in Fig. 4.9 and 4.10 respectively (post-processed in MATLAB using measured inductor currents and gate signals from hardware prototype). The hardware results for 240CPWM are commensurate with the analysis and simulation results under same operating conditions. The slight discrepancy in I_{cap_rms} for CSVPWM is because the modulation index for CSVPWM in experimental setup is

Table 4.2: Specifications of Hardware Prototype

Parameters	Values
DC-DC Stage	
Output Power P	5 kW
Input Voltage V_{in}	270 V
Output Voltage V_o	500 V
Duty Ratio D	0.46
Number of interleaved phases n	3
Inductance L_{dc}	150 uH
Resistance of Inductor r_L	20 mΩ
DC Link Capacitance C_{dc}	4.7 uF
ESR of DC Link Capacitor R_{ESR}	10 mΩ
Switching frequency $f_{sw,dcdc}$	200 kHz
DC-AC Stage	
Switching frequency $f_{sw,dcac}$	10 kHz
Load Resistance R_L	25 Ω
Inductance L_{ac}	3 mH
Modulation Index for CSVPWM M_i	$0.9M_{max}$
Modulation Index for 240CPWM M_i	M_{max}

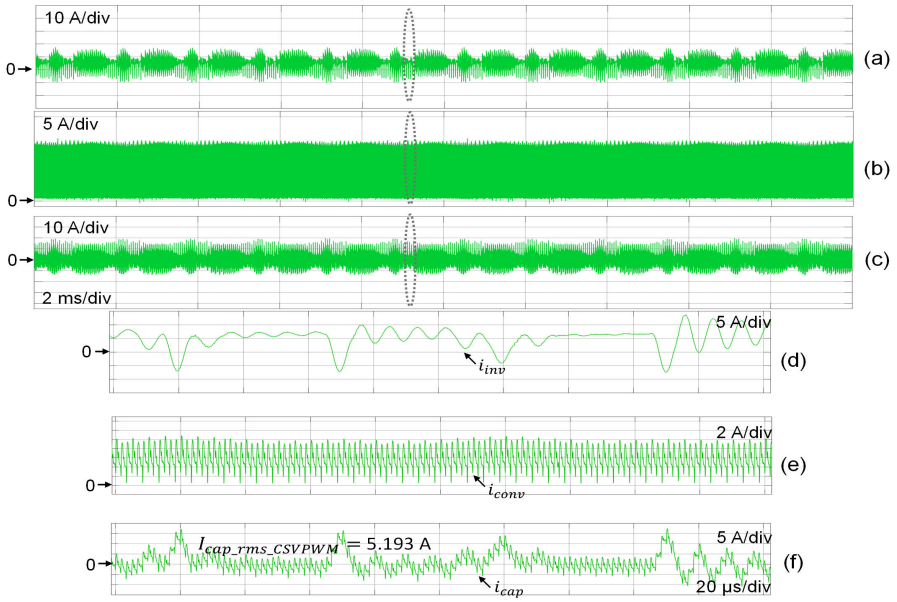

Figure 4.9: Experimental Results of DC Link Capacitor Current at 500 V, 5 kW for CSVPWM (a) i_{inv}, (b) i_{conv}, (c) i_{cap}, (d) Zoomed in i_{inv}, (e) Zoomed in i_{conv}, (f) Zoomed in i_{cap}

0.9 times the maximum modulation index (considering large dead time of Si IGBTs). When modulation index is maximum in CSVPWM, duration of applied zero states is minimum, thus DC-DC converter output current (i_{conv}) is dumped into the DC link capacitor for very small duration. When modulation index is reduced to $0.9M_{max}$ for CSVPWM, duration of applied zero states is increased. Thus, the duration for which i_{conv} is dumped into the DC link capacitor is increased leading to high I_{cap_rms}.

Now experimental results of DC link current stress at nominal power of 10 kW will be presented. DC link current stress at 10 kW, 7.5 kW and 5 kW will be shown both with CSVPWM and DPWM1 in order to verify the analysis in Fig. 4.6 as per the constant V/f mode of operation.

Fig. 4.11 shows the DC link capacitor current i_{cap} at 10 kW both for CSVPWM and 240CPWM. The figure shows the zoomed in version also to elaborate that with 240CPWM, variation in i_{cap} is reduced leading to low I_{cap_rms} i.e., 4.9 A as compared to CSVPWM (7.6 A).

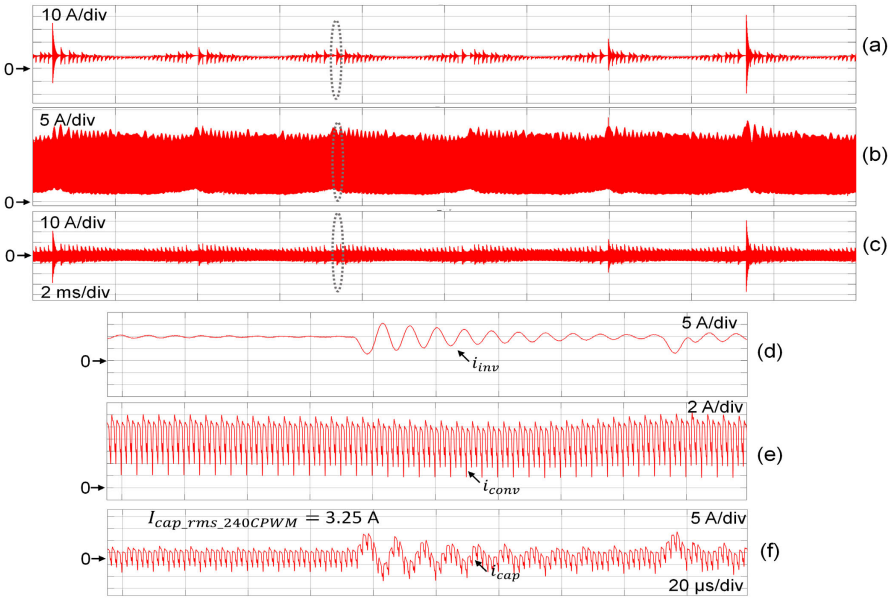

Figure 4.10: Experimental Results of DC Link Capacitor Current at 460 V, 5 kW for 240CPWM (a) i_{inv}, (b) i_{conv}, (c) i_{cap}, (d) Zoomed in i_{inv}, (e) Zoomed in i_{conv}, (f) Zoomed in i_{cap}

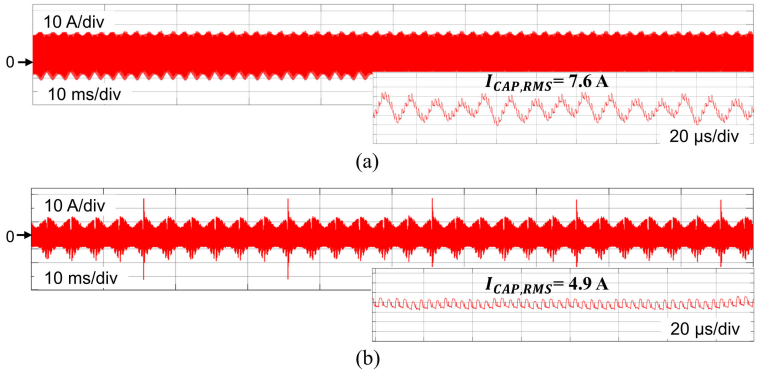

Figure 4.11: Experimental Results of DC Link Capacitor Current at 10 kW for (a) CSVPWM. (b) 240CPWM

i_{cap} for CSVPWM and 240CPWM at 7.5 kW (constant DC link voltage case) is shown in Fig. 4.12. As expected from the analysis, percentage saving in I_{cap_rms} for 240CPWM in this case is higher than 10 kW. It is because at 7.5 kW (for constant V_{dc} case), modulation index is 75% of the maximum modulation index which leads to higher duration of zero states for CSVPWM. This causes higher current stress on the DC link capacitor.

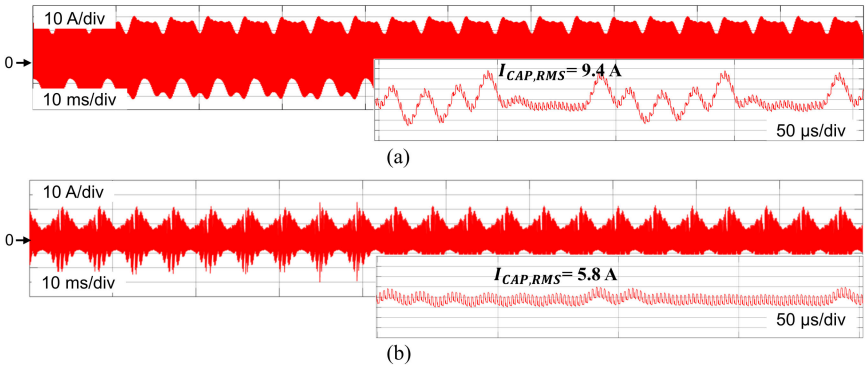

Figure 4.12: Experimental Results of DC Link Capacitor Current at 7.5 kW with Constant V_{dc} for (a) CSVPWM. (b) 240CPWM

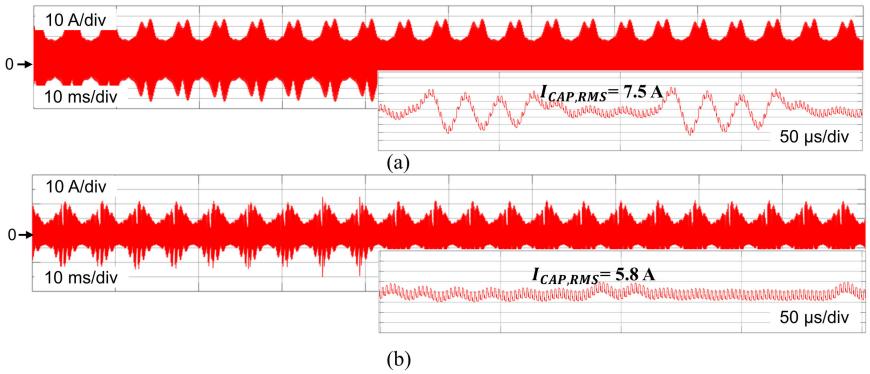

Figure 4.13: Experimental Results of DC Link Capacitor Current at 7.5 kW with Varying V_{dc} for (a) CSVPWM. (b) 240CPWM

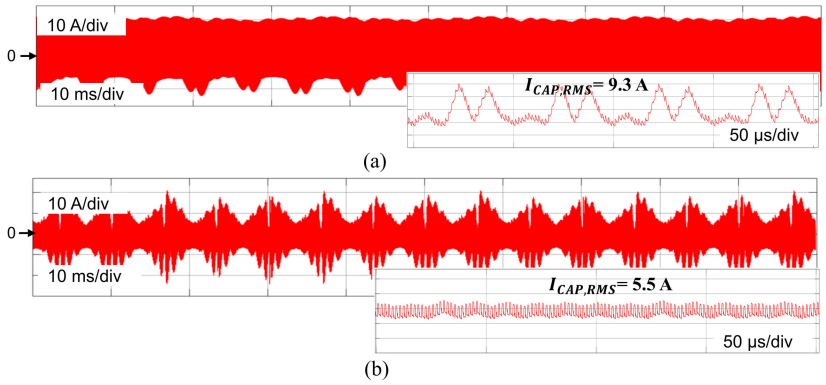

Figure 4.14: Experimental Results of DC Link Capacitor Current at 5 kW with Constant V_{dc} for (a) CSVPWM. (b) 240CPWM

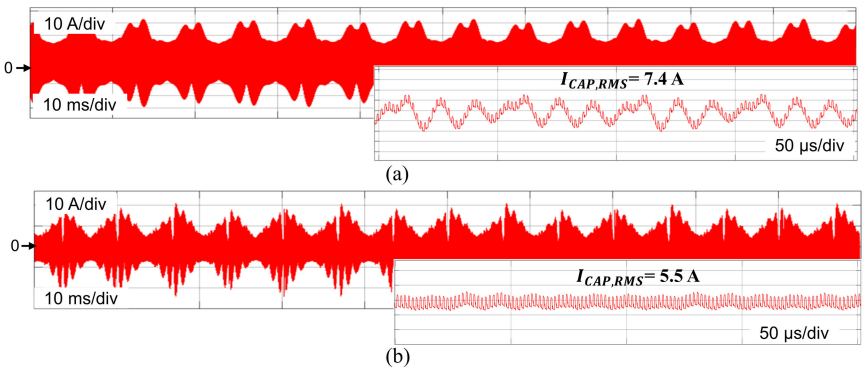

Figure 4.15: Experimental Results of DC Link Capacitor Current at 5 kW with Varying V_{dc} for (a) CSVPWM. (b) 240CPWM

4.4 Conclusion

Current stress on the DC link capacitor is analyzed and experimentally verified for 240CPWM with CSVPWM as a benchmark. Due to the elimination of zero states in 240CPWM, variation in current drawn by the inverter (i_{inv}) is reduced. Since the difference of i_{conv} and i_{inv} flows into the DC link capacitor, the variation in DC link capacitor current is also reduced leading to low I_{cap_rms} with 240CPWM. 240CPWM used in DC-AC stage helps to reduce I_{cap_rms} to 3.25 A at 5 kW (Modulation index $=M_{max}$) as compared to 5.193 A for CSVPWM (Modulation index $= 0.9M_{max}$), thus smaller DC link capacitor can be used for 240CPWM. Experimental results match with the analysis and simulations.

Chapter 5

CLOSE LOOP CONTROL FOR DYNAMIC DC LINK VOLTAGE CONTROL WITH 240CPWM

5.1 Introduction

Latest EVs and HEVs use high speed motors with speeds ranging from 6000 rpm to 17000 rpm (which translates to high fundamental frequency) depending upon number of poles in motor and the DC link voltage [56]. The DC link voltage required for 240CPWM has a dominant component at six times the fundamental frequency ($6f_1$) and some higher order harmonics. The frequency spectrum of the reference dynamic DC-link voltage is shown in Fig. 5.1. Hence, the DC-DC stage responsible for the DC link voltage control must have a robust control that can effectively track $6f_1$ DC link voltage. In [80], a multiloop feedback linearized control strategy is used to control the DC link voltage. However, the control method discussed is very complex and the input current ripple at inverter switching frequency is ignored. In [81] and [82], the DC link voltage is controlled in open loop fashion and the results are shown for maximum fundamental frequency of 100 Hz and 150 Hz respectively. Traditional voltage controller or simple open loop controller can no longer track the DC link voltage at high fundamental frequencies. In this chapter, a well-established dual loop controller is discussed that reduces the input current ripple, improves the DC link voltage waveshape along with comparable THD in line currents even at high fundamental frequencies as compared to open loop control. Then voltage mode control with Smith Predictor is designed to control the dynamic DC link voltage with 240CPWM that gives further improvement in terms of THD in line currents.

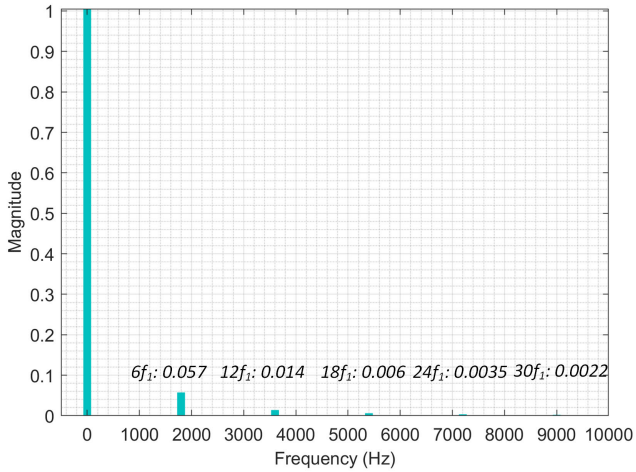

Figure 5.1: Normalized Frequency Spectrum of Reference Dynamic DC-link Voltage (Normalized with respect to the DC Component)

5.2 Design of Dual Loop Control

Fig. 5.2 shows the block diagram of dual loop control in cascaded architecture of DC-DC stage followed by DC-AC stage. In dual loop control, outer voltage loop and inner current are used for controlling the dynamic DC-link voltage. In this section, dual loop control is designed to track the fast variations in dynamic DC link voltage with fundamental frequency as high as 300Hz. The dynamic DC link voltage is generated by the front-end DC-DC stage. The expression for the dynamic DC link voltage reference can be equivalently given as:

$$V_{dc,ref} = \max\{v_a, v_b, v_c\} - \min\{v_a, v_b, v_c\} \tag{5.1}$$

where v_a,v_b and v_c are the reference phase voltages.

DC-DC converter in motor drives is normally a boost converter or its variant [60]. Bandwidth of its voltage control loop is limited by a right half plane (RHP) zero [83]. So, voltage control alone is not sufficient to track the dynamic DC link voltage which is required for 240CPWM. This work makes use of a well-established dual loop control for DC-DC converter that gives precise tracking of dynamic DC

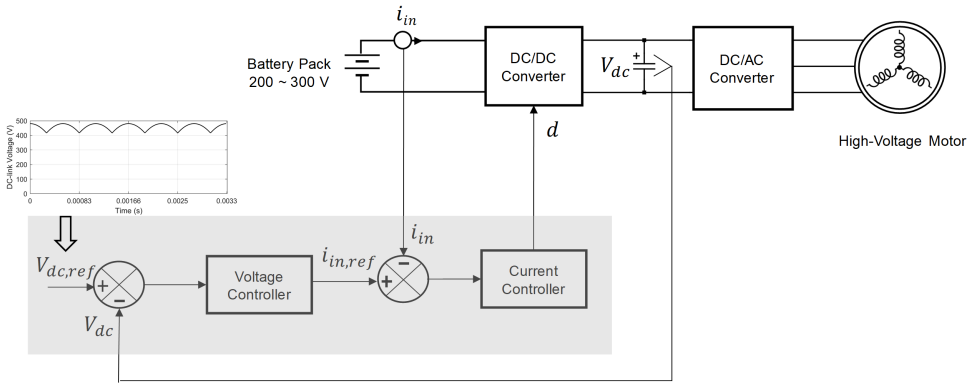

Figure 5.2: Dual Loop Control for Controlling the Dynamic DC-link Voltage in DC-DC converter

link voltage with 240CPWM. The outer loop with low bandwidth regulates the DC link voltage and the inner loop is the input current control loop with high bandwidth that improves the dynamic performance. Boost converter and other similar topologies suffer from inherent issue of RHP zero in control to output voltage transfer function that poses limitations in terms of maximum achievable control loop bandwidth. This zero makes the stabilization of the system considerably difficult. Higher switching frequency allows the use of smaller inductors, thereby pushing RHP zero further away that allows more control freedom. However, due to low efficiency of such converters at high switching frequency, a trade-off has to be made between efficiency and control bandwidth. n phase interleaved boost converter shifts the RHP zero to n times the RHP zero of a single phase converter. RHP zero of interleaved boost converter is given by $n(1-D)^2 R_L/L_{dc}$, where n is the number of interleaved phases, D is the duty ratio, R_L is the load resistance and L_{dc} is the inductance of DC-DC converter. Worst case RHP zero for the DC-DC boost converter with specifications shown in Table 5.1 comes out to be 35 kHz. As a rule of thumb, bandwidth of the controller is limited to one tenth of the RHP zero. So, the maximum achievable bandwidth for outer voltage loop is around 3.5 kHz.

Plant transfer functions of both the outer voltage loop (G_{vi}) and inner current

Table 5.1: Specifications of DC-DC Stage in Hardware Prototype

Parameters	Values
Output Power P	3 kW
Input Voltage V_{in}	180 V
Output Voltage V_o	410 V
Duty Ratio D	0.56
Number of interleaved phases n	3
Inductance L_{dc}	150 uH
DC resistance of Inductor R_{dc}	20 mΩ
DC Link Capacitance C_{dclink}	5 uF
Equivalent Series Resistance R_{ESR}	10 mΩ
Load Resistance R_L	56 Ω
Switching Frequency $f_{sw,dcdc}$	200 kHz

loop (G_{id}) are required to design the respective controllers (G_{cv}) and (G_{ci}). The expressions of plant transfer functions, duty to voltage (G_{vd}) and duty to current (G_{id}) for n phase interleaved boost converter are given below.

$$G_{vd} = \frac{v_o}{d} = \frac{V_o}{1-D} \frac{(1 - s\frac{L_e}{R_L})(1 + sC_{dclink}R_{ESR})}{1 + s(\frac{L_e}{R_L} + C_{dclink}R_{ESR}) + s^2 L_e C_{dclink}(1 + \frac{R_{ESR}}{R_L})} \tag{5.2a}$$

$$L_e = \frac{L_{dc}}{n(1-D)^2} \tag{5.2b}$$

$$G_{id} = \frac{i_{in}}{d} = T_{pix}\frac{s + w_{zi}}{s^2 + 2\omega_n\xi s + \omega_n^2} \tag{5.3a}$$

$$T_{pix} = \frac{nV_o(R_L + 2R_{ESR})}{L_{dc}(R_L + R_{ESR})} \tag{5.3b}$$

$$\omega_{zi} = \frac{1}{C_{dclink}(\frac{R_L}{2} + R_{ESR})} \tag{5.3c}$$

$$\omega_n = \sqrt{\frac{n(1-D)^2R_L + R_{dc}}{L_{dc}C_{dclink}(R_L + R_{ESR})}} \tag{5.3d}$$

$$\xi = \frac{C_{dclink}[R_{dc}(R_L + R_{ESR}) + nR_LR_{ESR}(1-D)^2] + L_{dc}}{2\sqrt{L_{dc}C_{dclink}(R_L + R_{ESR})[R_{dc} + n(1-D)^2R_L]}} \tag{5.3e}$$

Finally, G_{vi} is obtained from the ratio of G_{vd} and G_{id}.

$$G_{vi} = \frac{G_{vd}}{G_{id}} \tag{5.4}$$

k-method control is used to design the controllers. Transfer function of k-method controller is given by:

$$G_c(s) = \frac{K_c}{s}\frac{(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_p})} \tag{5.5}$$

where K_c is the controller gain, ω_z and ω_p are the locations of controller zero and pole respectively.

Due to the limitation of RHP zero explained above, bandwidth of outer voltage loop is kept as 3 kHz whereas for inner current loop, bandwidth is usually kept around one tenth of the switching frequency which corresponds to 20 kHz in our setup. Bandwidth of inner current loop is chosen as 15 kHz. k-factor method is used to design both the controllers that gives precise control in terms of required bandwidth and phase margin [84]. Both the controllers are designed for phase margin of 60°.

Fig. 5.3 shows the bode plots of inner current loop and its loop gain wherein phase margin of 60° and bandwidth of 15 kHz can be observed. And Fig. 5.4 shows

Table 5.2: Controller Parameters for Outer Voltage and Inner Current Loop

Controller Parameters	Outer Voltage Loop G_{cv}	Inner Voltage Loop G_{ci}
K_c	1836	200
w_z	8703 rad/s	23799 rad/s
w_p	40822 rad/s	373231 rad/s

the bode plots of outer voltage loop and its loop gain wherein phase margin of 60° and bandwidth of 3 kHz can be observed.

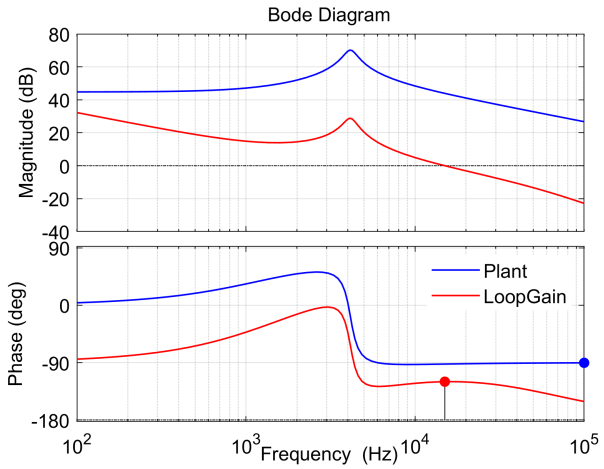

Figure 5.3: Bode Plot Analysis of Inner Current Loop

To verify the plant response obtained from analysis and simulations, network analyzer (Bode 100) is used in the experimental setup. Plant responses for current and voltage loop are measured for very low power level (V_{in} = 15V and V_o = 30V) and compared with the analytical plant responses at same operating conditions as shown in Fig. 5.5. The experimental plant responses match very well with the analytical ones. The steep fall in phase after 10 kHz in experimental responses is because of the delay introduced due to DSP processing time and RC filters in the experimental setup. Same delay is incorporated in the analysis by adding the delay G_{del}=e^{-sT_d},

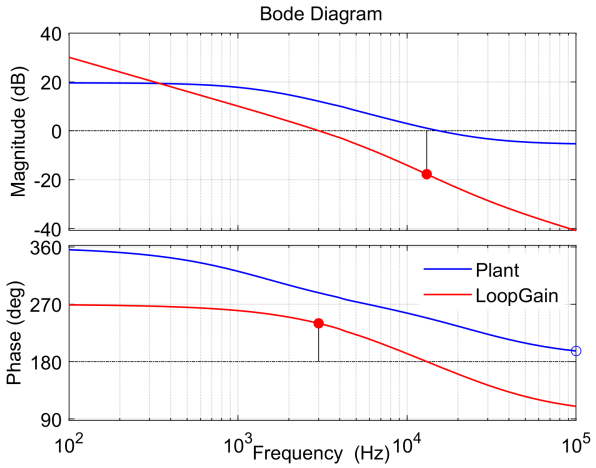

Figure 5.4: Bode Plot Analysis of Outer Voltage Loop

where $T_d = 1/f_{sw}$. High noise at very high frequencies in G_{id} (Fig. 5.5 (a)) is observed because sensed current (i_{in}) is used in network analyzer for this response. HLSR 50-P current sensor is used that gives very low output voltage ranging from 1.5 to 3 V corresponding to the sensed current. Moreover, it has a bandwidth of 400 kHz that allows high frequency noise in the G_{id} response. The response for G_{vd} (Fig. 5.5 (b)) is very clean because actual output voltage (V_o) is used in the network analyzer, hence sensor noise is bypassed.

5.3 Simulation Results and Experimental Validation

Simulation and experimental results with dual loop control and their comparison with open loop control is carried out in this section.

5.3.1 Steady State Performance

Simulation results of both the open loop control and dual loop control at 200 Hz, 3 kW are shown in Fig. 5.6. With dual loop control, DC link voltage is very smooth and ripple in input current is also reduced. Same set of waveforms are shown in Fig.

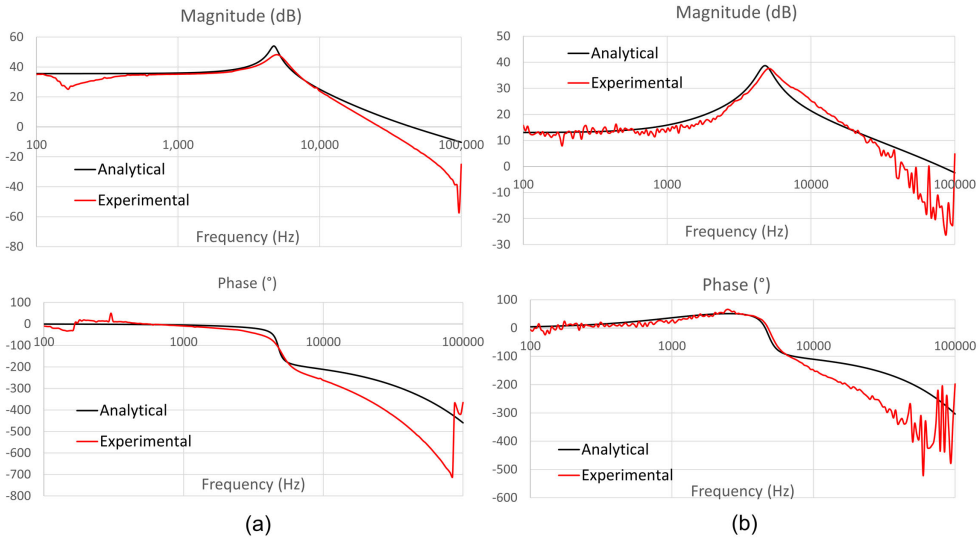

Figure 5.5: Analytical and Experimental Bode Plots (a) G_{id}, (b) G_{vd}

5.7 from experiments and similar conclusions are drawn from them.

The DC link voltage and input current are also shown for fundamental frequency of 300 Hz both in open and close loop control in Fig. 5.8 and Fig. 5.9 from PLECS simulation and experiments respectively. Now the difference between open loop and dual loop control is more pronounced because of higher fundamental frequency. This is because open loop control can not track very fast variations in dynamic DC link voltage that are at 1800 Hz ($6f_1$) corresponding to 300 Hz fundamental frequency.

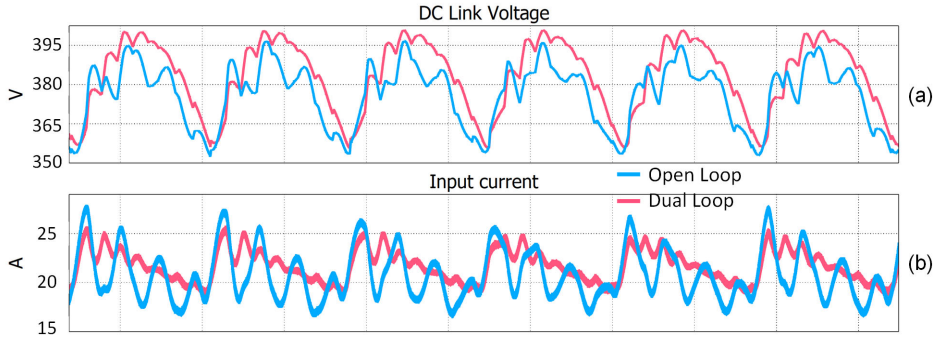

Figure 5.6: Comparison of Dual Loop Control with Open Loop Control at 200 Hz, 3 kW (a) Dynamic DC Link Voltage, (b) Input Current from PLECS Simulation

Fig. 5.10 shows the FFT of input current both for open and dual loop control

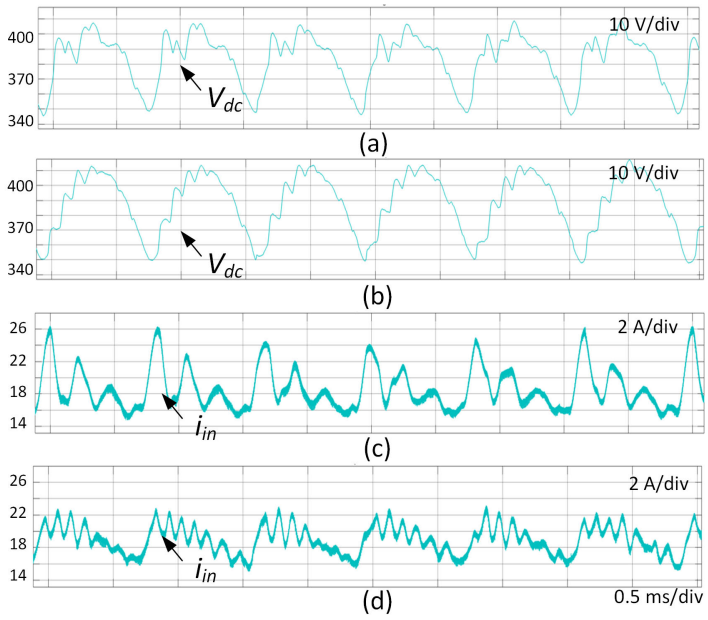

Figure 5.7: Experimental Waveforms at 200 Hz, 3 kW. DC Link Voltage (a) Open Loop Control, (b) Dual Loop Control, Input Current (c) Open Loop Control, (d) Dual Loop Control

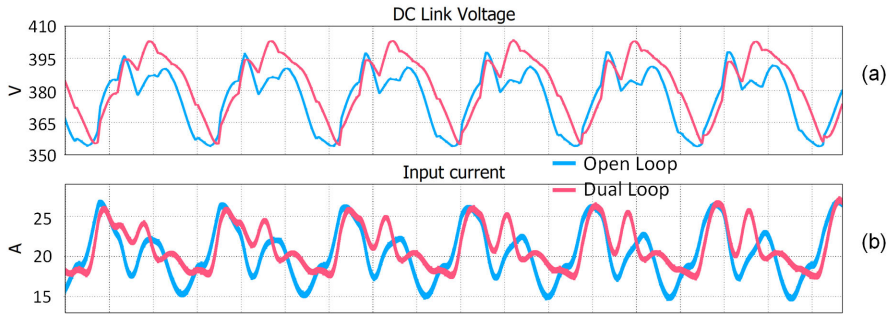

Figure 5.8: Comparison of Dual Loop Control with Open Loop Control at 300 Hz, 3 kW (a) Dynamic DC link Voltage, (b) Input current from PLECS Simulation

at 3 kW, 300 Hz. $6f_1$ is required for dynamic DC link voltage. Other harmonics at multiples of $6f_1$ are considerably reduced with dual loop control.

5.3.2 Transient Performance

This section discusses the transient response of dual loop controller when step or ramp change in DC link voltage is applied that corresponds to the change in speed command of electric vehicle. Fig. 5.11 shows the controller response when step change

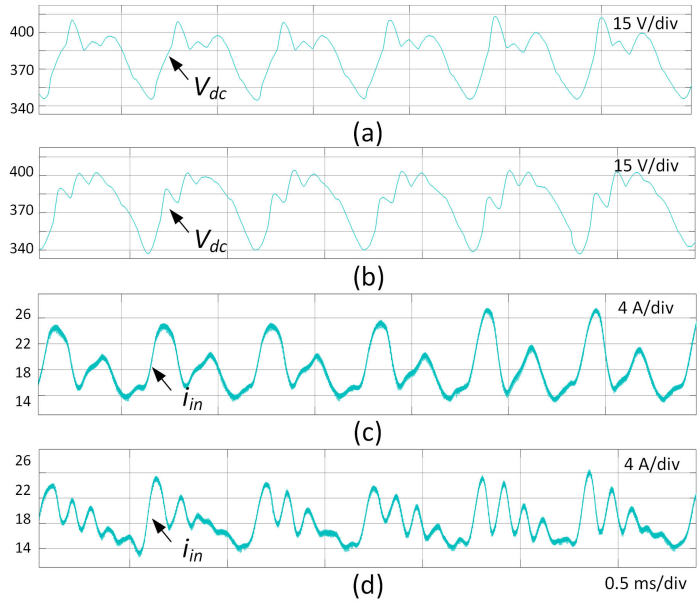

Figure 5.9: Experimental Waveforms at 300 Hz, 3 kW. DC Link Voltage (a) Open Loop Control, (b) Dual Loop Control, Input Current (c) Open Loop Control, (d) Dual Loop Control

in DC link voltage is applied from 250 V to 400 V at 200 Hz. With dual loop control, transient in voltage and input current is reduced as compared to open loop control. Fig. 5.12 shows the similar response at 300 Hz. The current transient in open loop control is as high as 40 A and it is reduced to just 30 A with dual loop control.

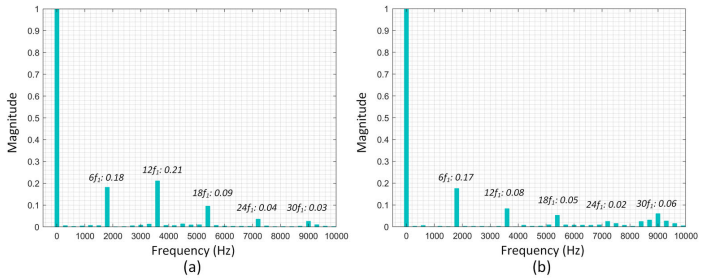

Figure 5.10: Measured Harmonic Spectrum of Input Current at 300 Hz, 3 kW (a) Open Loop control (b) Dual Loop control

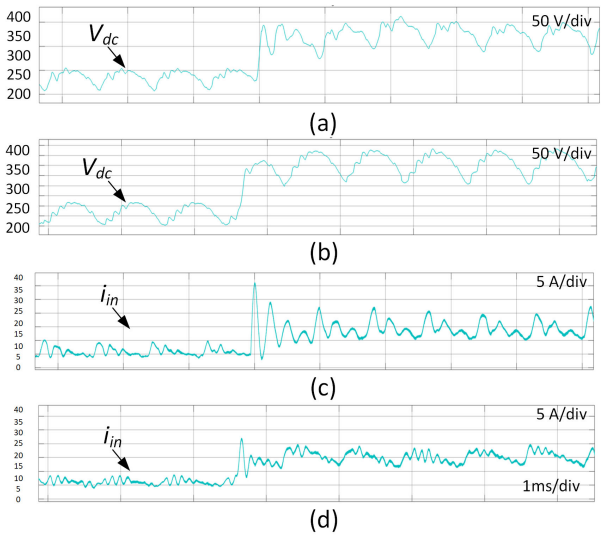

Figure 5.11: Experimental Waveforms for Step Change in DC Link Voltage at 200 Hz, 3 kW. DC Link voltage (a) Open Loop Control, (b) Close Loop Control. Input Current (c) Open Loop Control, (d) Close Loop Control

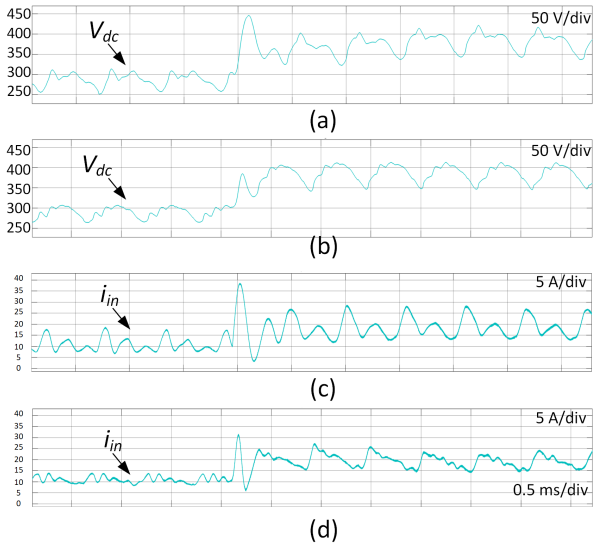

Figure 5.12: Experimental Waveforms for Step Change in DC Link Voltage at 300 Hz, 3 kW. DC Link Voltage (a) Open Loop Control, (b) Close Loop Control. Input Current (c) Open Loop Control, (d) Close Loop Control

Fig. 5.13 shows the experimental results with open loop control and dual loop control in response to the ramp change in DC link voltage from 300 V to 400 V with fundamental frequency of 300 Hz at 3 kW. With dual loop control, DC link voltage

waveshape is good and ripple in input current is also reduced.

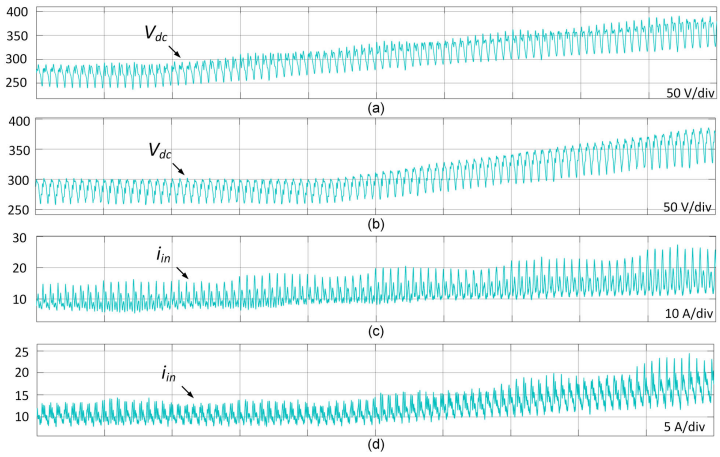

Figure 5.13: Experimental Waveforms for Ramp Change in DC Link Voltage at 300 Hz, 3 kW. DC Link Voltage (a) Open Loop Control, (b) Close Loop Control. Input Current (c) Open Loop Control, (d) Close Loop Control

5.4 Voltage Mode Control with Smith Predictor

Bandwidth of boost converter is limited by a RHP zero which makes the stabilization of control system difficult [85], [86]. Smith predictor based control is proposed to minimize the effect of RHP zero in boost converter and other similar converters [87]. Simplified duty to output voltage transfer function of three phase interleaved boost converter is given as follows:

$$G_s(s) = \frac{V_o}{1-D} \frac{(1-\frac{sL_e}{R_L})}{1+s\frac{L_e}{R_L}+s^2 L_e C_{dclink}} \tag{5.6}$$

Efficacy of voltage control with Smith predictor in terms of better DC link waveshape tracking, low input current ripple and low THD in load current are shown at maximum fundamental frequency of 300 Hz at 3 kW and compared with other well-known control methods.

The interpretation of the all-pass term as a Linear Pade approximation of a dead-time allows to use the notion of predicting the control-response by a Smith Predictor

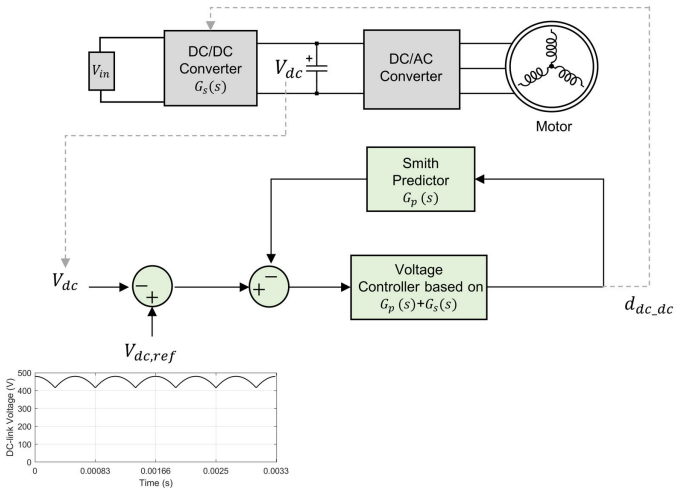

Figure 5.14: Block Diagram of Voltage Mode Control with Smith Predictor

as discussed in detail in [87]. The expression of predictor $G_p(s)$ comes out to be:

$$G_p(s) = \frac{2V_o}{1-D} \frac{(\frac{sL_e}{R_L})}{1 + s\frac{L_e}{R_L} + s^2 L_e C_{dclink}} \tag{5.7}$$

This predictor adds a feed-back loop to the controller showing an effect comparable to a path parallel to the controlled system which removes the all-pass behavior. The controller is designed based on the sum of plant and predictor i.e., $G_{sp}(s) = G_s(s) + G_p(s)$. The block diagram of control architecture with predictive controller is shown in Fig. 5.14. Fig. 5.15 shows the bode plot of plant $G_s(s)$ and sum of plant and predictor $G_{sp}(s)$.

The magnitude response of both the plants are same but the phase response shows that predictor results in a phase increase of 180°. This is because the principle of linear prediction generates the mirror image of RHP zero shifting the RHP zero into the left half plane without changing the location of poles.

For controller design based on plant and predictor, the specifications of the DC-DC stage in experimental prototype are shown in Table 5.1. The predictor design based on the parameters shown in Table 5.1 is as follows:

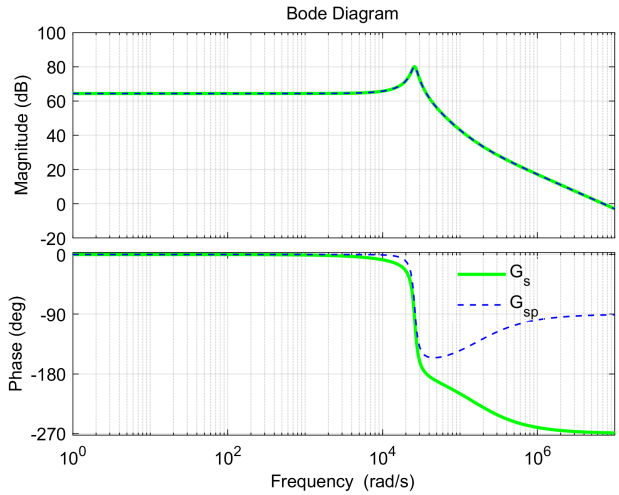

Figure 5.15: Bode Plot Analysis of Plant (Green), Plant and Predictor (Dotted Blue)

$$G_p(s) = \frac{6 * 10^6 s}{s^2 + 3569s + 7.7 * 10^8} \tag{5.8}$$

The controller transfer function $G_c(s)$ based on $G_p(s) + G_s(s)$ designed on the basis of Type-3 k-factor control comes out to be:

$$G_c(s) = \frac{1.1 * 10^{-7} s^2 + 0.005s + 56.6}{6.4 * 10^{-12} s^3 + 5.1 * 10^{-6} s^2 + s} \tag{5.9}$$

PLECS simulation waveforms of reference and generated DC link voltage with Smith Predictor and conventional dual loop control are shown in Fig. 5.16. The DC link voltage in dual loop control is delayed with respect to the reference that causes higher THD in line currents as compared to Smith Predictor (verified in experiments).

The experimental prototype is tested at 3 kW as a scaled down version of an EV/HEV drivetrain. The system is tested at 300 Hz fundamental frequency with the DC-AC stage employing 240CPWM and the DC-DC stage operating with current control, voltage control, dual loop control and voltage control with Smith predictor. Current control gives the lowest input current ripple by compromising the DC link voltage shape and THD in line currents (i.e., THD = 5.38%). Bandwidth of voltage

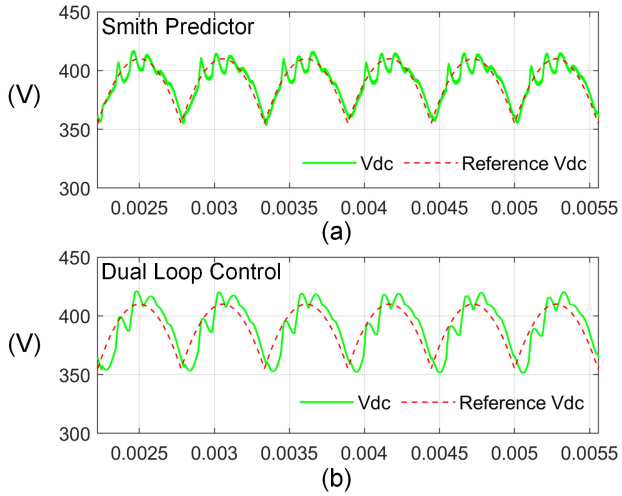

Figure 5.16: Comparison of DC Link Voltage Shape with Smith Predictor and Dual Loop Control at 3 kW with Fundamental Frequency of 300 Hz

control alone is limited by RHP zero, leading to very limited control on dynamically varying DC link voltage shape. Dual loop control delivers decent performance in terms of DC link voltage shaping and input current ripple but additional hardware (i.e., both the current and voltage sensors) is required to implement the dual loop control. Also, THD in line current is greater than 5%. Voltage control with Smith predictor yields decent DC link voltage shaping and minimum THD in line currents i.e., 4.88%. Bandwidth of voltage control with Smith predictor is kept at 15 kHz.

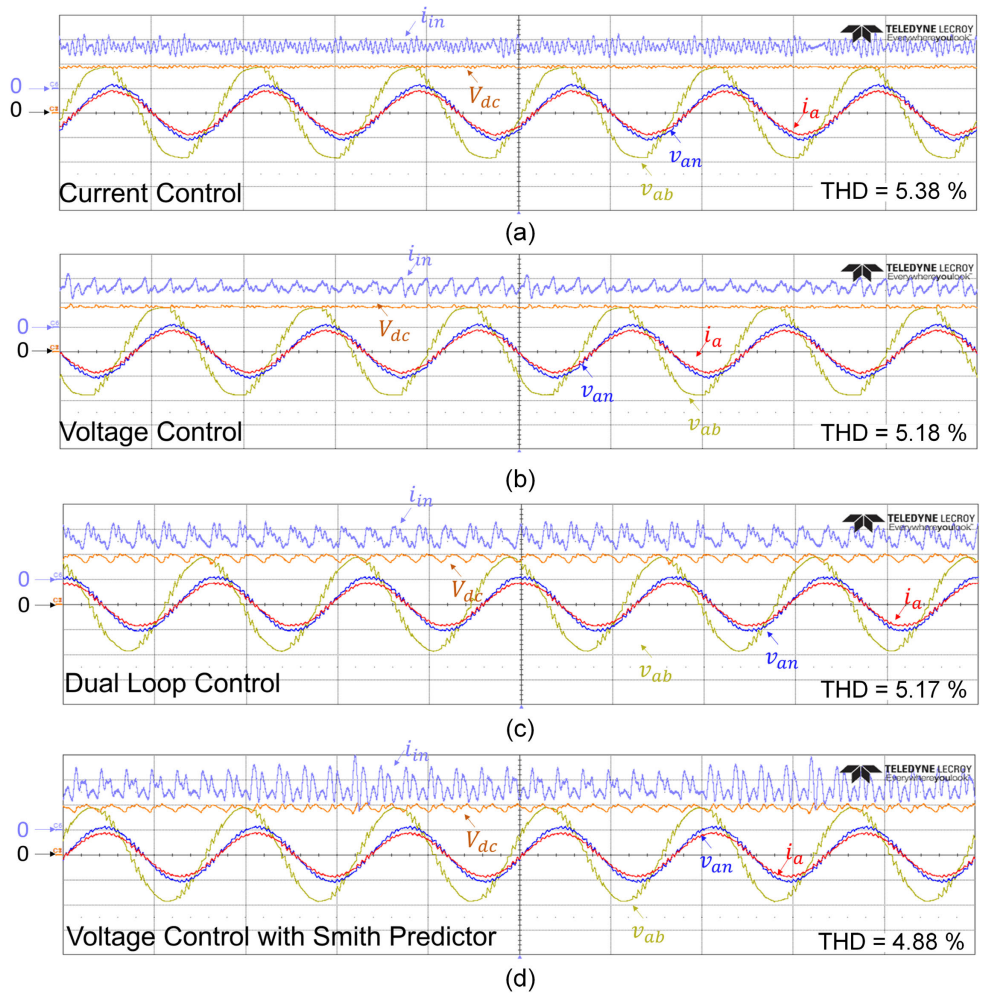

Figure 5.17: Experimental Results of All Control Methods Under Consideration for Shaping the Dynamic DC Link Voltage at 3 kW, 300 Hz

5.5 Conclusion

Dual loop control is designed for tracking the dynamically varying DC link voltage for 240CPWM. Outer voltage loop with low bandwidth and inner current loop with high bandwidth are designed to achieve control objectives. Efficacy of the designed close loop control is shown in terms of much better DC link voltage tracking, reduction in peak to peak input current ripple, reduction in input current ripple due to low

frequency harmonics, comparable THD performance in load current at maximum fundamental frequency of 300 Hz at 3 kW as compared to open loop control. Then voltage mode control of three phase interleaved boost converter with Smith predictor is proposed for shaping the dynamic DC link voltage for 240CPWM that minimizes the impact of RHP zero. Performance of voltage mode control with Smith predictor is verified using a two-stage drive system and compared with other well-known control methods at 3 kW with maximum fundamental frequency of 300 Hz.

Chapter 6

CONTROL AND PERFORMANCE OF 240CPWM IN THREE PHASE GRID-CONNECTED PV CONVERTER APPLICATION UNDER ADVERSE GRID CONDITIONS

6.1 Introduction

Grid connected photovoltaic (PV) systems have seen exponential growth in the recent decades, thanks to the global initiatives and agreements to combat climate change using renewable energy. With more and more PV converters integrating and interacting with the grid, they need to comply with tighter grid interconnection standards to ensure high quality current transfer to the utility grid [88]. Quality of currents injected by the PV inverter into the utility grid is assessed by the Total Harmonic Distortion (THD) value. For example, THD of current injected by the inverter into the utility grid must be less than 5% according to the IEEE 1547 grid interconnection standard [89]. Also, the currents should be sinusoidal and balanced. To meet these requirements, inverter current control plays a crucial role [90]. Various control strategies have been proposed to improve the THD in grid currents e.g., proportional integral (PI) control in the synchronous d-q reference frame, proportional resonant (PR) control in the stationary $\alpha\beta$ domain or more intricate controls like predictive control, deadbeat control and repetitive control [91, 92, 93]. In order to reduce the THD as well as the acoustic noise from AC inductors, most grid-connected PV inverters operate at high switching frequency i.e., 10-20 kHz that compromises the efficiency due to high switching loss [94]. Various soft-switching methods have been proposed to improve the inverter efficiency but they increase the component

count, cost and complexity [95, 96]. Discontinuous PWM (DPWM) methods first proposed in [97] have been widely deployed in three phase inverters to improve the efficiency typically at the expense of increased switching frequency ripple and THD [47]. Later Advanced Bus Clamped PWM (ABCPWM) methods or double switching clamping methods were proposed to improve the THD at maximum modulation index but these methods result in high THD at low modulation index operation and efficiency is compromised at non-unity power factor angles as compared to CSVPWM [53].

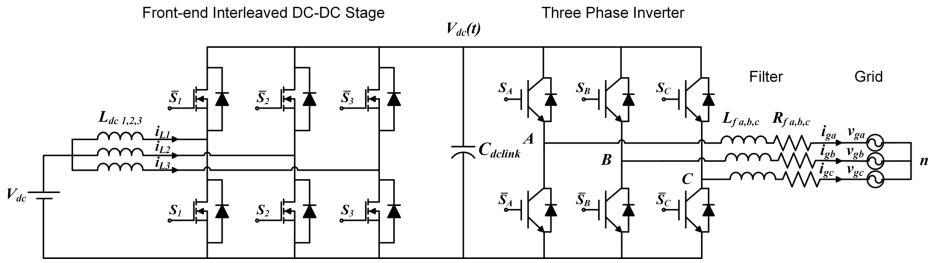

Figure 6.1: Schematic of Grid Connected PV Converter under Consideration.

240CPWM was first introduced for grid-connected PV application [98, 99, 100, 101, 102] and later for motor drives [82, 61, 103] and battery chargers [62]. This modulation method is named as double 120 flattop modulation in [98] and [99] wherein only the islanded mode of operation is elaborated that needs optimization in grid-connected mode. Only preliminary results with 120 flattop modulation in grid-connected mode are shown in [100]. The same modulation concept (named as single phase PWM) is used in [101] and [102] in which theoretical DC input current ripple and harmonic current have been derived and switching loss characterization is presented. All these studies show the performance of 240CPWM in PV converters either in islanded mode or very priliminary results in grid connected mode at unity power factor. In [104], 240CPWM was explored in grid connected mode under non-

unity power factor conditions only in simulations. In this chapter, performance of 240CPWM is evaluated in grid connected mode under non-unity power factors, active and reactive power support, disturbances in grid voltages like voltage unbalance and sag and swell in grid voltages from PLECS simulations and experiments.

240CPWM requires a six-pulse dynamic DC-link voltage varying in both average and instantaneous sense instead of a constant DC-link voltage. In [99], the dynamic DC-link voltage is obtained by indirectly regulating the DC link current in grid-connected PV inverter. Similar DC link voltage was established by employing input current controller in [101]. Utilizing input current control to regulate the six-pulse dynamic DC link voltage is not enough especially under unbalanced grid conditions or non-unity power factor angle. The DC-DC converter in the PV converter system is used to generate the dynamic DC link voltage either in open loop or close loop control. Three phase grid-connected PV converter under consideration is shown in Fig. 6.1. DC-DC stage is a three-phase interleaved boost converter and DC-AC stage is two-level three-phase inverter. In this work, a well-established dual-loop control is implemented to regulate the dynamic DC link voltage. The dual loop control is able to regulate the dynamic link voltage under grid disturbance and reactive power support.

6.2 Controller Analysis, Design and Constraints

Fig. 6.2 shows the control block diagram with 240CPWM in grid connection. The description of each control and their coordination is as follows:

6.2.1 Coordinated Control of DC-DC and DC-AC Stages

For robust operation of the PV converter with 240CPWM, both the DC-DC stage and DC-AC stages are required to work in coordination with each other. The mod-

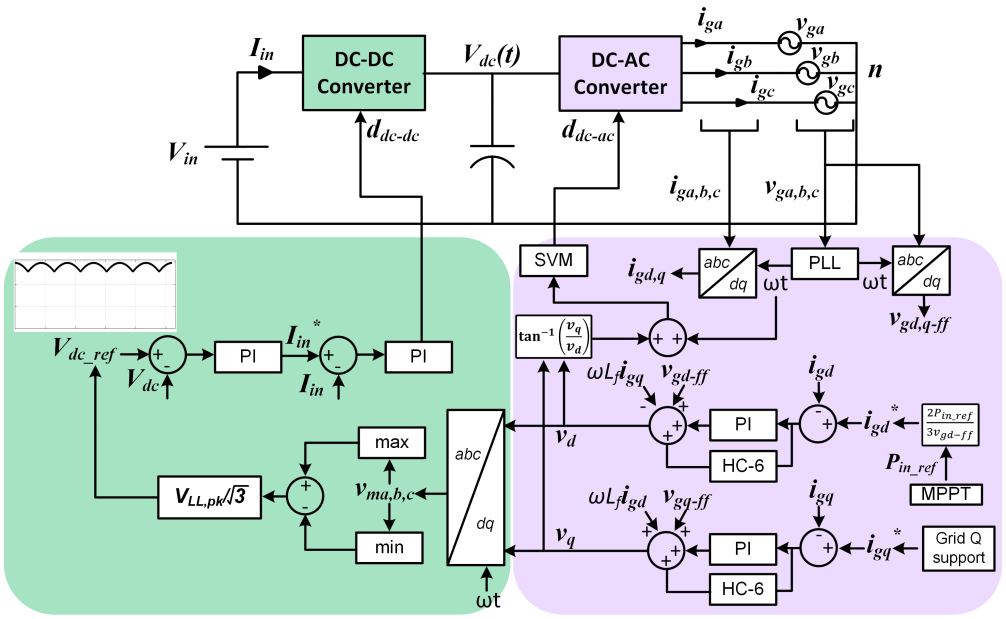

Figure 6.2: Control Block Diagram of 240CPWM in Grid Connection.

ulation index of DC-AC stage is always maintained at the maximum value (while its phase angle is controlled), and the primary control mechanism varies the magnitude, phase and waveshape of the DC link voltage.

In Fig. 6.2, $\omega L_f i_{gd}$ and $\omega L_f i_{gq}$ are the cross-coupling and v_{gd-ff} and v_{gq-ff} are the feed forward terms. R_f and $j\omega L_f$ are the resistance and impedance of the filter inductor respectively. i_{gd} and i_{gq} are the d and q components of grid current and v_d and v_q that are the outputs of grid current controller.

Output of inverter side current control is used to generate the DC link voltage reference for dual loop control of DC-DC stage as shown in Fig. 6.2. Output of inverter side current control is $v_{d,q}$ in dq reference frame. $v_{d,q}$ is transformed into time domain using dq to abc transformation as follows:

$$\begin{bmatrix} v_{ma} \\ v_{mb} \\ v_{mc} \end{bmatrix} = \begin{bmatrix} cos(\omega t) & -sin(\omega t) \\ cos(\omega t - 2\pi/3) & -sin(\omega t - 2\pi/3) \\ cos(\omega t + 2\pi/3) & -sin(\omega t + 2\pi/3) \end{bmatrix} \cdot \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{6.1}$$

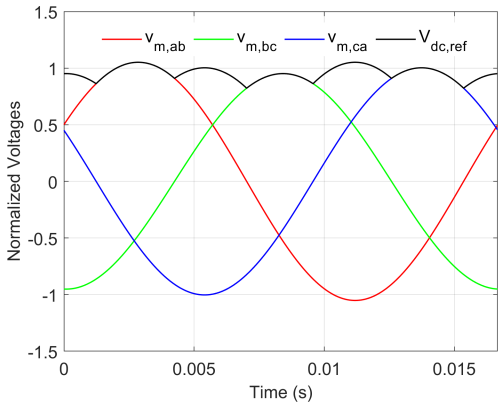

Figure 6.3: Dynamic DC Link Voltage Reference Corresponding to Unbalance in Grid Voltages.

The dynamic DC link voltage reference is obtained from v_{ma}, v_{mb} and v_{mc} as follows:

$$V_{dc,ref} = \frac{V_{LL,pk}}{\sqrt{3}} \cdot (\max\{v_{ma}, v_{mb}, v_{mc}\} - \min\{v_{ma}, v_{mb}, v_{mc}\}) \tag{6.2}$$

where v_{ma}, v_{mb} and v_{mc} are the inverter side current controller outputs transformed into abc domain. In case of grid disturbance, the controller output $v_{d,q}$ and therefore $v_{ma,b,c}$ adjust such that the dynamic DC link voltage reference follows the grid disturbance precisely. One such case of voltage unbalance is shown in Fig. 6.3 that corresponds to voltage unbalance in all three phases of the grid i.e., phase a and c are 10% higher and 10% lower than the nominal grid voltage respectively and phase b is at the nominal grid voltage. In Fig. 6.3, $v_{m,ab} = v_{ma} - v_{mb}$, $v_{m,bc} = v_{mb} - v_{mc}$ and $v_{m,ca} = v_{mc} - v_{ma}$ are shown with the DC link voltage following the grid disturbance for the sake of better visualization.

6.2.2 DC Link Voltage Control

A typical three phase grid connected PV converter consists of a DC-DC converter followed by a three-phase inverter. In conventional PWM methods (like CSVPWM), DC-DC converter is responsible for MPPT while the inverter regulates the DC link

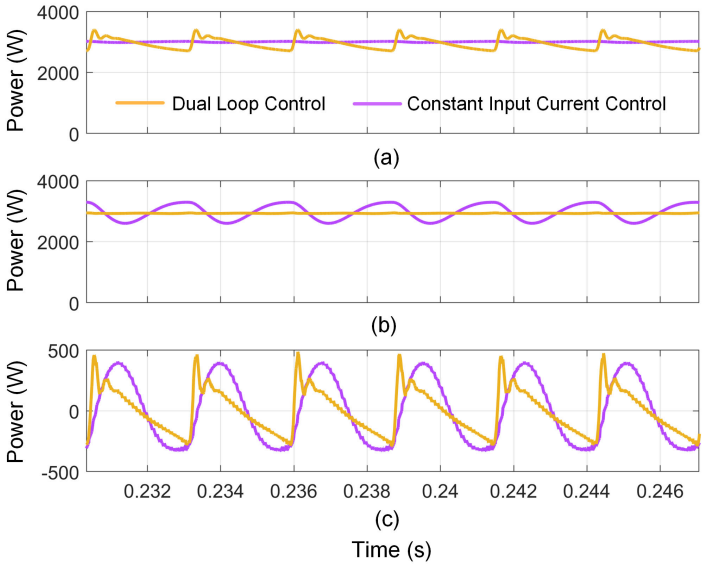

Figure 6.4: Power with Dual Loop Control and Constant Input Current Control from PLECS simulation (a) Input Power P_{in}, (b) Output Power P_{out}, (c) DC Link Capacitor Power P_{dclink}

voltage and grid side currents in a dual loop fashion. 240CPWM requires the dynamic DC link voltage shape instead of constant DC link voltage that is controlled by the DC-DC converter. With 240CPWM in DC-AC stage, the control architecture changes in such a way that DC-DC stage can no longer provide MPPT because it is responsible for six-pulse dynamic DC link voltage tracking. DC-DC converter in grid connected PV applications is normally a boost converter or its variant [105]. Bandwidth of its voltage control loop is limited by a right half plane (RHP) zero [101]. So, voltage control alone is not sufficient to track the dynamic DC link voltage which is required for 240CPWM. Dual loop control with outer voltage loop and inner current loop is used to regulate the dynamic DC link voltage. The outer loop with low bandwidth regulates the DC link voltage and the inner loop is the input current control loop with high bandwidth that improves the dynamic performance. The dual loop control gives better performance even under grid disturbances and non-unity power factor conditions.

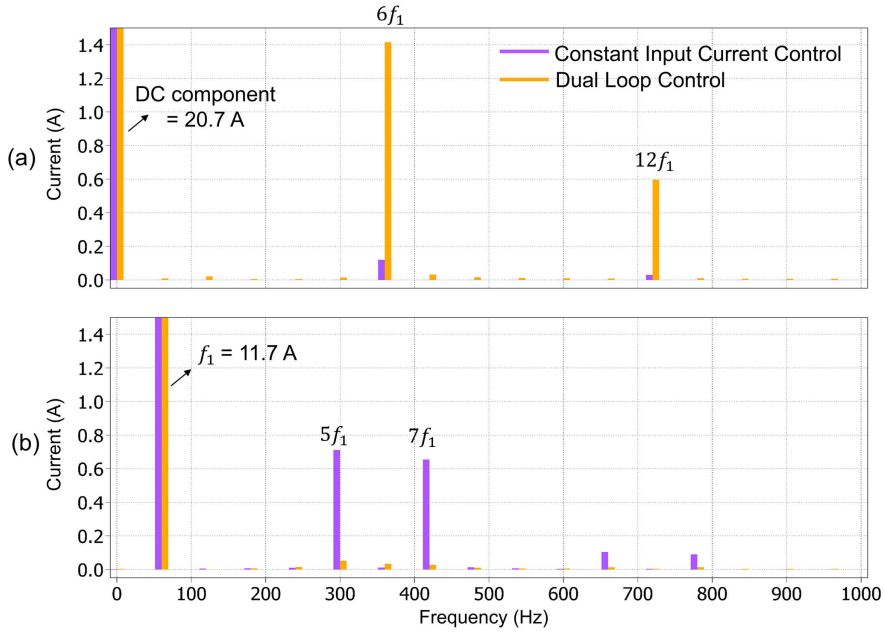

Figure 6.5: FFT of Currents Obtained from PLECS Simulation with Constant Input Current Control and Dual Loop Control in DC-DC stage (a) Input Current (b) Inverter Current

A constant input current control scheme has been described in previous works [101] where the DC-DC stage controls the input current to follow a constant DC reference (possibly from MPPT loop). With suitable control of the DC-AC stage along with the switching pattern of 240CPWM the DC link automatically follows a waveform that is somewhat similar to the desired DC link waveform given in (6.2). However, there are several drawbacks to this scheme. The DC link is distorted when compared with the desired waveform given in (6.2). The output grid current is highly distorted even for unity power factor operation and balanced grid voltages. The inverter current distortion in this scheme is due to the pulsating power associated with charging/discharging of the DC-link capacitor (to follow the six-pulse DC-link waveform) being supported mostly by the grid. The DC link capacitor power P_{dclink} is given by (6.3) under ideal lossless conditions.

$$P_{dclink} = P_{6f1} + P_{12f1} + P_{18f1} + ... = P_{in} - P_{out} \tag{6.3}$$

where P_{in} and P_{out} are the input and output power respectively. With 240CPWM, P_{dclink} draws $6f_1$ as a dominant harmonic component and with constant input current control, $6f_1$ harmonic power is supported from the inverter side. In the dual-loop control scheme implemented here, the pulsating power is slightly reduced and is mostly supported from the DC side, where it is easier to filter. P_{in}, P_{out} and P_{dclink} for dual loop control and constant input current control are shown in Fig. 6.4 from PLECS simulation where $6f_1$ pulsation is in agreement with the discussion above.

The FFT of DC input current and inverter current both with constant input current control and dual loop control are shown in Fig. 6.5. In dual loop control, the $6f_1$ harmonic in the input current is 12 times higher than constant input current control whereas $5f_1$ and $7f_1$ harmonic components in the inverter current are 22 and 53 times lower than constant input current control respectively. It may be noted that reducing the DC link capacitance reduces the pulsating power requirement and helps both the schemes achieve better grid current THD and/or better MPPT performance with smaller filters.

Boost converter and other similar topologies suffer from inherent issue of RHP zero in control to output voltage transfer function that poses limitations in terms of maximum achievable control loop bandwidth. This zero makes the stabilization of the system considerably difficult. Higher switching frequency allows the use of smaller inductors, thereby pushing RHP zero further away that allows more control freedom. However, due to low efficiency of such converters at high switching frequency, a trade-off has to be made between efficiency and control bandwidth. n phase interleaved boost converter shifts the RHP zero to n times the RHP zero of a single phase converter [106]. RHP zero of interleaved boost converter is given by $n(1-D)^2R_L/L_{dc}$, where n is the number of interleaved phases, D is the duty ratio, R_L is the load and L_{dc} is the inductance of DC-DC converter. RHP zero for the DC-DC boost converter

with specifications shown in Table 6.1 comes out to be 6.5 kHz. As a rule of thumb, bandwidth of the controller is limited to one tenth of the RHP zero. So, the maximum achievable bandwidth for outer voltage loop is around 650 Hz.

The dual loop control for DC-DC converter is shown in Fig. 6.2. Voltage loop is designed to track the dynamic DC link voltage required for 240CPWM. The six-pulse dynamic DC link voltage has dominant frequency components at 360 Hz. PI control is used for both the outer voltage loop and inner current loop. Bandwidth of outer voltage loop is kept at 600 Hz and inner current loop at 3 kHz.

6.2.3 Grid Side Current Control

Fig. 6.2 shows the control block diagram with 240CPWM in grid connection. A typical three phase grid connected PV converter consists of a DC-DC converter followed by a three-phase inverter. In conventional PWM methods (like CSVPWM), DC-DC converter is responsible for maximum power point tracking (MPPT) while the inverter regulates the DC link voltage and grid side currents in a dual loop fashion [23]. 240CPWM requires the dynamic DC link voltage shape instead of constant DC link voltage that is controlled by the DC-DC converter. With 240CPWM in DC-AC stage, the control architecture changes in such a way that DC-DC stage can no longer provide MPPT because it is responsible for six-pulse dynamic DC link voltage tracking. So, DC-AC inverter when modulated with 240CPWM is required to perform MPPT, PLL, ensure sinusoidal grid currents and execute grid support functions [104].

PI controller is the most popular choice for grid side current control. In three-phase systems, the three phase reference frame *abc* coordinates are transformed into synchronously revolving *dq* reference frame using Park transformation [107]. The PI controller is simple and straightforward. However, it has some inherent drawbacks i.e., it exhibits poor performance due to cross-coupling between d and q axes. This

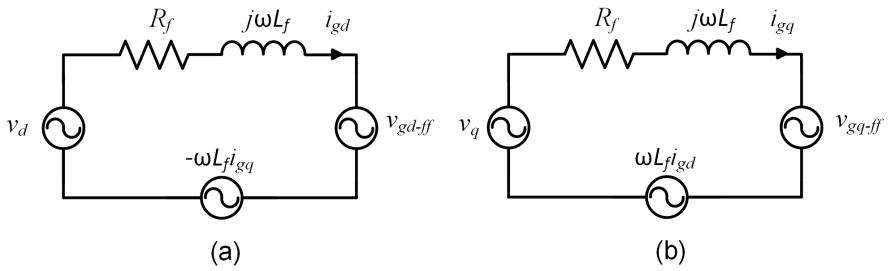

Figure 6.6: Model of the Grid Side Current Control in dq Reference Frame.

is overcome by introducing decoupling and feedforward terms [108], [109]. Moreover, PI controller cannot eliminate the low order harmonics that eventually increase the THD in grid currents [88].

Simplified model of grid side current control in dq reference frame is shown in Fig. 6.6. $\omega L_f i_{gd}$ and $\omega L_f i_{gq}$ are the cross-coupling and v_{gd-ff} and v_{gq-ff} are the feed forward terms. R_f and $j\omega L_f$ are the resistance and impedance of the filter inductor respectively. i_{gd} and i_{gq} are the d and q components of grid current and v_d and v_q are the outputs of grid side current controller. The dq components of sensed grid voltages that are used as feed forward terms (v_{gd-ff} and v_{gq-ff}) in grid current controller are defined in (6.4).

$$\begin{bmatrix} v_{gd-ff} \\ v_{gq-ff} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos(\omega t) & cos(\omega t - 2\pi/3) & cos(\omega t + 2\pi/3) \\ -sin(\omega t) & -sin(\omega t - 2\pi/3) & -sin(\omega t + 2\pi/3) \end{bmatrix} \cdot \begin{bmatrix} v_{ga} \\ v_{gb} \\ v_{gc} \end{bmatrix} \tag{6.4}$$

v_{gd-ff} and v_{gq-ff} are used to improve PI controller performance have undesired low frequency harmonics i.e., $3f_1$, $5f_1$ and $7f_1$ etc where $f_1 = 60$ Hz (frequency of the grid). These dominant harmonics in grid voltage subsequently inject harmonics at the same frequencies into i_{gd} and i_{gq} [110]. Rotating speeds for x_{th+1} and x_{th-1} harmonics correspond to x_{th} harmonic in dq reference frame [111]. Hence, to suppress the dominant low frequency harmonics of $5f_1$ and $7f_1$ in grid currents, a harmonic compensator at $6f_1$ (HC-6) is selected. Block diagram of grid side current control

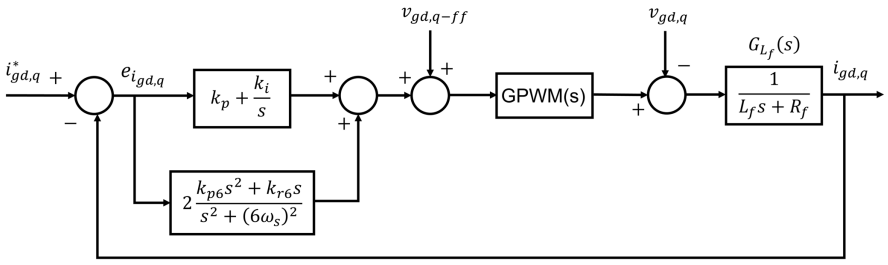

Figure 6.7: Block Diagram of the Grid side Current Controller.

consisting of HC-6 in parallel with PI controller (PI + HC-6) is shown in Fig. 6.7. The open loop transfer function of PI with HC-6 controller is given by (6.5) where K_p and K_i are the proportional and integrator controller gains for the PI controller, k_{p6} and k_{r6} are the proportional and integrator gains for the HC-6 controller and $\omega_s = 2\pi 60$.

$$G_{PI+HC-6}(s) = K_p + \frac{K_i}{s} + 2\frac{k_{p6}s^2 + k_{r6}s}{s^2 + (6\omega_s)^2} \tag{6.5}$$

Bode plot of the open loop gain of PI and HC-6 controller is shown in Fig. 6.8. The PI controller has high gain at low frequency range (less than 50 Hz) but its gain decreases substantially at high frequencies (greater than 200 Hz) which implies that PI controller cannot regulate any undesired harmonics existing beyond 200 Hz. PI + HC-6 controller has a high gain at low frequencies but has a much higher gain specifically at 360 Hz ($6f_1$). High gain at $6f_1$ confirms that PI + HC-6 controller can effectively compensate the undesired $5f_1$ and $7f_1$ harmonics in dq reference frame. The parameters of PI controller K_p and K_i are designed for bandwidth of 500 Hz. The design of HC-6 controller involves tuning of k_{p6} and k_{r6}. The relationship between k_{p6} and k_{r6} is given by $k_{r6} = k_{p6}(R_f/L_f)$. The boundary of controller gains is determined using Routh's stability criterion that determines the number of closed loop poles in right half s-plane. From Fig. 6.7, the closed loop transfer function of the overall current control loop is given as follows.

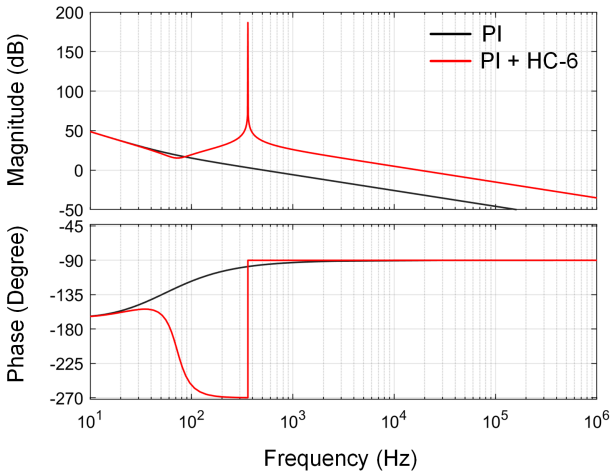

Figure 6.8: Bode Plot of PI and HC-6 Controller.

$$G_c(s) = \frac{G_{PI+HC-6}(s)G_{PWM}(s)G_{Lf}(s)}{1 + G_{PI+HC-6}(s)G_{PWM}(s)G_{Lf}(s)} \tag{6.6}$$

where G_{Lf} is the plant transfer function which is given by (6.7):

$$G_{Lf} = \frac{1}{L_f s + R_f} \tag{6.7}$$

$G_{PWM}(s)$ is the transfer function of the PWM unit in s-domain which includes the computation delay, sampler, zero-order hold unit. [112]:

$$G_{PWM}(s) = \frac{1 - 0.5T_s}{(1 + 0.5T_s)^2} \tag{6.8}$$

Using $k_{r6} = k_{p6}(R_f/L_f)$ in (6.6) simplifies $G_c(s)$ as follows where $N_{Gc}(s)$ and $D_{Gc}(s)$ are the numerator and denominator of $G_c(s)$ respectively.

$$\begin{aligned} N_{Gc}(s) = &-0.5(K_p + 2k_{p6})T_s s^3 + (K_p + 2k_{p6})s^2 \\ &-(0.5K_p(6\omega_s)^2 T_s)s + K_p(6\omega_s)^2 \end{aligned} \tag{6.9}$$

$$D_{Gc}(s) = L_f T_s s^4 + (L_f - 0.5(K_p + 2k_{p6})T_s)s^3 + (L_f(6\omega_s)^2 T_s + K_p + 2k_{p6})s^2 + (6\omega_s)^2(L_f - 0.5K_p T_s)s + K_p(6\omega_s)^2 \quad (6.10)$$

Using Routh's stability criterion, $D_{Gc}(s)$ in (6.10) is used to obtain the boundary of K_p and k_{p6} as follows:

$$0 < (K_p + 2k_{p6}) < \frac{2L_f}{T_s}$$
$$0 < K_p < \frac{2L_f}{T_s} \quad (6.11)$$

The value of k_{p6} is selected from the bode plot of $G_c(s)$ given in Fig. 6.9. Smaller value k_{p6} increases selectivity in harmonic compensation but degrades the dynamic response. However, higher value of k_{p6} makes the dynamic response better at the cost of worse steady-state performance. k_{p6} is selected based on bode plot such that it gives a fast dynamic response, a good steady-state performance and simultaneously satisfies (6.11). Based on the selected value of k_{p6}, k_{r6} is calculated using $k_{r6} = k_{p6}(R_f/L_f)$.

6.3 Simulation Results

In order to validate the designed performance of the controller with 240CPWM, PLECS simulation results are presented corresponding to the parameters given in Table 6.1.

Fig. 6.10 shows the inverter currents and their FFT with PI control. Undesired harmonics at fifth and seventh fundamental frequency ($5f_1$ and $7f_1$) are observed that distort the currents. THD of inverter currents is 6.9% with PI control in grid con-

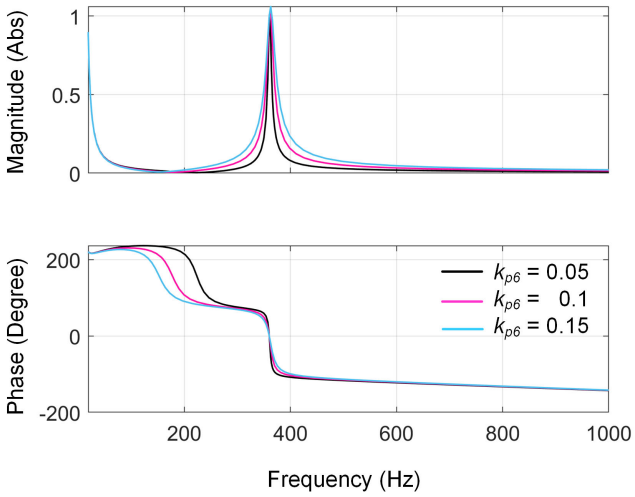

Figure 6.9: Bode Plot of $G_c(s)$ for Different Values of k_{p6}.

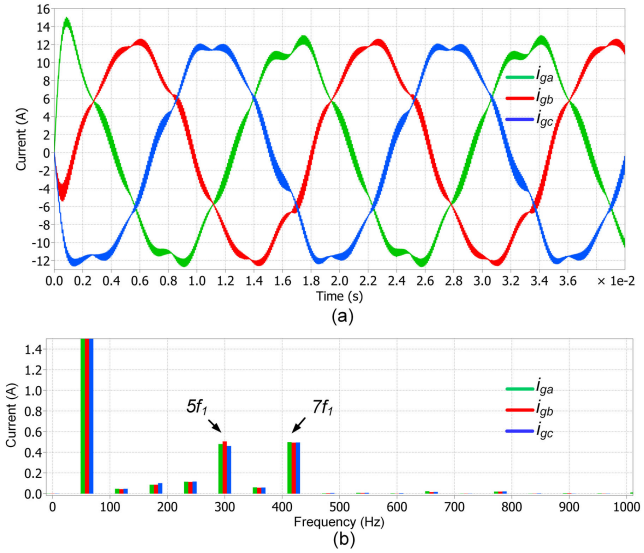

Figure 6.10: PI Controller (a) Inverter Currents, (b) FFT of Inverter Currents Obtained from PLECS simulation

nected PV converter with 240CPWM. THD of 6.9% violates the IEEE-1547 standard of grid interconnection.

Now, PLECS simulation results with the proposed PI+HC-6 controller are presented in Fig. 6.11. Both fifth and seventh fundamental frequency are reduced considerably resulting in smooth sinusoidal currents. THD of inverter currents in this

Table 6.1: Specifications of Grid Connected PV Converter in PLECS Simulation and Experiments.

	Parameter	Value
DC-DC Stage	Output Power P	3 kW
	DC link Voltage peak (with 240CPWM) $V_{dc,pk}$	300 V
	Number of interleaved phase n	3
	Inductance L_{dc}	560 uH
	DC link Capacitance C_{dc}	20 uF
	Switching frequency $f_{sw,dcdc}$	50 kHz
DC-AC Stage	Grid voltage v_g (line-to-line RMS)	208 V
	Filter Inductance L_f	3 mH
	Switching frequency $f_{sw,dcac}$	10 kHz
	Grid frequency f_1	60 Hz

case is only 3.9% which meets the IEEE-1547 standard of grid interconnection.

6.3.1 Active and Reactive Power Control

Fig. 6.12 shows the active power support provided by the inverter at different instants. At 0.06s, step change in d axis reference current i.e., i^*_{gd} from 8 to 12 A is applied which corresponds to increase in active power provided by the inverter (2 kW to 3 kW). At 0.1s, step change in i^*_{gd} from 12 to 8 A is applied which corresponds to decrease in active power provided by the inverter (3 kW to 2 kW). THD in currents are always lower than 5%. Change in i^*_{gd} correponds to the change in active power command as dictated by MPPT. Relation between active power reference command ($P_{PV,ref}$) and i^*_{gd} is given by (6.12).

$$i^*_{gd} = \frac{2P_{PV,ref}}{3V_{ph,pk}} \tag{6.12}$$

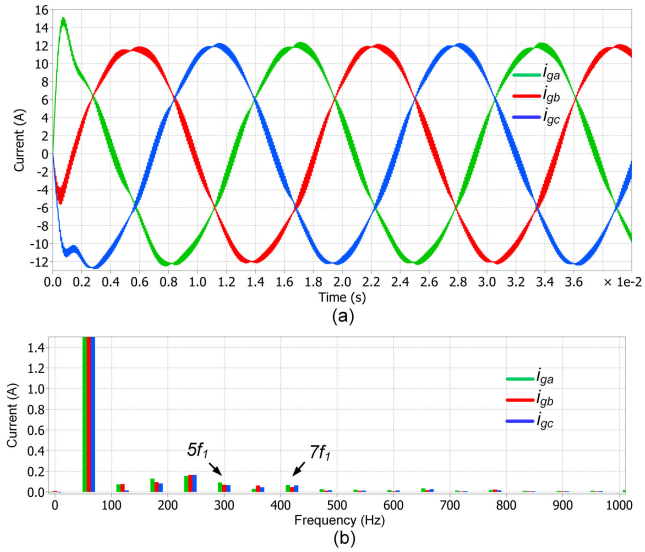

Figure 6.11: PI + HC-6 controller (a) Inverter Currents, (b) FFT of Inverter Currents Obtained from PLECS Simulation

In case of overvoltage condition on the grid side, the inverter absorbs reactive power from the grid. To emulate this scenario of overvoltage condition on the grid side, a step change in i_{gq}^* is applied from 0 to 7 A. The leading power factor on the grid side is due to the reactive power absorbed by the inverter as shown in Fig. 6.13. The active power is maintained at 3 kW whereas a step change in i_{gq}^* corresponds to 1.78 kVARs reactive power absorbed by the inverter. A slight decrease in the DC link voltage after the step change in i_{gq}^* is observed. This voltage drop can be calculated from the per phase equivalent circuit of three phase inverter [113]

$$v_{AB} = i_g(j\omega L_f) + v_g \tag{6.13}$$

For this case, i_{gd}= 12 A and i_{gq}= 7 A, hence $i_g = 13.89\angle 30°$. Using $\omega = 2\pi 60$, v_g = 300, L_f = 0.003 and $i_g = 13.89\angle 30°$ in (6.13) gives $v_{AB} = 292\angle 2.7°$. Hence, the DC link voltage drops from 300 V to 292 V for 30° leading power factor on the grid side.

Grid undervoltage condition is shown in Fig. 6.14 where the inverter injects

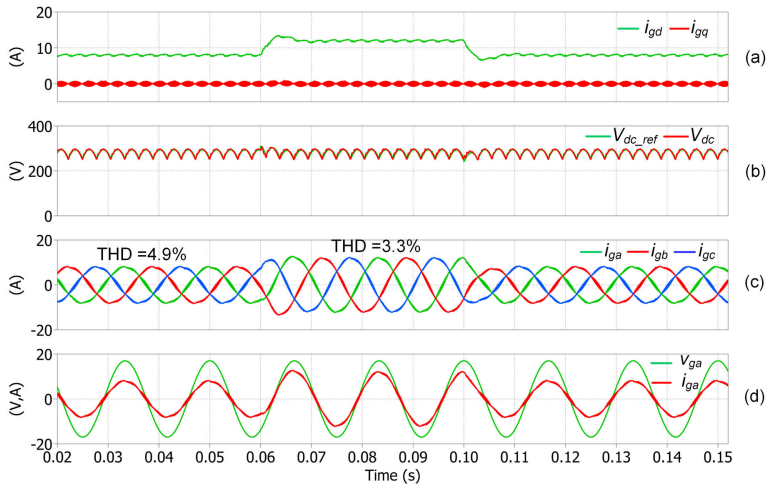

Figure 6.12: PLECS Simulation Results with a Step Change in i^*_{gd} from 8 to 12 A at 0.06s and Back to 8 A at 0.1s to Demonstrate Active Power Support Provided by the Inverter (a) Grid Currents Transformed into d-q Domain, i_{gd} and i_{gq} (b) Dynamic DC Link Voltage V_{dc} and its Reference $V_{dc,ref}$ (c) Grid Currents i_{ga}, i_{gb}, i_{gc} (d) Phase a Voltage v_{ga} (Scaled down by 10) and Grid Current i_{ga}

reactive power into the grid to bring the voltage back in nominal range. To emulate this scenario of undervoltage condition on the grid side, the step change in i^*_{gq} is applied from 0 to $-$ 7 A. The lagging power factor on the grid side is due to the reactive power (1.78 kVARs) injected by the inverter as shown in Fig. 6.14. The small increase in the DC link voltage after the step change in i^*_{gq} from 0 to $-$ 7 A is observed that can be calculated from (6.13).

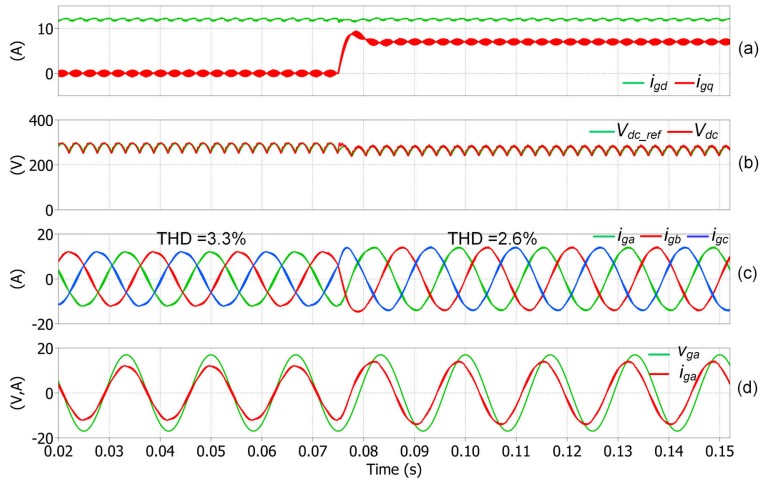

Figure 6.13: PLECS Simulation Results with a Step Change in i^*_{gq} from 0 to 7 A at 0.075s to Demonstrate Reactive Power Support (a) Grid Currents Transformed into d-q omain, i_{gd} and i_{gq} (b) Dynamic DC Link Voltage V_{dc} and its Reference $V_{dc,ref}$ (c) Grid Currents i_{ga}, i_{gb}, i_{gc} (d) Phase a Voltage v_{ga} (Scaled down by 10) and Grid Current i_{ga}

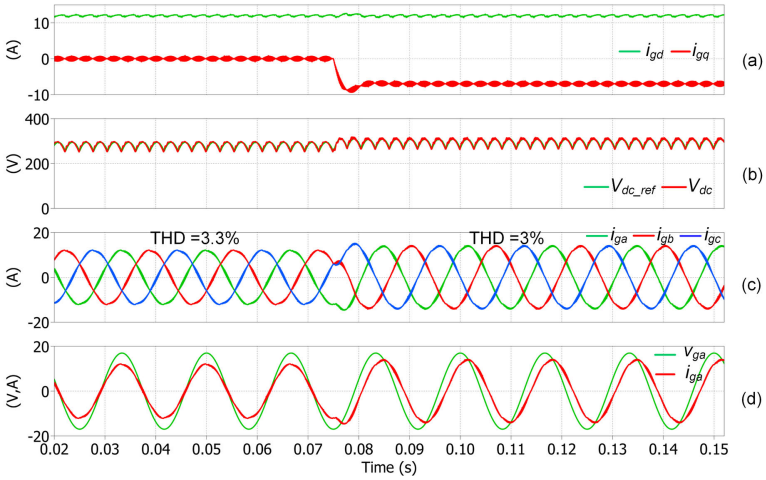

Figure 6.14: PLECS Simulation Results with a Step Change in i^*_{gq} from 0 to -7 A at 0.075s to Demonstrate Reactive Power Support (a) Grid Currents Transformed into d-q Domain, i_{gd} and i_{gq} (b) Dynamic DC Link Voltage V_{dc} and its Reference $V_{dc,ref}$ (c) Grid Currents i_{ga}, i_{gb}, i_{gc} (d) Phase a Voltage v_{ga} (Scaled down by 10) and Grid Current i_{ga}

6.3.2 *Unbalance in Grid Voltages*

Now the performance of 240CPWM in unbalanced grid voltage condition will be demonstrated. 10% unbalance in grid voltages is intoduced in simulation. Unbalance in grid voltage is applied such that v_{an} is 10% higher than nominal voltage, v_{bn} is at nominal voltage and v_{cn} is 10% lower than nominal voltage. The DC link voltage adapts as per the unbalance in grid voltages and line currents are balanced. Hence, 240CPWM works well in unbalanced grid conditions also without any need of additional control. The simulation results corresponding to grid unbalance condition is shown in Fig. 6.15.

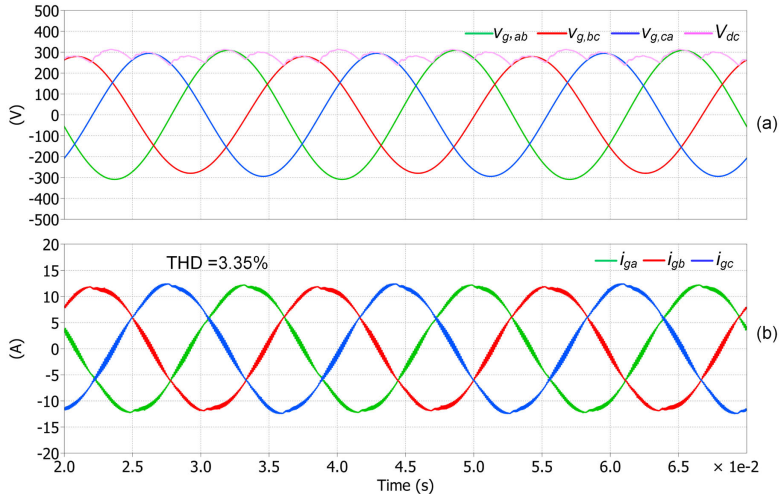

Figure 6.15: (a) Grid Line to Line Voltages $v_{g,ab}$, $v_{g,bc}$ and $v_{g,ca}$ and DC Link Voltage V_{dc}, (b) Line Currents $i_{ga,gb,gc}$ with 240CPWM in Grid-connected Mode under Grid Unbalance Condition.

6.3.3 *Sag and Swell in Grid Voltages*

240CPWM is evaluated during sag and swell in grid voltages as shown in Fig. 6.16(a) and (b) respectively. 10% sag and 10% swell in grid voltages is applied in simulation. The DC link voltage adjusts as per the decrease or increase in grid voltages. THD in grid currents for voltage sag case is 2.9% and it is 3.7% for voltage

swell case.

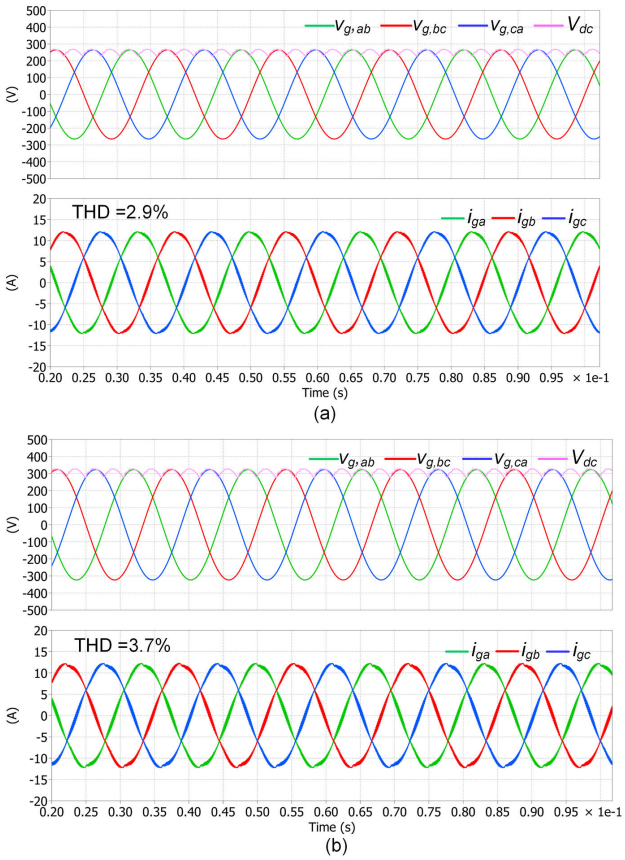

Figure 6.16: Grid Line to Line Voltages $v_{g,ab}$, $v_{g,bc}$ and $v_{g,ca}$ and DC Link Voltage V_{dc} and Line Currents $i_{ga,gb,gc}$ with 240CPWM in Grid-connected Mode (a) Sag in Grid Voltages, (b) Swell in Grid Voltages

To validate the performance of designed PI + HC-6, the FFT of inverter current with PI controller and PI + HC-6 controller for 240CPWM are shown in Fig. 6.17 from PLECS simulation corresponding to the experimental setup conditions where applied current reference at the inverter side is 11.7 A corresponding to 3 kW. With PI controller, FFT of inverter current shows dominant harmonics at $5f_1$ and $7f_1$ due to the DC link capacitor power pulsation unique to 240CPWM. The undesired harmonics at $5f_1$ and $7f_1$ are significantly reduced by applying PI + HC-6 controller.

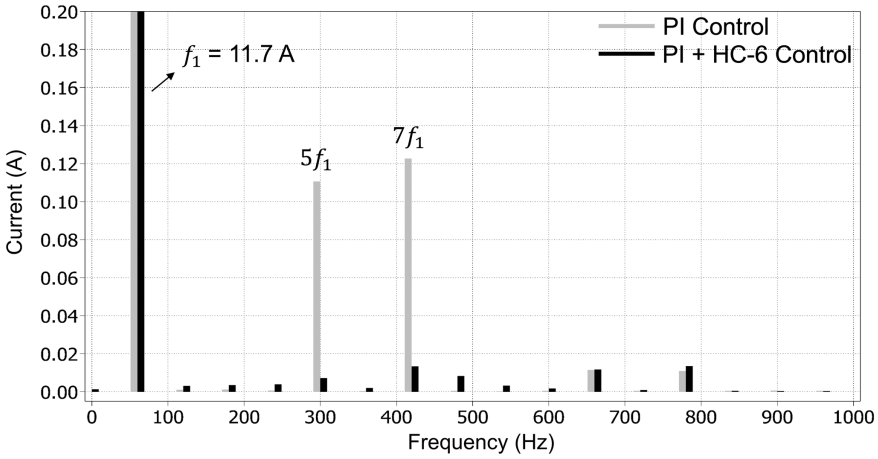

Figure 6.17: FFT of Inverter Current Obtained from PLECS Simulation with PI Controller and PI + HC-6 Controller.

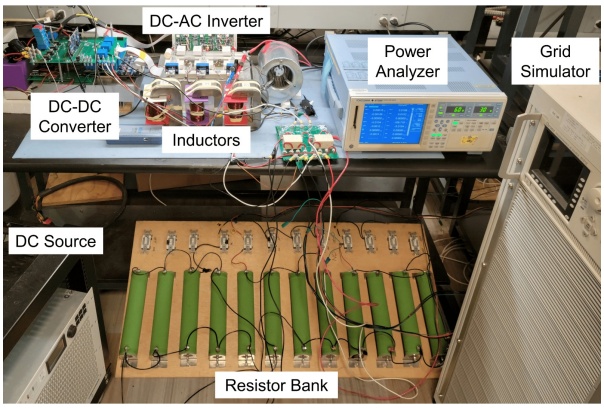

Figure 6.18: Picture of Experimental Setup.

6.4 Experimental Validation

The experimental set-up is rated at 3 kW and is shown in Fig. 6.18. The specifications of the grid-connected PV converter under consideration are demonstrated in Table 6.1. The parameters of PI + HC-6 controller for inverter side current control used in the experimental set-up are given in Table 6.2. All the experimental results are obtained with actual grid that has non-ideal grid voltages with low order harmonics except the results with sag/swell and unbalance grid voltage conditions that are obtained with grid simulator.

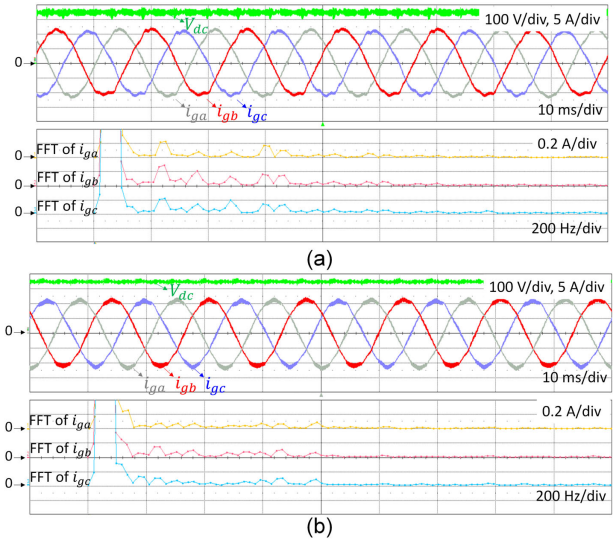

Figure 6.19: Experimental Waveforms of DC Link Voltage V_{dc}, Inverter Currents $i_{ga,gb,gc}$, FFT of Inverter Currents $i_{ga,gb,gc}$ (a) CSVPWM (b) DPWM1, All in Grid-connected Mode.

Table 6.2: Parameters of PI and HC-6 Controller Used in the Experimental Setup.

Controller	Parameter
PI	$K_p = 0.06$ $K_i = 20$
HC-6	$k_{p6} = 0.1$ $k_{r6} = 0.7$

The experimental waveforms are captured by a LeCroy HDO8038 oscilloscope with 10 MHz sampling frequency using LeCroy CP030 30 A 50 MHz current probes and LeCroy ADP305 100 MHz 1400 V differential voltage probes. The efficiency of PV converter is obtained using Yokogawa WT3000 precision power analyzer. The current waveforms are post-processed in MATLAB to obtain THD up to 1 MHz. Besides the operation of 240CPWM in grid-connected mode under unity power factor operation, following cases will be discussed to assess inverter performance under non-ideal conditions:

- Case I: Non-unity power factor

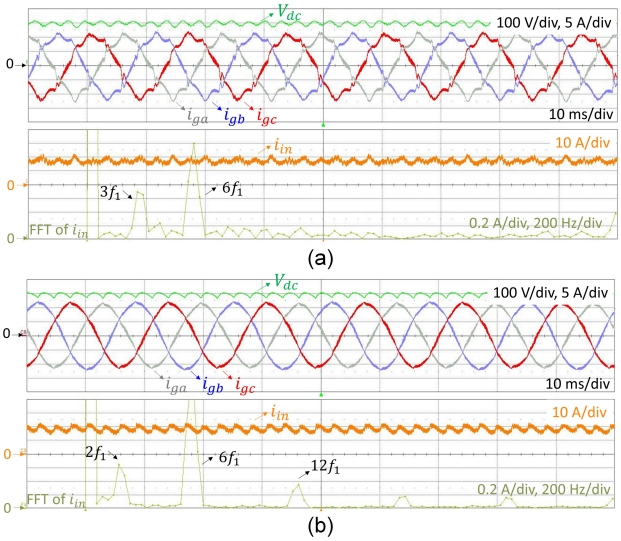

Figure 6.20: Experimental Waveforms of DC Link Voltage V_{dc}, Inverter Currents $i_{ga,gb,gc}$, Input Current i_{in}, FFT of Input Current i_{in} with 240CPWM (a) Constant Input Current Control (b) Dual Loop Control, in DC-DC Stage All in Grid-connected Mode.

- Case II: Unbalance in grid voltages
- Case III: Sag or swell in grid voltages

The experimental results in grid connected mode for CSVPWM and DPWM1 with PI + HC-6 controller at 3 kW and 208 V line to line RMS voltage are shown in Fig. 6.19. CSVPWM and DPWM1 are limited to 0.91 M_{max} due to large dead time of silicon IGBTs in the inverter. The DC link voltage for CSVPWM and DPWM1 is maintained at 350 V. The mean THD in inverter currents is measured as 4.8% for CSVPWM and 5% for DPWM1. Although CSVPWM has high low order harmonics (Fig. 6.19 (a)) as compared to DPWM1 and 240CPWM but the total THD is still highest for DPWM1 due to high switching frequency ripple in currents at current peaks (Fig. 6.19 (b)).

Experimental results with constant input current control and dual loop control of DC-DC stage are shown in Fig. 6.20. FFT of input current with dual loop control shows a dominant harmonic at $6f_1$ which is consistent with the simulation results.

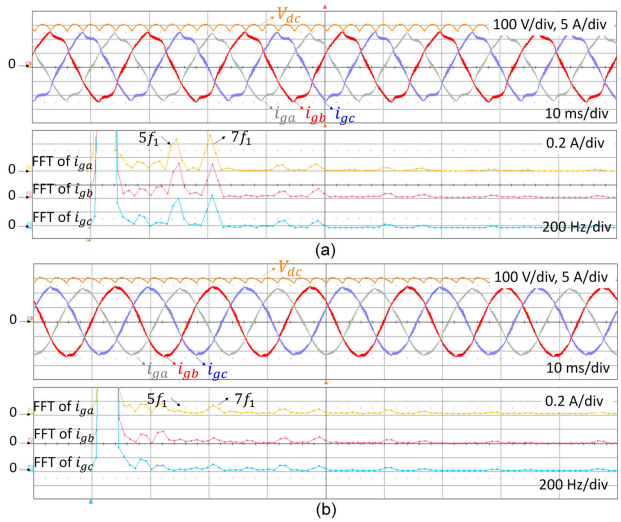

Figure 6.21: Experimental Waveforms of DC Link Voltage V_{dc}, Inverter Currents $i_{ga,gb,gc}$, FFT of Inverter Currents $i_{ga,gb,gc}$ with 240CPWM with (a) PI Controller Only (b) PI + HC-6 Controller, in DC-AC Stage All in Grid-connected Mode.

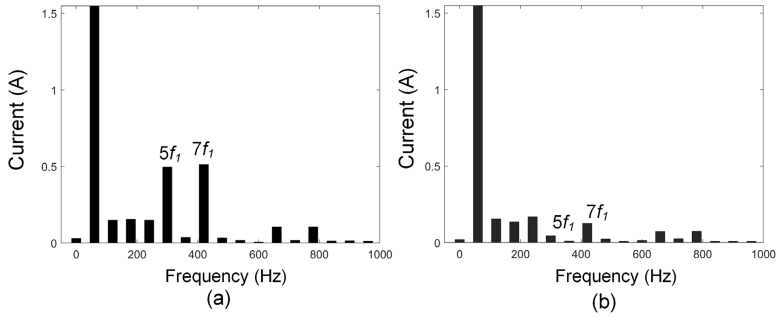

Figure 6.22: Frequency Spectrum of Inverter Current from Experiment at 3 kW with 240CPWM (a) With PI Controller (b) With PI + HC-6 Controller.

In case of constant input current control scheme, the $6f_1$ harmonic component is drawn from the output inverter current to provide the pulsating power for the DC link whereas using the dual loop control, $6f_1$ harmonic power is drawn from the DC side. The $6f_1$ harmonic in DC input current can be mitigated easily by adding a filter capacitor on the DC input side. However, minimizing the harmonics in the output AC side is difficult where large filters and complex control are required. Constant input current control scheme results in 11.2% THD in inverter currents which is not acceptable as per the IEEE-1547 standard for grid interconnection. Dual loop control

scheme gives superior performance with THD of 3.5%. Hence, dual loop control is selected as the controller of choice for DC-DC stage in this work.

To show the robustness of PI + HC-6 controller, experimental results in grid connected mode for 240CPWM with PI controller only and PI + HC-6 controller in the DC-AC stage are presented in Fig. 6.21 at 3 kW, 208 V. Fig. 6.22 shows MATLAB post-processed frequency spectrum of inverter current with PI and PI + HC-6 controller corresponding to the experimental waveforms shown in Fig.6.21. It can be observed that the 5th and 7th harmonics are the most dominant harmonic components in inverter currents with highest magnitude of 0.5 A. The harmonic compensator at 6th harmonic in *dq* reference frame corresponds to 5th and 7th harmonic in *abc* domain. Hence, the harmonic compensator under consideration reduces the magnitude of 5th and 7th harmonics to less than 0.1 A as demonstrated in Fig. 6.22 (b). Hence, the THD in inverter currents is reduced from 7.5% to 3.5% in 240CPWM by using HC-6 controller with PI controller. PI + HC-6 results in THD less than or equal to 5% for all PWM methods under consideration. The dual loop control in DC-DC stage generates and regulates six-pulse dynamically varying DC link voltage for 240CPWM as expected.

The combined efficiency of DC-DC and DC-AC stages are measured corresponding to the experimental results shown in Fig. 6.19 and 6.21 (b). At 3 kW, the total measured efficiencies for CSVPWM, DPWM1 and 240CPWM are 94.24 %, 95.73% and 96% respectively. 240CPWM has the peak efficiency of 96.4% at 2 kW as compared to 94.43% for CSVPWM.

Fig. 6.23 and 6.24 correspond to the active power support provided by the inverter in response to changes in solar irradiance. Step change in i^*_{gd} is applied corresponding to 2 kW and 3 kW which emulates the change in active power command generated from MPPT ($P_{PV,ref}$) using 6.12.

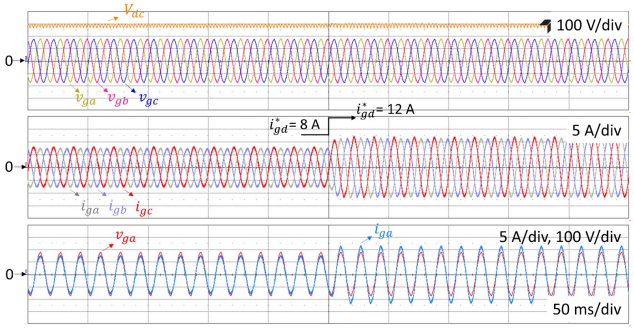

Figure 6.23: Experimental Waveforms of DC Link Voltage V_{dc}, Three-phase Voltages $v_{ga,gb,gc}$ and Inverter Currents $i_{ga,gb,gc}$ Corresponding to Active Power Support (Step Change in i^*_{gd} from 8 to 12 A) with 240CPWM in Grid-connected Mode.

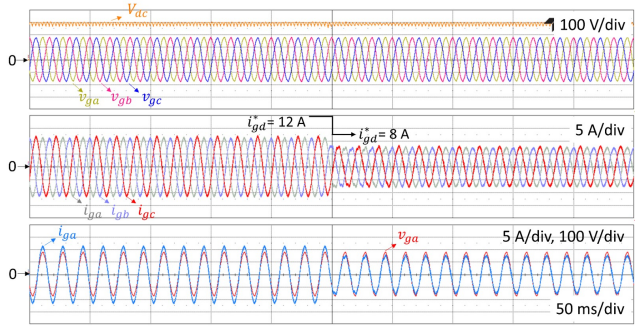

Figure 6.24: Experimental Waveforms of DC link voltage V_{dc}, Three-phase Voltages $v_{ga,gb,gc}$ and Inverter Currents $i_{ga,gb,gc}$ Corresponding to Active Power Support (Step Change in i^*_{gd} from 12 to 8 A) with 240CPWM in Grid-connected Mode.

6.4.1 Case I: Non-unity Power Factor

Experimental results are shown in Fig. 6.25 and Fig. 6.26 to access inverter performance with 240CPWM for grid over or undervoltage scenarios. In case of overvoltage condition on the grid side, the inverter absorbs the reactive power from the grid. To emulate this scenario of overvoltage condition on the grid side, the step change in i^*_{gq} is applied from 0 to 7 A. The leading power factor on the grid side is due to the reactive power absorbed by the inverter as shown in Fig. 6.25. The active power is maintained at 3 kW whereas a step change in i^*_{gq} corresponds to 1.78 kVARs reactive power absorbed by the inverter. A slight decrease in the DC link voltage after the step change in i^*_{gq} is observed. This voltage drop is constistent with 6.13

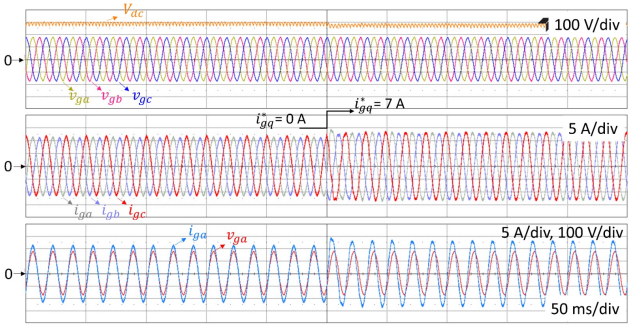

Figure 6.25: Experimental Waveforms of DC Link Voltage V_{dc}, Three-phase Voltages $v_{ga,gb,gc}$ and Inverter Currents $i_{ga,gb,gc}$ Corresponding to Reactive Power support (Step Change in i^*_{gq} from 0 to 7 A) with 240CPWM in Grid-connected Mode.

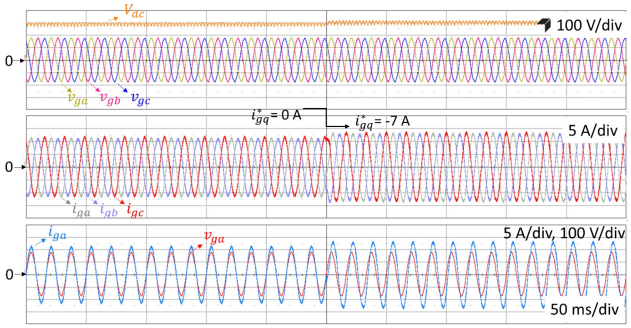

Figure 6.26: Experimental Waveforms of DC Link Voltage V_{dc}, Three-phase Voltages $v_{ga,gb,gc}$ and Inverter Currents $i_{ga,gb,gc}$ Corresponding to Reactive Power Support (Step Change in i^*_{gq} from 0 to -7 A) with 240CPWM in Grid-connected Mode.

[113].

Grid undervoltage condition is shown in Fig. 6.26 where the inverter injects reactive power into the grid to bring the voltage back in nominal range. To emulate this scenario of undervoltage condition on the grid side, the step change in i^*_{gq} is applied from 0 to $-$ 7 A. The lagging power factor on the grid side is due to the reactive power (1.78 kVARs) injected by the inverter as shown in Fig. 6.26. The small increase in the DC link voltage after the step change in i^*_{gq} from 0 to $-$ 7 A is observed that can be calculated from (6.13).

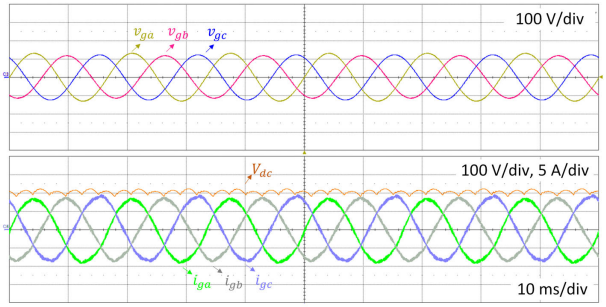

Figure 6.27: Experimental Waveforms of DC Link Voltage V_{dc}, Three-phase Voltages $v_{ga,gb,gc}$ and Inverter Currents $i_{ga,gb,gc}$ with 240CPWM in Grid-connected Mode under Grid Unbalance Condition.

6.4.2 Case II: Unbalance in grid voltages

Now the performance of 240CPWM in grid unbalance condition will be demonstrated. To introduce the unbalance in grid voltage, three phase programmable AC source (Chroma 61512) is used. This experiment is performed at 150 V ($V_{LL,RMS}$). Unbalance in grid voltage is applied such that v_{an} is 9% higher than nominal voltage, v_{bn} is at nominal voltage and v_{cn} is 8% lower than nominal voltage. This test is conducted at 1.6 kW (due to the limitations of the experimental setup with the grid simulator). The DC link voltage adapts as per the unbalance in grid voltages and inverter currents are balanced. Hence, 240CPWM works well in unbalanced grid conditions also without any need of additional control. The experimental results corresponding to grid unbalance condition is shown in Fig. 6.27.

6.4.3 Case III: Sag or swell in grid voltages

240CPWM is evaluated during sag and swell in grid voltages as shown in Fig. 6.28. In the grid simulator, four sequences are used to emulate the grid voltage sag and swell conditions as follows: In sequence 1 (S1), 12% swell in grid voltages is applied. Grid voltages are brought back to nominal value in sequence 2 (S2). In sequence 3 (S3), 6.5% sag in grid voltages is applied and they are brought back to nominal

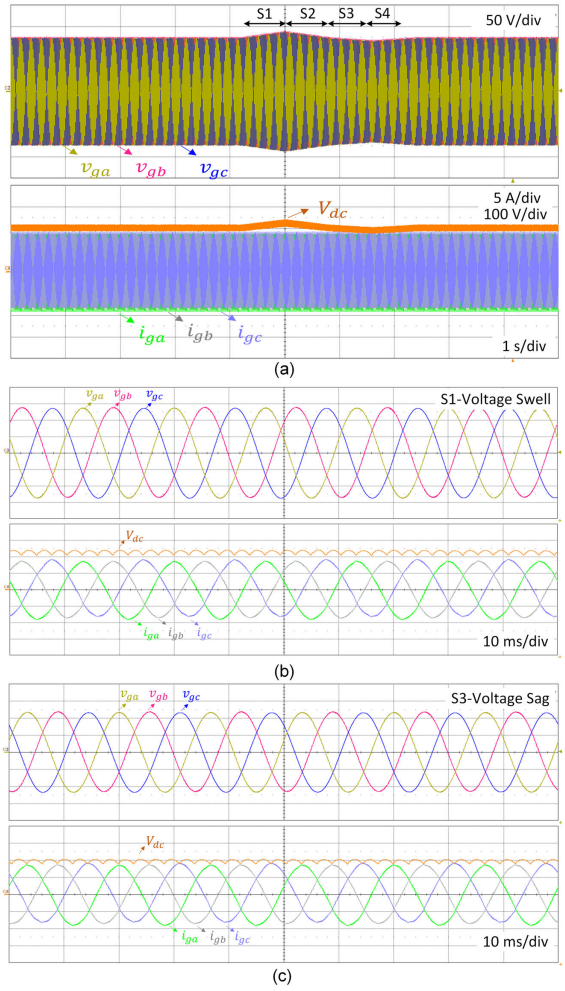

Figure 6.28: Experimental waveforms of DC link voltage V_{dc}, three-phase voltages $v_{ga,gb,gc}$ and inverter currents $i_{ga,gb,gc}$ with 240CPWM in grid-connected mode under (a) Voltage swell and sag conditions (b) zoomed in of Sequence S1 Corresponding to Voltage Swell (c) Zoomed in of Sequence S3 Corresponding to Voltage Sag.

voltage again in sequence 4 (S4). The DC link voltage adapts as per variation of grid voltages. Fig. 6.28 (a) shows the applied sag and swell in grid voltages marked as S1-S4 where the DC-link voltage adapts according to the applied sag/swell in grid voltages and inverter currents remain unchanged as expected. The zoomed in result of voltage swell condition (Sequence S1) is shown in Fig. 6.28 (b) whereas voltage sag condition (Sequence S3) is shown in Fig. 6.28 (c).

6.5 Conclusion

240CPWM is a relatively new PWM method that allows tremendous saving in switching loss as compared to conventional PWM methods due to 240° clamping in a fundamental cycle. Six pulse dynamic DC link voltage is required for 240CPWM instead of constant voltage which is provided by the DC-DC converter in close loop control. This work explores the operation of 240CPWM in three phase grid connected PV converters using PI and HC controller under various grid disturbances like sag/swell and unbalance in grid voltages. 10% unbalance, 6.5% sag and 12% swell in grid voltages is applied in the experiments using the grid simulator. The DC link voltage quickly adapts to these disturbances maintaining sinusoidal and balanced grid currents. Also, the experimental results at non-unity power factors are presented with 240CPWM for the first time. Undesired low frequency dominant harmonics in inverter currents are minimized using the HC controller that results in THD of 3.5% with 240CPWM in compliance with the IEEE-1547 grid interconnection standard. The coordinated control of both the DC-DC converter and DC-AC inverter is shown that allows synchronism between the grid voltages and dynamic DC link voltage. Hence, the implemented control scheme of low-loss 240CPWM in grid connected PV converter achieves smooth operation under non-unity powerfactor and grid disturbance conditions while maintaining THD as 3.5% and peak combined efficiency of DC-DC and DC-AC stage as 96.4% as compared to 94.43% for CSVPWM.

Chapter 7

PERFORMANCE METRICS OF 240CPWM IN THREE PHASE TRANSFORMERLESS GRID-CONNECTED PV CONVERTERS

7.1 Introduction

Distributed generation (DG) systems based on photovoltaic (PV) power have gained greater visibility over the past two decades to address the environmental concerns caused by excessive use of fossil fuels [114]. Traditionally, a line frequency transformer (60 Hz) is placed between the inverter and grid to match the grid voltage level and offer galvanic isolation. This line frequency transformer incurs additional power losses, makes the whole system heavy compromising on power density and cost [115]. Transformerless grid-connected voltage source inverters (VSIs) are now widely used in PV systems due to their low cost, small size and high efficiency [105], [116]. However, absence of a galvanic isolation in transformerless grid-connected VSIs causes the leakage current to flow through the solar panel's parasitic capacitance to ground. Depending upon the topology and the modulation method used, the leakage current can cause severe electromagnetic interference, high line current distortion, with additional losses in the system and safety hazard [117], [118].

In a transformerless grid-connected PV system, the inverter is expected to inject high quality current into the grid [110]. For the interconnection of a DG system with grid, the total harmonic distortion (THD) value of the grid current must be less than 5% according to the IEEE 1547 standard [119]. Moreover, the German standard VDE0126-1-1 specifies that the leakage current should be limited to 300 mA [41]. To reduce the CMV and leakage current in transformerless grid-

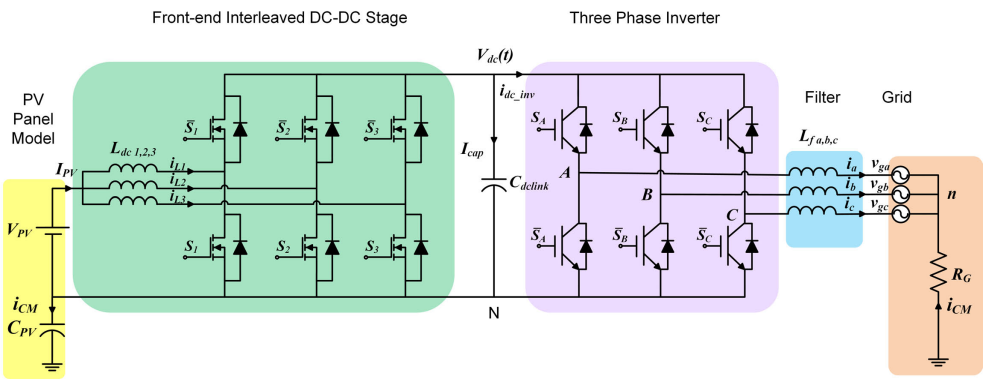

Figure 7.1: Block Diagram of a Two-stage, Grid-connected PV Converter Showing the Leakage Current Path.

connected PV systems, [120], [121] and algorithmic (PWM) solutions have been proposed [49, 122, 123, 124, 125]. With the advancement in digital signal processing technology, the PWM based algorithmic solutions are preferred because they improve the performance without compromising on cost and power density. Various modulation methods i.e., Reduced CMV PWM (RCMV-PWM) methods [49] such as Active Zero State PWM (AZSPWM) [122, 123], Remote State PWM (RSPWM) [124] and Near State PWM (NSPWM) [125] are discussed in literature to reduce CMV and leakage current. The RCMV-PWM methods effectively reduce the CMV and leakage current but typically at the expense of increased THD, switching loss, DC-link current stress with limited modulation index operation. In RCMV-PWM methods, the output line-to-line voltage is bipolar; the drawbacks are high dv/dt, large current ripples across filter inductors, and high switching losses that reduce the system efficiency [126].

240° Clamped space vector PWM (240CPWM) is among the lowest switching loss PWM methods. It effectively reduces the CMV and leakage current while ensuring lower switching loss and similar THD as compared to Conventional Space Vector PWM (CSVPWM) without requiring any hardware changes in the PV converter. 240CPWM requires a cascaded topology of DC-DC stage followed by DC-AC stage

where the DC-DC stage controls the dynamic DC link voltage needed for 240CPWM. In PV systems, DC-DC stage followed by DC-AC stage is a standard configuration [127, 128]. Hence, 240CPWM can be used in such two-stage, three-phase PV systems without increasing the component count or modifying the topology, by making use of the available DC-DC stage to generate the required dynamically variable DC link voltage. 240CPWM was first introduced for grid-connected PV application [98, 99, 100, 101, 102] and later for motor drives [61, 82, 103, 81] and battery chargers [62], [129]. Considering the grid-connected PV application of 240CPWM, the operating principle of 240CPWM is discussed in [98]. Switching loss analysis with 240CPWM is carried out in [102]. Common mode characteristics of 240CPWM in motor drives are discussed using a high frequency motor model in [82]. However, study on CMV and leakage current performance of 240CPWM in grid-connected PV inverter is non-existent in literature. Moreover, comprehensive and combined analysis of CMV, leakage current, DC link current stress, switching loss over the entire range of power factor and THD for 240CPWM and its comparison with conventional PWM methods in grid-connected PV inverter has not been presented before, and is one of the main contributions of this paper.

Fig. 7.1 shows the commonly used three-phase grid-connected PV converter under consideration where the DC-DC stage is a three-phase interleaved boost converter and the DC-AC stage is a two-level, three-phase inverter. We have used a three-phase interleaved boost converter in the DC-DC stage which is a commonly used configuration for higher power PV systems. Moreover, it reduces the input current ripple and improves the control bandwidth but a standard single-phase boost converter can be used as well. To assess the performance of PV converter system, the combined efficiency of both the DC-DC stage and DC-AC stage is required. The previous studies on 240CPWM in grid-connected PV converter have reported only the efficiency of the

DC-AC stage alone [98, 99, 100, 101, 102]. In this work, the peak combined efficiency of 96.4% is achieved at 2 kW with 240CPWM including both the DC-DC and DC-AC stage. Leakage path in transformerless grid connected PV inverters comprises of stray capacitance C_{PV} between the PV module and ground, and ground resistance R_G. It depends on various factors like PV panel, frame structure and weather conditions. C_{PV} is estimated to be 150-200 nF/kWp [94], [130], and at typical high power ratings of three phase grid connected PV inverters, C_{PV} also ranges from hundreds of nF to uF range that becomes the dominating factor of leakage current. Technical information documents from SMA provide the detailed calculation of C_{PV} for transformerless inverters where C_{PV} is estimated with different modules types assuming a continuous film of water on the glass surface [131, 132]. Standard module with crystalline silicon cells (monocrystalline, polycrystalline) has C_{PV} of 330 nF to 550 nF for a 5 kW PV system and thin-film module has C_{PV} of 500 nF to 800 nF for a 5 kW PV system. The value of C_{PV} is taken as 400 nF in this work corresponding to 3 kW experimental prototype. Value of R_G is uncertain, usually around few ohms. Based on thorough literature survey of transformerless grid connected PV inverters, R_G is taken as 10 Ω in this study [133, 134, 135, 136]. The main contributions of this work are listed as follows:

1. Comprehensive analysis and experimental validation of CMV and leakage current characteristics of 240CPWM for a transformerless grid-connected PV converter using the leakage path parameters corresponding to actual PV systems;

2. Detailed study on the leakage current considering all the lower and higher order harmonic components of the CMV (up to 150 kHz) in grid-connected PV application for all the PWM methods considered. Existing literature such as [42] on leakage current for any PWM method only account for the switching frequency

harmonic component of CMV, whereas leakage current depends strongly on higher order harmonics as well;

3. Rigorous analytical, simulation and experimental study on all the main performance metrics for a PV converter including THD, switching loss, DC link current stress, CMV and leakage current are carried out for 240CPWM and compared with other conventional methods. A new, combined performance index is proposed to compare the performance of different PWM schemes.

4. Extensive hardware results from a 3 kW, 208 V prototype are presented to fully validate the presented analysis and the superior performance of 240CPWM. It is shown experimentally that 240CPWM

   - improves light load efficiency by 5.5% and CEC[1] efficiency by 2.4%
   - reduces THD by 54%
   - reduces DC link current stress by 29%
   - reduces peak CMV by 66.7%
   - reduces leakage current by 50%

   as compared to CSVPWM at unity power factor without any changes in hardware.

7.2 Analysis on CMV and Leakage Current with 240CPWM

CMV of three phase inverter is defined as $v_{cm} = (v_{AN} + v_{BN} + v_{CN})/3$, where v_{AN}, v_{BN} and v_{CN} are the three phase voltages of inverter with respect to DC link negative [42]. Zero states (0 and 7) and active states (such as 1 and 2 in Sector I)

[1]California Energy Commission

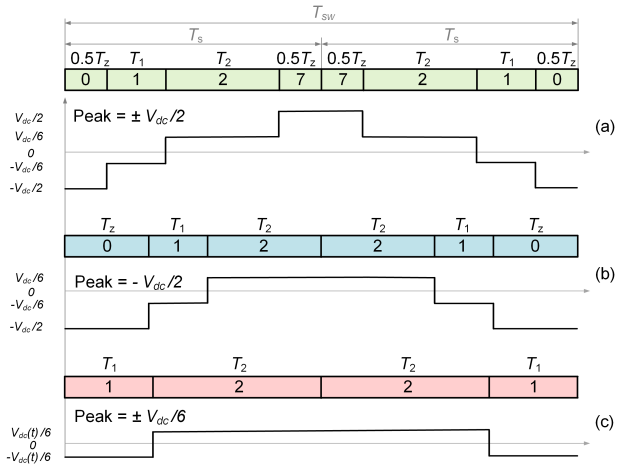

Figure 7.2: Switching Sequence and Corresponding CMV in a Switching Cycle of (a) CSVPWM, (b) DPWM1 and (c) 240CPWM.

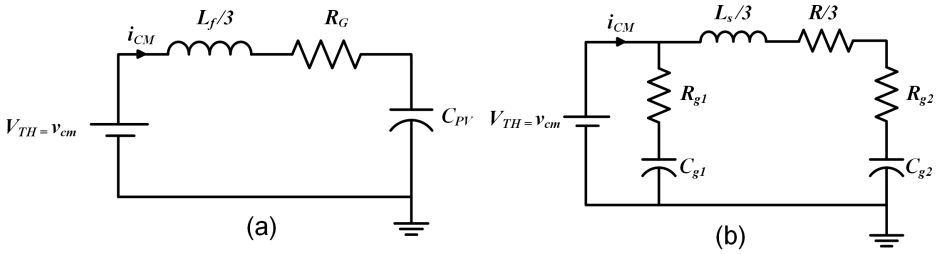

Figure 7.3: Common Mode Equivalent Circuit for (a) Grid-connected PV Inverter (b) Induction Machine for Motor Drive.

cause peak CMV magnitude of $\pm V_{dc}/2$ and $\pm V_{dc}/6$ respectively where V_{dc} is the DC link voltage. CSVPWM and DPWM1 use both the zero states causing peak CMV of $\pm V_{dc}/2$ while 240CPWM does not use any zero state which reduces the peak CMV to just $\pm V_{dc}/6$. CMV waveforms of all PWM methods under consideration and their switching sequences in a sub-cycle are shown in Fig. 7.2.

RMS value of CMV ($V_{CM,RMS}$) is used as an important metric to determine the common mode performance of a PWM method which is given by (7.1):

$$V_{CM,RMS} = \frac{2}{V_{dc}} \sqrt{\frac{1}{2\pi} \int_0^{T_s} V_{cm}^2 \, d\theta} \tag{7.1}$$

Detailed analysis of CMV for 240CPWM is presented in [63] for motor-drive applica-

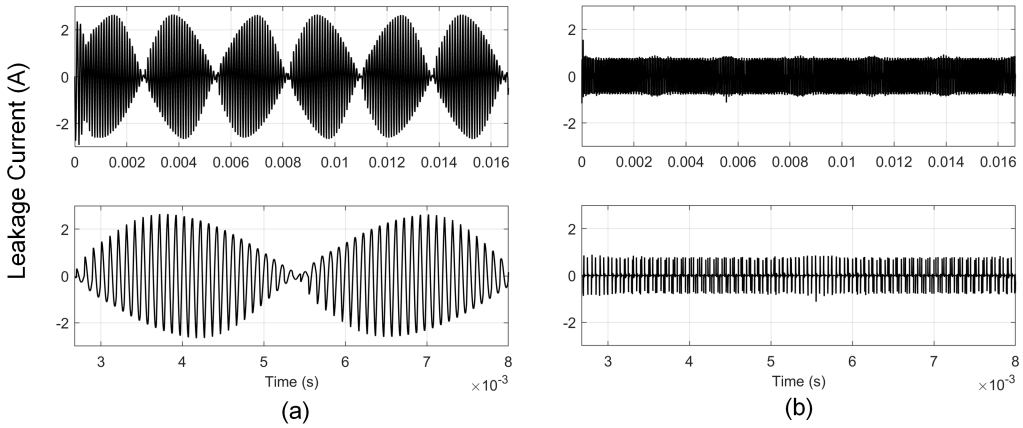

Figure 7.4: Simulated Leakage Current at 3 kW (a) Grid-connected PV Application (b) Motor Drive Application (Top: Leakage Current, Bottom: Zoomed In).

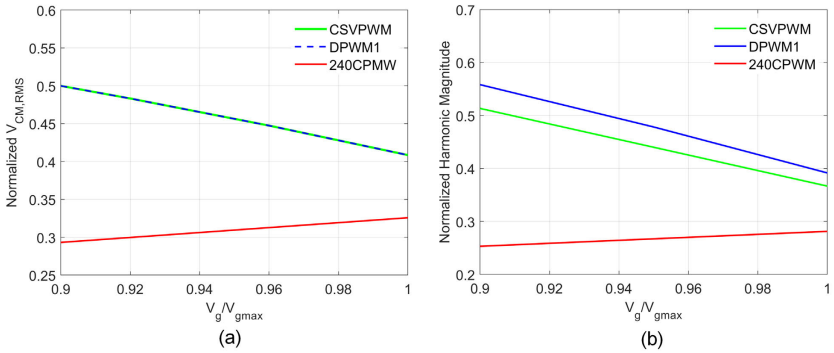

Figure 7.5: (a) RMS value of CMV (b) Switching Frequency Harmonic Component of CMV, All Normalized with Respect to $V_{dc}/2$ Against Normalized Grid Voltage (Grid Voltage Normalized with Respect to Maximum Grid Voltage).

tions which is expanded here for grid-connected PV application.

In terms of leakage current, grid connected PV system is very different from a motor drive application. Thevenin equivalent models to calculate leakage current for grid-connected PV converter and motor drive applications are shown in Fig. 7.3 where V_{TH} is the Thevenin voltage which is the common mode voltage. In motor drive applications, leakage current is mainly dependent on dv/dt of inverter and partially on CMV magnitude and waveshape because the parasitic or stray capacitance of a typical motor is very small (nano farads range) that makes the resonant frequency

Table 7.1: Specifications of PLECS Simulation and Experimental Setup.

	Parameter	Value
DC-DC Stage	Input voltage V_{PV}	150 V
	DC link Voltage peak for 240CPWM $V_{dc,pk}$	300 V
	Number of interleaved phases n	3
	Inductance L_{dc}	560 uH
	DC link Capacitance C_{dc}	20 uF
	Switching frequency $f_{sw,dcdc}$	50 kHz
DC-AC Stage	Output Power P	3 kW
	Grid voltage v_g (line-to-line RMS)	208 V
	Filter Inductance L_f	3 mH
	Switching frequency $f_{sw,dcac}$	10 kHz
	Grid frequency f_1	60 Hz
Leakage Path	Resistance R_G	10 Ω
	Capacitance C_{PV}	0.4 uF

very high. The common mode behavior of induction machine used in motor drives is mainly capacitive. The high dv/dt at machine terminals causes voltages on the machine bearing via the high-frequency (HF) machine capacitances leading to adverse effects such as shaft voltage, bearing current, leakage current and EMI [137]. In Fig. 7.3 (b), C_g is the distributed parasitic capacitance between stator winding of motor and grounded motor frame, L_s is the stator leakage inductance and R_g is the motor frame resistance. The leakage capacitance and resistance between stator winding of motor and grounded motor frame are divided into low frequency (LF) leakage path using C_{g1} and R_{g1} and HF leakage path using C_{g2} and R_{g2} [137, 137]. However, in grid connected PV converter the stray capacitance of PV module can be lumped as a single

capacitance C_{PV} and its value ranges from hundreds of nF to uF range. This changes the magnitude as well as shape of leakage current significantly in grid-connected PV system as compared to the motor drive system.

The common mode (CM) equivalent circuits in Fig.7.3 are used to calculate the leakage current for both the grid connected PV converter and motor drive system at 3 kW corresponding to the experimental set-up conditions as shown in Fig. 7.4. Consistent with exisiting literature, the value of C_{PV} is taken as 400 nF and value of R_G is taken as 10 Ω [133, 134, 135, 136] for grid-connected PV converter. For motor drive application, the values of distributed parasitic capacitances and motor frame resistances are taken from [137] i.e., C_{g1} = 0.33 nF, R_{g1} = 100 Ω, C_{g2} = 1.65 nF, R_{g2} = 220 Ω. The leakage current amplitude as well as the width of leakage current in grid-connected PV system (Fig. 7.4 (a)) is much higher as compared to the motor drive application (Fig. 7.4 (b)).

Because of the large stray capacitance in PV system, resonant frequency of common-mode circuit is closer to PWM frequency such that the CMV magnitude plays a more significant role in determining leakage current [94]. Thus, a PWM method with low CMV magnitude and low RMS value becomes suitable candidate to reduce the leakage current. 240CPWM has 66.77% lower CMV peak (Fig. 7.2) and 21% lower $V_{CM,RMS}$

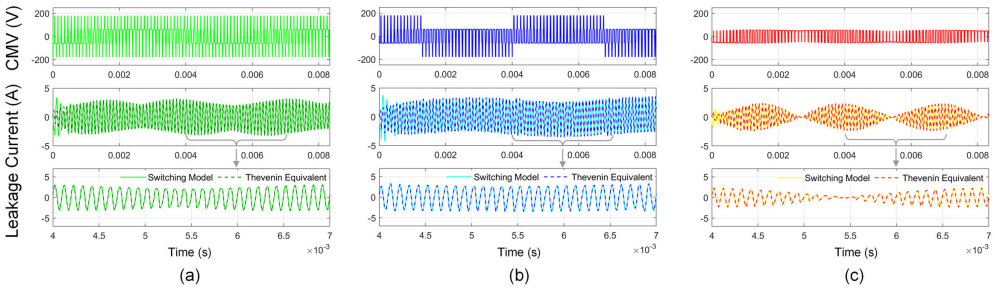

Figure 7.6: PLECS Simulation Waveforms of CMV (top), Leakage Current from Full Switching Model and Thevenin Equivalent Model of CM Circuit (Middle) and Zoomed In Versions (Bottom) (a) CSVPWM, (b) DPWM1, (c) 240CPWM.

(Fig. 7.5 (a)) as compared to CSVPWM (at maximum modulation index).

Harmonic magnitude of CMV gives insight to the leakage current [138]. Double Fourier integral analysis is deployed to analyze the spectrum of CMV [139]. CMV v_{cm} of a VSI is a function of harmonic component of phase leg output voltage C_{mn} which is given as follows:

$$v_{cm} = \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} C_{mn} \cos(m\omega_c t + n\omega_o t)$$
$$n = 3p, p = 0, 1, 2... \tag{7.2}$$

$\omega_c = 2\pi f_c$ and $\omega_o = 2\pi f_o$ are the carrier angular frequency and fundamental angular frequency, respectively. Carrier index variable m and the fundamental index variable n define the (angular) frequency of each harmonic component of the switched phase leg output voltage. Using the double Fourier integral analysis, the harmonic components of phase leg output voltage C_{mn} can be calculated using the following expression.

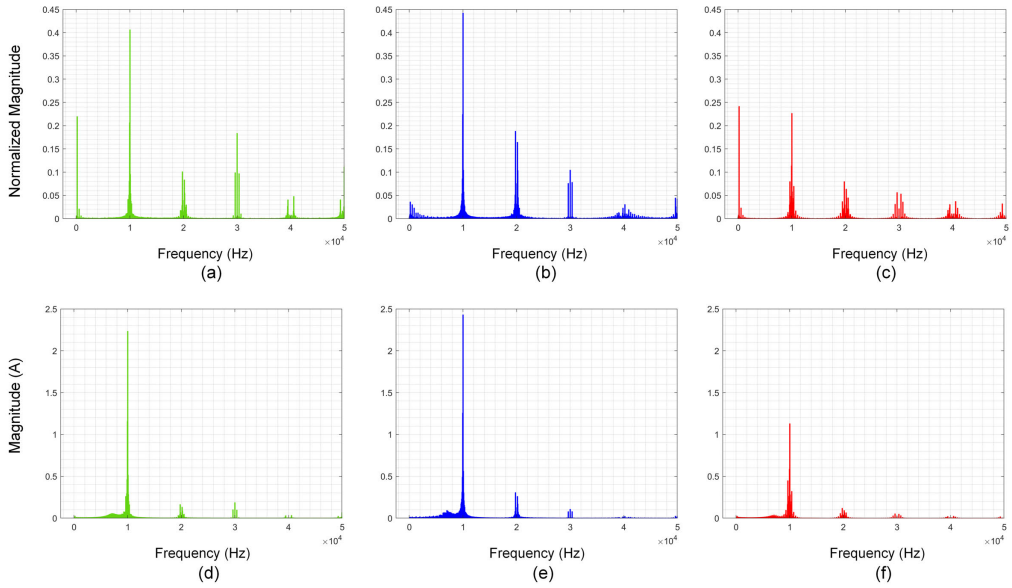

Figure 7.7: FFT of CMV from PLECS simulation at 3 kW (a) CSVPWM, (b) DPWM1, (c) 240CPWM. FFT of Leakage Current (d) CSVPWM, (e) DPWM1, (f) 240CPWM.

$$C_{mn} = \frac{1}{2\pi^2} \sum_{i=0}^{6} \int_{y_s(i)}^{y_e(i)} \int_{x_r(i)}^{x_f(i)} V_{dc} e^{j(mx+ny)} dxdy \tag{7.3}$$

$y_s(i)$, $y_e(i)$, $x_r(i)$ and $x_f(i)$ are outer and inner double Fourier integral limits. $x(i)$ can be thought of as a high frequency modulating wave and $y(i)$ as the low frequency modulated wave such that both of them are independently periodic. Fig. 7.5 (b) gives the variation of switching frequency harmonic component of CMV for all PWM methods under consideration against normalized grid voltage.

Trends of leakage current can be obtained from Fig. 7.5 (b) corresponding to switching frequency harmonic of CMV in PV application. For example, leakage current of DPWM1 will be slightly higher than CSVPWM in high modulation index range while 240CPWM will have the lowest value. To analytically calculate RMS leakage current, harmonic components of CMV (switching frequency harmonics and its sidebands) need to be considered. With harmonic component of CMV, leakage current can be obtained analytically from the CM equivalent circuit (or Thevenin equivalent circuit of Fig. 7.1) which is given in Fig. 7.3. The resonance frequency $f_{r,cm}$ of this common mode circuit is given by:

$$f_{r,cm} = \frac{1}{2\pi\sqrt{C_{PV} L_f/3}} \tag{7.4}$$

CMV and leakage currents from PLECS simulation both with switching model and Thevenin equivalent model corresponding to the parameters in Table 7.1 are shown in Fig. 7.3. The close match of leakage current obtained from PLECS switching model and Thevenin equivalent model validates the accuracy of the latter.

Using (7.2) and (7.3), leakage current $I_{cm,h}$ corresponding to individual harmonic of CMV $V_{cm,h}$ can be obtained as follows:

$$I_{cm,h} = \frac{V_{cm,h}}{R_G + 1/j\omega C_{PV} + j\omega L_f/3} \tag{7.5}$$

Harmonic components of CMV are taken up to 150 kHz in analysis to get accurate analytical values of leakage current. Total leakage current I_{cm} is obtained by adding all the harmonics of $I_{cm,h}$ as follows:

$$I_{cm} = \sqrt{\sum_{m=1}^{15}\sum_{n=0}^{18} {I_{cm,h}}^2} \tag{7.6}$$

$n = 3p$, $p = 0, 2, 4, 6$ for odd m, $p = 1, 3, 5$ for even m, where $n = 0$ to 18 represents fundamental frequency sidebands of corresponding switching frequency harmonic m.

Harmonic components of CMV and leakage current for switching frequency harmonics and its dominant sidebands are shown in Table 7.2. The table shows that switching frequency component (i.e., 10 kHz) of CMV and leakage current for all PWM methods is the most dominant one as explained earlier.

Table 7.3 shows the $V_{CM,RMS}$ and $I_{CM,RMS}$ obtained from analysis and simulation for all PWM methods at maximum modulation index. 240CPWM results in 21% saving in $V_{CM,RMS}$ and 15.2% saving in $I_{CM,RMS}$ as compared to CSVPWM. Saving in $I_{CM,RMS}$ due to 240CPWM is 21.5% as compared to DPWM1. A close match between analysis and simulation is observed because harmonics of CMV up to 150 kHz are considered for analytically calculating the leakage current.

Table 7.4 shows the $V_{CM,RMS}$ and $I_{CM,RMS}$ obtained from analysis and simulation for all PWM methods under consideration corresponding to experimental conditions. In our experimental set-up, CSVPWM and DPWM1 are limited at $0.91M_{max}$ due to large dead time of Si IGBTs.

The resonant frequency of common mode circuit for our experimental setup (L_f = 3 mH, C_{PV} = 0.4 uF) comes out to be 7.96 kHz. Leakage currents of all PWM

Table 7.2: Harmonic Components of CMV and Leakage Current for Switching Frequency Components and its Sidebands for CSVPWM, DPWM1 and 240CPWM.

			CSVPWM		DPWM1		240CPWM	
m	n	f_H/f_L	$V_{cm,h}$	$I_{cm,h}$	$V_{cm,h}$	$I_{cm,h}$	$V_{cm,h}$	$I_{cm,h}$
0	3	180	0.238	0.022	0.153	0.0014	0.241	0.0188
0	9	540	0.0238	0.0067	0.0033	0.0009	0.03478	0.0082
0	15	900	0.0085	0.004	0.0001	0.00004	0.00128	0.0005
1	0	10000	0.36	2.086	0.39	2.2599	0.2813	1.362
1	6	10360/ 9640	0.0365	0.1909/ 0.2374	0.0195	0.102/ 0.1268	0.0867	0.379/ 0.4716
1	12	10720/ 9280	0.0048	0.0227/ 0.0353	0.0006	0.0027/ 0.0043	0.0213	0.0849/ 0.1321
1	18	11080/ 8920	0.002	0.0088/ 0.0173	0.00007	0.0003/ 0.0006	0.0083	0.0303/ 0.0596
2	3	20180/ 19820	0.105	0.1679/ 0.1719	0.1695	0.2711/ 0.2775	0.0929	0.124/ 0.1271
2	9	20540/ 19460	0.039	0.0609/ 0.0654	0.01	0.0156/ 0.01677	0.0491	0.0642/ 0.0688
2	15	20900/ 19100	0.009	0.0138/ 0.0154	0.0004	0.0006/ 0.00069	0.0145	0.0185/ 0.021

Table 7.3: Comparison of RMS CMV and Leakage Current for CSVPWM, DPWM1 and 240CPWM Obtained from Analysis and PLECS Simulation at M_{max}.

PWM Method	$V_{CM,RMS}$ (V)		$I_{CM,RMS}$ (A)	
	Analysis	Simulation	Analysis	Simulation
CSVPWM	72	73	1.50831	1.56
DPWM1	72	73	1.63103	1.7
240CPWM	57.5	58	1.28	1.3

Table 7.4: Comparison of RMS CMV and Leakage Current for CSVPWM, DPWM1 and 240CPWM Obtained from Analysis and PLECS Simulation Corresponding to Experimental Conditions.

PWM Method	$V_{CM,RMS}$ (V)		$I_{CM,RMS}$ (A)	
	Analysis	Simulation	Analysis	Simulation
CSVPWM	85.3	85.8	1.95	1.98
DPWM1	85.3	86	2.11	2.16
240CPWM	48.05	51	1.073	1.09

methods under consideration is highest at carrier frequency (shown in Fig. 7.7). This is mainly due to resonance. In PV applications, due to large C_{PV}, resonant frequency of common mode circuit $f_{r,cm}$ is very close to the carrier frequency. So, there is always a risk of exciting the resonance which happens in our experimental setup too. So, PWM method with less CVM and less harmonic magnitude of CMV at switching frequency will cause small leakage current which is the case of 240CPWM. FFT of CMV and leakage current for CSVPWM, DPWM1 and 240CPWM are shown in Fig. 7.7 from PLECS simulation at 3 kW corresponding to experimental conditions. It can be observed that leakage current for all PWM methods under consideration have highest magnitude at 10 kHz.

The impedance of common mode circuit against frequency is plotted in Fig. 7.8.

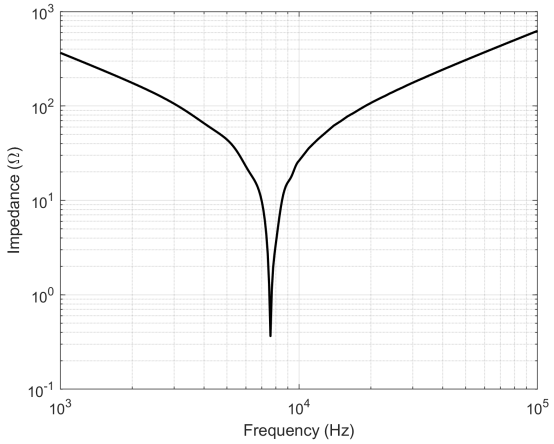

Figure 7.8: Impedance of Common Mode Circuit Against Frequency.

It shows that the impedance at high and low frequencies is very high, thus leakage current is low at such frequencies. The circuit becomes inductive in nature at high frequencies, so CMV with large magnitude at those frequencies cannot force high leakage currents. Close to resonant frequency (7.6 kHz), impedance of common mode circuit is very low. So, if CMV has harmonic components close to resonant frequency, leakage currents will be very high. For all PWM methods under consideration, CMV has a dominant component at switching frequency i.e., 10 kHz. So, PWM method with lowest harmonic component of CMV at 10 kHz will force lowest leakage current which is the case of 240CPWM.

7.3 Switching Loss, THD and DC Link Current Stress

7.3.1 Switching Loss Analysis

Switching loss performance of a PWM method can be evaluated by analyzing the switching energy loss in every sub-cycle [48]. For a given phase, normalized switching energy loss in every sub-cycle ($P_{SUB,PH}$) is given by the product of normalized DC link voltage ($V_{dc,norm}$), number of switching in a phase (n_{PH}) and the instantaneous line current in that phase (i_{PH}) in the sub-cycle.

To analyze the switching loss variation for a given PWM method over a sector, switching loss in a sub-cycle $P_{SUB,TOT}$ is used which is just the sum of $P_{SUB,PH}$ for three phases i.e., $P_{SUB,A}+P_{SUB,B}+P_{SUB,C}$. A well known metric called normalized switching loss (P_{SW}) is used to compare different PWM methods in terms of switching loss which is defined as the ratio of averaged $P_{SUB,TOT}$ for a given PWM method over a sector to the average $P_{SUB,TOT}$ for CSVPWM. P_{SW} facilitates the comparative evaluation of various techniques using switching losses of all three phases at different power factor angles.

$$P_{SW} = \frac{1}{2}\int_0^{\pi/3} P_{SUB,TOT}\ \mathrm{d}\alpha \tag{7.7}$$

Fig. 7.9 shows the variation of P_{SW} against the entire power factor angle range i.e., -90° to 90°. P_{SW} is symmetric around zero because of the symmetry in switch current at leading and lagging power factor angles. Because of complete elimination of zero states in 240CPWM, only one phase switches at any given instant and the other two remain clamped to positive or negative DC rail. At unity power factor (UPF), switching for the single phase is centered around zero crossing of current leading to tremendous saving in switching loss for 240CPWM as compared to CSVPWM. P_{SW} is lowest for 240CPWM in the entire power factor angle range as compared to CSVPWM and DPWM1. 85% saving in switching loss is obtained at unity power factor for 240CPWM as compared to CSVPWM. The highlighted area shows the operation of interest for most PV applications i.e., from power factor of -0.8 to 0.8 ($\phi = -37°$ to $\phi = 37°$).

Fig. 7.10 presents the power loss breakdown of DC-AC inverter for all PWM methods under consideration and DC-DC converter. For DC-AC inverter, switching loss is very different for CSVPWM, DPWM1 and 240CPWM. Conduction loss for DC-AC inverter remains the same because of equal RMS current through the switches for each PWM method. Saving in switching loss for 240CPWM as compared to CSVPWM

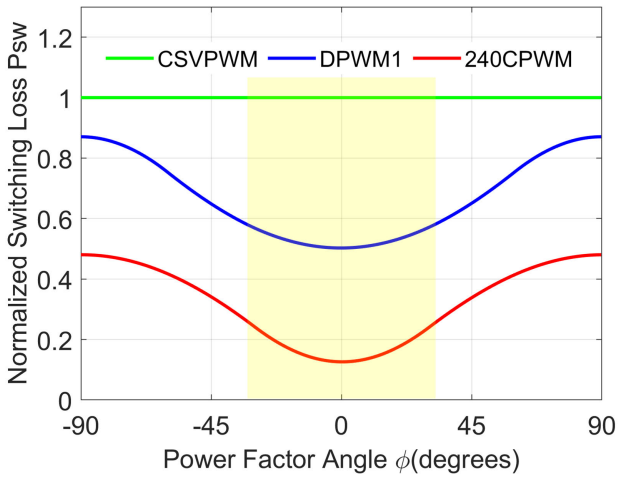

Figure 7.9: Variation of P_{SW} for All PWM Methods under Consideration Against Power Factor Angle.

conforms to the analysis i.e., 240CPWM results in seven times less switching loss as compared to CSVPWM at unity power factor. Loss breakdown for DC-DC stage is also shown in Fig. 7.10 (d) which is assumed to be same in all three cases, which is confirmed from simulation results.

7.3.2 THD Analysis

Stator flux ripple refers to the time integral of the error between the reference voltage vector and applied voltage vector at any given instant. The total RMS line current ripple can be calculated using RMS harmonic distortion factor, F_{DIST} which is given by the RMS stator flux ripple over a sector normalized with respect to the fundamental flux [140]. Analytical evaluation of harmonic distortion using F_{DIST} for 240CPWM and its comparison with CSVPWM and DPWM1 is discussed in detail for motor drive application in [82]. The variation of fundamental voltage in motor drives is according to the constant V/f mode such that the voltage changes proportionally with the speed. Hence, the voltage variation in motor drives is wide i.e., it ranges from very low values (close to zero) to the maximum value and so is the modula-

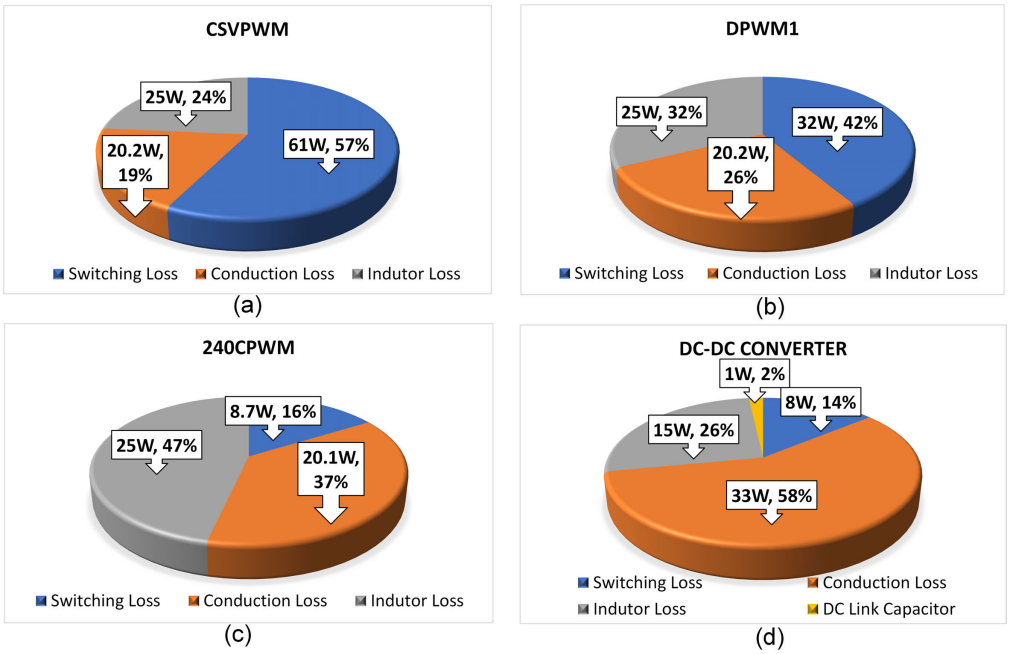

Figure 7.10: Loss Breakdown at 3 kW (Unity Power Factor) from PLECS Simulation. DC-AC Inverter (a) CSVPWM, (b) DPWM1, (c) 240CPWM, (d) DC-DC Converter.

tion index variation. However, the variation in grid voltage does not exceed $\pm 10\%$, hence the modulation index variation is from $0.9M_{max}$ to $1.1M_{max}$ in grid connected PV converter. The variation of harmonic distortion based on stator flux ripple for CSVPWM and DPWM1 corresponding to the variation in modulation index from $0.9M_{max}$ to M_{max} is shown in Fig. 7.11. 240CPWM operates at maximum modulation index irrespective of grid over/under voltage conditions. If there is a variation in grid voltage magnitude, then DC link voltage adapts accordingly so that 240CPWM operates at maximum modulation index. 240CPWM has similar THD as compared to CSVPWM at M_{max}.

7.3.3 DC Link Current Stress

Analysis on inverter side contribution to RMS DC link current is carried out in detail in [79] for CSVPWM. Due to the elimination of zero states in 240CPWM,

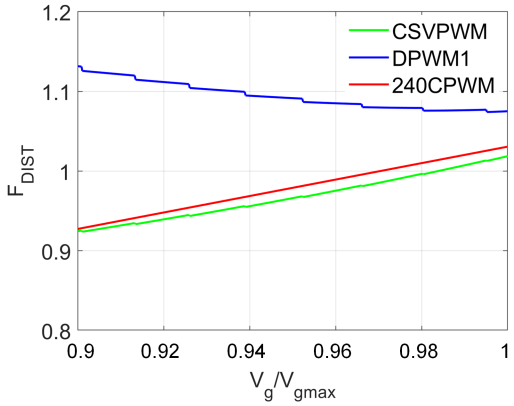

Figure 7.11: Normalized F_{DIST} Against Normalized Grid Voltage (Grid Voltage Normalized with Respect to Maximum Grid Voltage). F_{DIST} is Normalized with Respect to the Stator Flux Ripple Distortion of CSVPWM.

variation in current drawn by the inverter is reduced which in turn reduces the DC link capacitor current stress. The instantaneous DC link current due to inverter stage (i_{dc_inv}) is shown in Fig. 7.12 in one switching cycle for CSVPWM, DPWM1 and 240CPWM and it is given by:

$$i_{dc\_inv} = G_{S_A} i_a + G_{S_B} i_b + G_{S_C} i_c \tag{7.8}$$

Where G_{S_A}, G_{S_B} and G_{S_C} are the switching signals of inverter top switches S_A, S_B and S_C respectively and i_a, i_b and i_c are the line currents of the inverter. Corresponding to zero state (0 or 7) in CSVPWM and DPWM1, i_{dc_inv} becomes zero that forces high DC link capacitor current at those instants. RMS value of i_{dc_inv} in a subcycle i.e., $I_{dc\_inv,sub}$ can be calculated from RMS and average values of i_{dc_inv} as follows [103]:

$$I_{dc\_inv,sub} = \sqrt{i^2_{dc\_inv,rms} - i^2_{dc\_inv,avg}} \tag{7.9}$$

Variation of $I_{dc\_inv,sub}$ against sector angle α is shown in Fig. 7.13 for CSVPWM, DPWM1 and 240CPWM at different power factor angles. Since effect of current ripple

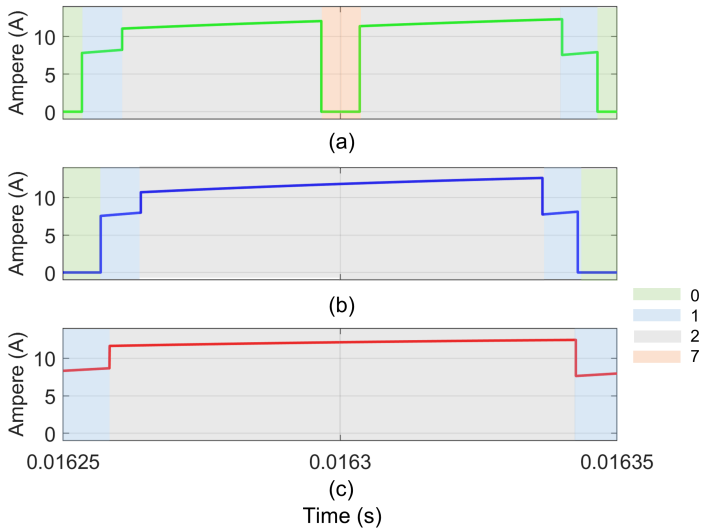

Figure 7.12: Simulation Results of i_{dc_inv} in One Switching Cycle in Sector I near Peak Inverter Current (a) CSVPWM, (b) DPWM1 and (c) 240CPWM.

is ignored, $I_{dc\_inv,sub}$ for CSVPWM and DPWM1 is similar because total duration of applied zero state is same in both the PWM methods. 240CPWM does not use any zero state. Hence, the variation in $I_{dc\_inv,sub}$ is reduced with 240CPWM as shown in Fig. 7.13.

DC link capacitor current stress determines the size of DC link capacitor. It is a strong function of PWM method and power factor angle. RMS value of current drawn by the inverter (RMS over fundamental period) normalized with respect to RMS value of line current i.e., $I_{dc\_inv,rms}$ is used to compare DC link capacitor current

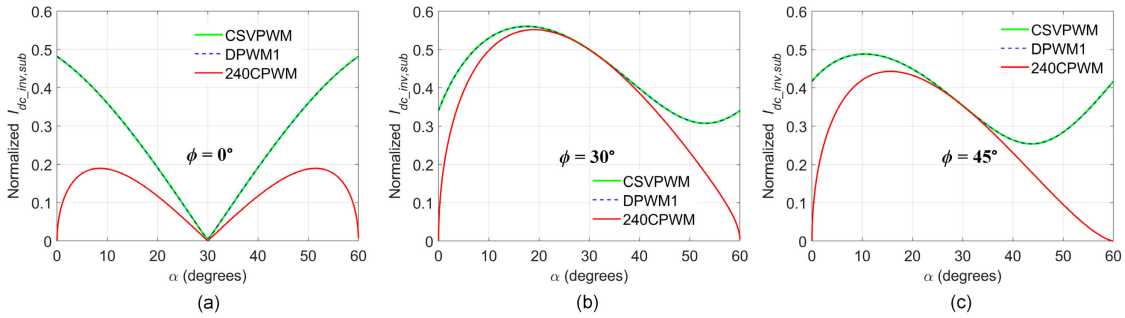

Figure 7.13: Variation of Normalized $I_{dc\_inv,sub}$ Against α (Normalized with Respect to RMS Line Current) (a) $\phi = 0°$, (b) $\phi = 30°$ and (c) $\phi = 45°$.

stress and it is given by:

$$I_{dc\_inv,rms} = \frac{3}{\pi}\int_0^{\pi/3} I_{dc\_inv,sub}\ \mathrm{d}\alpha \tag{7.10}$$

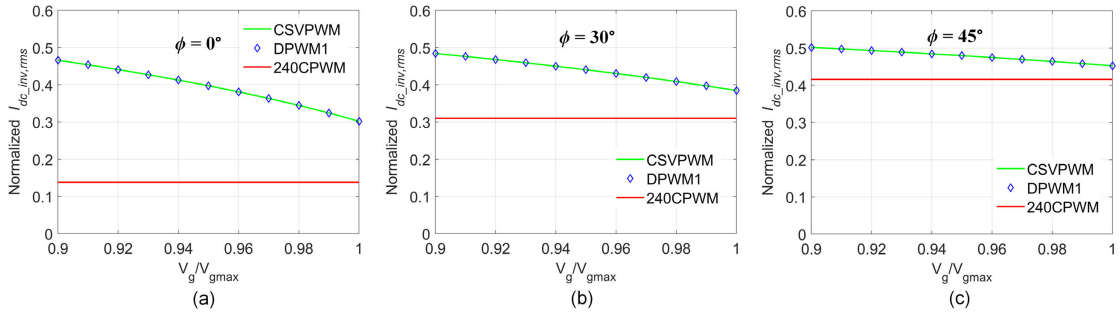

Figure 7.14: Normalized $I_{dc\_inv,rms}$ for All PWM Methods under Consideration (Normalized with Respect to RMS Line Current) (a) $\phi = 0°$, (b) $\phi = 30°$ and (c) $\phi = 45°$.

Variation in $I_{dc\_inv,rms}$ for all PWM methods under consideration at different power factor angles is shown in Fig. 7.14. $I_{dc\_inv,rms}$ is lowest for 240CPWM at unity power factor. $I_{dc\_inv,rms}$ for 240CPWM is lower than $I_{dc\_inv,rms}$ for CSVPWM and DPWM1 for a wide range of power factor angle i.e. from -65° to 65°. Percentage saving in $I_{dc\_inv,rms}$ for 240CPWM is around 54% as compared to CSVPWM at unity power factor at M_{max}. Variation in $I_{dc\_inv,rms}$ is symmetrical for a given leading and lagging power factor angle. Reduction in $I_{dc\_inv,rms}$ reduces the DC link capacitor current for 240CPWM i.e., $I_{cap,RMS}$ which is shown in the experimental section.

Table 7.5: Performance Comparison of Various PWM Methods Used in Three-phase Grid-connected PV Inverter Application.

Ref	P (kW)	RMS v_g (V)	V_{dc} (V)	PWM Method	f_{sw} (kHz)	C_{PV} (nF)	R_G (Ω)	L_f (mH)	$I_{CM,RMS}$ (A)	η (%)	THD (%)	$V_{CM,RMS}$ (V)
[94]	1	220	370	CSVPWM	10	200	NA	5	2.95	NA	4.2	NA[1]
[94]	1	220	370	DPWM1	15	200	NA	5	0.99	NA	4.6	NA
[94]	1	220	370	NSPWM	15	200	NA	5	0.37	NA	4.2	NA
[94]	1	220	370	AZSPWM1	10	200	NA	5	0.77	NA	4.6	NA
[141]	NA	10	60	RSPWM	10	220	10.75	1.8	NA	94.5	4.36	NA
[42]	2	220	400	Novel scalar PWM	30	220	NA	4.3	0.59	96.1[2]	4.66	91
Proposed	3	208	300	240CPWM	10	400	10	3	0.978	96.4[3]	3.8	48.5

[1] Not Available

[2] Efficiency of DC-AC stage only

[3] Combined efficiency of DC-DC and DC-AC stages

Table 7.5 shows the performance comparison of various PWM methods from literature as compared to 240CPWM at different test conditions. NSPWM and AZSPWM1 reduce the RMS leakage current but at the expense of THD and inverter efficiency. 240CPWM has promising performance as compared to the other PWM methods discussed in literature in terms of over-all efficiency, THD, RMS CMV and RMS leakage current. The RMS leakage current for 240CPWM seems higher in Table 7.5, but the apparent difference is due to higher power level (3 kW) and thus, higher C_{PV} is used for 240CPWM as compared to other PWM methods. Moreover, the resonant frequency of the common-mode circuit of our experimental setup is 7.6 kHz which is close to the switching frequency (10 kHz). The impedance of common mode circuit is very low near the resonant frequency that forces high leakage current. Leakage current can be considerably reduced by choosing the switching frequency of inverter away from resonant frequency.

7.3.4 Combined Weighted Performance Index

In order to compare 240CPWM with other PWM methods at same operating conditions, PLECS simulation results at 3 kW are presented in Table 7.6. 240CPWM is compared with RCMV-PWM methods along with CSVPWM and DPWM1 in terms of THD in line current (with leakage impedance), total loss in DC-DC and DC-AC stage, DC-link capacitor current stress, RMS CMV and leakage current as shown in Table 7.6. The parameters in the PLECS simulation are kept same as the specifications of our experimental set-up as shown in Table 7.1. To provide a comprehensive comparison of different PWM methods under consideration, a weighted performance indicator (wPI) is introduced as shown in (7.11). Each parameter is normalized with respect to the corresponding parameter for CSVPWM, for example RMS leakage current for each PWM method is normalized with respect to the RMS leakage current

Table 7.6: Comparison of 240CPWM with RCMV-PWM and Conventional Methods in terms of RMS CMV, Leakage Current, THD, Efficiency and DC Link Current Stress at 3 kW Based on Detailed Simulations under Identical Conditions.

PWM method	$I_{CM,RMS}$ (A)	THD (%)	$V_{CM,RMS}$ (V)	P_{loss} (W)	$I_{cap,RMS}$ (A)	wPI
CSVPWM	3.1	12.5	94.4	165	5.45	1
DPWM1	3.2	13.2	94.5	135	5.47	0.98
AZSPWM1[1]	0.76	6.2	58	165	5.69	0.68
AZSPWM3[1]	1.7	8.4	58.5	165	7.25	0.83
NSPWM[2]	0.91	7.3	58.2	150	4.46	0.64
240CPWM	1.09	5.7	46.8	111	3.7	0.45

[1] Not competitive due to high THD in grid-connected PV application and high switching loss resulting in lower efficiency of inverter.

[2] Not competitive due to high THD in grid-connected PV application

of CSVPWM (3.1 A). w_i are the weight coefficients that can be tuned according to the desired performance characterization in a particular application. We have set w_i = 0.2 for each parameter to get $wPI = 1$ for CSVPWM. For wPI calculation, THD (with leakage path considered), total loss in DC-DC and DC-AC stage, RMS CMV, RMS leakage current and RMS DC link capacitor current stress are considered. Based on the definition of wPI, lowest value indicates the best performing PWM method including the combined performance of all the parameters considered. 240CPWM has the lowest value of wPI showing that it has the combined best performance among

all the PWM methods under consideration.

$$wPI = w_1\frac{P_{loss}}{P_{loss_{CSVPWM}}} + w_2\frac{I_{CM,RMS}}{I_{CM,RMS_{CSVPWM}}} + w_3\frac{V_{CM,RMS}}{V_{CM,RMS_{CSVPWM}}} + w_4\frac{THD}{THD_{CSVPWM}} + w_5\frac{I_{cap,RMS}}{I_{cap,RMS_{CSVPWM}}} \tag{7.11}$$

7.4 Experimental Validation

The experimental set-up is rated at 3 kW and is shown in Fig. 7.15. The specifications of the grid-connected PV converter are given in Table 7.1. 240CPWM is compared with CSVPWM and DPWM1 in terms of THD in line current, switching loss at unity and non-unity power factor, DC link current stress, CMV and leakage current. The required waveforms are captured by a LeCroy HDO8038 oscilloscope with 10 MHz sampling frequency using LeCroy CP030 30 A 50 MHz current probes and LeCroy ADP305 100 MHz 1400 V differential voltage probes. The efficiency of PV converter is obtained using Yokogawa WT3000 precision power analyzer. The current waveforms are post-processed in MATLAB to obtain THD up to 1 MHz. The harmonic spectrums of CMV and leakage current are obtained by taking their FFT

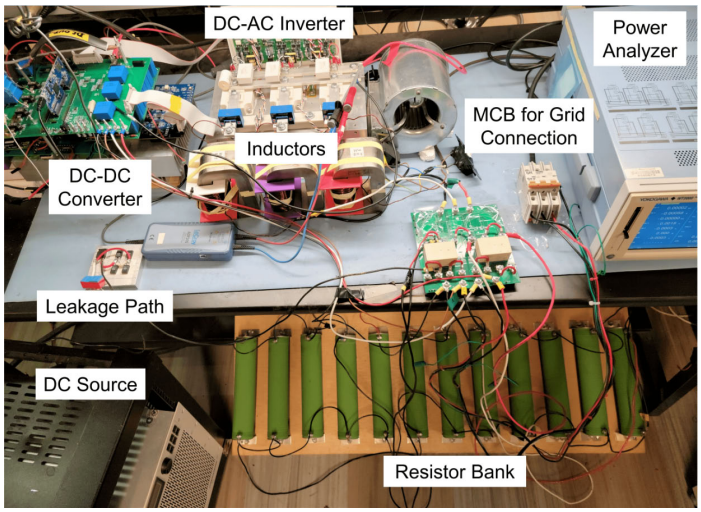

Figure 7.15: Picture of Experimental Set-up.

Table 7.7: Peak and CEC Efficiencies of Grid-connected PV Converter (DC-DC and DC-AC Combined) for all PWM Methods under Consideration.

PWM Method	Peak η (%)	CEC η (%)
CSVPWM	94.43	93.6
DPWM1	95.73	94.99
240CPWM	96.36	96

in MATLAB.

The experimental results in grid connected mode with CSVPWM, DPWM1 and 240CPWM at 3 kW and 208 V line to line RMS voltage without leakage path are shown in Fig. 7.16. 240CPWM operates at maximum modulation index M_{max} whereas CSVPWM and DPWM1 are limited to $0.91M_{max}$ due to large dead time of silicon IGBTs in the inverter. To compare all the PWM methods at same power level (3 kW), the DC link voltage for CSVPWM and DPWM1 is maintained at 350 V as compared to 300 V for 240CPWM. The mean THD in inverter currents is measured as 4.8% for CSVPWM, 5% for DPWM1 and 3.8% for 240CPWM.

The combined efficiency of DC-DC stage and DC-AC stage is measured. At 3 kW, the total efficiency is 94.24% for CSVPWM, 95.73% for DPWM1 while it is 96% for 240CPWM. The peak and California Energy Commission (CEC) [142] efficiencies of the PV system are shown in Table 7.7. The peak and CEC efficiency for 240CPWM is 96.4% (at 2 kW) and 96% respectively.

The overall efficiency of PV system including DC-DC stage and DC-AC stage at different percentages of the rated power (3 kW) for CSVPWM, DPWM1 and 240CPWM are shown in Fig. 7.17 which are then used to calculate the CEC efficiency as shown in Table 7.7. 240CPWM outperforms CSVPWM and DPWM1 in terms of overall efficiency under all the operating conditions. 240CPWM improves the light load efficiency (at 10% of the rated power) by 5.5% and CEC efficiency by 2.4% as

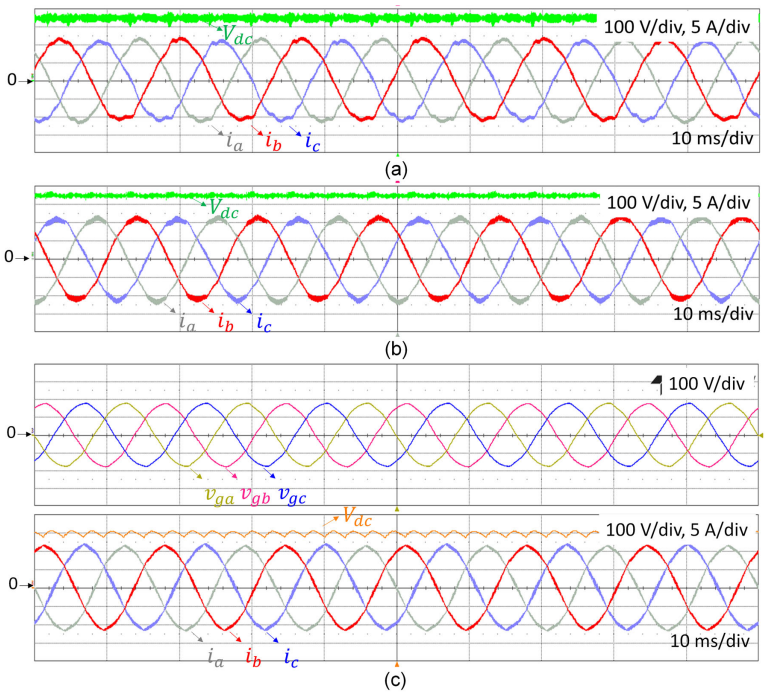

Figure 7.16: Experimental Waveforms of Three-phase Phase Voltages $v_{ga,gb,gc}$, DC Link Voltage V_{dc}, Line Currents $i_{a,b,c}$ (a) CSVPWM (b) DPWM1 (c) 240CPWM, All in Grid-connected Mode.

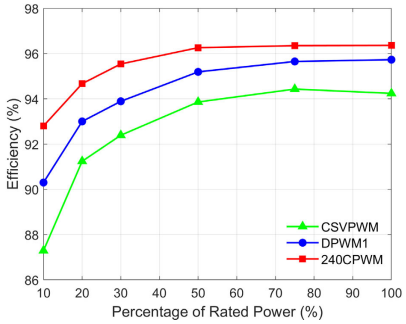

Figure 7.17: Overall Efficiency of Grid Connected PV Converter at Different Power Levels.

compared to CSVPWM.

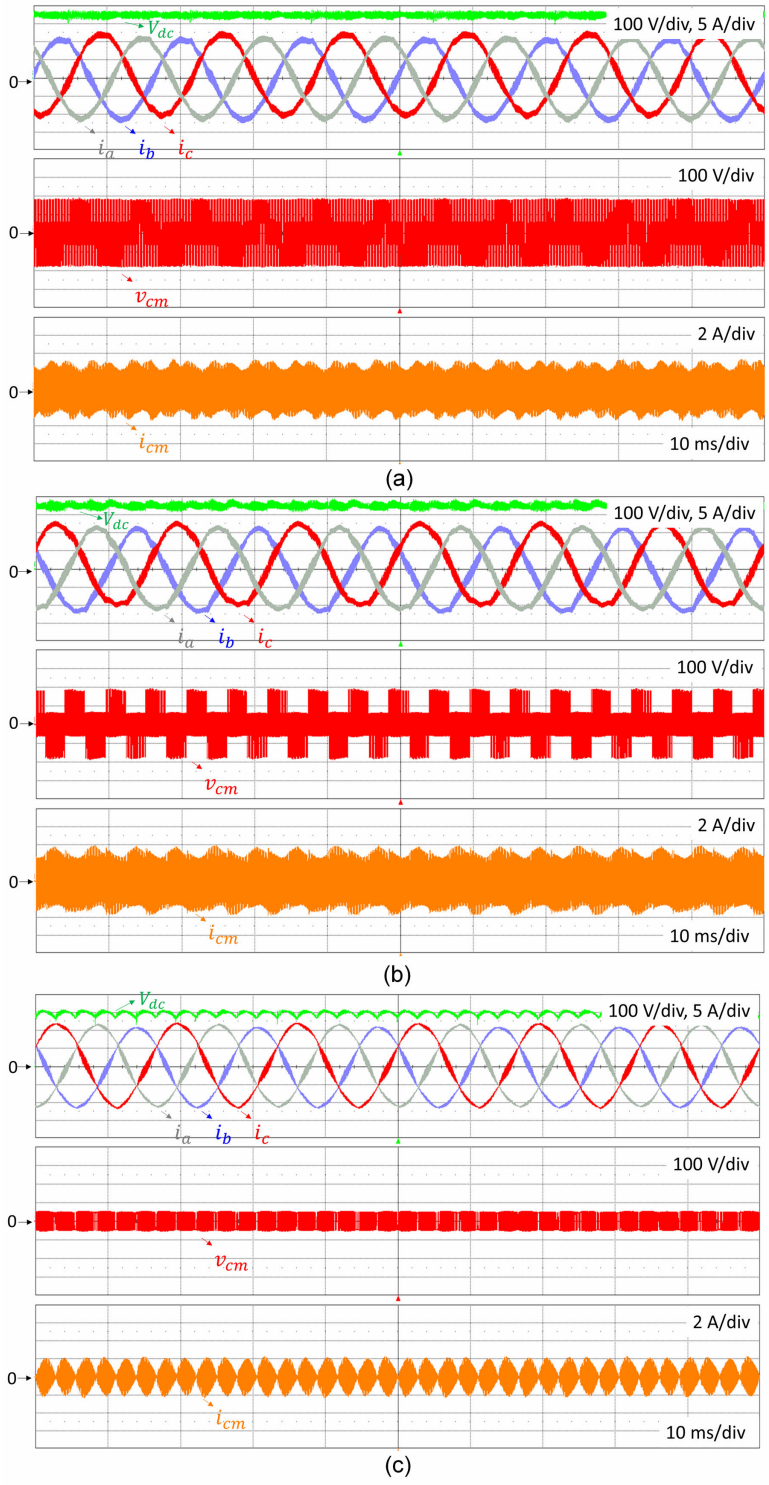

Figure 7.18: Experimental Waveforms of Line Currents $i_{a,b,c}$, DC Link Voltage V_{dc}, CMV v_{cm} and Leakage Current i_{cm} at 3 kW (a) CSVPWM (b) DPWM1 (c) 240CPWM.

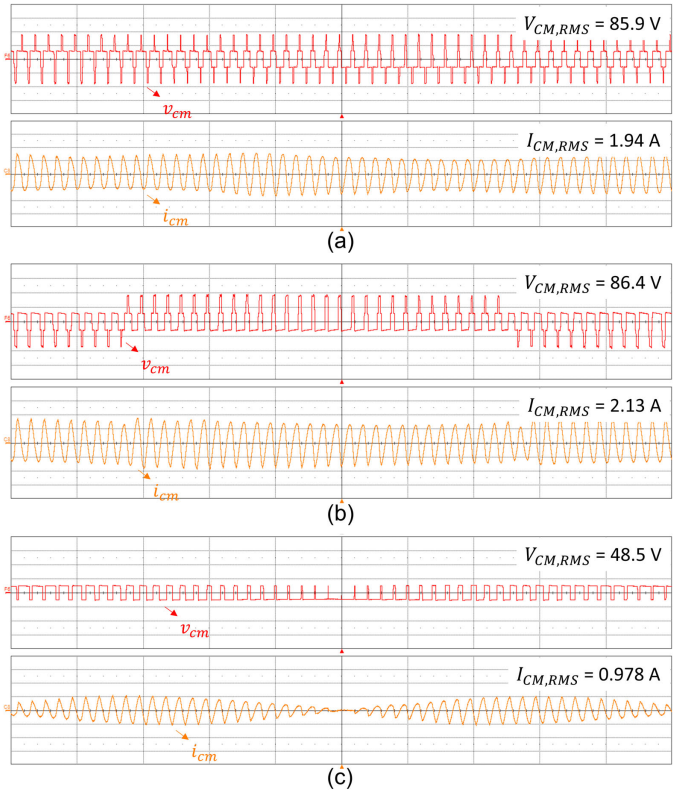

Figure 7.19: CMV (100 V/div) and Leakage Current (2 A/div) at 3 kW (a) CSVPWM (b) DPWM1 (c) 240CPWM (Time Scale = 500 us/div).

Experimental waveforms of CMV and leakage current for all PWM methods under consideration at 3 kW in grid-connected mode are shown in Fig. 7.18. Peak value of CMV for CSVPWM and DPWM1 is $\pm V_{dc}/2$ ($\pm$ 175 V) whereas it is $\pm V_{dc}/6$ ($\pm$ 50 V) for 240CPWM. Higher distortion in line current is visible for CSVPWM and DPWM1 due to increased leakage current as compared to 240CPWM. The measured THD in line currents i_a, i_b and i_c with leakage path are: 9.39%, 9.7% and 10% for CSVPWM, 10.94%, 11.3% and 11.6% for DPWM1 and 5.8%, 5.6% and 5.9% for 240CPWM. Contrary to the analysis shown in Fig. 7.11, CSVPWM has much higher THD as compared to 240CPWM. This is because the analysis is valid when the leakage path is not considered. Leakage current severely impacts the THD in line currents. With the leakage path, the leakage current for CSVPWM is much higher that increases

the THD for CSVPWM as compared to 240CPWM. Hence, 240CPWM reduces the CMV and leakage current while ensuring lower THD in line currents as compared to CSVPWM and DPWM1.

At same test conditions, zoomed in CMV and leakage current are shown in Fig. 7.19. $V_{CM,RMS}$ for CSVPWM and DPWM1 at 3 kW for V_{dc} = 350 V are approximately equal i.e., 85.9 V and 86.4 V respectively. This is because the duration of two zero states applied in CSVPWM is equal to the duration of one zero state in DPWM1. However, $V_{CM,RMS}$ decreases to just 48.5 V for 240CPWM since none of the zero states are used. Despite similar CMV for CSVPWM and DPWM1, DPWM1 has higher leakage current (2.13 A) as compared to CSVPWM (1.94 A). This is because leakage current in transformerless grid connected PV inverter is mainly dependent on the harmonic component of CMV at switching frequency and DPWM1 has higher harmonic component of CMV at switching frequency (10 kHz). Leakage current with 240CPWM is only 0.978 A. 240CPWM results in 46.7% saving in $V_{CM,RMS}$ as compared to CSVPWM/DPWM1 and 49.7% and 54% saving in $I_{CM,RMS}$ as compared to

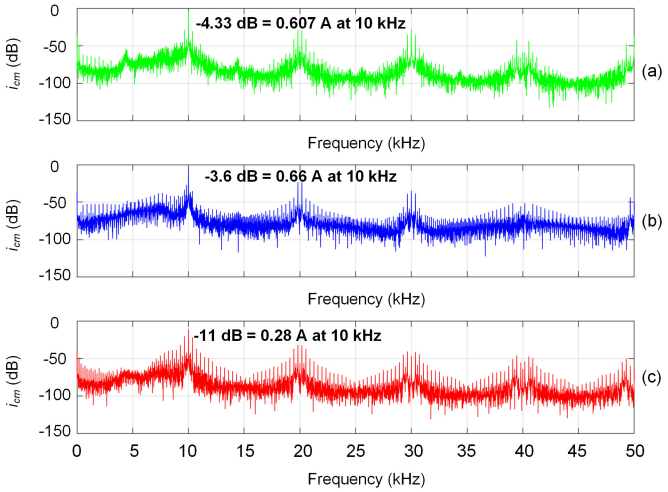

Figure 7.20: Spectra of Leakage Current from Experiments (Leakage Current Post Processed in MATLAB) (a) CSVPWM, (b) DPWM1 and (c) 240CPWM.

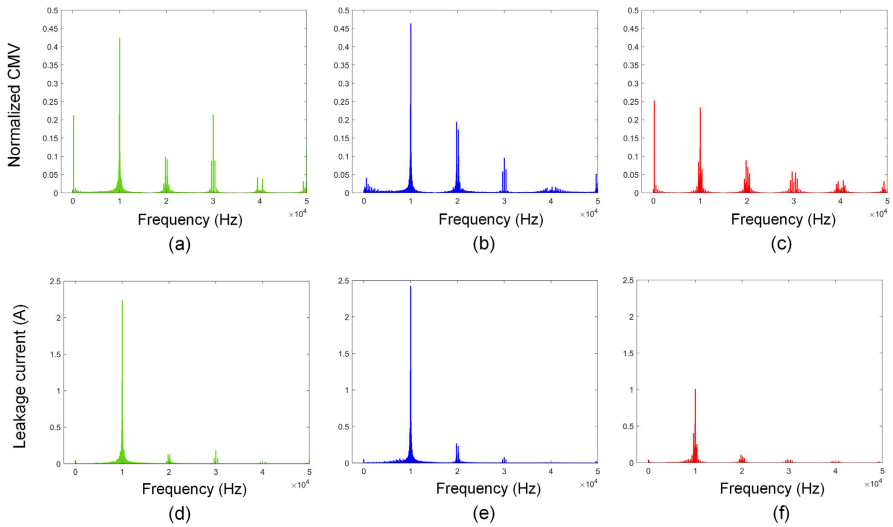

Figure 7.21: Frequency Spectrum of CMV (top) from Experiments for (a) CSVPWM (b) DPWM1 (c) 240CPWM, All Normalized with Respect to $V_{dc}/2$ and FFT of Leakage Current (Bottom) for (d) CSVPWM (e) DPWM1 (f) 240CPWM.

CSVPWM and DPWM1 respectively. The experimental results shown in Fig. 7.19 match very well with the analytical and simulation values of CMV and leakage current as shown in Table 7.4. Comparing the spectra of leakage current with CSVPWM, DPWM1 and 240CPWM shown in Fig 7.20, it is evident that this reduction predominantly comes at 10 kHz switching frequency component. The spectral peak at 10 kHz in leakage current is supressed with 240CPWM.

The FFT of CMV (normalized with respect to $V_{dc}/2$) and leakage current up to 150 kHz obtained by post processing the experimental waveforms in MATLAB for all PWM methods are shown in Fig. 7.21. The harmonic component of CMV at switching frequency mainly determines the magnitude of leakage current. The harmonic component of CMV at 10 kHz is the highest for DPWM1 as shown in Fig. 7.21 (a-c) which leads to the highest leakage current for DPWM1. 240CPWM has the lowest harmonic component at 10 kHz resulting in least leakage current as compared to CSVPWM and DPWM1.

Fig. 7.22 shows the current drawn by the inverter (i_{dc_inv}) and DC link voltage

Table 7.8: Comparison of 240CPWM with CSVPWM and DPWM1 in Terms of Measured RMS CMV, Leakage Current, DC Link Current Stress, THD and Efficiency.

PWM	$I_{CM,RMS}$ (A)	THD (%)	$V_{CM,RMS}$ (V)	η [1] (%)	η [2] (%)	$I_{cap,RMS}$ (A)
CSVPWM	1.94	9.7	85.9	96.2	94.2	5.5
DPWM1	2.13	11	86.4	97.5	95.7	5.45
240CPWM	0.98	5.8	48.5	98.1	96	3.9

[1] Efficiency corresponds to the efficiency of DC-AC stage only.

[2] Efficiency corresponds to the total converter including DC-DC and DC-AC stage.

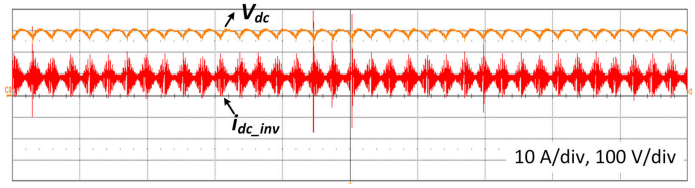

Figure 7.22: Current Drawn by the Inverter (i_{dc_inv}) and DC Link Voltage $V_{dc}(t)$ for 240CPWM.

with 240CPWM from experiments where it can be clearly observed that variation in i_{dc_inv} for 240CPWM is very small. This results in low DC link capacitor stress for 240CPWM as verified in Fig. 7.23.

The experimental results of DC link capacitor current stress for CSVPWM, DPWM1 and 240CPWM are presented in Fig. 7.23 (a), (b) and (c) respectively with RMS values ($I_{cap,RMS}$) of 5.5 A, 5.45A and 3.9 A respectively. The saving in $I_{cap,RMS}$ with 240CPWM is because of absence of zero states which reduces the variation in current drawn by inverter (i_{dc_inv}) that in turn reduces the variation in DC link capacitor current.

Table 7.8 shows the comparison of 240CPWM with CSVPWM and DPWM1 in

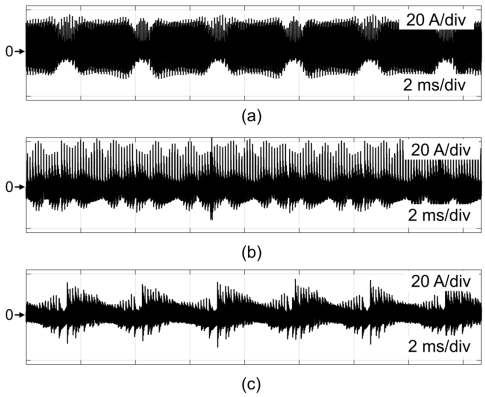

Figure 7.23: DC Link Capacitor Current from Experiments (a) CSVPWM, (b) DPWM1 and (c) 240CPWM.

terms of measured RMS CMV, leakage current, DC link current stress, THD and efficiency of both the DC-DC and DC-AC stage obtained from experiments where 240CPWM clearly outperforms CSVPWM and DPWM1.

7.5 Conclusion

Due to substantial parasitic capacitance of the PV panels, high leakage current is produced by transformerless grid connected PV converters that causes severe electromagnetic interference, distortion in line currents, safety hazards and additional losses in the system. A PWM method called 240CPWM with complete elimination of zero states is explored in transformerless grid connected PV converters that reduces the CMV and leakage current without compromising on the efficiency, THD or DC link capacitor current stress. Reducing the leakage current with 240CPWM means smaller common mode filters requirement that improves the power density and reduces the cost. It is shown experimentally that 240CPWM reduces peak CMV by 66.7%, RMS CMV by 44%, leakage current by 50%, THD by 54%, DC link capacitor current stress by 29% and switching loss by 85% at unity power factor as compared to CSVPWM in grid-connected PV converter at 3 kW. Measured peak efficiency of the PV con-

verter system including the DC-DC stage and DC-AC stage in grid-connected mode is 96.4% with 240CPWM.

Chapter 8

CONCLUSION AND FUTURE WORK

8.1 Conclusion

In this work, a new PWM method called 240° Clamped PWM (240CPWM) is studied in which each phase pole is clamped for 240° in a fundamental cycle near current peaks. Each phase pole switches only for 120° in a fundamental cycle and that too near the zero crossing of current, thus reducing the switching loss by 85% as compared to Conventional Space Vector PWM (CSVPWM). In 240CPWM, zero states are completely eliminated, and only the two nearest active states are always used ensuring that there is no penalty in terms of THD in line current. Application of 240CPWM in Hybrid Electric Vehicles (HEVs) is proposed and experimentally verified with a 10 kW hardware prototype. Moreover, performance of 240CPWM is studied in detail in three phase grid connected Photovoltaic (PV) converter under adverse grid conditions. The following list presents a summary of this work:

- **Chapter 2** talks about the space vector-based approach for different PWM methods. Conventional and clamping sequences are analyzed both with triangular comparison approach and space vector approach. Then double switching clamping sequences are shown that can be implemented using space vector approach.

- **Chapter 3** discusses 240CPWM concept in cascaded architecture of DC-DC stage followed by three phase inverter in detail. Switching loss characteristics of 240CPWM are thoroughly studied and compared with CSVPWM, DPWM1

and ACCPWM both with constant and varying DC link voltage cases. Typical constant V/f mode of Variable Speed Drives with constant load current is used to compare the characteristics of different PWM methods, where the fundamental voltage is proportional to the fundamental frequency. Switching loss for 240CPWM is only 31 W which is 6.8 times lower than CSVPWM with constant V_{dc} at 10 kW, 50 Hz operation. Likewise, switching loss for 240CPWM is 12W which is 15.5 times lower than CSVPWM with constant V_{dc} at 5 kW, 25 Hz operation. Finally, to analyze the efficacy of 240CPWM in EV/HEV powertrains, switching loss analysis is extended for two standard driving cycles i.e., City and Highway driving cycles.

- In **Chapter 4**, current stress on the DC link capacitor is analyzed and experimentally verified for 240CPWM with CSVPWM as a benchmark. Due to the elimination of zero states in 240CPWM, variation in current drawn by the inverter (i_{inv}) is reduced. 240CPWM used in DC-AC stage helps to reduce RMS DC link capacitor current to 3.25 A at 5 kW as compared to 5.193 A for CSVPWM, thus smaller DC link capacitor can be used for 240CPWM. Experimental results match with the analysis and simulations.

- In **Chapter 5**, dual loop control is designed for tracking the dynamically varying DC link voltage for 240CPWM. Outer voltage loop with low bandwidth and inner current loop with high bandwidth are designed to achieve control objectives. Efficacy of the designed close loop control is shown in terms of much better DC link voltage tracking and reduction in input current ripple as compared to open loop control. Then voltage mode control of three phase interleaved boost converter with Smith predictor is proposed for shaping the dynamic DC link voltage for 240CPWM that minimizes the impact of RHP zero. Performance

of voltage mode control with Smith predictor is verified using a two-stage drive system and compared with other well-known control methods at 3 kW with maximum fundamental frequency of 300 Hz.

- **Chapter 6** shows the performance of 240CPWM in grid connected PV converter. In this chapter, operation of 240CPWM in three phase grid connected PV converters is studied using PI controller along with Harmonic Compensator (HC) under various grid disturbances like sag/swell and unbalance in grid voltages. 10% unbalance, 10% sag and 10% swell in grid voltages is applied to emulate these voltage disturbance conditions in the grid. The DC link voltage quickly adapts to these disturbances maintaining sinusoidal and balanced grid currents. Also, the experimental results at non-unity power factors are presented with 240CPWM for the first time. Undesired low frequency dominant harmonics in inverter currents are minimized using the HC controller that results in THD of 3.5% with 240CPWM in compliance with the IEEE-1547 grid interconnection standard. The coordinated control of both the DC-DC converter and DC-AC inverter is shown that allows synchronism between the grid voltages and dynamic DC link voltage. Hence, the implemented control scheme of low-loss 240CPWM in grid connected PV converter achieves smooth operation under non-unity powerfactor and grid disturbance conditions while maintaining THD of 3.5% in grid currents and peak combined efficiency of DC-DC and DC-AC stage as 96.4% as compared to 94.43% for CSVPWM.

- In **Chapter 7**, 240CPWM is applied to Transformerless Grid Connected PV Converters and its performance is compared with other PWM methods in terms of switching loss, THD, DC link current stress, CMV and leakage current. 240CPWM is selected as an ideal candidate for grid connected PV converters

in terms of all round performance for each of the above metrics. A new, combined performance index is proposed to compare the performance of different PWM schemes, and it is shown that the 240CPWM achieves the best value for this index among the PWM methods studied. It is shown experimentally that 240CPWM reduces peak CMV by 66.7%, RMS CMV by 44%, leakage current by 50%, THD by 54%, DC link capacitor current stress by 29% and switching loss by 85% at unity power factor as compared to CSVPWM in grid-connected PV converter at 3 kW. Measured peak efficiency of the PV converter system including the DC-DC stage and DC-AC stage in grid-connected mode is 96.4% with 240CPWM.

8.2 Future Work

The potential future work for this research endeavor are listed as follows:

- Detailed analysis of 240CPWM in Electric Vehicle application with various driving cycles like Urban, Rural, American and European driving cycles.
- Dynamic modeling of motor that better demonstrates the actual EV powertrain performance as compared to RL load.
- Experimental validation of 240CPWM in multilevel inverter.
- Better and fast control algorithms to track dynamic DC Link voltage for fundamental frequency as high as 1000 Hz as required in EV/HEV powertrain.
- Application of 240CPWM in emerging grid-forming inverters.

REFERENCES

[1] O. Babatunde, J. L. Munda, and Y. Hamam, "Operations and planning of integrated renewable energy system: a survey," in *2020 5th International Conference on Renewable Energies for Developing Countries (REDEC)*. IEEE, 2020, pp. 1–6.

[2] A. Qazi, F. Hussain, N. A. Rahim, G. Hardaker, D. Alghazzawi, K. Shaban, and K. Haruna, "Towards sustainable energy: a systematic review of renewable energy sources, technologies, and public opinions," *IEEE Access*, vol. 7, pp. 63 837–63 851, 2019.

[3] C. Bhowmik, S. Bhowmik, A. Ray, and K. M. Pandey, "Optimal green energy planning for sustainable development: A review," *Renewable and Sustainable Energy Reviews*, vol. 71, pp. 796–813, 2017.

[4] "Global Energy Review 2020," https://www.iea.org/reports/global-energy-review-2020, 2020.

[5] R. M. Elavarasan, G. Shafiullah, S. Padmanaban, N. M. Kumar, A. Annam, A. M. Vetrichelvan, L. Mihet-Popa, and J. B. Holm-Nielsen, "A comprehensive review on renewable energy development, challenges, and policies of leading Indian states with an international perspective," *IEEE Access*, vol. 8, pp. 74 432–74 457, 2020.

[6] S. Manish, I. R. Pillai, and R. Banerjee, "Sustainability analysis of renewables for climate change mitigation," *Energy for Sustainable Development*, vol. 10, no. 4, pp. 25–36, 2006.

[7] S. Fritz, L. See, T. Carlson, M. M. Haklay, J. L. Oliver, D. Fraisl, R. Mondardini, M. Brocklehurst, L. A. Shanley, S. Schade *et al.*, "Citizen science and the United Nations sustainable development goals," *Nature Sustainability*, vol. 2, no. 10, pp. 922–930, 2019.

[8] W. G. Santika, M. Anisuzzaman, P. A. Bahri, G. Shafiullah, G. V. Rupf, and T. Urmee, "From goals to joules: A quantitative approach of interlinkages between energy and the Sustainable Development Goals," *Energy Research & Social Science*, vol. 50, pp. 201–214, 2019.

[9] N. C. Onat, M. Kucukvar, and S. Afshar, "Eco-efficiency of electric vehicles in the United States: A life cycle assessment based principal component analysis," *Journal of Cleaner Production*, vol. 212, pp. 515–526, 2019.

[10] "Inventory of U.S. Greenhouse Gas Emissions and Sinks: 1990–2019," 2019.

[11] UNECE, "Climate change and sustainable transport. United Nations Economic Commission for Europe," 2016.

[12] H. Ritchie and M. Roser, "CO_2 and greenhouse gas emissions," *Our World in Data*, 2020.

[13] P. Slowik, N. Lutsey, and C. Hsu, "How technology, recycling, and policy can mitigate supply risks to the long-term transition to zero-emission vehicles," 2020.

[14] C. McKerracher, A. Izadi-Najafabadi, A. O'Donovan, N. Albanese, N. Soulopolous, D. Doherty, M. Boers, R. Fisher, C. Cantor, J. Frith *et al.*, "Electric vehicle outlook 2020," *Bloomberg New Energy Finance*, 2020.

[15] T. Randall, "Here's how electric cars will cause the next oil crisis," *Bloomberg, New York, accessed Mar*, vol. 25, p. 2016, 2016.

[16] J. A. Sanguesa, V. Torres-Sanz, P. Garrido, F. J. Martinez, and J. M. Marquez-Barja, "A Review on Electric Vehicles: Technologies and Challenges," *Smart Cities*, vol. 4, no. 1, pp. 372–404, 2021.

[17] S. Habib, M. M. Khan, F. Abbas, L. Sang, M. U. Shahid, and H. Tang, "A comprehensive study of implemented international standards, technical challenges, impacts and prospects for electric vehicles," *IEEE Access*, vol. 6, pp. 13 866–13 890, 2018.

[18] M. Lapedus, "Electric cars gain traction, but challenges remain," *Semiconductor Engineering*, 2019.

[19] I. R. E. Agency, "Future of solar photovoltaic: deployment, investment, technology, grid integration and socio-economic aspects," *A Global Energy Transformation*, 2019.

[20] R. Schmalensee, *The future of solar energy: an interdisciplinary MIT study*. Energy Initiative, Massachusetts Institute of Technology, 2015.

[21] "Renewable Energy Capacity Statistics 2019, International Renewable Energy Agency, Abu Dhabi," 2019.

[22] J. Reimers, L. Dorn-Gomba, C. Mak, and A. Emadi, "Automotive traction inverters: Current status and future trends," *IEEE Transactions on Vehicular Technology*, vol. 68, no. 4, pp. 3337–3350, 2019.

[23] G. Tsengenes and G. Adamidis, "Investigation of the behavior of a three phase grid-connected photovoltaic system to control active and reactive power," *Electric Power Systems Research*, vol. 81, no. 1, pp. 177–184, 2011.

[24] B. Raza, "Interleaved DC-DC Converter with Wide Band Gap Devices and ZVT Switching for Flexible DC-Link in Electric Vehicle Powertrains," Ph.D. dissertation, Arizona State University, 2019.

[25] J. O. Estima and A. J. M. Cardoso, "Efficiency analysis of drive train topologies applied to electric/hybrid vehicles," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 3, pp. 1021–1031, 2012.

[26] A. Morozov, K. Humphries, T. Rahman, T. Zou, and J. Angeles, "Drivetrain analysis and optimization of a two-speed class-4 electric delivery truck," SAE Technical Paper, Tech. Rep., 2019.

[27] S. Tenner, S. Gimther, and W. Hofmann, "Loss minimization of electric drive systems using a DC/DC converter and an optimized battery voltage in automotive applications," in *2011 IEEE Vehicle Power and Propulsion Conference*. IEEE, 2011, pp. 1–7.

[28] "Where the Energy Goes: Electric Cars," https://www.fueleconomy.gov/feg/atv-ev.shtml.

[29] A. Ghazanfari, C. Perreault, and K. Zaghib, "EV/HEV industry trends of wide-bandgap power semiconductor devices for power electronics converters," in *2019 IEEE 28th International Symposium on Industrial Electronics (ISIE)*. IEEE, 2019, pp. 1917–1923.

[30] "Understanding PV System Losses, Part 2: Wiring, Connections, and System Availability," https://www.aurorasolar.com/blog/understanding-pv-system-losses-part-2-wiring-connections-and-system-availability/.

[31] L. Pan and C. Zhang, "A high power density integrated charger for electric vehicles with active ripple compensation," *Mathematical Problems in Engineering*, vol. 2015, 2015.

[32] M. Kamiya, "Development of traction drive motors for the Toyota hybrid system," *IEEJ Transactions on Industry Applications*, vol. 126, no. 4, pp. 473–479, 2006.

[33] "Electrical and Electronics Technical Team Roadmap," 2013. [Online]. Available: https://www.osti.gov/biblio/1220125

[34] Y. Shi, L. Wang, R. Xie, and H. Li, "Design and implementation of a 100 kW SiC filter-less PV inverter with 5 kW/kg power density and 99.2% CEC efficiency," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2018, pp. 393–398.

[35] Q. Huang, J. Li, and Y. Chen, "Control of electric vehicle," *Urban Transport and Hybrid Vehicles*, pp. 163–192, 2010.

[36] L. Quan, Z. Yi, and Z. Zude, "Research of drive control system in electric vehicle based on DSP," in *Proceedings 7th International Conference on Signal Processing, 2004. Proceedings. ICSP'04. 2004.*, vol. 1. IEEE, 2004, pp. 539–542.

[37] S. Weckx, C. Gonzalez, and J. Driesen, "Combined central and local active and reactive power control of PV inverters," *IEEE Transactions on Sustainable Energy*, vol. 5, no. 3, pp. 776–784, 2014.

[38] D. G. Photovoltaics and E. Storage, "IEEE standard for interconnection and interoperability of distributed energy resources with associated electric power systems interfaces," *IEEE Std*, pp. 1547–2018, 2018.

[39] Y. Murai, T. Kubota, and Y. Kawase, "Leakage current reduction for a high-frequency carrier inverter feeding an induction motor," *IEEE Transactions on Industry Applications*, vol. 28, no. 4, pp. 858–863, 1992.

[40] A. Muetze and A. Binder, "Calculation of circulating bearing currents in machines of inverter-based drive systems," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, pp. 932–938, 2007.

[41] X. Guo, J. Zhou, R. He, X. Jia, and C. A. Rojas, "Leakage current attenuation of a three-phase cascaded inverter for transformerless grid-connected PV systems," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 676–686, 2017.

[42] J. Xu, J. Han, Y. Wang, S. Habib, and H. Tang, "A novel scalar PWM method to reduce leakage current in three-phase two-level transformerless grid-connected VSIs," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 5, pp. 3788–3797, 2019.

[43] B. K. Bose *et al.*, *Modern power electronics and AC drives*. Prentice hall Upper Saddle River, NJ, 2002, vol. 123.

[44] F. Casanellas, "Losses in PWM inverters using IGBTs," *IEE Proceedings-Electric Power Applications*, vol. 141, no. 5, pp. 235–239, 1994.

[45] H. S. Patel and R. G. Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I–Harmonic Elimination," *IEEE Transactions on Industry Applications*, no. 3, pp. 310–317, 1973.

[46] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters: principles and practice*. John Wiley & Sons, 2003, vol. 18.

[47] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 49–61, 1999.

[48] D. Zhao, V. P. K. Hari, G. Narayanan, and R. Ayyanar, "Space-vector-based hybrid pulsewidth modulation techniques for reduced harmonic distortion and switching loss," *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 760–774, 2009.

[49] A. M. Hava and E. Ün, "Performance analysis of reduced common-mode voltage PWM methods and comparison with standard PWM methods for three-phase voltage-source inverters," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 241–252, 2009.

[50] J. Holtz, "Pulsewidth Modulation - a survey," *IEEE Transactions on Industrial Electronics*, vol. 39, no. 5, pp. 410–420, 1992.

[51] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Transactions on Industry Applications*, vol. 33, no. 3, pp. 756–764, 1997.

[52] G. Narayanan and V. Ranganathan, "Synchronised PWM strategies based on space vector approach. Part 1: Principles of waveform generation," *IEE Proceedings-Electric Power Applications*, vol. 146, no. 3, pp. 267–275, 1999.

[53] "Advanced bus-clamping PWM techniques based on space vector approach, author=Narayanan, G and Krishnamurthy, Harish K and Zhao, Di and Ayyanar, Rajapandian," *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 974–984, 2006.

[54] I. Aharon and A. Kuperman, "Topological overview of powertrains for battery-powered vehicles with range extenders," *IEEE Transactions on Power Electronics*, vol. 26, no. 3, pp. 868–876, 2011.

[55] K. K. Prabhakar, M. Ramesh, A. Dalal, C. U. Reddy, A. K. Singh, and P. Kumar, "Efficiency investigation for electric vehicle powertrain with variable DC-link bus voltage," in *IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2016, pp. 1796–1801.

[56] S. Chowdhury, E. Gurpinar, G.-J. Su, T. Raminosoa, T. A. Burress, and B. Ozpineci, "Enabling technologies for compact integrated electric drives for automotive traction applications," in *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*. IEEE, 2019, pp. 1–8.

[57] T. A. Burress, S. L. Campbell, C. Coomer, C. W. Ayers, A. A. Wereszczak, J. P. Cunningham, L. D. Marlino, L. E. Seiber, and H.-T. Lin, "Evaluation of the 2010 Toyota Prius hybrid synergy drive system," Oak Ridge National Lab.(ORNL), Oak Ridge, TN (United States). Power, Tech. Rep., 2011.

[58] T. A. Burress, C. Coomer, S. Campbell, A. Wereszczak, J. Cunningham, L. Marlino, L. Seiber, and H.-T. Lin, "Evaluation of the 2008 Lexus LS 600H hybrid synergy drive system," Oak Ridge National Laboratory (ORNL), Oak Ridge, TN, Tech. Rep., 2009.

[59] T. Burress, C. Coomer, S. Campbell, L. Seiber, L. D. Marlino, R. Staunton, and J. Cunningham, "Evaluation of the 2007 Toyota Camry hybrid synergy drive system," Oak Ridge National Laboratory (ORNL), Oak Ridge, TN, Tech. Rep., 2008.

[60] T. Burress, "Benchmarking EV and HEV Technologies Oak Ridge National Laboratory," in *2015 Annual Merit Review and Peer Evaluation Meeting*, 2016.

[61] Q. Lei and F. Z. Peng, "Space vector pulsewidth amplitude modulation for a buck–boost voltage/current source inverter," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 266–274, 2013.

[62] J. A. Anderson, M. Haider, D. Bortis, J. W. Kolar, M. Kasper, and G. Deboy, "New synergetic control of a 20kw isolated vienna rectifier front-end ev battery charger," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE, 2019, pp. 1–8.

[63] H. Qamar, H. Qamar, and R. Ayyanar, "Performance Analysis and Experimental Validation of 240-Clamped Space Vector PWM to Minimize Common Mode Voltage and Leakage Current in EV/HEV Traction Drives," *IEEE Transactions on Transportation Electrification*, 2021.

[64] M. Andre, "Driving cycles development: characterization of the methods," SAE Technical Paper, Tech. Rep., 1996.

[65] S. Davis and R. G. Boundy, "Transportation Energy Data Book: Edition 39," Oak Ridge National Lab.(ORNL), Oak Ridge, TN (United States), Tech. Rep., 2021.

[66] J.-S. Lai, H. Kouns, and J. Bond, "A low-inductance DC bus capacitor for high power traction motor drive inverters," in *Conference Record of the 2002 IEEE Industry Applications Conference. 37th IAS Annual Meeting (Cat. No. 02CH37344)*, vol. 2. IEEE, 2002, pp. 955–962.

[67] H. Wen, W. Xiao, X. Wen, and P. Armstrong, "Analysis and evaluation of DC-link capacitors for high-power-density electric vehicle drive systems," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 7, pp. 2950–2964, 2012.

[68] L. Jin and J. Zhang, "Modeling of DC link capacitor current ripple for electric vehicle traction converter," 2013.

[69] T. Burress and S. Campbell, "Benchmarking EV and HEV power electronics and electric machines," in *2013 IEEE Transportation Electrification Conference and Expo (ITEC)*. IEEE, 2013, pp. 1–6.

[70] T. Hosking, "Comparative evaluation and analysis of the 2008 toyota lexus, camry and 2004 prius dc link capacitor assembly vs. the sbe power ring dc link capacitor," in *2009 IEEE Vehicle Power and Propulsion Conference*. IEEE, 2009, pp. 717–723.

[71] G. Terzulli, "Evolution of power capacitors for Electric Vehicles," *report from a KYOCERA group company*, 2012.

[72] R. Earley, L. Kang, F. An, and L. Green-Weiskel, "Electric vehicles in the context of sustainable development in China," *The Innovation Center for Energy and Transportation (iCET), Background Paper*, vol. 9, 2011.

[73] X. Lu, W. Qian, D. Cao, F. Z. Peng, and J. Liu, "A carrier modulation method for minimizing the dc link capacitor current ripple of the HEV DC-DC converter and inverter systems," in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2011, pp. 800–807.

[74] Y. Nishida, N. Aikawa, S. Sumiyoshi, H. Yamashita, and H. Omori, "A novel type of utility-interactive inverter for photovoltaic system," in *The 4th International Power Electronics and Motion Control Conference, 2004. IPEMC 2004.*, vol. 3. IEEE, 2004, pp. 1785–1790.

[75] X. Lu and F. Z. Peng, "Theoretical analysis of DC link capacitor current ripple reduction in the HEV DC-DC converter and inverter system using a carrier modulation method," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2012, pp. 2833–2839.

[76] C. Sommer, A. Merkert, and A. Mertens, "A new control method for minimizing the DC-link capacitor current of HEV inverter systems," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2014, pp. 1188–1193.

[77] M. E. de Oliveira Filho, J. R. Gazoli, A. J. Sguarezi Filho, and E. Ruppert Filho, "A control method for voltage source inverter without dc link capacitor," in *2008 IEEE Power Electronics Specialists Conference*. IEEE, 2008, pp. 4432–4437.

[78] J. Hobraiche, J.-P. Vilain, P. Macret, and N. Patin, "A new PWM strategy to reduce the inverter input current ripples," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 172–180, 2009.

[79] J. W. Kolar and S. D. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," *IEE Proceedings-Electric Power Applications*, vol. 153, no. 4, pp. 535–543, 2006.

[80] Y. Liu and F. Z. Peng, "Fast control of PWAM boost-converter-inverter system for HEV/EV motor drives," in *2014 IEEE Applied Power Electronics Conference and Exposition-APEC 2014*. IEEE, 2014, pp. 2446–2452.

[81] M. Antivachis, J. A. Anderson, D. Bortis, and J. W. Kolar, "Analysis of a synergetically controlled two-stage three-phase DC/AC buck-boost converter," *CPSS Transactions on Power Electronics and Applications*, vol. 5, no. 1, pp. 34–53, 2020.

[82] D. Wu, H. Qamar, H. Qamar, and R. Ayyanar, "Comprehensive Analysis and Experimental Validation of 240°-Clamped Space Vector PWM Technique Eliminating Zero States for EV Traction Inverters With Dynamic DC Link," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 295–13 307, 2020.

[83] J. Alvarez-Ramirez, I. Cervantes, G. Espinosa-Perez, P. Maya, and A. Morales, "A stable design of PI control for DC-DC converters with an RHS zero," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 1, pp. 103–106, 2001.

[84] A. Ghosh, S. Banerjee, M. K. Sarkar, and P. Dutta, "Design and implementation of type-II and type-III controller for DC–DC switched-mode boost converter by using K-factor approach and optimisation techniques," *IET Power Electronics*, vol. 9, no. 5, pp. 938–950, 2016.

[85] W.-C. Wu, R. M. Bass, and J. R. Yeargan, "Eliminating the effects of the right-half plane zero in fixed frequency boost converters," in *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No. 98CH36196)*, vol. 1. IEEE, 1998, pp. 362–366.

[86] H.-H. Huang, D.-R. Wu, and K.-H. Chen, "A right-half-plane (RHP) zero alleviating skill in the solid-duty-control (SDC) boost converter," in *2010 IEEE Asian Solid-State Circuits Conference*. IEEE, 2010, pp. 1–4.

[87] "Analysis of a Smith-predictor-based-control concept eliminating the right-half plane zero of continuous mode boost and buck-boost DC/DC converters, author=Himmelstoss, FA and Kolar, Johann W and Zach, Franz C," in *Proceedings IECON'91: 1991 International Conference on Industrial Electronics, Control and Instrumentation*. IEEE, 1991, pp. 423–428.

[88] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398–1409, 2006.

[89] D. G. Photovoltaics and E. Storage, "IEEE Application Guide for IEEE Std 1547™, IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," 2009.

[90] Q.-N. Trinh, F. H. Choo, and P. Wang, "Control strategy to eliminate impact of voltage measurement errors on grid current performance of three-phase grid-connected inverters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7508–7519, 2017.

[91] A. Timbus, M. Liserre, R. Teodorescu, P. Rodriguez, and F. Blaabjerg, "Evaluation of current controllers for distributed power generation systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 654–664, 2009.

[92] Y. A.-R. I. Mohamed and E. F. El-Saadany, "A control scheme for PWM voltage-source distributed-generation inverters for fast load-voltage regulation and effective mitigation of unbalanced voltage disturbances," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 5, pp. 2072–2084, 2008.

[93] M. Castilla, J. Miret, A. Camacho, J. Matas, and L. G. de Vicuña, "Reduction of current harmonic distortion in three-phase grid-connected photovoltaic inverters via resonant current control," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1464–1472, 2011.

[94] C.-C. Hou, C.-C. Shih, P.-T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1971–1979, 2012.

[95] M. Kamalirad, H. Iman-Eini, B. Farhangi, and S. Bacha, "A reliable three-phase transformerless grid-connected PV inverter with inductive DC link," *IEEE Journal of Photovoltaics*, vol. 8, no. 5, pp. 1305–1312, 2018.

[96] J.-S. Lai, R. Young, G. Ott, J. W. McKeever, and F. Z. Peng, "A delta-configured auxiliary resonant snubber inverter," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 518–525, 1996.

[97] A. M. Trzynadlowski and S. Legowski, "Minimum-loss vector PWM strategy for three-phase inverters," *IEEE Transactions on Power Electronics*, vol. 9, no. 1, pp. 26–34, 1994.

[98] K. Rigbers, S. Schroder, R. de Doncker, P. Lurkens, M. Wendt, and U. Boke, "High-efficient soft-switching converter for three-phase grid connections of renewable energy systems," in *2005 International Conference on Power Electronics and Drives Systems*, vol. 1. IEEE, 2005, pp. 246–250.

[99] J. Shen, K. Rigbers, C. P. Dick, and R. W. De Doncker, "A dynamic boost converter input stage for a double 120 flattop modulation based three-phase inverter," in *2008 IEEE Industry Applications Society Annual Meeting*. IEEE, 2008, pp. 1–7.

[100] S. Engel, K. Rigbers, and R. W. De Doncker, "Digital repetitive control of a three-phase flat-top-modulated grid tie solar inverter," in *2009 13th European Conference on Power Electronics and Applications*. IEEE, 2009, pp. 1–10.

[101] H. Fujita, "A three-phase voltage-source solar power conditioner using a single-phase PWM control method," in *2009 IEEE Energy Conversion Congress and Exposition*. IEEE, 2009, pp. 3748–3754.

[102] Fujita, "Switching loss analysis of a three-phase solar power conditioner using a single-phase PWM control method," in *2010 IEEE Energy Conversion Congress and Exposition*. IEEE, 2010, pp. 618–623.

[103] H. Qamar, H. Qamar, D. Wu, and R. Ayyanar, "DC Link Capacitor Sizing for 240°-Clamped Space Vector PWM for EV Traction Inverters," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2021, pp. 835–841.

[104] H. Qamar, H. Qamar, and R. Ayyanar, "240°-Clamped PWM in Three Phase Grid-Connected PV Converter Application," in *2021 IEEE Energy Conversion Congress and Expo (ECCE)*. IEEE, 2021, pp. 835–841.

[105] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-connected photovoltaic systems: An overview of recent research and emerging PV converter technology," *IEEE Industrial Electronics Magazine*, vol. 9, no. 1, pp. 47–61, 2015.

[106] N. Rana, M. Kumar, A. Ghosh, and S. Banerjee, "A novel interleaved tri-state boost converter with lower ripple and improved dynamic response," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 7, pp. 5456–5465, 2017.

[107] "Synchronisation methods for grid-connected voltage source converters, author=Svensson, J," *IEE Proceedings-Generation, Transmission and Distribution*, vol. 148, no. 3, pp. 229–235, 2001.

[108] E. Twining and D. G. Holmes, "Grid current regulation of a three-phase voltage source inverter with an LCL input filter," *IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 888–895, 2003.

[109] R. Teodorescu and F. Blaabjerg, "Flexible control of small wind turbines with grid failure detection operating in stand-alone and grid-connected mode," *IEEE transactions on power electronics*, vol. 19, no. 5, pp. 1323–1332, 2004.

[110] Q. N. Trinh, P. Wang, Y. Tang, and F. H. Choo, "Mitigation of DC and harmonic currents generated by voltage measurement errors and grid voltage distortions in transformerless grid-connected inverters," *IEEE Transactions on Energy Conversion*, vol. 33, no. 2, pp. 801–813, 2017.

[111] A. I. Putri, A. Rizqiawan, T. Rachmilda, Y. Haroen, and P. A. Dahono, "Suppressing dead-time effect in current-controlled three-phase PWM inverters by using virtual inductor," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2018, pp. 867–871.

[112] T. Ye, N. Dai, C.-S. Lam, M.-C. Wong, and J. M. Guerrero, "Analysis, design, and implementation of a quasi-proportional-resonant controller for a multifunctional capacitive-coupling grid-connected inverter," *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 4269–4280, 2016.

[113] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. John wiley & sons, 2003.

[114] E. Kabir, P. Kumar, S. Kumar, A. A. Adelodun, and K.-H. Kim, "Solar energy: Potential and future prospects," *Renewable and Sustainable Energy Reviews*, vol. 82, pp. 894–900, 2018.

[115] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Transactions on Industry Applications*, vol. 41, no. 5, pp. 1292–1306, 2005.

[116] T. Kerekes, R. Teodorescu, M. Liserre, C. Klumpner, and M. Sumner, "Evaluation of three-phase transformerless photovoltaic inverter topologies," *IEEE Transactions on Power Electronics*, vol. 24, no. 9, pp. 2202–2211, 2009.

[117] O. Lopez, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesana, J. Malvar, R. Teodorescu, and J. Doval-Gandoy, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Transactions on Energy Conversion*, vol. 25, no. 1, pp. 140–147, 2010.

[118] T. Kerekes, R. Teodorescu, and U. Borup, "Transformerless photovoltaic inverters connected to the grid," in *APEC 07-Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*. IEEE, 2007, pp. 1733–1737.

[119] I. S. 1547.2, "IEEE application guide for IEEE Std 1547 (TM). IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems," 2009.

[120] S. Anand, S. K. Gundlapalli, and B. G. Fernandes, "Transformer-less grid feeding current source inverter for solar photovoltaic system," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 10, pp. 5334–5344, 2014.

[121] N. Noroozi and M. R. Zolghadri, "Three-phase quasi-Z-source inverter with constant common-mode voltage for photovoltaic application," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4790–4798, 2017.

[122] Y.-S. Lai and F.-S. Shyu, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part I: basic development," *IEEE Transactions on Industry Applications*, vol. 40, no. 6, pp. 1605–1612, 2004.

[123] J. Zitzelsberger and W. Hofmann, "Reduction of Bearing Currents in inverter fed drive applications by using Sequentially Positioned Pulse Modulation," *EPE journal*, vol. 14, no. 4, pp. 19–25, 2004.

[124] "Reduction of common-mode currents in PWM inverter motor drives, author=Cacciato, Mario and Consoli, Alfio and Scarcella, Giuseppe and Testa, Antonio," *IEEE Transactions on Industry Applications*, vol. 35, no. 2, pp. 469–476, 1999.

[125] E. Un and A. M. Hava, "A near-state PWM method with reduced switching losses and reduced common-mode voltage for three-phase voltage source inverters," *IEEE Transactions on Industry Applications*, vol. 45, no. 2, pp. 782–793, 2009.

[126] R. Rahimi, S. Farhangi, B. Farhangi, G. R. Moradi, E. Afshari, and F. Blaabjerg, "H8 inverter to reduce leakage current in transformerless three-phase grid-connected photovoltaic systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 910–918, 2017.

[127] C. P. Systems, "Grid-Tied PV Inverter, CH275KTL-DO/US-800 datasheet," https://www.chintpowersystems.com/wp-content/uploads/2021/12/CPS-SCH275KTL-DO-US-800-User-Manual-Rev-1.0-November-2021.pdf, 2021, original document from Chint Power Systems.

[128] ABB, "ABB string inverters", TRIO-20.0/27.6-TL-OUTD 20 to 27.6 kW datasheet," https://www.solaris-shop.com/content/TRIO-20.0-TL-OUTD-S1B-US-480-A%20Specs.pdf, 2015, original document from ABB.

[129] D. Menzi, D. Bortis, and J. W. Kolar, "Three-phase two-phase-clamped boost-buck unity power factor rectifier employing novel variable dc link voltage input current control," in *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*. IEEE, 2018, pp. 1–8.

[130] J. Roy, Y. Xia, and R. Ayyanar, "Performance evaluation of single-phase transfomer-less PV inverter topologies," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2018, pp. 3250–3255.

[131] SMA, "Leading Leakage Currents, SMA Technical Information, Leakage current-TI-en-26, version 2.6," https://files.sma.de/downloads/Ableitstrom-TI-en-26.pdf, 2015, original document from SMA.

[132] SMA., "Capacitive Leakage Currents, SMA Technical Information, Albeitstrom-TI-en-25, version 2.5," http://www.sprsolarroof.co.th/media/pdf/5d2846461b8bd.pdf, 2014, original document from SMA.

[133] Y. Zhou, W. Huang, P. Zhao, and J. Zhao, "A transformerless grid-connected photovoltaic system based on the coupled inductor single-stage boost three-phase inverter," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1041–1046, 2013.

[134] J.-S. Lee and K.-B. Lee, "New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1720–1732, 2013.

[135] Y. Bae and R.-Y. Kim, "Suppression of common-mode voltage using a multi-central photovoltaic inverter topology with synchronized PWM," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 9, pp. 4722–4733, 2013.

[136] R. Rahimi, M. Farhadi, G. R. Moradi, B. Farhangi, and S. Farhangi, "Three-phase filter-clamped transformerless inverter for grid-connected photovoltaic systems with low leakage current," *IEEE Transactions on Industry Applications*, 2020.

[137] M. Schinkel, S. Weber, S. Guttowski, W. John, and H. Reichl, "Efficient HF modeling and model parameterization of induction machines for time and frequency domain simulations," in *Twenty-First Annual IEEE Applied Power Electronics Conference and Exposition, 2006. APEC'06.* IEEE, 2006, pp. 6–pp.

[138] A. Janabi and B. Wang, "Hybrid SVPWM scheme to minimize the common-mode voltage frequency and amplitude in voltage source inverter drives," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1595–1610, 2018.

[139] M. Asefi and J. Nazarzadeh, "Integral-series Fourier analysis of chaotic PWM patterns for common mode voltage stresses," *IET Power Electronics*, vol. 11, no. 9, pp. 1591–1602, 2018.

[140] G. Narayanan and V. Ranganathan, "Analytical evaluation of harmonic distortion in PWM AC drives using the notion of stator flux ripple," *IEEE Transactions on Power Electronics*, vol. 20, no. 2, pp. 466–474, 2005.

[141] M. C. Cavalcanti, K. C. De Oliveira, A. M. De Farias, F. A. Neves, G. M. Azevedo, and F. C. Camboim, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 4, pp. 1360–1368, 2009.

[142] J. Liu, S. Cheng, and A. Shen, "A high efficiency two-stage inverter for photovoltaic grid-connected generation systems," *Journal of Power electronics*, vol. 17, no. 1, pp. 200–211, 2017.