Field Effect Transistors with Emerging Two-Dimensional Semiconductor Channels for Future Complementary-Metal-Oxide-Semiconductor (CMOS) Technologies

by

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ABSTRACT

The research of alternative materials and new device architectures to exceed the limits of conventional silicon-based devices has been sparked by the persistent pursuit of semiconductor technology scaling. The development of tungsten diselenide (WSe_2) and molybdenum disulfide (MoS_2), well-known member of the transition metal dichalcogenide (TMD) family, has made great strides towards ultrascaled two-dimensional (2D) field-effect-transistors (FETs). The scaling issues facing silicon-based complementary metal-oxide-semiconductor (CMOS) technologies can be solved by 2D FETs, which show extraordinary potential.

This dissertation provides a comprehensive experimental analysis relating to improvements in p-type metal-oxide-semiconductor (PMOS) FETs with few-layer WSe_2 and high-κ metal gate (HKMG) stacks. Compared to this works improved methods, standard metallization (more damaging to underlying channel) results in significant Fermi-level pinning, although Schottky barrier heights remain small (< 100 meV) when using high work function metals. Temperature-dependent analysis reveals a dominant contribution to contact resistance from the damaged channel access region. Thus, through less damaging metallization methods combined with strongly scaled HKMG stacks significant improvements were achieved in contact resistance and PMOS FET overall performance. A clean contact/channel interface was achieved through high-vacuum evaporation and temperature-controlled stepped deposition. Theoretical analysis using a Landauer transport adapted to WSe_2 Schottky barrier FETs (SB-FETs) elucidates the

prospects of nanoscale 2D PMOS FETs indicating high-performance towards the ultimate CMOS scaling limit.

Next, this dissertation discusses how device electrical characteristics are affected by scaling of equivalent oxide thickness (EOT) and by adopting double-gate FET architectures, as well as how this might support CMOS scaling. An improved gate control over the channel is made possible by scaling EOT, improving on-off current ratios, carrier mobility, and subthreshold swing. This study also elucidates the impact of EOT scaling on FET gate hysteresis attributed to charge-trapping effects in high-κ-dielectrics prepared by atomic layer deposition (ALD). These developments in 2D FETs offer a compelling alternative to conventional silicon-based devices and a path for continued transistor scaling. This research contributes to ongoing efforts in 2D materials for future semiconductor technologies. Finally, this work introduces devices based on emerging Janus TMDs and bismuth oxyselenide (Bi_2O_2Se) layered semiconductors.

DEDICATION

This dissertation is dedicated to my partner and my family who have supported me continuously throughout my education.

ACKNOWLEDGMENTS

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INTRODUCTION

1.1 Background and Motivation

Chipmakers have been releasing CMOS integrated circuits (ICs) with an exponentially rising number of individual MOSFETs and an exponentially falling cost per transistor to the market for decades. The constant reduction in MOSFET size, for short scaling, is essential to this progression. With an annual volume of approximately $300 billion, the semiconductor chip business can be generally classified into two main domains: More Moore and More Than Moore. More Moore takes over 70% of the entire chip market and includes digital integrated circuits like microprocessors and memories[1]. It is captivating to note that standard digital integrated circuits (ICs) rely on a single semiconducting material, Si, a single type of transistor, the Si MOSFET, and a single circuit technique, silicon CMOS, which uses both n-channel MOSFETs, in which the transistor's output current is carried by electrons, and p-channel MOSFETs, in which the current is carried by holes. MOSFET gate length has decreased from 10 μm (1970) and is now approaching 10 nm (2020) as illustrated in Figure 1(a)[1]. The supply voltage V_{DD} has also decreased as noted by the labels on the solid blue line (from 15 V to 0.68 V) illustrated in Figure 1(a) [1-2]. The roadmap indicates targets for future CMOS nodes (towards year 2030) with MOSFET gate length at 5.1 nm presenting serious challenges for silicon technologies as they face difficulties in scaling below 10 nm channel lengths.

Another roadmap for advanced Si technology from TSMC shows the evolution of MOSFET scaling and indicates that that 2.6 trillion MOSFET per chip is commercially

available at the 7 nm technology node[3] (Figure 1(b)). In order to continue these scaling trends (as dictated by Moore's Law), physical scaling alone is not sufficient. A critical issue for bulk semiconductors like silicon relates to degradation in mobility when channel thickness is reduced as needed for scaling down channel length. Moreover, quantum-mechanical source-drain tunneling must be considered as the distance between the MOSFET source and drain regions becomes so small (few nanometers). Given that a heavy carrier effective mass lowers source-drain tunneling, it may turn out that heavy effective mass materials or materials with anisotropic effective mass will become preferred for sub-5 nm MOSFETs. According to International Roadmap for Device and Systems (IRDS) 2022[4], scaling in recent years has concentrated on additional performance-boosting methods, such as applying strain to the channel, stress boosters, high-κ metal gates to sustain scaling at low voltage. The IRDS also indicates that for "More Moore" scaling the FinFET continues to be the primary device architecture and that a shift to gate-all-around (GAA) devices is anticipated to begin soon. Fin-width scaling limitations could be the reason behind this circumstance[4]. The IRDS 2022 edition also indicates that the 2 nm technology node with GAA technology will be available around 2023.[4] More importantly, the IRDS envisions that by 2028 (1.5 nm node) two-dimensional (2D) materials will play a significant role in complementary devices and that by 2034 (0.7 nm node and beyond) 2D materials will be the primary channel material.[4]

Graphene was the first 2D material to be thoroughly examined, and its potential as a material for electronic devices has been intensively investigated. Since the discovery of graphene in 2004, 2D materials have attracted a lot of attention for their potential use in

electronic devices, circuits, and systems[1]. The lack of a bandgap in graphene limits its applicability as a semiconductor for efficient switching behavior. Semiconductors can change from a non-conductive (OFF) state to a conductive (ON) state and vice-versa with the application of a gate voltage. Since graphene lacks a band gap, switching applications are not likely given its small ON/OFF ratio and limited gate voltage control. On the other hand, transition metal dichalcogenides (TMDs), for example MoS_2, WSe_2, etc., offer a configurable bandgap (with thickness) that may be tailored for certain device applications. Thus, semiconducting 2D TMDs are promising candidates to enable downscaling of FETs supporting the continuation of Moore's law for years to come[2]. This is due to their layered van der Waals (vdW) structure that can be thinned down to a single atomic sheet (< 1 nm) with dangling-bond-free surfaces. A thin semiconducting body is needed for extreme scaling of transistors to maintain good electrostatic control of the channel thereby suppressing short-channel effects (SCE) that would otherwise degrade their performance. In 2011, a team of researchers at IBM's T. J. Watson Research Center realized the first MoS_2 FET. Under the direction of Dr. Andras Kis, the group created a MoS_2 FET with channel thickness of three atomic layers[5]. According to this study, MoS_2 can be utilized to make functional transistors, which are essential components of contemporary electronic

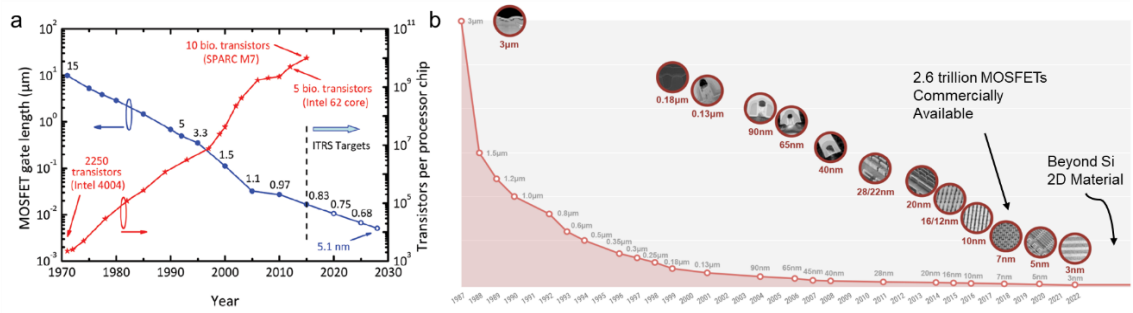

Figure 1. (a) The number of transistors integrated on a single computer chip and the MOSFET gate length's evolution. The processor supply voltage (VDD) is indicated by the digits above the gate length curve.[1] (b) Advance Si roadmap of TSMC.[3]

devices. The MoS_2 channel three-layer thickness demonstrated the feasibility of constructing atomic-scale electrical devices. Figure 2(a) illustrates the first ever fabricated MoS_2 FET. The source and drain, two reservoirs of mobile charges, are connected by a channel area that makes up the FET. A thin insulating barrier divides the channel from the third electrode, or gate. The channel conductivity is governed by the applied gate-source voltage (V_{GS}), and the drain current (I_D) is driven through the transistor by the drain-to-source voltage (V_{DS}). Figure 2(b) illustrates the transfer characteristic for the FET and with extracted FET mobility (μ_{FET}) in the 200-230 $cm^2V^{-1}s^{-1}$ range, which at the time represented a noteworthy accomplishment for 2D materials[5].

Bulk semiconductors are utilized to create the channel in modern CMOS technology, but these materials cannot be scaled below 5 nm in thickness without posing substantial problems relating to variance, surface roughness, and dangling bonds, which reduce charge carrier mobility (see inset Figure 3a)[6–9]. This presents a limit to the scaling of transistors (e.g., cannot be scaled to channel lengths below ~10 nm), even for non-planar designs such as FinFET and nanowire/nanosheet devices. However, sub-10 nm channel length FETs with well-controlled electrostatics and suitable mobilities can be fabricated

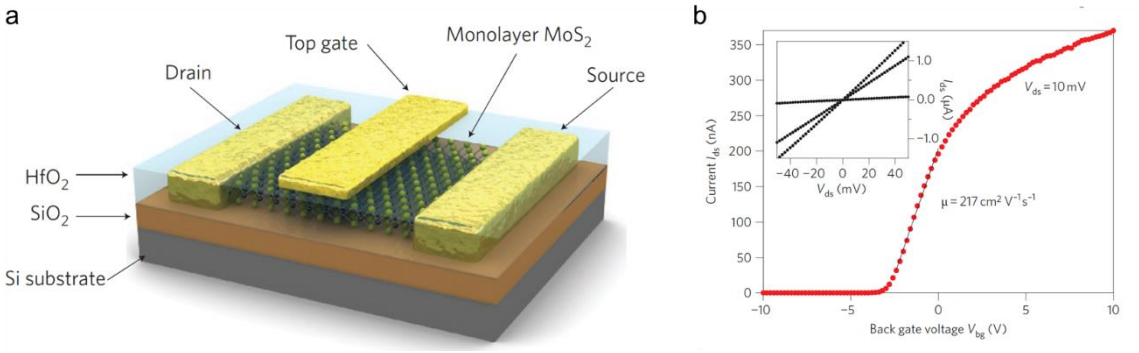

Figure 2. (a) 3D schematic of a back gated MoS_2 FET with SiO_2(270 nm) as gate stack showing source, drain and top gate[5] (b) First demonstration of room temperature transfer characteristics for MoS_2 back gated FET with a 10 mV drain to source bias.[5]

using 2D semiconductors (e.g., TMDs) which retain their desirable electronic properties even at the limit of a single atomic layer (i.e., monolayer with thickness < 1 nm)[10–15]. Thus, 2D semiconductors may be integrated into CMOS processes to enable the ultimate scaling of CMOS technology. Additionally, 2D FETs can be integrated in the back-end-of-line (BEOL) of CMOS processes to support monolithic 3D integration of integrated circuits (ICs) based on multi-tier integration of 2D devices[16]. Moreover, different 2D materials can be stacked to assemble unique artificial materials known as van der Waals (vdW) heterostructures that may enable new and improved electronic functionality[17–19]. Figure 3(a) illustrates a roadmap for the introduction of 2D semiconductors in CMOS technology to enhance density of integration and improve chip performance, as well as for monolithic 3D integration and added functionality (e.g., CMOS+X)[20]. A state-of-the-art silicon gate-all-around (GAA) FET with stacked "nanosheets" (~5 nm thickness) is shown along the silicon track, whereas an FET with stacked 2D nanosheets (< 1 nm thickness) illustrates the ultimate scaling of the same device architecture along the 2D materials track[21]. The inset shows the effect of body thickness scaling on carrier mobility, contrasting the

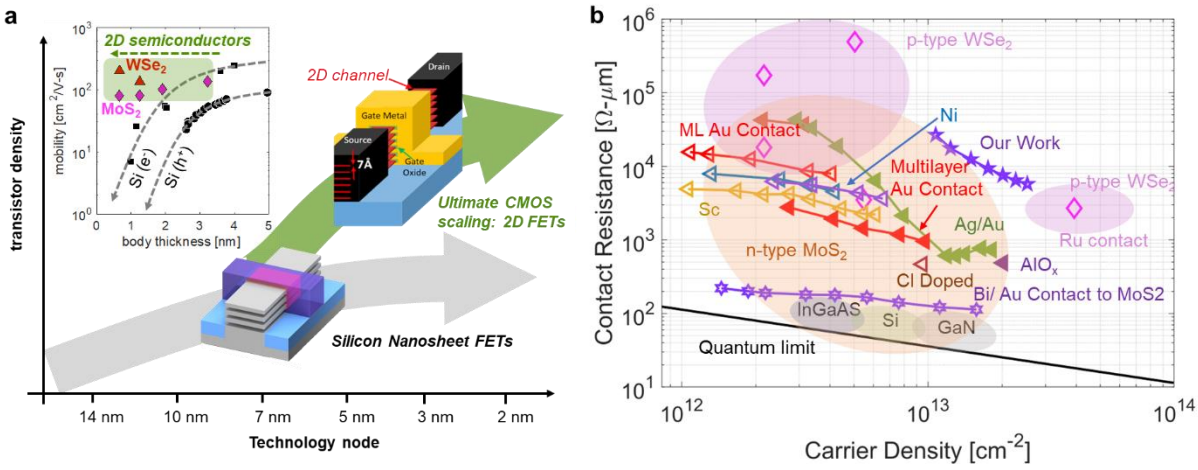

Figure 3. (a) Roadmap for introduction of 2D materials in CMOS technology to enhance scaling, density of integration, and chip performance, as well as to enable new functionality (e.g., in CMOS+X), and 3D monolithic integration. Two tracks are shown, one for silicon gate-all-around (GAA) FETs with stacked nanosheets (each sheet ~ 5 nm in thickness), and one for FETs with stacked 2D nanosheets (< 1 nm thickness for monolayer semiconductors) © [2021] IEEE. Reprinted, with permission, from[15]. Inset shows mobility degradation with scaling both thickness in Si devices (e.g., the nanosheet thickness), while 2D semiconductors shown negligible degradation down to a monolayer. (b) Plotting recently published contact resistance of several semiconductor technologies (Si, III-Vs, and MoS_2) as a function of carrier density revealing the state-of-the-art contact technique for MoS_2 transistors[16,17,55].

prohibitive degradation in silicon[9,10] against 2D semiconductors (MoS_2, WSe_2)[11–16] showing little or no effect in mobility down to a monolayer (< 1 nm).

CMOS technology uses complementary n-type and p-type transistors to implement logic functions. To achieve the ultimate scaling of CMOS technology with 2D materials, both n-type and p-type MOS (i.e., 2D NMOS and 2D PMOS) FETs are needed. While substantial efforts have been dedicated to improving 2D NMOS devices (e.g., using MoS_2 semiconducting channels), the performance of 2D PMOS FETs has fallen behind. Consequently, new efforts have emerged[21–23] to elucidate the weaknesses of 2D PMOS devices and to develop improved methods to enhance their performance. In the typical

device configuration, metal contacts are placed directly over the 2D semiconducting channel, forming Schottky barriers (SB), and are referred to as SB-FETs[24–27]. As established by previous work[12,25], this leads to the contacts playing a significant role in the operation and performance of the device. However, a comprehensive study of contacts in 2D PMOS FETs in the context of these recent efforts is lacking. Fig 1.(b) plots contact resistance as a function of carrier density from recent published papers showing that contact resistance for MoS_2 can get to as low as 200 Ω-μm[28]. Compared to the best reported result of MoS_2 , p-type WSe_2 shows contact resistance of 2.7 K-Ω-μm, which is one magnitude higher.

Hence, my study updates the examination of 2D WSe_2 PMOS devices, focusing on contact resistance and how it affects device performance. Moreover, recent research has demonstrated the need for strongly scaled insulators to improve gate control and lessen the effect of the Schottky barriers[29]. Still, previous efforts aimed at improving 2D PMOS FETs through improved contacts have only demonstrated devices without scaled insulators (i.e., used silicon substrate as common gate with thick gate dielectrics > 100 nm)[23]. Contrarily, our study shows several ways to increase contact resistance using SB-FETs with a few nm high-κ metal-gate (HKMG) stacks. Furthermore, we report improvements in 2D PMOS FET performance benchmarks against the best published results, and elucidate the performance limits of extremely scaled 2D PMOS FETs through quasi-ballistic transport models based on the Landauer formalism.

The electrostatics of the FET must be maintained throughout scaling in order to reap the benefits of the reduced dimensions and improved contact resistance in terms of

power savings and switching speeds. To accomplish that, the gate electrode must offer superior gate control. This greater gate control can be attained solely by reducing the equivalent oxide thickness (EOT). The EOT targets in the IRDS are provided indirectly; an EOT of 0.6 nm is targeted in 2022 based on the reported inversion layer thickness of 1 nm.[4,5] Good gate control, minimal gate leakage, exceptional interface, small remote dispersion, minimal electrically active border traps, high dielectric breakdown field, uniform deposition on top of 2D semiconductors, and threshold voltage tuning with metal gate are some of the factors that are imposed on successful EOT scaling. These eventually lead to high ON current and low OFF current, help achieve the theoretical limit subthreshold swing (SS) of 60 mV/dec, high FET reliability, and small gate hysteresis. Current density (gate current) for most of the dieletric material increase with scaling of EOT towards 1 nm or less. In general, insulators with higher dielectric constants such as HfO_2 yield reduced current densities at comparable EOT. Previous work has focused on finding suitable gate insulator through model efforts considering tunneling and other physical mechanisms (e.g., trapping)[28]. From the band alignment with 2D channel material, dielectric constant, and effective mass, potential gate insulators have been identified from amorphous, layered and native oxides. It was concluded that layered insulators, such as MICA or TiO_2, are suitable for p-type FETs but not for n-type transistors. Similar to amorphous oxide Al_2O_3, amorphous HfO_2 exhibits adequate capacity to prevent leakage current. Establishing dependable interface and border trap densities as well as characterizing insulator defect bands is critical. The phenomenon of hysteresis is a significant obstacle in the development of FETs with emerging 2D semicondcutors. When

a transistor is subjected to successive forward and reverse voltage sweeps, its electrical characteristics will exhibit fluctuations known as hysteresis. In modern electronics, this kind of hysteresis can result in diminished dependability, increased power consumption, and inaccurate signal processing. However, the scaling of EOT can help address and reduce hysteresis effects. EOT scaling is the process of lowering the thickness of the gate dielectric while preserving its electrical characteristics. As such, the research presented in this dissertation focued on styding the potential of EOT scaling to enhance the management of charge carriers within the transistor channel. This work establishes the connection between FET hysteresis and EOT scaling, clarifying how a reduction in EOT can aid in the attenuation of hysteresis. Improvement in gate control, limiting hysteresis, and reducing charge trapping by reducing the EOT has been observed in this work, which would ultimately result in more dependable and effective FET devices. On top of scaling of EOT further imporvment have been demonstrated using a double gated transistor structure with single atomic layer as the channel. These double-gated architecture offers a flexible framework for adapting and improving semiconductor device performance. With independent gate control, important parameters such as Subthreshold swing, field effect mobility, on-off ratio can be precisely optimized, which improves efficiency, lowers power consumption, and improves overall functionality in a variety of electronic applications. In addition to Si technology, these 2D-materials-based double-gated transistors are expected to meet the demands of advanced computer technologies like cloud computing and the Internet of Things, which require highly integrated and adaptable electronic systems. Double gate FET architectures consist of two surface gates allows it to achieve very low

leakage and introduce adjustable field gradients which potentially will limit short channel effects[29]. This work describes double gate device architecture with symmetric top and bottom gate over the channel and same level of overlaying with drain and source region, that allows to regulate the transit of injected carriers over the Schottky contacts barrier at the drain and source. The double gate devices demosntrated improved features such as reduced subthreshold swing and high on/off, and reconfigurable threshold voltage control. The combination of Double-Gate control and EOT scaling creates an additive impact that makes it possible to develop FET devices that not only satisfy CMOS scaling requirements but also help realize new and extremely efficient semiconductor architectures.

CHAPTER 2

Improvements in 2D p-type WSe_2 transistors towards ultimate CMOS scaling

2.1 Device Design and Fabrication

P-type conduction in 2D FETs can be achieved using a variety of techniques, including contact engineering, chemical doping, and/or electrostatic doping. Our work uses a transfer length method (TLM) structure to demonstrate p-type devices with few layer (3-5 layer) WSe_2 channels. These are designed and fabricated with a high-κ metal-gate (HKMG) stack featuring 8 nm of either Al_2O_3 or HfO_2 gate dielectrics. High work function (WF) metal contacts were used to facilitate the injection and conduction of positively charged carriers (holes) into the WSe_2 channels. This is enabled through the suitable alignment of metal contact Fermi levels with the edge of the valence band in the semiconducting channel. This

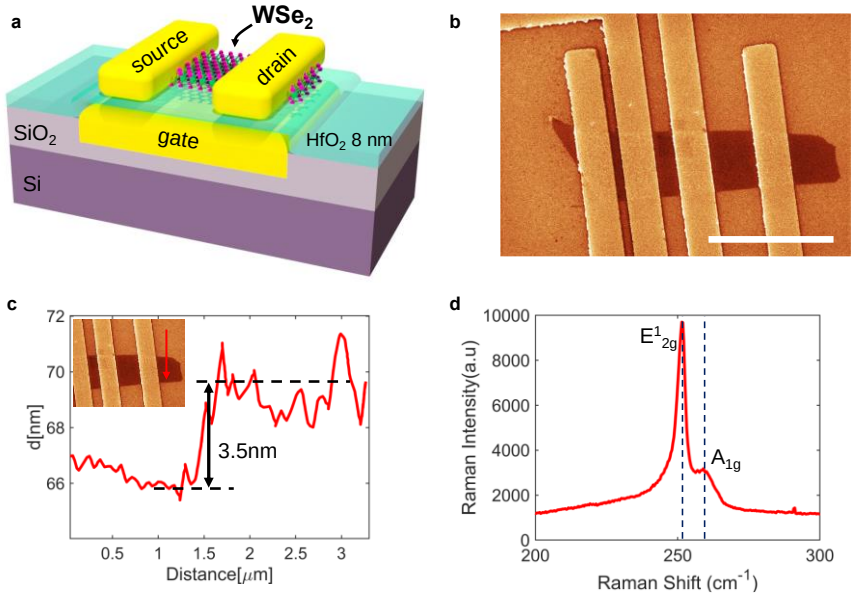

Figure 4. (a) Schematic of 2D WSe_2 PMOS FETs studied in this work. The FETs are configured in a transfer length method (TLM) structure and have a gate-first design with high-κ metal-gate (HKMG) stack. Two different gate dielectrics were used in this work (Al_2O_3 and HfO_2) with a thickness of 8 nm. (b) Scanning electron microscope (SEM) image of the WSe_2 TLM structure (scale bar indicates 3 μm in length). (c) Atomic force microscopy (AFM) surface topography scan (non-contact mode) reveals a WSe_2 channel thickness of ~3.5 nm (approximately 5 layers). (d) Raman spectrum of the channel region showing E^1_{2g} and A_{1g} peaks consistent with ~5 layers of WSe_2.

work presents results on devices with Pt (WF of 5.65 eV)[34] and Pd (WF of 5.22 eV)[23] metal contacts. A 3D schematic of the TLM structures is shown in Figure 4a. In brief, a gate-first technique was used to fabricate FETs with HKMG stacks and various channel lengths on a TLM configuration. As shown by previous work[35], the gate-first approach can lead to improved 2D FET uniformity, channel mobility, and subthreshold swing. Our gate-first HKMG process includes patterning and deposition of a Cr/Au metal gate (e-beam lithography, evaporation, and lift-off) followed by atomic-layer deposition (ALD) of the high-κ-dielectric (8 nm Al_2O_3 or HfO_2).

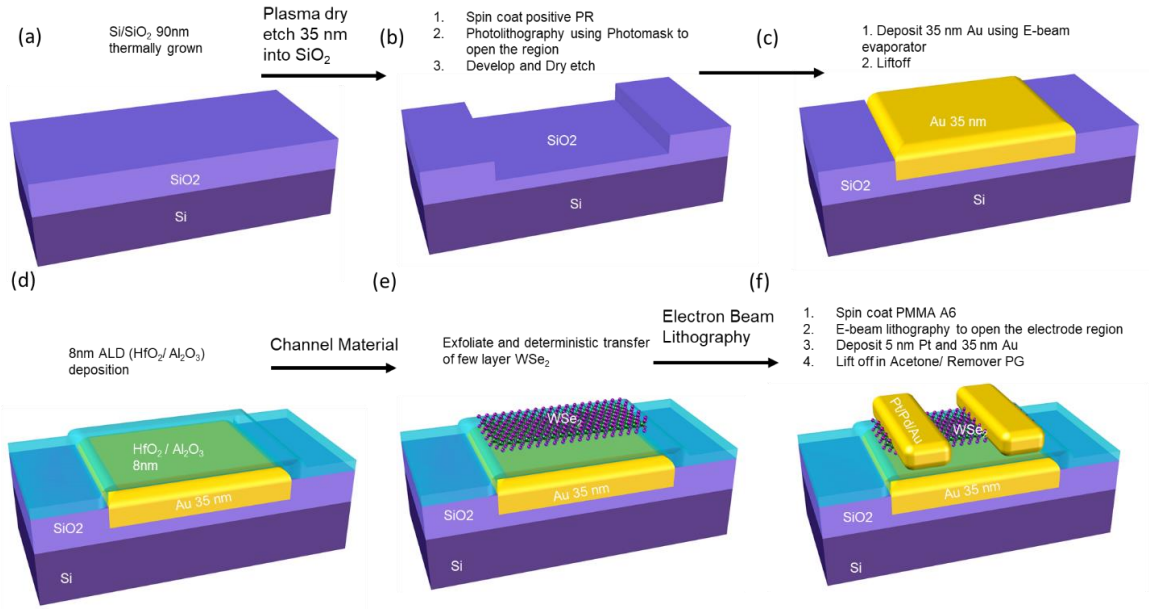

Figure 5. (a)3D schematic of Si/SiO_2(90 nm) (b) Si/SiO_2 has been trenched by oxygen plasma at a rate of 60 Å per second. (c) E-beam evaporation of gate metal (d) 8 nm ALD at 180 ºC (e) Exfoliate and deterministic transfer of few-layer WSe_2. (f) Electron beam lithography to pattern source and drain electrode, followed by metal evaporation and liftoff.

The thickness and relative permittivity of the ALD dielectrics are verified by non-contact atomic force microscopy (AFM) and capacitance measurements. Once the gate stack is in place, a deterministic transfer process is used to form the WSe_2 channel. Here, exfoliated WSe_2 samples were carefully selected through optical inspection to obtain the

desired thickness and homogeneity across the entire TLM structure. After transferring the WSe_2 channels, the metal contacts (i.e., the source and drain electrodes of the FETs) are prepared through e-beam lithography, deposition, and lift-off. Figure 5. Shows the device fabrication process flow from the starting wafer to 2 terminal field effect transistor. We note that the quality of the contracts, and consequently the performance of the FETs, depends strongly on this metal deposition process as will be described in the sections below. The contacts are placed at different distances to result in FETs with various channel lengths. A scanning electron microscopy (SEM) image of a typical sample is show in in Figure 4(b). The SEM images provide verification of the surface morphology and WSe_2 channel uniformity.

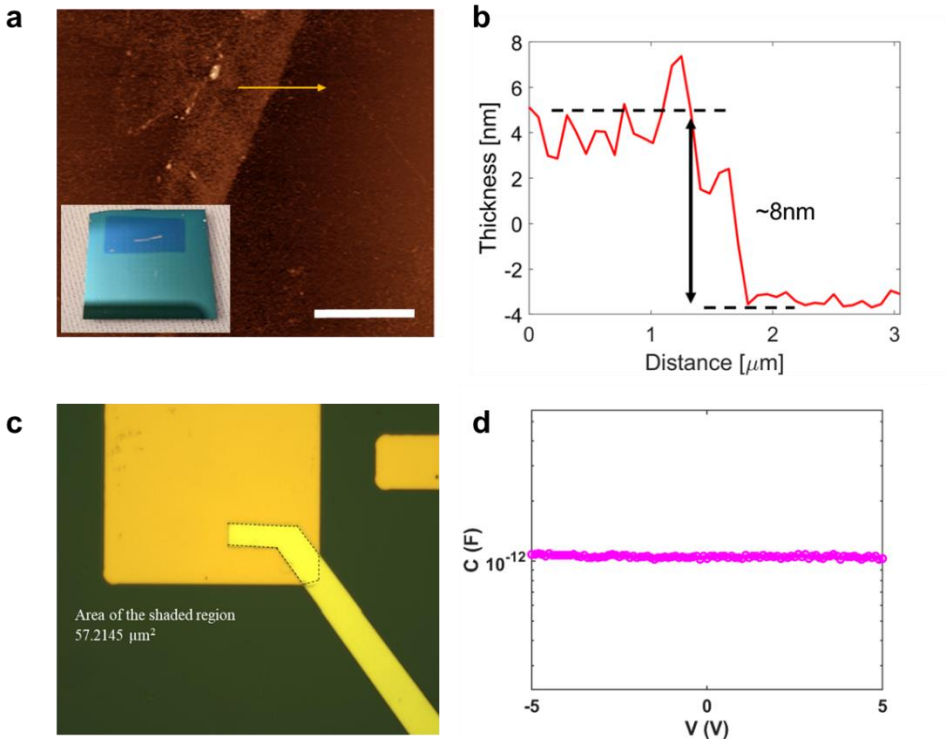

Figure 6. (a) & (b) non-contact mode AFM image revealing a step height of 8 nm corresponding to ALD HfO_2 film thickness (c) Optical image of a metal -insulator-metal with an overlapping area of 57.2145 μm^2. (d) Measured capacitance is 1pf over the entire range of applied voltage, is used to calculate the dielectric constant of HfO_2.

2.2 2D Material and High-κ-dielectric Insulator Characterization

In our analysis we need to use Oxide capacitance per unit area to analyze our devices. Which is why we have done gate stack characterization. Figure 6 shows dielectric gate stack characterization. Non-contact mode AFM surface topography has been conducted to obtain HfO_2 gate dielectric layer thickness. The ALD deposition rate employed to construct the devices used in this work is consistent with the measured film thickness (Figure 6 (b)). Optical microscope image showing the metal-insulator-metal (MIM) capacitance test structure (Figure 6 (c)). It functions as a parallel-plate capacitor with 8 nm HfO_2 ALD dielectric. The area of the capacitor (enclosed by dashed line) is ~57.2 μm^2. (right). The capacitance is measured at ~1 pF over the full range of entire voltages. The dielectric constant of the oxide is obtained as $K_{ox} = Ct_{ox}/\varepsilon_0 A$, where C is capacitance, A is the area, ε_0 is the permittivity of free space (8.854 x 10-12 Fm^{-1}) and t_{ox} = 8 nm is the oxide thickness. We extract a dielectric constant of 16.889 for HfO_2.

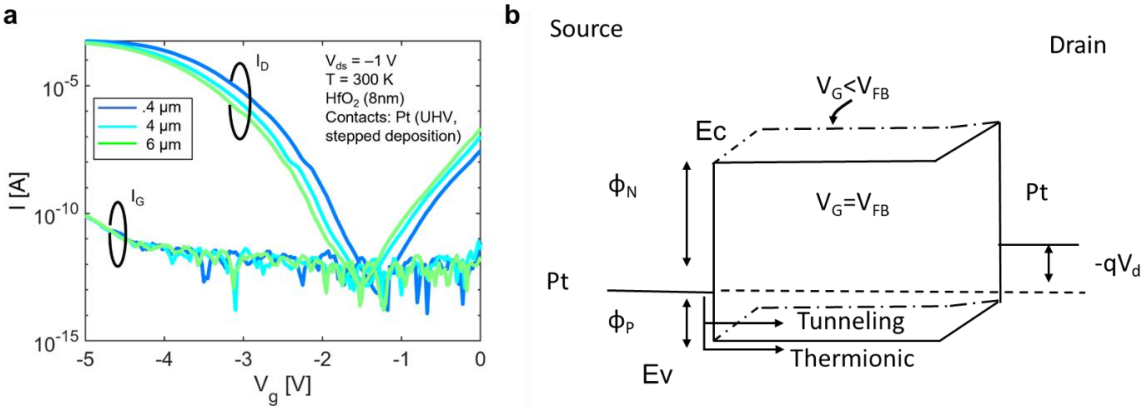

Figure 7. (a) Typical I-V characteristics for three different channel lengths are shown (.4µm, 4µm, 6µm) where gate current (I_G) is negligible over all gate voltages compared to drain current (I_D). (b) Band diagram showing the mechanism of injecting hole into the channel

Additional analysis and precise determination of the channel thickness is obtained from atomic force microscopy (AFM) surface topography scans across the WSe_2 regions. A typical AFM measurement is shown in Figure 4(c) where a step in the surface profile reveals a channel thickness of ~3.5 nm (this corresponds to approximately 5 layers of

WSe_2). To further verify the quality and number of WSe_2 layers Raman spectroscopy in the channel region of the fully fabricated FETs have been conducted. A typical Raman spectrum is shown in Figure 4d, where the first and second peaks, centered near 250 cm^{-1}, correspond to the E^1_{2g} and A^1_g modes. As explained in previous work[36], these vibrational modes and the position of the peaks are sensitive to the number of WSe_2 layers. For example, the E^1_{2g} peak will experience a right shift (away from 250 cm^{-1}) with increasing number of layers, but the A^1_g mode exhibits little dependency on film thickness. In our Raman spectra we observe right shifts in E^1_{2g} peaks that are consistent with approximately 4-5 layers of WSe_2. In addition to the peak position, the full width at half maximum (FWHM) can serve to indicate the crystalline quality of the WSe_2 sample[37]. We observe FWHM of ~4.8 cm^{-1} indicating that the crystalline quality of the channel regions has not been compromised after the fabrication process. Figure 7(a) illustrates initial p-type WSe_2 FET data showing negligible gate leakage. The gate current is around 100 pA to 1 nA, whereas the drain current is at 100 µA in the ON state. The combination of electron and hole current flowing respectively in the conduction and valence bands results in ambipolar transfer characteristics. However, the alignment of the electronic bands in the channel and the Fermi levels in the source/drain contacts determines the relative strength of the electron and hole branches. In this case, a better alignment with the valence band results in a stronger p-type conduction. Relating to the p-type WSe_2 devices presented in this work, the energy band diagram (Figure 7(b)) depicts the charge transport mechanism in a Schottky barrier (SB) MOSFETs. The band diagram, which is displayed for a negative V_{ds}, represents biasing conditions when V_g is greater than or equal to the flat-band voltage (V_{fb}). We see that there is a smaller Schottky barrier for holes than for electrons in the flat-band condition, which explains why p-type conduction is stronger. When going beyond V_{fb} and biasing deeper into the ON-state a triangular barrier is formed at the Schottky contact/channel junction enabling tunneling to begin. Both thermionic emission and tunneling (field emission) mechanisms for injecting holes into the channel are illustrated in Figure 7(b).

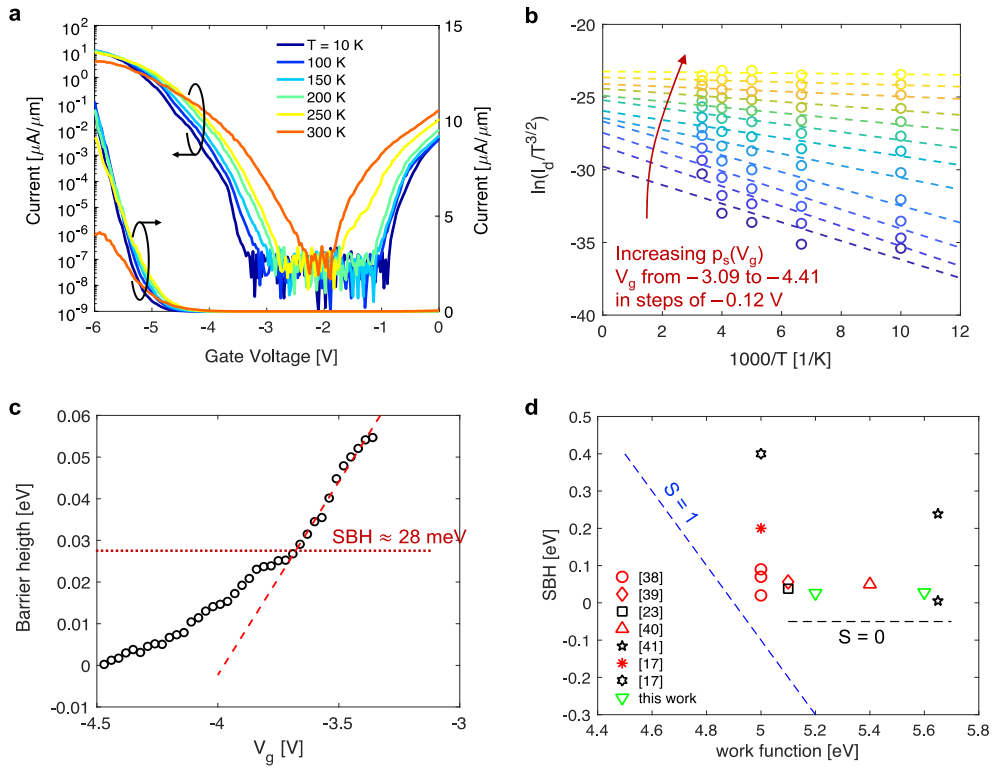

Figure 8. (a) I_d-V_g characteristics at different temperatures ranging from 300 K down to 10 K for WSe_2 PMOS FET with L = 400 nm, and for V_{ds} = –1 V. Current (normalized to channel width) is plotted in linear (right axis) and logarithmic scale (left axis). (b) Arrhenius plot of thermionic emission current in 2D semiconductor obtained for different values of V_g (from –3.09 V to –4.41V) corresponding to different values of sheet carrier density, p_s. The slope (dashed lines) can be used to extract barrier height. (c) Extractions of barrier height plotted as a function of gate bias, the dashed lines indicate the flat-band voltage for which a deviation from the linear trend is observed, and where barrier height is exactly the Schottky barrier height. (d) Our extracted Schottky barrier heights (SBH) as a function of the metal work function. Also shown are extractions from previous published works on WSe_2 PMOS FETs with different types of metals. The collection of experimental results appears to indicate significant Fermi level pinning (S ~ 0). However, the SBH is small (< 100 meV) in most cases, suggesting other factors contributing to large contact resistivity observed in 2D PMOS FETs.

2.3 Analysis of Schottky Barriers

Device performance is greatly influenced by the Schottky junctions between source/drain contacts and the semiconducting channel because they can greatly affect

contact resistivity. [12,25]. The Schottky barrier height (SBH), which represents the potential energy barrier preventing the injection of charge carriers from metal to semiconductor, is a crucial characteristic for these junctions. We can select metal contacts with WF that result in good band alignment (i.e., a small SBH) and ideally a seamless injection of charge carriers into the channel. However, non-ideal effects may be at play, such as Fermi-level "pinning", affecting our ability to correctly adjust the SBH[40,41]. Therefore, it is essential to extract the SBH to identify the contribution of Schottky junctions on contact resistivity. Figure 8a plots the I_d-V_g characteristics for a WSe_2 PMOS FET with Al_2O_3 gate dielectric, Pt/Au contacts (deposited with standard e-beam evaporation technique), and L = 400 nm, measured at various temperatures from 300 K down to 10 K, and V_{ds} = –1V. We note that a different I_{on} is achieved in this device (compared to Figure 7a) because of a larger contact resistance resulting from the standard e-beam evaporation technique. However, it is still useful to extract SBH from the off-state region measurements of this device. In the off-state region of operation (V_g > ~ –4 V in this device), source-to-drain conduction is limited by thermionic emission of charged carriers over large energy barriers at the metal/semiconductor interface. For this thermally activated process, a higher temperature results in more charge injection into the channel and larger current as evidenced in Figure 8(a).

The theory of thermionic emission for 2D semiconductors dictates that the current is given by $I = WA^*T^{3/2} \exp\left(-\frac{q\phi_B}{k_BT}\right)\left[1 - \exp\left(-\frac{qV_{ds}}{k_BT}\right)\right]$, where $A^* = q(8\pi k_B{}^3 m^*)^{1/2}/h^2$ is the Richardson constant, k_B is the Boltzmann constant, h is Planck's constant, and ϕ_B is the barrier height[43–45]. Considering the equation for thermionic emission, we can extract barrier height (ϕ_B) from the slope of Ln ($I/T^{3/2}$) as a function of 1/T as shown in Figure 4b for different values of V_g.

The extractions of barrier heigh for different V_g are plotted in Figure 8(c). As V_g is increased negatively towards the on-state, the height of the potential energy barrier drops down linearly. At flat-band, further change in V_g will not continue to reduce the barrier height. Instead, a deviation from the linear trend is observed in the extractions with increasing V_g, as the barrier becomes narrower and tunneling starts to contribute

significantly to the injection of carriers into the channel. The transition is labeled in Figure 8(c) at a flat-band voltage of approximately –3.7 V. At this voltage, the extracted barrier heigh corresponds to the Schottky barrier height (SBH), for which we obtain ~28 meV for Pt contacts, and ~25 meV for Pd contacts. The extractions of SBH are plotted in Figure 8(d) as a function of metal work function (WF). This plots includes our experimental results, as well as extractions of SBH from previous works on WSe_2 using different metal contacts[23,29,44-48]. A blue dotted line labeled with slope S = 1 illustrates the ideal case at the Schottky-Mott limit[49], where a change in WF translates directly to a chance in SBH. However, the collection of experimental results seem to reveal a weak dependence of SBH on WF (S ~ 0), indicative of severe Fermi-level pinning. While this could be a concern for contact resistivity, the SBH is still small (< 100 meV) in most cases, suggesting that other mechanisms could be responsible for the large contact resistivity typically observed in 2D PMOS FETs. In fact, our work shows that significantly different contact resistance can be achieved in devices with the same metal WF for which we extract similar low SBH (see Figure 8(a)). Indeed, the access resistance (i.e., the resistance of the semiconducting channel underneath the metal contact) can have a more dominant contribution towards the contact resistance if significant damage is introduced in this region during the metal deposition. Accordingly, we attribute the large improvements in contact resistance achieved in our WSe_2 PMOS FETs to reduced damage in the semiconducting channel access regions (underneath the metal contact) through adjustments in the deposition process (e.g., high-vacuum evaporation), and by implementing a stepped evaporation/deposition approach. As discussed in previous work, these changes can help minimize damage in the access regions resulting in overall improvements in contact resistivity and FET performance[11,23].

Figure 9(a) summarizes the results from this work and other recent efforts[21–23,30–33] aimed at lowering contact resistance in 2D WSe_2 PMOS FETs. This figure plots contact resistance as a function of carrier concentration in the semiconducting channel (carriers are holes for PMOS devices and their density increases as we push the device deeper into

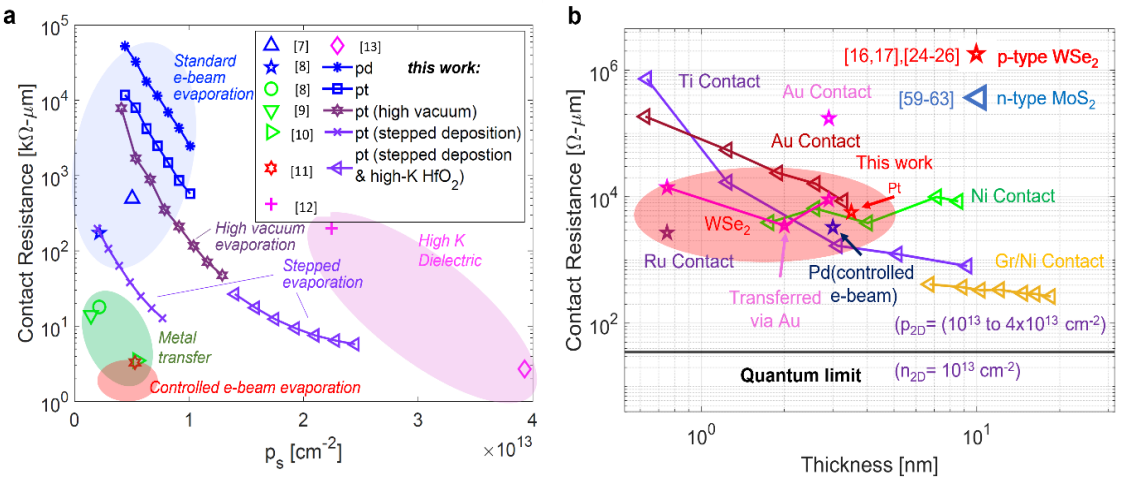

Figure 9. (a) Summary of trends on improvements of 2D PMOS FET contact resistance as function of sheet carrier density and the methods to achieve those improvements. Results from this work show advances in contact resistance from standard e-beam evaporation to high-vacuum and stepped evaporation on devices with scaled high-κ dielectric and metal gate (HKMG) stacks. (b) published data of Scaling of R_c with thickness of n-type MoS_2 and p-type WSe_2 [16,17,24-26,59-63]. R_c has been extracted for a electron carrier density of 10^{13} cm^{-2} for n-type MoS_2 and 10^{13} to $4x10^{13}$ cm^{-2} for p-type WSe_2.

strong inversion). As shown, standard methods used to deposit contacts, such as electron-beam (e-beam) evaporation, typically leads to large contact resistance (blue shaded region). However, significant improvements can be obtained by either metal transfer[31–33] or through a controlled e-beam evaporation[23] (green and red shaded regions respectively). Also, larger carrier concentrations can be achieved using high-κ dielectrics in the gate stack (improved gate capacitance), and this may also alleviate contact resistance[21,22] (pink shaded region). Our experimental results indicate a progression in contact resistance improvement starting from standard e-beam evaporation (pressure ~10-5 torr), followed by high vacuum evaporation (pressure ~10^{-6} torr), then higher vacuum (~10^{-7} torr) and stepped deposition. As previously discussed, a high vacuum metal deposition helps minimize damage to the underlying channel and improves resistance[11]. Moreover, a stepped evaporation can help

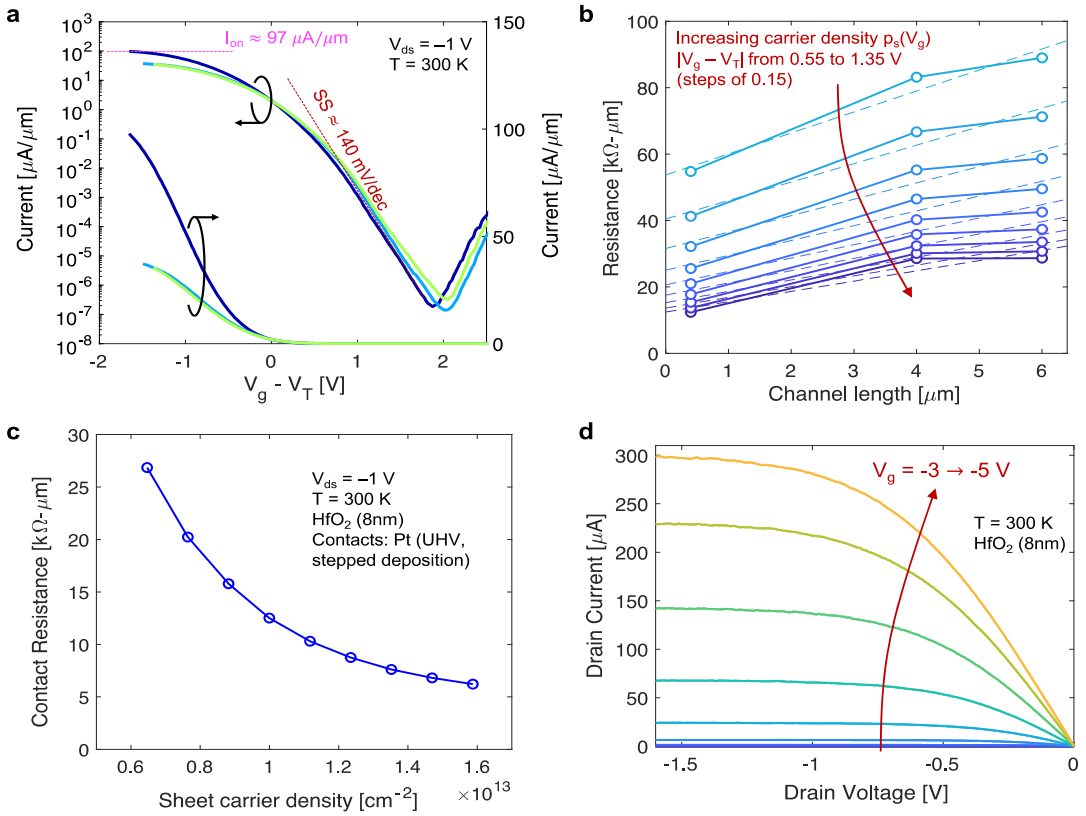

Figure 10. (a) Drain current (I_d) vs. gate voltage above threshold ($V_g - V_T$) for WSe_2 PMOS FETs with different channel lengths (400 nm, 4 μm, 6 μm) measured at room temperature with drain-to-source voltage of V_{ds} = –1 V. These devices show a subthreshold swing of ~ 140 mV/dec and on-state current normalized to channel width (W) of about 97 μA/μm (b) Total resistance vs. channel length for increasing sheet carrier density (as labelled, measurements correspond to $V_g - V_T$ ranging from –0.55 V to –1.35 V) (c) Contact resistance extracted from extrapolation to L = 0 as a function of channel sheet carrier density. (d) Drain current (I_d) vs. drain voltage (V_d) characteristics under different gate biasing conditions from subthreshold to strong inversion (V_g in steps of –0.25 V).

maintain the sample near room temperature also reducing damage. Finally, by switching from Al_2O_3 to HfO_2 (high- κ of ~17) we achieve further improvements. These are further explained in the electrical characterization and discussion section of this report. Figure 9(b) summarizes the results from this work and previous published data to figure out a trend for contact resistance as a function of channel material thickness. For n-type MoS_2 it is noticed that with increasing number of layer thickness contact resistance tend to decrease. However

for p-type WSe_2 a clear trend has not yet been observed. More data points need to be taken to come to a clear conclusion how layer thickness affects the contact resistance.

2.4 Electrical Characterization

Electrical measurements of the 2D PMOS devices is used to extract key performance parameters such as on-state current per micrometer of channel width (W), the inverse subthreshold slope (i.e., the subthreshold swing), the contact resistance, and the channel mobility. Typical drain current (I_d) versus gate voltage (V_g) characteristics measured at room temperature (T = 300 K) for three different channel lengths (L = 400 nm, 4000 nm, and 6000 nm) are shown in Figure 10(a). The I_d-V_g characteristics are measured with a drain-to-source voltage of V_{ds} = –1 V and are plotted in both linear and logarithmic scale for the current axis (y-axis). Minimal to negligible gate leakage was observed for all devices. These measurements are from devices with 8 nm HfO_2 gate dielectric and with Pt/Au (10 nm/25 nm) source and drain contacts deposited under high vacuum (10^{-7} torr) using a stepped evaporation approach. This high vacuum and stepped evaporation approach resulted in the best performing devices. As labeled in Figure 10a, for a device with L = 400 nm we obtain on-state current $I_{on} \approx 97$ μA/μm (normalized to W), and subthreshold swing SS ≈ 140 mV/dec. These values are indicative of high-performance 2D FETs and are further analyzed in context of recent published results in the "I_{on} vs SS benchmarking" section below.

As mentioned earlier, contacts play a significant role in the performance of these 2D SB-FETs and necessitates further investigation. Using the transfer length method (TLM) we analyze measurements of resistance (obtained from normalized I_{on}) as a function of L to extract contact resistance and hole mobility respectively from the vertical intercept (i.e., extrapolation to L = 0) and from the slope[38,39]. Figure 10b plots resistance (in units of kΩ-μm) as a function of channel length for various levels of channel sheet carrier density given by $p_s = (1/q)\, C_{ox}(|V_g - V_T|)$, where C_{ox} is the oxide capacitance per unit area and V_T is the threshold voltage. Thus, a larger p_s corresponds to a larger gate bias above threshold and results in lower contact resistance (vertical intercept). Here, V_T was extracted at a fixed I_d = 10 μA. Similar results in the analysis of resistance are obtained using V_T extracted from

the extrapolation of a linear fit to the I_d-V_g data at the peak transconductance (g_m). Figure 10c plots the contact resistance as a function of sheet carrier density reaching a value as low as ~6 kΩ-µm. This is comparable to the recently reported record PMOS contact resistance of 2.7 kΩ-µm, and to other recently reported value of 3.3 kΩ-µm but at smaller sheet carrier densities[22,23] (both of these previous results, along with our own results shown in Figure 3(b). As described below, a similar contact resistance at a smaller sheet carrier density may be indicative of better-quality interface between metal contact and semiconducting channel. For our own devices, which combine the methods of these previous efforts (i.e., a low pressure stepped evaporation and a HKMG stack), we expect further reduction in contact resistance with reduced base pressure during metal evaporation (currently limited to ~10^{-7} torr with our existing tools). Nonetheless, these WSe_2 PMOS FETs already show outstanding performance with superior off-state performance (as indicated by SS) and cutting-edge on-current levels (as indicated by I_{on}) compared to previous work. Sheet resistance and hole mobility both have been extracted as a function of sheet carrier density and plotted. Which corresponds to V_g over threshold (Figure 10). We note that hole mobilities extracted from the slope of the resistance vs. channel length in ranges from approximately 125 up to ~150 cm^2/V-s.

Further discussion of device performance and benchmarking of I_{on} vs SS is provided below. For completion, Figure 12(a) plots I_d as a function of V_d at different gate biasing conditions ranging from the off-state ($V_g < V_T$) to on-state ($V_g > V_T$). The I_d-V_d family of curves in Figure 10(d) are from room temperature measurements on 2D WSe_2 PMOS FETs with 8 nm HfO_2 gate dielectric and a channel length L = 400 nm. The gate voltage was changed from –3 V to –5 V in steps of –0.25 volts.

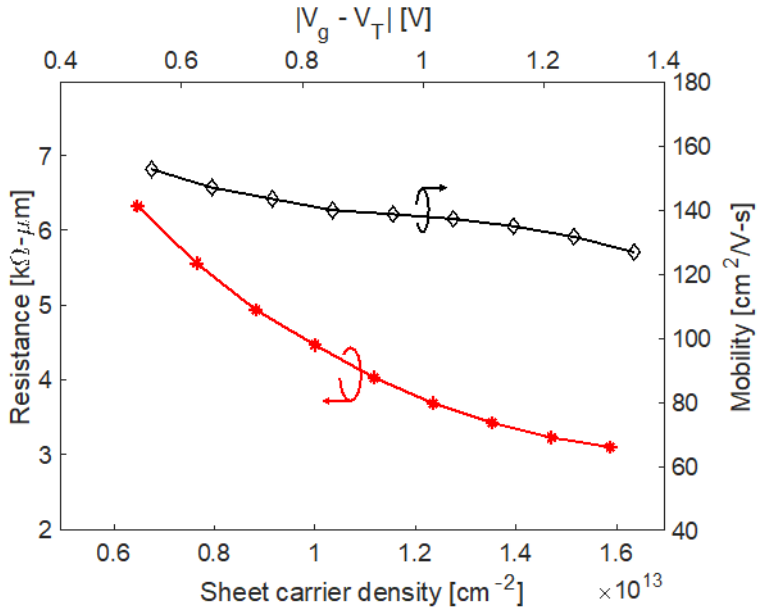

Figure 11. Sheet resistance and field effect mobility has been extracted as a function of sheet carrier density. Sheet resistance and field effect mobility have both been extracted using the slope of resistance normalized by width for various channel lengths.

2.5 I_{on} vs SS Benchmarking

With the use of HKMG stacks, high-vacuum evaporation, and stepped metal contact deposition, we have shown the electrical properties of high-performance WSe_2 PMOS FETs and showed considerable improvements in contact resistivity. Here we show benchmarking of on-state current (I_{on}) versus subthreshold swing (SS) against previous work to indicate superior FET performance. Figure 12(a) compares our experimental results for devices prepared using low base pressure evaporation and stepped deposition of the metal contacts (to achieve low contact resistivity of ~6 kΩ-µm, comparable to previous efforts) against previous reports[22,23,50,51].

For comparison, the effective oxide thickness (EOT), calculated as $t_{ox}*(K_{SiO2}/K_{ox})$, is labeled for each data point. Here, t_{ox} and K_{ox} are the thickness and dielectric constant of the gate oxide, and K_{SiO2} is the dielectric constant of SiO_2. Our results are for devices with 8 nm Al_2O_3 as well as 8 nm HfO_2 gate dielectrics (I_{on} extracted at sheet carrier densities of ~7×10^{12} and ~3.5×10^{13} cm^{-2} respectively) with few layer (~3 layers) of WSe_2. Compared

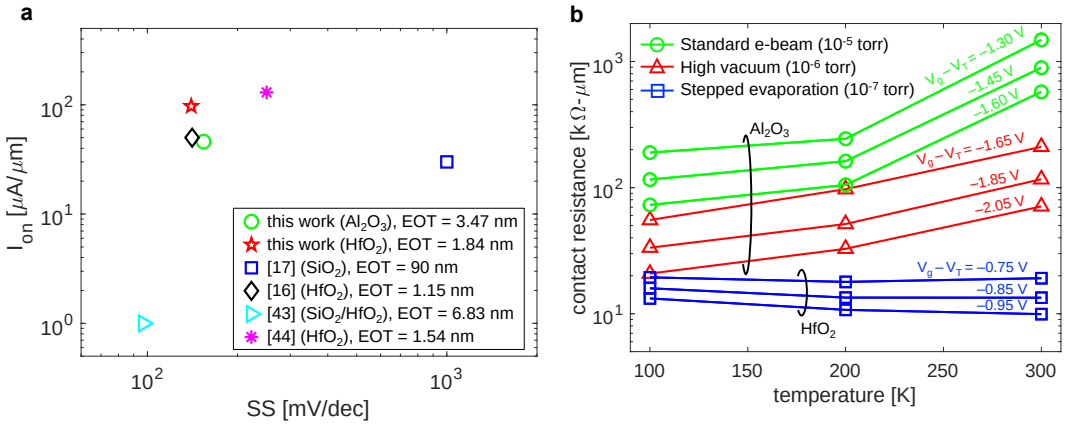

Figure 12. (a) 2D PMOS FET performance benchmark of on-state current (I_{on}) versus subthreshold swing (SS). This plot includes our results from WSe_2 devices prepared with high-vacuum evaporation and stepped metal contact deposition (low contact resistivity of ~ 5 kΩ-μm) with two different high-κ dielectrics (Al_2O_3 and HfO_2). Also shown are previous results with record contact resistivities. Our devices show improvements indicated by higher I_{on} while maintaining low SS (see text). (b) Contact Resistance as a function of temperature from three devices prepared with different metal evaporation techniques. For each case three curves are shown corresponding to three different V_g (i.e., different sheet carrier density). Moving from standard e-beam evaporation (10^{-5} torr), to mid-level vacuum (10^{-6} torr), and higher vacuum (10^{-7} torr) plus stepped evaporation we see a reduction in contact resistance and a transition in the temperature dependence (see text).

to previous reports, we show improvements in performance as determined by a large I_{on} while simultaneously a small SS. We note, however, that our data is on devices with few layers (~3 layers) of WSe_2 compared to other efforts which are devices with WSe_2 monolayer channels. Nonetheless, our results indicate that significant improvements in contact resistivity combined with scaled HKMG architectures can result in desirable improvements in 2D PMOS FETs towards ultimate scaling of CMOS technology.

As already established, contacts play a crucial role in the performance and operation of 2D FETs, and the Schottky junctions at the metal connections with the channel are a key part of this role. However, our results show that even under significant Fermi-level pinning (i.e., poor control of Schottky barrier height with metal work function), the SBH for hole injection into WSe_2 channels is typically small (<100 meV). Furthermore, contact resistance appears to be more strongly dependent on the methods used to evaporate and deposit the metal contacts, and less by the workfunction of the metal and the SBH. Thus, we determine that resistance of the channel access region (i.e., the WSe_2 region underneath

the metal contact) can contribute significantly to contact resistance[11,52]. By using methods to fabricate metal contacts that minimize the damage to the access region we reduce the overall contact resistivity and improve performance. As further evidence we explore the temperature dependence of contact resistance for devices fabricated using different methods (i.e., standard e-beam evaporation, evaporation at lower pressure, and further reduction in pressure plus stepped deposition). Figure 12(b) plots contact resistance as a function of temperature for all three devices at different levels of sheet carrier density (i.e., different V_g, with larger V_g resulting in larger sheet carrier density and smaller contact resistance). The results show a clear transition from contact resistance *increasing* with temperature (i.e., dominated by scattering in the access region) for devices fabricated using standard e-beam evaporation at 10^{-5} torr, to contact resistance *decreasing* with temperature (i.e., dominated by thermionic emission in the Schottky barriers) for devices fabricated using a stepped evaporation at lower pressures of 10^{-7} torr[9]. By using a high vacuum and stepped evaporation, less damage is introduced during fabrication of the contacts leading to reduced scattering in the access region. Moreover, a high-κ gate dielectric (~17 for HfO_2) under the access region may enhance carrier density also reducing the access resistance. Altogether, this helps to significantly improve (reduce) the contact resistance to where we start to see a transition in the temperature dependence (dominance of Schottky barriers or interface resistance). This interface vs access resistance effects were previously observed in MoS_2 n-channel FETs.

CHAPTER 3

Landauer Based Modeling

3.1 Modeling Calculation and Fitting

Finally, we use a ballistic transport model based on the Landauer formalism to clarify the performance boundaries of extremely scaled 2D PMOS FETs. [53–55]. Here, the drain-to-source current for is given by

$$I = \frac{2q}{h}\int_{-\infty}^{\infty} T(E)M(E)[f(E,E_{Fs}) - f(E,E_{Fd})]dE,$$

where f is the Fermi function, $M(E)$ is the density of modes (e.g., $M(E) = (g_v/h)[2m_h^*(E_V - E)]^{1/2}$ in the valence band, where g_v is the valley degeneracy and m_h^* is the hole effective mass). The transmission coefficient $T(E)$ is obtained based on the series combination of scatterers and is given by[24]

$$T = \left[1 + \left(\frac{1 - T_S}{T_S}\right) + \left(\frac{1 - T_D}{T_D}\right) + \left(\frac{1 - T_C}{T_C}\right)\right]^{-1}$$

For energies between the edge of the conduction band and the peak of the barrier for holes or electrons, T_S and T_D are calculated using the WKB approximation for tunneling probabilities across a triangular shaped barrier (Figure 13.a) as[24,27]

$$T_{WKB} = exp\left\{-\frac{2\pi}{h}\int_0^{x_0}\sqrt{2m_h^*[E - E_V(x)]}dx\right\},$$

and T_C (i.e., transmission through the channel) is set equal to 1 for ballistic transport.), but T(E) account for thermionic emission and tunneling through the Schottky barriers at the contacts. The Fermi level at the source/drain is respectively given by $E_{Fs} = qV_C + qV_{ds}/2$

and $E_{Fd} = qV_C - qV_{ds}/2$. The relationship between the potential in the channel (V_C) and V_{gs} is determined by capacitive coupling of the gate to the channel[4–6] and is calculated as

$$V_C = (V_g - V_0)\frac{C_{ox}}{C_{ox} + C_q(V_C)}$$

where C_q is the quantum capacitance of the channel given by

$$C_q(V_C) = \frac{q^2}{4k_BT_L}\int_{-\infty}^{+\infty} D(E)sech^2\left(\frac{E - V_C}{2k_BT_L}\right)dE$$

and $D(E)$ is the density of states in the channel (containing both conduction and valence bands)[57].

$$V_0(V_C) = \Phi_{MS} - \frac{q}{C_{ox}}\left\{\int_{-\infty}^{+\infty} D_{it,a}(E)f(E,qV_C)dE - \int_{-\infty}^{+\infty} D_{it,d}(E)[1 - f(E,qV_C)]dE\right\}$$

where $D_{it,a}(E)$ and $D_{it,d}(E)$ are the acceptor and donor-like interface trap densities respectively. The transcendental equation for V_C must be solved numerically to obtain a self-consistent solution. Figure 14 shows an example of the channel potential calculated as a function of the gate voltage for different densities of interface traps.

Here, V_0 accounts for the work-function difference between the gate and the channel (Φ_{MS}) and contains the charge contribution from interface traps. Interface traps can be acceptor-like or donor-like and trap occupancy is calculated using Fermi functions[63-65]. The parameter V_0 allows accounting for a metal-semiconductor work function difference and for the effects of surface states (interface traps)[26,27,60,61]. Figure 13(b) plots the current contribution from holes (green dotted line) in the valence band, electrons (red dashed line)

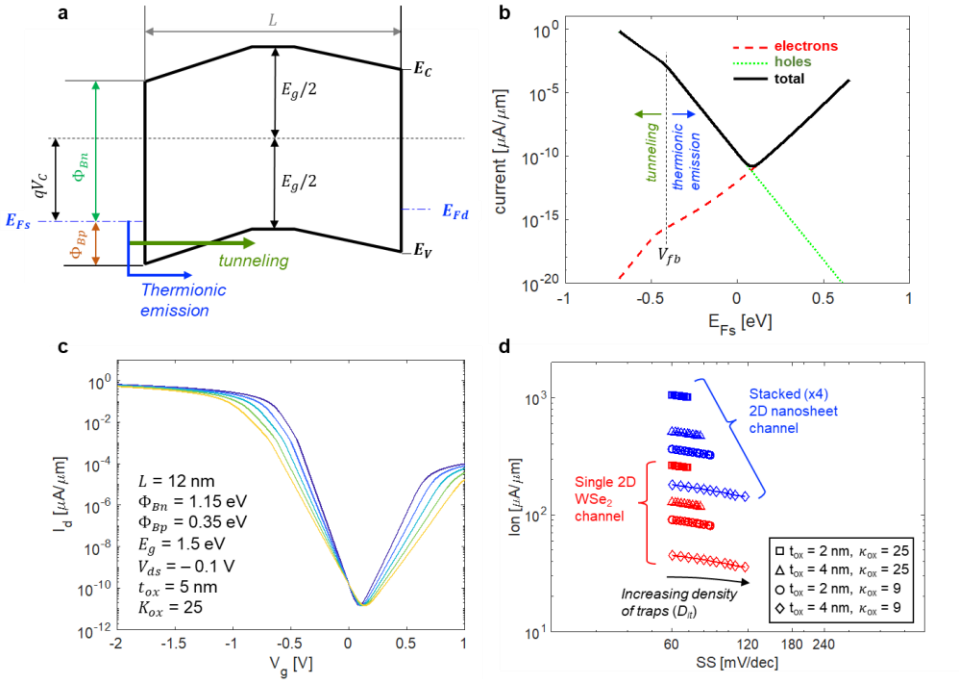

Figure 13. (a) Energy-band diagram for short-channel 2D WSe_2 PMOS FET with definitions of relevant energy levels and potentials used in calculation of ballistic FET I-V characteristics (see text). (b) Calculations of electron, hole, and total FET drain-to-source current as a function of the channel potential (i.e., relative position of the Fermi-level in the source to the semiconductor bands). Note that the zero energy reference is exactly at the middle of the bandgap. (c) Calculation of ballistic drain-to-source current as a function of V_g for various levels of interface trap density (model parameters labelled in this plot). (d) Model predictions of Ion vs SS in ballistic devices with different gate dielectrics (thickness and dielectric constant) as well as different levels of interface trap density. All values are for V_g = – 2 V (sheet carrier density vary from ~ 10^{12} to ~7×10^{12} cm^{-2}). Results in red are for single 2D WSe_2 channel, results in blue are for stacked 2D nanosheet channels.

in the conduction band, as well as the total current (solid black line) as a function of the channel potential. The labels in the plot show where the I-V characteristics transition from purely thermionic emission to where tunneling starts to contribute (this happens when bands go flat at the metal/semiconductor junctions).

Figure 13(c) plots the drain current vs gate voltage (I_d-V_g) characteristics at room temperature for interface traps densities (D_{it}) of 0, 4×10^{12}, 8×10^{12}, 1.2×10^{13}, and 1.6×10^{13} $cm^{-2}eV^{-1}$. We note that these are typical trap densities for FETs with 2D channel

materials[29]. Model parameters for these calculations are shown in Figure 13(c). As shown, interface traps can impact on-state current as well as subthreshold swing. The calculations in Figure 13(b) serve only as an example of the modeling approach and the model parameters were not adjusted to fit any particular device. Instead, we now apply the Landauer-based model to simulate ballistic WSe_2 SB-FETs (SBH adjusted to fit extractions from WSe_2 FETs with Pt contacts) and estimate performance benchmarks of I_{on} vs SS in nanoscale devices with ballistic transport. We show calculations for devices with ultrascaled gate dielectrics with different EOT, as well as for different levels of interface trap density. Figure 13(d) plots the calculations of I_{on} vs SS in single channel 2D WSe_2 FETs (red lines with symbols), as well as for stacked 2D nanosheet FETs (blue). All values are for $V_g = -2$ V (sheet carrier densities vary from ~10^{12} to ~7×10^{12} cm^{-2}). The model calculations indicate that large I_{on} (~270 µA/µm) values can be achieve together with ideal SS values (~ 60 mV/dec) in single-channel device with 2 nm HfO_2 gate dielectrics at moderate sheet carrier densities of ~7×10^{12} cm^{-2} (larger I_{on} can be achieved at higher sheet carrier densities by further scaling of t_{ox}, or at larger V_g). Moreover, by stacking 2D nanosheets a multiplicative effect on current will result in significant enhancement in performance.

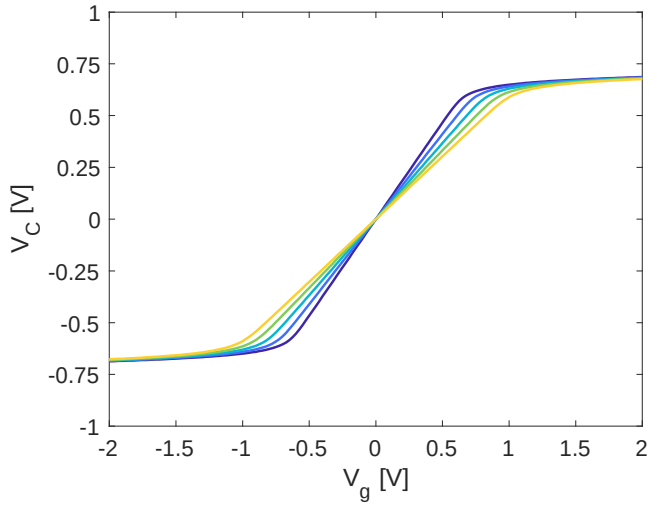

Figure 14. Calculation of channel potential as a function of gate voltage for various levels of interface trap density (model parameters same as those in main text Figure 6c). The calculations include both acceptor-like and donor-like traps with densities ranging from 10^{12} up to 10^{13} $cm^{-2}eV^{-1}$

This work provides significant insights on emerging methods to enhance contact quality and improve performance of FETs with 2D channel materials. This is presented in context of recent efforts that have emerged to elucidate the issues encountered with 2D PMOS devices. Comprehensive analysis is given for characterizing contact resistance, and to identify the key components that contribute to contact resistance in 2D PMOS FETs. Devices prepared using these improved methods, such as high-vacuum evaporation and stepped deposition of metal contacts to reduce damage to channel access regions, as well as using scaled HKMG stacks, resulted in noticeable improvements on benchmarks of I_{on} vs SS. Moreover, we present a physics-based model estimates for nanoscale ballistic WSe_2 devices to elucidate the performance of extremely scaled 2D PMOS FETs towards the ultimate CMOS scaling limits.

Chapter 4

EOT Scaling and Double Gate Tunning of the channel

The hunt for new materials and creative device architectures has become essential in the never-ending quest for smaller, quicker, and more energy-efficient electronic technologies. The use of double-gate design MOSFETs is one research direction that has attracted a lot of interest for improving the gate control of the channel in ultrascaled devices. Having a second gate modifies the electrostatics and can help improve the overall characteristics of the device. Double-gated MOSFETs have also enabled formerly unachievable features[66]. In my work, I explore the performance of MoS_2 double-gated FETs compared to single-gated FETs, and I especially address the electrostatic properties and gate-stability of this new device architecture. By studying the properties of double-gate designs, compared to single-gate devices, this work highlights potential improvements towards the significant advances in 2D FET technologies. Not only is the path toward innovative device architectures using large-area CVD-grown monolayer MoS_2 FETs intriguing, but it will play a crucial role in determining how the electronics industry develops in the future.

In addition to presenting electrical characterization of wafer-scale double-gated CVD-grown monolayer MoS_2 FETs, I have studied the scaling of Equivalent EOT to approach 1 nm resulting in additional improvements in device. Here, EOT scaling, device architecture, and interface quality all play a delicate interplay that is essential to the success of 2D-material-based FETs. EOT scaling is a key tactic that not only addresses the unrelenting need for shrinking but also has a profound impact on device performance. An

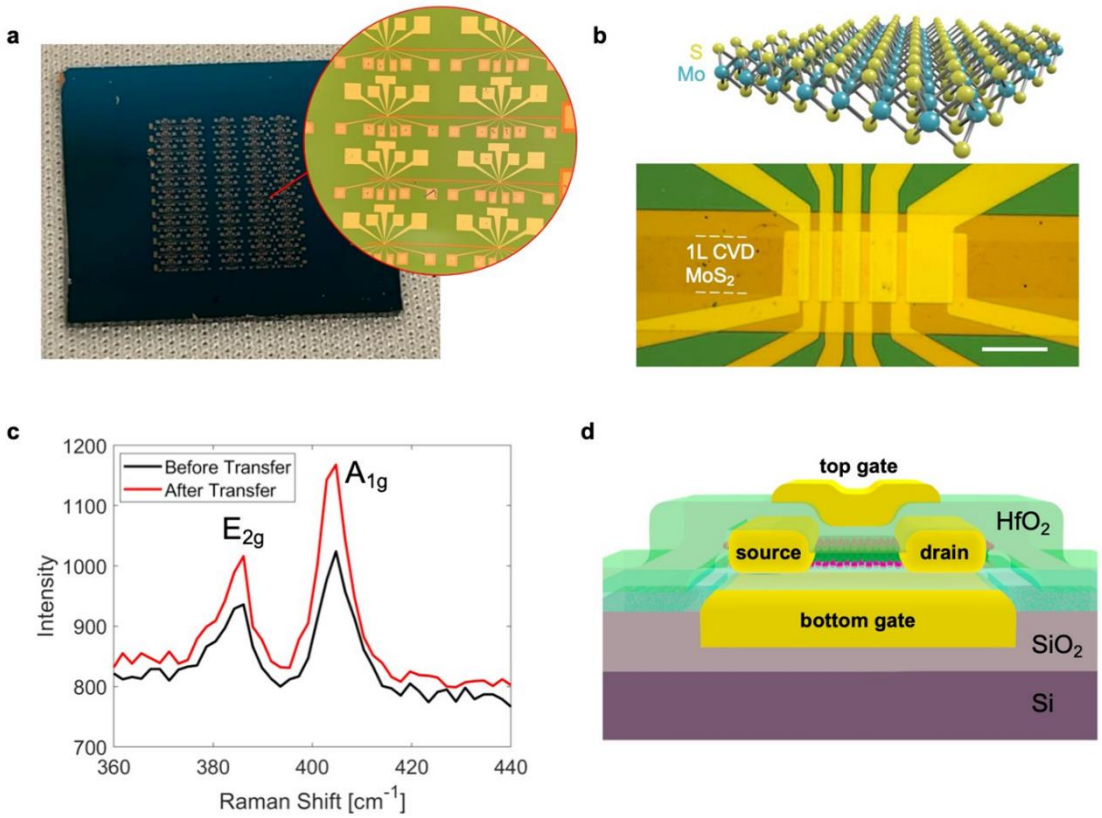

Figure 15. (a) 1 by 1 cm Si/SiO_2 wafer with 60 as fabricated double gated monolayer MoS_2 Field Effect Transistor devices. (b) Optical image focused on 1 device with 5 channel length ranging from 360 nm to 7000 nm. Bottom gates are extended below the entire channel region whereas Top gates have the same length of overlapping with source and drain region. Channel length has been defined as the distance between the source and drain. (c). Raman spectra of CVD grown MoS_2 showing the quality of the film consistency after wet transfer process. (d) a 3D schematic showing our device structure to control the channel using top and bottom gate at the same time.

essential feature of FET operation, the electrostatic control over the channel, is directly impacted by EOT, which also determines the scalability of the channel length. Thus, in this work I investigate the effects of EOT scaling in the framework of MoS_2 FETs performance, focusing on electrostatics-related parameters such as subthreshold swing, as well as other gate-stack scalability/stability parameters including gate hysteresis, gate leakage, and how

these are impacted by EOT scaling. The benefits of a lower EOT go much beyond simple miniaturization; they have the capacity to completely alter the parameters of speed, power efficiency, and device dependability. I will elucidate the complex relationship between EOT scaling and MoS_2 FET performance throughout the next section. Through analyzing the subtleties of this correlation, I hope to draw attention to the novel advancements that scaling EOT can bring about in the development of 2D material-based devices with improved performance.

4.1 Double-Gate Device fabrication

The bottom gate electrode is isolated from the 2D channel material (in this case 1L CVD-grown MoS_2) with a thin insulating layer of high-κ dielectric. This back-gate acts as a regular gate which helps regulate the flow of current across the semiconductor channel between the source and drain terminals. In both top- and bottom-gate stacks, the high-κ dielectric layers play a very important role towards EOT scaling sub-1 nm. To maintain good control over the channel at lower voltage levels, which is critical to cut power consumption and boost device performance, the scaling of EOT is crucial. This section of my dissertation describes the fabrication and characterization of double-gated MoS_2 (1L CVD-grown) FETs, and extensive analysis on EOT scaling and the improvements it offers towards the ultimate CMOS scaling.

CVD-grown monolayer MoS_2 materials have been transferred onto a 1 cm by 1 cm Si/SiO_2 substrate via wet etching of Cu substrate. Monolayer MoS_2 was purchased from 6 carbon 2D Material technology. These were CVD grown on top of Copper (Cu) film. The CVD film was spin coated with PMMA at 3000 rpm and baked for a min before it has been

dipped into Cu etchant solution. The floating PMMA film with material has been fished out from the Cu etchant solution to Di water for a rinse. Followed by the film is fished out again and merged into 2% HCL solution to have all the Cu etchant residue remove. The film was then fished out and rinsed in 3 steps of DI water to remove HCL and flatten out the surfaces. The film was then blown with N_2 air gun for 5 min thoroughly to remove any remaining water vapor, and finally was transferred onto the targeted substrate that was already pre-patterned with bottom gate electrode with high-κ-dielectric on top. Right after the transfer process, photolithography has been done on the sample to have the source and drain patterned with varying channel length (360nm, 850 nm, 1600 nm, 3200 nm, 7000 nm).

In previous study (section 2.2), it was mentioned that ALD deposition on top of 2D channel materials presents difficulties that can impact device electrical performance. This is due to non-uniform deposition, confirmed with atomic-force-microscopy (AFM), potentially resulting in high gate leakage. As a solution to this problem, instead of direct ALD deposition, a seeding layer has been deposited to improve subsequent ALD film adhesion and uniformity. The seeding layer encourages consistent, well-defined growth, guaranteeing a high-quality channel/dielectric interface with few flaws and variances. A good interface between the channel and the dielectric can be ensured by selecting seeding layers that are compatible with the gate dielectric material. Here, the seeding layer ensures that the dielectric ALD deposition happens uniformly over the semiconductor surface. Without it, the dielectric could grow unevenly, changing the properties of the device and

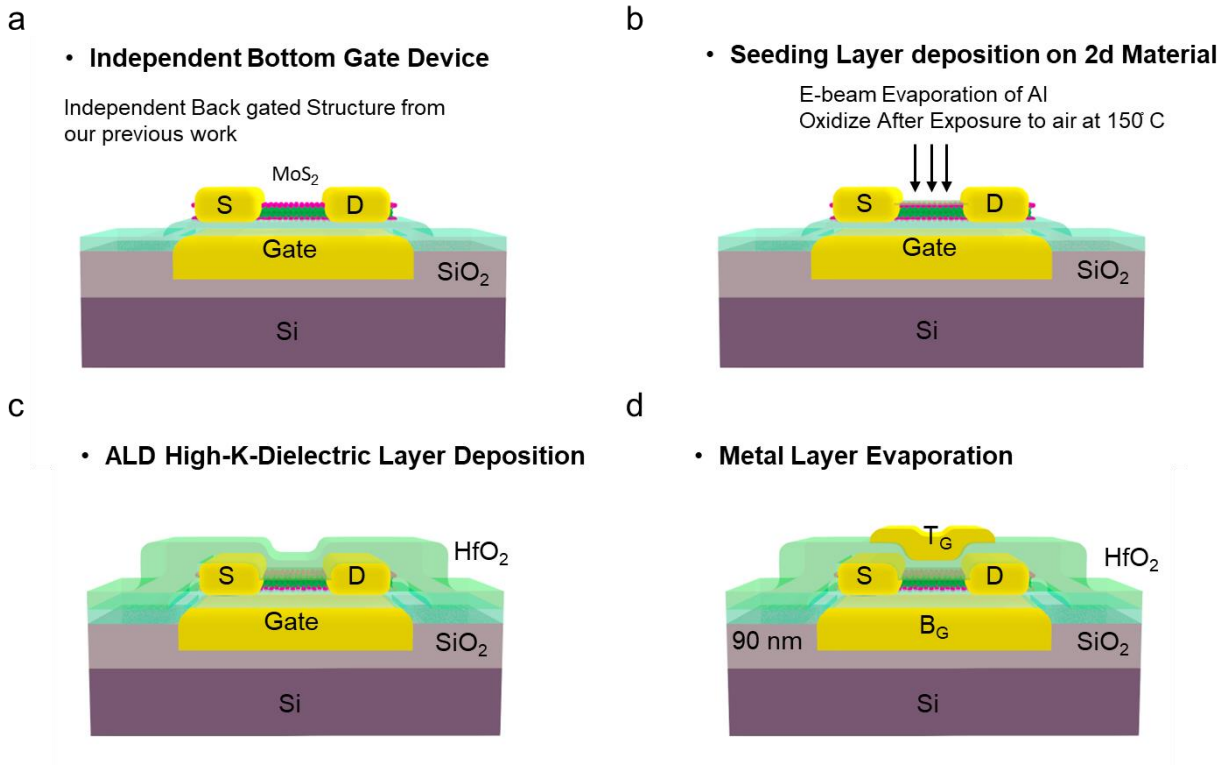

Figure 16. (a) Obtained independent back gate FET structure with MoS_2 as channel material. (b) A seeding layer of 1 nm Al_2O_3 has been deposited with E-beam evaporation and oxidized at presence of air at 150º C. (c) ALD growth of high-κ-dielectric (3 nm, 5 nm, 10 nm). (d) Final Schematic of the double gated structure of the 2D FET showing gate stack on both side of the channel material.

having large gate leakage through gate stack. It also promoted adhesion between the channel material and the high-κ-dielectric layer. In this work, I have used 1 nm Al_2O_3 as a seeding layer (Figure 16(b)). Al_2O_3 is compatible with a wide range of gate dielectric materials (HfO_2, Al_2O_3 ALD layer) used in our FET fabrication. Achieving a high-quality channel with few flaws and variances requires this homogeneity. Here, 1 nm Al was deposited with e-beam evaporation at a rate of 0.1 A/s and was treated thermally to convert into Al_2O_3. Then, ALD deposition of HfO_2 (3 nm, 5 nm, or 10 nm) was done at 180º C to achieve conformal deposition. Finally, the top gate was patterned, and metal was deposited

with e-beam evaporation chamber. The bottom gate and source-drain pad regions were under the high-κ-dielectric gate stack. To open those pads, I had to do a 3-step dry etching process to etch HfO_2, Al_2O_3 and HfO_2 respectively. Opening these pads ensures my electrical measurements to be accurate and does not have any additional resistivity issues.

4.2 Double-Gate MoS_2 FET Characteristics

This section analyses the electrical characteristics of double-gated MoS_2 FETs compared to single top-gated counterparts. Having a double-gate structure can help enhance control over the channel region, as it allows to independently adjust the electrical

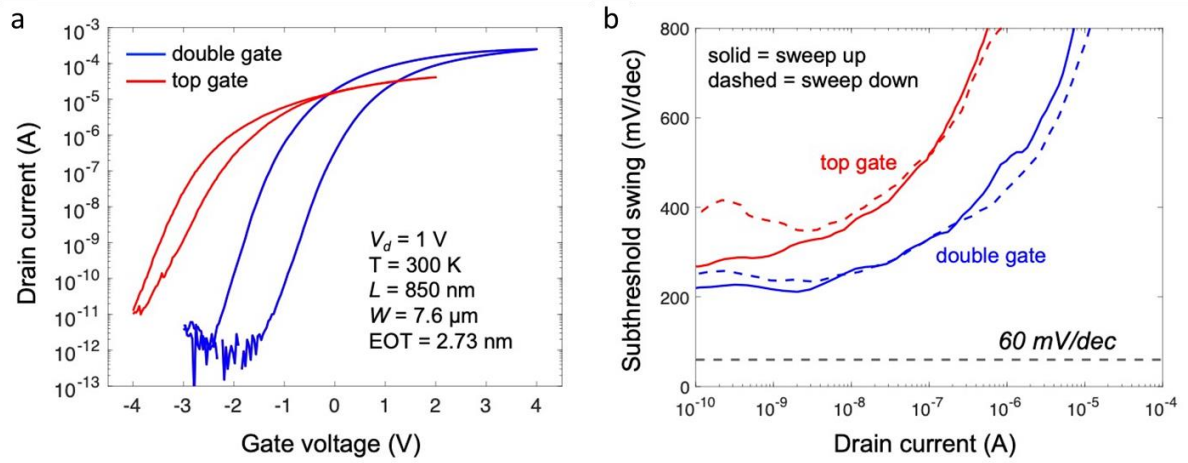

Figure 17**.** (a) Drain current as a function of gate voltage for Top gated and double gated device has been shown. A clear on-off ratio and on state current increase has been observed with a double gate. (b) Subthreshold swing for gate voltage going up and down both shows reduced number for double gate devices.

characteristics[66]. The separate gates can be biased independently to adjust threshold voltage, which is an added functionality that may be crucial for applications requiring accurate voltage control such as in analog and mixed signal systems. Alternatively, they can be biased in common mode (both at same voltage) to achieve superior electrostatic

control. To verify theoretical claims on double-gated device performance this work conducted systematic experimental characterization to extract key performance parameters such as contact resistance, field effect mobility, sheet resistance and Schottky barrier height. Figure 15(a) shows the 2 cm x 2 cm Si wafer on which the CVD grown MoS_2 has been transferred. Each of the chips contains a total of 60 structures, 48 of which have a double gated FET structure and 12 of which have a top gate FET structure. The idea was to have different sets of structure to compare characteristics of both types of devices and at the same time check consistency of the performances across the multiple devices. Each structure has five different channel lengths to allow analysis of contact resistance and sheet resistance through the TLM method. Width of all the devices were 7.6 µm throughout all the device structures.

Figure 17(a) illustrates a log linear plot of drain current as a function of gate voltage for the device with equivalent oxide thickness of 2.73 nm. Equivalent oxide thickness was calculated as $t_{ox}*(K_{SiO2}/K_{ox})$, is labeled for each data point (explained in detail in section 2). 10 nm, 5 nm & 3 nm HfO_2 corresponds to an EOT of 2.73 nm, 1. 57 nm and 1.08 nm. The blue plotted line represents I_d-V_g for a double gated device, while the red plotted line represents drain current for the top-gated device. The obtained on-off ratio for a top gated device is roughly 10^6, and the on-off ratio obtained as high as 10^8 with a high on current per micron for a double gated device. It can be seen that on-current of 30 µA/µm for double gated structure while we see an on current of 6 µA/µm for top gated structures. With two gate electrodes, double-gate FETs enable more exact channel control. More efficiently modify the conductance of the channel by varying the voltages on both gates

independently. As a result, the device's properties are adjusted, and performance is enhanced. We can modify the threshold voltage to the appropriate level by putting two voltages on each gate. While turning the device on, we can create a higher electric field across the channel; while turning it off, we can create a smaller electric field since we can independently control the channel. By enabling a smoother transition between the on and off states, it can improve subthreshold swing and lessen abrupt switching. The extracted subthreshold swing as a function of drain current for biasing positive and negative direction have been illustrated in Figure 17 (b). We retrieved SS by taking drain current at various levels and obtaining various slopes for each current. Additionally, it significantly outperforms the top gate for double gates. With precise gate modulation on both sides, it was possible to adjust the threshold voltage on the back gate and improve the switching on characteristics of the double gate device. The potential energy landscape in the channel region may be precisely controlled owing to the double-gate construction. The potential energy barrier for carriers can be adjusted by properly designing the gates. Hence, subthreshold swing is significantly reduced. Double gate modulation has produced larger hysteresis. It would be caused by the two gate capacitances on either side. Leaving more oxide traps on both sides contributes to hysteresis.

Drain current as a function of gate voltage has been illustrated in Figure 18 (a) to verify if the channel length dependence of carrier injection into the channel has been following the trend (current decreases with larger channel length for same width or normalized width). My devices do show consistency with all different channel lengths for almost all of the structures in the wafer. Figure 18 (b) illustrates the extraction of total

resistance for four different channel lengths for normalized width of each channel. It shows a nice clear trend with channel length. We extracted contact resistance from the Y axis intersect and sheet resistance and mobility from the slopes of the different carrier density. The detailed equations and extraction parameters have been discussed in the previous section (Improvement in p-type WSe_2 device performance metrics). The low intrinsic field effect mobility for the top gated device was found to be 3 $cm^2V^{-1}s^{-1}$. Mobility was extracted from the slope of the TLM resistance as a function of channel length. A lower mobility is always observed in CVD grown MoS_2 channels, hence the area of tiny grains near the source drain contact that causes an increase in contact resistance cannot be the cause of the reduced mobility. In comparison to the top gate state, the contact resistance was globally lowered by a factor of one, suggesting enhanced charge transfer for all bias values. Increases in the double-gate dielectric's unit-area capacitance or double-gate voltage may be used to accomplish further reductions. Because of the additional staggered top gate, MoS_2 FETs have great contact resistance tunability, which is related to more efficient modulation of charge injection. Thus, it is possible to further enhance FET performance by lowering contact resistance through the use of double-gate architecture. Contact resistance also decreased because of improved alignment between the operating parameters of the

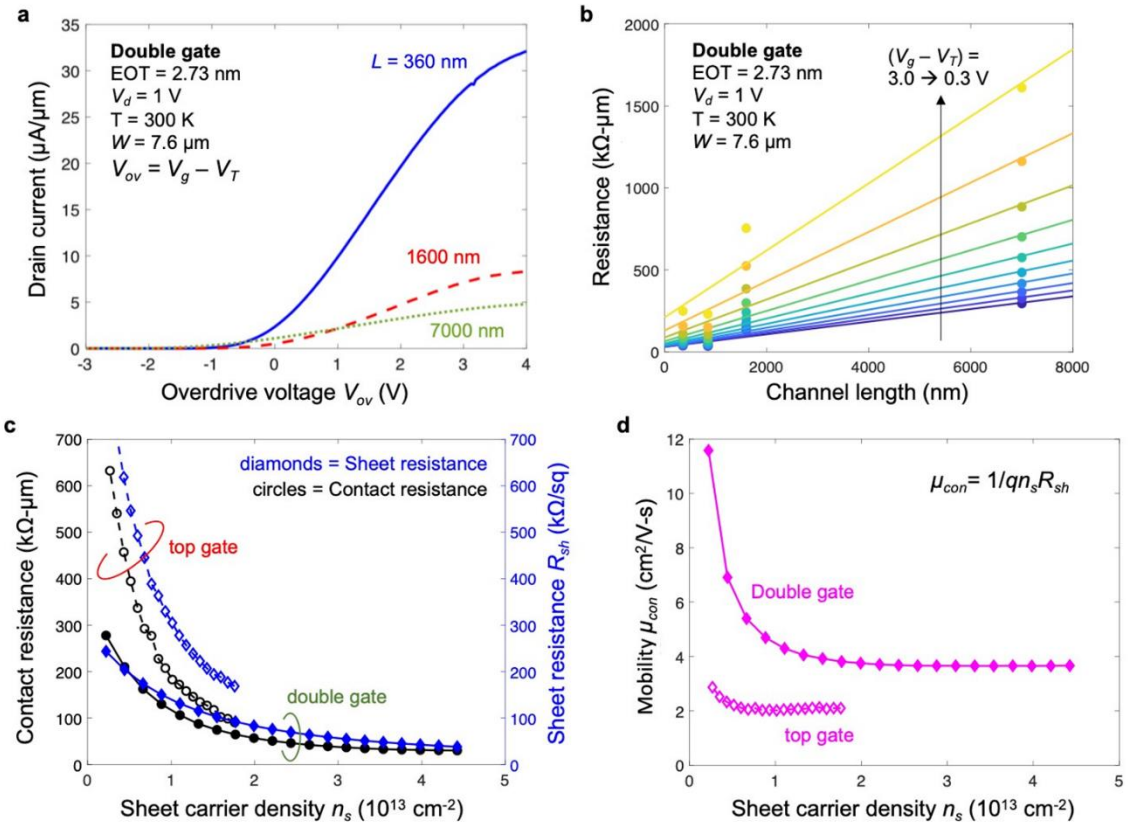

Figure 18**.** (a) Drain to source current as a function of Gate overdrive voltage (V_G-V_{TH}) for three channel lengths (360 nm, 1600 nm, 7000 nm) has been illustrated. (b) Total resistance as a function of four different channel lengths has been plotted. The slope of these data normalized by width tends to extract field effect mobility and sheet resistance and the y axis intersects corresponds to contact resistance. (c) Contact resistance and sheet resistance as a function of sheet carrier density, (d) conductance mobility as a function of sheet carrier density has been presented

device and the voltage levels in the contacts made possible by this change. To improve carrier injection and conduction in the channel and to lower contact resistance, it is possible to independently modulate the channel behavior and the gate to channel barrier. Hence, Figure 18 (c) illustrates that I obtained much lower contact resistance for double gated device compared to the top gated device and was able to tune into higher sheet carrier density values by tunning both top and bottom gates and as a result able to achieve lower

contact resistance and sheet resistance values. By applying bias to both the gate voltage and the channel, we can precisely define the channel and create a stronger electric field, which improves charge carrier mobility. Hence, the carriers experience less scattering and interference from impurities or defects[72]. Figure 18 (d) further shows our claim and shows mobility enhancement with double gated structures. We obtain a mobility of 12 $cm^2V^{-1}s^{-1}$ and 3.5 $cm^2V^{-1}s^{-1}$ for monolayer CVD grown MoS_2 double gated and top gated FET respectively. I_d-V_g characteristics for top gated devices show a reduction in drain current which can be attributed to the decreased carrier mobilities. It is very evident that double-gate FETs inherently provide more options for optimizing device characteristics. Even with the same material and fabrication techniques, the additional gate on top enables more precise control over the channel region and can lead to better mobility.

We further did temperature dependent I_d-V_g to extract the Schottky barrier height. Obtained Schottky barrier height was .11 eV for EOT 2.73 and .14 eV for 1.57 EOT. It was

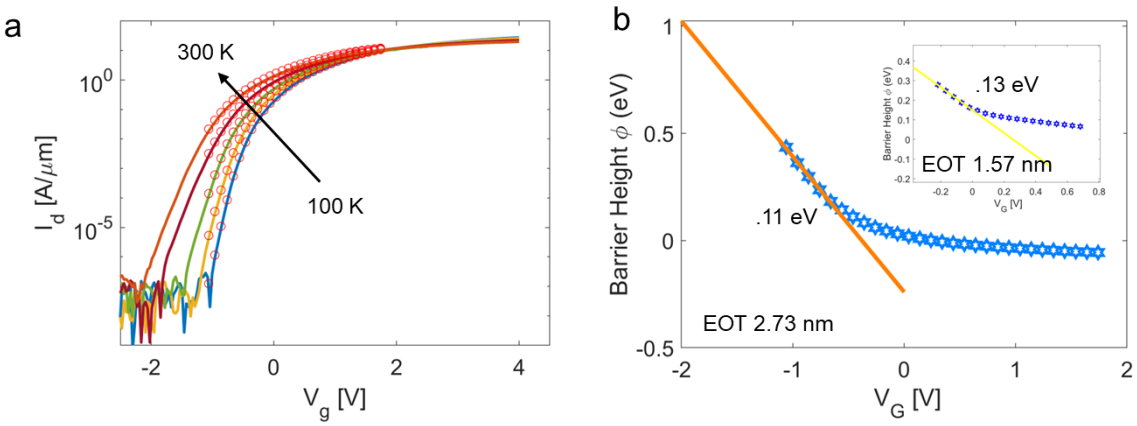

Figure 19. (a) I_d-V_g as a function of different temperature (b) Extracted barrier height is .11 eV (c) Field effect mobility as a function of temperature for increasing gate voltage

consistent for both double gated and top gated device. The purpose of extracting Schottky barrier height was to make sure if we get a large barrier height for any of the devices. It confirms that my extraction of other parameters such as contact resistance, subthreshold swing, field effect mobility and sheet resistance is not at all impacted by the large Schottky barrier height values. The transconductance mobility showed a decrease with an increasing temperature from 16 $cm^2V^{-1}s^{-1}$ to 5 $cm^2V^{-1}s^{-1}$ from 100 k to 300 k. The data were consistent for all double gated devices on the large area of CVD monolayer MoS_2 channel.

4.3 Effect of EOT Scaling

For two-dimensional material Field-Effect Transistor (FET) devices, equivalent oxide thickness (EOT) scaling is essential for several reasons. EOT scaling potentially leads to improved gate control, reduction of short channel effect, threshold voltage control, enhanced carrier transport and reduction of interface trap density[67-70]. The gate dielectric becomes thinner when the EOT is reduced. Improved electrostatic control over the channel is made possible by this thin dielectric. Device performance is enhanced because the gate can modulate the channel more successfully with a thinner dielectric layer. It also results in less scattering and trapping of charge carriers. Better carrier mobility and overall device performance result from this. EOT scaling can assist make the most of the potential of 2D materials, which have the potential for high carrier mobilities. Simultaneously, transition metal dichalcogenides, or TMDs, have distinct electrical characteristics and improved EOT scaling compatibility. By doing this, it guarantees that the gate dielectric is optimized to meet the unique needs of these materials and enhances their overall performance. To

further prove my statements, I have fabricated a total of 3 wafers with 3 different Equivalent oxide thicknesses (1.08 nm, 1.57 nm, 2.73 nm), both having 48 double gate device structures and 12 top gate device structures with 5 channel lengths. I calculated thickness of gate dielectric that would provide same capacitance as actual gate dielectric. For my devices 1.08 nm, 1.57 nm, 2.73 nm refers to 3 nm, 5 nm, and 10 nm of ALD HfO_2. Fabricated devices have been characterized electrically to obtain comprehensive analysis

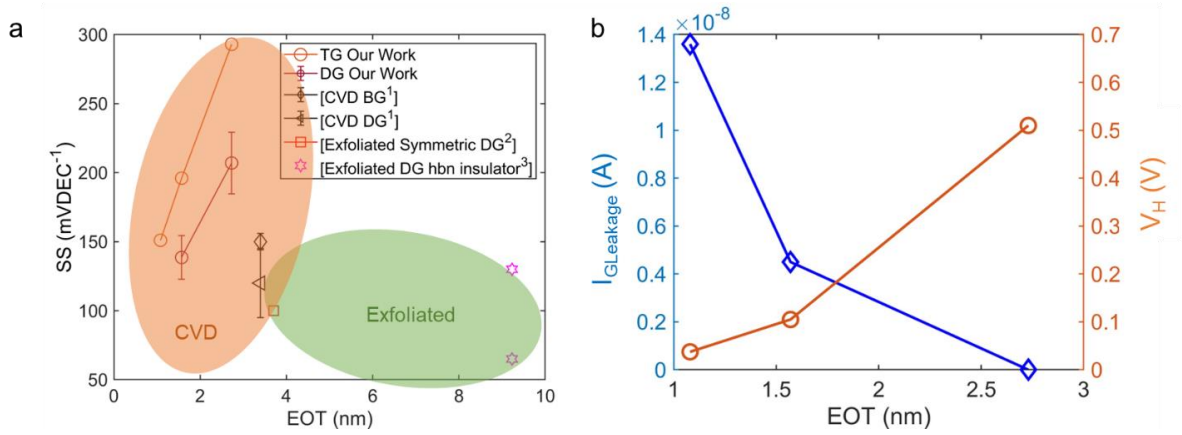

Figure 20. (a) Subthreshold swing as a function Equivalent oxide thickness has been presented for Top gated device, double gated device compared to ideal theoretical trend. Also, shows published data as comparison to my data points. [70,71,72] (b) Gate leakage tends to increase with reducing EOT while hysteresis is decreasing with reducing EOT.

on the effect of EOT. Figure. 20(a) illustrates one of the key parameters - subthreshold swing as a function of different Effective oxide thickness. For a top gated structure, we obtained SS 151, 196 and 293 mV/dec for EOT of 1.08 nm, 1.57 nm and 2.73 nm respective. It also shows recent published data for only double gated device architectures. While that shows a significant downtrend with the scaling of EOT, however the SS values are still far from ideal which is 60 mV/dec. However, we saw a significant improvement in subthreshold swing when we biased both gate at the same time and obtained a SS of 138

and 207 mV/dec for EOT of 1.57 and 2.73 nm stack respectively. The ideal equation for subthreshold swing is given by [70-71].

$$SS = \frac{k_B T}{q} \ln(10) \left[1 + \frac{C_q + C_{it}}{C_{ox}}\right]$$

Here channel capacitance is determined C_q – Quantum capacitance, C_{it} – Interface trap capacitance and C_{ox} – Oxide capacitance per unit area. For ideal calculation we have considered an interface trap density (D_{it}) of $1x10^{13}$ $cm^{-2}eV^{-1}$. The data on the right shows SS values for the exfoliated MoS_2 channel with double gated structures. The devices with exfoliated channel region achieve close to the limit of the subthreshold swing which is 65 mV/dec. On top of the exfoliated channel this work used exfoliated Boron Nitride as the gate dielectric on both side of the channel. These exfoliated hBN layers lack oxide traps which contribute less to the interface trap density, and result in improved subthreshold swing values. However, for my devices I have ALD gate high-κ-dielectric on both sides of the channel material. These dielectrics contain more oxide traps or defects compared to the exfoliated insulator and as a result it leads to higher subthreshold swing. In order for us to get to the theoretical limit, the ALD dielectric growth will have to be optimized with less traps. My data shows consistency with the other published data for double gated device architecture with CVD grown MoS_2 channel. For Interface traps near the conduction band edge of the 2D material (MoS_2) energy bandgap can change the rate at which carriers are injected into or withdrawn from the channel when the FET is in the off state, which can have an impact on the subthreshold swing. Higher interface trap density leads to more traps and these traps could capture carriers, raising the energy barrier for carriers to cross the bandgap and delaying transistor activation. Whereas, the impact of these traps is

diminished with lower interface trap density, allowing carriers to move more freely leading to a steeper turn on and hence lower subthreshold swing. From our obtained results it can be said that our devices have been showing a substantial amount of charge being trapped in the dielectric region. The interface trap density could be improved by having a double gate control over the channel region compared to that of top gate device. Having a double gate with a scaled EOT shows the roadmap towards CMOS scaling. Figure 20 (b) shows gate leakage and hysteresis as a function of EOT. When the gate voltage is being swept up (increasing gate voltage) or swept down (decreasing gate voltage), the relationship between the gate voltage and the drain current changes, because it is directly related to charge trapping and detrapping[75]. Hysteresis effects are typically more prone to thinner gate dielectrics. For our device it was seen that for thinner gate dielectric we notice a much lower hysteresis compared to the thicker gate dielectric. At the same time, it is also observed that for a certain voltage electric field across the gate stacks increases as EOT reduces. As a result of the stronger electric field carriers have an easier time tunneling from the gate terminal to the channel causing a higher gate leakage. For our device we saw a larger gate leakage due to reduction of EOT. Ideally, with a reduced subthreshold swing for scaling of EOT, the current density in the channel should increase. My data elucidate drain current normalized to width and plotted as a function of gate voltage for all three different EOT. I could obtain a larger on current for 1.08 nm EOT devices compared to the 1.57 nm and 2.73 nm devices. More precise electrostatic channel control is possible with smaller EOT. A higher on-current is the result of a more noticeable modification of the

conductance of the channel caused by this control. This has been consistent for all EOT and illustrated in Figure 21.

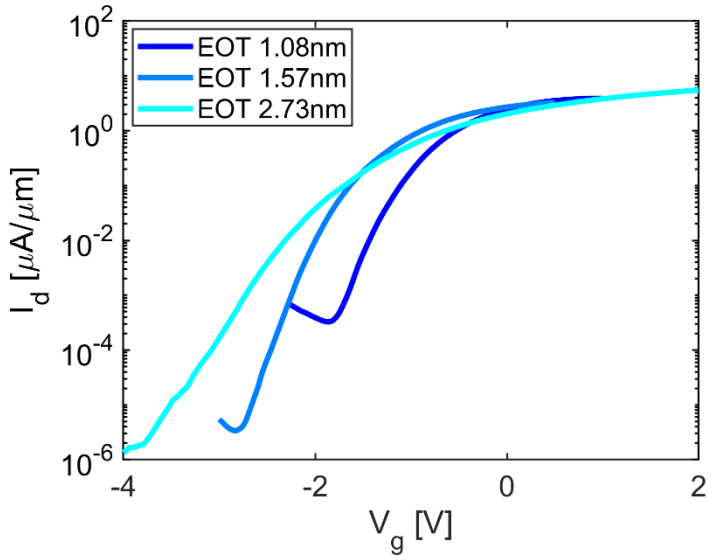

Figure 21. Drain current as a function of gate voltage for three different equivalent oxide thickness. The on current per µA per µm keeps increasing with reducing EOT.

It shows the I_d-V_g as a function of different equivalent oxide thickness. The subthreshold swing steep is visible with changing EOT. Slight improvement in on current can also be noticed with reduction of EOT for 1L MoS_2 FET. Stronger electrostatic coupling between the gate electrode and the channel is made possible by thinner gate dielectrics. As a result, the gate voltage can modulate the channel's conductivity more effectively. As a result, the device can turn on and off more successfully, improving on-current. We do see a lower off current value for 1.08 nm EOT, however that comes from the larger gate leakage that was discussed in the previous section. Larger gate leakage contributes to the off current and makes it go higher.

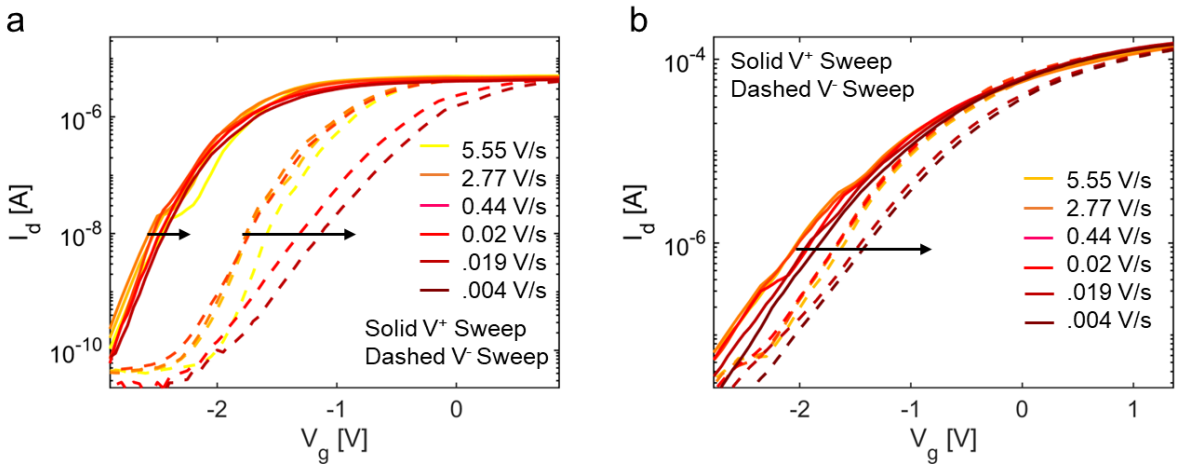

Figure 22**.** To Capture the impact of oxide traps with widely distributed time constant, we adjusted the sweep rate and plotted gate transfer characteristics for positive and negative sweep direction (a) & (b) is respectively for EOT of 2.73 nm and EOT of 1.57 nm device.

4.4 Voltage Sweep Rate Dependent Hysteresis Analysis

Charge trapping in oxide traps with extremely broad time constant distributions has a significant impact on the performance of MoS_2 transistors. These flaws cause the gate transfer characteristics to hysteresis and deteriorate mobility and other performance metrics, which poses a serious problem for these new technologies in terms of reliability and performance. I have conducted a thorough analysis of the hysteresis in double gated MoS_2 FETs and demonstrated that the problem can be identified with the result of threshold voltage shifts brought on by both negative and positive bias direction of the gate voltage. Although these instabilities are widely recognized in Si devices, their significance increases in two-dimensional devices due to the significantly higher defect densities mostly in the high-κ-dielectric insulator regions[75]. These defects contribute to the hysteresis on

the gate transfer characteristics. So, I have performed an analysis of these hysteresis to show the contribution from the threshold voltage shift resulting from positive negative bias temperature stabilities to the interface trap. Now, there is a specific time that is required for each particular defect to capture or emit a carrier under favorable biasing condition.

So, we wanted to capture the impact of oxide traps with widely distributed time constants. So, we adjusted the sweep rate from a range of .004 V/s to 5.55 V/s by adjusting the step voltage and sampling time steps. All the measurements have been done in room temperature and ambient pressure. My device's channel length was large enough (360 nm), which does not show the detrimental affect by the ambient and light. By utilizing both V^+ and V^- sweep directions to measure the gate transfer characteristics at V_d = 1 V, the hysteresis was examined. I computed the sweep rate, which is provided by this equation, in order to quantify the effect of oxide traps. [74,75]

$$Sweep\ Rate\ , S = \frac{V_{Step}}{T_{Step}}$$

V_{Step} is the step voltage and T_{Step} is the sampling time. For my measurements I have put the V_{Step} as constant for all three different EOT and only changed the T_{Step} to change the sweep rate. Larger T_{Step} allow to increase the number of slower traps which are able to contribute to hysteresis. I mostly focused on the top gate device transfer characteristics for all different EOT. Figure 22 (a) and (b) illustrate drain current as a function of gate biasing in both positive and negative direction for different sweep rate ranging from 5.55 V/s to .004 V/s. The gate biasing range for EOT 2.73 nm, 1.57 nm and 1.08 nm was -3 V to 2 V, -1 V to 1 V and -.8 V to .8 V respectively.

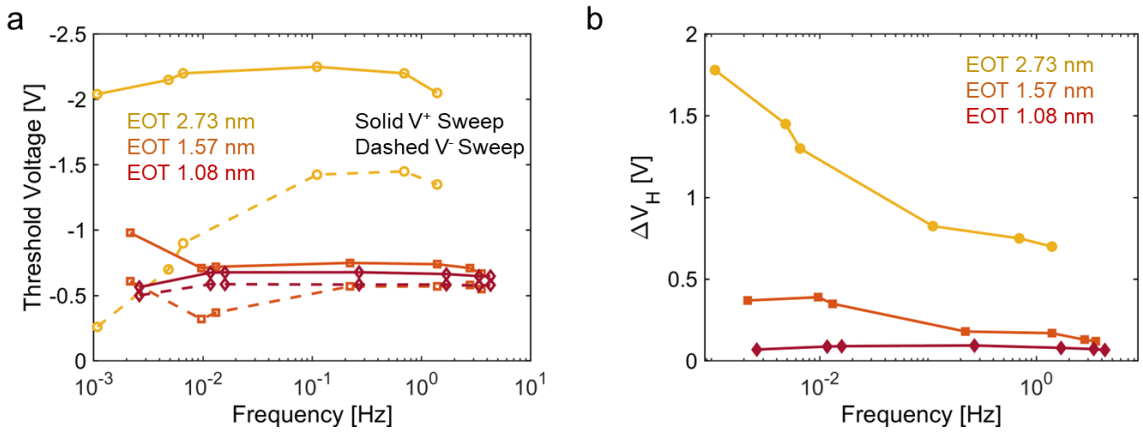

Figure 23. (a) The hysteresis width ΔVH can be treated as a difference between the V_{th} shifts of the I_d–V_g characteristics measured using the V^+ and V^- sweep modes (b) ΔVH as a function of scaling of EOT indicates the number of defects Is typically reduced

The hysteresis width was measured around V_{th} which was extracted using a constant current method. We notice that the V threshold shift towards more positive with decreasing sweep rate. The majority of defects are above the fermi level when the gate bias is less than the flat band voltage. It permits effective electron emission discharge. Hence, compared to V^+ sweep, the threshold voltages determined by V^- sweep are more positive. The sweep rate has a significant impact on the extent of this degradation. The hysteresis decreases with a faster sweep rate and increases noticeably with a slower sweep rate. A PBTI (Positive Bias Temperature Stability) type degradation is observed [75]. Since Sweep rate, which establishes the stress time, has a significant influence on the amount of PBTI deterioration, slower sweeps result in a bigger hysteresis. [73]

Essentially, these data enabled us to divide the overall hysteresis width into the threshold voltage shifts V^{+}_{th} and V^{-}_{th} acquired for the I_d–V_g characteristics as a function of frequency, which were determined using the V^{+} and V^{-} sweep modes. The quantity of oxide traps that can contribute to hysteresis can be determined, with a substantial dependence on Vg. Because traps with capture/emission periods longer than the sweep time cannot react, the number of traps that can contribute is dependent on the sweep rate. Figure 23 (a) illustrates how the threshold voltage has shifted over different sweep directions as a function of frequency. Frequency has been calculated using the number of V_{Step} for each biasing condition with following equation,[75.]

$$f = \frac{1}{NT_{step}}$$

N is the number of V_{Step} of duration T_{step}. In comparison to the narrower sweep range, the hysteresis breadth is significantly higher due to a significantly increased PBTI contribution for EOT of 2.73 nm device. Increase of frequency towards log scale shows a decrease of hysteresis shift. With a thinner dielectric, the number of defects and traps is typically reduced, leading to a cleaner oxide layer at the interface. We can notice that the hysteresis and interface traps reduce with smaller EOT. While for 2.73 nm the same behavior is also noticed on the scaled EOT devices, but not as steep as compared to larger EOT devices. The shift decrease slope is flatter when we scale it down towards 1 nm. Which means the subthreshold swing and other parameters are less affected by the defects in scaled EOT. This is more concisely illustrated in Figure 23 (b). This mechanism can be more precisely described with the Band diagram illustrated in Figure 24. Border traps, which are traps located a few nanometers away from the channel and insulator interface, have the ability

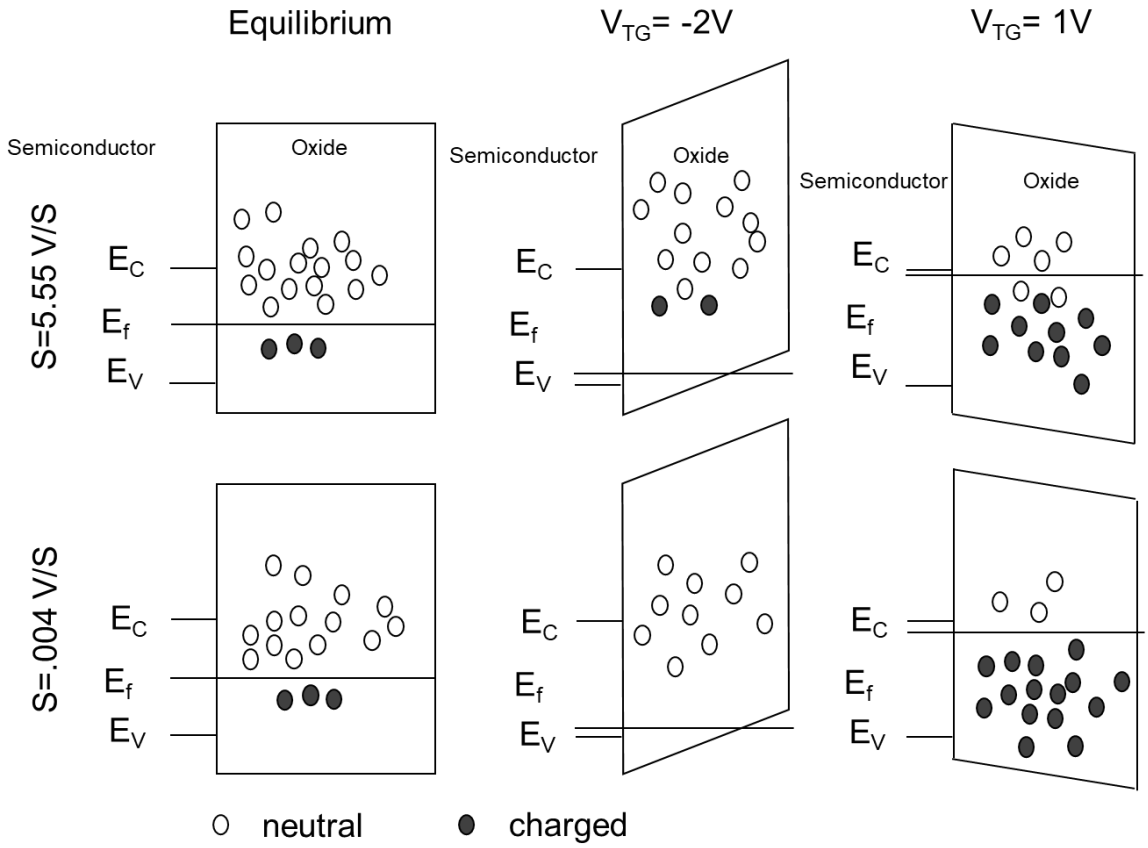

Figure 24**.** The mechanism of having larger hysteresis during slower sweep rate and smaller hysteresis during faster sweep rate has been elaborated with band diagram.

to transfer charges with the channel during device operation through the carrier capture or emission process. The capture and emission times determine how they behave. When the system is in equilibrium, as shown by the flat-band voltage, the defects situated beneath the Fermi level E_F exhibit negative charge, but those above E_F are neutral[75,76-77]. Now, the concentration of charged defects has a significant influence on the device's threshold voltage. In instance, band-bending shifts most defects above the fermi level if a negative gate bias below flatband voltage is applied. Therefore, charged defects can release an electron into the channel and neutralize themselves, with the exception of those having extremely high emission time constants. As a result, the threshold voltage is negative

during the V^+ bias direction and more positive during the V^- bias direction. This is considered the PBTI effect mentioned above[75]. On the other hand, a significant number of defects are below fermi level, which is near to the MoS_2 conduction band, when applied bias is greater than flat band voltage. Neutral defects can take an electron from the channel and become charged, with the exception of those with very large capture time constants. PBTI is the result of Not growing and threshold voltage becoming more positive. The gate hysteresis is the most evident effect of both problems on the operation of MoS_2 FETs. The band diagram shows the same effect considering the slowest sweep rate and highest sweep rate I could achieve using our instrument Keithley 4200 SMU. For a faster sweep rate with a gate voltage larger than flat band voltage most of the charged defects are below fermi level, however there are some neutral defects Those neutral defects need more time to take an electron from the channel and become charged. On the other hand, for a slower sweep rate the time constant is larger and all those neutral defects are able to take an electron and become charged and get captured in the data, hence gives rise to the larger hysteresis. Now, a thinner dielectric usually results in fewer defects and traps, (Thinner dielectric layer has less volume leads to lesser traps in the oxide) which cleans the oxide layer at the interface. With decreasing EOT, we can see that the hysteresis decreases. The threshold voltage shift shows a decrease at 2.73 nm EOT, but as we scale it down to 1 nm, it becomes flatter. This indicates that the flaws in scaled EOT have less of an impact on the subthreshold swing and other metrics. Especially at an EOT of 1.08 nm there hasn't been any significant change with hysteresis as a function of frequency. Sweep rate has a lesser effect on these devices. The number of traps can be calculated for each of the devices which contribute to the

hysteresis. Our thorough investigation of the hysteresis analysis of top-gated FETs with EOT scaling provides insight into the degradation of the device caused by the charging and discharging of oxide traps. I was able to map oxide traps with widely distributed time constants accurately by using an additional incremental hysteresis sweep technique. This research is going to shed light on advanced fabrication techniques, material engineering, scaling of EOT and precise gate control to both gates does lead to much better performance metrics and go beyond Moore's law.

Chapter 5

Novel Material exploration

It was discussed earlier in this dissertation that the microelectronics industry is searching for alternative semiconductor materials as silicon-based transistors are reaching their physical limits. As discussed earlier, 2D TMDs have emerged as promising candidates for beyond-Si CMOS, but significant challenges remain. For example, their lack of high-quality native oxides, in contrast to silicon with native silicon dioxide (SiO_2), presents challenges towards scalability and stability of metal-oxide-semiconductor (MOS) stacks. Thus, while 2D TMDs have demonstrated significant potential for use in MOSFETs and other device applications, it is imperative to explore other materials beyond TMDs for various reasons such as band gap engineering, compatibility with CMOS and with advanced device architectures (e.g., gate-all-around nanosheet FETs), high-quality semiconductor/dielectric interface, high-mobility and injection velocity, etc. This chapter of my dissertation discusses initial experimental work on emerging 2D semiconductors beyond TMDs. This includes 2D Janus TMD semiconductors as well as 2D bismuth oxychalcogenides (e.g., Bi_2O_2Se), two novel material systems with interesting and potentially transformative properties for future electronic devices.

5.1 Janus Dichalcogenide Field Effect Transistor

Recently, Janus TMDs, a new family of 2D semiconductors with a significant cross-plane (cp) dipole has been introduced. Janus TMDs contain two faces of different chalcogen atoms[79]. Here, the difference in electronegativity of the chalcogen atom faces results in large charge transfer within the 2D layer structure[79]. A large E-field is produced

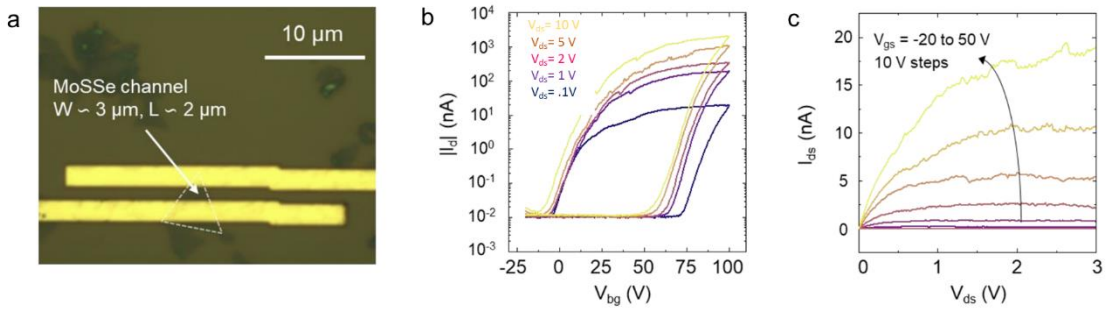

Figure 25: (a) Schematic The synthesized 2D Janus TMDs exhibit field-effect-transistor (FET) performance much like those in classical TMDs demonstrating its electrical grade. Gate stack was SiO_2 300 nm. (b) & (c) I-V characteristics of backgated Janus MoSSe FET. I_d-V_d showing a transition from off state to on state with gate step from -20 V to 50 V.

as a result of this effect, pointing in an out-of-plane direction. For example, in MoSSe, variation in electronegativity between S and Se atoms, results in a dipole across the 2D slab and a significant difference in work-function between the two surfaces for a whole layer. Janus TMD are a promising candidate for highly efficient solar cells[79]. Theoretically, it has been demonstrated that multilayer Janus solar cells can produce a photocurrent that is greater than that of thin-film silicon devices, pointing to a prospective material that could be used in photovoltaics devices[80,81]. This underlines the great potential of Janus materials in thin-film photodiodes. Despite these intriguing theoretical predictions, there have been few actual experiments to yet mostly because manufacturing 2D Janus devices is difficult and limited material quality.

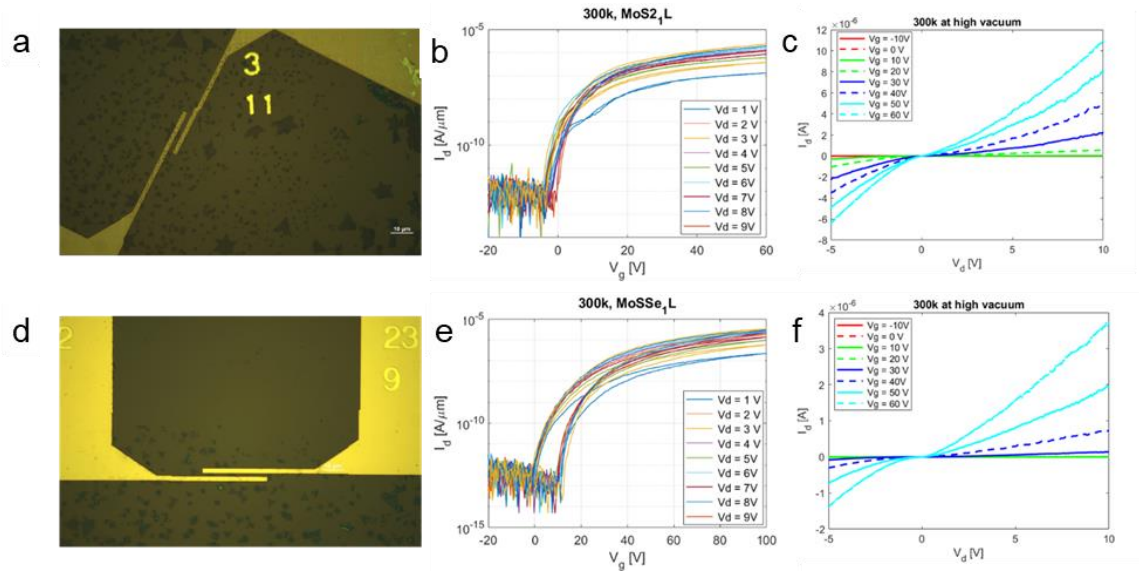

Figure 26: (a) Optical image of monolayer MoS_2 FET device with a channel length of 2 µm and channel width of 4.1 µm. (b) &(c) $I_d - V_g$ as a function of different drain voltage of the as fabricated monolayer MoS_2 FET) Optical image of monolayer Janus MoSSe FET with a channel length of 1.6 µm and a channel width of 1.8 µm. (e) & (f) I_d-V_g as a function of different drain voltage (1V - 9V) of Janus FET at room temperature.

In my studies of Janus TMDs, I have fabricated back-gated MoSSe FETs on Si/SiO_2 wafers and conducted electrical characterization. The measurements revealed large current density with a large on-off ratio of 10^6. The I_d-V_d shows current as a function of different gate steps starting from the off state to on state. We have previously been able to fabricate two Janus FET devices. One with CVD grown MoSSe and other with exfoliated SWSe. Figure 26 shows a temperature dependent comparison between two terminal MoS_2 FET and MoSSe Janus FET. MoSSe shows a larger on current and a smaller subthreshold swing compared to the MoS_2 FET device, which are two of the key performance metrics of transistor device. Both the devices had a 300 nm global SiO_2 gate stack. Electrical transport can be improved by fabricating them with an independent gate and HKMG stack as dielectric. The fabrication process for that is mentioned in detail in Figure 26.

Further, we worked on exfoliated and converted SWSe (Figure 27) as channel material to fabricate FET structures. IV characteristics for SWSe FET device has been shown below. Obtained field effect mobility was 26 $cm^2V^{-1}s^{-1}$.

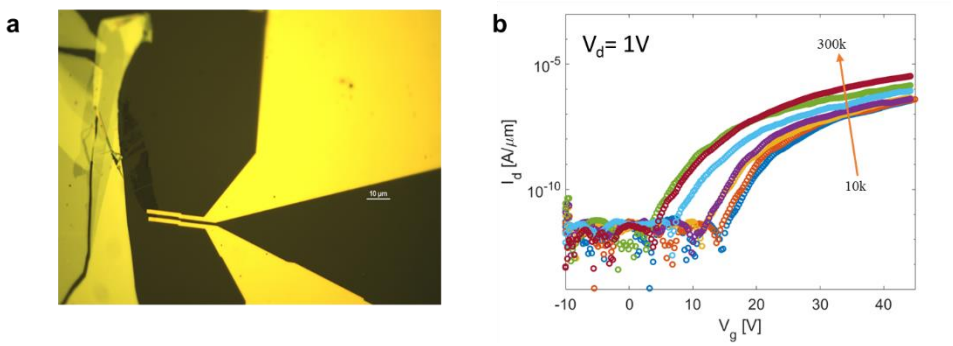

Figure 27. (a) optical image of exfoliated and converted Janus SWSe FET with a channel length of 1 um. (b) I_d as a function of V_g for low temperature to room temperature.

Also, it has been found that when these 2D Janus TMDs are exposed to a little quantity of solution, whether from sources that are exfoliated or CVD, they begin to curl (for example, DMF, acetone, IPA, PMMA). The cause is the accumulation of intrinsic strain brought on by various chalcogen atoms. Our prior fabrication process required a masking with photoresist or PMMA to fabricate transistor devices. Which actually initiates the curling process of these Janus monolayers. We have worked on a new fabrication process that avoids solution processing directly on the channel material and also compatible with back end of the line process integration.

Figure 28 shows 2 terminal Janus nanoscroll FET with Pd/Au contact. The device also had a great electrical responsiveness, and its I-V behavior was compatible with simulations of conventional FET. The devices substantially shielded (scrolled) structure kept the device's response constant over a variety of gaseous environments during the annealing and vacuum cycles. Starting WSe_2 monolayers demonstrated typical p and n-

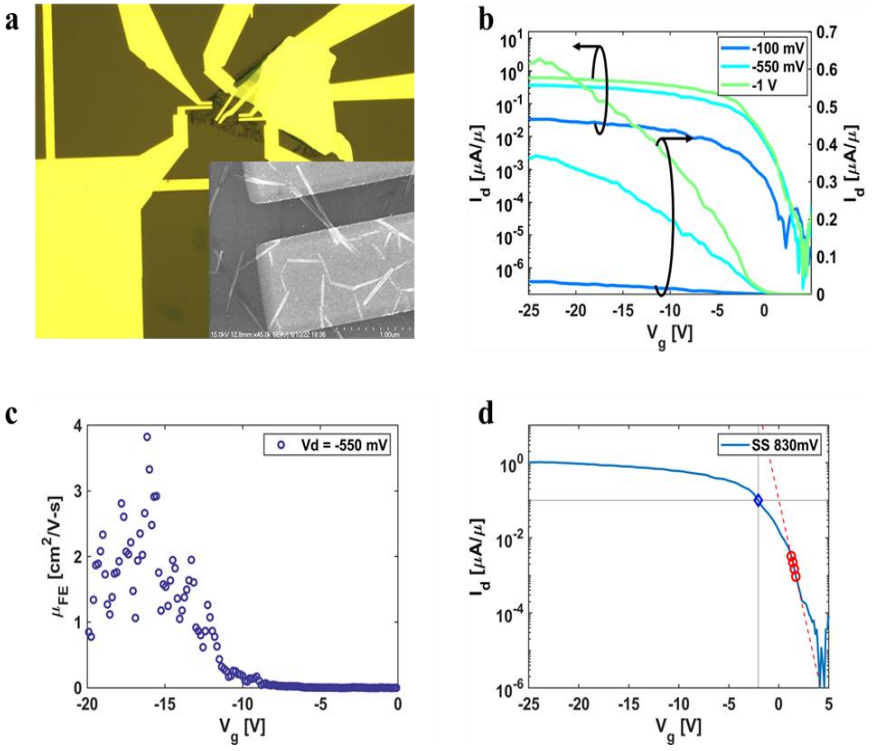

Figure 28. a. Optical image of backdated Janus SWSe FET with a channel length of 370 nm. b. Transfer characteristics (I_d-V_g) plotted in both log and a linear scale for SWSe scroll FET with Pd/Au contact as a function of drain voltage at room temperature c. extracted Field effect mobility d. extracted subthreshold swing.

type conduction, while Janus nanoscrolls only showed p-type conduction, which is now unexplained and calls for further research. Using Equation, the entire field effect mobility was computed [74,80].

$$\mu = \frac{d(\frac{Id}{Vd} \cdot \frac{L}{W} \cdot)}{dVg} \cdot \frac{1}{Cg}$$

Here, L and W are the channel length and width, respectively, μ is the field effect mobility, C_g is gate capacitance per unit area (F/cm^2), and V_g is the gate bias voltage. Extracted field effect mobility was in the 3-4 cm^{2}V^{-1}s^{-1} range, with an on/off ratio > 10^3 for multi-walled nanoscrolls and > 10^5 for fewer walls[74]. The Janus nanoscrolls FETs mobility values are

comparable to flat Janus MoSSe (5-10 cm^2/V-s). We observe that harsh plasma processing/chemical treatment steps during lithography lead to large vacancy defects being generated in Janus TMDs, which are likely associated to reduced mobility values[74]. Nevertheless, channel and gate-stack engineering, such as optimizing the number of walls in the scrolls, may be used to increase mobility. The extracted subthreshold swing was 830 mV/dec.

5.2 Photoresponse Analysis of Janus SWSe and WSe_2 channel

By taking measurements while the channel region is under controlled illumination, a separate effort is made to comprehend the impact of the electric field in the channel region. For this purpose, we have prepared a WSe_2 back gated FET device (90 nm SiO_2) and did transfer characteristics on both dark and in illuminated state. (Figure 29a shows optical image of a back gated FET before and after Janus conversion). While attempting to control the channel through gate, a considerable on-off ratio was only seen in the off-state region (Figure 29b). A zero-gate bias I_d-V_d shows (Figure 29 (c)) a significant difference at dark and illuminated state and at a drain voltage of -2.5V responsivity was calculated as 1.372 nAW^{-1}. Responsivity was calculated from the equation $R = \frac{I_{illuminated} - I_{dark}}{P_{illuminated}}$, where R is responsivity, $P_{illuminated}$ is illuminated power of laser, $I_{illuminated}$ denotes as measured current under light, I_{dark} denotes as measured current under dark[69]. Furthermore, the channel region was converted to SWSe into plasma processing chamber. To secure a good electrical property, a high vacuum anneal, and a chloroform treatment were performed prior to the construction of the device. The same measurements were performed after conversion, and we obtained a slightly higher responsivity of 2.458 nAW^{-1}(Figure 29 (d)). The on-off ratio before and after Janus conversion at a drain voltage of -2.5V is 68.67 and

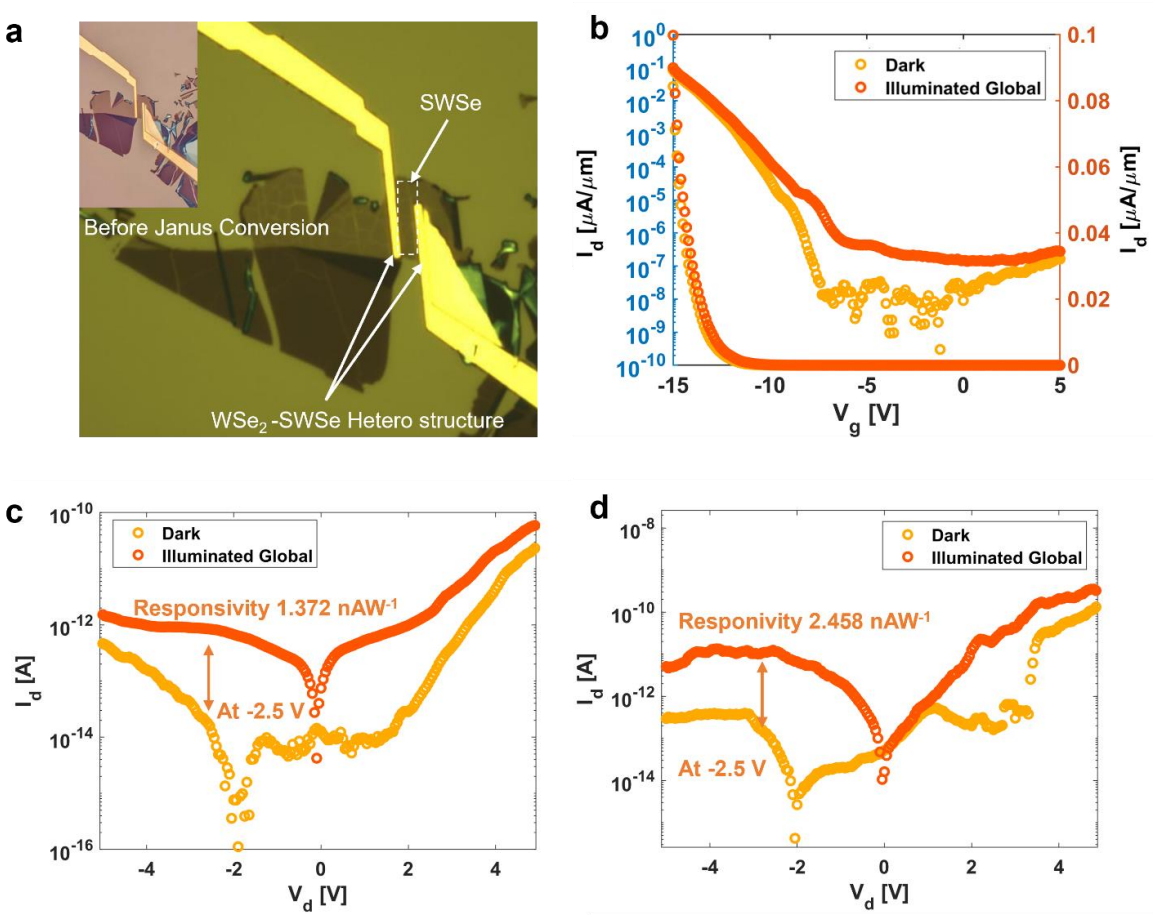

Figure 29. a. Optical image showing WSe_2 FET before and after Janus (SWSe) conversion in the channel region. b. Drain current as a function of gate voltage has been plotted in both linear and log scale for WSe_2 FET for a drain voltage of -1 V. c. & d. show I_d as a function of V_d for a zero bias gate voltage. All measurements were taken in the dark and using direct afterglow illumination of the channel area.

123.9 respectively. We are planning to do these same measurements on a device where the channel will be encapsulated with high k dielectric and side contacts will be used as our source and drain contact. As there won't be any solution process immediately on the material, which likes to scroll up right quickly, this method will be less damaging to the channel region. Due to its distinct structure (Both MoSSe and SWSe), the built-in electric field effect has great potential for solar cell and photodetector systems. Its adjustable characteristics and effective separation and collection of photo-generated charge carriers make it a promising choice for advanced optoelectronic applications.

5.3 Novel Device Fabrication with Bi_2O_2Se

Electronics researchers and engineers are taking an interest in bismuth-oxy-selenide (Bi_2O_2Se) as a possible contender in the search for new semiconductor materials for next-generation Field-Effect Transistor (FET) devices. Bi_2O_2Se, was recently reported to have grown via powder evaporation[82]; the resultant material exhibited outstanding on/off ratio, ultra-high carrier mobility, moderate bandgap and air-stable properties. Bi_2O_2Se has a special set of characteristics that make it ideal for FET applications. Bi_2O_2Se is a member of a group of substances called topological insulators. In bulk form, these materials are insulators, but they have conductive surface states that are called topological surface states. Charge carriers have great mobility in these states, which shield them from scattering. Additionally, it is appropriate for digital electronics applications due to its intrinsic band gap. These materials can be grown on top of MICA substrate using the cracking metal-organic chemical vapor deposition (c-MOCVD) technique[82]. First, it demonstrates ultrahigh carrier mobility, moderate band gap, outstanding stability, and excellent mechanical properties. Second, by layer-by-layer oxidation of the underlying 2D Bi_2O_2Se semiconductor at high temperatures, bismuth selenite (Bi_2SeO_5) can be conformally produced with atomically thin dielectric layers which ensures a chemically clean and crisp interface[82.83]. An optimal gate dielectric for Bi_2O_2Se FETs can be directly provided by the insulating Bi_2SeO_5, owing to its high dielectric constant and strong band alignment with the semiconductor. The native oxide Bi_2SeO_5 forms an atomically sharp interface with Bi_2O_2Se and can directly serve as a gate dielectric. Using this native oxide dielectric, high-

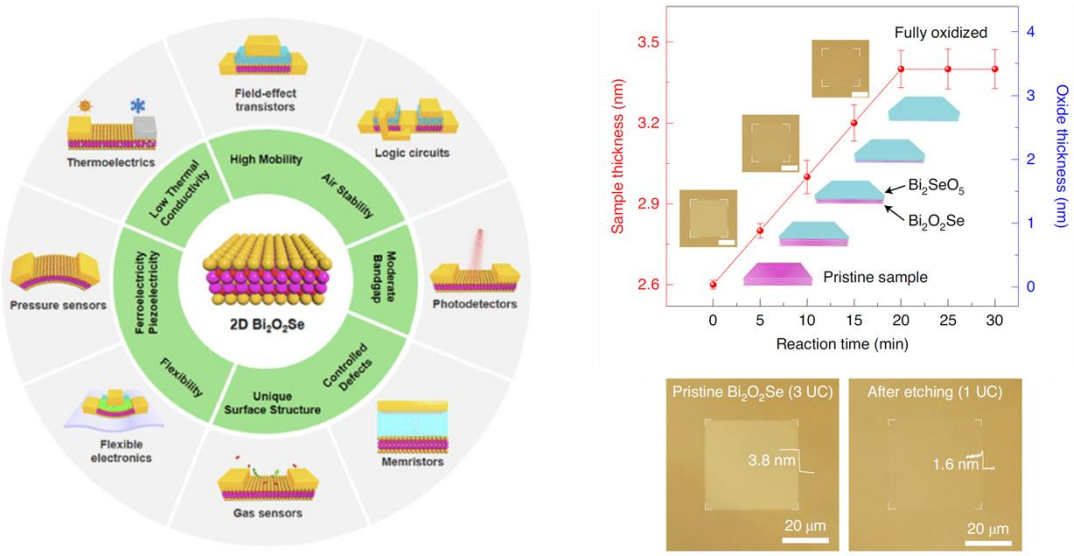

Figure 30**.** Schematic of New emerging air stable, high mobility Bi_2O_2Se film showing its potential application[82]. Film thickness and Oxide thickness as a function of reaction time showing the native oxidation of the Bi_2O_2Se followed by AFM images showing the ability to obtain thinner sample[82].

performance Bi_2O_2Se field-effect transistors can be fabricated. The air stable semiconductor Bi_2O_2Se has a mobility value of more than 20,000 $cm^2V^{-1}s^{-1}$; before, this level of mobility was only seen in chemical vapor deposited graphene. High ionic contribution from low frequency phonon modes theoretically leads to large mobility for Bi_2O_2Se[84]. The in-plane static dielectric constant as thickness decreases towards the 2D limit and its implications for FET scaling are still not well understood or supported by enough number of experimentations. These bismuth oxychalcogenide shows different range of band gaps (.7 eV to 1.6 eV depending on the elemental composition)[82]. Bi_2O_2Se is a widely desired material for a variety of electronic applications due to its many fascinating electrical characteristics, as demonstrated by device-level investigations conducted thus far. According to previous studies conducted on Bi_2O_2Se, transistors have demonstrated FET mobilities as high as 750 $cm^2V^{-1}s^{-1}$ in few nm channels (~ 6–20 nm)

Figure 31. (a) Bi_2O_2Se film on Mica merged in 16% HF solution (b) A bubble math sonication peel off the film from Mica and allow transfer on to Si substrate (c) Raman spectra shows films quality consistency after wet transfer

and theoretical values of mobility as high as 4,600 $cm^2V^{-1}s^{-1}$ [83]. These values surpass those of silicon and other 2D TMDs with similar thicknesses. The dielectric constant of Bi_2SeO_5 is 21 which is larger than the high-κ-dielectric HfO_2, Al_2O_3, SiO_2[85]. Because it may provide conformal gate dielectrics with sub-1 nm equivalent oxide thickness (EOT) and excellent interface quality, this native oxide is essential for MOS device scalability. Furthermore, it is possible to etch the native oxide Bi_2SeO_5 without endangering the underlying Bi_2O_2Se. Recent work has showed that the native oxide may be selectively etched using a wet etch method, at the same time maintaining the mobility of the underlying semiconductor, which opens a possibility to fabricate a lot of complex device architecture for this material. In light of this, Bi_2O_2Se is a young yet promising semiconductor platform for the semiconductor industry's future and the upholding of Moore's law.

Bi_2O_2Se that I used was primarily grown on MICA substrate[82]. So, we had to go through a transfer procedure to etch MICA from underneath transfer the floating film on top of Si/SiO_2. The transfer process includes 16% HF solution dip for 3 hours and a water Bath sonication for a minute to finally peel the film off completely from MICA. The transferred MICA then treated other processing steps before we start fabricating devices

on it. Figure 32. shows some preliminary data that we have obtained for our Bi_2O_2Se devices. It's a two terminal FET. The thickness of the material is 30 nm approximately. The I_d-V_g looks very promising and for sure with thinner samples we will be able to tune the band to get a nice subthreshold swing. A 480 Degree thermal oxide treatment can oxidize the top surface where we can actually use the native oxide as gate dielectric. All the measurements have been done in room temperature. Data has been taken for all different drain voltages. The data presented in Figure 32 was for 1V drain voltage. It can be seen that a on/off ratio of 10^5 is obtained with Ti /Au as the contact material. All the devices have a gate stack of 12 nm HfO_2 and 2 nm Al_2O_3. One of the devices showed an on-off ratio of 107. The subthreshold swing was around 629 mV/dec. Normalized on current was 45 µA/µm and transconductance peak mobility 23 $cm^2V^{-1}s^{-1}$. The comparatively thicker channel devices didn't show any gate control.

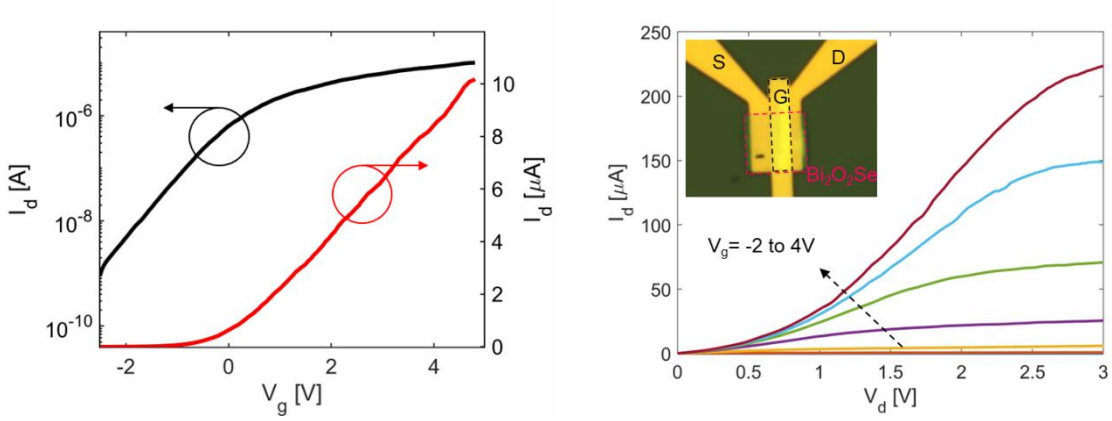

Figure 32. (a) Preliminary top gated Bi_2O_2Se FET. I_d-V_g both log and linear scale. (b) Preliminary top gated Bi_2O_2Se FET. I_d-V_d characteristics for a gate step of -2V to 4V. The insets show the optical image of the top gated FET device.

The as grown films were 30 nm – 50 nm thick. The thickness can be scaled down by oxidizing the top layer of the surfaces. I have worked on some Ar plasma etching techniques to etch some of the top layer successfully. The etch rate has been determined

by the etching power and gas flow. After obtaining a thinner material a lot of improvements in the transfer characteristics can be made. Good thermal stability is a critical component of device reliability, particularly in high-temperature settings, and Bi_2O_2Se demonstrates this quality.

Some additional devices have been fabricated and characterized based on their selective

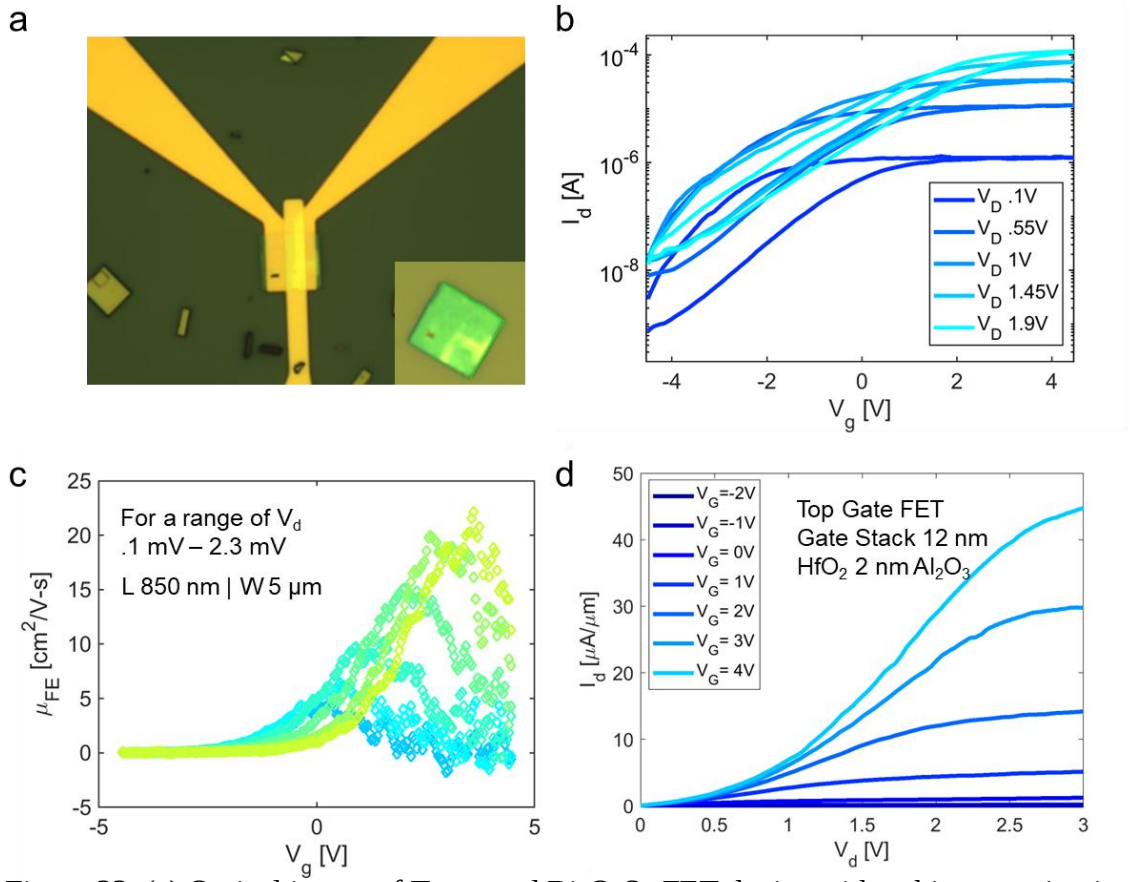

Figure 33. (a) Optical image of Top gated Bi_2O_2Se FET device with a thinner region in as the channel. (b) I_d-V_g for five different drain voltage (c) Extracted transconductance mobility (d) I_d-V_d as a function of gate voltage steps.

approximated thickness. Drain current has been plotted as a function of gate voltage for a range of drain voltage from .1V to 1.9 V. Transconductance mobility has been extracted (peak mobility of 24 $cm^2V^{-1}s^{-1}$), illustrated as of Figure 33 (b).

While Bi_2O_2Se shows great promise as a next-generation material for FET devices, it's important to note that ongoing research is needed to optimize its properties, improve device fabrication techniques, and fully explore its potential in various electronic applications. Undoubtedly, the investigation of Bi_2O_2Se in relation to Field-Effect Transistor (FET) devices has uncovered encouraging properties; nonetheless, additional study is necessary to fully realize its potential. Research efforts can be tailored to specific applications, such as optoelectronics, low-power electronics, or sensing, to gain significant insights into how Bi_2O_2Se can meet certain market needs.

CHAPTER 6

CONCLUSION

My research reveals in-depth improvements in important performance metrics, such as carrier mobility, on/off current ratio, and subthreshold swing. These advances are made possible by using rigorous fabrication, device design, and materials engineering techniques. We look at methods to reduce contact resistance and improve the 2D material and dielectric interface, leading to appreciable improvements in device properties. Our research also shows that the electrical characteristics of WSe_2 are tunable, providing the opportunity to modify its bandgap for certain device applications. These developments in 2D p-type WSe_2 transistors offer a compelling alternative to conventional silicon-based methods and suggest a potential path for the further development of CMOS technology. In order to realize progressively scaled CMOS technology, this research is expected to contribute to the ongoing study of 2D materials for future semiconductor devices.

Further, I presented an investigation into the electrical performance of CVD-grown monolayer MoS_2 FETs featuring double gate control. Double gates, which offer independent modulation of the channel region, provide a versatile platform for channel engineering. Our devices with double gated structures showed a significant improvement in the subthreshold swing, contact resistance and transconductance mobility in comparison to top gate design of the same device architectures. Obtained contact resistance for double gated and Top gated FET was 13.96 KΩ-μm and 100.06 KΩ-μm, respectively. Moreover, we explored the impact of scaling the Equivalent Oxide Thickness (EOT) on the FET's electrical characteristics. EOT scaling reduces the thickness of the gate high-κ-dielectric

dielectric (HfO_2 10 nm, 5 nm & 3 nm), leading to enhanced electrostatic control over the MoS_2 channel. This scaling results in a more efficient and precise modulation of the device properties, contributing to a reduction in subthreshold swing (We obtained 125 mV/dec for 1.08 nm EOT) and threshold voltage variation. Negative & positive bias temperature instability measurements were performed to further analyze the hysteresis of our devices with different EOT to extract the interface trap density shift. Our research unveils the effectiveness of EOT scaling in minimizing interface traps and improving the quality of the dielectric-MoS_2 interface. These results provide insight into how double gate control and EOT scaling in CVD-grown monolayer MoS_2 FETs can progress the field of 2D material electronics and pave the way for high-performance, low-power semiconductor applications. I investigated the possibility of improving the performance of Field-Effect Transistors (FETs) made of 2D materials by combining the scaling of the effective oxide thickness with the use of double-gate control. Scaling effective oxide thickness and double-gate control work together synergistically to improve the performance of 2D material FETs overall. I believe that the implementation of high-performance, next-generation electronic devices will be considerably aided by these tactics, further solidifying 2D materials as a competitive choice for cutting-edge semiconductor technology.

In essence, the investigation of Janus TMD dichalcogenides and Bi_2O_2Se represents a major advancement toward the development of sophisticated FET devices that can meet the increasing needs of contemporary electronics. These materials have the potential to transcend 2D TMDs and become essential parts of the next generation of FETs by utilizing their special characteristics and engineering opportunities. Janus TMD dichalcogenides

and Bi_2O_2Se are potential possibilities that can not only meet but significantly beyond the expectations for high-speed, low-power, and multifunctional FET devices with complex architecture since FET scaling and performance continue to be of utmost importance. These materials offer a compelling way ahead for semiconductor technology and the development of electronics due to their exceptional qualities. My preliminary data on both types of these devices supported this conclusion and revealed future prospect of these materials in semiconductor roadmap.

The journey through my doctoral research has been a transformative exploration into the world of two-dimensional Field-Effect Transistor (2D FET) devices. In the beginning, I concentrated on improving the performance of p-type WSe_2 FETs by taking advantage of this material's special qualities to increase reliability and efficiency in electronic applications. As the study progressed, I explored double-gated device transfer characteristics and used monolayer CVD MoS_2's potential as a channel region. Double gates were a breakthrough that made it possible to achieve even further improvement in device performance. Concurrent research on Equivalent Oxide Thickness (EOT) scaling made possible more control and scalability. I explored the fascinating field of emerging semiconductor materials, moving beyond the well-known field of transition metal dichalcogenides (TMDs) which presented boundless opportunities for innovation and the potential to redefine the landscape of semiconductor technology. To sum up, my doctoral journey includes the careful tuning of p-type WSe_2 FETs and their improvement in device performance, the implementation of MoS_2 channel double-gated devices, and the investigation of new semiconductor materials outside of TMDs. The information and

expertise I've acquired have improved my academic career and added to the continuous search for new developments in the field of semiconductor technology.

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