Development and Comparison of Industry Available Flyback Topologies

by

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ABSTRACT

This paper introduces an application space of Power over Ethernet to Universal Serial Bus (USB) Power Delivery, and develops 3 different flyback approaches to a 45 Watt solution in the space. The designs of Fixed Frequency Flyback, Quasi-Resonant Flyback, and Active Clamp Flyback are developed for the application with 37 Volts (V) to 57 V Direct Current (DC) input voltage and 5 V, 9 V, 15 V, and 20 V output, and results are examined for the given specifications. Implementation based concerns are addressed for each topology during the design process. The systems are proven and tested for efficiency, thermals, and output voltage ripple across the operation range. The topologies are then compared for a cost and benefit analysis and their highlights are identified to showcase each systems prowess.

DEDICATION

This thesis is dedicated to my wife, Emily. With her, I can truly have it all.

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CHAPTER 1

BACKGROUND AND BASIS

Power over Ethernet

A long-standing market for DC-DC converters is Power over Ethernet (PoE). Power over Ethernet is a specification which allows for power delivery to take place over an Ethernet cable which also delivers data. PoE recently underwent an update to the specification in 2018 to IEEE802.3bt+ which allowed the power range to expand to 100 Watts over an Ethernet line. This opened up for the possibility within industry to develop DC-DC converters within a higher power range than the previous specifications, and encouraged companies to look into the possibility of utilizing Ethernet ports for more general charging purposes including phones, laptops, and additional Internet of Things (IoT) connected devices.

PoE benefits in the marketplace stem from many sides. Installation of PoE allows for network cables to be another primary source of power, especially with the higher power ratings. While certified electricians are needed to install AC lines, network cables can be installed anywhere and do not require a certification for installation. This makes them cheaper and more accessible around a site. The use of PoE for an increasing array of smart devises also decreases cabling concerns, using only one cable to provide both power and data along with hooking it up to the network.

The power for PoE comes from a central source installed in the site. The standard installation for PoE is an Ethernet switch which is enabled to send and receive data and can be rated up to a certain power. Specifications for PoE have been updated since their inception, and older Ethernet switches and infrastructure may not be rated for the power

or have the number of ports necessary for the new ratings or all the smart applications which could be included in buildings. The PoE market has adapted for this change and if the Ethernet switch is not capable of the PoE that is needed in the end application, a PoE Midspan can be implemented in the infrastructure to increase the power rating. The Midspan will introduce additional power capabilities and additional ports to the Ethernet port and can be equipped with an Uninterruptable Power Supply to ensure that the system does not lapse power in case of an outage. [1]

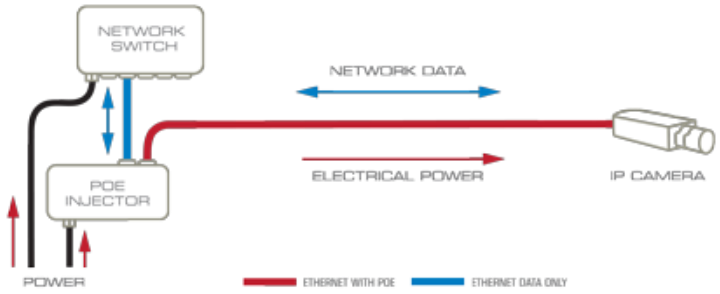

Figure 1 Power over Ethernet Structure [1]

USB-C Power Delivery

The addition of charging possibilities for higher power devices opened the door for a range of options. One of these options is USB-C Power Delivery (USBPD) based devices. USBPD utilizes the USB-C cable end in order to deliver power to a variety of end power devices and is capable of varied output voltage as requested by the charged device. The USBPD port defaults to 5 V and can be negotiated to a varied output voltage of 9 V, 15 V, or 20 V, with capabilities of 3 A for 5 V, 9 V, and 15 V, and up to 5 A at 20 V. The USB-C cable end is compatible with a variety of devices and is quickly becoming

a more widely adopted charging port and protocol. This range of operations and the widely adopted USB-C port means end devices can be cell phones, tablets, laptops, Internet of Things (IoT) cameras, and many more. Another benefit of using USBPD devices is the ability to transfer power and data over the same port, rather than needing a distinct power port and a distinct data port. USB-C ports can support power and data transfer for functions like HDMI and Ethernet ports. [2]

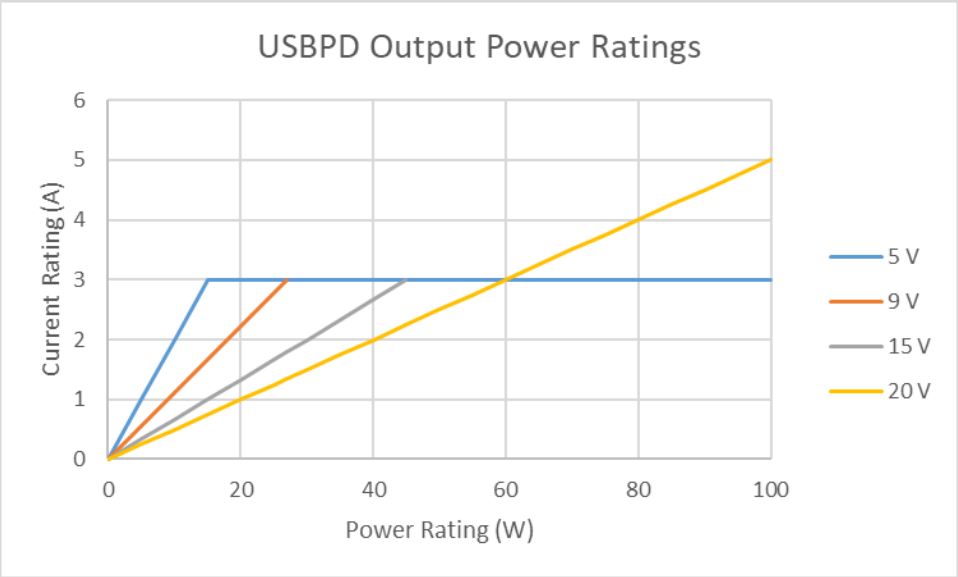

Figure 2 USBPD Output Ratings Chart

Combination of PoE and USBPD

The combination of PoE and USBPD is what will be investigated within the scope of this project. This is an emerging market combining two data capable ports for a convenient charging and connected solution. This general solution category allows for a large range of input power and a wide breadth of powered devices to utilize the adapter. The PoE protocol sets the input voltage for the design with its specifications from 37 V to 57 V DC input, and USBPD sets the output voltage as 5 V, 9 V, 15 V, and 20 V. This

application will be developed for 45 Watts, as this is a convenient pick-off point for low power laptops to receive their necessary charging level. For this design, a standard frequency minimum point will be selected at 100 kHz.

Power Rating	45 W
Input Voltage	37 V to 57 V
Output Voltage	5 V to 20 V
Output Current (≤15V)	3 A
Output Current (20V)	2.25 A
Operating Frequency Min	100 kHz
Output Ripple Spec	±5 %

Table 1 Design Parameters

CHAPTER 2

UNIVERSAL CONSIDERATIONS

While each topology comes with its own implementation concerns, certain concerns come from the application which is attempting to cover a wide range of output voltages. Having a wide range of output voltages affects the rating of each element, it means that every element must be rated to the maximum voltage it will experience. This mean that the system must be designed for the maximum output voltage, as this will be the case with the maximum voltage stress across the system on both primary and secondary side.

V_{cc} Variation

In addition to maximum voltage ratings, the system must be ensured to operate at the minimum rated voltage, which is to ensure that all controllers can operate from voltage supplied from a 5 V output and a 20 V output without being below the minimum operating voltage or above the maximum rated voltage. While this works well for some controllers this could cause over-voltage conditions or under-voltage conditions for others. On the primary side the controllers output voltage is supplied proportional to the output voltage, and while taking into account the ratings of the controller it requires that a different ratio must be used for minimum output voltage as is used for maximum to provide a stable supply voltage without exceeding or becoming insufficient. As the primary side voltage ratio will be active under all conditions the highest supply voltage to the controller needs to be regulated and limited to ensure the controller is not damaged.

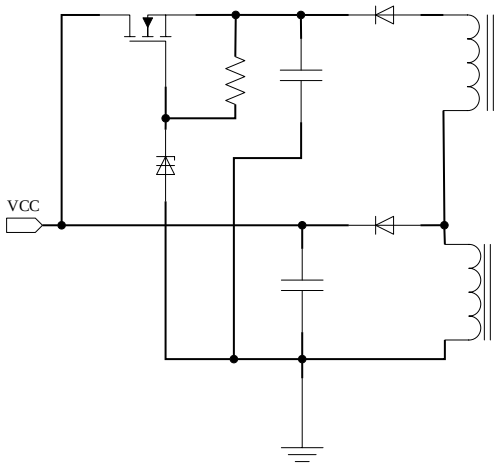

Figure 3 Vcc Split Winding Schematic

In addition to output voltage variation, all components must be designed to the maximum rating of the input voltage as well. This ensures that the converter can operate under all conditions of both input and output.

Current Sensing Methods

The controllers chosen for these designs feature varying levels of current sense thresholds in their systems. Because of the high currents moving through the designs at minimum input voltage and maximum power, the current sense resistor required is a significant loss mechanism of the design. In order to best implement a standardized design to compare between topologies, a current sense transformer is implemented instead of a current sense resistor.

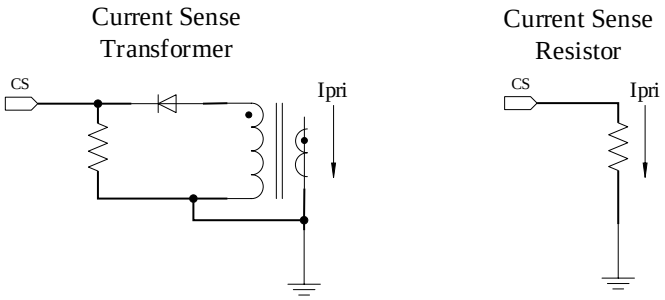

Figure 4 Current Sense Methods Schematics

Transformer Winding

When designing the transformer, turns ratio is chosen during the topology design selection, but there are many additional parameters to take into account during the physical design of the transformer. One major concern when figuring out exact design is ensuring that the transformer does not saturate during the operation of the converter. A general rule of thumb is to determine turns ratio, then determine how many turns the transformer should have to create the ratio. This parameter can be determined by setting a maximum flux (B_{max}) which is to not be exceeded during operation. Generally, a B_{max} of 0.3T is the accepted maximum flux density to be had in a final design. Using this, the maximum primary turns (N_{pri}) can be found by utilizing the designed inductance, the cross-sectional area of the core (A_e), and the primary peak current ($I_{pripeak}$).

$$A_e = \frac{L_{pri} I_{pri_{peak}}}{N_{pri} B_{max}}$$

Equation 1 Cross-Sectional Area

Synchronous Rectifier

When implementing a converter with a higher output current, a synchronous rectifier (SR) can be used in place of a diode to decrease secondary losses. This decreases losses on the output proportional to the output current rating. Typically at low currents, SR's would not improve efficiency as much as at higher output currents and may be disabled up until a certain current is applied.

$$P_{diode} = V_{drop} I_{RMS} \ \ versus \ \ P_{SR} = R_{DS_{on}} I_{RMS}^2$$

Equation 2 Synchronous Rectifier Power Dissipation

Snubbers

While the primary and secondary side switches are rated for each topology, but this does not account for all of the voltage rating needed for each switch. The primary and secondary side switches will both see spiking as a result of parasitic elements from the transformer and switches. Parasitic elements are introduced by the transformer and the switches on both side of it. The transformer has a natural leakage inductance, which is the energy stored in between the windings of the transformer. The windings within the transformer stackup also introduce voltage potential differences between them, which creates a capacitance in the transformer. Within the switches, there is a dynamic capacitance rating which changes with drain to source voltage, which is the output capacitance of the MOSFET known as C_{oss}.

The primary side voltage spike can be calculated as a result of these parasitic elements along with the current passing through the switch during the turn-off.

$$V_{pri_{spike}} = I_{pri_{pk}} \sqrt{\frac{L_{pri_{leakage}}}{C_{trans} + C_{oss}}}$$

Equation 3 Primary Leakage Spike [3]

This spike introduces a design hurdle, as it can significantly increase necessary switch ratings. Traditionally, this voltage spike has been handled with the introduction of a snubber over the primary switch. A snubber is an element in the system which is intended to absorb spiking and dissipate the energy over a resistor capacitor network in order to reduce the impact on the switch. A popular and simple snubber used in flyback converters is the Resistor Capacitor Diode (RCD) snubber. [3]

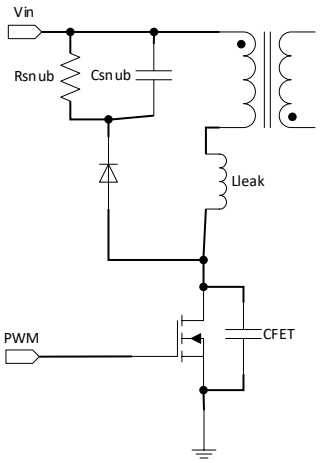

Figure 5 RCD Snubber Schematic

The RCD snubber must feature a diode rated at the same level as the primary side switch, and captures the energy from the spikes to discharge it between cycles. This behavior requires the resistor to dissipate enough power to absorb the next voltage spike.

$$R_{snub} = \frac{2V_{snub}(V_{snub} - V_{out}N_{ps})}{L_{pri_{leakage}} I_{pri}^2 f_{sw}}$$

Equation 4 RCD Snubber Resistor

The capacitor is sized to keep the ripple voltage on the clamp instead of the MOSFET.

$$C_{snub} = \frac{V_{snub}}{V_{ripple} R_{snub} f_{sw}}$$

Equation 5 Snubber Capacitor

The same method of snubbing can be taken with the secondary side MOSFET, as the voltage spike on the secondary must be dissipated as well.

$$V_{\mathrm{sec}_{spike}} = \mathrm{I}_{\mathrm{recovery}} \sqrt{\frac{L_{sec_{leak}}}{C_{oss}}} + \frac{V_{in}}{N_{ps}}$$

Equation 6 Secondary Leakage Spike

A simple RC snubber can also be used depending on the speed and the protected voltage, which would simplify the snubber design, and features one less component.

$$R_{snub_{RC}} = \sqrt{\frac{L_{leakage}}{C_{oss}}}$$

Equation 7 RC Snubber Resistor

An additional implementation concern can arise from the expected thermal rise of lossy components. Ideally in industry design, a max thermal level will be met according to design specification. During the board design stage, care must be taken to allow components the space necessary to dissipate their power into the copper planes surrounding them. This would also require possible size increases to components in order to meet expectations, or changing subsystems to increase efficiency.

Finally, system implementation can have variation and as such margin must be designed into the final specifications. As such, the final product of design equations

should not be indicative of minimum voltage or current ratings, and margin should be designed on top of the estimated values to account for variation.

USBPD Universal Board

To begin the designs, a universal daughter card for USBPD was designed for ease of use and ease of comparison. This created a known and stable platform to enable USBPD on each topology. For the purposes of the project, the USBPD controller which was chosen is the FUSB3307. This enables all of the output voltages, up to the rated power of the design. The board layout was designed to best protect the integrity of the signals, and allow for the largest possible power paths along with a condensed design on the board itself. The board connects to the motherboard of each topology through the inputs of Output Voltage, Output Ground, and the Cathode of the optocoupler.

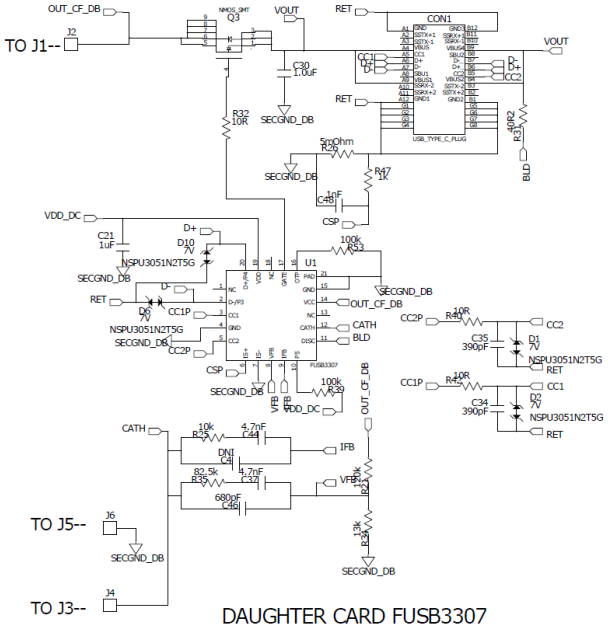

Figure 6 FUSB3307 Daughter Card Schematic

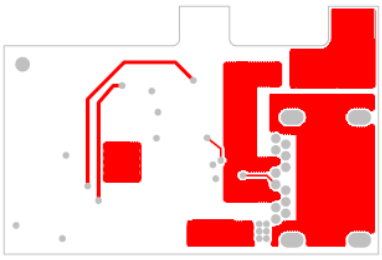

Figure 7 Bottom Layer of FUSB3307 Daughter Card

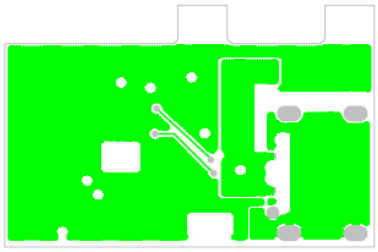

Figure 8 Inner Layer 2 of FUSB3307 Daughter Card

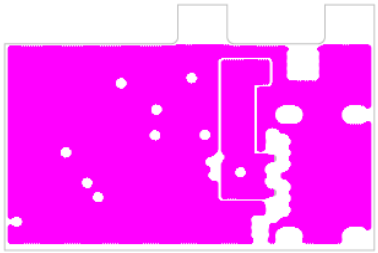

Figure 9 Inner Layer 1 of FUSB3307 Daughter Card

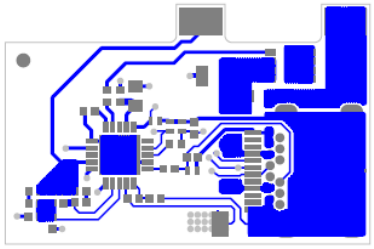

Figure 10 Top Layer of FUSB3307 Daughter Card

The biggest considerations with the layout of the daughter card come from the complexity of the USB-C port. The port features a reversible 24-pin connector, which require careful routing to ensure that signals reach the correct pin on the FUSB3307

controller. Additionally, the ground from the motherboard must maintain its isolation from the return path of the port, as the return from the port is a signal required by the controller for current sensing and limiting for the powered device.

CHAPTER 3

FIXED FREQUENCY FLYBACK

Fixed Frequency Flyback Theory of Operation

A traditional flyback converter is a system with a fixed frequency featuring a single switch. The fixed frequency aspect of the design means that regardless of the discharge of the transformer, the switch will turn on when it hits the switching time. This implementation fo a flyback converter is utilized mostly for ease of use, and it is generally the flyback which is known by theory. It works best with lower powered systems, as switching losses and snubbing losses increase with output power and system does not take into account any measures to mitigate operating losses, or any recycling of energy. The fixed frequency system is best known for simplicity and ease of implementation, as well as low cost components and smaller total component count.

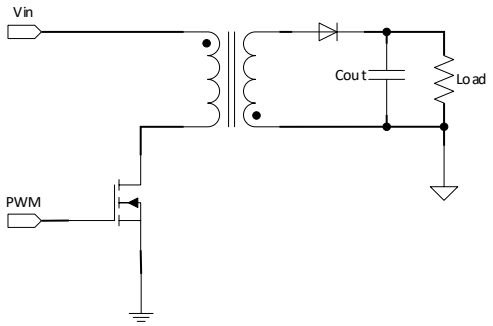

Figure 11 Generic Flyback Topology Schematic

Fixed frequency flyback converters can operate in either Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM). In DCM, the converter delivers all of the energy stored in the transformer to the secondary side during the off-cycle, then features a dead-time where the secondary current falls to zero before the next on cycle.

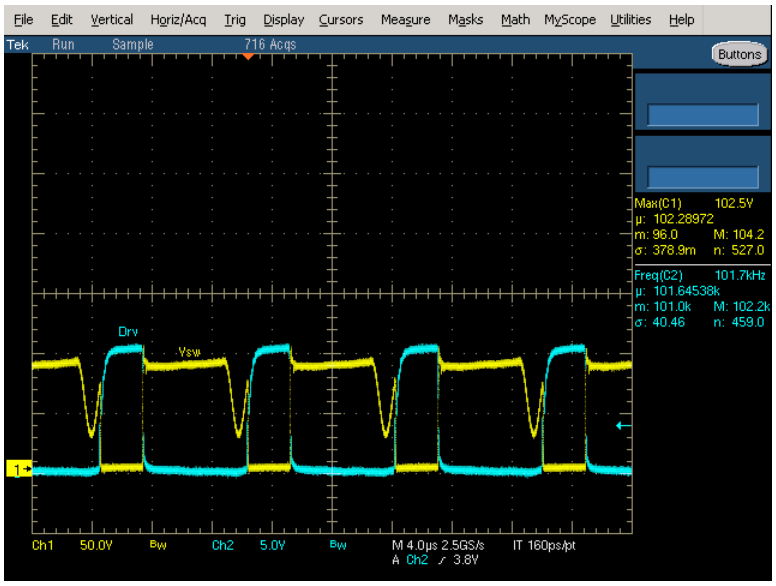

Figure 12 DCM Operation of Fixed Frequency Flyback

DCM operation allows for a lower inductance value to be used and has the by-product of zero current turn-on switching on the main MOSFET. DCM also results in higher peak currents in the primary and secondary sides, as well as increase capacitance requirements, which can increase losses over the on-cycle of the switch and increase component count.

During CCM operation, the transformer energy does not fully discharge during the off-cycle of the primary switch. This leads to no dead-time and a constant charge and discharge cycle for the transformer centered on the mean current.

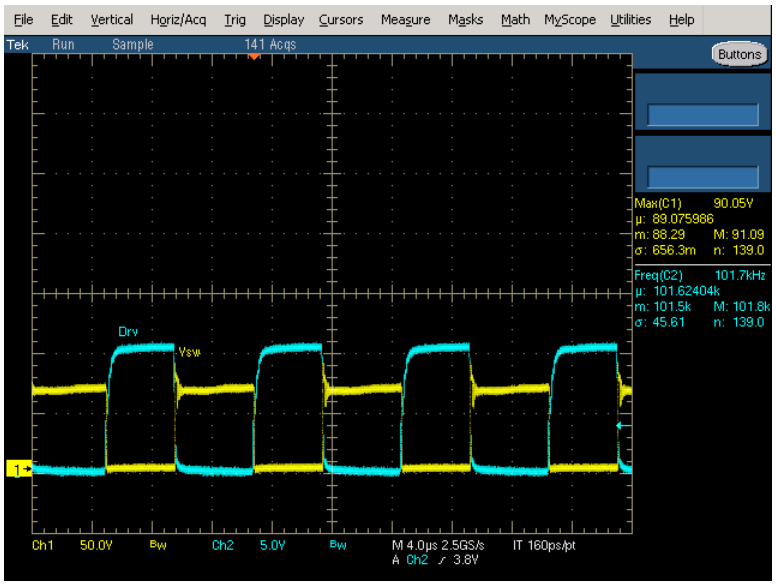

Figure 13 CCM Operation of Fixed Frequency Flyback

CCM operation features lower peak currents and lower ripple over the transformer, along with smaller input and output capacitances. CCM is offset by the need for a larger transformer and higher switching losses.

Fixed Frequency Flyback Converter Design

To begin the design of a fixed frequency flyback converter, a maximum duty cycle and turns ratio must be determined using input and output voltage.

$$\frac{V_{out}}{V_{in}} = n_{ps}\frac{D}{1-D}$$

Equation 8 Flyback Duty Cycle

One simple way to design turns ratio is to assume a duty cycle of 50%, and allow the voltage ratio of the nominal input voltage and maximum output voltage to determine the primary to secondary ratio.

$$\frac{V_{out_{max}}}{V_{in_{nom}}} = n_{ps}$$

Equation 9 Turns Ratio Estimation

Once a turns ratio is decided, maximum and minimum duty cycles can be determined for the system as well using the upper and lower bounds of input and output voltages.

One method of influencing the mode of operation to DCM or CCM is through changing of the inductance of the transformer. Due to the nature of peak-current mode control, designing a transformer with lower inductance will lead to DCM operation while designing with higher inductance will lead to CCM, as peak currents increase when inductance decreases.

$$I_{pri_{peak}} = \frac{V_{in}}{L_{pri}} D_{max} T_s$$

Equation 10 Fixed Frequency Primary Peak Current

Flyback transformer primary inductance is set according to the mode of operation and primary peak current and primary ripple current considerations. Primary peak current also reflects onto the secondary side proportional to the primary to secondary turns ratio.

$$I_{\mathrm{sec}_{peak}} = I_{pri_{pk}} N_{ps}$$

Equation 11 Fixed Frequency Secondary Peak Current

The peak currents can be used for determining losses in the system, as well as assisting with component ratings.

Having calculated the primary and secondary side currents, a secondary side capacitance can next be determined. Output capacitance has three major requirements: ripple voltage, RMS current requirement, and equivalent series resistance (ESR) limit.

The final capacitance value is chosen such that all of the requirements are met simultaneously.

Ripple voltage is determined in the specification of the design, and is given as a percentage of the output voltage.

$$\Delta V_{out} = \frac{I_{out} D T_s}{C_{out}}$$

Equation 12 Fixed Frequency Output Ripple

RMS current rating is an inherent rating to the capacitors, and must meet the requirement by the converter. The converter requires this to be met due to the current sent to the secondary side.

$$I_{Cout,RMS} = I_{out} \sqrt{\frac{D}{1 - D}}$$

Equation 13 Fixed Frequency Output Capacitor RMS Rating

ESR is another capacitor component trait, and is determined as a maximum limit that can be used to meet the specification requirements. This is set by the allowable ripple and the currents of the capacitor.

$$ESR_{max} = \frac{\Delta V_o}{I_{in} + I_{out}} \quad where \;\; I_{in} = \frac{I_{out} D}{1 - D}$$

Equation 14 Fixed Frequency Output Capacitor ESR Max

As all three of these requirements must be met, one of them will be the limiting factor on output capacitor selection. In order to meet all of them, more capacitors can be added or individual concerns may be met by changing part selection to increase capacitance per capacitor, RMS per capacitor increases, or ESR per capacitor may be reduced.

Another major component rating to take into consideration when designing a flyback converter is the voltage and current rating of the primary and secondary switches. In a flyback converter the primary side voltage rating takes into account the input voltage and the reflected voltage from the secondary side of the transformer.

$$V_{pri} = V_{inmax} + V_{outmax}N_{ps}$$

Equation 15 Primary Switch Voltage Rating

Using this same method, the secondary side rectifying voltage rating can be determined.

$$V_{sec} = \frac{V_{inmax}}{N_{ps}} + V_{outmax}$$

Equation 16 Secondary Switch Voltage Rating

The equations showcase that one of the only methods of changing the voltage rating on each switch is to change the turns ratio. Additionally, the switch current ratings must meet the peak current ratings on each side of the transformer given by $I_{pripeak}$ and $I_{secpeak}$.

Fixed Frequency Flyback Implementation Concerns

Industry available pulse width modulation (PWM) controllers utilize peak-current mode control, where the primary side inductor current is measured using a current-sense resistor to determine the on-cycle of the switch. This allows for a voltage-based signal to be sent from the secondary side to determine that the correct amount of energy is being sent over per switching cycle. For a peak-current mode controlled system with a varied output voltage the converter is ensured to operate in both DCM and CCM modes as lighter loads will ensure operation in DCM operation, while lower output voltages and

higher loads will approach CCM operation. While the design may lean closer to one mode, the system must be able to accompany both modes of operation throughout its input/output spectrum. This leads the designer to design for the maximum load point to be in DCM or CCM and have to accommodate the other load points as needed.

Additional benefits between DCM and CCM operation can be found when looking through a practical implementation. When implementing a synchronous rectifier in DCM, the SR controller will turn off the secondary side switch once the conduction of the secondary switch reaches zero. In CCM operation, the SR controller will stay on until the turn-on of the primary switch, creating a small cross-conduction window where both switches are on simultaneously, which can result in voltage spikes. This is due to the method which SR controller operates, where it detects a voltage difference over the secondary side switch in order to determine whether the switch is conducting current.

The cross-conduction introduces a power loss element, though it can be minimized with layout. The SR controller can be utilized in series of either polarity of the secondary side of the transformer, however it is generally easier to use at the low-side due to the ability to use the output voltage to power the controller. The SR controller detects the voltage of the drain and source of the secondary switch, which in the case of low-side rectification includes the transformer side, or secondary ground. When routing either of these signals during layout, care can be taken to put the signals as close as possible to the SR controller and their respective signal origins in order for the controller to have the most accurate voltage reading between drain and source of the switch. This will allow for the best detection time for when the primary switch has turned on, and will

therefore result in the best turn-off time of the SR switch, minimizing cross-conduction losses.

Fixed Frequency Flyback Expected Losses

Predicted efficiency within a converter can help the designer gain insight into how well a system will perform, and once it is operational, whether something is not working as intended. While there are many small loss elements within a converter, the main elements of loss are identifiable from the rest in a given design. The best assumption on efficiency to make would be during the worst cases possible, which would be given during minimum input voltage, maximum output voltage, at max output current.

Losses in a flyback converter begin with currents. While peak currents are used for component ratings, RMS currents are used to calculate losses. The RMS currents do utilize peak currents in their calculations though.

$$I_{priRMS} = I_{pri_{peak}}\sqrt{D}$$

Equation 17 Fixed Frequency Primary RMS Current

Where $I_{pripeak}$ is derived from EQUATION NUMBER, and the duty cycle of the converter is designed to be 50%. Secondary RMS current is directly proportional to the turns ratio of the transformer.

$$I_{secRMS} = I_{priRMS}N_{ps}$$

Equation 18 Fixed Frequency Secondary RMS Current

Switch losses are a large part of calculating efficiency in a fixed frequency flyback design. These come in the form of conduction losses of the MOSFET, and the losses related to switching the MOSFET on and off.

Utilizing the RMS currents on the primary and secondary side of the system, the losses within the conduction of the MOSFETs can be calculated for both primary and secondary sides. These are proportional to the R_{DSon} of the MOSFET, found in the datasheet for the given component. For the primary side, FDMS86255 has a 12.4mΩ resistance, and the secondary side FDMS86202 has 7.2mΩ.

$$P_{pri_{FETConduction}} = R_{DS_{onPRI}} I_{priRMS}^2$$

Equation 19 Primary Switch Conduction Loss

$$P_{sec_{FETConduction}} = R_{DS_{onSEC}} I_{secRMS}^2$$

Equation 20 Secondary Switch Conduction Loss

After the conduction losses of the MOSFET come the losses involved in switching the MOSFET on and off. This encompasses the V_{DS} of the MOSFET and the drain current of the MOSFET cross conducting for a short period of time during the turn on and the turn off, known as hard-switching, along with the actual power needed to turn on the switch. In order to determine an estimate for the cross conduction on the switches, a cross-conduction time must be determined using the characteristics of the chosen switch.

Ciss	Coss	Crss	g	Vth	Rg
3200 pF	291 pF	11 pF	35 S	3 V	0.7 Ω

Table 2 FDMS86255 Specifications

These characteristics are then used to determine the turn on and turn off time of the switch. For the system, a gate resistor of 47Ω is also used between the drive signal and the gate of the MOSFET. Assuming CCM operation, the first time to calculate is the time for current to reach the gate to begin turning on the switch. [4]

$$T1_{on} = -R_{gate}C_{iss}\ln\left(1 - \frac{\frac{I_{out}N_{ps}}{1-D}}{g(V_{drive} - V_{th})}\right)$$

Equation 21 Cross Conduction On Time 1

The second time during the turn on period comes from the time for voltage to reach the gate.

$$T2_{on} = \frac{V_{DS}R_{gate}C_{rss}}{V_{drive} - \left(V_{th} + \frac{\frac{I_{out}N_{ps}}{1-D}}{g}\right)}$$

Equation 22 Cross Conduction On Time 2

The calculated times are then used to estimate the primary cross-conduction losses.

$$P_{sw_{on}} = \frac{1}{2}V_{DS}\frac{I_{out}N_{ps}}{1-D}f_{sw}(T1_{on} + T2_{on})$$

Equation 23 Cross Conduction Turn On Loss

The second part of the switching losses from the primary side comes from the turn-off period. This is calculated as the time it takes to turn off the switch, and is when the voltage across the MOSFET is rising while the current is active. The time taken to transmit the current to the MOSFET is the first time.

$$T1_{off} = R_{gate}C_{iss}\ln\left(\frac{\frac{\frac{I_{out}N_{ps}}{1-D}}{g} + V_{th}}{V_{th}}\right)$$

Equation 24 Cross Conduction Off Time 1

The second timing is how long it takes to transmit voltage.

$$T2_{off} = \frac{V_{DS} C_{rss} R_{gate}}{V_{th} + \frac{\frac{I_{out} N_{ps}}{1 - D}}{g}}$$

Equation 25 Cross Conduction Off Time 2

Using the same formula for the turn off as the turn on, the power can be estimated again.

$$P_{sw_{off}} = \frac{1}{2} V_{DS} \frac{I_{out} N_{ps}}{1 - D} f_{sw} \left(T1_{off} + T2_{off} \right)$$

Equation 26 Cross Conduction Turn Off Loss

And total switching losses can be calculated as the sum of the turn on and turn off losses.

One element which features high relative losses in the flyback design is the transformer. The transformer can be broken up into two different types of losses: conduction losses, and core losses.

Conduction losses in the transformer are caused by the resistance of the windings of the transformer. This means that the design would want to utilize the most copper possible in order to wind the transformer to meet specifications in order to decrease the resistance. There are two types of losses associated with conduction losses, DC losses and AC losses. While DC losses would point to using one larger AWG wire to maximize the possible utilization area, due to capacitance and high frequency interaction between the windings, many smaller windings will want to be used in parallel, known as litz wire. This can reduce AC losses and allow for a simpler DC based estimation.

$$P_{conduction} = R_{DC} I_{RMS}^2$$

Equation 27 Transformer Conduction Loss

For the final version of the transformer, 10 primary windings were used and 5 secondary windings. The DC resistance for these were 36mΩ for primary and 20mΩ for secondary.

The core losses for the transformer come from the steinmetz equation typically, however the chosen core by Hitachi Metals includes a modified Steinmetz equation to calculate losses. The modified equation features the parameters of P_{core} as core loss in kW/m^3, K_h as a hysteresis loss function, K_e eddy current loss coefficient, B_m as magnetic flux density in Teslas, and X as exponent. [12]

$$P_{core} = (K_h f_{sw} + K_e f_{sw}^2) B_m^x$$

Equation 28 Transformer Core Loss / Volume

Given the core material of ML29D, the parameters are given between the frequencies of 50kHz and 250kHz.

K_h	K_e	X
0.1035	7.178E-07	2.323

Table 3 Hitachi Metals ML29D Ferrite Material Specifciations

Magnetic flux density is then calculated as a function of the number of primary turns, the primary inductance, the peak currents on the primary side, and the cross-sectional area of the transformer.

$$B_{max} = \frac{L_{pri} I_{pri_{peak}}}{N_{pri} A_e}$$

Equation 29 Max Flux Density

Using these equations, the core power loss in the transformer can be calculated.

$$P_{RM8LP} = P_{core} V_{core}$$

Equation 30 Transformer Core Loss

Total losses in the transformer can be calculated as the sum of conduction and core losses.

Losses within a fixed frequency flyback are focused within the switches and transformer mainly, however those aren't the only lossy elements in the topology. One additional loss element of the system comes from the output capacitors. The losses over output capacitors comes from the current entering and exiting the capacitors, along with the ESR of the chosen capacitors. The capacitors chosen for the system feature 15mΩ capacitance, and with two of them this equates to 7.5mΩ.

$$P_{Cout} = I_{secRMS}^2 ESR$$

Equation 31 Output Capacitor Loss

The final major loss component in the Fixed Frequency flyback system comes from the snubber. A snubber in Fixed Frequency flyback is just an instrument to dissipate extra power, and is therefore a purposefully lossy subcircuit. [3]

$$P_{snub} = \frac{1}{2} V_{snub} I_{snub} t_{spike} f_{sw}$$

Equation 32 Snubber Loss

$$t_{spike} = \frac{L_{prileak} I_{pri_{peak}}}{V_{snub} - V_{out} N_{ps}}$$

Equation 33 Time of Voltage Spike

All major losses total together against output power rating give the estimated efficiency.

P_{priFET}	P_{secFET}	$P_{transformer}$	P_{cout}	P_{snub}	Total
704 mW	547 mW	3.97 W	570 mW	185 mW	5.976 W

Table 4 Estimated Losses of Fixed Frequency Flyback

And total efficiency can be gained as a function of rated output power versus total loss.

$$Efficiency_{estimate} = \frac{P_{out}}{P_{out} + Loss}$$

Equation 34 Efficiency Equation

This leads to a final efficiency estimate of 88.3% for the fixed frequency flyback.

Fixed Frequency Flyback Converter Schematic

With the major components designed for the fixed frequency flyback, a schematic can be created.

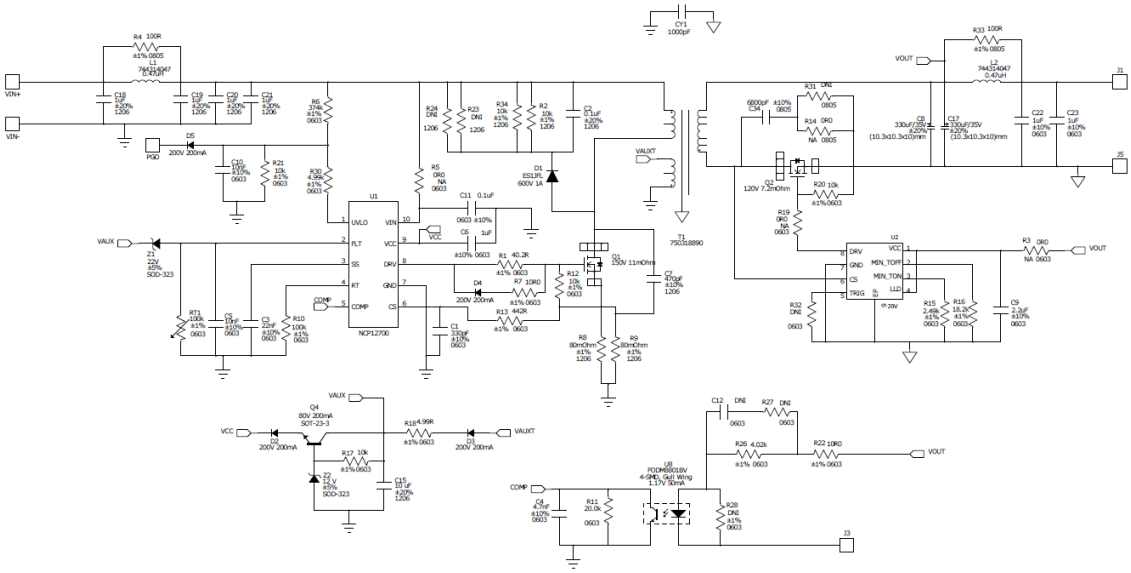

Figure 14 Fixed Frequency Flyback Converter

The original schematic for the fixed frequency flyback converter changed between instantiation and implementation. Future designs required the changing of the current sense resistors into a current sense transformer. This meant air-wiring some components into the current sense pin to get the best comparisons. Additionally, the

output capacitors were changed into lower ESR capacitors to better match the other designs.

Fixed Frequency Flyback Converter Layout

For the fixed frequency flyback system, the layout is mainly focused on attempting to keep the thermals of the primary side switch and the primary snubber as low as possible. This was done by increasing the copper area around the components which have the largest losses associated with them. With this in consideration the final layout is very copper heavy, even though components are low. The switch used is only 5 mm x 6 mm, however the area around it is almost four times the size in order to attempt to sink as much heat as possible. Vias are used to join the 4 layers together for thermal dissipation throughout the maximum possible copper space within the board.

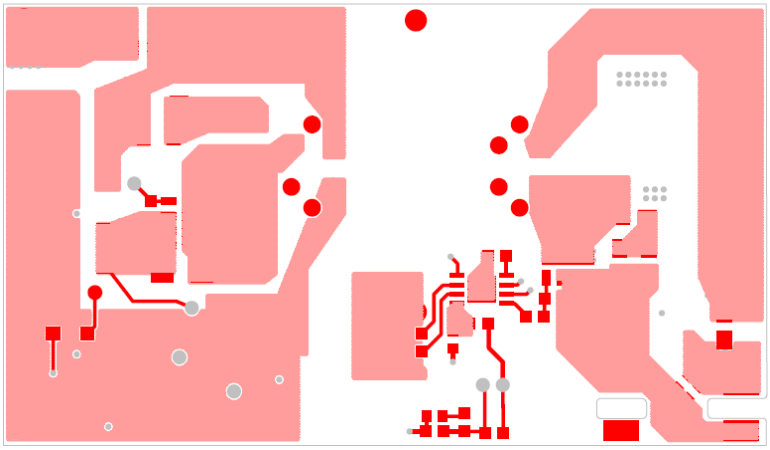

Figure 15 Bottom Layer of Fixed Frequency Flyback Layout

The bottom layer of the board features the SR controller, feedback resistors, additional primary side routed signals, and more thermal planes for power nodes.

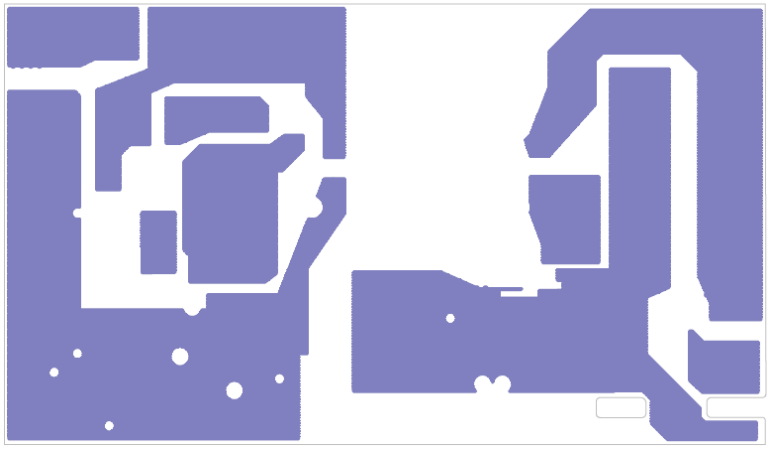

Figure 16 Inner Layer 2 of Fixed Frequency Flyback Layout

Inner layer 2 features additional copper planes for thermal dissipation across all the components, and is used for signal integrity from noise sources.

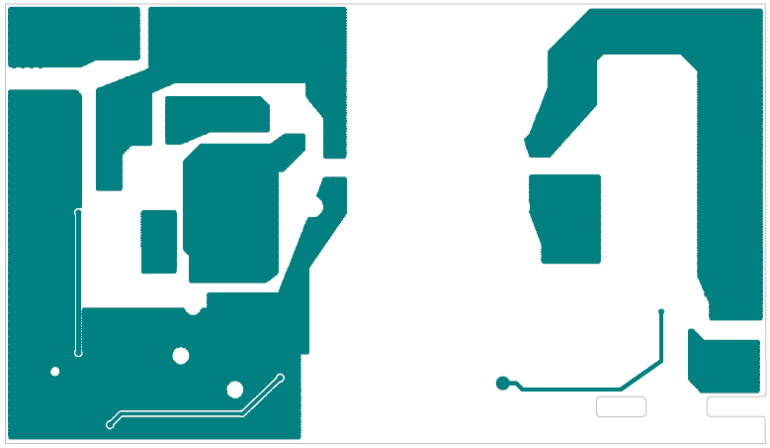

Figure 17 Inner Layer 1 of Fixed Frequency Flyback Layout

Inner layer 1 features additional copper for the power signals, the primary side ground plane, and the output voltage signal to the feedback system and the input voltage system.

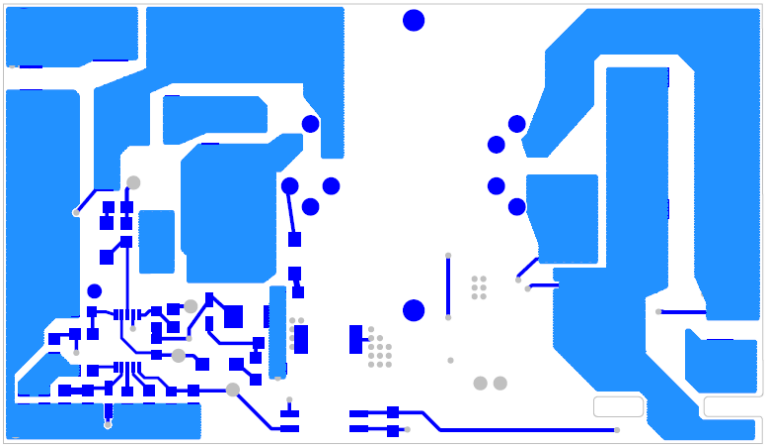

Figure 18 Top Layer of Fixed Frequency Flyback Layout

The top layer of the design features the primary and secondary switches, as well as the controller and local resistors and capacitors. This layer is also where the tall standing components are placed, as they should all be on the same side of the board for power density.

The final dimensions of the board were mostly limited by the sizable components in the case of the fixed frequency flyback, as the transformer required substantial board space.

Fixed Frequency Flyback Results

With the systems major components designed and the implementation concerns taken into consideration, the board was developed.

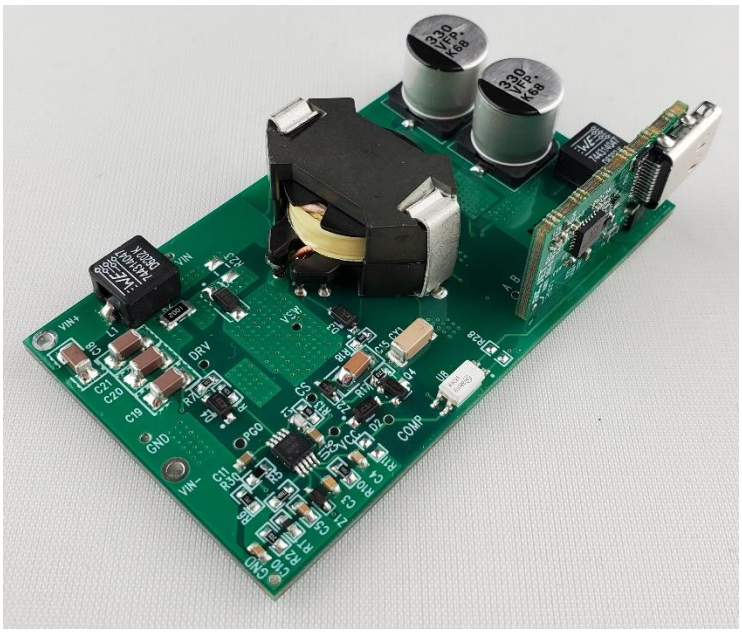

Figure 19 Assembled Board Picture of Fixed Frequency Flyback

The initial layout was changed for the final implementation, as a future design required switching from current sense resistors to current sense transformers, and the final capacitors changed from 330 µF each to 470 µF each. The changes to the final board were implemented to better match the additional topology designs, as controllers limited the potential use of current sense resistors, and lower ESR output capacitors were later used.

The system utilizes the standard USBPD protocol, which enables a default voltage of 5 V. This protocol then allows the sink device to communicate its requested voltage to the power supply, which the power supply then supplies up to its capabilities. With the system operational, the steps to check output voltages and efficiency can be taken in rising order. Care is taken at this step to ensure all subcircuits are operational at all output voltages, as without proper design to V_{cc} subcircuits it is possible to lapse power to the system with output voltage varying from 5 V to 20 V. It is also possible to supply too

much voltage and damage the subsystems or IC's, so voltages across the system must be monitored when verification takes place.

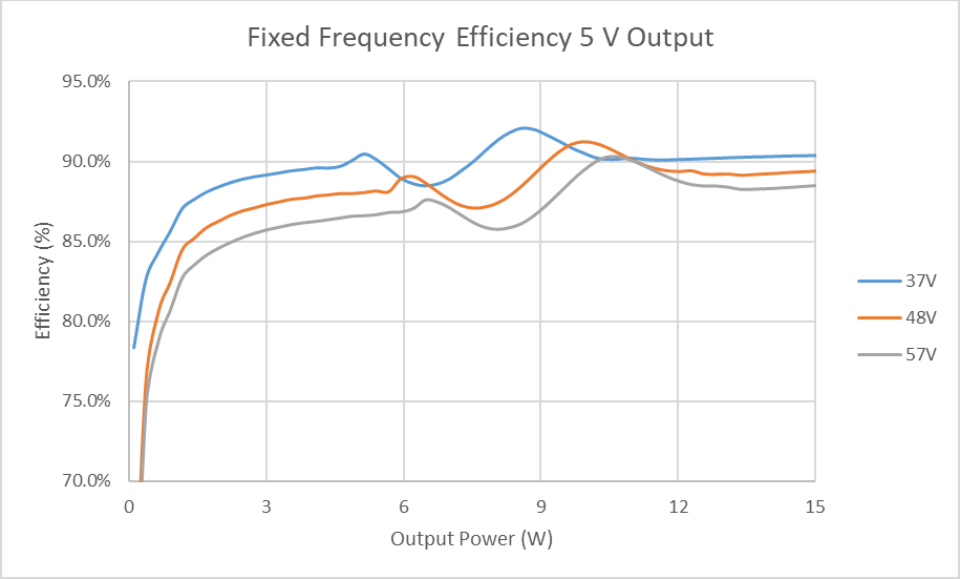

Figure 20 Efficiency Plot 5 V Output Fixed Frequency Flyback

37 V Input	48 V Input	57 V Input
90.4 %	89.4 %	88.5 %

Table 5 Full Load Efficiency 5 V Output Fixed Frequency Flyback

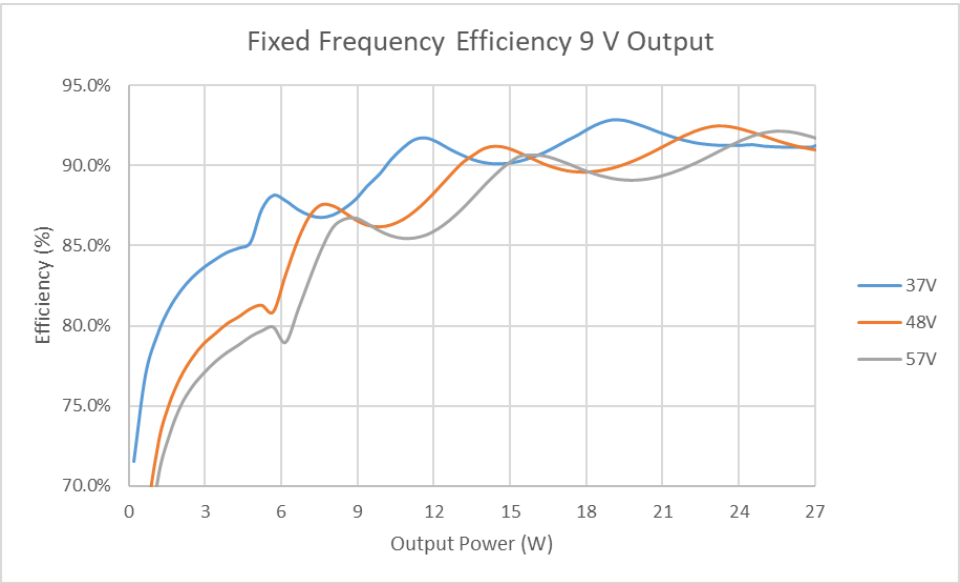

Figure 21 Efficiency Plot 9 V Output Fixed Frequency Flyback

37 V Input	48 V Input	57 V Input
91.2 %	91.1 %	91.8 %

Table 6 Full Load Efficiency 9 V Output Fixed Frequency Flyback

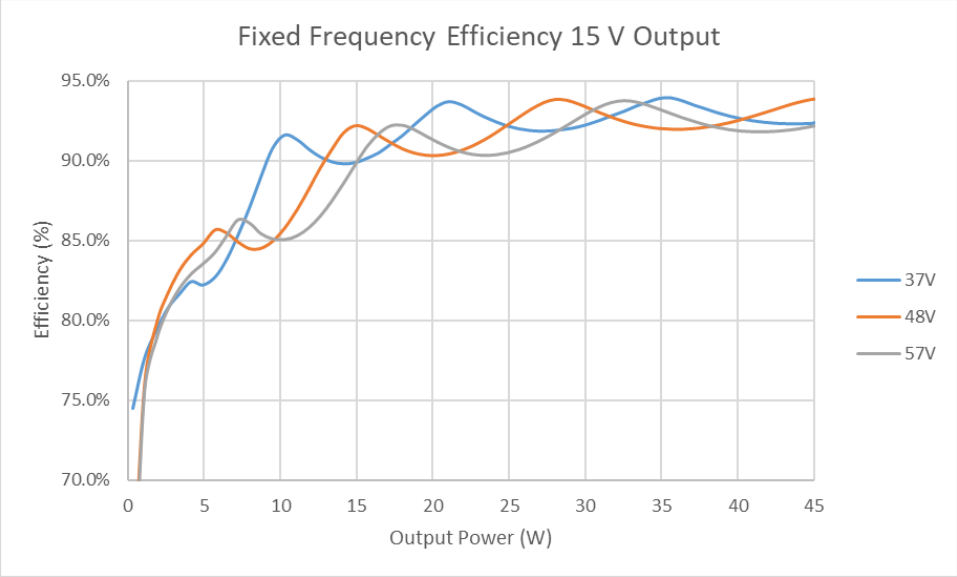

Figure 22 Efficiency Plot 15 V Output Fixed Frequency Flyback

37 V Input	48 V Input	57 V Input
92.3 %	93.8 %	92.1 %

Table 7 Full Load Efficiency 15 V Output Fixed Frequency Flyback

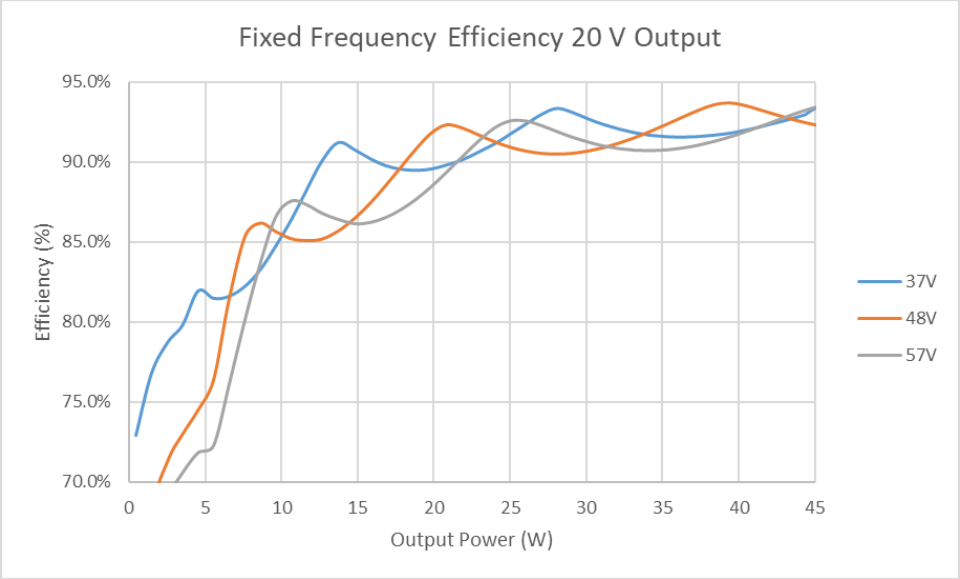

Figure 23 Efficiency Plot 20 V Output Fixed Frequency Flyback

37 V Input	48 V Input	57 V Input
93.0 %	92.2 %	93.5 %

Table 8 Full Load Efficiency 20 V Output Fixed Frequency Flyback

The final efficiency of the board can be seen in the above plot, at the predicted load point. Final efficiency of the board was then taken from the input of the board to the output of the board. In USBPD specification, due to the non-attached cable the efficiency does not have to be taken at the end of the cable. This means that the direct output voltage of the board is the efficiency, not the final seen voltage at the sink.

The 37 V input 20 V output full load efficiency of the Fixed Frequency design comes out to 93%. There is a discrepancy between the predicted efficiency and the final efficiency, which can be explained through the final system results.

To start, when looking at the final system efficiency above, some peaks and valleys can be seen in the results. This is due to the DCM operation of the system, and where the switch is turning on. During the valley of efficiency, the system is turning on at

the height of the ring in DCM, causing the most switching losses. The inverse is true for the peak, where the switch turns on during the valley. The final efficiency of the system was estimated using CCM operation. It was anticipated that at peak load and minimum input voltage the system would be operating in CCM given the system components chosen, however this was not the case. At the highest load the system was operating in DCM nearing CCM operation, which allowed for the inductor current to reach zero and the voltage on the drain to ring down closer to zero, which effectively benefited from a lower voltage turn-on condition, lower peak currents of CCM, and zero current switching. This effect could be seen to increase efficiency during peak operating condition, and improves efficiency.

Additionally, the transformer is another spot of improved efficiency. To achieve precise inductance in the transformer during the build, an airgap was introduced in the center leg of the core to reduce final inductance while utilizing the same turns ratio. An airgap serves two functions, and while one is to help gain the precise inductance to be introduced into the system, it also lowers the slope of the B-H curve of the core. This means that the predicted B_{max} has ended up being greater than in reality. As the transformer was a large element of loss stemming from the flux density introduced into the element, even a small difference in flux density can have a large difference in the final core losses. If the introduced airgap lowered B_{max} by 50%, the core power would decrease by up to 80%. [5]

In addition to the efficiency, thermals need to be taken into account throughout the operating range. While the design is more efficient than estimates would have shown, the power dissipated in the system is still focused in a few key components.

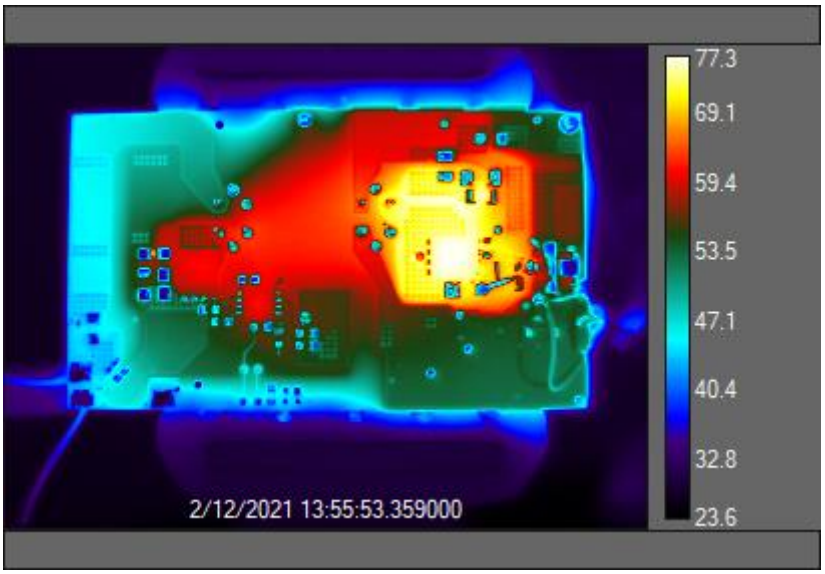

Figure 24 Thermal Image 37 Vin Full Load Bottom Fixed Frequency Flyback

Pri FET	Snubber	Sec FET
77.29 °C	75.94 °C	60.13 °C

Table 9 Temperatures 37 Vin Full Load Bottom Fixed Frequency Flyback

The bottom side thermal capture of the board shows the primary FET and the snubber as the hottest components. The snubber heat and lack of secondary FET heat would contradict the loss estimates, and say that potentially the RMS currents on the secondary are less than anticipated and that the leakage characteristics of the system which contribute to snubber losses are higher than estimated.

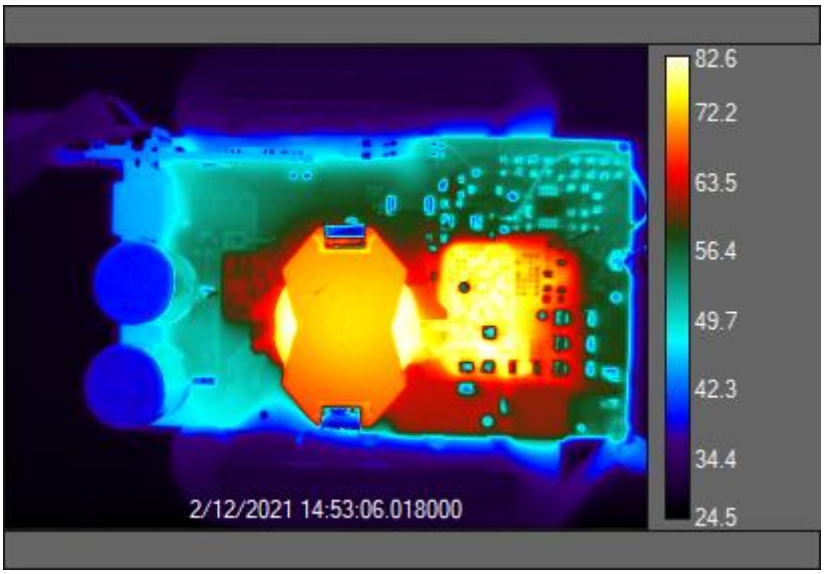

Figure 25 Thermal Image 37 Vin Full Load Top Fixed Frequency Flyback

Transformer Core	Windings
71.32 °C	82.55 °C

Table 10 Temperatures 37 Vin Full Load Top Fixed Frequency Flyback

The thermal images of the top of the board at the minimum input voltage and maximum power show that the major components dissipating power are the the transformer and the snubber. Furthermore, the major source of heat in the transformer can be seen as the windings, which could indicate higher losses in the windings than the core.

As the efficiency changes over the range of input voltage, the thermal characteristics change over the course as well.

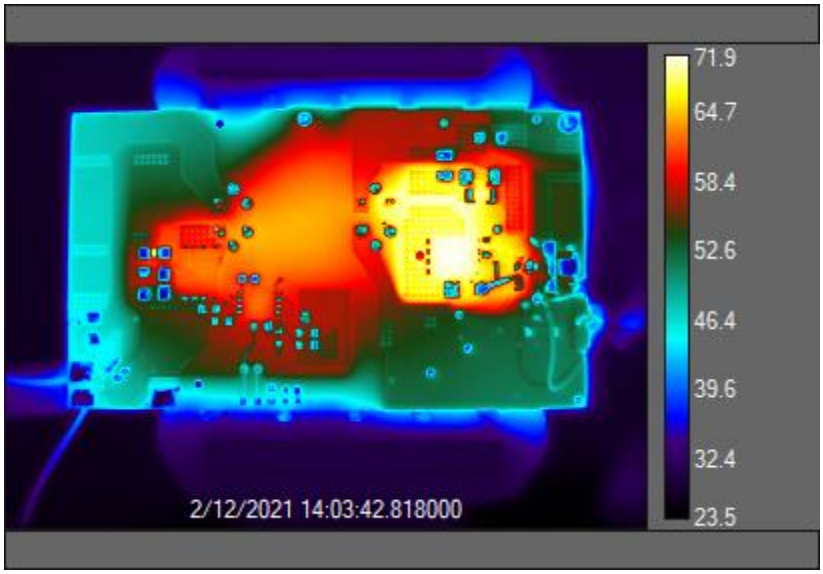

Figure 26 Thermal Image 57 Vin Full Load Bottom Fixed Frequency Flyback

Pri FET	Snubber	Sec FET
71.89 °C	70.55 °C	62.25 °C

Table 11 Temperatures 57 Vin Full Load Bottom Fixed Frequency Flyback

The bottom side of the board at 57 V full load shows a much cooler snubber and primary side FET. This coincides with the lower losses seen in Figure 21.

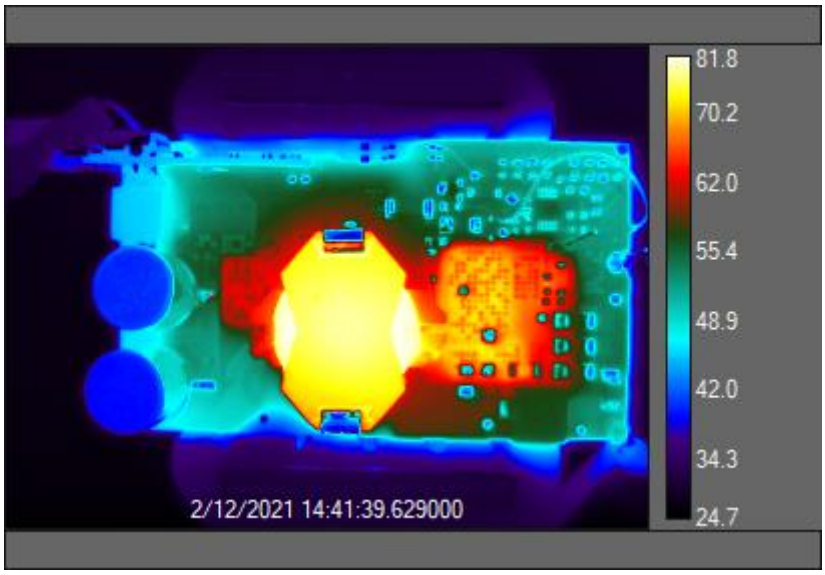

Figure 27 Thermal Image 57 Vin Full Load Top Fixed Frequency Flyback

Transformer Core	Windings
76.48 °C	81.83 °C

Table 12 Temperatures 57 Vin Full Load Top Fixed Frequency Flyback

On the top side of the board, the transformer and windings have decreased in temperature as well.

At maximum input voltage, the temperature of the primary FET decreased, even with a higher input voltage. The reason for this is that at the highest output power, the system was achieving valley switching at 57 V, while it was switching closer to a peak at 37 V.

An additional piece of USBPD implementation is the ripple specification to be met. The ripple is met by output capacitance choice, between ESR and total capacitance used. The most difficult point to meet the ripple specification is generally at minimum output voltage, maximum input voltage.

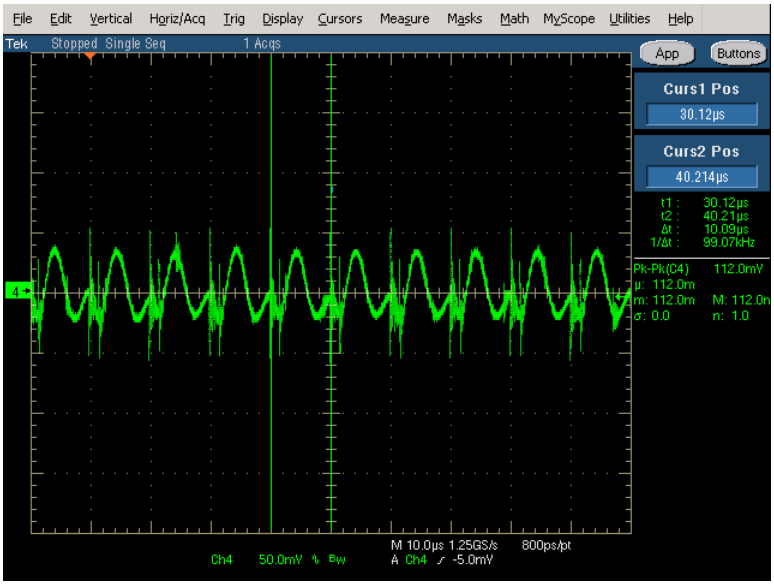

Figure 28 Ripple Capture 57 Vin 5 V / 3 A Output Fixed Frequency Flyback

As shown in the waveform, the total ripple for 57 V input 5 V output at maximum current is 112 mV, which is a 2.24% total ripple, and is within the ±5% specification for USBPD standards.

Overall, the final implementation of the fixed frequency flyback converter has exceeded the expectations set during the design stage by final implementation changes. Losses were saved on the primary MOSFET and the transformer. As these were the biggest loss mechanisms in the system, changes which benefit these losses will naturally have the biggest impact on efficiency.

CHAPTER 4

QUASI-RESONANT FLYBACK

Quasi-Resonant Flyback Theory of Operation

The Quasi-Resonant (QR) flyback is a refined variation of the traditional flyback converter, instead of operating with a fixed frequency the converter varies its frequency to keep in DCM throughout the operation range. In DCM parasitic elements attached to the switch node cause a ring after the conduction period of the secondary side, which the QR converter uses to enable valley switching. Valley switching benefits the design through reduced switching losses, which reduces thermal stress on the MOSFET and increases efficiency of the system. The major distinction with a QR when compared to a fixed frequency design is that the turn on is determined by the valley of the switch node instead of a fixed time, which causes a variable frequency as load increases and results decreased switching losses from the valley switching.

The NCP1342 controller which was chosen for this design can function from 1st to 6th valley during operation. Using the system feedback voltage, the controller will determine the optimal valley to switch in at each operating point, ensuring hysteresis between valleys in order to not overlap valleys at any given point. [6]

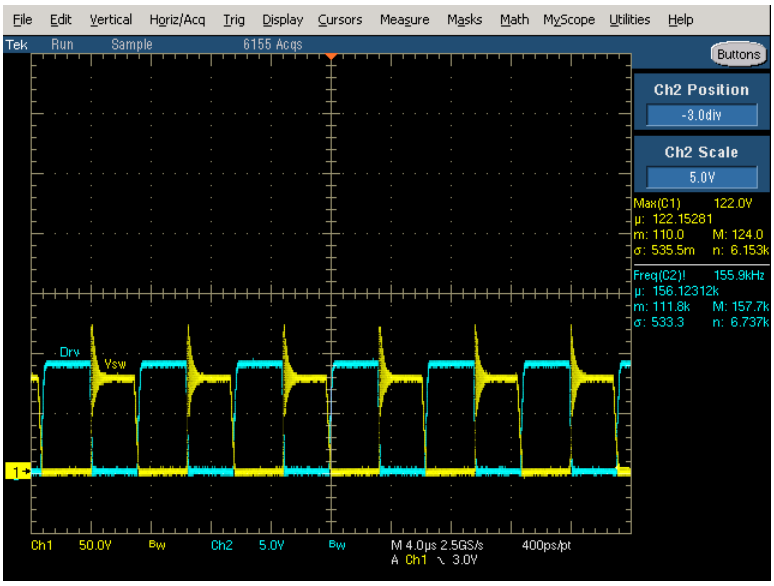

Figure 29 1st Valley Operation QR Flyback

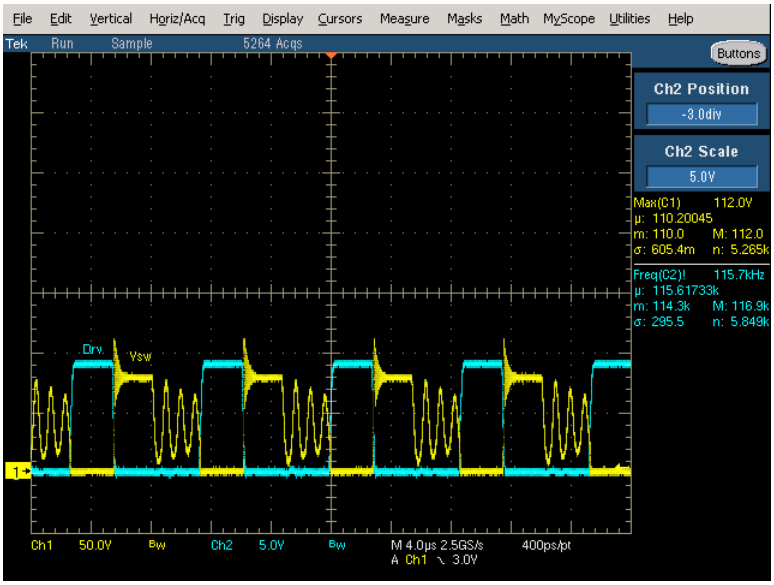

Figure 30 4th Valley Operation QR Flyback

With each valley of operation the V_{ds} at turn on changes. As the operating valley approaches first valley, the converter switches as the minimum turn on voltage, which increases with each subsequent valley of operation as the ring dampens.

Quasi-Resonant Flyback Converter Design

The QR converter design begins with choosing a turns ratio. The same method as fixed frequency can be used to determine this ratio, as shown in Equation 9. Following this calculation, it is important to declare a maximum operating frequency and an estimated efficiency to help set the peak current. For this design 150 kHz was used as a maximum frequency and 92% was estimated as the peak efficiency which can be used to determine the peak current and calculate a primary inductance. The estimated efficiency is not intended to be the final efficiency, but is used to aid in the design of the system.

$$I_{pk_{pri}} = \frac{2P_{out}}{\eta}\left(\frac{1}{V_{inmin}} + \frac{1}{N_{ps}V_{out}}\right) + \pi\sqrt{\frac{2P_{out}C_{oss}F_{swmax}}{\eta}}$$

Equation 35 QR Primary Peak Current

$$L_{pri} = \frac{2P_{out}}{I_{pk_{pri}}^2 \eta F_{swmax}}$$

Equation 36 QR Primary Inductance

The duty cycle and RMS currents can then be estimated from this to help calculate output capacitance.

$$D_{max} = \frac{I_{pk_{pri}}L_{pri}F_{sw}}{V_{inmin}}$$

Equation 37 QR Duty Cycle Max

$$I_{RMS_{pri}} = I_{pk_{pri}}\sqrt{\frac{D_{max}}{3}}$$

Equation 38 QR Primary RMS Current

$$I_{RMS_{sec}} = I_{pk_{sec}}\sqrt{\frac{1 - D_{max}}{3}}$$

Equation 39 QR Secondary RMS Current

Where I_{pksec} is the same as the fixed frequency calculation given by Equation 11. Using these, a maximum output capacitor ESR and RMS rating can be determined.

$$ESR_{max} = \frac{\Delta V}{I_{pk_{sec}}}$$

Equation 40 QR Output Capacitor ESR Max

$$I_{C_{rms}} = \sqrt{I_{RMS_{sec}}^2 - I_{out}^2}$$

Equation 41 QR Output Capacitor RMS Current Rating

And output capacitance can be calculated through Equation 12. Similarly, switch ratings can be given through the peak currents calculated above, and the voltage ratings as shown in Equation 15 and Equation 16. [7]

Quasi-Resonant Implementation Concerns

One of the benefits of QR flyback is the ease of implementation. The inductance is designed based on the desired operating frequency, and the controller keeps the system in DCM surrounding that value. Since the system is constantly in DCM, the SR and primary switch do not cross conduct as the secondary current will always reach zero before the next on time.

As with the fixed frequency design, one concern to keep in mind is to include a snubber to absorb the rings from the C_{oss} and L_{leak} on the primary side. The values for the snubber in the QR flyback converter can be calculated with the same methods as used in the fixed frequency using Eqautions 3, 4, and 5.

Quasi-Resonant Flyback Expected Losses

The losses in the QR are expected to be lower than the losses in the fixed frequency design, as the design is always meant to be valley switching and should not feature any cross-conduction. The losses in the switch of the QR system is minimized as the V_{ds} of the switch during turn on should be low by design.

$$P_{sw_{on}} = \frac{1}{2}\left(V_{in} - V_{out}N_{ps}\right)^2 C_{oss}F_{sw}$$

Equation 42 QR Turn On Loss

$$P_{sw_{off}} = \frac{I_{pk_{pri}}\left(V_{in} + V_{clamp} + V_{out}N_{ps}\right)F_{sw}t_{off}}{6}$$

Equation 43 QR Turn Off Loss

The conduction of the primary switch is calculated using Equation 19, and secondary is with Equation 20. [7]

The transformer losses in the system can be calculated using the same method as fixed frequency flyback. The final wound transformer featured a primary resistance of 25 mΩ, and a secondary resistance of 14 mΩ. Transformer conduction losses are estimates with Equation 27, and core losses with Equation 28 and Equation 30.

Losses through the snubber in the system can be estimated with Equation 32.

The losses in the output capacitor are calculated with Equation 31.

Pri FET	Sec FET	XFMR	Cout	Snub	Total
127 mW	191 mW	2.713 W	113 mW	461 mW	3.605 W

Table 13 Estimated Losses of QR Flyback

The total loss of 3.605 W puts the system efficiency estimate at 92.6% at low line full load.

Quasi-Resonant Flyback Converter Schematic

After the major component calculations and implementation based considerations, the QR converter schematic can be designed. Similar to the fixed frequency system, the converter features all the major systems with setting resistors, and local decoupling capacitors.

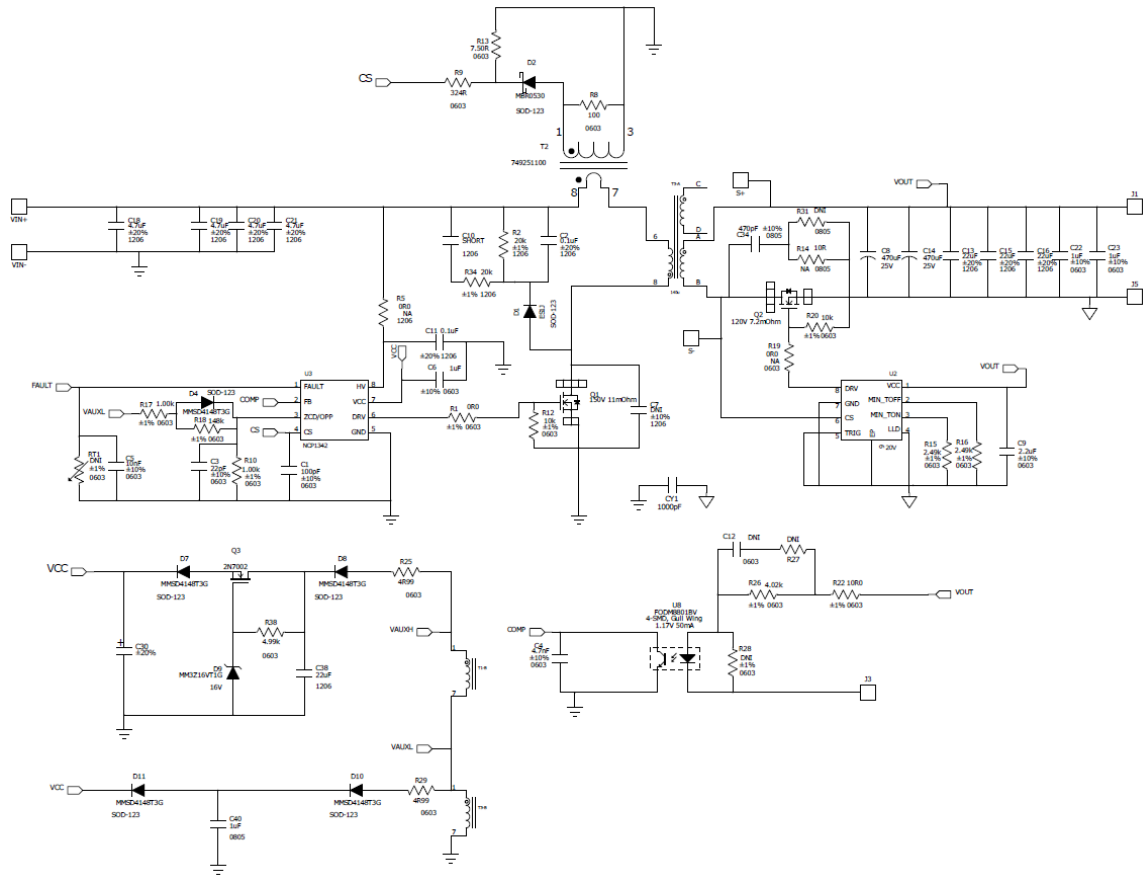

Figure 31 QR Flyback Schematic

Quasi-Resonant Flyback Converter Layout

In the QR system, the layout was made to accommodate the most copper in the primary and secondary power paths. As with the fixed frequency board, signaling was placed in the bottom half of the design, and a ground plane was places in the middle

layers to attempt to protect sensitive signals from the switch node and other noise. The main power dissipation mechanisms in this system are the snubber, the switch, and the secondary switch. Because of this the bulk of the copper is made to surround these components. The current sense signal comes from above the primary switch, and as such is routed below a ground plane, and in between more ground planes on the same layer as to prevent the impact of the switch node noise.

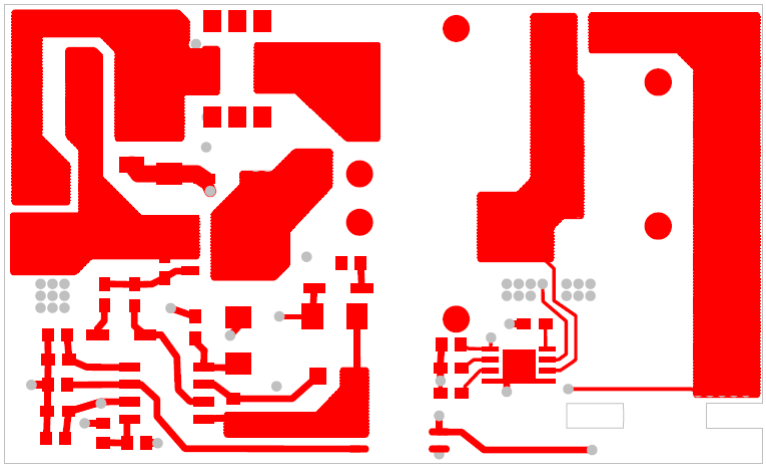

Figure 32 Bottom Layer of QR Flyback Layout

The bottom layer is where the primary controller, primary switch, and SR controller are placed. In addition, the standing components of the board, like output capacitors, transformer, and daughter card are all standing on the bottom layer.

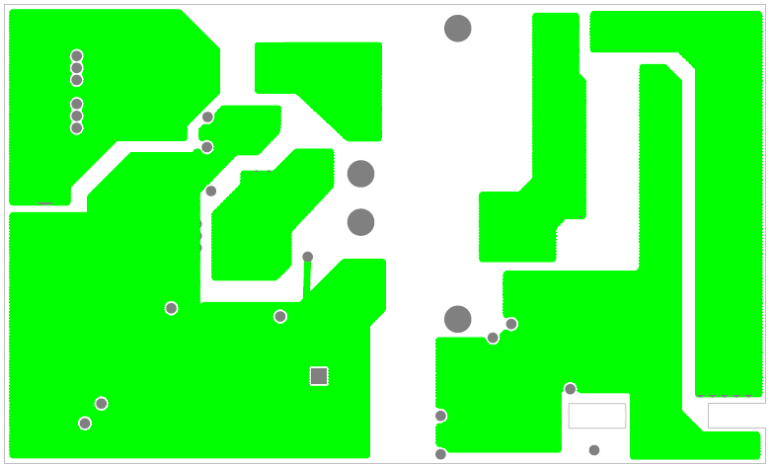

Figure 33 Inner Layer 2 of QR Flyback Layout

Inner layer 2 is a copper planes layer, to assist with thermals and signal integrity.

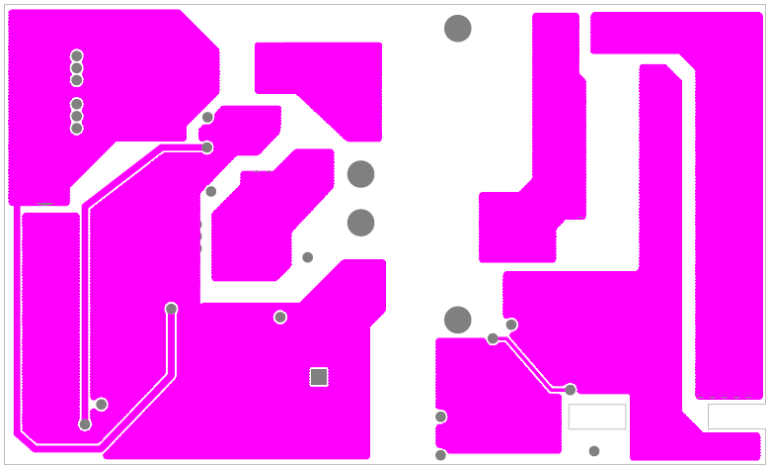

Figure 34 Inner Layer 1 of QR Flyback Layout

Inner layer 1 is a copper plane layer to assist with thermals and signal integrity, but also features the input voltage to controller and the CS signal routing underneath and in between the ground planes.

Figure 35 Top Layer of QR Flyback Layout

The top layer is mainly housing the VCC circuit and the secondary FET, as well as more copper planes for the power paths.

Quasi-Resonant Flyback Results

The final winding of the transformer only allowed for four pins on the primary side, while five were necessary due to the split VCC structure. While in the other designs the transformer bobbin had six primary pins, on this one a flying lead was used on the primary side for the fifth lead. This enabled the lead to be attached anywhere on the board, and was attached directly to a resistor on the primary side aux circuit. As one flying lead was already used, the design also utilized flying leads on the secondary side of the transformer for flexible routing of the secondary windings.

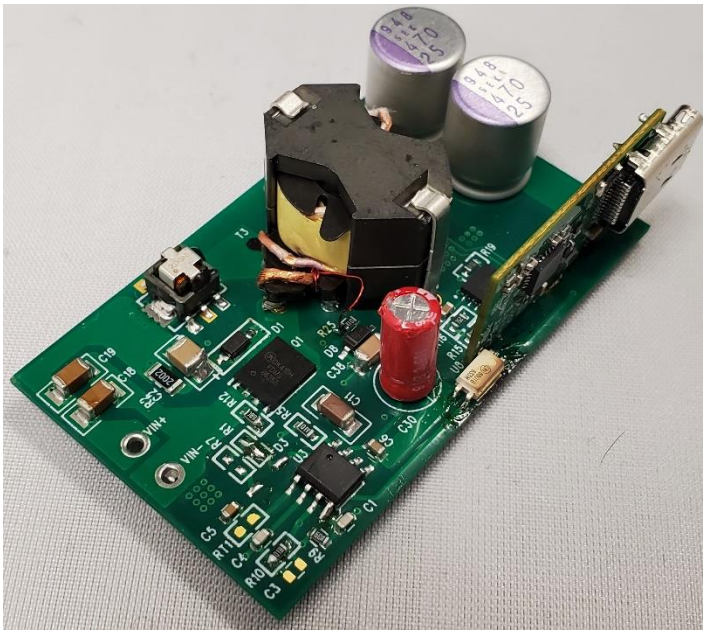

Figure 36 Assembled Board Picture of QR Flyback Board

This layout was unchanged in the assembly phase, as the initial design worked for its intended purpose and universal changes were made prior to the layout of this board.

As with the fixed frequency design, care is taken to ensure subsystem functionality during startup. The biggest subsystem verification with these board is the primary V_{CC} management, which the same system was used as from the fixed frequency design. The prior design experience and utilizing the same aux winding ratio ensures that this step is a quick verification for the consecutive designs.

The board still starts up at 5 V, and USBPD communication then cycles it through the consecutive voltages to check efficiency across the output range.

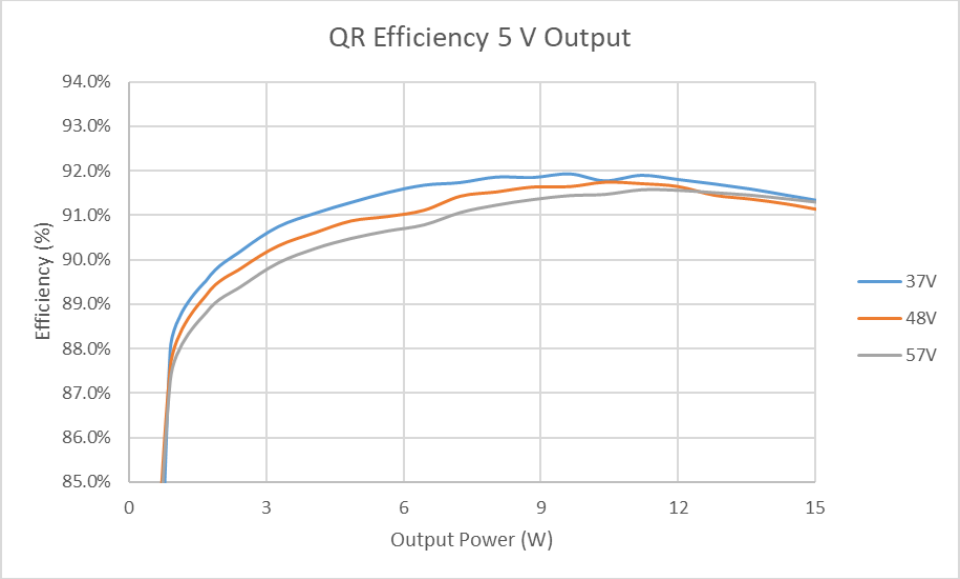

Figure 37 Efficiency Plot 5 V Output QR Flyback

37 V Input	48 V Input	57 V Input
91.2 %	91.0 %	91.2 %

Table 14 Full Load Efficiency 5 V Output QR Flyback

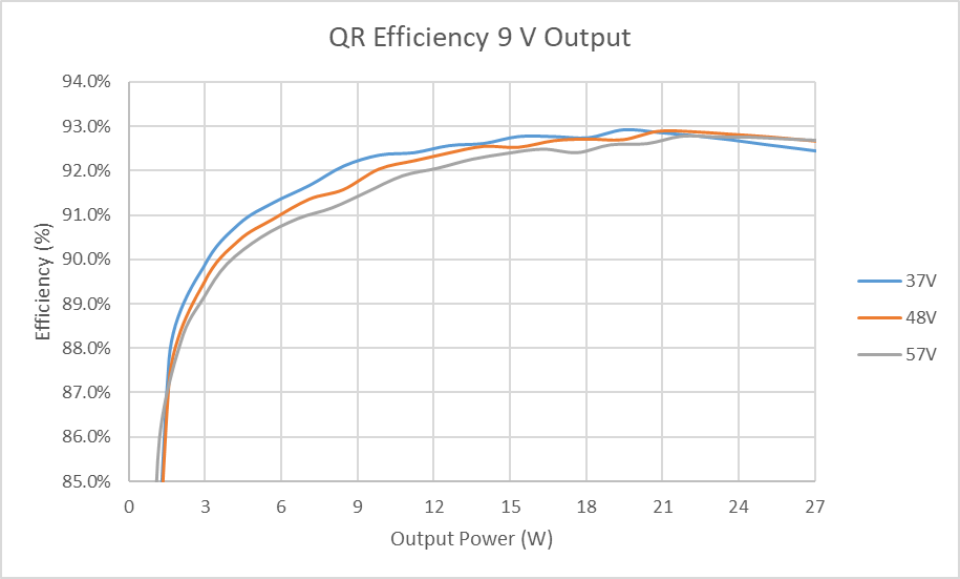

Figure 38 Efficiency Plot 9 V Output QR Flyback

37 V Input	48 V Input	57 V Input
92.4 %	92.6 %	92.7 %

Table 15 Full Load Efficiency 9 V Output QR Flyback

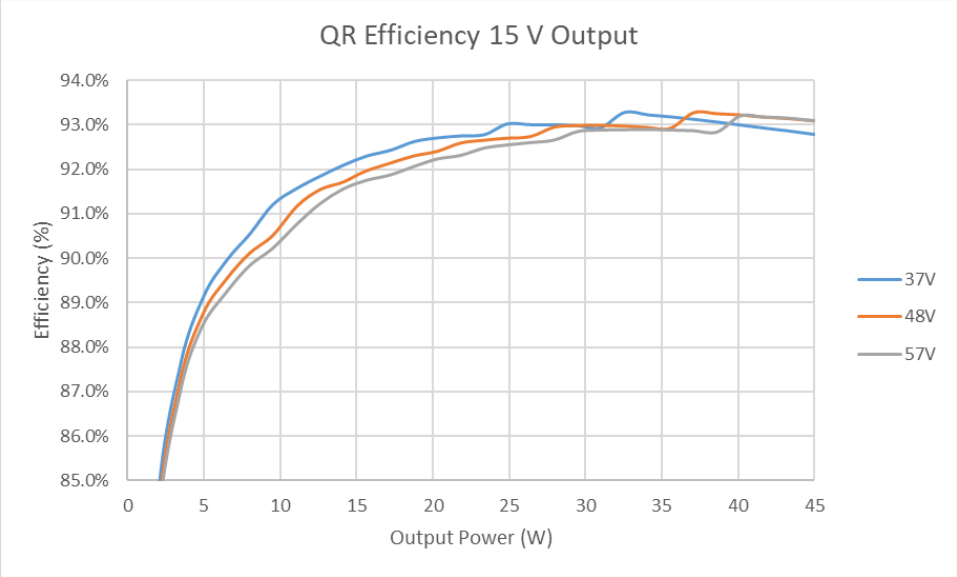

Figure 39 Efficiency Plot 15 V Output QR Flyback

37 V Input	48 V Input	57 V Input
92.7 %	93.0 %	93.1 %

Table 16 Full Load Efficiency 15 V Output QR Flyback

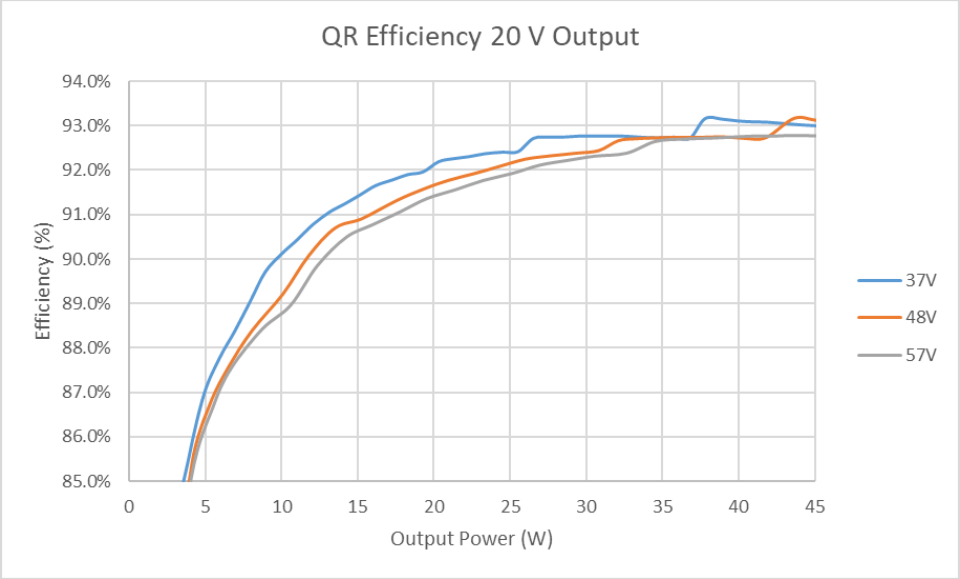

Figure 40 Efficiency Plot 20 V Output QR Flyback

37 V Input	48 V Input	57 V Input
93.0 %	93.1 %	92.8 %

Table 17 Full Load Efficiency 20 V Output QR Flyback

The full load efficiency of the QR system at 37 V input and 20 V output is 93%. This is higher than the estimated efficiency, however is close to the estimate.

As with Fixed Frequency, the efficiency is taken from input of the board to output of the board with no cable losses taken into account. With the QR switching in different valleys throughout the operation range the efficiency can be seen peaking and settling as power increases. These bumps in efficiency occur when the controller changes valleys from 1st to 2nd, 2nd to 3rd, etc. At 57 V input voltage, the max load efficiency is lower than the lower input voltage points. This could be due to the converter not entering first valley operation at the highest load.

Thermals were taken on the system after efficiency was measured. The thermals were allowed to settle at the various input and output voltages.

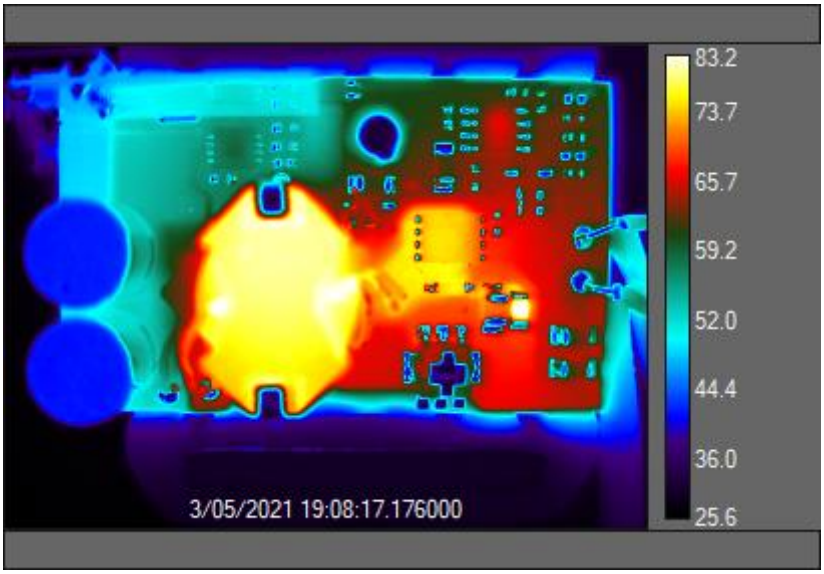

Figure 41 Thermal Image 37 Vin Full Load Top QR Flyback

Transformer	Windings	Pri FET	Snubber
80.17 °C	83.20 °C	74.71 °C	82.64 °C

Table 18 Temperatures 37 Vin Full Load Top QR Flyback

It can be seen that the transformer and the snubber are the hottest components on the primary side. This would correspond to the estimated losses, as the most losses are focused in those components. The snubber is a very hot component even though the losses are about 1/5th of the transformer losses, as the size is also very small in comparison. The primary FET is getting hot in this thermal capture, and can be seen as dissipating more than 0.127 W of energy. This must be made up for elsewhere in the converter in lower losses, as the efficiency is not drastically off from the estimate.

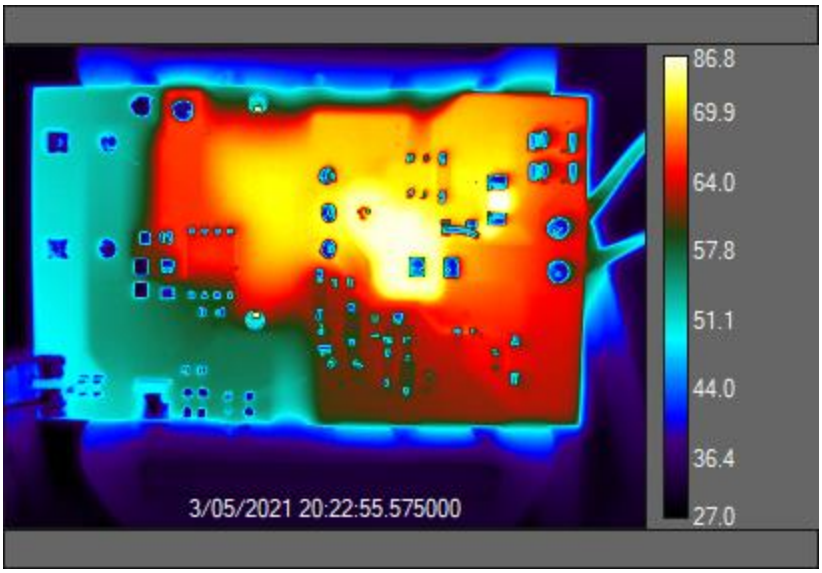

Figure 42 Thermal Image 37 Vin Full Load Bottom QR Flyback

Sec FET	Pri Snubber
65.69 °C	86.84 °C

Table 19 Temperatures 37 Vin Full Load Bottom QR Flyback

On the bottom side of the converter, it can be seen that the primary switch and the snubber are the hottest nodes. This corresponds to the top side of the converter, as these were the hotter components on that side as well.

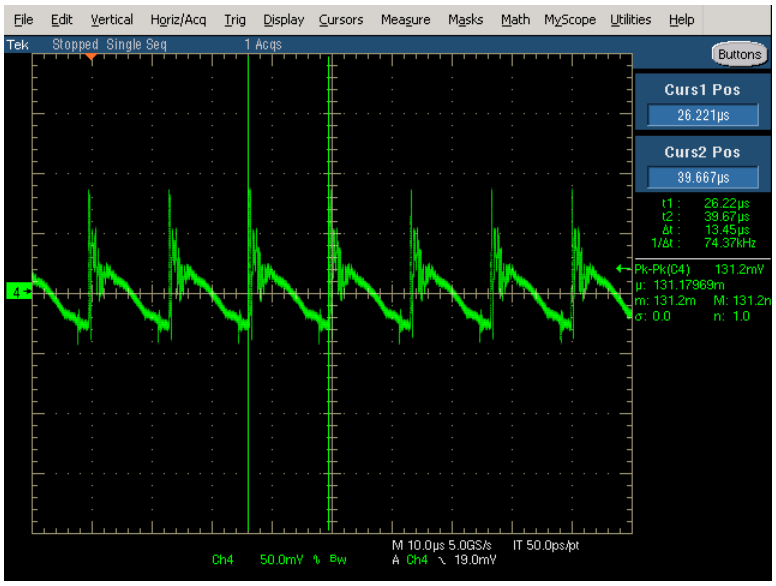

Figure 43 Ripple Capture 57 Vin 5 V / 3 A Output QR Flyback

The ripple of the QR flyback system at 57 V input and 5 V output was measured at 131 mV, which comes to a 2.62% ripple and is well within the ±5% specification. The QR flyback in particular suffered from a high frequency ripple from the turn off of the primary switch, which was corrected for with placing smaller ceramic capacitors in parallel with the electrolytic capacitors on the output.

The overall design of the QR flyback system is shown as a system which is efficient over the load range of the converter. The system maintains a high efficiency at full load for all of the USBPD voltages and shows that the maximum efficiency can be seen just before full load on the system.

CHAPTER 5

ACTIVE CLAMP FLYBACK

Active Clamp Flyback Theory of Operation

Active Clamp flyback (ACF) is a topology which actively embraces parasitic elements which are designed around in the other topologies. The snubber which is present in Fixed Frequency Flyback and Quasi-Resonant Flyback topologies is still utilized to capture the leakage energy from the transformer, but is instead recycled back into the system by replacing the diode in the primary snubber with an active switch. The act of charging and discharging the snubbing circuit, in the case of Active Clamp Flyback known as a “clamp”, enables the system to achieve true zero-volt switching and to reuse leakage energy back in the system rather than just dissipating it between cycles. At the turn off of the main switch, the current which would normally cause a leakage related spike in the primary side is instead passed through the active switch when the body diode of the switch is forward biased, which results in its own zero-volt switching. As the secondary side power delivery stage of the switching cycle concludes, the active clamp is turned off, after which the leakage inductance in the transformer resonates with the switch capacitance and rings the switch node down, which enabled zero-volt switching during the on cycle of the primary switch. [8]

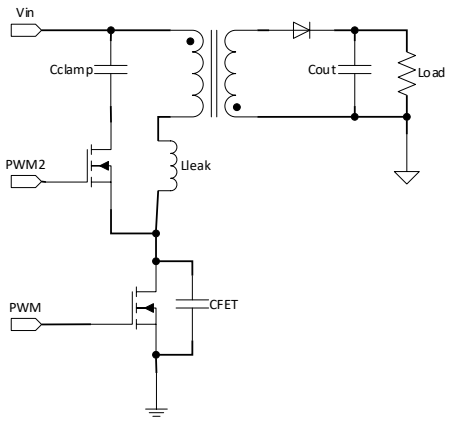

Figure 44 Active Clamp Flyback Generic Schematic

The waveforms of an ACF topology are similar to CCM operation in a fixed frequency converter as seen in Figure 12, or 1st Valley operation in a QR converter as in Figure 27.

The controller used for implementing ACF is the NCP1568 by ON Semiconductor. This controller utilizes a frequency modulation scheme in order to achieve zero volt switching across all line and load conditions. The frequency modulation ensures zero volt switching by increasing the frequency as output voltage is increased and as load is decreased, therefore keeping negative current in the design low while still enabling the magnetizing current to discharge the switch node capacitance. [8]

Active Clamp Flyback Converter Design

The design of an active clamp flyback system begins very similarly to other designs, with determining a maximum duty ratio. As with the other designs, a worst case scenario can be assumed at 50%, and designed around there. This then leads the design directly to a suggested turns ratio.

$$N_{ps} = \frac{V_{inmin} D_{\max}}{(1 - D_{max}) V_{outmax}}$$

Equation 44 Duty Max Based Turns Ratio

After the turns ratio is determined, a different order of operations must be taken due to the use of the parasitic elements as an integral part of the system. The switches are the next aspect to be determined, which can be calculated utilizing the same equations as the prior topologies.

Once the switch ratings are decided, the output capacitance of the FET (C_{oss}) is utilized to estimate negative current of the converter which plays a role in an estimated inductance calculation. This is in order to determine ZVS throughout the operation. The total switch capacitance is then calculated.

$$C_{sw_{tot}} = C_{osspri} + \frac{C_{oss_{sec}}}{N_{ps}} + C_{ossclamp}$$

Equation 45 Switch Node Total Capacitance

The negative current is then estimated for the system, with the negative current as a parameter of the controller. In the controller used, 270 ns is the specification given. The negative current changes throughout the varied input and output spectrum.

$$I_{neg} = -\frac{C_{sw_{tot}} \left(V_{in} + V_{out} N_{ps}\right)}{T_{ZVS}}$$

Equation 46 ACF Negative Current

Finally, the inductance also depends on the duty ratio in order to ensure ZVS operation in the most difficult conditions. In the case of a USBPD system, this would be a minimum input voltage, minimum output voltage condition.

$$D_{max_{Vinmin}} = \frac{N_{ps}V_{outmin}}{N_{ps}V_{outmin} + V_{inmin}}$$

Equation 47 Max Duty Cycle

Once the parameters are all calculated, a maximum primary inductance can be calculated to ensure negative current as the input voltage minimum. Also utilized in the equation is the minimum ACF switching frequency. This is a set parameter, and has been set to 100 kHz for the design.

$$L_{pri} = \frac{V_{inmin}D_{\max_{Vinmin}}}{2F_{swmin}[\frac{I_{outmax}}{(1 - D_{\max_{Vinmin}})N_{ps}} - I_{negVinminVoutmin}]}$$

Equation 48 ACF Primary Inductance

While the other designs don't utilize a leakage calculation in the design stage, the active clamp flyback depends on leakage for its basic operation. Due to being such a fundamental part of the system, the leakage must be estimated in order to assist with the design of the major components of the remainder of the system. A very basic estimation can be used in practice, and this will vary with transformer construction, layer assembly, amount of turns, and even vary from transformer to transformer in the same batch.

$$L_{prileak} = 2\% * L_{pri}$$

Equation 49 Leakage Estimation

Unlike the other designs where a snubber is meant to lessen the parasitic impacts onto the circuit, the clamp in the active clamp flyback must be designed as a main component of the system. The clamp cap is recommended based on the minimum duty cycle of the converter when operating in active clamp flyback. This is found with the maximum input voltage and minimum output voltage.

$$D_{min} = \frac{N_{ps}V_{outmin}}{N_{ps}V_{outmin} + V_{inmax}}$$

Equation 50 Minimum Duty Cycle

This parameter will provide the longest off time and therefore the longest discharging cycle. The clamp capacitance can then be calculated as a result of this.

$$C_{clamp} = \frac{(D_{min} - 1)^2}{16\pi^2 F_{swmin}^2 L_{prileak}}$$

Equation 51 ACF Clamp Capacitance

The peak current on the primary side can be calculated utilizing the on time of the active clamp flyback at the maximum output and minimum input conditions.

$$T_{on} = \frac{D_{max}}{F_{sw}}$$

Equation 52 On Time

$$I_{pripeak} = \frac{T_{on}V_{inmin}}{L_{pri} + L_{prileak}} + I_{neg}$$

Equation 53 ACF Primary Peak Current

Utilizing the peak primary current can lead to design of the transformer. As with previous design criteria, the peak flux should be designed to not exceed 0.3 T. This can be used to back calculate the number of primary turns to be utilized.

The final major component to be designed as part of system operation is output capacitance. The RMS currents of the secondary side can be calculated as a reflection of the input RMS current.

$$I_{RMSpri} = \sqrt{\frac{D_{max}\left(I_{pripeak}^2 + I_{pripeak}I_{neg} + I_{neg}^2\right)}{3}}$$

Equation 54 ACF Primary RMS Current

The maximum RMS provides the rated current of the capacitors. The maximum ESR of the output capacitance can be calculated as a product of acceptable ripple voltage.

Finally, the output capacitance is calculated as a product of off time, ripple, and RMS currents. [9]

$$C_{outmin} = \frac{I_{RMSsec} T_{off}}{V_{out_{ripple}}}$$

Equation 55 ACF Minimum Output Capacitance

Active Clamp Flyback Implementation Concerns

Active clamp flyback is a highly efficient system at full load, however the active clamp flyback mode of operation does not hold efficiency at lighter loads on the system. The solution to this issue which is implemented in ON Semiconductors NCP1568 controller is a bi-modal system. When the active clamp flyback system operates a lighter loads, it switches back to a traditional flyback DCM operating mode. During the DCM flyback mode, the system utilized only the body diode and snubbing elements of the clamp circuit and the low side switch. This acts similarly to the fixed frequency flyback system with a resistor capacitor diode snubber. This allows for a much higher efficiency light load, and once the system reaches a high enough load to benefit from active clamp mode, it begins utilizing the clamp during operation.

Utilizing a bi-modal system means that the design must account for the efficiency between both modes and attempt to maximize between the two. [10]

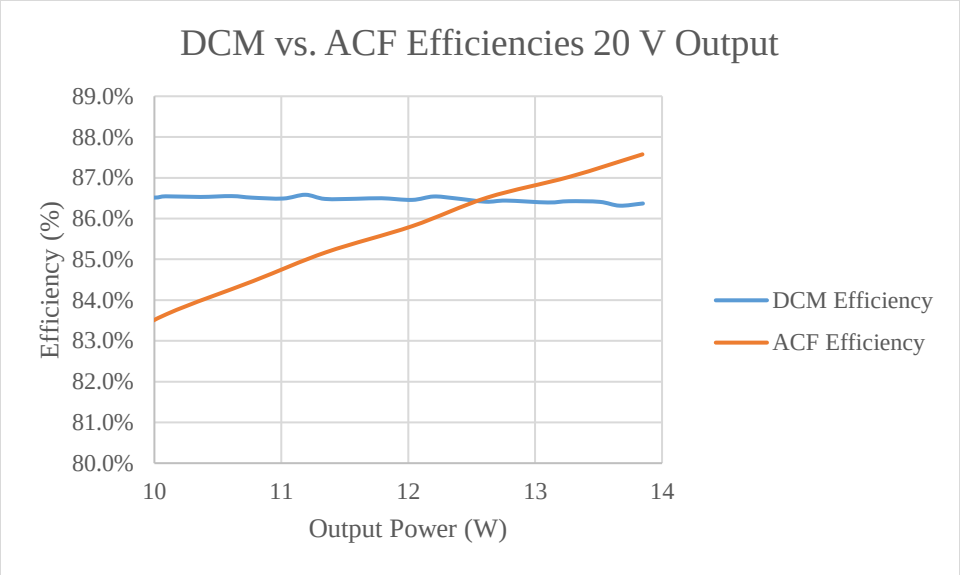

Figure 45 DCM vs. ACF Efficiency Plot ACF Implementation

The graph shows that above 12.5 W the system operates best in ACF mode of operation, while below it operates best in DCM. While this points to the best point to transition, it is necessary to place hysteresis on either side of the transition point in order to prevent the system from overlapping the operating modes, which could lead to decreases efficiency, audible noise, and strain on the system during the transition.

Because of the use of DCM at lighter loads, it is also necessary to implement a resistor across the snubber to dissipate the power during the lighter loads. The resistor can be a higher value, as it only needs to dissipate the leakage spike at light loads and will not be dissipating as much energy as a snubber in a fixed frequency or quasi-resonant flyback converter. This will allow the clamp to act as a traditional snubber during DCM and act as the active clamp during ACF operation without dissipating the recyclable energy.

One additional concern for the active clamp flyback system is the need for a level shifted gate drive for the active clamp FET. This need can be met by various gate drivers

on the market, but timing must be taken into account in this component, as too long of propagation delays can cause inefficiencies in the system. For this design, NCP51530 was chosen with a 60 ns typical and 100 ns maximum propagation delay. [11]

Active Clamp Flyback Expected Losses

Similar to the previous designs, the losses in an active clamp flyback converter begin by calculating the RMS currents through the switches and transformer. RMS currents in an active clamp flyback need to be calculated through the primary FET, the secondary FET, and the active clamp FET. RMS currents are calculated during the design formulas section.

The only RMS which was not calculated during the design stage is the clamp FET current. The RMS current through the clamp FET is the current flowing into an undamped first order LC filter during the off time of the primary FET [9].

$$I_{LC_{Clamp}} = I_{pripeak} \cos\left(\frac{t}{\sqrt{L_{prileak} C_{clamp}}}\right)$$

Equation 56 ACF Clamp RMS Current

$$t_{off} = \frac{1 - D_{max}}{F_{sw}}$$

Equation 57 Off Time

$$T_{eval} = t_{off} - T_{zvs} - T_{rise}$$

Equation 58 ACF Evaluation Time for Clamp Current

$$I_{clamp} = \sqrt{F_{sw} \int_0^{T_{eval}} I_{LC_{Clamp}}^2 dt}$$

Equation 59 ACF Clamp Current

The final conduction losses of the three FETs can be calculated using the RMS currents, and the R_{DSon} of the FETs. The FETs utilized in the ACF design are FDMS86255 for the primary and clamp FETs with 12.4 mΩ on-resistance, and FDMS86101 with 8 mΩ on-resistance for the secondary FET.

While in the other topologies switching losses needed to be calculated as part of the final loss mechanisms, in active clamp flyback one of the main benefits of the topology is ZVS, which means that switching losses are theoretically zero.

The next major loss component is the transformer. As mentioned previously, the losses are divided into conduction losses and core losses. Conduction losses stem from primary RMS currents, but unlike the other topologies active clamp flyback has additional current in the primary side by recycling the clamp energy, meaning that it is not equivalent to just the primary FET current.

$$I_{trans_{RMSpri}} = \sqrt{I_{clamp}^2 + I_{pri_{RMS}}^2}$$

Equation 60 ACF Primary RMS of Transformer

The secondary current of the transformer is then the same as the RMS current through the secondary FET. The final wound transformer featured a primary resistance of 25 mΩ, and a secondary resistance of 14 mΩ.

The second part to transformer losses comes from the core losses associated with the transformer, which is an inherent property of the material chosen, and depends on the flux. In this case, the material is ML29D, and the core size chosen is RM6. As B_{max} was calculated in the design section, this can then be used to calculate that core losses per area.

As with before, the final major power loss element in the system is the output capacitors. This system features the same output capacitors as the previous systems which is two capacitors that have 15 mΩ a piece for a total ESR of 7.5 mΩ.

With the losses calculated, the total can be summed for a final efficiency estimate. With the snubber being utilized to recycle the energy back into the system the energy does not need to be accounted for and can instead be assumed as zero.

PriFET	SecFET	ClampFET	Trans	Cout	Total
67 mW	174 mW	130 mW	2.67 W	163 mW	3.204 W

Table 20 Estimated Losses of Active Clamp Flyback

This leads to a final estimated system efficiency of 93.4% efficiency.

Active Clamp Flyback Converter Schematic

With values calculated, a schematic can be put together for the ACF system. As the system features the addition of another switch and a level shifting driver for it, the schematic contains additional components on the primary side. As the NCP1568 utilized a feedback based multi-mode system to improve efficiency at light loads, the auxiliary circuit also contains an element meant to bias the transitions thresholds for ACF to DCM and from DCM to ACF for changing output voltages. This circuit takes the aux voltage which is proportional to V_{out} and utilizes it to increase the feedback voltage to the necessary levels to ensure a balanced transition at each output voltage and load.

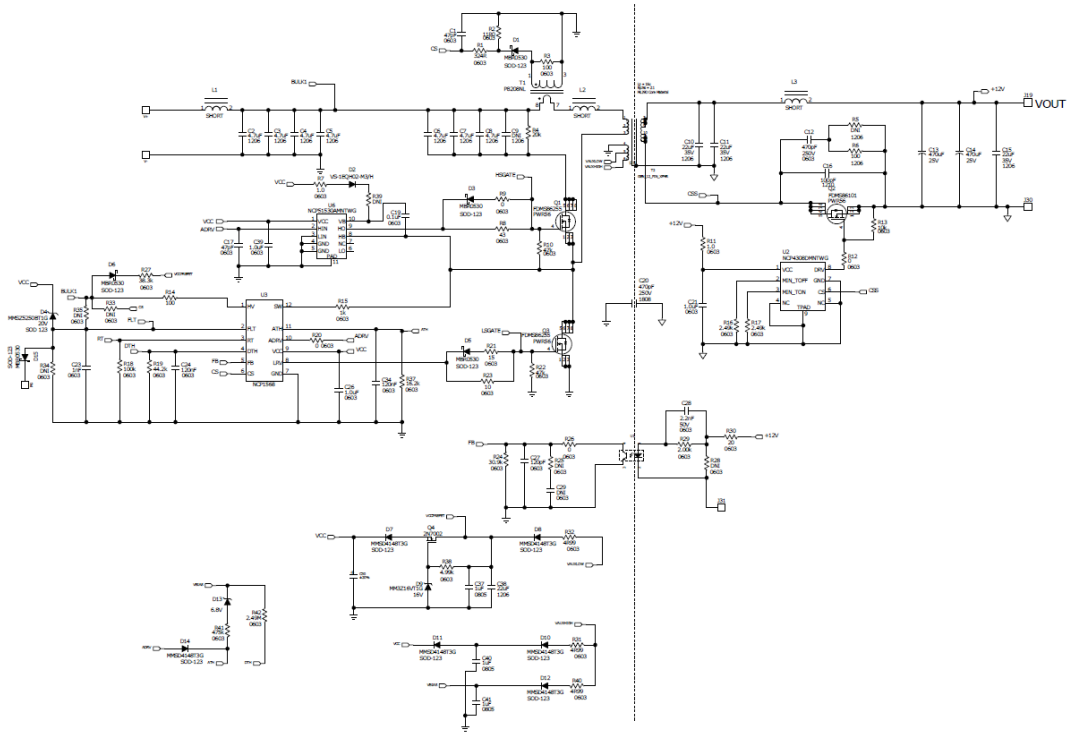

Figure 46 Active Clamp Flyback Schematic

Active Clamp Flyback Converter Layout

In the Active Clamp Flyback, the losses are fairly small and focused in the transformer. This means that the layout design can focus mostly around power density, as thermals do not need to be distributed into the copper on the PCB. This means that the most space taken by this design is by the additional circuitry for V_{cc} and the added gate drive and clamp FET.

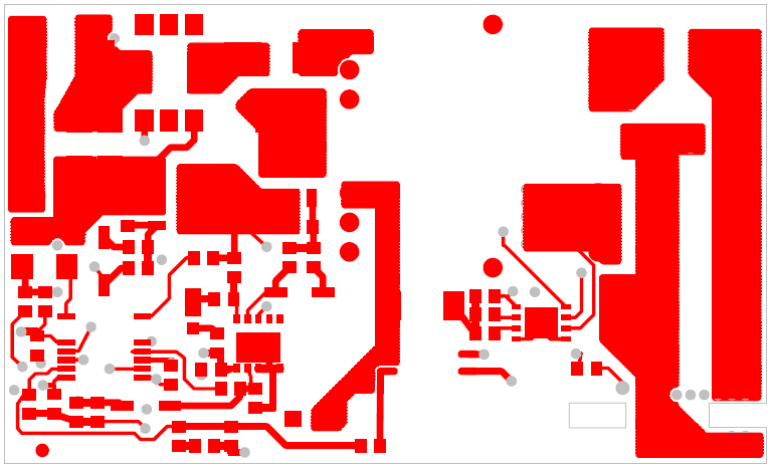

Figure 47 Bottom Layer of Active Clamp Flyback Layout

The bottom layer of the ACF board holds the primary controller, SR controller, both primary switches, the high side driver, and the standing components. The biasing circuit to assist with transitions makes the primary side V_{cc} circuit more complex, which means the circuit must be laid out on both sides to accommodate enough space.

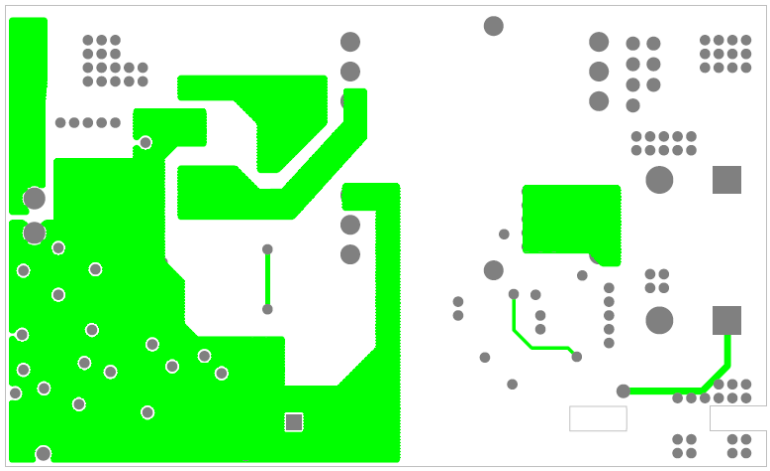

Figure 48 Inner Layer 2 of Active Clamp Flyback Layout

Inner layer 2 of the board is mainly a primary ground plane, along with more conduction planes on the primary side. This enables the shielding of sensitive signals from the noisier signals on other layers.

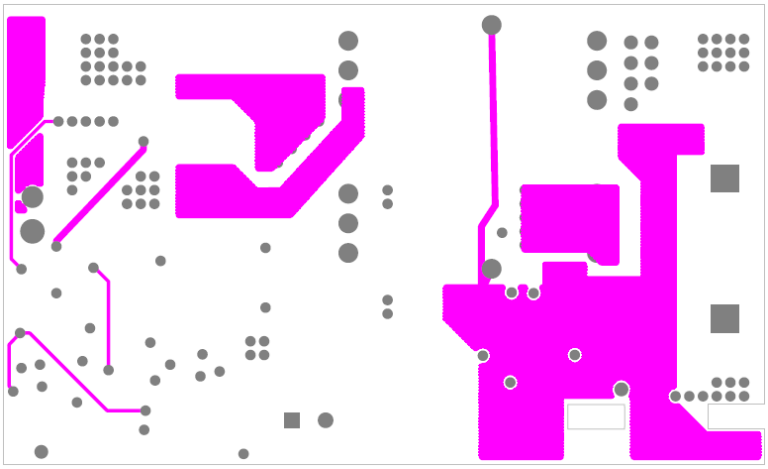

Figure 49 Inner Layer 1 of Active Clamp Flyback Layout

Inner layer 1 is where the secondary ground plane is housed, as well as primary CS and input voltage signals for the controller.

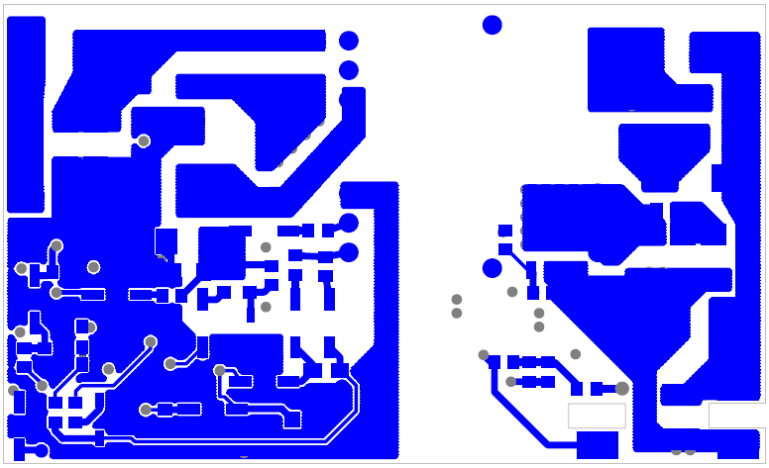

Figure 50 Top Layer of Active Clamp Flyback Layout

The top layer of the board is another a surface mount layer which includes the secondary switch and more primary V_{cc} circuit components, as well as controller configuration components.

The inner layers are utilized to isolate sensitive signals from noisy signals, as well as create a ground connection through the IC and V_{cc} routing. The major difference in the exterior layers of the layout is the addition of the clamp FET, which requires a gate drive

from the level shifting driver. The level shift driver requires a few additional components in order to lift the boost drive voltage above the switch node voltage. The secondary side of this layout mimics the other two layouts as well.

Active Clamp Flyback Results

The final board of the active clamp flyback came together without major edits. No additions were made outside of the footprints of the printed board.

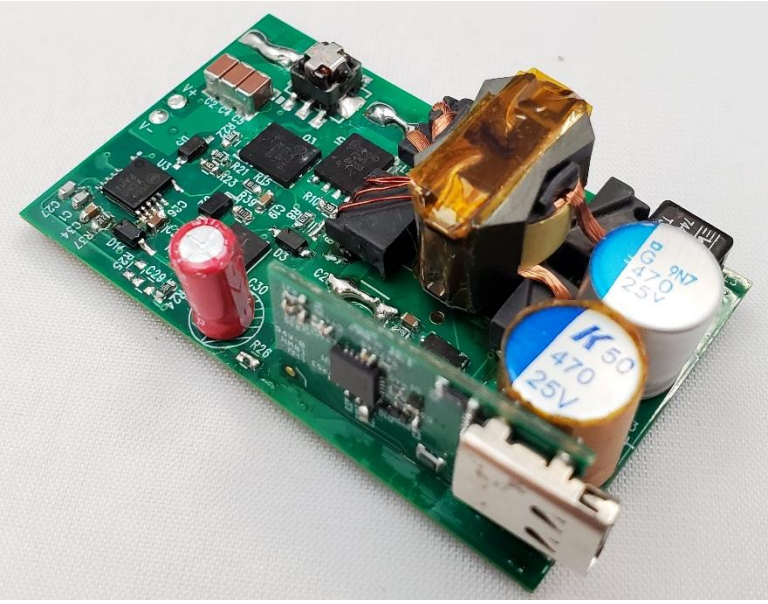

Figure 51Assembled Board Picture of Active Clamp Flyback Board

It can be seen that the silicon on the board takes up a significant area, as the transformer is a much smaller footprint and the losses of the board were not a major limiting factor in layout, which reduced the major copper planes necessary for the system thermals.

Final efficiency on this board began at 5 V output and 37 V input as well, and moved up in testing on both input and output voltage.

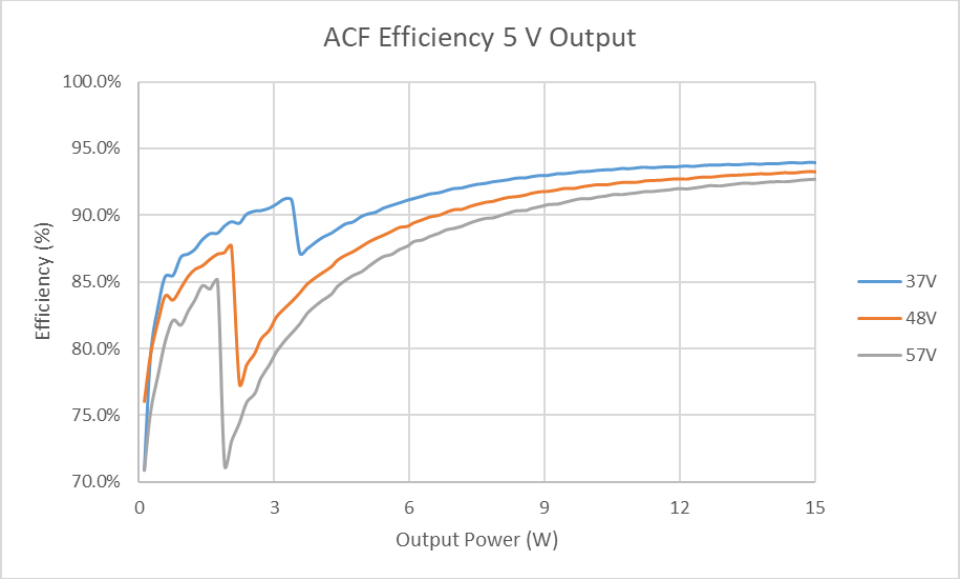

Figure 52 Efficiency Plot 5 V Output Active Clamp Flyback

37 V Input	48 V Input	57 V Input
93.9 %	93.3 %	92.6 %

Table 21 Full Load Efficiency 5 V Output Active Clamp Flyback

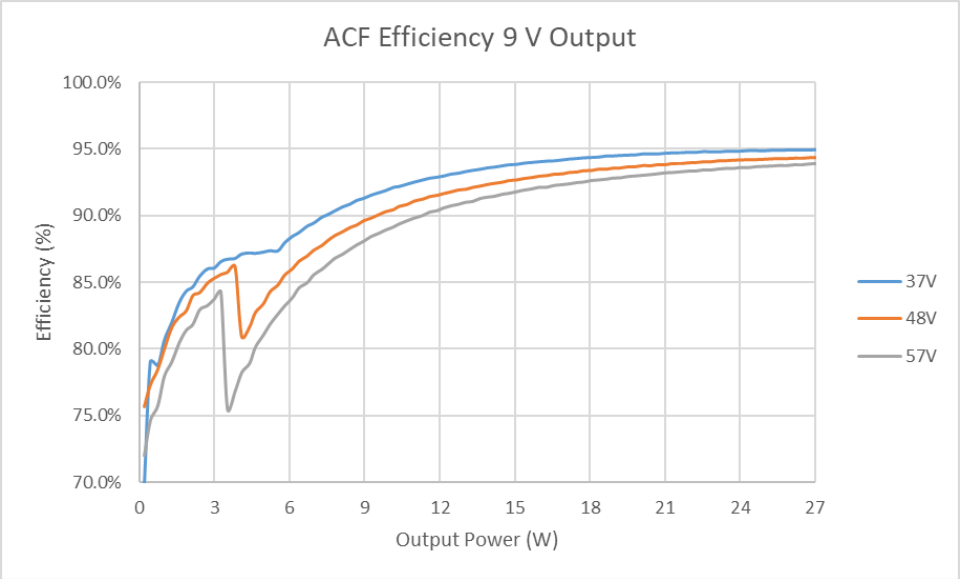

Figure 53 Efficiency Plot 9 V Output Active Clamp Flyback

37 V Input	48 V Input	57 V Input
94.9 %	94.3 %	93.9 %

Table 22 Full Load Efficiency 9 V Output Active Clamp Flyback

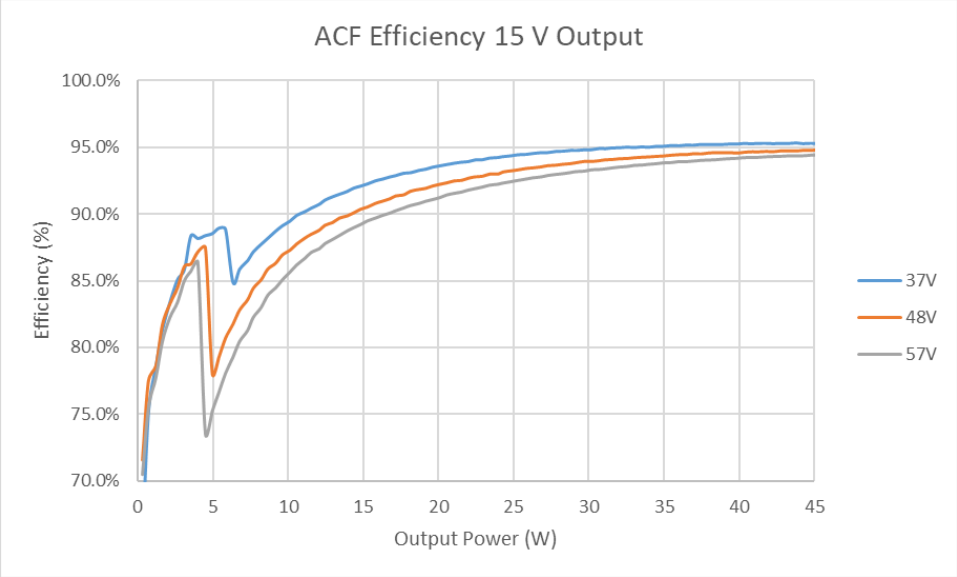

Figure 54 Efficiency Plot 15 V Output Active Clamp Flyback

37 V Input	48 V Input	57 V Input
95.2 %	94.8 %	94.4 %

Table 23 Full Load Efficiency 15 V Output Active Clamp Flyback

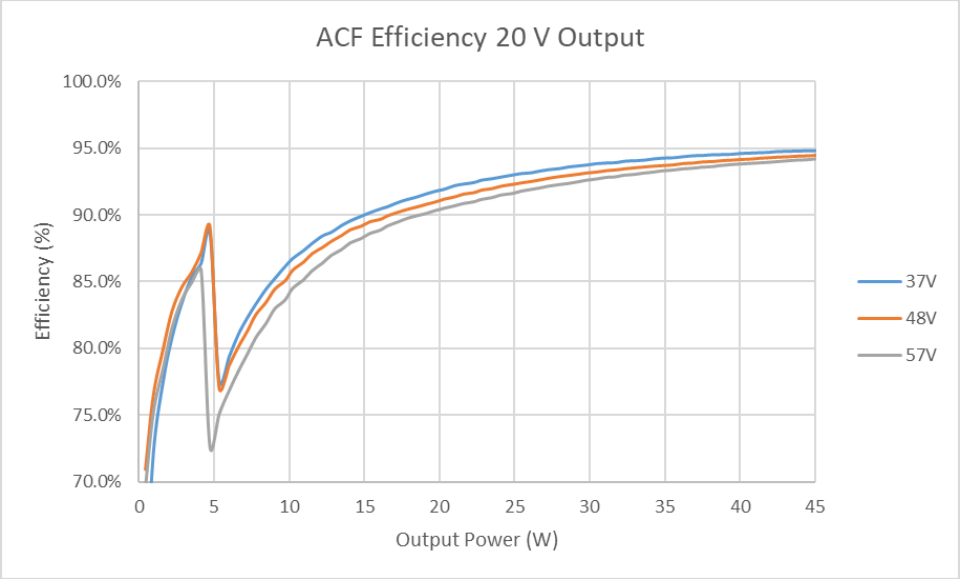

Figure 55 Efficiency Plot 20 V Output Active Clamp Flyback

37 V Input	48 V Input	57 V Input
94.8 %	94.5 %	94.2 %

Table 24 Full Load Efficiency 20 V Output Active Clamp Flyback

The final full load efficiency of the system at 37 V is seen at 94.8%. This is higher than the anticipated full load efficiency, and can be attributed again to the air gap of the core which reduces the B_{max}. Additionally, the final full load efficiency at each output voltage is high as well, indicating that the change in output voltage does not affect efficiency drastically.

In each of the efficiency plots, a dip can be seen around 6 W operation. This is attributed to the two separate modes of operation, as above the 6 W point is in ACF operation while below is in DCM. As seen previously, this is not the ideal point of transition. Due to the hysteresis of the transition point, the transition from ACF operation at higher to DCM operation at lower load is lower than the optimal point and this data was taken with a decreasing load. The decreasing load is taken to enable the thermals of

the system to settle at the hottest point. If the same data is taken at an increasing load, the transition point shows closer to 12 W which is the ideal point.

At the light load, efficiency decreases in ACF mode even with zero volt switching operation. This is due to the magnetizing current always operating in CCM, which creates additional losses in the transformer. While the CCM magnetizing current helps at high loads, it hurts at light load, as shown in the ACF efficiency plots. [8]

Additionally, the design was made without significant copper area to sink heat. Thermals show in this case that the major silicon components are not the main loss mechanism of the design.

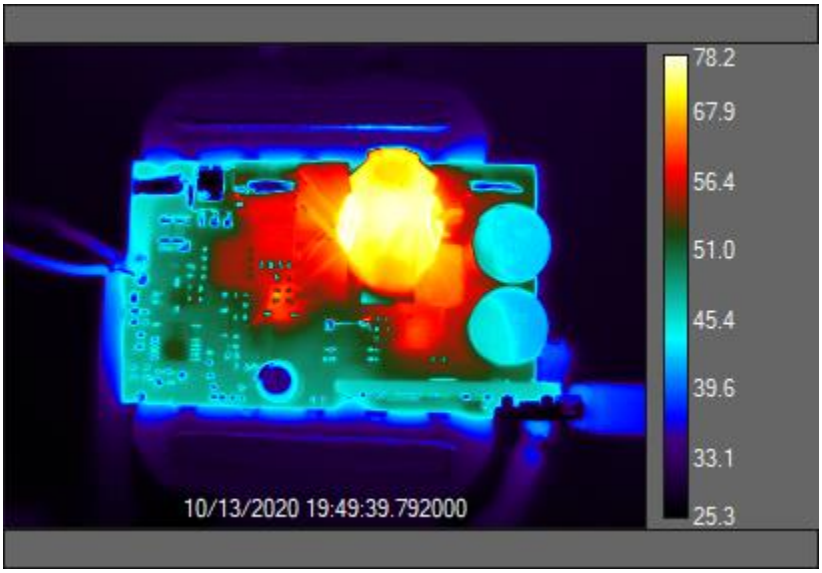

Figure 56 Thermal Image 37 Vin Full Load Top Active Clamp Flyback

Transformer	Windings	Pri FET	Clamp FET
75.15 °C	78.23 °C	54.72 °C	57.96 °C

Table 25 Temperatures 37 Vin Full Load Top Active Clamp Flyback

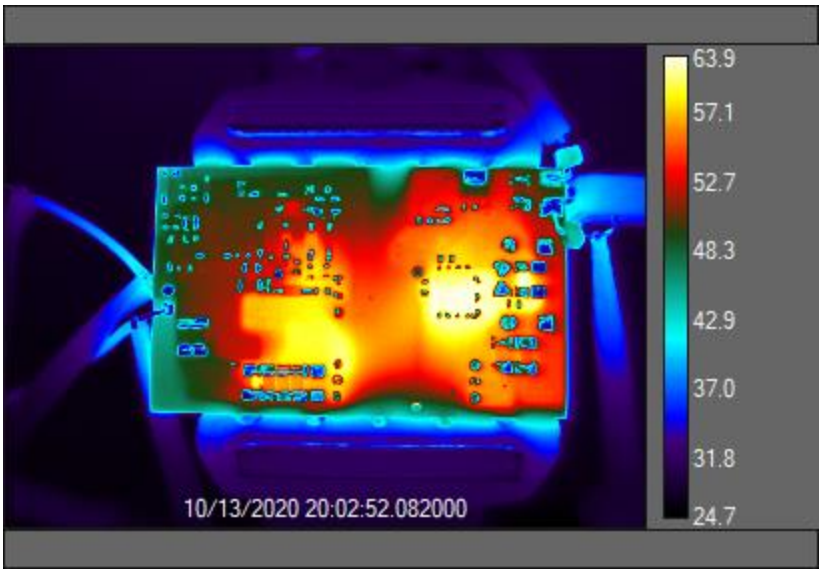

Figure 57 Thermal Image 37 Vin Full Load Bottom Active Clamp Flyback

Sec FET
63.90 °C

Table 26 Temperatures 37 Vin Full Load Bottom Active Clamp Flyback

The system captures show a very cool board, as the temperature hues increase relative to the maximum temp. On the top of the board, the maximum temperature is within the transformer windings, while on the bottom the secondary FET is the hottest component.

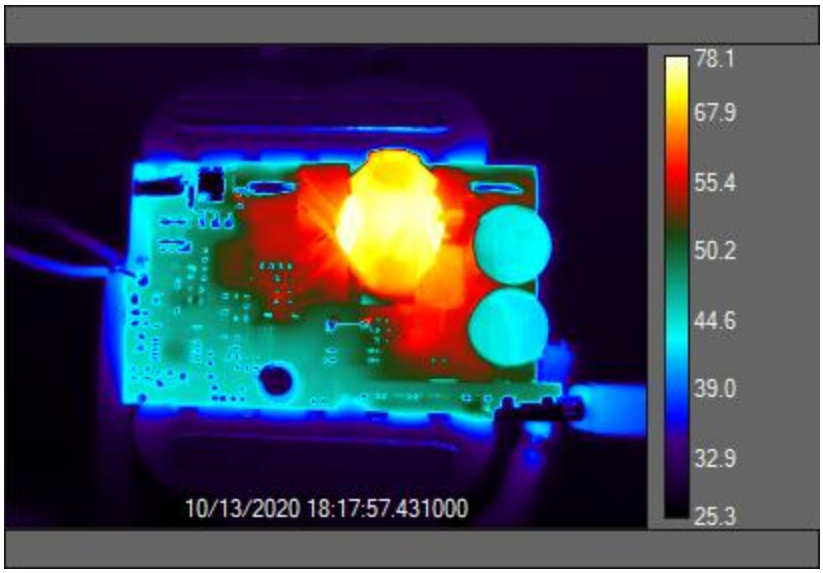

Figure 58 Thermal Image 37 Vin 15 Vout Full Load Top Active Clamp Flyback

Transformer	Windings	Pri FET	Clamp FET
73.83 °C	78.14 °C	52.30 °C	56.48 °C

Table 27 Temperatures 37 Vin 15 Vout Full Load Top Active Clamp Flyback

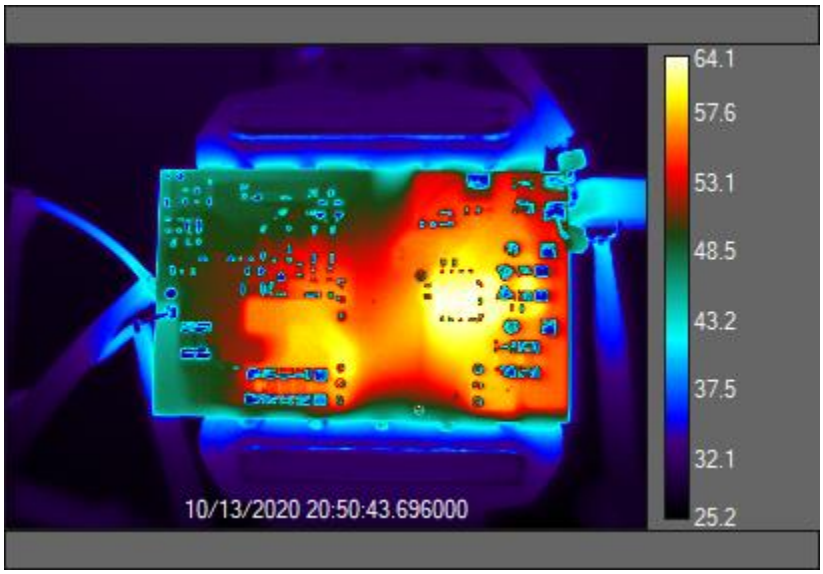

Figure 59 Thermal Image 37 Vin 15 Vout Full Load Bottom Active Clamp Flyback

Sec FET
64.10 °C

Table 28 Temperatures 37 Vin 15 Vout Full Load Bottom Active Clamp Flyback

Additionally, it can be seen that the maximum output power at 15 V does not change the major components maximum temperatures. This indicates that the higher output currents does not change the thermal signature of the board as much as output power contributes.

The USBPD ripple spec is verified after the power and thermal ratings.

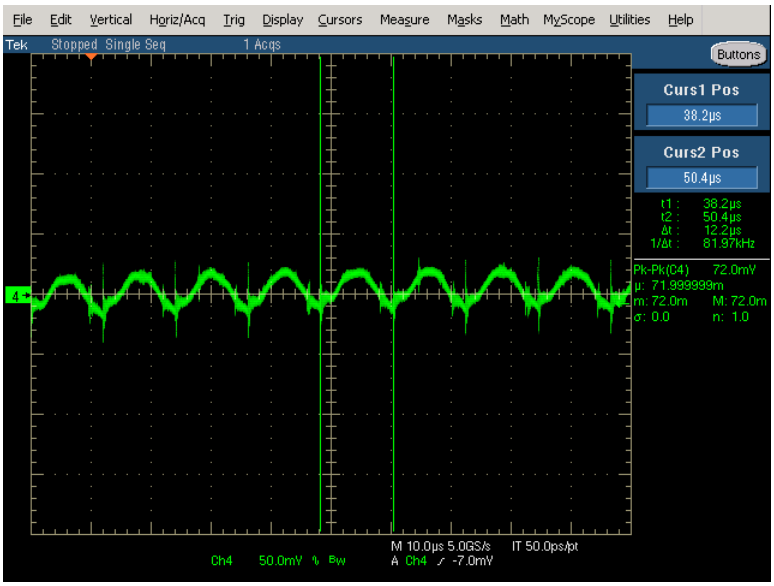

Figure 60 Ripple Capture 57 Vin 5 V / 3 A Output Active Clamp Flyback

The final ripple of the system at 57 V input and 5 V output maximum load is 72 mV, which is a 1.44% total ripple, and is within the ±5% specification for USBPD standards.

Overall, the final implementation of the active clamp flyback design has shown to be a high efficiency design for PoE to USBPD. The losses were saved on the transformer by the air gap, and potentially more losses than anticipated are present on the secondary

FET. The final efficiency is higher than anticipated, and is shown to be consistently high throughout the operation range of load and output voltages.

CHAPTER 6

RESULTS COMPARISON

Each topology features its own unique benefits which is gained in the forms of ease of design, efficiency, and cost. The designer must choose which priorities are necessary for a given design. For the most part, the scope of the project will set the efficiency and cost requirement. Customers or the end application will determine how efficient or costly the design can be, as certain applications can demand a higher premium than others or have thermal requirements that require higher efficiency. Ease of design is introduced as a factor for the designer when cost and efficiency can be met by any topology, however it is not a quantifiable metric as it is subjective to the designer and is related to any sub-specification set for the design.

Efficiency Comparison

Efficiency as compared by topology varied based on input and output voltage. For the purposes of the design 45 W was chosen as the output power and 20 V is the maximum specified voltage by the USBPD specification. This opens the possibility for 15 V and 20 V to meet the full power, and the topologies can be compared at full load efficiency. While the topologies can be compared at any given input voltage, the nominal input voltage is 48 V for PoE.

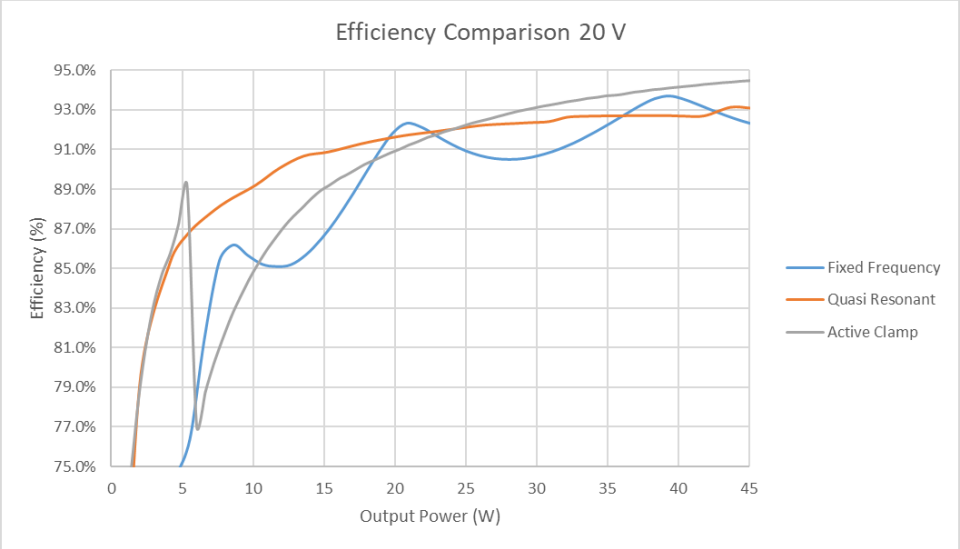

Figure 61 Efficiency Comparison 48 Vin 20 V Output

In the results for 20 V output, it can be seen that at full load the active clamp flyback is the clear frontrunner for full load efficiency. This is due to the full use of the recycled energy in the system and zero-volt switching. The next closest is the QR flyback, as it makes use of the 1st valley switching for minimizing switching losses. Coming up as the lowest efficiency at full load is the fixed frequency design.

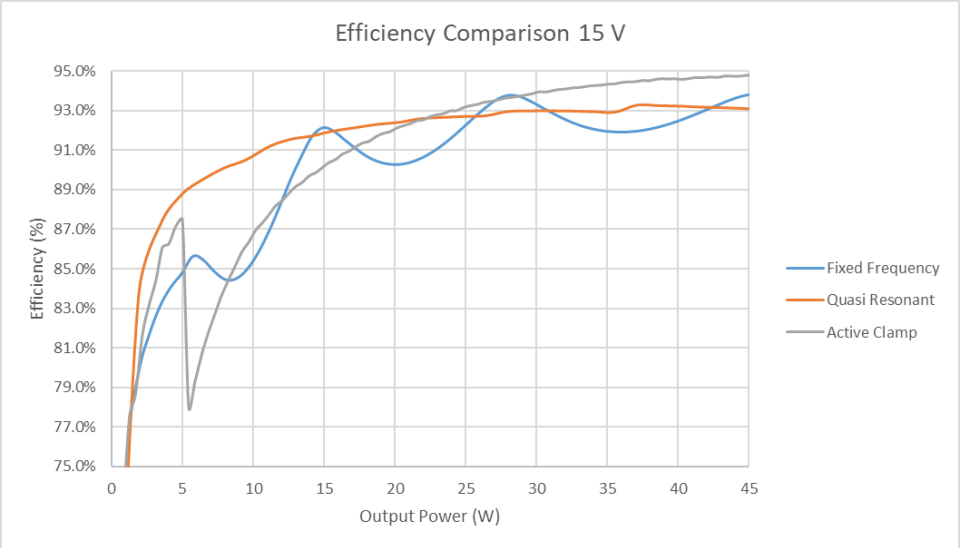

Figure 62 Efficiency Comparison 48 Vin 15 V Output

In 15 V operation, the active clamp flyback again holds the highest full load efficiency among the topologies. In this instance, the fixed frequency design does hold a higher efficiency than the QR design. This could be due to the fixed frequency switching in a valley and benefiting from the valley switching without having to specifically design for it at this point.

During use, the converter will likely not be at full load during the entirety of its operation. While full load is a metric to measure system efficiency, it is not the only consideration. As active clamp flyback decreases in output load, the efficiency decreases drastically. The bi-modal operation of the system also creates inefficient operation in the lower active clamp mode operation, as can be seen by the efficiency dipping to below 80% efficiency before the mode transition takes over to help pull efficiency back up.

The fixed frequency flyback design holds a higher efficiency at certain load points among the range, however holds lower efficiency than the QR or ACF topologies at other points due to switching at a peak or valley. The design benefits from the ringing on the switch node at certain points, but also suffers at others.

For maximum full load efficiency in the design, the active clamp flyback is much higher than the others, but for the consistency and lighter load efficiencies the QR is the most consistent throughout the range. The QR flyback controller has 1^{st} through 6^{th} valley switching, as well as light load skip features to help the system maintain a fairly consistent efficiency all the day down the range. [6]

In this case, if thermals is the limiting factor the ACF topology will have a clear benefit as at full load operation, the design boasts the highest efficiency and therefore the

lowest losses to dissipate in its design. Otherwise, simplicity of design or light load efficiencies may determine the choice.

Highest load efficiencies are not the only consideration to the design with varying output voltages.

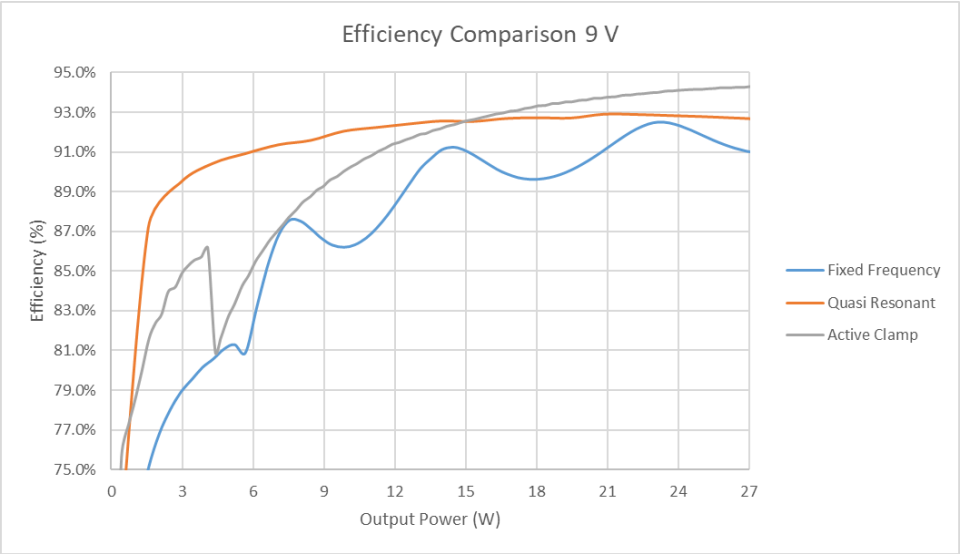

Figure 63 Efficiency Comparison 48 Vin 9 V Output

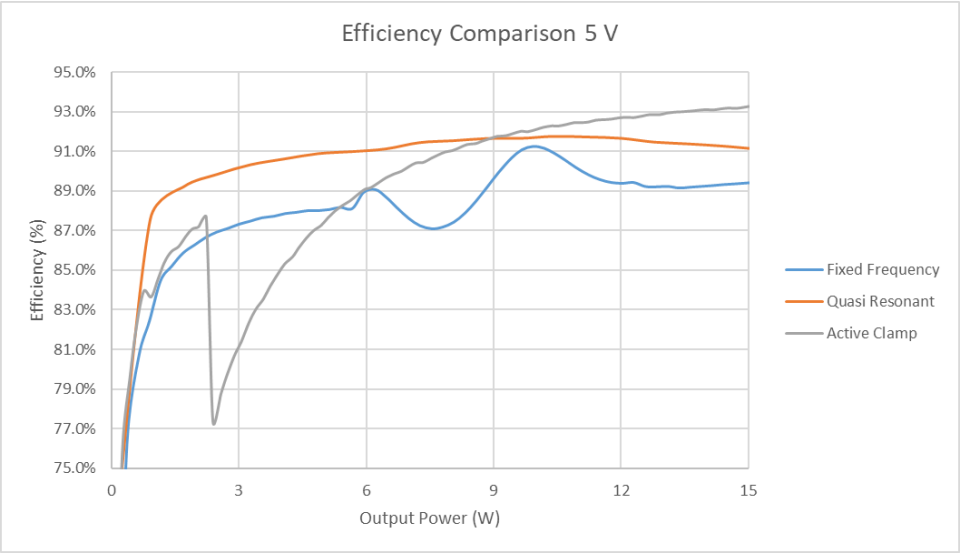

Figure 64 Efficiency Comparison 48 Vin 9 V Output

The efficiency comparisons of 5 V and 9 V outputs match the results for 15 V and 20 V outputs, with the included observation that QR clearly exceeds the fixed frequency design at these output voltages in efficiency.

Cost of Design

Each design comes with its own efficiency benefits but another concern is the cost to implement the design. The cost includes the passive components (resistors and capacitors), discrete semiconductors (MOSFETs and diodes), and controllers and drivers. Some components are universal per system but others are unique to each system and potential subsystems.

Fixed Frequency	Quasi Resonant	Active Clamp
64 Components	68 Components	94 Components

Table 29 Component Count

Based from components count, the fixed frequency design and the QR design are similar. The active clamp flyback design features a much higher component count than the other topologies, mainly due to the addition of a driver and additional FET onto the design. Adding another semiconductor onto the design adds any local control passives, and any additional decoupling capacitors to the design.

While the fixed frequency design and the QR design are close on component count, the active clamp flyback features the addition of another switch and a high side driver. These components are more expensive than adding more passive components to the bill of materials, and bring the price up to a more premium point than the fixed frequency and QR flyback topologies.

CHAPTER 7

CONCLUSION

When building a power supply with a flyback topology, there are multiple topologies which are available for designers to choose from. The considerations which are employed to make the decisions of which topology to use come from efficiency, thermal, and cost limitations. Each topology has its own unique advantages for the end application.

When using a fixed frequency flyback, the designer must choose a point to operate in DCM versus CCM mode, and make the necessary adjustments to account for both modes of operation including ensuring SR layout integrity. The design must also account for the additional heat which is dissipated by switching losses and snubbing losses in the system, either by sizing components with appropriate space and power rating or by allowing the design enough copper to sink the heat into the board.

Utilizing a QR system avoids the inconsistency of the peak and valley switching which is inherent to DCM mode of the fixed frequency design, while also allowing the SR to have ample time to turn off before the next on cycle of the primary switch. The valley switching and multiple valley operation modes of the QR controller allows the system to maintain a consistently good efficiency from light load to full load as well. The snubber must be taken care to be able to sink the necessary power to be dissipated through it, and the primary switch should also have the necessary copper to sink heat as well.

The Active Clamp flyback system had the most efficient full load operation of all the studied topologies, and therefore holds the lowest thermal dissipation through the

design. This allows the designer to be less concerned about heat sinking in the design, and place higher priority on signal integrity and the additional layout concerns which are introduced by adding an additional MOSFET and driver to the design. The addition of the high side FET and driver give the system a higher total cost, but also the higher efficiency at full load. The design must be tuned after design to ensure that the mode transitions are placed in the correct load points, otherwise efficiency can suffer in the light to medium load points.

Overall, the flyback topology is a good topology for the PoE to USBPD space as it provides high efficiency and power dense designs. The choice of which topology to use comes from the design requirements as set by the end application, which could help choose which aspect of the design to place the highest priority on and therefore which method will be used to meet that specification.

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