Potential Induced Degradation (PID) of Photovoltaic Modules:

Influence of Superstrate, Encapsulant and Substrate

by

Farrukh ibne Mahmood

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved June 2023 by the
Graduate Supervisory Committee:

GovindaSamy TamizhMani, Chair
Bradley Rogers
Jaewon Oh
John Rajadas

ARIZONA STATE UNIVERSITY

August 2023

ABSTRACT

Solar photovoltaic (PV) generation has seen significant growth in 2021, with an increase of around 22% and exceeding 1000 TWh. However, this has also led to reliability and durability issues, particularly potential induced degradation (PID), which can reduce module output by up to 30%. This study uses cell- and module-level analysis to investigate the impact of superstrate, encapsulant, and substrate on PID.

The influence of different substrates and encapsulants is studied using one-cell modules, showing that substrates with poor water-blocking properties can worsen PID, and encapsulants with lower volumetric resistance can conduct easily under damp conditions, enabling PID mechanisms (results show maximum degradation of 9%). Applying an anti-soiling coating on the front glass (superstrate) reduces PID by nearly 53%. Typical superstrates have sodium which accelerates the PID process, and therefore, using such coatings can lessen the PID problem.

At the module level, the study examines the influence of weakened interface adhesion strengths in traditional Glass-Backsheet (GB) and emerging Glass-Glass (GG) (primarily bifacial modules) constructions. The findings show nearly 64% more power degradation in GG modules than in GB. Moreover, the current methods for detecting PID use new modules, which can give inaccurate information instead of DH-stressed modules for PID testing, as done in this work.

A comprehensive PID susceptibility analysis for multiple fresh bifacial constructions shows significant degradation from 20 to 50% in various constructions. The presence of glass as the substrate exacerbates the PID problem due to more ionic activity

available from the two glass sides. Recovery experiments are also conducted to understand the extent of the PID issue.

Overall, this study identifies, studies, and explains the impact of superstrate, substrate, and encapsulant on the underlying PID mechanisms. Various pre- and post-stress characterization tests, including light and dark current-voltage (I-V) tests, electroluminescence (EL) imaging, infrared (IR) imaging, and UV fluorescence (UVF) imaging, are used to evaluate the findings. This study is significant as it provides insights into the PID issues in solar PV systems, which can help improve their performance and reliability.

To Allah Almighty, who made this possible.

Thanks to my parents for their unconditional

love and support through my program

ACKNOWLEDGMENTS

Thanks to my Ph.D. dissertation advisor Dr. GovindaSamy TamizhMani for his precious guidance, support, and advice throughout the program. I would also like to thank my committee members, Dr. John Rajadas, Dr. Bradley Rogers, and Dr. Jaewon Oh, for their input and time throughout the program. Thanks to all the excellent staff, especially Mr. Sai Tatapudi, Dr. Fang Li and Dr. Akash Kumar, and Arizona State University Photovoltaic Reliability Lab (ASU-PRL) students who helped me in my work. I would also like to thank Dr. Cecile Molto and the Florida Solar Energy Center University of Central Florida (FSEC-UCF) team, who provided valuable input for my work. Thanks to Dr. Peter Hacke from the National Renewable Energy Laboratory (NREL) for his important suggestions for my work. Parts of this work are supported by NREL and the Department of Energy, Office of Energy Efficiency and Renewable Energy (EERE) under award numbers DE-EE-0008565 and DE-EE-0009345.

TABLE OF CONTENTS

Page

LIST OF TABLES vii

LIST OF FIGURES viii

CHAPTER

1: INTRODCUTION 1

1.1 Global Solar Outlook 1

1.2 PV Module Components 3

1.3 PV Module Degradation and Reliability 8

1.4 Motivation and Outline 12

2: LITERATURE REVIEW 15

2.1 PV System Configuration 15

2.2 Pathways for Leakage Current (LC) 17

2.3 Testing Methods for PID 19

2.4 PID Mechanisms 24

2.5 PID Prevention (Effect of System Configuration and Module Construction) 44

2.6 PID Recovery (Effect of System Configuration and Ambient Conditions) 51

3: METHODOLOGY 58

3.1 Impact of PID due to Backsheet, Encapsulant, and AS coating (One Cell Modules) 58

CHAPTER Page

3.2 Impact of PID on DH-stressed GG and GB modules (Commercial Modules).....63

3.3 Impact of PID (focus on PID-p) on Bifacial Modules (Commercial Modules).....66

4: RESULTS AND DISCUSSION 73

4.1 Impact of PID due to Backsheet, Encapsulant, and AS coating (One Cell Modules).....73

4.2 Impact of PID on DH-stressed GG and GB modules (Commercial Modules).....87

4.3 Impact of PID (focus on PID-p) on Bifacial Modules (Commercial Modules).....109

5: CONCLUSIONS 144

REFERENCES 148

LIST OF TABLES

Table Page

1. PID Mechanisms and Degradation Modes in Different Cell Technologies [65], [66], [82], [91], [97], [90], [123], [98], [99], [119], [124], [122], [111], [125], [115], [121], [118], [126], [127] 43
2. Encapsulants Properties [132], [133], [134], [135], [136] 46
3. Testing Configuration for the One-Cell Modules 61
4. Nameplate IV Parameters at STC, Maximum Current (I_{MP}), Maximum Voltage (V_{MP}) 64
5. Module Details 69
6. Testing Details 70
7. Pre and Post-PID R_{SH} and R_S Data for Modules With Different Backsheets 74
8. Ratings for the Modules With Different Backsheets 77
9. Pre and Post-PID R_{SH} and R_S Data for Modules With Different Encapsulants 80
10. Pre and Post-PID R_{SH} and R_S Data for Modules With and Without AS Coating 84
11. R_{SH} and R_S Data Pre and Post-PID (After DH) for GG Modules From Dark IV 93
12. R_{SH} and R_S Data Pre and Post-PID (After DH) for GB Modules From Dark IV 104
13. Percentage Change in Series and Shunt Resistance for the Rear Stressed Side Measured Using Flash IV at Low Irradiance (200 W/M^2) 111
14. Percentage Change in Series and Shunt Resistance for the Front Stressed Side Measured Using Flash IV at Low Irradiance (200 W/M^2) 127
15. Backsheet Module With Bifacial PERC Cell Details 131
16. Testing Details 131

LIST OF FIGURES

Figure Page

1. Trends in Renewable Energy [10]..... 2
2. Electricity Generation by Different Solar Technologies [11]..... 2
3. Annual PV Production by Technology [12]..... 3
4. Structure of a Typical PV Module [15]..... 7
5. Structure of a Bifacial PV Module. The Substrate can be TBS, and the Module can be Frameless, too [16]..... 8
6. Three Typical Failure Scenarios for Wafer-Based c-Si Photovoltaic Modules [20]..... 9
7. Outline for the PID Studies..... 14
8. PV System Grounding: A. Negative Pole Grounded; B. Positive Pole Grounded, C. Ungrounded Floating Potential [44]..... 16
9. LC Paths in a PV Module for a Negatively Biased Cell [41]..... 17
10. PID Testing Setup [57]..... 20
11. PID Test Setup for Stressing One Side of a Bifacial Module. Here Front Side is Under Stress, and the Rear Side is at the Same Potential as The Cell [66]..... 22
12. Market Share for Different Cell Technologies. PERC is Most Dominant Among Yellow Highlighted (PERC/PERL/PERT/TOPCON) Technologies With an 80% Share [77], [78]..... 25
13. Market Share for Mono-Facial and Bifacial Cells Used in Mono-Facial and Bifacial PV Modules [77]..... 25
14. Monofacial Al-BSF and PERC Cell [79]..... 26
15. Bifacial PERC and PERT Cell [80], [81]..... 26

Figure Page

16. (A) Transmission Electron Microscope (TEM) Image of a Stacking Fault Showing PID-S, (B To D) EDX Image Using Scanning Transmission Electron Microscope (STEM) for the Same Stacking Fault Near Si/Sin_x Interface [86] 28
17. Suggested Band Diagram for a Na Decorated Stacking Fault [86] 29
18. Change in IV Curves due to PID-P [66] 33
19. EQE Analysis on the Front (A) and Rear (B) [66] 33
20. (A). SEM at the Rear of P-PERC Showing Holes, (B). Magnified SEM of the Hole, (C). TEM Image Showing Missing Sin_x/Alo_x Layers [100] 34
21. PID-P in N-PERT (Front P^+ Emitter) Modules [107] 36
22. EQE Analysis (A) Before PID, (B) 5s, (C) 10s, (D) 20s, (E) 30, (F) 60, And (G) 120s After PID [107] 37
23. PID-P Process Based on K-Centers (A) Before PID, (B) and (C) During PID Under a Negative Bias [107] 39
24. Degradation in Module Parameters due to Multiple PID Processes [114] 40
25. SEM and EDX Images for Front of the N-PERT Cell After PID At -1000V, 85 °C and 480 Hours [115] 42
26. Market Share for Different Encapsulants [77] 46
27. Module Construction Used in the Study 59
28. Cross-Section of the Backsheets Used in this Study. (A) BS-1 (TPT). (B) BS-2. (C) BS-3. (D) BS-4. (E) BS-5. 60
29. Testing Method for the One-Cell Modules 62
30. Test Layout for PID in the Environmental Chamber 62

Figure Page

31. GB Module (Left in Black). GG Module (Right in Red)..... 64

32. Testing Method for the GG and GB Modules..... 66

33. Methodology for (A) Round-1, (B) Round-2, (C) Round-3, (D) Round-4..... 69

34. Testing Method for PID 72

35. PID Recovery Method..... 72

36. Degradation in IV Parameters in The Modules With Different Backsheets..... 74

37. % EL Gray Value and FF Degradation in the Modules With Different Backsheets ... 75

38. EL Images Pre and Post-PID Stress for Modules With Different Backsheets At 100% I_{SC} and 30 S Exposure 76

39. Time Series Plot of LC for 192 H of PID Stress for Modules With Different Backsheets 77

40. Degradation in IV Parameters in the Modules With Different Encapsulants 80

41. % EL Gray Value and FF Degradation in the Modules With Different Encapsulants 81

42. EL Images Pre and Post-PID Stress for Modules With Different Encapsulants at 100% I_{SC} and 30 S Exposure 82

43. Time Series Plot of LC for 192 H of PID Stress for Modules With Different Encapsulants..... 82

44. Degradation in IV Parameters in Modules With and Without AS Coating 84

45. % EL Gray Value and FF Degradation in the Modules With and Without AS Coating 85

46. EL Images Pre and Post-PID Stress for Modules With and Without AS Coating at 100% I_{SC} and 30 S Exposure 86

Figure Page

47. Time Series Plot Of LC for 192 H of PID Stress for Modules With and Without AS Coating 86
48. Degradation in IV Parameters After 2000 Hours Of DH Stress 88
49. Pre and Post-DH EL Images at 100% Isc and 60-Sec Exposure 89
50. Zoomed View Showing the Appearance of Striation Rings in GG-1 and GG-2 Cells Post-DH 89
51. % EL Gray Value Degradation Post-DH Stress 90
52. Degradation in IV Parameters After PID Stress on DH-Stressed Modules 92
53. Pre and Post-PID (After DH) EL Images at 100% Isc and 60-Sec Exposure 92
54. % EL Gray Value Degradation and % Degradation in R_{SH} and R_S Because of PID After DH Stress 93
55. LC Time Series Plot for 192 Hours of PID Stress (Post DH) 94
56. GG-2 (+ve Bias) Module Labels and Circled Cells Which Show Degradation 94
57. Red Arrows Indicate Pre and Post PID (After DH) Reflectance Analysis For The GG-2 Module at The Edge of Cell B7. 95
58. % Pmax Degradation due to DH and PID (After DH) in Both GG Modules 98
59. % EL Gray Value Degradation due to DH and PID (After DH) in Both GG Modules 99
60. Outdoor IR Images Under Short Circuit for Both GG Modules after Sequential DH And PID 99
61. Degradation in IV Parameters After 2000 Hours of DH Stress 101
62. Pre and Post-DH EL Images at 100% Isc and 60-Sec Exposure 101
63. % EL Gray Value Degradation Post-DH Stress 102

Figure Page

64. Degradation in IV Parameters After PID Stress on DH-Stressed Modules 103

65. Pre and Post-PID (After DH) EL Images at 100% Isc and 60-Sec Exposure 103

66. % EL Gray Value Degradation and % Degradation in R_{SH} and R_S Because of PID After DH Stress 104

67. LC Time Series Plot for 192 Hours of PID Stress (Post DH) 105

68. % Pmax Degradation due to DH and PID (After DH) in Both GB Modules 107

69. % EL Gray Value Degradation due to DH and PID (After DH) in Both GB Modules 108

70. Outdoor IR Images Under Short Circuit for Both GB Modules After Sequential DH and PID 108

71. Degradation in IV Parameters for The Rear Stressed Side at 1000 W/M^2 110

72. Degradation in IV Parameters for The Rear Stressed Side At 200 W/M^2 110

73. EL Images For the Rear Stressed Side at 100% I_{SC} and 30-Sec Exposure With Gray Value Change 111

74. Pmax Change for MA-1 and MB-1 for Various States at The Stressed Rear Side at 1000 W/M^2 112

75. I_{SC} Change for MA-1 and MB-1 for Various States at The Stressed Rear Side at 1000 W/M^2 112

76. V_{OC} Change for MA-1 and MB-1 for Various States at the Stressed Rear Side at 1000 W/M^2 113

77. FF Change for MA-1 and MB-1 for Various States at the Stressed Rear Side at 1000 W/M^2 113

Figure Page

78. Pmax Change for MA-1 and MB-1 for Various States at The Stressed Rear Side at 200 W/M^2 114

79. I_{SC} Change for MA-1 and MB-1 for Various States at the Stressed Rear Side at 200 W/M^2 114

80. V_{OC} Change for MA-1 and MB-1 for Various States at the Stressed Rear Side at 200 W/M^2 115

81. FF Change for MA-1 and MB-1 for Various States at The Stressed Rear Side at 200 W/M^2 115

82. EL Sweep Images for the Stressed Rear Side of MA-1 (Post Storage Only) 116

83. EL Sweep Images for the Stressed Rear Side of MB-1 (Post Storage Only) 116

84. EL Change for MA-1 for Various States at The Stressed Rear Side at 100% I_{SC} And 30s Exposure With Gray Value Change 116

85. EL Change for MB-1 for Various States at the Stressed Rear Side at 100% I_{SC} and 30s Exposure With Gray Value Change 116

86. Degradation in IV Parameters for the Front Unstressed Side at 1000 W/M^2 117

87. Degradation in IV Parameters for the Front Unstressed Side at 200 W/M^2 117

88. EL Images for the Front Unstressed Side at 100% I_{SC} and 30-Sec Exposure With Gray Value Change 118

89. Pmax Change for MA-1 and MB-1 for Various States at the Unstressed Front Side at 1000 W/M^2 119

90. I_{SC} Change for MA-1 and MB-1 for Various States at the Unstressed Front Side at 1000 W/M^2 119

Figure Page

91. V_{OC} Change for MA-1 and MB-1 for Various States at The Unstressed Front Side at 1000 W/M^2 120

92. FF Change for MA-1 and MB-1 for Various States at The Unstressed Front Side at 1000 W/M^2 120

93. Pmax Change for MA-1 and MB-1 for Various States at The Unstressed Front Side at 200 W/M^2 121

94. I_{SC} Change for MA-1 and MB-1 for Various States at The Unstressed Front Side at 200 W/M^2 121

95. V_{OC} Change for MA-1 and MB-1 for Various States at the Unstressed Front Side at 200 W/M^2 122

96. FF Change for MA-1 and MB-1 for Various States at the Unstressed Front Side at 200 W/M^2 122

97. EL Sweep Images for the Unstressed Front Side of MA-1 (Post-Storage Only)..... 123

98. EL Sweep Images for the Unstressed Front Side of MB-1 (Post-Storage Only)..... 123

99. EL Change for MA-1 for Various States at The Unstressed Front Side at 100% I_{SC} and 30s Exposure With Gray Value Change 123

100. EL Change for MB-1 for Various States at the Unstressed Front Side at 100% I_{SC} and 30s Exposure With Gray Value Change 123

101. Average LC Data for 168h of Stress and Log Scale LC Plots for the First 900s of Stress (Stabilized After 300s) 124

102. Degradation in IV Parameters for the Front Stressed Side at 1000 W/M^2..... 127

103. Degradation in IV Parameters for the Front Stressed Side at 200 W/M^2..... 127

Figure Page

104. EL Images for the Front Stressed Side at 100% I_{SC} and 30-Sec Exposure With Gray Value Change 128

105. Degradation in IV Parameters for the Rear Unstressed Side at 1000 W/M^2 129

106. Degradation in IV Parameters for the Rear Unstressed Side at 200 W/M^2 129

107. EL Images for the Rear Unstressed Side at 100% I_{SC} and 30-Sec Exposure With Gray Value Change 130

108. Average LC Data for 168h of Stress and Log Scale LC Plots for The First 900s of Stress (Stabilized After 300s) 130

109. Pmax Change for ME-1 for Various States at 1000 W/M^2 132

110. I_{SC} Change for ME-1 for Various States at 1000 W/M^2 132

111. V_{OC} Change for ME-1 for Various States at 1000 W/M^2 133

112. FF Change for ME-1 for Various States at 1000 W/M^2 133

113. EL Change for ME-1 for Various States 100% I_{SC} and 30s Exposure With Gray Value Change 134

114. Degradation in IV Parameters for the Front Stressed Side at 1000 W/M^2 135

115. Degradation in IV Parameters for the Front Stressed Side at 220 W/M^2 135

116. EL Images for the Front Stressed Side at 100% I_{SC} and 30-Sec Exposure With Gray Value Change 136

117. Degradation in IV Parameters for the Rear Unstressed Side at 1000 W/M^2 137

118. Degradation in IV Parameters for the Rear Unstressed Side at 200 W/M^2 137

119. EL Images for the Rear Unstressed Side at 100% I_{SC} and 30-Sec Exposure With Gray Value Change 138

Figure Page

120. Average LC Data for 168h of Stress and Log Scale LC Plots for The First 900s of Stress (Stabilized After 300s) 138

121. Degradation in IV Parameters for the Rear Stressed Side at 1000 W/M^2 140

122. Degradation in IV Parameters for the Rear Stressed Side at 200 W/M^2 140

123. EL Images for the Rear Stressed Side at 100% I_{SC} and 30-Sec Exposure With Gray Value Change 141

124. Degradation in IV Parameters for the Front Unstressed Side at 1000 W/M^2 142

125. Degradation in IV Parameters for the Front Unstressed Side at 200 W/M^2 142

126. EL Images for the Front Unstressed Side at 100% I_{SC} and 30-Sec Exposure With Gray Value Change 143

127. Average LC Data for 168h of Stress and Log Scale LC Plots for The First 900s of Stress (Stabilized After 300s) 143

CHAPTER 1: INTRODCUTION

1.1 Global Solar Outlook

Global energy consumption has exponentially increased because of urbanization and continual growth in the world population. Moreover, the environmental damage caused by the continuous use of fossil fuels and the limited duration for which fossil fuels may be utilized has prompted the usage of renewable energy sources [1], [2]. Solar energy is one of the fastest-growing renewable energy resources. There are two main types of solar technologies, i.e., concentrated solar power (CSP) and solar PV [3]. Among both solar technologies, PV accounts for more than 95% of capacity and generation. Moreover, solar PV accounts for 3.6% of global electricity generation, making it the third most significant renewable energy source behind hydropower and wind [4], [5].

Solar PV is based on the photovoltaic effect whereby incoming photons are converted to voltage [6] discovered by Edmond Becquerel in 1839 [7], [8]. The first silicon solar cell was made in 1954 at Bell laboratories. There are various types of solar PV technologies, namely, crystalline silicon (c-Si) (mono and poly/multi), thin film, III-V, and some next-generation technologies (organic, quantum dots, perovskites) [9]. C-Si has the most significant market (over 95%) share of all the current PV technologies. Figures 1 to 3 below show some of the abovementioned solar energy and PV statistics.

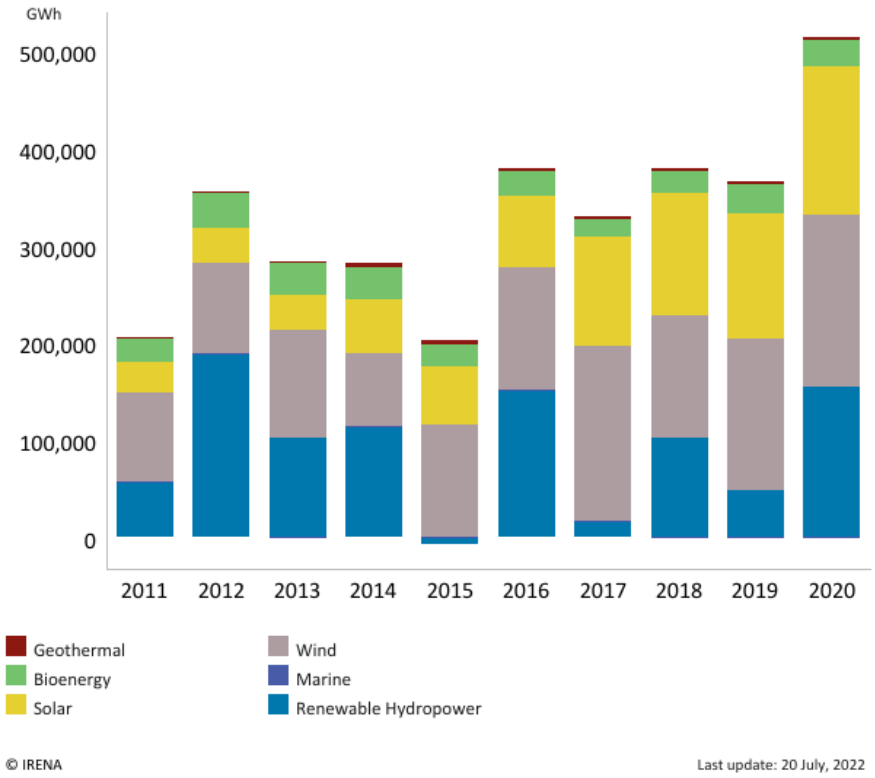

Fig. 1. Trends in Renewable Energy [10]

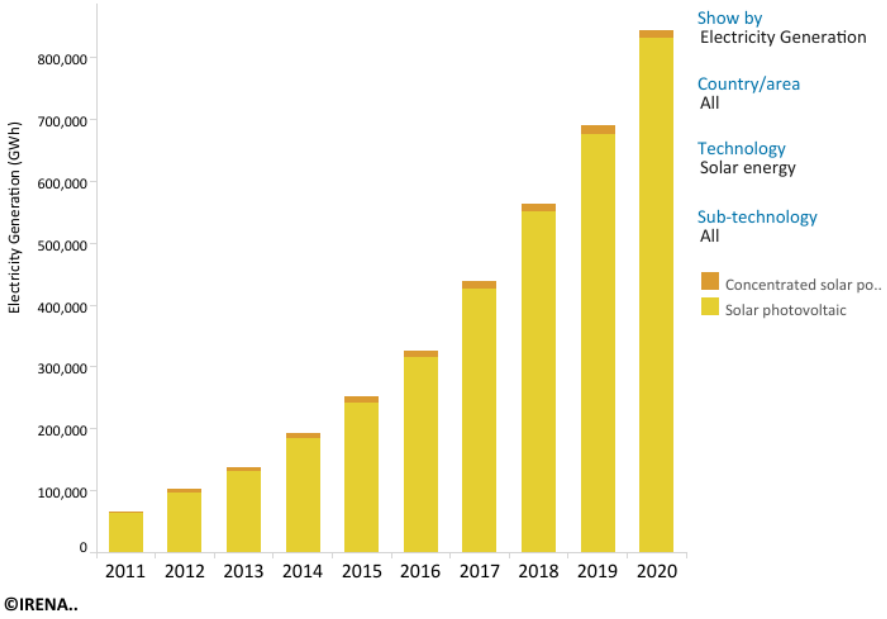

Fig. 2. Electricity generation by different solar technologies [11]

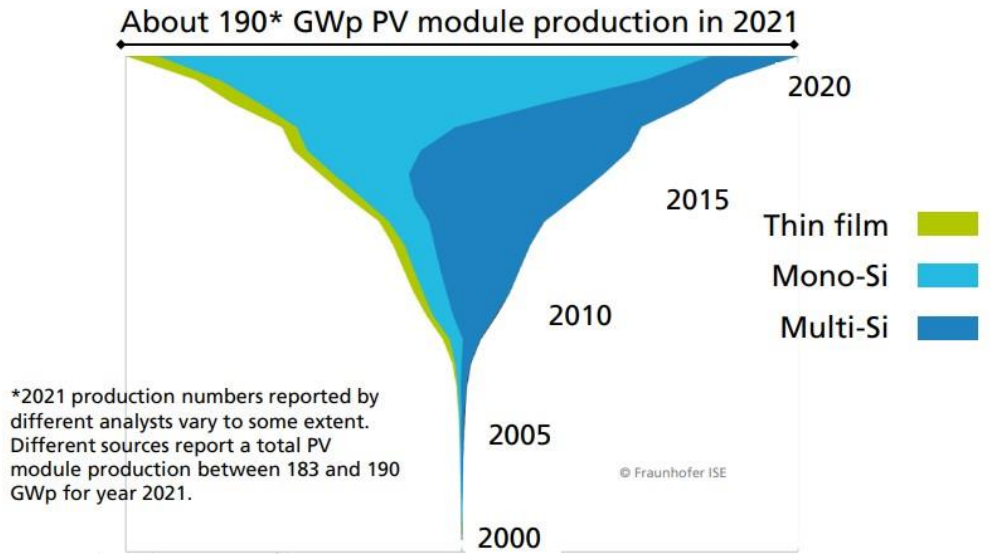

Fig. 3. Annual PV production by technology [12]

1.2 PV module components

A PV module is made up of various components. Typically, the following structure is followed, i.e., superstrate (front glass), encapsulant, solar cells, encapsulant, substrate (backsheet or glass), and a frame (may or may not be used depending on the construction). The materials used in the module construction must be of high quality to ensure a long module lifetime and a better levelized cost of energy (LCOE). Fig. 4 below shows the typical components of a PV module, and Fig.5 shows a bifacial module construction.

Solar Cells*:* The solar cell is an essential component of a PV module that converts light (photons) to electrical output. As mentioned above, various types of cells are available, but most of the market is dominated by c-Si solar cells. The efficiency of the PV module varies depending on the type of c-Si cell used, either mono-crystalline (more efficient due to high purity level of silicon) or poly-crystalline (less efficient due to low purity of silicon and more grain boundaries). The PV cell's foundation is a very thin wafer, generally 0.1mm

thick, consisting of either positive p-type silicon or negative n-type silicon. An anti-reflective coating (ARC) is also present on the cell. Busbars and metallic fingers (typically made using screen-printed silver) on the cell surface collect the electrons produced in response to the incoming photons. Cell interconnects feature a copper core covered with lead-tin solder and connects cells in series [13]. There are several cell sizes and configurations (series or parallel connection), each with a distinct efficiency level; these include standard full cells, half-cut cells, shingled cells, multi-bus bar cells, and interdigitated back contact cells [14].

Superstrate/Front Glass: The superstrate is a high-strength, low-iron tempered glass that is 2.5 to 3.5 mm thick and is built to withstand multiple field stressors. The glass used is highly transparent for efficient light transmission for better performance. An ARC coating on the rear of the glass is also used to enhance light transmission. The front glass shields the PV cells from hail and extreme weather conditions. According to the International Electrotechnical Commission (IEC) standard, the PV modules must resist an impact from hail stones with a diameter of 1 inch flying up to 60 mph. Tempered glass is also significantly safer than regular glass in the case of an accident since it shatters into small fragments instead of razor-sharp pieces [14].

Encapsulant: The encapsulant is a precisely engineered polymer, a highly transparent covering used to enclose and hold cells during manufacturing. The encapsulant material must be exceptionally robust and resistant to severe temperatures and humidity, and it contributes significantly to the long-term performance by avoiding moisture ingress in PV

modules. The encapsulant is placed on both sides of the cells, absorbs stresses, and protects the cells and connected wires from vibrations and immediate impact. The cells are initially encased with encapsulant before being integrated into the superstrate and substrate during production. The most popular and widely used encapsulant is ethylene vinyl acetate (EVA). Some newer and much better encapsulants, such as Polyolefin Elastomer (POE), are also entering the market but are still not widely used due to higher costs [14].

Substrate: The substrate is the layer at the rear of a PV module that serves as a moisture barrier and exterior skin to offer mechanical and electrical insulation. In traditional modules, the substrate is usually a backsheet material composed of several polymer materials that give the module protection, thermal stability, and ultra-violet (UV) resistance. In conventional mono-facial modules, the backsheet layer is usually opaque and either white or black. But with the advent of bifacial modules, which can produce power from both front and rear transparent backsheets are also being used. Furthermore, bifacial modules (also some mono-facial frameless modules) sometimes employ a glass material as the substrate instead of a polymer backsheet. The polymer backsheet and rear glass have pros and cons as the substrate, which is discussed more deeply in the literature review section [14].

Frame: The module frame is usually made of anodized Aluminum (Al) and plays a crucial role in preserving the edge of the laminate. Edge sealants are also placed under the frame lining to prevent moisture ingress at the edge of PV modules. The frame provides a sturdy mounting structure for the PV modules and is meant to be lightweight, rigid, and capable

of handling various mechanical stressors. Depending on the manufacturer, the frame can be silver or black, and the corner portions can be screwed, pressed, or clamped together to provide varying levels of strength and rigidity. Most modules are built with a frame, but there are also some constructions where a frame is not used, typically bifacial and glass-glass modules [14].

Junction Box and Module Connectors: The junction box is on the back of a PV module. It is designed to be weatherproof as it houses the cell interconnect sets and the bypass diodes (to prevent reverse currents). The junction box is also needed to secure the wires to connect the PV modules in strings. Multi-contact, 4 mm (MC4) connectors are used for module interconnection. These weatherproof connectors maintain an excellent electrical connection between modules with minimum resistance, as absolute PV system voltages can be as high as 1500 V [14].

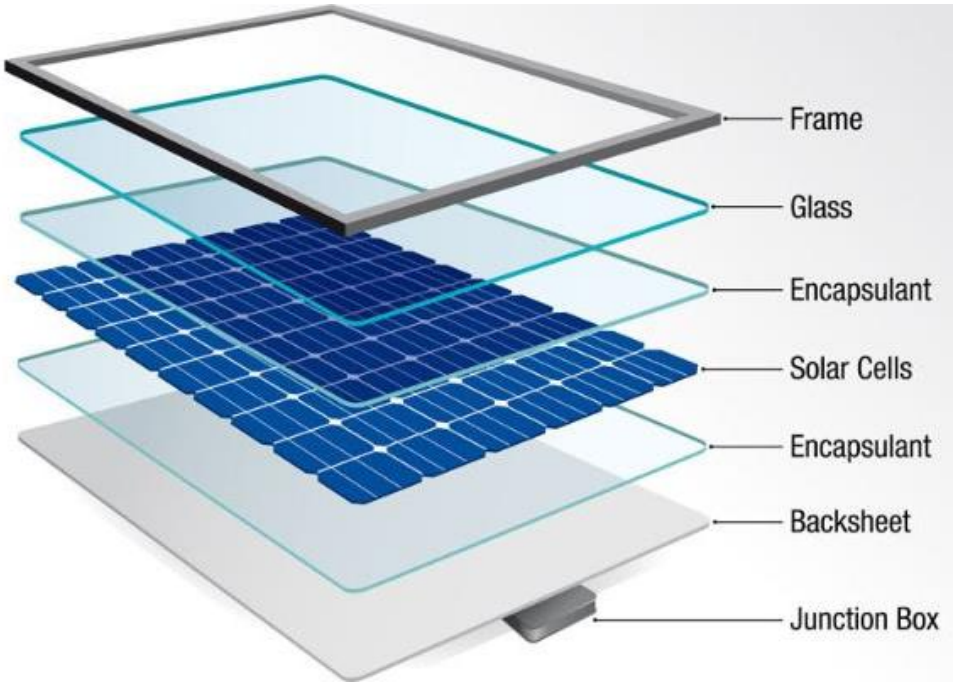

Fig. 4. Structure of a typical PV module [15]

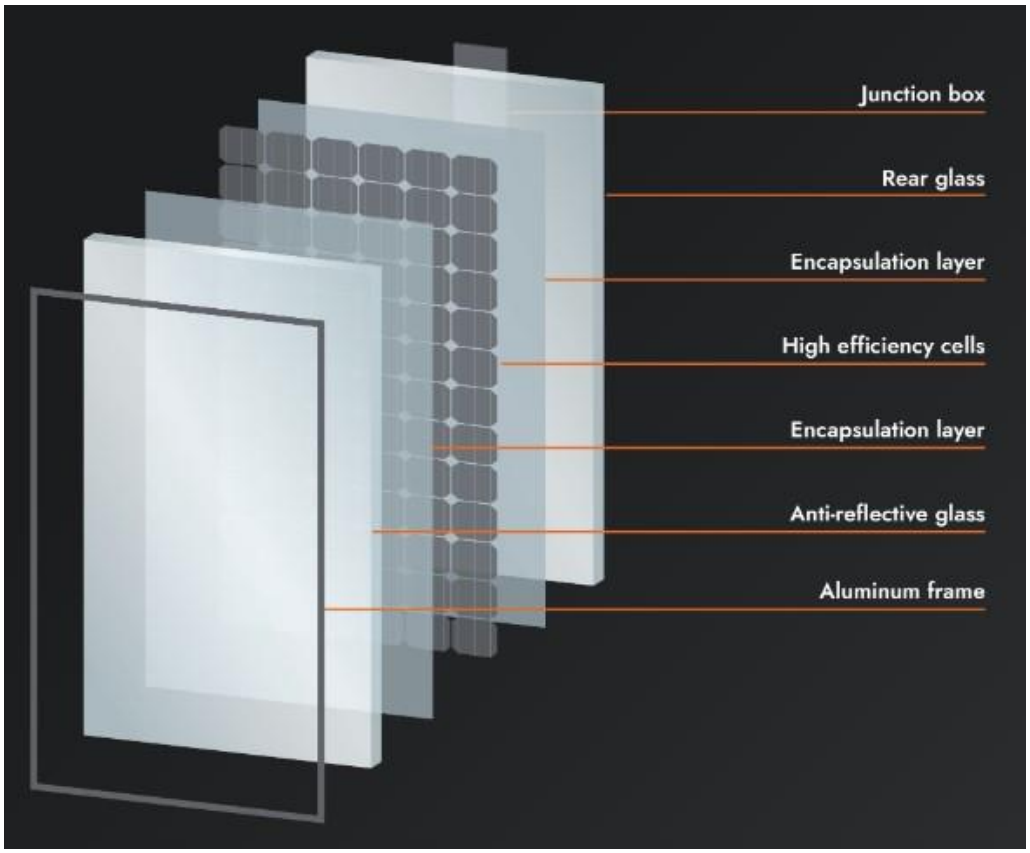

Fig. 5. Structure of a bifacial PV module. The substrate can be TBS, and the module can be frameless, too [16]

1.3 PV Module Degradation and Reliability

PV modules are subjected to numerous internal and external stressors that impact their performance and reliability during field operations [17] . Internal stressors are usually caused by the composition of the PV modules and processing-related impacts, such as poor module manufacturing techniques and incompatibility in the bill of materials (BOM). External stressors are mainly due to ambient conditions, including irradiance (UVA and UVB components), temperature, moisture/ humidity, mechanical loads, soiling, voltage, and harmful chemicals/ pollutants [18], [19]. These internal and external stressors can lead to module degradation and failure. These can be divided into three main classifications: Infant-failure, midlife failure, and wear-out-failure. Infant failures mainly occur due to

faulty PV modules. Midlife failures primarily include interconnect issues, glass breakage, junction box failure, cell issues, encapsulant, and backsheet failure. Wear-out-failures appear at the end of the module's life and typically include delamination, cell cracks, and encapsulant discoloration [20]. Fig. 6 shows the typical failure modes for PV modules.

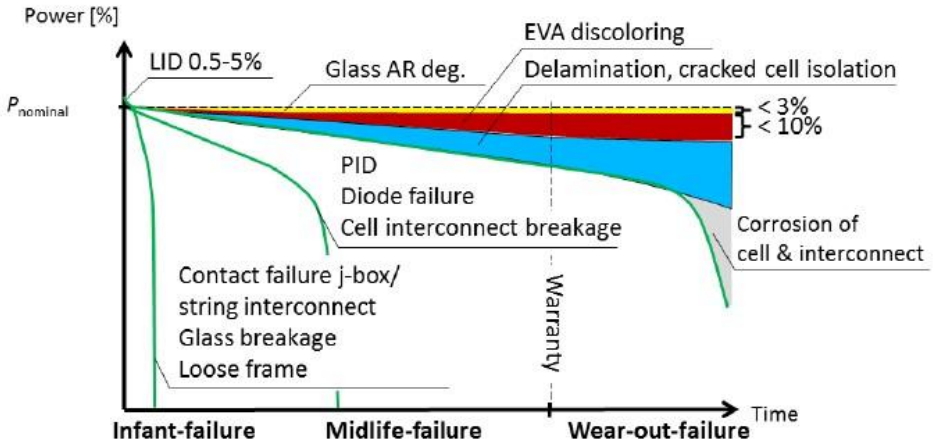

Fig. 6. Three typical failure scenarios for wafer-based c-Si photovoltaic modules [20]

As per the National Renewable Energy Lab (NREL) database, the most common degradation modes in PV modules over the previous decade include hotspots (33%), ribbon discoloration (20%), glass breakage (12%), encapsulant discoloration (10%), cell breakage (9%) and PID (8%) [21].

Hotspots: Hot spots are regions of a PV module with high temperatures that may damage the cells or other components of the module [22], [23]. Hot spots can be caused by cellular obstructions, including cell shadowing, mismatched cells, and interrupted cell connections [24]. If the cell is under such conditions, the voltage can reverse, becoming equal and opposite to the other cells connected in series. Consequently, the defective solar cell puts

unnecessary strain on the remaining cells in series resulting in high heat-dissipation sites, which lead to the formation of hot spots [21], [25].

Corrosion and Ribbon/Encapsulant Discoloration: One of the most prevalent issues in the field and the cause of ribbon discoloration is the corrosion of PV modules [26]. Corrosion processes are usually linked to other deterioration processes [27]. Therefore, it is difficult to identify the origin of a module's corrosion. Corrosion occurs in the presence of an electrolyte, oxidizing agent, and metal [28]. Any PV module component that starts to deteriorate has a higher chance of corroding, which allows water and oxygen to enter the module. Mainly, corrosion is significantly influenced by the degradation of the backsheet and encapsulant [29]. When the PV module operates in environments with high UV, temperature, and humidity, EVA (the most widely used encapsulant) degrades, forming acetic acid, which speeds up metal corrosion. Metals with lower oxidation potential corrode at higher rates. Due to contact with water, the solder joint edges on the front of the cell start to corrode. The corrosion process then gradually moves toward the center, which causes the silver (Ag)-solder contact to deteriorate, raising the series resistance [30]. On the rear of the cell, corrosion can cause the Al-solder bond degradation. Subsequently, other metals also start corroding as the corrosion process continues.

Due to the formation of acetic acid under the conditions mentioned above, the color of EVA also changes to yellow or brown; this causes encapsulant discoloration, which can lead to a reduction in photons that can reach the cell, thus reducing module power [31].

Delamination: PV module delamination can occur due to adhesion loss between the cell and encapsulant. In environments with high temperatures and humidity, moisture ingress can lead to a loss in the encapsulant's adhesive bonds, promoting delamination [32].

Cell and Module Breakage: PV module and cell breakage usually occur during transportation, installation, or maintenance. Sometimes high winds or hail can also damage the modules. Damaged PV modules or cells can operate at lower efficiencies but are still a safety hazard due to electric shocks. Also, breakage can increase moisture penetration, leading to other degradation processes within the module and cell [21].

To lower the LCOE of solar energy, the performance and lifetime of PV modules must be improved, and they should have high reliability. Therefore, it is necessary to study the reliability of PV modules as multiple degradation processes are occurring in the field, as mentioned above. Although, it is challenging for the industry to monitor degradation in the field throughout the module lifetime (25+ years) to improve module reliability. Therefore, PV modules are stressed using accelerated testing methods to determine the degradation and failure modes so that new developments to improve module performance and reliability can be done as fast as possible [33]. Usually, various pre-and post-characterization tests are done throughout the accelerated stress testing to determine which module parameters are most affected. These outcomes then help in enhancing PV module durability and reliability. Generally, IEC 61215 and other IEC standards are used in accelerated stress testing [21].

1.4 Motivation and Outline

Numerous PV reliability issues have been discussed in the section above. Many of these have been researched and substantially reduced. PID is a relatively new reliability problem observed in 2005, and it can cause a reduction in the module power output of more than 40% in a relatively short time frame [34], [35]. Consequently, PID can be a massive problem for the PV industry and manufacturers as PV has grown exponentially in the past decade, as indicated in Fig.1 to 3. Furthermore, the problem is more prevalent in c-Si PV modules. As they currently dominate the PV market, it becomes imperative to understand and reduce the PID issue in new and already installed PV modules. Hence, it is essential to comprehend the impact of PID in PV modules due to the influence of different PV components to facilitate better designs to tackle the PID issue. Therefore, this work aims to understand the influence of PID due to PV superstrate, encapsulant, and substrate in c-Si PV modules. The study also aims to provide post-manufacturing PID recovery and prevention methods and explain and understand varying PID mechanisms. The main problems that this work aims to address are discussed below:

- Study based on one-cell modules
    - What is the impact of PID due to different backsheet structures (substrates) in a PV module, and what type of PID mechanisms can occur?
    - How do different encapsulant types affect PID, and what is the best combination for the backsheet and encapsulant to overcome or reduce PID?

- Can the use of an Anti-soiling (AS) coating on the front glass help in preventing PID?

➢ Study based on DH-stressed GB and GG modules

- How do traditional GB and emerging GG/ bifacial modules behave when subjected to PID with reduced interface-adhesion strengths due to accelerated DH stress?
- What are the different PID mechanisms that can occur in different polarities in both GB and GG modules?

➢ Study based on fresh bifacial modules

- What is the susceptibility of PID in different configurations of the newly emerging bifacial modules, i.e., glass-transparent backsheet (G-TBS), GG-framed, and GG-frameless modules?
- What is the impact of PID, and what PID processes can occur on the rear and front of these new bifacial technologies under both negative and positive bias?
- What recovery mechanism can be used to reduce the impact of PID in these bifacial modules?

The rest of the dissertation is organized in the following way. Chapter 2 details a literature review on PID and its impact on PV modules. Chapter 3 discusses the methodology for this study's experimental work. Chapter 4 presents and discusses the results obtained from the experiments in chapter 3. Chapter 5 presents the conclusions of the study with relevant future perspectives. The figure below shows the outline of the work.

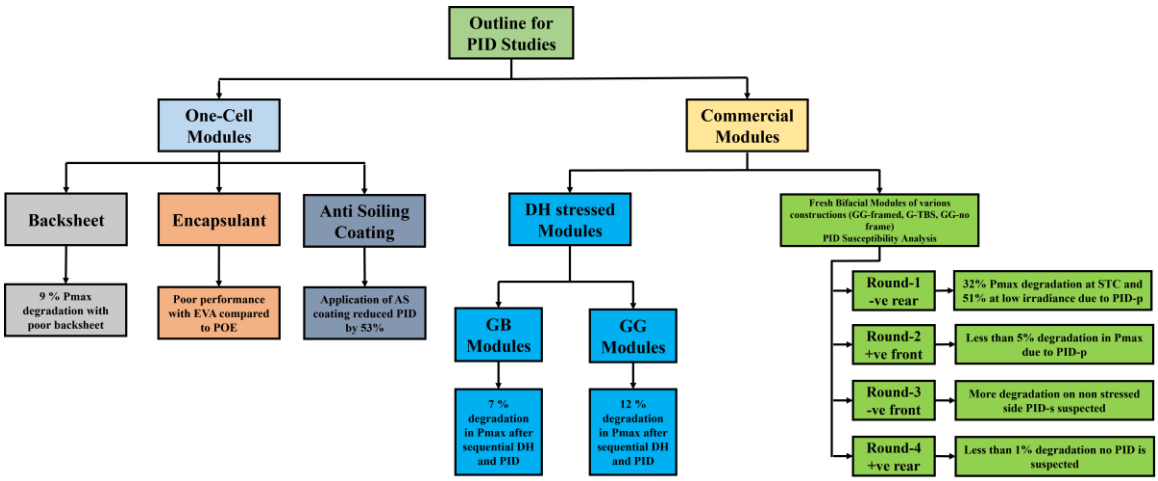

Fig. 7. Outline for the PID studies

CHAPTER 2: LITERATURE REVIEW

For c-Si and thin-film modules, the Jet Propulsion Laboratory (JPL) initially reported PID in 1985 [36]. Florida Solar Energy Center (FSEC), NREL, and BP Solar also looked at the possible dangers of high system voltage stress on different PV modules in the early 2000s [37]. In 2005 PID was observed for the first time in the field-operated PV modules (rear-junction n-type c-Si) made by SunPower in an outdoor test array in Germany [38]. The process was also observed in Evergreen's modules in 2008 [39]. In 2010 Pingel et al. devised the term PID to describe these processes [40].

There are multiple issues on PID that researchers must address. Several factors can impact PID, like the ARC on the cell, encapsulant in the module, backsheet type, front or rear glass, framed or frameless construction, and grounding configuration. Moreover, ambient conditions such as light, humidity, temperature, and dirt accumulation on the module can also play a role in influencing the PID mechanisms. The development of entirely PID-free PV modules has been hampered by the intricacy of PID and its poor understanding [41]. Consequently, this study aims to answer some of the questions relating to PID so that a better understanding can be obtained.

2.1 PV System Configuration

PV modules are typically connected in series to ensure efficient system operation. Additionally, for safety purposes, the frames of PV modules are grounded. In large PV systems, arrays of PV modules are connected to inverters for converting DC to AC power to be exported to the grid. Previously, transformer-based inverters have been used, which need either negative or positive pole grounding for operation. Transformerless inverters are becoming more common in PV systems to reduce costs. Transformerless inverters

cannot be grounded, so the PV system has a floating potential. Based on the inverter used in the PV system, the PID process can occur when leakage currents flow from the module frame to the solar cells or the other way around as per the module's bias and location in the string. Since the absolute voltage of PV systems is expected to increase (from 1000V to 1500V) to reduce expenses, the PID problem can become more acute in the future [42]. PV system grounding is illustrated in Fig.8 below. It can be observed that in configurations a and b, the modules at the end are either under positive or negative bias. In contrast, in configuration c, there is a floating potential where half of the modules are under negative bias, and the other half are under positive bias [43].

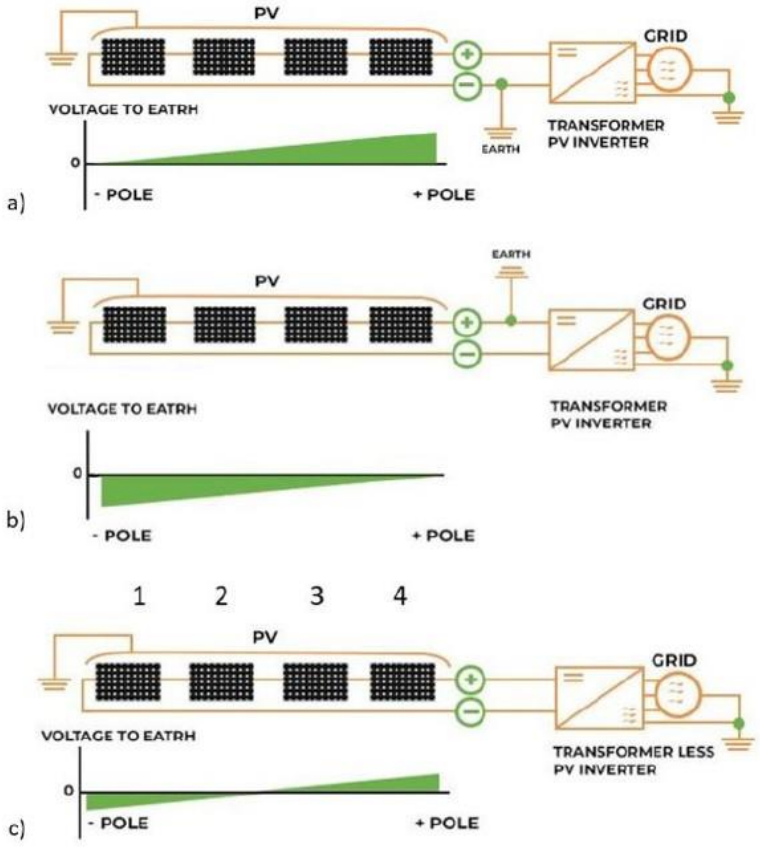

Fig. 8. PV system grounding: a. negative pole grounded; b. positive pole grounded, c. ungrounded floating potential [44]

2.2 Pathways for Leakage Current (LC)

The system configuration (Fig. 8) used in a PV system determines the polarity/bias experienced by the modules. Moreover, the magnitude of the potential difference between the solar cell and the grounded module frame is determined by the module's location in the string. The potential difference between the cell and frame leads to the development of an electric field. If the cells are negatively biased to the grounded frame, the direction of the electric field (positive charges flow in the same direction as the electric field) is towards the cell. In contrast, when the cells are positively biased to the grounded frame, the electric field is towards the frame. Since the superstrate, encapsulant, and substrate are not pure insulators, the build-up of an electric field can cause the flow of LC through the module, leading to the progression of PID. Fig. 9 shows a negatively biased cell's LC paths in a PV module. Each numbered path from 1 to 6 is detailed below [41]. The direction of the red arrows in Fig.9 would be reversed for a positively biased cell.

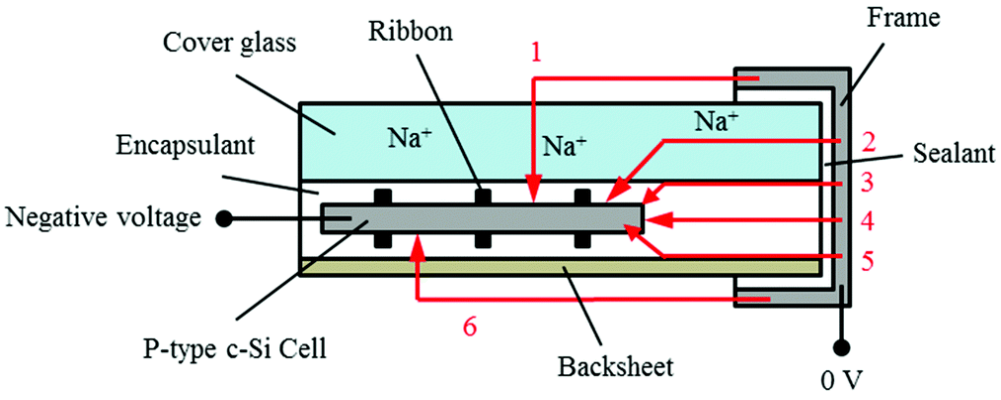

Fig. 9. LC paths in a PV module for a negatively biased cell [41]

1) The surface of the superstrate (front glass) and the bulk of the superstrate and encapsulant
2) The bulk of superstrate and encapsulant

3) The boundary between superstrate and encapsulant and the bulk of encapsulant
4) Majority of the encapsulant
5) The boundary between the encapsulant and substrate (backsheet/TBS/glass) and the bulk of the encapsulant
6) The surface of the substrate and the bulk of the substrate and encapsulant

In the LC paths mentioned above, path number 1 is typically the most damaging for the module due to the increased conductivity of the superstrate/front glass in humid environments [45]. As the backsheet material (normal backsheet or TBS) has good insulation and electrical resistance [46], the LC path 6 is frequently overlooked. But if a backsheet has poor construction or very high-water uptake capacity, LC through path 6 cannot be neglected. Moreover, backsheets can also degrade during field operation due to moisture ingress, increasing the LC through path 6 [47], [48]. Furthermore, if the substrate used in the module is glass, like in many new bifacial constructions, that can also significantly increase the LC through path 6 due to the increased conductivity of glass under humid conditions [49]. Although, if the GG module is, the frameless magnitude of LC can be reduced as they have metallic clamps for mounting instead of a full-frame [50].

There is no direct correlation between LC and PID [51]. One reason could be the simultaneously happening PID recovery and degradation process. It is also observed that the diffusion processes constrain the degradation, and the rate of PID does not change with the LC above a specific level of surface conductivity [52]. Along with moving from the front glass through the encapsulant to the dielectric layer, a part of the LC also moves from the glass to the metallic contacts and connecting ribbons of the cells, leading to PID on the cell. Furthermore, the characteristics such as conductivity and passivation of the SiN_x ARC

and dielectric layers (AlO_x and SiO_x) can also influence the intensity and rate of PID. For instance, an increase in the conductivity of the ARC can allow more LC but exhibit reduced PID due to a decline in the Na^+ transmission [40]. Consequently, LC can act as an indicator for PID but not as a measure for PID [43].

2.3 Testing Methods for PID

Indoor Testing at the Module Level: Indoor testing for PID was initially introduced by JPL [53]. Currently, two main methods exist for indoor PID testing of PV modules. Method 1 utilizes an environmental chamber with DH conditions at a temperature of 60 °C ± 2 °C and relative humidity (RH) at 85 % ± 3 % for a duration of 96 h. Method 2 uses an Al foil on the surface of the PV module at a temperature of 25 °C ± 1 °C and RH of less than 60% for 168 h. In both cases, a potential difference, typically 1000 V (or 1500 V), is applied between the cell and the module frame or foil. The polarity can be negative or positive depending on the intended test, and LC is also monitored. Fig.10 shows a typical test setup.

In method 1, the moisture forms a layer of water on the surface of the module, acting as a conducting film. Due to the uneven distribution of water vapors on the module, a non-uniform electric field is formed, which is more field-representative. In contrast, in method 2, the Al foil acts as a conducting layer that forms a uniform electric field; however, the Al foil method is cheaper owing to lower temperature and humidity requirements. Furthermore, both methods are carried out under dark conditions, which is not characteristic of field conditions. Since other factors can also influence PID in the field, control modules are usually used to better understand PID dynamics [54]. Both these methods have been set as per IEC testing standard 62804-1 “Photovoltaic (PV) modules - Test methods for the detection of potential-induced degradation - Part 1: Crystalline

silicon" [55]. The conditions in the standard are set so that outdoor environmental conditions are closely matched [56]. But occasionally, the temperature, humidity, dwell time, and voltage conditions for both methods, as set in the IEC standard, are changed depending on the test's purpose [57].

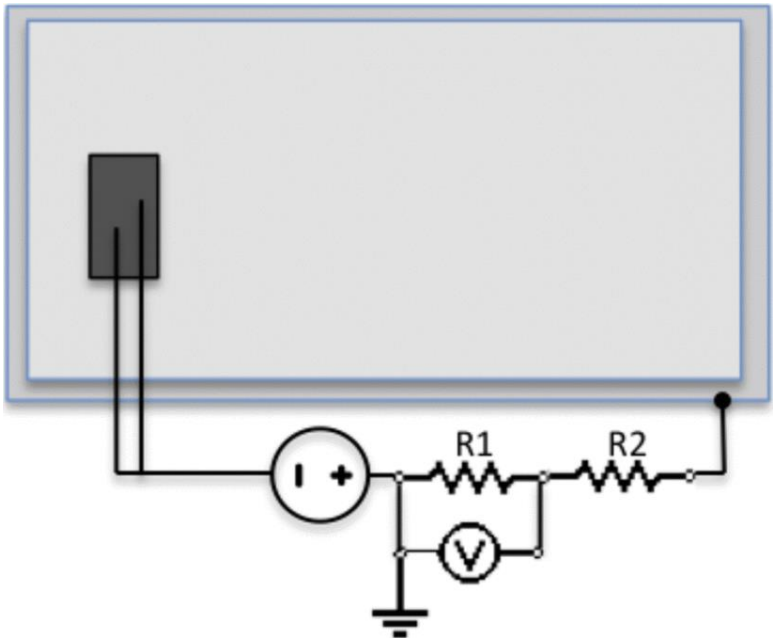

Fig. 10. PID testing setup [57]

Some new IEC standards are also established mainly for bifacial PV modules to understand the influence of light on the module rear in recovering specific PID processes [40], [58]. Consequently, the DH test at 85 °C, 85 % RH for 96 h with voltage bias from IEC 62804-1 was included in IEC 61215-2:2021 "Terrestrial photovoltaic (PV) modules – Design qualification and type approval – Part 2: Test procedures" [59]. Moreover, IEC 61215-1-1 "Terrestrial photovoltaic (PV) modules - Design qualification and type approval - Part 1-1: Special requirements for testing of crystalline silicon photovoltaic (PV) modules" [60] includes recovery of the rear side of bifacial modules by exposing them to an irradiance of 2 kWh/m^2. The testing is mainly intended for PID-shunting (PID-s) and

does not focus on PID-polarization (PID-p). Moreover, other critiques include that the rear side of bifacial modules experiences low irradiance in the field. Furthermore, PID-p mechanisms can occur on either side of the module; hence, light recovery should be done on both sides.

A new method for PID testing under light conditions was done using a grounded electrolytic jell on the module surface for humidity/moisture. The jell was covered by a thin transparent layer of Polyethylene terephthalate (PET) for UV transmission and prevention of jell evaporation as module temperature increases [61]. Another method uses a transparent conductive oxide (TCO) layer to provide surface conduction [62]. To incorporate new PID testing methods, a new version of IEC 62804-1 is underway [63]. Some other methods test modules in extended DH stress to reduce interface adhesion strengths. A potential difference is applied afterward to observe PID leading to corrosion and delamination [64].

An alteration is done for bifacial PV modules only to understand PID dynamics on one side using the Al foil method. Both sides are covered with the Al foil, with the stressed side at an opposite potential to the cell and the non-stressed side at the same potential as the cell, avoiding unnecessary stress at the non-stressed side [65], [66]. Fig. 11 shows the test setup.

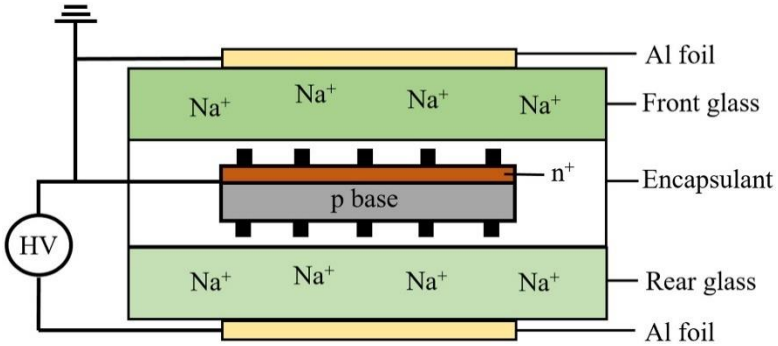

Fig. 11. PID test setup for stressing one side of a bifacial module. Here front side is under stress, and the rear side is at the same potential as the cell [66]

Indoor Testing at the Cell Level: The corona discharge technique has been used for PID analysis at the cell level for non-encapsulated cells [67]. The method uses the tip of a thin wire under a high voltage to produce positive ions to be deposited on the cell's surface. However, this method does not produce reliable results as it can change the characteristics of the ARC. Consequently, new techniques have been established to pack the cell between encapsulant and glass to mimic a laminated module [68]. This method has grown popular [69] and provides better results that are comparable to module-level PID analysis [70].

Outdoor Testing: Modules in the field are affected by various factors (rain, soiling, heat, irradiance, etc.) simultaneously and can be hard to emulate during indoor tests. Furthermore, the PID stress is not continuous in outdoor conditions compared to indoor testing methods. Therefore, field testing of PV modules is essential to fully understand PID. However, as numerous variables are at play in outdoor conditions, evaluating PID data when using outdoor tests can be challenging. In this regard, indoor tests are ideal as the effect of each variable can be studied easily [71].

Typically, PV modules are connected to a load or a power optimizer unit for outdoor testing, and one terminal is supplied with the system voltage. LC is also measured, and a reliable mounting configuration is used to prevent unnecessary LC paths. Generally, IV curves are used to monitor the system using multi-curve IV tracers. Control modules under unbiased conditions are also used throughout testing to isolate the effect of other variables [72].

Characterization techniques: Primarily the following characterizations are used to understand the module-level PID. These include IV curve analysis, Electroluminescence (EL), Photoluminescence (PL), Dark IV (DIV), UV fluorescence (UVF) imaging, infrared (IR) imaging, reflectance spectrophotometry, external quantum efficiency (EQE) and internal quantum efficiency (IQE). To understand PID at the cell level, coring techniques are used [73] to isolate module components. Techniques such as thermogravimetric analysis (TGA), differential scanning calorimeter (DSC), Raman spectroscopy, Fourier transform infrared spectroscopy (FTIR), scanning electron microscopy (SEM), scanning transmission electron microscopy (STEM), X-ray diffraction (XRD), energy dispersive X-ray spectroscopy (EDX), secondary ion mass spectroscopy (SIMS) and electrochemical impedance spectroscopy (EIS) are used to understand the physical, structural and chemical properties of the isolated components like cell and encapsulant [74]. Recently, EIS has been utilized to comprehend various PID mechanisms and understand degradation in electrical parameters in PID-affected cells [75]. For example, the Nyquist plot obtained using EIS shows a decline in shunt resistance (R_{SH}) due to cell cracking, but if the cell is affected by PID, the plot shows a reduction in both R_{SH} and capacitance [76]. Since non-

uniformity can also be measured using this technique, researchers can differentiate between PID-s and PID-p [43].

2.4 PID mechanisms

Various PID mechanisms can occur in PV modules, and different module technologies can have varying PID processes. Even the same type of modules can have different degradation modes due to PID when the stress conditions are changed [41]. This section discusses the main c-Si cell structures, and then the impact of PID on these different module technologies is explained.

Cell Technologies: Initially, the market for c-Si solar cells used in PV modules was dominated by mono facial aluminum back surface field (Al-BSF) cells. But with the advent of bifacial cells and enhancements in the cell structure, newer technologies like passivated emitter rear contact (PERC) are now leading in the PV industry [77]. PERC cells were initially marketed as mono-facial cells but are currently manufactured as bifacial cells. Bifacial cells can collect photons at the front side and have a metallization structure at the rear, allowing photons to be absorbed at the backside. In contrast, mono-facial cells only allow light to be absorbed at the cell front and have a full rear metallization. Many other cell technologies have also been developed. They are usually marketed as bifacial cells such as passivated emitter rear totally diffused (PERT), passivated emitter rear locally diffused (PERL), tunnel oxide passivated contact (TOPCON), interdigitated back contact (IBC) and heterojunction (HJT). Fig. 12 shows the market share for different c-Si cell technologies, and Fig. 13 shows the market share for mono-facial and bifacial cells used in PV modules.

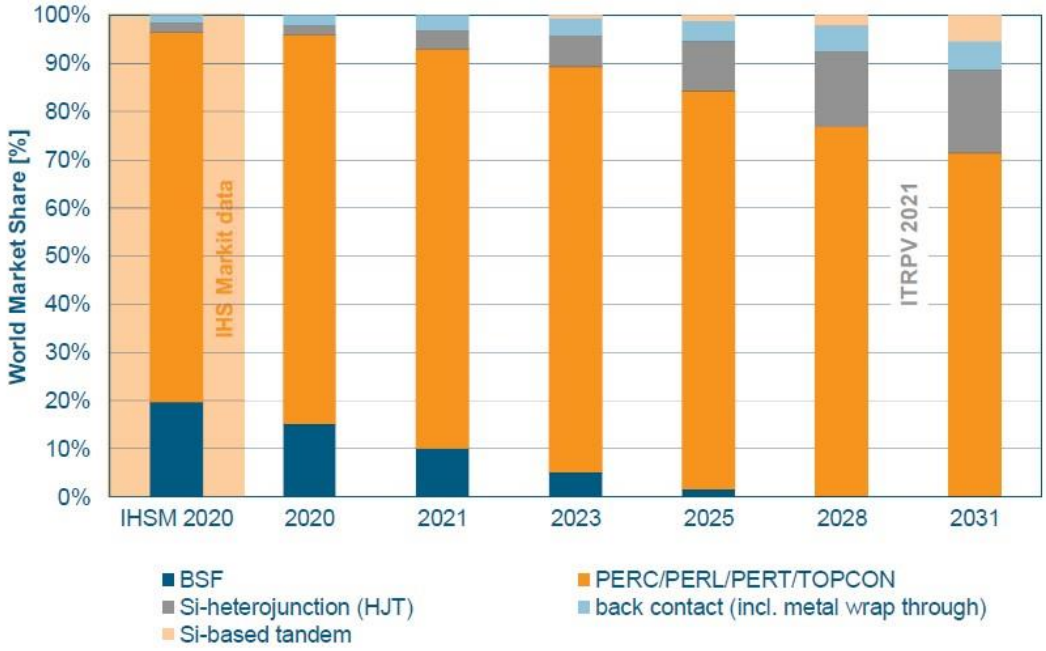

Fig. 12. Market share for different cell technologies. PERC is most dominant among yellow highlighted (PERC/PERL/PERT/TOPCON) technologies with an 80% share [77], [78]

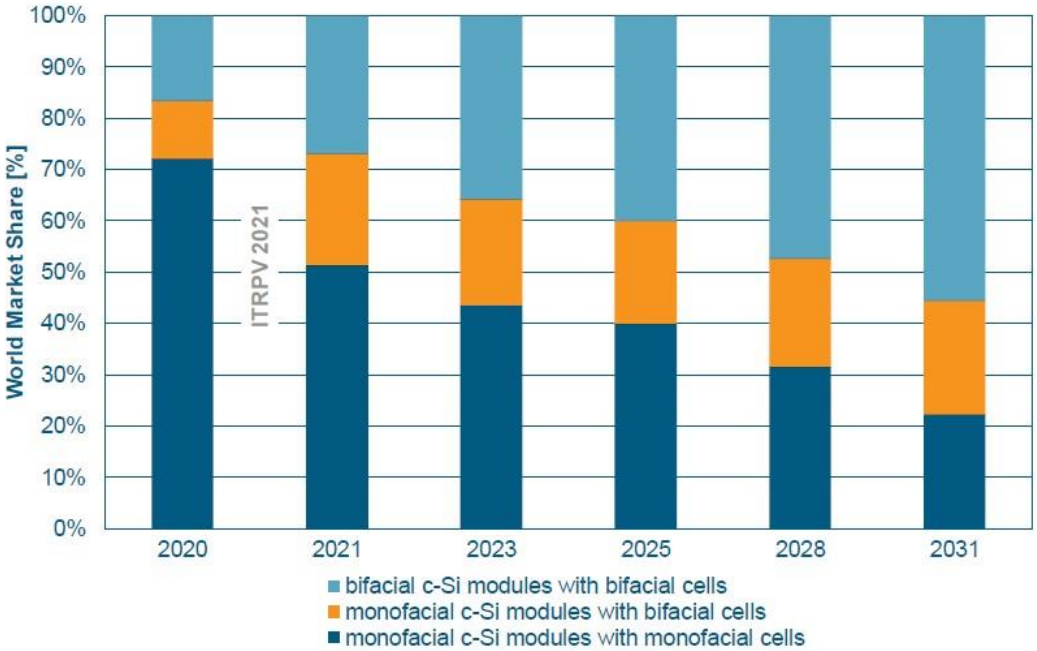

Fig. 13. Market share for mono-facial and bifacial cells used in mono-facial and bifacial PV modules [77]

The cell architectures for the leading technologies, as indicated above, are shown below in Fig. 14 and 15.

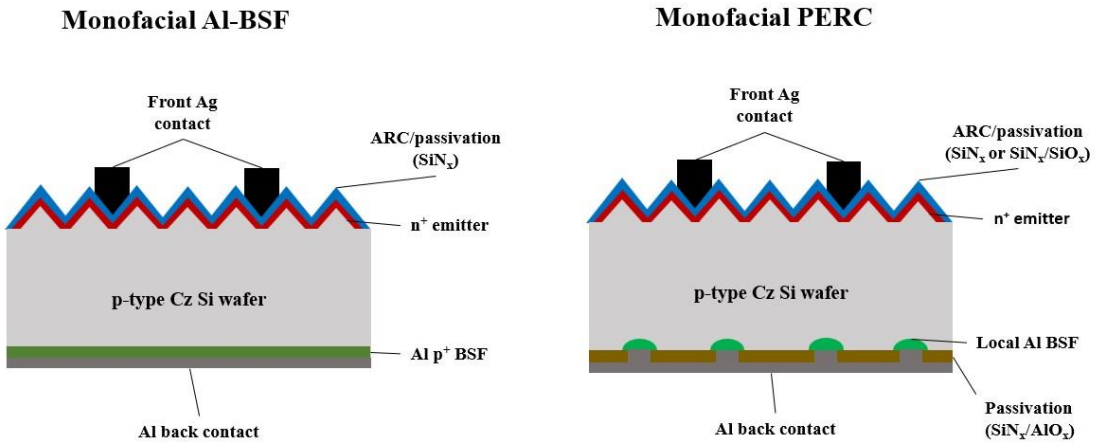

Fig. 14 Monofacial Al-BSF and PERC cell [79]

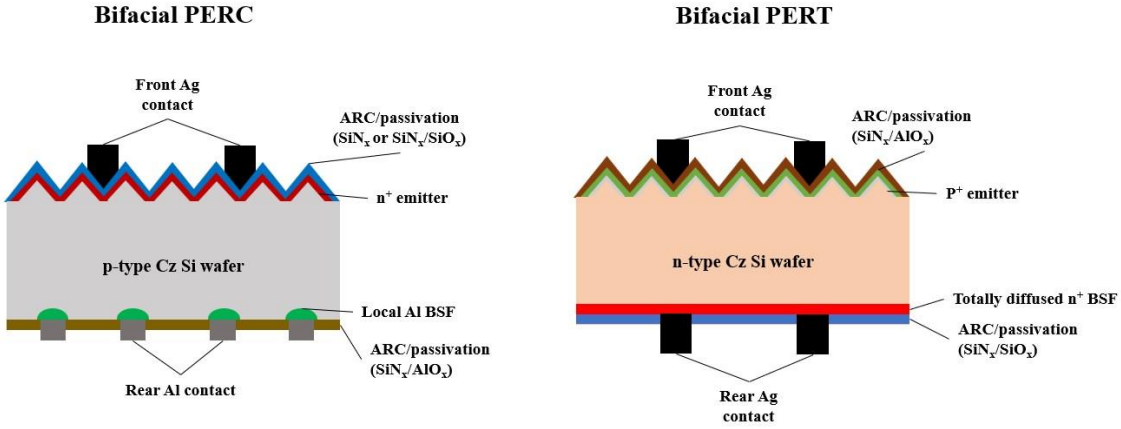

Fig. 15. Bifacial PERC and PERT cell [80], [81]

There are three main PID mechanisms PID-s, PID-p, and PID-corrosion (PID-c). These are discussed below on the main PV cell technologies shown above.

Al-BSF/p-PERC n^+ Front Side Negative Bias: Negatively biased Al-BSF or PERC (front) cells have been reported to undergo PID-s [57], [65]. Due to a negative voltage bias, the Sodium ions (Na^+) in the front glass drift towards the dielectric; there, the Na^+ can permeate the Si stack leading to stacking faults and shunting of the p-n junction [69]. PID-s leads to a drop in the module power (Pmax), fill factor (FF), $R_{SH,}$ and open circuit voltage (V_{OC}). The second diode saturation current (J_{02}) and the second diode ideality factor (n_2) increase. The short circuit current (I_{SC}) can also slightly degrade sometimes [82]. Shunting areas can appear as dark spots in the EL and PL images [83]. During EQE/IQE measurements, the reduction can be observed at short wavelengths or even for the full spectrum for severe PID-s [58]. Sometimes hotspots can also be observed during IR analysis [69], [84].

Through an analysis based on STEM and EDX, Na atoms have been found in the stacking faults. Although glass is the major contributor to Na^+, impurities on the cell's surface during production can also contribute to Na^+. Free electrons reduce Na^+ ions in the n^+ emitter region and, therefore, cannot provide an opposite charge at the end of the dielectric layers, so the drift of Na^+ persists. As shown in Fig. 14 (Bifacial PERC), if SiO_x is present, lateral thermal diffusion of Na^+ can occur, advancing them to the stacking faults. Once the Na atoms are in the stacking faults, their electronic composition changes, and an ohmic channel is formed in the middle of n^+ and the p-doped region. As a result, the Si band gap has partially populated defect levels. Consequently, hopping conduction creates shunting channels across the p-n junction when the local defect level concentration is adequately high, affecting Rsh. Furthermore, in the depletion area, these defect levels provide new centers for Shockley-Read-Hall (SRH) recombination when the defect level

concentration is comparatively low. This results in an increase in J_{02} and n_2 [69], [85], [86], [87].

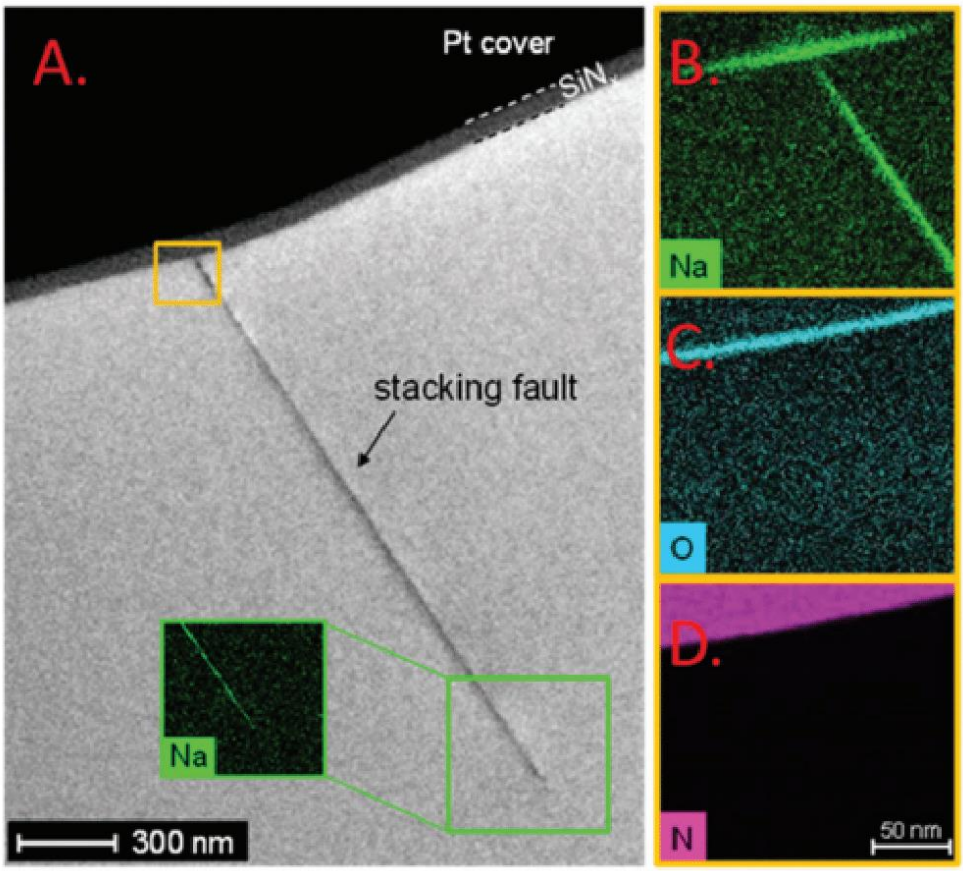

Fig. 16. (A) Transmission electron microscope (TEM) image of a stacking fault showing PID-s, (B to D) EDX image using scanning transmission electron microscope (STEM) for the same stacking fault near Si/SiN_x interface [86]

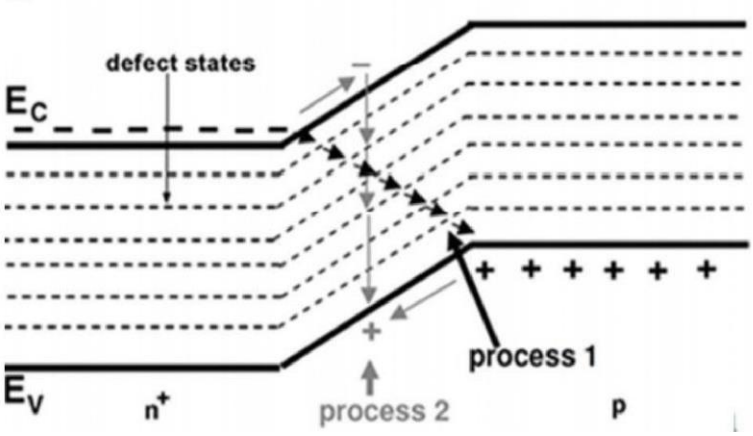

Fig. 17. Suggested band diagram for a Na decorated stacking fault [86]

Possibly dislocations serve as the defect nuclei for the stacking faults production because Na atoms increase the stress in their immediate environment, which causes the dislocations to split into partial dislocations and develop laterally. The two-dimensional stacking fault grows more via Na penetration between the partial dislocations. This aligns with density functional theory simulations, demonstrating that Na diffusion is not conducive to empty stacking faults but is significantly more convenient when stacking faults full of Na [88]. Si-Si bonds, therefore, lengthen across the stacking fault to handle the high Na content, which causes the stacking faults to extend. This is consistent with the Na-decorated stacking faults width found in [86] to be greater than intrinsic stacking faults width. Na+ can also infiltrate into microcracks, boosting recombination centers and shunting the p-n junction. The broader and deeper the microcrack, the stronger the PID effect [89].

Al-BSF/p-PERC n^+ Front Side Positive Bias: After 14-day stress at 1000 V, 85°C, and RH less than 2%, one research has suggested a PID-p impact in cells that are positively biased

[90]. Due to a drop in I_{SC} and V_{OC} and a meager reduction in FF, the impact was attributed to PID-p. However, no process has been suggested. The effect is more noticeable when a SiNx/SiOx dielectric stack is employed instead of only a SiNx layer. Furthermore, for the modules with SiNx and SiNx/SiOx stacks, these drops saturate correspondingly after a day and after 20 minutes. The authors argue that the SiOx layer is crucial to the PID-p process by inhibiting the dissipation of accumulated negative charges.

At positive bias, some corrosion mechanisms have also been reported. Following DH (85°C/85%RH) with applied bias +600 V, Hacke et al. found electrochemical corrosion of silver (Ag) gridlines of p-type c-Si modules [82], [91]. Busbars have been observed to have a dark tint, which is compatible with the production of Ag oxide. Another significant finding was the production of bubbles above the busbars [92]. Acetic acid production from the hydrolysis of the EVA at high temperatures is thought to cause bubble formation. Additionally, the acetic acid functions as a catalyst to quicken the corrosion reaction at the cell gridline surface by offering a mobile counter ion that allows corrosion byproducts to migrate. Under positive bias weathering, it is also possible to see thinning of the Si_xN_y layer, with consequent color change and reduced operating cell current [82]. The alteration in the reflectance of the dielectric layer is what causes the color change [93]. Through changes in hydrogen concentration (chemical passivation) and positive dielectric fixed charge density (field-effect passivation), the reduction in layer thickness also impairs the efficiency of cell surface passivation [94]. According to Morita et al., the Si_xN_y film is hydrolyzed by water at high temperatures into a type of hydrous silica and ammonia, which results in anisotropic silicon etching [95]. Such a condition worsens carrier recombination and interface flaws, significantly reducing module performance [96].

Studies by [97] on c-Si mini modules with poly EVA showed a considerable I_{SC} loss when cells are under +1000 V stress because of EVA discoloration and delamination from enhanced chemical reactivity at the front-side EVA/cell metallization interface. At the Ag gridlines under hot and humid circumstances (85 °C, 85% RH), an electrochemical reaction can cause discoloration of the EVA encapsulant near the cell gridlines. The discoloration is attributable to the development of silver sulfide (Ag_2S) or silver oxide (Ag_2O) species at the EVA/Ag gridline interface, according to a chemical compositional study performed using X-ray photoelectron spectroscopy (XPS). Both optical microscopy and XPS depth profiling showed the movement of Ag ions from the cell gridlines into the bulk of the EVA. However, the lack of the Ag signal at the EVA/glass contact suggests poor ionic transport across the encapsulant's nominal 0.45 mm thickness. By applying the elimination method, it is assumed that the sulfur in the samples examined here comes from the outside air and diffuses into the module through the porous polymer backsheet [97].

p-PERC p-type Rear Side Negative Bias: PID-p is seen on p-PERC modules at the p-type rear side under a negative bias. The reason is the build-up of positive charges in the dielectric layers, which raises the surface recombination velocity (SRV) of minority carrier electrons.

Due to PID-p, a significant drop in I_{SC} is observed, and the first diode saturation current (J_{01}) and first diode ideality factor (n_1) also increase. A reduction in Pmax and V_{OC} is seen due to this. FF is relatively less impacted. Furthermore, these reductions in IV parameters become more significant at low irradiance due to injection-dependent rear SRV [66]. PID-p shows up as a uniform decrease in the image intensities taken using EL and

PL. EQE/IQE measurements show a reduction in the full spectrum. At the impacted side (rear), a peak at long wavelengths is observed, and for the non-impacted side (front), a reduction is seen at longer wavelengths [61], [65], [98].

The rear side of p-PERC with a SiN_x/AlO_x dielectric stack was stressed by Luo et al. at -1000 V, 50°C, and 30% RH. The IV parameters are reduced during the first 40 hours of the stress. Though after that, the parameters begin to recover. The EQE spectra also support an increase in SRV on the backside. Fig. 18 and 19 show the change in IV parameters and EQE. The researchers give the following rationale. Holes are depleted at the AlO_x/Si interface as positive charges move into the rear dielectric stack. As a result, SRV increases, and the I-V parameters are affected. The Si band bending increases as more positive charges move into the SiN_x/AlO_x stack until an inversion layer of electrons is formed along the rear p-type Si surface. Consequently, the majority-carrier holes are forced away from the rear surface lowering the SRV [66].

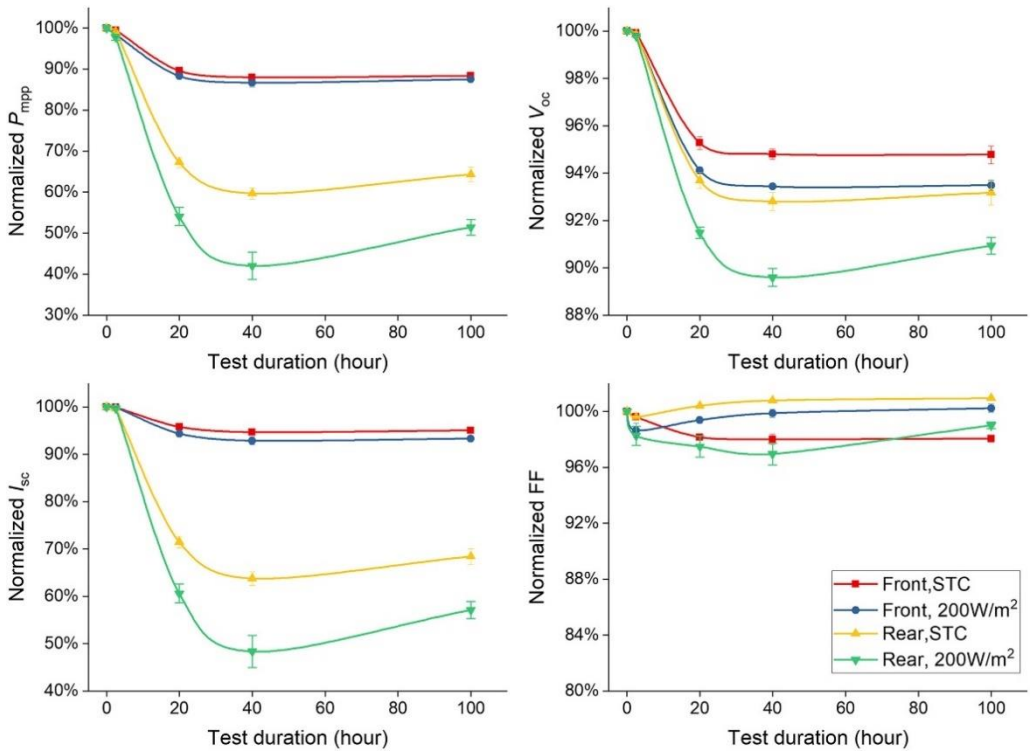

Fig. 18. Change in IV curves due to PID-p [66]

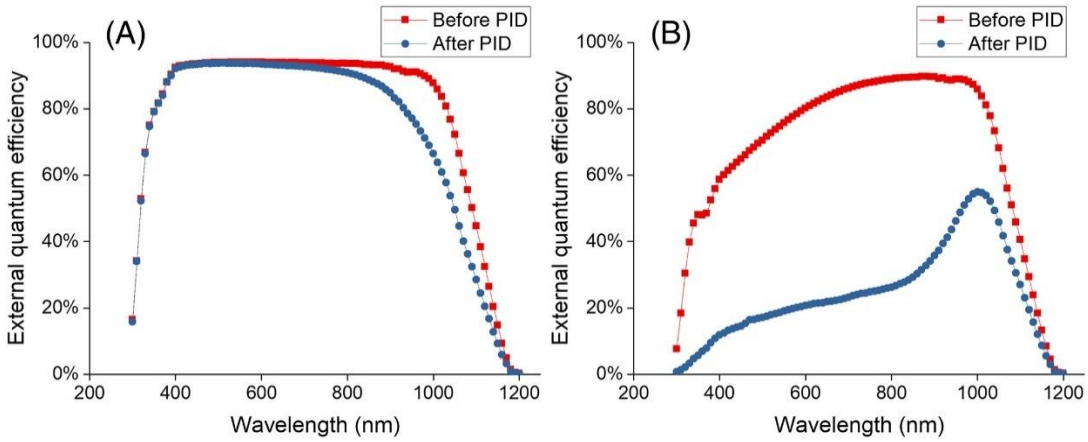

Fig. 19. EQE analysis on the front (A) and rear (B) [66]

PID-s and PID-p are both recoverable, as discussed in the recovery section (2.6). PID-c, however, is not recoverable.

PID-c, along with PID-p, has also been observed at the rear of p-PERC by Sporleder et al. [98], [99], [100], [101]. At stress for 24 hours at -1000 V, 85°C, and RH less than

2%, they notice a deterioration that cannot be solely attributed to the PID-p influence. Although the I-V parameters are affected similarly to PID-p, the damage is not recoverable, which is inconsistent with the PID-p mechanism. Moreover, SEM shows circular damage spots on the surface of the dielectric layers. In these holes, the SiN_x/AlO_x layers have been destroyed, as shown by TEM analysis based on focus ion beam. Consequently, leaving a heterogeneous SiO_2 layer at the end. Fig. 20 shows the SEM and TEM images. The authors propose an electrochemical etching process (corrosion) at the Si/AlO_x contact since this layer is too thick to be a native oxide [98], [99], [100], [101].

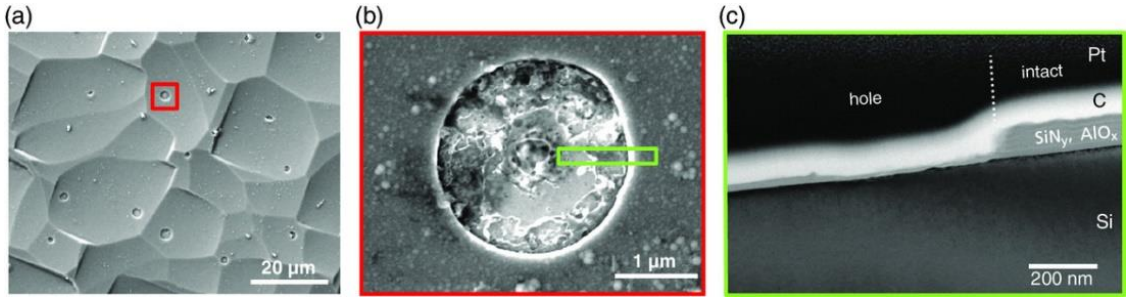

Fig. 20. (a). SEM at the rear of p-PERC showing holes, (b). Magnified SEM of the hole, (c). TEM image showing missing SiN_x/AlO_x layers [100]

The authors explain the following mechanism. Alkali metal ions, such as Na+, are driven through SiN_x/AlO_x layers and onto the Si/AlO_x interface under a negative bias. They then spread in a circular pattern around the Si surface, overcompensating for the AlO_x field-effect passivation. As the Si surface gets increasingly cathodic, a lateral corrosive reaction forms a circular hole, the bottom of which is filled by a layer of SiO_2. The AlO_x layer or the manufacturing of c-Si wafers where oxygen enters the melt via the SiO_x crucible and is integrated into the crystal during Si solidification are the most likely sources of oxygen for this mechanism. Gaseous hydrogen production and volume expansion of the produced SiO_2 layer are likely to blame for the delamination of the SiN_x/AlO_x stack. This process

could be related to the SiN_x corrosion that Hacke et al. observed on the front side of cells under 85°C, 85% RH [102], [103]. Additionally, during the early stages of PID-c, when the oxidation process has just begun, but the dielectric layers have not yet been pulled up, they are marked by dark patches on spatially resolved IQE [62] and laser beam-induced current (LBIC) studies. The enhanced SRV caused by the SiO_x production at the Si/AlO_x contact is indicated by these dark areas [98], [99], [100], [101]. However, considerable research is needed to understand this mechanism fully.

Moreover, the authors also observed some degradation due to Na penetration (no name given for this process) due to samples recovering partly after some time and showing no signs of PID-c [99]. Due to partial recovery, the degradation cannot be attributed to PID-p, where a complete recovery is expected.

p-PERC p-type Rear Side Positive Bias: Few studies describe the impact of positive bias on the rear of p-PERC. It is suggested that there is no impact under these conditions [66].

n-PERT p^+ Front Side Negative Bias: Under negative bias, a build-up of positive charges in the front dielectric layers causes cells to undergo PID-p. A SiN_x/AlO_x layer or a SiO_x/SiN_x layer can passivate the front p^+ emitter in n-PERT modules. Nevertheless, the SiN_x/AlO_x stack has superior passivation qualities and is more popular [104]. Although most of the research is focused on n-PERT with the front SiO_x/SiN_x layer, which indicates that for n-PERT modules with a front SiN_x/AlO_x layer, the PID process may differ from the explanation given here. Almost similar degradation in IV parameters is seen at the front n-PERT, as discussed previously on the rear of p-type PERC under a negative bias.

However, some changes are observed in EQE/IQE at shorter wavelengths as a reduction is seen at the stressed side (front), whereas a reduction in longer wavelengths is seen at the non-stressed side (rear) [70], [105], [106]. It is unclear where the accumulated positive charges come from, but some investigations have shown that Na^+ ions are not always to blame. Yamaguchi et al. conducted experiments for a few seconds to several minutes (10 minutes) at -1000 V, 85°C, RH less than 2% to study the early phases of PID on the front side of n-PERT modules with SiO_x/SiN_x layer [107], [108]. It is suggested that PID-p occurs during the first five seconds and then reaches saturation in the first minute. Increased SRV on the front side is another indicator in the EQE analysis. Fig. 21 and 22 show these results.

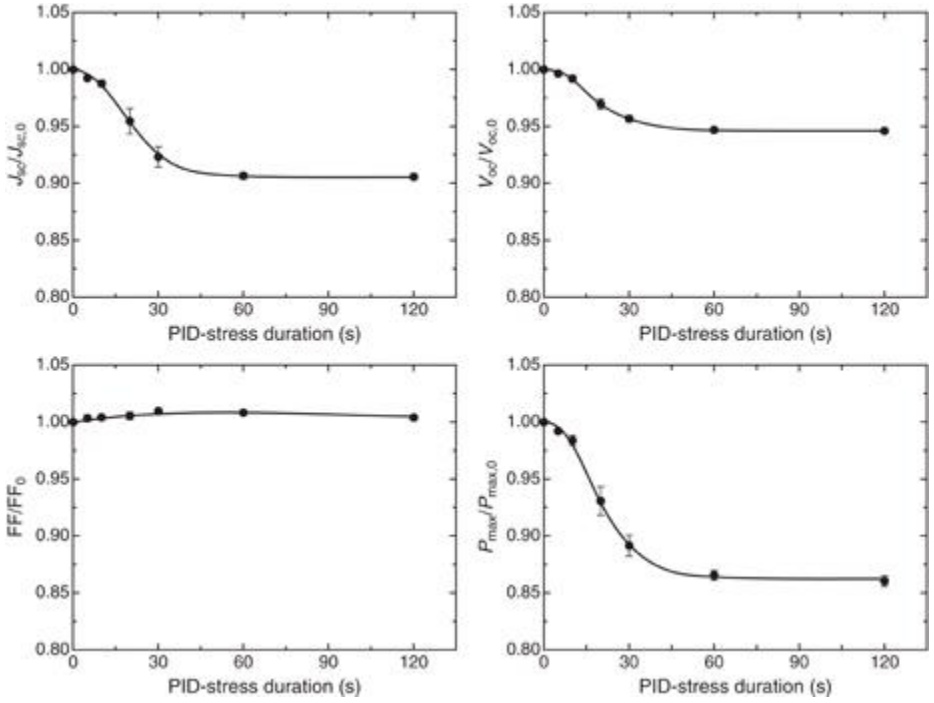

Fig. 21. PID-p in n-PERT (front p^+ emitter) modules [107]

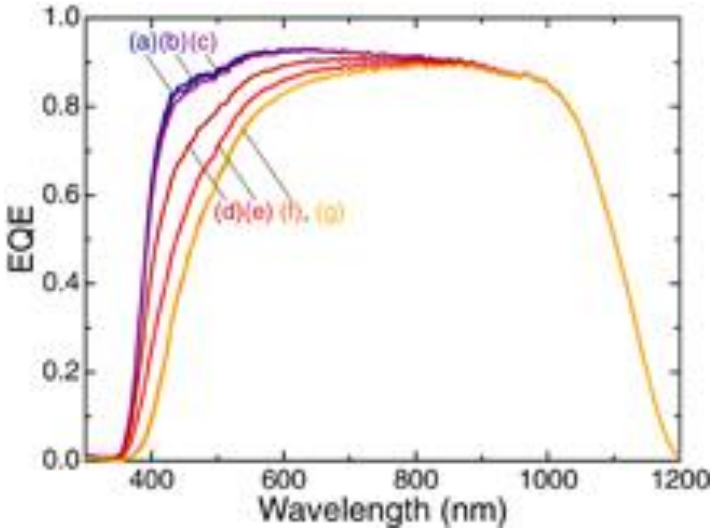

Fig. 22. EQE analysis (a) before PID, (b) 5s, (c) 10s, (d) 20s, (e) 30, (f) 60, and (g) 120s after PID [107]

Since the Na+ ion migration through a SiN_x film would take considerable time, this rapid deterioration cannot be fully explained by their movement [109]. Additionally, Bae et al. showed PID-p regardless of the Na source after 48-hour stress at -1000 V and 60°C, and Hara et al. found no Na build-up at Si surface on PID-p damaged n-PERT modules [110], [111]. A mechanism using the K-centers in the SiN_x ARC has been suggested by Yamaguchi et al. to account for the rapid PID-p. An electrically neutral, negative, or positive link between three N atoms and two Si atoms is a K-center (K_0, K^-, or K^+). The shift in charge states of the K-centers could cause the rapid PID-p.

The net charge in the passivation layers changes to a higher positive value because of a positive charge injection, which causes K^- and K_0 to release electrons and transform into a K^+ defect [112]. Then, at the Si surface, more minority-charge carrier electrons recombine. When all the K centers are positively charged, the saturation effect that has been seen could happen. However, the SRV governed by the recombination sites at the Si

dielectric interface may also be used to explain it [113]. Fig. 23 shows the K-center mechanism described by Yamaguchi et al.

Although it provides a convincing justification for the speed of the PID-p process, it fails to explain where the positive charges collected on the SiN_x surface come from. Yamaguchi et al. have carried out cyclic voltammetry and electron-spin resonance measurements on their samples to evaluate their K-center model [107]. In the insulator film, the saturation of Q_f is comparable to Pmax saturation. Furthermore, the proposed model is supported by the saturation value of Q_f (7×10^{12} cm^{-2}), on par with the density of K_0 centers 4×10^{12} cm^{-2}.

Following rapid PID-p, the researchers also carried out lengthier PID experiments at - 1000 V, 85°C, and RH less than 2% for 40 days with characterization every few seconds. They found additional mechanisms, i.e., PID-c and degradation due to Na penetration [114], [115]. Fig. 24 illustrates the three deterioration phases and how they affect the module parameters.

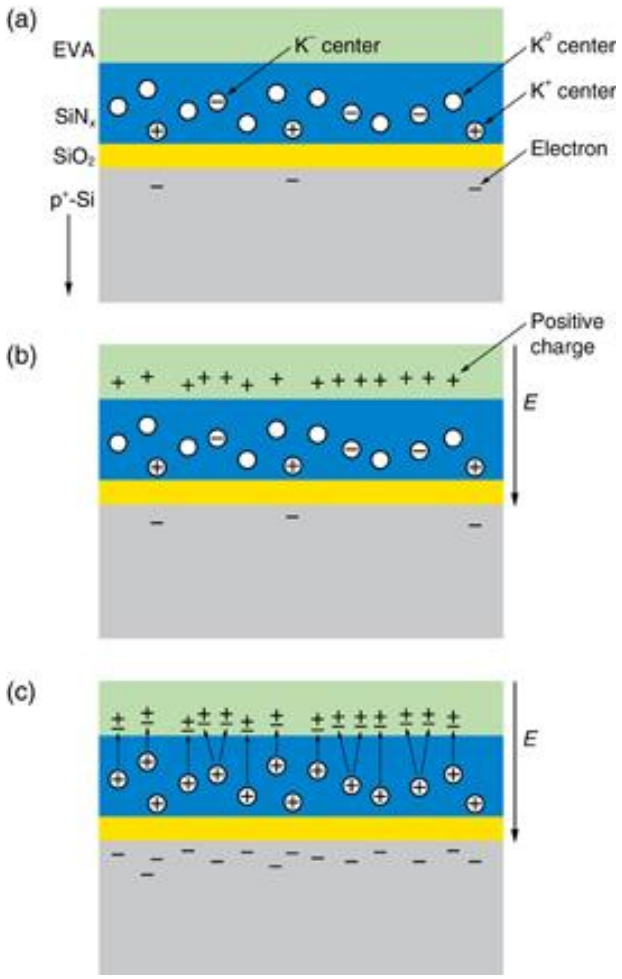

Fig. 23. PID-p process based on K-centers (a) Before PID, (b) and (c) During PID under a negative bias [107]

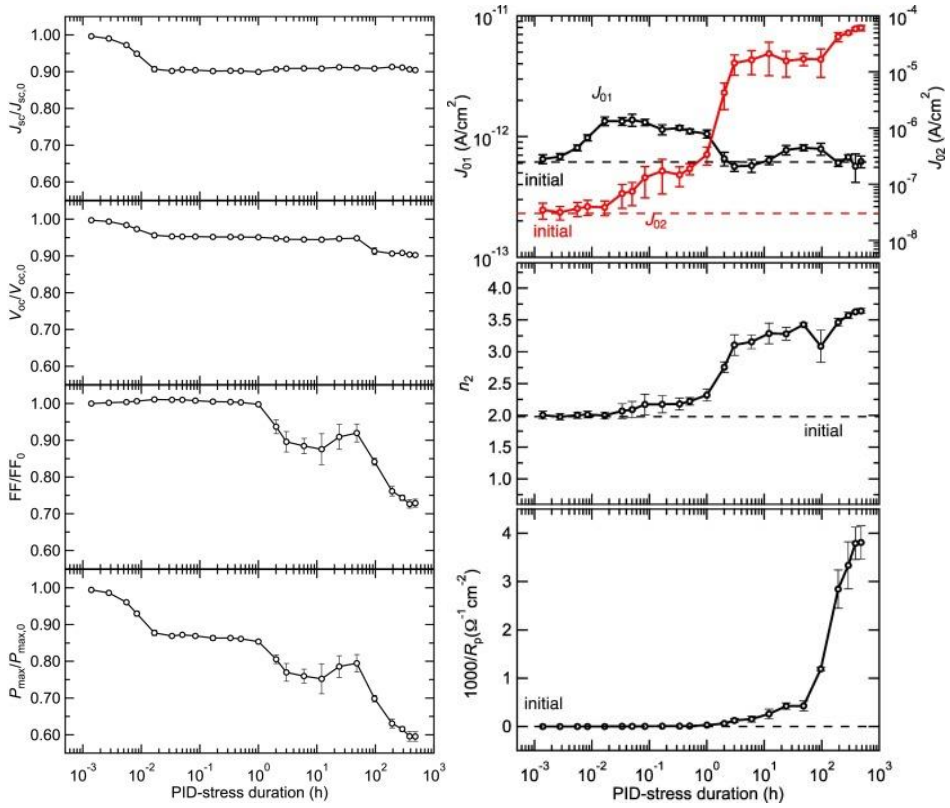

Fig. 24. Degradation in module parameters due to multiple PID processes [114]

The rapid PID-p mentioned above is responsible for the initial degradation, which has a saturating effect on the IV parameters after the first minute. Na penetration is responsible for the second deterioration stage. It starts after an hour of stress and is distinguished by a FF drop and a rise in J_{02} and n_2, indicating an impact in the space charge region (SCR). The deterioration is attributable to increased recombination in the SCR, not the p-n junction shunting because R_{SH} is not considerably impacted. This can be due to Na atoms in the SCR causing the development of defect levels. Na would travel through the Si stacking faults from the front passivation layers to the p-n junction, quite away from the surface, and function as recombination centers. The ability of the internal electric field to deter Na^+ can lead to no shunting [114]. More research is needed to support this concept,

as other researchers do not see any evidence of Na^+ entry into the p^+ emitter of n-PERT modules due to PID [116].

Furthermore, theoretical considerations suggest that p-doped regions would not allow Na^+ to travel via the stacking fault. The contact of the boron dopant with the Si stacking fault would be inadequate for the Si stacking fault energy to be sufficiently reduced for the Na^+ ion to penetrate [117]. Additionally, Na+ cannot be reduced in p+ locations. The same researchers have further characterized the third decline due to PID-c occurring after 96 hours [118]. It is distinguished by a further decline in FF and Voc and increases in J_{02}, n_2, and $1000/R_{SH.}$ The production of Na-based dome-shaped protuberances at the edges of the c-Si pyramid (Fig. 25) would be the primary factor in the partial breakdown of the SiN_x layer. The most significant electric fields are found on top of pyramids, which may help explain why the Na protuberances appear, but how they develop is still unknown [115]. The higher $1000/R_{SH}$ shows that the junction has been shunted, but PID-s is not likely to happen on a p^+ emitter. Additionally, reverse bias dark I-V curves have a linear characteristic, which often denotes the introduction of numerous contaminants into the SCR. Since the cells used had non-passivated ends, Na^+ impurities may enter the SCR area from the edges of the cells, which could account for the effect on R_{SH} [119].

The degradation process, as explained above, is not observed by other researchers, and various sources state a slower deterioration mechanism without saturation [119]. The reason could be the different characteristics of the n-PERT cell used in the experiments. Still, more work is needed to understand the processes involved fully.

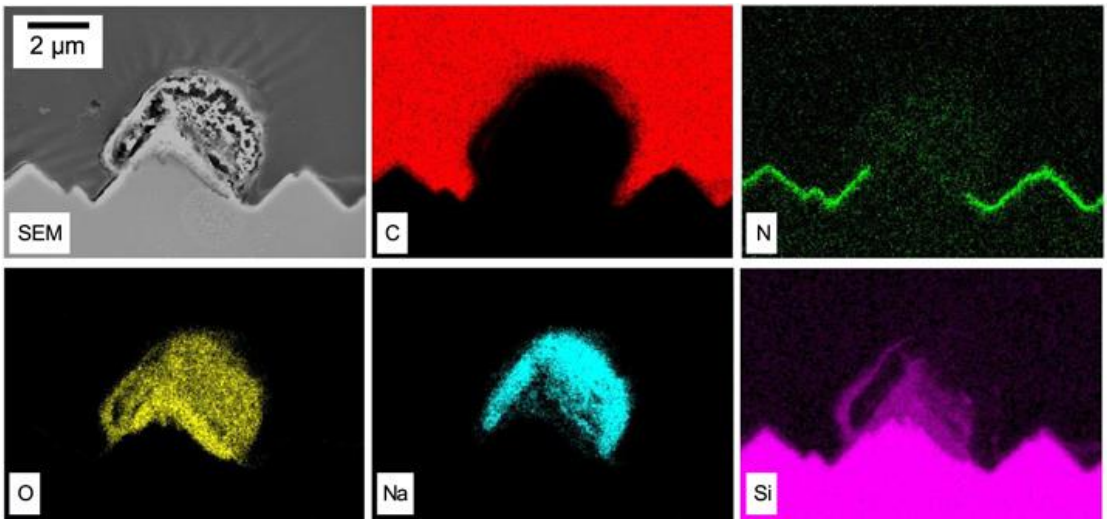

Fig. 25. SEM and EDX images for front of the n-PERT cell after PID at -1000V, 85 °C and 480 hours [115]

n-PERT p^+ Front Side Positive Bias: No significant data is available to understand the mechanisms involved due to PID at the front of n-PERT under positive bias. Some authors have suggested no impact under these conditions [111].

n-PERT n^+ Rear Side Negative Bias: Carolus et al. have studied the rear side on n-PERT cells at -1000V, 60 °C, and RH less than 60% for 721 hours. A reduction in IV and EQE is observed. However, the authors point out that the deterioration could be due to high temperature during the experiment instead of PID [120]. Yamaguchi et al. studied the PID influence on the front side of the n-type G-TBS bifacial module with a rear p^+ emitter and a SiN_x ARC on both sides (comparable to the rear of a GG n-PERT module) at -1000 V, 85 °C, RH less than 2% for 24 hours [121].

Findings demonstrate a substantial drop in Pmax, FF, and Voc, an increase in $J_{01,}$ and a minor decrease in I_{SC}. The EQE spectrum is reduced at short wavelengths, indicating more significant n^+ recombination. They propose a Na penetration as the source of the

observed impact since PID-p cannot occur on n-type materials under a negative bias. Na^+ can travel from the glass to the n^+ side, get reduced, and decorate the Si stacking faults. Na-decorated stacking faults may act as recombination centers since the junction is far away to be shunted. Na penetration from the non-passivated edges could be responsible for the drop in J_{02}, R_{SH}, and FF. After 30 to 60 minutes, IV parameters are severely saturated, but no reasoning is offered [121].

n-PERT n^+ Rear Side Positive Bias: On similar modules (G-TBS bifacial module with a rear p^+ emitter and a SiN_x ARC on both sides), Yamaguchi et al. executed PID under a positive bias. They noted a reduction in V_{OC} and I_{SC}, with EQE declining at shorter wavelengths [121]. Devoto et al. also observed similar results [122]. PID-p is offered as the plausible explanation for the degradation by both researchers, but no mechanisms have been explained. Still, considerable work is needed to understand the PID mechanisms at the n^+ rear side of n-PERT under both biases.

Table 1 below summarizes the PID mechanisms and degradation modes in the cell technologies discussed above (Al-BSF, p-PERC, n-PERT). Details about other less-used technologies (p-PERL, n-TOPCON, n-IBC, n-HJT) are also summarized in the table. Furthermore, the main PID mechanisms PID-s, PID-p, and PID-c have been explained in detail above as per explanations given by different authors [43].

Table 1. PID mechanisms and degradation modes in different cell technologies [65], [66], [82], [91], [97], [90], [123], [98], [99], [119], [124], [122], [111], [125], [115], [121], [118], [126], [127]

Technology	Side	Cell under negative bias	Cell under positive bias
Al-BSF	Front	PID-s	PID-p, PID-c
p-PERC	Front	PID-s	PID-p, PID-c

	Rear	PID-p, PID-c, Na penetration	No effect
n-PERT	Front	PID-p, PID-c, Na penetration	No effect
	Rear	Na penetration	PID-p
p-PERL	Front	PID-s	PID-p, PID-c
	Rear	PID-p, PID-c, Na penetration	No effect
n-TOPCON	Front	PID-p, PID-c, Na penetration	No effect
	Rear	No effect	No effect
n-IBC	Front	Na penetration	PID-p
	Rear	PID-s	PID-p
n-HJT	Front	PID-c, Na penetration	No effect
	Rear	PID-c. Na penetration	No effect

2.5 PID Prevention (Effect of System Configuration and Module Construction)

System Configuration: PV system configurations have been detailed in section 2.1. The LC increases as the potential difference between the cell and the frame (grounded) increases [128]. Therefore, as the absolute system voltage increases, PID can also be expected to increase. Moreover, modules at the end of the string experiencing a higher potential difference can rapidly undergo PID. Although, researchers have not discovered a linear dependence between Pmax degradation and the size of the system voltage [119].

Methods for preventing PID at the system level include using micro-inverters or micro-optimizers that can enhance the voltage of every PV module independently. By reducing the voltage, modules susceptible to higher voltages might have a reduced risk of PID [41]. Unlike grounded PV systems, the voltage differential in the modules may be

reduced using ungrounded PV systems. Nevertheless, additional forms of PID can occur since half string is under a positive polarity and the other half is under negative polarity. By grounding the PV system's negative pole, any PID linked to Na^+ ions may be inhibited. This technique adds a substantial expense since an offset box is required for ungrounded PV systems. Additionally, this method cannot control PID-p that manifests at both biases.

Superstrate: Superstrate or front glass for PV modules has been detailed in section 1.2. Since soda lime glass is a major contributor to Na^+ ions, disrupting the charge on the front glass or replacing it with any material that has no Na^+ can significantly limit PID.

Applying a Na^+ barrier layer between the front glass and the encapsulant, such as a TiO_2, can be a way to restrict PID-s; however, doing so often lowers the optical performance of the module [129]. Alternatives to soda-lime glass include borosilicate, aluminosilicate, quartz, and chemically toughened glass. These materials contain little or no Na [58]. The LC flowing into the module would be reduced since such glass materials have higher bulk resistivities, which could stop the PID mechanism [130]. Although, the use of these materials is rare due to the higher cost than conventional soda-lime glass. Another method to avoid PID-s is by obstructing the LC. Oh, et al. demonstrated this using a thin, flexible Corning Willow Glass sheet. The sheet can be used on the front glass of field functioning modules. Also, this glass is commercially available [131].

Encapsulant: EVA is the most widely used encapsulant. Fig. 26 shows the market share for some of the encapsulants. Table 2 shows the main properties of some of these encapsulants. Generally, for an encapsulant to perform better, it should have a low WVTR and high resistivity. The main reason for EVA being used by most manufacturers is the low cost and

an already developed supply chain, even though EVA has been shown to have reliability issues. POE is solving most of the issues EVA has but is not as widely used because of its high cost. Similarly, other encapsulants listed in Table 2 are expensive (apart from other issues), preventing their widespread use.

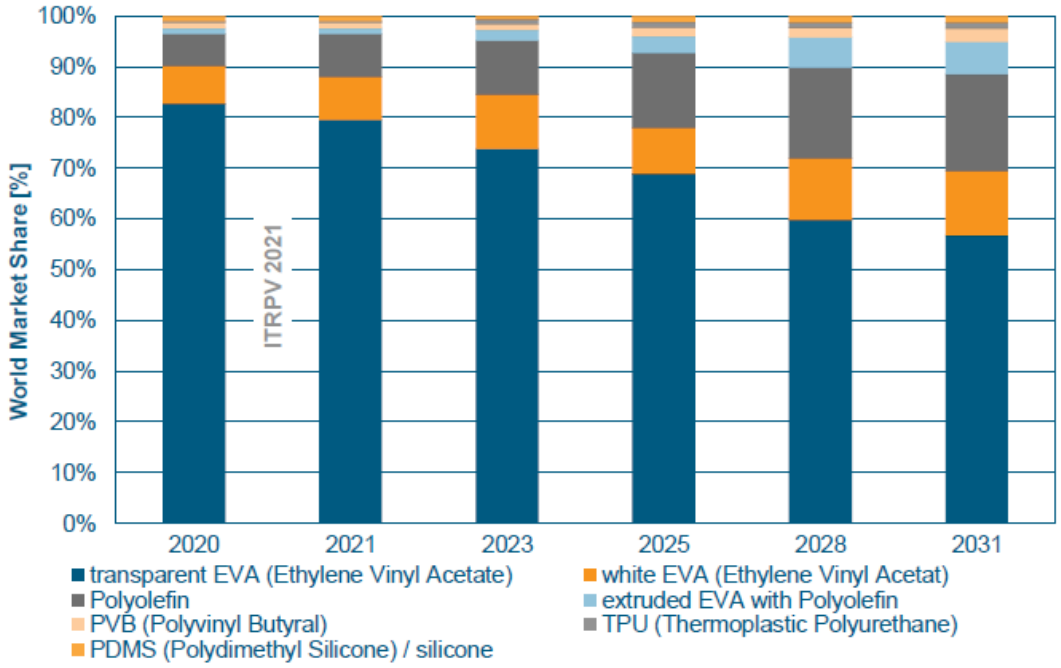

Fig. 26. Market share for different encapsulants [77]

Table 2. Encapsulants properties [132], [133], [134], [135], [136]

Encapsulant	**WVTR ($g.m^{-2}.day^{-1}$)**	**Resistivity (Ω.cm)**
EVA	5 – 34	$10^{14} – 10^{15}$
POE	0.89 – 3.30	$10^{16} – 10^{17}$
Thermoplastic Polyurethane (TPU)	12.84	2.7×10^{14}
Thermoplastic Polyolefin (TPO)	0.89 – 2.85	$10^{14} – 10^{18}$
Polyvinyl Butyral (PVB)	19.26 – 40.05	$10^{10} – 10^{12}$
Polydimethyl Silicone (PDMS)	10 – 200	$10^{14} – 10^{15}$
Ionomer	0.19 – 0.31	10^{16}

To curb PID, EVA can be replaced with any encapsulant with better properties like POE (lower WVTR and higher resistivity) [66]. One study tested various encapsulants

(using mini modules) against PID-s (at 85°C, 85% RH, -1000V, and 40h dwell time); these included 6 EVA, 1 POE, 1 PVB, 1 TPU, and 1 ionomer-based encapsulant materials. In POE and ionomer encapsulants, no PID was observed. PVB and TPU were heavily impacted by PID (low resistivity and high WVTR). Different EVA sheets showed variable PID based on their variable properties. In the field under high temperature and humidity, the properties of the encapsulant material can vary, and their performance can degrade over time [136]. However, one study has shown that even under extended DH stress POE still shows better resistance against PID than EVA [49].

As explained earlier, EVA can degrade, forming acetic acid to speed up the PID process. POE, which exhibits stronger resistivities and improved chemical stability, is a strong contender to replace traditional EVA. One study experimented with 3 different POE encapsulants and observed no PID-s in contrast to conventional EVA. It is speculated that EVA's increased thermodynamic compatibility with highly polar ions like Na^+ is due to the interaction of its polar functionality and acidic degradation products [137]. The effects of PID with EVA and different POE encapsulants on the front of n-PERT modules under a negative bias have been examined too. PID-p is recognized; however, POE dramatically diminishes the effect [113].

Moreover, in p-PERC, PID-s and PID-p have been curbed using POE [138]. EVA with higher resistivity has also shown reduced PID-s susceptibility [50]. A combination of encapsulants like EVA-ionomer has also shown reduced PID impact and is less expensive [139].

Substrate: Details for the substrate were given in section 1.2. However, GG and G-TBS constructions (mostly bifacial) were not discussed. They can significantly impact PID;

therefore, their detail is discussed here, along with PID prevention. Based on the installation location, G-TBS and GG constructions have advantages and disadvantages [140].

G-TBS Pros [50], [132], [140]

- Weight is less than GG modules.
- Transportation, handling, maintenance, and installation are easier.
- More scalable as production is similar to mono-facial modules.
- Mostly they are framed, which provides more support.
- Field operating temperatures are lower than GG modules, so performance is better
- Backsheet material has better electrical resistance.

G-TBS Cons [133], [141], [142]

- Backsheets can degrade due to moisture ingress over time.
- Water penetration can lead to crack formation, delamination, and reduced electrical resistance.
- Some materials can degrade under increased UV exposure.

GG Pros [74], [143]

- Framed GG construction is more robust than G-TBS, enabling them to tolerate severe environmental conditions and rough handling.
- Less prone to moisture ingress given that the edge sealant is good.

GG Cons [50], [144]

- Frameless GG construction can break easily if not handled properly.
- Weight is more than G-TBS construction.

- If the correct encapsulant is not used, GG modules can experience delamination and trap chemicals released by the encapsulant under stress (like EVA).
- Running temperatures are high as compared to G-TBS construction, reducing performance.

If the construction is based on a backsheet or TBS, the material must prevent moisture ingress at the substrate level to prevent PID. That can be achieved with a material composed of multiple layers with a lower water vapor transmission rate (WVTR) [145]. Al in the backsheet material has also been shown to reduce PID [146].

In the case of GG modules, moisture ingress is not a big problem if the edge seal is good. However, moisture can penetrate if the edge seal weakens over time, and PID susceptibility can increase. Framed GG modules can show more PID degradation because of additional Na^+ ions from the rear glass; however, frameless GG modules might be less prone to PID in the field since pathways for LC are lowered. In most studies, GG modules are more prone to PID than G-TBS modules [132], [147].

Cell Level: To prevent Na^+ ion, the SiN_x is sufficient if there is zero potential difference, and the temperature is low. However, an extra dielectric layer is essential since PID processes are more effective at high temperatures and potential differences. Some studies have used SiN_x/SiO_x layers on p-PERC to curb PID-s [90]. Another team of researchers has used SiN_x/SiO_yN_x layers to prevent PID by lowering charge trapping [148]. By reducing the voltage differential across the SiN_x ARC, PID can be controlled. Therefore,

SiN_x ARC with a higher refractive index may be utilized as more UV can be absorbed, enhancing the electrical conductivity of the SiN_x layers [124]. One study confirms that SiN_x ARC with higher refractive index exhibits can limit PID-s [40].

A suitable compromise must be made to minimize PID without lowering the module output, as an increased SiN_x refractive index also reduces optical performance [149]. Utilizing layers of SiN_x is one way to get the advantages of a high refractive index without reducing optical performance. By using two layers of SiN_x (instead of one with a refractive index of 1.97 and 70nm width), one with a refractive index of 1.97 (54nm top layer) and one with a refractive index of 2.44 (18nm layer), a reduced PID-p was seen on n-PERT cells (given that SiN_x is not close to Si) [116]. Other researchers have also reported reduced PID activity when using multiple layers of SiN_x with different refractive indexes (given that Si close to SiO_x is thin to allow tunneling) [150].

The AlO_x layer, which often replaces the SiO_x layer on the front side of n-PERT cells, must be thin and electrically conductive to reduce PID-p. It also produces excellent results when more intricate dielectric layers are used. Using a SiO_x layer between the AlO_x and SiN_x layers on the back of bifacial p-PERC considerably reduces PID-p [151]. The reason is the increased SiO_x band gap (9.0 eV), leading to a larger breakdown voltage of the AlOx-SiO_x-SiN_x layers. A reduction in PID was also observed by adding a SiO_xN_y layer to the SiN_x/SiO_x and SiN_x/AlO_x layers on the front and rear of p-PERC cells. The reason is amplified field-effect passivation and SiO_xN_y layer shielding AlO_x from corrosion [152].

Some other measures can also be used to prevent or reduce PID at the cell level, like changing the doping level at the emitter. Employing an emitter sheet with a smaller

resistance PID-s was prevented in p-type cells. The reason is exceptionally elevated phosphorus concentration in the emitter leading to Na gettering [148]. Furthermore, in n-PERT cells, changing the boron (emitter) doping and dielectric characteristics reduced PID-p, with a significant impact coming from the dielectric layers [153]. Another study uses n-PERT cells with surface-etched boron with high doping concentration to reduce the band bending effect and prevent PID-p [43], [150].

2.6 PID Recovery (Effect of System Configuration and Ambient Conditions)

System Configuration: When the system voltage is off at night, PID-s and PID-p gradually recover [85]. Applying a reverse bias voltage can speed up the recovery process. The Na^+ ion's capacity to diffuse back from the Si stacking fault due to a concentration gradient is mainly responsible for the recovery. Therefore, it has primarily been examined on the front side of PERC modules as a diffusion-driven process [154]. As affected locations recover at varying speeds, the module recovery is gradual due to varied Na concentrations in the stacking fault [155]. Consequently, when PID-s is more severe, the recovery process takes longer. Studies suggest that R_{SH} recovers only by 50%. In contrast, Pmax can fully recover, showing that the residual Na atoms in the stacking fault, SiN_x, or SiO_x layers influence the PID-s affected modules [58]. Accordingly, both R_{SH} and Pmax should be observed during the recovery process. Degradation due to Na-penetration can recover similarly as well. The de-trapping of accumulated positive or negative charges in the dielectric layers is the foundation of PID-p recovery. Recovery has been studied on p-PERC and n-PERT bifacial modules (both rear and front) [90]. Recovery can happen at night in the field, but the

process is gradual, and the IV data does not show full recovery. Furthermore, using a reverse bias is not a good option since more equipment might be needed and could result in other PID mechanisms.

Temperature: An Arrhenius relationship with LC is observed for varying temperatures when the RH is fixed. Equation 1 shows the relationship between LC and temperature [156].

$$I\ (RH, V, T) = I_0\ (RH, V) e^{\frac{-E_a(RH)}{k_B T}} \qquad 1$$

Where I (RH, V, T) is LC, I_0 (RH, V) is current at initial condition, E_a is the activation energy, k_B is Boltzmann constant, and T is module temperature). The E_a is high for higher values of RH [45].

Some researchers have used different contacting methods, i.e., only air and frame, Al foil on the surface, and DH at 85% RH to plot the LC as an inverse temperature function. An Arrhenius relationship with a similar Ea was attained, although crossing with the LC axis was not the same. Hence f_{ground} was added to explain the difference, as shown in equation 2 [157].

$$I_{mod}\left(RH, T_{ref}\right) = I_{ref}(RH).f_{ground}.e^{\frac{-E_a(RH)}{k_B}}.\left(\frac{1}{T_{mod}} - \frac{1}{T_{ref}}\right) \qquad 2$$

Due to an increase in temperature, the LC also increases. In contrast to the maximum power loss, the PID rate rises with temperature [123]. The mobility of Na^+ ions is also increased at higher temperatures, which can accelerate PID-s and PID-c [101]. According to a study, temperature accelerates PID degradation rates more than voltage [119]. High temperatures may speed up the recovery process, although the amount of

recovery achieved is independent of temperature. Heat treatment in the field is also inappropriate and might strain the modules unnecessarily [40].

Humidity: Humidity is primarily responsible for controlling the amplitude of LC [57]. A relatively high conductive coating can form on the front glass under high humidity or wet environments, making LC the central leakage channel perpendicular to the front glass. LC can rise by two orders of magnitude during rain and increase due to morning dew condensation [72]. Despite the increased conductivity of glass and encapsulant materials at higher temperatures, the LC magnitude is lowered if the temperature rises for the remainder of the day and dries the module [45]. Increasing humidity can accelerate the speed of PID-s and Pmax loss because of moisture ingress through the substrate and encapsulant [52].

Consequently, depending on the weather conditions, PID may emerge after a few years of operation. Modules in continually wet climates are anticipated to exhibit the highest LC and a more significant PID impact [158]. PID is shown to accelerate when a preceding DH stress is conducted because of a greater electric field and LC from the decreased bulk resistivity of the encapsulant due to moisture ingress [159]. Additionally, acetic acid can evolve from EVA when moisture enters the system, which leads to corrosion between the Ag fingers and the Si emitter layer. No significant rise in LC is seen when the length of the DH stress is more than 3000 hours at 85°C and 85% RH, although the PID process can significantly increase. One reason for this can be that compared to the original condition when all the electrodes in the cell are corrosion-free, a minute electric field is developed around the corroded electrodes. Similar studies on n-HJT modules showed that PID accelerated because of a more significant decrease in TCO layers (PID-

c). While G-BS modules exhibit deterioration because of moisture ingress leading to PID. Some studies have found no moisture ingress in GG HJT modules. In general, PID susceptibility over time is significantly influenced by the permeability of the TBS material in bifacial G-TBS bifacial modules [146].

The front glass surface conductivity is minimal in dry circumstances, and LC is observed only near the module edges [160]. The main contributors to LC are surface and bulk glass conductivities and the conductivity at the encapsulant-glass contact [45]. Some researchers have established a correlation between the LC and humidity by considering the difference between ambient and module humidity. For different RH, the development of LC over time follows a sigmoidal Boltzmann function and reaches saturation within a few days. A generic model for the LC is also developed based on these results [72].

Soiling: For RH levels over 55%, a dirty surface exhibits lower glass resistance than a clean surface. Due to reduced resistance, LC can flow, and PID can occur [72]. Moreover, PID-s accelerates close to the module edges, where dirt can collect easily [161]. A study also shows that different kinds of soil influence the resistivity of the glass sheet at different degrees of humidity [162]. Another study demonstrates that the LC increases as dust accumulates until reaching a maximum value. The LC then progressively diminishes because the ions in the dust dissolve slowly in the water layer [163].

Light: Contingent on the light intensity and the module's PID sensitivity, concurrent lighting during PID stress can delay or prevent PID-s [164]. Additionally, more degradation due to PID-s has been documented in PV modules with shading [165]. The SiN_x layer's capacity to absorb light raises its conductivity, which causes light to impact PID-s. Due to a reduction in the voltage difference in the SiN_x layer during the PID stress,

the drift of Na^+ is minimized, which reduces PID-s [41]. Additionally, the Na^+ ions might be neutralized by the photogenerated electrons in the SiN_x layer. PID-s can also be delayed or suppressed by a UV component below 400 nm because SiN_x layers typically absorb light in the 300–390 nm region. Furthermore, SiN_x layers with a higher refractive index have superior absorption qualities and may be less affected by PID-s [166].

In contrast, light may or may not affect PID-p during stress testing. A study exposed n-PERT and p-PERC modules to a 24-hour PID stress under a range of irradiance levels from 0, 250, to 800 Wm^{-2}. The study suggested that light does not affect PID-p on the front side of n-PERT modules with a SiN_x/SiO_x passivation layer, but it prevents PID-p on the rear side of p-PERC modules with a SiN_x/AlO_x passivation stack. Moreover, it is seen that PID-p on the rear of p-PERC can be averted by a low irradiance of 10 Wm^{-2} [61]. Furthermore, for p-PERC modules made using a different manufacturing technique, a variable level of PID-p prevention under light is observed [98]. However, it is unclear how light affects PID-p. Although the SiN_x layers increased conductivity under illumination plays a role, it is also essential to consider the characteristics of the dielectric layer in contact with the Si surface.

The total voltage is the sum of the potential drops at each layer (glass-encapsulation-passivation layers etc.), which are proportional to the individual resistances. Hence, even though the voltage difference in the SiN_x layer drops under illumination, the potential difference in the AlO_x layer grows [62]. Furthermore, if the electrical resistance of the dielectric layer between the SiN_x layer and the Si surface is low, the charges can dissipate. In that case, it may be postulated that illumination prohibits PID-p. Another study suggests that to avoid PID-p on the rear of p-PERC modules, the electrical resistances of

SiN_x and AlO_x layers must be the same under illumination [98]. The elevated resistance of the SiO_x layer can be why light on the front side of n-PERT modules with a SiN_x/SiO_x passivation layer does not affect PID-p. Time-resolved PID experiments on p-PERC modules with an AlO_x/SiN_x passivation layer have been performed at -1000 V, 50°C, RH less than 2%, and 30 minutes with concurrent rear illumination [167]. The IV and IQE show degradation because of PID-p during the first five minutes. A drop in I_{SC} is observed, which recovers completely after reaching maximum degradation in most instances.

As explained by Sporleder et al., the SiNx K-centers are suggested to have a role in the process [167]. Three states are observed., initial state A, degraded state B, and regenerated state C. The SiN_x K-centers charge states are dispersed randomly in state A, and the AlO_x layer is negatively charged. By repelling electrons, it restricts the SRV at the p-type Si. The positive charge in the SiN_x layer increases as the PID stress continues because of the release of electrons and the conversion of K and K_0 into K^+. When there are enough positive charges in the SiN_x layer, the field effect passivation of the AlO_x layer is decreased. When all K-centers are positively charged, the SRV reaches a saturation point if the PID stress is maintained, i.e., state C. Inversion happens at the Si surface if there are more K centers than fixed negative charges in the AlO_x layer. Once Na^+ ions have enough time to drift through the SiN_x layer, it cannot be ruled out that they can also be linked to the depolarization of the passivation layer. The only difference between this behavior and that seen in the dark is that the light can speed up the process [66].

Additionally, by de-trapping stored charges at the Si surface, light can recover PID-p. A complete or partial recovery effect has been documented under illumination in p-PERC cells with rear SiNx/AlOx passivation stack impacted by PID-p. However, the recovery

behavior of p-PERC modules can differ based on the manufacturer [62]. After 5 hours of exposure to sunlight, a complete recovery of PID-p was observed on the front of n-PERT and TOPCON modules with a SiN_x/AlO_x passivation layer [127]. However, bifacial n-PERT cells with a front SiN_x/SiOx stack were unaffected under illumination [61]. It can be assumed that the module may have a minimal PID-p effect in the field if the characteristics of the dielectric permit PID-p light recovery faster than PID-p deterioration. Moreover, a high irradiance must be reflected on the module rear for the PID-p recovery. Consequently, the amount of irradiance that can reach the module rear depends on the mounting arrangement. Furthermore, surface albedo can also influence rear-side recovery as it can range from 16% (concrete) to 90% (snow) [43], [147].

CHAPTER 3: METHODOLOGY

3.1 Impact of PID due to Backsheet, Encapsulant, and AS coating (One Cell Modules)

Synopsis: PID-s can reduce the performance of PV modules in the field. The majority of PID studies are focused on preventing PID by altering the glass, cell, or encapsulant in PV modules. The impact of backsheet type on PID-s hasn't received much attention in research. Since the backsheet type affects the rate of water vapor transfer, this significantly impacts the conductivity of the encapsulant and, in turn, the amount of voltage drop in the encapsulant layer during the PID stress. Lower voltage drops in the encapsulant and severe PID are associated with higher encapsulant conductivity. Hence, this study uses different backsheet and encapsulant materials to understand the impact of PID due to these components. Moreover, a method for preventing PID using an AS coating on the front glass is also explored.

Experimental Setup: This investigation included a total of seven identical one-cell modules. The effects of the various backsheets were examined in five of them. A single module with a different encapsulant was employed to investigate the impact of the encapsulant on the backsheet because of PID. One module was used to explore the impact of using AS coating on the front glass. The glass, encapsulant, cell, encapsulant, and backsheet comprise the structure of single-cell modules, like commercial modules, with alterations made for the necessary testing in the backsheet and encapsulant. Low iron, 203 x 280 x 3.2 mm solar glass was used. An aluminum BSF solar cell with a 156mm x 156mm p-base monocrystalline silicon substrate was utilized. Using a semiautomatic tabbing machine, a 60-Sn/40-Pb tabbing ribbon was soldered onto the busbars of the cells to form the connections. A 150 °C temperature was applied for lamination. At the cell's back,

silicone PV-804 sealant was used to attach single-pole junction boxes [168]. 3M aluminum tape was utilized to cover the sides of the one-cell modules to imitate a frame for PID testing. The figure below shows the one-cell modules used in the study.

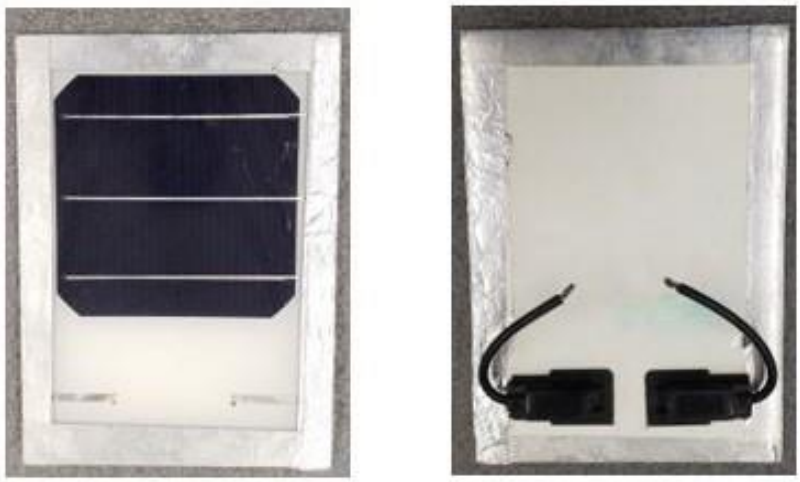

Fig. 27. Module construction used in the study

This investigation employed various backsheets from five manufacturers—namely, Backsheet-1 (BS-1), BS-2, BS-3, BS-4, and BS-5. With a thickness of 0.34mm, BS-1 is a standard Tedlar/polyvinyl fluoride (PVF)-polyethylene terephthalate (PET)-Tedlar/PVF (TPT) backsheet. Polyvinylidene Difluoride (PVDF), adhesive, PET, and Florine film (a patented substance) make up BS-2 with a thickness of 0.32mm. BS-3 has a 0.39mm thickness and comprises Polyamide (PA), Aluminum, PET, and PA. The thickness of BS-4 is 0.31 mm and is composed of ethylene chlorotrifluoroethylene (ECTFE)-an adhesive-and-PET-an adhesive. BS-5 comprises PVDF-an adhesive-PET-an adhesive with 0.32 mm total thickness. All five backsheet structures are shown in the figure below.

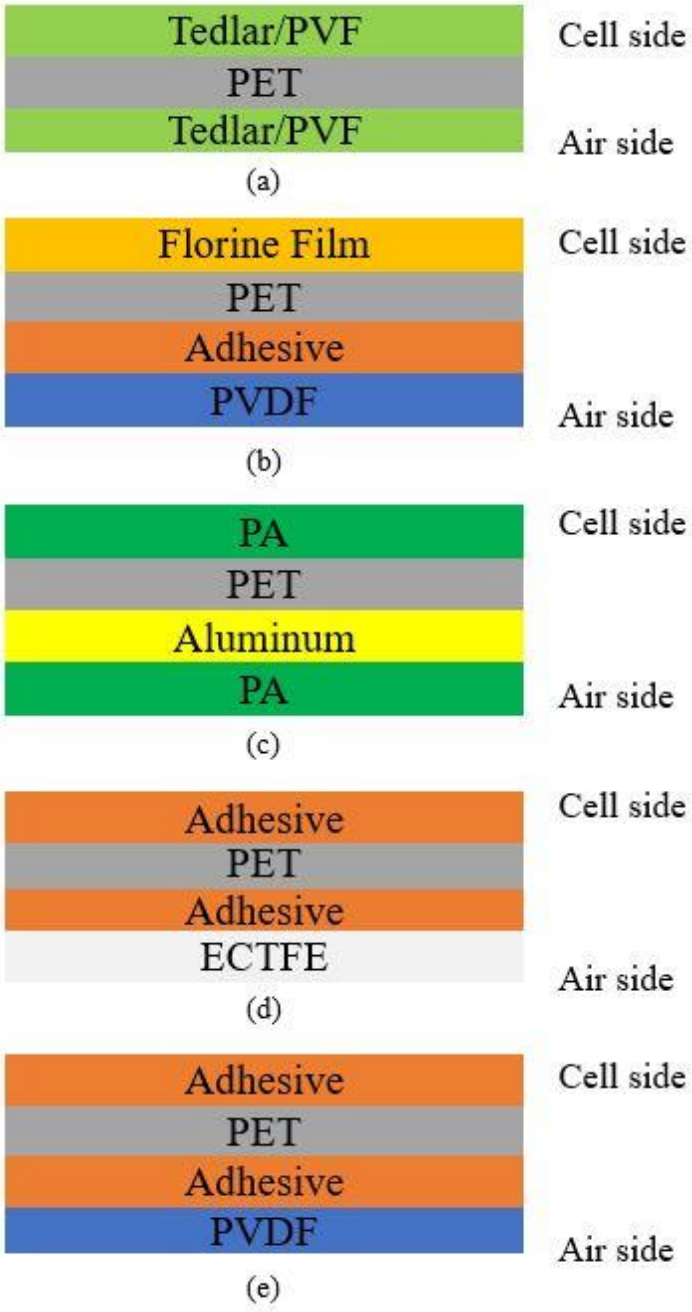

Fig. 28. Cross-section of the backsheets used in this study. (a) BS-1 (TPT). (b) BS-2. (c) BS-3. (d) BS-4. (e) BS-5.

Six modules have EVA as the encapsulant with a thickness of 0.46mm. One module has POE as the encapsulant with a similar thickness as EVA to understand the impact of a different encapsulant relative to the backsheet. Furthermore, one module was coated with

the AS coating on the front glass to study its impact on PID. The table below reviews the details mentioned above.

Table 3. Testing configuration for the one-cell modules

One-cell modules	Backsheet type	Encapsulant Type	AS coating
Module-1/ M-1	BS-1	EVA	No
Module-2/ M-2	BS-2	EVA	No
Module-3/ M-3	BS-3	EVA	No
Module-4/ M-4	BS-4	EVA	No
Module-5/ M-5	BS-5	EVA	No
Module-6/ M-6	BS-4	POE	No
Module-7/ M-7	BS-3	EVA	Yes

Pre and post-characterization tests were done to determine the change in performance parameters for all the modules. These tests included: Indoor light IV utilizing a solar cell IV tracer with a short arc xenon lamp at STC for determining IV parameters, EL through an EL camera at 100% and 10% I_{SC} at a 30s exposure for EL images analysis, and dark IV for determining R_{SH} and R_S. Following IEC standard 62804-1, the modules were put for PID stress in an indoor environmental chamber at -1000 V, 85°C, and 85% RH. By shorting the module connections, a negative voltage was sent to each one-cell module's cell, while a positive voltage was delivered to the faux metal frame that covered the sides. Using a Keithley datalogger, the LC was also monitored during the experiment. The modules did not significantly degrade during the first 96 hours of the PID stress (round 1). To determine how PID impacted all the modules, the single-cell modules were put to round 2 of PID stress in the environmental chamber for 192 hours, totaling 288 hours of PID stress. The test method's general layout is shown in Fig. 29, and the chamber setup is shown in Fig. 30.

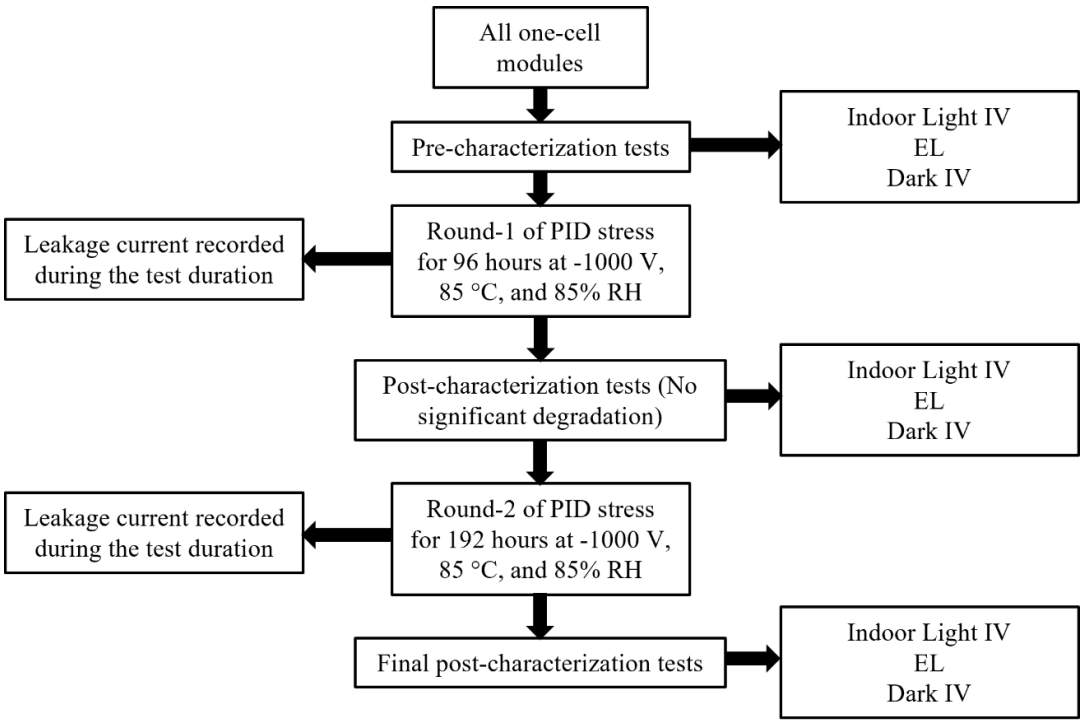

Fig. 29. Testing method for the one-cell modules

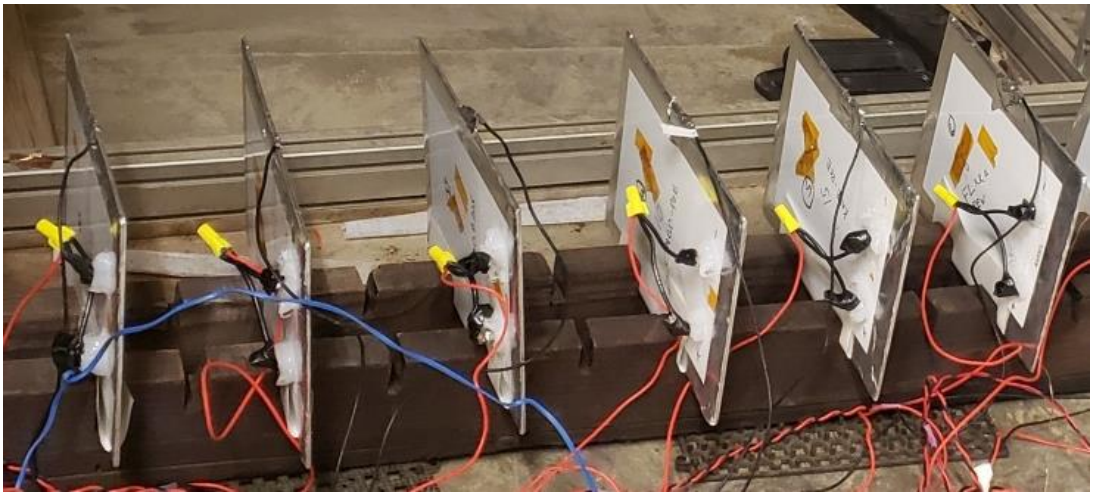

Fig. 30. Test layout for PID in the environmental chamber

3.2 Impact of PID on DH-stressed GG and GB modules (Commercial Modules)

Synopsis: The GB PV module has long been the industry standard, but the GG module is gradually gaining ground. PV modules in hot, humid areas with high string voltages are susceptible to degeneration due to PID. As per the literature, PID has only been researched thus far on brand-new modules with high interfacial adhesion. After a few years in the field, the PV modules exhibit poor interfacial adhesion. Evaluation of PV modules with poor interfaces is thus crucial. In this study, GG and GB PV modules are exposed to DH2000 at 85°C and 85% RH in an environmental chamber to understand the susceptibility to PID due to reduced interfacial adhesion strength. This approach is more field-representative. However, it must be understood that this study's purpose is not to compare GG and GB modules.

Experimental Setup: Two identical GB modules from Company A and two identical GG modules from Company B were employed for this study. The GB module weighs 23 kg, measures 2004 mm by 996 mm by 35 mm, and comprises of glass-encapsulant-cell-encapsulant-backsheet-frame. It is a 380 W mono-facial module with 144 cells arranged in a half-cut arrangement. The cells used are PERC measuring 78 mm x 156 mm. The frame is made of anodized Al alloy, the front glass is 3.2mm coated tempered glass, and the encapsulant utilized is EVA. The GG module is a 33.5 kg, bifacial, frameless module made of glass, encapsulant, cell, and glass that measures 1991 mm by 989 mm by 7 mm. It uses 72 full bifacial cells, which are PERC (156 mm x 156 mm) with a module power rating of 360W. The glass utilized for the front and back is 3.2 mm thick tempered glass, and the encapsulant is EVA. Fig.31 below shows the modules, and Table 4 shows the nameplate data.

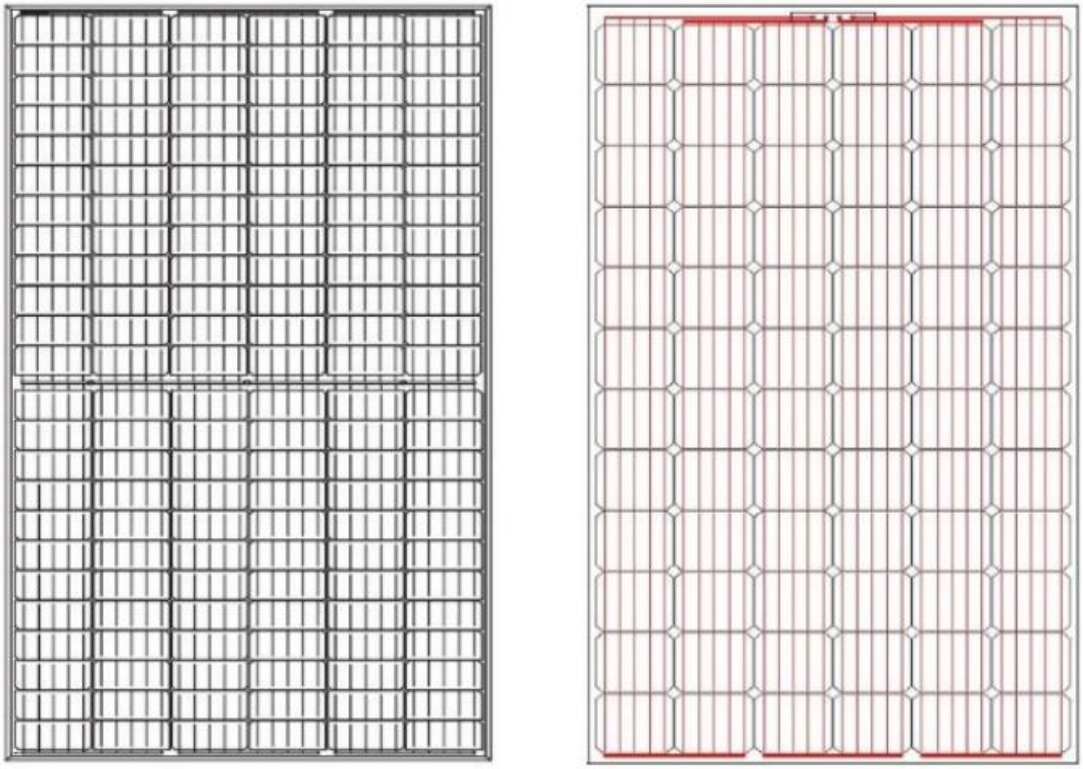

Fig. 31. GB module (left in black). GG module (right in red)

Table 4. Nameplate IV parameters at STC, maximum current (I_{MP}), maximum voltage (V_{MP})

Module	**I_{SC}/A**	**V_{OC}/V**	**I_{MP}/A**	**V_{MP}/V**	**FF/%**	**Pmax/W**
GB	9.96	49.0	9.36	40.6	77.9	380.0
GG/Front	9.99	47.6	9.32	38.6	75.8	360.0

According to IEC 61215-2, all four modules were subjected to DH stress in an indoor environmental chamber under short circuit conditions for 2000 hours at 85°C and 85% RH. The same modules were then exposed to PID in an indoor environmental chamber at 1000 V, 60 °C, and 85% RH following IEC 62804-1.

For PID, the modules were stressed for both negative and positive bias. A negative voltage was applied to the cell via shorted module connections to stress one GB and one GG module under negative polarity, and a positive voltage was maintained for the frame.

For positive bias (other GB and GG modules), a positive voltage was applied to the cell via shortened module leads while the frame was at a negative potential. The anodized Al frame was removed for the GB modules to reveal the conductive Al layer underneath to provide the frame with voltage. For GG modules, the voltage was supplied by building a faux Al frame covering all four sides of the module using 3M Al tape since the GG module was frameless. The conductive copper tape was applied at the module borders to guarantee perfect electrical continuity throughout the frame.

Two rounds of PID stress application were performed, with round 1 lasting 96 hours. Since round 1 revealed slight deterioration, round 2 for 192 hours of PID stress was carried out, totaling 288 hours of PID stress. A Keithley datalogger was also used to observe the LC during both PID cycles.

Pre and post-characterization tests were performed to determine the change in performance parameters for all the modules. These included: outdoor light IV was used for determining the IV parameters (results were converted to STC at 1000 W/m^2 and 25°C), EL was used for EL analysis, and dark IV was done to compute R_{SH} and R_S (calculated using the slope method). To assess the impact of the stress testing on the performance of all the modules, reflectance tests and outdoor IR imaging for possible hot cells were also performed before and after the stress tests. The approach utilized to test all the modules is shown in Fig. 32 [169].

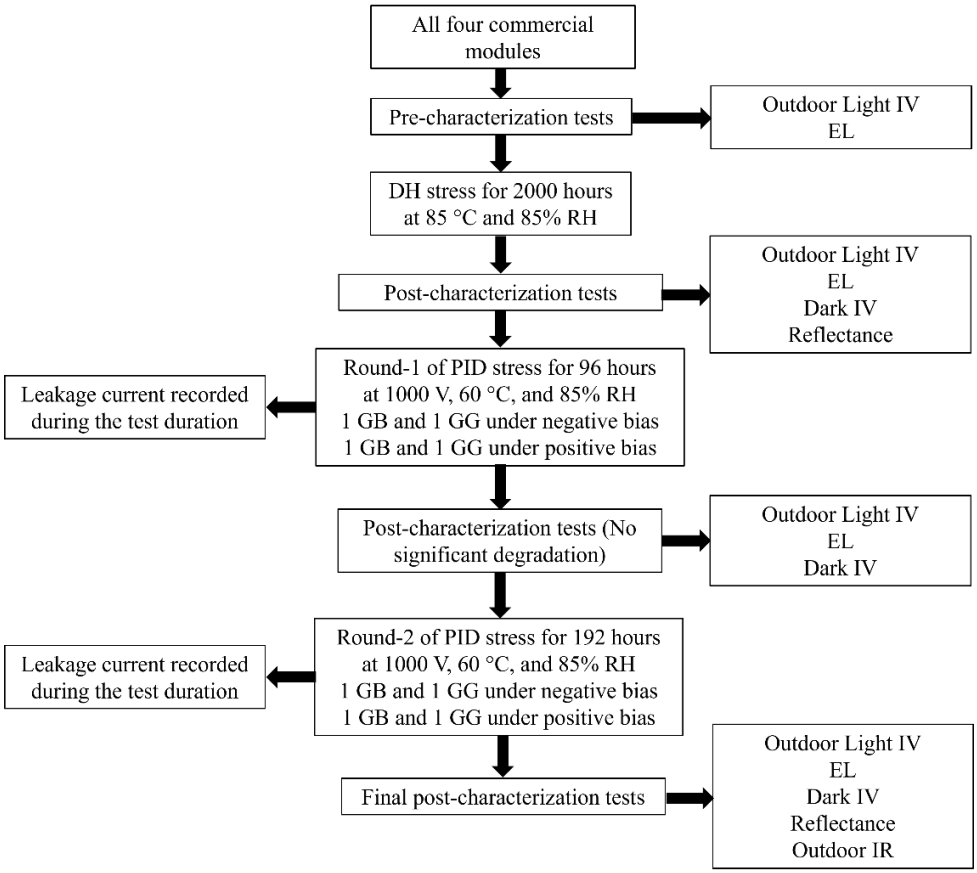

Fig. 32. Testing method for the GG and GB modules

3.3 Impact of PID (focus on PID-p) on Bifacial Modules (Commercial Modules)

Synopsis: PV strings operating at high voltages in hot, humid environments are susceptible to PID. PID-p is the fastest PID mechanism and can reduce module power quickly. PID-p may sometimes be restored under the light in specific circumstances. However, this effect is less prominent on the rear side of bifacial PV modules receiving lower irradiance. Comprehending PID-p in bifacial modules is critical since they will overtake monofacial PV modules as the industry standard over the next 10 years. In this work, we conducted indoor PID testing on 14 commercial bifacial p-PERC modules to induce PID-p (three different module construction, three different manufacturers). The aluminum foil technique

is used to conduct four rounds of PID testing for 168 hours at 25°C and 54% RH. Both positive and negative voltage bias are examined for each module side. The findings reveal that Pmax loss of up to 32% under STC and 51% at low irradiance can occur in certain instances. Recovery under sunlight is also carried out; results indicate that Pmax has recovered almost entirely. Since there is a lack of a thorough investigation of PID-p utilizing commercial bifacial PV modules (on both sides under positive and negative bias), the findings of this research can be significant to the PV community and industry. This work can provide insight into PID problems in bifacial PV modules, which are projected to rise in popularity in the coming years.

Experimental Setup: A total of 14 commercial bifacial PERC modules were used. These included three distinct bifacial module construction types from three separate manufacturers. The module information is compiled in Table 5. According to IEC standard 62804-1, the modules were stressed for PID using the Al foil technique for 168 hours at +/- 1500V, 25°C, and 54% RH (to imitate Arizona weather conditions). PID stress was applied to the module four times, with each round focusing on a different side under a different polarity. The cell's potential was maintained on the module's unstressed side. This technique was used to apply monofacial PID stress on the stressed side of the module while avoiding stress on the non-stressed side [170]. For instance, if the rear side is stressed at a negative bias, it means that the cell is at a negative potential, the stressed rear side is at a positive potential, and the unstressed front side is at a negative potential (same potential as the cell). After recovery, M-B was utilized in rounds 3 and 4 due to module unavailability.

Fresh modules were used for this study. The specifics of the PID testing are shown in Table 6. To prevent foil from coming into touch with the module frame, the module

edges were taped with Kapton. The front and back of the modules had rectangular-shaped Al sheets applied to them (the front and rear Al sheets were not in touch), and 3M Al tape was used to establish an electrical connection between the small sheets (to ensure Al foil was in good contact with the module surface). To provide proper contact between the Al foil and the module surface (front/rear), roofing material (thermoplastic polyolefin rubber membrane) was applied to the modules' front and back. To ensure that the Al foil made complete contact with the module surface, the modules were positioned horizontally on a test rack inside the environmental chamber, extra insulated weights were also positioned at the top, and horizontal platforms were placed on the back of the modules. The module testing setup for each cycle is shown in Fig. 33.

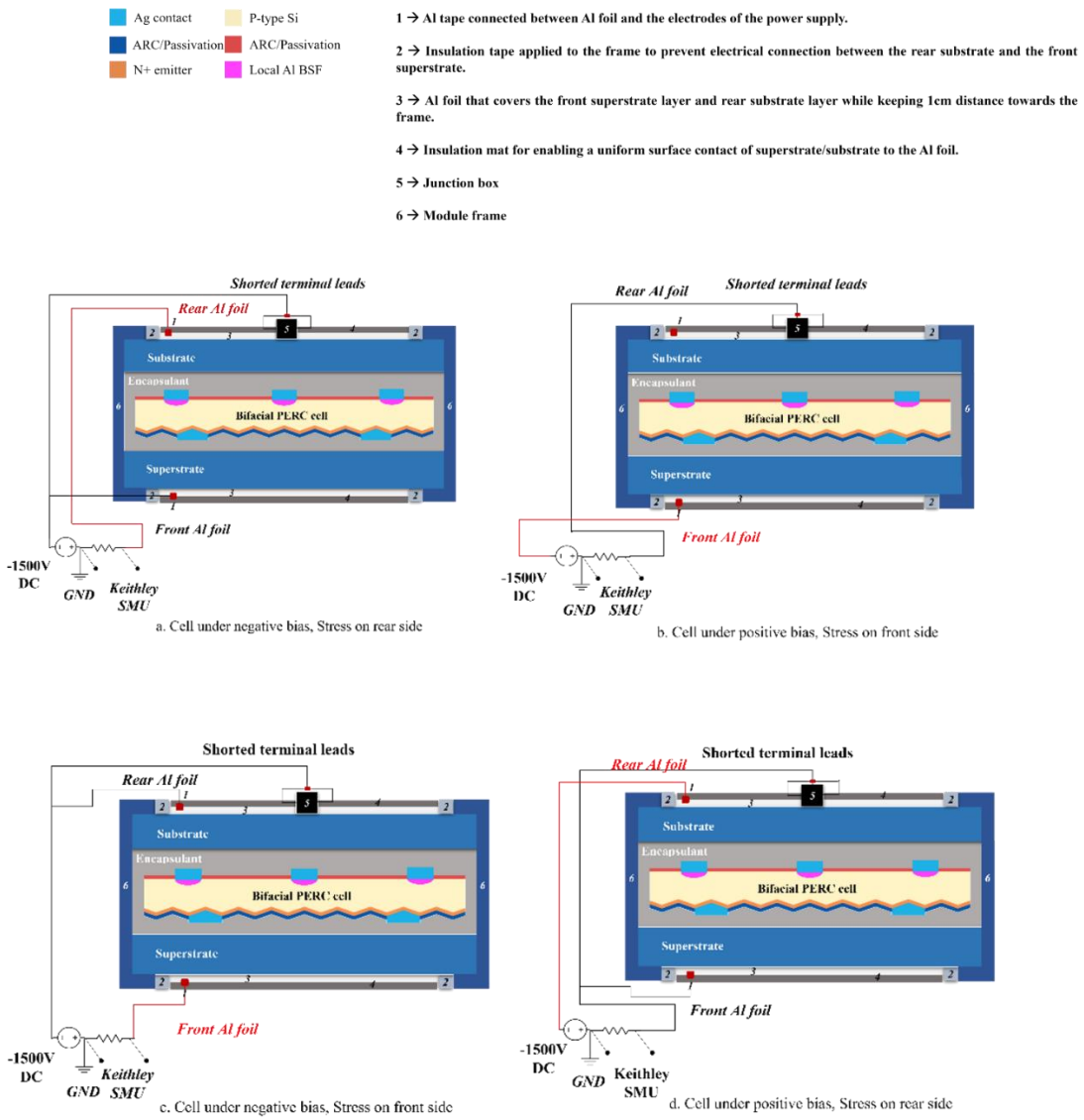

Fig. 33. Methodology for (a) Round-1, (b) Round-2, (c) Round-3, (d) Round-4

Table 5. Module Details

Module Name	Number of Modules	Manufacturer	Module Construction	Cell type and dimensions	Encapsulant
M-A	4	A	GG-NF (2*3.2mm glass)	PERC-72-Full-cell 156 x156 mm	EVA

M-B	2	B	GG-F (2*2.0mm glass)	PERC-144-Half-cut78 x156 mm	EVA
M-C	4	C	G-TBS-F (3.2mm glass)	PERC-144-Half-cut 78 x156 mm	EVA
M-D	4	A	G-TBS-F (3.2mm glass)	PERC-144-Half-cut 78 x156 mm	EVA

Table 6. Testing details

Round	**Cell Polarity**	**Stressed side**	**Modules tested**	**Expected PID mechanism according to literature in p-PERC cells (Detail in the literature review section)**
1	Negative (-ve)	Rear	MA-1, MB-1, MC-1, MD-1	PID-p, PID-c, Na penetration
2	Positive (+ve)	Front	MA-2, MB-2, MC-2, MD-2	PID-p, PID-c
3	Negative (-ve)	Front	MA-3, MB-1, MC-3, MD-3	PID-s
4	Positive (+ve)	Rear	MA-4, MB-2, MC-4, MD-4	No impact

The main aim of this study was to test the susceptibility of PERC bifacial modules to PID-p, though other PID mechanisms are also considered, but the focus is on PID-p.

Pre and post-characterization tests, including Flash IV and EL, were conducted before and after each round to examine the change in performance characteristics. The Spire 5600, which has a class A+ spectrum, was used for Flash IV. For each module, the IV was performed on both sides at low irradiance (200W/m^2) and at STC (1000W/m^2). Control modules were also employed to guarantee the same settings throughout the experiment. IV parameters, including Pmax, FF, ISC, VOC, $R_{SH,}$ and R_S, were acquired

through the Flash test for the EL Sensovation HR-830 camera model was used. At 100% and 10% I_{SC}, EL was performed on both module sides, and image analysis was also used to determine the gray value.

A series of EL images were taken for severely deteriorated modules at bias levels of 0.4A, 0.55A, 10%, 40%, 70%, and 100% of I_{SC}. The cell-level dark IV curves were extracted from these images by analyzing them using the EL sweep technique described in [171]. The model in [172] was then used to evaluate these curves and derive R_S and the J_{01}. Using a Keithley data logger, the LC for each cycle of PID stress was also measured.

With an average dose of 19.4 kWh/m^2 for the module front and 18.4 kWh/m^2 for the module rear, the modules with the greatest deterioration were also recovered in open circuit under sunlight. The testing and recovery strategy for the experiment is shown in Fig. 34 and 35 [173].

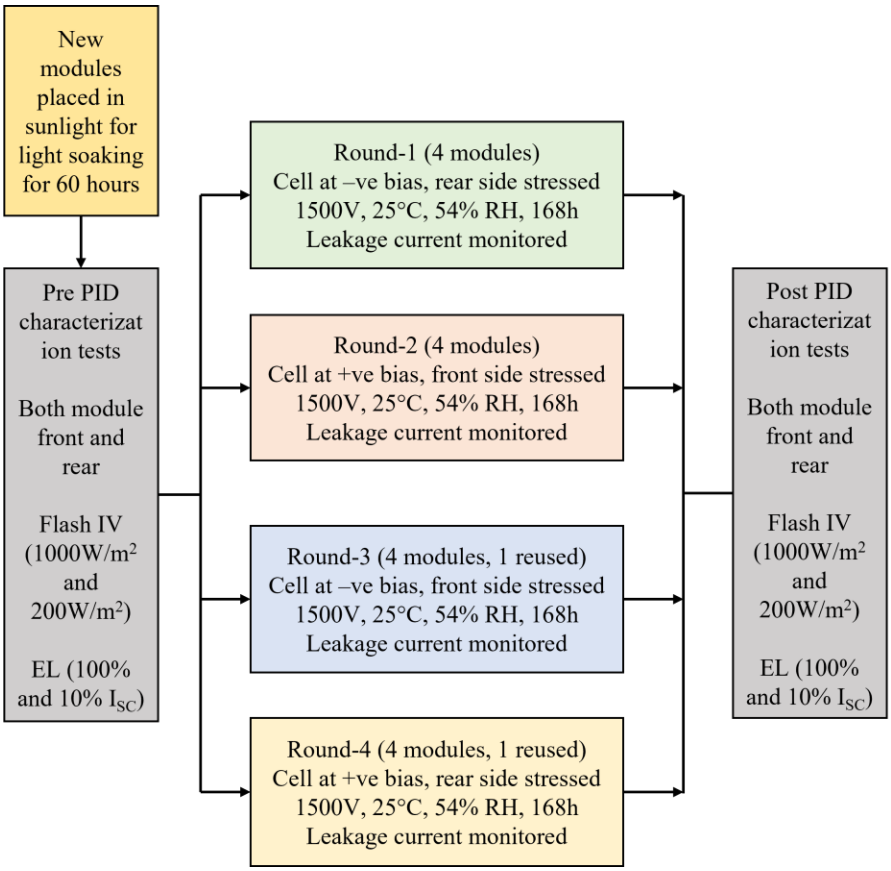

Fig. 34. Testing method for PID

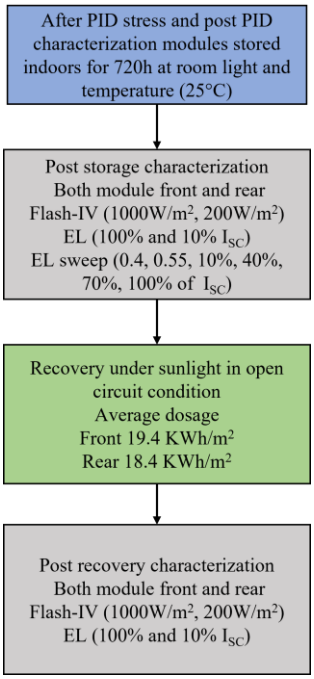

Fig. 35. PID recovery method

CHAPTER 4: RESULTS AND DISCUSSION

4.1 Impact of PID due to Backsheet, Encapsulant, and AS coating (One Cell Modules)

The degradation in the modules due to the PID stress is detailed in the sections below. The backsheet section discusses the impact of PID on the different backsheet materials. The Encapsulant section talks about the influence of PID due to encapsulation. The AS Coating section examines the effect of PID due to the application of AS coating on the front glass of the module.

The percentage difference between pre-stress (0h) and post-stress characterization (96+192h) is calculated using the following equation.

$$\%\ degradation = \frac{Post\ data - Pre\ data}{Pre\ data} * 100 \qquad 3$$

Backsheets: For all one-cell modules with various backsheets, Pmax, FF, I_{SC}, and V_{OC} degradation percentages are shown in Fig. 36. Utilizing indoor light IV, this information is gathered for all the modules pre and post-stress. The findings demonstrate that the different backsheet materials influence the PID phenomenon-related deterioration. The results demonstrate that PID-s produces the least deterioration in Pmax (1.613%) and FF (1.351%) for the one-cell module with BS-1, while PID-s causes the most significant degradation in Pmax (8.690%) and FF (6.259%) for the module with BS-5. Based on the Pmax and FF degradation, the modules may be placed in the following order: M-5 (worst), M-4, M-3, M-2, and M-1 (best).

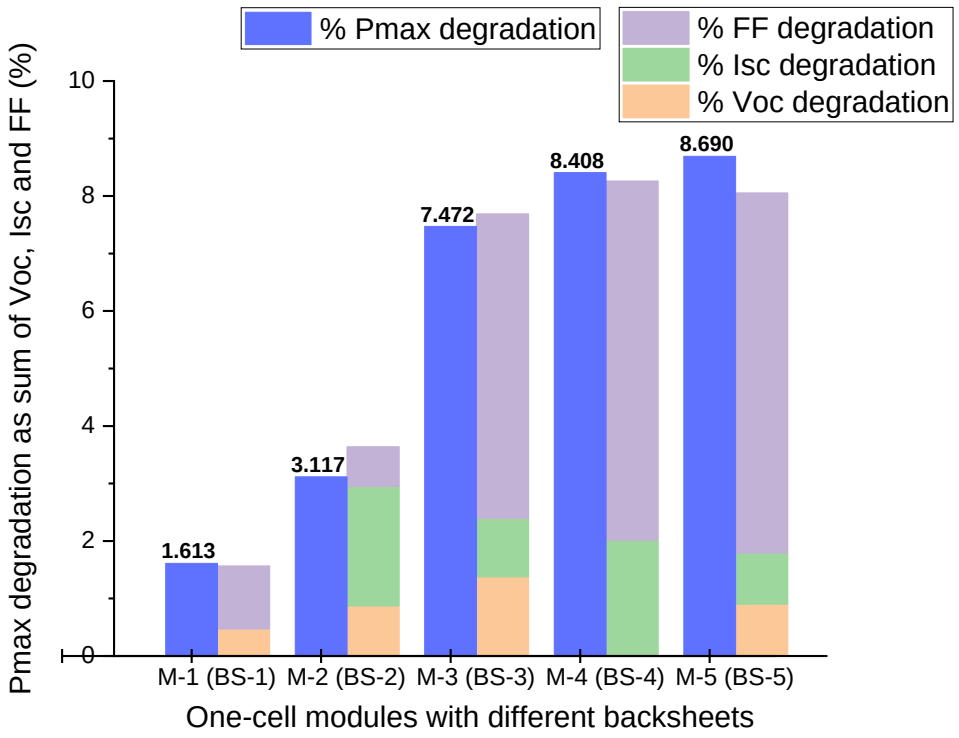

Fig. 36. Degradation in IV parameters in the modules with different backsheets

The R_{SH} and R_S data pre and post-PID stress calculated using dark IV are shown in Table 7. Fig. 37 shows the % degradation in EL gray values against FF. Results are similar, as seen in Fig. 36.

Table 7. Pre and post-PID R_{SH} and R_S data for modules with different backsheets

One-cell modules	**R_{SH} (Pre-0 hrs) / Ω**	**R_{SH} (Post 96+192 hrs) / Ω**	**R_S (Pre-0 hrs) / Ω**	**R_S (Post 96+192 hrs) / Ω**
M-1	695.825	40.502	0.014	0.015
M-2	1065.300	14.503	0.016	0.016
M-3	264.220	1.900	0.014	0.014
M-4	895.000	12.187	0.015	0.020
M-5	1410.080	2.840	0.014	0.015

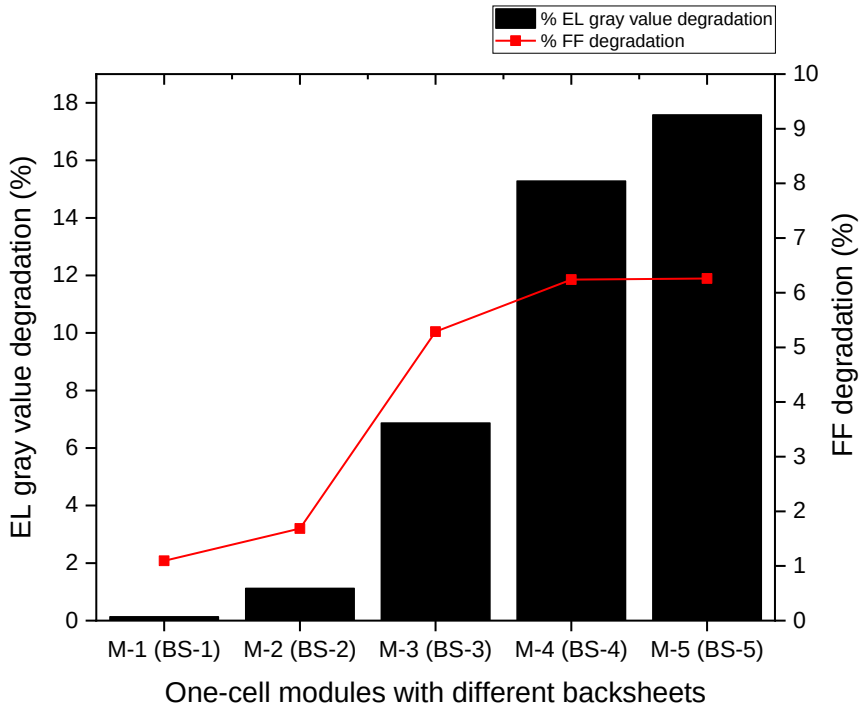

Fig. 37. % EL gray value and FF degradation in the modules with different backsheets

The EL patterns for each one-cell module before and after stress are shown in Fig. 38. Additionally, gray value analysis using these EL images is carried out. Fig. 36 shows the % change in value between pre- and post-characterization. Again, it is clear from the EL images and the plot that as the FF deteriorates for these modules mainly due to a decrease in R_{SH}, as shown in Table 7, the EL gray value also deteriorates. As a result, more darkened EL images are seen, with M-1 (BS-1) showing the least degradation and M-5 (BS-5) showing the most. The degradation is more pronounced at the margins, indicating that deterioration occurs because moisture enters the module's edge.

Fig. 39 displays the LC in microamps (uA), along with the average values; The results show that M-4 (BS-4) has the highest LC, and the best performing module is M-1

(BS-1) with the lowest amount of LC. M-2, 3, and 5 are outliers in the data for the LC. This can be understood, as mentioned in literature [174], that LC can be a sign of PID, but there is no correlation between the two. This implies that LC may not be sufficient to predict whether a certain module would deteriorate higher or lower. However, it acts as a signal that the PID phenomenon could manifest [175].

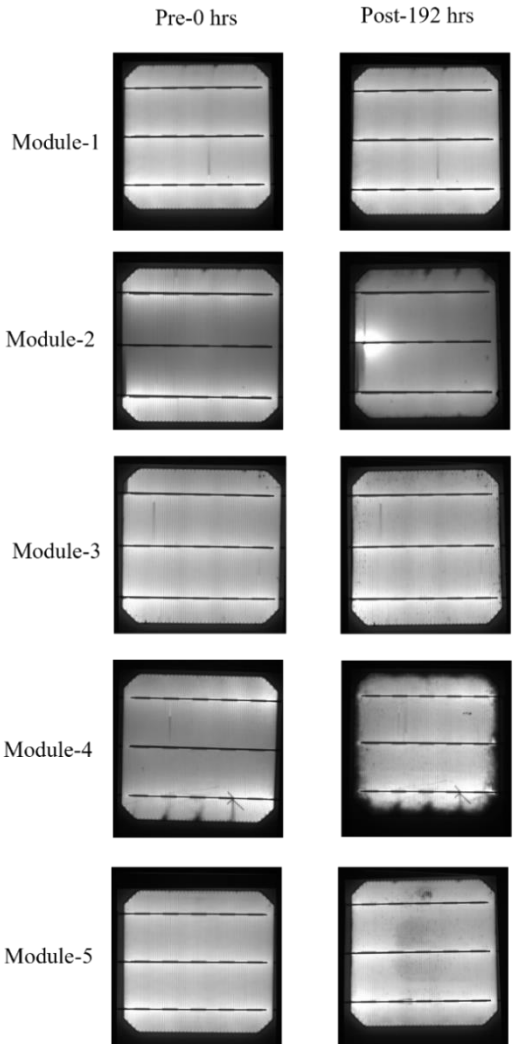

Fig. 38. EL images pre and post-PID stress for modules with different backsheets at 100% I_{SC} and 30 s exposure

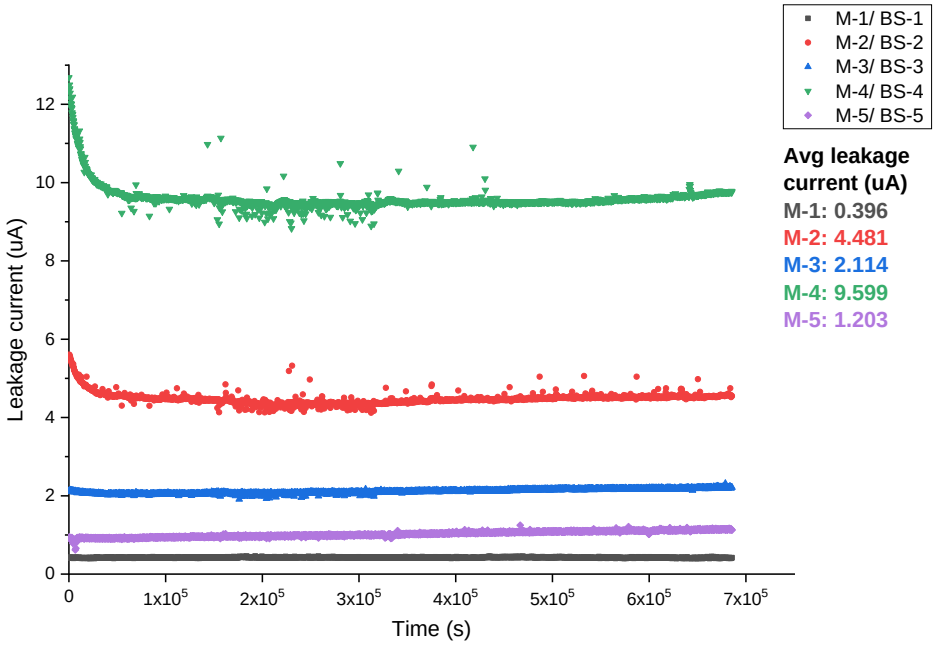

Fig. 39. Time series plot of LC for 192 h of PID stress for modules with different backsheets

The modules may be organized in the following order according to the % deterioration in the Pmax, FF, RSH, and EL gray value data computed using the pre- and post-stress tests.

Table 8. Ratings for the modules with different backsheets

One-cell modules	Backsheet	Performance
Module-1	BS-1	Best
Module-2	BS-2	Good
Module-3	BS-3	Average
Module-4	BS-4	Bad
Module-5	BS-5	Worst

Since these are polymeric backsheets, the one-cell modules experience PID-s with various backsheets as moisture may be injected into the modules via the backsheets at high temperatures and RH, as in this research (85 °C and 85% RH), which can result in PID mechanisms [45]. The performance of M-1 with BS-1 is the best. The TPT backsheet (BS-

1) comprises Tedlar/PVF-PET-Tedlar/PVF. The TPT backsheet is a strong material [176] with a very low water vapor transfer rate (WVTR) of 0.08 (g*cm/cm2/d) [177], which means it absorbs less moisture. As a result, M-1 with BS-1 operates most effectively and has the least amount of PID-s. When the same TPT material was employed in a different investigation, the PID (for TPT)-related deterioration was similarly shown to be extremely low. As demonstrated in Fig. 36, M-2 with BS-2 performs the second best but is not as excellent as TPT. PVDF, an adhesive, PET, and a film made of Florine make up BS-2. Although this backsheet resembles the worst-performing BS-5, the Florine layer in BS-2, a proprietary material employed by the manufacturer and based on Fluro-skin technology, makes a difference. This Florine layer could be the key to improving M-2's performance and reducing the amount of PID-s it experiences. In terms of performance, M-3 with BS-3 is approximately midway between excellent and bad-performing modules. PA, Al, PET, PA, make up BS-3. The use of Al in the backsheet has been shown to reduce PID-s and consequently improve performance [178], which could account for why M-3 is exhibiting an average performance. PA is not as good as PET and is known to deteriorate more quickly than PET under severe DH conditions, resulting in chalking [176]. However, this work [178] used n-type c-Si cells with PVF-Aluminum-PVF (PAP) backsheets and was conducted under different conditions. Adding Al may improve a backsheets performance because free electrons in the Al reduce PID by partially reversing the electric field produced by the voltage bias. An electric field is created when a bias is placed between the front glass and the cell. Charge polarization resulting from the electric field pulls the free electrons in the backsheet. The secondary electric field produced by the generated charges cancels out the initial electric field.

Consequently, PID decreases [178]. Another advantage of having an Al layer in the backsheet might be that less moisture can penetrate, resulting in less encapsulant conductivity and lower PID. PET makes up the majority of BS-4 and BS-5 (M-4 and M-5). The maximum amount of PID is experienced by these two modules. This may be due to the material's increased susceptibility to moisture penetration, which increases the severity of PID-s [177]. Additionally, BS-4 and 5 only include two highly water-resistant layers (ECTFE, PVDF, PET). All three other backsheet materials have a minimum of three highly water-resistant layers (PA, Al, PET, PVDF, Florine film, and Tedlar/PVF), which improves their performance and reduces their susceptibility to PID.

According to the presented data, the backsheet material can impact PID-s; if the material has more water-resistant layers, the PID phenomena can be controlled, and deterioration can be minimized.

WVTR for all the backsheets may have allowed a measurement of the water uptake for all the materials. However, to avoid misinterpretation, this was not done based on the research of Kempe et al. He suggests that the RH only changes by a few percent at most and that most backsheets have an equilibration time constant of approximately a day. Such measurements may not help understand the PID effect based on the backsheet materials [179], [180].

Encapsulant: For one-cell modules with distinct encapsulants (EVA and POE) and BS-4 as the backsheet, the percentage drop in Pmax, FF, I_{SC}, and V_{OC} is shown in Fig. 40. The findings show that the module with POE has no degradation in Pmax (0%) or FF (0%), while the module with EVA has a reduction in Pmax of 8.408% and a decline in FF of 6.240% because of PID-s.

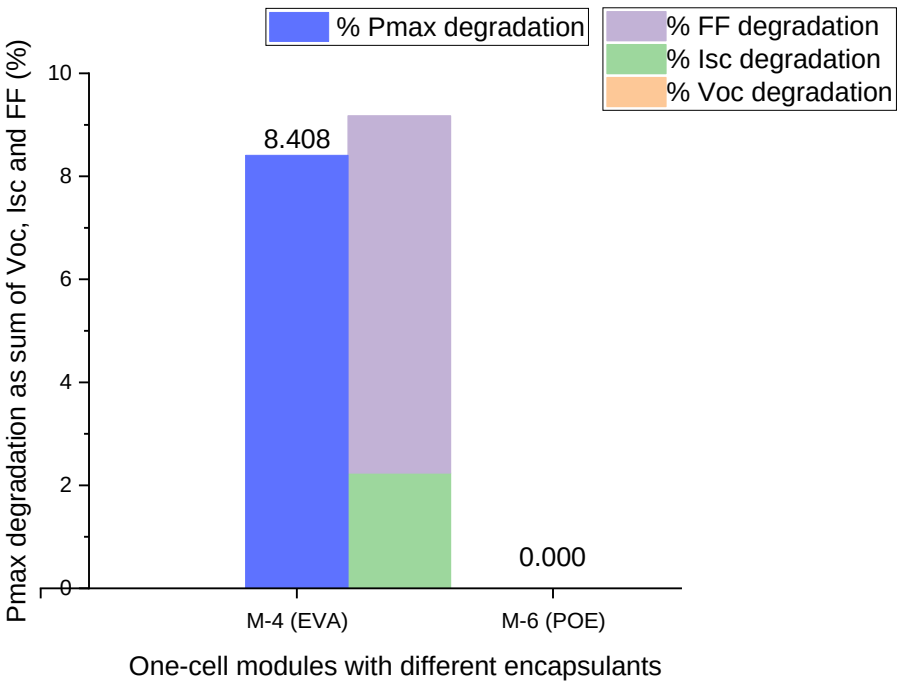

Fig. 40. Degradation in IV parameters in the modules with different encapsulants

The R_{SH} and R_S data pre and post-PID stress calculated using dark IV are shown in Table 9. Fig. 41 shows the % degradation in EL gray values against FF. Results are similar, as seen in Fig. 40.

Table 9. Pre and post-PID R_{SH} and R_S data for modules with different encapsulants

One-cell modules with the same BS	**Encapsulant**	**R_{SH} (Pre-0 hrs) / Ω**	**R_{SH} (Post 96+192 hrs) / Ω**	**R_S (Pre-0 hrs) / Ω**	**R_S (Post 96+192 hrs) / Ω**
M-2/ BS-4	EVA	895.000	12.187	0.015	0.020
M-6/ BS-4	POE	645.790	361.310	0.018	0.018

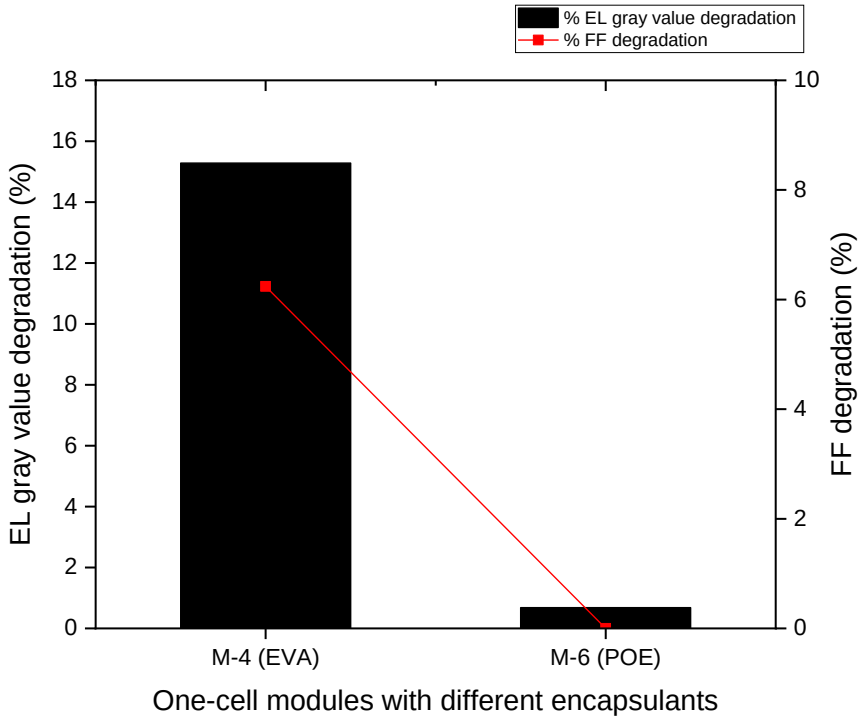

Fig. 41. % EL gray value and FF degradation in the modules with different encapsulants

The EL images for each one-cell module are shown in Fig. 42. The gray value analysis is also carried out and is presented in Fig. 41, along with the % FF deterioration. The EL images and plot demonstrate that where FF deteriorates more because of a decrease in R_{SH}, the EL gray value also deteriorates, leading to more black areas, as visible in the module. M-6 (POE) experiences virtually no PID, while M-4 (EVA) is significantly shunted due to PID-s.

The LC for M-4 (EVA) and M-6 (POE) is shown in Fig. 43, and M-6, with POE as the encapsulant, has a much lower leakage current than M-4 with EVA.

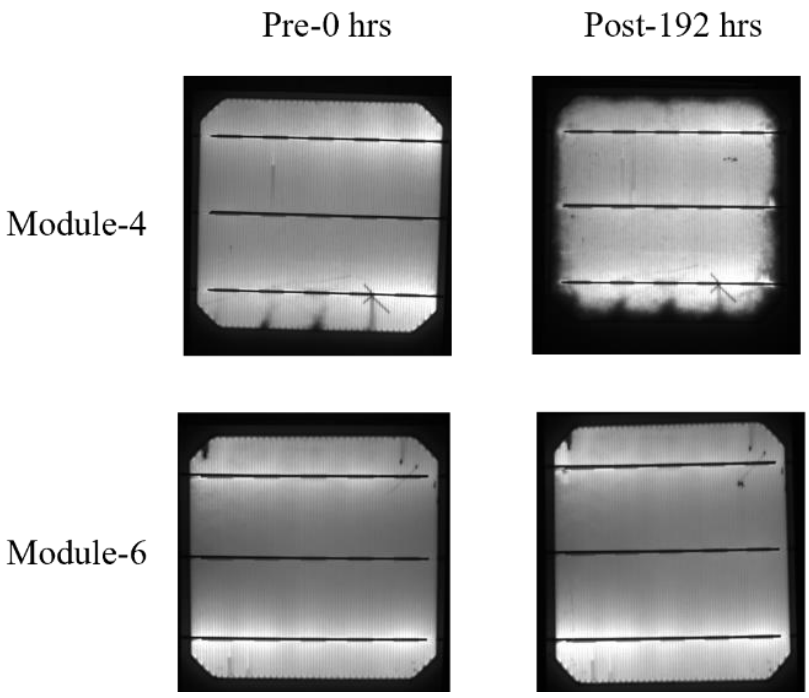

Fig. 42. EL images pre and post-PID stress for modules with different encapsulants at 100% I_{SC} and 30 s exposure

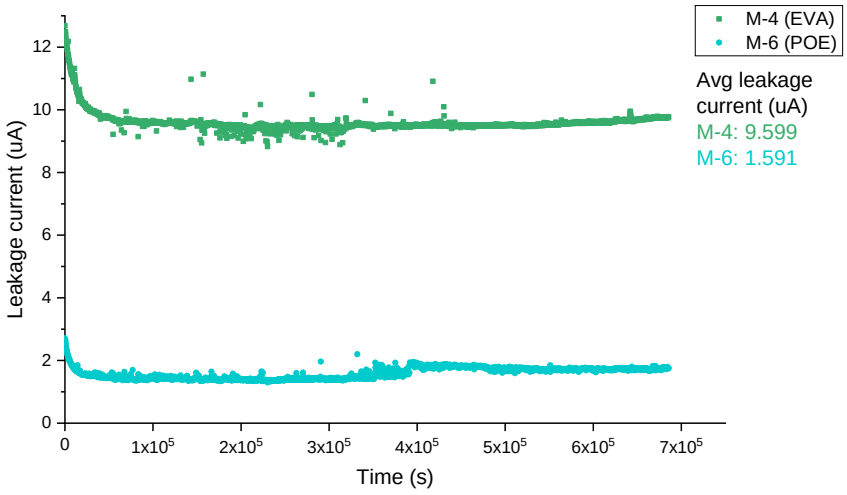

Fig. 43. Time series plot of LC for 192 h of PID stress for modules with different encapsulants

All the data indicates that POE (M-6) performs very well compared to EVA (M-4) as an encapsulant in the modules for preventing PID-s. This is primarily owing to the

significant volumetric resistance differential between POE (10^{15}–10 Ω cm) and EVA (10^{13}–10^{14} Ω cm) [137], which results in less PID deterioration [119]. Additionally, compared to EVA, which has a greater diffusion coefficient of $1.5x10^{-10}$ m^2/s and a higher water solubility of 30.5 $g/m^3/mbar$, POE has an extremely low diffusion coefficient of $2x10^{-9}$ m^2/s and water solubility of 1 $g/m^3/mbar$. The low permeability of the encapsulant is dictated by a lower diffusion coefficient and water solubility [181]. Numerous studies have assessed and shown the efficacy of POE against EVA in terms of decreased PID [123], [138], [182], [183]. Less activation voltage is available for PID owing to the high volumetric resistance of POE and its low diffusion coefficient and water solubility, which results in less degradation [184].

The interesting finding from this research is that M-4 with BS-4, constructed similarly to M-6 except for the encapsulant (EVA and POE), is one of the least effective modules in this study, with an 8% Pmax decrease. However, when POE is used instead of EVA in M-6 with the same BS-4, there is essentially no loss in Pmax. This shows that a good encapsulant with high volumetric resistance, reduced diffusion coefficient, and water solubility, such as POE, can eliminate the PID influence even if the backsheet has a high WVTR [180].

AS Coating: For one-cell modules with and without AS coating, the percentage drop in Pmax, FF, I_{SC}, and V_{OC} is shown in Fig. 44. The findings show that the module without AS coating shows a degradation in Pmax of 7.472% and FF of 5.287%, while the module with AS coating has a reduction in Pmax of 3.533% and a decline in FF of 2.564% because of PID-s.

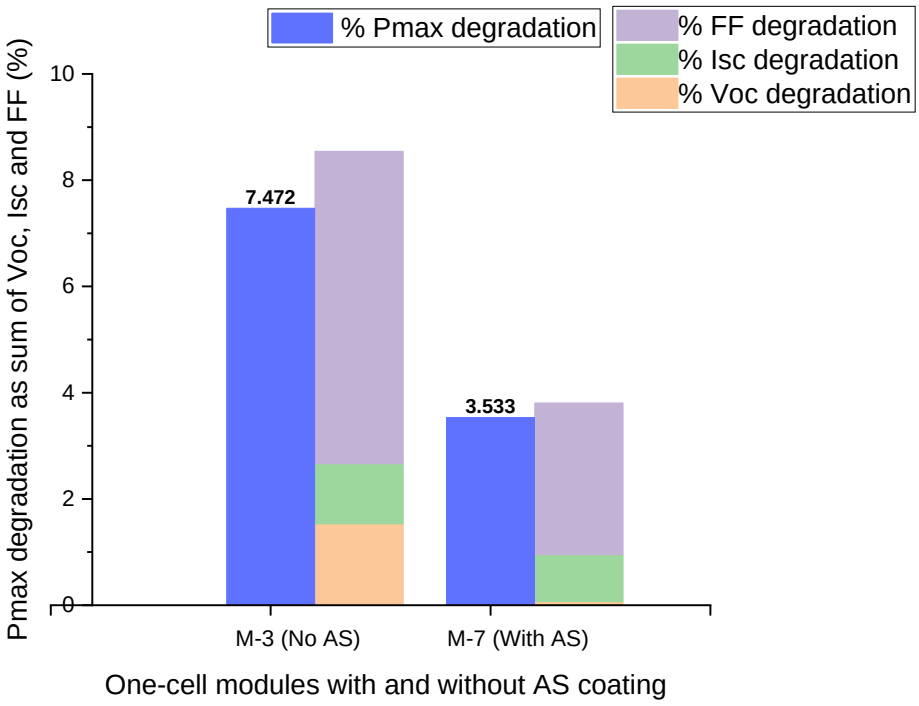

Fig. 44. Degradation in IV parameters in modules with and without AS coating

The R_{SH} and R_S data pre and post-PID stress calculated using dark IV are shown in Table 10. Fig. 45 shows the % degradation in EL gray values against FF. Results are similar, as seen in Fig. 44.

Table 10. Pre and post-PID R_{SH} and R_S data for modules with and without AS coating

One-cell modules with the same BS (BS-3) and encapsulant (EVA)	**R_{SH} (Pre-0 hrs) / Ω**	**R_{SH} (Post 96+192 hrs) / Ω**	**R_S (Pre-0 hrs) / Ω**	**R_S (Post 96+192 hrs) / Ω**
M-3 without AS	264.220	1.900	0.014	0.014
M-7 with AS	181.500	5.800	0.014	0.014

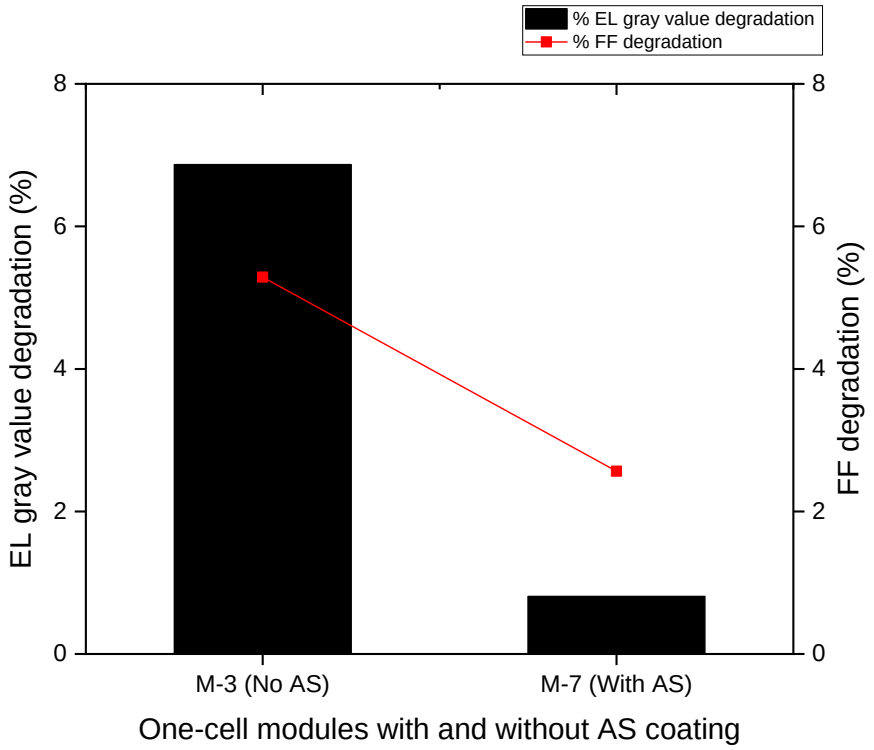

Fig. 45. % EL gray value and FF degradation in the modules with and without AS coating

The EL images for each one-cell module are shown in Fig. 46. The gray value analysis is also carried out and is presented in Fig. 45, along with the % FF deterioration. The EL images and plot demonstrate that where FF deteriorates more because of a decrease in R_{SH}, the EL gray value also deteriorates, leading to more black areas, as visible in the module. M-7 with AS coating experiences less PID, while M-3 without AS coating has more PID degradation.

The LC for M-3 (without AS coating) and M-7 (with AS coating) is shown in Fig. 47, and M-7, with AS coating, has a lower LC than M-3 without AS coating.

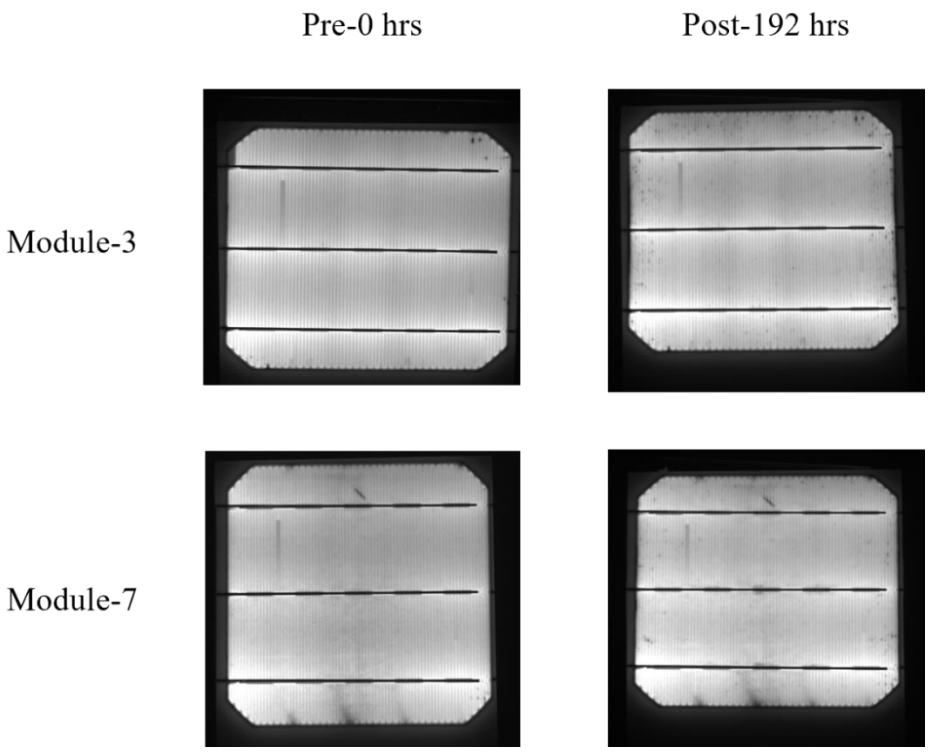

Fig. 46. EL images pre and post-PID stress for modules with and without AS coating at 100% I_{SC} and 30 s exposure

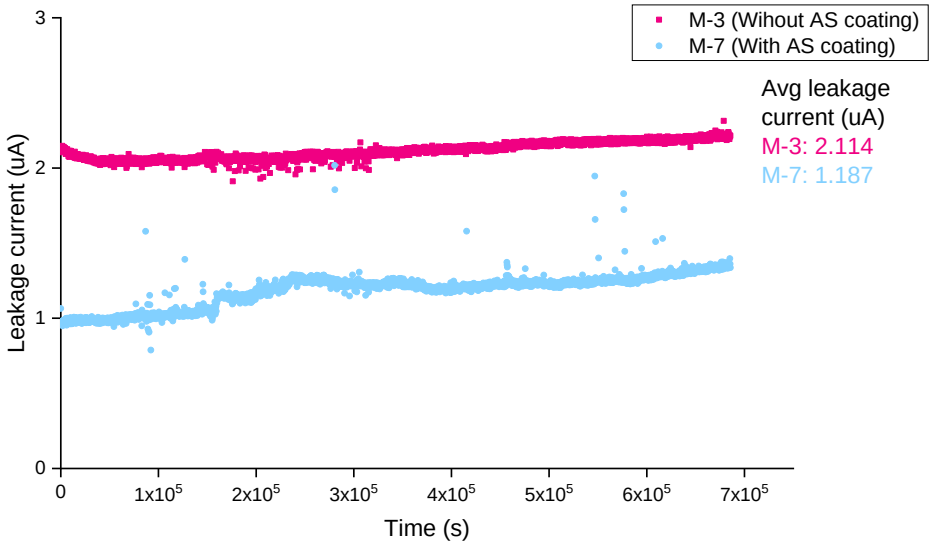

Fig. 47. Time series plot of LC for 192 h of PID stress for modules with and without AS coating

The results from IV data, EL, dark IV, and LC all indicate that applying the AS coating reduces the impact of PID-s. The primary cause of the decreased reduction in PID-s is the hydrophobic qualities of the AS coating, which prevent a persistent moisture buildup on the glass surface. As a result, the AS coating breaks up the glass's continuous surface conductivity [185], [186]. According to the literature [187], the bulk of the encapsulant, the bulk of the glass, and the surface of the glass all experience significant voltage drop from the applied voltage (1000V) during PID stress leaving only a minimal amount of the voltage (known as the activation potential) available for the sodium deposition reaction on the cell surface. When moisture is present on the glass surface, the surface conductivity increases, resulting in a low voltage drop and a more significant percentage of voltage remaining for the sodium deposition process. The voltage drop on the glass surface is increased by eliminating moisture from the glass surface or coating it with a hydrophobic AS coating. This reduces voltage availability for sodium deposition on the cell surface, lowering the PID loss [188].

4.2 Impact of PID on DH-stressed GG and GB modules (Commercial Modules)

The GG module section discusses the impact of sequential DH and PID in GG modules. The GB module section talks about the influence of sequential DH and PID in GB modules. The percentage difference between pre-stress (0h) and post-stress characterization (96+192h) is calculated using equation 3.

For GG modules, PID was done on both fresh and DH-stressed modules to confirm that DH-stressed modules will have a more severe PID effect than fresh samples. The fresh modules undergoing PID degraded by less than 1 %, whereas modules undergoing PID after DH had significantly more degradation.

Only DH-stressed modules were tested for PID due to resource unavailability for GB modules. The overall degradation in GB modules stressed for PID after DH was less, so by extrapolation, fresh samples would not have degraded due to the precedence set by the initial testing.

GG Modules-DH Stress: This study is based only on the front side of GG modules.

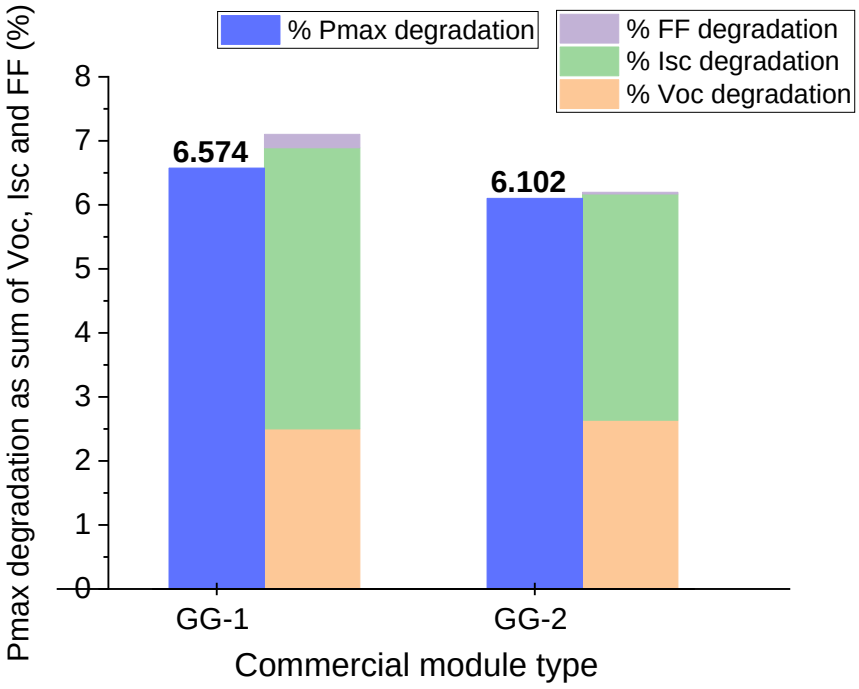

Fig. 48. Degradation in IV parameters after 2000 hours of DH stress

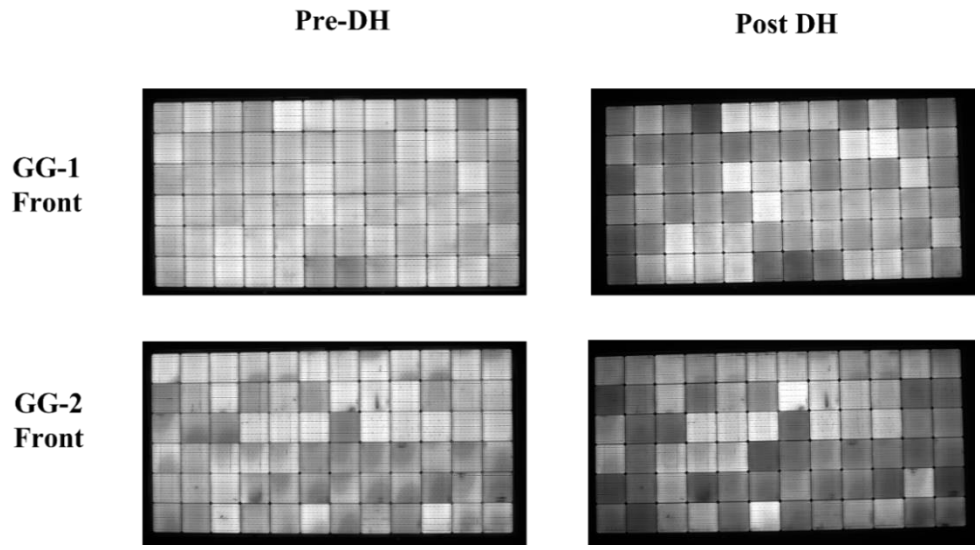

Fig. 49. Pre and post-DH EL images at 100% Isc and 60-sec exposure

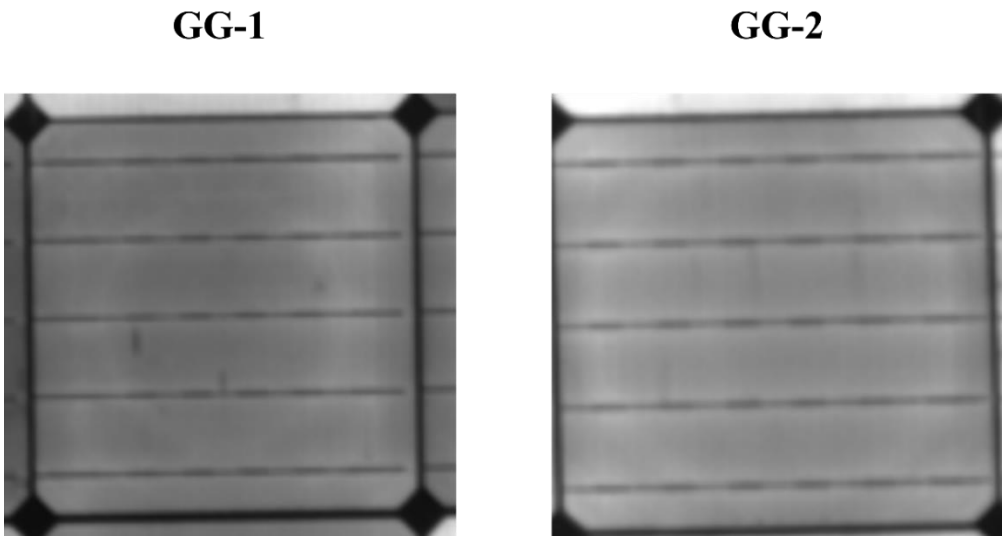

Fig. 50. Zoomed view showing the appearance of striation rings in GG-1 and GG-2 cells post-DH

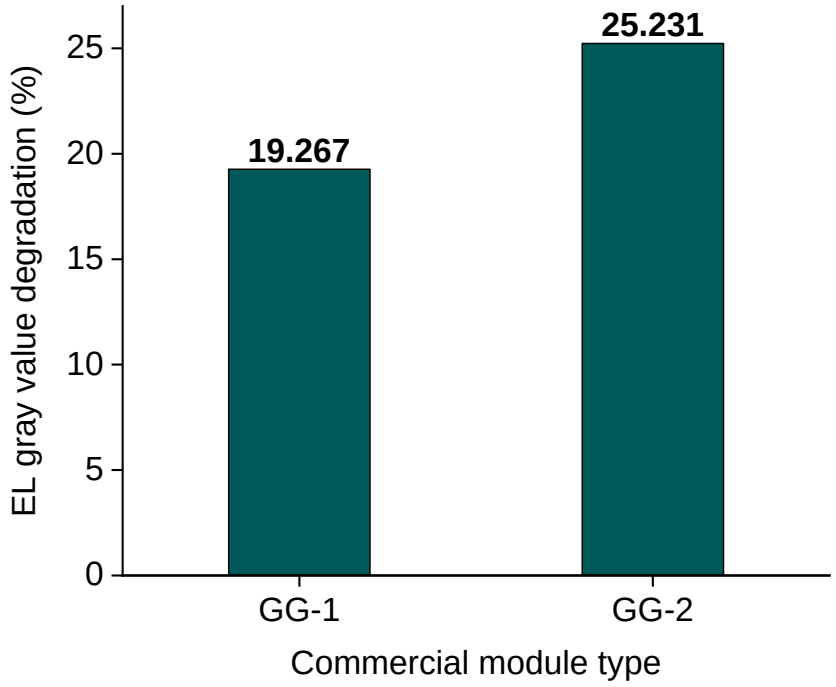

Fig. 51. % EL gray value degradation post-DH stress

The percentage deterioration for GG modules is shown in Fig. 48 for Pmax, FF, I_{SC}, and V_{OC}. Pre- and post-DH outdoor light IV data generated these outcomes. The findings show that DH stress causes GG modules to deteriorate by 6% to 7% in Pmax and 0% to 0.5% in FF. Losses in I_{SC} and V_{OC} affect the total loss of power (Fig. 48). Fig. 49 displays the EL images taken pre and post-DH stress. The EL gray value deterioration estimated from the pre-and post-EL images is shown in Fig. 51. After DH stress, cell darkening in GG modules is detected. Furthermore, the magnified image of the cells for GG-1 and GG-2 is shown in Fig. 50, and a circular ring can be seen on some of the cells after the DH stress.

Our investigation demonstrates that, as shown in Pmax and EL image analysis, the GG modules are more susceptible to deterioration because of the DH stress over 2000 hours (Fig.48,49,50, and 51). The primary purpose of the DH stress is to evaluate how sensitive the PV modules are to moisture [189]. Since water vapor cannot pass through the glass, using glass on the back instead of a backsheet should reduce the likelihood of moisture getting within the PV module [190]. However, the data computed in this study shows that these GG modules are more sensitive to moisture. Since these are frameless GG modules, a high-quality edge sealant is essential to reduce moisture ingress [74], [144]. Therefore, moisture penetration can be caused by the absence of or use of a low-quality edge sealant in these modules. According to Kempe et al. [179], [191], more significant deterioration in these GG modules owing to DH stress may be caused by EVA as the encapsulant (which has a high diffusivity) paired with a weak or no edge seal. According to EL analysis, cell darkening is detected in the GG modules, as seen in Fig. 49 and 50. Cell darkening in the module after DH stress is caused mainly by the acetic acid produced by EVA. The grid-contact resistance may be significantly increased by acetic acid's ability to damage the glass-cell interface [192]. Furthermore, the dual glass structure of GG modules can trap heat during DH stress and can cause cell deterioration [50], [193], [194]. This may be another factor contributing to their increased vulnerability to DH stress. Another result of the DH stress in the GG modules is the emergence of a ring-like structure, as illustrated in Fig. 50. The module manufacturing process can cause these circular structures called striation rings [20], [195], [196].

GG Modules-PID after DH stress: GG-1 was stressed under a negative bias, and GG-2 was stressed under a positive bias.

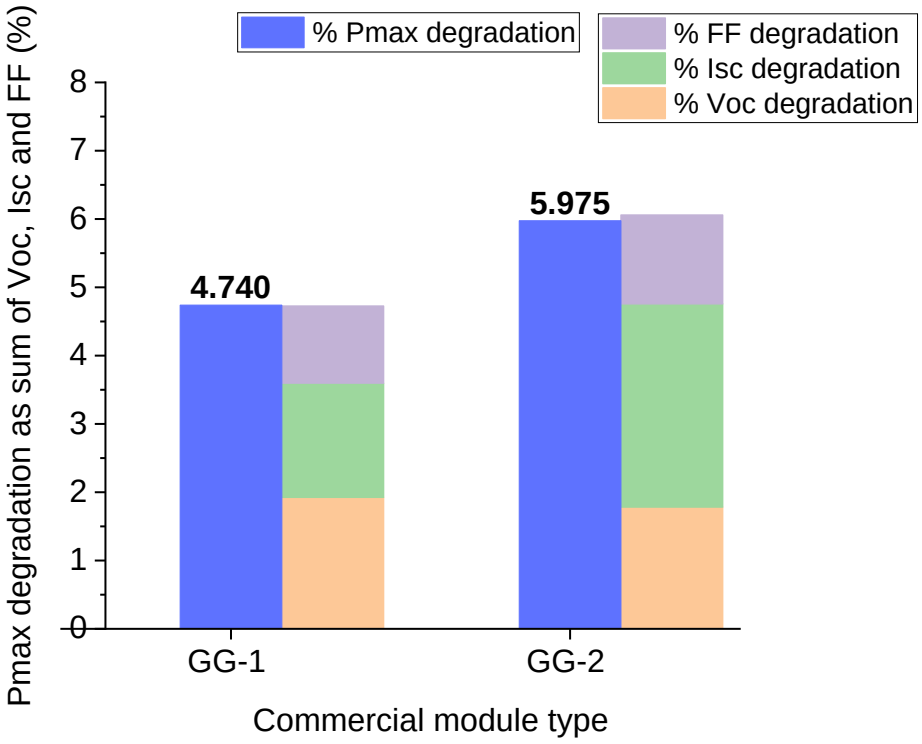

Fig. 52. Degradation in IV parameters after PID stress on DH-stressed modules

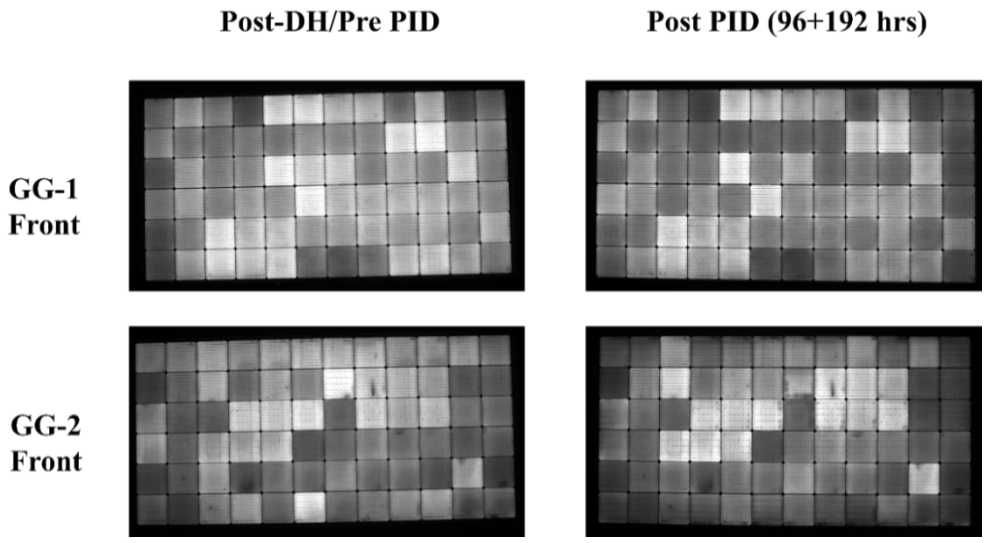

Fig. 53. Pre and post-PID (after DH) EL images at 100% Isc and 60-sec exposure

Table 11. R_{SH} and R_S data pre and post-PID (after DH) for GG modules from dark IV

Module Type	R_{SH} Pre PID/Ω	R_{SH} Post PID/Ω	R_S Pre PID/Ω	R_S Post PID/Ω
GG-1	6783	2453	0.600	0.600
GG-2	6151	4372	0.610	0.624

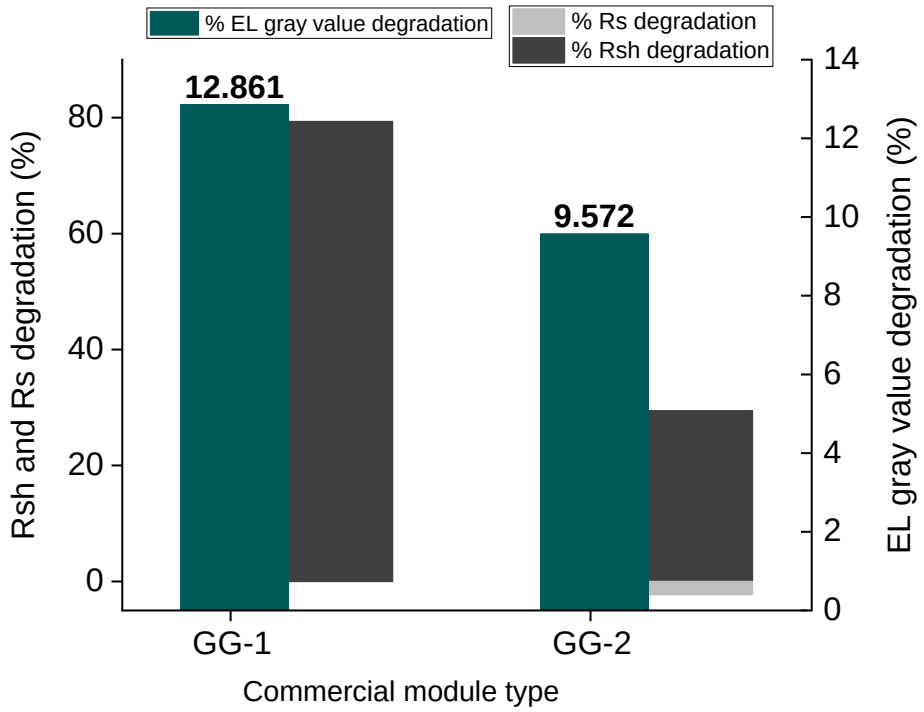

Fig. 54. % EL gray value degradation and % degradation in R_{SH} and R_S because of PID after DH stress

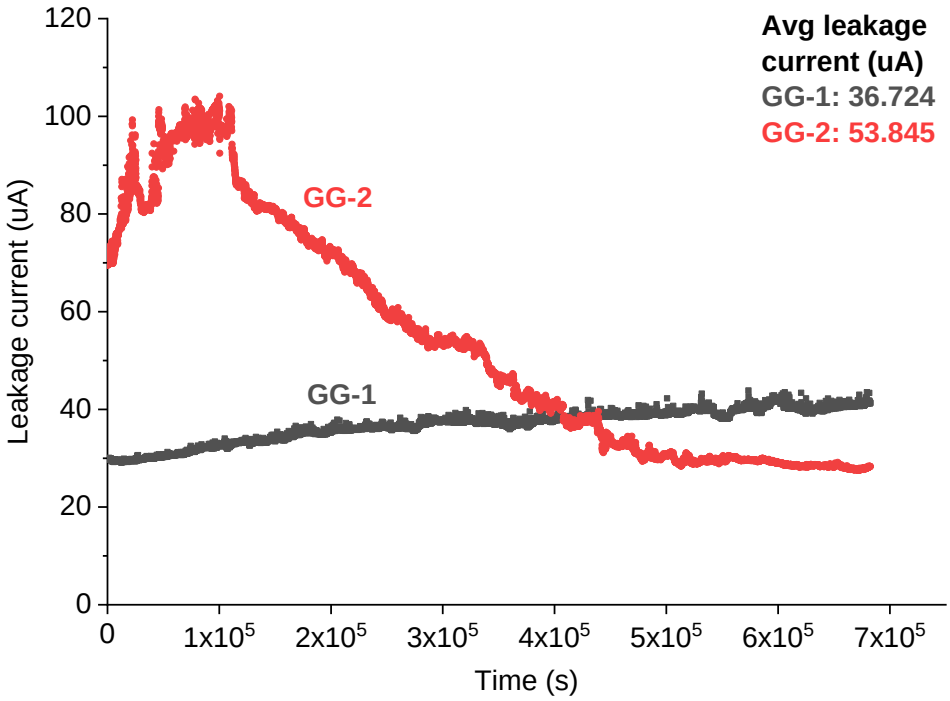

Fig. 55. LC time series plot for 192 hours of PID stress (Post DH)

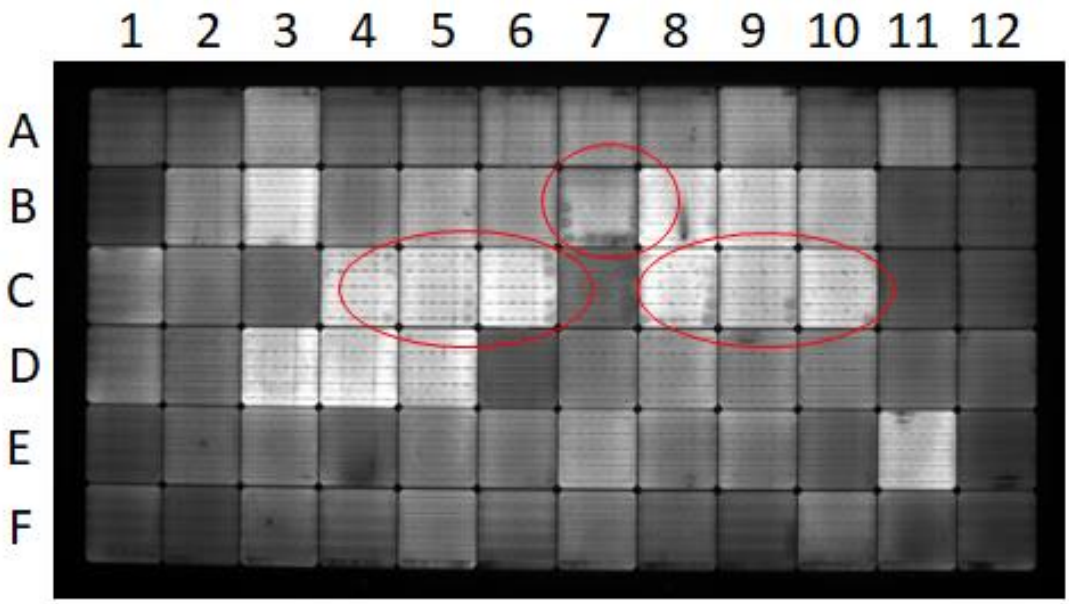

Fig. 56. GG-2 (+ve bias) module labels and circled cells which show degradation

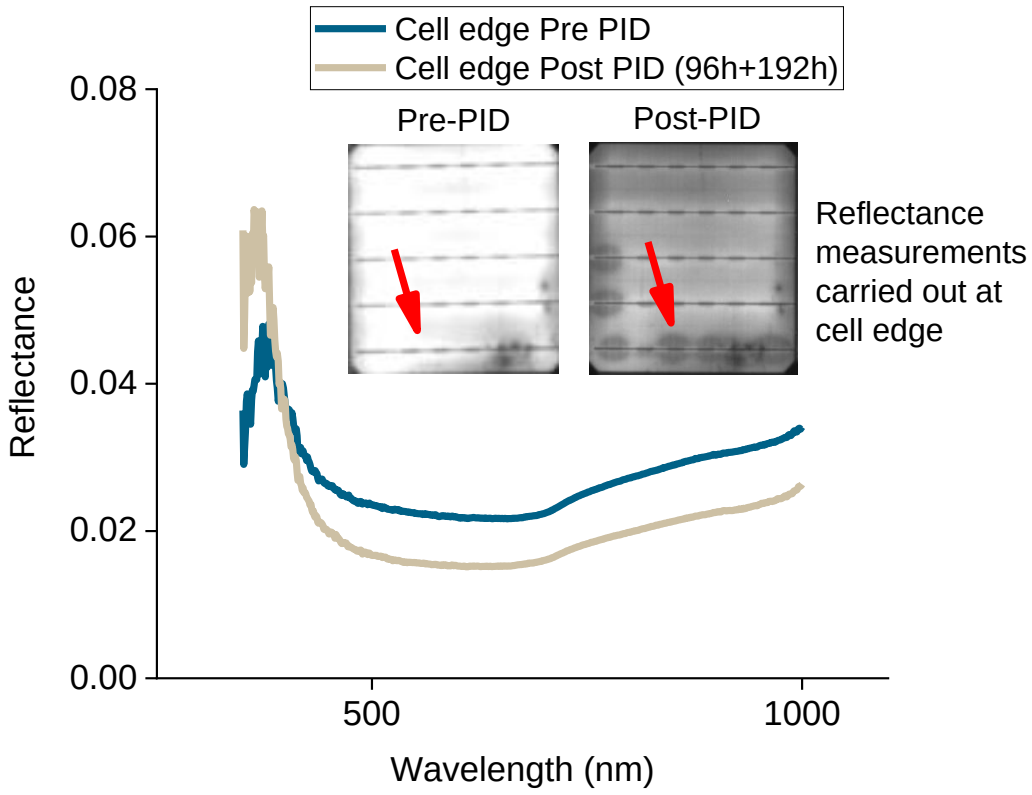

Fig. 57. Red arrows indicate pre and Post PID (after DH) reflectance analysis for the GG-2 module at the edge of cell B7.

The PID data described in this section are for both rounds (96+192 hours), as there was insignificant deterioration in the first 96 hours. The PID following DH stress-related percentage deterioration in Pmax, FF, I_{SC}, and V_{OC} for the GG modules is shown in Fig. 52. These conclusions were reached utilizing outdoor light IV pre and post-PID data (after DH stress). The findings indicate that the Pmax loss for GG-1 under negative bias is 4.7%, and for GG-2 under positive bias is 6%, with a significant contribution from I_{SC}, V_{OC}, and FF. These GG modules seem to be more vulnerable to PID following DH. Although the GG frameless modules were covered with a faux Al frame for PID testing, considering the worst-case scenario for these modules. The EL images for each module pre and post-PID

are shown in Fig. 53. The worsening of the EL gray value because of the PID stress is also seen in Fig. 54. Additionally, Fig. 54 combines the findings from dark IV. It displays the percentage of R_{SH} and R_S deterioration for the GG modules. Table 11 displays the pre- and post-PID data for R_{SH} and R_S. The findings imply that GG-1 has a considerable reduction in R_{SH}, which accounts for the darker cell regions in the EL. The EL is less black due to a rise in R_S and a minor decrease in R_{SH} for GG-2. This assertion is supported by the decline of the % EL gray value. Fig. 55 displays the time series plot of the LC for each module. The graph shows that GG-2 has a larger average LC over the 192 hours of PID stress. The GG-2 module displays tiny circular structures/spots at cell locations B-7, C4-6, and C8-9 after DH and PID stress, as seen in Fig. 56. Fig. 57 shows the pattern changes between pre- and post-PID measurements using a reflectance spectrometer at cell point B-7.

After DH stress, the GG modules exhibit strong PID susceptibility for both polarities. When there is a negative bias, PID-s is driven mainly by the flow of Na^+ ions from the glass or the contaminated cell towards the silicon lattice, where it can diffuse into the PN junction [51], [87], causing a reduction in the module's FF and R_{SH} [197], [198]. For GG-1, a decrease in FF, I_{SC}, V_{OC}, and R_{SH} is the leading cause of power loss. These findings suggest that PID-s and PID-p, two different PID processes, may be active. The loss in FF and R_{SH} is caused by PID-s under the negative bias, as explained earlier, but the loss in I_{SC} and V_{OC} may be ascribed to PID-p [199]. Ions at the Si/passivation interface and Na^+ ions from the glass may move toward the Si_xN_y/Al_xO_y passivation layer due to a negative bias. The field passivation effect of the passivation layer degrades because of this migration of charges [200]. More recombination happens when minority-carrier electrons travel to the surface and recombine with the majority-carrier holes as charges build up in

the Si_xN_y/Al_xO_y stack. As a result, I_{SC} and V_{OC} deteriorate, which aids in the module's loss of Pmax owing to PID-p [199]. The two glass sides of GG modules may increase the amount of Na^+ ions and pollutants accessible for the PID process, leading to a greater sensitivity to PID.

The principal power loss for the GG-2 module is caused by a drop in I_{SC}, V_{OC}, and FF, as well as a minor drop in R_{SH}. Additionally, the GG-2 module has the largest LC and suffers from the most significant Pmax deterioration. Additionally, tiny circular rings or bubbles develop in the GG-2 module due to PID stress after DH, as illustrated in Fig. 56 and 57. The data from the reflectance spectrometer also support a decrease in the reflectance parameter. Kern et al. [49] and a few other researchers explain the process that is taking place. They postulate that PID-c, which may promote interfacial oxidation, delamination, and impurity deposition at the Si/passivation interface, is to blame for this problem in GG modules containing EVA. If there is a positive bias, the Si_xN_y layer may deteriorate because of the moisture buildup and an acidic environment due to EVA. The researchers do not notice PID-c when EVA is switched with POE in corresponding GG modules [49]. Similar results are reported by Brecl et al., and they observe that the positively biased module degrades more rapidly than the negatively biased module. Line corrosion, cell deterioration, and EVA evaporation are the significant causes of the degradation. After 200 hours, the first indications start to show, and after 1000 hours of stress, the corrosion is entirely observable. Additionally, they see bubble-like formations at the front glass, and macro analysis suggests that they may be caused by the development of acetic acid [92]. Additionally, Sinha et al. report similar reductions in electrical parameters, including Pmax, I_{SC}, V_{OC}, and FF, that are equivalent to our results, concluding

that corrosion is the most probable cause [97]. Since the module was only exposed to PID stress for 288 hours in our situation, we are just seeing the early stages of corrosion or delamination in GG-2; as previously stated, complete corrosion is expected to happen after 1000 or more hours of PID. Additionally, most of the research focuses on negative bias degradation. More research is required to thoroughly understand the processes involved since very few studies focus on the degradation mechanisms with a positive bias [169].

GG Modules- Combined results for DH and PID:

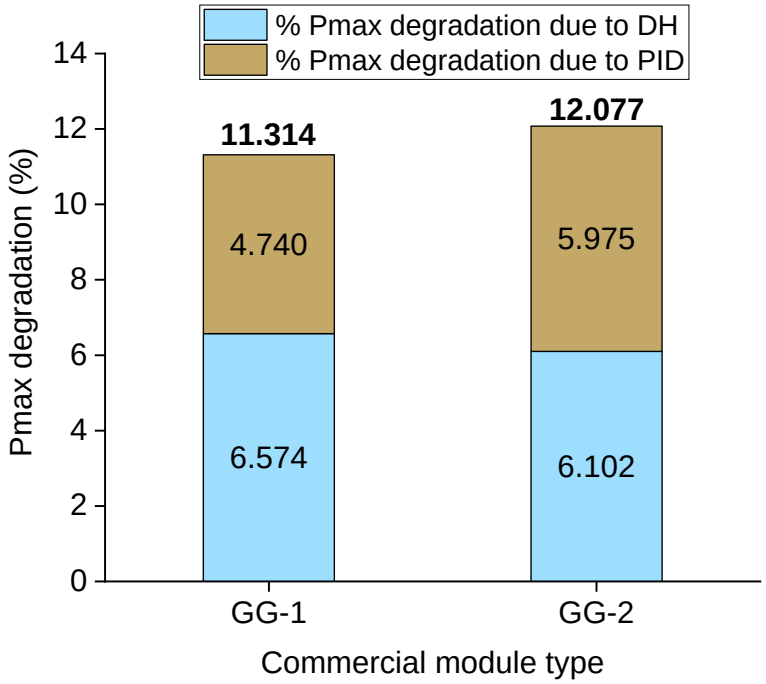

Fig. 58. % Pmax degradation due to DH and PID (after DH) in both GG modules

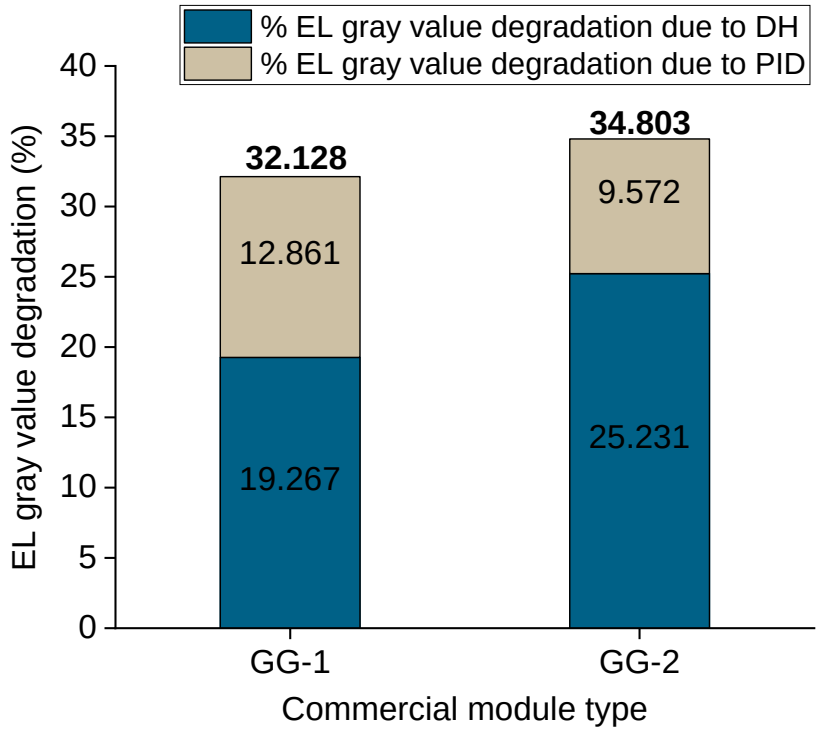

Fig. 59. % EL gray value degradation due to DH and PID (after DH) in both GG modules

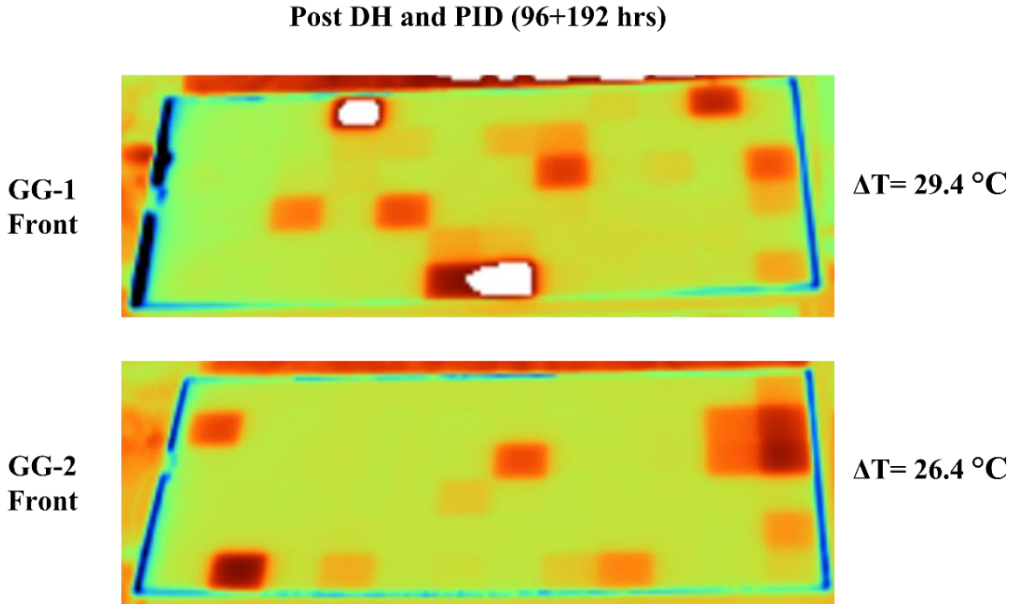

Fig. 60. Outdoor IR images under short circuit for both GG modules after sequential DH and PID

The percentage of Pmax deterioration by sequential DH and PID is shown in Fig. 58 for both GG modules. Similarly, Fig. 59 illustrates the percent deterioration in EL gray value caused by serial DH and PID. After serial DH and PID, the GG modules declined by 11–12% in Pmax. Several PID processes, such as PID-s, PID-p, and PID-c, can occur as the interfacial bonds deteriorate. As can be observed from the study's findings, employing solely new modules cannot provide a comprehensive picture of module dependability for PID since interfacial adhesion strengths might degrade in the field after 10 to 12 years. As shown in Fig. 60, IR images for GG modules were captured under short-circuit settings on a bright day with irradiation of 1062 W/m^2 and an ambient temperature of 23.5°C. The temperature data was collected using Fluke SmartView® IR analysis software, and the delta temperature was computed using equation 4.

$$\Delta T = Max\ module\ temp - Avg\ module\ temp \qquad 4$$

The IR images were only taken after DH and PID stress, and the ΔT is compared with the control module data, which was unstressed throughout the study. After DH and PID, there is a greater ΔT in the GG modules (Fig. 60). This could be because of the dual glass, which retains heat and raises module temperature [50]. Another factor may be the full cell structure, resulting in a more considerable I^2R loss dissipated as heat. Additionally, the problem worsens following DH and PID stress, which is supported by the study of the control module's (unstressed module) measurements, where ΔT for the control GG module is 8.9°C. In contrast, it is between 26 and 29°C for the stressed modules.

This research only examined a statistically small number of modules; hence it is advised that these findings should not be applied to all GG available in the market.

Additionally, since modules come from a specific manufacturer, the company's quality control and the bill of materials may significantly impact the modules' susceptibility to deterioration [169].

GB Modules-DH Stress:

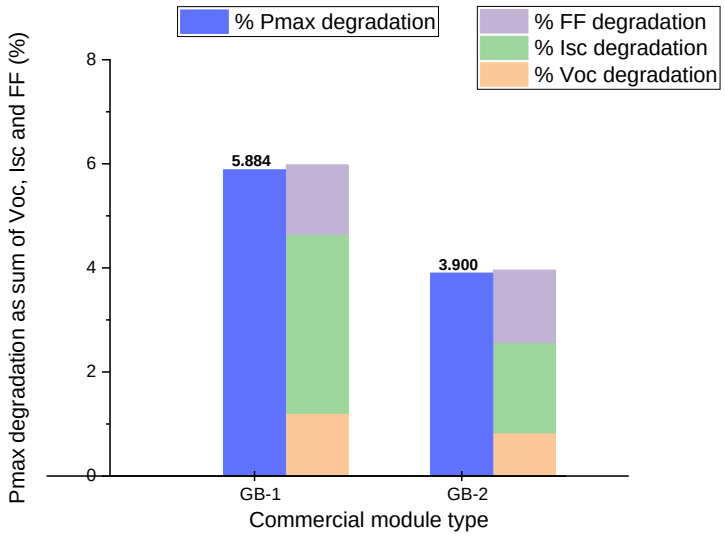

Fig. 61. Degradation in IV parameters after 2000 hours of DH stress

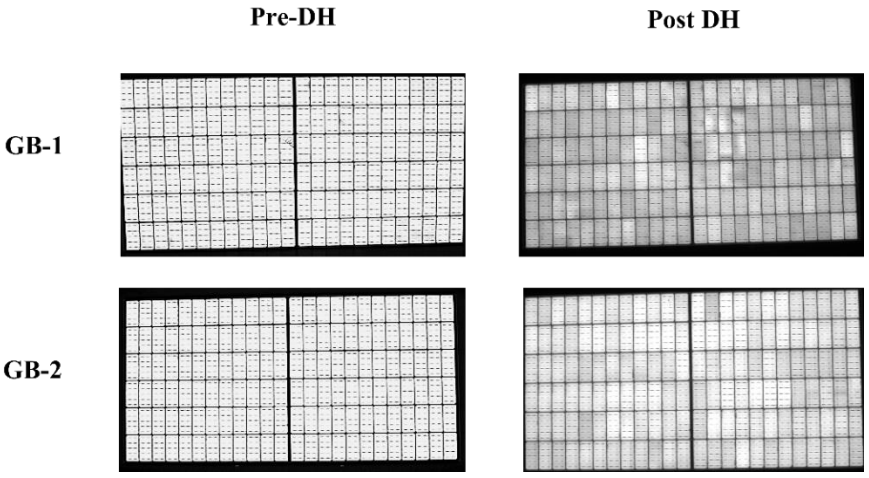

Fig. 62. Pre and post-DH EL images at 100% Isc and 60-sec exposure

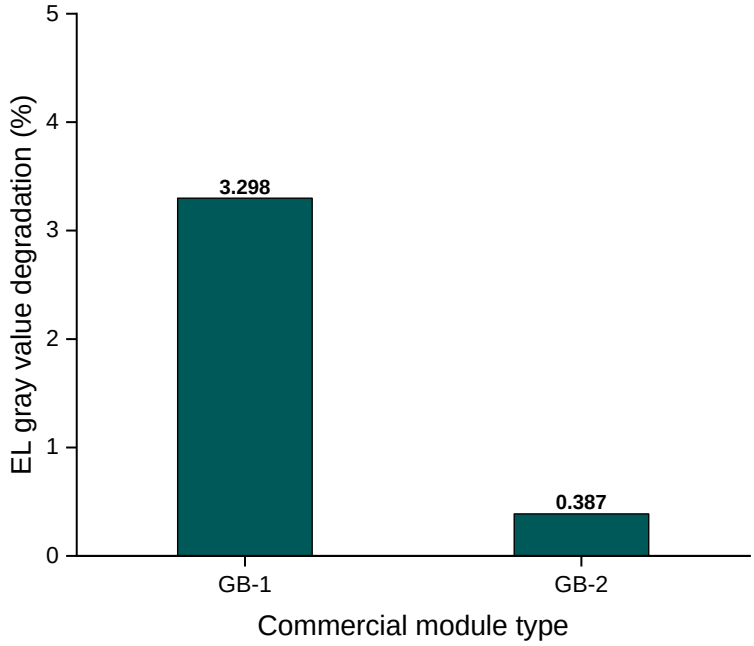

Fig. 63. % EL gray value degradation post-DH stress

The percentage deterioration for GB modules is shown in Fig. 61 for Pmax, FF, I_{SC}, and V_{OC}. Pre- and post-DH outdoor light IV data generated these outcomes. The findings show that DH stress causes GB modules to deteriorate by 4% to 6% in Pmax and 1% to 1.5% in FF. Losses in I_{SC}, $V_{OC,}$ and FF affect the total loss of power (Fig. 61). Fig. 62 displays the EL images taken pre and post-DH stress. Some cell darkening can be seen in the EL images for the GB modules post-DH. The EL gray value deterioration estimated from the pre-and post-EL images is shown in Fig. 63.

During the DH stress, moisture can permeate through the backsheet, leading to deterioration. After DH stress, the acetic acid that EVA produces is the major cause of cell darkening in the GB modules. The grid-contact resistance may be greatly increased by

acetic acid because it can corrode the glass in the space between the silicon cell and the silver paste [169], [192] .

GB Modules-PID after DH Stress: GB-1 is stressed under a negative bias, and GB-2 is stressed under a positive bias for PID.

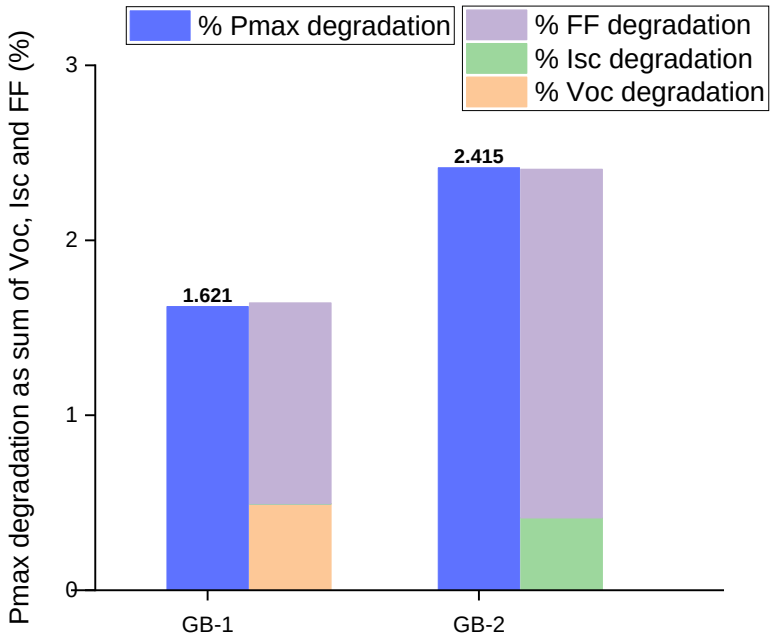

Fig. 64. Degradation in IV parameters after PID stress on DH-stressed modules

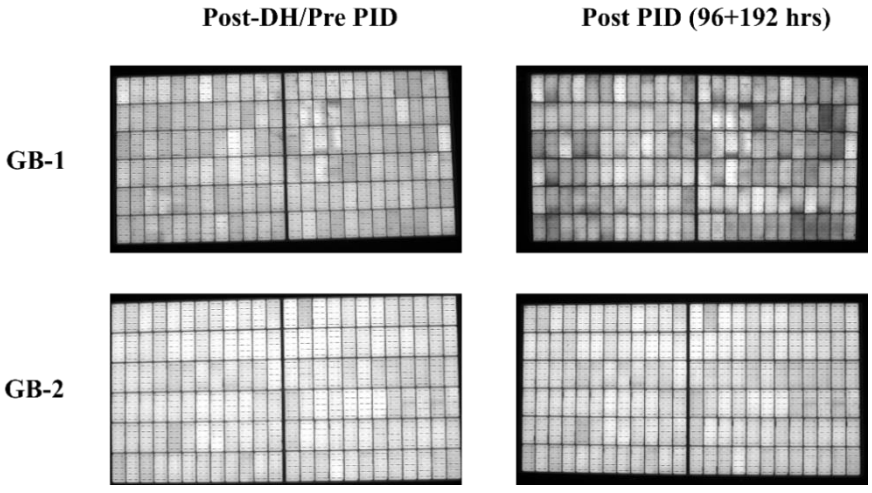

Fig. 65. Pre and post-PID (after DH) EL images at 100% Isc and 60-sec exposure

Table 12. R_{SH} and R_S data pre and post-PID (after DH) for GB modules from dark IV

Module Type	R_{SH} Pre PID/Ω	R_{SH} Post PID/Ω	R_S Pre PID/Ω	R_S Post PID/Ω
GB-1	12029	3316	0.533	0.541
GB-2	5000	5000	0.511	0.528

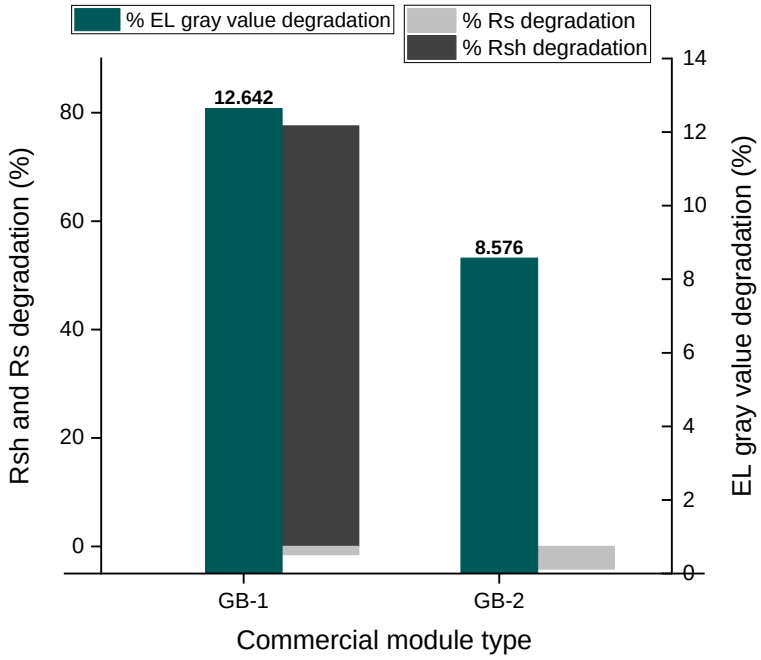

Fig. 66. % EL gray value degradation and % degradation in R_{SH} and R_S because of PID after DH stress

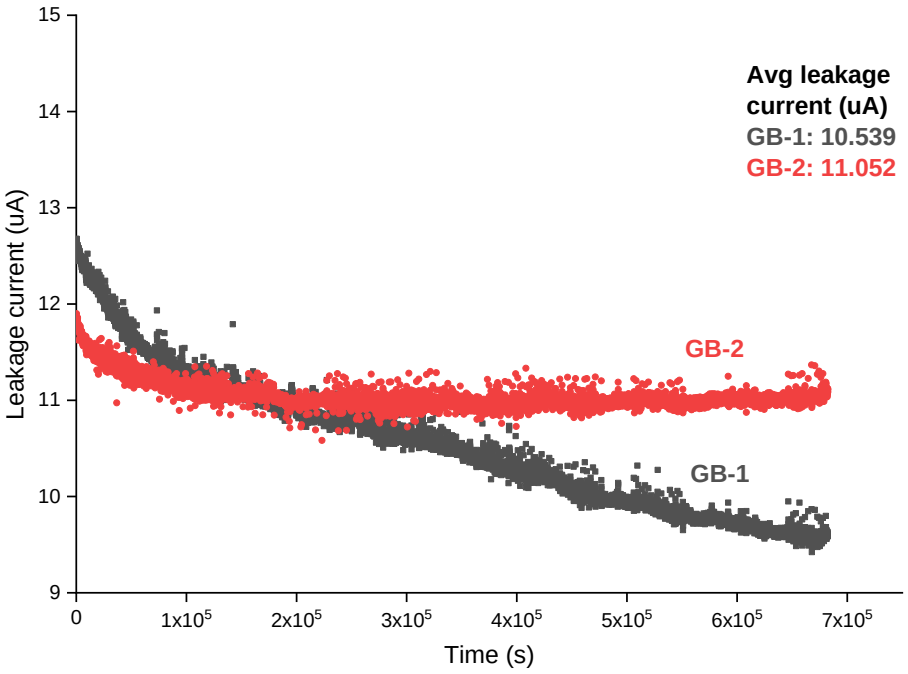

Fig. 67. LC time series plot for 192 hours of PID stress (Post DH)

The PID data described in this section are for both rounds (96+192 hours), as there was negligible deterioration in the first 96 hours. The PID following DH stress-related percentage deterioration in Pmax, FF, I_{SC}, and V_{OC} for the GB modules is shown in Fig. 64. These conclusions were reached utilizing outdoor light IV pre and post-PID data (after DH stress). The findings indicate that the Pmax loss for GB-1 under negative bias is 1.6%, and for GB-2 under positive bias is 2.5%, with a large contribution from FF. The EL images for each module pre and post-PID are shown in Fig. 65. The worsening of the EL gray value because of the PID stress is also seen in Fig. 66. Additionally, Fig. 66 combines the findings from dark IV and displays the percentage of R_{SH} and R_S deterioration for the GB modules. Table 12 displays the pre- and post-PID data for R_{SH} and R_S. The findings imply

that GB-1 has a considerable reduction in R_{SH}, which accounts for the darker cell regions in the EL. The EL is less black due to a rise in R_S and no change in R_{SH} for GB-2. This assertion is supported by the decline of the % EL gray value. Fig. 67 displays the time series plot of the LC for each module. The graph shows that both GB modules have a similar LC, with GB-2 having a slightly higher average LC.

According to the results shown in Fig. 64, 65, and 66, the power loss in GB-1 appears to be caused by a reduction in FF and R_{SH} resistance, suggesting a PID-s mechanism, as explained earlier in the GG section.

For GB-2, the main power loss is caused by a drop in FF, which may be connected to an elevated R_S as determined by dark IV measurements. These outcomes support results presented by Kern et al. Under a positive bias, they see a comparable rise in R_S that causes a decline in FF in GB modules. They explain this as the result of electrochemical corrosion of the module's metallization. This is similar to the PID-c of grid fingers causing electrochemical oxidation caused by water penetrating the module and coming in contact with the metallization [49], [92]. The PID-c mechanism is explained in the GG section [169].

GB Modules - Combined results for DH and PID:

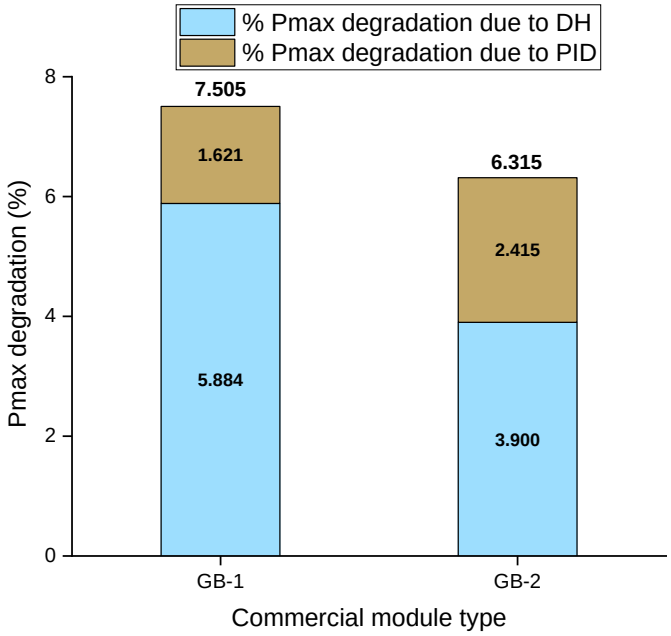

Fig. 68. % Pmax degradation due to DH and PID (after DH) in both GB modules

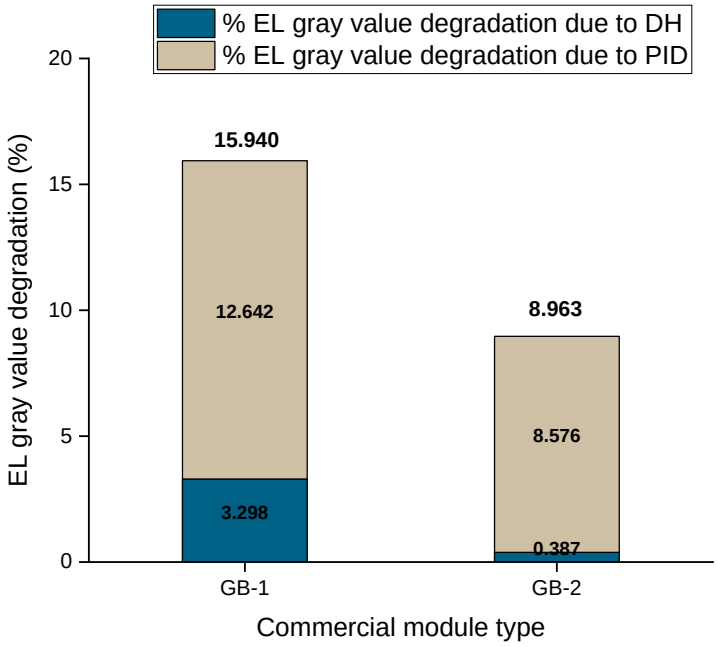

Fig. 69. % EL gray value degradation due to DH and PID (after DH) in both GB modules

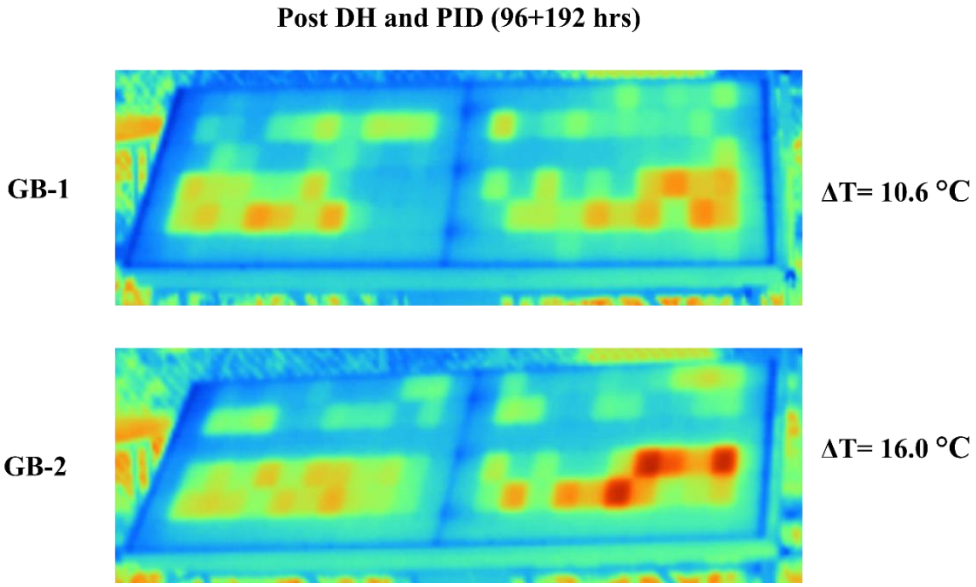

Fig. 70. Outdoor IR images under short circuit for both GB modules after sequential DH and PID

The percentage of Pmax deterioration by sequential DH and PID is shown in Fig. 68 for both GB modules. Similarly, Fig. 69 illustrates the percent deterioration in EL gray

value caused by serial DH and PID. After serial DH and PID, the GB modules declined by 6–7% in Pmax. PID processes such as PID-s and PID-c can occur as the interfacial bonds deteriorate. As shown in Fig. 70, IR images for GB modules were captured under short-circuit settings on a bright day with irradiation of 1062 W/m^2 and an ambient temperature of 23.5°C. The temperature data was collected using Fluke SmartView® IR analysis software, and the delta temperature was computed using equation 4.

The IR images were only taken after DH and PID stress, and the ΔT is compared with the control module data, which was unstressed throughout the study. After DH and PID, there is minimal change ΔT in the GB modules (Fig. 70). The ΔT for the control GB module is 11.8°C, and for GB-1 and GB-2 it is 10.6°C and 16°C respectively. For GB-1, there is no change in ΔT. For GB-2, the slight increase in ΔT can be attributed to the increase in R_S. The change is significantly low, which can be attributed to the backsheet, which allows heat to escape from the module. Also, the half-cell structure leads to lower I^2R losses due to lower current on both module sides.

This research only examined a statistically small number of modules; hence it is advised that these findings should not be applied to all GB available in the market. Additionally, since modules come from a specific manufacturer, the company's quality control and the bill of materials may greatly impact the modules' susceptibility to deterioration [169].

4.3 Impact of PID (focus on PID-p) on Bifacial Modules (Commercial Modules)

The percentage difference between pre and post-characterization tests was calculated using 3.

Round-1 (Cell at -ve bias with stress at rear side): The results for the stressed rear side are presented first, followed by results for the unstressed front side.

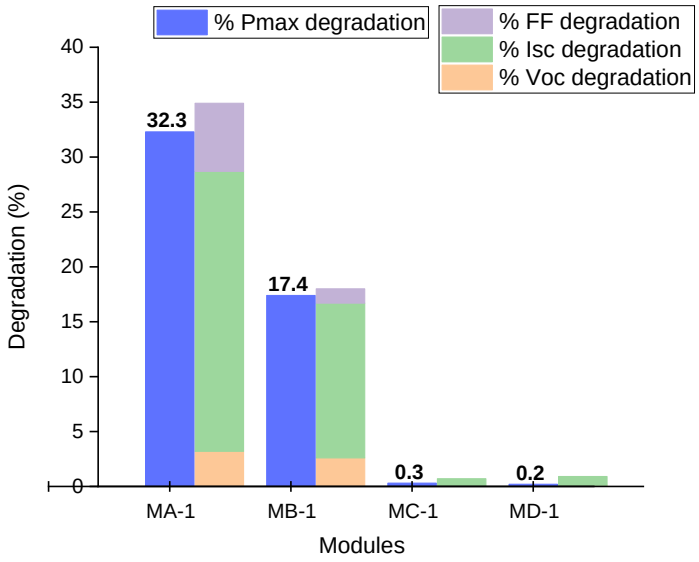

Fig. 71. Degradation in IV parameters for the rear stressed side at 1000 W/m^2

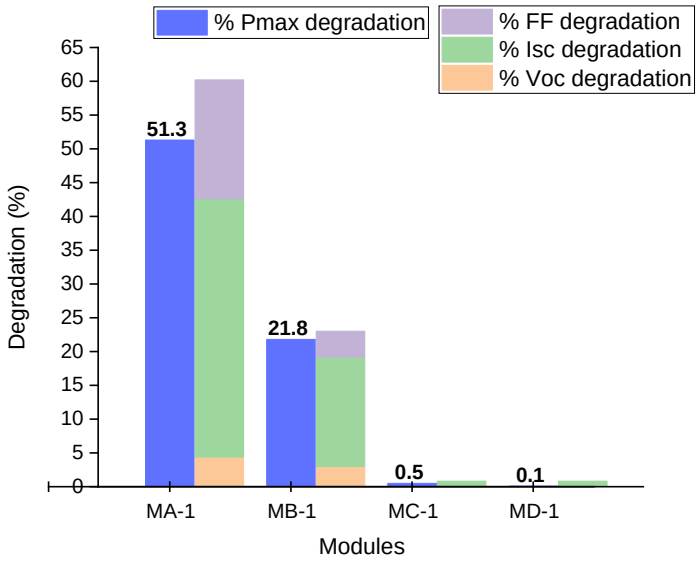

Fig. 72. Degradation in IV parameters for the rear stressed side at 200 W/m^2

Table 13. Percentage change in series and shunt resistance for the rear stressed side measured using Flash IV at low irradiance (200 W/m^2)

Rear side IV at 200 W/m^2	**% change in R_S**	**% change in R_{SH}**
MA-1	+50.9	0
MB-1	+11.7	0
MC-1	0	0
MD-1	0	0

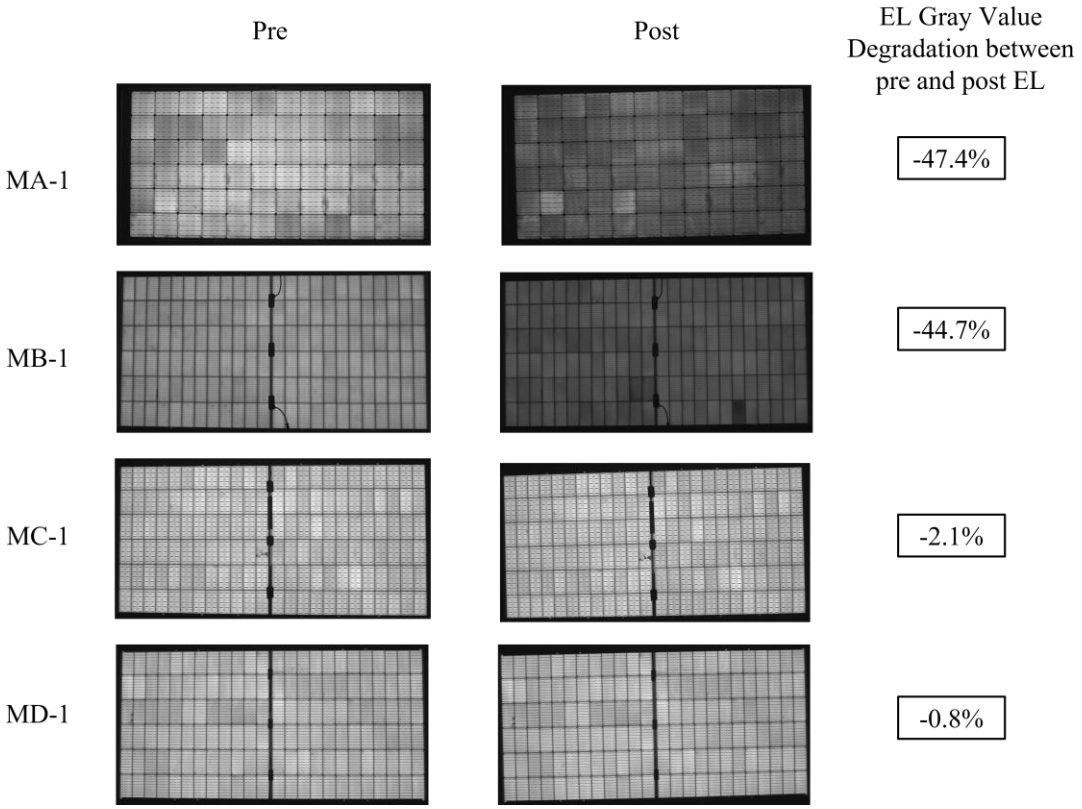

Fig. 73. EL images for the rear stressed side at 100% I_{SC} and 30-sec exposure with gray value change

MA-1 and MB-1 were recovered under sunlight after storage at room temperature and light for 720h.

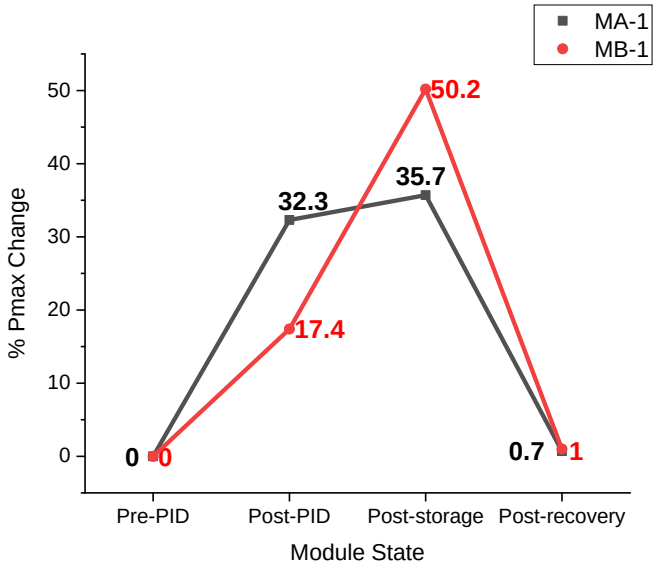

Fig. 74. Pmax change for MA-1 and MB-1 for various states at the stressed rear side at 1000 W/m^2

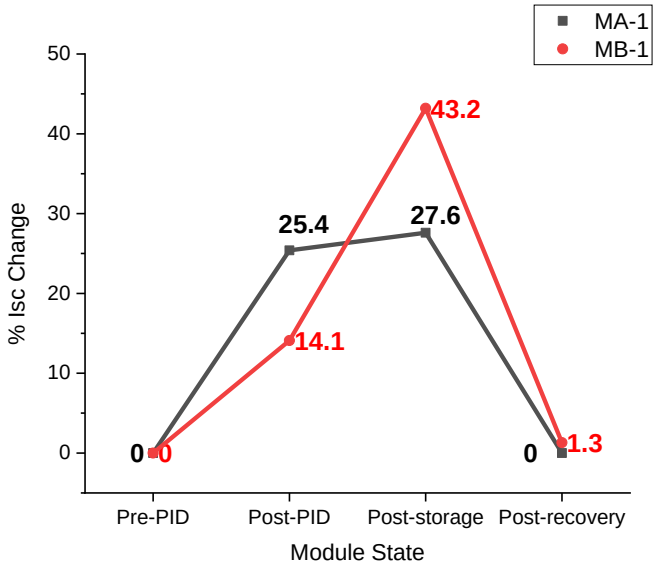

Fig. 75. I_{SC} change for MA-1 and MB-1 for various states at the stressed rear side at 1000 W/m^2

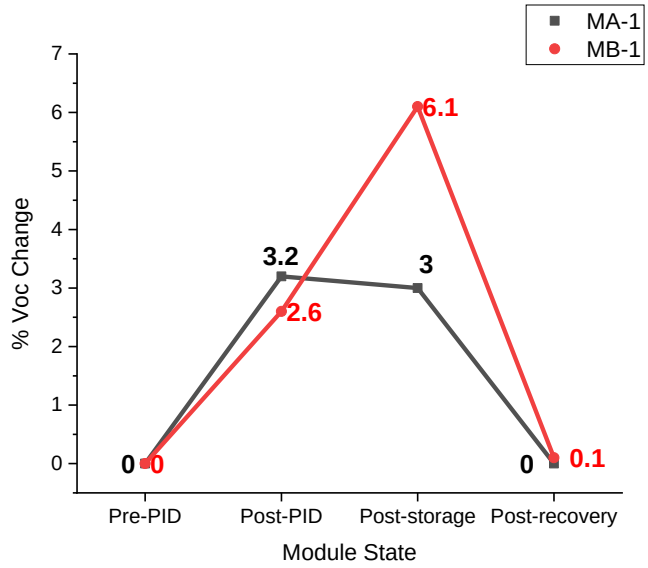

Fig. 76. V_{OC} change for MA-1 and MB-1 for various states at the stressed rear side at 1000 W/m^2

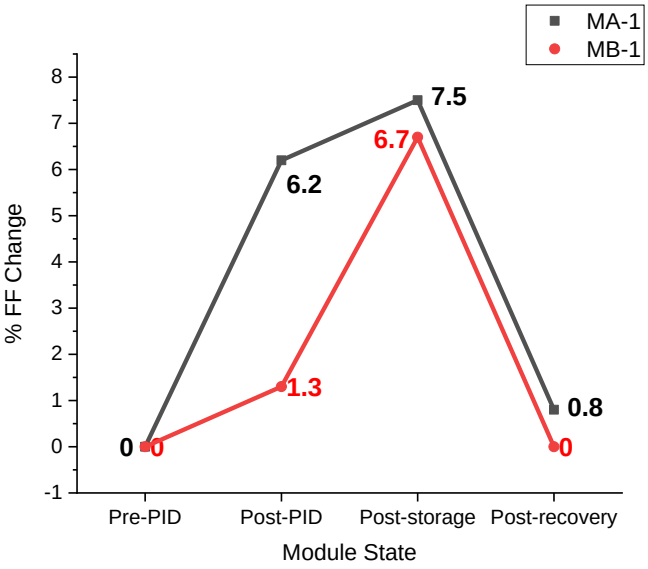

Fig. 77. FF change for MA-1 and MB-1 for various states at the stressed rear side at 1000 W/m^2

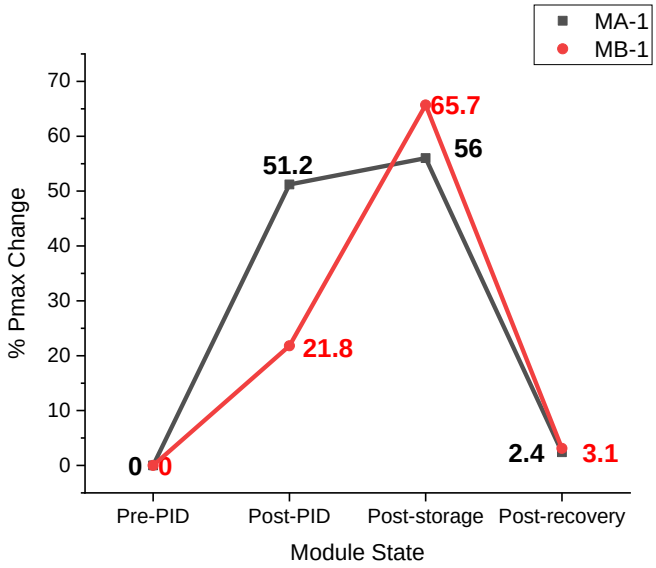

Fig. 78. Pmax change for MA-1 and MB-1 for various states at the stressed rear side at 200 W/m^2

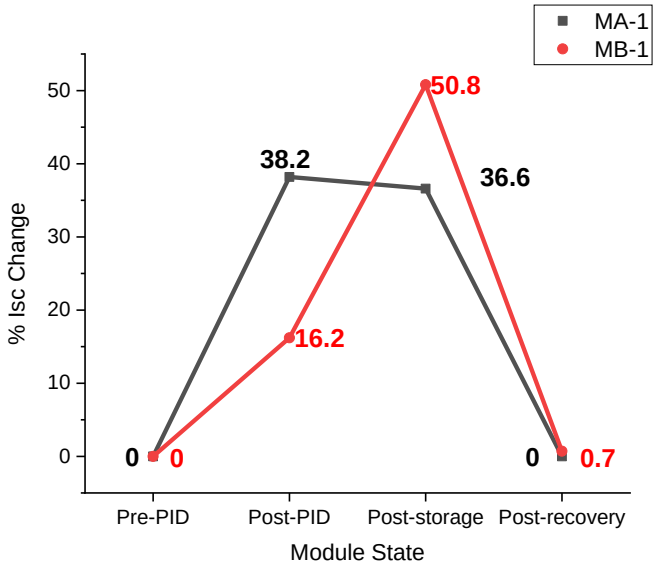

Fig. 79. I_{SC} change for MA-1 and MB-1 for various states at the stressed rear side at 200 W/m^2

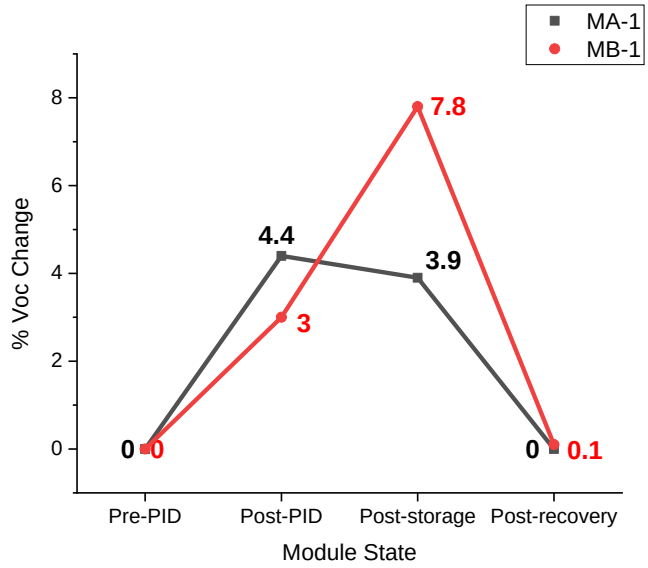

Fig. 80. V_{OC} change for MA-1 and MB-1 for various states at the stressed rear side at 200 W/m^2

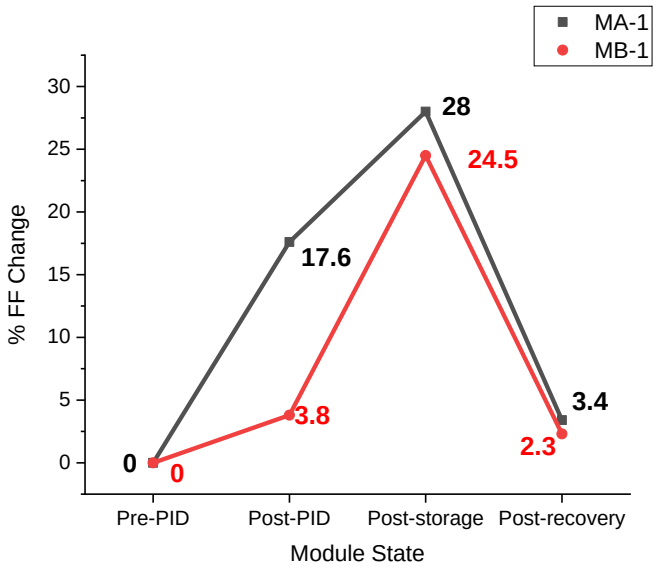

Fig. 81. FF change for MA-1 and MB-1 for various states at the stressed rear side at 200 W/m^2

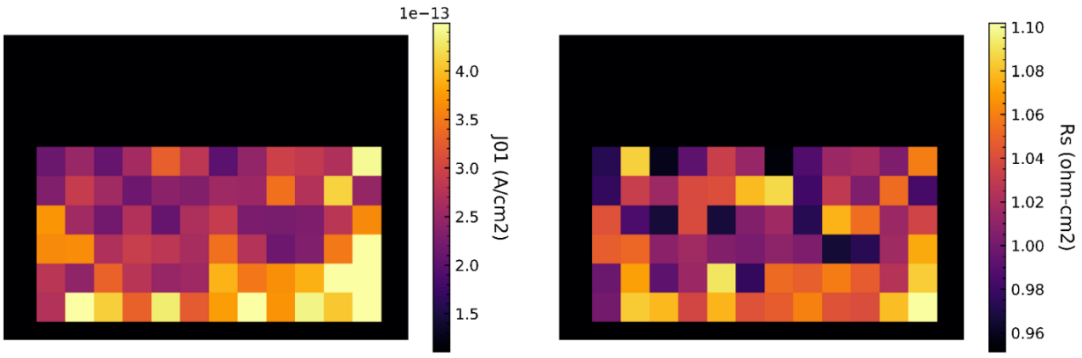

Fig. 82. EL sweep images for the stressed rear side of MA-1 (post storage only)

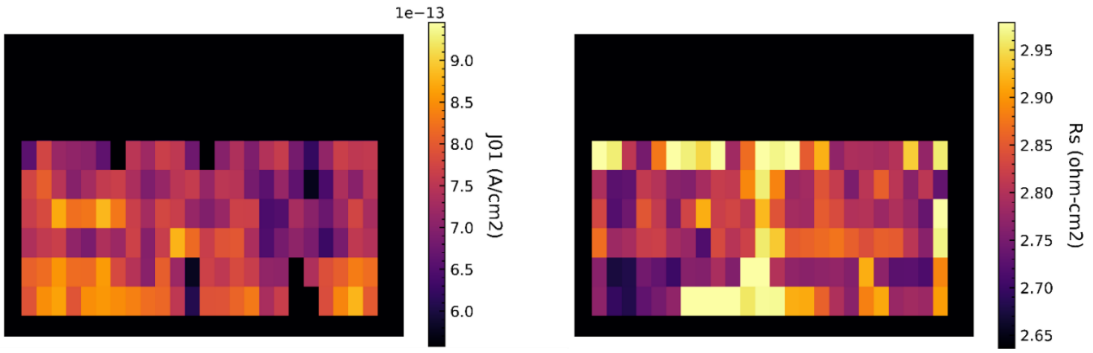

Fig. 83. EL sweep images for the stressed rear side of MB-1 (post storage only)

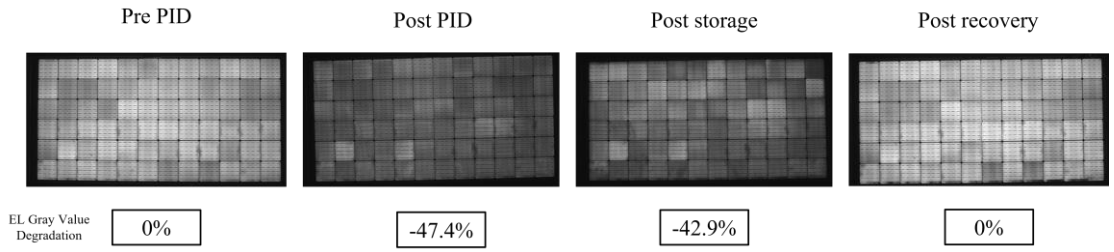

Fig. 84. EL change for MA-1 for various states at the stressed rear side at 100% I_{SC} and 30s exposure with gray value change

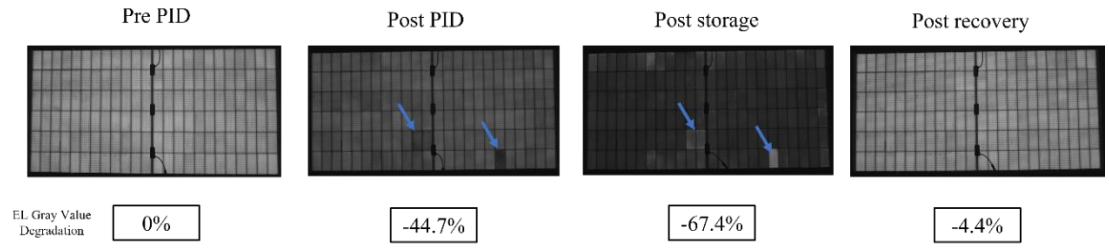

Fig. 85. EL change for MB-1 for various states at the stressed rear side at 100% I_{SC} and 30s exposure with gray value change

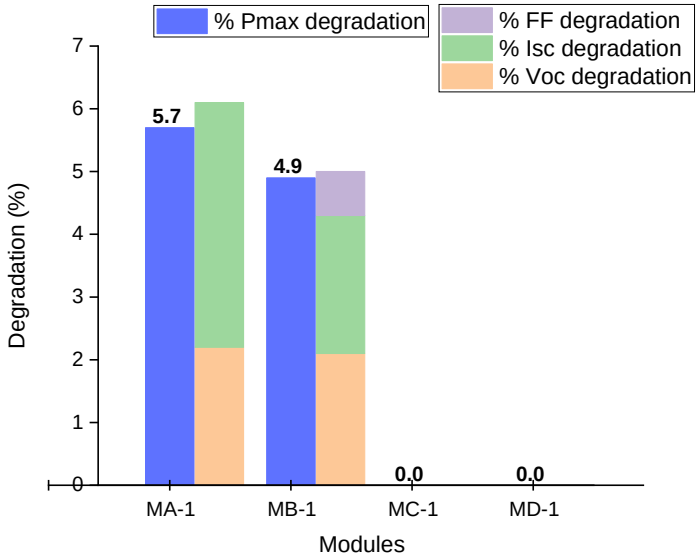

Fig. 86. Degradation in IV parameters for the front unstressed side at 1000 W/m^2

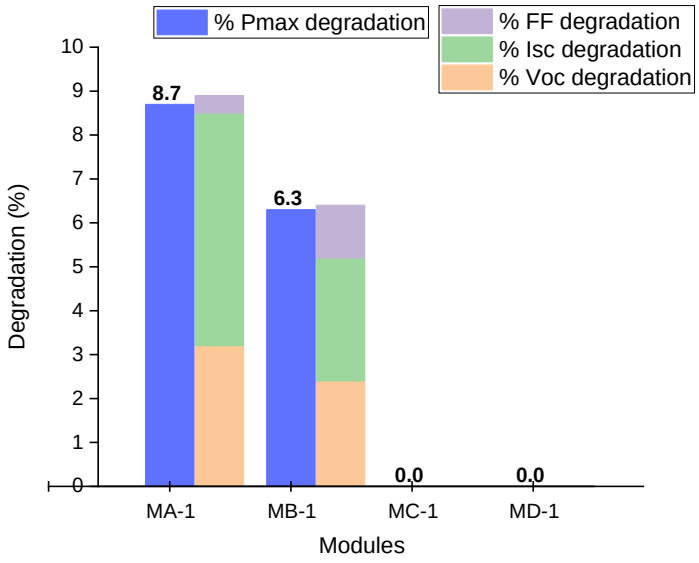

Fig. 87. Degradation in IV parameters for the front unstressed side at 200 W/m^2

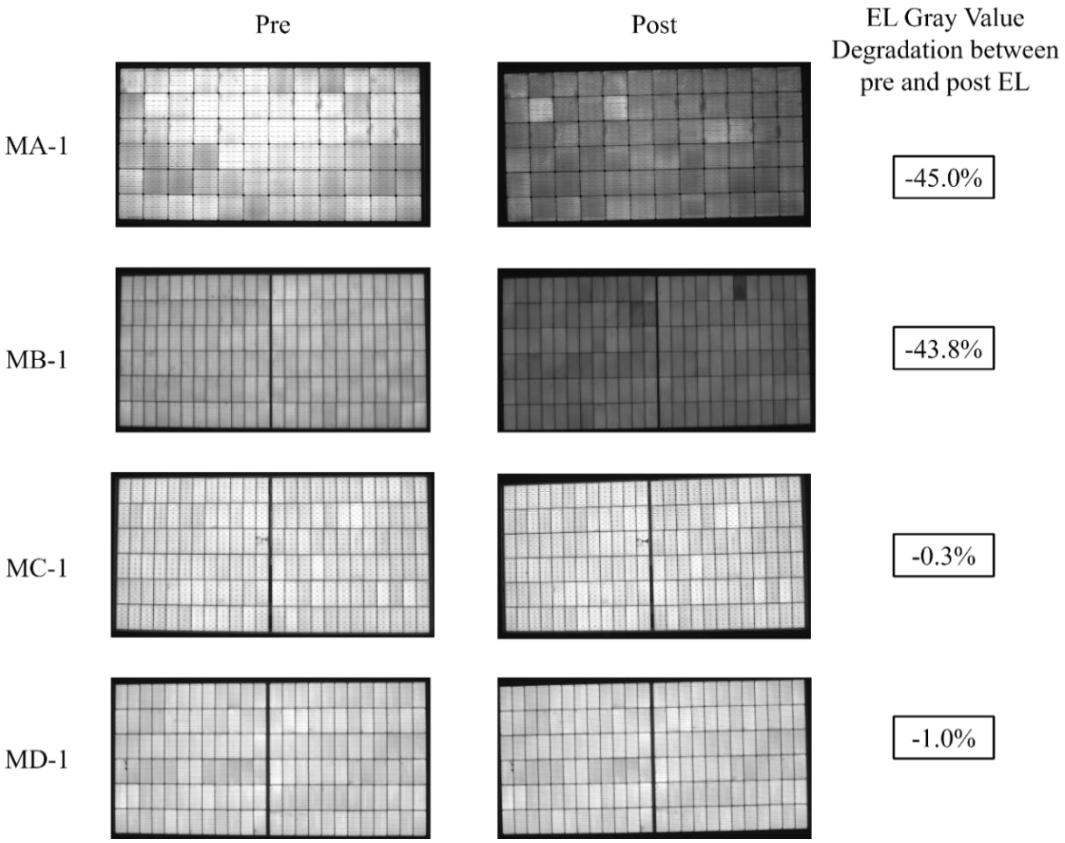

Fig. 88. EL images for the front unstressed side at 100% I_{SC} and 30-sec exposure with gray value change

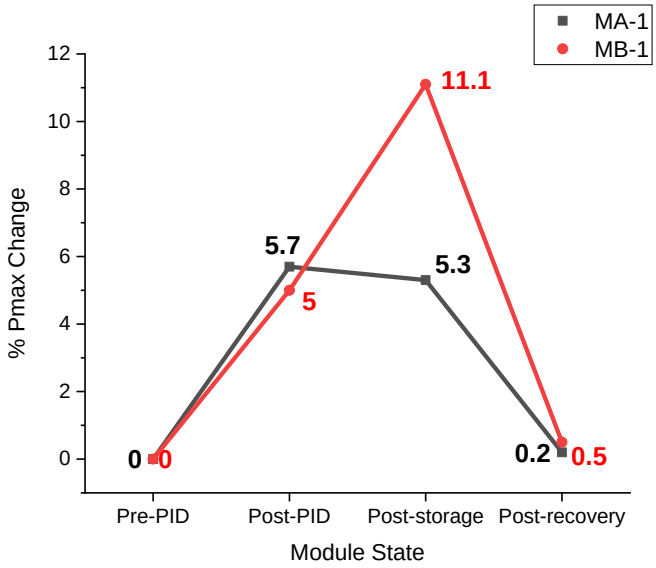

Fig. 89. Pmax change for MA-1 and MB-1 for various states at the unstressed front side at 1000 W/m^2

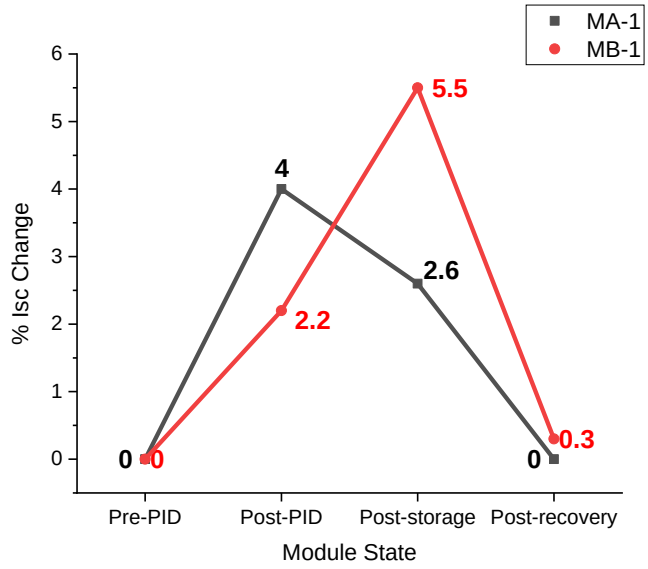

Fig. 90. I_{SC} change for MA-1 and MB-1 for various states at the unstressed front side at 1000 W/m^2

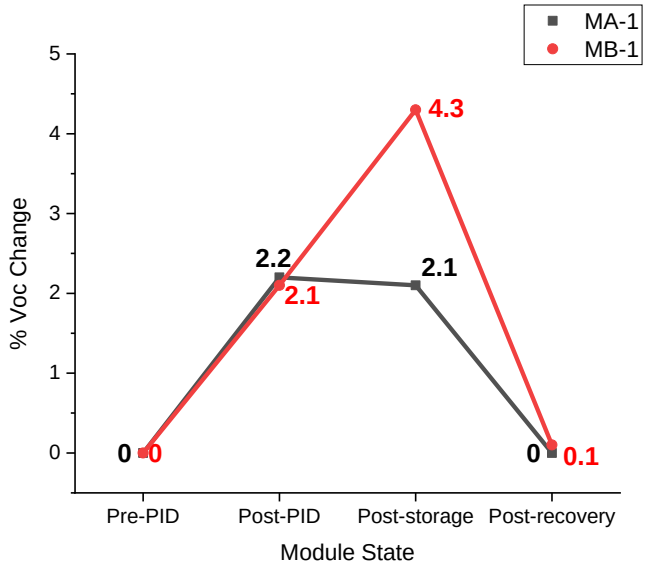

Fig. 91. V_{OC} change for MA-1 and MB-1 for various states at the unstressed front side at 1000 W/m^2

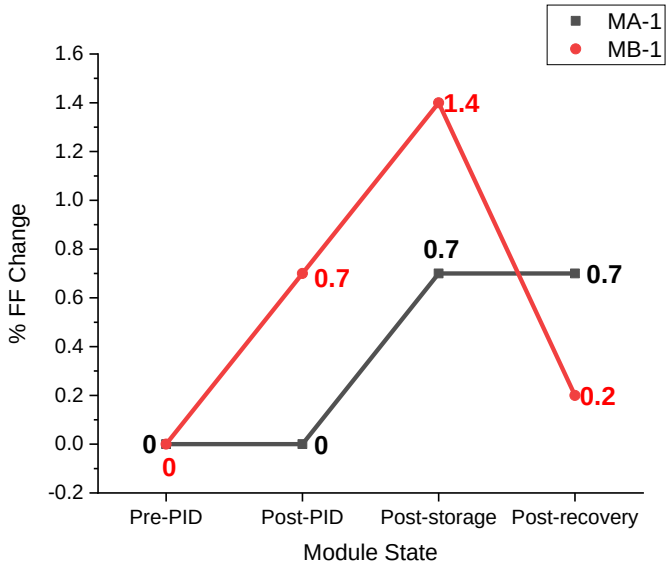

Fig. 92. FF change for MA-1 and MB-1 for various states at the unstressed front side at 1000 W/m^2

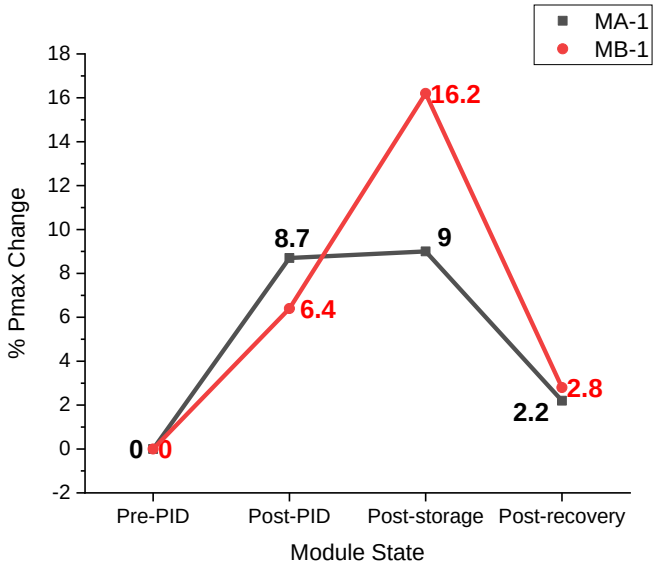

Fig. 93. Pmax change for MA-1 and MB-1 for various states at the unstressed front side at 200 W/m^2

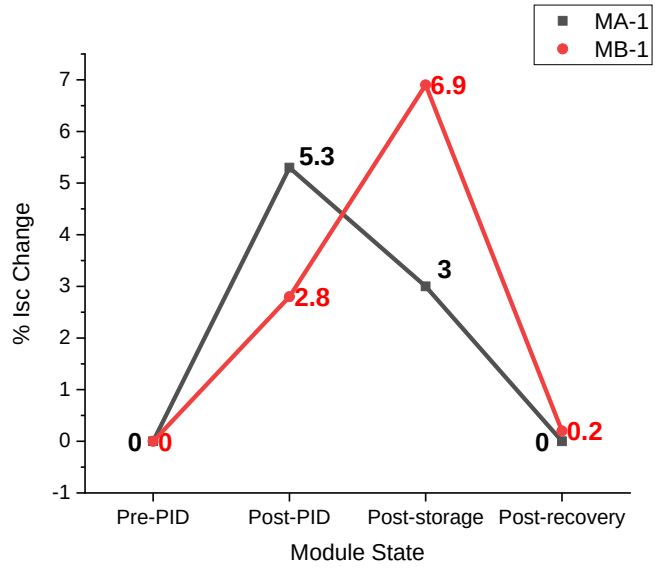

Fig. 94. I_{SC} change for MA-1 and MB-1 for various states at the unstressed front side at 200 W/m^2

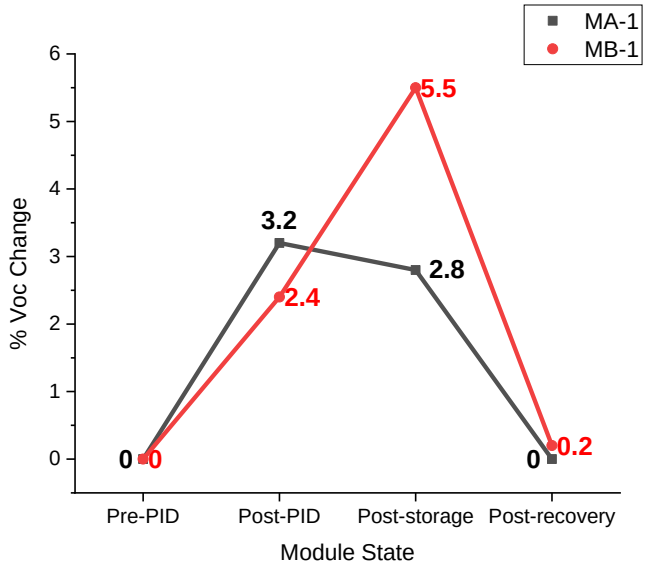

Fig. 95. V_{OC} change for MA-1 and MB-1 for various states at the unstressed front side at 200 W/m^2

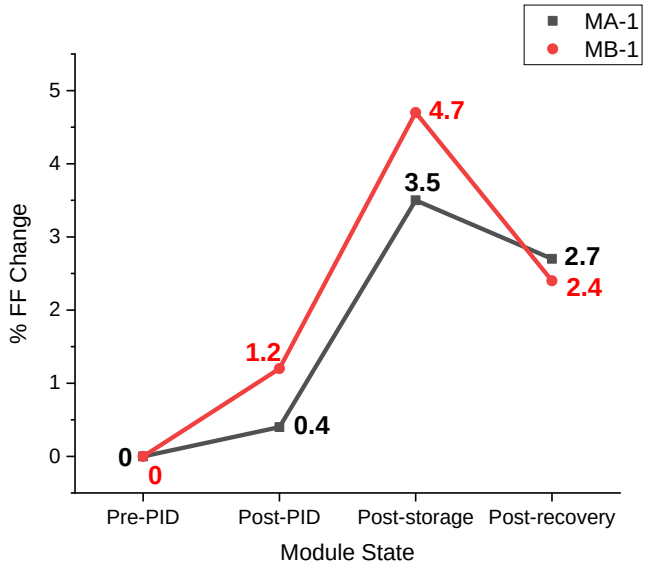

Fig. 96. FF change for MA-1 and MB-1 for various states at the unstressed front side at 200 W/m^2

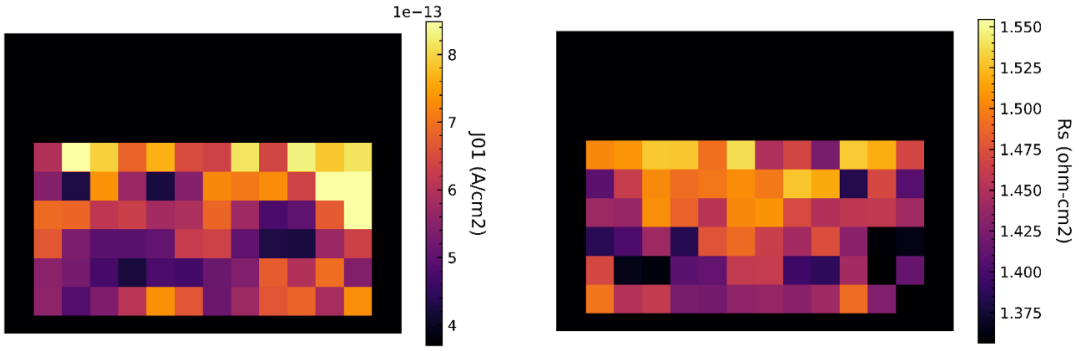

Fig. 97. EL sweep images for the unstressed front side of MA-1 (post-storage only)

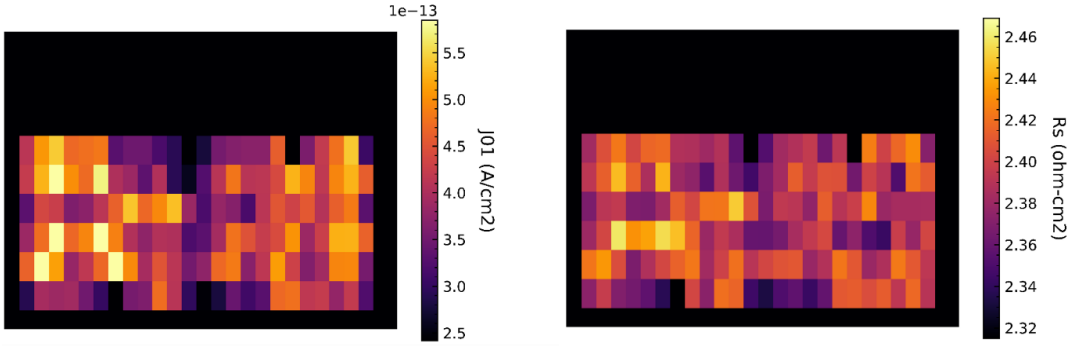

Fig. 98. EL sweep images for the unstressed front side of MB-1 (post-storage only)

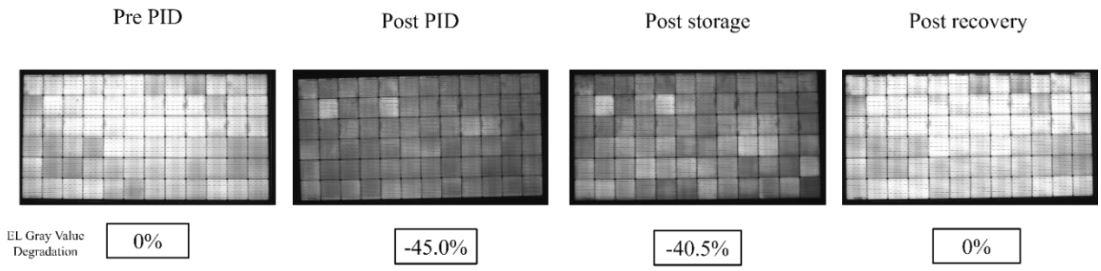

Fig. 99. EL change for MA-1 for various states at the unstressed front side at 100% I_{SC} and 30s exposure with gray value change

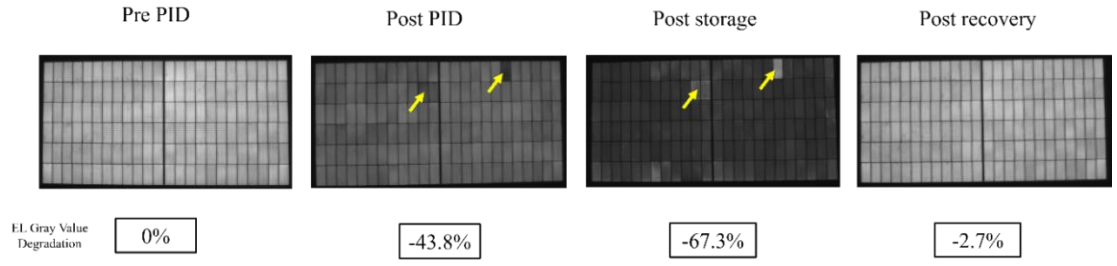

Fig. 100. EL change for MB-1 for various states at the unstressed front side at 100% I_{SC} and 30s exposure with gray value change

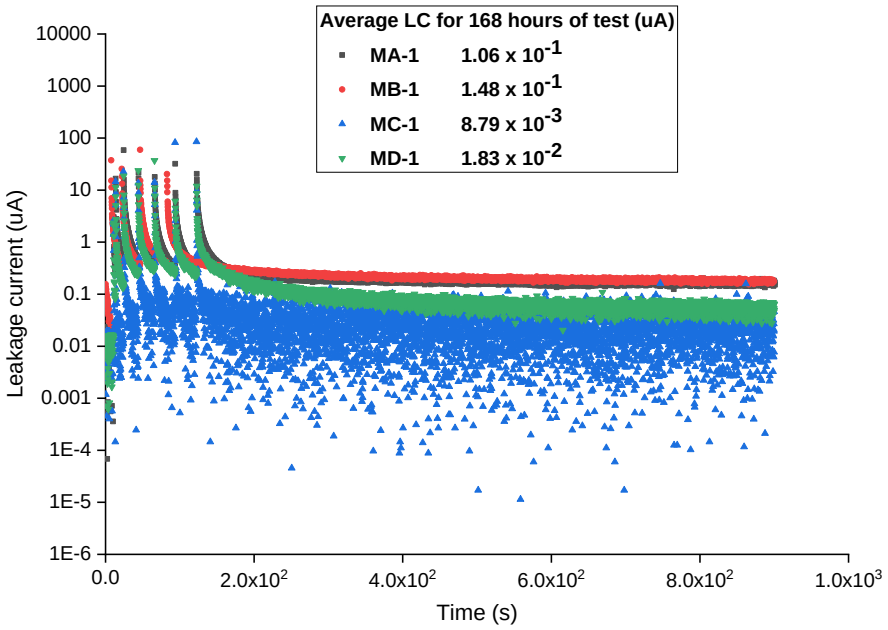

Fig. 101. Average LC data for 168h of stress and log scale LC plots for the first 900s of stress (stabilized after 300s)

The results from round 1, including IV and EL, point to a maximum decrease in Pmax of 32% at STC with a negative bias with the stress at the rear side. While MC-1 and MD-1 decline less than 1% in Pmax, MA-1 and MB-1 have a greater vulnerability to PID. PID-p may be blamed for the decline in both MA-1 and MB-1 since it is known that PID-p causes an increase in Rs and a considerable decrease in I_{SC} and V_{OC}. EL backs up these results. Both MA-1 and MB-1 have high average LCs. A PID-p mechanism is further supported by MA-1 and MB-1's almost full recovery in Pmax. The method is described in [199]. The front of MA-1 and MB-3 also show some decrease in Pmax which can be attributed to the bleeding effect caused due to degradation due to PID stress at the module rear.

Positive charges like Na^+ ions and ionic charges at the silicon-passivation interface (due to contamination) may transfer to the AlO_x/SiN_x layer when the cell is under a negative bias with respect to the rear side. AlO_x offers field effect passivation by repelling minority carrier electrons due to its negative charge density. The AlO_x/SiN_x layer's ability to passivate against field effects is reduced when positive charges are introduced. The majority carrier holes recombine with the minority carrier electrons near the surface as more positive ions accumulate in the AlO_x/SiN_x layer, decreasing the IV parameters [199]. The K-center mechanism (discussed in the literature review section) can also explain the decrease in IV parameters.

The degradations are more pronounced when IV parameters are acquired at a lower irradiance (200W/m2). This is related to the shift in the rear surface recombination injection-level dependency caused by the PID-p progression, which alters the surface charge density of the AlO_x/SiN_x layer [199]. Additionally, in [201], it is shown that for p-type silicon, surface recombination velocity decreases as carrier concertation increases. The amount of fixed charge in the passivation layer further complicates the injection-dependent recombination behavior. As the positive charge density increases, the injection-level dependence of the effective surface recombination velocity changes [201].

PID-p is recovered in the light; however, the rear side of bifacial modules is often at a lower irradiance, which might cause more severe deterioration of the rear of bifacial modules during field operation. This is crucial for PID-p susceptibility in bifacial modules.

Another intriguing outcome is the continued deterioration of the IV characteristics in MB-1 during storage and recovery. Additionally, EL in Fig. 85 demonstrates partial recovery in specific cells (blue arrows). On the other hand, MA-1 exhibits almost the same

levels of deterioration after storage that were detected after PID. The research done in [202] may explain this mechanism. They recommend a PID progression in three stages. Before PID (stage A), Post-PID (stage B), and recovery (stage C). In the case of MA-1, the module has degraded almost completely after PID and is at B; after storage, the condition is midway between B and C; therefore, we see partial recovery. The module state for MB-1 following PID is between A and B, and after storage, most cells shift to B (maximum degradation). However, some cells move to a state between B and C (partial recovery), also known as an inversion layer, as shown by the blue arrows in Fig. 85. Both modules achieve condition C during sunlight recovery [202]. The EL sweep results taken after storage for MA-1 and MB-1 also highlight this information. MA-1 for some cells shows a higher J_{01} and higher R_S, which suggests maximum degradation; for some cells, a lower J_{01} and lower R_S indicates a partial recovery. The same result can be seen for EL sweep images for MB-1. However, flash IV and EL post storage for MA-1 shows that loss in Pmax is less when compared with MB-1 [173].

Round-2 (Cell at +ve bias with stress at the front side): The results for the stressed front side are presented first, followed by results for the unstressed rear side.

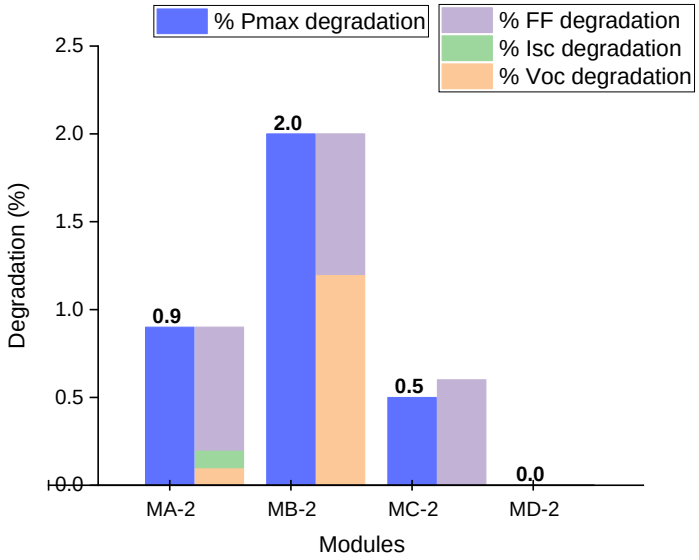

Fig. 102. Degradation in IV parameters for the front stressed side at 1000 W/m^2

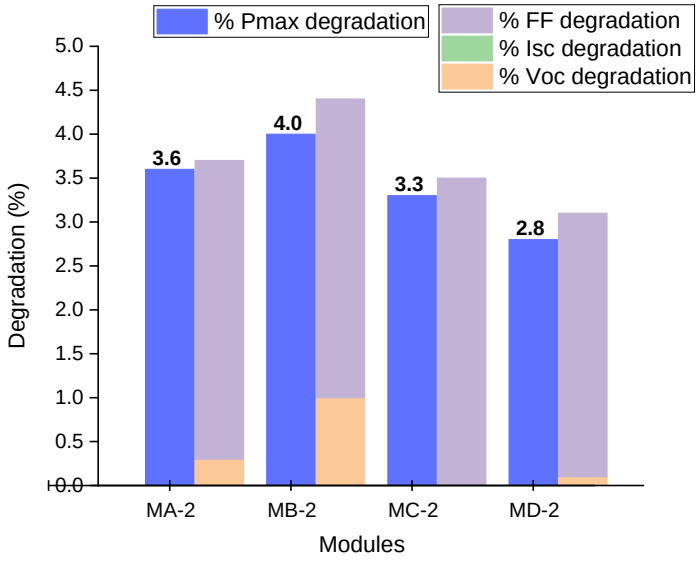

Fig. 103. Degradation in IV parameters for the front stressed side at 200 W/m^2

Table 14. Percentage change in series and shunt resistance for the front stressed side measured using Flash IV at low irradiance (200 W/m^2)

Front side IV at 200 W/m^2	**% change in R_S**	**% change in R_{SH}**
MA-2	+0.8	-15.5
MB-2	0	-14.0
MC-2	+9.2	-20.9

MD-2	0	-20.6

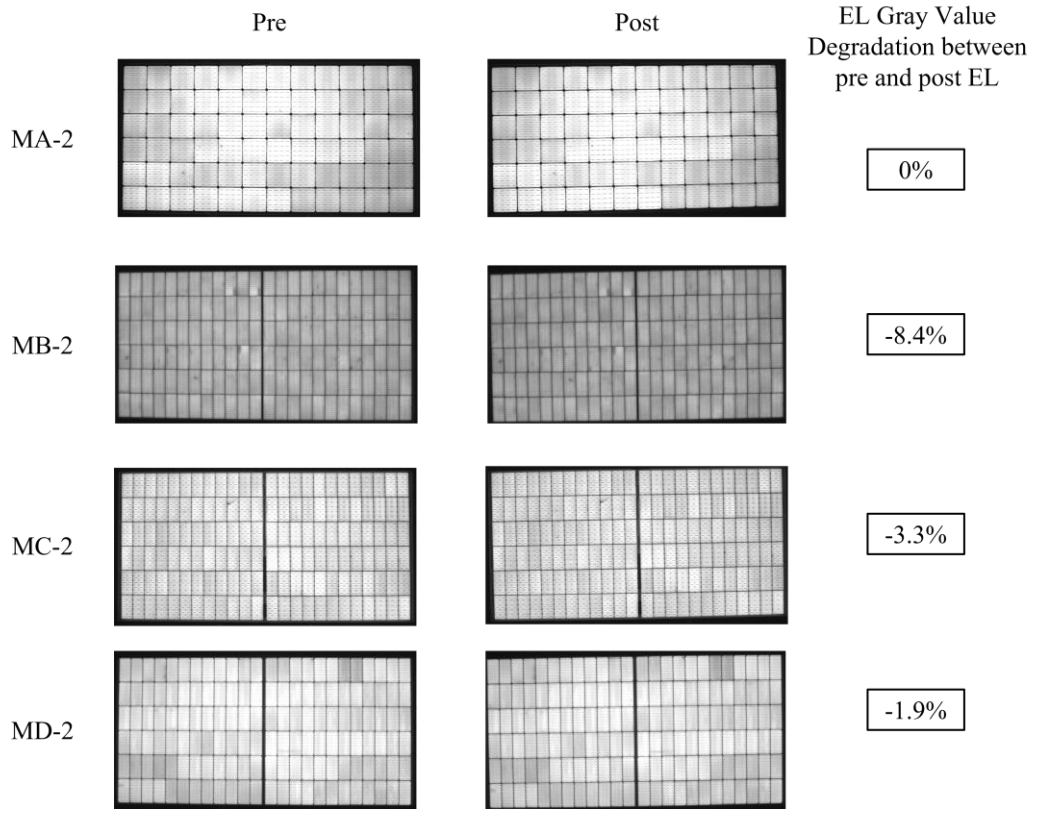

Fig. 104. EL images for the front stressed side at 100% I_{SC} and 30-sec exposure with gray value change

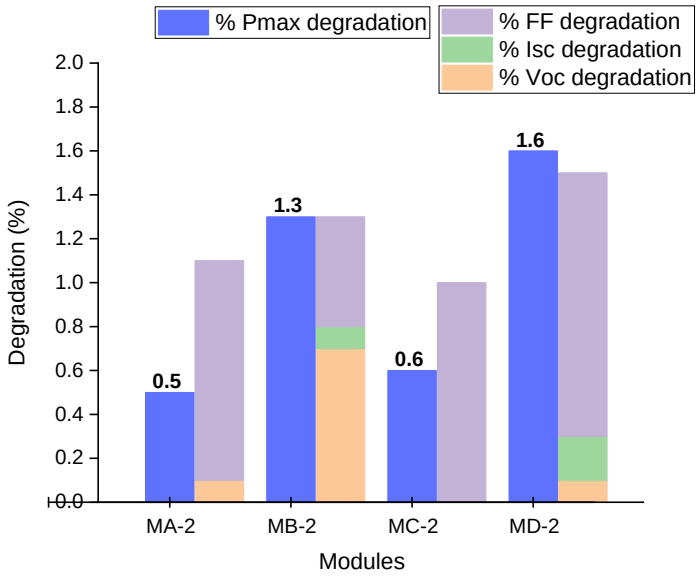

Fig. 105. Degradation in IV parameters for the rear unstressed side at 1000 W/m^2

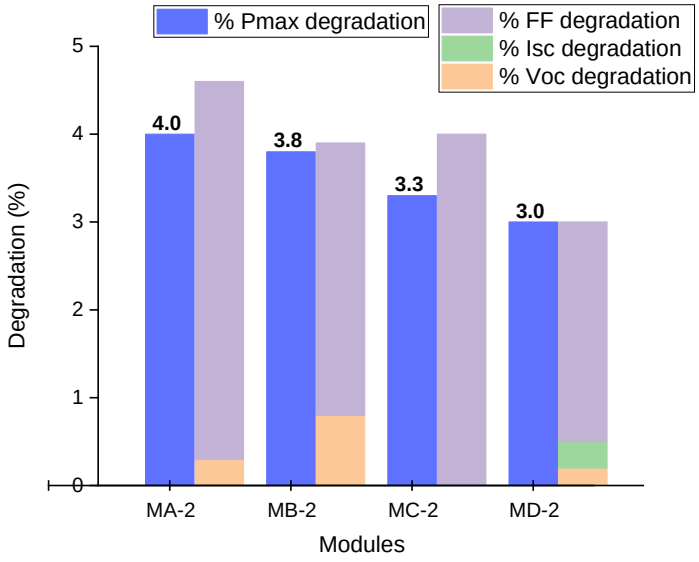

Fig. 106. Degradation in IV parameters for the rear unstressed side at 200 W/m^2

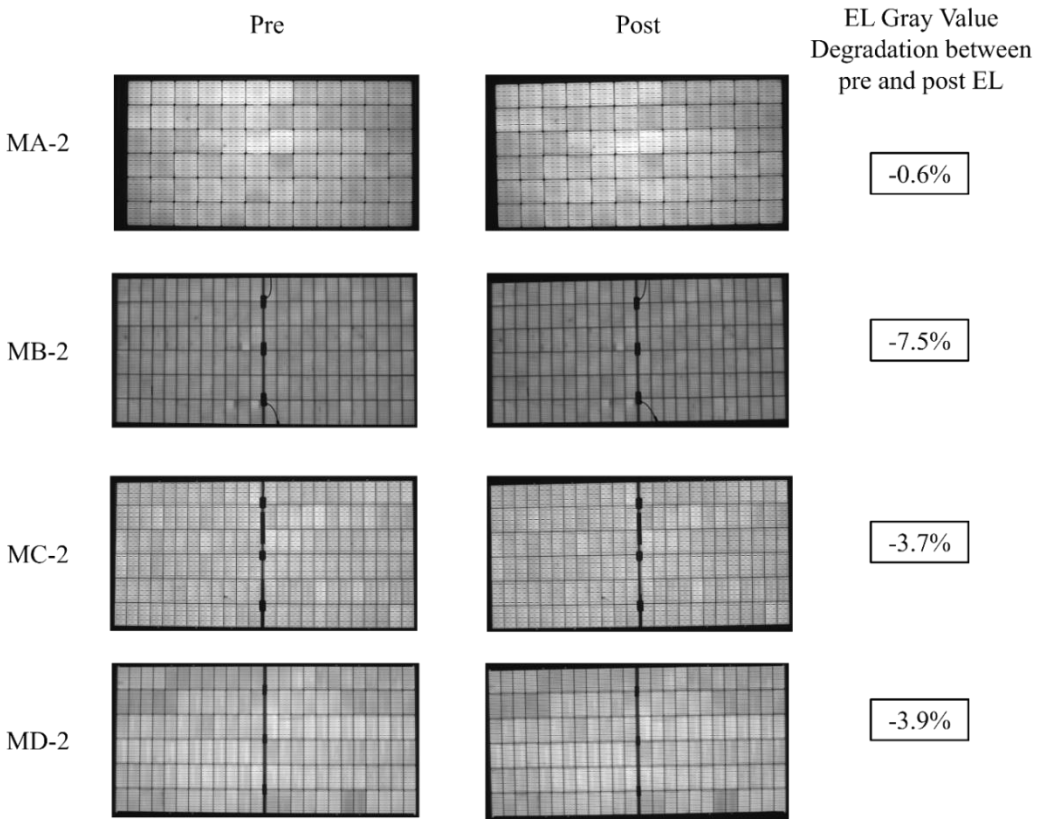

Fig. 107. EL images for the rear unstressed side at 100% I_{SC} and 30-sec exposure with gray value change

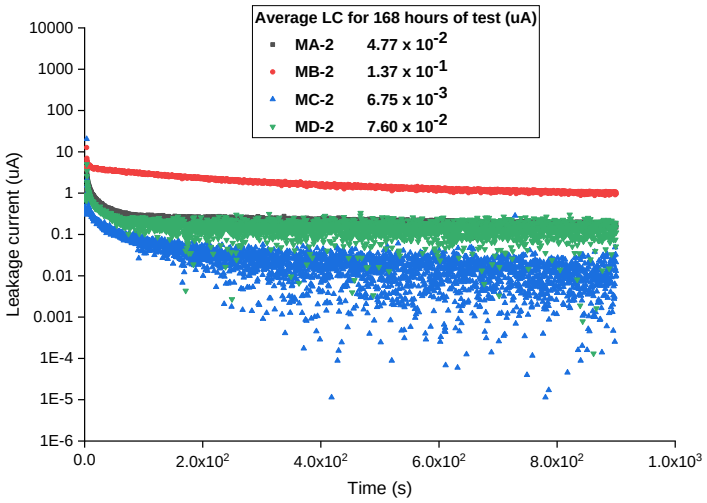

Fig. 108. Average LC data for 168h of stress and log scale LC plots for the first 900s of stress (stabilized after 300s)

Pmax deterioration in round 2 is less than 5% across all modules. These findings are also supported by EL and LC data. We also blame PID-p for the decline in this round. Using data for the conventional backsheet module with bifacial PERC cell (module details are listed in Table. 15) presented below, we can argue that the mechanism causing degradation when the cell at a positive bias with respect to the front side is PID-p, even though significant degradation in I_{SC} is not observed (the results for this module are separated to maintain consistency of module type as all are bifacial modules, but the results are included here to explain the PID mechanism for round-2).

Table 15. Backsheet module with bifacial PERC cell details

Module Name	**Number of Modules**	**Manufacturer**	**Module Construction**	**Cell type and dimensions**
M-E	1	D	Glass-Backsheet (monofacial)	Bifacial PERC-144-Half-cut 78 x156 mm

Table 16. Testing details

Round	**Cell Polarity**	**Stressed side**	**Modules tested**	**Expected PID mechanism according to literature in p-PERC cells (Detail in the literature review section)**
2	Positive (+ve)	Front	ME-1	PID-p

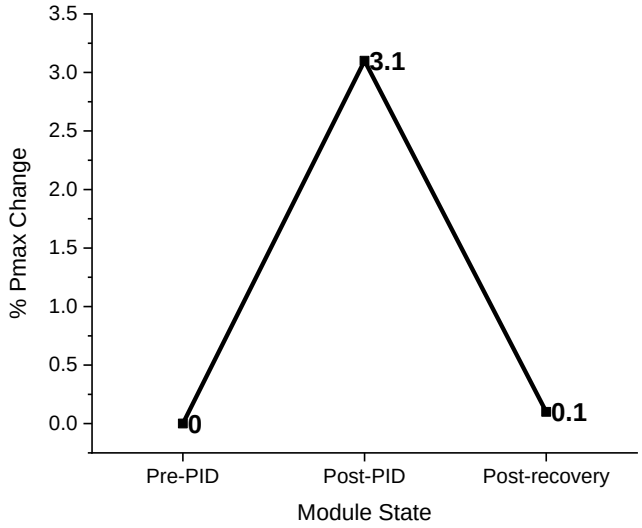

Fig. 109. Pmax change for ME-1 for various states at 1000 W/m^2

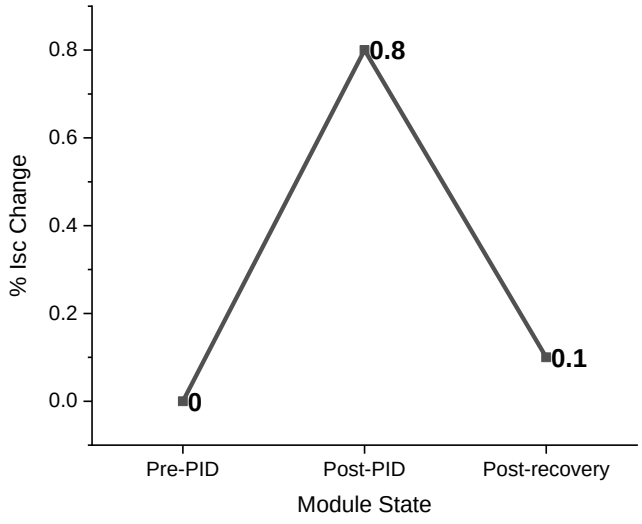

Fig. 110. I_{SC} change for ME-1 for various states at 1000 W/m^2

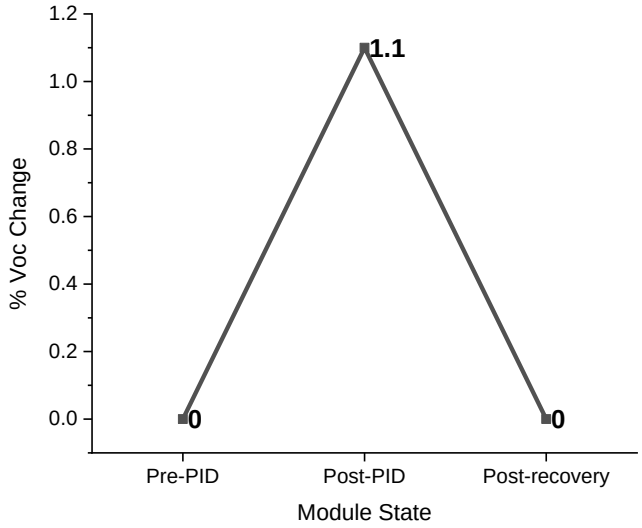

Fig. 111. V_{OC} change for ME-1 for various states at 1000 W/m^2

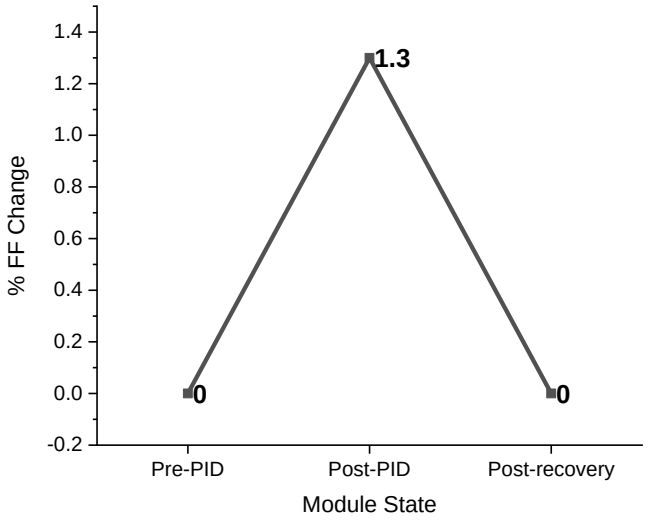

Fig. 112. FF change for ME-1 for various states at 1000 W/m^2

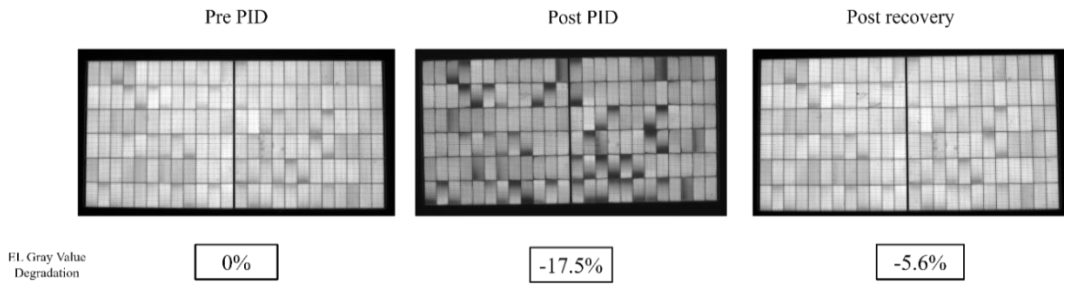

Fig. 113. EL change for ME-1 for various states 100% I_{SC} and 30s exposure with gray value change

Under sunlight, ME-1 recovers nearly entirely. Since the Na^+ ion is involved in PID-s and cannot be forced into the junction at a positive bias, the mechanism cannot be PID-s. Contrarily, PID-c is an irreversible process. Therefore, a PID-p mechanism for round-2 is suggested due to full recovery and positive bias stress [173].

Round-3 (Cell at -ve bias with stress at the front side): MB-1 was employed again in round three after recovery due to module unavailability. For both stressed and unstressed sides (at 1000W/m^2 and 200W/m^2), all other modules (MA-3, MC-3, MD-3) exhibited less than a 1% drop in Pmax, suggesting no degradation. For MB-1, both the stressed and non-stressed sides are considered since the unstressed side shows higher deterioration.

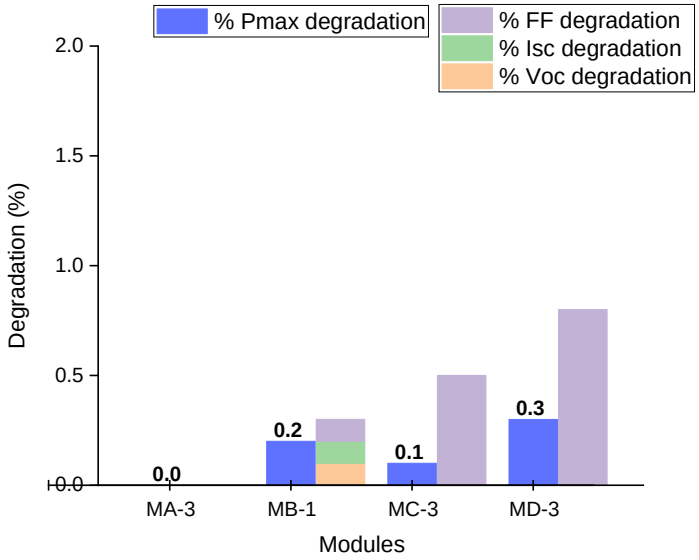

Fig. 114. Degradation in IV parameters for the front stressed side at 1000 W/m^2

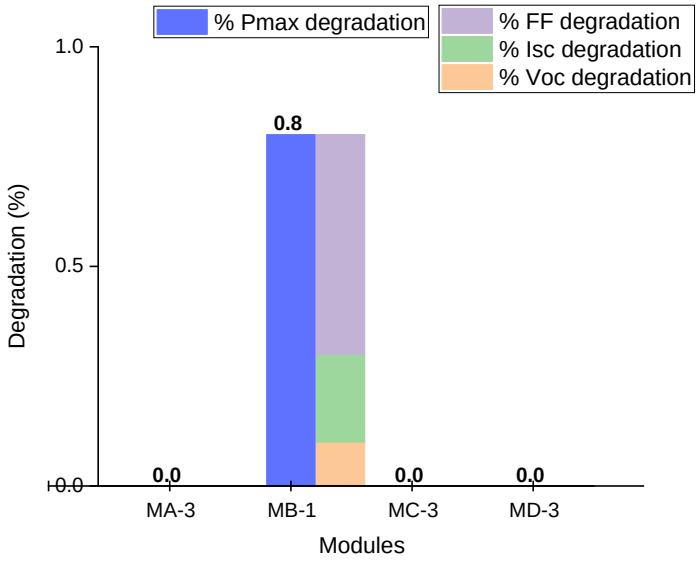

Fig. 115. Degradation in IV parameters for the front stressed side at 220 W/m^2

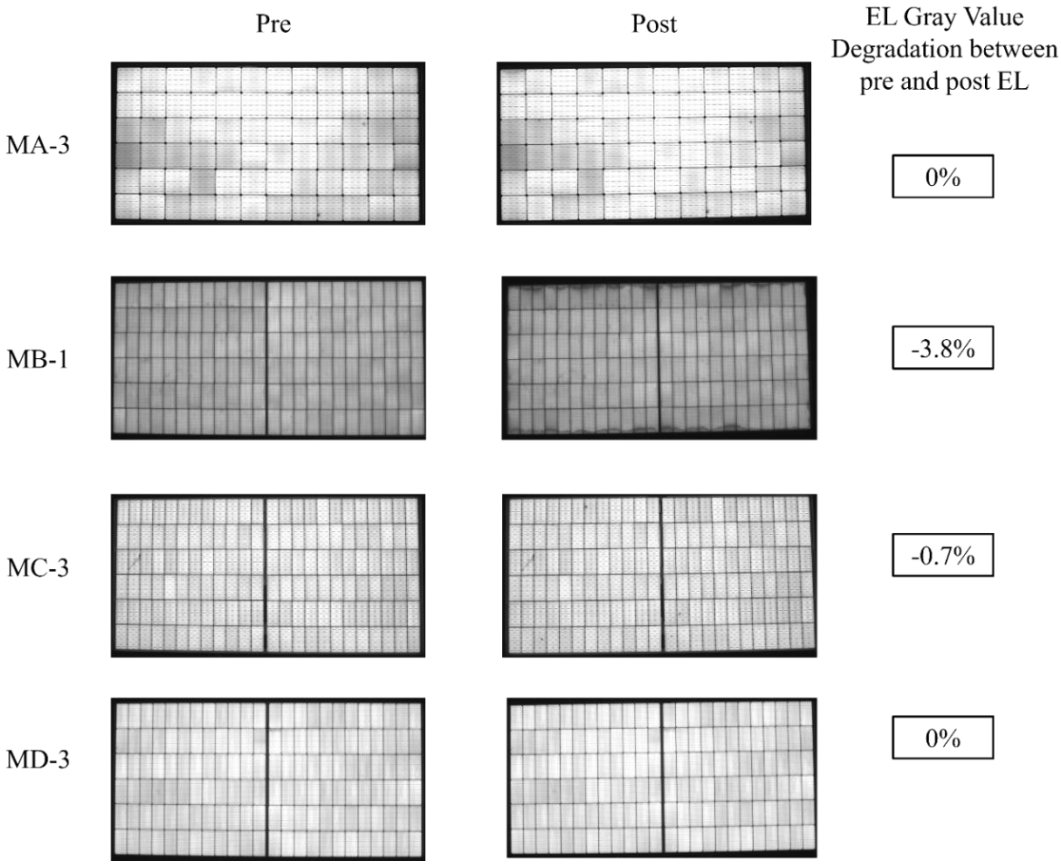

Fig. 116. EL images for the front stressed side at 100% I_{SC} and 30-sec exposure with gray value change

At 200W/m^2, the stressed side's R_S and R_{SH} changed by +12.1% and -14.0%, respectively.

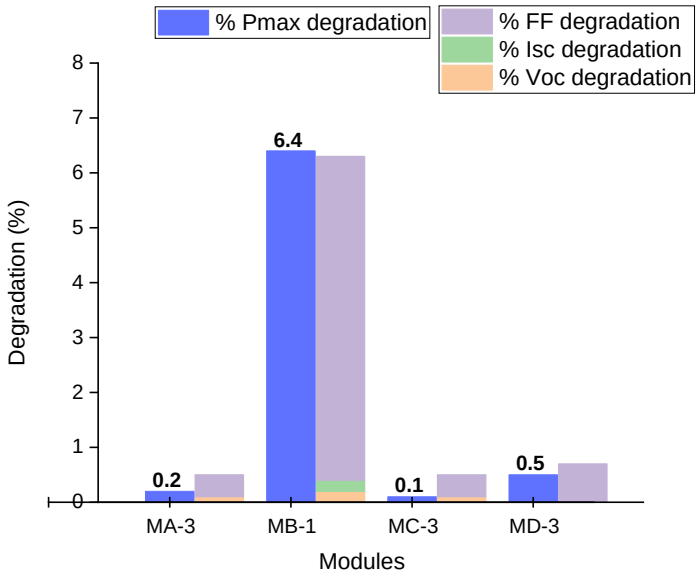

Fig. 117. Degradation in IV parameters for the rear unstressed side at 1000 W/m^2

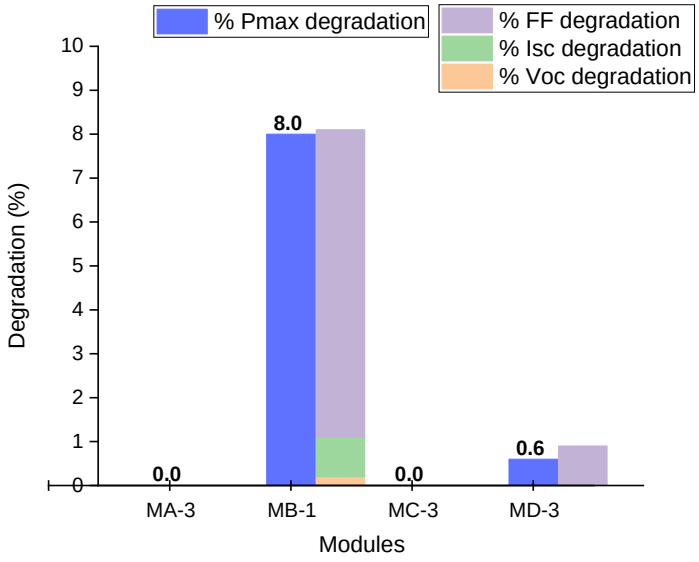

Fig. 118. Degradation in IV parameters for the rear unstressed side at 200 W/m^2

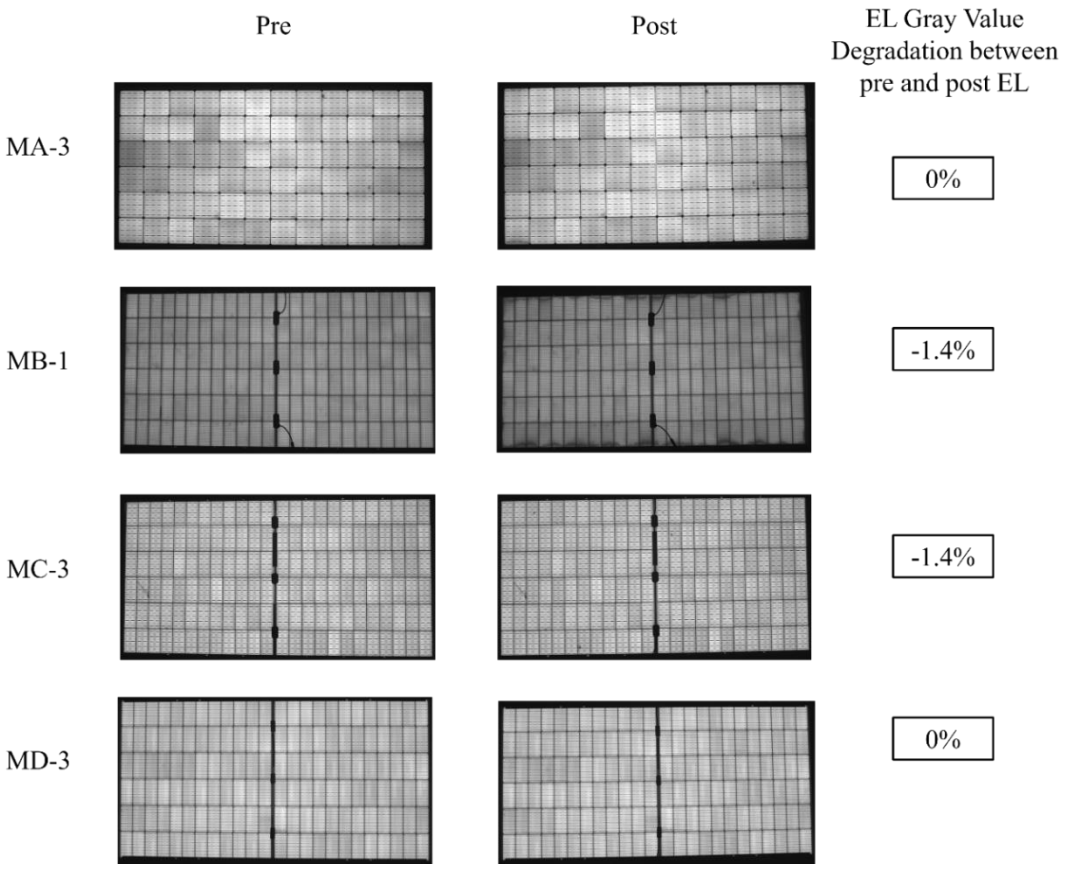

Fig. 119. EL images for the rear unstressed side at 100% I_{SC} and 30-sec exposure with gray value change

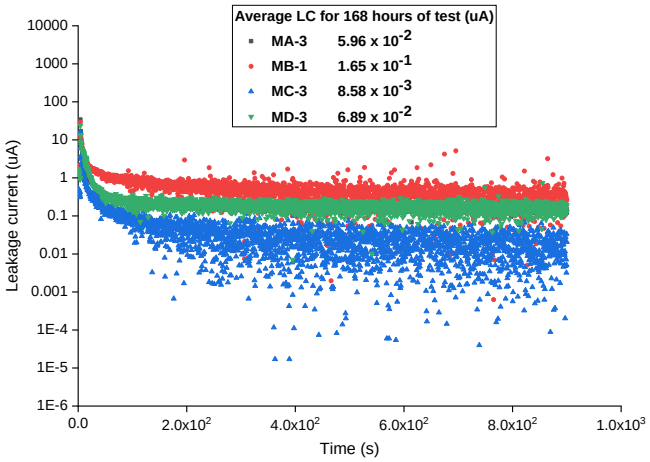

Fig. 120. Average LC data for 168h of stress and log scale LC plots for the first 900s of stress (stabilized after 300s)

Only MB-1 shows deterioration in round-3, while Pmax degradation in other modules is less than 1%. The deterioration may be linked to a PID-s process (explained in the literature review section) when there is a negative bias at the front of the PERC cell. The EL's recognizable patterns, as well as the drops in FF and $R_{SH,}$ confirm this. However, the unstressed module's rear shows more significant deterioration than the front.

This may be attributed to two factors. One cause could be the reuse of MB-1 in round-3. Stress for 168+168 hours in both rounds might result in moisture infiltration in the modules, as revealed by EL, which indicates additional cell darkening at the module borders. Therefore, moisture intrusion might result in more stress on the unstressed rear side. These findings also point to certain drawbacks of the monofacial PID stress approach for bifacial modules utilizing Al foil, which is still being tested [173].

Round-4 (Cell at +ve bias with stress at rear side): When tested at 1000W/m^2 and 200W/m^2, all modules exhibited a Pmax drop of less than 1%, suggesting no deterioration. The literature also supports these results, as discussed earlier [173].

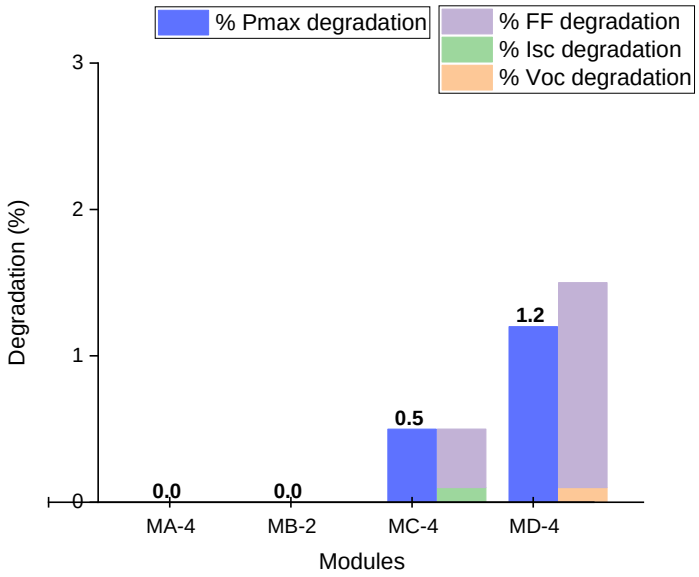

Fig. 121. Degradation in IV parameters for the rear stressed side at 1000 W/m^2

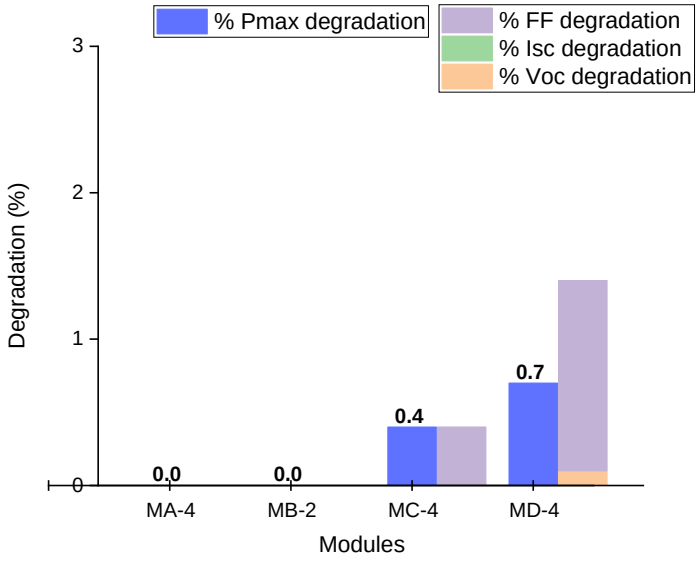

Fig. 122. Degradation in IV parameters for the rear stressed side at 200 W/m^2

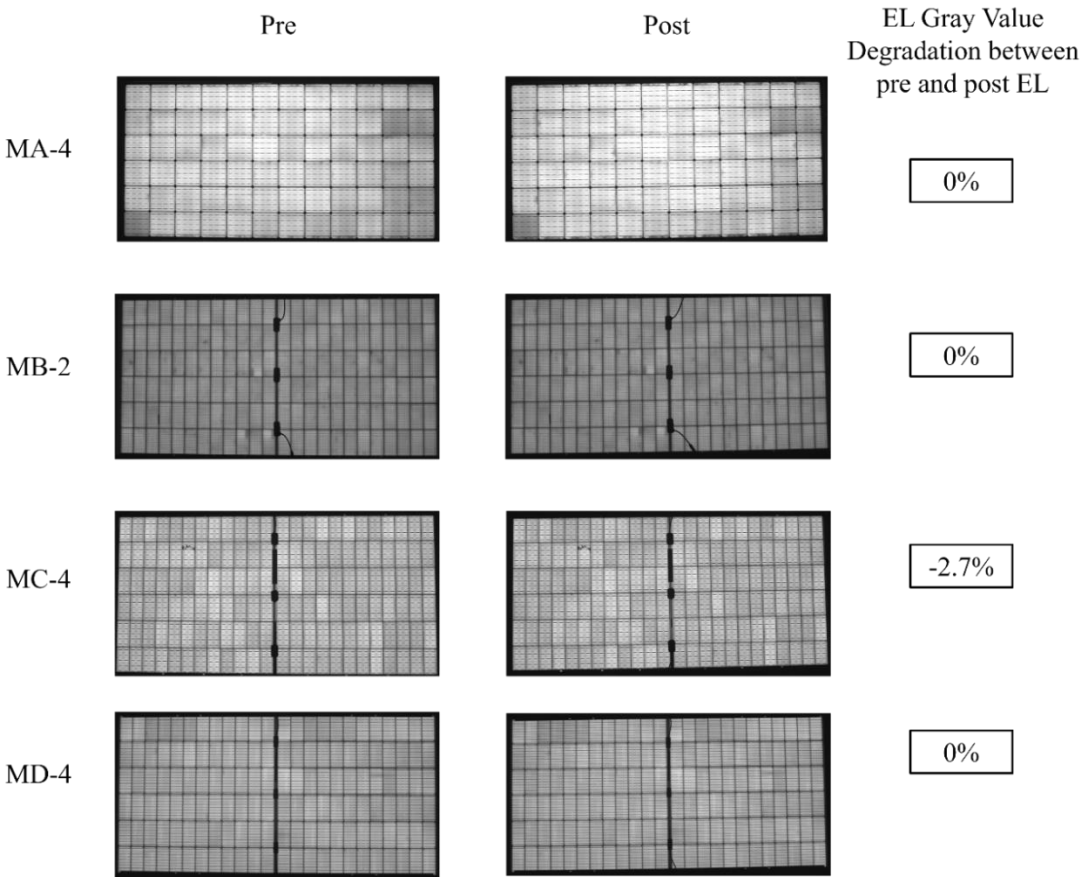

Fig. 123. EL images for the rear stressed side at 100% I_{SC} and 30-sec exposure with gray value change

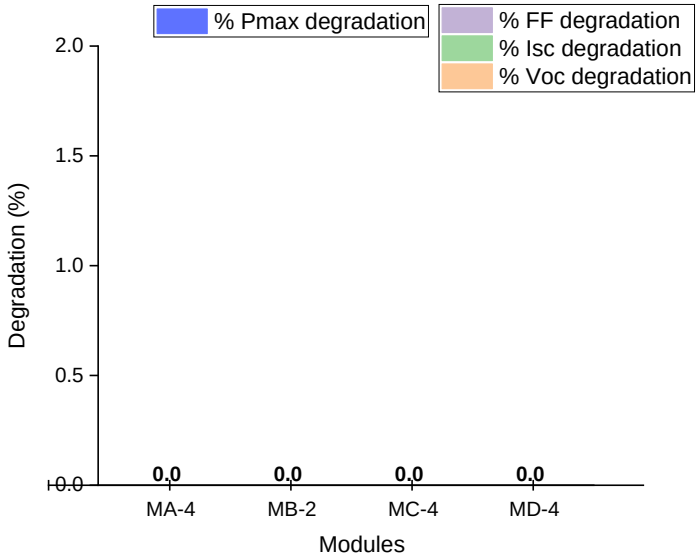

Fig. 124. Degradation in IV parameters for the front unstressed side at 1000 W/m^2

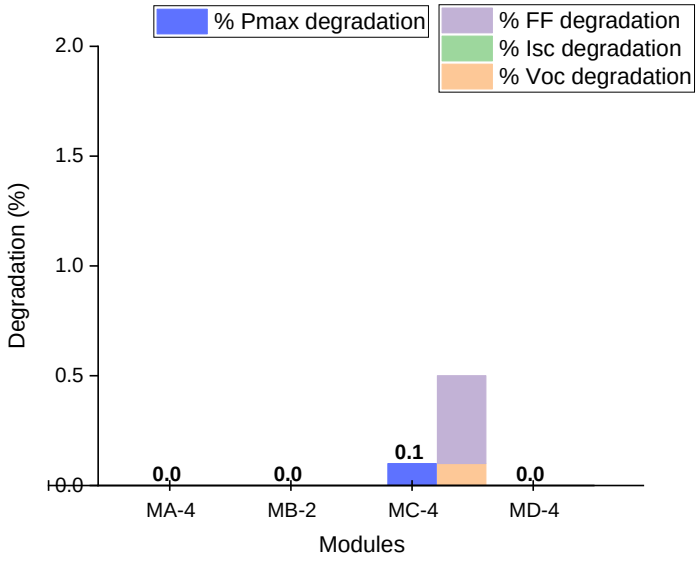

Fig. 125. Degradation in IV parameters for the front unstressed side at 200 W/m^2

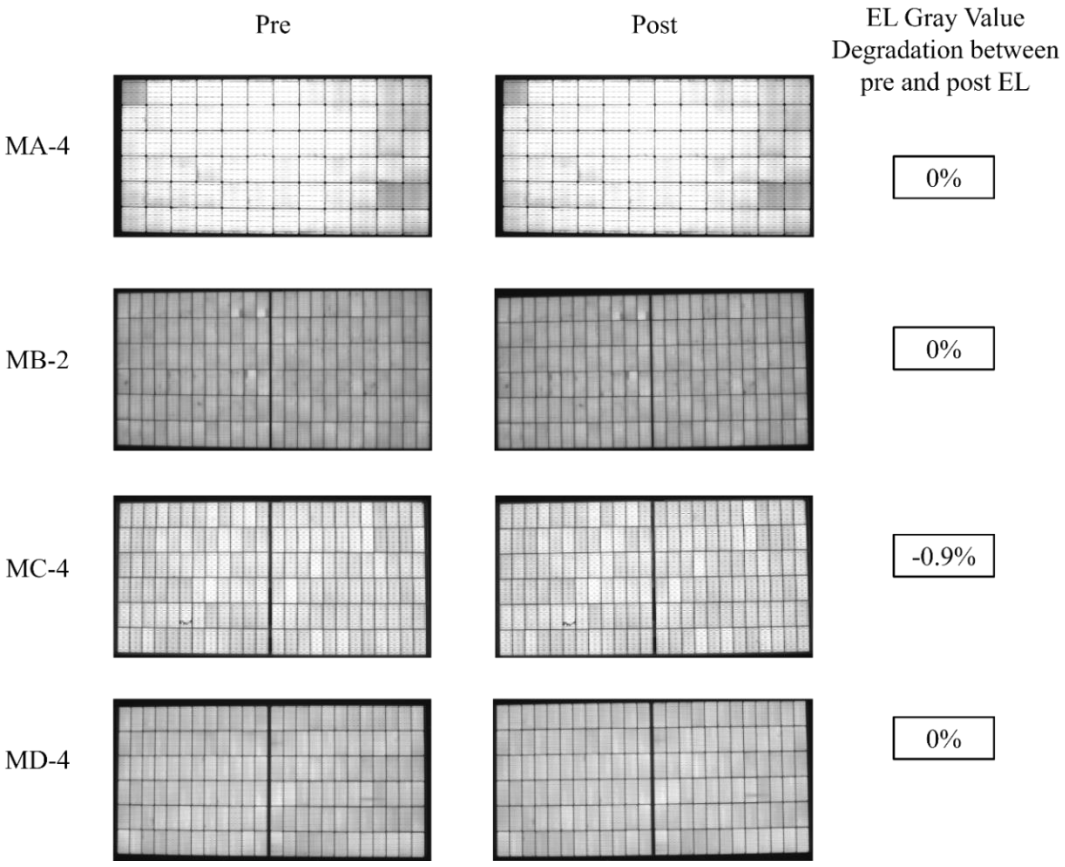

Fig. 126. EL images for the front unstressed side at 100% I_{SC} and 30-sec exposure with gray value change

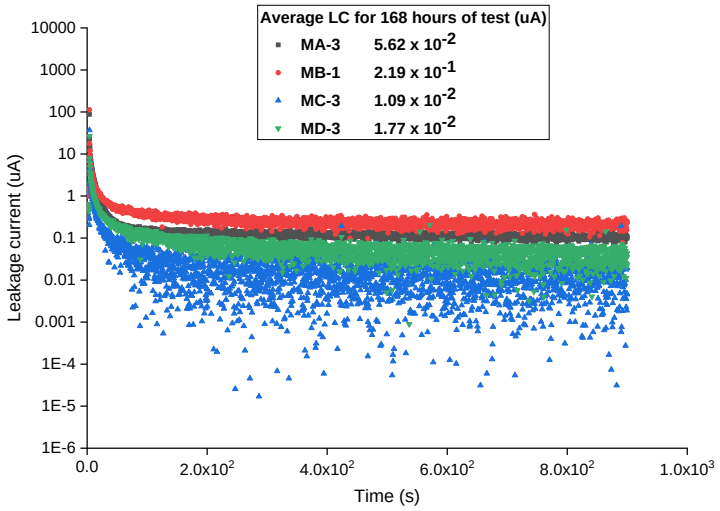

Fig. 127. Average LC data for 168h of stress and log scale LC plots for the first 900s of stress (stabilized after 300s)

CHAPTER 5: CONCLUSIONS

In conclusion, this dissertation has explored and analyzed the topic of PID in PV modules in-depth, from various perspectives, and through different research methods. This study sought to comprehend the impact of superstrate, encapsulant, and substrate on PID using various one-cell and commercial modules. The findings presented in the previous chapters make it clear that all three components can significantly affect the progression of PID in PV modules. These findings have substantial implications for the PV industry and can be used to inform future research, policy, and practice. In this final chapter, the study's key results are summarized, and recommendations for future research are presented.

- Backsheet: The module's components, including the front glass, encapsulant, cell type, and backsheet, might affect performance due to PID. Although there has been much research on the glass surface, cell type, and encapsulant, there has been little to no research on the impact of backsheets and their interactions with encapsulants. Therefore, employing similar one-cell modules, a portion of this research has examined the effects of various backsheets and encapsulants on PID. The findings show that the backsheet material might affect PID. We see a decrease in Pmax between 0% and 9% for excellent and poor backsheet materials. The more a backsheet is damaged by moisture penetration due to high water transmission, the more PID is noticed since the backsheet material has fewer water barrier layers.
- Encapsulant: The same is valid for encapsulants, where POE, which has a far higher volumetric resistance than EVA, does not degrade due to PID. Furthermore, when it comes to the backsheets, we see that a particular backsheet module that suffers severely from PID with EVA exhibits no PID when the encapsulant is changed to POE,

demonstrating the ability of a better encapsulant with higher bulk resistance to maintain module performance even when the backsheet is partially damaged.

- AS coating: It is also investigated how PID may be decreased by applying a hydrophobic AS coating on the glass surface. It is well known that a dirt buildup on glass surfaces may worsen the PID problem. Therefore, it is expected that hydrophobic AS coating on the installed/soiled modules in the field would have three advantages: lowering the soiling problem, reducing the PID issue owing to lower soiling level, and reducing the PID issue due to lower surface conductivity level. Although the PID problem was decreased by the AS coating we applied, it was not entirely resolved. Our manually coated layer likely has some pinholes that cause the flow of LC via water-filled pinholes.
- PID on pre-DH stressed GG modules: Given that GG construction is anticipated to dominate the PV industry, it is vital to identify their failure mechanisms. Our findings suggest that GG modules are more susceptible to PID problems (11 to 12 percent deterioration owing to sequential DH and PID). The conclusion above is supported by data from characterization tests such as IV, EL, dark IV, reflectance spectrometer, and outdoor IR. We found that the GG modules utilized in our research deteriorate more owing to the absence of or use of a weak edge sealant in conjunction with EVA as the encapsulant, allowing moisture to permeate/reduce the strength of interface adhesive connections in the module under DH stress. This increased presence of moisture limits the module's output and creates striation rings, indicating incorrect or substandard module fabrication. In addition, during the PID test, when the adhesion interface strengths are already diminished owing to DH, the enhanced moisture sensitivity in the

GG modules activates PID-s and PID-p in the negative bias. Under a positive bias, the early phase of PID-c is seen, resulting in a more significant power loss. In addition, the double glass construction works as a heat trap, resulting in a higher module operating temperature, which harms the overall performance and longevity of the module.

- PID on pre-DH stressed GB modules: The GB modules subjected to serial DH and PID stress exhibit 4 to 6% deterioration owing to DH stress and an additional 1.5 to 2.5% degradation due to PID. Due to serial DH and PID, GB modules have a 6 to 7 percent overall deterioration. The reduction in DH stress is primarily attributable to moisture entering via the backsheet. Due to decreased interfacial adhesion strengths during the DH stress, the modules experience some deterioration during the PID stress. Under a negative bias, GB-1 encounters PIDs because most of its power loss is due to FF. Under a positive bias, the GB-2 modules undergo the early phases of PID-c as a result of a decrease in FF and an increase in R_S.
- PID in bifacial modules focused on PID-p: In this part of the work, a comprehensive analysis of PID susceptibility in commercial c-Si bifacial modules was performed. We discovered that the most significant deterioration in Pmax of bifacial modules due to PID-p occurs when the cell is at a negative bias relative to the rear side (32%). This deterioration is more severe at lower irradiances (51%), which is significant for bifacial modules since the back side works at a lower irradiance in the field. After storage and before recovery, more deterioration is also detected in one module. All modules recover almost completely when exposed to sunlight for 18-19 kWh/m^2 of average insolation. When the cell is under a positive bias relative to the module front, the deterioration is less than 5%, and we suggest that the process involved is PID-p. When the cell is under

a negative bias with regard to the front, it is seen that a PID-s process is responsible for Pmax deterioration in the module. When the cell is at the positive bias relative to the module rear, Pmax deterioration in all modules is less than 1%, indicating that no PID process is happening. The given results clearly indicate that PID-p is observable in commercially available module technologies; hence, the findings of this work might be of great use to the PV community, since the use of bifacial modules is anticipated to rise in the future.

REFERENCES

[1] M. Asad, F. I. Mahmood, I. Baffo, A. Mauro, and A. Petrillo, “The Cost Benefit Analysis of Commercial 100 MW Solar PV: The Plant Quaid-e-Azam Solar Power Pvt Ltd.,” *Sustain.*, vol. 14, no. 5, pp. 1–13, 2022.

[2] F. ibne Mahmood, M. Z. U. A. Afridi, H. A. Raza, and H. A. Khalid, “Investigation and Comparison of DC and AC Nanogrid Networks using MATLAB/Simulink,” *Int. J. Eng. Work.*, vol. 9, no. 5, pp. 131–143, 2022.

[3] H. A. Raza, A. Bin Ahmed, A. K. Janjua, M. Ali, M. Sattar, and M. Z. U. A. Afridi, “Performance analysis and cost reduction of Brayton Cycle based Solar Thermal Tower Power Plant using TRNSYS,” in *2020 IEEE 23rd International Multitopic Conference (INMIC)*, 2020, pp. 1–6.

[4] P. Bojek, “IEA Solar PV,” 2022.

[5] S. Ali *et al.*, “A Comprehensive Study of 18-19 years field Aged modules for Degradation Rate Determination along with defect Detection and Analysis Using IR, EL, UV,” in *2018 15th International Bhurban Conference on Applied Sciences and Technology (IBCAST)*, 2018, pp. 28–35.

[6] M. Bilal, M. N. Arbab, M. Z. U. A. Afridi, and A. Khattak, “Increasing the output power and efficiency of solar panel by using concentrator photovoltaics (CPV),” *Int. J. Eng. Work.*, vol. 3, no. 12, pp. 98–102, 2016.

[7] M. Becquerel, “Mémoire sur les effets électriques produits sous l’influence des rayons solaires,” *C. R. Hebd. Seances Acad. Sci.*, vol. 9, pp. 561–567, 1839.

[8] “Edmond Becquerel: The Man Behind Solar Panels - Solenergy Systems Inc.” [Online]. Available: https://solenergy.com.ph/solar-panel-philippines-edmond-becquerel/. [Accessed: 05-Oct-2022].

[9] “Solar Photovoltaic Technology Basics | NREL.” [Online]. Available: https://www.nrel.gov/research/re-photovoltaics.html. [Accessed: 05-Oct-2022].

[10] “Latest Trends in Renewable Energy,” 2022. [Online]. Available: https://www.irena.org/Statistics/View-Data-by-Topic/Capacity-and-Generation/Statistics-Time-Series. [Accessed: 05-Oct-2022].

[11] “Solar energy Data.” [Online]. Available: https://www.irena.org/solar. [Accessed: 05-Oct-2022].

[12] Fraunhofer Institute for Solar Energy Systems ISE with support of PSE Projects GmbH, “Photovoltaics Report,” 2022.

[13] Hamsini Gopalakrishna, “Accelerated Reliability Testing of Fresh and Field-Aged

Photovoltaic Modules: Encapsulant Browning and Solder Bond Degradation," 2020.

[14] "Solar Panel Construction — Clean Energy Reviews." [Online]. Available: https://www.cleanenergyreviews.info/blog/solar-panel-components-construction. [Accessed: 08-Oct-2022].

[15] J. Shah, "EVA Sheet: An Important Constituent of a Solar Module," *Saur Energy International*, 2022. [Online]. Available: https://www.saurenergy.com/solar-energy-blog/eva-sheet-an-important-constituent-of-a-solar-module-explained. [Accessed: 09-Oct-2022].

[16] "Bifacial PV Modules," *Boviet Solar*. [Online]. Available: https://bovietsolar.com/technology/bifacial-modules. [Accessed: 14-Oct-2022].

[17] F. Mahmood *et al.*, "Temperature coefficient of power (Pmax) of field aged PV modules: impact on performance ratio and degradation rate determinations," in *Reliability of Photovoltaic Cells, Modules, Components, and Systems X*, 2017, pp. 52–58.

[18] M. Aghaei *et al.*, "Review of degradation and failure phenomena in photovoltaic modules," *Renew. Sustain. Energy Rev.*, vol. 159, no. February, p. 112160, 2022.

[19] M. A. Afridi, M. Arbab, M. Bilal, H. Ullah, and N. Ullah, "Determining the effect of soiling and dirt particles at various tilt angles of photovoltaic modules," *Int. J. Eng. Work.*, vol. 4, no. 8, pp. 143–146, 2017.

[20] M. Köntges *et al.*, "Performance and reliability of photovoltaic systems," 2014.

[21] J. Kim, M. Rabelo, S. P. Padi, H. Yousuf, E.-C. Cho, and J. Yi, "A Review of the Degradation of Photovoltaic Modules for Life Expectancy," *Energies*, vol. 14, no. 14, p. 4278, 2021.

[22] M. Dhimish, V. Holmes, B. Mehrdadi, M. Dales, and P. Mather, "Output-Power Enhancement for Hot Spotted Polycrystalline Photovoltaic Solar Cells," *IEEE Trans. Device Mater. Reliab.*, vol. 18, no. 1, pp. 37–45, 2018.

[23] N. Ishaq, F. Altaf, Z. U. A. Afridi, and N. Arbab, "Performance Analysis of Perturb & Observe and Open Circuit Voltage Algorithms for MPPT Tracking at Different Environmental Conditions," *Int. J. Eng. Work.*, vol. 8, no. 4, pp. 143–148, 2021.

[24] E. Molenbroek, D. W. Waddington, and K. A. Emery, "Hot spot susceptibility and testing of PV modules," in *IEEE Photovoltaic Specialists Conference*, 1992, vol. 1, no. November 1991, pp. 547–552.

[25] M. Afridi, A. Kumar, F. ibne Mahmood, and G. Tamizhmani, "Hotspot testing of glass/backsheet and glass/glass PV modules pre-stressed in extended thermal cycling," *Sol. Energy*, vol. 249, pp. 467–475, 2023.

[26] D. C. Jordan, T. J. Silverman, J. H. Wohlgemuth, S. R. Kurtz, and K. T. VanSant, "Photovoltaic failure and degradation modes," *Prog. Photovoltaics Res. Appl.*, vol. 25, no. 4, pp. 318--326, 2017.

[27] J. Li, Y. C. Shen, P. Hacke, and M. Kempe, "Electrochemical mechanisms of leakage-current-enhanced delamination and corrosion in Si photovoltaic modules," *Sol. Energy Mater. Sol. Cells*, vol. 188, no. September, pp. 273–279, 2018.

[28] J. H. Kim, J. Park, D. Kim, and N. Park, "Study on mitigation method of solder corrosion for crystalline silicon photovoltaic modules," *Int. J. Photoenergy*, vol. 2014, pp. 13–17, 2014.

[29] A. Omazic *et al.*, "Relation between degradation of polymeric components in crystalline silicon PV module and climatic conditions: A literature review," *Sol. Energy Mater. Sol. Cells*, vol. 192, no. December 2018, pp. 123–133, 2019.

[30] H. Xiong *et al.*, "Corrosion behavior of crystalline silicon solar cells," *Microelectron. Reliab.*, vol. 70, pp. 49–58, 2017.

[31] G. Oreski and G. M. Wallner, "Evaluation of the aging behavior of ethylene copolymer films for solar applications under accelerated weathering conditions," *Sol. Energy*, vol. 83, no. 7, pp. 1040–1047, 2009.

[32] J. H. Wohlgemuth, P. Hacke, N. Bosco, D. C. Miller, M. D. Kempe, and S. R. Kurtz, "Assessing the causes of encapsulant delamination in PV modules," *2016 IEEE 43rd Photovolt. Spec. Conf.*, pp. 0248–0254, 2016.

[33] D. C. Jordan and S. R. Kurtz, "Photovoltaic degradation rates—an analytical review," *Prog. photovoltaics Res. Appl.*, vol. 21, no. 1, pp. 12–29, 2013.

[34] Jaewon Oh, "Elimination of Potential-Induced Degradation for Crystalline Silicon Solar Cells," 2016.

[35] H. A. Raza, F. I. Mahmood, and G. TamizhMani, "Use of non-contact voltmeter to quantify potential induced degradation in CdTe modules," *Sol. Energy*, vol. 252, pp. 284–290, 2023.

[36] G. Mon, L. Wen, R. Ross, and D. Adent, "Effects of temperature and moisture on module leakage currents," in *18th IEEE PVSC*, 1985, pp. 1179–1185.

[37] D. Carlson *et al.*, "Corrosion effects in thin-film photovoltaic modules," *Prog. Photovoltaics Res. Appl.*, vol. 11, no. 6, pp. 377–386, 2003.

[38] R. Swanson *et al.*, "The surface polarization effect in high-efficiency silicon solar cells," in *15th PVSEC*, 2005.

[39] I. Rutschmann, "Auch module von evergreen zeigen polarizationsverhalten," in

Photon, 2008, pp. 122–123.

[40] S. Pingel *et al.*, "Potential induced degradation of solar cells and panels," in *2010 35th IEEE Photovoltaic Specialists Conference*, 2010, pp. 002817–002822.

[41] W. Luo *et al.*, "Potential-induced degradation in photovoltaic modules: A critical review," *Energy Environ. Sci.*, vol. 10, no. 1, pp. 43–68, 2017.

[42] R. Malachi, S. Schönberger, J. Mayer, and M. Kasemann, "Techno-economic analysis of utility scale PV power plants with up to+/-1500VDC," in *29th European photovoltaic solar energy conference and exhibition, Amsterdam, The Netherlands*, 2014, pp. 2323–2326.

[43] C. Molto *et al.*, "Review of Potential-Induced Degradation in Bifacial PV Modules," *Energy Technol.*, p. 2200943, 2023.

[44] "Understanding Potential Induced Degradation (PID) and ways to mitigate it," *Novergy Solar*, 2020. [Online]. Available: https://www.novergysolar.com/understanding-potential-induced-degradation-pid-and-ways-to-mitigate-it/. [Accessed: 11-Oct-2022].

[45] N. G. Dhere, N. S. Shiradkar, and E. Schneller, "Evolution of leakage current paths in MC-Si PV modules from leading manufacturers undergoing high-voltage bias testing," *IEEE J. Photovoltaics*, vol. 4, no. 2, pp. 654–658, 2014.

[46] J. Berghold, O. Frank, H. Hoehne, S. Pingel, B. Richardson, and M. Winkler, "Potential induced degradation of solar cells and panels," in *25th EUPVSEC*, 2010, pp. 3753–3759.

[47] J. wei Zhang, D. kun Cao, S. Diaham, X. Zhang, X. qian Yin, and Q. Wang, "Research on potential induced degradation (PID) of polymeric backsheet in PV modules after salt-mist exposure," *Sol. Energy*, vol. 188, no. October 2018, pp. 475–482, 2019.

[48] G. Jorgensen, K. Terwilliger, G. Barber, C. Kennedy, and T. McMahon, "Measurements of backsheet moisture permeation and encapsulant-substrate adhesion," 2001.

[49] D. B. Sulas-Kern *et al.*, "Electrochemical degradation modes in bifacial silicon photovoltaic modules," *Prog. Photovoltaics Res. Appl.*, vol. 30, no. 8, pp. 948–958, 2022.

[50] S. Felder, Thomas C Choudhury, Kaushik Roy Garreau-Iles, Lucie MacMaster, H. Hu, W. J. Gambogi, and T. J. Trout, "Analysis of glass-glass modules," in *New Concepts in Solar and Thermal Radiation Conversion and Reliability*, 2018, pp. 44–52.

[51] V. Naumann, K. Ilse, and C. Hagendorf, “On the discrepancy between leakage currents and potential-induced degradation of crystalline silicon modules,” in *Proceedings of 28th European Photovoltaic Solar Energy Conference and Exhibition, Paris, France*, 2013, pp. 2994–2997.

[52] P. Hacke *et al.*, “Accelerated testing and modeling of potential-induced degradation as a function of temperature and relative humidity,” *2015 IEEE 42nd Photovolt. Spec. Conf. PVSC 2015*, vol. 5, no. 6, pp. 1549–1553, 2015.

[53] A. R. Hoffman and E. L. Miller, “Bias-humidity testing of solar-cell modules,” 1978.

[54] P. Hacke, S. Spataru, and S. Johnston, “Correction for metastability in the quantification of PID in thin-film module testing,” in *2017 IEEE 44th Photovoltaic Specialist Conference (PVSC)*, 2017, pp. 2819–2822.

[55] “IEC TS 62804-1: 2015 Photovoltaic (PV) modules-Test methods for the detection of potential-induced degradation-Part 1: Crystalline silicon,” *IEC--International Electrotech. Comm. Ed*, vol. 1, 2015.

[56] P. Hacke, R. Smith, K. Terwilliger, G. Perrin, B. Sekulic, and S. Kurtz, “Development of an IEC test for crystalline silicon modules to qualify their resistance to system voltage stress,” *Prog. Photovoltaics Res. Appl.*, vol. 22, no. 7, pp. 775–783, 2014.

[57] P. Hacke *et al.*, “System voltage potential-induced degradation mechanisms in PV modules and methods for test,” *2011 37th IEEE Photovolt. Spec. Conf.*, pp. 000814–000820, 2011.

[58] J. Oh, S. Bowden, and G. S. TamizhMani, “Potential-Induced Degradation (PID): Incomplete Recovery of Shunt Resistance and Quantum Efficiency Losses,” *IEEE J. Photovoltaics*, vol. 5, no. 6, pp. 1540–1548, 2015.

[59] “IEC 61215: Terrestrial photovoltaic (PV) modules-Design qualification and type approval– Part 2: Test procedures.” IEC, 2016.

[60] “IEC 61215-1-1:2021 RLV.” IEC, 2021.

[61] W. Luo *et al.*, “Investigation of the Impact of Illumination on the Polarization-Type Potential-Induced Degradation of Crystalline Silicon Photovoltaic Modules,” *IEEE J. Photovoltaics*, vol. 8, no. 5, pp. 1168–1173, 2018.

[62] K. Sporleder, M. Turek, N. Schüler, V. Naumann, D. Hevisov, and C. Hagendorf, “Quick test for reversible and irreversible PID of bifacial PERC solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 219, no. September 2020, p. 110755, 2021.

[63] “IEC TS 62804-1:2015 | rural electrification, solar power, LVDC.” IEC, 2015.

[64] P. L. Hacke, J. Kempe, Michael D Wohlgemuth, J. Li, and Y.-C. Shen, “Potential-induced degradation-delamination mode in crystalline silicon modules,” 2018.

[65] J. Carolus, J. A. Tsanakas, A. van der Heide, E. Voroshazi, W. De Ceuninck, and M. Daenen, “Physics of potential-induced degradation in bifacial p-PERC solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 200, p. 109950, 2019.

[66] W. Luo *et al.*, “Elucidating potential-induced degradation in bifacial PERC silicon photovoltaic modules,” *Prog. Photovoltaics Res. Appl.*, vol. 26, no. 10, pp. 859–867, 2018.

[67] M. Schütze, M. Junghänel, S. Koentopp, Max B Cwikla, Sebastian Friedrich, J. W. Müller, and P. Wawer, “Laboratory study of potential induced degradation of silicon photovoltaic modules,” in *2011 37th IEEE Photovoltaic Specialists Conference*, 2011, pp. 000821–000826.

[68] P. Hacke *et al.*, “Influence of impurities in module packaging on potential-induced degradation,” 2012.

[69] D. Lausch *et al.*, “Potential-Induced Degradation (PID): Introduction of a Novel Test Approach and Explanation of Increased Depletion Region Recombination,” *IEEE J. Photovoltaics*, vol. 4, no. 3, pp. 834–840, 2014.

[70] S. Yamaguchi and K. Ohdaira, “Degradation behavior of crystalline silicon solar cells in a cell-level potential-induced degradation test,” *Sol. Energy*, vol. 155, pp. 739–744, 2017.

[71] J. Berghold, S. Koch, A. Böttcher, A. Ukar, M. Leers, and P. Grunow, “Potential-induced degradation (PID) and its correlation with experience in the field,” *Photovoltaics Int.*, vol. 19, no. 7, pp. 82–93, 2013.

[72] M. Koehl and S. Hoffmann, “Impact of rain and soiling on potential induced degradation,” *Prog. Photovoltaics Res. Appl.*, vol. 24, no. 10, pp. 1304–1309, 2016.

[73] H. R. Moutinho *et al.*, “Development of coring procedures applied to Si , CdTe , and CIGS solar panels Tempered glass,” *Sol. Energy*, vol. 161, no. January, pp. 235–241, 2018.

[74] A. Sinha *et al.*, “Glass / glass photovoltaic module reliability and degradation : a review,” *J. Phys. D. Appl. Phys.*, vol. 54, no. 41, p. 413002, 2021.

[75] Z. Purohit, D. Verma, and B. Tripathi, “Electro-analytical investigation of potential induced degradation in mc-silicon solar cells: case of sodium ion induced inductive loop,” *Phys. Chem. Chem. Phys.*, vol. 20, no. 28, pp. 19168–19176, 2018.

[76] N. Katayama, S. Osawa, S. Matsumoto, T. Nakano, and M. Sugiyama, “Degradation and fault diagnosis of photovoltaic cells using impedance spectroscopy,” *Sol.*

Energy Mater. Sol. Cells, vol. 194, pp. 130–136, 2019.

[77] "International Technology Roadmap for Photovoltaic (ITRPV) 2020 Results," 2020.

[78] X. Wang and A. Barnett, "The evolving value of photovoltaic module efficiency," *Appl. Sci.*, vol. 9, no. 6, p. 1227, 2019.

[79] A. Kumar, M. Bieri, T. Reindl, and A. G. Aberle, "Economic viability analysis of silicon solar cell manufacturing: Al-BSF versus PERC," *Energy Procedia*, vol. 130, pp. 43–49, 2017.

[80] C. A. Deline, S. Ayala Pelaez, W. F. Marion, W. R. Sekulic, M. A. Woodhouse, and J. Stein, "Bifacial PV system performance: separating fact from fiction," 2019.

[81] T. S. Liang *et al.*, "A review of crystalline silicon bifacial photovoltaic performance characterisation and simulation," *Energy Environ. Sci.*, vol. 12, no. 1, pp. 116–148, 2019.

[82] P. Hacke *et al.*, "Characterization of multicrystalline silicon modules with system bias voltage applied in damp heat," 2011.

[83] V. Naumann, C. Hagendorf, S. Grosser, M. Werner, and J. Bagdahn, "Micro structural root cause analysis of potential induced degradation in c-Si solar cells," *Energy Procedia*, vol. 27, pp. 1–6, 2012.

[84] T. Kaden, K. Lammers, and H. J. Möller, "Power loss prognosis from thermographic images of PID affected silicon solar modules," *Sol. Energy Mater. Sol. Cells*, vol. 142, pp. 24–28, 2015.

[85] V. Naumann *et al.*, "The role of stacking faults for the formation of shunts during potential-induced degradation of crystalline Si solar cells," *Phys. status solidi (RRL)--Rapid Res. Lett.*, vol. 7, no. 5, pp. 315–318, 2013.

[86] V. Naumann *et al.*, "Explanation of potential-induced degradation of the shunting type by Na decoration of stacking faults in Si solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 120, pp. 383–389, 2014.

[87] V. Naumann, D. Lausch, and C. Hagendorf, "Sodium decoration of PID-s crystal defects after corona induced degradation of bare silicon solar cells," *Energy Procedia*, vol. 77, pp. 397–401, 2015.

[88] B. Ziebarth, M. Mrovec, C. Elsässer, and P. Gumbsch, "Potential-induced degradation in solar cells: Electronic structure and diffusion mechanism of sodium in stacking faults of silicon," *J. Appl. Phys.*, vol. 116, no. 9, p. 093510, 2014.

[89] X. Gou, X. Li, S. Wang, H. Zhuang, X. Huang, and L. Jiang, "The effect of microcrack length in silicon cells on the potential induced degradation behavior,"

Int. J. Photoenergy, vol. 2018, 2018.

[90] S. Jonai, K. Nakamura, and A. Masuda, "Universal explanation for degradation by charge accumulation in crystalline Si photovoltaic modules with application of high voltage," *Appl. Phys. Express*, vol. 12, no. 10, p. 101003, 2019.

[91] P. Hacke *et al.*, "Acceleration factor determination for potential-induced degradation in crystalline silicon PV modules," in *2013 IEEE International Reliability Physics Symposium (IRPS)*, 2013, pp. 4B–1.

[92] K. Brecl, M. Bokalič, and M. Topič, "Examination of photovoltaic silicon module degradation under high-voltage bias and damp heat by electroluminescence," *J. Sol. Energy Eng.*, vol. 139, no. 3, 2017.

[93] J. Henrie, S. Kellis, S. M. Schultz, and A. Hawkins, "Electronic color charts for dielectric films on silicon," *Opt. Express*, vol. 12, no. 7, pp. 1464–1469, 2004.

[94] R. S. Bonilla, B. Hoex, P. Hamer, and P. R. Wilshaw, "Dielectric surface passivation for silicon solar cells: A review," *Phys. status solidi*, vol. 214, no. 7, p. 1700293, 2017.

[95] K. Morita and K. Ohnaka, "Novel selective etching method for silicon nitride films on silicon substrates by means of subcritical water," *Ind. Eng. Chem. Res.*, vol. 39, no. 12, pp. 4684–4688, 2000.

[96] K. O. Davis *et al.*, "Manufacturing metrology for c-Si module reliability and durability Part II: Cell manufacturing," *Renew. Sustain. Energy Rev.*, vol. 59, pp. 225–252, 2016.

[97] A. Sinha *et al.*, "Understanding interfacial chemistry of positive bias high-voltage degradation in photovoltaic modules," *Sol. Energy Mater. Sol. Cells*, vol. 223, p. 110959, 2021.

[98] K. Sporleder *et al.*, "Potential-induced degradation of bifacial PERC solar cells under illumination," *IEEE J. Photovoltaics*, vol. 9, no. 6, pp. 1522–1525, 2019.

[99] K. Sporleder *et al.*, "Root cause analysis on corrosive potential-induced degradation effects at the rear side of bifacial silicon PERC solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 201, p. 110062, 2019.

[100] K. Sporleder *et al.*, "Local corrosion of silicon as root cause for potential-induced degradation at the rear side of bifacial PERC solar cells," *Phys. status solidi (RRL)--Rapid Res. Lett.*, vol. 13, no. 9, p. 1900163, 2019.

[101] K. Sporleder *et al.*, "Microstructural analysis of local silicon corrosion of bifacial solar cells as root cause of potential-induced degradation at the rear side," *Phys. status solidi*, vol. 216, no. 17, p. 1900334, 2019.

[102] P. Hacke *et al.*, “Application of the terrestrial photovoltaic module accelerated test-to-failure protocol,” in *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)*, 2014, pp. 0930–0936.

[103] P. Hacke *et al.*, “Test-to-failure of crystalline silicon modules,” in *2010 35th IEEE Photovoltaic Specialists Conference*, 2010, pp. 000244–000250.

[104] J. Schmidt, R. Peibst, and R. Brendel, “Surface passivation of crystalline silicon solar cells: Present and future,” *Sol. Energy Mater. Sol. Cells*, vol. 187, pp. 39–54, 2018.

[105] V. Benda and L. Černá, “PV cells and modules--State of the art, limits and trends,” *Heliyon*, vol. 6, no. 12, p. e05666, 2020.

[106] J. Šlamberger, M. Schwark, B. B. Van Aken, and P. Virtič, “Comparison of potential-induced degradation (PID) of n-type and p-type silicon solar cells,” *Energy*, vol. 161, pp. 266–276, 2018.

[107] S. Yamaguchi, K. Nakamura, A. Masuda, and K. Ohdaira, “Rapid progression and subsequent saturation of polarization-type potential-induced degradation of n-type front-emitter crystalline-silicon photovoltaic modules,” *Jpn. J. Appl. Phys.*, vol. 57, no. 12, p. 122301, 2018.

[108] S. Yamaguchi, A. Masuda, and K. Ohdaira, “Progression of rapid potential-induced degradation of n-type single-crystalline silicon photovoltaic modules,” *Appl. Phys. Express*, vol. 9, no. 11, p. 112301, 2016.

[109] M. Wilson, A. Savtchouk, P. Edelman, D. Marinskiy, and J. Lagowski, “Drift characteristics of mobile ions in SiNx films and solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 142, pp. 102–106, 2015.

[110] S. Bae *et al.*, “Potential induced degradation of n-type crystalline silicon solar cells with p+ front junction,” *Energy Sci. Eng.*, vol. 5, no. 1, pp. 30–37, 2017.

[111] K. Hara, S. Jonai, and A. Masuda, “Potential-induced degradation in photovoltaic modules based on n-type single crystalline Si solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 140, pp. 361–365, 2015.

[112] V. Sharma, C. Tracy, D. Schroder, S. Herasimenka, W. Dauksher, and S. Bowden, “Manipulation of K center charge states in silicon nitride films to achieve excellent surface passivation for silicon solar cells,” *Appl. Phys. Lett.*, vol. 104, no. 5, p. 053503, 2014.

[113] B. M. Habersberger and P. Hacke, “Impact of illumination and encapsulant resistivity on polarization-type potential-induced degradation on n-PERT cells,” *Prog. Photovoltaics Res. Appl.*, vol. 30, no. 5, pp. 455–463, 2022.

[114] Y. Komatsu, S. Yamaguchi, A. Masuda, and K. Ohdaira, “Multistage performance deterioration in n-type crystalline silicon photovoltaic modules undergoing potential-induced degradation,” *Microelectron. Reliab.*, vol. 84, pp. 127–133, 2018.

[115] K. Ohdaira, Y. Komatsu, T. Suzuki, S. Yamaguchi, and A. Masuda, “Influence of sodium on the potential-induced degradation for n-type crystalline silicon photovoltaic modules,” *Appl. Phys. Express*, vol. 12, no. 6, p. 064004, 2019.

[116] G. J. Janssen *et al.*, “Minimizing the polarization-type potential-induced degradation in PV modules by modification of the dielectric antireflection and passivation stack,” *IEEE J. Photovoltaics*, vol. 9, no. 3, pp. 608–614, 2019.

[117] Y. Ohno, T. Taishi, Y. Tokumoto, and I. Yonenaga, “Interaction of dopant atoms with stacking faults in silicon crystals,” *J. Appl. Phys.*, vol. 108, no. 7, p. 073514, 2010.

[118] S. Yamaguchi, B. B. Van Aken, A. Masuda, and K. Ohdaira, “Potential-Induced Degradation in High-Efficiency n-Type Crystalline-Silicon Photovoltaic Modules: A Literature Review,” *Sol. RRL*, vol. 5, no. 12, p. 2100708, 2021.

[119] M. Barbato, A. Barbato, M. Meneghini, G. Tavernaro, M. Rossetto, and G. Meneghesso, “Potential induced degradation of N-type bifacial silicon solar cells: An investigation based on electrical and optical measurements,” *Sol. Energy Mater. Sol. Cells*, vol. 168, pp. 51–61, 2017.

[120] M. D. Kempe, D. L. Nobles, L. Postak, and J. A. Calderon, “Moisture ingress prediction in polyisobutylene-based edge seal with molecular sieve desiccant,” *Prog. Photovoltaics Res. Appl.*, vol. 26, no. 2, pp. 93–101, 2018.

[121] S. Yamaguchi, A. Masuda, and K. Ohdaira, “Changes in the current density--voltage and external quantum efficiency characteristics of n-type single-crystalline silicon photovoltaic modules with a rear-side emitter undergoing potential-induced degradation,” *Sol. Energy Mater. Sol. Cells*, vol. 151, pp. 113–119, 2016.

[122] I. Devoto and A. Halm, “Comprehensive study of PID mechanisms for n-type bifacial solar cells,” in *Proceedings of the 36th European Photovoltaic Solar Energy Conference and Exhibition (EU PVSEC 2019), Marseille, France*, 2019, pp. 9–13.

[123] W. and Luo *et al.*, “Investigation of potential-induced degradation in n-PERT bifacial silicon photovoltaic modules with a glass/glass structure,” *IEEE J. Photovoltaics*, vol. 8, no. 1, pp. 16–22, 2017.

[124] K. Hara, K. Ogawa, Y. Okabayashi, H. Matsuzaki, and A. Masuda, “Influence of surface structure of n-type single-crystalline Si solar cells on potential-induced degradation,” *Sol. Energy Mater. Sol. Cells*, vol. 166, pp. 132–139, 2017.

[125] T. Ishii, S. Choi, R. Sato, Y. Chiba, and A. Masuda, “Potential-induced degradation

in photovoltaic modules composed of interdigitated back contact solar cells in photovoltaic systems under actual operating conditions," *Prog. Photovoltaics Res. Appl.*, vol. 28, no. 12, pp. 1322–1332, 2020.

[126] Y. Xu, A. Masuda, and K. Ohdaira, "Influence of light illumination on the potential-induced degradation of n-type interdigitated back-contact crystalline Si photovoltaic modules," *Jpn. J. Appl. Phys.*, vol. 60, no. SB, p. SBBF08, 2021.

[127] W. Luo *et al.*, "Investigation of polysilicon passivated contact's resilience to potential-induced degradation," *Sol. Energy Mater. Sol. Cells*, vol. 194, pp. 168–173, 2019.

[128] B. Bora *et al.*, "Accelerated stress testing of potential induced degradation susceptibility of PV modules under different climatic conditions," *Sol. Energy*, vol. 223, pp. 158–167, 2021.

[129] K. Hara, H. Ichinose, T. N. Murakami, and A. Masuda, "Crystalline Si photovoltaic modules based on TiO 2-coated cover glass against potential-induced degradation," *RSC Adv.*, vol. 4, no. 83, pp. 44291–44295, 2014.

[130] M. Kambe *et al.*, "Chemically strengthened cover glass for preventing potential induced degradation of crystalline silicon solar cells," in *2013 IEEE 39th Photovoltaic Specialists Conference (PVSC)*, 2013, pp. 3500–3503.

[131] J. Oh, G. TamizhMani, S. Bowden, and S. Garner, "Surface disruption method with flexible glass to prevent potential-induced degradation of the shunting type in PV modules," *IEEE J. Photovoltaics*, vol. 7, no. 1, pp. 62–67, 2016.

[132] G. Oreski *et al.*, "Designing new materials for photovoltaics: opportunities for lowering cost and increasing performance through advanced material innovations," 2021.

[133] O. K. Segbefia, A. G. Imenes, and T. O. Saetre, "Moisture ingress in photovoltaic modules: A review," *Sol. Energy*, vol. 224, pp. 889–906, 2021.

[134] G. Oreski *et al.*, "Properties and degradation behaviour of polyolefin encapsulants for photovoltaic modules," *Prog. Photovoltaics Res. Appl.*, vol. 28, no. 12, pp. 1277–1288, 2020.

[135] M. López-Escalante, L. J. Caballero, M. F, M. Gabás, A. a Cuevas, and J. Ramos-Barrado, "Polyolefin as PID-resistant encapsulant material in PV modules," *Sol. Energy Mater. Sol. Cells*, vol. 144, pp. 691–699, 2016.

[136] J. Berghold, S. Koch, B. Frohmann, P. Hacke, and P. Grunow, "Properties of encapsulation materials and their relevance for recent field failures," in *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)*, 2014, pp. 1987–1992.

[137] B. M. Habersberger, P. Hacke, and L. S. Madenjian, "Evaluation of the PID-s susceptibility of modules encapsulated in materials of varying resistivity," in *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC)(A Joint Conference of 45th IEEE PVSC, 28th PVSEC & 34th EU PVSEC)*, 2018, pp. 3807–3809.

[138] M. Barbato, M. Meneghini, A. Cester, A and Barbato, G. Meneghesso, G. Tavernaro, and M. Rossetto, "Potential induced degradation in high-efficiency bifacial solar cells," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, 2016, p. PV-2.

[139] J. Kapur, K. M. Stika, C. S. Westphal, J. L. Norwood, and B. Hamzavytehrany, "Prevention of potential-induced degradation with thin ionomer film," *IEEE J. Photovoltaics*, vol. 5, no. 1, pp. 219–223, 2014.

[140] E. Urrejola *et al.*, "bifiPV2020 bifacial workshop: a technology overview," 2020.

[141] "JinkoSolar: Transparent backsheet vs dual glass - Advantages and disadvantages," 2020. [Online]. Available: https://www.pv-tech.org/industry-updates/jinkosolar-transparent-backsheet-vs-dual-glass-advantages-and-disadvantages/. [Accessed: 25-Oct-2022].

[142] C. Buerhop, O. Stroyuk, T. Pickel, J. Hauch, and I. M. Peters, "Identification of solar module behavior originating from backsheet failure-from lab studies to field tests," in *2021 IEEE 48th Photovoltaic Specialists Conference (PVSC)*, 2021, pp. 0831–0834.

[143] R. Kopecek *et al.*, "Bifaciality: One small step for technology, one giant leap for kWh cost reduction," *Photovoltaics Int*, vol. 26, pp. 32–45, 2016.

[144] M. D. Kempe, A. A. Dameron, and M. O. Reese, "Evaluation of moisture ingress from the perimeter of photovoltaic modules," *Prog. Photovoltaics Res. Appl.*, vol. 22, no. 11, pp. 1159–1171, 2014.

[145] D. E. Mansour *et al.*, "Effect of backsheet properties on PV encapsulant degradation during combined accelerated aging tests," *Sustainability*, vol. 12, no. 12, p. 5208, 2020.

[146] O. A. Arruti, L. Gnocchi, Q. Jeangros, A. Virtuani, and C. Ballif, "Potential Induced Degradation Mechanism in Rear-Emitter Bifacial Silicon Heterojunction Solar Cells Encapsulated in Different Module Structures," in *2021 IEEE 48th Photovoltaic Specialists Conference (PVSC)*, 2021, pp. 2032–2036.

[147] W. Porter, "Bifacial modules: there are two sides to every solar panel." White Paper: Burn & McDonnell, 2019.

[148] J. Oh, B. Dauksher, S. Bowden, G. Tamizhmani, P. Hacke, and J. D'Amico, "Further

studies on the effect of SiNx refractive index and emitter sheet resistance on potential-induced degradation," *IEEE J. Photovoltaics*, vol. 7, no. 2, pp. 437–443, 2017.

[149] J. Ding *et al.*, "Light management of PERC solar cell with the front and back dielectric multilayers," *Prog. Photovoltaics Res. Appl.*, vol. 30, no. 2, pp. 180–190, 2022.

[150] S. Yamaguchi, B. B. Van Aken, M. K. Stodolny, J. Löffler, A. Masuda, and K. Ohdaira, "Effects of passivation configuration and emitter surface doping concentration on polarization-type potential-induced degradation in n-type crystalline-silicon photovoltaic modules," *Sol. Energy Mater. Sol. Cells*, vol. 226, no. February, p. 111074, 2021.

[151] T. Pu, H. Shen, K. H. Neoh, F. Ye, and Q. Tang, "Reduced power degradation in bifacial PERC modules by a rear silicon oxide additive layer," *Int. J. Energy Res.*, vol. 45, no. 6, pp. 8659–8665, 2021.

[152] S. Ma, H. Tang, Z. Li, X. Kong, and W. Shen, "Application of SiOxNy films in industrial bifacial PERC solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 230, p. 111199, 2021.

[153] M. K. Stodolny *et al.*, "PID-and UVID-free n-type solar cells and modules," *Energy Procedia*, vol. 92, pp. 606–616, 2016.

[154] J. Hylský, D. Strachala, P. Vyroubal, P. Čudek, J. Vaněk, and P. Vanýsek, "Effect of negative potential on the extent of PID degradation in photovoltaic power plant in a real operation mode," *Microelectron. Reliab.*, vol. 85, pp. 12–18, 2018.

[155] D. Lausch *et al.*, "Sodium outdiffusion from stacking faults as root cause for the recovery process of potential-induced degradation (PID)," *Energy Procedia*, vol. 55, pp. 486–493, 2014.

[156] J. Del Cueto and T. McMahon, "Analysis of leakage currents in photovoltaic modules under high-voltage bias in the field," *Prog. Photovoltaics Res. Appl.*, vol. 10, no. 1, pp. 15–28, 2002.

[157] S. Hoffmann and M. Koehl, "Effect of humidity and temperature on the potential-induced degradation," *Prog. Photovoltaics Res. Appl.*, vol. 22, no. 2, pp. 173–179, 2014.

[158] V. Naumann, O. Breitenstein, K. Ilse, M. Pander, K. Sporleder, and C. Hagendorf, "Increase of PID susceptibility of PV modules under enhanced environmental stress," 2020.

[159] A. Masuda *et al.*, "Influence of hygrothermal stress on potential-induced degradation for homojunction and heterojunction crystalline Si photovoltaic

modules," *Jpn. J. Appl. Phys.*, vol. 59, no. 7, p. 076503, 2020.

[160] P. Zhao *et al.*, "Mechanism analysis of potential-induced degradation of P-type crystalline Si solar cells," in *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, 2016, pp. 2756–2760.

[161] J. Berghold *et al.*, "PID: from material properties to outdoor performance and quality control counter measures," in *Reliability of Photovoltaic Cells, Modules, Components, and Systems VIII*, 2015, pp. 73–86.

[162] P. Hacke, P. Burton, A. Hendrickson, S. Spataru, S. Glick, and K. Terwilliger, "Effects of photovoltaic module soiling on glass surface resistance and potential-induced degradation," in *2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, 2015, pp. 1–4.

[163] M. A. Islam, M. Hasanuzzaman, and N. Abd Rahim, "Effect of different factors on the leakage current behavior of silicon photovoltaic modules at high voltage stress," *IEEE J. Photovoltaics*, vol. 8, no. 5, pp. 1259–1265, 2018.

[164] P. Hacke *et al.*, "Interlaboratory study to determine repeatability of the damp-heat test method for potential-induced degradation and polarization in crystalline silicon photovoltaic modules," *IEEE J. Photovoltaics*, vol. 5, no. 1, pp. 94–101, 2014.

[165] A. Masuda and Y. Hara, "Effect of light irradiation during potential-induced degradation tests for p-type crystalline Si photovoltaic modules," *Jpn. J. Appl. Phys.*, vol. 57, no. 8S3, p. 08RG13, 2018.

[166] D. C. Nguyen, Y. Ishikawa, S. Jonai, K. Nakamura, A. Masuda, and Y. Uraoka, "Elucidating the mechanism of potential induced degradation delay effect by ultraviolet light irradiation for p-type crystalline silicon solar cells," *Sol. Energy*, vol. 199, no. 55–62, 2020.

[167] K. Sporleder, V. Naumann, J. Bauer, D. Hevisov, M. Turek, and C. Hagendorf, "Time-resolved investigation of transient field effect passivation states during potential-induced degradation and recovery of bifacial silicon solar cells," *Sol. RRL*, vol. 5, no. 7, p. 2100140, 2021.

[168] J. Oh *et al.*, "Reduction of PV module temperature using thermally conductive backsheets," *IEEE J. Photovoltaics*, vol. 8, no. 5, pp. 1160–1167, 2018.

[169] F. ibne Mahmood, A. Kumar, M. Afridi, and G. Tamizhmani, "Potential induced degradation in c-Si glass-glass modules after extended damp heat stress," *Sol. Energy*, vol. 254, pp. 102–111, 2023.

[170] J. Carolus *et al.*, "Why and how to adapt PID testing for bifacial PV modules?," *Prog. Photovoltaics Res. Appl.*, vol. 28, no. 10, pp. 1045–1053, 2020.

[171] D. J. Colvin, E. J. Schneller, and K. O. Davis, “Cell dark current--voltage from non-calibrated module electroluminescence image analysis,” *Sol. Energy*, vol. 244, pp. 448–456, 2022.

[172] S. Suckow, T. M. Pletzer, and H. Kurz, “Fast and reliable calculation of the two-diode model without simplifications,” *Prog. photovoltaics Res. Appl.*, vol. 22, no. 4, pp. 494–501, 2014.

[173] F. ibne Mahmood *et al.*, “Susceptibility to polarization type potential induced degradation in commercial bifacial p-PERC PV modules,” *Prog. Photovoltaics Res. Appl.*, 2023.

[174] P. Hacke *et al.*, “Accelerated testing and modeling of potential-induced degradation as a function of temperature and relative humidity,” *IEEE J. Photovoltaics*, vol. 5, no. 6, pp. 1549–1553, 2015.

[175] S. Voswinckel, T. Mikolajick, and V. Wesselak, “Influence of the active leakage current pathway on the potential induced degradation of CIGS thin film solar modules,” *Sol. Energy*, vol. 197, pp. 455–461, 2020.

[176] P. Gebhardt, L. P. Bauermann, and D. Philipp, “Backsheet Chalking—Theoretical Background and Relation to Backsheet Cracking and Insulation Failures,” in *Proceedings of the 35th European Photovoltaic Solar Energy Conference and Exhibition, Brussels, Belgium*, 2018, pp. 24–28.

[177] S. Schulze, A. Apel, R. Meitzner, M. Schak, C. Ehrich, and J. Schneider, “Influence of polymer properties on potential induced degradation of PV-modules,” in *28th European Photovoltaic Solar Energy Conference*, 2013.

[178] S. Yamaguchi, C. Yamamoto, A. Masuda, and K. Ohdaira, “Influence of backsheet materials on potential-induced degradation in n-type crystalline-silicon photovoltaic cell modules,” *Jpn. J. Appl. Phys.*, vol. 58, no. 12, p. 120901, 2019.

[179] M. D. Kempe, “Modeling of rates of moisture ingress into photovoltaic modules,” *Sol. Energy Mater. Sol. Cells*, vol. 90, pp. 2720–2738, 2006.

[180] F. ibne Mahmood and G. Tamizhmani, “Impact of different backsheets and encapsulant types on potential induced degradation (PID) of silicon PV modules,” *Sol. Energy*, vol. 252, pp. 20–28, 2023.

[181] M. Jankovec, E. Annigoni, C. Ballif, and M. Topič, “In-situ determination of moisture diffusion properties of PV module encapsulants using digital humidity sensors,” in *2018 Ieee 7Th World Conference On Photovoltaic Energy Conversion (Wcpec)(A Joint Conference Of 45Th Ieee Pvsc, 28Th Pvsec & 34Th Eu Pvsec*, 2018, pp. 0415–0417.

[182] W. Luo *et al.*, “Investigation of Potential-Induced Degradation in Bifacial n-PERL

Modules," *IEEE J. Photovoltaics*, vol. 10, no. 4, pp. 935–939, 2020.

[183] L. Spinella *et al.*, "Chemical and mechanical interfacial degradation in bifacial glass/glass and glass/transparent backsheet photovoltaic modules," *Prog. Photovoltaics Res. Appl.*, 2020.

[184] J. Kuitche and G. TamizhMani, "Accelerated lifetime testing of photovoltaic modules solar America board for codes and standards," 2013.

[185] S. R. V. Tatapudi, "Potential induced degradation (PID) of pre-stressed photovoltaic modules: effect of glass surface conductivity disruption," Arizona State University, 20152.

[186] B. Bora *et al.*, "Mitigation of PID in commercial PV modules using current interruption method," in *Reliability of Photovoltaic Cells, Modules, Components, and Systems X*, 2017, pp. 89–94.

[187] G. TamizhMani and J. Kuitche, "Accelerated Lifetime Testing of Photovoltaic Modules Solar America Board for Codes and Standards," 2013.

[188] F. I. Mahmood and G. TamizhMani, "Impact of Anti-soiling Coating on Potential Induced Degradation of Silicon PV modules," in *2022 IEEE 49th Photovoltaics Specialists Conference (PVSC)*, 2022, pp. 1198–1200.

[189] J. Karas *et al.*, "Degradation of copper-plated silicon solar cells with damp heat stress," *Prog. Photovoltaics*, vol. 28, no. 11, pp. 1175–86, 2020.

[190] G. Cattaneo *et al.*, "Lamination process and encapsulation materials for glass–glass PV module design," *Photovoltaics Int.*, no. October, pp. 1–8, 2014.

[191] M. D. Kempe, "Control of moisture ingress into photovoltaic modules," in *Conference Record of the Thirty-first IEEE Photovoltaic Specialists Conference*, 2005, pp. 503–506.

[192] C. Peike *et al.*, "Origin of damp-heat induced cell degradation," *Sol. Energy Mater. Sol. Cells*, vol. 116, pp. 49–54, 2013.

[193] D. C. Jordan, C. Deline, M. Deceglie, T. J. Silverman, and W. Luo, "PV Degradation – Mounting & Temperature," in *2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)*, 2019, pp. 0673–0679.

[194] M. W. P. E. Lamers *et al.*, "Solar Energy Materials and Solar Cells Temperature effects of bifacial modules : Hotter or cooler?," *Sol. Energy Mater. Sol. Cells*, vol. 185, no. March, pp. 192–197, 2018.

[195] M. Köntges *et al.*, "Reviewing the practicality and utility of electroluminescence and thermography images," *Inst. Sol. Energy Res. Hamelin, Emmerthal, Ger.*, 2014.

[196] G. Coletti *et al.*, “Removing the effect of striations in n-type silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 130, pp. 647–651, 2014.

[197] J. Bauer, V. Naumann, S. Großer, C. Hagendorf, M. Schütze, and O. Breitenstein, “On the mechanism of potential-induced degradation in crystalline silicon solar cells,” *Phys. status solidi (RRL)–Rapid Res. Lett.*, vol. 6, no. 8, pp. 331–333, 2012.

[198] B. Li *et al.*, “Suppression of potential-induced degradation in monofacial PERC solar cells with gradient-designed capping layer,” *Sol. Energy*, vol. 225, no. May, pp. 634–642, 2021.

[199] W. Luo *et al.*, “Elucidating potential-induced degradation in bifacial PERC silicon photovoltaic modules,” *Prog. Photovoltaics Res. Appl.*, vol. 26, no. 10, pp. 859–867, 2018.

[200] A. G. Aber;e, S. Glunz, and W. Warta, “Field effect passivation of high efficiency silicon solar cells,” *Sol. Energy Mater. Sol. Cells*, vol. 29, no. 2, pp. 175–182, 1993.

[201] A. G. Aberle, S. Glunz, and W. Warta, “Impact of illumination level and oxide parameters on Shockley--Read--Hall recombination at the Si-SiO2 interface,” *J. Appl. Phys.*, vol. 71, no. 9, pp. 4422–4431, 1992.

[202] K. Sporleder, V. Naumann, J. Bauer, M. Turek, and C. Hagendorf, “Potential Induced Degradation Studies with high Temporal Resolution Reveal Changes of Field Effect Passivation States at the Rear Side of Bifacial Silicon Solar Cells,” in *2021 IEEE 48th Photovoltaic Specialists Conference (PVSC)*, 2021, pp. 0935–0938.