Application of WBG Devices in Power Converters: Topologies, Control, and

Hardware Design Considerations

by

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ABSTRACT

Wide-BandGap (WBG) material-based switching devices such as gallium nitride (GaN) High Electron Mobility Transistors (HEMTs) and Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) are considered very promising and valuable candidates for replacing conventional Silicon (Si) MOSFETs in various industrial high-frequency high-power applications, mainly because of their capabilities of higher switching frequencies with less switching and conduction losses. However, to make the most of their advantages, it is crucial to understand the intrinsic differences between WBG-based and Si-based switching devices and investigate effective means to safely, efficiently, and reliably utilize the WBG devices.

Firstly, a comprehensive understanding of traditional Modular Multilevel Converter (MMC) topology is presented. Different novel SubModule (SM) topologies are described in detail. The low frequency SM voltage fluctuation problem is also discussed. Based on the analysis, some novel topologies which manage to damp or eliminate the voltage ripple are illustrated in detail. As demonstrated, simulation results of these proposed topologies verify the theory. Moreover, the hardware design considerations of traditional MMC platform are discussed. Based on these, a 6 kW smart Modular Isolated Multilevel Converter (MIMC) with symmetrical resonant converter based Ripple current elimination channels is delivered and related experimental results further verify the effectiveness of proposed topology.

Secondly, the evolution of GaN transistor structure, from classical normally-on device to normally-off GaN, is well-described. As the benefits, channel current capability and drain-source voltage are significantly boosted. However, accompanying the evolution of GaN devices, the dynamic on-resistance issue is one of the urgent problems to be solved since it strongly affects the GaN device current and voltage limit.

Unlike traditional methods from the perspective of transistor structure, this report proposes a novel Multi-Level-Voltage-Output gate drive circuit (MVO-GD) aimed at alleviating the dynamic on-resistance issue from engineering point of view. The comparative tests of proposed MVO-GD and the standard 2-level gate driver (STD-GD) are conducted under variable test conditions which may affect dynamic on-resistance, such as drain-source voltage, gate current width, device package temperature and so on. The experimental waveforms and data have been demonstrated and analyzed.

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Chapter 1

INTRODUCTION

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1.1 Overview of Wide-band-gap (WBG) Power Devices

In modern industries, requirements for the performance of various power electronic based converters are becoming stricter in terms of capacity, voltage level, efficiency, and size (switching frequency related issues). In order to enhance the performance of existing power converters, replacing conventional Si switching devices with wide-band-gap (WBG) switching devices such as gallium nitride (GaN) high electron mobility transistors (HEMTs) and silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) is currently a popularly adopted method.
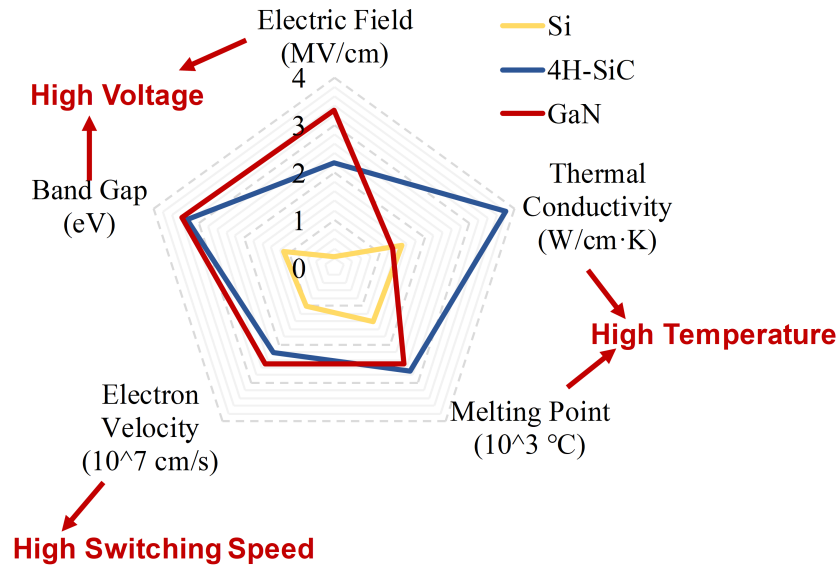
Figure 1.1: Si vs. SiC vs. GaN, the Material Characteristics Comparison.

WBG semiconductor materials offer superior characteristics to those of Si, as shown in Fig. 1.1. The respective merits of GaN and SiC lead to the advantageous

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adoption of GaN HEMTs for low (< 1 kW) to mid (< 10 kW) power applications and SiC MOSFETs for mid to high (> 10 kW) power applications in practical design scenarios, as shown in Fig. 1.2. The superiority of GaN HEMTs is yet to be fully utilized because they feature some form of heterogeneous integration with dissimilar substrate. This leads to large thermal boundary resistance between GaN and substrate, causing the self-heat issue, which may cause the switching device to overheat. However, GaN HEMTs offer the highest efficiency and switching speed, and SiC MOSFETs provide the highest voltage, current, and temperature capabilities. GaN's wide band gap allows power applications with voltages between 100 V and 600 V to use smaller, more efficient chips, reducing costs and energy consumptions. SiC, with higher thermal conductivity, is suited for the highest power applications that require large heat dissipation. Current flow is another critical difference. SiC is a 'vertical' device which is optimized for high power only, while commercial GaN has a 'lateral' structure that makes monolithic ('same chip') integration possible. The lateral structure enables GaN power ICs to integrate power FETs with drive, logic, protection, sensing and control.

The GaN HEMT is designed with a unique aluminum gallium nitride (AlGaN)/GaN heterojunction structure where two-dimensional electron gas (2DEG) is formed. The 2DEG allows large bidirectional current and yields extremely low on resistance. GaN HEMTs are currently divided into three types: depletion mode (D-mode), enhancement mode (E-mode), and cascode devices. The D-mode GaN HEMT, as shown in Fig. 1.3(a), is naturally on because of the 2DEG and can be turned off with negative gate-source voltage. The E-mode GaN HEMT, as shown in Fig. 1.3(b), is normally off because the 2DEG has been depleted by an additional P-doped layer of GaN or AlGaN on the gate, and it can be turned on with appropriate gate-source voltage. The cascode GaN HEMT, as shown in Fig. 1.3(c), is also normally off because it consists
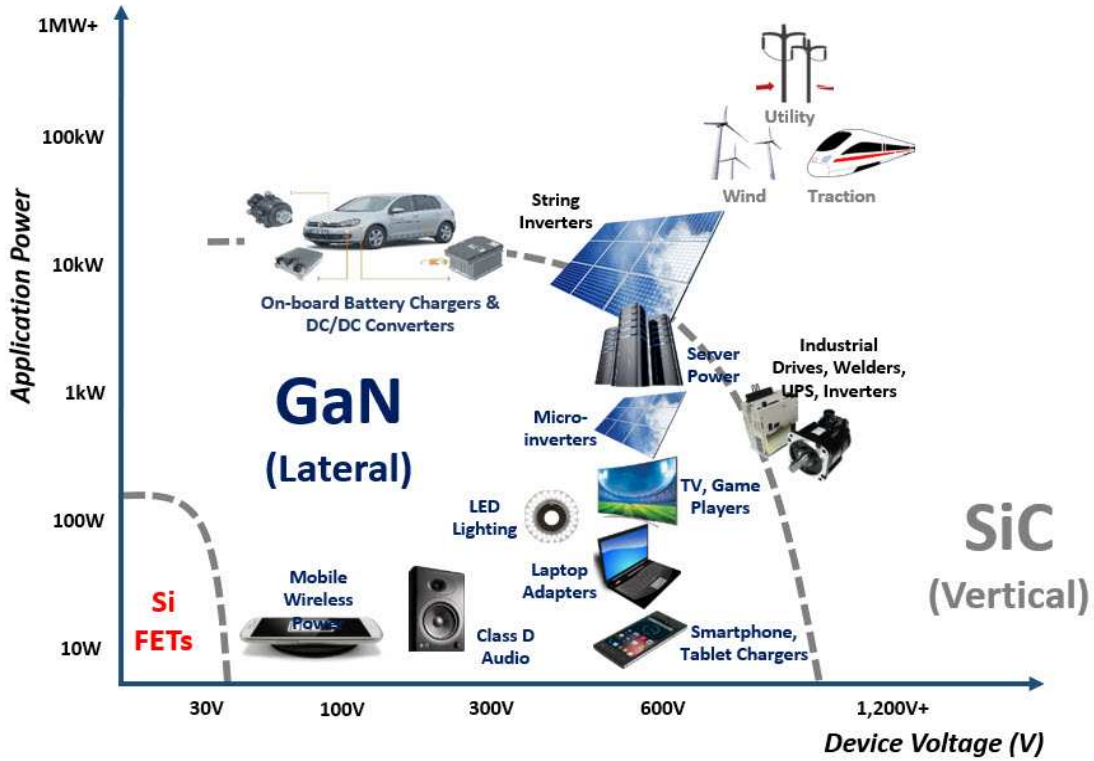
Figure 1.2: Landscape of WBG Devices [1].

of a D-mode GaN HEMT and an additional high-speed low-voltage Si MOSFET, and it can be turned on with appropriate gate-source voltage applied on the Si MOSFET. E-mode and cascode GaN HEMTs possess different characteristics mainly because of the additional Si MOSFET in the cascode device: the E-mode device offers lower on resistance, higher operating temperature, and no body diode, while the cascode device offers less strict driving requirements [5–9].
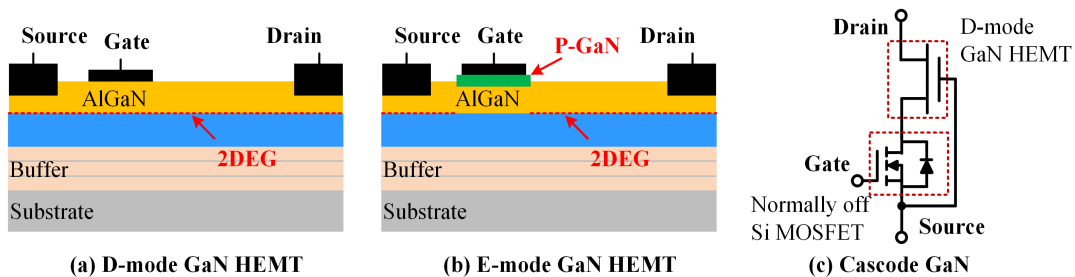
Figure 1.3: Structure of GaN HEMTs.

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The SiC MOSFET has a similar structure to that of Si MOSFET, as shown in Fig. 1.4, but the thickness can be made an order smaller because of SiC's higher voltage capability. This leads to much smaller on resistance (although not as small as that of the GaN HEMT). Additionally, the SiC MOSFET offers the highest power capability. The operation of the SiC MOSFET is the same as that of the Si MOSFET: with appropriate gate-source voltage, the device can be turned on, and the body diode is used for reverse conduction during off state [10].
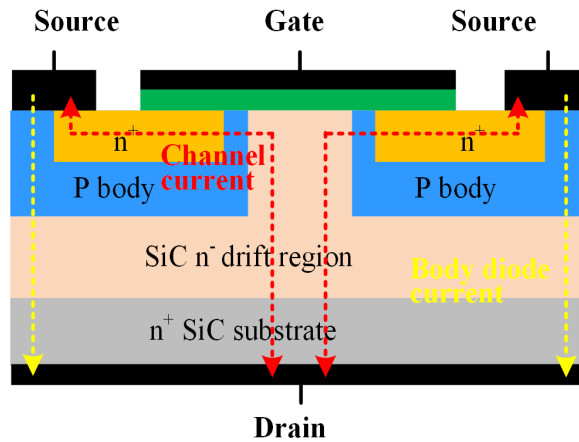
Figure 1.4: Structure of SiC MOSFETs.

The main challenge of using the WBG semiconductor switching devices is overcoming potential difficulties introduced from their high slew rates, which could worsen electromagnetic interference (EMI) level and may cause voltage oscillation and instability [5–9]. Besides, the high slew rates result in additional issues in some advanced applications, such as monolithic integration of GaN HEMTs and series-connected WBG devices. The following paragraphs will introduce the challenges when designing WBG devices based converters.

1.2 Overview of Modular Multilevel Converters

The high-power voltage source converters (VSCs) are taking higher and higher market share and faster developments compared with the current source and the matrix converters over the past decade [11–14]. Among them, the high-power modular multilevel converter (MMC) is widely accepted in industry and energy system since it features the low dv/dt, low expense for redundancy, small filter size, high modularity, excellent harmonic performance and high-power quality [15–19]. However, utilization of MMC in applications with variable frequency scenarios, such as adjustable speed drives, is not that popular due to the serious challenge induced from the normal operation of MMC [20–23].

One of the typical characteristics of MMC is the floating capacitor from each sub-module (SM), the voltage of which is controlled at its nominal value with limited fluctuation. This SM capacitor voltage control is fundamental and indispensable requirement to fulfill a high-performance close loop control for precise current output and high-power quality. However, due to the modulation strategies on the arms in general MMC control, the SM floating capacitor inevitably experiences wide voltage fluctuations induced by fundamental and second order circulating ripple current. Therefore, the switching devices in each SM are under high risk while the normal operation of MMC is also more or less affected. This problem is further exacerbated under low fundamental frequency region, which is kind of universal situation during the startup of a motor. In order to restrict the SM capacitor voltage ripple within acceptable range, the capacitance of each SM need to be large enough to compensate the highest voltage ripple under certain low frequency. Despite this, when the fundamental frequency is close to zero, the SM capacitor is still predictably forced to stand tremendous voltage ripple. Under this situation, simply increasing the capacitance

alone is no more a reasonable solution.

In recent years, many methods have been proposed to solve the SM capacitor voltage ripple issue at low frequency. One effective approach is low-frequency circulating current injection [24–26]. Second-harmonic circulating current is introduced and controlled to minimize the energy fluctuation. However, this injected low-frequency current significantly increases the device power loss as well as the current stress. High frequency circulating current injection is proved to be another good method [27–29]. The low-frequency voltage ripple or the energy fluctuations are shaped into high-frequency components and thus the SM capacitor can be charged or discharged at a faster speed. Therefore, the voltage ripple can be effectively damped and the required SM capacitance is reduced. However, besides the increased current stress and device conduction loss, another drawback of this method is the additional inducted common mode (CM) voltage at the motor terminals, which damages the motor.

Some novel topologies aimed at minimizing the low-frequency voltage ripple are also proposed [30–38]. Cross-connected channels are introduced to help absorb and balance the energy fluctuation between the upper arm and lower arm by properly controlling the flowing ac current in these channels [30, 31]. Based on these, horizon-connected channels built by DHBs are further proposed in [30] to replace the original cross-connected channels. The pulsating energy ripple in the three adjacent SMs can be eliminated as the vectoral low frequency current sum is zero. However, many extra active DHB control loops are added to the control strategy and thus increase control complexity.

In this report, a new horizon-connected ripple current elimination approach based on CLLC circuit is proposed for variable-speed drives. The three SMs on same level but from three phase legs are connected to a common capacitor through a high-frequency half-bridge CLLC channel. As a result, the arm current flows into the

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CLLC channel instead of the original SM capacitor. On the secondary side, the current converges at the common capacitor and then get cancelled each other because the vectoral sum of the current is zero. On the other hand, the SM capacitor supports the dc-link voltage of the CLLC stage on the primary side while the common capacitor plays the same role on the secondary side. Therefore, the three SM capacitors are coupled together through the bidirectional CLLC stages, by which the energy-exchange enables a dynamic voltage-balance state between these three SMs. That is, the unexpected low-frequency energy ripples induced from both fundamental and second-order harmonic current almost disappears and the SM capacitance is significantly reduced.

1.3 Challenges of Dynamic On-resistance of Discrete Gallium Nitride (GaN) Transistors

Gallium Nitride (GaN) is a high-performance transistor using GaN and AlGaN semiconductor materials grown on top of a Si substrate [39]. The lateral device structure features very low gate and output charge, fast switching and no body diode thus zero reverse recovery charge [40]. Therefore, GaN transistors show outstanding advantages on high switching frequency high power density applications, especially the High-electron-mobility transistors (HEMTs) are the most widely utilized GaN transistors [39–43]. However, in addition to the exciting device characteristics, the increasing dynamic on-resistance issue under high drain-source voltage also becomes a serious technical issue on GaN devices, the root-cause of which is reported as electron trapping effect [3, 44, 45].

When high drain-source voltage is applied on the device, large vertical electrical field drops between the drain terminal and the device substrate. Generally, there are two kinds of this substrate voltage bias: static substrate voltage bias and dynamic

substrate voltage bias [46]. For discrete device, the substrate of device is tied to the source terminal to maximally avoid the substrate bias, as proposed by the GaN manufacture [47, 48]. When the GaN device switches from off-state to on-state, the substrate bias effect can be observed. Although the drain-source voltage is reset to zero, the trapped electrons in the buffer layer are not released immediately [46]. Thus, the device on-current carrying capability by two-dimensional electron gas (2DEG) is reduced and manifested as increasing dynamic on-resistance issue, which is also called current collapse in some papers [49–51].

Some effective approaches aimed at solving the dynamic on-resistance issue from transistor semiconductor structure angle have been proposed [51–53]. Additional p-GaN region doped right beside the drain terminal of device enables the hole injection [49]. This method is proved to be effective on releasing the trapped electrons and reducing the device dynamic on-resistance. Optimizing device buffer layer is another good choice from device fabrication angle to help alleviate the electron trapping effects [53].

However, although so many excellent ideas have been proposed to optimize the GaN device structure, the dynamic on-resistance issue is yet not able to be fully eliminated. Since the increasing dynamic on-resistance, R_{dson}, is an important impact factor in converter design when considering the system efficiency and cooling system size, proper strategies to reduce the R_{dson} based on current available commercial GaN devices from engineering point of view are also very necessary to be explored, such as suitable gate drive profile. A well-customized gate drive profile called Multi-level Voltage Output Gate Drive (MVO-GD) will be discussed in later sections, which manages to inject plenty of additional holes through the gate channel into the device to increase the electrons density in 2DEG region. In this method, a large but short current pulse is generated to finish the hole injection when the turn-on signal comes.

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Then, the gate current drops till a very small value for the rest on period.

1.4 Dissertation Outline

Chapter 2 presents a comprehensive description of Modular Multilevel Converters (MMs) including the classical topology and general control strategies. The high SubModule (SM) capacitor voltage fluctuation under low system operating frequency is discussed. Some novel topologies aimed at solving this problem are introduced and described in detail, which are also validated using PLECS. Moreover, the hardware development of a traditional MMC platform and a 6 kW newly proposed MIMC platform are also presented.

Chapter 3 investigates the state-of-the-art discrete GIT GaN HEMTs fabricated by Infineon Technologies. Gallium Nitride high-electron-mobility transistors (GaN-HEMTs) have been widely investigated in high-frequency and high-efficiency applications in the voltage range up to 600 V due to its excellent characteristics featured from lateral transistor structure, such as very low gate and output charge, fast switching and no body diode or reverse recovery charge. However, GaN-HEMTs suffer from trapping effects induced by high drain source voltage bias, which results in abnormal dynamic on-resistance increasement. Unlike traditional methods from the perspective of transistor structure, this report proposes a novel multi-level Voltage Output gate drive circuit (MVO-GD) aimed at alleviating the dynamic on-resistance issue from engineering point of view. The comparative tests between proposed MVO-GD and the standard 2-level gate driver (STD-GD) are conducted under variable test conditions which may affect dynamic on-resistance, such as drain-source voltage, gate current width, device package temperature and so on. The experimental waveforms and data have been demonstrated. The on-resistance can be improved as much as 15% - 20%. Moreover, the new gate drive strategy has also been verified through

efficiency tests on 2 kW buck converter and 2.5 kW PFC Platform. The results show that the efficiency improvement is as large as 0.13% on buck converter while 0.18% on PFC platform.

Conclusions and future work are given in Chapter 4.

CHAPTER 2: SMART MODULAR ISOLATED MULTILEVEL CONVERTER (MIMC) WITH CLLC BASED RIPPLE CURRENT ELIMINATION CHANNELS

In this Chapter, a comprehensive understanding of traditional MMC topology is presented. Different novel SM topologies are described in detail. The low frequency SM voltage fluctuation problem is also discussed. Based on the analysis, some novel topologies which manage to damp or eliminate the voltage ripple are illustrated in detail. As demonstrated, simulation results of these proposed topologies verify the theory. Moreover, the hardware design considerations of a traditional MMC platform are discussed. Based on these, a 6 kW smart modular isolated multilevel converter (MIMC) with CLLC based Ripple current elimination channels is delivered and related experimental results further verify the effectiveness of proposed topology.

2.1 Overview of Modular Multilevel Converter (MMC)

Typical future requirements at the system level include: (1) inherent redundancy to make the availability of the whole power electronics system extremely high; (2) modular design to improve the scalability of the power converter; eliminating large passive filters; (3) eliminating bulky transformers; real power exchange from several systems through a common dc link. To overcome these challenges, the high-power voltage source converters (VSCs) are taking higher and higher market share and faster developments compared with the current source and the matrix converters over the past decade due to the problems of CSC and matrix converter such as resonances, non-controllable reactive currents, unclamped device voltage, requirement for reverse

blocking semiconductors [11–14]. As a result, to fulfill the future requirements for the converter, the essential improvement of VSC and multilevel VSC is the most critical point. The main issues to be improved are summarized as: the requirement of high-pulse frequencies and, in consequence, high dv/dt of the semiconductors; the danger of short circuits at the dc side causing extremely high surge currents; the unfavorable, slow dynamic behavior of dc voltage controllability; the complex construction and lack of scalability when increasing the voltage or power range. To address these problems, the high-power modular multilevel converter (MMC) is widely accepted in industry and energy system since it features the low dv/dt, low expense for redundancy, small filter size, high modularity, excellent harmonic performance and high-power quality [15–19]. Except these, it also presents the following unique features: (1) the internal arm currents flow continuously and can be controlled to a given value; (2) the distributed stray inductances and chokes in the converter arms will not affect the converter operation. Oppositely, certain level of inductance is necessary to limit high frequency circulating currents; (3) the elimination of dc-link capacitor will eliminate the danger of huge dc-link capacitor discharging current while dc short circuit fault happens; (4) the dc bus voltage is controlled by the converter quickly and directly. Thus, the instantaneous real power flow is controlled better and faster.

Fig. 2.1 shows a classical topology of a three phase MMC system. The MMC consists of two arms per phase leg, which is normally named as upper am and lower arm. The dc source system is connected to the upper and lower arms of each phase leg and the three phase ac system is connected to the middle point of each phase. Each arm, either upper or lower arm, is formed by n series connected sub-modules (SMs) and an arm inductor L to suppresses the circulating current. The arm inductor can limit the inrush current during the pre-charge procedure or caused by the voltage step change between arms. As the SMs in each arm can be controlled to kick in or

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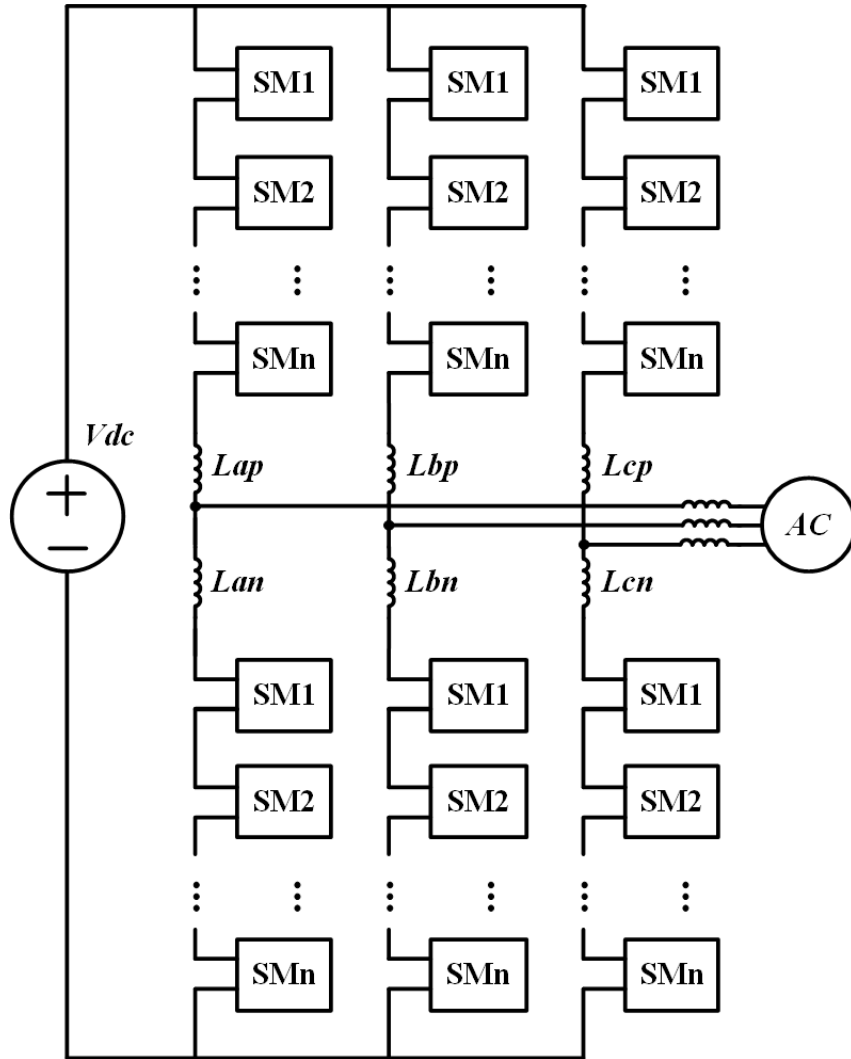
Figure 2.1: Traditional MMC Topology.

bypass to generate required voltage, the MMC is able to convert the input dc voltage into a multilevel ac voltage according to appropriate modulation method. The total capacitor voltage of inserted modules, including both upper and lower arms, is equal to the dc link voltage. The output voltage is generated by subtracting the dc-link positive voltage by the total capacitor voltage of the inserted modules in the upper arm. The energy stored in each arm increases when the current flows in positive direction and charges the capacitor. In the same way, the energy decreases when the

negative current flows in and discharges the capacitor. The energy variation ideally remains zero at the end of the period under fundamental frequency, however, it has a fundamental frequency ripple. The energy ripple results in the voltage variation on the module capacitor, thus the capacitance should be large enough to constrain the voltage ripple within a limit. The arm inductor helps to limit the inrush current caused by the instantaneous voltage difference between the arms. Also, it minimizes the magnitude of ac circulating current in MMC.

2.1.1 MMC Submodule Topology
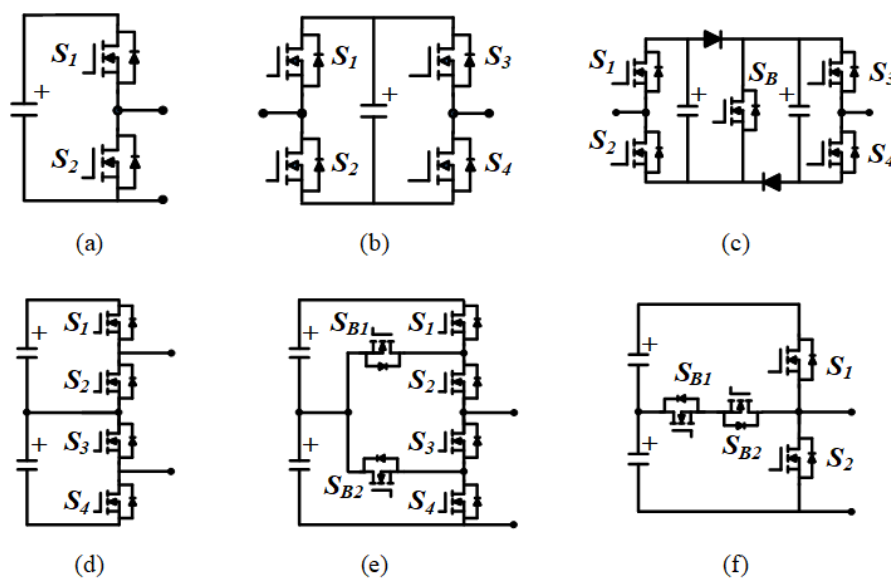
Figure 2.2: MMC SM Topologies. (a) HB;(b) FB;(c) CD;(d) CHB;(e) NPC;(f) NPP.

Many topologies of Sub-Modules (SMs) have been proposed to meet different requirements such as half-bridge submodule (HB-SM), full-bridge submodule (FB-SM), the clamped double submodule (CD-SM), cascaded H-bridge submodule (CH-SM) which are the most popular configurations among them, shown in Fig. 2.2. The half-bridge submodule (HB-SM) consists of two switches, which is the simplest to generate two level unipolar output voltage: $+V_{dc}$ and 0, as it chops the SM capacitor

voltage [14, 15]. Also, this cell provides bidirectional current flowing. The major advantage is its simple design structure and easy control. Whats more, only one device will be activated under normal operation. Hence this cell has low power loss and high efficiency. However, the major disadvantage of this cell is that it is unable to deal with the dc fault blocking. Unless an antiparallel connection of thyristors is applied across the ac output terminals to limit the fault current.

The full-bridge submodule (FB-SM), as shown in Fig. 2.2(b), has been deeply studied and widely applied [14, 15]. The FB-SM consists of two sets of half bridge switches. Each set of bridge switches in complimentary way. This cell can carry bidirectional current and provide bipolar output voltage. Therefore, it can theoretically generate three voltage levels: $+V_{dc}$, 0, -V_{dc}. Under this configuration, the dc fault blocking can be eliminated using the negative voltage. Also, the major salient advantage compared with the HB-SM is that it generates smaller voltage ripple. However, this cell requires twice the switches under same submodule rating, which leads to higher cost. Whats worse, two switches are activated under normal condition which results in higher power loss and lower efficiency.

The clamp-double submodule (CD-SM), shown in Fig. 2.2(c), consists of two sets of half bridge switches, two more clamp diode and one normally on switch with anti-parallel diode. The CD-SM is realized by connecting two HB-SMs in series along with two additional diodes and a single IGBT device as shown in Fig. 2.2(c). During the normal operation, the device S_B is continuously in ON state and resulting in a cascade connection of two HB-SMs. When a dc fault occurs, all the devices in CD-SM are turned OFF, and it generates positive or negative voltage levels at the output, depending on the current direction. Hence, the CD-SM can be used in the HVDC applications to block the dc-side fault current [54, 55]. However, the power losses, efficiency, and design complexity are significantly high due to the additional devices.

Several hybrid SMs are developed to handle the dc faults, to improve the efficiency with less device count, and to achieve the better capacitor voltage controllability [56–63]. These SMs are still in the research and development stage, yet to implement in the commercial products.

The cascaded H-bridge submodule (CH-SM) is kind of multilevel SubModule, in which two series connected switches form the bridge leg instead of alone one, as shown in Fig. 2.2(d). This cell generates three voltage levels like FB-SM. However, it provides lower device power loss and high efficiency compared with FB-SM, just like FB-SM [17, 18]. Currently, the CH-SM is commercially used in the MMC-based motor drive systems [64].

The 3L-NPC-SM, as shown in Fig. 2.2(e), is constructed with four semiconductor devices, two clamping diodes, and two capacitors. The loss distribution between the devices and the neutral-point voltage balance are the major issues in the NPC-SM [65]. Due to the neutral-point balancing issue, the operating region of NPC-SM is limited at the higher modulation indices [66]. The NPC-SM has higher device power losses and low efficiency compared with the HB-SM. From the control and design perspective, the NPC-SM is not an attractive solution for the MMC.

Another variation of a three-level SM is a Neutral-Point Piloted SubModule (3L-NPP-SM) and its configuration is shown in Fig. 2.2(f). In NPP configuration, the neutral point is connected to the output terminal through an anti-series connection of IGBT devices. Also, the devices in each leg should be designed with two times the voltage blocking capability of the NPC and ANPC SMs [67]. The NPP-SM generates three positive voltage levels only. This SM is not suitable for the bipolar operation and cannot block the dc fault current.

2.1.2 Mathematical Modeling of MMC

The simplified equivalent model of a three-phase MMC is shown in Fig. 2.3, in which each arm is modeled as equivalent voltage source which composes of different voltage components. In traditional HB-MMC, there are six arm converters. The arm currents are composed of a complex mixture of the ac side three phase currents, dc-link current and circulating currents flowing internally within the converter structure. Due to mutual interconnections, each arm converter voltage affects the current of all converters and external ports. To achieve precise control of power exchange between the ac grid and dc-link as well as energy balance among the submodule capacitors, it is of interest to decompose the original arm current into several new components attributed to particular power exchange.
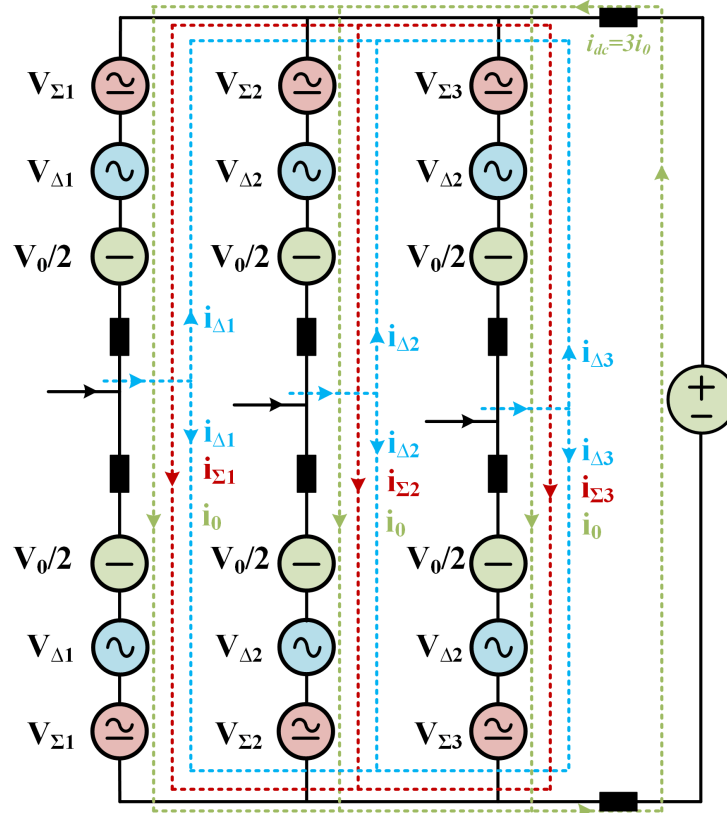
Figure 2.3: Equivalent Circuit Model of MMC.

These new current components generally create three decoupled subsystems related to the energy exchanges among the arm converters, ac and dc terminals and energy exchanges among the arm converters themselves. Assuming normal operation of the converter with no common mode currents on either ac or dc side, the basic equations according to Kirchhoffs Current Law (KCL) related to the converter topology are:

$$i_\mathrm{a} + i_\mathrm{b} + i_\mathrm{c} = 0 \tag{2.1}$$

$$i_\mathrm{abc} = i_\mathrm{abc,up} - i_\mathrm{abc,low} \tag{2.2}$$

$$i_\mathrm{dc} = i_\mathrm{a,up} + i_\mathrm{b,up} + i_\mathrm{c,up} = i_\mathrm{a,low} + i_\mathrm{b,low} + i_\mathrm{c,low} \tag{2.3}$$

The six converter arm currents can be split into five new components which are classified in following three types according to the path they are flowing in. (1) Asymmetrical or differential mode current space vector (two independent components, flowing in opposite directions in upper and lower arm converters) related to the grid current and exchange of energy between the arm converters and ac grid. (2) Symmetrical or circulating mode current space vector (two independent components, flowing in same direction in upper and lower arm converters) which is related to internal current power exchange between phases/arms. (3) Common mode current (single component) related to the dc link current and power exchange between the arm converters and the dc-link. The differential mode current vector is driven by an arm voltage space vector demonstrated in Fig. 2.4.

In the Laplace domain, it can be estimated using equation Eq. 2.4 and the corresponding equivalent block diagram is shown in Fig. 2.5.

$$I(s) = \frac{V_\mathrm{s}(s) + V_\Delta(s)}{s(L_\mathrm{g} + \frac{L_\mathrm{arm}}{2})} \tag{2.4}$$

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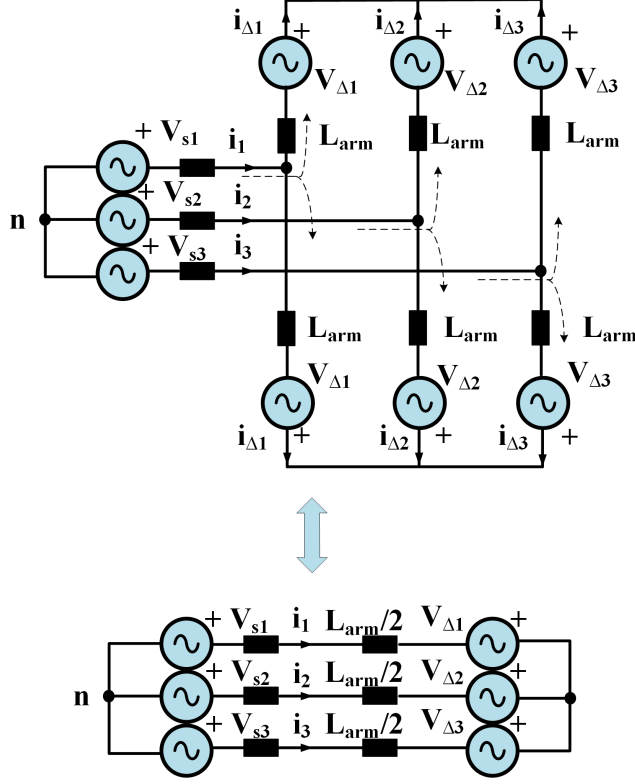
Figure 2.4: Equivalent Scheme for Differential Asymmetric Components.
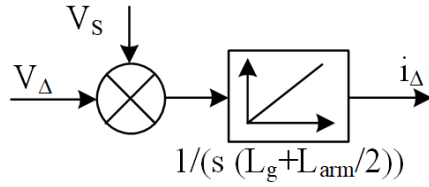
Figure 2.5: Equivalent Block Diagram for Ac Side Current calculation.

The symmetrical (circulating) mode current space vector can be calculated as:

$$i_\Sigma = \frac{i_{\text{up}} + i_{\text{low}}}{2} \tag{2.5}$$

$$V_\Sigma = \frac{V_{\text{up}} + V_{\text{low}}}{2} \tag{2.6}$$

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These new vectors are called symmetrical mode vectors as they act is same directions in the upper and lower arms. As the consequence these current components constituting this vector are circulating within the converter. The circulating current and voltage vectors can be mutually interlinked via the equivalent circuit shown in Fig. 2.6 and the control diagram shown in Fig. 2.7.
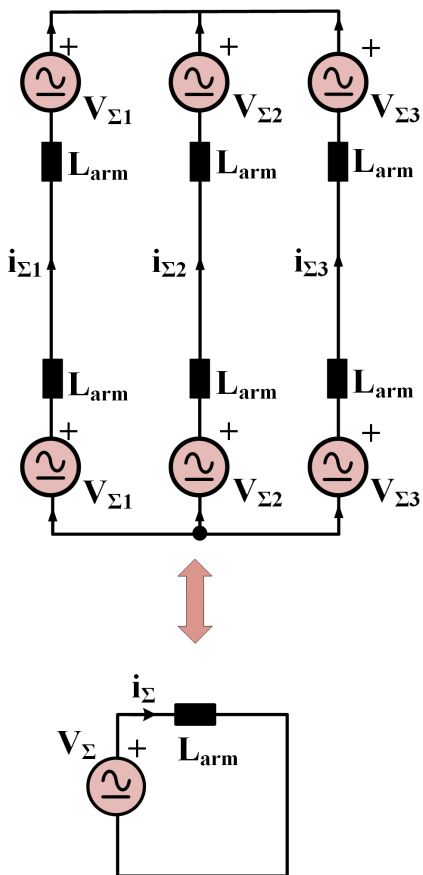
Figure 2.6: Equivalent Scheme for Circulating Symmetrical System.

In normal operation the circulating currents may have complex spectrum, dominated by the dc component, fundamental and second harmonic. The circulating currents should be ideally suppressed to zero. But they play a crucial role in transfer of energy between the arms and thus they should be carefully controlled in order to maintain arm dc bus voltages. The common mode current components of the upper

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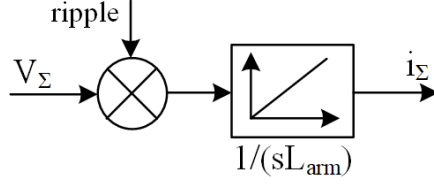
Figure 2.7: Block Diagram of the Circulating Current Model.

and lower arms are:

$$i_{0,\text{low}} = \frac{i_{\text{a,low}} + i_{\text{b,low}} + i_{\text{c,low}}}{3} = \frac{i_{\text{dc}}}{3} \tag{2.7}$$

$$i_{0,\text{up}} = \frac{i_{\text{a,up}} + i_{\text{b,up}} + i_{\text{c,up}}}{3} = \frac{i_{\text{dc}}}{3} \tag{2.8}$$

The common mode voltage components of the upper and lower arms are:

$$v_{0,\text{low}} = \frac{v_{\text{a,low}} + v_{\text{b,low}} + v_{\text{c,low}}}{3} \tag{2.9}$$

$$v_{0,\text{up}} = \frac{v_{\text{a,up}} + v_{\text{b,up}} + v_{\text{c,up}}}{3} \tag{2.10}$$

The sum of the two voltage is:

$$v_0 = v_{0,\text{up}} + v_{0,\text{low}} \tag{2.11}$$

Fig. 2.8 presents the equivalent scheme for the common mode current and voltage. In Laplace domain, the following transfer function can be derived:

$$I_{\text{dc}}(s) = \frac{V_0(s) + V_{\text{dclink}}(s)}{2L_{\text{dc}} + \frac{2}{3}L_{\text{arm}}} \tag{2.12}$$

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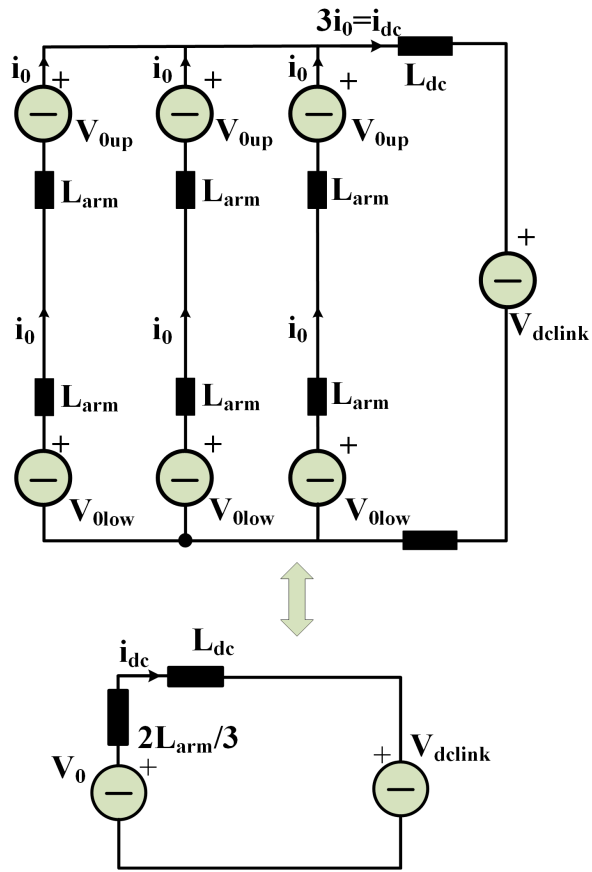
Figure 2.8: Equivalent Scheme for the Common Mode System.
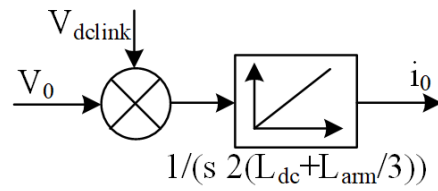
Figure 2.9: Block diagram of the Dc-link Current Model.

The corresponding equivalent block diagram described in Fig. 2.9.

In conclusion, the common mode voltage/current component is responsible for building of the dc-link voltage across the converter dc terminals and building the total dc current. The common mode voltage and current components are identical in all arms. As the consequence, the common mode sub-system is fully decoupled from the asymmetrical and symmetrical sub-systems. Combining the driving voltage for the differential mode, common mode and circulating current components discussed above, an integrated equivalent circuit model can be derived as already presented in Fig. 2.3. The addition of the three equivalent voltages will become the voltage command for the arm converter.

2.2 Classical Control Method for MMC

2.2.1 MMC Outer Energy Control Loops

The command of each current command of the three current components is generated from the energy loop. The differential mode current will affect the energy balance between the upper and lower arm. The circulating current will affect the energy balance among the three phase legs. The common mode current is controlled by the total energy balance of the converter. So, three energy control loops described as follows serves as the outer loop for the current loops.

(1) **Total Energy Control Loop**: Total energy loop regulates the power balance between dc bus side and ac output side, in which the dc current reference is generated for further inner current loop. The control diagram is shown in Fig. 2.10. The total energy is calculated by adding up all the SMs stored energy. A PI block is utilized to get the required dc current reference and a nominal dc current value is added in the loop as a feedforward to accelerate the control.

$$E_{tot} \rightarrow \oplus \rightarrow \boxed{PI} \rightarrow \boxed{\diagup} \rightarrow \oplus \rightarrow I_{dc\_ref}$$

$$E_{tot\_fbk} \qquad\qquad I_{dc\_nom}$$
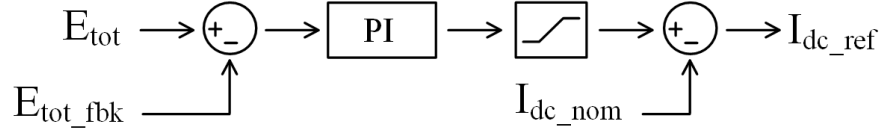
Figure 2.10: Total Energy Control Loop.

(2) **Phase Energy Control Loop**: Phase energy loop is utilized to control the energy balance between three phase legs, which is distorted by the common mode circulating current flowing among them. The control diagram is shown in Fig. 2.11. The phase leg energy is calculated by adding the upper arm energy and lower arm energy in each phase leg. This energy control gives the common mode circulating current reference for following circulating current control loop.

$$2E_{nom} \rightarrow \oplus \rightarrow \boxed{PI} \rightarrow \boxed{\diagup} \rightarrow I_{cir\_com\_ref}$$

$$E_p+E_n$$
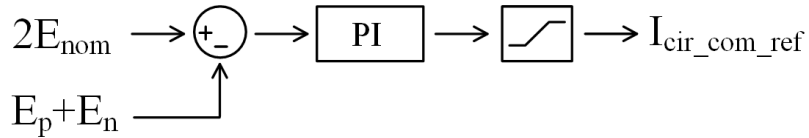
Figure 2.11: Phase Energy Control Loop.

(3) **Arm Energy Control Loop**: The main function of arm energy loop is to restrict the energy difference between the upper arm and lower arm. The excess arm energy divergence induces additional circulating current between arms and further distorts the current quality. As shown in Fig. 2.12, the subtraction of upper and lower arm energy is sent into the PI controller and the generated reference is added into the circulating current control loop.

$$0 \rightarrow \oplus \rightarrow \boxed{PI} \rightarrow \boxed{\diagup} \rightarrow I_{cir\_diff\_ref}$$

$$E_p-E_n$$
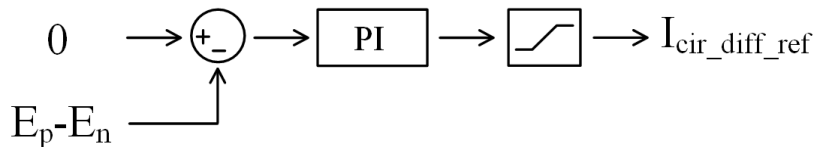
Figure 2.12: Arm Energy Control Loop.

2.2.2 MMC Outer Energy Control Loops

As discussed in previous subsection, the references for current control loops are already generated from the energy loops. The next thing is to find the appropriate circuit model to provide the plant for different current control loops. The equivalent circuit model shown in Fig. 2.3 tends to be the chosen one to illustrate MMC inner current control loops. The individual loops between each current and its corresponding voltage are already illustrated in Fig. 2.4, 2.6 and 2.8. In the Fig. 2.3, the SMs in each arm are replaced by three controlled voltage source which are responsible to their corresponding current components:

(1) **dc current Control Loop**: Each phase leg of MMC is modulated to generate required output power. That is to say, all the SM capacitors are inevitably discharged to provide the output power and thus the voltage will keep dropping without supplement. Therefore, the dc bus needs to inject sufficient dc current into these SMs to charge these capacitors and pull the reduced SM voltage back to its nominal level. Another PI control block is used as shown in Fig. 2.13. The reference comes from the discussed total energy loop and a voltage feedforward of rating dc bus voltage is implemented.

(2) **Output Current Control Loop**: The output current mainly comes from the fundamental component of arm current. The detailed the control diagram is shown in Fig. 2.13. The whole control is transferred to d-q frame and the PLL block is utilized to synchronize with the grid. The current reference in d-axis and q-axis control the real and reactive power, respectively.

(3) **Circulating Current Control Loop**: TThe undesired circulating current increase the peak/RMS value of the arm current, which consequently increases

the rating of devices, device power losses, and the SM voltage ripple. Although well designed arm inductors help suppress the circulating current, precise control strategy is the essential method to thoroughly solve the problem. The primary goal of circulating current control is to limit the pulsating second and forth order harmonics in the arm converter, which are the major components in arm current. The added arm inductors provide control freedoms for all six arms. As shown in Fig. 2.13, a PR controller based integrated controller are utilized to help suppress or reshape the circulating current.

In summary, the complete control diagram is summarized and shown in Fig. 2.13.
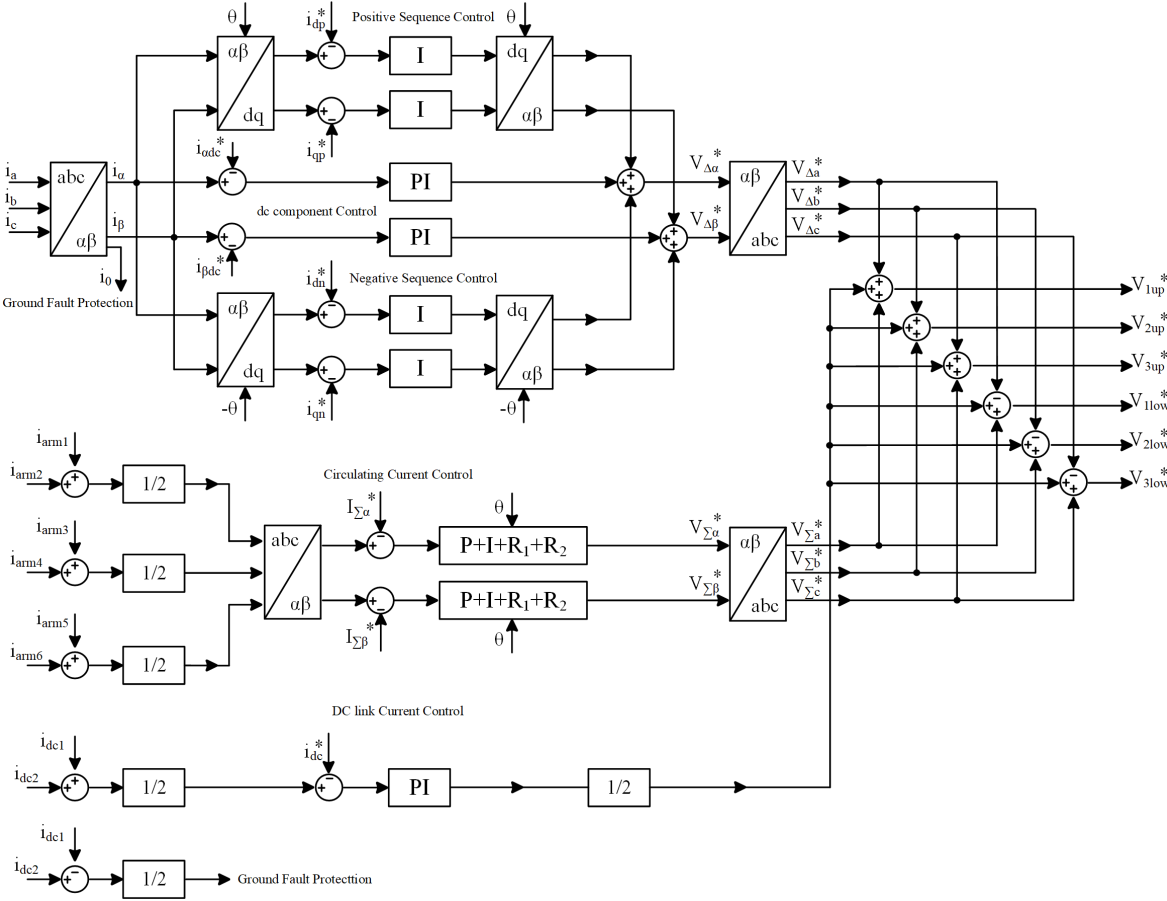
Figure 2.13: Integrated Control Strategy.

2.2.3 Capacitor Voltage Balance Control

The SM capacitor voltage balance control is involved to ensure that the stored energy is equally distributed in all the SMs. On the other word, each SM capacitor voltage is regulated at the same value. This means a lot for the MMC to achieve low THD and high power-quality. Based on the capacitor voltage balancing, the capacitor voltage control methods are categorized into distributed and centralized control approaches, as shown in Fig. 2.14. In distributed control, each SM capacitor voltage is regulated around the nominal value by voltage balance control, which generates a comparison signal integrated in the modulation signal of each SM. The distributed control only appears in PSC-PWM based MMC [68–70] and presents good controllability.
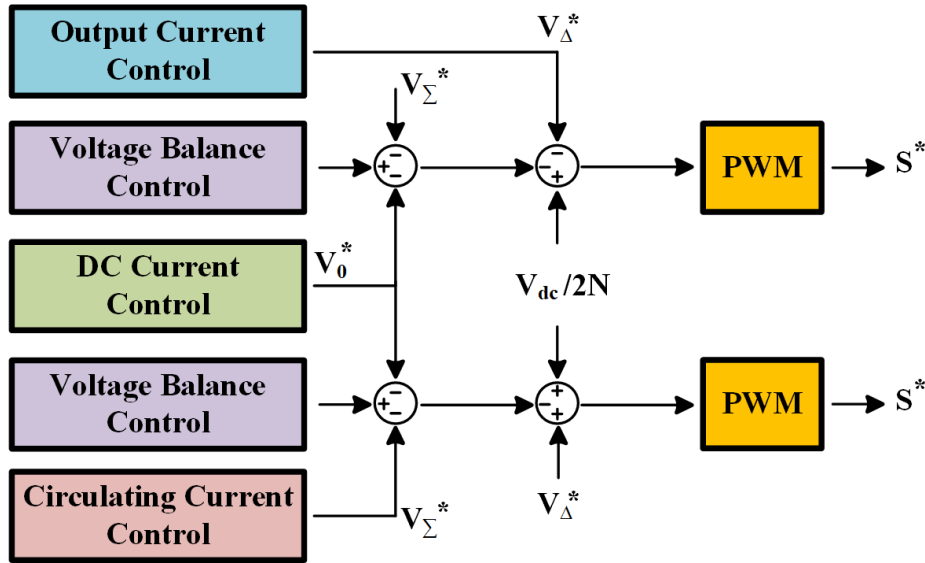
Figure 2.14: Block Diagram of Distributed Voltage Balance Control.

The block diagram of centralized control is shown in Fig. 2.15. In this method, a certain number of SMs out of N SMs in an arm are selected to generate the required voltage level. Therefore, this control method is more like a SM selection method. The

good point of this one is that it can be compatible with many modulation strategies such as PSC-PWM, LSC-PWM, NLM and so on [71–74].
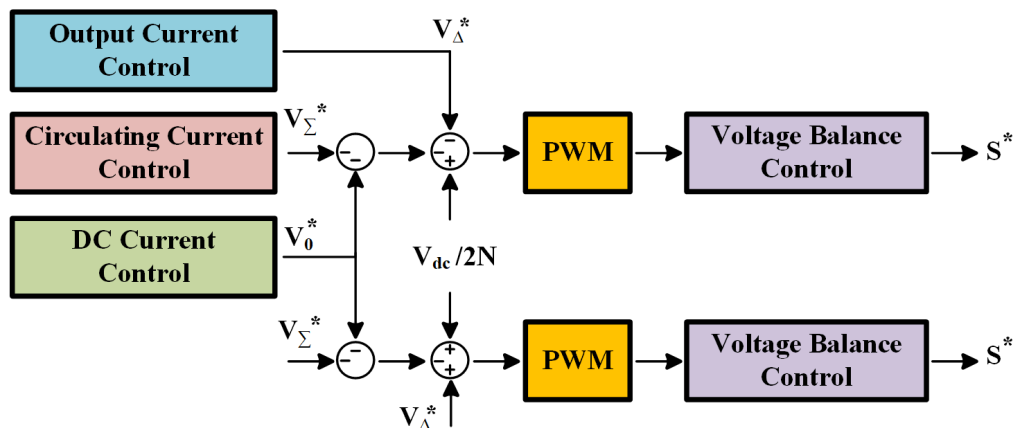
Figure 2.15: Block Diagram of Centralized Voltage Valance Control.

The simplest way to balance the SM capacitor voltage is by the periodical rotation of gating signal pattern based on the phase voltage switching state redundancy [75]. However, this method is difficult to apply for MMC with a large number of SMs per arm. Other hand, the capacitor voltage balance can be achieved by adjusting the duration of PWM gating pulses in the real-time [76, 77]. These approaches can be implemented with the PSC-PWM scheme only.

The sorting based voltage balance control is developed to regulate the SM capacitor voltage. In this approach, the SM capacitor voltage is normalized with respect to their nominal voltage. The normalized capacitor voltage is compared with other capacitors voltage. The output of each comparison is added together, which results in a virtual index number. These virtual index numbers are rearranged in either ascending or descending order based on the direction of the arm current. When the arm current is positive, the SMs with the lowest voltage is chosen to be inserted to let them charge and avoid any overcharging of those capacitors with the highest voltages and vice-versa [73, 74, 78, 79]. The resultant index numbers are compared with the

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reference index number, which gives an ON and OFF state of the SM. These states are applied to the SMs in each PWM period [66, 80].

2.3 Simulation of Traditional MMC Topology

In this section, the MMC simulation results are demonstrated and the system specifications are shown in the Table 2.1 below.

Table 2.1: System Specifications of 150 kW MMC Simulation.

Parameters	Values
AC output voltage	1500 V
AC output frequency	150 Hz
DC link voltage	3 kV
Arm inductance	2 mH
Grid inductance	0.1 mH
SM capacitance	300 μF
Number of SMs per arm	3
Sampling frequency	20 kHz
System power rating	150 kW

As shown in the figure, the grid voltage and current waveforms are shown in Fig. 2.16. The result remains normal. Whats more, arm voltage and arm current result are shown in Fig. 2.17. The voltage steps change is correct and so as the arm current of both upper arm and lower arm.

For the capacitor voltage balance, since the number of modules is small, sorting method is used. In this method, all the module voltage in one arm will be sorted and the highest voltage module is always be selected to be discharged and the lowest voltage module is always selected to be charged. The switching mode of the circuit
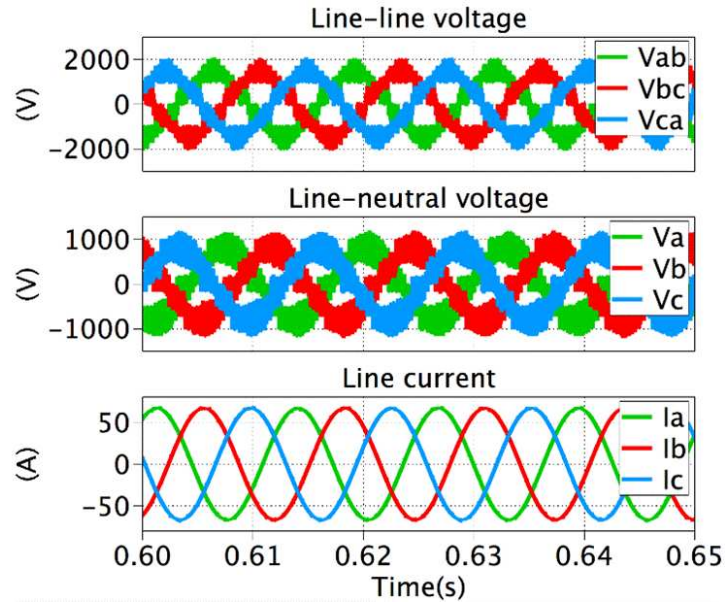
Figure 2.16: MMC Output Voltage and Current Simulation.
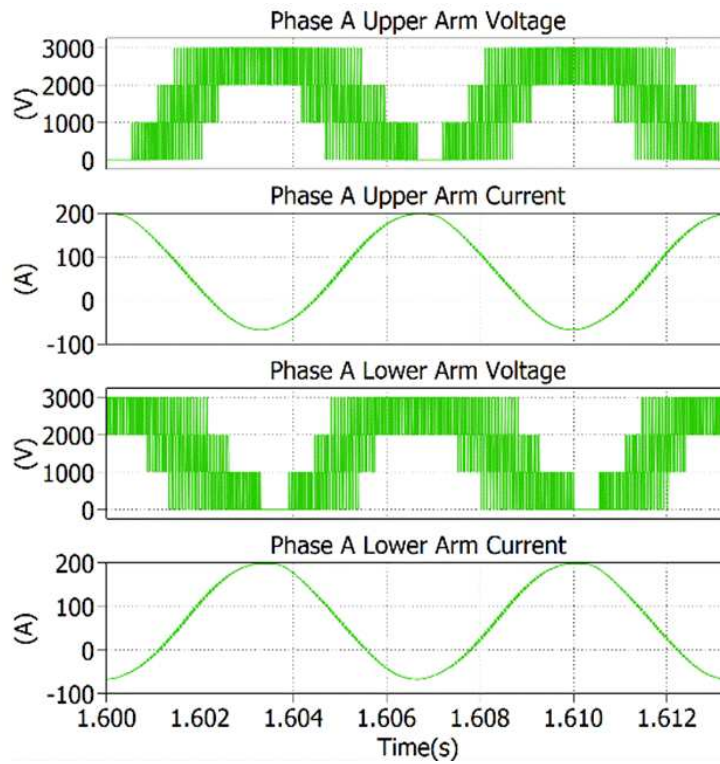
Figure 2.17: MMC Arm Voltage and Current Simulation.

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is built in the simulation and the balancing results are shown in Fig. 2.18.
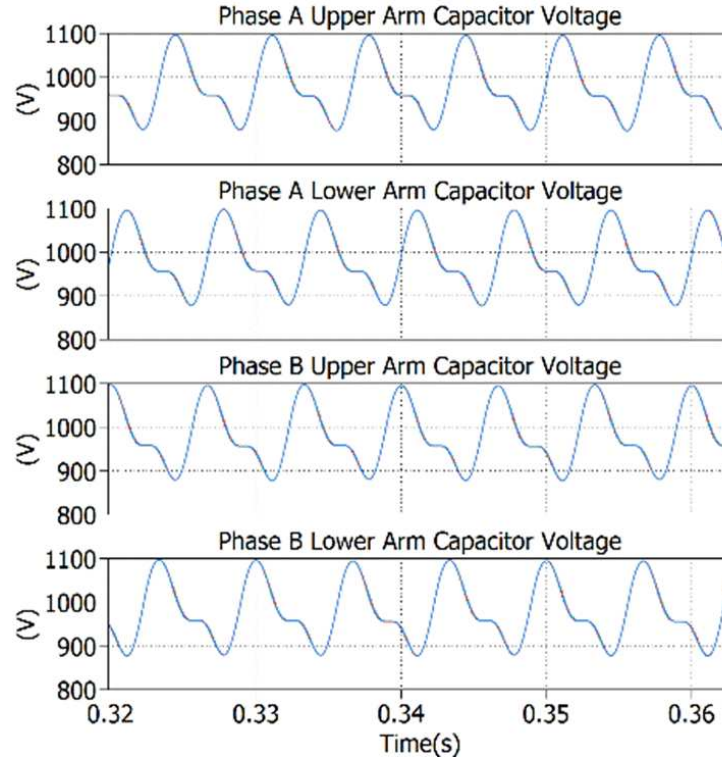
Figure 2.18: MMC Capacitor Voltage Balance Simulation Result.

2.4 Proposed Modular Isolated Multilevel Converter (MIMC)

A basic drawback of the MMC is the capacitor size. Instead of absorbing only switching frequency ripple current, the module capacitor in MMC needs to undertake the fundamental frequency current, which is at the half magnitude as the output current, as well as a significant second order harmonic current circulating among phases. It can also be understood as: a fundamental frequency energy ripple that reveals on the capacitor. To fulfill a high-performance close loop control for precise input and output current, the submodule capacitor voltage needs to be precisely controlled at its nominal value with limited fluctuation. In order to limit the SM capacitor voltage ripple within acceptable range, the capacitance of each SM need to be large enough to

compensate the highest voltage ripple under certain low frequency. From the industrial capacitor catalog, it can be summarized that the capacitor size is related to the total energy of the capacitor. Therefore, large capacitance ultimately leads to bulky capacitor size. This problem is further exacerbated under low fundamental frequency region, which is kind of universal situation during the startup of a motor. Even when the fundamental frequency is close to zero, the SM capacitor is still predictably forced to stand tremendous voltage ripple. Under this situation, simply increasing the capacitance alone is no more a reasonable solution. Therefore, utilization of MMC in applications with variable frequency scenarios, such as adjustable speed drives, is not that popular as expected [20–23].

In recent years, many methods have been proposed to solve the capacitor size issue. One effective approach is low frequency circulating current injection [24–26]. A second order harmonic current is introduced and controlled to minimize the energy fluctuation. However, this injected low-frequency current significantly increases the device power loss as well as the current stress. High frequency circulating current injection is proved to be another good method [27–29]. The low-frequency voltage ripple or the energy fluctuations are shaped into high-frequency components and thus the SM capacitor can be charged or discharged in a faster speed. Therefore, the voltage ripple can be effectively damped and the required SM capacitance is reduced. However, besides the increased current stress and device conduction loss, another drawback of this method is the additional inducted common mode (CM) voltage at the motor terminals.

One class of methods aim at reducing capacitor size by new module structure [30–38]. To reduce the inrush current in the dc short circuit failure, a common method is to replace the Half-Bridge (HB) module by a Full-Bridge (FB) module [30–33]. But the capacitor size can also be reduced by implementing this. The reason is that the

FB module can output positive and negative voltage, so the arm voltage can become negative. Therefore, the vector of [arm voltage, arm current] under FB configuration can have values in four quadrants. The phase shift between the two can be random. Since the instantaneous energy waveform is the integration of the instantaneous arm voltage and current with time, the four quadrant characteristics makes the energy ripple to have twice frequency of the fundamental frequency. However, the original MMC can only have a positive arm voltage, so the energy ripple frequency is the same as the fundamental frequency. With the similar power level and output voltage, the Full-bridge module can reduce the arm energy ripple at most by half. Therefore, replacing HB module by FB module is an effective method to reduce the capacitor size. However, it will bring the disadvantages of the conduction loss and switching loss increase since the same arm current now flows through two times of devices. To reduce the loss, a clamp-double SM [34, 35] or semi-FB SM [36] have been proposed, in which the module can be configured into one FB or two HBs by modulating the middle switch. If DC short circuit happens, half number of FBs is enough to generate a negative ac voltage to cancel out the source voltage, so only half number of the clamp-double SM needs to be installed compared to the number of HBs. But then in normal operation, the capability of generating a negative arm voltage is limited. Therefore, the capacitor size reduction is limited. To overcome the challenge, a double-zero submodule has been invented to further reduce the conduction loss brought by FB modules, as well as reducing the capacitor size [37, 38]. This module controls the capacitor charging and discharging by the middle SiC MOSFET. In bypass mode, the conduction loss is the same as the traditional HB module, because two conduction branches are in parallel. Due to the further loss reduction, the arm can be equipped with more such modules, so the arm voltage can have a higher negative value, which makes the capacitor size further reduced. The double connection of the double-zero

submodule can reduce the capacitor size by exactly half.

Another class of methods focuses on cross-connecting modules [81–83]. They are introduced to help absorb and balance the energy fluctuation between the upper arm and lower arm by properly controlling the flowing ac current in these channels [81, 82]. Based on these, horizon-connected channels built by DHBs are further proposed in [83] to replace the original cross-connected channels. The pulsating energy ripple in the three adjacent SMs can be eliminated as the vectoral low frequency current sum is zero. However, many extra active DHB control loops are added to the control strategy and thus increase control complexity.

As shown in Fig. 2.19, a new horizon-connected ripple current elimination approach based on CLLC circuit is proposed for variable-speed drives. The three SMs on same level but from three phase legs are connected to a common capacitor through a high-frequency half-bridge CLLC channel. As a result, the arm current flows into the CLLC channel instead of the original SM capacitor. On the secondary side, the current converges at the common capacitor and then get cancelled each other because the vectoral sum of the current is zero. On the other hand, the SM capacitor supports the dc-link voltage of the CLLC stage on the primary side while the common capacitor plays the same role on the secondary side. Therefore, the three SM capacitors are coupled together through the bidirectional CLLC stages, through which the energy exchange enables a dynamic voltage balance state between these three SMs. That is, the unexpected low-frequency energy ripples induced from both fundamental and second order harmonic current almost disappear and the SM capacitance is significantly reduced.
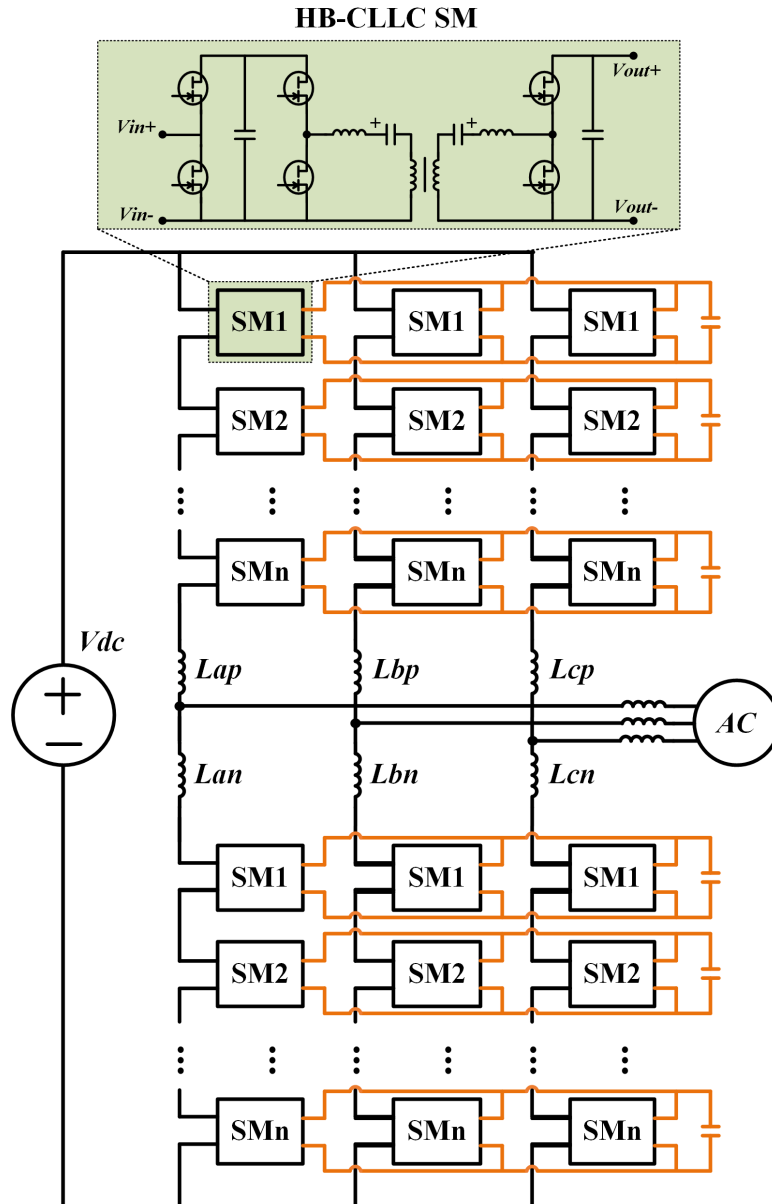
Figure 2.19: Circuit Diagram of the Proposed MIMC.

2.4.1 Mathematical Derivation of Capacitor Current Cancellation

Taking phase A as an example, the ideal equations of single arm converter output voltage and current can be expressed as equation Eq. 2.13 to Eq. 2.16:

$$i_{\text{up}}(t) = \frac{I_{\text{dc}}}{3} + \frac{I_{\text{a}}(\omega(t) + \varphi)}{2} + \sum_{h=2}^{k} i_{\text{h}}(t) \tag{2.13}$$

$$i_{\text{low}}(t) = \frac{I_{\text{dc}}}{3} - \frac{I_{\text{a}}(\omega(t) + \varphi)}{2} + \sum_{h=2}^{k} i_{\text{h}}(t) \tag{2.14}$$

$$v_{\text{up}}(t) = \frac{V_{\text{dc}}}{2} - V_{\text{a}} \cos(\omega(t)) \tag{2.15}$$

$$v_{\text{low}}(t) = \frac{V_{\text{dc}}}{2} + V_{\text{a}}(\omega(t)) \tag{2.16}$$

Also, it is assumed that the switching function can be expressed as Eq 2.17 and 2.18, in which the PWM modulation does not consider arm dc bus voltage variations ($M_0 = 1$). M_1 is the modulation index of each arm:

$$S_{\text{up}}(t) = \frac{M_0}{2} + M_1 \cos(\omega(t)) \tag{2.17}$$

$$S_{\text{low}}(t) = \frac{M_0}{2} - M_1 \cos(\omega(t)) \tag{2.18}$$

Combining Eq 2.13, 2.14, 2.17 and 2.18, the arm capacitor current can be calculated as:

$$i_{\text{C,up}}(t) = i_{\text{up}}(t) \times S_{\text{up}}(t) \tag{2.19}$$

$$i_{C,\text{low}}(t) = i_{\text{low}}(t) \times S_{\text{low}}(t) \qquad (2.20)$$

Moreover, considering only the dc and fundamental components of the arm current, combining the power balance Eq. 2.21 between the ac and dc side, the current flowing through the SM capacitor can be derived as shown in Eq. 2.22:

$$I_{\text{dc}} \times V_{\text{dc}} \times M_0 = \frac{3}{2} \times V_{\text{a}} \times I_{\text{a}} \times M_1 \qquad (2.21)$$

$$i_{\text{aC,up}}(t) = \frac{3}{16} I_{\text{a}} \cos(\omega(t)) + \frac{1}{8} I_{\text{a}} \cos(2\omega(t)) \qquad (2.22)$$

Therefore, SM capacitor current contains fundamental frequency and 2nd order harmonic components, which further induce the voltage ripple of same frequencies on the SM capacitor. This is the root cause of the low frequency ripple across the SM capacitor. The resultant dc bus voltage spectrum can be derived by the Eq. 2.23:

$$
\begin{aligned}
V^e(t) &= S_{\text{up}}(t) \times \frac{N}{C} \int (S_{\text{up}}(t) \times i_{\text{up}}(dt)) \\
&+ S_{\text{low}}(t) \times \frac{N}{C} \int (S_{\text{low}}(t) \times i_{\text{low}}(dt))
\end{aligned}
\qquad (2.23)
$$

Generally speaking, the dc bus voltage spectrum contains several spectral components, especially considering injected third harmonic. However, among them the most dominant component is the second order harmonics and can be expressed in Eq. 2.24:

$$
\begin{aligned}
V^e(t) &= \frac{N}{\omega C} \left(\frac{I_{\text{a}} M_0 M_1}{8} \sin \varphi - \frac{I_{\text{dc}} M_1^2}{12} \sin(2\omega(t)) \right. \\
&+ \frac{3 I_{\text{a}} M_0 M_1}{16} \sin(2\omega(t) + \varphi) + \frac{I_{\text{a}} M_0 M_1}{8} \sin(2\omega(t) - \varphi))
\end{aligned}
\qquad (2.24)
$$

This equation also presents the direct driving voltage for the circulating current. It needs to be pointed out that the effect of third harmonics injection is limited and

therefore ignored in the calculation of dc bus voltage. Any higher order harmonics such as forth and sixth order harmonics are also not counted in this due to their low amplitude.

$$i_{\text{aC,up}}(t) + i_{\text{bC,up}}(t) + i_{\text{cC,up}}(t) = 0 \tag{2.25}$$

In traditional MMC topology, the arm current absolutely flows through the SM capacitor. However, in the proposed MIMC topology, the arm current from three phase legs flow through the CLLC ripple current elimination channels instead and converge at the common capacitor located on the secondary side. By applying the Eq. 2.22 to both phase B and phase C, it can be concluded that the vectoral sum of the three-phase fundamental and second order current is zero, as expressed in Eq. 2.25. That is to say, neither the original SM capacitor nor the common shared capacitor needs to conduct low frequency ripple current. As a result, the sizing of the SM capacitance only depends on the high frequency switching ripple, which consists of the original SM switching ripple and the newly introduced CLLC resonance frequency switching ripple. In conclusion, the required SM capacitance is greatly reduced compared to the traditional case.

2.4.2 Description and Analysis of Newly Proposed SM in MIMC

The SM in MIMC is required to have three major features: (1) high voltage isolation: the isolation is the key to form the claimed parallel connection, and the isolation level here is as high as the dc-link voltage of the whole converter; (2) bidirectional power flow: the original capacitor current is ac current, so the following stage needs to be able to conduct bidirectional current; (3) low switching loss: the additional conduction loss is unavoidable since the full current will flow through each additional

switch on the path to the final capacitor, but the switching loss can be minimized by employing soft switching topologies. Therefore, a SM composed of the half bridge and the CLLC converter is developed and simplified schematic of which is shown in Fig. 2.20 and Fig. 2.21.
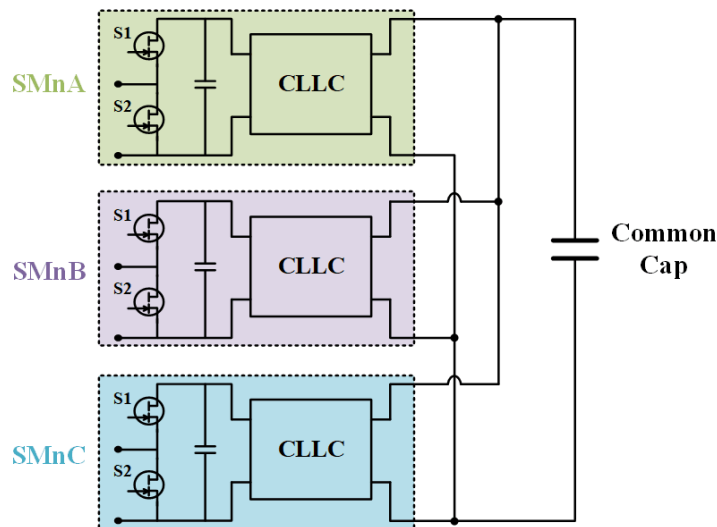
Figure 2.20: Illustration Schematic of the Ripple Current Elimination Channels.
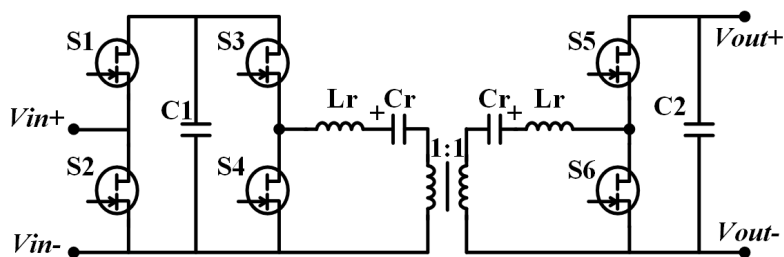
Figure 2.21: Simplified SM Schematic.

The reason to select the CLLC converter as the isolation stage instead of DAB is that CLLC/LLC operates at ZVS and ZCS at the same time, but DAB operates at ZVS with maximum current at turn-off [84–86]. In addition, there are two other major drawbacks of DAB. First, DAB loses the soft switching at light load because its load current is the main force to charge and discharge the junction capacitance.

In the proposed topology, the dc link current after the first half bridge is equal to the original capacitor current, which is pure ac value including fundamental and second order harmonic components. Therefore, the main ac current in the transformer will cross zero and stay close to zero for a long time. During this time, DAB will lose the soft-switching capability. Secondly, active phase angle control needs to be applied for all DABs to achieve bidirectional power flow as well as the gain adjustment. Therefore, the overall control becomes more complex. Moreover, the tradeoff between the phase angle and the switching loss needs to be considered, which means the energy transfer speed is limited. Compared to DAB, the ZVS in CLLC/LLC depends on the magnetizing current [87]. When operating under DCX mode, the load current is always zero during the dead-time. Thats to say, the dc current profile deals no effect on soft switching on all load range. Another benefit of the DCX mode is the simplified control strategy. High frequency switching with fixed 50% duty cycle is sufficient to achieve the goal. Therefore, it is not necessary to be involved in the overall current control loops of MMC.

Among the resonant converters, CLLC is chosen over LLC because it features the symmetrical resonant architecture and symmetrical voltage gain curve in both power flow directions [87, 88]. As for CLLC converter, there are two types: Full-Bridge (FB) version and Half-Bridge (HB) version. Although the device current stress in FB is lower, the cost is the double switching devices. Another main issue is focused on the resonant capacitor. Half the SM capacitor voltage will drop on the resonant capacitor in HF-CLLC. In exchange, the winding voltage is also halved and lower the requirement on maximum flux density of transformer core. Therefore, the topology selection needs careful consideration. In the built downscaled prototype, the HF-CLLC is the preferred selection because of fewer switching devices, looser design of planar transformer and the comparable assembling of resonant capacitor bank [89].

In each SM, there are three GaN devices based half-bridges (HBs) in total. The first one follows the modulation command of normal MMC operation. The rest two HBs, together with two resonant tanks, form the bidirectional CLLC resonant circuit, in which a well-designed planar transformer is employed. The turns ratio of the transformer is set as 1:1 since the major task of the CLLC is bidirectional power transfer with galvanic isolation. In the HB version CLLC schematic shown in Fig. 2.22, the inverting switches S_3 and S_4 run at 50% duty cycle and 180° out of phase. On the secondary side, the S_5 is synchronized with S_3 while the S_6 strictly follows the S_4. There are generally two operation states as shown in Fig. 2.22. For the positive cycle, as the S_1 and S_3 are conducting, the resonant tank is kicked in and the resonant current increases in a sinusoidal shape. Since the switching frequency is set to be very close to the resonance frequency, the impedance of resonant tank can be regarded as zero. Therefore, the high-voltage square-waveform switching node voltage is applied on the magnetizing inductance and the induced magnetizing current increases in a triangular shape. The load current is carried by the resonant current and the power is transferred to the secondary side through the transformer. When transferred to the negative state, the S_4 and S_6 are conducting while the S_3 and S_5 are turned off. The resonant capacitor applies negative dc voltage on the primary winding. The resonant current is in a freewheeling mode and will not flow out. Therefore, the whole operation cycle demonstrates a half-wave rectification.
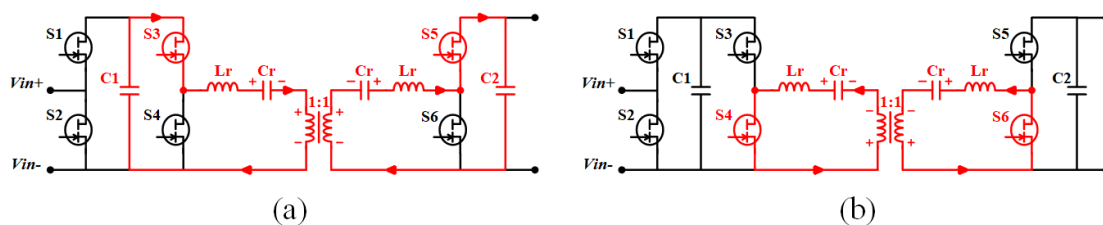
Figure 2.22: CLLC Operation Illustration Schematic: (a) positive cycle; (b) negative cycle.

Transformer design considerations are introduced here in advance as guideline. More details will be given in hardware development section. The transformer design is very critical for the CLLC resonant converter inside the SM. High switching frequency introduces high core loss and winding loss. The planar transformer stands out for very high frequency applications ($\geq$ 500 kHz) because of some prominent merits [84, 85]. The PCB trace formed windings largely diminish the skin and proximity effects, which greatly reduced the ac winding loss. Unlike the Litz-wire wound transformer, better coupling minimizes the leakage inductance as well as the ac winding loss. Low-profile and high filling factor significantly improve the power density compared to the traditional design. Last but not the least, the easy fabrication and assembling process is also very important characteristics in modular design such as MMC.

A comprehensive design methodology is fully explored in [109] and employed in the hardware development of proposed SM. The summarized flow chart of step-by-step design process is presented in Fig. 2.23.

First of all, the constraints for planar transformer design in proposed topology can be summarized as follows:

(1) $B_{\mathbf{max}} < B_{\mathbf{sat}}$: The maximum flux density ($B_{\max}$) determined by Volt-Second of transformer is normally much less than the saturation flux density (B_{sat}) of the core material..

(2) $g < g_{\mathbf{max}}$: The air-gap length (g) should be confined as well. If g is too large, the fringing flux causes more winding loss.

(3) $J < J_{\mathbf{max}}$: The current density (J) in the winding should be smaller than the maximum allowable current density ($J_{\max}$). $J_{\max}$ is limited by the winding temperature rise.
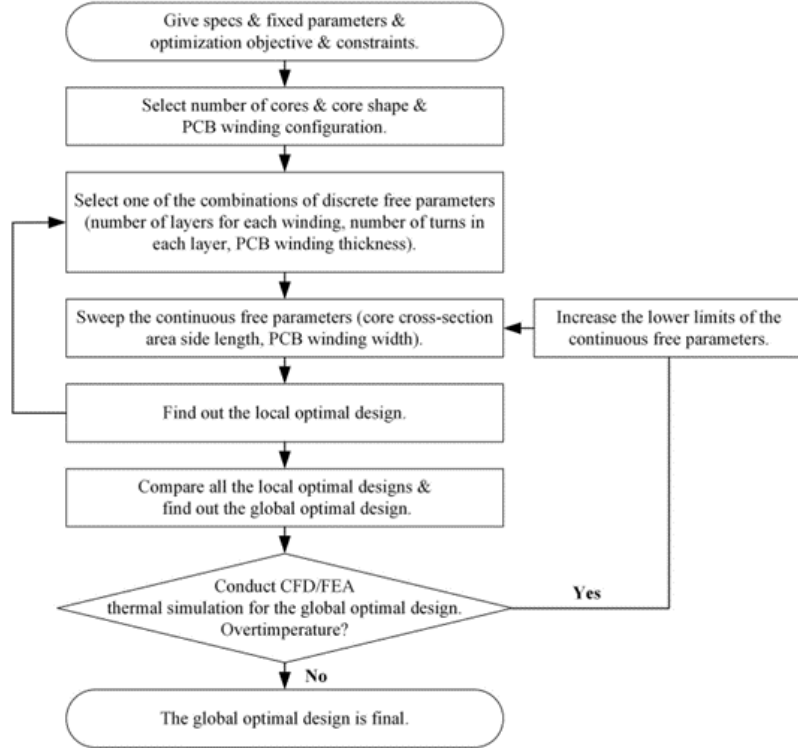
Figure 2.23: Generalized Design Methodology for High-Power-Density Planar Transformers.

(4) **Insulation distance**: The two major concern in this part include the distance between two adjacent windings (δ_{ww}) and the distance between winding and magnetic core (δ_{cw}). Together with the number of turns, these two fixed parameters are closely related to iteration of effective window area calculation.

(5) **Minimize L_{leakage}**: The leakage inductance (L_{leakage}) is not the priority here since an external inductor is employed. However, larger leakage inductance means stronger leakage magnetic field intensity, which can cause more ac winding loss.

(6) **Minimize C_{intra} and C_{inter}**: Compared with traditional transformer, planar transformer has much higher winding stray capacitance, which may affect the

soft switching. The high interwinding capacitance indicates larger common node noise crossing primary and secondary winding, especially in high voltage applications. Therefore, these two should also be minimized.

For the device selection in the half bridges, the voltage and current rating of the device is exactly the same as the front stage half bridge. For the resonant inductance and capacitance sizing, the guideline is to achieve the smallest possible leakage inductance, and then calculate the resonant capacitance according to the inductance. The reason is that the converter is working at DCX, so it doesnt require a certain ratio between the leakage inductance and the magnetizing inductance to form a gain curve that provides narrower frequency variation range to fulfill the voltage gain variation. Since the leakage inductance is formed inside the transformer, the leakage inductance should be sized as small as possible in order to reduce the loss of the transformer. In this case, the leakage inductance is calculated according to the specific winding structure which is discussed in later section. In order to adapt to the non-ideal cases that the converter is not operating at exactly DCX, an external planar inductor is designed to provide the converter a gain variation range while operating in a reasonable switching frequency range.

In summary, the proposed MIMC module provides the capability for the parallel connection of the three phase modules. It features high efficiency and high power density due to the employment of ZVS and planar transformer. However, the proposed MIMC still suffers from higher device power loss than the conventional MMC since the same current flows through more devices. Therefore, the utilization of MIMC and MMC is a trade-off between power density and the efficiency.

2.5 Simulation of Proposed MIMC Topology

The proposed MMC topology with ripple current cancellation stages has been verified using PLECS simulation tool. The general operation performance has been demonstrated. The current waveforms at different positions of the module are fully investigated. Besides, a downscaled laboratory prototype is also built to realize the proposed topology and demonstrate the claimed benefits. The simulation and hardware specifications are listed in Table 2.2. Since the comparative tests are conducted for the traditional MMC and proposed MMC, two different sets of SM capacitor bank need to be prepared. As for the SM capacitance presented in the table, the value on the left is the capacitance required in traditional MMC topology while the right one is for the proposed topology.

Table 2.2: Key Specifications of Proposed MIMC.

Parameters	Simulation	Experiment
Rated power	55 kW	4.8 kW
DC-link bus	2.2 kV	400 V
Rated peak AC current	42 A	10 A
Number of SMs per arm	3	2
SM capacitance	1 mF / 1 μF	240 μF / 1 μF
Nominal SM capacitor voltage	740 V	200 V
SM switching frequency	20 kHz	20 kHz
Common linked capacitor	1 μF	100 μF
Arm inductance	5 mF	2 mF
Nominal fundamental frequency	60 Hz	60 Hz

In the simulation study, the circuit exactly follows the schematic described before and supplies a three-phase RL load. Meanwhile, a comparison between the traditional

MMC and the proposed one has been conducted in the simulation. The basic operation waveforms of the traditional MMC topology are shown in Fig. 2.24(a). At one point, the simulated topology will switch from MMC to MIMC. The basic operation waveforms of the proposed MIMC are shown in Fig. 2.24(b). The dynamic waveform when switching between these two topologies are presented in Fig. 2.25.
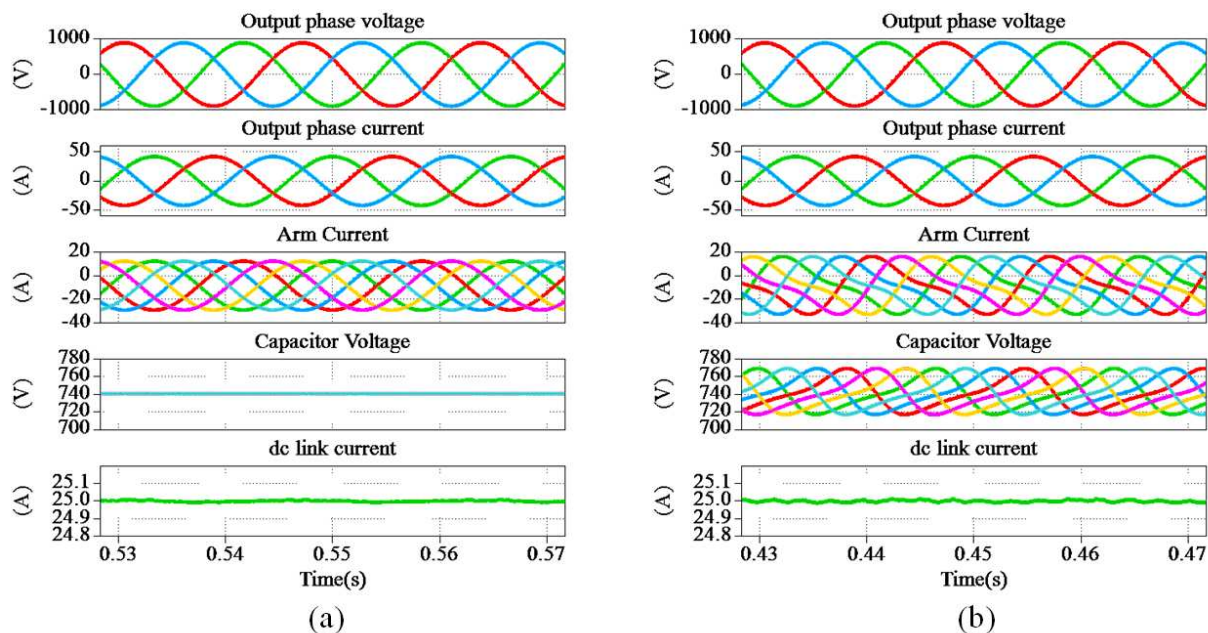
Figure 2.24: Simulation Results Comparison Between (a) Traditional MMC and (b) Proposed MIMC.

The two major differences between the waveforms of MMC and MIMC are: (1) MMCs capacitor voltage contains large fundamental and second order harmonics, but MIMCs capacitor voltage is almost only formed of dc component; (2) MMCs arm current contains significant second order harmonic, but MIMCs arm current has very little harmonics. It demonstrates that the low frequency currents from adjacent arms successfully converge at the common capacitor and cancels each other. The arm current, which supposes to flow through the SM capacitor, run all the way into the CLLC channels instead. The flat dc voltage and the switching function also will not

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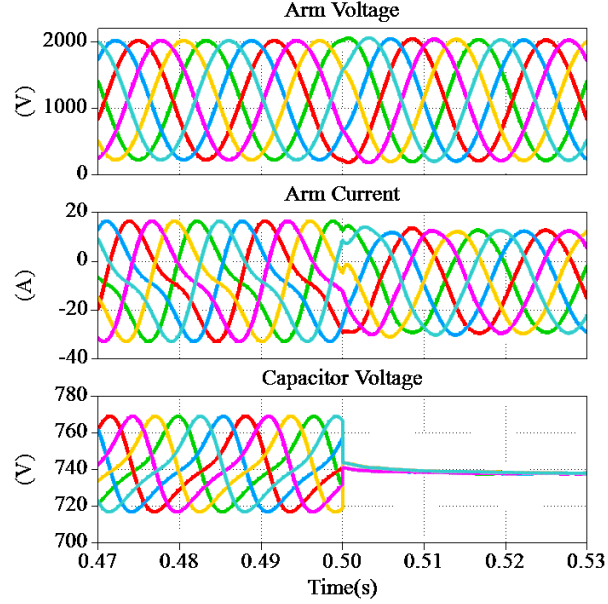
Figure 2.25: Simulation of Topology Switch from Traditional MMC to the Newly Proposed.

generate second order current in the arm as well. As SM capacitance are the same in the simulations for both topologies, a perfect flat dc voltage can be observed on the SM capacitor in MIMC. Actually, the SM capacitance in MIMC can be sized much smaller.

The current detail in the CLLC current cancellation stage is also demonstrated in Fig. 2.26 while the FFT analysis of the current at different points of SM is presented in Fig. 2.27. Ideally, all the original fundamental and second-order harmonic capacitor current flows through this channel. From the current profile point of view, the magnetizing current presents a high-frequency triangular waveform while the resonant current appears to be a high-frequency sinusoidal waveform with changing amplitude, the envelope of which is formed by the low frequency ripple current. Since the SM capacitor is also involved in the resonant loop, the high-frequency ripple current flowing through the capacitor also follows the envelope. But the difference is that it is disconnected from the resonant loop during the negative resonant cycle. Therefore,

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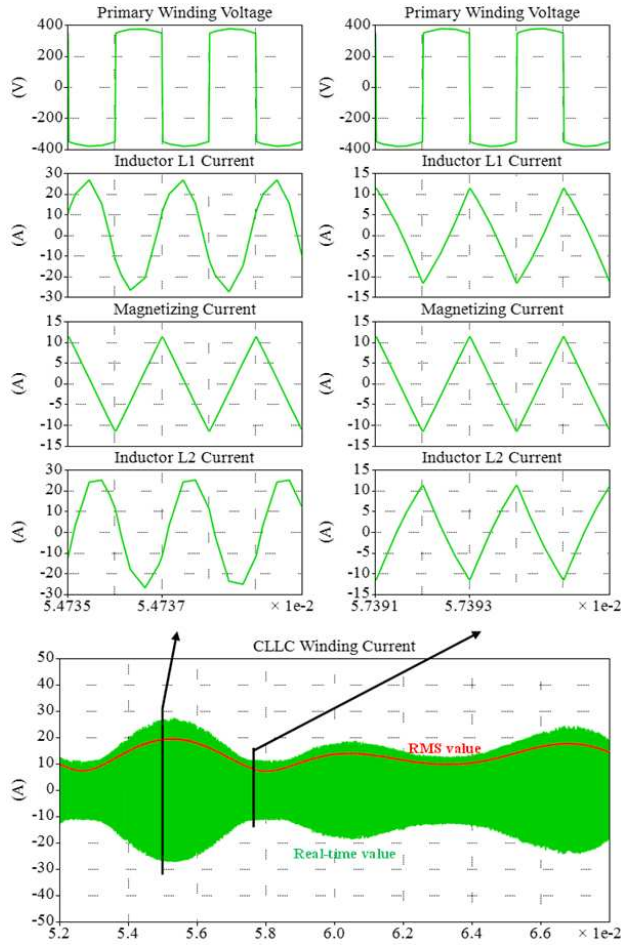
Figure 2.26: Simulation Results of CLLC Resonant Circuit.

the ripple current profile becomes a chopped high-frequency ac waveform.

As can be seen in Fig. 2.27, only little fundamental and second order harmonics can be observed in original SM capacitor while most of the components are found in current after the SM capacitor. Thats to say, major part of the current flows into the CLLC channel. This is the reason why the large voltage ripple on SM capacitor in traditional MMC disappears. Thats to say, the effectiveness of the proposed topology on reducing the SM capacitor voltage ripple is verified. It needs to point out that the existing low frequency current in SM capacitor is due to the imperfect physical circuits, which will be discussed in later hardware development section. As for the
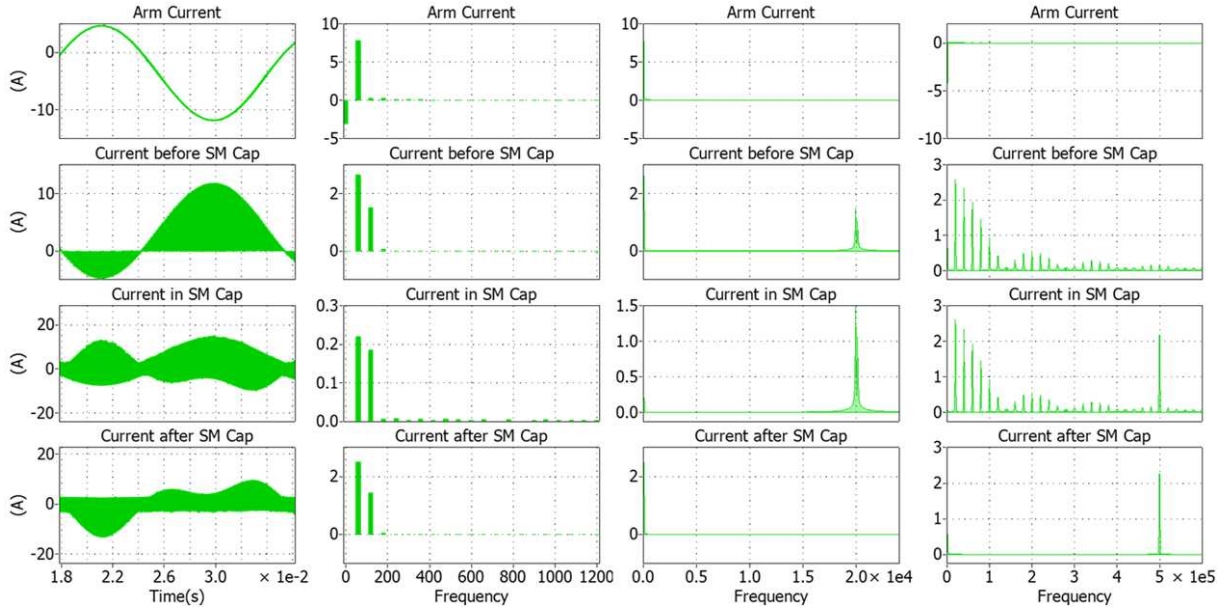
Figure 2.27: FFT Analysist of Current Components at Different Points in SM of MIMC.

high frequency range, 20 kHz component and 500 kHz component can be observed. The former frequency component comes from the SM switching frequency while the latter one comes from the CLLC resonance frequency. This is because either the SM front HB or the CLLC share the same dc bus capacitor which is formed by the SM capacitor.

The CLLC winding current in three phases is demonstrated in Fig. 2.28. From zoom out version Fig. 2.28(a), it can be summarized that the power flow will be positive if the SM capacitor voltage is larger than that of the common capacitor. Thats to say, the SM with higher voltage will send out the energy to the common capacitor while the SM with lower voltage will draw power from the common capacitor. Then, the voltage value of three SM capacitors and the common capacitor maintains a dynamic balance state. On the other hand, the pulsating energy in three SMs are freely exchanged through the CLLC channels and the common capacitor. As a result, no fundamental and second order harmonic ripple components can be

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observed in each capacitor, which significantly reduce the occupied volume by capacitors. In the zoomed in version in Fig. 2.28(b), it can be seen that the three CLLCs are synchronized, which manages to minimize the induced very high frequency ripple on common capacitor. Besides, the current resonant direction also reflects the power flow direction.
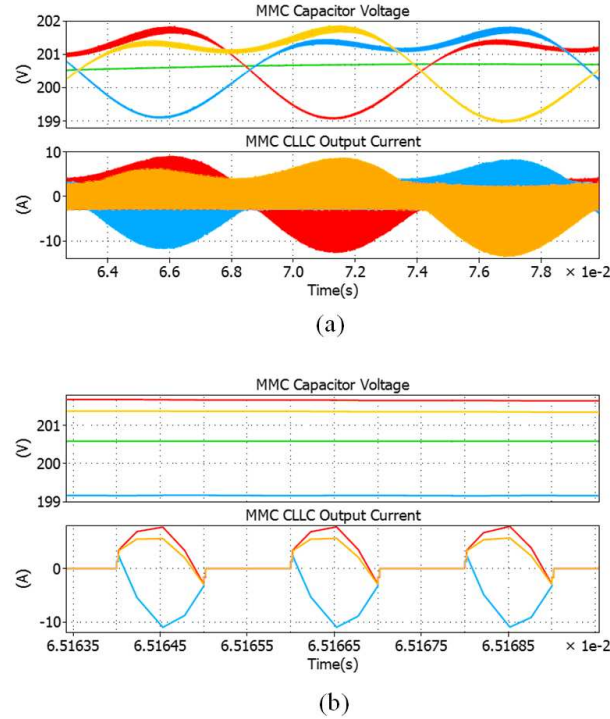
Figure 2.28: CLLC Winding Current and Dc Bus Voltage in Three Phases: (a) Zoom Out; (b) Zoom In.

Besides the RL load, the motor drive load is also simulated. The start-up process in the simulation is shown in Fig. 2.29, in which the fundamental frequency ramps up from 0 Hz to 60 Hz. The arm current presents a perfect sinusoidal and the SM capacitors keep zero low-frequency voltage ripple even when the frequency is close to zero. With the same capacitor, the MIMC can run from zero frequency to high frequency while keeping the output voltage and current always a perfect sinusoidal waveform. The benefit is significant compared to conventional MMC. The desired

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capacitance in MMC is reverse proportional to the output frequency. Ideally, it cannot start up from zero frequency. To avoid bulky capacitor, a high frequency current injection method is used to start up the MMC from zero frequency. However, it introduces large additional loss to the converter. A tradeoff analysis between size and efficiency will be conducted and the capacitor will be sized at a certain low frequency close to zero. Therefore, the capacitor size will be two or three times larger compared to that in grid-connected application. However, the capacitance in MIMC is independent from the system operation frequency. It is only sized to absorb the switching frequency ripple in SM. The capacitance will keep the same when operation frequency increases from low to high. At the same time, the capacitor voltage will always present negligible low-frequency harmonics. Therefore, in variable speed drive application, the proposed MIMC presents a significant reduction on the capacitor size compared to the traditional MMC.
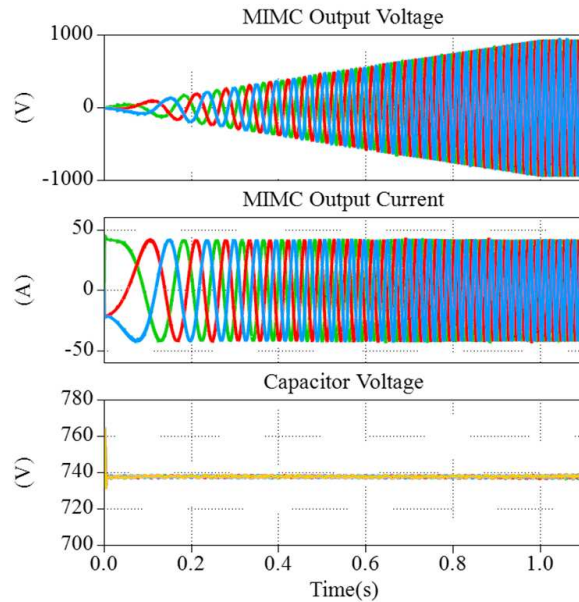
Figure 2.29: Simulation of Motor Drive Start-up Process Using Proposed MMC Topology.

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2.6 Hardware Development of Proposed MIMC Topology

2.6.1 SM Capacitance Sizing Methodology

In this subsection, an analytical method for calculation of minimum SM capacitance in HB-MMC is presented. The basic criteria considered in these calculations are maximum permissible repetitive voltage ripple and the required maximum converter voltage to avoid modulation in presence of dc bus ripple. Assuming that the circulating current is negligible, the stored energy in the arm converter can be expressed as:

$$\frac{dW_{\text{C,up}}}{dt} = -v_{\text{up}}(t) \times i_{\text{up}}(t) \tag{2.26}$$

$$\frac{dW_{\text{C,low}}}{dt} = -v_{\text{low}}(t) \times i_{\text{low}}(t) \tag{2.27}$$

Based on the mentioned arm voltage and current Eq. 2.13, 2.14, 2.15 and 2.16, the time varying stored energy variations, for example the upper arm, can be derived as shown in Eq. 2.28. Combining the Eq. 2.21, an alternative expression for time varying energy ripple is further presented in Eq. 2.29:

$$\Delta W_{\text{C,up}}(t) = \frac{1}{\omega} \left(\frac{V_a I_{\text{dc}}}{3} \sin(\omega(t)) - \frac{V_{\text{dc}} I_a}{4} \sin(\omega(t) + \phi) \right) \\ + \frac{V_a I_a}{8\omega} \sin(2\omega(t) + \phi) \tag{2.28}$$

$$\Delta W_{\text{C,up}}(t) = \frac{S}{12\omega} \left(\frac{2M_1}{M_0} \sin(\omega(t)) \cos\phi - \frac{M_1}{4M_0} \sin(\omega(t) + \phi) \right. \\ \left. + \sin(2\omega(t) + \phi) \right) \tag{2.29}$$

The SM capacitance selection must ensure that the energy variations do not produce excessive repetitive peaks. This condition can be expressed in Eq. 2.30 via the stored energy decomposition:

$$\frac{C}{2N}V_c^2 + \Delta W_{C,up}(t) = \frac{C}{2N}V_{up}(t)^2 \tag{2.30}$$

From the instantaneous energy variation, the peak of the energy fluctuation can be found:

$$\Delta W_{C,max} = \frac{C}{2N}V_{c,max}^2 - \frac{C}{2N}V_c^2 \tag{2.31}$$

The number of modules in HB-MMC can be calculated by:

$$N = \frac{V_c}{V_{c,module}} \tag{2.32}$$

In general, V_c equals to the dc bus voltage in HB based MMC configuration. $V_{c,module}$ is decided according to the switching devices voltage rating. The $V_{c,max}$ in Eq. 2.31 is limited to be no more than k% of the V_c (the typical value of k% can be 105% - 110%). Combining Eq. 2.31 and 2.32, the SM capacitance can be estimated as:

$$V = \frac{2N}{k^2 - 1} \times \frac{\Delta W_{C,max}}{V_{c,module}^2} \tag{2.33}$$

The SM capacitance sized in this way ensures that the dc bus voltage fluctuations are kept below the capacitor repetitive voltage rating and that sufficient voltage margin is provided in given operational conditions. However, it still needs to leave some

margin in order to further increase the dc bus stiffness in case of large power system transients, load shading which are causes of large energy fluctuations. In traditional MMC topology as discussed before, the major components in SM capacitor current are fundamental, second order harmonic and the high frequency SM switching ripple. Following the methodology mentioned above gives the required SM capacitance. However, this is no longer the case in proposed MIMC.
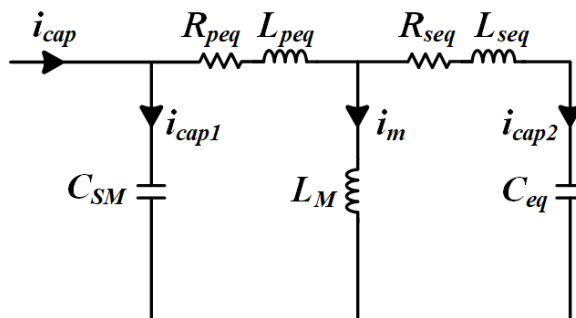
Figure 2.30: Simplified Equivalent Circuit Model of SM-CLLC.

The fundamental and second order harmonic get eliminated by the CLLC circuits. Therefore, the remaining current in SM capacitor is divided in following three parts: (1) The switching ripple of original SM. During the on period, the SM capacitor conducts the arm current and get charged. (2) The switching ripple of CLLC resonant tank. As the SM capacitor also forms the dc link bus of the CLLC stage, it provides the dc voltage applied on the transformer winding. Therefore, the sinusoidal resonant current flows through the capacitor and generate very high frequency voltage ripple. However, this part is dominated by the SM switching ripple. (3) Little low frequency ripple from arm current. Although this part ideally should be zero due to the current elimination, the actual hardware circuit of HB-CLLC is not perfect and behaves like a huge capacitor bank paralleled with SM capacitor, as shown in Fig. 2.30. Generally speaking, carefully designed and assembled CLLC circuits can maximize the C_{eq} and features several orders of magnitude difference between C_{SM} and C_{eq}. However, since

the C_{eq} is close related to the physical circuit model, it is quite difficult to predict the accurate equivalent capacitance. According to actual experiments, few second-order harmonic ripple can still be observed on the SM capacitor, which dominates the switching ripple of CLLC resonant tank and SM. Therefore, it is quite necessary to leave enough margin when sizing the SM capacitance. Based on the experimental results, it is recommended to size the SM capacitance assuming 5% of original arm current still flow through the SM capacitor.

In conclusion, since almost all the low-frequency ripple is transferred to the CLLC stage, the major consideration of the SM capacitor selection should be absorbing the SM-HB switching ripple. However, the actual hardware circuit determines that the SM capacitance is still dominated by the few low frequency ripple flowing into the SM capacitor. Thus, appropriate margin when sizing the capacitance should be considered. Despite all the discussed concerns above, the SM capacitance is already significantly reduced.

2.6.2   SM CLLC Resonant Tank and Transformer Design Considerations

As is known, the magnetizing current is the main charging/discharging current for the junction capacitor during the dead-time since the resonant current crosses zero at the device turn off moment. The biggest difference between the CLLC of MIMC and the traditional CLLC is that the flowing load current, which is a mix of fundamental and second order harmonic currents. Thus, the envelope of the resonant current follows the shape of the load current, which means the amplitude of the resonant current in the CLLC keeps changing. The detailed waveform will be shown in later section. As a result, the load current for the CLLC can be as low as zero. At that moment, the junction capacitor energy needed in the soft switching will only be provided by the magnetizing current solely, which becomes a guideline for designing

the magnetizing inductance. In summary, the peak magnetizing current needs to be able to fully charge or discharge the junction capacitors of switching devices.

In general, the sizing of leakage inductance is very important in some applications. However, it is not the first priority here due to two major reasons. First, an external inductor is employed to build the resonant tank. The excessive leakage inductance can be integrated in resonant inductance by flexibly adjusting the external inductor. Second, the isolation level between primary and secondary winding should be considered based on the whole dc bus voltage. This high isolation requirement enlarges the distance between the core and the winding as well as the distance between the primary winding and the secondary winding, which results in larger leakage inductance. Additionally, it is also preferred to minimize the inter-winding capacitance to reduce the induced common mode noise. Therefore, the interleaving winding structure, which is good for leakage inductance minimization at cost of higher inter-winding capacitance and short distance between two sides, is not adopted. Instead, parallel routing strategy is employed in the transformer design as shown in Fig. 2.31. Alternatively, the inner layer 1 and 2 can be set as shielding layer to further reduce the inter-winding capacitance.
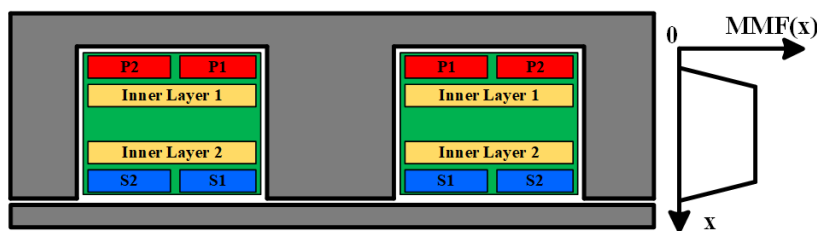
Figure 2.31: Winding Structure of the Planar Transformer.

As for the resonant tank, external inductors are employed to alleviate the thermal stress of the high-power-density planar transformer. For the design of independent resonant inductors, both the planar inductor and the Litz-wire wound inductor can

be utilized. The low-profile less-labor-intense planar inductor is selected. The design and optimization of the planar inductor is very similar to the design of the planar transformer but two major differences. First, the maximum flux density ($B_{\max}$) in a planar inductor is determined by the peak current rather than the voltsecond. Second, uniformed current direction means no flux canceling between the adjacent turns in the inductor. Therefore, the number of turns for a planar inductor should be as few as possible to avoid the excessive ac winding loss.

For the resonant capacitor, film capacitors and ceramic capacitors can be taken into consideration. The ceramic capacitors usually exhibit smaller size, lower equivalent series resistance, and higher corner frequency. Although the voltage rating of ceramic capacitors is limited compared to film capacitors, the selected half-bridge topology only utilizes half the capacitor voltage. Besides, the modularity of MMC enables lower voltage rating of single SM. Therefore, the voltage rating requirement of the capacitor is still significantly reduced. Meanwhile, multiple capacitors can be paralleled to reduce the thermal stress for each capacitor. Moreover, the capacitance value should be consistent under the operating temperature range. Eventually, the C0G/NP0 ceramic capacitors are employed in the design of proposed SM. The ultimate parameters of the resonant tank are also listed in Table 2.3.

2.6.3 SM CLLC Resonant Tank and Transformer Design Considerations

As the resonant tank design and SM capacitance sizing strategies have been discussed, what left here in SM development is the gate drive circuits and switching stage development. Since the new SM in MIMC needs to be operated under high frequency (20 kHz for front HB stage and 500 kHz for CLLC), GaN transistor is selected since it features low output charge, low gate charge, zero reverse-recovery charge and low channel on-resistance. As a benefit, GaN devices present higher switching frequency,

Table 2.3: Key Specifications of CLLC Magnetics

Parameters	Values
Resonant frequency	500 kHz
Switching frequency	500 kHz
Operation mode	DCX
Planar transformer core material	E58/11/38 - 3F36
Planar transformer $B_{\max}$	80 mT
Turns ratio	2 : 2
Number of turns	3
Resonant tank inductor	1.15 μH
Resonant tank capacitor	88 nF

higher switching transient, lower gate loss and lower power loss compared to the SiC devices. However, in high-frequency applications, the major challenges of GaN lay on crosstalk issue and parasitic induced oscillation (V_{gs} and V_{ds} ringing).

The CoolGaN IGOT60R070D1 fabricated by Infineon Technologies is a high-performance transistor technology for power conversion in the voltage range up to 600 V, which is selected to build up the bridges in SM. The electrical model of the IGOT60R070D1 CoolGaN HEMT is presented in Fig. 2.32. Compared to traditional MOSFET, the IGOT60R070D1 shows two major differences. First, the GaN HEMT has no intrinsic body diode from source to drain like a SJ MOSFET, for example. And second, the gate does have a diode structure that clamps the gate-source (or gate-drain) voltage to approximately 3 V - 3.5 V. The exact clamp voltage varies with the fabrication, junction temperature and gate current flowing through the R_{dio}. As a result, the V_{gs}, which control the channel conductivity, is a function of both current and drain current. This is a very important characteristic in GaN since it

strongly affects the gate driver design.
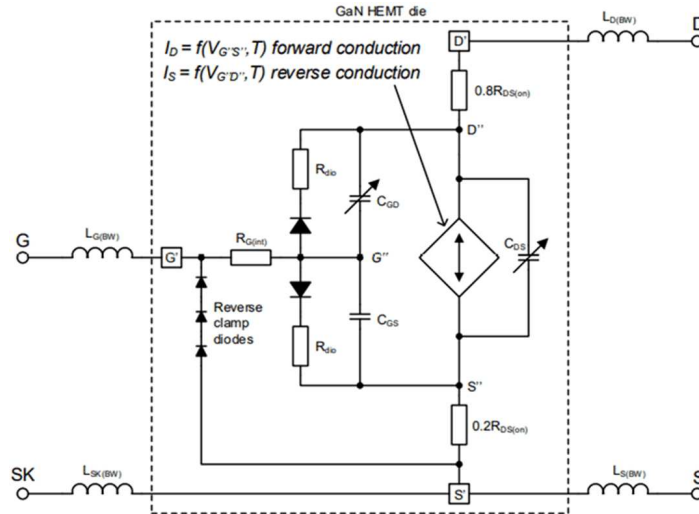
Figure 2.32: Electrical Model of a P-gate GaN HEMT.

Due to the special device structure, it is not feasible to specify a single externally measured gate-source voltage that will properly enhance the gate under all variations of temperature and drain current. For example, at high temperature and maximum drain current, a V_{gs} of 4 V may be just enough to keep the device on and result in a gate current of 10 mA. But at a lower temperature and zero drain current, the same applied V_{gs} could result in hundreds of milliamps of unnecessary gate current. Moreover, specifying an absolute maximum gate voltage is not appropriate due to the drain current and temperature dependency. Therefore, the nominal and maximum gate voltages in the forward direction are not specified: only the gate current is specified, as the internal gate diode will clamp the voltage to a safe level even at the maximum specified gate current.

Based on these special characteristics, a novel gate drive circuit integrated with a RC network is applied in the SM gate drive circuits. The inserted RC network acts as a high pass filter. It offers a low impedance path for fast signals, whereas slow signals experience a significantly higher resistance. Therefore, the device is being

turned on and off with a high current (several hundreds of milliamps) whereas the steady-state current, which is needed to keep the device in the on-state, is limited to a few milliamps. That is to say, a three-level gate current profile can be achieved on a standard two-level gate driver. The illustration schematic is shown in Fig. 2.33.
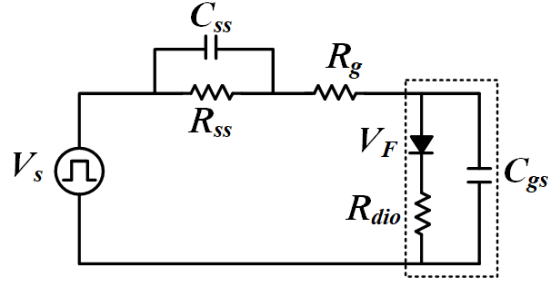
Figure 2.33: Illustration Schematic Gate Drive Circuit with RC Network.
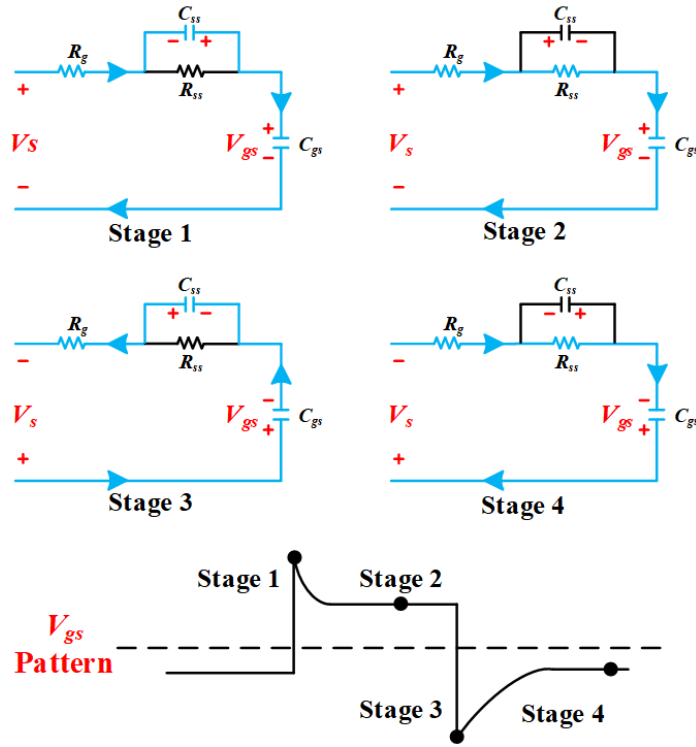
Figure 2.34: Circuit States under Different Switching Stages.

As shown in Fig. 2.34, during the turn-on transient at stage 1, the gate current

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will flow into the C_{ss} other than the R_{ss} and thus the V_{gs} can be calculated as:

$$V_{gs} = V_s - I_g(t) \times R_g + V_{Css}(t) \tag{2.34}$$

The $V_{Css}(t)$ is added to the initial gate-source voltage while the energy stored in C_{ss} is transferred to C_{gs}. Therefore, the gate current is temporarily boosted and increases the dv/dt in GaN switching transient. After C_{ss} is fully discharged and Vgs reaches the rating value at stage 2, the gate current is transferred from C_{ss} to R_{ss}. It should be noted that the voltage polarity on C_{ss}/R_{ss} branch is reversed at steady on state. Therefore, the V_{gs} can be calculated as (suppose the internal diode is not conducting):

$$V_{gs} = V_s - I_g(t) \times R_{ss} - I_g(t) \times R_g \tag{2.35}$$

At turn-off period at stage 3, when the negative V_s voltage is applied, the $V_{Css}(t)$ is also added to the V_s voltage and help discharge the C_{gs} together. Therefore, a negative clamp voltage across the gate-source can be achieved and calculated using Eq. 2.34. Meanwhile, the C_{ss} will also be discharged by R_{ss} until zero voltage. This ultimate voltage value can be zero because there is no gate current flowing in gate loop during steady off state. Therefore, the ultimate V_{gs} at stage 4 exactly equals to the V_s. Finally, the developed gate drive circuit for GaN device is shown in Fig. 2.35.

As discussed above, the developed gate drive circuits can minimize the required gate current at different periods and thus the gate loss can be reduced. The second benefit is the higher dv/dt during the switching transient, which means less switching loss because the switching transient time is shortened. The third benefit compared to the traditional two-level gate drive circuit is the good immunity on cross talk effect.
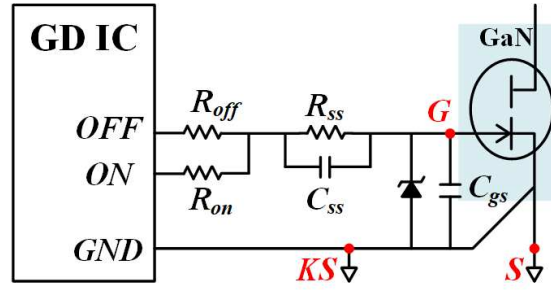
Figure 2.35: The Developed Gate Drive Circuit with RC Network.

The temporary negative voltage clamp can effectively overwhelm the induced voltage boost on the gate-source voltage during the transient period.

Since the gate drive of GaN device is very sensitive to the parasitic, especially under high dv/dt in our case, the voltage oscillation on both gate-source voltage and drain-source voltage needs to be well suppressed in case of any false trigger. Although the negative voltage clamp can increase the tolerance of the induced voltage oscillation, it is far from enough. In a word, the voltage oscillation must be effectively damped and suppressed. One effective way is to use decoupling capacitor, which can provide an alternative and short path for this high frequency ripple current and thus reduce the voltage oscillation. Lets focus on the equivalent circuit model of the circuits including gate loop and power loop, as shown in Fig. 2.36. During the switching transient, the loop parasitic, such as L_{par} in power loop and L_s in gate loop, will respectively resonate with junction capacitance or the gate-source capacitance. Therefore, minimizing the parasitic inductance in loops is of great importance to suppress the voltage oscillation.

Three major loops that suffer from voltage ringing are taken into consideration: main power loop, gate drive loop and gate power supply loop, as shown in Fig. 2.36. As for the main power loop, these capacitors are designed to vary from 0.1 nF to 1 μF, as listed in Table 2.4, to filter out the high frequency noise. 2 - 4 ceramic
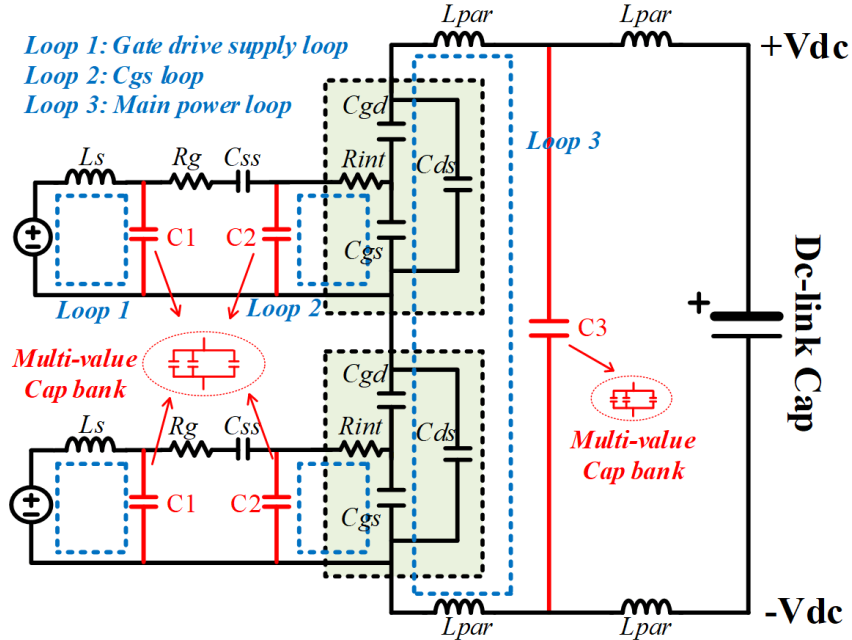
Figure 2.36: Derived Equivalent Circuits Model with Added Multi-value Decoupling Capacitor Banks.

capacitors with same capacitance are placed in parallel to enhance the performance. The decoupling capacitor bank on power loop are placed as close as possible to the switching stage to maximally reduce the main power loop parasitic inductance. As for the gate drive loop, extra gate-source capacitors are added to stabilize the gate voltage during the switching transient. Since the gate drive loop length should be short and take up limited space on board, the required capacitance should be relatively low and the total volume is also limited. Therefore, these capacitors are designed to vary from 10 pF to 1 nF and the package of which is 0603, as shown in Table 2.4. As for the gate power supply loop, multi-value decoupling capacitors are indispensable because the DCDCs to supply the gate drive power are placed not close to the gate drive loop. The power supply loop is sacrificed a little bit since the gate drive loop is the top priority to optimize in the circuit layout. Therefore, these capacitors should be placed right next to the gate drive loop to minimize the power supply loop for

the gate drive. That is to say, the return path of the gate current is much shortened. Under low dv/dt, this strategy may have limited effect. However, under high dv/dt in our case with high speed GaN device, the improvement on damping gate loop ringing is significant. The selected capacitance varies from 10 pF to 10 nF as also listed in Table 2.4.

Table 2.4: Multi-value Decoupling Capacitor Bank of Different Loops

Loop	Capacitor bank setting	Total capacitance
Main power loop	100 nF x 3 6.8 nF x 5 1 nF x 5 100 pF x 5 10 pF x 5	339.55 nF
Gate drive loop	1 nF x 1 100 pF x 1 10 pF x 1	1.11 nF
Gate drive power supply loop	10 nF x 3 1 nF x 1 100 pF x 1 10 pF x 1	11.11 nF

Combining all the design considerations discussed above, the novel SM integrated with CLLC resonant circuit is developed and presented in Fig. 2.37.

2.6.4   Arm Inductor Selection Methodology

To find the resultant voltage induced by a current harmonic in the circulating current, the arm current equation discussed before can be reshaped with following
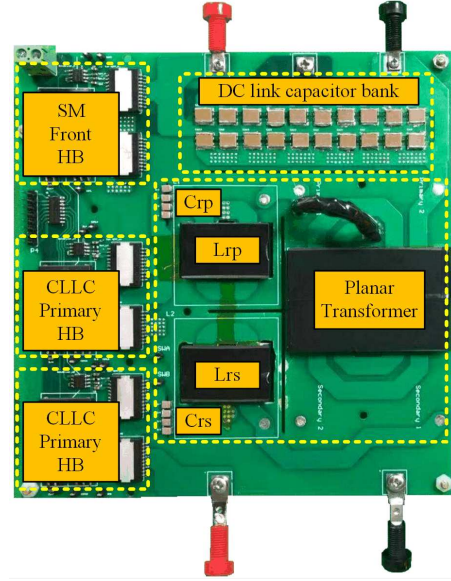
Figure 2.37: Newly Proposed Novel SM Prototype for MIMC.

assumption, as shown in Eq. 2.36.

$$i_{\text{up}}(t) = i_{\text{up}}(t) = \sum_{h=2}^{n} I_{\text{h}} \cos(h\omega t + \phi_{\text{h}}) \tag{2.36}$$
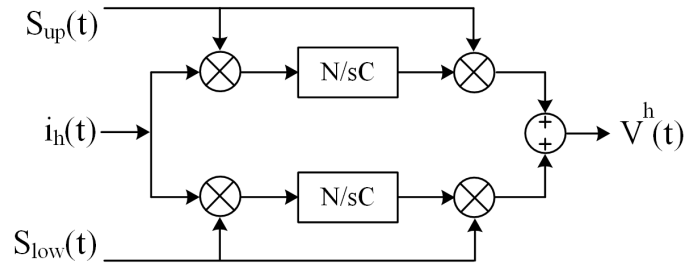
Figure 2.38: Arm Converter Voltage Derivation Diagram.

By repeating the calculation of arm converter voltage shown in Fig. 2.38, the ultimate expression of circulating current produced voltage is presented in Eq. 2.37:

$$v_{\text{h}}^{h} = \frac{N}{2\omega C} \left(\frac{M_0^2}{h} + \frac{hM_1^2}{2(h^2 - 1)} + \frac{hM_3^2}{2(h^2 - 9)} \right) I_{\text{h}} \sin(h\theta + \phi_{\text{h}}) \tag{2.37}$$

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Therefore, the impedance of the arm converter can be derived:

$$Z_{\mathrm{h}} = \frac{V_{\mathrm{h}}^h}{I_{\mathrm{h}}e^{(j\theta_{\mathrm{h}})}} = \frac{N}{2j\omega C}\left(\frac{M_0^2}{h} + \frac{hM_1^2}{2(h^2-1)} + \frac{hM_3^2}{2(h^2-9)}\right)I_{\mathrm{h}}\sin(h\theta + \phi_{\mathrm{h}}) \qquad (2.38)$$

The equivalent impedance of one phase leg is equal to the sum of Z_{h} and the impedance of two arm inductors. The major harmonic voltage in the phase leg generated from the fundamental frequency arm current is the ac component in the V_{h}^e in Eq. 2.24. If involving the arm inductor, the related block diagram of whole phase leg can be derived as shown in Fig. 2.39.
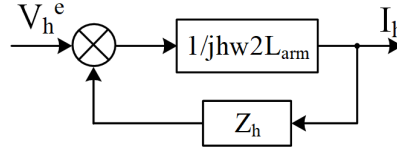
Figure 2.39: Block Diagram Between Arm Converter Voltage and Current.

According to the block diagram, the related transfer function is then presented in Eq. 2.39:

$$I_{\mathrm{h}} = \frac{V_{\mathrm{h}}^e}{1 - \frac{N}{\omega^2 L_{\mathrm{arm}}C}\frac{2(h^2-1)M_0^2 + h^2 M_1^2}{8h^2(h^2-1)h}} \qquad (2.39)$$

The denominator in Eq. 2.39 sends out a message that the circulating current harmonics can get very high value regardless of the excitation voltage in case when the following condition is met:

$$1 - \frac{N}{\omega^2 L_{\mathrm{arm}}C}\frac{2(h^2-1)M_0^2 + h^2 M_1^2}{8h^2(h^2-1)h} = 0 \qquad (2.40)$$

Therefore, to prevent the resonance, the arm inductor along with the arm capacitance should be carefully sized so that:

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$$L_{\mathrm{arm}}C > \frac{N}{\omega^2 L_{\mathrm{arm}}C} \frac{2(h^2-1)M_0^2 + h^2 M_1^2}{8h^2(h^2-1)h} \tag{2.41}$$

In traditional MMC topology, the most critical case is for the lowest circulating current harmonic, which means the second order harmonic. Therefore, set the harmonic order (h) as 2, the equation becomes:

$$L_{\mathrm{arm}}C > \frac{N}{\omega^2} \frac{3M_0^2 + 2M_1^2}{48} \tag{2.42}$$

However, this may end up with a very bulky inductor. To reduce the passive size, the inductor can be sized for h = 4. Meanwhile, the second harmonic circulating current can be suppressed using the circulating current control of the converter. Besides the circulating current suppression, inrushing current limitation during the dc fault is another tough task of arm inductor. Three general possible fault modes of MMC are shown in Fig. 2.40. Aimed at these fault cases, different equivalent circuit models can be derived to help determine the required inductance to limit the huge surge current. Theses short circuit loops may involve single arm inductor or both of them and the related equations the fault current di/dt in three fault cases are listed in Eq. 2.43 to 2.44. Therefore, the required inductance that can achieve mild fault current change slope can then be determined, which should be able to cover all three cases. This value is then compared with the one got from Eq. 2.42 and the larger one becomes the ultimately optimized inductance selection.

$$Model1 : \frac{di_{\mathrm{SC}}1}{dt} = \frac{\frac{V_{\mathrm{dc}}}{2} + \sqrt{\frac{2}{3}}V_{\mathrm{LLrms}}}{L_{\mathrm{arm}}} \tag{2.43}$$

$$Model2 : \frac{di_{\mathrm{SC}}2}{dt} = \frac{\frac{V_{\mathrm{dc}}}{2} + \sqrt{2}V_{\mathrm{LLrms}}}{L_{\mathrm{arm}}} \tag{2.44}$$
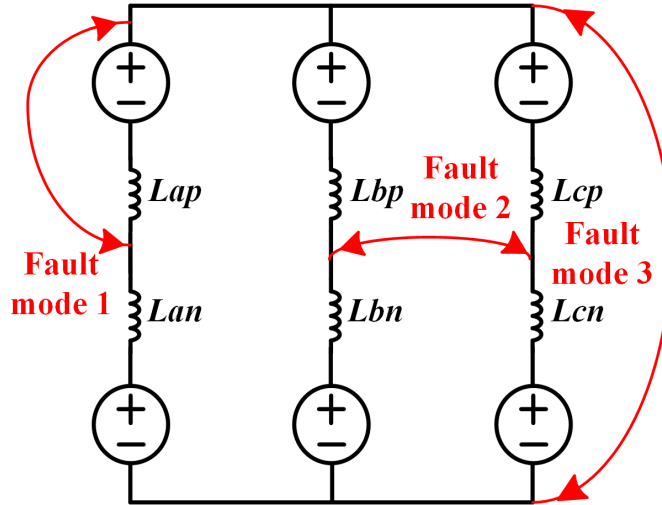
Figure 2.40: Short cCircuit Fault Modes of MMC.

$$Model3 : \frac{di_{\mathrm{SC}}3}{dt} = \frac{V_{\mathrm{dc}}}{2L_{\mathrm{arm}}} \tag{2.45}$$

2.6.5 Development of Central Controller Integrated with Fiber Optics

Central Controller Development

The realization of multi control objectives requires the cooperation between multi controllers so that the control bandwidth can be maximized. However, multi controllers introduce new challenges: (1) hierarchy of controller architecture allocation to ensure the effective cooperation; (2) timing cooperation between controllers. Asynchronized operation surely results in chaos of whole control algorithm, which leads to the ultimate wrong command output.

To maximize the control bandwidth and reduce the control cycle, the System hierarchy should be as less as possible to reduce the intermediate decision part. On the other hand, simplified control architecture means more task is allocated on each controller which means more calculation to do. The common design of central control architecture includes two level control and three level control. Three level design is

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usually applied for MMC with hundreds of cells. Besides the control complexity, the major challenge is the synchronization of different controllers from different levels. As the developed MMC platform only contains 12 - 18 submodules, two level control is enough to handle all the control process. Therefore, the central control system consisting of central DSP, central FPGA and local FPGA is demonstrated in Fig. 2.41, which also gives a general function division.
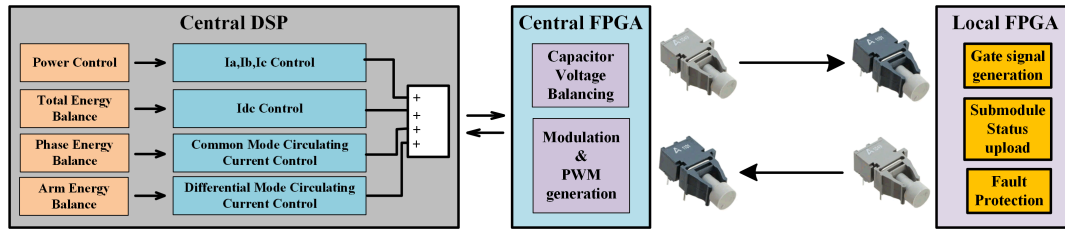
Figure 2.41: Control Architecture of Central Controller.

The central DSP TMS320F28335 from TI company is mainly in charge of the whole current control algorithm and arm reference command generation. Then the different outputs from different control loops are combined to form the ultimate reference commands for six arm converters. After that, the command is transmitted to central FPGA to do further modulation. Besides, the ADCs in DSP are used to sample the six arm currents, output three phase ac currents and dc bus voltage. These analog signals are acquired by the sensor system. After filtering and conditioning, these processed signals are transmitted to the DSP. The central FPGA are responsible for the submodule voltage balance control, gate command generation and submodules status data upload.

The central FPGA acts as the bridge between the central DSP and submodules. The data package, which contains the SM status such as voltage, current and temperature, is sent to the central FPGA. The preliminary response to these data packages is judging if each SM is in good condition. Once abnormal status, such as over voltage,

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over temperature or over current is triggered, shut down signal will be sent to all SM-s. If everything works fine, the central FPGA further uploads all the data to central DSP to finish the close loop control for the next cycle. Meanwhile, once receiving the reference commands from central DSP, the central FPGA starts the gate signal generation process. First, the FPGA determines how many SMs are required in each arm according to the received reference command. Second, the ever-ongoing voltage balance control delivers the sorting results of all SMs in each control cycle. Finally, combining these two results, the central FPGA determines the SMs to be kicked in or bypassed and send out the relative gate command to each SM.

The local FPGA is the brain of SM as it does the following jobs: (1) responses to the gate command from central FPGA and generates ultimate gate signal integrated with dead time to drive all half bridges; (2) cooperates with the sensor circuits at SM and collects the SM status information (capacitor voltage, device current and device temperature) and uploads to the central FPGA; (3) fast reacts to the local fault such as over voltage fault and over current fault.

Due to the frequent and redundant information exchange between the central DSP and central FPGA, these two brains need to be close to each other as much as possible. By doing so, the short communication distance can minimize the parasitic inductance and reduce the bit-error-rate and reduce the effect. Moreover, it also minimizes the influence from environmental noise such as radiated noise from power switching stages. Therefore, the central DSP and FPGA are integrated together on a single controller board. On the other hand, the central controller needs to interface with plenty of SMs and sensing circuits at the same time, which leads to the high demand for digital controller resource. That is to say, the central FPGA need to leave sufficient I/O ports. Reference to the industrial controller design, the DSP+FPGA based central controller also adopts the concept of modular design, as shown in Fig.

2.42.
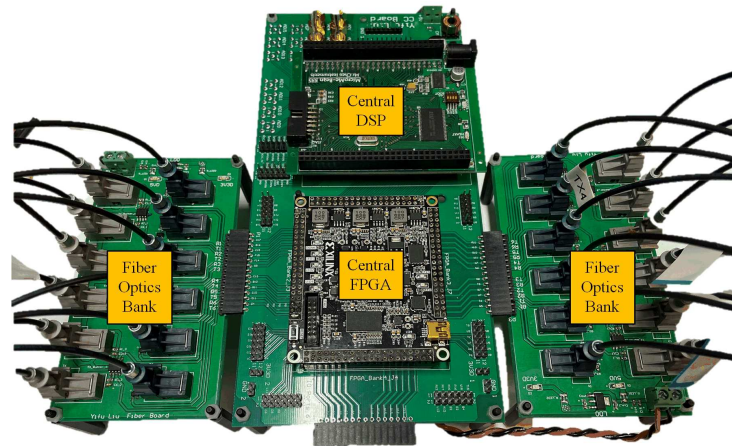
Figure 2.42: Developed Central Controller Board.

In real lab environment, the central controller is usually far away (> 5 m) from the SMs to reduce the effect from EMI noise. As a result, any communication using insulated wires will get seriously distorted by the parasitic. Under this situation, the fiber optic tends to be a good solution to long distance communication platform because it features the high noise immunity, easy connecting, compatible with standard TTL circuitry and adjustable distance links. The only draw backs are the volume and the cost, which are not the concern in lab environment. Therefore, the HFBR series are selected since they are excellent for solving problems with voltage isolation/insulation, EMI/RFI immunity or data security.

The complete link of HFBR fiber optic includes a transmitter and a receiver. The transmitter incorporates a 660 nm LED while the receiver includes a monolithic dc coupled, digital IC receiver with open collector Schottky output transistor. Moreover, a shield has been integrated into the receiver IC to provide additional, localized noise immunity. The typical interface circuit is shown in Fig. 2.43.

On the transmitter side, as the I_F modulates the internal LED, the cable distance becomes an important factor when sizing the I_F because the LED signal inside the

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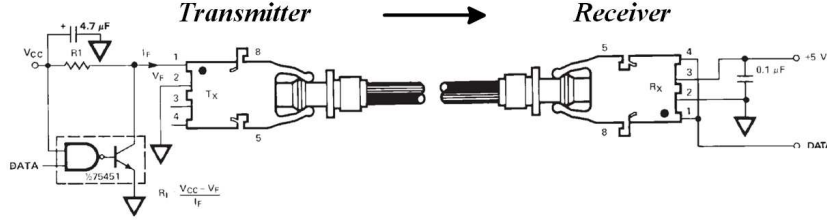
Figure 2.43: Interface Circuit of HFBR Fiber Optic.

cable decades with the distance. However, this I_F needs to be strictly restricted within the SOA or the lifetime of the transmitter will be affected. Moreover, longer distance means larger propagation delay of the communication. Therefore, the R_1, which can be estimated using Eq. 2.46, need to be flexibly adjusted to achieve the desired I_F.

$$R_1 = \frac{V_{CC} - V_F}{I_F} \tag{2.46}$$

Ultimately, the communication between the central FPGA and the local FPGA of each SM is carried by the fiber optics with 5m long cable. For each phase, a standalone fiber optic board is developed and interfaced with the central controller board as shown in Fig. 2.42. The propagation delay of this communication is controlled within 40 ns regardless of the filter circuits.

SM Controller Development

As can be noticed that the SM controller part is missing in the SM prototype figure shown in Fig. 2.37. This is because the modular structure is adopted in the hardware development to increase the fault tolerance. Another benefit is the easy and convenient debug process.

The compact SM controller board, which integrated with gate drive function, communication function and sensing function, is presented in Fig. 2.44. The local FPGA is placed quite close to the fiber optics and the voltage sensor to minimize the
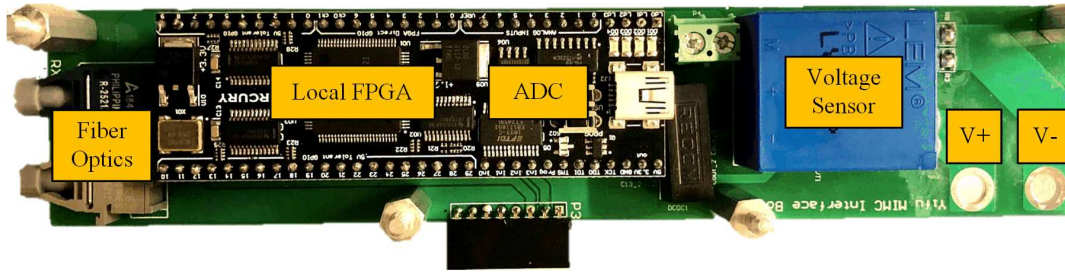
Figure 2.44: SM Controller Card.
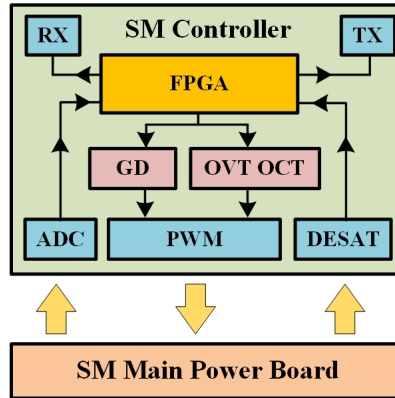
Figure 2.45: SM Function Illustration Map.

trace length. All the peripheral auxiliary circuits, such as condition, communication ICs, power supply ICs and filter circuits are located right below the FPGA. A detailed function illustration map is shown in Fig. 2.45. After collecting data from voltage sensor, the FPGA will first judge if it triggers the over voltage protection. Then, it will send the voltage data out through the transmitter of fiber optics. Meanwhile, the local FPGA keeps sensing the receiver link to acquire the gate command for the front HB of MIMC SM. As for the CLLC resonant circuit, the local FPGA generates a 500 kHz square wave with 0.5 duty cycle and sends to the gate driver ICs on SM through the connectors. It should be noted that all the filters for gate signal is placed right by the gate driver IC side. These filters can damp the high frequency noise induced by the long trace between the SM control card and SM itself. Also, it provides enough immunity for common mode noise induced by the switching stages.

High-Speed High-Accuracy Communication System Development

The communication between two controllers requires either bidirectional or unidirectional data transfer from one port to the other. In a digital communication system of industrial application, there are general two methods widely applied: parallel communication and serial communication. The crucial difference between these two popular communication protocols is that in serial communication only one communication link is employed to finish the data transfer from one end to the other. As against in parallel communication, multiple parallel links are used that transmits each bit of data simultaneously. A detailed comparison between serial communication and parallel communication is listed in Table 2.5.

Table 2.5: Comparison Between Serial Communication and Parallel Communication.

Specs	Serial communication	Parallel communication
Transmission speed	Slow	Very fast
Number of links	1	n for n bits
Number of bits per cycle	1	n for n bits
Cost	Low	High
Effective distance	Long	Short
Crosstalk	No	Yes
High frequency operation	More efficient	Less efficient

At first glance, the parallel communication seems to be always faster on data transmission. For example, if transmitting a 10 bits data, the parallel communication can finish the task in one cycle at a cost of 8 links, which is an acceptable cost. In contrast, the serial communication takes 10 cycles to send out all the bits with single link. Simple arithmetic seems to show that the parallel communication can

transmit 10 times as fast as the serial communication. However, parallel data ports suffer extremely from inter-symbol interference (ISI) and noise, and thus the data can be corrupted over long distance. Moreover, since the wires in parallel communication are usually close attached, small amounts of capacitance and mutual inductance exist and generate high frequency noise. As a result, the bandwidth is much smaller compared to the serial communication, which means worse bit rate and the communication efficiency is affected. Also, more noise means that the transmission has to be conducted with a low Signal-to-Noise Ratio (SNR), which increase the fault bit ratio and reduce the communication quality. However, if using serial communication with differential wires, the SNR can be boosted and the whole system manages to achieve a higher bit rate without suffering from the noise.

In a conclusion, the optimal communication protocol should be carefully considered and analyzed according to specific experimental application. Generally speaking, the parallel communication is more suitable and faster in short distance transmission while the serial communication is the better choice in long distance communication. In the developed MIMC platform, the parallel communication is applied for the information exchange between the central DSP and central FPGA. Since both controllers are located on the same board, the communication wires are based on short and wide PCB trace. Therefore, the distance, parasitic inductance and capacitance are all minimized. Also, the sufficient data ports on both controllers provide strong support. The serial communication is employed in the data exchange between the central FPGA and local FPGA because these two are usually far away from each other. On the other hand, the serial communication is able to reject the common mode noise induced by the switching stage at local FGA side. The detailed development description of these two protocols are demonstrated in following sections.

To implement the parallel communication on central controller, the External In-

terface (XINTF) function of DSP need first to be activated. Generally speaking, the XINTF is mapped into three fixed memory-mapped zones. Every XINTF zone can be individually configured with unique read and write access timing and each has an associated zone chip-select signal. This chip-select signal is pulled low so that an access to that zone is currently taking place. On DSP 28335, the zone chip select signals are independent. The external address bus, XA, is 20 bits wide and is shared by all of the zones. What external address is generated depends on which zones are being accessed. The major signal descriptions that used in parallel communication are listed in Table 2.6 and the general function map is shown in Fig. 2.46.

Table 2.6: XINTF Signal Ports Introduction.

Port	Description
XD	Bidirectional 32-bit data bus.
XA	Address bus placed on the ports on the rising edge of XCLKOUT and held on the bus until the next access.
XCLKOUT	Single output clock derived from the XTIMCLK to be used for on-chip and off-chip wait-state generation and as a general-purpose clock source.
XWE/XRD	Active low write/read strobe, flag to determine the write or read process.
XZCS6/7/0	Zone chip-selects.

The general process of one communication cycle of XINTF can be described as follows: First, the chip-select XZCS6 determines the work zone and the address information will be placed on ports through XA; Second, the mode selection XRD or XWE will be pulled down to decide whether to read (receive data) or write (send out data) for this cycle; After sensing the low XRD or XWE signal, the data will be placed on ports through XD. During this period, the data transmission is finished.

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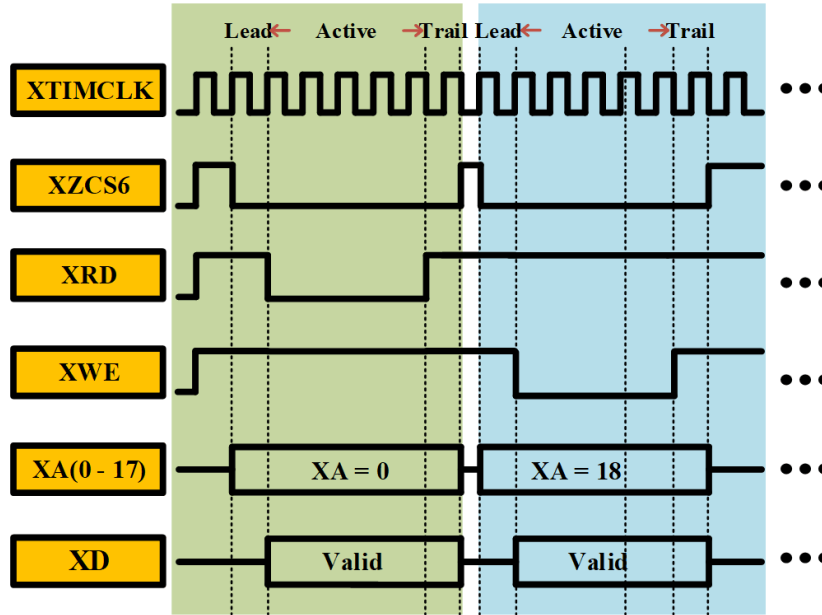
Figure 2.46: XINTF Function Map.

After fixed time (the active period), the mode selection XRD or XWE will return high to send out the end signal. Finally, the chip select XZCS6 returns high and formally terminate the whole write or read cycle and wait for the next cycle.

As the XINTF in DSP 28335 is already packaged as a standard function module, the only thing left for user to do is configuring different setting registers. Among these registers, the clock cycle time in XTIMCLOCK and active time during the data transmission are the two value that can be optimized according to communication result. These two can be pushed to extremely small if excellent noise immunity and parasitic minimization is achieved. In this way, at least on DSP side the communication speed reaches the fastest level.

If regarding the central DSP as the master controller because of the XINTF function, the central FPGA plays the role of slave controller. Unlike the DSP with highly modular and integrated function block, the central FPGA provides huge space for personized and customized function design. In this case, the central FPGA need to

simulate the function of XINTF in order to cooperate with the central FPGA. Two important notes should be highlighted. First, the time clock of two controllers must be synchronized. Second, buffer region should be created to temporarily store the data just like a hub. The connection map is shown in Fig. 2.47, which is a standard operation. Also, the simulated XINTF function inside the central FPGA is demonstrated as a simplified block diagram.
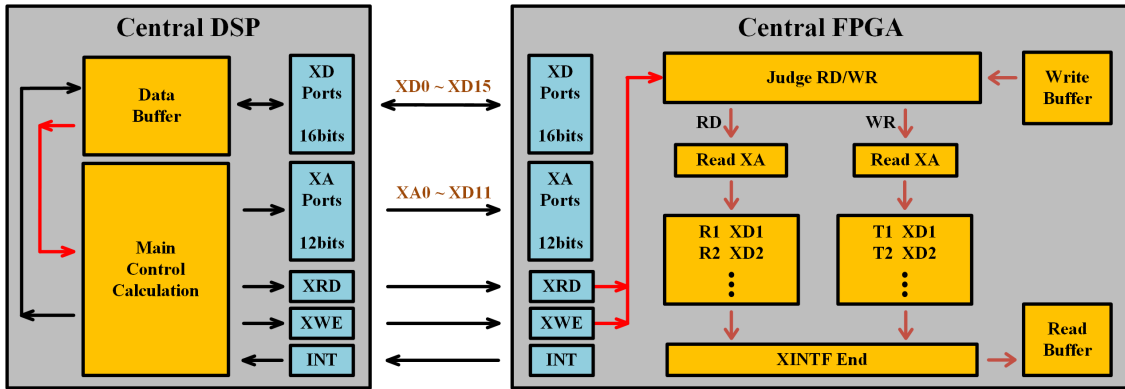
Figure 2.47: Connection Map Between DSP and FPGA.

As can be seen, the XRD/XWE that marks the operation mode need to be sensed by FPGA so that it can decide whether to implement READ operation or WRITE operation. In advance, the same address table will be recorded in FPGA to match the data with the target address. The read buffer and write buffer are separately prepared. As for the write buffer, the data to send out will be put in before the READ operation cycle starts. As for the read buffer, all the data from ports will be stored here and need to be extracted out before the WRITE operation cycle ends. Since the FPGA clock is synchronized by the XTIMCLOK from DSP, the transmission speed also reaches the fastest level at FPGA side if the simulated XINTF function can follow up the whole process on DSP side. However, as the function block in FPGA is not a modular or integrated block, it cannot be as fast as that on DSP side. Therefore, the whole parallel transmission speed is determined by the performance on FPGA side. As may

be questioned, two DSP should be the better choice compared to the DSP+FPGA structure. This is true but not a possible case in MMC platform because there are not enough free I/O ports left in DSP to finish the communication with plenty of SMs. Also, if setting the DSP I/O as a free port, it is much slower compared to that in FPGA. This is because the I/O ports in DSP are already defined and integrated in different function modules. Simply toggling these I/O ports according to code result requires longer response time and thus the propagation delay is long. In conclusion, a high-performance parallel communication based on XINTF is employed in central controller. The ultimate clock frequency is set as 37.5 MHz and each communication cycle reaches 2 MHz, which is quite enough to deal with the control cycle of a 20 kHz MIMC system.

In a digital communication system of industrial application, serial communication is the process of sequentially sending data one bit per cycle through single link and is the most widely used approach to transfer information between data processing equipment and peripherals. Over the years, dozens of serial protocols have been crafted to meet needs of embedded systems. USB (universal serial bus), and Ethernet, are a couple of the more well-known computing serial interfaces. Other very common serial interfaces include SPI, I2C, and the serial standard we're here to talk about today. Each of these serial interfaces can be sorted into one of two groups: synchronous or asynchronous. The synchronous serial communication always works with a clock signal for synchronization, so all controllers on a synchronous serial bus share the same clock signal. This enables a more straightforward and faster serial data transmission, but it also requires at least one extra link between communicating controllers. Examples of synchronous communication include SPI, and I2C. The Asynchronous serial communication means that data package is transferred without the additional clock signal. This communication protocol is perfect for minimizing the required links and

I/O ports, but it is quite necessary to put some extra effort into reliably transferring and receiving data. Examples of asynchronous communication include UART, CAN and RS232. Considering the long distance and high cost of synchronization between the central FPGA and local FPGA, the asynchronous serial communication protocol is employed in MIMC case. Among different serial communication protocols, UART stands out as the optimal choice because it features low cost, no distance limitation, high speed and high customizing flexibility.

UART, or universal asynchronous receiver-transmitter, is one of the most used device-to-device communication protocols. In UART communication, two UARTs communicate directly with each other. The transmitting UART converts parallel data from a controller like a CPU into serial form, transmits it in serial to the receiving UART, which then converts the serial data back into parallel data for the receiving controller. Only two wires are needed to transmit data between two UARTs. It should be noted that UART can also be synchronized if necessary. But this also means an additional clock line is required. Data flows from the TX port of the transmitting UART to the RX port of the receiving UART, as shown in Fig. 2.48.
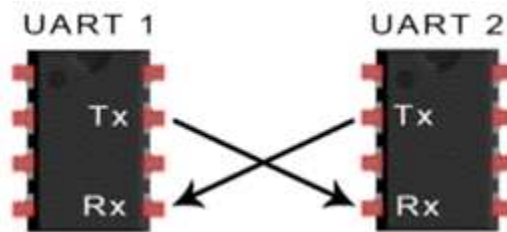
Figure 2.48: Connection Map of Classical UART.

To be more specifically, the UART that is going to transmit data receives the data from data buffer. Data is transferred from the data buffer to the transmitting module in parallel form. After the transmitting module gets the parallel data from the data bus, it adds a start bit, a parity bit, and a stop bit, creating the data packet

as shown in Fig. 2.49. Next, the data packet is output serially, bit by bit at the TX port. The receiving module of another UART decodes the data packet bit by bit at its RX port. The receiving UART then converts the data back into parallel form and removes the start bit, parity bit, and stop bits. Finally, the receiving UART transfers the data packet in parallel to the data buffer waiting for further processing.
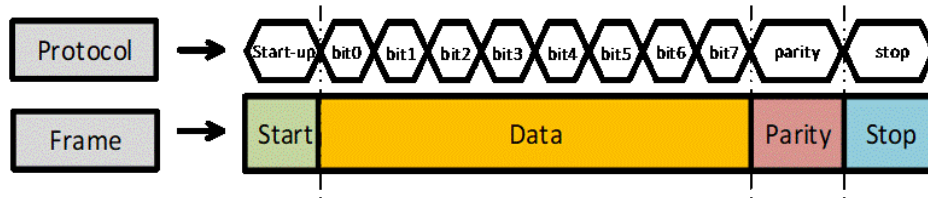
Figure 2.49: Data Package of Classical UART.

To be more specifically, lets focus on single bit level of this data packet. Each bit records either 1 (high voltage level in analog circuit) or 0 (zero voltage in analog circuit). The data value toggling between 0 and 1 presents ideally as a square wave. However, the real circuit model of data toggling between 0 and 1 should be estimated as RC network considering the existence of filter circuit. Thats to say, the data toggling presents more like a trapezoidal wave. This is quite important for the data acquisition in serial communication because it means there is a blurred region that should be avoided. In other words, the data acquisition should be hold at the wave ramp edge and be activated at the mid of the wave. This whole operation trick can be called as hold-and-sense as shown in Fig. 2.50. The hold time can be minimized by adjusting the filter parameters but the trade-off between the ringing and circuits time constant. As the data acquisition is based on level-sensing other than the edge-sensing, the tolerance of voltage ringing is pretty high. This is good for the hold time minimization and thus the whole data packet transmission time can be reduced. From the Fig. 2.50, the data sense region is also very wide and the data acquisition point is at the right mid. Theoretically, this region can be shortened according to the

experimental performance. Reduce the sense region every 10 ns until the bit error rate of data acquisition is over 5%, which is the margin of small probability event. After the optimization of these two parameters, the transmission time of this UART data packet can be significantly reduced.
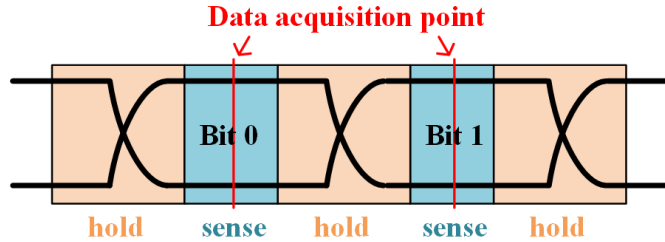
Figure 2.50: Hold-and-sense Operation.

The bidirectional communication between local FPGA and central FPGA using UART is demonstrated in Fig. 2.51. The TX and RX blocks stand for the UART coding module integrated data buffer block. The bidirectional communication is going on simultaneously and the speed is set as 3 Mbps. The local FPGA uploads the module status data and receive the gate command every switching cycle, which is also the control cycle.
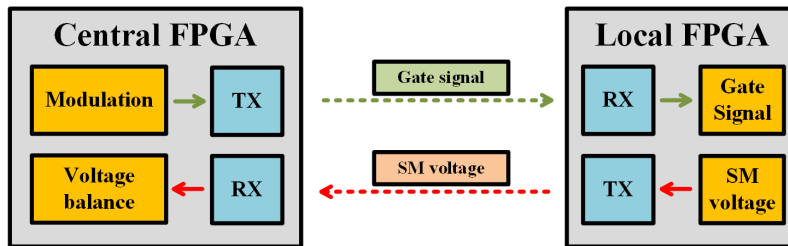
Figure 2.51: Bidirectional Communication Between FPGAs.

Voltage and Current Sensor System development

The voltage and current sensor system is another important subsystem in MIMC development because it need to collect required voltage and current data for central

controller to implement the whole close loop control. As already discussed in control section, SM capacitor voltages, output phase currents, six arm currents, dc current dc bus voltage are indispensable elements to finish the whole current control. The capacitor voltages of all SMs are necessary to finish the energy control as well as the voltage balance of each arm. Arm currents are the most important data to extracting different current components, especially the circulating current components. Also, they provide the current flow direction for the voltage balance control. Moreover, considering the three-phase unbalance problem, the negative sequence current components can also be filtered out and employ the control loop to recover the three-phase balance. DC bus voltage and current are for total energy balance between the dc side and ac side. Therefore, sensor system for the data acquisition of these control objectives is of significant importance. Since all the sensed values are of fundamental frequency ($<$ 120 Hz), the requirement on measurement accuracy and propagation delay is relatively soft. However, the main challenge lays on the isolation because the ground of different SMs are quite different but all the data share the same digital ground. Thus, an isolated sensing system is preferred. The details are discussed under this section.

As claimed, the senor system includes voltage sensor and current sensor. The voltage senor for SM capacitor voltage is built up based on LV25-P from LEM company, which is closed loop voltage transducer using the Hall effect. The LV25-P stands out due to following features: (1) excellent accuracy; (3) excellent linearity; (2) high immunity to external interference. As the TTL voltage level of micro-controller is from 0 V to 3.3 V, the conditioning circuit is required to shape the output within this acceptable range. In this MMC case, the analog output is 0 V - 5 V and a single proportional amplifier circuit is applied to do the conditioning. The simplified schematic is shown in Fig. 2.52. For voltage measurement, a current proportional

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to the measured voltage must be passed through an external resistor R_{M} which is selected according to specific demand. A filter circuit formed by R_{f} and C_{f} is followed to filter out the high frequency noise. The time constant design needs to be careful because the equal time delay is also added on the control loop. The good news is that the delay tolerance is high since the control objectives are all low frequency components. Proportional amplifier is to reshape the signal to adapt to the DSP ADC ports. Finally at the signal output, +/-5 V Schottky diode bank is employed to protect the DSP ADC ports because they are very sensitive to the voltage value.
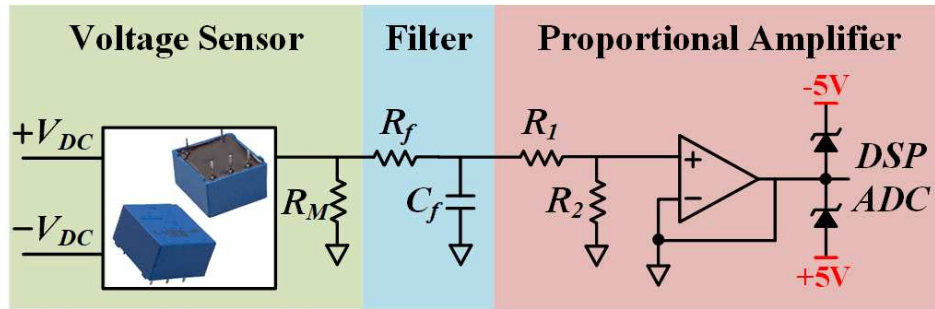
Figure 2.52: Schematic of Voltage Sensor Circuit.

As the name applies, the current sensor is used to measure the arm current and output phase current. The isolated current transducer LA35-NP also from LEM company is used to build up the current sensor system. For the current measurement, it is the same as that of voltage sensor. However, as the arm current and ac current are bidirectional, the output of current sensor is actually the positive and negative symmetry. As the ADC is not able to take care minus value, additional adder circuit needs to be integrated with the original conditioning circuit to shift the output to positive value, which is shown in Fig. 2.53.
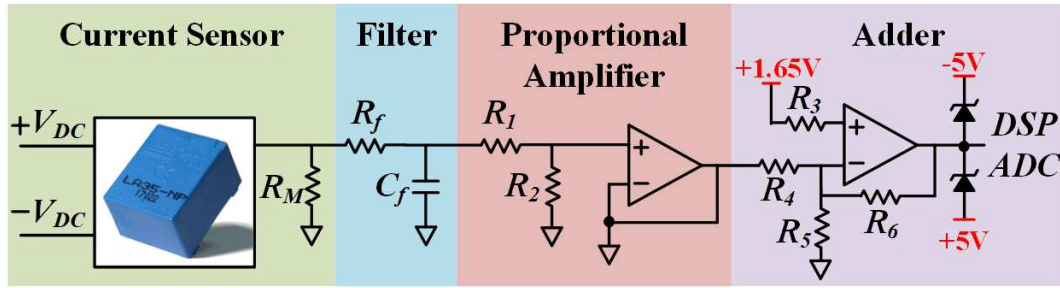
Figure 2.53: Schematic of Current Sensor Circuit.

2.7 Experimental results of porposed MIMC

The first experimental test is focused on the developed SM. The gate driving and switching performance need to be fully assessed. The front HB of the SM is configured as a buck converter and ran at 400 V / 10 A condition. The waveform of one switching period of lower device is shown in Fig. 2.54. The inserted RC work successfully increased the transient gate current. When coming into the steady on state, both the gate current and gate voltage returns to rated value. Almost zero voltage oscillation can be observed on V_{gs} and V_{ds}, which should be attributed to the well designed decoupling capacitor bank and optimized board layout as discussed in previous section.
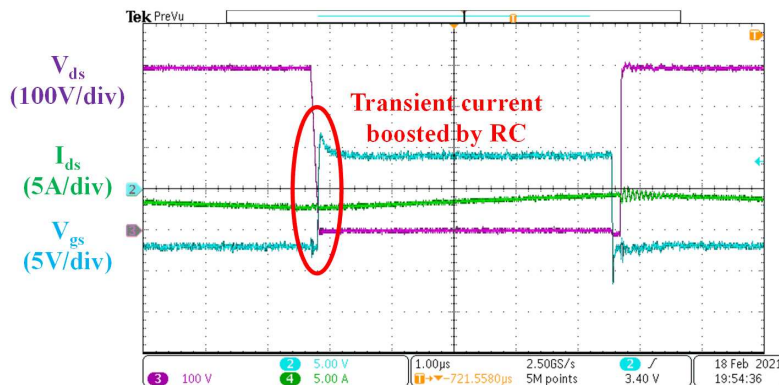
Figure 2.54: Switching Transient Waveform of Front HB of MIMC SM.

After the test of front HB, the CLLC resonant circuit, which contains other two

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HBs, is to be tested. The related operation waveforms of the CLLC are demonstrated in Fig. 2.55 and Fig. 2.56. The Fig. 2.55 is a zoom in session while the load current is zero. This happens when the load current flowing through the CLLC crosses zero. As discussed before, the load current of the CLLC is ac current that equals to the original capacitor current in the traditional MMC. In Fig. 2.55, $V_{\text{gs\_Ls}}$ represents the gate-source voltage of the low side switch; $V_{\text{ds\_Ls}}$ represents the drain-source voltage of the low side switch; V_{primary} represents the voltage on the primary winding; I_{primary} represents the current in the primary winding. The waveform of $V_{\text{gs\_Ls}}$ and $V_{\text{ds\_Ls}}$ during the deadtime demonstrates the ZVS operation. The winding current I_{primary} now equals to the magnetizing current and presents as a triangular waveform. During the dead-time period, the magnetizing current reaches the peak value and helps charge and discharge the junction capacitor to achieve the ZVS. This peak value can be adjusted by changing the magnetizing inductance to guarantee the ZVS of the HB-CLLC under all load range. Fig. 2.56 shows the waveforms when the load current is not around zero. When the current flows into the HB-CLLC channel, it gets modulated and shaped into a high-frequency sinusoidal resonant current by the resonant tank. At this time, the winding current becomes the combination of triangular magnetizing current and sinusoidal resonant current. The load current becomes zero at each turn on/off transient and the ZVS is always implemented by the magnetizing current.

The downscaled hardware platform of the proposed MIMC rated at 4.8 kW with 2 SMs per arm has been built and tested in the lab, as shown in Fig. 2.57. The experiment results with three-phase RL load are obtained and shown in Fig. 2.58 to Fig. 2.62

Fig. 2.58 shows the zoomed-out arm converter output voltage for upper and lower arms of phase A, and the output phase voltage V_{a0} at the middle point of the phase leg.
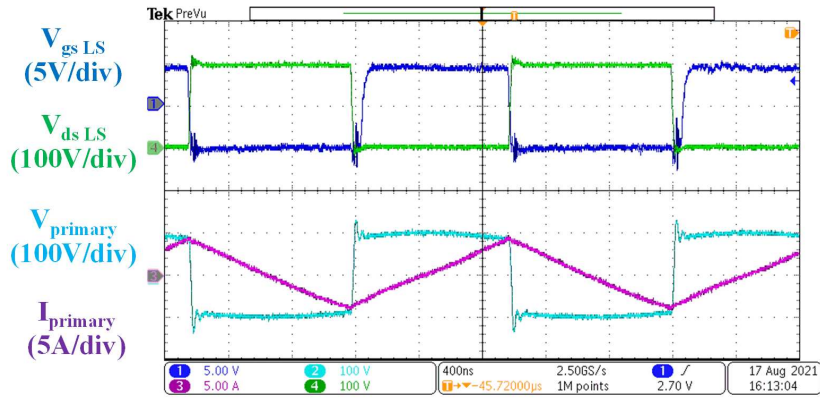
Figure 2.55: Operation Performance of CLLC Circuit at Zero Load Current.
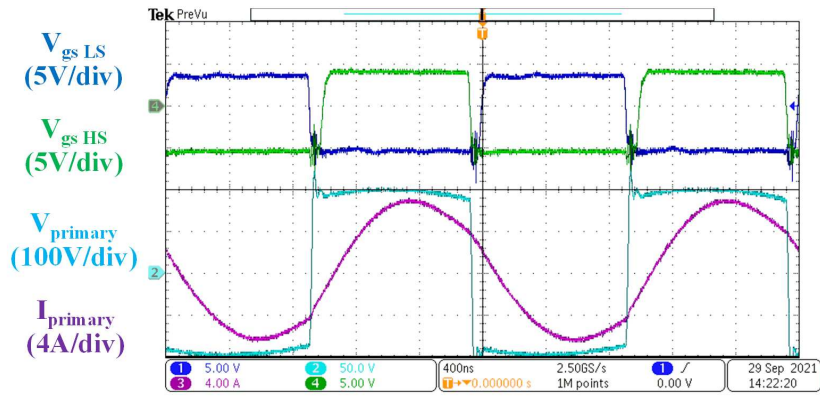
Figure 2.56: Operation Performance of CLLC Circuit with Load Current.
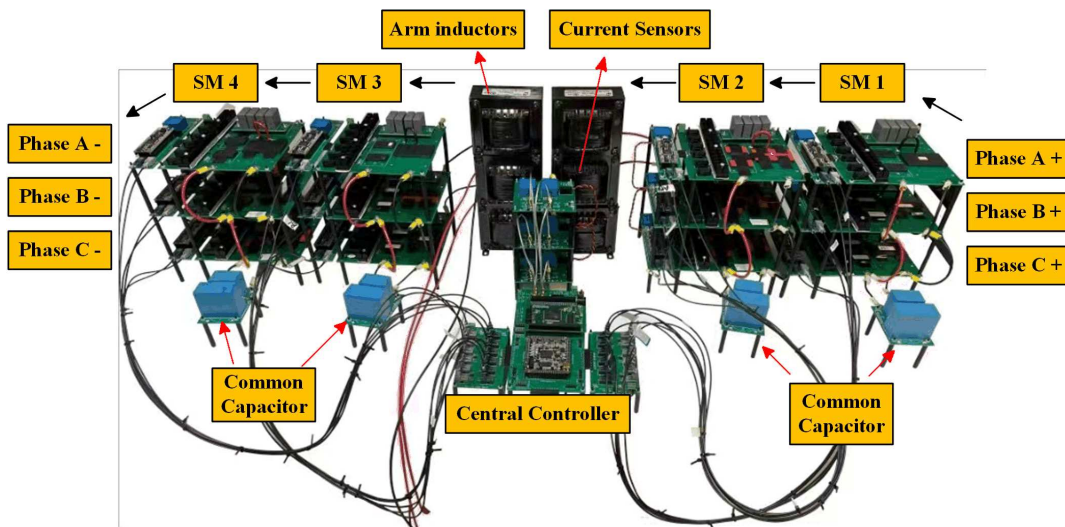
Figure 2.57: Downscaled 4.8 kW MIMC Prototype.
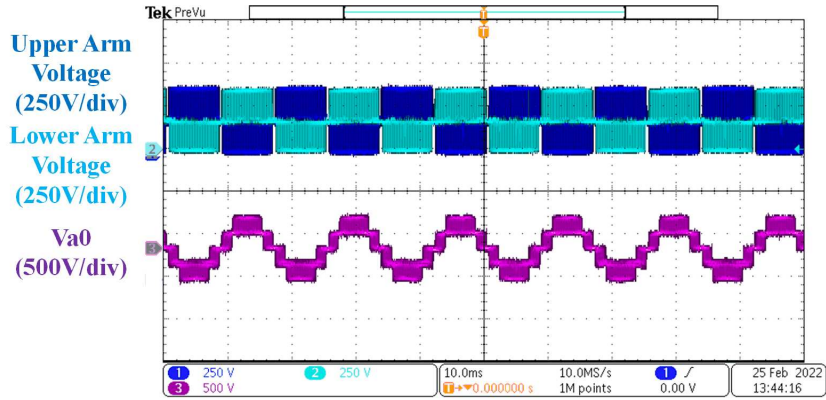
Figure 2.58: Phase Leg Voltage Performance.

The envelope of the PWM arm voltage is shown as a very flat square waveform, which verifies that the capacitor voltage in the module has no low frequency fluctuation, as claimed in the previous sections. The switching node voltage V_{a0} presents a very perfect sinusoidal multilevel waveform, which verifies that there is no second order harmonic voltage in the arm, as claimed before.
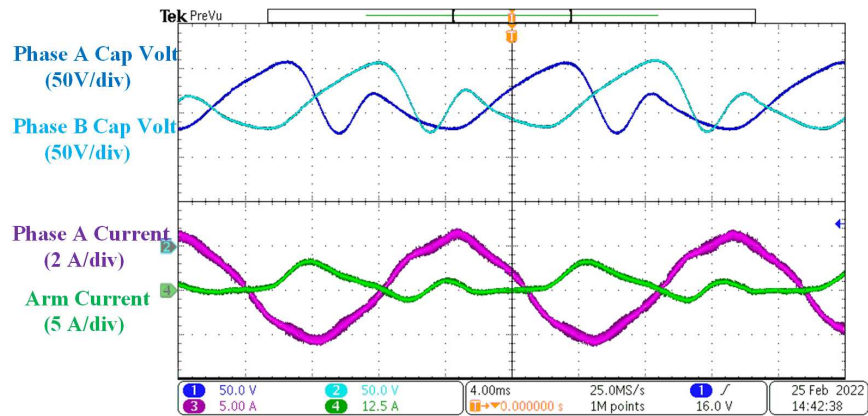
Figure 2.59: DSM Voltage Fluctuation and Arm Current Performance Comparison of Traditional MMC.

In order to present a more intuitive difference between the proposed MIMC and traditional MMC, the steady state performance of arm current and capacitor voltage for both topologies under same test conditions is shown in Fig. 2.59. 80 μF capacitor
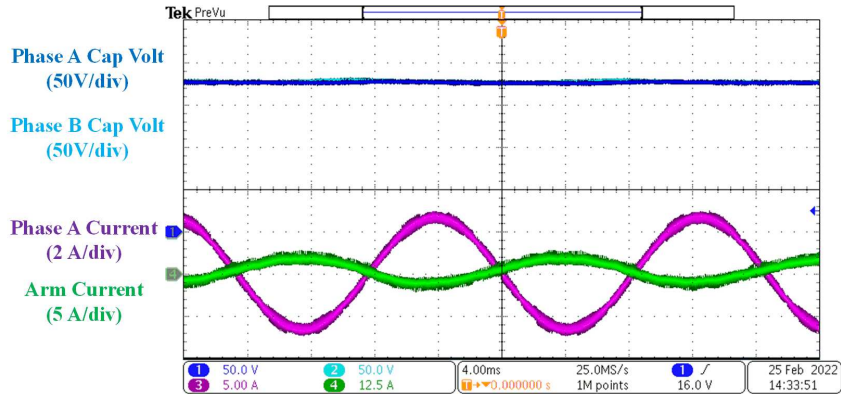
Figure 2.60: SM Voltage Fluctuation and Arm Current Performance Comparison of Proposed MIMC.

is used for MMC but only 20 μF capacitor is used for MIMC. The Fig. 2.59 presents the waveforms for the traditional MMC while the Fig. 2.60 presents the waveforms for the proposed MIMC. In each single plot, the upper two waveforms demonstrate the capacitor voltage of adjacent SMs in phase A and B. The following features can be observed: (1) the capacitor voltage in MMC has large fundamental and second order harmonic current of which the peak-to-peak value is nearly 40% of the rated voltage; but the capacitor voltage in MIMC is perfectly flat with negligible harmonics. Moreover, the capacitance in MIMC is only 25% of the capacitance in the MMC. (2) the arm current in MMC has significant low frequency harmonic distortion, but the arm current in MIMC contains very little harmonics. (3) the THD of the output current in MMC is much higher than the MIMC. These results verify the claimed benefits of MIMC over MMC: much smaller capacitance is needed to generate low THD output voltage and current.

With the amazing experimental results at 60 Hz as a basis, the experiments are further extended to variable frequency operation. Before conducting the tests, the SMs capacitance is increased to 240 μF in the MMC topology to stand huge voltage ripple under very low output frequency. But for the proposed MIMC topology, the SM

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capacitance is further reduced to 10 μF to demonstrate its prominent performance. The experimental waveforms of variable frequency operation are shown in Fig. 2.61 to 2.63. In each figure, the upper figure shows the capacitor voltage in three phases of the MMC converter; the lower figure shows the capacitor voltage in three phases of the MIMC converter. Fig. 2.61 to 2.63 show the results at output frequency equal to 30 Hz, 15 Hz and 7 Hz respectively. At 30 Hz, MMCs capacitor voltage presents a 33% peak to peak voltage ripple, but MIMCs capacitor voltage presents only 4% peak to peak voltage ripple. At 15 Hz, the MMCs ripple quickly increases to 65%, but MIMC only goes up to 8%. At 7 Hz, MMCs ripple becomes as significant as 115%, but MIMC still keeps as low as 10%. As the MIMC hardware is not a perfect circuit model, a few low-frequency current components still flow into the SM capacitor and introduce this 4% to 10% ripple. It is also noted here SM capacitance in MMC is 240 μF but that in MIMC is as small as 10 μF. When system operation frequency decreases, the SM capacitor voltage ripple MMC.

In a conclusion, as for MMC case, the side-effect of using distributed half-bridge modules to support the dc link instead of using series connected capacitor is the fundamental frequency energy ripple on the capacitor. To generate an arm voltage with low THD, a big capacitance needs to be used to suppress the ripple. In variable frequency operation, the capacitance is inversely proportional to the frequency. In order to reduce the capacitor size, the energy ripple cancellation technique through connecting the modules in three phases in parallel is adopted in proposed MIMC. Connecting the modules at different voltage potential together requires the module to be equipped with isolation. Therefore, an isolated half-bridge module is proposed to replace the original half-bridge module. By using the proposed MIMC topology, the capacitor size and the inductor size can be significantly reduced, which has been demonstrated through simulation and down-scaled experiments.
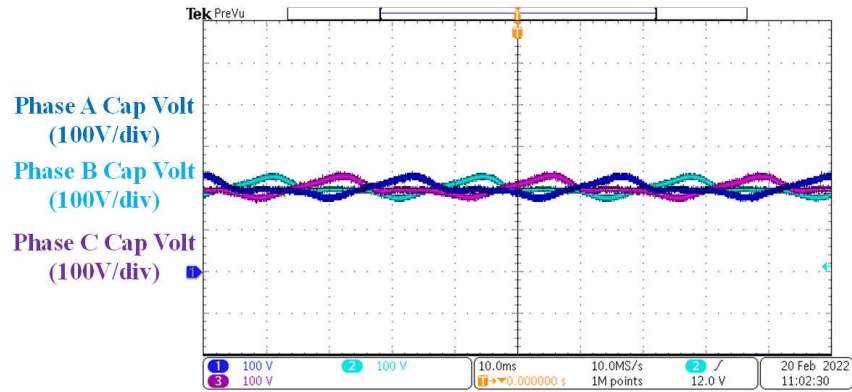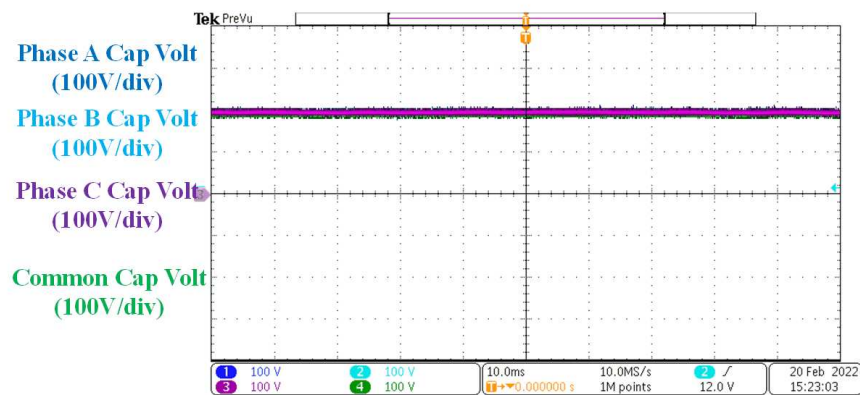
Figure 2.61: SM Voltage Fluctuation in Three Phase Legs at 30 Hz. (a) MMC; (b) MIMC.

2.8 Other Proposed Topologies for Reducing Capacitor Low Frequency Voltage Ripple Fluctuations

2.8.1 Ripple Decoupling of Modular Multilevel Converter with Flux Cancelled Three-port Converter

A new MMC topology with three-port converter that using customized LLC circuits to couple the SMs from same voltage level together. The fundamental and the second order harmonic current ripple can be eliminated as their induced magnetic flux are cancelled in the coupled core. Thus, system power density and efficiency can

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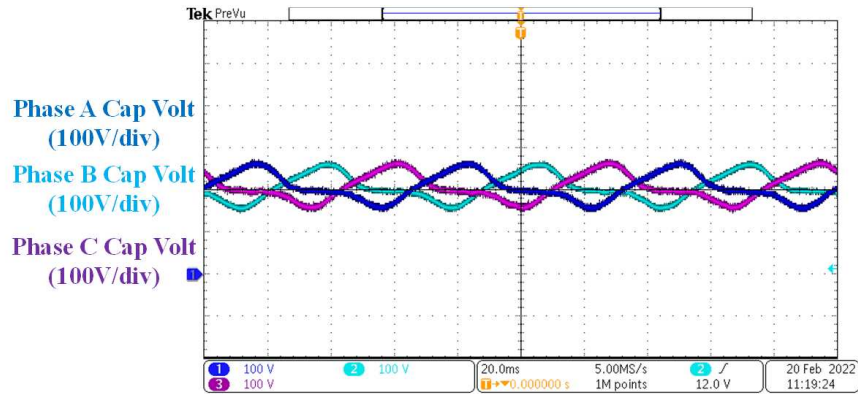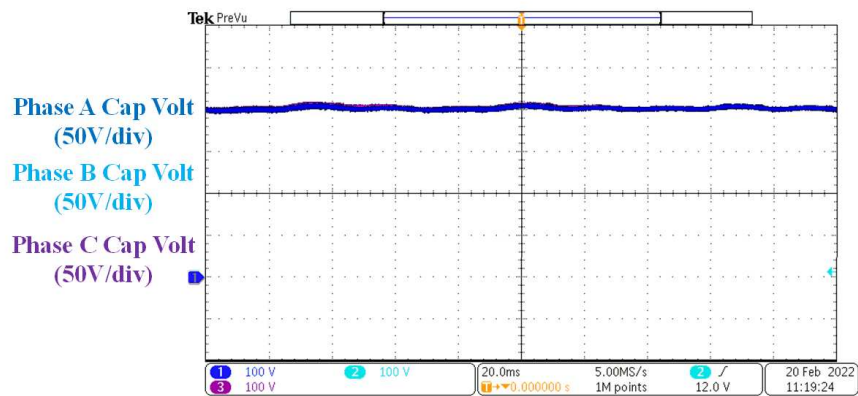
Figure 2.62: SM Voltage Fluctuation in Three Phase Legs at 15 Hz. (a) MMC; (b) MIMC.

be significantly improved since the capacitor size is much reduced.

The introduced MMC configuration topology with control-less isolation stage is shown in the Fig. 2.64. Compared with the traditional MMC, the innovative part is that the three SMs of same level in each phase are coupled through an LLC based flux cancelled three-port converter. During the normal operation, the arm current of three phase flows through each primary side winding of the three-port converter instead of the SM capacitor and generates three phase magnetic flux in the shared core. These induced magnetic fluxes can be completely cancelled in the shared transformer core
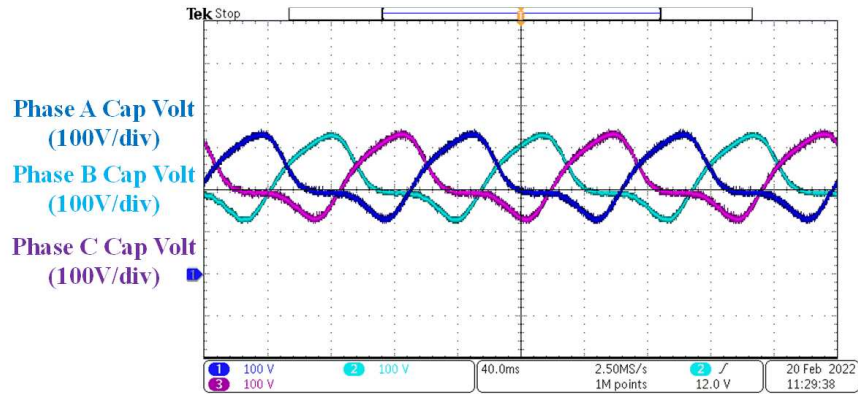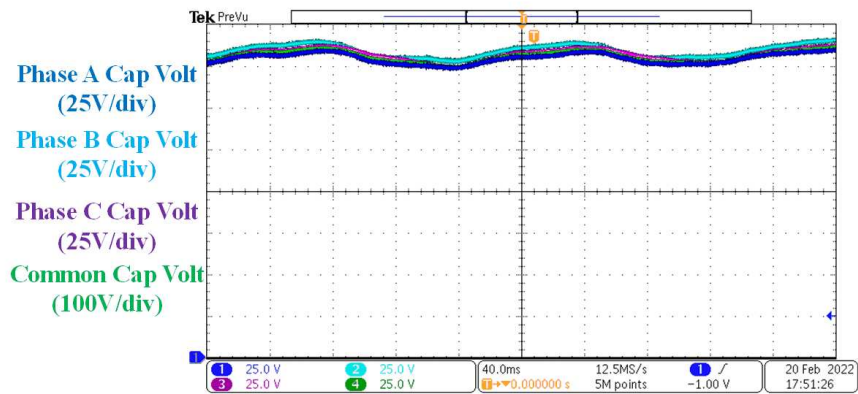
Figure 2.63: SM Voltage Fluctuation in Three Phase Legs at 7 Hz. (a) MMC; (b) MIMC.

as the vectoral sum of induced magnetic flux is zero. That is, no more low frequency voltage ripple is generated since no more low frequency current flows through the SM capacitor. Therefore, the flux cancellation ensures ripple free SM capacitor voltage and zero voltage fluctuation is effectively achieved.

The detailed topology of three-port converter coupling with three SMs on each level is shown in Fig. 2.65. Compared with traditional LLC circuits, the primary side windings of three SMs on same voltage level from three phase are coupled in the same core. The coupled LLC stages are synchronized and switching under high
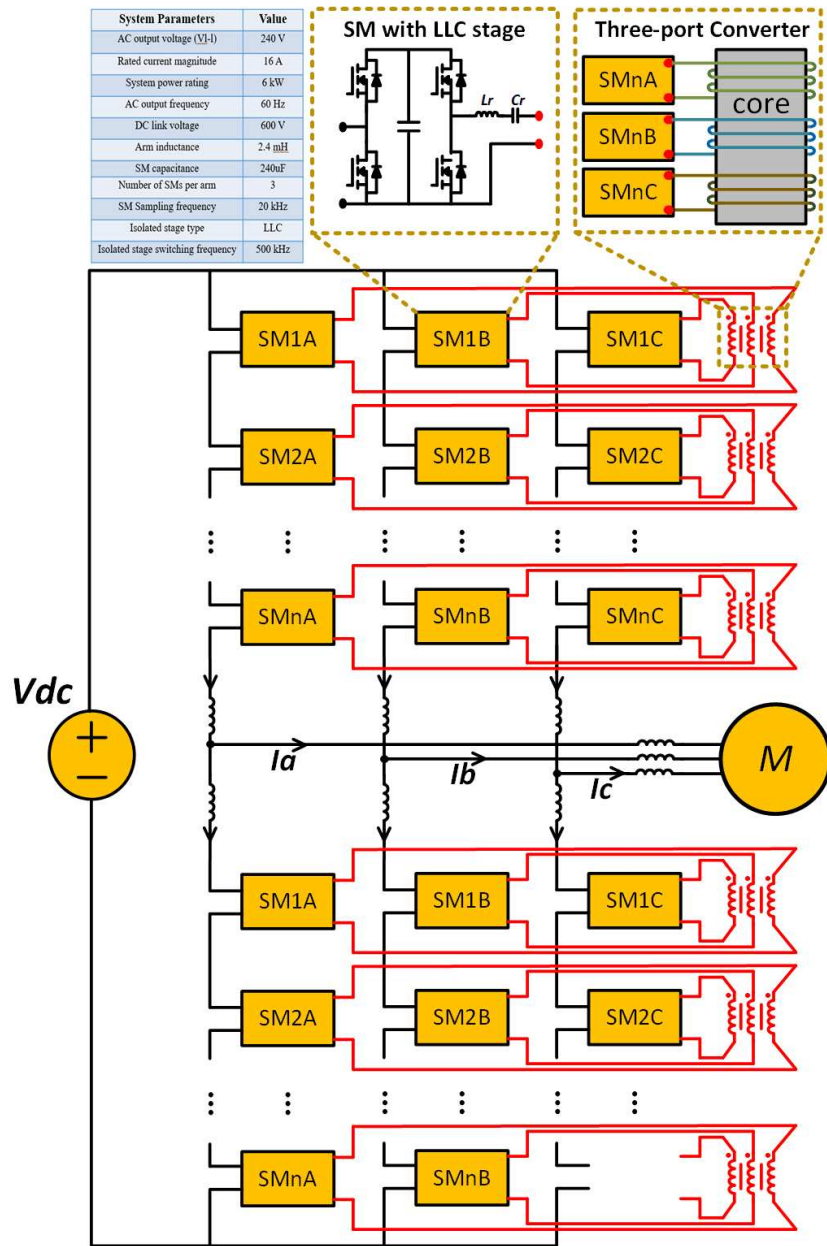
Figure 2.64: Proposed New MMC Topology.

frequency to avoid unexpected inrush current. During the normal operation, the arm current of three phase flows through primary side winding of each LLC instead of the SM capacitor. The arm current flowing through the windings generates three phase interleaving magnetic flux in the coupled core. These induced magnetic fluxes can be completely cancelled in the shared transformer core since the vectoral sum of induced magnetic flux is zero.
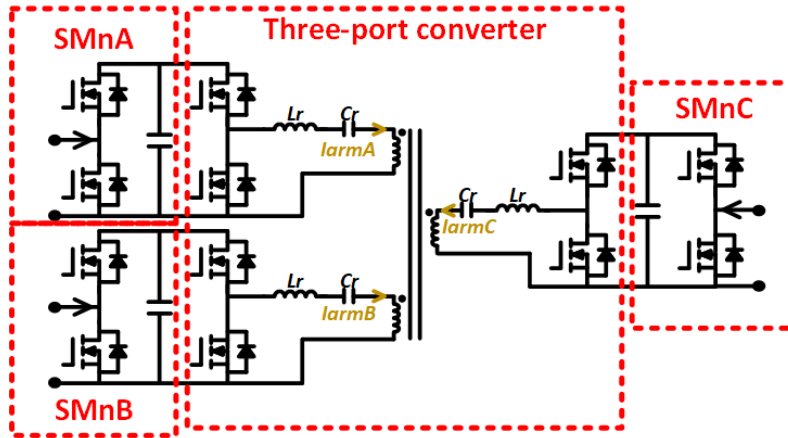
Figure 2.65: Three-port Converter with SMs.

The three-port converter consists of two parts: LLC circuits and coupled core. A high frequency half bridge LLC circuit without secondary side is applied. Since the low frequency current flows into the isolation stage, soft switching is required in this high frequency circuit to avoid high switching loss. Although DAB and LLC can both achieve soft switching, LLC is the preferred solution in this high frequency case. The resonant tank in LLC circuit shapes the loop current in phase with the switching point voltage which ensures zero loop current during switching. However, the DAB switches when the loop current reaches peak point. Therefore, LLC generates much less switching loss compared with DAB while both topologies achieve soft switching successfully, especially in high frequency case. In the current case, the difference between this LLC and the traditional LLC is that the input current on the dc side is

actually low-frequency ac current. While the half bridge uses 50%, the ac side of the half bridge has the resonance sin-wave current due to the LC resonance circuit. This current has a time-varying amplitude. When the dc side current changes its polarity, the half-bridge ac side current changes its phase. Although this LLC doesn't have the secondary side, the primary side still flows the full load current (the original module capacitor current). The final magnetizing current doesn't have the load current because the flux generated by the load current of three phase get cancelled with each other. That is why although there is no secondary side, the primary side still needs the LC resonance circuit to make the load current resonant to zero while the device is being turned off.

A down-scale simulation of proposed new MMC topology has been built and for comparison purpose, the simulation structure is designed to transfer from traditional MMC topology to the new topology during middle running point. The Fig. 2.66 shows the whole phase capacitor voltage of three cases: (1) traditional MMC case with 240 μF cap in each SM; (2) New MMC case with 240 μF cap in each SM; (3) New MMC case with 24 μF cap in each SM. As shown in the Fig. 2.67, the voltage balancing is achieved for all three cases. However, the prominent point is that the capacitor voltage ripple has been significantly reduced once the topology is switched to the Newly proposed with three-port converter. As only switching ripple flows into the capacitor, even one tenth of the capacitance is enough.

Another comparison simulation without phase energy control loop is conducted for both traditional MMC case and the new case. The simulation result shown in Fig. 2.68. During traditional MMC case, the arm current is filled with low frequency ripple since no more phase energy loop is applied to limit the circulating current. After entering new MMC operation, the arm current ripple is immediately reduced and thus only contains fundamental and dc part as the second order harmonic has

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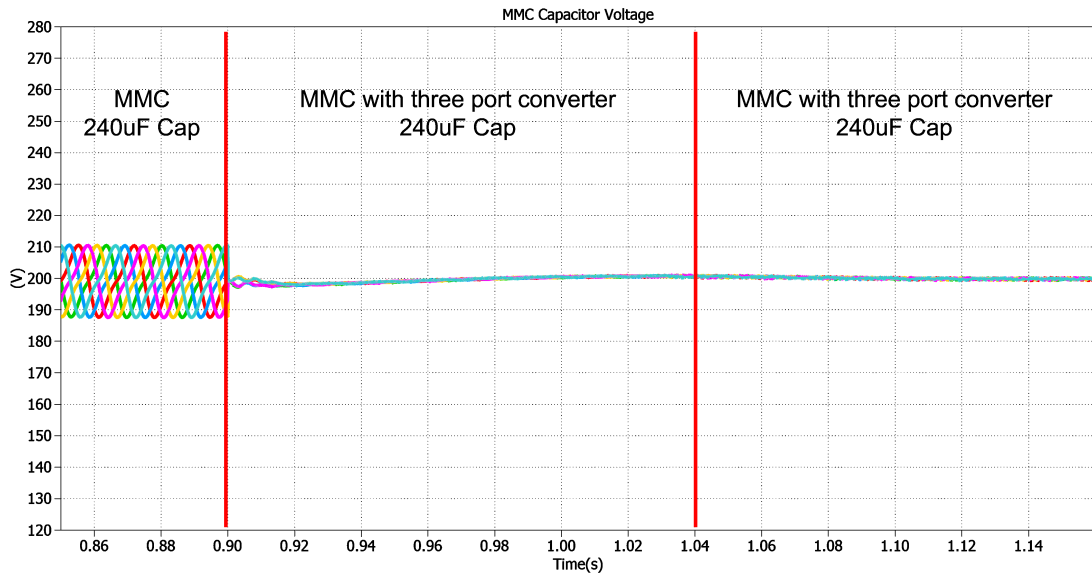
Figure 2.66: MMC Capacitor Voltages in Varying Cases.
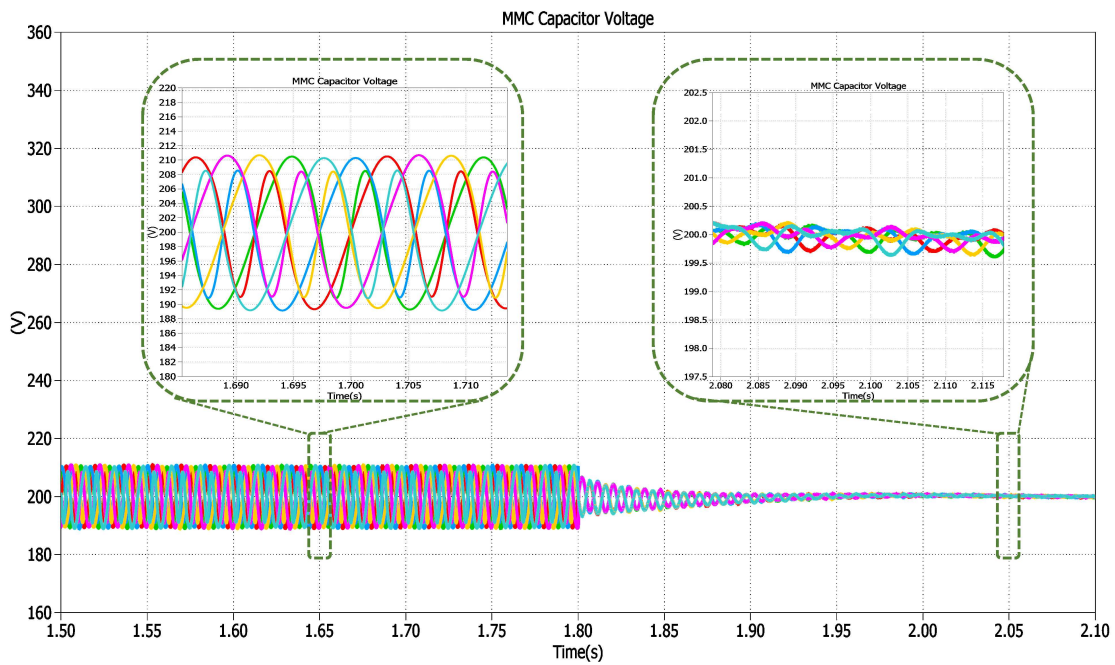
Figure 2.67: MMC Capacitor Voltages Without Phase Energy Balance Control: Traditional vs Proposed.

been removed due to the flux cancellation. Therefore, it has been verified that the new MMC no longer needs to phase energy control loop compared with traditional case.
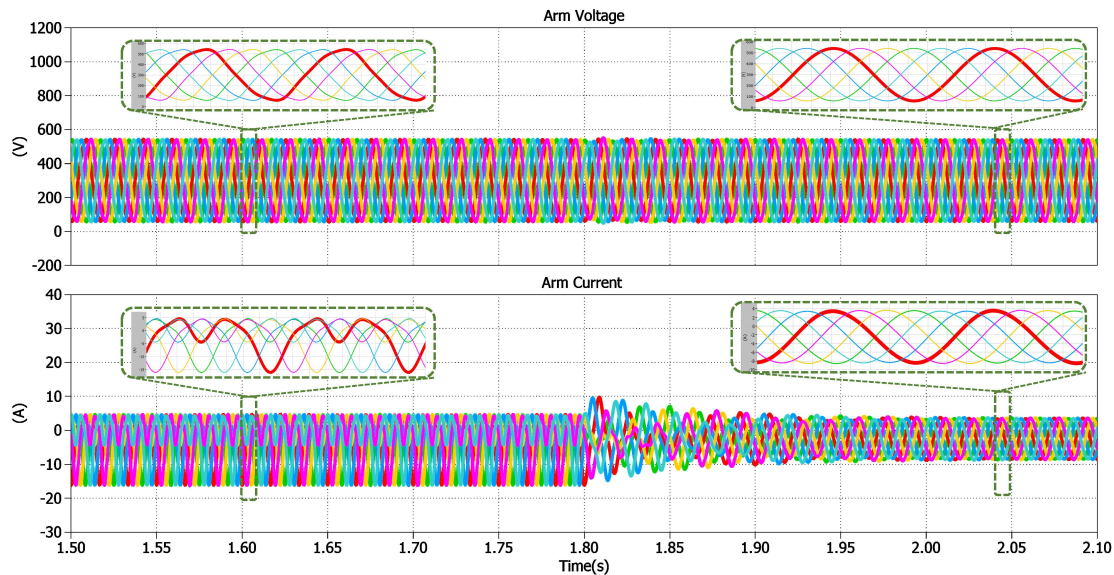
Figure 2.68: MMC Arm Voltage and Current Without Phase Energy Balance Control: Traditional Vs Proposed.

To simulate the practical starting process in motor drive case, the third simulation is then conducted in which system frequency varies from 0 Hz to 60 Hz. The related simulation result is shown in Fig. 2.69. As it shows, the system output current and voltage changes smoothly from zero to rated frequency.

In summary, a new MMC topology with three-port converter that using customized LLC circuits to couple the SMs from same voltage level together. The fundamental and the 2nd order harmonic current ripple can be eliminated as their induced magnetic flux are cancelled in the coupled core, as presented in above simulation results.
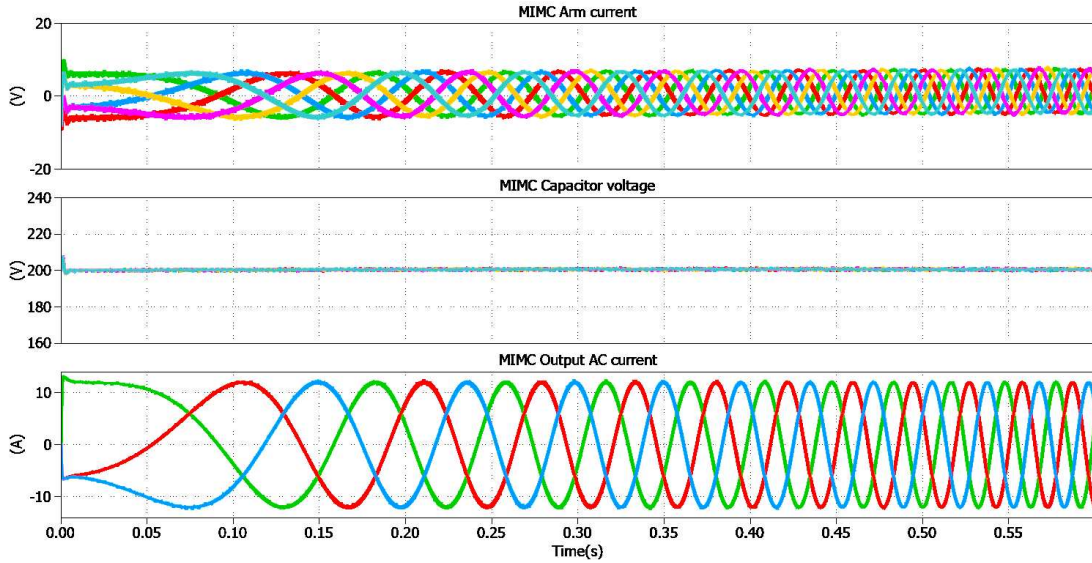
Figure 2.69: MMC Motor Drive Zero Frequency Start-up.

2.8.2 Series Connected Modular Multilevel Converters

As for the proposed series connected modular multilevel converters, there are two different versions: Full Bridge version (FBSC-MMC) and Half Bridge version (HBSC-MMC). The FBSC-MMC, in which each phase consists of four arm converters just like a full bridge, are series connected to support the dc-link as shown in Fig. 2.70. As for the HBSC-MMC, there are also four arms for each phase. Two of the arms consists of cascaded connected submodules and are just like single phase leg in traditional MMC topology. The other two arms are formed by series switches such as high voltage MOSFET, which are only activated when the ac voltage changes polarity. As shown in Fig. 2.71, three phase legs are series connected in vertical direction to support the dc bus voltage as well.

As presented in Fig. 2.70, three phase limbs of FBSC-MMC are assembled in vertical direction to support the dc-link voltage. As a result, the direct ac voltage is only the one third of the original MMC configuration. The two output ports of
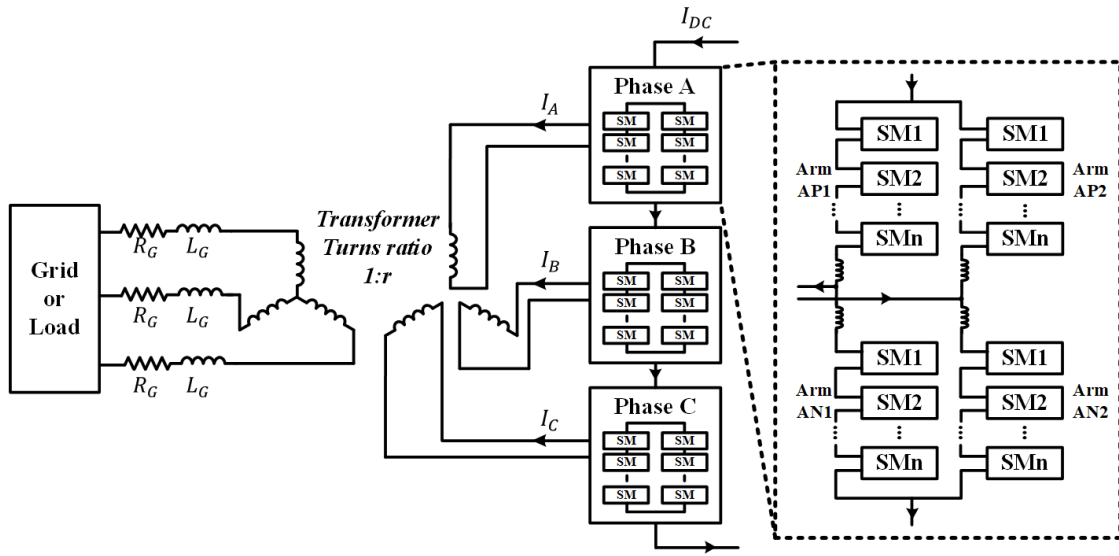
Figure 2.70: Proposed FBSC-MMC Topology.
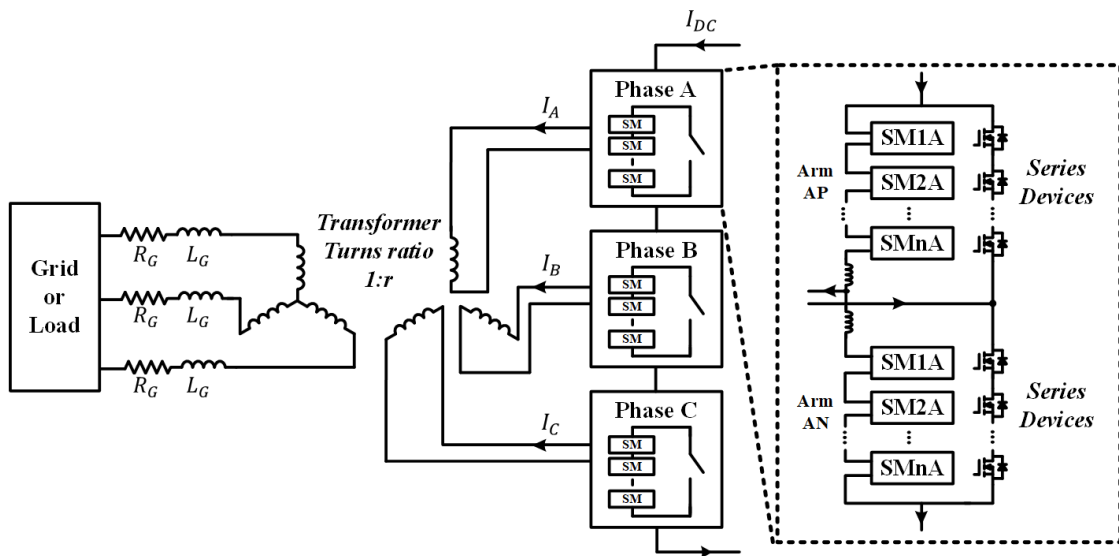
Figure 2.71: Proposed HBSC-MMC Topology.

each phase leg are connected to an ac transformer which has the following function: (1) creates isolation between load and the MMC system; (2) generates required AC grid voltage amplitude. The operation of each phase is very similar to the traditional three-phase MMC except for the modulations which can be explained through the equivalent functions for each arm current and arm voltage. The circuit symmetry can be maintained by making each phase leg provide half of the ac voltage. In each phase leg, the sum of the upper arm voltage and the lower arm voltage is equal to one third of the dc-link voltage. And each arm has an average voltage of one sixth of the dc voltage. In order to keep the arm voltage positive even when the ac voltage reaches the maximum, the output voltage of one phase should be equal to the modulation index multiplying one third of the dc voltage; but the equation for MMC is that the output voltage is equal to half dc voltage multiplying the modulation index. To be clearer, take phase A as example to derive the equivalent functions for the arm converter as shown in Eq 2.47, 2.48 and 2.49. Where V_{AP1} is the upper arm voltage of the phase leg 1; V_{AN1} is the lower arm voltage of the phase leg 1; V_{AP2} is the upper arm voltage of the phase leg 2; V_{AN2} is the lower arm voltage of the phase leg 2; V_{a} is the output ac phase to neutral voltage; V_{dc} is the total dc-link voltage of the converter.

$$V_{\mathrm{a}} = V_{\mathrm{AP1}} - V_{\mathrm{AP2}} \tag{2.47}$$

$$V_{\mathrm{AP1}} = V_{\mathrm{AN2}} = \frac{V_{\mathrm{dc}}}{6} - \frac{V_{\mathrm{a}}}{2} \tag{2.48}$$

$$V_{\mathrm{AP2}} = V_{\mathrm{AN1}} = \frac{V_{\mathrm{dc}}}{6} + \frac{V_{\mathrm{a}}}{2} \tag{2.49}$$

The arm current equivalent function is similar with that in conventional MMC. It can be divided into two parts: dc current and ac current. The dc current I_{dc} can be evenly distributed into the two phase-legs of the phase A. and the ac current is evenly distributed into the two arms of one phase leg. The arm current expressions are in the following Eq. 2.50 and 2.51.

$$I_{AP1} = I_{AN2} = \frac{I_{dc}}{2} + \frac{I_a}{2} \tag{2.50}$$

$$I_{AP2} = I_{AN1} = \frac{I_{dc}}{2} - \frac{I_a}{2} \tag{2.51}$$

Where I_{AP1} is the upper arm current of leg 1 in phase A; I_{AP2} is the upper arm current of the leg 2 in phase A; I_{AN1} is the lower arm current of the leg 1 in phase A; I_{AN2} is the lower arm current of the leg 2 in phase A; I_{dc} is the total dc current on the dc-link; I_a is the ac output current of phase A.
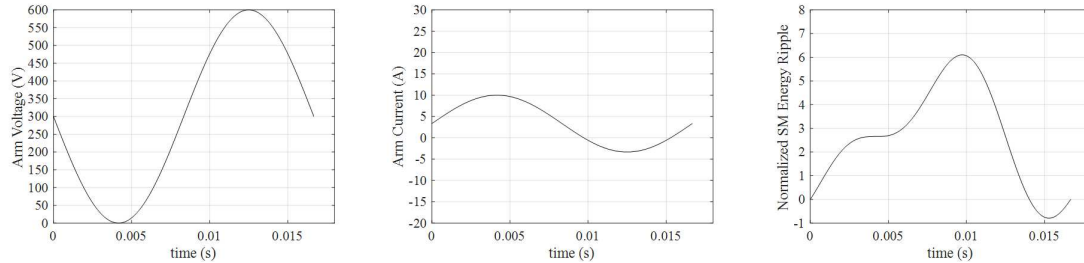
Figure 2.72: Estimated Arm Current, Voltage and Normalized Voltage Ripple of Traditional MMC.

The next step is to verify the energy balance. The arm energy can be obtained by integration of the product of arm voltage and arm current over one fundamental period. The calculation result is shown in Fig. 2.73 and the that if conventional MMC is shown in Fig. 2.72. As the figure shows, the energy starts from zero at the beginning
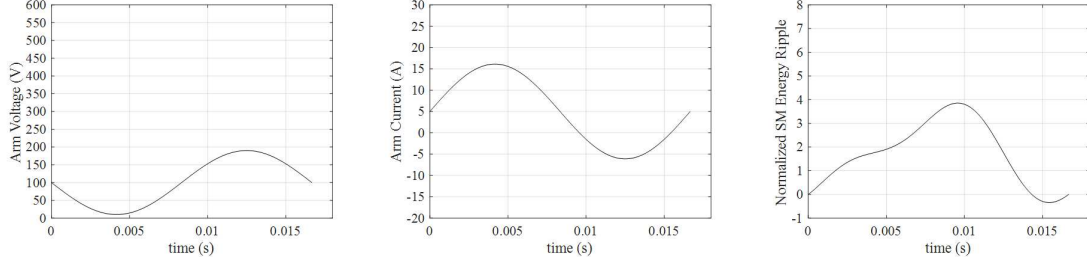
Figure 2.73: Estimated Arm Current, Voltage and Normalized Voltage Ripple of Proposed FBSC-MMC.

of the period and returns to zero when the period ends. Therefore, the energy can naturally be kept balanced in this topology. Up to now, it is theoretically verified that the topology can work properly in generating the required voltage and current while keeping the stored energy balanced. In order to compare the capacitor size of this topology with the three phase MMC, the energy ripple of the two topologies is calculated and compared. The energy ripple is demonstrated by the difference between the maximum energy and the minimum energy. The energy can be calculated by half capacitance multiplying the voltage square. Therefore, the energy ripple ΔE is proportional to the capacitance and the square of the capacitor dc voltage, assuming the voltage ripple ΔU is a fixed percentage of the rated capacitor voltage.

The 2ω harmonic component does not exist either in the dc current or in the circulating current of each phase. When the 120° phase shifted three-phase voltage adds together to form the dc voltage, the harmonics of 2ω or its integer times get cancelled. It also contains zero 3ω harmonic component. Take one arm as one equivalent half bridge and calculate its harmonics as follows. The 2ω harmonics function in the output voltage of the half bridge comes from the cross-multiplication of the capacitor voltage and the modulation function. The capacitor current can be obtained based on the arm current mentioned before as shown in Eq. 2.52 - 2.56.

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$$I_{\text{C,AP1}} = (\frac{I_{\text{dc}}}{2} + \frac{I_{\text{a}}}{2}) \times D_{\text{AP1}} \tag{2.52}$$

$$D_{\text{AP1}} = \frac{(\frac{V_{\text{dc}}}{6} - \frac{V_{\text{a}}}{2})}{V_{\text{dc}}} \tag{2.53}$$

$$V_{\text{a}} = \frac{V_{\text{dc}}}{3} \times M \times \sin(\omega t) \tag{2.54}$$

$$I_{\text{a}} = I_{\text{dc}} \times \frac{2}{M} \times \sin(\omega t) \tag{2.55}$$

$$I_{\text{C,AP1}} = \frac{I_{\text{dc}}}{4} \cos(2\omega t) + (\frac{1}{2M} - \frac{M}{4}) I_{\text{dc}} \sin(\omega t) \tag{2.56}$$

Then, the output voltage of the half bridge can be obtained by the capacitor voltage and the modulation function, thus the 2ω harmonic in the voltage can be calculated using Eq. 2.57 and 2.58.

$$V_{\text{C,AP1}} = \frac{1}{2\omega C} \frac{I_{\text{dc}}}{4} \cos(2\omega t) + \frac{1}{\omega C} (\frac{1}{2M} - \frac{M}{4}) I_{\text{dc}} \sin(\omega t) \tag{2.57}$$

$$V_{\text{O,AP1,2w}} = V_{\text{O,AP2,2w}} = -\frac{M}{4\omega C} (\frac{1}{2M} - \frac{M}{4}) I_{\text{dc}} \cos(2\omega t) \tag{2.58}$$

Therefore, 2ω components in the two phase-legs have the same amplitude and phase. 2ω loop current no longer exists since they cancel each other in the loop. In

addition, 2ω current also does not exist in the dc loop with the dc source. The reason is that the 2ω voltage in three-phases are $120°$ phase shifted with each other and the sum of them is equal to zero. The 3ω voltage components in the upper arm and lower arm of one phase leg cancel each other as they are $180°$ phase-shifted with each other. Thus, there is also no 3ω circulating current between the two legs of each phase, and there is no 3ω circulating current between cascaded three phase chain-link and the DC source. The only component that cannot be cancelled between arms or three phases is the 6ω harmonic. However, its value is such small compared with the original 2ω harmonic in MMC that it gives almost zero influence. In conclusion, the harmonics of arm voltage and current in this topology are significant smaller compared with the traditional MMC topology, which leads the reduction in capacitor volume.

20 MW with 20 kV dc bus voltage PLECS simulation of proposed FBSC-MMC topology has been conducted high quality waveforms that can be achieved with an infinite number of submodules. For the sake of simplicity, all the waveforms are referred to the converter side of the transformer and presented according to the sign conventions as shown in Fig. 2.74. The top right shows that the steady state output performance of ac side. The top right figure and bottom tight figure present the arm voltage and current result. Obviously, there is no more second order harmonics, which confirming the analyzed harmonic feature of the FBSC-MMC topology. The bottom left figure demonstrates the voltage balance of all SMs in Phase A.

As already presented in Fig. 2.71, Each phase of the converter comprises a half bridge with two arms of MMC cascaded cells. To achieve sufficient voltage rating, it is intended that the half bridge limb is formed by series connected MOSFET due to its low conduction loss. While the ac voltage is positive, the upper half bridge limb is turned on, so the voltage of the upper MMC arm is connected to the output; while the ac voltage is negative, the lower one is turned on, so the voltage of the lower MMC
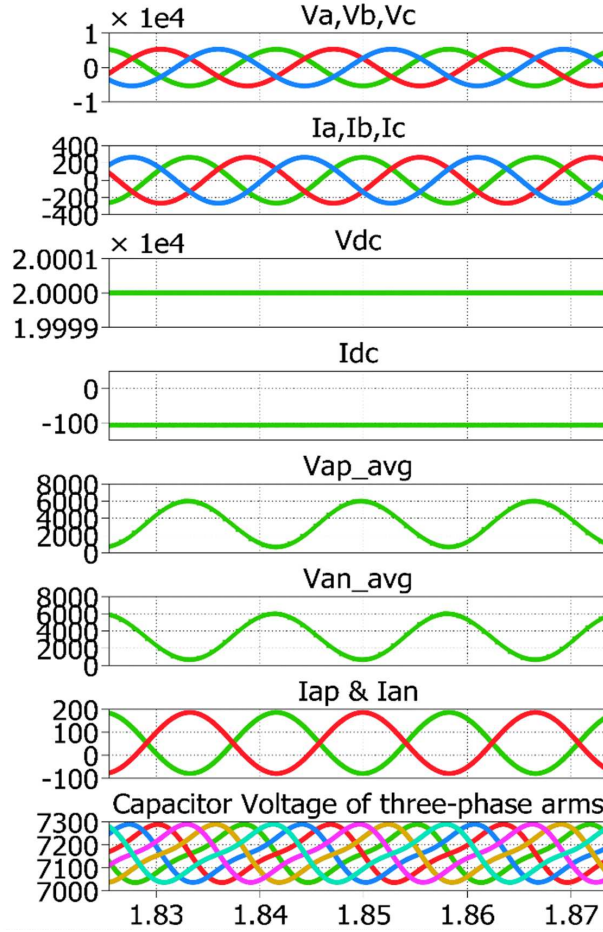
Figure 2.74: Steady State Performance of Proposed FBSC-MMC.

arm is reversely connected to the output. Therefore, only one arm is connected to the output during each half fundamental cycle and the inserted MMC arm voltage is equal to the positive sinusoidal voltage. During the other half cycle, the arm voltage is equal to the dc voltage minus the positive sinusoidal voltage. According to the system configuration, the dc voltage of each phase here is also one third of the V_{dc}. The resulted arm voltage with this operation principle is always positive. The arm current contains both dc current and ac current. The dc current is equal to the dc source current. The ac current is just zero when this arm is not connected to the ac side, and equal to negative output current when the arm is connected to the ac side.

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To further explain the operation principle of this topology in details, take the phase A as example. S_1 and S_2 is used to respectively represent the switching state of the upper series connected MOSFETs and lower series connected MOSFETs. When the output voltage V_a is positive, S_1 is closed. The output voltage is equal to the upper arm voltage V_AP. During this time, the lower arm voltage V_AN is equal to one third of dc voltage minus V_AP. When the output voltage V_a is negative, switch S_2 is closed, and the output voltage is equal to minus lower arm voltage. When V_a is positive, the output current and the dc current both flow through the upper arm, but the lower arm only conducts the dc current. When the output voltage V_a is negative, S_2 is closed, so the upper arm only conducts the dc current and the lower arm conducts both. The normalized arm voltage and current of phase A can be calculated in Eq. 2.59 - 2.66 and shown in Fig. 2.75.

When $S_1 = 1$, $S_2 = 0$, we have:

$$V_\mathrm{AP} = V_\mathrm{a} \tag{2.59}$$

$$V_\mathrm{AN} = \frac{V_\mathrm{dc}}{3} - V_\mathrm{AP} \tag{2.60}$$

$$I_\mathrm{AP} = I_\mathrm{dc} - I_\mathrm{a} \tag{2.61}$$

$$I_\mathrm{AN} = I_\mathrm{dc} \tag{2.62}$$

When $S_1 = 0$, $S_2 = 1$, we have:

$$V_{AP} = \frac{V_{dc}}{3} - V_{AN} \tag{2.63}$$

$$V_{AP} = -V_a \tag{2.64}$$

$$I_{AP} = I_{dc} \tag{2.65}$$

$$I_{AN} = I_{dc} + I_a \tag{2.66}$$
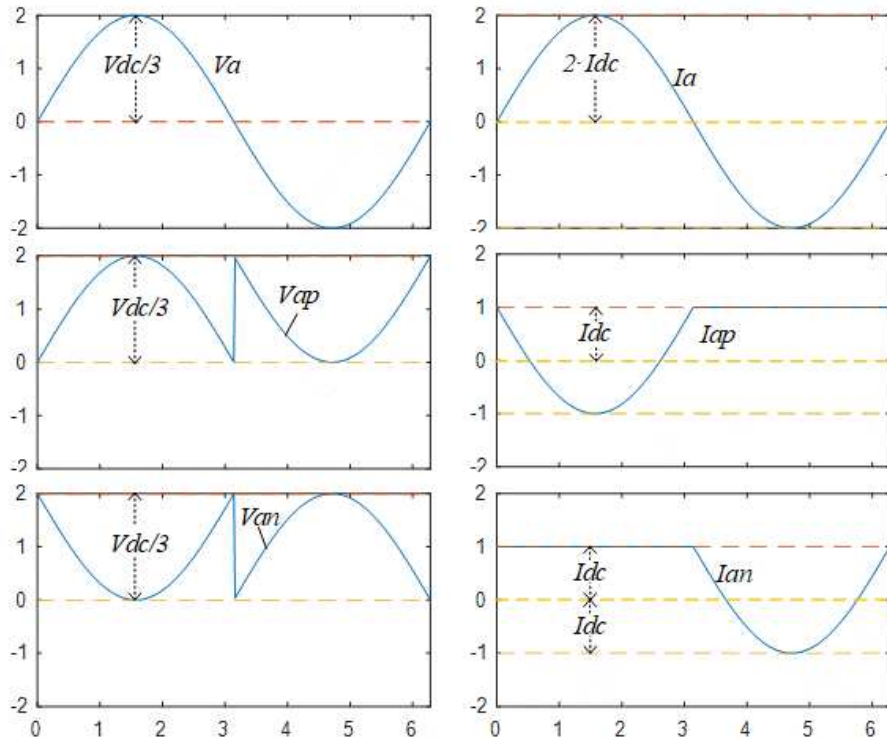
Figure 2.75: Normalized Arm Voltage and Current Calculation Result of Proposed HBSC-MMC.

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It can be seen that the difference between this topology and the MMC is that its output voltage is the product of the total dc voltage and the modulation index, not the product of half dc voltage and the modulation index. The difference between HBSC-MMC and the FBSC-MMC is that its arm voltage is not continuous and jumps at the time of the half fundamental cycle. The same balance verification is also conducted based on the same calculation procedure. Just like what we did in FBSC-MMC, the derived energy ripple is also derived and shown in Fig. 2.76. it can be seen its energy ripple is similar with that in MMC. Since the number of arms is also six in this topology, the total arm energy ripple is similar with that in MMC as well. In terms of harmonics, the arm voltage and current also do not involve any 2ω and 3ω ripple. The lowest harmonic that the arm contains is 6ω. The sum of the 2ω voltage in three-phases equals to zero, since they are $120°$ phase shifted. The 3ω voltage of the upper and lower arms in each phase cancel each other since they are $180°$ phase shifted. The 6ω exists in the dc current, arm voltage and arm current since it cant get canceled either between arms or among three phases. But its value is very small, so its impact is very small. Due to the elimination of the 2ω current in the arm current, the capacitor size is reduced significantly.
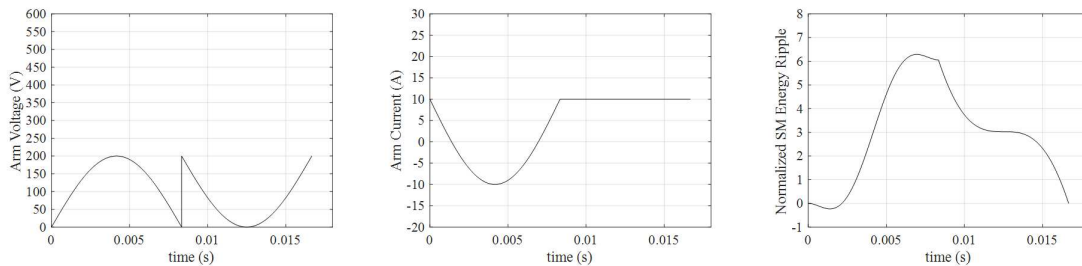
Figure 2.76: Estimated Arm Current, Voltage and Normalized Voltage Ripple of Proposed HBSC-MMC.

A 10 kW with 600 V dc bus voltage PLECS simulation of proposed HBSC-MMC topology is also conducted. High quality output current can be observed and the
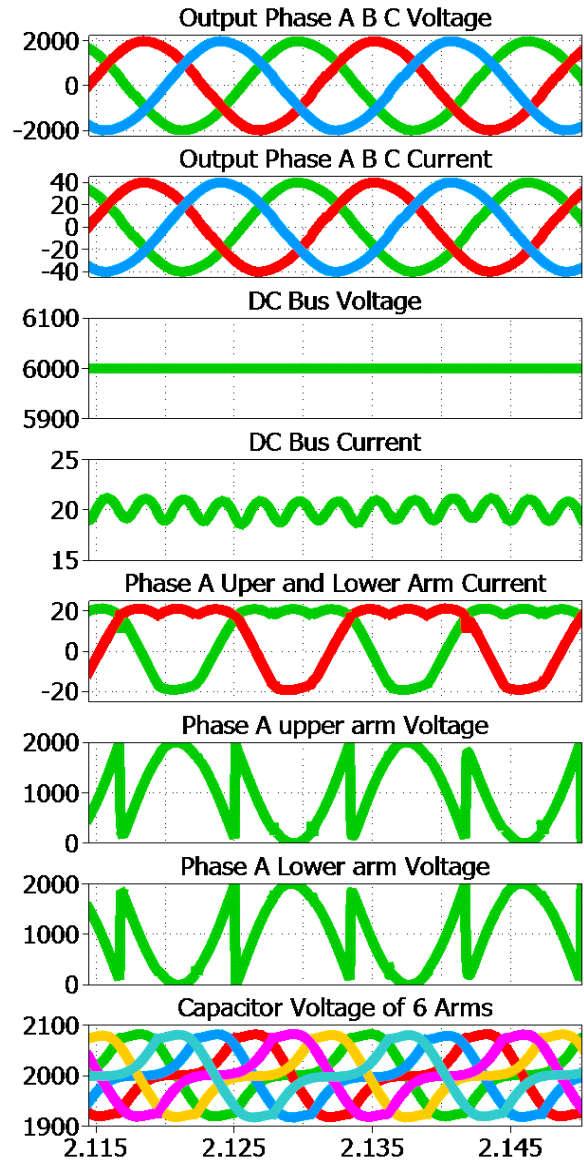
Figure 2.77: Estimated Arm Current, Voltage and Normalized Voltage Ripple of Proposed HBSC-MMC.

capacitor voltages keep balance under voltage sorting and balancing control. The arm voltage and current have sudden change in the medium of the fundamental cycle, which introduces the sixth harmonics in the dc current. However, this ripple can be kept within 10% of the rated dc current, and its impact on the phase voltage/current is quite low as well From top to bottom they are: ac phase voltage (on converter side), ac phase current (on converter side), dc voltage, dc current, phase a upper arm voltage average, phase a lower arm voltage average, phase a upper and lower arm current, capacitor voltage of the arms in three phase. It can be observed that the dc bus current is ripple free and the arm voltage/current doesnt contain second and third harmonics, confirming the analyzed harmonic feature of the proposed topology. As shown in the Fig. 2.77, the arm voltage and current have sudden change at the middle of the fundamental cycle, which introduces the sixth harmonics in the dc current. However, this ripple is able to be kept within 20% of the rated dc current, and its impact on the phase voltage/current is low as well.

2.8.3 T-type Modular Multilevel Converters

The problem of the conventional VFDs for high power applications are bulky size. The proposed SiC-based TMMC is a high-power density, high scalability, and Low-EMI modular multilevel converter, which is suitable for medium voltage drive. Compared to traditional 2-level (2L) converter and 3-level (3L) NPC, the bulky filter is removed. Compared to MMC, the power density is improved by at least 30%.

Take traditional 2L-converter, 3L-NPC, Cascaded-H-Bridge (CHB) and MMC for comparison. The first condition for comparison is with the usage of Si-IGBT. The problem of 2L and 3L converter is the bulky output filters because of the low switching frequency of the high voltage Si-IGBT they use. CHB and MMC can overcome this problem by increasing the number of modules and using lower voltage device in the

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modules. But the problem with CHB is that it requires a bulky low frequency multi-phase transformer and the problem with MMC is that it requires large volume of capacitor due to its fundamental current flow especially at low frequency.

Then the question becomes whether the power density of the traditional 2L-converter, 3L-NPC, Cascaded-H-Bridge (CHB) and MMC can be improved by simply replacing the Si IGBT by SiC MOSFET rather than modifying the topology. Therefore, the second condition for comparison is with the usage of SiC-MOSFET. For 2L and 3L converter, the filter size can be reduced by switching the SiC MOSFET at much higher frequency. However, it requires series connection of device to satisfy its voltage level since the maximum voltage rating of the current available SiC MOSFET is much lower than Si-IGBT. And the series connection can bring the following four problems: (1) the gate driving signal of the devices needs to be synchronized precisely; (2) the dv/dt level of series connected devices is the product of a single device dv/dt and the number of devices; (3) the circuit structure of the two-level and three-level converter requires the isolated gate driver for each device which brings high cross-talking noise; (4) the reliability of series devices is low. Therefore, if the SiC MOSFET is used in the conventional two-level or three-level converters, the dv/dt of a single device needs to be reduced by slowing down the switching speed of the device. This can be implemented by adding a big snubber circuit or extra miller capacitor. However, it sacrifices the benefits of fast switching speed feature of SiC device. The requirement for device synchronization also limits the maximum switching frequency of the device. The excessive voltage overshooting on the dc-link will need additional redundant devices to be added, which lowers the device utilization rate, in another word, lowers the system efficiency. The proposed TMMC can address the above four problems since it is a series half-bridge/H-bridge module structure in which each module is rated according to the device rating, and no series device connection is

needed. Thus the four problems becomes four advantages of SiC-based TMMC: (1) the module operates independently thus no device-level synchronization is required; (2) the dv/dt is at the single-device level, which is much lower than that of series devices, thus the dv/dt caused dc-link voltage overshooting problem is mitigated to the minimum level (3) the cross-talking leakage current caused by the high dv/dt on two sides of the isolation transformer in the gate driver is significantly reduced because the gate driver power is drawn directly from the dc capacitor of the module and the highest isolation level is the isolation between the upper device and the lower device of a single half-bridge/H-bridge, which is equal to the dc voltage of a single module; (4) the system reliability is greatly improved and minimum redundancy number can be used to reach the reliability goal, because if one module get shorted or broken, the system can continue to operate by bypassing the failure module.

In summary, the proposed TMMC topology is able to significantly reduce the capacitor size and is quite appropriate to be used with SiC device since it overcomes the major disadvantage of SiC MOSFET such as high EMI noise, high common mode current, and low reliability. In addition, the use of high voltage SiC-MOSFET can also lower the total module numbers to conquer the disadvantage of TMMC. In a word, the concept of TMMC is to use more active devices to reduce or substitute the passive components, mainly the bulky capacitor.

The general schematic of proposed TMMC topology is shown in Fig. 2.78. The first innovativeness is that it creates a middle arm, which is composed of cascaded H-bridge and connects to the middle point of the front-end rectifier, to make the converter operate under half dc-link when the output voltage is below 0.5 p.u. When the output voltage is above 0.5 p.u., the upper and lower arm is in usage and the operation is the same as MMC. When the output voltage is below 0.5 p.u., one of the upper arm and lower arm is used with the middle arm. In this case, only half

dc voltage is supplying the power. So, the arm voltage is reduced by half because the arm voltage is equal to half dc voltage minus the ac voltage. The arm current is equal to one third of the dc current minus half output current, and it increases by a very small percentage because the output current remains constant as rated. The dc current increased to two times but this increase can be ignored because the dc current is much smaller than the ac current at low power low frequency operating point. Therefore, the fundamental frequency energy ripple in one arm is reduced to half of the original. The capacitor size which depends on the energy ripple amplitude is also reduced by half. Because of the capacitor installation in the extra arm, the overall capacitor size is reduced by 30%. The system power density is improved by 30% because the capacitor size takes up 90% of the total volume.

The second innovativeness is that this T-type MMC does not use any extra thyristor arm or series IGBT arm to create this half dc-link voltage and the extra arm still has the same modular structure as the original arm. The only difference is that the half bridge is replaced by H-bridge because the middle arm needs to undertake the voltage in both directions. Therefore, all the advantages of modular structure such as low dv/dt, low common mode noise, low EMI, high scalability, low THD, high reliability can be kept.

The third innovativeness is that this TMMC can start the motor from very low frequency easily by generating a ramping dc voltage from zero. At a wide frequency range of [30 Hz, 150 Hz], the dc-link voltage keeps a constant. Only at the start-up, when the frequency is below 30 Hz, the voltage is lowered down by bypassing two diode bridges with turning off the corresponding thyristor pair. At extremely low frequency of [0, 15 Hz], the dc voltage is ramping up linearly from zero by using only the fourth diode bridge and its corresponding H-bridge. The output ac voltage and frequency, the input dc voltage is shown in Fig. 2.79(a). Because of the use of the

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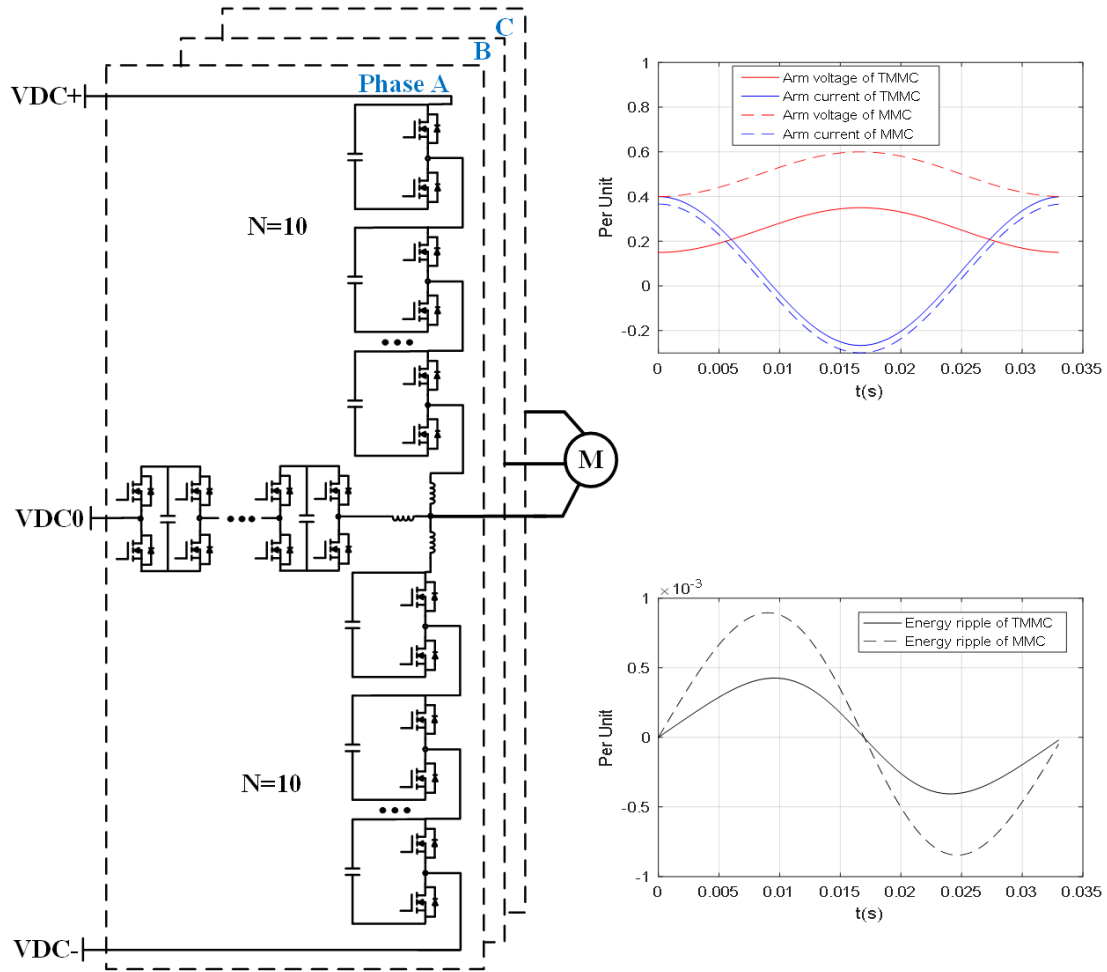
Figure 2.78: Proposed TMMC Topology and Estimated Arm Current, Voltage and Normalized Energy Ripple Compared to Traditional MMC.

middle arm, the actual utilized voltage by the inverter is reduced to half dc voltage when the frequency is lower than 30 Hz, which is shown in Fig. 2.79(b). In the full frequency range, the output current is always equal to the full rating. The output voltage is proportional to the frequency and the dc voltage keeps constant in the frequency range of [0.2 p.u., 1 p.u.], but the utilized voltage at [0.2 p.u., 0.5 p.u.] is only half dc-link because only the upper arm and the middle arm is operating. For the frequency range of [0.1 p.u., 0.2 p.u.], the dc voltage is stepped down to $\frac{1}{2}$ V_{dc} by bypassing two diode bridges in the front end, but the utilized voltage is only $\frac{1}{4}$ V_{dc}.

For the frequency range of [0 p.u., 0.1 p.u.], the dc voltage is ramping up linearly from 0 to $\frac{1}{4} V_{dc}$ by using the fourth diode bridge and H-bridge together and bypassing the other three diode-bridges, but the actual utilized voltage is from 0 to $\frac{1}{8} V_{dc}$. It is obvious that the dc voltage has a much higher utilization rate with the new topology, which reduces the arm energy ripple.
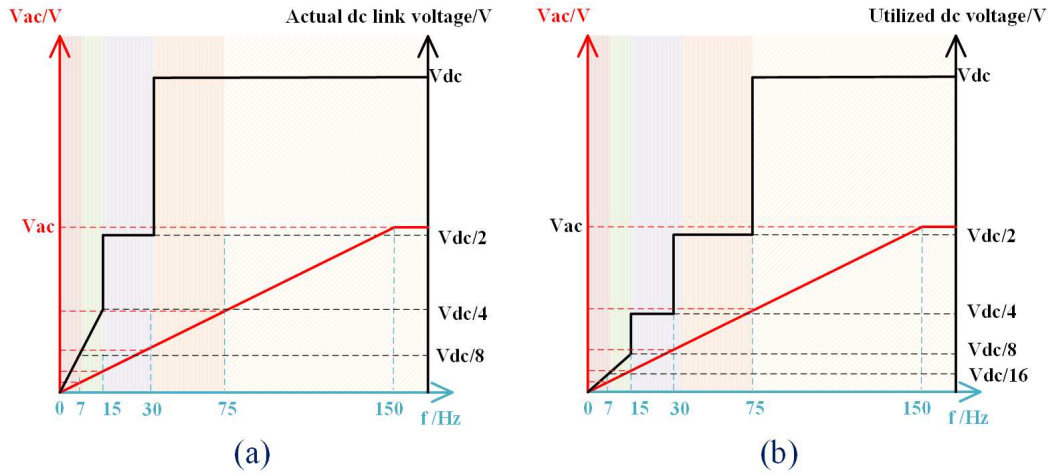
Figure 2.79: Motor Operation V/f Curve and the Corresponding (a) Actual Dc Voltage; (B) Utilized Dc Voltage.

Moreover, the capacitance needed for each operating point is shown in Fig. 2.80. From this figure it can be seen that the capacitance designed for 30 Hz (0.2 p.u.), half dc-link voltage is able to satisfy the ripple requirement during the whole operating range.

A 150 kW / 3 kV system simulation of proposed TMMC topology is conducted for motor drive. As discussed above, the V/f control is employed as well as the variable dc bus voltage to maximize the utilization of dc bus voltage. The utilized dc voltage increased step by step as the frequency increases as shown in Fig. 2.81. Both voltage and current maintain steady and clean as expected. The close loop control is doing well as can be seen from Fig. 2.82. The steady total energy presents the perfect energy balance between the ac side and dc side. The phase energy represents the

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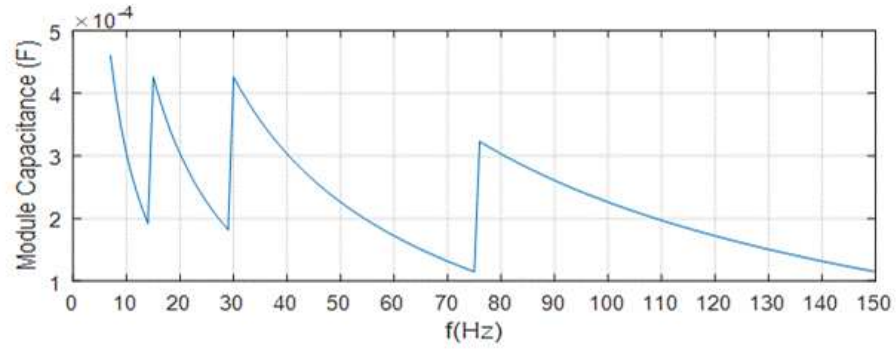
Figure 2.80: Required Capacitance as Frequency Changes.

fundamental ac output current. Arm energy result gives out two messages: (1) The capacitor voltages of SMs are well balanced that contributes to the voltage balance control. This is because the unbalanced voltage will generate other harmonics ripple which distorts the arm energy. (2) The circulating current is well controlled since the energy ripples are balanced among three phases.
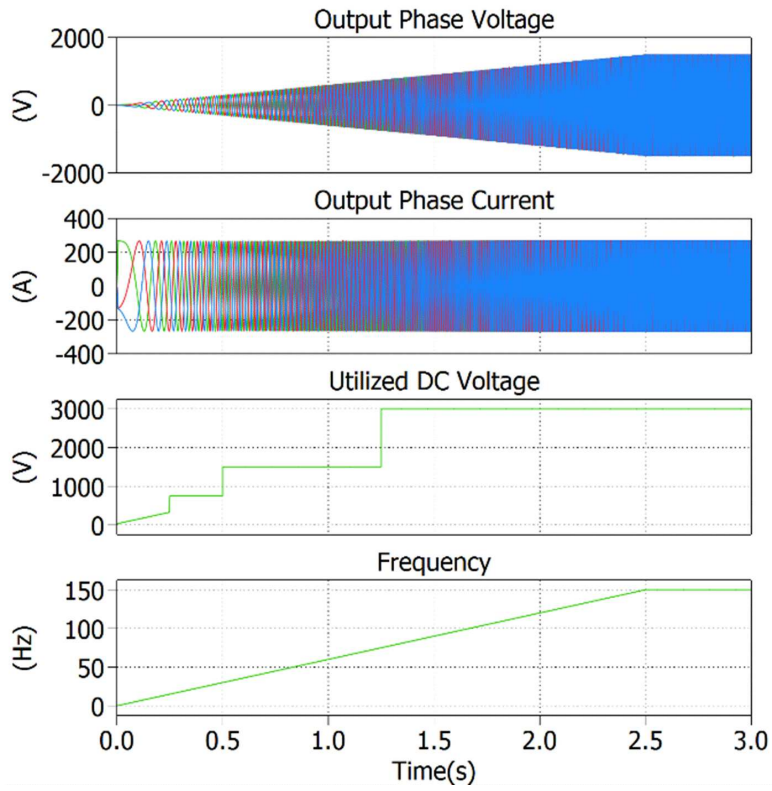
Figure 2.81: Motor Drive Start-up Simulation of the TMMC Topology with Variable Dc Bus.
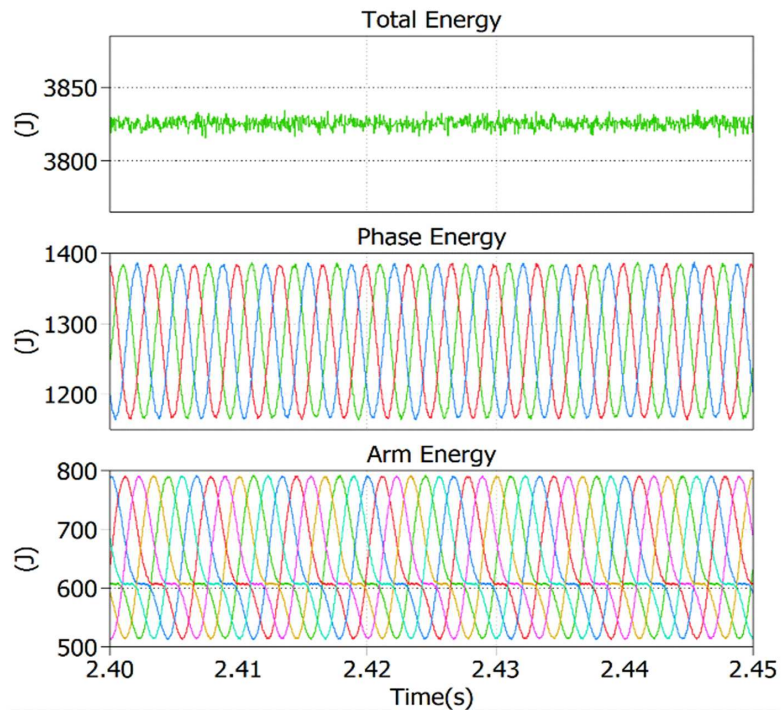
Figure 2.82: System Energy States.

Chapter 3

A MULTI-LEVEL-VOLTAGE-OUTPUT GATE DRIVER FOR DYNAMIC ON-RESISTANCE SUPPRESSION IN GAN-HEMTS

In this Chapter, the evolution of semiconductor structure of GaN transistor, including classical normally on device, GIT normally off GaN and p-GaN doped Infineon CoolGaN-HEMTs, is well-described. As the benefits, the channel current capability and drain-source voltage are significantly boosted. However, accompanying the evolution of GaN devices, many challenges become more and more prominent, such as crosstalk issue, parasitic issue, protection challenge and so on. The dynamic on-resistance issue is one of the urgent problems to be solved since it strongly affects the GaN device current limit and voltage limit. Unlike traditional methods from the perspective of transistor structure, this report proposes a novel Multi-Level-Voltage-Output gate drive circuit (MVO-GD) aimed at alleviating the dynamic on-resistance issue from engineering point of view. The comparative tests of proposed MVO-GD and the standard 2-level gate driver (STD-GD) are conducted under variable test conditions which may affect dynamic on-resistance, such as drain-source voltage, gate current width, device package temperature and so on. The experimental waveforms and data have been demonstrated and analyzed.

3.1   Overview of GaN HEMTs

Gallium Nitride high-electron-mobility transistors (GaN-HEMTs) is first introduced to the world in 2004 with depletion-mode RF transistors made by Eudyna Corporation in Japan. Using GaN on silicon carbide (SiC) substrates, Eudyna successfully brought transistors into production designed for the RF market [90]. The

HEMT structure was based on the phenomenon first described in 1975 by T. Mimura et al. [91] and in 1994 by M. A. Khan et al. [71], which described a two-dimensional electron gas (2DEG) near the interface between an AlGaN and GaN heterostructure interface featuring the high-electron-mobility characteristic of GaN transistor. During the past decades, the GaN devices have been widely investigated and four key electrical properties of GaN transistor compared to other popular semiconductor materials are shown in Table 3.1 [92–96]. Using the data from Table 3.1 (and adjusting for the enhanced mobility of the GaN 2DEG), the theoretical minimum device on-resistance (the inverse of conductivity) can be estimated [93].

Table 3.1: Material Properties of GaN, SiC and Si at 300 Kelvin.

Specifications	GaN	Si	SiC
EG (eV)	3.4	1.1	3.2
EBR	3.3	0.3	3.5
V_S (V)	2.5	1.0	2.0
μ	990 - 2000	1500	650

SiC and GaN both have a superior relationship between on-resistance and breakdown voltage due to their higher critical electric field strength. his allows devices to be smaller and the electrical terminals closer together for a given breakdown voltage requirement. GaN has an extra advantage compared with SiC. As a result of the enhanced mobility of electrons in the 2DEG. This translates into a GaN device with a smaller size for a given on resistance and breakdown voltage. When applying the GaN, Si and SiC materials to MOSFET fabrication, those excellent material properties can be further translated into transistor electrical characteristics as shown in Table 3.2. For a fair comparison, all the transistors selected at same voltage and current rating that fabricated by Infineon Technologies.

Table 3.2: Key Electrical Properties of GaN, SiC and Si Power Transistors.

Specifications	GaN IGO60R070D1	Si I- PL65R095CFD7	SiC IMBG65R072M1H
Blocking Voltage V_{ds}	650 V	650 V	650 V
On-resistance R_{dson}	55 mΩ	68 mΩ	72 mΩ
Output Capacitance C_{oss}	72 pF	72 pF	112 pF
Output charge Q_{oss}	41 nC	40 nC	68 nC
Total Gate Charge Q_g	5.8 nC	53 nC	22 nC
Reverse Recovery Charge Q_{rr}	0 nC	1560 nC	60 nC

As the Table 3.2 shows, the GaN device presents following advantages on electronical characteristics: (1) Low on-resistance. The low resistance means low conduction loss and reduce the thermal issue. Therefore, the cooling size can be reduced; (2) Low output capacitance. The low output capacitance features fast charging and discharging time of Q_{oss}, which means the turn-on and turn-off transient is faster. As a benefit, the switching loss can be reduced. (3) Low output charge. Since the turn-on switching loss is close to the output charge because the discharging current of the junction capacitance flows through the channel resistance and generate loss. This resistive loss is also added to the turn on loss. Therefore, low output charge means low discharging current and thus low switching loss; (4) Low gate charge. Low gate charge obviously means low gate loss and fast charging and discharging time of gate-source capacitance. This enable the GaN work under high switching frequency that can be as high as megahertz. (5) Zero reverse recovery charge. This characteristic features zero third quadrant loss during the deadtime that significantly reduce the

loss during the deadtime. Benefit from above advantages, GaN-HEMTs are quite popular and widely employed in high-frequency and high-efficiency applications in the voltage range up to 650 V. The commercial application range of these transistors are described in Fig. 3.1.
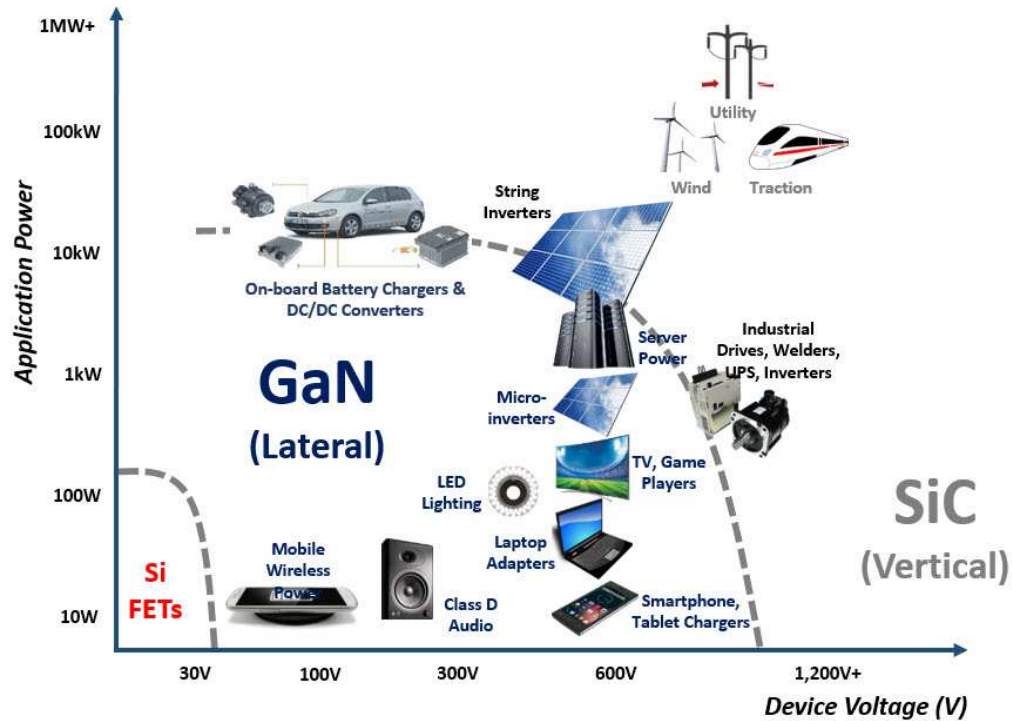
Figure 3.1: Powe Transistors Application Distribution map.

3.2 Evolution of GIT GaN FET Structure and Root Cause of Dynamic On-resistance

Fig. 3.2 illustrates the cross section of the classical Gate Injection Transistor (GIT). This classical GaN, which is first proposed by Prof. Yasuhiro Uemoto, is fabricated with a self-clamping p-gate structure that additionally solves the problem of gate Over Voltage (0 V) sensitivity [2]. In this structure, a Pd-based Ohmic gate was adopted on the p-AlGaN cap layer, which managed to improve the hole
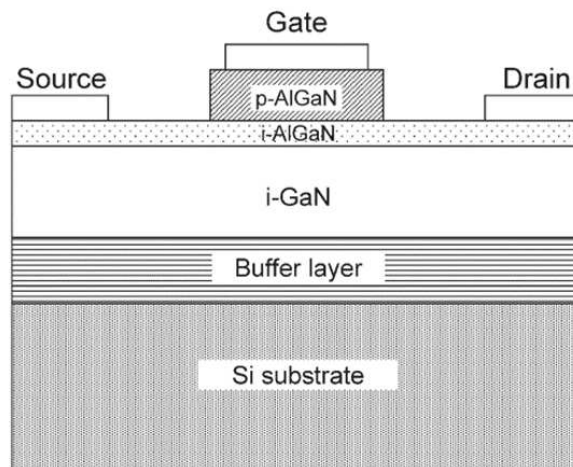
Figure 3.2: Schematic Illustration of the GIT Structure [2].

injection and the current capability of the device. Therefore, the device was named as gate injection transistor. This new device principle utilizes hole-injection from the p-AlGaN to the AlGaN/GaN heterojunction, which simultaneously increases the electron density in the channel, resulting in a dramatic increase of the drain current owing to the conductivity modulation. The conduction path between the source and drain contacts are called lateral two-dimensional electron gas (2DEG) structure [2, 45], which is formed at the heterojunction between the GaN and AlGaN layers. The doped p-GaN creates a depletion region between the p-GaN and AlGaN and a normally-off operation of the device is formed.

When applying high drain-source voltage on GaN transistors during off-state, the high voltage bias drops between the drain terminal and the device substrate and then results in the electron trapping effects [45]. The electron trapping effect, which is also called current collapse in some papers, can be contributed to surface trapping and buffer layer trapping [3]. When the high drain-source voltage is applied during off state, the electrical filed between the drain and gate terminal will expel part of the electrons out of the 2DEG and these electrons are trapped in device

buffer layer. When turn on signal comes and channel is on, the high voltage bias returns to zero in tens of nanoseconds but the trapped electrons can not be released instantaneously. As a result, the 2DEG electron density is reduced mad the device on-state current carrying capability by 2DEG also degrades. This phenomenon presents as the increasing dynamic on-resistance and this value will drop relatively slowly back to the nominal value, which is also called static on-resistance as recorded in datasheet. The whole electrons trapping effect is demonstrated in Fig. 3.3.
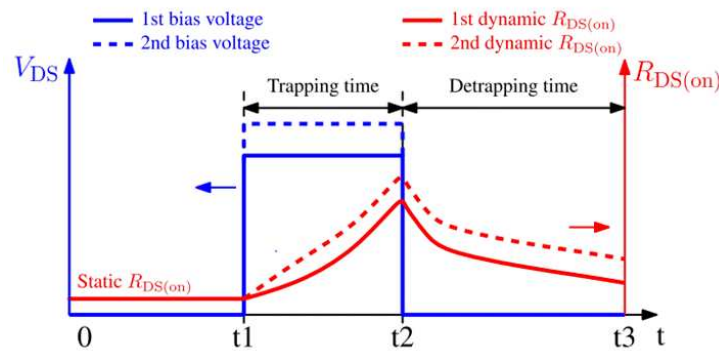
Figure 3.3: On-resistance Change Due to Electrons Trapping Effects [3].

In order to release the trapped electrons for normally-off GaN devices, a new technology using an additional p-GaN region called Hybrid Drain-embedded GIT (HD-GIT) is developed and utilized in the Infineon CoolGaN devices [4] as shown in Fig. 3.4. This additional p-GaN region is straight electrically connected to the drain terminal of the device. To avoid the same depletion of the 2DEG under the p-GaN region, a thicker i-AlGaN layer is designed for the whole device width except the region under the gate p-GaN. Since the normally-off operation still needs to be maintained, the thickness of i-AlGaN layer right underneath the doped p-GaN region on the gate terminal side also needs to be selectively and carefully thinned. In this way, plenty of holes can be injected from the p-GaN region at the drain side and effectively improve

the channel conductivity during the switching transient. However, this method still cant fully solve the current collapse issue.
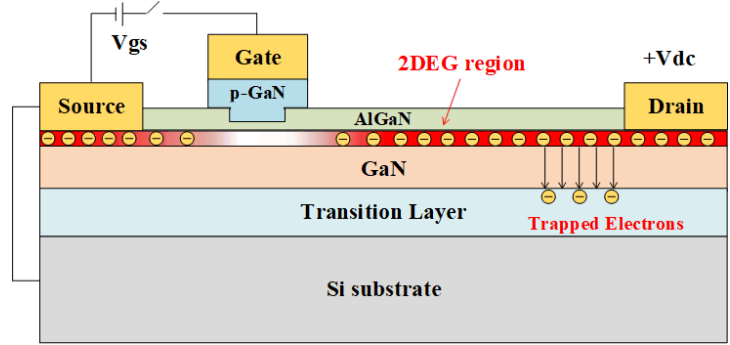
Figure 3.4: Hybrid-Drain-Embedded GIT (HD-GIT) with Recessed Gate Structure.
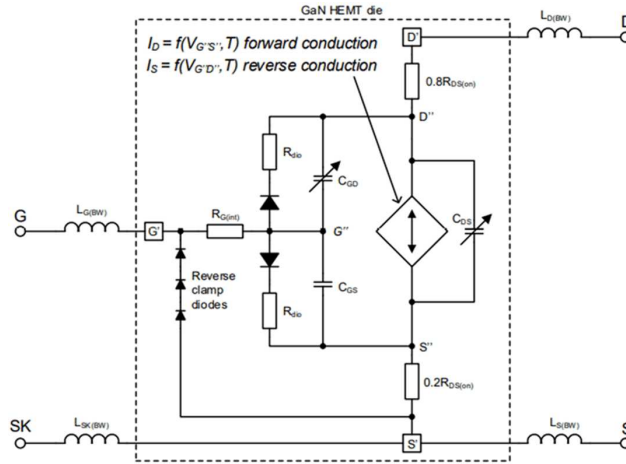
Figure 3.5: Equivalent Circuit of Infineon E-mode CoolGaN-HEMT [4].

A more detailed equivalent circuit of Infineon e-mode CoolGaN-HEMT is shown in Fig. 3.5 [4]. In general, this GaN-HEMT can be regarded as a resistor whose conductivity is controlled by an applied gate voltage in many ways, very similar to a MOSFET. It should be pointed out that the device conducting channel can be estimated using a bidirectional current source between D and S pin. As for the source pin S, there are two connections: one is the conventional source terminal

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for main current loop while the other pin SK is the Kelvin connection specially for gate driver circuit. This split structure can decouple the gate drive loop and main power loop and thus protect the gate drive circuit from the high voltage oscillation on drain source voltage. Also, it minimizes common source impedance effects which can slow down the switching speed of the device, because voltage developed across the common source impedance will subtract from the applied gate voltage, thus reducing the effective gate drive. Another characteristic of this structure is the absence of body diode across the source terminal and drain terminal. In FET like SJ MOSFET, the body diode begins to conduct current when the drain-source voltage goes negative, which generate huge third quadrant conduction loss. But in the GaN HEMT, the HEMT turns back on and behaves as a forward-conducted diode. This is because the HEMT will turn on when the gate voltage is higher than either the source or the drain voltage. One more novel structure is the internal gate diode in parallel with the C_{gs}. During the turn on transient, the gate current flows through the C_{gs}. Once the miller pleatu ends and C_{gs} is fully charged, the gate current will transfer to the internal gate diode and reaches the steady on state. During this time, gate current is around 10 mA - 20 mA and keeps the internal diode continuously on. Therefore, the V_{gs} is actually positively clamped and this value is around 3 V - 3.5 V. That is to say, the internal diode can maintain the V_{gs} stable and protects the gate source pin.

Considering the device structure and electrical model of GaN transistor, hole injection can also be theoretically fulfilled from gate terminal by injecting large gate current. However, the additional p-GaN region on the gate side has limited ability on injecting required hole. Whats more, the gate current during steady on-state is reduced to 10 mA - 20 mA to keep the channel on. The current of this level can hardly supplement enough additional holes into the 2DEG region. However, if a short but high amplitude current pulse is injected into the gate of the device at the beginning of

the on state, in another word, right after the end of the turn-on transient, additional holes can be injected into the 2DEG region. Shown in Fig. 3.6, this high hole injection induces a higher 2DEG density and the enhanced 2DEG density stays higher even during the normal long-pulse gate current of the low hole injection which is a typical value described in the datasheet [81]. As a result, the channel conductivity of the GaN HEMTs is much improved compared to that under the typical gate driving scheme without the high hole injection.
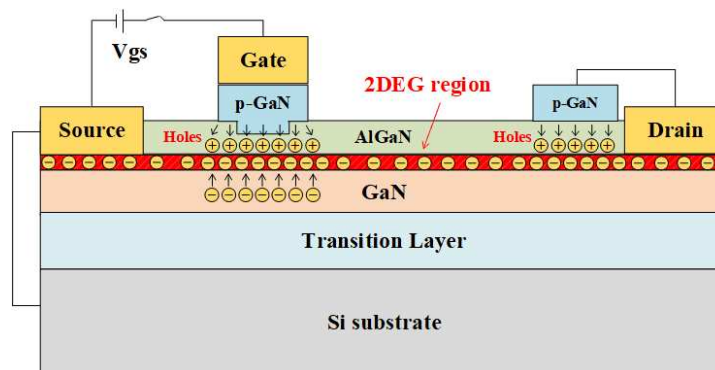
Figure 3.6: Holes Injection Process from Both Gate and Drain Terminals.

3.3   Proposed Multi-Level-Voltage-Output Gate Driver

3.3.1   Gate Current Profile of Proposed Multi-Level-Voltage-Output Gate Driver

The traditional gate current generated by 2-level voltage source gate driver can be divided in three stages as shown in Fig. 3.7. During the steady off-state period T1, the gate current is zero. When the turn-on signal comes, the device enters the on-state T2. During the turn on transient period in T2, the gate current first reaches a high value in very short time to turn on the device. At the miller plateau when the V_{gs} maintains constant, the gate current keeps unchanged and determines the

dv/dt of the device during the switching transient. After the miller plateau, the gate current continues dropping since the C_{gs} is approaching fully charged. Generally, when the gate voltage is fully raised up, the switching transient ends and the gate current starts decreasing quickly until it reaches the rating value. As for the Infineon CoolGaN device, the gate current continuously drops till around 10 mA and then is kept constant 10 mA during the rest on period to maintain the forward conduction of the internal gate diode. When the turn off signal comes, the gate voltage is pulled down to negative level and starts discharging the C_{gs} of the device. Once the C_{gs} get fully discharged, the gate voltage V_{gs} is clamped to this negative level and the gate current becomes zero for the rest of the off period.
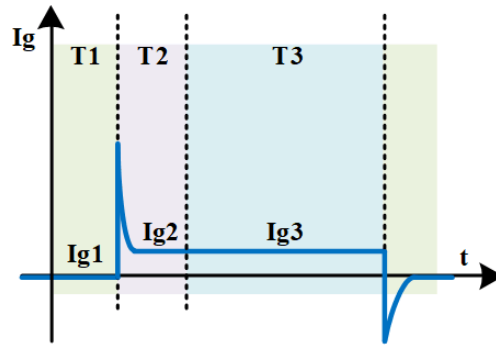
Figure 3.7: Gate Current Profile of Traditional 2-level STD-GD.
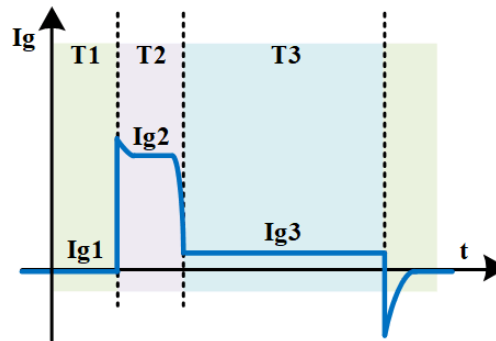
Figure 3.8: Gate Current Profile of the Proposed MVO-GD.

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In contrast, the proposed MVO-GD injects an additional high but short gate current pulse I_{g2} right after the end of the turn-on transient, which is the major difference compared to traditional 2-level gate drive strategy as shown in Fig. 3.8. This high gate current implements the extra hole injection into the 2DEG layer through the gate terminal to achieve dynamic R_{dson} reduction. The amplitude of this extra gate current can be comparable or much higher than the gate current at the miller plateau. The duration time of this current can vary from fifty nanoseconds to several hundreds of nano-seconds. The amplitude and the pulse width of this current both affect the degree of the dynamic R_{dson} reduction and need to be flexibly customized according to specific performance on hole injection and dynamic R_{dson} reduction during the experiment. The optimized parameters will be explored and verified in the later experiment section. The equations to calculate the required gate current in each period are shown in Table 3.3.

Table 3.3: Gate Current Comparison at Different Stages.

Gate current stage	Standard 2-level GD	Proposed MVO-GD
I_{g1} at T1	0	0
I_{g2} at T2	5 mA - 10 mA	500 mA - 2 A
I_{g3} at T3	5 mA - 10 mA	5 mA - 10 mA

The high-level gate current pulse I_{g2} is set as 500 mA - 2 A, which is quite a large range. More detailed instructions about deciding this value will be discussed. Since we are cooperating with Infineon Technology on this project, the high gate current pattern is one of the core discussions in our meetings. The primary goal of this high current pulse is to ensure enough hole injection, which is impossible to be mathematically estimated. Therefore, the experimental performance is the most

effective and straight method to filter out the optimal gate current profile (pulse width and amplitude). Generally speaking, higher current pulse and longer pulse duration time indicate better performance on dynamic on-resistance improvement. However, these two control variables cannot be increased unlimitedly.

First, the maximum of the current pulse width and amplitude need to be determined or explored. There is no doubt a reliability issue if using high current pulse for a long time. We should take this into consideration during the experiments instead of freely increasing the pulse gate current amplitude or width. According to the advice from the Infineon Technology technicians, the gate current better not exceeds 2 A and the current pulse width at this level should be less than 2 μs, which can be regarded as a safety region in their lab test. It should be noted that this profile still way exceeds the data recorded in datasheet, for example the 2 A / 50 ns of IGOT60R070D1. The reason is the different criteria inside the Infineon Technology. Writing the datasheet follows the commercial standards while the lab tests on devices are based on industrial standards. The commercial standards are quite soft and conservative compared to the industrial standards. According to reliable sources from Infineon technicians, the device still maintains stable and excellent performance for thousands of hours switching using 2 A / 2 μs gate current profile. That is to say, the reliability is not a problem within this range.

The tradeoff between the current pulse amplitude and the width should also be carefully considered. Different sets of current pulse width and amplitude are explored during the tests. The gate current pulse amplitude varies from 500 mA to 2 A with an interval of 250 mA. For each amplitude level, we set the pulse width varies from 300 ns to 2 μs with an interval of 300 ns (we set the last point as 2 μs instead of 2.1 μs). After finishing all the double-pulse tests using these different current pulse sets, the dynamic on-resistance measurement data are collected and analyzed. We apologize

that all the specific data and related figures are reserved by Infineon Technology, which is confidential according to the signed agreements. However, we are allowed to draw an illustration plot to roughly demonstrate the results that can help size the gate current profile as shown in Fig. 3.9. Finally, the current pulse of 750 mA is the optimal gate current profile for 600 V/ 70 mΩ device.
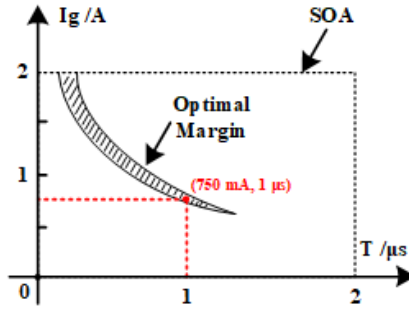
Figure 3.9: High Level Gate Current Region.

A new sizing factor that is directly related to the hole injection performance or dynamic on-resistance improvement can be introduced and expressed in Eq. 3.1:

$$M = I_{\mathrm{G,high}} \times t_{\mathrm{G,high}} \tag{3.1}$$

The three major and core conclusions summarized from plenty of experimental results are as follows:

(1) **Gate current profile of short pulse width but high amplitude is preferred.**: The dynamic on-resistance damps slowly from a large value as the channel is turned on. Therefore, the faster finish the hole injection, the better improvement performance can be achieved.

(2) **Higher M always gives means better dynamic on-resistance improvement. However, the hole injection performance tends to be saturated**

once M exceeds some point. Once crossing this point, the further dynamic on-resistance improvement is not worth the additional gate loss.: This hole injection increases the electron density in 2DEG regions. It is easy to understand that this increasement is not unlimited and tends to be achieving some saturation point, which is pretty much like the RC charging process.

(3) **The optimal region or the saturation point changes when the work conditions change, such as drain source voltage, channel current, device temperature and so on.**: The different work conditions result in different boosted dynamic on-resistance, which leads to different turning points that additional gate loss cover the benefits from dynamic on-resistance improvement.

In conclusion, the tradeoff between the dynamic on-resistance reduction performance and the additional gate drive power consumption and loss needs to be carefully considered without causing obvious reliability problem. The double-pulse test can help you find the optimized pulse amplitude and width, and a relatively low amplitude gate current pulse is preferred, like the selected 750 mA case.

3.3.2 Safe-Operation-Area (SOA) Discussion

One prominent concern of proposed method is the device reliability issue induced by gate current pulse of high amplitude and long duration time. Clearly according to the SOA recorded in data sheet, the proposed method will induce severe reliability issue on device or even destroy the gate. However, after close discussion with Infineon Technicians, we find it is not a problem anymore.

Since we cooperate with Infineon Technology on this project, this topic is also under the discussion with their technicians. According to the meeting records, there

are generally two sets of test criterions in the Infineon Technology: commercial application level and industrial application level. The industrial application level is widely applied in lab test. However, when writing the datasheet, the Infineon Technology follows commercial application level, which is quite soft and mild compared with the industrial application level. Lets take this I_g SOA 2 A at 50 ns as example. During their lab test, the device still shows pretty good and stable performance under this condition even over thousands of hours switching. Although it is forbidden to point out the most extreme test condition of the device, 2 A at 50 ns is still very safe for the device and shows nearly no effect on the device lifetime.

However, as you already pointed out, there is no doubt a reliability issue if using high current pulse for a long time. We should also take this into consideration during the experiments instead of freely increasing the pulse gate current amplitude or width. According to the advice from the Infineon Technology, the gate current better not exceed 2 A / 2 μs. The tradeoff between the current pulse amplitude and the width should also be carefully considered since it is essentially a thermal problem inside the GaN device. Therefore, we explore the different sets of current pulse width and amplitude during the tests. The gate current pulse amplitude varies from 500 mA to 2 A. For each amplitude level, we set the pulse width varies from 300 ns to 2 μs. Finally, the current pulse of 750 mA is the case to be published while the data about higher current amplitude under different pulse width are reserved by the Infineon Technology.

On the other hand, the primary goal of our method is to explore the possible solution to reducing the dynamic on-resistance under high drain-source voltage. The performance improvement is currently the top priority compared with the reliability issue of the device. Right now, the continuous drain-source current limit of the Infineon GaN device is 30 A due to the thermal issue, in which the dynamic on-

resistance issue contributes a lot. However, the proposed method can effectively reduce the dynamic on-resistance value and thus can push this continuous drain-source current limit to a higher level.

3.3.3 Developed MVO-GD Circuit
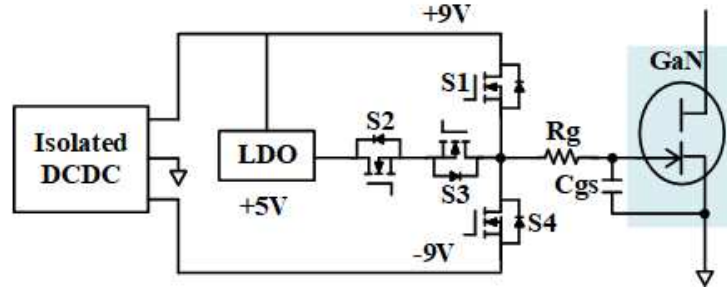
Figure 3.10: Holes Injection Process from Both Gate and Drain Terminals.

To fulfill the proposed gate current pattern, a 3-level gate drive circuit is proposed and shown in Fig. 3.10. The three group of switches, S_1, S_2/S_3 and S_4 are complimentary switched on and off. Switch combination of S_2 and S_3 is in charge of blocking the voltage bidirectionally when these two are in off states. A simplified circuit function map is shown in Fig. 3.11. When the high-level voltage needs to be applied to turn on the device, S_1 is turned on while the other switches are off. To kick in the mid-level voltage after the high current pulse, S_2, S_3 are turned on while the S_1, S_4 are kept off. When the turn off signal comes, S_4 is then turned on and the rest switches are off. Whats more, this low-level voltage discharges the gate capacitor and clamps the gate voltage at a steady negative value.

If the high-level voltage is applied during the period T2, the equivalent C_{gs} will be charged by the high-level voltage through the gate resistor R_g, creating the current pattern presented in Fig. 3.11. At the end of turn on transient, the internal gate diode of the CoolGaN device starts to conduct. The voltage and current of the gate
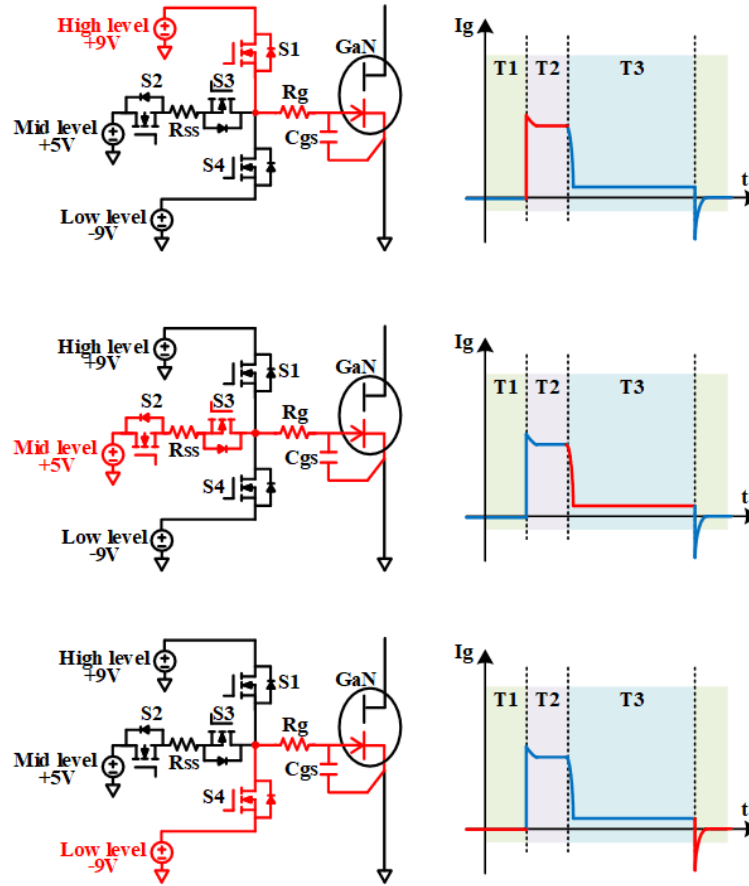
Figure 3.11: Simplified Circuit Function Map of the Proposed MVO-GD.

diode follow a nonlinear V-I characteristic curve. It is around 3 V - 3.5 V if a low gate current 10 mA is fed into the gate, which is the normal case. However, if gate current of hundreds of milliamps is injected into the gate diode, the gate voltage can rise to 4.5 V - 5 V. The gate resistor Rg in Fig. 3.11 is carefully calculated by the needs of injecting high gate current I_{g2} into the gate at the beginning of the on period T2. Assume the high-level voltage is V_{ccH}; mid-level voltage is V_{ccM}; the voltage on the gate diode is V_{diode}. V_{diode} is a function of the current flowing into the gate diode, which is I_g. The equation for R_g is as follows:

$$R_{\mathrm{g}} = \frac{V_{\mathrm{ccH}} - V_{\mathrm{gs}}(I_{\mathrm{g2}})}{I_{\mathrm{g2}}} \qquad (3.2)$$

The value of I_{g2} is decided by the required percentage of dynamic R_{dson} reduction, which needs to be adjusted according to experimental results. To generate the steady state gate current I_{g3}, the mid-level voltage is applied. The I_{g3} is sized around 10 mA to 20 mA for forward conduction of device internal gate diode, which ultimately clamps the gate-source voltage at 3 V - 3.5 V (devices of different ratings give different clamp voltage). Therefore, additional resistor R_{ss} is inserted to shape the required I_{g3} and can be estimated using Eq. 3.2. It should be noted that this R_{ss} cannot be placed on the path of I_{g1} and I_{g2}. Therefore, it has been inserted on the mid-branch of the 3-level VSC-GD before the joined switching node.

$$R_{\mathrm{ss}} = \frac{V_{\mathrm{ccM}} - V_{\mathrm{diode}}(I_{\mathrm{g3}})}{I_{\mathrm{g3}}} - R_{\mathrm{g}} \qquad (3.3)$$

When switching to the off state, S_4 is turned on while the rest three switches are shut down. Then a negative transient current is drawn from the gate and the C_{gs} gets fully discharged quickly. The gate voltage is finally clamped at the low-level voltage and the gate current becomes zero as shown in Fig. 3.11.

Besides the main function circuits discussed in previous section, multi-value parallel decoupling capacitors are employed to eliminate the high frequency oscillation induced by high dv/dt. Three major loops that suffer from voltage ringing are taken into consideration: main power loop, gate drive loop and device driving power supply loop, as shown in Fig. 3.12. As for the main power loop, these capacitors are designed to vary from 10 pF to 100 nF, as listed in Table 3.4, to filter out the high frequency noise. 2 - 4 ceramic capacitors of the same value are placed in parallel to
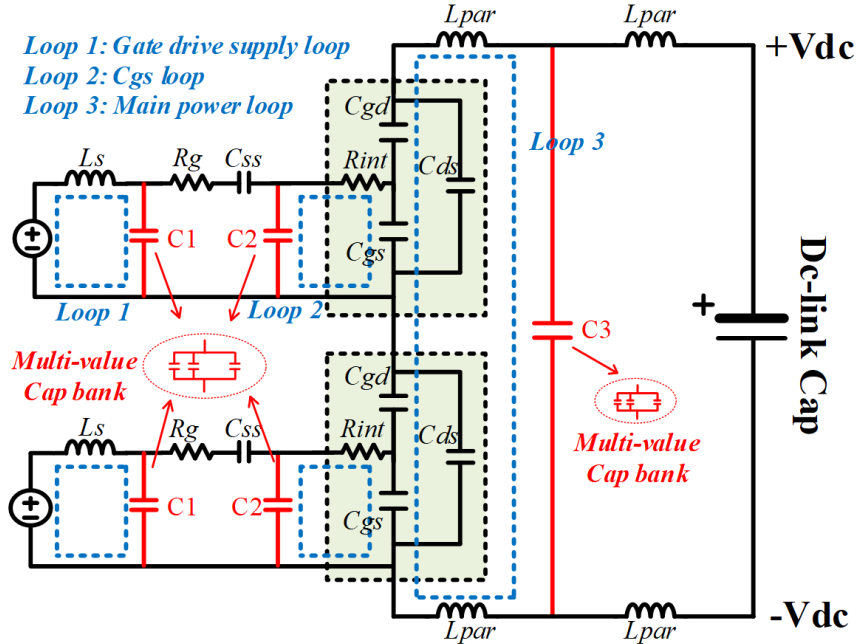
Figure 3.12: Derived Equivalent Circuits Model with Added Multi-value Decoupling Capacitor Banks.

enhance the performance. Multi-value parallel decoupling capacitors for main power loop are placed as close as possible to the device switching stage to maximally damp the high frequency noise induced by the loop parasitic inductance. As for the gate drive loop, extra gate-source capacitors are added to stabilize the gate voltage during the switching transient. These capacitors are designed to vary from 10 pF to 3.3 nF as shown in Table 3.4. Moreover, the footprint package of theses capacitors is set as 0603 to minimize the occupied volume. As for the gate power supply loop, multi-value decoupling capacitors are indispensable because the DCDCs to supply the gate drive power are not placed close to the gate drive loop. This loop is sacrificed a little bit since the gate drive loop is the top priority in the circuit layout. Therefore, these capacitors should be placed right next to the gate drive loop to minimize the power supply loop for the gate drive. That is to say, the return path of the gate current is shortened as much as possible. Under low dv/dt, this strategy may provide limited

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effect. However, under high dv/dt in our case, the improvement on damping gate loop ringing is significant. The selected capacitance varies from 10 pF to 10 nF as also shown in Table 3.4.

Table 3.4: Multi-value Decoupling Vapacitor Bank of Different Loops.

Loop	Capacitor bank setting	Total capacitance
Main power loop	100 nF x 3 6.8 nF x 5 1 nF x 5 100 pF x 5 10 pF x 5	339.55 nF
Gate drive loop	1 nF x 1 100 pF x 1 10 pF x 1	1.11 nF
Gate drive power supply loop	10 nF x 3 1 nF x 1 100 pF x 1 10 pF x 1	11.11 nF

3.3.4   Developed On-resistance Measurement Circuit

To verify the effectiveness of the proposed method on Rdson reduction, an accurate Rdson measurement method needs to be adopted. The first step to obtain the R_{dson} is to sense the V_{dson}. The challenge for V_{dson} sensing is how to block the high V_{dson} during off state. A novel V_{dson} sensing circuit is proposed that can sense the V_{dson} in both first quadrant (forward conduction) or third quadrant (reverse conduction) [97], as shown in Fig. 3.13.
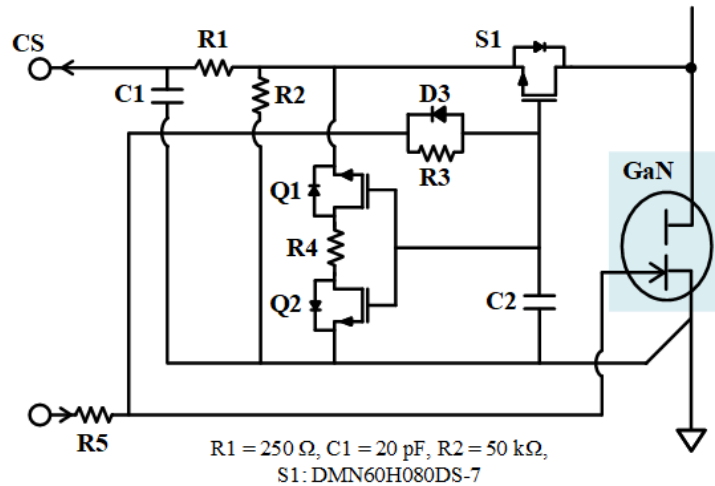
Figure 3.13: Dynamic On-resistance Sensing Circuit.

The MOSFET S_1 is connected to the drain of the device to measure the V_{dson}. When the device is on, S_1 is also turned on. The voltage between the source of S_1 and the source of the GaN device is the V_{dson} of GaN. When the device is off, the high voltage MOSET S_1 is turned off and can block the high voltage. The output of the sensing circuit needs to be clamped to a fixed low voltage to avoid any high voltage appearing at the output port. To clamp the sensing output to a fixed low voltage, a bidirectional switch formed by two switches (Q_1 and Q_2) is connected between the output and the source of the GaN. When the GaN is off, Q_1 and Q_2 will be turned on, the sensing output will be clamped at the on voltage of the Q_1 and Q_2, and the high voltage V_{ds} will be blocked by S_1. R_1 and C_1 are RC filter to filter out the high frequency noise. The key parameters of main components are also shown in Fig. 3.13. When GaN device is in the third-quadrant operation, which conducts current from source to drain with the gate off, the Q_1 and Q_2 is on and S_1 is off. However, the main device current may flow through Q_1, Q_2 and the diode of S_1, since this path is in parallel with the GaN device, and the third-quadrant impedance of the GaN device is as big as the impedance on this path. Therefore, a resistance of R_4 is added in the

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Q_1 and Q_2 path to increase the impedance on this measurement path and prevent the high main current to burn the measurement circuits.

When the measurement circuit stats working during the on period, the S_1 is in series connection with the R_2. According to the datasheet of MOSFET S_1, the R_{ds} under normal continuous state is $67\ \Omega$ which is far smaller than the R_2. Therefore, the voltage drops on the R_2 when S_1 is on is almost equal to the V_{ds} of the device. After passing the filter based on R_1 and C_1, this V_{ds} on R_2 is then captured by the oscilloscope from CS terminal. Therefore, we can collect the GaN V_{ds} waveform as well as the related data points for further data processing in Matlab.

3.4 Experimental Results

3.4.1 Double-Pulse Test Platform and Data Acquisition
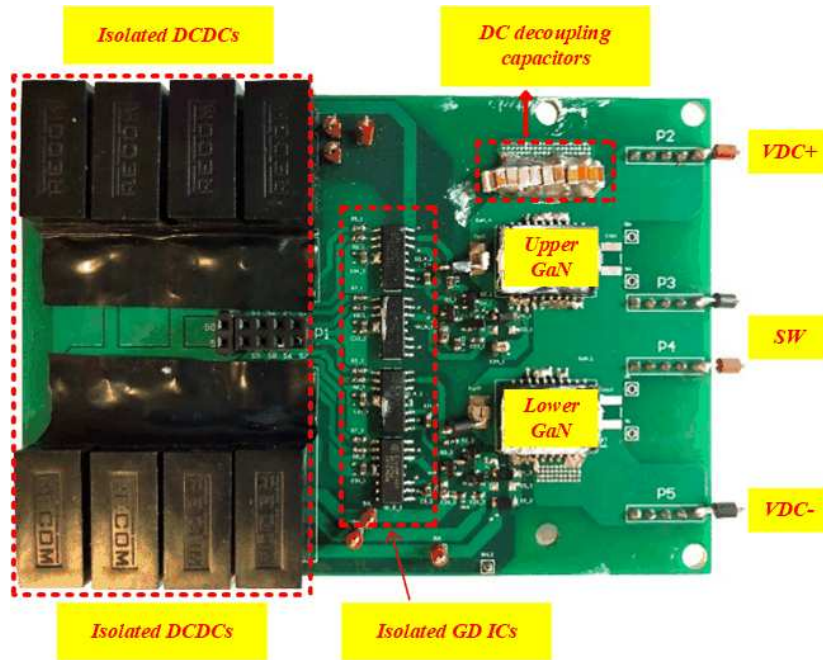
Figure 3.14: The Developed GaN Half-bridge Platform.

As shown in Fig. 3.14, the well-designed GaN half-bridge board equipped with the R_{ds} measurement circuit is built up to verify the degree of dynamic R_{ds} reduction using proposed MVO-GD. Since the gate drive result is of the most importance, the layout of the gate drive loop and main power loop is the top priority. Besides the multi-value decoupling capacitor bank, One recommended way to minimize the voltage oscillation is to minimize the stray inductances along the current path in the power loop. One possible way to achieve reasonably small overshoots with the DSO packages is to minimize the area defined by the power-loop current. In practice, this means using the mid-layers as a current return path to route the current back as close as possible to the forward path. This concept is shown in Fig. 3.15. The two layers are connected with vias.
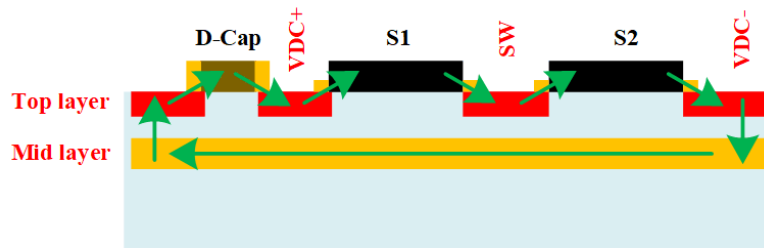
Figure 3.15: Main Current Loop on PCB Board.

The different comparative double-pulse tests will be conducted between MVO-GD and STD-GD with different parameter setting and different working conditions, such as varying dc-link voltage, different device temperature and changing pulse width of the extra high gate current I_{g2}. However, the very first step of these series of double pulse tests should be the R_{ds} sensing test and data acquisition.

Let us take the STD-GD under 600 V / 15 A case as example to explain how we extract the measured device on-resistance value. The R_{dson} measurement circuit and the position we place the probes are shown in Fig. 3.16. The original double-pulse
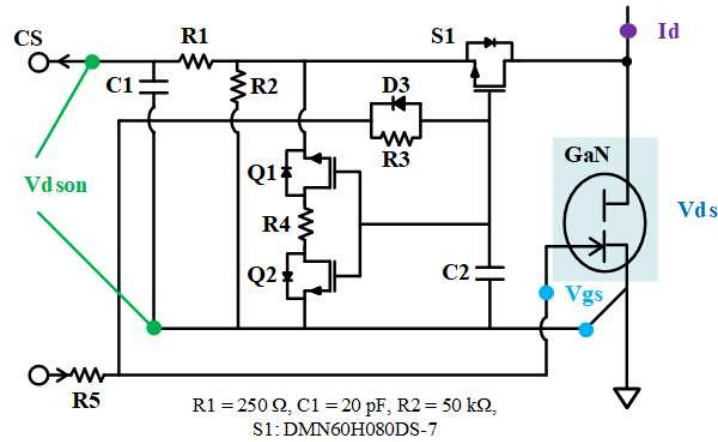
Figure 3.16: Dynamic On-resistance Sensing Circuit with Probes.

test waveform is shown in Fig. 3.17. As requested by the Infineon Technology, an oscilloscope with high noise immunity and good dv/dt immunity differential probe is utilized to present the waveforms and record the data points in an excel file.

To demonstrate the overall waveform of the double-pulse test in Fig. 3.17(a), the oscilloscope time scale is set as 4 μs/div. However, only the waveform of second pulse is what we truly focus on, which is round 8 μs. After carefully checking the waveform, the data of all four channels are reserved as a excel file for further processing in Matlab. The data sampling rate is fixed at 100k points. Since the high-frequency noise on the measured V_{dson} is small, it will have limited impact on the measurement of the dynamic on-resistance. Therefore, the sampling rate of 100k is enough for our test. Once we get the file, we use Matlab to extract the data of all four channels and apply a moving average filter to filter out the high-frequency noise mentioned before. Generally, the waveforms during second pulse are recorded as a 20k points data for each channel. After the digital moving average filter, the 20k points table is further compressed as a 4k points table. Then, the dynamic on-resistance R_{dson} is extracted by dividing the V_{dson} by the I_{d} and saved as another 4k points table. Finally, all these

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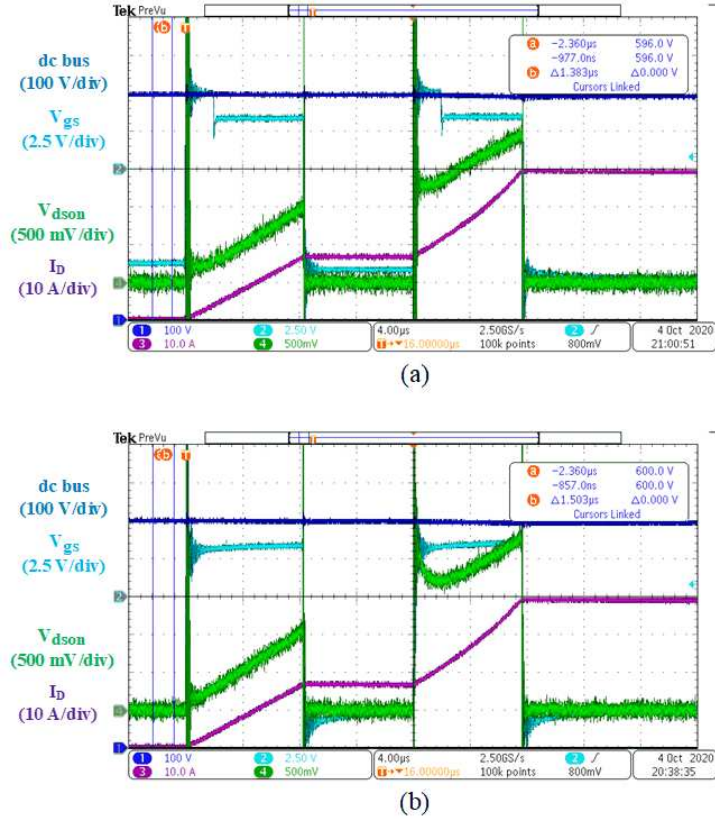
Figure 3.17: Double-pulse Test Waveforms: (a) Zoom out Version of MVO-GD;(b) Zoom out Version of STD-GD.

refined tables are what we use to plot the figures in Matlab and shown in the report.

Fig. 3.18 shows the processed double-pulse test waveforms using Matlab. For STD-GD, the steady state gate current I_g is set as 20 mA. As for MVO-GD, the high gate current pulse I_{g2} is set to be 750 mA. The steady state gate current I_{g3} for gate diode forward conduction is also set to be 20 mA. The duration time of the high current pulse in MVO-GD varies from 300 ns to 1.5 μs.

3.4.2 R_{dson} Measurement under Different Drain-source Voltage

The effect of drain source voltage amplitude on the dynamic R_{dson} as well as on the improvement of the dynamic R_{dson} have been studied in this section since it is

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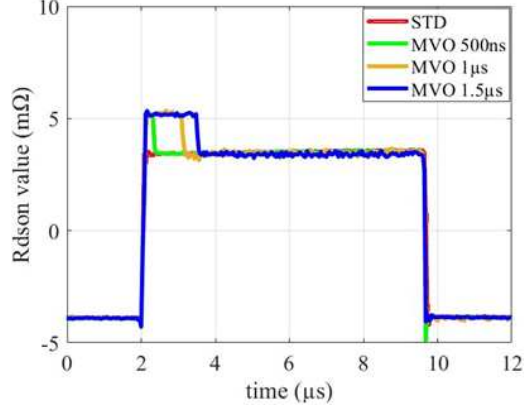
Figure 3.18: Sampled V_{gs} Waveform with Different High-level Current Pulse Width.

directly related to the substrate bias. The dynamic R_{dson} issue is more prominent at high drain source voltage condition than that in the lower voltage case. The related R_{dson} measurement result for STD-GD is shown in Fig. 3.19(a) while those of the MVO-GD are shown respectively according to pulse width in Fig. 3.19(b)(c)(d).

As shown in Fig.3.19 (a), once the drain source voltage is gradually increased from 400 V to 600 V, the dynamic R_{dson} changed from 1.56 times of the base R_{dson} to 2.25 times of the base R_{dson}. The R_{dson} difference between the 400 V and 500 V cases are not big, but shows significant growth when voltage increases from 500 V to 600 V. The trend of the increase is nonlinear. This is expected because higher drain source voltage means higher substrate bias and results in worse dynamic R_{dson} issue. In the MVO-GD 300 ns case shown in Fig. 3.19(b), the dynamic R_{dson} is reduced from 1.63 times of base value to 1.57 times of the base value at $V_{\text{dson}} = 500$ V case; and it reduces from 1.56 times of the base value to 1.4 times of the base value at $V_{\text{dson}} = 400$ V case. The percentage of R_{dson} drop in these two cases is close, which is around 10 % - 15 %. However, when the V_{dson} is 600 V, the dynamic R_{dson} drops from 2.25 times of the base value to 1.57 times of the base value, which is almost 40 % drop. It means

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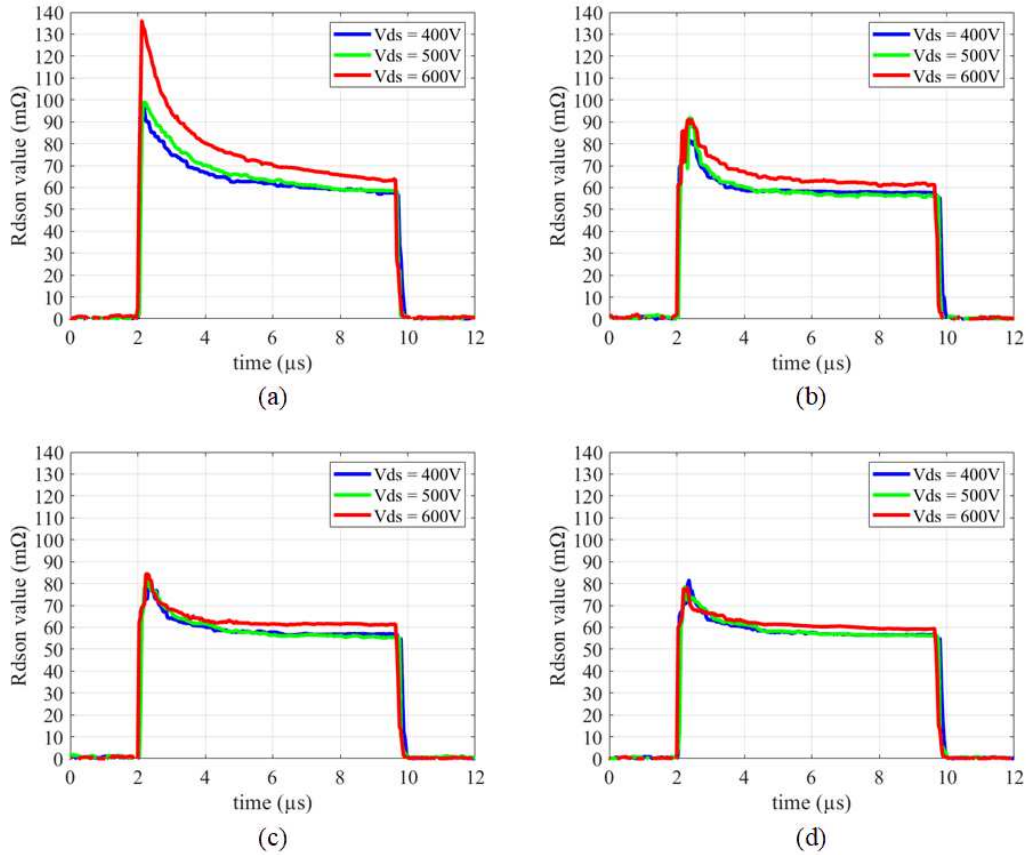
Figure 3.19: Dynamic On-resistance Test Results Compariso Between MVO-GD and STD-GD: (a) Dynamic R_{dson} under Different V_{dson} in STD-GD When $I_{dson} = 15$ A; (b) Dynamic R_{dson} under Different V_{dson} in MVO-GD 300 ns When $I_{dson} = 15$ A; (c) Dynamic R_{dson} under Different V_{dson} in MVO-GD 1 μs When $I_{dson} = 15$ A; (d) Dynamic R_{dson} under Different V_{dson} in MVO-GD 1.5 μs When $I_{dson} = 15$ A.

that the dynamic R_{dson} improvement is much more significant when V_{dson} is above 500 V. If further increasing the high current pulse width, as shown in Fig. 3.19(c) and (d), the dynamic R_{dson} drops from 1.57 times at 300 ns to 1.42 times at 1 μs and 1.3 times at 1.5 μs. The improvement is still outstanding, but the gate drive loss and device reliability issue also becomes more and more unneglectable. Therefore, the tradeoff needs to be seriously considered.

In summary, the dynamic R_{dson} shows limited difference when the V_{dson} is under

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500 V. However, an obvious increase can be observed for both dynamic and steady R_{dson} when the V_{dson} is above 500 V; Meanwhile, the performance of the proposed MVO-GD is also more and more prominent on either dynamic R_{dson} or the steady R_{dson}, especially when the V_{dson} reaches 600V. Therefore, compared with the STD-GD, the MVO-GD can effectively reduce the conduction loss and thus push the drain source voltage to higher level within a limited thermal environment.

3.4.3 R_{dson} Measurement under Different Device Junction Temperature

The device temperature is another important point that may affect the dynamic R_{dson} of the Infineon CoolGaN device. The double-pulse tests for both STD-GD and MVO-GD with same experiment specifications are conducted both under 400 V / 15 A condition but in two different device junction temperature conditions. One is kept at room temperature while the other is heated till 125°C by a blow welding machine. The related experiment results are shown in Fig. 3.20(a) and (b). Under room temperature, the dynamic R_{dson} improvement is close to the similar setup cases discussed in previous sections. However, as the device junction temperature is increased to a relatively high value, the dynamic R_{dson} in STD-GD sharply increased while the static R_{dson} also became larger. With the device junction temperature raised up from 25 °C to 125 °C, the peak dynamic R_{dson} in STD-GD jumps from 99 mΩ to 200 mΩ, which is almost doubled. Meanwhile, the static R_{dson} increases from 60 mΩ to 125 mΩ. However, the dynamic R_{dson} in the MVO (1.5 μs / 750 mA) case is milder. The peak dynamic R_{dson} increases from 85 mΩ to 175 mΩ. In addition, at 125 °C, the steady state R_{dson} of MVO-GD is 120 mΩ while that of the STD is 125 mΩ. Thus, the MVO-GD also presents a 5% R_{dson} improvement in steady state.

In summary, as the device junction is heated to 125 °C, the dynamic on-resistance issue becomes much worse. In this situation, the proposed MVO-GD generates less
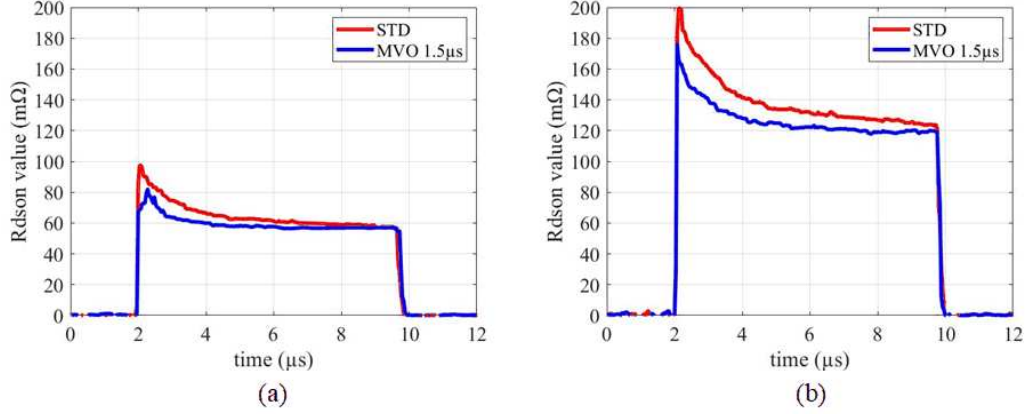
Figure 3.20: Dynamic On-resistance under Different Device Junction Temperature: (a) Dynamic R_{dson} at $T_{\mathrm{j}} = 25$ °C when $V_{\mathrm{dson}} = 400$ V, $I_{\mathrm{dson}} = 15$ A; (b) Dynamic R_{dson} at $T_{\mathrm{j}} = 125$ °C when $V_{\mathrm{dson}} = 400$ V, $I_{\mathrm{dson}} = 15$ A;

conduction loss due to the dynamic R_{dson} improvement as shown in Fig. 3.20(b). It is worth noting that the drain-source voltage in the test is only 400 V. More exciting result is foreseeable if the drain-source voltage is pushed to higher voltage, such as 500 V or even 600 V.

3.4.4 R_{dson} Measurement under Different Gate Current Pulse Width in Period T2

In this section, the gate current pulse width is adjusted while the other test conditions are kept unchanged to demonstrate the effect of gate current pulse width on the dynamic R_{dson} alone. Basically, the current pulse width stands for the additional holes that are injected into the device 2DEG. In the STD-GD, the gate current is kept as low as 20 mA all the time. As for the MVO-GD, the amplitude of high-level gate current pulse I_{g2} is set as 750 mA while the mid-level gate current I_{g3} keeps the same as that in the STD-GD. The associated dynamic R_{dson} measurement results in 400 V / 15 A double-pulse test are shown in Fig. 3.21. Theoretically, the STD-GD can be

regarded as MVO-GD with zero high level current pulse. Once a 300 ns high-level current pulse is applied during the on state, the dynamic R_{dson} can be effectively reduced because large amounts of holes flow into the channel to increase the electrons density during this period. However, as the current duration time is extended to 1.5 μs, not much dynamic R_{dson} improvement can be further obtained. This means that the injected holes are close to some saturation point. Longer current pulse is about to reduce the marginal revenue of the hole injection method since the additional gate loss from the high current pulse is also getting larger and larger. At some critical point, the gate power consumption may overwhelm the benefits from improving the dynamic on-resistance. Therefore, the trade-off between gate current pulse width and the dynamic on-resistance improvement degree should be considered.
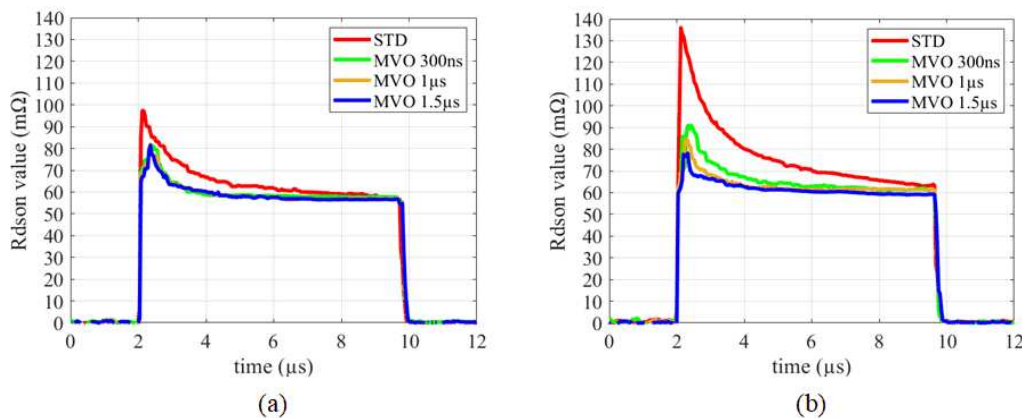
Figure 3.21: Dynamic On-resistance under Different Gate Current Profiles: (a) Dynamic R_{dson} under Different Gate Current Pulse Width When $V_{\text{dson}} = 400$ V, $I_{\text{dson}} = 15$ A; (b) Dynamic R_{dson} under Different Gate Current Pulse Width when $V_{\text{dson}} = 600$ V, $I_{\text{dson}} = 15$ A.

As shown in Fig. 3.21(b), the dynamic R_{dson} gap between the STD-GD and MVO-GD tends to be larger once the dc-link voltage increases from 400 V to 600 V. In 400 V case, the MVO-GD improves the dynamic R_{dson} by almost 20%; When coming to 600 V case, the MVO-GD improves the dynamic R_{dson} by nearly 40%, which is

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quite remarkable. This is mainly because the dynamic R_{dson} in the STD-GD increases quite a bit when the drain source voltage rises, which also verifies the result shown in previous section. However, the dynamic R_{dson} in MVO-GD case presents little variation when the voltage raises from 500 V to 600 V, which again demonstrates the effectiveness of the R_{dson} improvement. In conclusion, the proposed MVO-GD can restrict the dynamic R_{dson} within a relatively small value even if the device drain source voltage is pushed to an extreme high level. As reduced dynamic R_{dson} means less conduction loss, the thermal issue can be significantly alleviated especially under high power applications. Therefore, the MVO-GD enables the device work under higher voltage and power compared to that in conventional STD-GD.

It is also worth noting that the dynamic R_{dson} difference between MVO-GD 300 ns case and MVO-GD 1.5 μs case also becomes larger when $V_{\mathrm{ds}} = 600$ V. According to the previous analysis, this means the saturation gate charge rises when the V_{ds} is higher. The deeper illustration is that more electrons get trapped at higher voltage. Therefore, more holes need to be injected to help attract more electrons filling in the missing parts and restore the electron density in 2DEG.

3.5   Buck Converter Efficiency Test

The R_{dson} measurement results on the double-pulse test platform already confirm that the dynamic R_{dson} increasement can be effectively reduced using proposed MVO-GD regardless of varying experimental conditions. However, this exciting verification is just based on the pulse level test so far. The dynamic R_{dson} study needs to be further extended to power converters to see whether it still hold the benefits under continuous switching mode. Since the R_{dson} is directly related to the conduction loss, the efficiency of power converters can be a good reference to reflect the change of R_{dson}. If conducting the efficiency test on these converters, the R_{dson} gap between

the STD-GD and MVO-GD can be directly observed from efficiency data. A 400 V / 2 kW synchronous buck converter with 0.5 duty cycle has been built based on the proposed half-bridge hardware. The test set-up parameters are listed in Table 3.5.

Table 3.5: Buck Converter Specifications.

Parameters	Value
V_{in}	400 V
V_{out}	200 V
f_{sw}	32.5 kHz - 130 kHz
Duty ratio	0.5
Inductor	760 μH
Dc-link Cap	12 μF
DUT	Infineon IGOT60R070D1
Power	2000 W

In the following buck converter efficiency test, switching frequency and converter power level are the two major control variables to shape the efficiency curve. The related efficiency data will be analyzed and discussed. The switching details of buck converter test are shown in Fig. 3.22 and Fig. 3.23. The dc/dt between the STD-GD and MVO-GD is synchronized around 32 V/ns and thus the switching loss is almost the same. Under this high dv/dt, the V_{ds} and V_{gs} voltage overshoots are well suppressed. Although some high frequency noise as high as 62 MHz can be observed but it is just small concern and shows little influence on the results.

The device loss also consists of two parts: switching loss and conduction loss. The switching loss depends on the switching node voltage dv/dt while the conduction loss counts on the on-resistance of the devices. This is where MVO-GD should have advantages over STD-GD. From the zoomed in switching waveforms shown in

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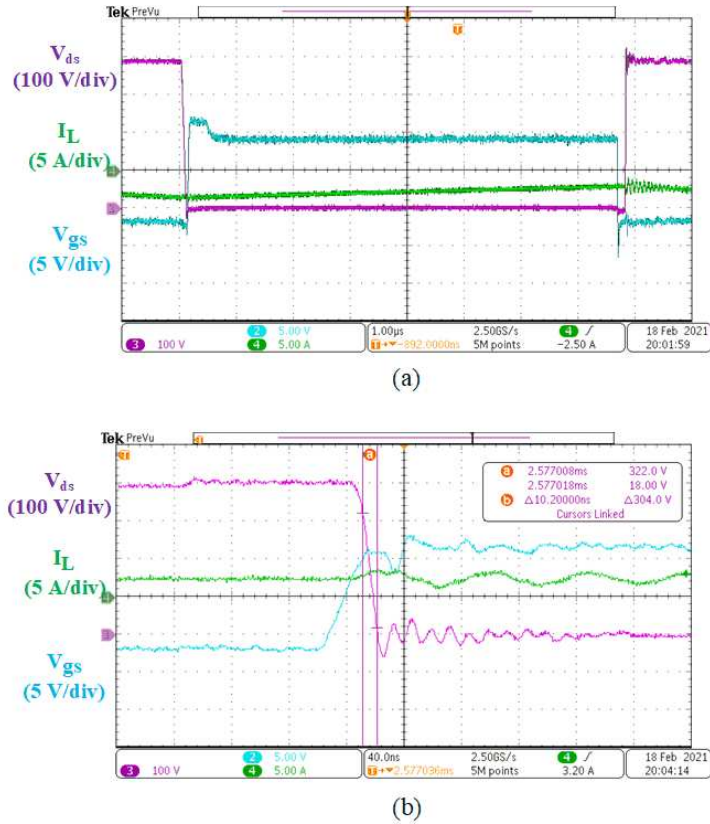
Figure 3.22: Switching Waveforms of MVO-GD: (a) Zoom Out; (b) Zoom In.

Fig. 3.22(b) and Fig. 3.23(b), similar slew rates of switching node voltage can be observed both for MVO-GD and STD-GD, which means the device switching loss can be regarded the same for both cases. Since all the rest experimental set-up is unified, the only factor that may cause the loss difference is the device conduction loss. Therefore, any difference in converter total loss directly comes from conduction loss gap between two cases, which further means the difference in dynamic R_{dson}.

During the efficiency test, all the data are collected from the power analyzer through an USB port. Since the thermal issue does affects the transistor loss, only the data within last 5 minutes in a 20-minute efficiency test are reserved for a more convincing and reliable conclusion. This is because that the tested platform cannot
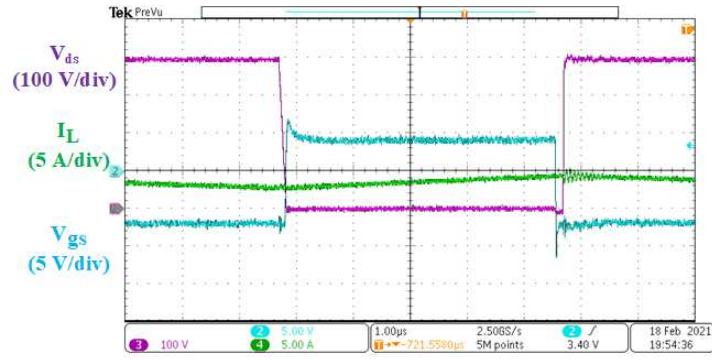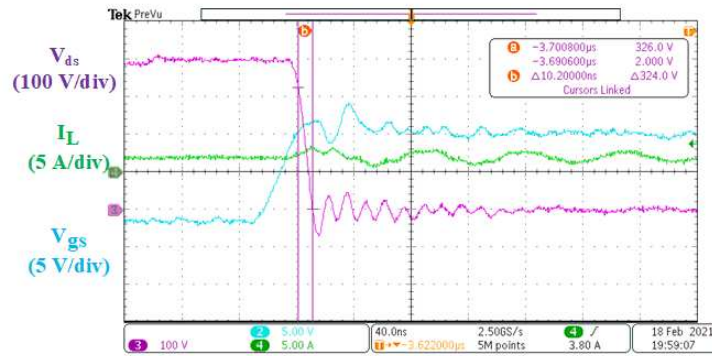
Figure 3.23: Switching Waveforms of STD-GD: (a) Zoom Out; (b) Zoom In.

reach thermal saturation unless it is running for long enough time. Once achieving the thermal saturation, the device temperature remains unchanged so as the transistor loss.

3.5.1 Buck Efficiency Test under Different Power Level

To fully study the R_{dson} improvement of the proposed drive strategy under rated operating condition, the efficiency tests for both STD-GD and MVO-GD are conducted under different power levels. Higher power means higher flowing current and thus amplifies the conduction loss in the half-bridge, which is the core reason for the widening efficiency gap. As the switching transient is already synchronized, the efficiency

gap in the buck converter is only determined by the dynamic R_{dson} difference.
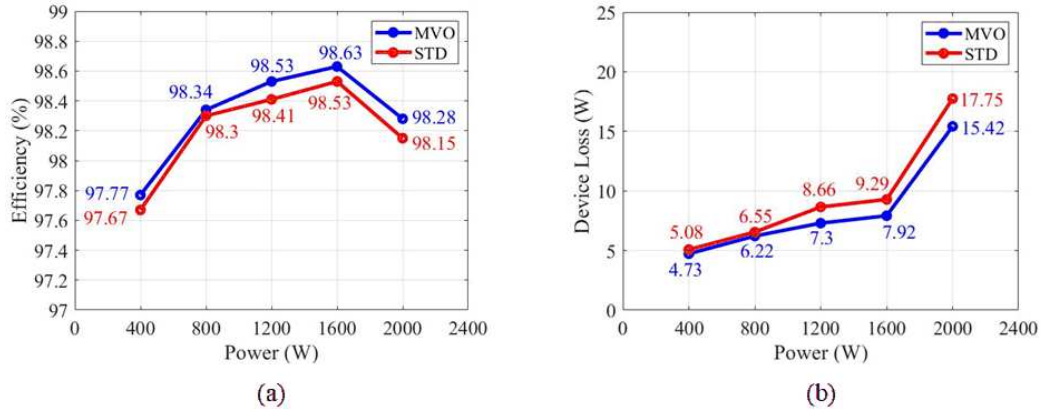
Figure 3.24: 100 kHz Buck Converter Test Results under Different Power Levels: (a) Efficiency Curve; (b) GaN Device Loss.

The efficiency curve and GaN device loss comparison between the STD-GD and MVO-GD are shown in Fig. 3.24. As shown in the Fig. 3.24(a), the efficiency gap is not obvious when the power is less than 800 W. This is because that the device current is as low as 3.2 A and consequently the conduction loss gap induced by dynamic R_{dson} is almost neglectable. However, as the power increases, the efficiency gap between the STD-GD and MVO-GD becomes more and more prominent. Finally, this value reaches as large as 4 W when running at 2 kW. The gate drive power consumption shown in Fig. 3.24(b) keeps almost unchanged, which brings zero effect on the efficiency. Thus, the conduction loss gap directly represents the efficiency gap or the dynamic R_{dson} gap. This significant efficiency gap fully validates the dynamic R_{dson} improvement under rated operating condition using proposed MVO-GD strategy.

3.5.2 Buck Efficiency Test under Different Switching Frequency

The other studied variable in the efficiency test is the switching frequency of the GaN device. The efficiency test under 32.5 kHz, 65 kHz, 100 kHz and 130 kHz switching frequency are conducted on the buck converter. The related experiment result is organized in chart line shown in Fig. 3.25. The positive correlation between loss reduction and switching frequency is a further proof of the good performance of MVO-GD on improving the dynamic R_{dson}. Higher switching frequency generally means more switching cycles under same period. Assuming the same duty cycle, as switching frequency is higher and higher, the on period of the device tends to be shorter and shorter. Since the effect of dynamic R_{dson} mainly appears within a few microseconds after it is turned on, the dynamic R_{dson} region takes a bigger portion during the on period and thus the average R_{dson} becomes larger in STD-GD. However, as for the MVO-GD, since the dynamic R_{dson} effect has been reduced, it can benefit more from MVO-GD in terms of loss reduction in high-frequency applications. Although the switching loss also increases under higher switching frequency, both cases are consistent in this loss growth and thus makes no impact on the efficiency gap. In conclusion, although the dynamic R_{dson} issue is more severe under higher switching frequency, the proposed MVO-GD demonstrates a quite effective dynamic R_{dson} improvement and prominent advantages over the STD-GD strategy.

3.6 Power Factor Correction (PFC) Converter Efficiency Test

In previous sections, the proposed MVO-GD strategy has been proved effective on reducing the dynamic R_{dson} under double-pulse test and buck converter. However, the buck converter is the most basic application that extends the test from pulse mode to the continuous mode. All the experiment setup during one single test stays fixed,
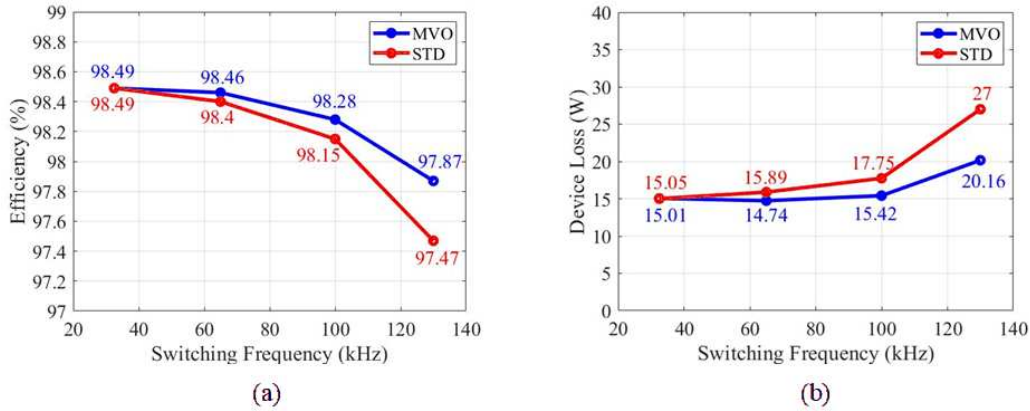
Figure 3.25: 2 kW Buck Converter Test Results under Different Switching Frequency(a) Efficiency Curve; (b) GaN Device Loss.

such as the duty ratio, current value, current direction and so on. This simple and monotonous buck converter platform causes the conclusion not persuasive enough if trying to popularize this MVO-GD method in more complex applications, such as AC-DC converters. Therefore, the comparative tests between the proposed MVO-GD and STD-GD on a more complicated and industrial platform is necessary and important. Moreover, the benefits of this method make it very suitable for high-voltage and high-efficiency applications using GaN devices.

After comprehensive consideration, the Power Factor Correction (PFC) is chosen as the targeted industrial application platform to further validate the proposed MVO-GD. Firstly, as the system efficiency is the core characteristic of PFC application, the advantages of proposed method can get maximally highlighted. Secondly, the varying current direction and amplitude create a more challenging environment. In addition, the duty ratio of fast switching stage also keeps changing under the closed loop control of PFC. All these characteristics strengthened the persuasiveness of proposed MVO-GD.

A 400 V / 2.4 kW high-frequency totem-pole PFC platform has been well assem-
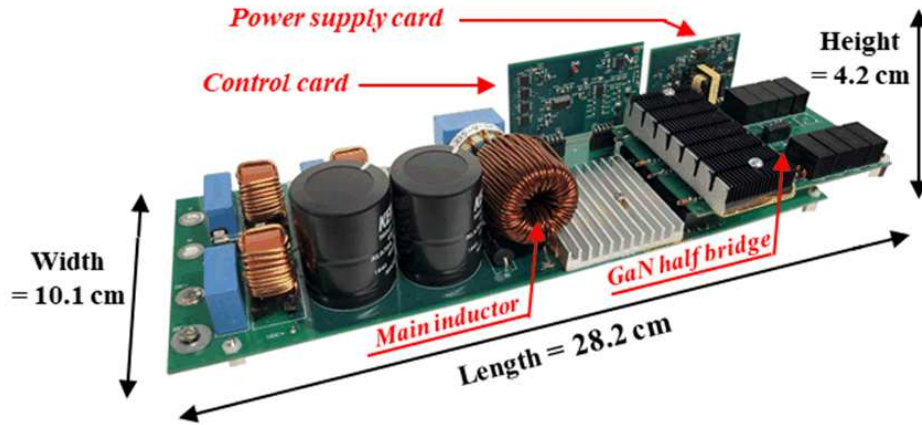
Figure 3.26: 2.4 kW PFC Platform.

bled as shown in Fig. 3.26. All the important specs are listed in Table 3.6. This PFC is designed to work in Continuous Current Mode (CCM) for much lower input current ripple and better total harmonic distortion factor. Also, all diodes along the current path have been replaced with low on-resistance Si transistors.

The PFC main inductor consists of three stacked distributed airgap cores using high-flux material from Magnetics, which can maintain high inductance over a wide frequency range without overlaying windings to minimize the stray capacitances. EMI filters are placed on both input side and output side, which are aimed to reduce the common mode noise and differential mode noise on the power ports of the PCB board toward the AC input power source and the load. The control card and other auxiliary circuits including MOSFET drivers are supplied by a flyback circuit based auxiliary power supply daughter card. As for the mentioned control card, a CCM-PFC controller IC from the Infineon Technology is used for classic Totem-pole PFC close loop control operation. Besides, additional analog circuits like DCM monitor and zero window comparator have been added for better stability and reliability.

The PFC main inductor consists of three stacked distributed airgap cores using

Table 3.6: PFC Platform Specifications

Parameters	Value
V_{in}	230 V
V_{dc}	400 V
f_{sw}	65 kHz - 95 kHz
Duty ratio	0.05 - 0.95
Dc-link Cap	1.2 mF
Main inductor	3 x C058071A2, 650 μH
PFC IC	ICE3PCS01GXUMA1
Power	2500 W

high-flux material from Magnetics, which can maintain high inductance over a wide frequency range without overlaying windings to minimize the stray capacitances. EMI filters are placed on both input side and output side, which are aimed to reduce the common mode noise and differential mode noise on the power ports of the PCB board toward the AC input power source and the load. The control card and other auxiliary circuits including MOSFET drivers are supplied by a flyback circuit based auxiliary power supply daughter card. As for the mentioned control card, a CCM-PFC controller IC from the Infineon Technology is used for classic Totem-pole PFC close loop control operation. Besides, additional analog circuits like DCM monitor and zero window comparator have been added for better stability and reliability.

The PFC steady-state waveform has been demonstrated in Fig. 3.27. Once starting the ac input source, the dc bus of this PFC platform is first pre-charged through the diode bridge. Then, the auxiliary power supply card gets activated by the input ac voltage and wakes up the control card in a short period. The PFC platform can finish boosting the dc bus voltage till the rated value in 200 ms. During the steady

state, the inductor current closely keeps in phase with the input voltage and the current ripple on the main inductor is within 1.5 A.
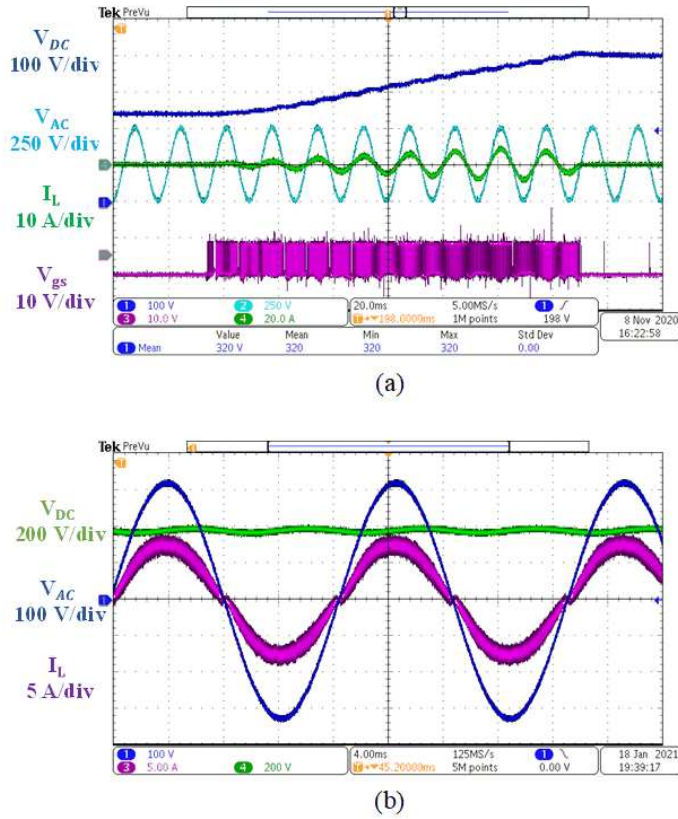
Figure 3.27: PFC Platform Performance: (a) PFC No-load Start-up; (b) PFC Steady State Waveform.

3.6.1 PFC Efficiency Test Under Different Power Level

The comparative PFC efficiency tests for MVO-GD and STD-GD cases are conducted at multi-power levels from 400 W to 2400 W. Since the PFC platform holds larger size and volume, the efficiency test running time is further extended to 30 minutes for sufficient thermal saturation. Moreover, the same mother board for the comparative experiment guarantees the same electromagnetic loss and dc bus electrolytic capacitor loss.

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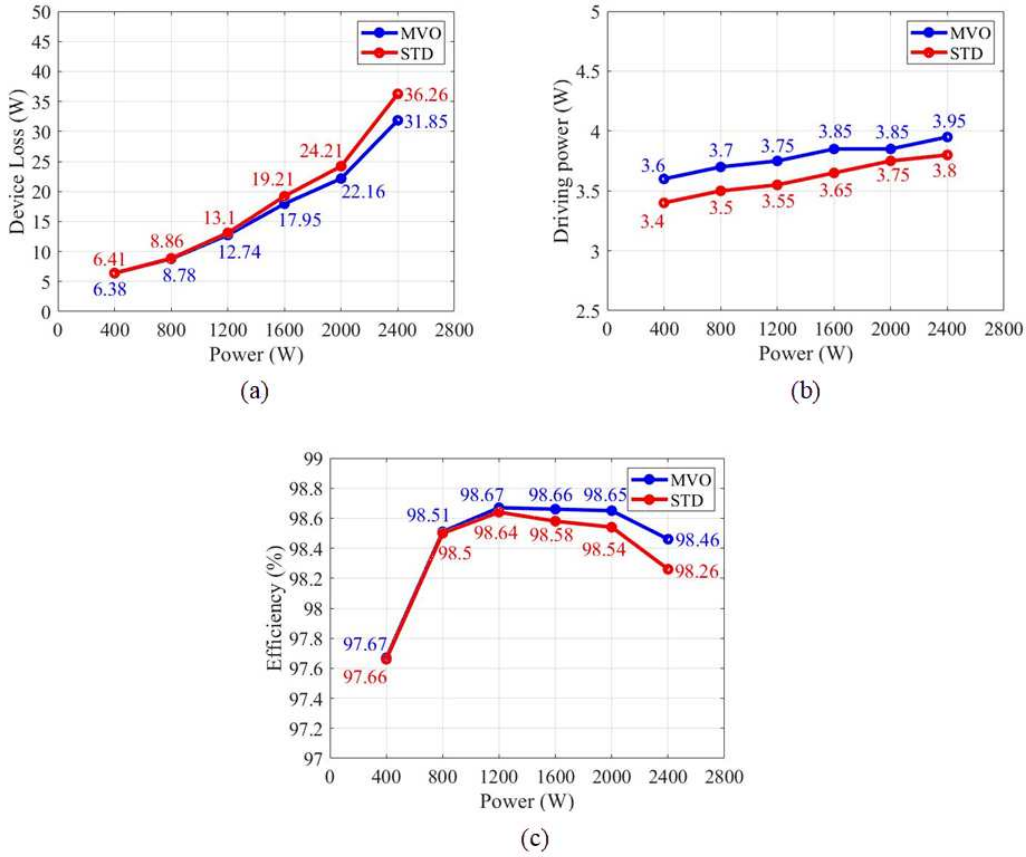
Figure 3.28: 85 kHz PFC Test Results under Different Power Levels: (a) GaN Device Loss; (b) Gate Drive Power; (c) Efficiency Curve.

The specific experimental results of these two cases are demonstrated in Fig. 3.28(a). Since the switching loss has been modulated as the same, the GaN device loss gap directly stands for the conduction loss gap which further means R_{dson} gap. As shown in Fig. 3.28(b), little power gap between MVO-GD and STD-GD can be observed as the power increases. Thus, the gate driver power can hardly cause efficiency gap between these two cases.

The efficiency tests result of both cases have been well organized into a chart line shown in Fig. 3.28(c). The efficiency gap between STD-GD and MVO-GD is neglectable at low-power region. However, as the power increases, the efficiency gap

is growing and achieves 0.2% at 2.4 kW, which means 4.8 W device conduction loss gap. This significant loss gap validates the improvement on R_{dson} by the proposed MVO-GD strategy even under more complicated work condition. If using MVO-GD, the PFC power can be pushed to a higher level while keeping the high-efficiency performance.

3.6.2   PFC Efficiency Test Under Different Switching Frequency

As conducted in previous buck converter efficiency test, the comparative efficiency tests under 65 kHz, 85 kHz and 95 kHz are all conducted under 2 kW and 2.4 kW power. The 30-minute run time is also guaranteed. Meanwhile, all the rest experiment setup is the same as that in the tests under different power levels.

The associated experiment results are shown in Fig. 3.29. As expected, the efficiency gap between the MVO-GD and the STD-GD tends to increase and thus the dynamic R_{dson} improvement becomes more and more obvious and remarkable, just like the test results on buck converter. Especially in the test at 2.4 kW at 95 kHz, the efficiency improvement reaches 0.19%, which means the reduced power loss is as large as 4.6 W. Although involving changing duty ratio and varying current condition, significant efficiency or the dynamic R_{dson} improvement can still be observed. Therefore, this experiment result further verifies the effectiveness and superiority of the proposed MVO-GD drive strategy.

3.7   Conclusion and Future work

The dynamic on-state resistance issue of Gallium Nitride high-electron-mobility transistors (GaN-HEMTs) under high drain-source voltage are well discussed in this section. A novel voltage source based Multi-Level-Voltage-Output gate drive (MVO-GD) strategy is proposed, which can inject plenty of holes into the layers through gate

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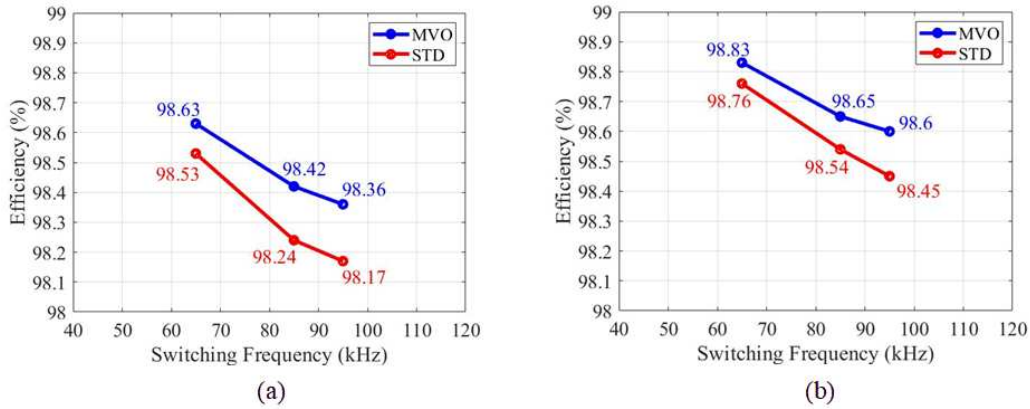
Figure 3.29: PFC Efficiency Curve under Different Switching Frequency: (a) 2 kW PFC; (b) 2.4 kW PFC.

channel and help restore the electrons density in the 2DEG. In this way, the dynamic on-state resistance issue is effectively improved. The well-designed gate drive circuit is described in detail as well as the on-state resistance measurement circuit. The proposed gate drive strategy is then verified on three hardware platforms: double-pulse test, buck converter and Totem-pole PFC. The double-pulse test explores the influence of different test conditions on the dynamic on-state resistance as well as the performance of proposed MVO-GD. Ultimately, remarkable advantages on dynamic R_{dson} improvement can be observed compared to standard 2-level gate during the tests, especially under high drain-source voltage and high temperature. Moreover, the efficiency test on both buck converter and totem-pole PFC platform further verifies the feasibility and superiority of MVO-GD since efficiency boost can be observed from the experimental result. With higher switching frequency and higher power, the efficiency gap is getting larger and larger. The experimental results show that the efficiency improvement is as large as 0.13% on buck converter while 0.20% on PFC platform. In conclusion, the proposed MVO-GD strategy shows great effectiveness on dynamic on-resistance restriction and remarkable efficiency improvement in high-

power and high-efficiency applications.

3.8 Acknowledgement

Chapter 4

CONCLUSIONS AND FUTURE WORK

In modern industries, requirements for the performance of various power electronic based converters are becoming stricter in terms of capacity, voltage level, efficiency, and size (switching frequency related issues). In order to enhance the performance of existing power converters, replacing conventional Si switching devices with wide-bandgap (WBG) switching devices such as gallium nitride (GaN) high electron mobility transistors (HEMTs) and silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) is currently a popularly adopted method.

Chapter 2 presents a comprehensive description of Modular Multilevel Converters (MMs) including the classical topology and general control strategies. The high Submodule (SM) capacitor voltage fluctuation under low system operating frequency is discussed. Some novel topologies aimed at solving this problem are introduced and described in detail, which are also validated using PLECS. Moreover, the hardware development of a traditional MMC platform and a 6 kW newly proposed MIMC platform are also presented.

Chapter 3 investigates the state-of-the-art discrete GIT GaN HEMTs fabricated by Infineon Technologies. Gallium Nitride high-electron-mobility transistors (GaN-HEMTs) have been widely investigated in high-frequency and high-efficiency applications in the voltage range up to 600 V due to its excellent characteristics featured from lateral transistor structure, such as very low gate and output charge, fast switching and no body diode or reverse recovery charge. However, GaN-HEMTs suffer from trapping effects induced by high drain source voltage bias, which results in abnormal

dynamic on-resistance increasement. Unlike traditional methods from the perspective of transistor structure, this report proposes a novel multi-level Voltage Output gate drive circuit (MVO-GD) aimed at alleviating the dynamic on-resistance issue from engineering point of view. The comparative tests between proposed MVO-GD and the standard 2-level gate driver (STD-GD) are conducted under variable test conditions which may affect dynamic on-resistance, such as drain-source voltage, gate current width, device package temperature and so on. The experimental waveforms and data have been demonstrated. The on-resistance can be improved as much as 15% - 20%. Moreover, the new gate drive strategy has also been verified through efficiency tests on 2 kW buck converter and 2.5 kW PFC Platform. The results show that the efficiency improvement is as large as 0.13% on buck converter while 0.2% on PFC platform.

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