MOCVD Based *In-Situ* Etching of β-Ga$_2$O$_3$ using Triethylgallium (TEGa)

by

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ABSTRACT

Over the past decade, gallium oxide has drawn significant attention from the research community due to its exceptional properties. With a high theoretical breakdown field of 8MV/cm, a wide band gap of 4.7eV, and an impressive Baliga's figure of merit (BFOM) that is 3444 times that of Si, gallium oxide demonstrates great promise for application in high-frequency and high efficiency power electronics. Moreover, gallium oxide stands out as the preferred ultra-wide bandgap semiconductor for power device manufacturing, thanks to the availability of bulk substrates through cost-effective melt growth techniques and high-quality epitaxial layers with low defect density. This paves the way for the commercialization of Ga_2O_3 based power electronics, positioning it to compete against established SiC and GaN technologies [4], particularly in the multi kilo-volt class medium and high voltage device segment.

This thesis presents the investigation of a novel *in-situ* etching technique for β- which can be carried out within a Metal Organic Chemical Vapor Deposition reactor (MOCVD) using triethylgallium (TEGa) as the etching agent. The experiments were performed in an Agnitron Agilis 100 oxide MOCVD reactor and the TEGa is fed via the showerhead along with nitrogen carrier gas. Due to higher chamber temperature, TEGa undergoes pyrolysis leading to formation of Ga and hydrocarbon species. Hydrocarbons are subsequently removed through the exhaust and Ga adatoms deposit on the sample surface and react with the gallium oxide resulting in formation of volatile gallium suboxide (Ga_2O). Since the substrate is kept at high temperature, the suboxide desorbs from surface resulting in etching. Impact of MOCVD chamber parameters like chamber pressure, TEGa flow rate and substrate temperature on etch characteristics like etch rate and surface

morphology is studied in detail and a kinetic model for etch rate is developed. Wide range of etch rates from 0.3 µm/hr to 8.5µm/hr is demonstrated by controlling the TEGa molar flow rate. Smooth surface morphology on the etched surface is also demonstrated on (010) and (001) β-Ga_2O_3 substrate orientations. Furthermore, patterned etching of β-Ga_2O_3 is also studied with vertical and smooth sidewalls demonstrated along few in plane directions. To conclude, a precise control etching technique is demonstrated based on MOCVD using TEGa as etchant.

DEDICATION

I want to dedicate this to my family and friends.

ACKNOWLEDGMENTS

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CHAPTER 1

INTRODUCTION TO GALLIUM OXIDE

Gallium oxide is an ultra-wide bandgap semiconductor with several polymorphs, of which monoclinic β-phase is the most stable and widely studied in the entire gallium oxide family. Researchers have been studying β-phase gallium oxide material system since late 1960s as a potential optical material. Geller was the first person to study the crystal structure of monoclinic β-phase gallium oxide using three-dimensional X-ray diffraction data from a single crystal Ga_2O_3 [1]. Since then, the compound has undergone several reinvestigations, refining the earlier findings from the Geller study. However, beginning 21st century, researchers around the world are starting to see the true potential of Gallium oxide technology with first demonstration of single crystal (010) $β-Ga_2O_3$ field effect transistor by National Institute of Information and Communications, a premier research institute in Japan [2]. Subsequently, gallium oxide has seen an exponential rise in interest for applications in future high-power electronics and high-power RF devices.
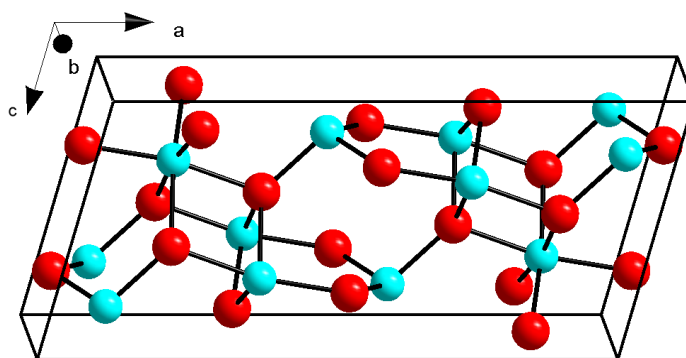
Figure 1.1: Monoclinic $β-Ga_2O_3$ Unit cell. Each unit cell has four Ga_2O_3 molecules and each Ga atom is crystallographically distinct.

After first demonstration of metal semiconductor field effect transistor (MESFET) on β-Ga$_2$O$_3$ [2] , the ultra-wide bandgap semiconductor has undergone rapid maturation in the past decade. Owing to its favorable intrinsic material properties namely critical electric field strength, tunable n-type doping, mobility, and melt grown substrates. Because of this, researchers started exploring gallium oxide for usage in power electronics, where high performance is expected at minimal cost. Moreover, among all the materials properties of gallium oxide, the most important which sets gallium oxide apart from rest of other wide bandgap semiconductors, is its ability to produce single crystal high quality melt grown β-Ga$_2$O$_3$ substrates at low cost. Due to this the semiconductor has seen tremendous growth in a very short period, leading its way for commercialization in future [3]. Availability of high-quality single crystal scalable substrates at lost cost has also enabled large scale integration on gallium oxide, leading to circuit and application-level demonstrations [4].
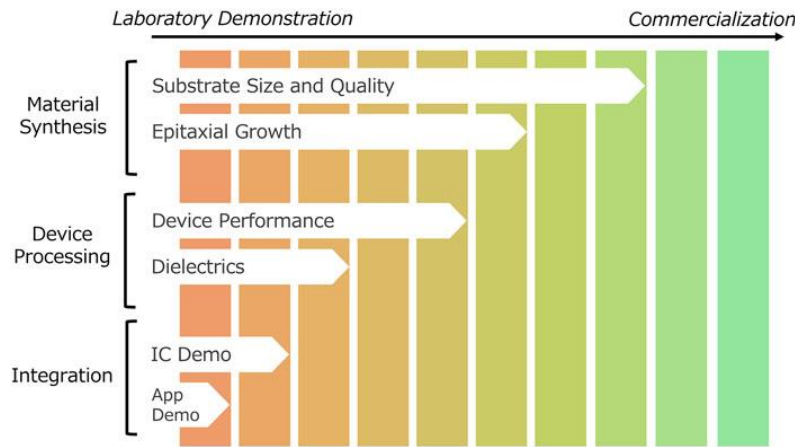
Figure 1.2 shows the progress of individual sectors as of 2021 supporting gallium oxide technology for near future commercialization for high power electronics [3].

1.1: BULK GROWTH TECHNOLOGY

Gallium oxide is the only wide bandgap semiconductor capable of crystallization and eventually producing substrates using melt growth techniques like Czocharlski (CZ), Edge-Defined Film-fed growth (EFG) and Float Zoan (FZ) while most other wider bandgap semiconductors rely on vapor transport processes for crystallization. This unique advantage of melt based bulk growth of β-Ga_2O_3 offers good manufacturability, cost, and scalability and eventually lowers the cost of making power electronic devices. Right now, high quality native substrates of β-Ga_2O_3 with different orientations and doping are commercially available in varying sizes between 25x25 mm^2 and 100mm. 150mm (-201) oriented β-Ga_2O_3 crystal has been shown through Edge Defined Film fed Growth (EDG) by The Leibniz Institute [5]. Their research further found that to scale the gallium oxide crystal diameter the O_2 concentration must be higher in the growth chamber. Nevertheless, despite the growth advantages that gallium oxide holds over other wider bandgap semiconductors, there remain several key challenges impeding manufacturing and scalability [5]. The existence of (100) and (001) cleavage planes complicate the fabrication and polishing of boules. These cleavage planes are susceptible to mechanical stresses during polishing, often resulting in cracks during fabrication. In conclusion, the potential availability of large diameter, high-quality single crystals at a low cost, combined with the intrinsic material properties of gallium oxide, positions it as a promising candidate for the next generation of semiconductor material.

CZOCHRALSKI (CZ)

The Czochralski method is the widely used technique in the semiconductor industry for producing large-diameter single crystal boules [3]. For example, silicon, germanium, sapphire, and gallium arsenide are among the common semiconductors manufactured using this method, owing to its key attributes such as scalability, manufacturability, and cost-effectiveness. In this technique, high purity gallium oxide powder is used as a starting point. The powder is then melted to form molten Ga_2O_3 melt in a crucible suitable for this high temperature growth conditions. Typically, iridium crucible is used for this purpose. Furthermore, gallium oxide seed crystal is dipped in the molten Ga_2O_3 melt and slowly pulled out at a controlled rate while rotating the crucible. Because of this it attains the boules shape and seed crystal orientation. After allowing the boule to cool down, the gallium oxide single crystal is annealed to further improve the uniformity and release internal stresses.
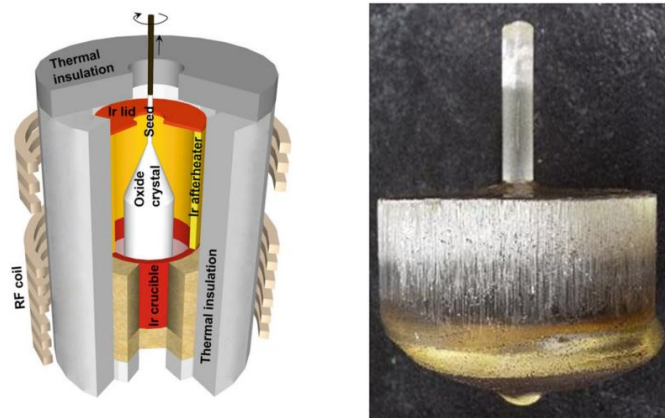
Figure 1.3 shows Czochralski (CZ) growth process schematic and the 50mm Fe doped (010) β-Ga_2O_3 boule grown through CZ growth process [3].

EDGE DEFINED FILM FED GROWTH (EFG)

Edge Defined Film Fed Growth (EFG) was initially developed for the growth of sapphire ribbons, and it is still the technique of choice for the growth of Al_2O_3 substrate. Like Czochralski method, β-Ga_2O_3 powder precursor is taken in iridium (Ir) crucible and (SnO_2) or (SiO_2) impurities were added simultaneously to the crucible to dope the crystal intentionally. Figure 1.4 illustrates the working schematic of Edge Defined Film Fed Growth process. The growth pressure is set to atmospheric pressure and growth atmosphere is usually mixture of 98% nitrogen and 2% oxygen. Radiofrequency (RF) source is used to heat up the crucible up to melting point of β-Ga_2O_3 , 1800℃. After reaching the melting point of β-Ga_2O_3 the melt is moved up the slit, like shown in fig 1.4, in the iridium die. The initiation of crystal growth is done by introducing the seed crystal in contact with the melt, leading to the formation of β-Ga_2O_3 single crystal ribbon shown in fig 1.4. This technique mitigates the issues like high thermal stresses induced during growth of boules in Czochralski (CZ) method.
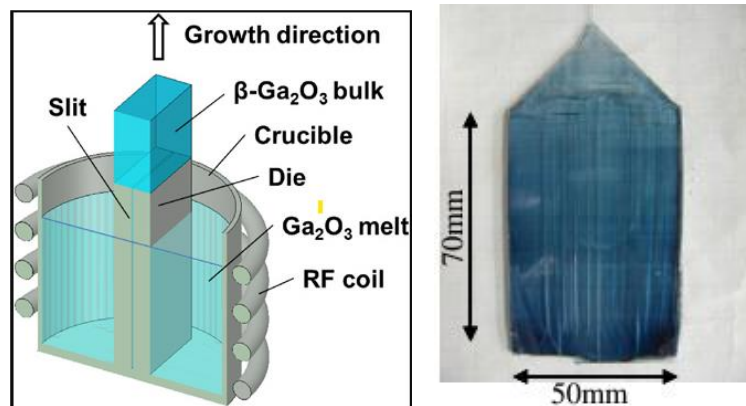
Figure 1.4 schematic diagram shows the growth of β-Ga_2O_3 through Edge Defined Fim Fed Growth (EFG) Process and a single crystal grown through EFG process [3].

FLOAT ZONE (FZ)

Floating Zone (FZ) method is another type of melt growth technique, which is suitable for growing high quality single crystal β-Ga_2O_3. In this technique, no crucible is used for the growth of crystals, leading to high quality gallium oxide crystals. Figure 1.5 shows the basic schematic of floating zone technique for growing β-Ga_2O_3 using lump heating. Sintered gallium oxide is used as the initial source. The source is heated by lump and is melted simultaneously. To start the crystal growth of gallium oxide a seed crystal is used. The melted source is held by surface tension of the molten β-Ga_2O_3. To further proceed the growth of crystal, source and crystal are set in motion in opposite directions, leading to formation of crystalline gallium oxide shown in figure 1.5. The following chamber conditions are used for the growth of β-Ga_2O_3 crystals: 20% N_2 and 80% O_2. Excess O_2 also leads to formation of voids in the gallium oxide. Studies have found that higher oxygen concentrations used in float zone technique for growth have shown lower resistivity substrates compared to CZ and EFG method. This may be due to the presence of oxygen impurities.
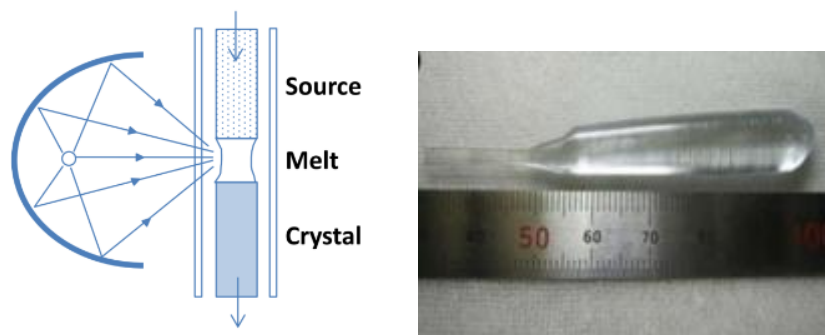
Fig 1.5 schematic diagram shows the growth of β-Ga_2O_3 through Float Zone (F)Z Process and an undoped single crystal grown through FZ process [3].

1.2: EPITAXIAL GROWTH & DOPING of β-Ga$_2$O$_3$

β-Ga$_2$O$_3$ has a possibility of growing homoepitaxy on its native substrates in all orientations [6]. While it is theoretically possible to grow GaN on its native substrates, the stringent conditions required for homoepitaxy of GaN, along with the cost and complexity associated with this process, leave GaN with no choice but to undergo heteroepitaxy on silicon substrates. This gives gallium oxide an advantage in areas where there is a requirement of crystalline, strain and/or defect free interface for better mobility and improved overall performance in power device applications. Moreover, simplistic nature of homoepitaxy, usually β-Ga$_2$O$_3$ epi layers are grown using Molecular Beam Epitaxy (MBE) or Metal Organic Vapor Phase Epitaxy (MOVPE/MOCVD) [10]-[11], or Halide Vapor Phase Epitaxy (HVPE) [7] chambers and are discussed further below, provides better compatibility with the existing processes, and leads to lower cost of producing gallium oxide epi layers. Furthermore, undoped epi layers are shown to be insulating and n-type doped with Sn and Si demonstrated doping concentration controllability up to 10^{20} cm^{-3}. Epitaxial techniques also have distinct applications in device applications. Typically, MBE is used for lateral power devices which require flat epi for current to flow along the substrate. And MOCVD or HVPE technique is used due to their high growth rates for vertical power devices which require thick epi for device fabrication.

MOLECULAR BEAM EPITAXY (MBE)

Growth rates in Molecular Beam Epitaxy (MBE) are low compared to other epitaxial techniques of β-Ga_2O_3 [8]. This is primarily due to formation of suboxide as intermediate product and slow desorption of volatile Ga_2O from surface. Typically, MBE growth of β-Ga_2O_3 starts with the evaporation of Ga from Ga effusion cell. Then the vaporized Ga reacts with highly reactive O_2, typically supplied through ozone or plasma, on the heated substrate of gallium oxide at high vacuum conditions. This results in the formation of suboxide (Ga_2O) on the sample. Like studied in chemical kinetics, this is the rate determining step of the reaction and determines the growth rate β-Ga_2O_3 epi. Eventually further oxidation of suboxide leads to the formation of gallium oxide epi. The rate of suboxide formation is slow, and additionally, temperature-driven desorption of suboxide ($Ga2O$) restricts overall growth in MBE. Typical growth rate that can achieved with MBE are 3nm/min for (010) oriented β-Ga_2O_3 at 750ºC and 0.17nm/min for (100) at 750ºC [9].

MBE Growth Mechanism:

$$Ga_{(g)} + O_{2\ (Ozone/Plasma)} \rightarrow Ga_2O$$

$$Ga_2O + O_2 \rightarrow Ga_2O_{3(s)}$$
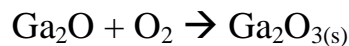
Higher growth rates are possible with MBE as well with direct supply of catalyst vapor and consequently exchange of catalyst metal ion by Ga. Researcher have coined a term for this reaction called Metal Oxide Catalyzed Epitaxy (MOCATAXY). By introducing this oxide catalyst, growth has been shown to improve the growth rate of gallium oxide epi when compared to conventional MBE. Moreover, growth rate can also be further boosted

by directly introducing suboxide (Ga$_2$O) instead of Ga. This minimizes the suboxide formation step and augmenting the growth rate to exceed 25nm/min for (010)-oriented samples. In earlier case, growth rate for (010) has increased to 5nm/min and for (001) oriented sample it increased to 1.5nm/min at 950ºC [10].

DOPING and DEFECTS

For power devices, especially for vertical devices like diodes and FETs, require uniform and accurate doping concentrations across the epi layer because these devices operate at higher voltages and frequencies compared to conventional CMOS. Changes in the doping lead to peak field crowding at non uniform regions of epi which might lead to unintentional device breakdown during operation. Donor doping of MBE grown gallium oxide epis have been demonstrated with different n type donors namely Sn, Ge, and Si. However, the real-world manufacturability is only limited to native substrates grown through Czochralski (CZ) and Edge Defined Film Fed Growth (EFG) techniques [11]. Other bulk growth technologies like Float Zone (FZ) and Vertical Bridgeman (VB) come with challenges to grow manufacturable epis with considerable doping. MBE doping of β-Ga$_2$O$_3$ with Sn or SnO offers wide range of doping possibilities with different electron concentrations. But due to larger activations energy requirement, mobilities are consistently low in comparison to other n type donor atoms. Ge is also another suitable n-type dopant of β-Ga$_2$O$_3$. This solves the issue of low electron mobility compared to earlier cases [12]. However, the strong dependency on MBE growth conditions limits the controllability of electron concentrations across the epi, results in drastic variation of electron concentration. Of all the suitable n-type dopants, Si is the best electronically suitable donor for β-Ga$_2$O$_3$.

MOCVD grown gallium oxide epis with Si doping demonstrated highest hall electron mobility of ~200 cm^2/VS [10].

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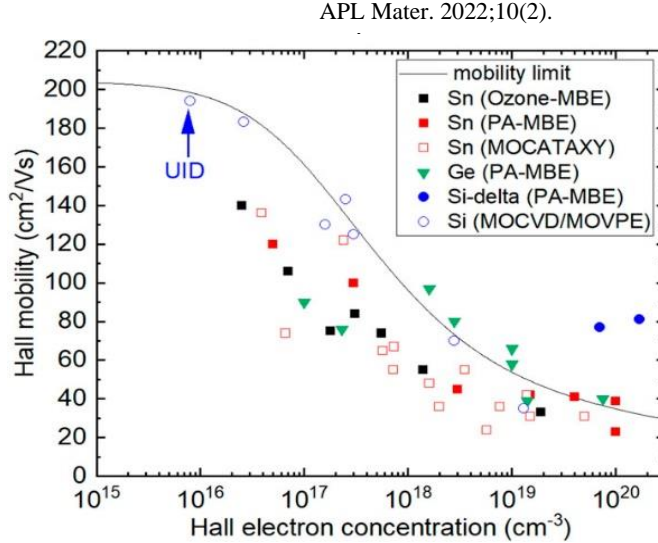
Figure 1.6 shows the electron mobility (cm^2/Vs) against electron concentration (cm^{-3}) of MBE grown β-Ga$_2$O$_3$ thin films. With Si doped MOCVD grown thin film has the highest electron mobility at 10^{16} (cm^{-3}) electron concentration [13].

Even with homoepitaxy on β-Ga$_2$O$_3$, interface is neither ideal, nor defect free due to its low symmetric monoclinic structure of gallium oxide. Twin boundary formation is unavoidable in this case. Although this issue is impending, only (100) and (-201) orientated substrates are affected primarily [3]. Twin boundaries would be detrimental to electrical properties as they can trap electrons, leading to decreased electron mobility. In addition to extended defects like twin boundary, surface and interface defects are inevitable irrespective of epitaxy technique used to grow the epi or thin film. This is primarily due to island coalescence and facet formation. Finally, MBE homoepitaxial growth of β-Ga$_2$O$_3$ is

promising due to its ability to grow high crystalline thin films with low interface states. Moreover, the simple chemistry involved during growth, like directly introducing vapor phase Ga into reaction chamber, helps to minimize the byproducts and utilize this technique in exploring new dopant elements. Furter, MBE is useful especially in cases where there is need to form heterostructures to benefit the formation of two-dimensional electron gas (2DEG) for high electron mobility and high sheet electron density. Nonetheless, slow growth rates are still a concern for growing thick films to study vertical device architectures. In the next section, a higher growth rate technique will be discussed, and it will be more commercially effective for scaling β-Ga_2O_3 power devices in future.

MOVPE/MOCVD grown β-Ga_2O_3 thin films.

Similar to advancements in MBE homoepitaxy and doping of β-Ga_2O_3, Metal Organic Vapor Phase Epitaxy (MOVPE/MOCVD) has seen rapid progress in recent years, owing to its high growth rate (upwards of 10µm/hr.) [14] and record room temperature mobility (186 cm^2/Vs) compared to other epitaxial techniques available on gallium oxide. Moreover, MOVPE technique offers controlled n-type doping with broad spectrum of electron concentration (10^{16}-10^{20} cm^{-3}) ideal for both vertical and lateral device fabrications. Furthermore, high growth rates seen in MOVPE/MOCVD further amplifies the gallium oxide potential for industrial applications [10]. Additionally, this technique enables the growth of not only the β phase but also other polymorphic phases of gallium oxide by varying growth conditions and chamber parameters. A basic schematic of MOCVD setup is shown below.

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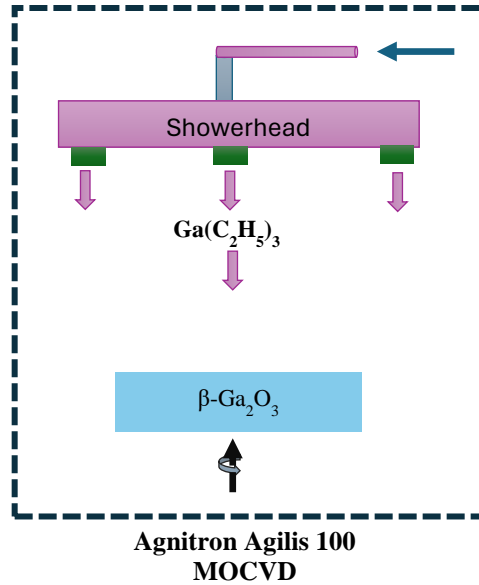
Figure 1.7 Basic Schematic of MOCVD with gallium oxide substrate loaded into the chamber and triethylgallium is flowing into the chamber through showerhead [15].

Unlike MBE, where Ga is supplied directly through Ga effusion cells, in MOVPE/MOCVD Ga is supplied through metal organic (MO) precursor. The MO precursor then undergoes pyrolysis resulting in deposition of Ga droplets on β-Ga_2O_3 surface. Hydrocarbons generated during pyrolysis will then be removed through the exhaust valve. Oxygen is either directly supplied to MOCVD or through water dissociation in the growth chamber for oxidation of Ga droplets to gallium suboxide (Ga_2O) and eventually to gallium oxide, along with Nitrogen (N_2) precursor. Epilayer formation in this case is similar to MBE except that the Ga source in MOVEP/MOCVD is supplied via Metal Organic (MO) precursor. Although the MOVPE growth mechanism is not fully studied from adatom adsorption, desorption, nucleation processes and growth propagation on

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different growth orientations point view, the following growth mechanism illustrates the basic growth proceedings in metal organic vapor phase epitaxy [14].

MOVPE/MOCVD Growth Mechanish:

$$MO\text{-}Ga_{(g)} + O_{2(g)} + N_{2(g)} \rightarrow Ga_2O$$

$$Ga_2O + O_2 \rightarrow Ga_2O_{3(s)}$$
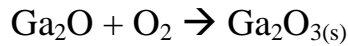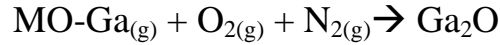
Si has shown promising results as donor in MOVPE/MOCVD grown gallium oxide epi with mobility exceeding (180 cm^2/Vs) at electron concentration of 10^{16} (cm^{-3}) [6]. However, other donors like Ge and Sn and Zr are less studied in particular to MOCVD. Moreover, the effect of carbon incorporated from metal organic precursor during MO pyrolysis still needs to be studied extensively. However, some earlier studies have shown that total electron concentration in the conductive gallium oxide thin films is not equal to total dopant concentration [13]. This illustrates that the total electron concentration is not only dependent on the dopant concentration but also depends on Carbon concentration and trap defects in the MOCVD/MOVPE grown β-Ga$_2$O$_3$. Compressive investigation is required to fully understand the carbon incorporation in the thin films. Besides that, prior investigation on distinctive behavior of Si and Sn dopants in the (010) β-Ga$_2$O$_3$ thin films has shown memory effect for the Sn doped substrates [12]. And also, same study reported incorporation issues with Sn at higher doping concentrations. However, Si doping showed reliable results leading to a wider window of doping and free electron concentration.
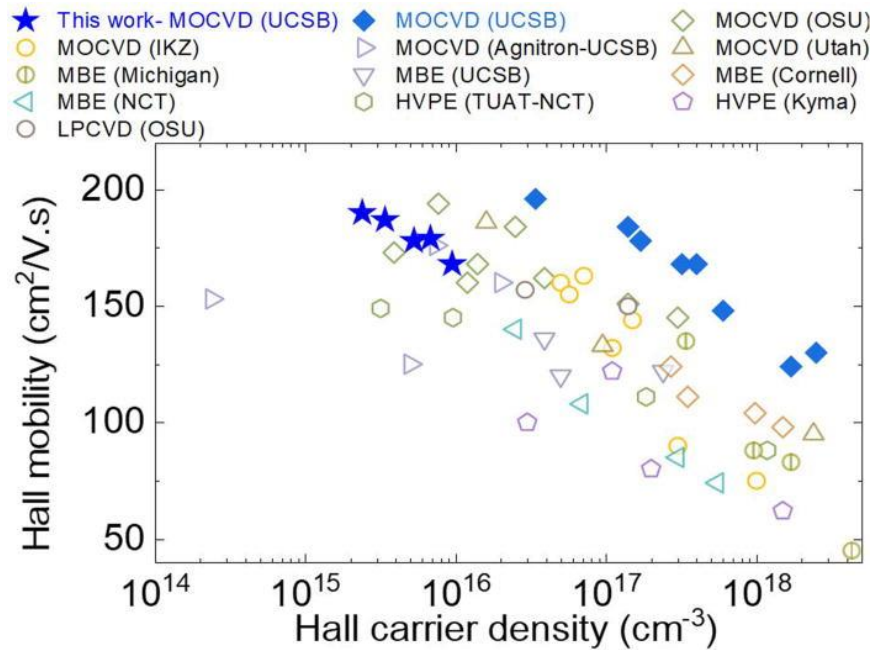
Figure 1.8 shows the electron mobility (cm^2/Vs) against hall carrier density (cm^{-3}) of MOCVD grown films [15].

1.3: HIGH VOLTAGE POWER SWITCHING

Currently most of the power semiconductor market is still dominated by Si technology which is based on diodes, Bipolar Junction Transistors (BJTs) and Insulated Gate Bipolar Transistors (IGBTs). However, SiC and GaN technologies are slowly replacing the Si in this segment due to their higher efficiency and operating frequencies. High voltage switching or high voltage blocking capabilities have long been studied on silicon and rapid advancements have been made in this realm. The invention of MOSFET architecture and low on resistance of BJT combined lead to the development of IGBTs for high voltage

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applications. However, because of its narrower bandgap and reduced tolerance for higher electric fields, researchers have begun investigating wide bandgap semiconductors for high voltage power switching.

Table 1, Power semiconductors material comparison for high voltage switching [10].

Properties	SiC	GaN	β-Ga_2O_3
E_g (eV)	3.3	3.4	4.8
E_c (MV/cm)	2.5	3.4	8
μ (cm^2/Vs)	800	1200	200
K (W/cmK)	4.2	1.5-2.5	0.1-0.2
Baliga's FOM	340	1450	3444

In addition to applications in power switching, gallium oxide, with its ultra-wide bandgap, has great potential for high efficiency power electronics, especially with applications in future generations electric vehicles and renewable energy. The parameters that decide the efficiency of the power devices are breakdown field (E_c) and on-resistance (R_{on}). Higher efficiency is achieved when the on-resistance and switching losses are low at given breakdown voltage. For all power devices, a drift region with specific doping concentration and length are required for optimal blocking of voltage on off-state. In on-state, the drift region conducts current due to presence charge carries. However, increased doping in the regions increases the on-state current, but it also reduces breakdown voltage in off-state.
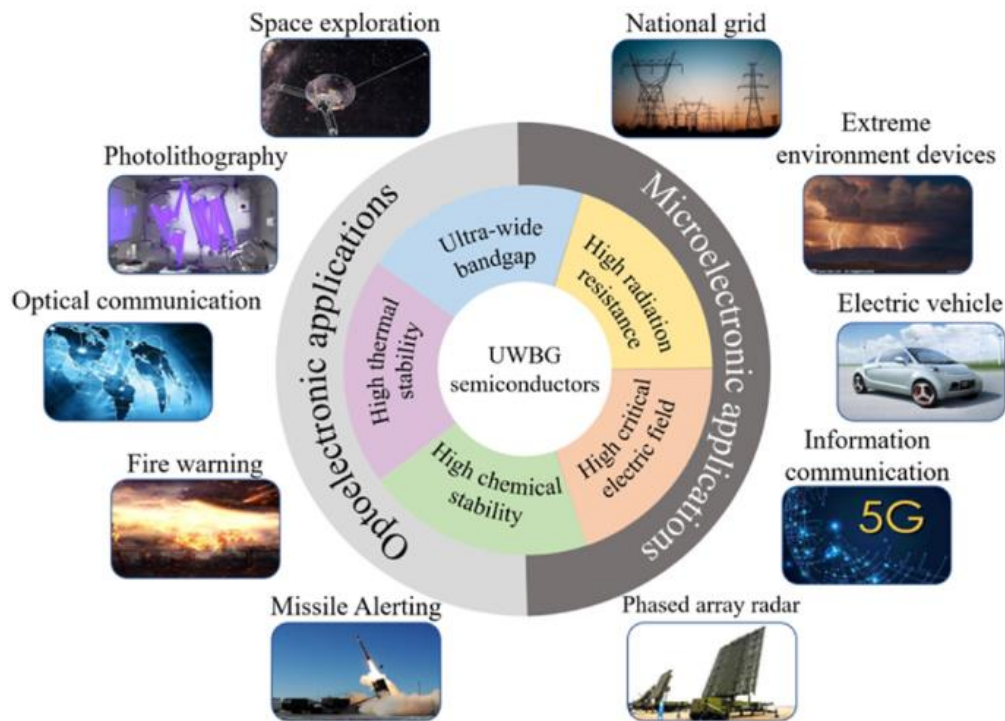
Figure 1.9 shows an overview of all the potential application of β-Ga$_2$O$_3$ in different

areas due to its high efficiency power switching [29].

1.4: VERTICAL DEVICES

In some sense, vertical device architecture is preferred for high voltage applications due to

high current densities and high voltage handling capabilities [16]. This is enabled in

vertical device architecture because of the possibility of thicker drift layers used to

distribute the current across the drift region [3]. A lot of devices that are demonstrated on

β-Ga$_2$O$_3$ so far are Schottky barrier diodes (SBDs), Fin Field Effect Transistors and Current

Aperture Vertical Electron Transistors (CAVETs) take the vertical device architecture.

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Moreover, current output for a vertical transistor with 4µm thick drift layer is higher than the lateral device with 4µm long drift layer. However, this argument does not hold true for high frequency power devices where lateral device architecture is much more suitable due to lower switching losses.
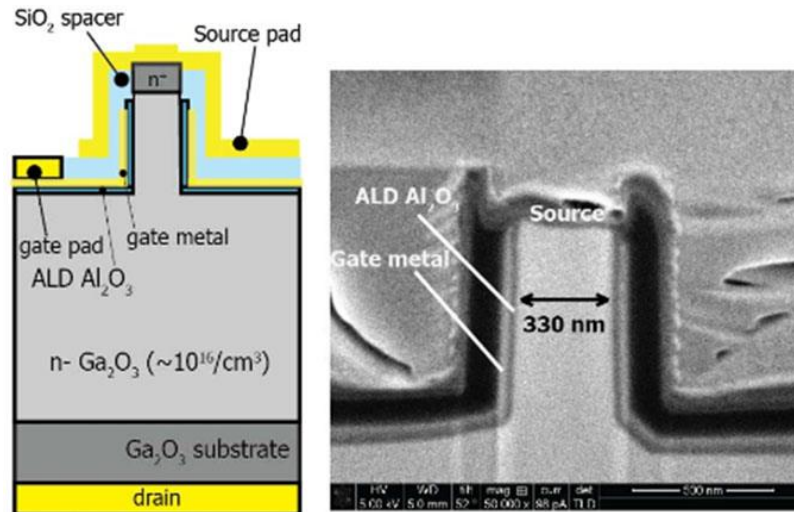
Figure 1.10 shows the both schematic and FIB cross-section image of vertical device on β-Ga$_2$O$_3$ substrate [3].

The theoretical explanation for the breakdown in the vertical devices is as follows:
Any power switching device requires a well optimized drift region that depletes under reverse bias voltage and support breakdown. Similarly same drift region conducts with an on-resistance (R_{on}=$1/Ndq\mu$) in forward bias voltage due to presence of dopant atoms (N_d). The power device that gives lowest on-resistance at a given voltage offer lower conduction losses (I^2R_{on}). Therefore to reduce the conduction losses, doping density (N_d) can be increased. However, this will increase the electrical field in the material and reduce the

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breakdown. Finally for a well optimized power switching device, ideal doping density is required for efficient functioning.
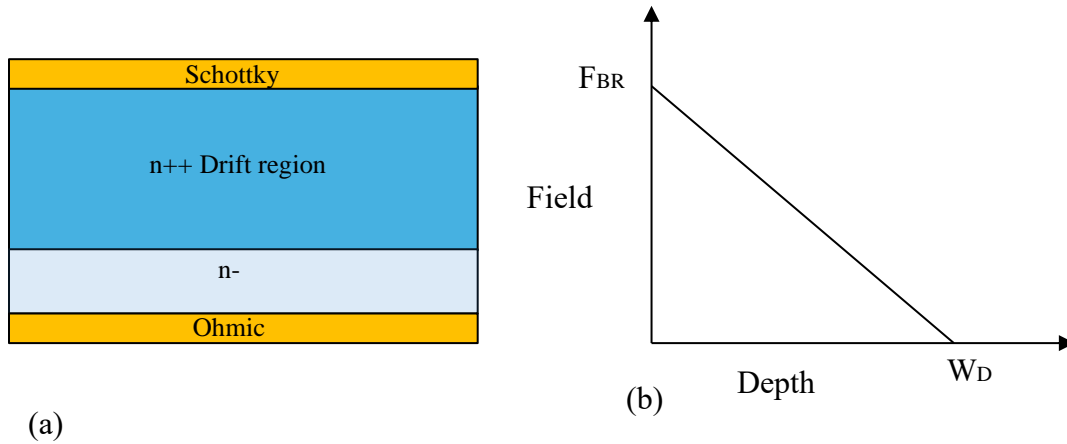
Figure 1.11 (a) 1D schematic of a vertical device with schottky contact at top and ohmic contact at back. (b) describe the field under reverse bias.

$$V_{BR} = \frac{qN_dW^2}{2\varepsilon_0\varepsilon} = \frac{F_{BR}W}{2}$$

Where ε_s is the dielectric constant of the semiconductor and ε_0 is the permitivity of free space.

1.5: LATERAL DEVICES

In contrary to vertical device topology where the primary need is to block and operate at higher voltages, lateral transistor topology is well suited for switching applications due to lower switching losses and higher gain [10]. Lateral transistors have lower capacitive footprint with lower on-resistance (R_{on}) which leads to more efficient and faster switching. Moreover, due to lower on-resistance and lower capacitive footprint charge required to switch between on and off state is minimal leading to lower energy dissipation compared to vertical topology where the presence of thick drift layer expends more energy to switch. on and off the device. As a result, lateral transistor device architecture is mostly used for RF switching, power switching and switch mode power amplifiers.
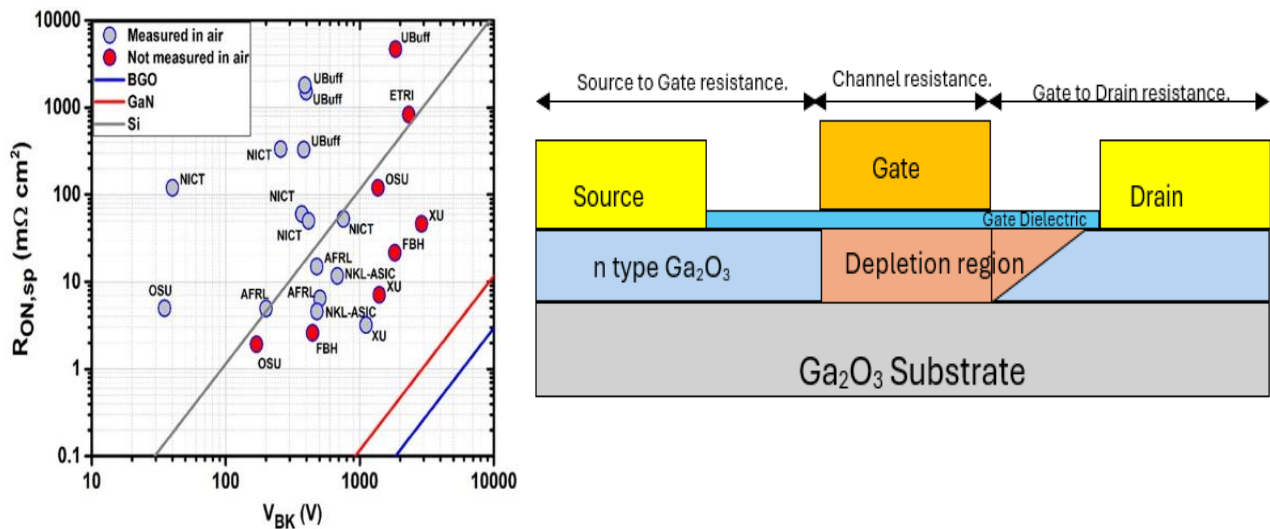
Figure 1.12 (a) On-resistance against Breakdown Voltage (V_{BR}) for laterla β-Ga$_2$O$_3$ devices . (b) a schematic of later β-Ga$_2$O$_3$ transistor [17].

The theoretical explanation for the breakdown in the lateral devices is as follows:

The 2D nature of laterl device makes the calculation of breakdown voltage (V_{BR}) complicated compared to vertial devices. This is due to depletion of charge in both X and Y directions under reverse bias.
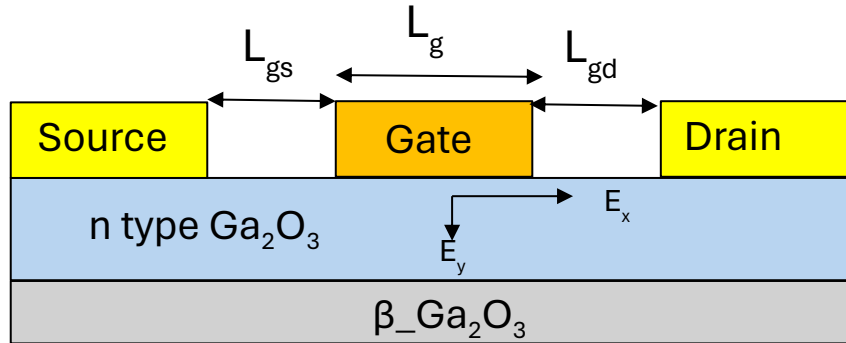
Figure 1.13 a schematic of later β-Ga₂O₃ transistor with field componets along X and Y directions.

$$E_X = E_X L_{gd}$$

Where E_X is the average electric field along X direction (Figure 1.13)

$$E_Y = \frac{qn_s}{\varepsilon_0 \varepsilon}$$

Where E_Y is the average electric field along X direction (Figure 1.13)

$$E = E_X{}^2 + E_Y{}^2$$

$$V_{BR} = L_{gd} \sqrt{E^2 - (\frac{qn_s}{\varepsilon_0 \varepsilon})^2}$$

CHAPTER 2

ETCHING TECHNIQUES ON GALLIUM OXIDE

Pattering the semiconductor is the most basic and necessary process in the device fabrication. While temporary patterning can be achieved through photolithography using either photoresist or dielectric material as a hard mask, to realize the actual pattern on the substrate requires a set of etching techniques (wet etching, dry etching etc.), either combined or used alone, to produce the desired features. These low dimensions features are the building blocks for making various device architecture to realize the true potential of semiconductors. In case of gallium oxide, which is widely praised as a next gen power semiconductor due to its attractive material properties, devices that can be implemented are UV solar blind photodetectors and various types of high voltage transistors, didoes, and RF devices [18]. However, to fabricate them we need etch processes that can effectively remove the unwanted material and form high aspect ratio three dimensional structures. Over the years, many etching approaches have been demonstrated on β-Ga_2O_3 including dry etching [19], wet etching [20], MBE based low damage etching [21] and metal-assisted chemical etching [22]. However, all these processes have listed one or more drawbacks including surface damage, inclined side walls, poor control on etch rate, irregular etch depths, and etch surface morphology reconstruction. These are non-ideal consequences for fabricating low dimensional features on different orientation of β-Ga_2O_3 substrates. Wet etching recipes like HF, H_3PO_4 (hot) and KOH (hot) are mostly used to study crystal defects on β-Ga_2O_3 because of its isotropic etching nature and induces less surface damage compared to other etching techniques [23]. In addition to studying crystal

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defects, wet etching can sometimes also be used to fabricate low-dimensional features on β-Ga$_2$O$_3$ substrates. Nonetheless, because of less control on etch rate and aggressive lateral etching resulting in inclined side walls. Therefore, it is not an effective technique to fabricate low-dimensional features with high aspect ratio. In addition to wet etching, dry etching of β-Ga$_2$O$_3$ has also been demonstrated for patterning [19]. However, because of high RF power used to generate Ar plasma and corrosive nature of chlorine gas severely damages the gallium oxide surface, resulting in performance degradation. Furthermore, metal-assisted chemical etching (Mach etch) of β-Ga$_2$O$_3$ was demonstrated in early 2000's as an effective way to etch β-Ga$_2$O$_3$ because this technique offers high aspect ratio structures when compared with other standard methods [24]. However, a stronger dependence on orientation of crystal planes and variation in oxygen dangling bonds concentration at the surface are leading to highly anisotropic etching. In addition to that, macetched β-Ga$_2$O$_3$ has also shown surface reconstruction at etched surface resulting in lower Schottky barrier height (SBH) compared to bulk crystal. Hence, it is also not a promising technique for etching β-Ga$_2$O$_3$ and fabricating high voltage power devices. More recently, MBE based low damage etching has been demonstrated using in-situ Ga reaction. In this Ga effusion cell is used to introduce Ga into the MBE chamber [9]. The vapor phase Ga reacts with gallium oxide and forms gallium suboxide. The resulting gallium suboxide desorbs from the surface at elevated temperatures resulting in etching. However, due to limitations with MBE chamber higher etch rates are difficult to achieve.

2.1: DRY ETCHING

Dry etching is one of many standard etching techniques available to make small feature sizes which are typically used in integrated chip manufacturing. The versatility of dry etching makes it a primary choice for patterning the wafers or substrates due to high etch rates, high vertical selectivity and reproducibility. In dry etching, plasma driven chemical reactions are used in vacuum load lock chambers to etch the desired material. Neutral gases are introduced as etching species in the dry etching processes. Dry etching can also sometimes be called plasma etching. The nomenclature is usually perplexing due to usage of various terms like plasma etching, reactive ion etching (RIE) [19] and high-density plasma etching (HDP). Although all etch processes refer to dry etching, each etch process has nuanced differences like using second excitation source in the plasma in HDP and increasing the ion energy in RIE [25]. Typical advantages of dry etching or plasma etching are high resolution pattern transfer (high vertical selectivity compared to lateral) and low chemical wastage compared to wet etching [19].

DRY ETCHING of β-Ga$_2$O$_3$

Etching oxides poses challenges owing to their higher chemical inertness and stronger bond strength. This difficulty extends to gallium oxide as well. Due to this, standard reactive ion etching (RIE) is not suitable for etching β-Ga$_2$O$_3$ substrates. To solve this problem, inductively coupled plasma (ICP) etching is the alternative solution owing to its high-density plasma (HDP) [25]. Moreover, ICP is widely used for etching gallium oxide because of its higher etch rates and reduced ion damage. Below table briefly summarizes the dry etching recipes on β-Ga$_2$O$_3$ and various etchant combinations which have been reported over the years due to their higher efficacy in etching gallium oxide compared to conventional chorine or fluorine based. As seen in the table below, chlorine (Cl$_2$, BCl$_3$) based ICP offers the higher etch rates in comparison to fluorine (SF$_6$,) based. Oxides like β-Ga$_2$O$_3$ typically requires ion assistance like Ar due to stronger bonds. Ion assisted chlorine-based recipes have shown the higher etch rates in the table below [19].

Table 2, Summary of various dry etch recipes on β-Ga$_2$O$_3$ with maximum etch rates [19].

Plasma Chemistry	Ga$_2$O$_3$ Samples	Plasma Source	Maximum etch rate (A^{o}min^{-1})
SF$_6$/Ar	MOCVD thin film (EPI)	ICP/2MHz	350
Cl$_2$/BCl$_3$	Bulg EFG	RIE/13.56MHz	120
BCl$_3$/Ar	Bulk (-201)	ICP/2MHz	1600
SF$_6$	Bulk EFG	RIE/13.56MHz	160
Cl$_2$/Ar, BCl$_3$AR	Bulk (-201) EFG	ICP/2MHz With different biasing	1300

DRY ETCHING CHALLENGES

Although dry etching carries many advantages like high selectivity along vertical direction and high-resolution pattern transfer, high density plasma used in ICP causes rough surfaces on gallium oxide resulting in degradation in device performance. Moreover, roughness caused due to etching also affects the inversion charge mobility in the gallium oxide electronic devices [19]. Furthermore, dry etching damages the interface quality, which is important for the high voltage performance of β-Ga_2O_3, resulting in degradation of electrical properties. For instance, Schottky barrier height (SBH) measured on an ICP etched gallium oxide substrate showed less SBH compared to unetched surfa(Khanna et al. 2019). Further, there are cases that reported ICP etched substrates showed severe drain induced barrier lowering (DIBL) due to higher interface tarps.
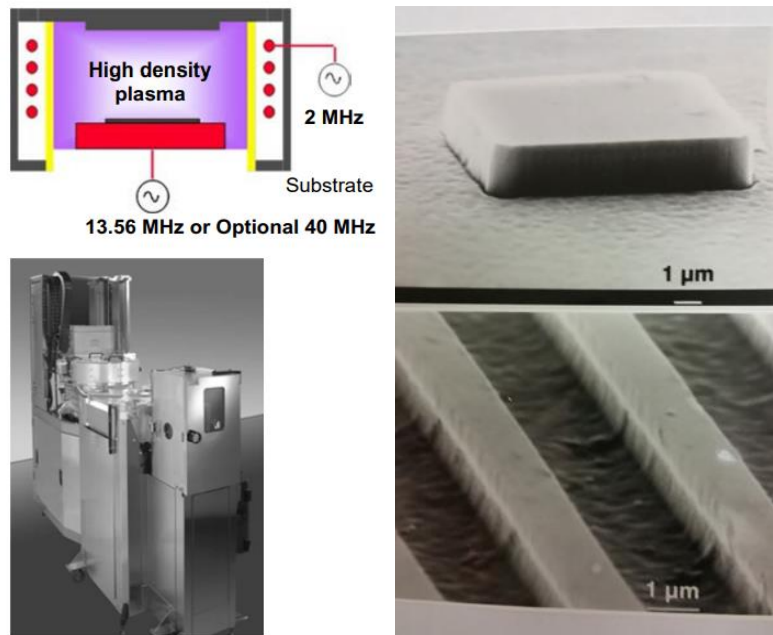
Figure 2.1 a schematic of ICP dry etching system and a actual dry etching tool. SEM images of β-Ga_2O_3 after drying etching [19].

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DRY ETCHING REMEDIES

While dry etching damages the top and side wall surfaces, there are remedies to offset the ICP induced damage. Remedies include post wet etching treatments like treating the etched surfaces with TMAH solution to smoothen the roughness caused due to dry etching. Moreover, annealing after etching showed the improvement of SBH significantly compared to unannealed substrates [18].

2.2: WET ETCHING

Similar to dry etching, wet etching of gallium oxide has also been extensively studied due to fewer etch related damage, lower cost, reasonable etch rate and high throughput. However, wet etching is limited by its isotropic nature (etching undergoes similar fashion in all directions) which limits the fabrication of high aspect ratio features. As mentioned in the chapter 1, requirement of high aspect ratio features on gallium oxide is crucial due to its potential application in high voltage power switching which requires very thick drift layer.Morever, wet etching depends on orientation of substrate which further hampers the fabrication of high aspect ratio features [22].

WET ETCHING of GALLIUM OXIDE

Plethora of chemicals have shown effective etching of gallium oxide including HF, H_3PO_4, HCl, HNO_3 and KOH [22], [23]. Table 3 summarizes the different etchants and their maximum etch rates on various gallium oxide samples. As can be seen in the table, HF etch rate on gallium oxide is very minimum compared to other chemical etchants. Due to this, it is widely used as post treatment procedure to smoothen the rough surfaces and cleanse

while fabricating devices. Moreover, H_3PO_4, when treated directly with gallium oxide tends to dissolve. Nonetheless, H_3PO_4 etches gallium oxide at elevated temperatures [20]. Furthermore, gallium oxide also dissolves in KOH solution due to formation of suspected $Ga(OH)_4$, which is soluble in base. Similar to H_3PO_4, Hot KOH can etch β-Ga_2O_3 at higher temperatures. In addition to conventional wet etching, photoelectro chemical has also been demonstrated with improved etching results due to illumination of UV light [25]. Wet etcing also results in varied Ga-O dangling bond density due to presence of two distinct crystallographic sites for Ga. As mentioned in the introduction, one gallim atom Ga (1) is present in the tetrahedral site and other gallium atom Ga (2) is present in the octahedral site.

Table 3, Summary of various wet etch recipes on β-Ga_2O_3 with maximum etch rates [20].

Etchant	Ga_2O_3 Samples	Orientation	Maximum etch rate (nm min^{-1})
HF	Grown by FZ	(100)	0.98
H_3PO_4	Fe doped Substrate	(010)	92 (160ºC)
HCl	MBE Epi	(100)	900
KOH + NaOH	EFG	(010)	2800 (490ºC)
H_3PO_4	Grown by FZ	(100)	690 (190ºC)

WET ETCHING CHALLENGES AND ADVANTAGES

Isotropic nature of wet etching is the key limitation to employ wet etching on gallium oxide, which typically requires high aspect ratio structures to realize kilo volt (KV) switching capability. Moreover, wet etching is comparatively cheap when compared to dry etching

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but due to the requirement of specialty chemical for etching, cost escalates when used in bulk quantities. Furthermore, hazardous nature of these chemicals makes it harder to safely dispose them. Among all the issues, wet etching has its merits like high throughput and offers smoother etched surfaces with RMS roughness of 0.34-0.38nm [20], [22], [23].

doi.org/10.1016/j.jallcom.2017.09.336
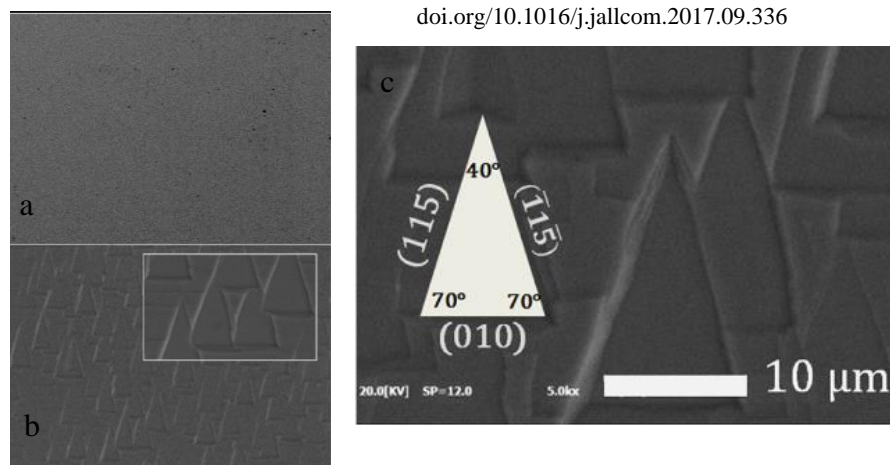
Figure 2.2 (a) and (b) shows surface morphology of PEC etching of (010) and (-201) β-Ga$_2$O$_3$. SEM images of β-Ga$_2$O$_3$ after wet etching in KOH solution with miller planes.

2.3: MAC ETCHING

Mac etch is an electrochemical etching technique that uses open circuit to etch the semiconductor and was demonstrated in early 2000s by li et al.in [25]. In this, two different half reactions takes place at different locations resulting in etching of semiconductors. Similar to dry etching, mac etching can offer high anisotropic etching (aggressive etching in one direction compared to other) and etching is only limited by the feature size of the

catalyst pattern used to the etch. In this etching process, first holes are generated by oxidant and these holes travel to the anode side and reacts with semiconductor. Reacted semiconductor forms soluble ionic form which dissolves in the acidic solution resulting in etching. Below is an example of mac etching on Si with both half reactions at cathode and anode [22].

Cathode reaction (at metal):

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+$$

$$2H^+ + 2e^- \rightarrow H_2$$
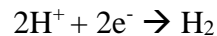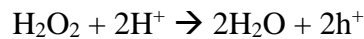
Anode reaction (at Si (semiconductor)):

$$Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6$$

Overall rection:

$$Si + H_2O_2 + 6HF \rightarrow 2H_2O + H_2SiF_6 + H_2$$
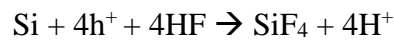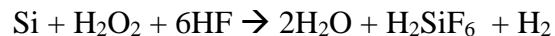
There are two types of mac etch mechanisms. One is forward mac etch, where etching takes place underneath the catalyst metal. And the other one is inverse mac etch, here etching happens where metal is   not covering resulting inverted mask patterns on the semiconductor.
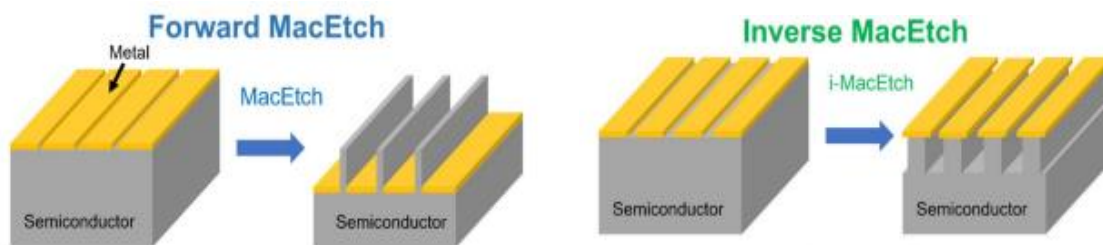
Figure 2.3 a schematic illustrating the forward and inverse macetch mechanisms [22].

MACETCHING of β-Ga$_2$O$_3$

During late 2018 and early 2019, reports began to surface regarding macetching conducted on gallium oxide for the fabrication of devices such as Schottky diodes and photodiodes [24]. Additionally, other studies have emerged, detailing the suitability of Pt as a catalyst for electrochemical etching (macetching) on gallium oxide and investigation of orientation dependence of macetching on (010) β-Ga$_2$O$_3$. Like any semiconductor, gallium oxide is etched via macetching by first immersing the samples in the Hf and K$_2$S$_2$O$_8$ with Pt catalyst patterned on it. It is found that gallium oxide proceeds through inverse macetch, where removal of material takes place in the exposed region resulting in formations of 3D structures like show in figure 2.3.The proposed mechanism for this is as follows: UV light is illuminated on to the gallium oxide substrate resulting in the generation of e$^-$ and hole pair. The electrons migrate to the Pt catalyst and hole stay at the site of generation due to poor mobility of holes in gallium oxide. This further results in etching due to oxidation of Ga$^+$ and subsequent removal of oxidized gallium oxide by HF. This only takes in the regions where gallium oxide is not covered with the Pt catalyst. Figure 2.4 illustrates the proposed macetching mechanism where electron-hole pair is generated due to UV illumination and consequently migration of electrons to Pt catalyst.
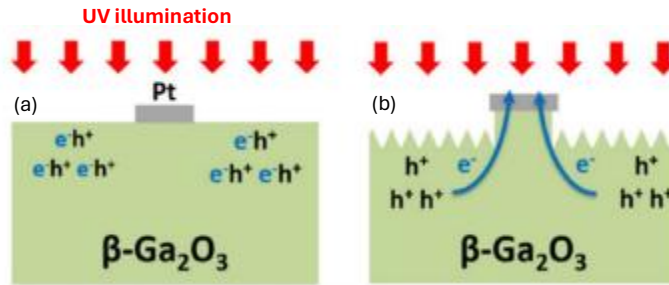
Figure 2.4 (a) and (b) show the proposed macetching mechanism on gallium oxide [22].
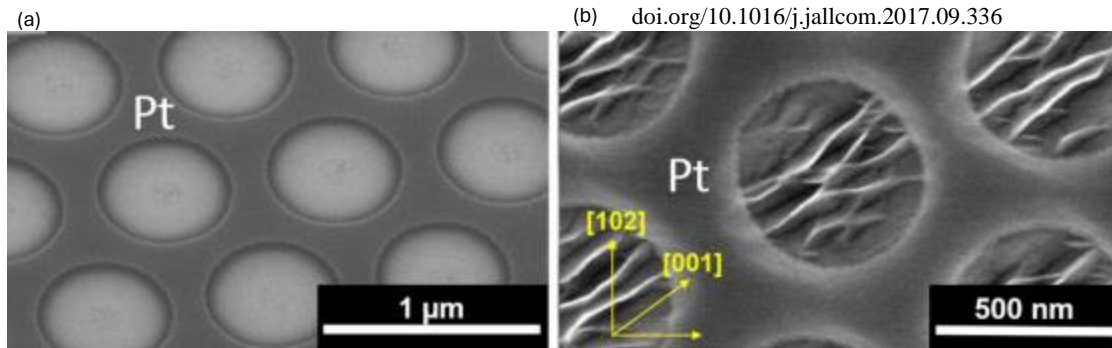
Figure 2.5 (a) and (b) show the SEM images of gallium oxide substrate. (a) is taken after UV illumination and (b) after macetching [22].

Etch rates of β-Ga$_2$O$_3$ etched through macetch depends on number of factors including carrier concentration and temperature of the oxidizing solution. Studies have shown that as doping concentration increased form $10^{17} - 10^{18}$ cm^{-3} etch rate with increase of 0.28 times. This further confirms that presence of catalyst Pt affects the macetching on gallium oxide. Moreover, other studies have also demonstrated that macetch rates were higher at elevated temperatures compared to room temperature. In addition to that, same study reported that at higher temperatures macetching demonstrated higher anisotropy I.e. vertical etching is much more significant compared to later etching.

MACETCHING CHALLENGES

While macetching appears promising as an etching technique for gallium oxide to fabricate high aspect ratio 3D structures, Schottky diodes demonstrated using macetching have shown a reduced Schottky barrier height (SBH) compared to the unetched region. However, the actual devices exhibit rectifying behavior under bias. Further, studies have been conducted to understand the reason causing lower Schottky barrier height. Both TEM and XPS characterization have concluded that gallium oxide in the macetched region has different gallium oxide morphology with reduction in the oxygen atom owing to surface reconstruction. At the etched region GaO_4 tetrahedral structure shares oxygen atoms leading to deficiency of oxygen and reduced dangling bonds [22].

2.4: MBE GALLIUM ETCHING of β-Ga$_2$O$_3$

MBE gallium etching was demonstrated by Siddharth Rajan's group at OSU on gallium oxide [9]. This etching primarily relies on the following chemical reaction: (Ga$_2$O$_3$ (s) + Ga $\rightarrow$ Ga$_2$O). By intentionally limiting the oxygen supply in the MBE chamber, Ga flux reacts with gallium oxide resulting in the formation of suboxide which further evaporates due to high substrate temperature. Sublimation of suboxide from the substrate results in in-situ MBE low damage etching of gallium oxide. Below schematic illustrates the basic working of MBE low damage etching with silicon dioxide hard mask. In this work, array of etch rates were demonstrated ranging from 3 to 30nm/min and concluded etch rate is only constrained by the supply of Ga flux. Moreover, this work also demonstrated the fabrication of high aspect ratio 3D structures [21].
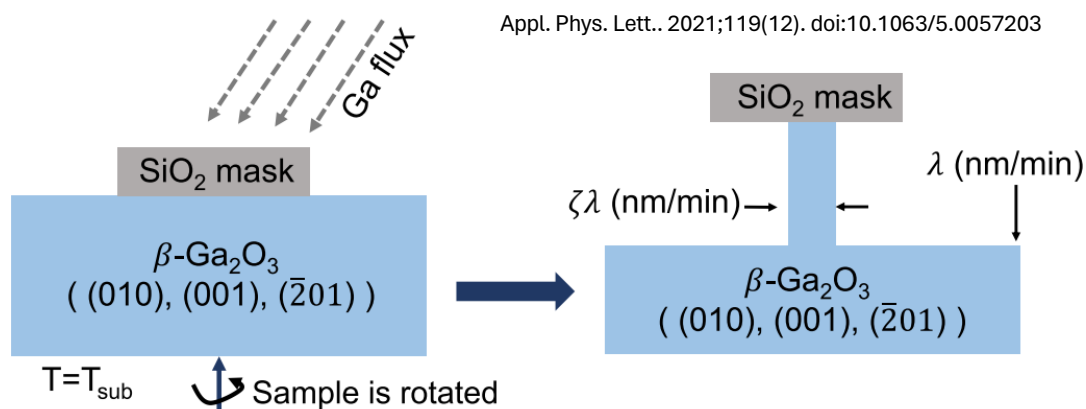
Figure 2.6 shows the schematic of MBE setup used for low damage etching of β-Ga$_2$O$_3$ with SiO$_2$ hard mask and deep etching results in reduction of fin width in lateral direction [21].

Three different HVPE grown Fe and Sn doped substrates namely (010), (001) and (-201) are used in this study. And substrate temperature has been varied from 550ºC to 800 ºC to study the effect of temperature on etch rate. However, Study concludes that there is no effect of substrate temperature on etch rate at a given Ga flux on all three samples β-Ga$_2$O$_3$ and makes this technique ideal for etching β-Ga$_2$O$_3$. This study also found that vertical side walls can be fabricated along all directions with reduction in fin width in some directions. Moreover, side walls morphology is distinct across the samples with smooth sidewalls along following planes (001), (100), (101). Apart from studying etching characteristics, this study also investigated the purity of etched surface through XPS analysis and Si segregation effect by making Schottky didoes on both etched and unetched surfaces to verify any loss of Schottky barrier height (SBH) due to etching. It was found that no loss of SBH along with near unity ideality factor and also low reverse leakage current in reverse bias, making this is a versatile technique for etching gallium oxide.
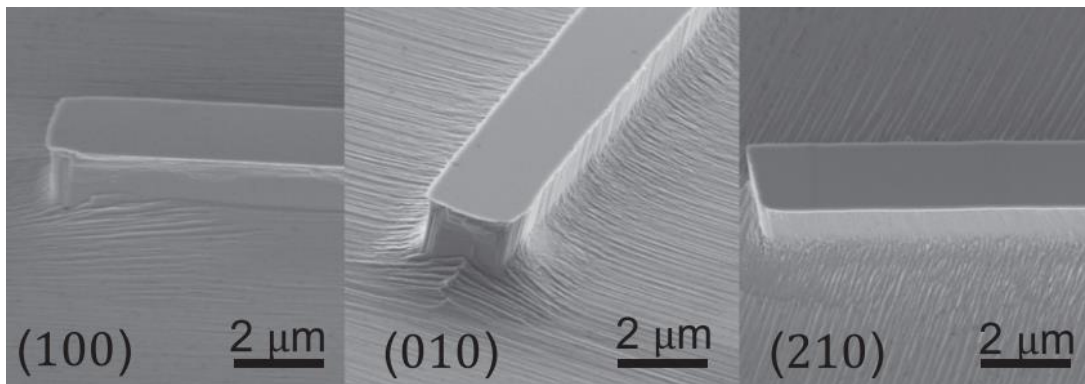
Figure 2.7 shows the tilted SEM images of fin fabricated through MBE etching. Sidewalls are smooth along few directions and rough along other directions [22].

CHAPTER 3

NOVEL MOCVD BASED IN-SITU GALLIUM ETCHING

This chapter has been adapted from reference [15]*.*

MOCVD offers the highest quality growth of gallium oxide with extremely low compensating acceptor concentrations [15]. Therefore, an in-situ etching technique that can integrated with MOCVD growth will be highly beneficial. In this work, we demonstrate that Ga etching can proceed within an MOCVD chamber by using metal organic precursors such as triethygallium (TEGa). When MO precursors such as TEGa are introduced into the chamber without oxygen, TEGa undergoes pyrolysis releasing Ga adatoms on the sample surface. At sufficiently high substrate temperatures, the deposited Ga adatoms undergo suboxide reaction with gallium oxide as explained before (Ga_2O_3 (s) + Ga $\rightarrow$ Ga_2O) [15]. This new technique is highly versatile since it can be performed in-situ within the MOCVD chamber, enabling integration of epitaxial growth and etching. This allows achieving extremely clean regrowth interfaces without exposure to vacuum. In this work, in addition to demonstrating In-situ TEGa etching, we also studied etching characteristics including etch rate and RMS surface roughness by varying triethyl gallium (TEGa) flow rate, substrate temperature (T_{sub}) and chamber pressure (P).

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3.1: EXPERIMENT PROCEDURE

The etching experiments were conducted on ($\overline{2}$ 01) oriented β-Ga$_2$O$_3$ epitaxial films pre-grown on c-plane sapphire substrates using MOCVD and bulk Fe-doped (010) and Sn-doped (001) β-Ga$_2$O$_3$ substrates. The entire study was conducted in Agnitron's Agilis 100 MOCVD reactor using TEGa as the source for Ga and nitrogen as the carrier gas. TEGa flow rate varies from 3.63 μmol/min to 140.47 μmol/min to determine its effect on etching characteristics, like etch rate and RMS roughness. Subsequently substrate temperature (T$_{sub}$) and chamber pressure were also varied from 800ºC to 1000ºC and 3-60 Torr to study its effect on etch rate.

Fig 3.1 illustrates the general mechanism of in-situ Ga etching of β-Ga$_2$O$_3$ in the Agilis 100 MOCVD reactor. TEGa is introduced through the showerhead located above the sample at a distance of 6 inches (far injection showerhead). At high enough substrate temperatures, there is uniform deposition of Ga droplets on the sample surface from pyrolysis of TEGa resulting in etching of the β-Ga$_2$O$_3$ sample. Blanket etching of the samples was carried out on β-Ga$_2$O$_3$/sapphire and β-Ga$_2$O$_3$ bulk substrates to estimate the etch rates and surface morphologies. A blue light source (λ=470 nm) fiberoptic reflectometer equipped in Agnitron's Agilis 100 MOCVD reactor was used for *in-situ* monitoring of etch rate. In addition, etch depth (thus etch rate) was also estimated by measuring the thickness of samples before and after the etching process (*ex-situ*) using a Filmetirs (F50) thin film analyzer. The presence of refractive index contrast between the β-Ga$_2$O$_3$ film and the substrate underneath is critical for the use of both the optical methods described above. As a result, ($\overline{2}$01) oriented β-Ga$_2$O$_3$/sapphire samples were used to

measure the etch rate of the films. Moreover, etch rate was also measured ex-situ using Dektak profilometer and AFM. For studying patterned etching, spoke wheel structure, as shown in figure 3.5 (a), is used to study anisotropy in lateral etch rates and sidewall morphologies.

200nm thick SiO_2 is used as hard mask during this etching study. SiO_2 is deposited at 350 ºC with 170 sccm of silane (SiH_4) and 710 sccm of Nitrous Oxide (N_2O) using Plasma Enhanced Chemical Vapor Deposition (PECVD). After that substrates were coated with AZ 3312 photoresist at 3000 RPM for lithography exposure. Coated substrates were then loaded and exposed under Heidelberg Mask Less Aligner (MLA) at 100 mJ/cm^2 dose and developed in the AZ 300 MIF developer for 60 seconds. Hard mask opening for MOCVD etching of gallium oxide is done through wet etching of SiO_2 using (1:10) buffer oxide etchant. Samples are then loaded into the MOCVD for etching. After etching is carried out, samples are treated with Hydrochloric Acid (HCL) to remove gallium droplets from the sample surface. Consequently, SiO_2 hard mask is removed by dipping the substrates into (1:10) ratio buffer oxide etchant. Finally, thin layer of 6nm Nickle (Ni) is sputtered on two different orientations of gallium oxide substrates etched in MOCVD for SEM characterization. Tilted SEM images of side walls are shown in fig 3.6 and fig 3.7.

Step 1 $(C_2H_5)_2\text{-Ga (TEGa)} \rightarrow \text{Ga} + C_XH_Y$

Step 2 $4\text{Ga (g)} + \text{Ga}_2\text{O}_3 \text{ (s)} \rightarrow 3\text{Ga}_2\text{O (g)}$ (Ga etching)

Suboxide desorbs from

Showerhead

$\text{Ga}(C_2H_5)$

Pumped C_xH

SiO_2

β-Ga$_2$O$_3$

$T=T_{sub}$
700-1000 °C

Agnitron Agilis 100 MOCVD

SiO_2

β-Ga$_2$O$_3$

Mask Removal

β-Ga$_2$O$_3$

Etched Sample
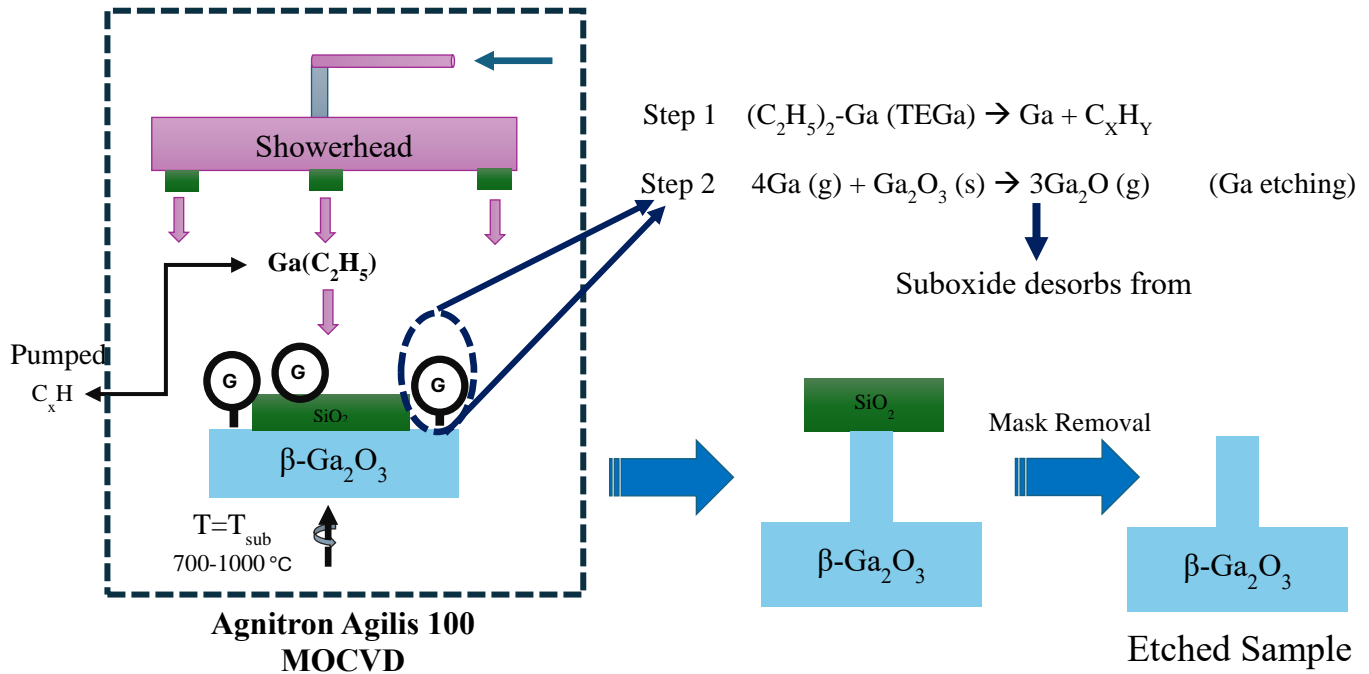
Figure 3.1 illustrates the step by step working of In-situ MOCVD etching and mechanism and additional schematics showing etch results after hard mask removal.

3.2: RESULTS AND INTERPRETATION

Etching characteristics mentioned in the earlier section like etch rate (µm/hr) and RMS roughness (nm) are plotted against MOCVD chamber parameters like TEGa flow rate (µmol/min), and substrate temperature (T_{sub} °C) in the figure 3.2. Figure 3.2 (a) shows the plot against etch rate and substrate temperature at three different molar flow rates including 15.7, 48.4 and 75.6 µmol/min and chamber pressure is kept at 15 Torr throughout all experiments. This is because highest etch rate was obtained at 15 Torr chamber pressure shown in figure 3.2 (c). With increase in substrate temperature until 900 ºC etch rate

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increased at all three molar flow rates. However, beyond 900 ℃ etch rate saturated with increase in substrate temperature. The reason for this is that at high substrate temperature like 900 ℃ and above. Etch rate is only limited by the supply of TEGa into the chamber, meaning all TEGa is converted into Ga and is instantaneously available for etching. In other words, etching is not limited by the suboxide reaction rate, instead etching depends on the supply of flow rate of TEGa at substrate temperature > 900 ℃. Figure 3.2 (b) shows the plot against etch rate and TEGa flow rate at three different substrate temperatures namely 800, 900 and 1000 ℃ with chamber pressure is again kept at constant at 15 Torr for same reason mentioned earlier. Initially etch rate increased linearly with TEGa flow rate until approximately 100 µmol/min beyond that etch rate saturated with molar flow rate of TEGa at all substrate temperatures. The reason for that is because all the supplied Ga in the form of TEGa under 100 µmol/min flow rate is converted into suboxide with no further backlog of Ga left on the gallium oxide surface to affect the incoming Ga from after pyrolysis of TEGa, resulting in linear increase until etch rate reached its threshold. However, once flow rate reaches the threshold limit, here it is 100 µmol/min, etch rate starts to saturate. This is because supply of incoming Ga exceeds the suboxide reaction rate, resulting in saturation of etch rate. At constant substrate temperature of 800 ℃, figure 3.2 (c) shows the effect of MOCVD chamber pressure (P) on etch rate at two different molar flow rates of TEGa 24.2 and 75.6 µmol/min. Maximum etch rate was obtained at chamber pressure (P) of 15 Torr. This is the optimal MOCVD chamber pressure to yield highest etch rate for the molar flow rates mentioned above. However, increase or decrease in chamber pressure from 15 Torr resulted in decrease in etch rate. While the exact reason for this phenomenon remains unclear, potential explanations may include either the

extended residence time of TEGa required to reach the gallium oxide surface under high chamber pressure conditions or the reduced concentration of Ga on the gallium oxide surface at low chamber pressure, resulting in lower etch rates outside of optimal pressure conditions. Furthermore, etch rates measured on β-Ga$_2$O$_3$/Sapphire substrates are compared to bulk substrates which were loaded simultaneously for etching. Figure 3.2 (d) shows the normalized etch rate vs TEGa molar flow rate (μmol/min) of three different types of gallium oxide substrates namely (-201) β-Ga$_2$O$_3$/Sapphire, (010) Ga$_2$O$_3$ and (001) Ga$_2$O$_3$ substrates at two different TEGa molar flow rates. SiO$_2$ hard mask is used to measure the etch depths on ex situ metrology tools. Etch depths were measured using atomic force microscope (AFM) and Dektak profilometer for simultaneous agreement. Although normalized etch rates on bulk substrates of gallium oxide are lower compared to gallium oxide on sapphire, the etch still follows the same etching trend, i.e. etch rate increases with increase in TEGa molar flow rate.
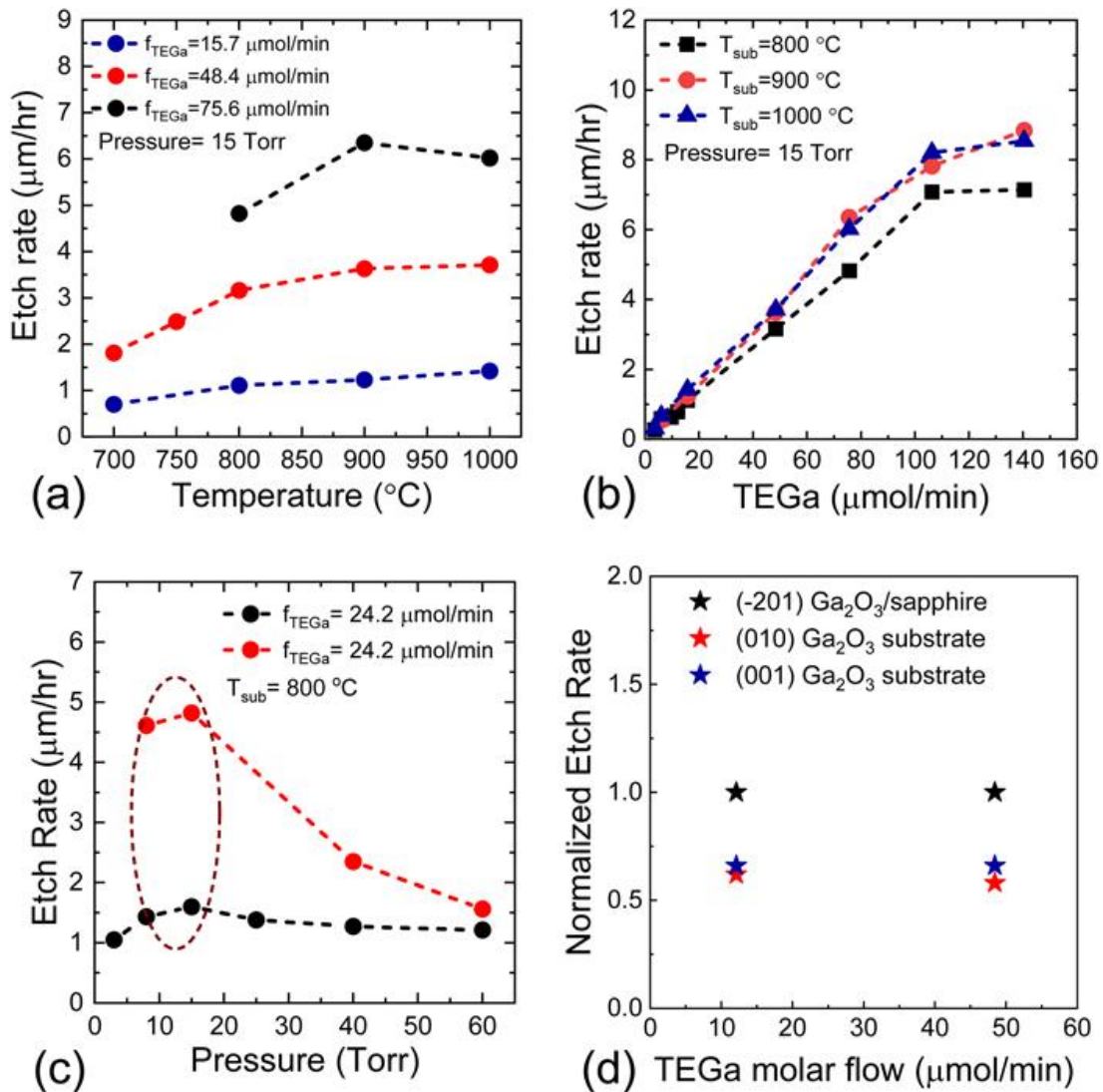
Figure 3.2 (a) Etch rate (µm/hr) vs substrate temperature (T_{sub} °C) for three different Molar flow rates with chamber pressure kept at 15 Torr. (b) Etch rate vs TEGa flow rate at three different substrate temperatures (°C) and chamber pressure kept at 15 Torr. (c) Etch rate (µm/hr) vs Chamber pressure (P) at two different Molar flow rates (µmol/min) and substrate is kept at T_{sub} = 800 °C. (d) Normalized Etch rate vs TEGa flow rate (µmol/min) on (-201) Ga_2O_3/Sapphire, (010) Ga_2O_3/Sapphire and (001) Ga_2O_3/Sapphire.

In addition to studying etching characteristics, in this study we also investigated the surface morphology of two different bulk substrates etched through this technique including Fe doped (010) β-Ga$_2$O$_3$ and Sn doped (001) β-Ga$_2$O$_3$. Figure 3.3 (a) shows the variation of RMS roughness (nm) with substrate temperature (ºC) at constant molar flow rate (f_{TEGa} = 484.3 µmol/min) and chamber pressure (P = 15 Torr). RMS roughness decreased with increase in substrate temperature on both the bulk substrates with smoothest surface was obtained on (001) β-Ga$_2$O$_3$ at substrate temperature (T_{sub} = 1000ºC) . This decrease in surface roughness due to increase in substrate temperature might be due to better diffusion of Ga adatoms across the gallium oxide sample and also faster desorption of suboxide with no backlog of Ga left on the sample resulting in smoother surfaces at elevated temperatures.

Figure 3.3 (b) shows the variation of RMS roughness on (010) β-Ga$_2$O$_3$ against TEGa molar flow rate at two different substrate temperatures, 800 and 1000 ºC, and chamber pressure is again kept at constant at P = 15 Torr. For lower substrate temperature, lower RMS roughness is obtained at lower TEGa molar flow rate. However, this trend exhibits opposite behavior as shown in figure 3.3 (b). However, at higher substrate temperature, lowest roughness is obtained at higher flow rate. AFM and SEM images of etched surfaces of both (010) and (001) β-Ga$_2$O$_3$ bulk substrates are shown in figure 3.4. Both SEM and AFM images resonate with each other with the visible elongated grooves travelling along [001] direction in (010) and [010] direction in (001) β-Ga$_2$O$_3$. Moreover, surface roughness was obtained on both the substrates with the following values, 2.8nm and 3.1 nm respectively.

Pattern etching was done in addition to the blanked etching with SiO$_2$ hard mask.

Figure 3.4 (e) and (f) show the SEM images of pattern etching with masked and etched regions. Similar elongated grooves [27] can be seen here as well. In figures 3.5 and 3.6, tilted SEM images of both bulk substrates used for patterned etching are shown. For (010) β-Ga_2O_3 [001] in plane direction was found to be smoothest compared to others, figures shown in 3.5 (c). Similarly, on (001) β-Ga_2O_3, [010] in plane direction was found to be smoothest and all other sidewalls are rough. Also, SEM image of spoke wheel structure is shown in the figure 3.5 (a) and is noticeable that all sidewalls are right angle to the gallium oxide surface.Moreover, lateral etching was also seen with lowest lateral to vertical etching is found along sidewalls with smoothest surface.
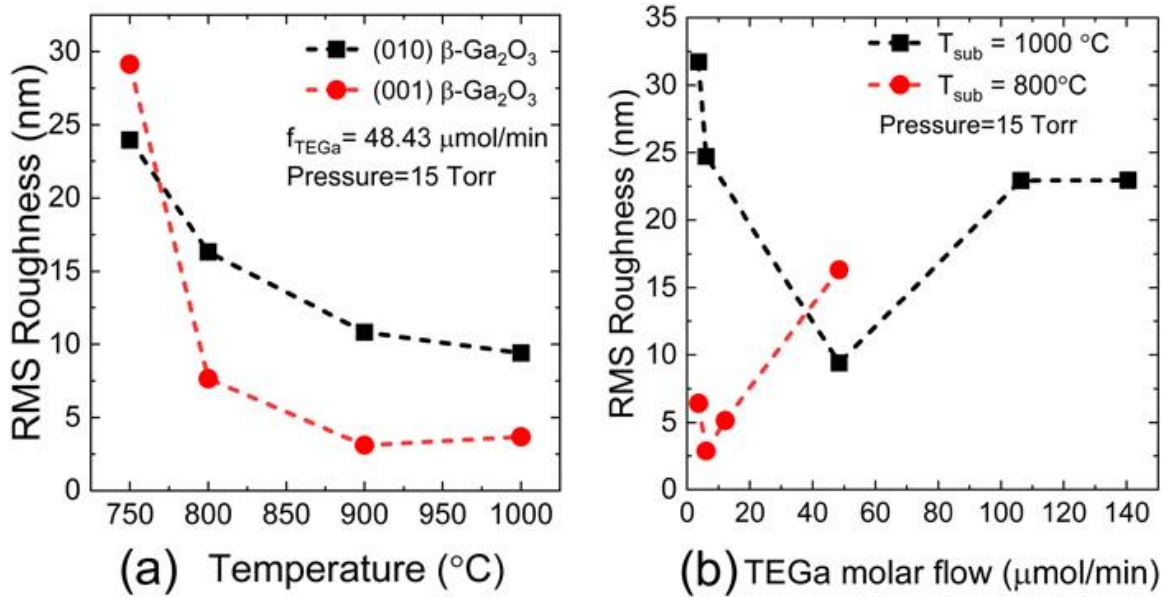

Figure 3.3 (a) RMS roughness (nm) measured on 5x5 μm^2 vs Substrate temperature (°C) of (010) and (001) β-Ga_2O_3 at chamber pressure (P = 15 Torr) and Molar flow rate (f_{TEGa} = 48.43 μmol/min) (b) RMS roughness (nm) vs TEGa molar flow rate (μmol/min) at T_{sub} = 800 and 1000 °C and Chamber pressure (P = 15 Torr) on (010) β-Ga_2O_3.
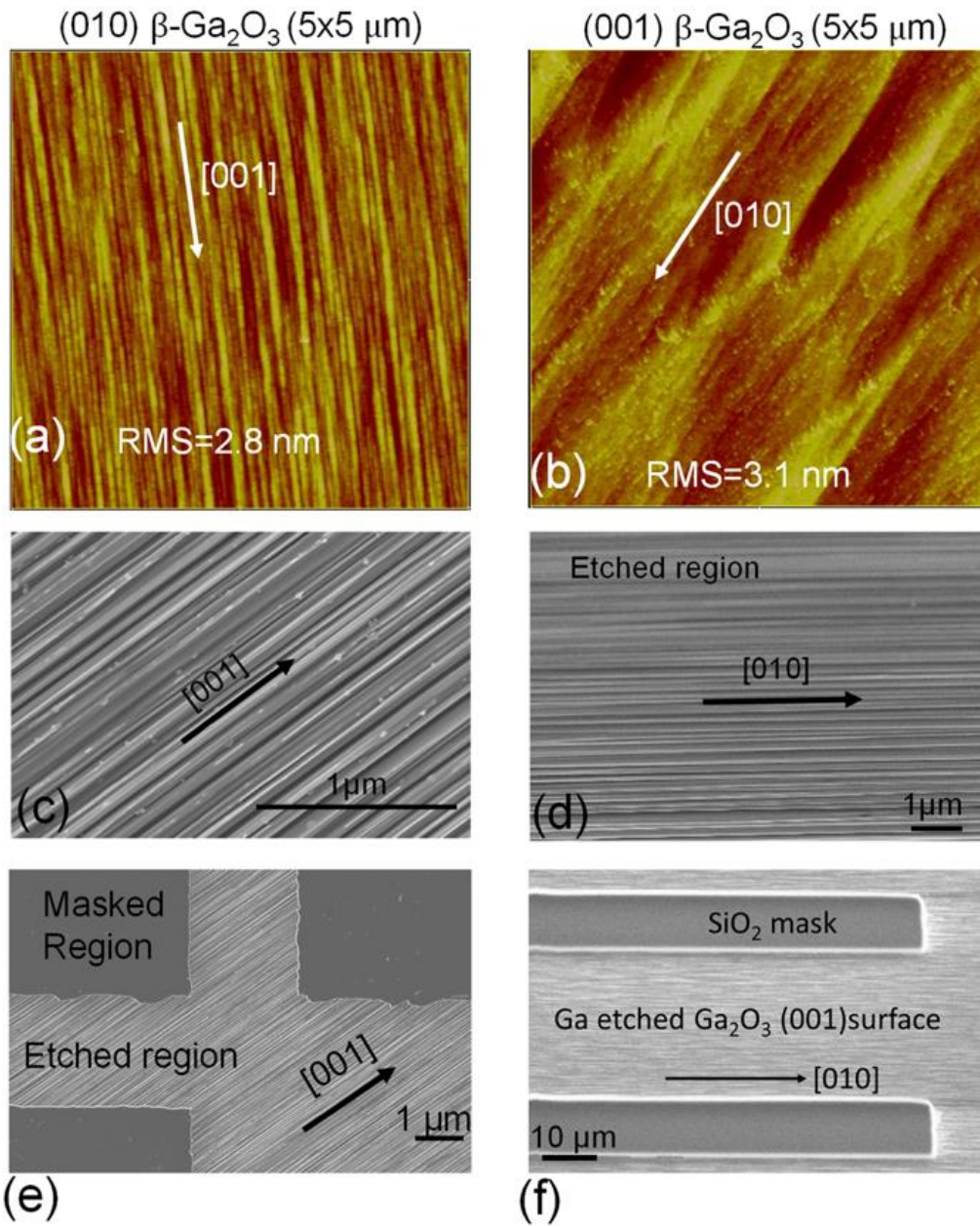
Figure 3.4 (a) and (b) show the Atomic Force Microscopy (AFM) images of MOCVD etched (5x5 μm^2) surface of (010) and (001) β-Ga₂O₃. (c) and (d) show the Scanning Electron Microscopy (SEM) images of etched surfaces with elongated grooves along [001] direction on (010) β-Ga₂O₃ and [010] direction on (001) β-Ga₂O₃. (e) shows the patterned etching on (010) β-Ga₂O₃. (f) shows patterned etching on (001) β-Ga₂O₃.
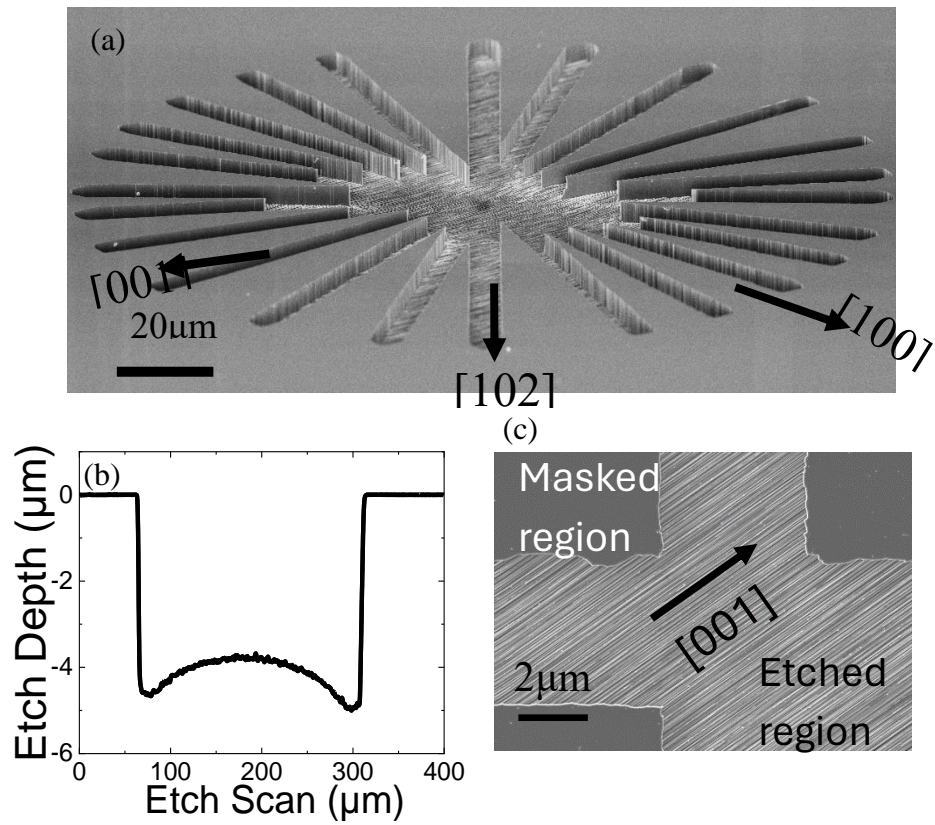
Figure 3.5 (a) shows the tilted SEM image of spoke wheel structure on (010) β-Ga$_2$O$_3$.

(b) shows the Dektak etch depth measurement vs etch scan. (c) illustrates the etched

region and masked region on (010) β-Ga$_2$O$_3$.

Figure 3.6 (a), (b), (c) and (d) show the smooth sidewalls on (010) β-Ga$_2$O$_3$ substrate.

Figure 3.7 (a), (b), (c) and (d) show the rough sidewalls on (010) β-Ga$_2$O$_3$ substrate.
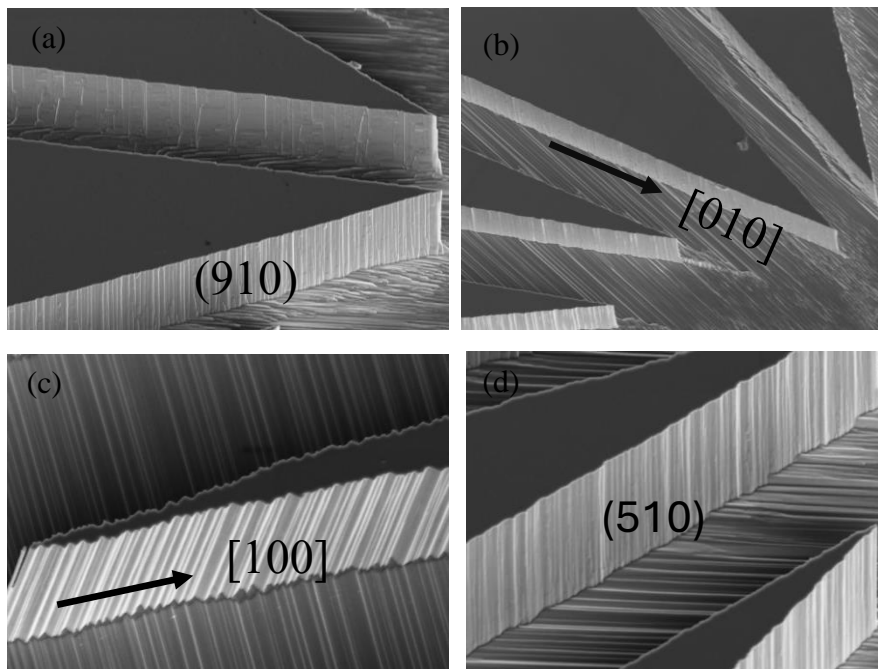
Figure 3.8 (a) and (b) show the smooth sidewalls on (001) β-Ga$_2$O$_3$ substrate. (c) and (d) show the rough sidewalls on (001) β-Ga$_2$O$_3$ substrate.

3.3: KINETIC MODEL FOR ETCH RATE

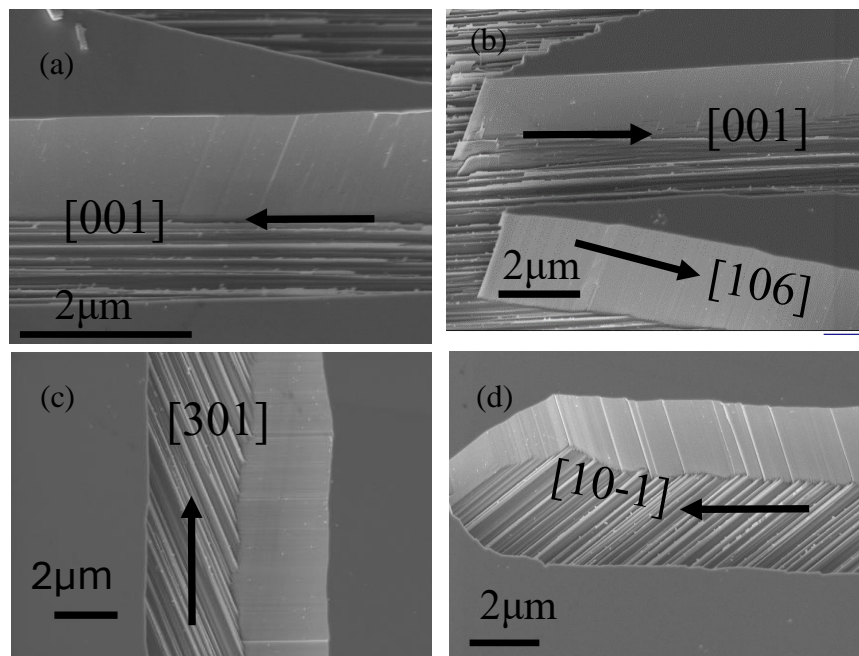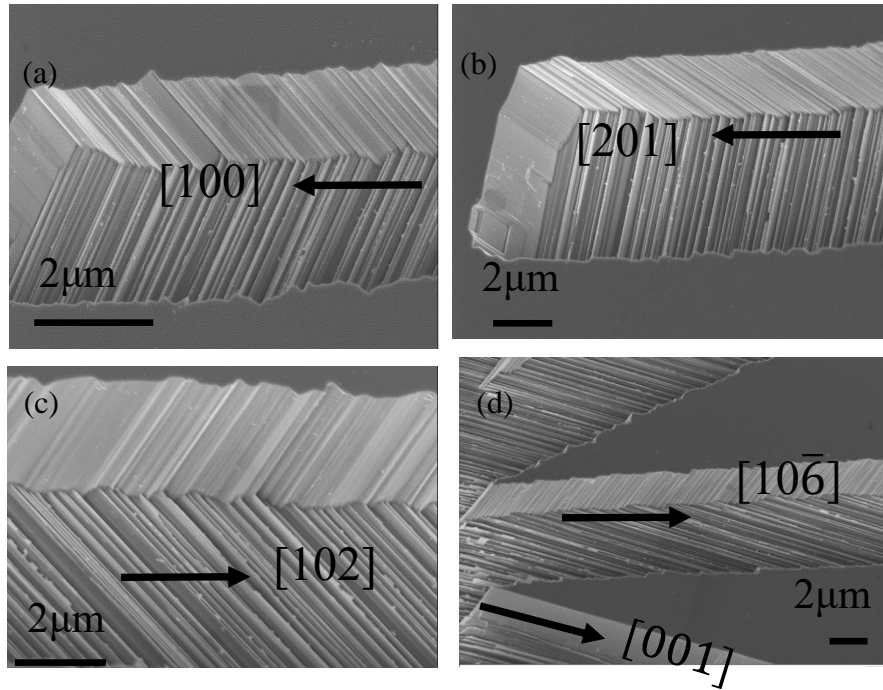A kinetic model for etch rate has been developed for this in-situ MOCVD etching technique based on the surface conservation of Ga and Ga$_2$O atoms [28]. Several assumptions were made, including the assumption that all triethylgallium (TEGa) will undergo pyrolysis at optimal chamber pressure, resulting in 1 Ga atom per TEGa molecule. Therefore, flow rate of TEGa (J_{TEGa}) is equal to flow rate of Ga (J_{Ga}) atoms on to the surface. This proposed kinetic model is studied at low Ga flux regime due to linear dependence of etch rate on TEGa flow rate.
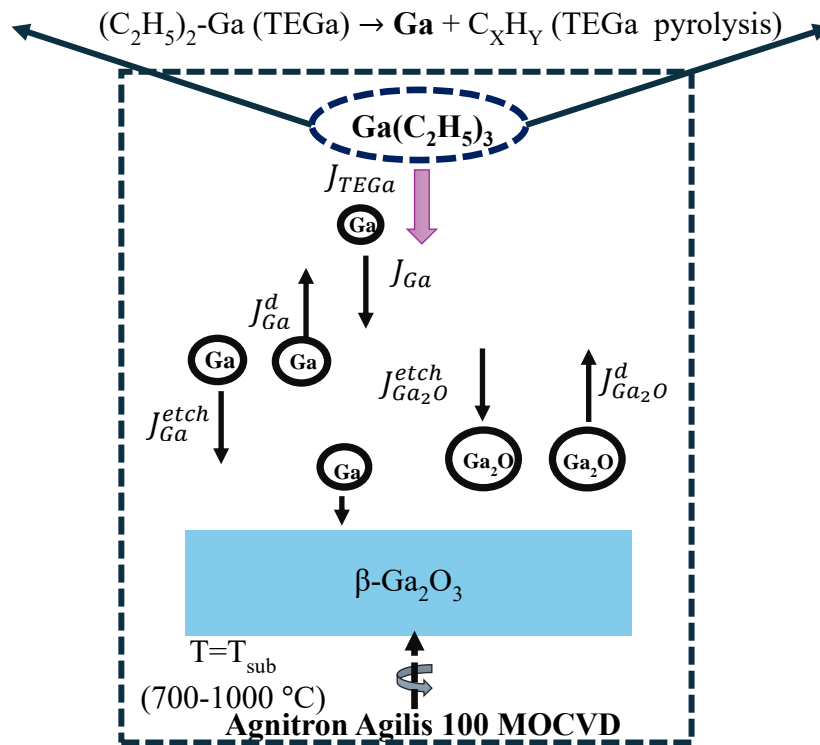
Figure 3.9 Schematic illustrates the Ga and Ga$_2$O conservation on the Ga$_2$O$_3$ substrate.

At low gallium flux (TEGa flow), the total substrate coverage is less than the combined

coverage of gallium and suboxide, as illustrated in Figure 3.10. This implies that there is

no accumulation of Ga or Ga_2O remaining on the Ga2O3 surface to impede the incoming

gallium flux. Now, rate at which Ga coverage on substrate varies can be written as rate of

incoming gallium (J_{Ga}) after pyrolysis, rate of Ga consumed in etching (J_{Ga}^{etch}) and rate

of desorbed Ga from the substrate (J_{Ga}^{d}). Simultaneously, for Ga_2O we can write the

suboxide coverage rate as suboxide formation rate ($J_{Ga_2O}^{etch}$) and suboxide desorption rate

($J_{Ga_2O}^{d}$).

we can write $(\frac{d\sigma_{Ga}}{dt})$ and $(\frac{d\sigma_{Ga_2O}}{dt})$ as follows:

$$(\frac{d\sigma_{Ga}}{dt}) = J_{Ga} - J_{Ga}^{etch} - J_{Ga}^{d}$$

$$(\frac{d\sigma_{Ga2O}}{dt}) = J_{Ga_2O}^{etch} - J_{Ga_2O}^{d}$$

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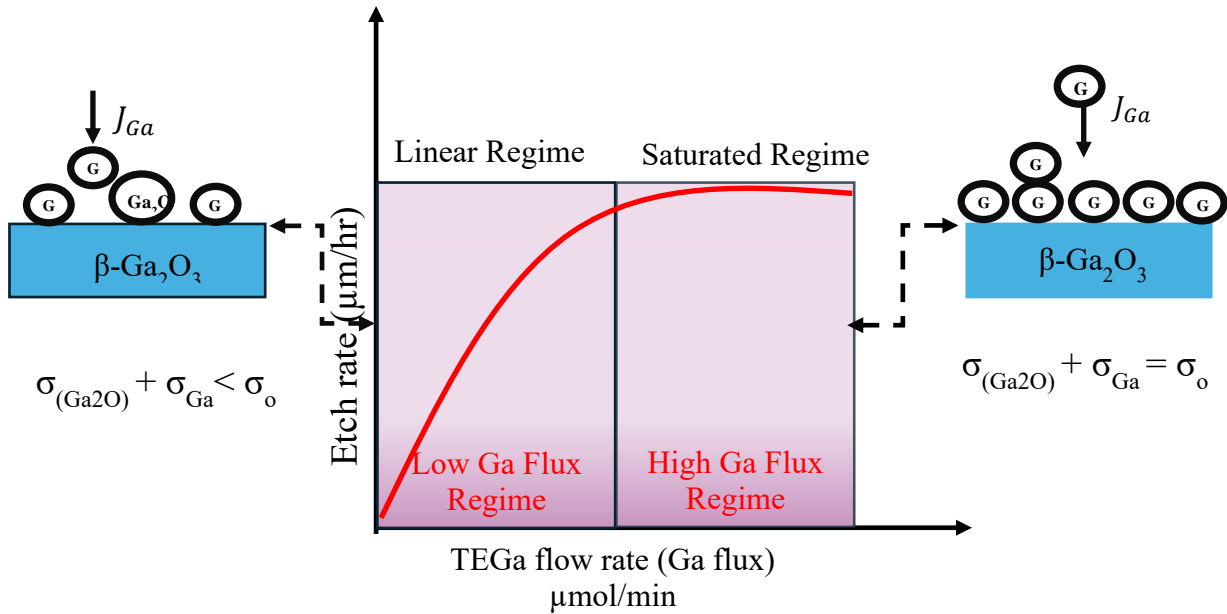
Figure 3.10 Schematic illustrates the surface coverage on Ga_2O_3 at both low and high Ga flux regimes.

Now we can write these $(\frac{d\sigma_{Ga}}{dt})$ and $(\frac{d\sigma_{Ga_2O}}{dt})$ in Arrhenius equation form since this etching mechanism is based on chemical kinetics.

$$J_{Ga}^{etch} = 4\sigma_{Ga}ke^{\frac{-E_s}{KTsub}}$$

$$J_{Ga_2O}^{etch} = 3\;\sigma_{(Ga2O)}\,ke^{\frac{-E_s}{KTsub}}$$

Here, E_s = Activation energy.

K= Boltzmann constant.

K= constant independent of temperature.

Similarly, we can write for $J_{Ga_2O}^d$ and J_{Ga}^d as follows:

$$J_{Ga}^d = A_1\sigma_{Ga}ke^{\frac{-E_{d1}}{KTsub}}$$

$$J_{Ga_2O}^d = A_2\;\sigma_{(Ga2O)}\,ke^{\frac{-E_{d2}}{KTsub}}$$

Here, A_1 and A_2 = Constants

E_{d1} and E_{d2} = Energy barriers for desorption.

Finally etch rate can be written as:

$$R = \frac{\frac{J_{Ga}}{4\rho}}{1 + \frac{A_1}{4k}e^{\frac{E_s-E_{d1}}{KT_{Sub}}}}$$

Figure 3.11 (a) shows the visual of Gallium (Ga) flux and Gallium suboxide (Ga_2O) flux conservation on Ga_2O_3 substrate. (b) show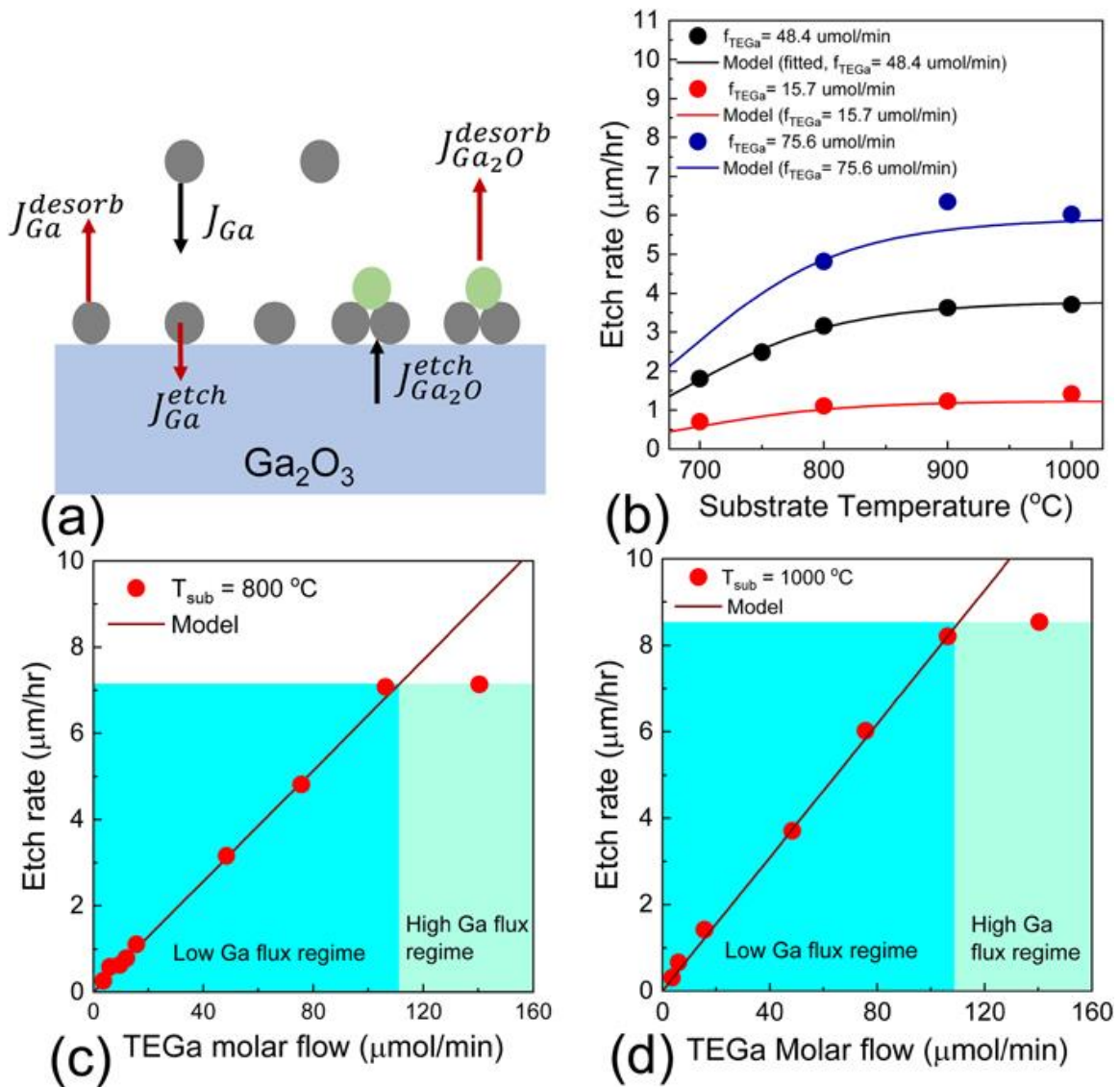s the fitting of experimental data for etch rate and substrate temperature at three different molar flow rates of TEGa (Ga flux). (c) and (d) show the model fitting for etch rate and TEGa molar flow rate at two different substrate temperatures ($T_{sub} = 800$ and 1000 ℃).

Table 4: shows the fitted values and the unknown parameters.

Parameter	Fitted Valu
C_1	0.079 µm/µmol
C_2	3.15×10^{-8}
E_A	1.45 eV

3.4: CONCLUSION

To conclude, a novel in-situ etching technique is demonstrated on β-G_2O_3 based on self-reaction mechanism using triethylgallium as etchant in MOCVD. Key etching characteristics like etch rate and RMS roughness are studied against the MOCVD chamber parameters like molar flow rate, chamber pressure and substrate temperature. Blanket and patterned etching was also demonstrated using this technique on (010) and (001) bulk gallium oxide substrates. High etch rates as high as 8.5 µm/hr is demonstrated at $T_{sub} > 900$ ℃ and TEGa molar flow > 100 µmol/min. Moreover, RMS roughness as low as 2.8 nm on (010) β-Ga_2O_3 and 3.1 nm on (001) is demonstrated. Tiled SEM images on spoke-wheel structures showed vertical sidewalls on (010) and (001) β-Ga_2O_3. Etch anisotropy was also investigated on (010) β-Ga_2O_3 showing different sidewall profiles and lateral etching rates along different in-plane orientations. Ultimately, aside from all the advantages that we get from this technique, the incorporation of MOCVD regrowth following etching supremely positions this method above others, offering lower contamination and interface defects.

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