Techniques on Galvanically Isolated RF Chip-to-Chip Communication Circuits and Pulse-Width Modulated Class-E Power Amplifiers

by

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ABSTRACT

This thesis presents three novel studies. The first two works focus on galvanically isolated chip-to-chip communication, and the third research studies class-E pulse-width modulated power amplifiers. First, a common-mode resilient CMOS (complementary metal-oxide-semiconductor) galvanically isolated Radio Frequency (RF) chip-to-chip communication system is presented utilizing laterally resonant coupled circuits to increases maximum common-mode transient immunity and the isolation capability of galvanic isolators in a low-cost standard CMOS solution beyond the limits provided from the vertical coupling. The design provides the highest reported CMTI (common-mode transient immunity) of more than 600 kV/μs, 5 kVpk isolation, and a chip area of 0.95 mm^2. In the second work, a bi-directional ultra-wideband transformer-coupled galvanic isolator is reported for the first time. The proposed design merges the functionality of two isolated channels into one magnetically coupled communication, enabling up to 50% form-factor and assembly cost reduction while achieving a simultaneously robust and state-of-art performance. This work achieves simultaneous robust, wideband, and energy-efficient performance of 300 Mb/s data rate, isolation of 7.8 kVrms, and power consumption and propagation delay of 200 pJ/b and 5 ns, respectively, in only 0.8 mm^2 area. The third works studies class-E pulse-width modulated (PWM) Power amplifiers (PAs). For the first time, it presents a design technique to significantly extend the Power back-off (PBO) dynamic range of PWM PAs over the prior art. A proof-of-concept watt-level class-E PA is designed using a GaN HEMT and exhibits more than 6dB dynamic range for a 50 to 30 percent duty cycle variation. Moreover, in this work, the effects of non-idealities on performance and design of class-E power amplifiers for variable supply on and pulse-width operations are

characterized and studied, including the effect of non-linear parasitic capacitances and its exploitation for enhancement of average efficiency and self-heating effects in class-E SMPAs using a new over dry-ice measurement technique was presented for this first time. The non-ideality study allows for capturing a full view of the design requirement and considerations of class-E power amplifiers and provides a window to the phenomena that lead to a mismatch between the ideal and actual performance of class-E power amplifiers and their root causes.

DEDICATION

TO MY PARENTS,
FARIBA AND MAHMOUD

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CHAPTER 1

Introduction

1.1 Galvanically Isolated RF Chip-to-Chip Communication System

From the early developments of electrical systems, galvanic isolators (GIs) have proved to be a necessity for safe and reliable communication of data and control signals between circuits that experience dynamic and high voltage (HV) ground differences; this need for a fail-safe communication interface, lead to the development of first GIs using bulky mechanical relays and transformers[1]–[3]. However, in the 1970s, owing to solid-state technology advancements, implementation of GIs on a chip-scale became possible through the development of optocouplers, which remain available as a traditional GI solution[1]–[5]. Today, GIs are offering isolated digital data and control buses in countless commercial and industrial applications, including modern home appliances (e.g., digitally controlled washing machines), EVs, industrial systems, network/medical equipment, and lab instruments. A generic communication system utilizing bidirectional GIs is demonstrated in Figure 1-1. Through time, one fact about GIs remained unchanged: they are required in systems that use them in high numbers, and therefore their cost, size, and performance are pivotal to the overall system specifications. Presently, GIs are demanded to lend themselves to full CMOS integration with minimum area and fabrication steps to minimize implementation cost and enable silicon system on chip integration--while performing a robust, reliable, and efficient communication. However, optocouplers can achieve reliable isolation ratings; however, they suffer from a lack of low-cost CMOS integration, aging, and poor power efficiency[6]–[9]. In recent years, the development of CMOS RF

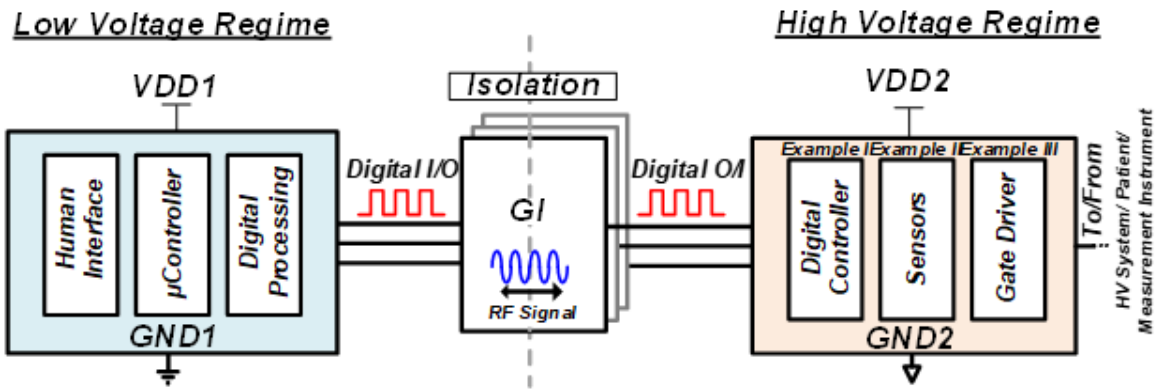

Figure 1-1 A Generic Galvanically isolated system

transceivers and passive devices such as on-chip transformers has paved the way for a new generation of GIs that adopt CMOS RF chip-to-chip communication to offer full CMOS integration. CMOS GIs not only target to address the shortcomings of the optical solutions but also to meet the increasingly demanding and specifications for the modern applications[9]–[16]. These requirements include communication durability and functionality in the presence of disruptions from fast-changing high-voltage common-mode transient (CMT) that appear across the transmitter die and the receiver die grounds. They are measured in terms of isolation rating (ISR, in kV) and CMT immunity (CMTI, in kV), referring to the CMT's maximum magnitude and transient slew-rate resiliency, respectively. Other key performance metrics for GIs are data rate, power consumption, and propagation delay. Prop. delay should be minimum to ensure system stability in control applications. These requirements for reliable and resilient RF communication in the presence of high-voltage disruption in addition to the cost and size--while meeting additional communication specifications such as low propagation delay, power consumption, and high data rate--introduces complex design challenges that were not either absent or not a concern in mainstream RFIC transceivers and must be addressed. GIs

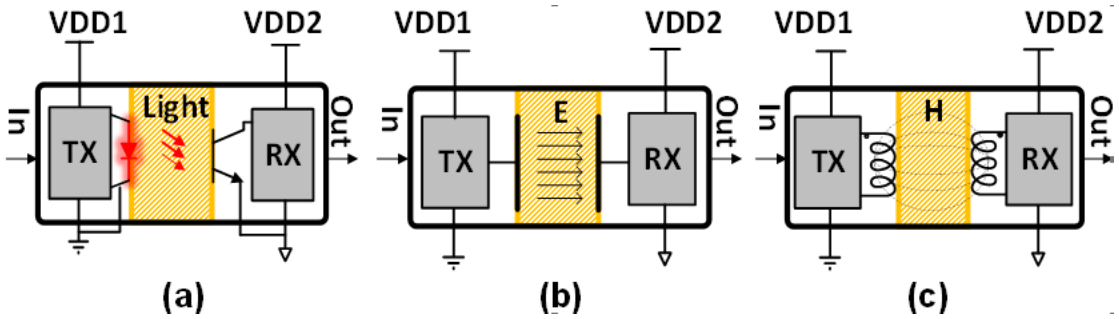

Figure 1-2 (a) Optocoupler (b) Capacatively and (c) Magnetically Coupled GIs

mainly consists of two dies: a transmitter (TX) die and a receiver (RX) die, where the circuits on the TX die are galvanically isolated from the circuits on the RX die using an isolating barrier made of a dielectric material. To transmit digital information from the TX die to the RX die through this high voltage dielectric, an RF coupling mechanism is required, such as light [17], [18], an RF electrical field, or an RF magnetic field [1]–[5], [8]–[20].

Figure 1-2 (a)-(c) shows three GI architectures with three different coupling methods. Optocouplers are a traditional solution for GIs that use light to communicate between the two dies. Although they offer high isolation ratings, they have yet to be integrated into silicon with low cost. Furthermore, they exhibit a shorter lifetime, lower CMTI, and slower data rate in comparison with CMOS GIs [9], [26], [27]. Magnetic coupling is an alternative for optocouplers. Magnetic coupling uses an RF magnetic field to enable data transfer across the HV barrier, and this method can be integrated into silicon, but it is limited in isolation. In addition to a high isolation rating, a GI must maintain reliable communication performance, hence requiring an RX circuit with high CMTI. However, achieving high CMTI while maintaining high sensitivity and power efficiency is a major challenge in

fully-CMOS magnetic coupled GIs. In this work, two methods on GIs are presented to achieve state of the art galvanically isolated chip-to-chip communication performance.

1.1.1 Research Questions

Some of the key question that this thesis aims to answer regarding galvanic isolators are:

1- Is it feasible to use an on-chip lateral resonant coupling to achieve robust and common-mode resilient galvanically isolated chip-to-chip communication?
2- Can functionality of two uni-directional magnetic coupled galvanic isolators be merged into one magnetic link shared in both directions to reduce chip area and manufacturing cost?
3- Is it feasible to implement a low-cost GI with simultaneous high performance on GI metrics, including isolation rating, data rate, energy efficiency, and CMTI?

1.1.2 The method I: A laterally resonant coupled magnetic coupled isolator

This work presents a magnetic coupled galvanically isolated chip-to-chip communication system that utilizes laterally coupled resonators combined with a new differential receiver architecture for GIs. The on-chip lateral resonant coupled technique in this method is investigated for the first time to enable low-cost enhancement of isolation rating and reliability. The highlights of this work are 1) fully integrated, small form factor GI solution in CMOS that does not alter the native fabrication process or add extra steps to packaging/assembly and achieves an isolation rating that exceeds the breakdown voltage allowed by the process's IMD thickness, 2) a novel low-power and low-latency RX architecture that enables high CMTI while maintaining high sensitivity, and 3) a differential resonant coupled channel that consists of a center-tapped transformer RX

interface to both improve the CMTI and reduce in-band interference, thanks to the inherent band-pass filtering.

1.1.3 Method II: An Ultra-wideband bi-directional

Today many applications require GIs to offer bidirectional communication to either enable read/write functionality in data applications or to provide feedback or status monitor signals in control applications. Currently, GI products achieve bi-directivity using two separate unidirectional GIs, assembled in opposite directions, which consume a large area. This method presents a fully CMOS BDGI that addresses the aforementioned challenges and drawbacks to achieve state-of-art GI performance on all performance metrics. Some of the highlights of the GI presented in this work are: (1) achieving bi-directivity using a shared communication channel in both directions for 50% area and cost reduction (2) new low-power differential GI receiver using source-gate coupled input stage for simultaneously CMTI enhancement and wide-band polarity modulated signal detection, with an automatic digital counter-pulse cancellation technique (3) differential double-isolated transformer communication channel for achieving high full-CMOS isolation without altering the process, in this work we demonstrated that double isolated topology also achieve low performance sensitivity to chip alignment offset and therefore bondwire lengths, and in conjunction with the implemented receiver can provide interference immunity thanks to symmetric center-tapped structure and (4) re-configurable wide-band GI transmitter architecture with ringing cancellation mechanism to increase channel capacity, and capability of generating high-Z mode during reception to support bi-directional communication (5) a digital self-interference cancellation to prevent self-reception.

1.2 Introduction to Efficiency and Dynamic Range Enhanced Switch-Mode Power Amplifiers

RF power amplifiers (RFPAs) are key components in RF transceivers and omnipresent in wireless communication circuits. Wireless communication can be described as the transfer of energy and information [28]. RF power amplifiers utilize DC power to generate a high power version of a low power modulated input signal and deliver it to their output load, usually the antenna. RFPAs are known as one of (if not the one) highest power consuming blocks in wireless transceivers, thus from the early days of vacuum tubes until now (transistor's era), efficiency enhancement of power amplifiers is heavily researched. The efficiency of power amplifiers is calculated by their ability to convert the DC power to RF power with minimum loss. Thus high efficiency means less heating, larger communication range for the same available DC power, and less power consumption, which results in lower maintenance and operation cost, especially for base station applications and longer battery life for battery-operated devices.

Through time, the design of RF PAs has been continuously evolving due to two major factors 1) Technology Development 2) Evolution of Radio Standards, causing new PA architectures to emerge, disappear and sometimes, reappear.

Early power amplifiers used vacuum tubes as an amplification device. With the inventions of transistors, today RFPAs are dominated by transistor-based architectures. Furthermore, recently, the development of compound material based transistors (GaN and GaAs) has enabled new possibilities over previously Si-based designs. Especially for base

station applications, GaN RF transistors can enable higher efficiency and power handling capability for RFPAs.

In addition, in modern days, the use of high peak to average power ratio (PAPR) OFDM signals in LTE and WLAN applications is standard and has introduced major challenges to the design of power amplifiers when compared with earlier constant envelope modulation methods. Since these modern standards –while offering desirable RF system performance– were not optimized for hardware implementation[29], they desire high-performance PAs that not only support high dynamic ranges but also should maintain high efficiency when they back off from their peak transmission power. Moreover, this problem is exacerbated since high PAPR standards also distribute a heavier share of the probability density of output power at lower power values meaning the modulated RF signal spends a longer time at power back off rather than a peak. This becomes more challenging to know that RF power amplifiers are physically known to express the opposite behavior, with their efficiency peaking at the highest output power and drop rapidly when backed off from maximum output power, as shown in Figure 1-3. Therefore there is a need for a PA topology with a high PAPR (dynamic range) and high efficiency.

1.3 Motivation

RFPA architectures traditionally use current source topologies (known as linear topologies); despite offering highly linear performance and great dynamic range, they still lack efficiency. Switch-mode power amplifier (SMPAs) is another category of RFPAs that enable achieving both theoretically and practically higher peak efficiencies when compared with current source PAs, reaching maximum 100% efficiency, which makes them an excellent choice for constant envelop applications they have been demonstrated to achieve

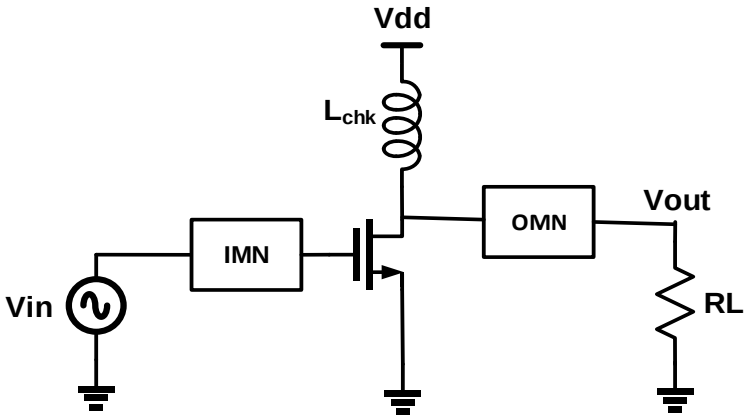

Figure 1-4 A General Current-Source Power Amplifier

highest reported efficiencies when using GaN HEMT devices. However, unlike linear RFPAs since SMPAs utilize transistors as a switch, controlling the output power of SMPAs through modulation of input amplitude (no dynamic range) has limited their practicality. Thus, different techniques and topologies have been developed to adapt SMPAs for amplitude modulated applications, taking advantage of the inherently high efficiency of SMPAs. Furthermore, with continuous growth and advance of digital fabrication technologies, SMPAs are highly desired for enabling an all-digital transmitter, promising a more holistic transmitter allowing for higher compatibility and integration. Class-E power amplifier is a flagship SMPA topology that is highly desirable due to its ability to achieve the highest efficiency among SMPAs, using only one transistor, which allows high cost and complexity in comparison with dual transistors PAs such as Class-D.

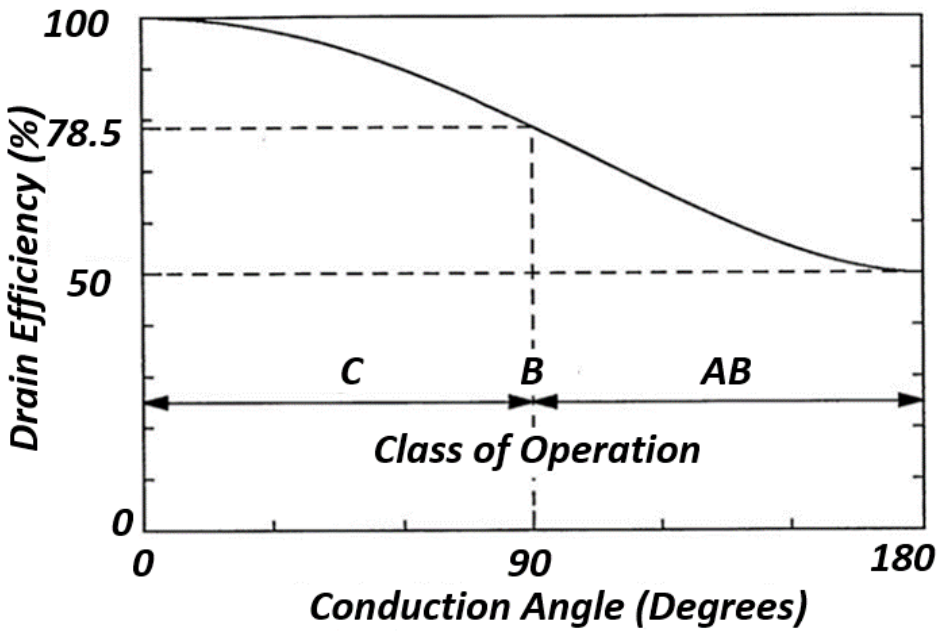

Figure 1-5 Efficiency of current source PA vs. angle of conduction and classes A,B, and C definition [30][36]

To date, Dynamic enhancement techniques developed for SMPAs such as supply modulation (Envelope elimination and restoration aka EER), outphasing/LINC (**LI**near amplifications using **N**on-linear **C**omponents), and PWM (pulse-width modulation). However, they suffer from either large efficiency drop with power back off or have a limited dynamic range. This work investigates class-E PWM SMPA for base station applications, with GaN utilized as the switching device for the RFPA to achieve high RF performance, which can be combined with a driver/modulator implemented in CMOS to enable low-cost PWM operation. This work shows that class-E PWM SMPAs can achieve a superior efficiency profile with a slower loss mechanism compared to the prior art and also studies the efficiency profile under variable supply voltage, showing that when PWM

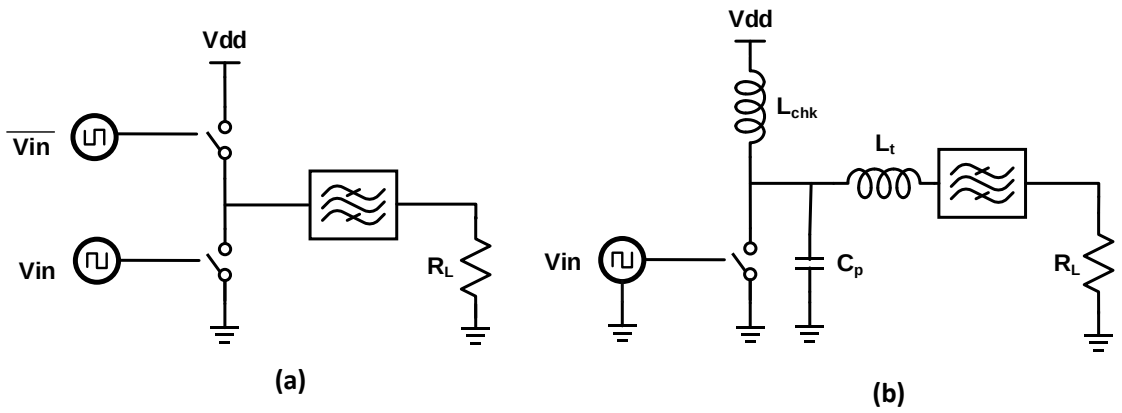

Figure 1-6 (a) Class-D and (b) Class-E RF Power-Amplifier Schematics

is combined with a multi-level implementation, not only the pulse-swallowing PWM limitation of SMPAs is addressed, but also a significantly higher efficiency and dynamic range for the same number of discrete-levels can be achieved in comparison with previously reported work, therefore making the proposed Class-E PWM PA an excellent candidate. A literature review shows that little investigation has been done on class-E PWM RFPAs from the PA design perspective.

In this work class-E, PWM PA's previously unexplored characteristics and behavior are investigated, including the behavior of class-E PAs (and techniques to enhance them) under variable duty cycles and supply voltages, including the effect of non-idealities such as non-linear parasitic transistor capacitances.

1.4 Current Source Power Amplifiers

Current source power amplifiers, as their name implies, are power amplifiers that utilize the amplifier transistor as a current source. Figure 1-4 shows a general demonstration of current source RFPAs. In this configuration, the DC biasing of the gate determines the

quiescent operation point and thus the conduction angle during large-signal operation[30]. Depending on the conduction angle, these PA are classified to Class-A, B, AB, and C, with a trade-off between the power utilization factor, linearity, and maximum efficiency, depicted in Figure 1-5. With class-A being the most linear and class-C, the most efficient in this category. Class AB PAs are the most popular PAs due to their balanced linearity, efficiency, and power utilization factor (PUF) among these classes. In this class, the output power can be controlled by the input voltage swing. However, Class-AB PAs peak efficiency is limited to ~80% in theory and drop significantly with back-off from peak power operation, as demonstrated in Figure 1-1.

1.5 Switch-Mode Power amplifiers

Switch-mode PAs, as the name suggests, use the power transistor as a switch instead of a current source. Since a switch ideally maintains zero voltage across it when it's ON and conducts no current when it's off, a switch in combination with a bandpass filter can be utilized to generate a periodic waveform while all the power drawn from the supply is converted to output power and no power is theoretically consumed in the transistor enabling a maximum efficiency of 100%. Class-D PA is a double-switch SMPA that operates using hard switching between ground and supply (shown in Figure 1-6). Although, ideally, Class-D SMPAs achieve 100% efficiency, in reality, the input and output capacitance of the switching transistors, crow-bar current, and ON resistance of switching devices introduce losses that diminishes the SMPAs efficiency. Class E PAs (shown in Figure 1-6) was introduced in [31] by Nathan Sokal in 1975 as an alternative for Class-D PAs, a single switch architecture that can address practical limitations of Class-D PA and also achieve the highest PA efficiency. Class-E PAs use one switching transistor in a soft-

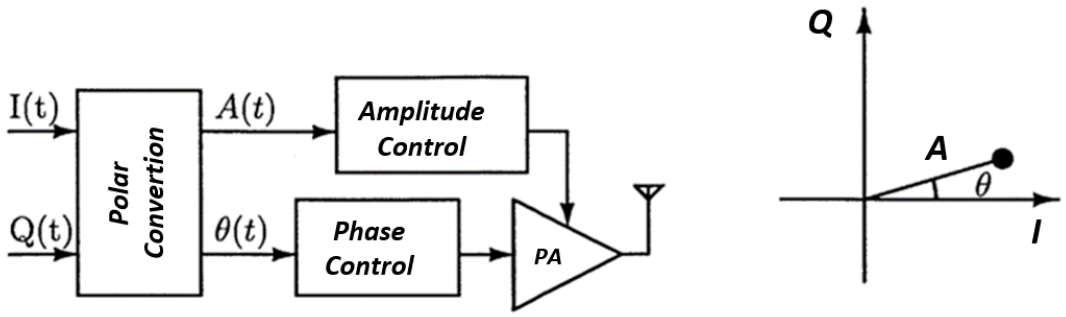

Figure 1-7 (a) Block diagram and (b) Vector Decomposition in Polar RF PAs [36]

switching configuration, and absorb the output capacitance of the switch (Cds) in the output network of the PA that is used to shape the waveform and create a non-overlap between voltage and current waveforms [32], thus eliminates Cds losses that do exist in class-D. Furthermore, Class-E PAs won't experience crow-bar current like Class-Ds and are less sensitive to rise time and fall time of the square wave input signal. Considering the large output capacitance of power RF devices (especially in high power PAs) and also the fact that driving signals have a non-zero rise time and fall time (tr and tf), class-E PAs have shown a superior performance when compared to class-D PAs, especially in GaN PAs where the transistors have a high breakdown voltage, and large-signal swings of class-E PAs are tolerable. In CMOS PAs, class-D can be preferred due to the low breakdown voltage of the deep sub-micron process and the fact that class-E PAs, unlike class-D, produce stress voltages higher than 3x of the supply voltage value.

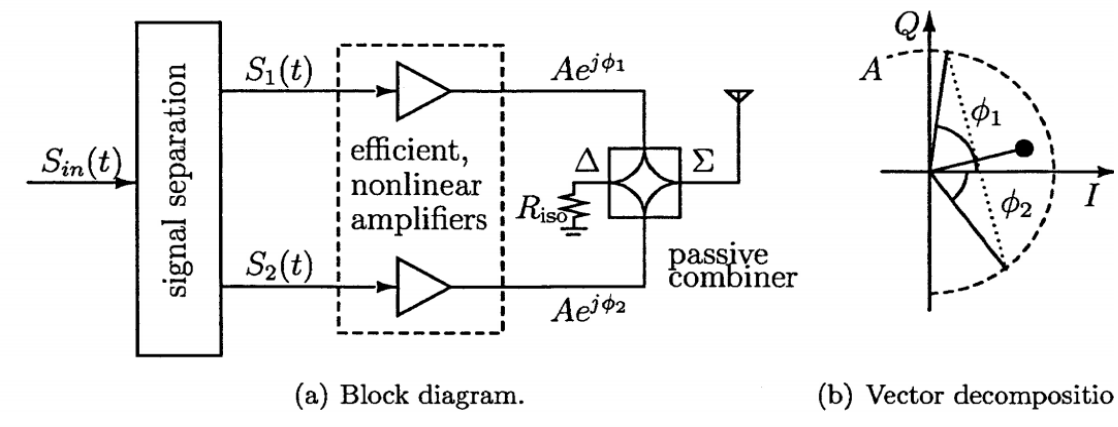

Figure 1-8 (a) Block diagram and (b) Vector Decomposition for LINC PAs [36]

1.5.1 Linearization and Efficiency Enhancement techniques

1.5.1.1 Polar/Envelope Elimination and Restoration (EER)

Although SMPAs offer the highest efficiency, however, they were developed for constant envelope applications, and due to their switching and non-linear structure, linearization techniques need to be used to make them suitable for non-constant applications. One of these techniques, first mentioned in [33], is EER. In this method, the input of the SMPA is used to control the phase of the PA output and a supply modulator to control the envelope of the PA output[34], [35]. Since amplitude information is separated from the input signal and later is restored at the output, this method is named EER. However, the increase in bandwidth and PAPR in modern standards results in lower efficiency of the supply modulator, and with an excess of the loss, the total efficiency of the system can be comparable or less than the achievable efficiency from conventional linear PAs (e.g.,

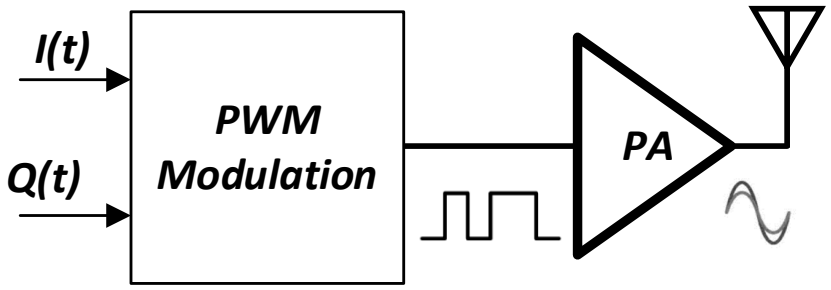

Figure 1-9 Conceptual Block Diagram of a Pulse-Width Modulated PA

Class-AB) family, neutralizing the benefits of the SMPA utilization and their higher efficiencies.

1.5.1.2 Linear Amplification Using Non-Linear Components

LINC systems linearize switch-mode PAs using out-phasing technique enabling linearization of non-linear PAs such as SMPA and Class C PAs. In LINC output of two non-linear PAs are power combined, and the total output power is controlled by out-phasing (controlling the relative phase difference between the two PA branches) [36]. Depending on the phase difference between the two PAs, different amplitudes can be generated. The maximum Pout is achieved with the two PAs in-phase, and minimum out power is achieved with the two PAs being 180 degrees out of phase. In this method, achieving low power output (and thus high dynamic range) is challenging since any time mismatch between the two branches will lead to amplitude errors, especially at lower amplitudes, and the efficiency of the PA drops drastically with the power back-off making this approach impractical for large PAPR applications.

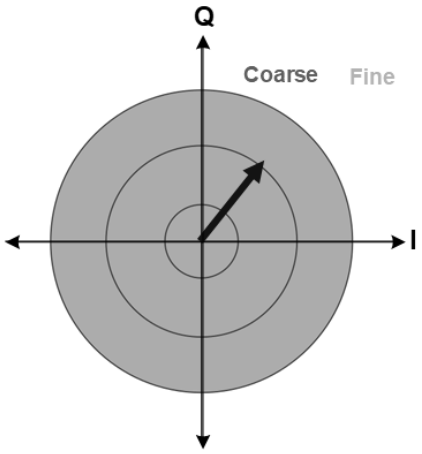

Figure 1-10 Concept of Class-G Power Amplifier

1.5.1.3 Pulse-Width Modulation (PWM)

PWM PAs modulate an SMPA's output power by controlling the duty cycle of the square wave input signal of the power amplifier. This technique can be implemented using class-D [37] and class-E PAs[38]. However, the dynamic range of PWM SMPA is limited due to pulse swallowing of the digital input signal at lower duty cycles due to the large gate capacitance of the power transistors, limiting the PWM operation range to practically a minimum pulse width of ~30 percent duty cycle[39]. In a PWM class-E GaN SMPA driven by a CMOS driver[39], [40] is used to implement a PWM PA, however, had a limited dynamic range, and after the duty cycle limit was achieved, the PA was driven in linear mode to overcome the dynamic range limitation, causing a steep (fast) roll-off from peak efficiency with power back-off.

1.5.1.4 Multi-level Switch-Mode Power Amplifiers

Multilevel power amplifiers were first introduced in 1976. This class combines a fine power control method at the PA input, such as the amplitude of input in case of linear PA or the phase difference of two branches in out-phasing topology in case of SMPAs, with a

coarse discrete level power (amplitude) controlling method that acts as a gear shifter (such as modulation of voltage supply between a discrete set of voltages or power combining of power amplifiers that can be turned ON and OFF individually) when the fine control method reaches its limits. Figure 1-10 shows the concept of Class-G modulation, with circles showing the coarse power control and the shaded area showing the fine power control, which modulates the power within the boundary of one circle to the next adjacent circle. Utilizing Class-G operation in both linear and switch-mode PA systems eliminates the need for wideband linear regulation circuits, allowing achieving higher efficiency, bandwidth, and less efficiency to bandwidth increment sensitivity in comparison with ET and polar (EER) supply modulation. In [41][42] a class-G supply modulator is used in combination with a linear GaN class-AB amplifier for base stations. In [43]–[45] a multi-level supply modulator is used in combination with out-phasing SMPAs, and in [46] a discrete set of duty cycles is combined with out-phasing SMPAs. In [46] combination of all these three methods: discrete duty cycles, discrete voltage levels, and out-phasing operation of SMPAs are also simulated for achieving an enhanced efficiency profile; however, this method can be implemented only at the expense of significantly higher complexity. SMPA based Class-G PAs allow for higher total efficiency in comparison with linear class-G PAs due to the higher inherent efficiency of SMPAs. SMPA multilevel works from [43]–[46] utilized class-E PAs class-E PAs due to its higher peak efficiency. However, in all these works, the steep slope of efficiency roll-off with power backoff is a major limitation resulting in requiring a higher number of discrete supply levels for achieving a certain power back off, which leads to more number of supply switching which

consequently can reduce the overall efficiency or the need for mixing more than two power control methods.

1.5.2 Research Questions

This research tries to answer the following question regarding PWM Class-E PAs for base-stations:

1- Is it feasible to enhance class-E power amplifiers' duty cycle sensitivity and, therefore, their dynamic range?
2- What are the non-ideality effects in class-E power amplifiers' performance and their causes in the presence of variable pulse-width and supply conditions?
3- Can Class-E PWM PAs demonstrate a superior efficiency-power back off profile compared to prior art when changing the supply levels to lower values upon reaching the lower bound of the duty-cycle range?

1.5.3 Method

This work studies the design of GaN class-E PWM PAs and investigates techniques and many of the challenges of designing PWM PAs, including the effect of multi-level supply variation combined with pulse-width modulation for the first time. Detailed explanations on the reason for choosing class-E PWM and its significance presented with formulated design guidelines. This work introduces *efficiency roll-off,* indicating the efficiency sensitivity to power back off, as a critical factor for determining the average efficiency and dynamic range in multilevel PA architectures. A comparison of efficiency roll-off between different PAs classes by this work demonstrates that class-E PWM combined with the multi-level operation can achieve a superior efficiency and dynamic range profile for a

lower number of levels when compared with the prior art. Duty-cycle sensitivity in SMPAs is investigated and compared, showing a superior performance from Class-E PAs, enabling a broader dynamic range to be reached using a 50%-30% duty cycle variation. Furthermore, a duty cycle sensitivity enhancement technique for Class-E PAs is introduced to boost the dynamic range achievable within the practical range of input signal's duty-cycle above the previously known limits. This research furthers its investigation to explore the influence of non-idealities such as parasitic capacitance non-linearity of switching transistors in PWM operation of class-E PAs for the first time on circuit-level along with a supporting theory and proposes a design methodology to exploit this effect to reach an efficiency profile that increases with power back-off. Also, the effect of self-heating is characterized in class-E PAs with variable supply and pulse-width for the first time through simulation and empirical results. A novel dry-ice based measurement technique was proposed for the low-cost and practical characterization of heating effects in power amplifiers.

CHAPTER 2

A Common-Mode Resilient CMOS Galvanically Isolated RF Chip-to-Chip Communication System

Galvanic isolator (GI) RF integrated circuits (RFICs) are in high demand for a wide range of consumer and industrial applications, including control systems, biomedical sensors/equipment, and isolated data links [9], [13]–[15], [26], where digital control signals or data must be reliably communicated between two chips while maintaining galvanic (DC) isolation between them. GIs allow safe and reliable interfacing of low voltage integrated circuits (ICs), such as microcontrollers or DSP circuits, with ICs that operate in high voltage domains or are susceptible to fast common-mode high-voltage (HV) transients, as demonstrated in Figure 2-1. GIs are omnipresent in various systems (from automotive to home appliances) and are used in high numbers per system (with one GI in each signal path) to communicate multiple signals, which emphasizes the need for low-cost GI solutions that offer a high level of CMOS integration with systems such as microcontrollers and gate drivers. A GI's key performance specifications are cost, reliability, isolation rating, common-mode transient immunity (CMTI), and propagation delay. The cost of GIs is associated with fabrication technology, die area, and packaging and assembly cost. Isolation rating (kV) is the maximum transient magnitude a GI can withstand reliably without dielectric failure, and CMTI (kV/μs) refers to the highest transient slew rate tolerable by a GI without affecting its output [9], [26].

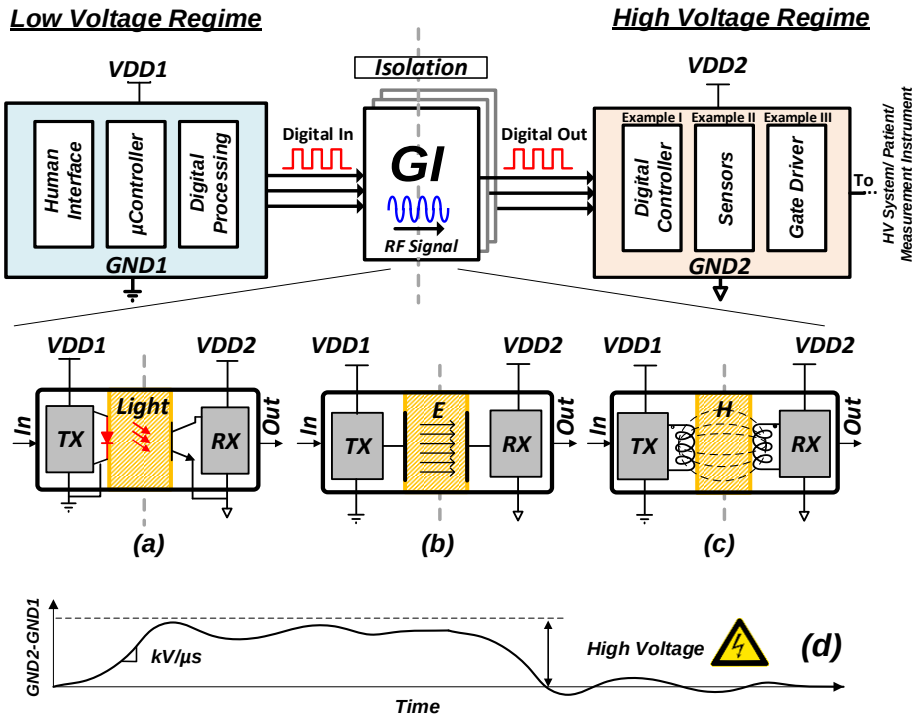

Figure 2-1 Generic communication system utilizing an isolator (a) Optocouplor (b) Capacitively coupled (c) and Magnetically Coupled GIs (d) Common mode transient wave form across GND2 and GND1.

GIs mainly consists of two dies: a transmitter (TX) die and a receiver (RX) die, where the circuits on the TX die are galvanically isolated from the circuits on the RX die using an isolating barrier made of a dielectric material. To transmit digital information from the TX die to the RX die through this high voltage dielectric, an RF coupling mechanism is required, such as light [17], [18], an RF electrical field, or an RF magnetic field [1]–[5], [8]–[20]. Figure 2-1 (a)-(c) shows three GI architectures with three different coupling methods. Optocouplers are a traditional solution for GIs that use light to communicate between the two dies. Although they offer high isolation ratings, they have yet to be integrated into silicon with low cost. Furthermore, they exhibit a shorter lifetime, lower

CMTI, and slower data rate in comparison with CMOS GIs [9], [26], [27]. Magnetic coupling is an alternative for optocouplers. Magnetic coupling uses an RF magnetic field to enable data transfer across the HV barrier, and this method can be integrated into silicon, but it is limited in isolation.

In addition to a high isolation rating, a GI must maintain reliable communication performance, hence requiring an RX circuit with high CMTI. However, achieving high CMTI while maintaining high sensitivity and power efficiency is a major challenge in fully-CMOS magnetic coupled GIs.

This work presents a magnetic coupled galvanically isolated chip-to-chip communication system that utilizes laterally coupled resonators combined with a new differential receiver architecture for GIs. The highlights of this work are 1) fully integrated, small form factor GI solution in CMOS that does not alter the native fabrication process or add extra steps to packaging/assembly and achieves an isolation rating that exceeds the breakdown voltage allowed by the process's IMD thickness, 2) a novel low-power and low-latency RX architecture that enables high CMTI, while maintaining high sensitivity, and 3) a differential resonant coupled channel that consists of a center-tapped transformer RX interface to both improve the CMTI and reduce in-band interference, thanks to the inherent band-pass filtering.

In-depth background information and analysis of magnetic coupled GIs and the proposed method are given in Section 2-1. In Section 2-2, the implemented GI solution is explained with detailed circuit and system-level descriptions. In Section 2-3, measurement results are presented for the passive structures and full RF chip-to-chip channel. Additionally,

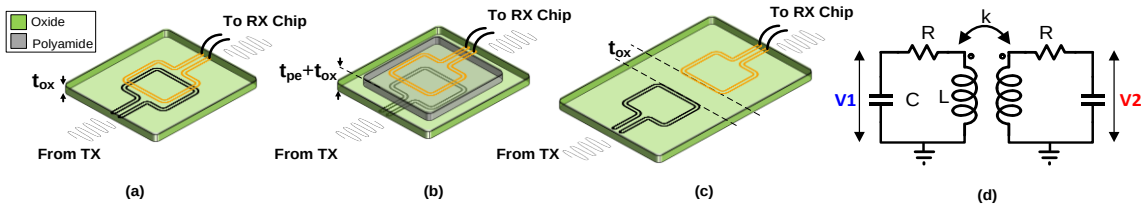

Figure 2-2 .Magnetically Coupled GI topologies (a) Stacked CMOS (b) Stacked CMOS with post-processing (c) CMOS Integrated Lateral Magnetic coupling (this work)

Table 2-1: Magnetic Coupling Topology Comparison Summary

Topology	Stacked Coupling Fig. 2(a)	Stacked Coupling with Non-CMOS dielectric Fig. 2(b)	Lateral Coupling -This Work- Fig. 2(c)
Insulation Material	SiO2	Polyimide	SiO2
Isolation Rating(kV)	≤ 2.5	> 3.0	> 3.0
Standard CMOS & Packaging	✓	✗	✓
IMD thickness Independent	✗	✓	✓
Alignment Insensitive	✓	✗	✓

measurements are provided for multiple ICs over multiple wafer lots and assemblies to understand design sensitivity. Section V concludes this paper.

2.1 Background and Proposed Method

2.1.1 Stacked Coupling

For realizing fully integrated CMOS magnetically coupled GIs to-date, two magnetically coupled inductors have been stacked, and a high-voltage barrier has been realized by the IMD oxide that fills the vertical interspace between the two inductors, as illustrated in Figure2-2(a). In this method, the CMOS process's IMD thickness (t_{ox}) is the bottleneck for the maximum achievable isolation rating [15], [47]. However, this method has been limited to 2.5 kV (<2kVrms) [9], [13], thus preventing it from fulfilling applications in the popular

3kVrms isolation range. .Methods such as inserting additional layers of thick dielectrics (e.g. polyimide or die-attach fill adhesives with a thickness of t_{pe}) between two inductors has been proposed (Figure2-2 (b)) to increase the effective dielectric thickness to more than the IMD's oxide thickness (to a total of $t_{ox}+t_{pe}$) for achieving higher isolation capability. However, these methods require non-standard CMOS packaging, altering the native CMOS process, or increasing the packaging and assembly steps, and they introduce large chip-to-chip gain sensitivity to the assembly alignment of the TX and RX chips [4], [8], [12], [16], [18]–[22]. Table 2-1 shows a comparison of various magnetic coupled GI topologies, which illustrates the disadvantages of stacked coupling.

2.1.2 Lateral Coupling

To circumvent the limitations of stacked magnetic coupling, this work proposes lateral magnetic coupling. In this method, the oxide thickness between the two inductors (t_{ox}) is not limited by the process's IMD thickness and is instead determined by the horizontal spacing of the inductors [1], which can be adjusted by the layout, as illustrated in Figure 2-2 (c). Table 2-1 also illustrates the various advantages of lateral coupling compared to other magnetic coupling architectures, including its ability to use standard CMOS fabrication and packaging.

2.1.3 Resonant Coupling

In an inductively coupled system, the voltage gain from the TX to RX is determined by the magnetic coupling strength. Because the coupling factor in laterally coupled inductors is weaker than vertical (stacked) coupling [53], this work resonantly couples inductors to maximize the signal strength from the transmitter to the receiver. Figure 2-2(d) illustrates

a weakly-coupled transformer with a primary and secondary having a coupling factor of k, equivalent inductance of L, the series resistance of R, and quality factor of Q, resonated with a shunt capacitance of C. Voltage gain (V2/V1) of a non-resonant transformer is equal to its coupling factor k. When resonated, it can be shown that resonance will increase the transformer's voltage gain to more than k. The voltage gain, A(s), for the resonant magnetically coupled system in Fig. 2(d) is derived as follows.

Voltage gain for a circuit network can be derived using Z-parameters as shown in (1).

$$A=\frac{V2}{V1}=\frac{Z_{21}}{Z_{11}} \tag{1}$$

For the resonant coupled system in Figure 2-2(d) Z-parameters can be derived similarly to derivations in [54]. Z_{21} and Z_{11} can be derived as (2) and (3).

$$Z_{21}(s)|_{s=j\omega}=\frac{j\omega kL}{(1+j\omega RC-\omega^2LC)^2-k^2\omega^4C^2L^2} \tag{2}$$

$$Z_{11}(s)|_{s=j\omega}=\frac{(R+j\omega L)(1+j\omega RC)+j\omega C\left[\omega^2L^2\left(k^2-1\right)+j\omega RL\right]}{(1+j\omega RC-\omega^2LC)^2-k^2\omega^4C^2L^2} \tag{3}$$

Using (1-3), the closed form equation for A(s) can be derived as (4):

$$A(s)|_{s=j\omega}=\frac{j\omega kL}{(R+j\omega L)(1+j\omega RC)+j\omega C\left[\omega^2L^2\left(k^2-1\right)+j\omega RL\right]} \tag{4}$$

At resonance frequency of $s=j\omega_0$, (1) can be simplified and re-written as (2) for the voltage gain at the resonance frequency.

$$|A(s)|_{s=j\omega_0}=\left|\frac{V_2}{V_1}(j\omega_0)\right|\cong kQ \tag{5}$$

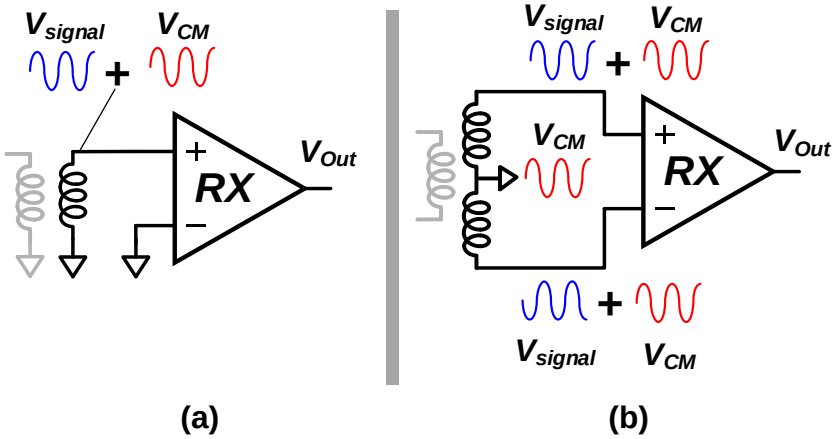

Figure 2-3Transformer Coupled GI receiver (a) Conventional single-ended, and (b) Center-tapped differential architecture (this work

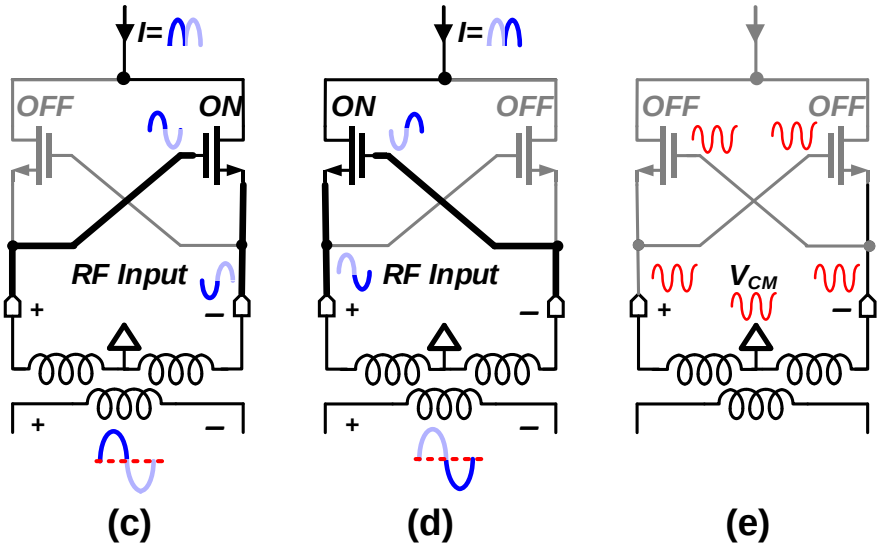

Figure 2-4 Operation of the proposed full-wave rectification RF receiver's input stage utilizing two differential gate-source coupled half-wave rectifiers during: (c) differential positive half-cycle rectification (d) differential negative half-cycle rectification

it can be seen that resonant coupling significantly boosts voltage gain of a magnetic coupled structure when compared with the same structure prior to resonance.

2.1.4 RF Energy Detector Receiver

Conventional GI transceivers Figure 2-3(a), uses a single-ended topology which is prone to common-mode (CM) transients and limited receiver sensitivity, as these structures only rely on high-pass filtering at the receiver's input to attenuate noise. This work uses a center-tapped transformer-coupled architecture in combination with a differential RF detector circuit, as depicted in Figure 2-4(b). Since the center-tap of the transformer's secondary winding is connected to RX chip's floating ground, common-mode transients due to ground fluctuations (Figure 2-1(d)) will appear on both the positive and negative terminals of the differential detector and therefore be rejected.

The implemented receiver in this work uses a differential RF rectifying input stage that converts the received RF energy into a current that is detected using a current comparator. Typical diode-based detectors have poor input signal sensitivity [9], [55], and as all of these solutions are inherently single-ended, thus are vulnerable to common-transients present in GI systems. Unlike prior art that uses diode-based or conventional common-source or common-gate topologies for their input stage, this work proposes an input that couples the RF signal through both the gate and source of each of the RF input transistors. This input stage is shown in Fig. 2-4(c)-(e) during different modes of operation. This topology is different from a standard differential amplifier (e.g., LNAs) because a differential input signal is seen across the gate and source of *each* transistor, as illustrated in Fig. 2-4 [56], [57]. The cross-coupled pair forms two half-wave rectifying transistors that together enable full-wave rectification (Figure 2-4(c), (d)) while rejecting common-mode transients

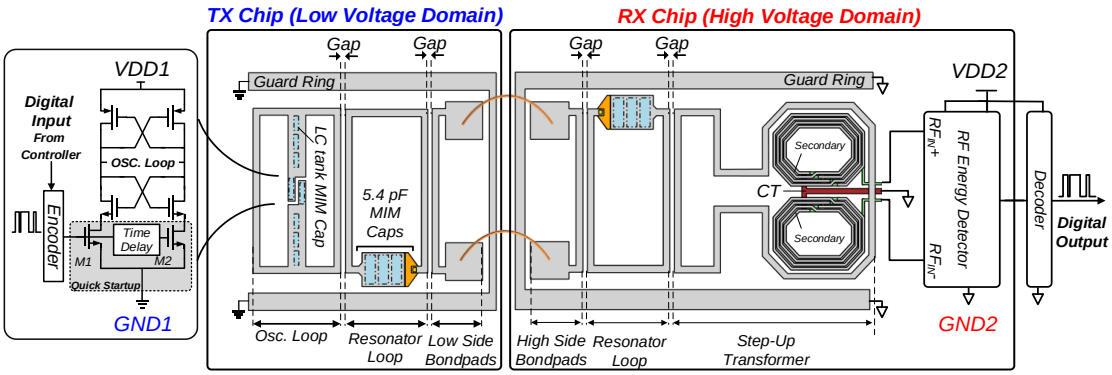

Figure 2-6 Block diagram of the implemented Laterally Coupled Galvanic Isolator

(Figure 2-4(e)). Furthermore, in this topology, the presence of CM signals doesn't increase the current consumption. Therefore, the system maintains its efficiency during CM rejection and achieves high CMTI without requiring additional power-consuming interference cancellation circuitry, thus minimizing the system's circuit complexity and maximizing its efficiency.

2.2 Design and Implementation

2.2.1 Architecture Overview

The concept of resonant lateral coupling introduced in Section 2-1 has been implemented in the presented GI system depicted in Figure 2-5. The system includes two chips connected together through two bondwires. The transmitter chip (TX Chip) is a low voltage die (connected to VDD1 and GND1) that can be integrated with the microcontroller. The receiver chip (RX Chip connected to VDD2 and GND2) can be integrated with high voltage circuitry and is prone to high-voltage transients through GND2's fluctuations. VDD1 and VDD2 supplies are generated to be 5 V with reference to GND1 and GND2, respectively.

The oscillator on the TX Chip serves as a transmitter and generates an RF voltage oscillating at 2.8 GHz. Magnetic coupling between the Oscillator (Osc.) Loop, Resonator Loop, and an inductor connected to the Low Side Bondpads transfers the oscillator signal to the bondpads of the Low Voltage (TX) Chip. Bondwires transfer the signal from the Low Voltage Chip to the High Voltage (RX) Chip. On the High Voltage Chip, the RF signal is coupled to the primary coil of a center-tapped step-up transformer through a Resonator Loop. The output of the transformer delivers a differential signal to the RF Energy Detector and is resonated with the receiver's input capacitance. To maximize the system coupling, all of the resonant structures resonate at the same frequency [58]. The system is implemented using a fully differential topology to maximize CMTI [15].

2.2.2 Transmitter Circuit

The oscillator uses an NMOS-PMOS cross-coupled architecture [59], where the output LC tank consists of the inductance formed by the Osc. Loop and a combination of parasitic capacitance from the cross-coupled active pair and MIM capacitors. This technique ensures that the generated RF signal's frequency always matches the communication channel's resonance frequency [15]. The digital input control signal turns the oscillator ON and OFF to modulate the generated RF signal. The oscillator is controlled through the switch transistors M1 and M2. In order to accelerate the oscillator's kick-off, a short delay cell has been implemented on M2's gate path, which causes M1 to turn on slightly before M2 and create a quick startup condition for the oscillator. This fast transmitter kick-off shortens the propagation delay from the system's digital input to digital output.

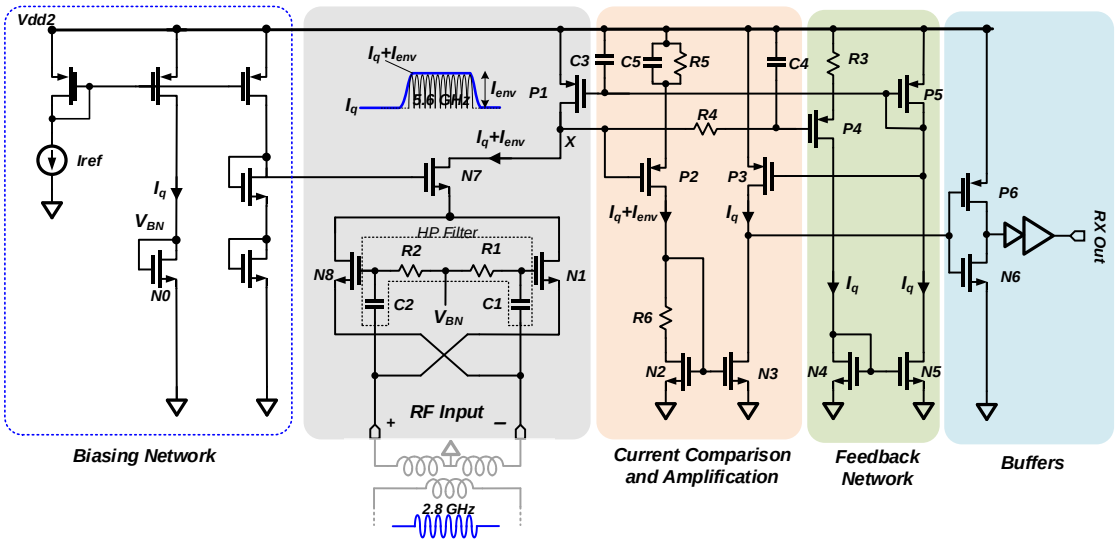

Figure 2-6 RF Energy Detector receiver schematic

2.2.3 Isolation through Lateral Oxide Gaps

Adding each Resonator Loop increases the number of Gaps by one, thus enhancing the system's isolation capability and reliability. Since the breakdown voltage of an insulator is directly proportional to the oxide thickness, increasing the thickness (Gap width or number of Gaps) increases the isolation rating. This design uses a Gap width of 3 µm. The multiple resonant structures in the architecture act as bandpass filters, thus increasing system noise immunity. The DC transient energy (and its harmonics) that appears on the GI's High Voltage ground (GND2) resides in the MHz frequencies, thus requiring narrowband filtering to remove this noise [15] [9].

2.2.4 Center-tapped Solenoid Step-up Transformer

The center-tapped transformer provides passive voltage gain for the RF Energy Detector receiver, thus reducing the power consumption and gain specifications required by the

receiver and alleviating the need for a low noise amplifier (LNA). The transformer also provides additional isolation through the oxide separating its primary and secondary coils. A floating ground connection to the transformer's center tap causes any DC transients to appear as a common-mode to the differential receiver for enhanced common-mode rejection and protection for the receiver's input devices against large transients.

One of the disadvantages of monolithic transformers is their occupied die area. In this work, a solenoid structure similar to [60] has been utilized with the advantage of using windings in multiple metal layers to achieve double the turns ratio within the same chip area compared to single-layer windings. The secondary coil inductors consist of 8 turns, four on the top metal, and four on the lower level metals, with the lower metal layers connected together to reduce sheet resistance. The transformer's secondary coil differential output is loaded and resonated by the receiver's capacitive input impedance [15].

2.2.5 RF Energy Detector Receiver Circuit

The RX architecture of Figure 2-6 is implemented to achieve low-power RF detection with high resiliency against noise and common-mode transients while exhibiting high sensitivity and short propagation delay. The presented circuit consists of four main stages. The input stage consists of a differential full-wave rectifier that receives the RF energy from the center-tapped transformer and converts it to a current that is proportional to the envelope of the received RF signal (I_{env}). Using a rectifier input stage with its gates biased at threshold voltage enables low power consumption and high receive sensitivity. The current during RF reception (I_q+I_{env}) is compared with the reference current (I_q), which is the quiescent current during idle mode. This difference (I_{env}) is amplified in the Current

Comparison and Amplification Stage and delivered to the last Buffers Stage that buffers the digital signal to drive an external off-chip load.

2.2.6 RF Input Stage and Envelope Tracking

The receiver input terminals are connected to the sources of N1 and N8, and are capacitively cross-coupled via C1 and C2 to their gates, thus forming a rectifying full-wave differential input pair, with N1 and N8 conducting the negative and positive half-cycles of the received RF signal. This results in a full-wave rectified current that has a frequency of 5.6 GHz, which is double the carrier frequency. The RC parasitics and the limited frequency response of transistors P1 and N7 provide a low-pass frequency response at N7's drain node (Node X). This low-pass response filters the rectified current to provide an envelope current, I_{env}. Since the RF detector's input pair is cascaded by N7, the presence of an RF signal increases the current of N7 from its quiescent value (I_q) to a total of I_q+I_{env}. The total current of N7 is compared with its quiescent value, I_q, using the comparator circuit.

2.2.6.1 Current Comparison and Feedback Network

The reference DC quiescent current (I_q) is generated by the Biasing Network shown in Figure 2-6. This quiescent current is mirrored through current mirroring between N0 and input transistors N1 and N8. The V_{ds} of N7 is biased at $I_q \times R3$ + (P4's V_{gs}) through the feedback network transistors P4 and P5. In idle mode, the feedback network also regulates the comparator's input transistors (P2 and P3) to their threshold voltage in order to increase the RX sensitivity and minimize the power consumption. A higher RX sensitivity also

reduces the propagation delay since a fewer number of RF input cycles are needed to build up a voltage above the RX detection level.

The increase in N7's current is amplified in the second stage using the implemented current comparator. The current comparator inputs are formed by the gates of P2 and P3. P2 and P3 are both regulated to have a current of I_q, however upon RF reception, P2's current is allowed to increase due to the high-pass filter response formed by R5-C5, while P3's current is maintained at I_q. Hence, the Feedback Network ensures that the current comparator always compares the change in the current due to the RF signal (I_{env}) with the quiescent current value (I_q). The current amplification of the envelope signal is performed through transistors N2 and N3. When an RF signal is applied, I_{env} increases the current through N2, and N2 enters the triode region. This creates a current amplification between N2 and N3, where N3 remains in saturation. The current to voltage conversion is performed in the comparator's output stage formed by transistor's P3 and N3. This stage is directly connected to the digital buffer stage.

2.2.7 Digital Buffering

The voltage output of the current comparator is provided to an inverter to create a digital output. The inverter is subsequently followed by buffering inverters to provide driving capability for driving either the input capacitance of the oscilloscope or off-chip decoder circuit.

2.2.8 Noise Reduction Mechanisms

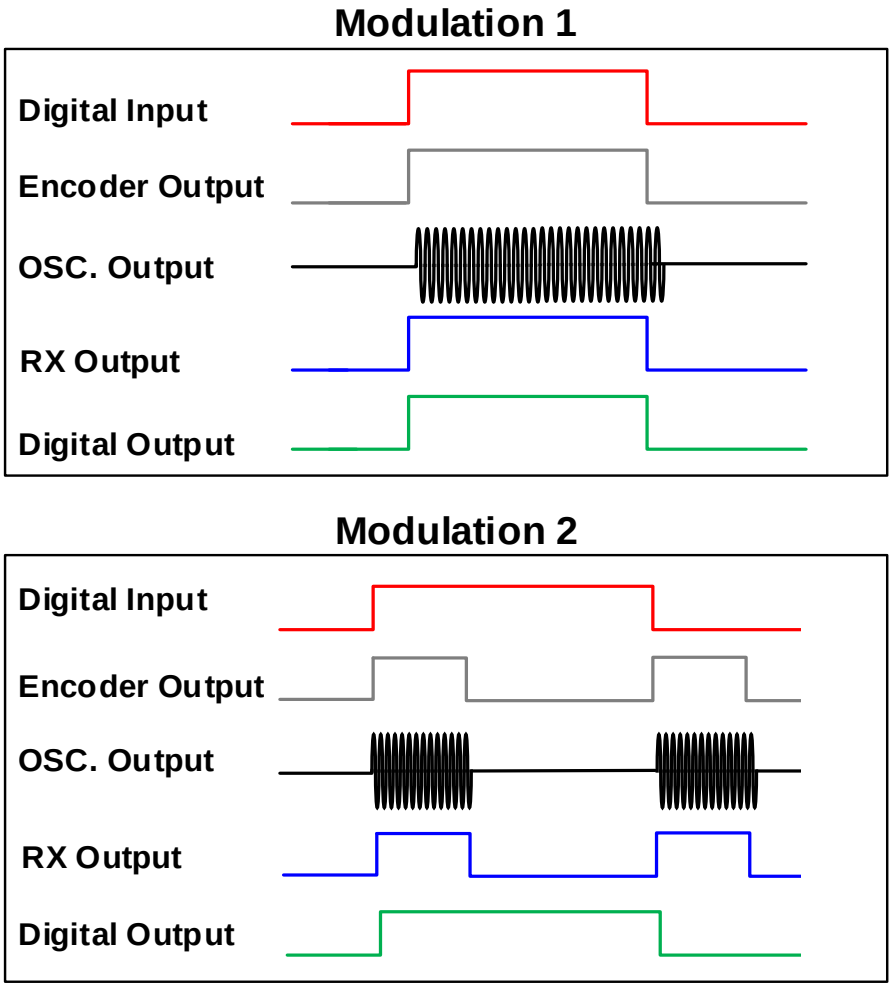

Figure 2-7 Digital to RF Modulation Schemes

The presented GI is designed to be resilient against both common-mode noise and differential noise (e.g. due to mismatch in CM noise path) to ensure that the RX Chip won't detect noise as received signals and interpret them as a data change. This system implements the center-tap transformer coupling and differential gate-source coupled RF detector concept presented in Section 2-1 to enhance CMTI. Furthermore, the band-pass filtering due to the narrowband nature of the resonantly coupled communication channel

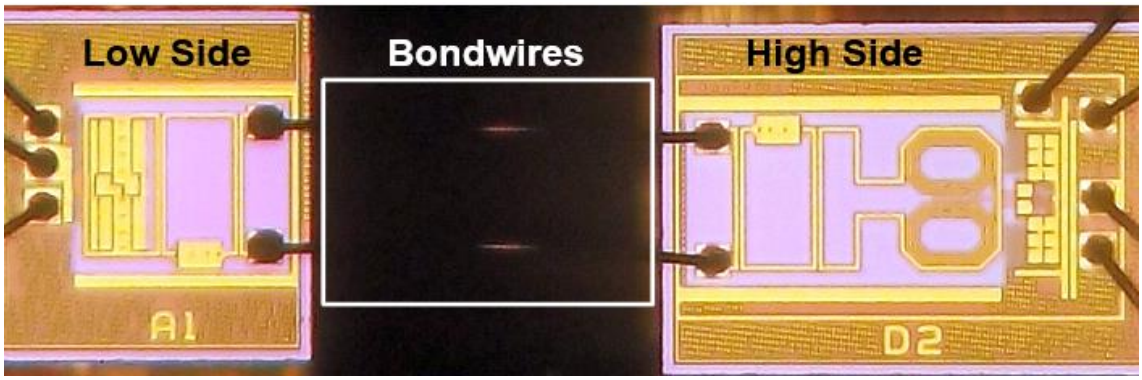

Figure 2-8 System Module Micrograph with High Side and Low Side Chips Assembled together in a SOIC-16 Wide Body Package

provides attenuation to any differential out-of-band noise. The system's symmetry also diminishes the mismatch in the CM noise path. The RF Energy Detector receiver structure also incorporates an input high-pass filtering formed by R1-C1 and R2-C2, which provides an additional layer of immunity to any differential or common-mode low-frequency noise seen at the receiver's input.

2.2.9 Digital-to-RF Modulation

Two modulation schemes based on OOK (ON-OFF keying) have been implemented to convert the digital (data) control signal to an RF communication signal. Figure 2-7 illustrates these two schemes. In Scheme-1, the oscillator is ON when the digital control signal is high, and the oscillator is OFF when the digital control is low. The receiver detects the envelope of the received RF waveform and recreates the control signal's waveform. Scheme-1 is optimum for higher data rates. In Scheme-2, an edge detector on the oscillator's input detects the digital control signal's rising and falling edges and turns on the oscillator only during these events, thus reducing power consumption significantly. However, the speed is limited in Scheme-2 because two pulses are created, one for each

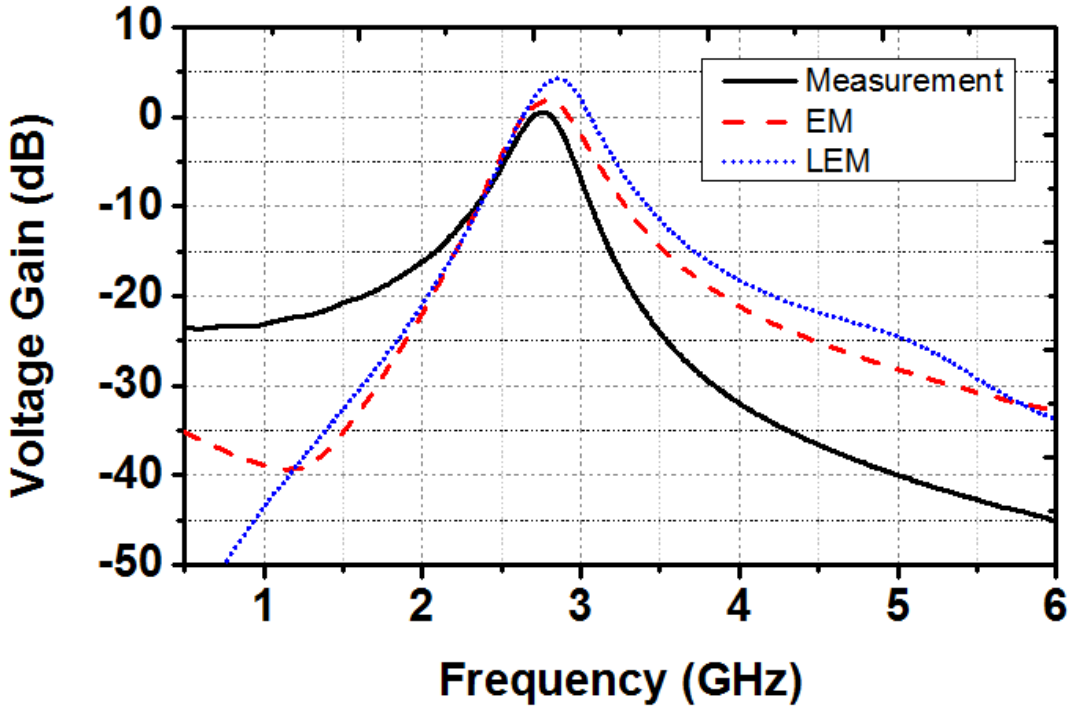

Figure 2-9 Measured and Modeled High Side Chip Signal Voltage Gain (|Z21/Z11|) From the High Side Chip Bondpads to the Transformer's Single-ended Output.

edge. These two modulations allow for a frequency detector to adaptively switch between Scheme-1 and Scheme-2, depending on the input data rate.

2.3 Fabrication and Measurement Results

The presented GI system is realized in a 0.25 µm CMOS process. The total area of the two chips is 0.95mm^2. The Low Voltage and High Voltage chips are assembled as a multi-chip module in a SOIC-16 wide-body package using a low-cost bond wire assembly solution (Figure 2-8). Test structures were implemented for both active and passive characterization. To achieve first-pass system design success, a combination of test

structure measurements, EM simulations, and a custom lumped element model (LEM) for the entire system was used to design and predict the transmitter-to-receiver channel's voltage gain, resonance frequency, and data rate (i.e., transient performance).

2.3.1 Passive Structure Measurements

The excellent correlation between EM and LEM simulation results and measurements is demonstrated in Figure 2-9, which plots the RX (High Voltage Domain) Chip's voltage gain over frequency. The measurement results show that a voltage gain higher than 0 dB is achieved at the operation frequency of 2.8 GHz, which proves that a laterally magnetic coupled channel may achieve low voltage attenuation. This result also shows that the implemented communication channel has inherent bandpass filtering due to the resonator-based structure. To achieve high accuracy, passive characterization, open and short on-chip de-embedding structures were fabricated for accurate calibration and de-embedding of the RF pads [61].

2.3.2 Process Variation Sensitivity

Multiple chips from different wafers (each from three different lots) were measured to study the sensitivity of the implemented system to process variation. The resonance frequency is used as the indicator of process variation sensitivity, and it is plotted for three different lots in Fig. 2-11(a). The results show less than ±0.3% sensitivity to process variation.

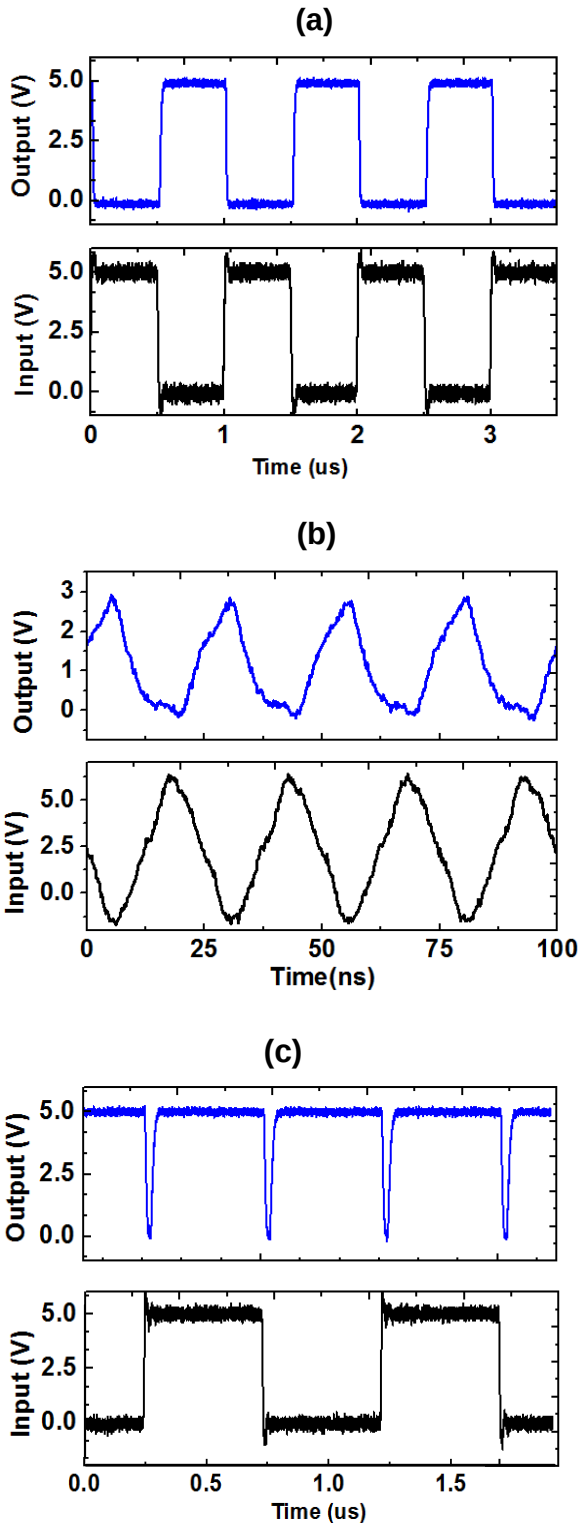

Figure 2-10 Full system digital input-output waveforms: (a) Scheme-1, 2Mbps, (b) Scheme-1, 80Mbps, and (c) Scheme-2, 2Mbps

2.3.3 Post-assembly Chip Distance Offset Sensitivity

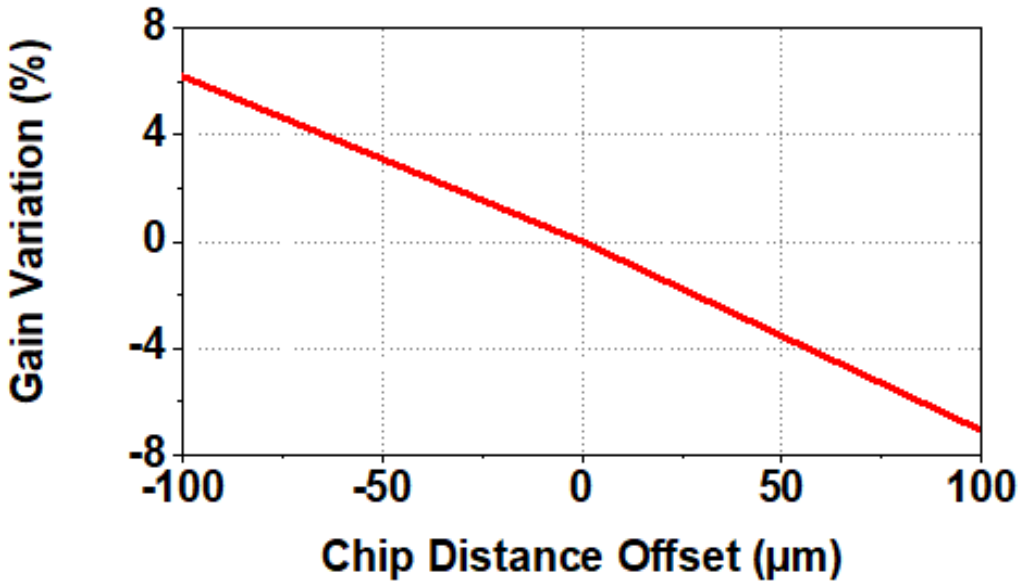

Figure 2-11 Simulation of voltage gain sensitivity to post-assembly chip distance offset

Chip assembly lines have process variation; therefore, the distance between the co-packaged TX and RX chips in Fig. 7 may vary between assemblies. This chip distance offset results in a change in bondwire length. The voltage gain sensitivity of the implemented system's communication channel was studied using a model developed from the passive structures' measurement results and EM simulations. Figure 2-11(b) shows the analysis result for the chip distance offset sensitivity, which demonstrates less than ±8% gain variation for a 200μm offset window and illustrates that the implemented channel is relatively insensitive to assembly errors.

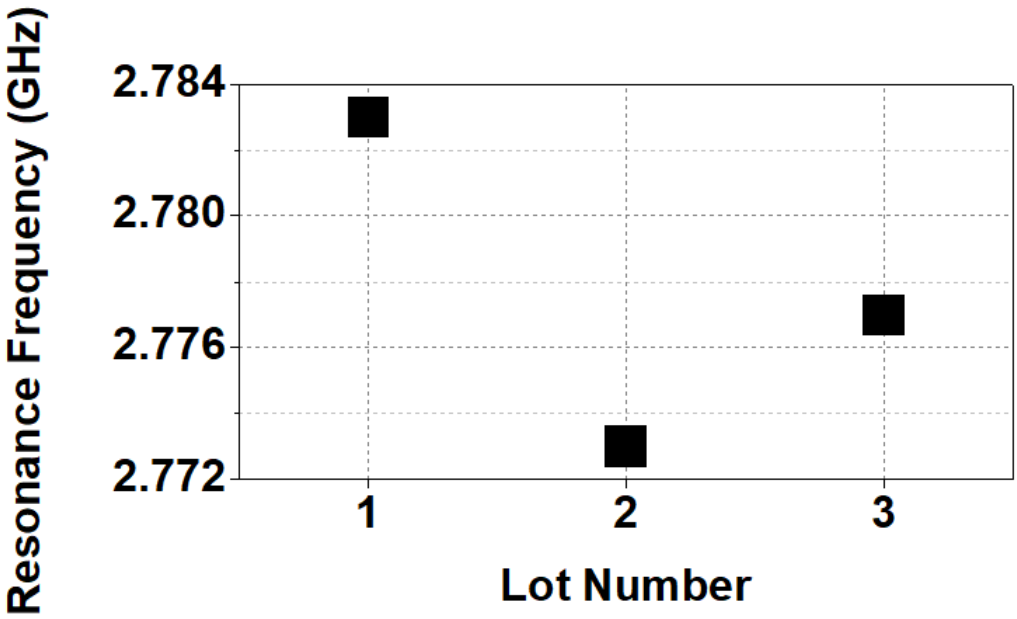

Figure 2-12 Process variation (Lot-to-Lot) of measured resonance frequency

2.3.4 Full-Channel Data Rate and Isolation Performance

System measurements for both modulation schemes show a maximum of 80 Mbps data rate from modulation Scheme-1 and up to 32 Mbps from modulation Scheme-2. Figure 2-10(a) and Figure 2-10(b) shows the measurement results for Scheme-1 at 2 Mbps and 80 Mbps, respectively. System measurements for Scheme-2 at 2 Mbps are given in Fig. 10(c). The encoder for Scheme-2 is externally implemented using a set/reset logic. The results confirm successful chip-to-chip communication, proving the functionality of the TX, RX, and the laterally coupled communication GI channel.

2.3.5 Propagation Delay

The propagation delay from the transmitter's digital control input to the high voltage receiver's output is measured as 13.6 ns for the 1-to-0 transition and 17.6 ns for the 0-to-1 transition, thus giving a typical propagation delay of 15.6ns. The simulation results estimate the rise and fall times to within 6% of the measurement results.

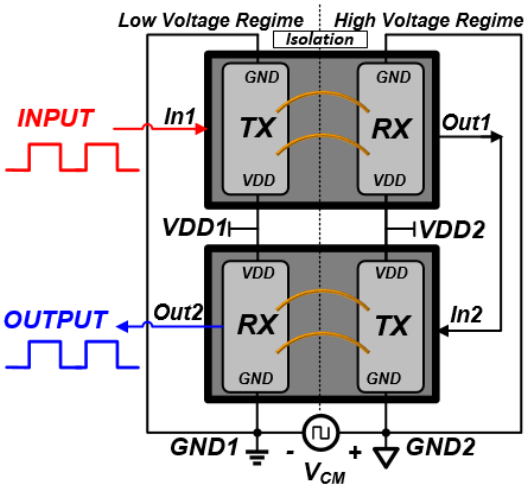

Figure 2-13 CMTI measurement confuguration

2.3.6 System Power Consumption

The receiver demonstrates a low power consumption of 0.23 nJ/b with less than 100µA quiescent current during idle mode and maintains a high sensitivity of 20 mV.

The TX has 6.58nJ/b power consumption. The measurements conclude that using Scheme-2 and reducing the transmitter's supply voltage significantly reduces the transmitter's DC power consumption. Up to 96% transmit power reduction is achievable using Scheme-2 over Scheme-1 for the same supply voltage. Reducing the TX VDD1 from 5 V to 3.5 V gives 50% power reduction for the same scheme. This implies that subsequent implementations may have significant power savings.

2.3.7 Common-mode Transient Immunity and Isolation Rating

A standard 1-minute dielectric breakdown stress test was done to measure the isolation capability of the implemented GI. The measurement results show successful durability of 5 kVpk (3.34 kVrms) for a 1-minute duration. CMTI was measured by applying HV transients with controlled slew rates across the grounds of the TX chip and RX Chip while

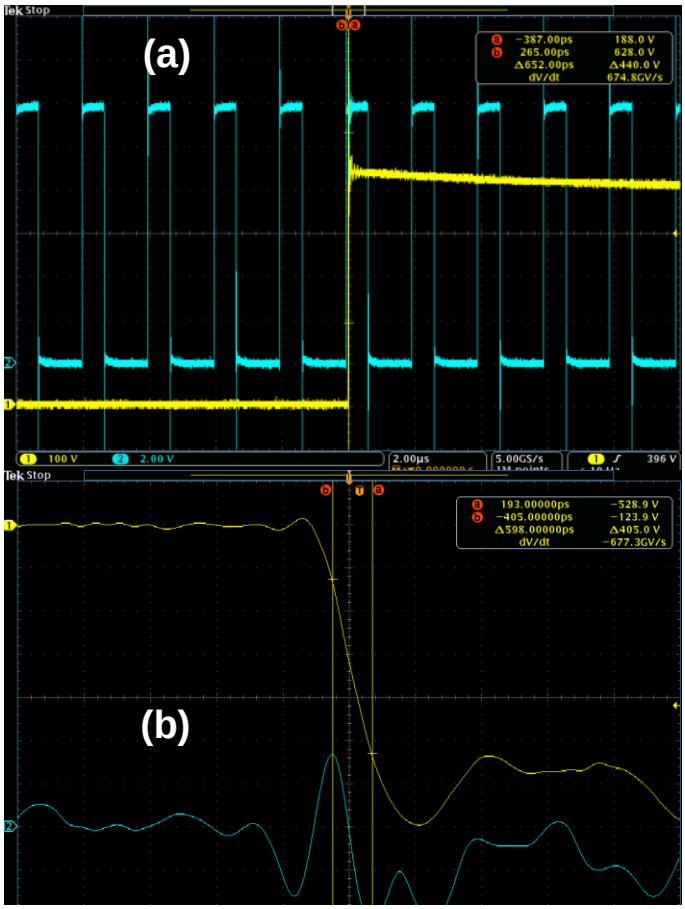

Figure 2-14 CMTI during (a) Rising-Edge (b) and Falling Edge

monitoring the digital output. The CMTI is recorded as the highest slew rate that doesn't affect the digital output value. The loop-back configuration [9] shown in Figure 2-13 is used for the measurements. In this setup, the common-mode transient (V_{CM}) is applied at GND2 while the digital output is monitored via an oscilloscope. Measurement results for CMTI are shown in Figure 2-14 shows a typical CMTI ~650 kV/µs HV from measurements.

TABLE 2-2 - RESULTS AND COMPARISON

Parameter	**This Work**	[51]	[52]	[21]	[18]
Isolation (kVrms)	3.34	3	3	3	3
$CMTI_{min}$ (kV/us)	**650**	35	100	65	10
Data Rate (Mbps)	80	100	150	25	10
Prop Delay (ns)	**15.5**	23	7.2	32	100
I_{RX}, 1Mbps (mA)	**0.1**	1.35	1.1	1.6	7
I_{Total}, 1Mbps (mA)	**1.9**	1.7	3.3	1.8	27
Standard CMOS	**Yes**	No	No	No	No
Insulation Material	**SiO_2**	Polyimide	Polyimide	SiO_2	Glass
Coupling Method	**Lateral**	Stacked	Stacked	Capacitive	Optical

2.4 Conclusion

The presented galvanic isolator solution uses the lateral on-chip spacing between resonant structures to reach 5 kVpk (3.3 kVrms) isolation from a standard foundry 4-metal layer process. The presented common-mode transient resilient RX combined with the laterally resonant coupled differential channel and center-tapped transformer enables a CMTI of 650 kV/us the highest reported to date, which is more than 6x times of the industry-leading products [21], more than 10x times the CMTI achieved from prior standard CMOS works [9], and two times higher receiver energy efficiency. These results demonstrate the efficacy of resonant lateral coupling technique and gate-source coupled receivers and demonstrate that when combined, these two methods can reach their full potential. Also, the presented results prove the superiority of lateral coupling over stacked coupling for CMTI enhancement. To the best of the authors' knowledge, this is also the first work that achieves 3 kVrms isolation using a non-altered standard CMOS process and packaging. The laterally coupled topology shows less than 8% per 100 µm chip alignment sensitivity, which is 4 times less sensitive than post-processing techniques [14]. The total silicon area, including low voltage and high voltage chips, was minimized to less than 0.95 mm^2, which is less than the smallest work reported to date[9]. Comparison of this work with state-of-

the-art GIs for applications with similar isolation (3 kVrms category) demonstrates (Table 2-2) that this work shows the highest CMTI, and one of the lowest RX and total current consumption, and propagation delay. These results are achieved even though this work uses only standard CMOS technology, with no post-processing methods. This work also demonstrates superiority over state-of-the-art optocouplers. The 80 Mbps data rate from this work allows it to be used for a wide range of applications, including isolating signal buses such as I^2C, CAN, full-speed USB, and industrial controllers. This work demonstrates a previously unexplored resonant lateral magnetic coupling application and presents a new RX architecture for low power, high CMTI RF detection.

CHAPTER 3

A Wide-Band Galvanically Isolated Bi-Directional Chip-to-Chip Communication

3.1 Introduction

In recent years, transformer magnetic coupled transceivers have emerged as an attractive solution for CMOS GIs. In the prior art, various single transformer solutions have been proposed to achieve high isolation rating and reliability, however at the expense of additional design and assembly steps, oversized chip area, high chip distance sensitivity or reduction of communication performance and energy efficiency[12], [14], [19], [22]. On

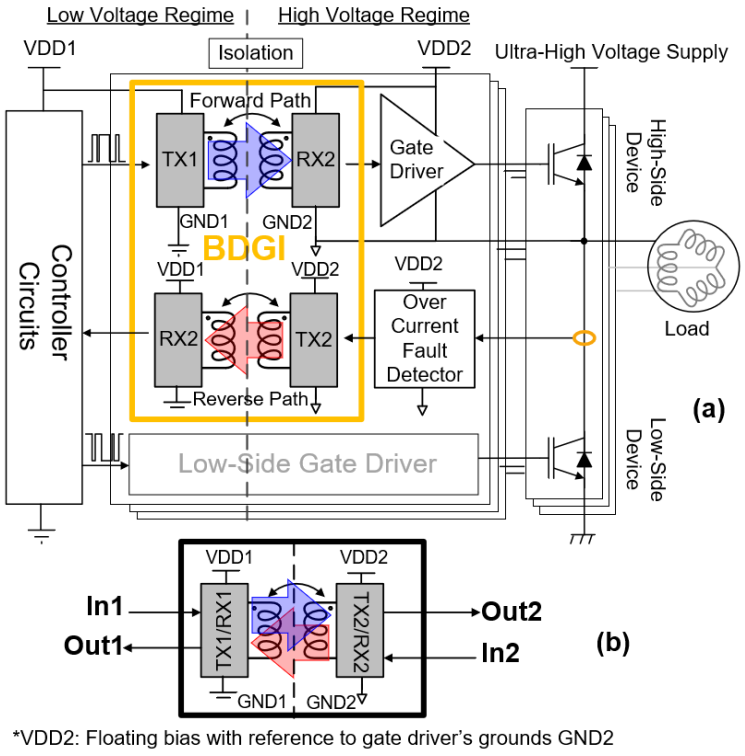

Figure 3-1 (a) Galvanically isolated Half-Bridge system using a conventional BDGI (b) Proposed BDGI using a Time-Division Duplex channel

the other hand, GI transceivers that have been proposed using ultra-wideband techniques for improvement of communication performance (data rate, propagation delay, energy efficiency) come short in offering high CMTI or isolation rating[9], [13]. Therefore a solution that can offer high isolation rating, communication performance, and CMTI at the same time is in high demand. Furthermore, Currently, BDGI products use two individual uni-directional isolators, with one isolator dedicated to the forward path signal flow and one dedicated to the reverse path, which provides a duplex solution that consumes significant area [62]. This work [16] proposes time-division-duplexing (TDD) realized with ultra-wideband (UWB) pulse polarity modulation (PPM) transceiver to merge the functionality of two inductively coupled channels into one inductively coupled channel between the two chips that can be used in both directions. The proposed system enables up to 50% form-factor and assembly cost reduction from existing topologies. This work also presents novelties applicable to both uni-directional and BDGIs, including a new high data rate, low power, and low propagation delay UWB transceiver architecture, and a double isolated transformer-coupled channel using two series-connected transformers to achieve state-of-art performance. To the best of our knowledge, this is the first time a UWB Bi-Directional Galvanic Isolator is implemented and reported.

Background and System Requirements

Figure 3-1 (a) shows one application of BDGIs in a CMOS power management solutions for power device (e.g. IGBT or GaN) gate drivers[9], [14], [15], [62]. In this application, a PWM digital control signal must be communicated from a low voltage die consisting of microcontrollers to an ultrahigh voltage die with gate drivers, and a fault detection signal

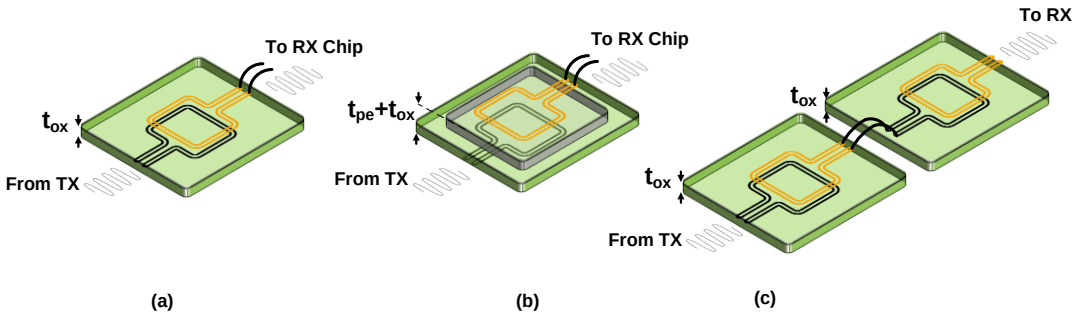

Figure 3-2 Magnetically Coupled GI topologies (a) Fully CMOS (b) CMOS with additional non-CMOS dielectric (Post-Processing) (c) Double-Isolated CMOS

TABLE I: MAGNETIC COUPLING TOPOLOGY COMPARISON SUMMARY

Topology	Double Isolated CMOS Fig 3(c)	Stacked Coupling Fig 3(a)	CMOS with Post-Processing Fig 3(b)
Insulation Material	SiO2	SiO2	Polyimide
Isolation Rating	2	1	> 1
Standard CMOS & Packaging	✓	✓	✗
IMD thickness Independent	✓	✗	✓
Alignment Insensitive	✓	✓	✗

from the high voltage die to the microcontroller (low voltage die) in the time of overcurrent or short circuit in the inverter circuit, while maintaining reliable DC isolation between the two chips. Short propagation delay is critical in this application to minimize the delay from the time a short circuit happens until the time that a shut-down command is performed to avoid any catastrophic failures. Furthermore, the harsh operation condition for isolated gate driver requires high common-mode noise resiliency, including common-mode transient immunity against the high-voltage transients across GND1 and GND2 and magnetic coupling noise from the ambiance of the circuit. Due to the omnipresent use of isolated

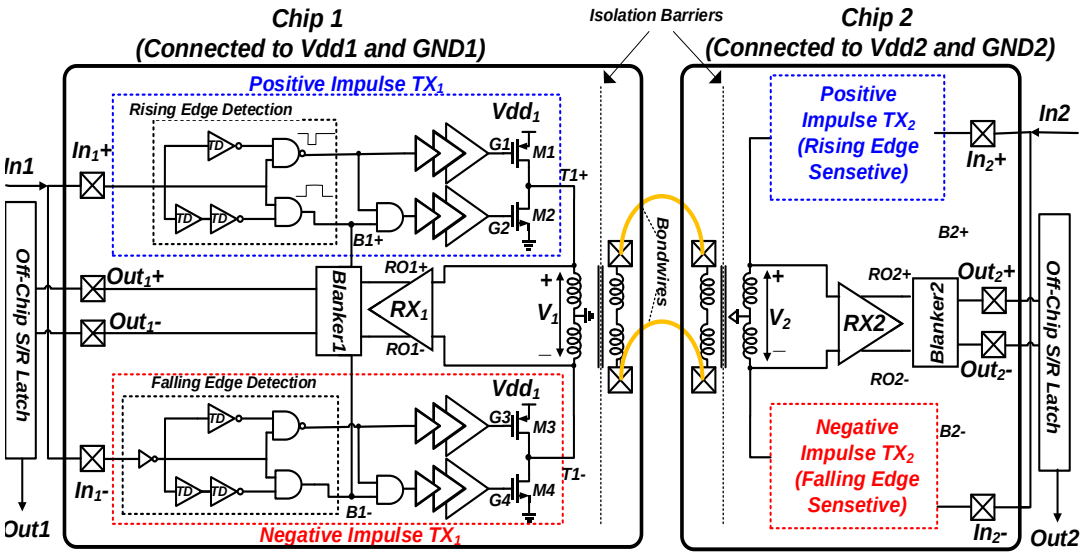

Figure 3-3 Implemented UWB BDGI

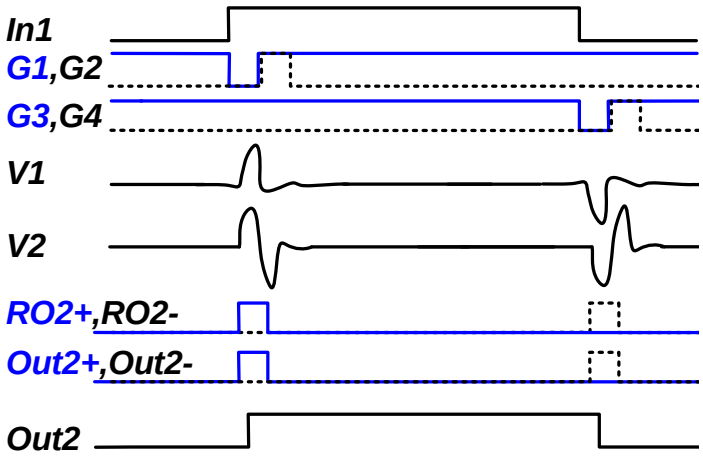

Figure 3-4 BDGI waveforms during communication from Chip 1 to Chip 2

gate drive inverters in consumer applications (e.g. air conditioner, electric vehicles, kitchen appliances, etc.) therefore, there is a high demand for low cost (associated with fabrication technology, area, packaging, and assembly) GI solutions that offer a high level of CMOS integration with microcontroller and gate drivers. Currently, BDGI products use two

individual uni-directional isolators, with one isolator dedicated to the forward path signal flow and one dedicated to the reverse-path, as shown in Figure 3-1(a), which consumes significant silicon area. To maximize the data rate, minimize the chance of interference, and also minimize the power consumption, a system that communicates with minimum transmission and reception time is desired for this application.

3.1.1 Proposed System

This work proposes a time-divided duplex implemented with a UWB transceiver (Figure 3-1(b)). As juxtaposition of the proposed solution and conventional solution in Figure 3-1 shows, TDD enables up to 50% area, and assembly cost reduction. UWB communication allows transmitting short narrow impulses, which allow minimizing the transmission time. Conventional GIs use narrowband transceivers; however, due to the fact that GIs integrated with gate drivers require high voltage fabrication processes with large process nodes, narrow band frequencies that can be generated are significantly less that the resonance frequency of the transformer coupling channel [9]. This causes a lower gain, and hence higher transmitting power to reach above the receiver's sensitivity. Furthermore, narrowband communication causes long voltage build-up times on the receiver side, which requires more cycles of RF power to be transmitted, increasing transmission time and propagation delay. Finally, a UWB GI transceiver not only enables shorted transmission time but also, due to its wide band, can utilize the maximum bandwidth of the transformer channel achieving again and speed higher than that of narrowband for the same transmitting power [9]. UWB communication, when combined with pulse polarity modulation, can also minimize Bit error rate and propagation delay.

3.2 Design and implementation

3.2.1 Architecture Overview

The implemented BDGI is depicted in Figure 3-3 and includes two chips connected together through two bondwires. Each chip consists of a differential coreless transformer with a center-tapped primary coil and a transceiver connected to the primary of the transformer. The two chips have identical architecture. The transmitter structure in Figure 3-3 is detailed on Chip 1, and the receiver is detailed on Chip2. Figure 3-4 illustrates the circuit waveforms during a uni-directional communication from Chip 1 to Chip 2. The transmitter encodes the input data (In1) rising edge and falling edge to a differentially positive and negative impulse, respectively (V1).The receiver (RX1) translates the received impulses (V2) to a short digital pulse on RO2+ upon detection of a positive impulse and a short digital pulse on RO2- upon detection of a falling edge. Blanker2 and Blanker1 are the self-interference cancellation units; here, because Chip 1 is transmitting, and Chip 2 is not transmitting, Blanker2 passes the data from RX2's outputs to the output pads. An off-

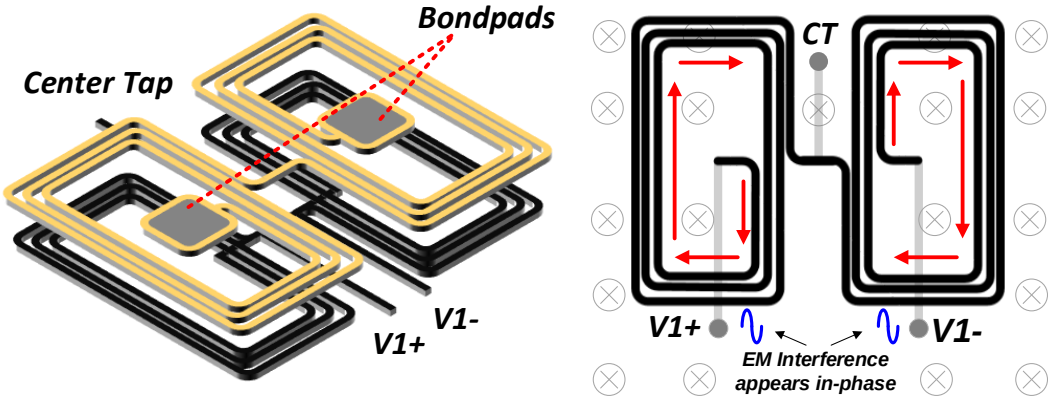

Figure 3-5 Center-tapped transformer

chip S/R latch decodes the received impulses (Out2). Since Chip 1 is transmitting in this example, during the transmission of Chip 1, Blanker1 ensures that Chip 1's outputs (Out1+ and Out1-) remain at zero and don't pass RX1's output to Chip1's outputs to cancel self-interference. Encoding the input data rising and falling edges too short impulses (UWB) minimizes the transmit and receive signal time length and also allows the channel to remain free as long as the data value remains unchanged, which is desirable for TDD. Additionally, UWB modulation reduces power consumption by shortening the transmission and reception time. Moreover, UWB pulse polarity was chosen over OOK and narrowband (single tone) communication methods because narrowband methods take more time for the transmitted and received voltage to rise above the receiver's sensitivity. Thus UWB PPM minimizes the propagation delay[4].

3.2.2 Inductive Coupled Channel: Double Isolated Transformer

To date, for realizing fully CMOS integrated magnetically coupled GIs, two stacked magnetically coupled inductors are used, and a high-voltage barrier is realized by the inter-metal-dielectric (IMD) oxide that fills the vertical interspace between the two inductors[9], [13], as shown in Figure 3-2(a). In this method, the CMOS process's IMD thickness is the bottleneck for the maximum achievable isolation rating [9], [13]. Methods such as inserting additional layers of thick dielectrics (e.g. polyimide or die-attach fill adhesives) between two inductors have been proposed (Figure 3-2 (b)) to increase the effective dielectric thickness for achieving a higher isolation capability [14]; however, at the expense of

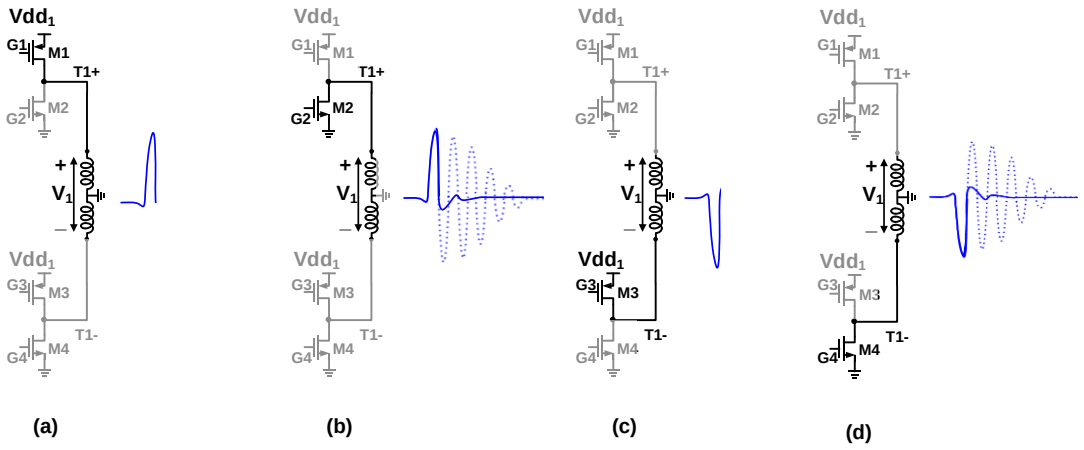

Figure 3-6 (a) Positive Impulse Generation (b) and its Accelerated Damping (c) Negative Impulse Generation and (d) its Accelerated Damping

requiring non-standard CMOS/packaging, alternating the native CMOS process, or increasing the packaging and assembly steps and large chip-to-chip gain sensitivity to the assembly alignment of TX and RX chips. In this work, a double isolated transformer is formed by connecting two stacked transformers in series through bondwires (Figure 3-2 (c)). Since Chip 1 and Chip 2 are connected through bondwires placed between the transformers' secondary coils (the sides that have bondpads), the two transformers are connected in series, realizing effectively two IMD barriers between the two chips and achieve two times the isolation rating of one transformer, without adding extra steps or alternating the native CMOS fabrication process as shown in Figure 3-2 (c). Table 2-1 provide a comparison between these three methods. Figure 3-5 shows one of the two transformers. The transformer's coils benefit from an odd-symmetry design that translates magnetic transients to a common mode electrical signal that is rejected by the differential receiver, thus increasing the CMTI and EMI of the circuit from an even-symmetry design.

The center-tap of each transformer is also connected to the ground of its respective chip to reject common mode transients coming from high voltage fluctuations of GND2 and eliminate ground loops.

3.2.3 Ultra-Wideband Transmitter

Detailed architecture of transmitter is shown in Figure 3-3 for Chip 1. Chip 2's TX is identical to Chip 1 and is depicted on a block level. The UWB transmitter on each chip consists of two branches: the positive impulse generator (connected to T1+ on Chip 1) that creates an impulse when detecting a rising edge at its input In1+, and the negative impulse generator (connected to T1-) that creates an impulse when detecting a falling edge at its input In1-. The logic circuit at the input of each transmitter branch generates two non-overlapping signals upon detection of their respective activating edge (G1-G2 at rising edges and G3-G4 at falling edges). These signals control the PMOS-NMOS output stage (M1-M2 and M3-M4) connected to the transformer. The transformer's inductance acts as a UWB pulse-shaping filter. Since the transformer is center-tapped, either a differentially positive or negative impulse is generated across the transformer input (V1 in Figure 3-4). Each transmitter creates an impulse by turning on and off its corresponding output stage's PMOS switch (e.g. M1), which can cause a slowly decaying ringing accompanying the generated impulse. To eliminate this ringing, the output stage's NMOS device (e.g. M2) is therefore turned on immediately after the PMOS turns off to accelerate the signal damping. This allows an immediate Q reduction of the parallel RLC formed by the transformer and its parasitic capacitance, which enables a fast damping action. This technique releases the channel for the reception (high impedance mode) faster than the

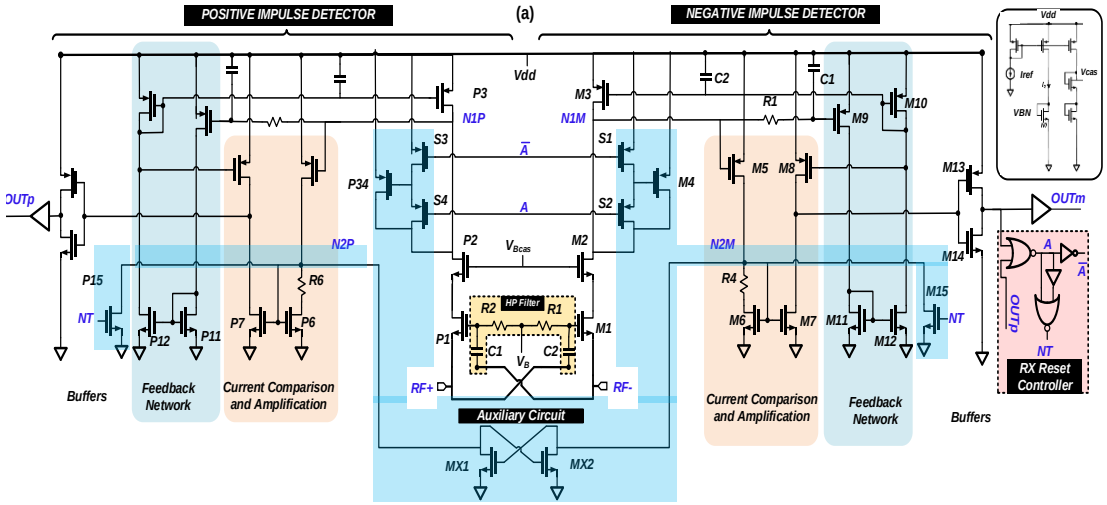

Figure 3-7 RF Detector Circuit Schematic

slow current control introduced in [9] and can therefore attain higher data rates. Figure 3-6 shows the operation of the transmitter at different phases in addition to the transmitted wave shape in the absence of the fast damper.

3.2.4 Receiver

A reliable GI not only should offer high isolation capability but also should be able to maintain reliable communication during harsh operation conditions. To enable a low-power RF detection with high resiliency against noise and common-mode transients, high sensitivity, and short propagation delay, the RX architecture of Figure 3-7 is used, where the circuit consists of a biasing network and four main stages. The circuit consists of a positive impulse detector unit and a negative impulse detector unit. The center-tapped transformer from the communication channel in Figure 3-3 is connected to the first stage, which is the RF input stage of the receiver. The input stage consists of M1 and P1, which work as the input stage for the negative and positive impulse detector, respectively, with

their gates and sources cross-coupled to the transformer's differential input and biased close to the transistors' threshold voltage. Since the input devices are connected in opposite polarities to the input and biased, each will conduct only one polarity of the differential signal at the time. During the reception of a positive signal, only P1 conducts, and during the reception of negative signals, only M1. During common-mode operation, the signals appear in phase on both gate and source of each transistor; therefore, both transistors remain off, and neither will conduct nor amplify the common-mode signal. The operation of feedback and comparator circuits is identical to that of chapter 2. Since the received signals are accompanied by a counter pulse and fast settling ringing, the MX1 and MX2 are connected to the circuit in order to sequence the received signal. As soon as a negative (positive) impulse is received, the MX pair latches node N2P (N2M) to the ground, preventing the counter impulse detection. As soon as the output began shaping at outm and outp,a feedback signal to switches S1,2 (or S3,4) blocks the input and node N1M and N1P from a change of status until the output is back to zero, therefore rejecting any ringing. After a determined delay (generated by the Reset controller unit) M15 and P15 reset the circuit and return the circuit to reception mode.

3.2.5 Blanker

A blanker unit (Figure 3-8) is placed between the receiver outputs (RO+ and RO-) and the chip’s outputs (Out+ and Out-) to mute the chip’s receiver outputs during data transmission and avoid self-interference from the chip’s transmitter. The blanker is triggered on the rising edge of the blanking input (OR a combination of B+ and B-) and

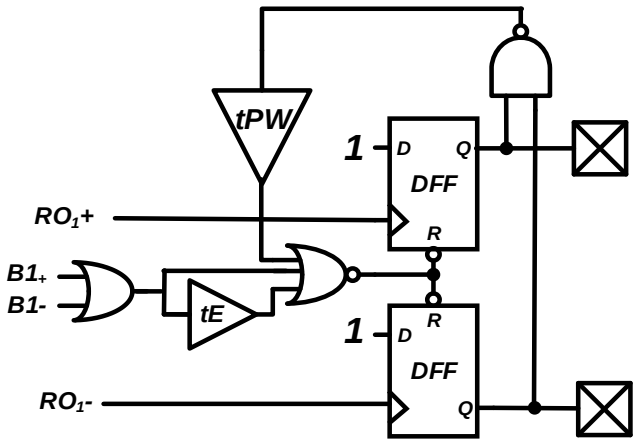

Figure 3-8 Blanker circuit

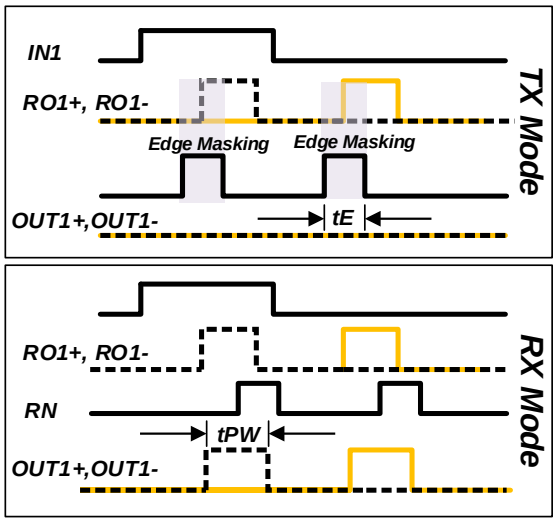

Figure 3-9 Wave forms for Blanker circuit

mutes the output for a total time of TE. The TPW delay set the output pulse widths for each received impulse and was designed to be long enough for the pulses to be detected using an external decoder (e.g. SR latch). Digital Buffering

The voltage on the output of the current comparator is provided to an inverter to create a digital output. The inverter is subsequently followed by buffering inverters to provide

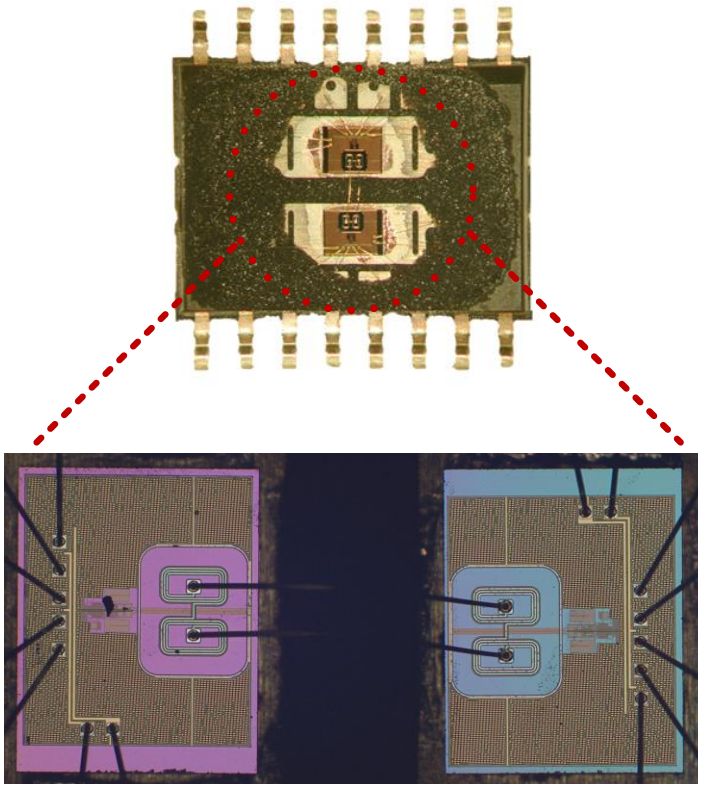

Figure 3-10 System module micrograph with chips assembled together in a SOIC-16 Wide Body package

driving capability for driving either the input capacitance of the oscilloscope of the detector circuit.

3.2.6 Noise Rejection

Noises in this system can come from two sources: electrical coupling to GND2 or magnetic coupling to the transformer. Conventional transformer-coupled GIs use single-ended topology [9], [13], [14], as shown in Figure 2-3(a), which is prone to both magnetic and common-mode transients. This work uses a center-tapped topology in conjunction with the presented RX circuit, as shown in Figure 2-3 (b). The center-tapped topology ensures that

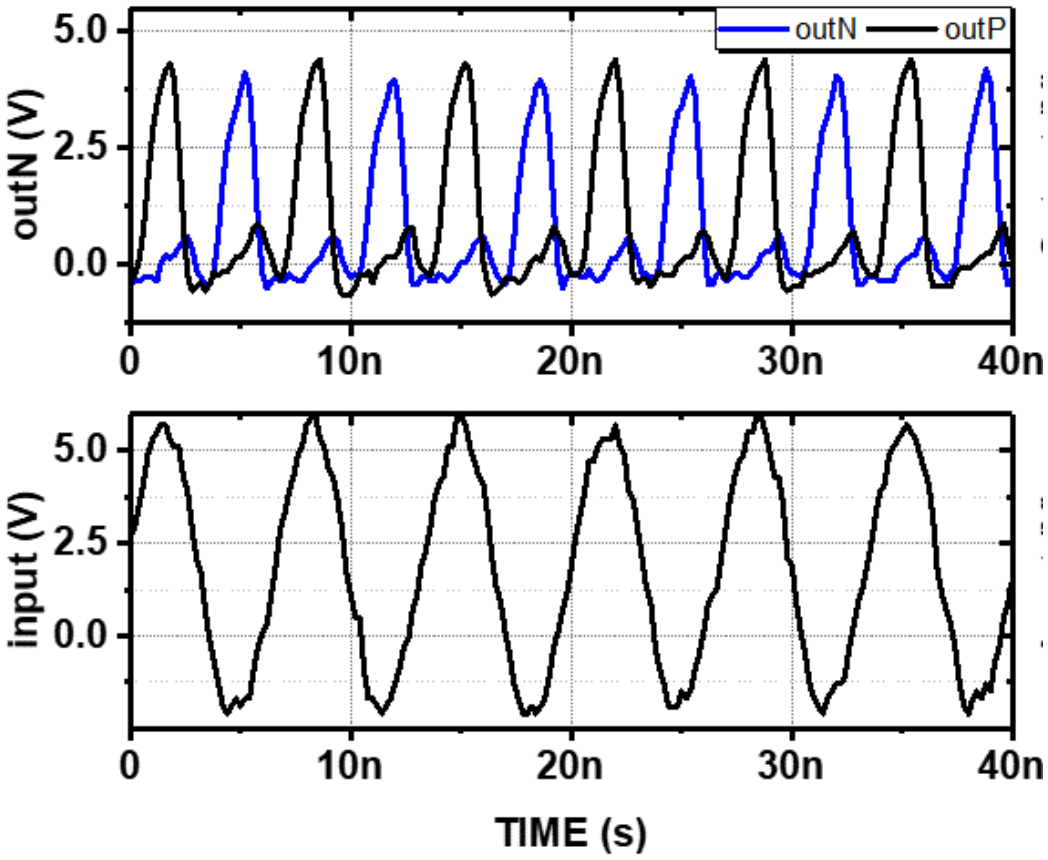

Figure 3-11 Measured uni-directional communication from Chip 1 to Chip 2 at 300 Mb/s

the noise from the GND2 is seen as a common-mode signal at the RX input and thus rejected. The odd-symmetric design of the transformer ensures both dotted heads are connected to the center-tapped, and subsequently, common-mode magnetic noises will be translated to common-mode electric signals rejected at the receiver's input. The high-pass filter at the RX input ensures further suppression of noise to achieve a higher common-mode transient immunity

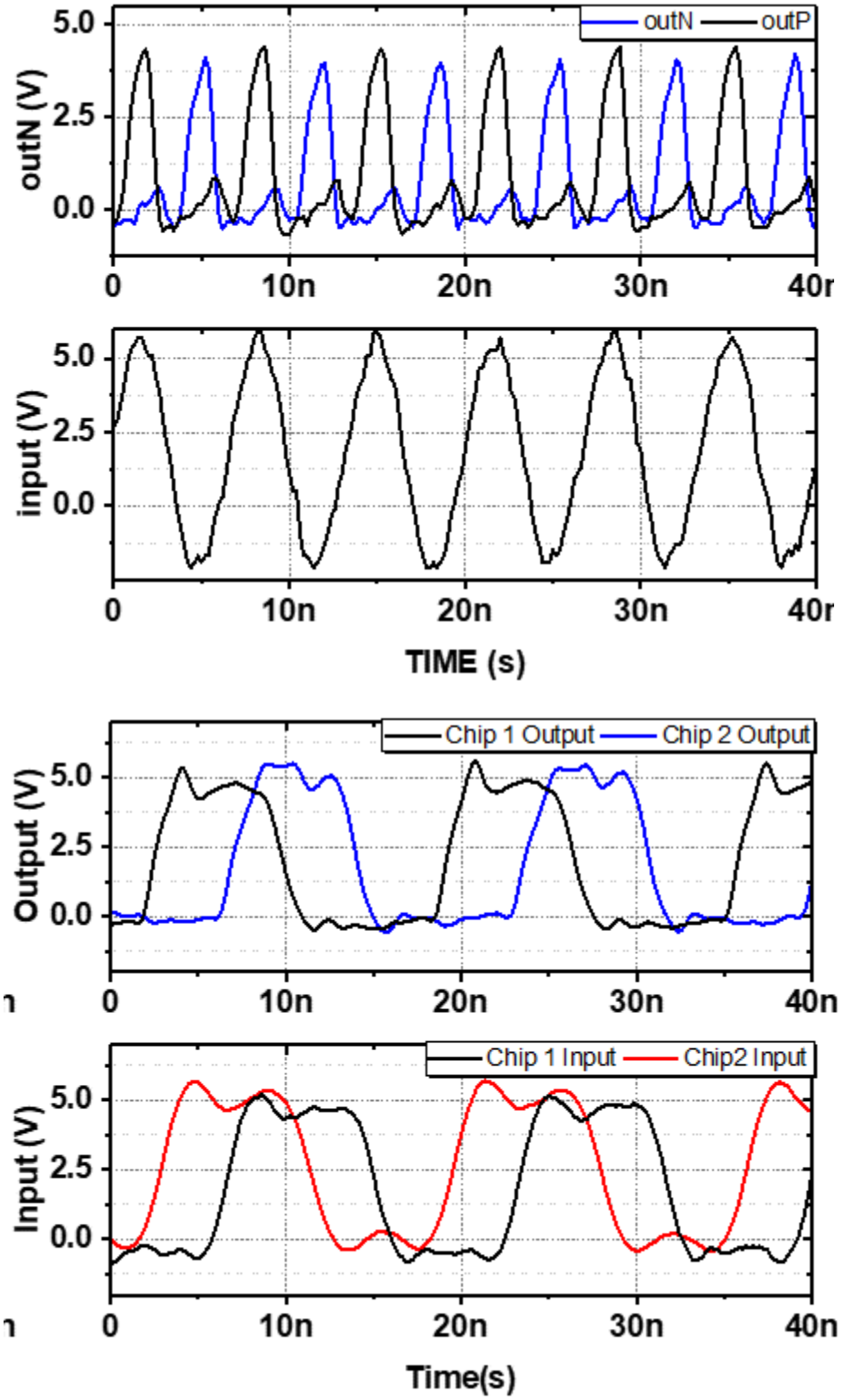

Figure 3-12 Measured bi-Directional interleaved performance at 136 Mb/s

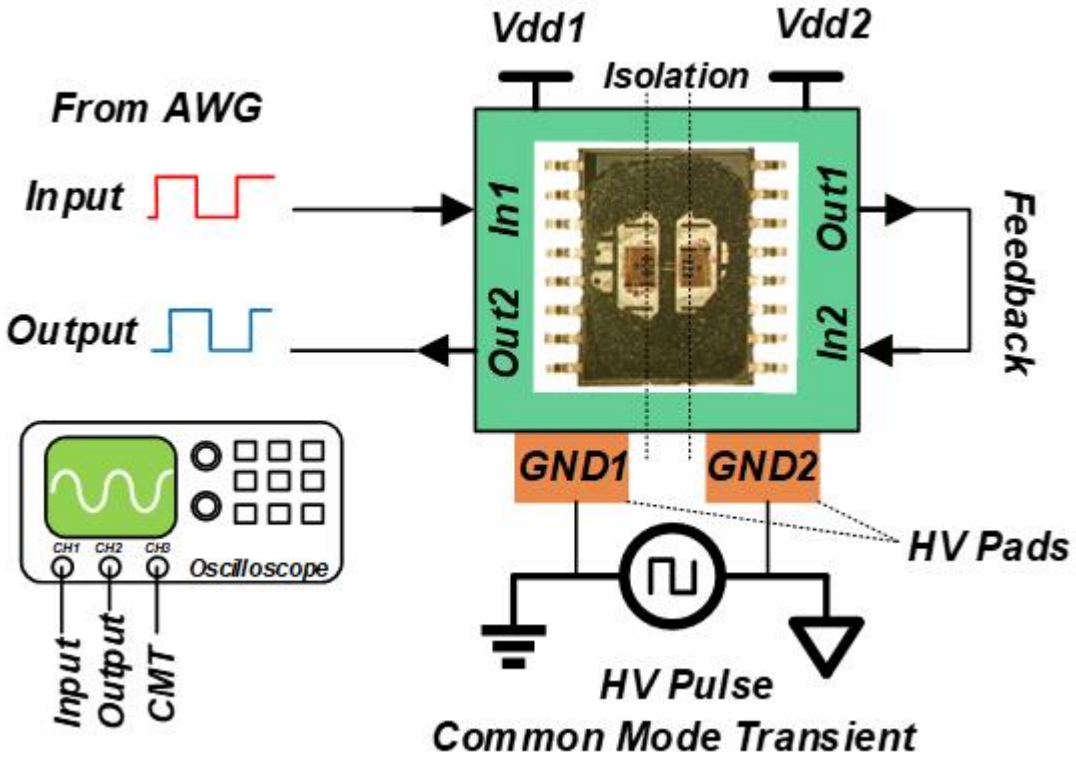

Figure 3-13 CMTI Setup

3.2.7 Independent control of Positive and Negative Impulse Transmitters

The positive and negative impulse transmitters can be controlled independently. In Figure 3-3 they are shorted together at the input to automatically encode input data edges to PPM impulses. This independent control provides flexibility to the user to implement modulations other than PPM. Moreover, since two consecutive positive or negative impulses will not be interpreted as a data value change, they can be used to transfer protocol/scheduling information. Furthermore, in control applications requiring fault detection, a rising edge can be sent multiple times for higher reliability

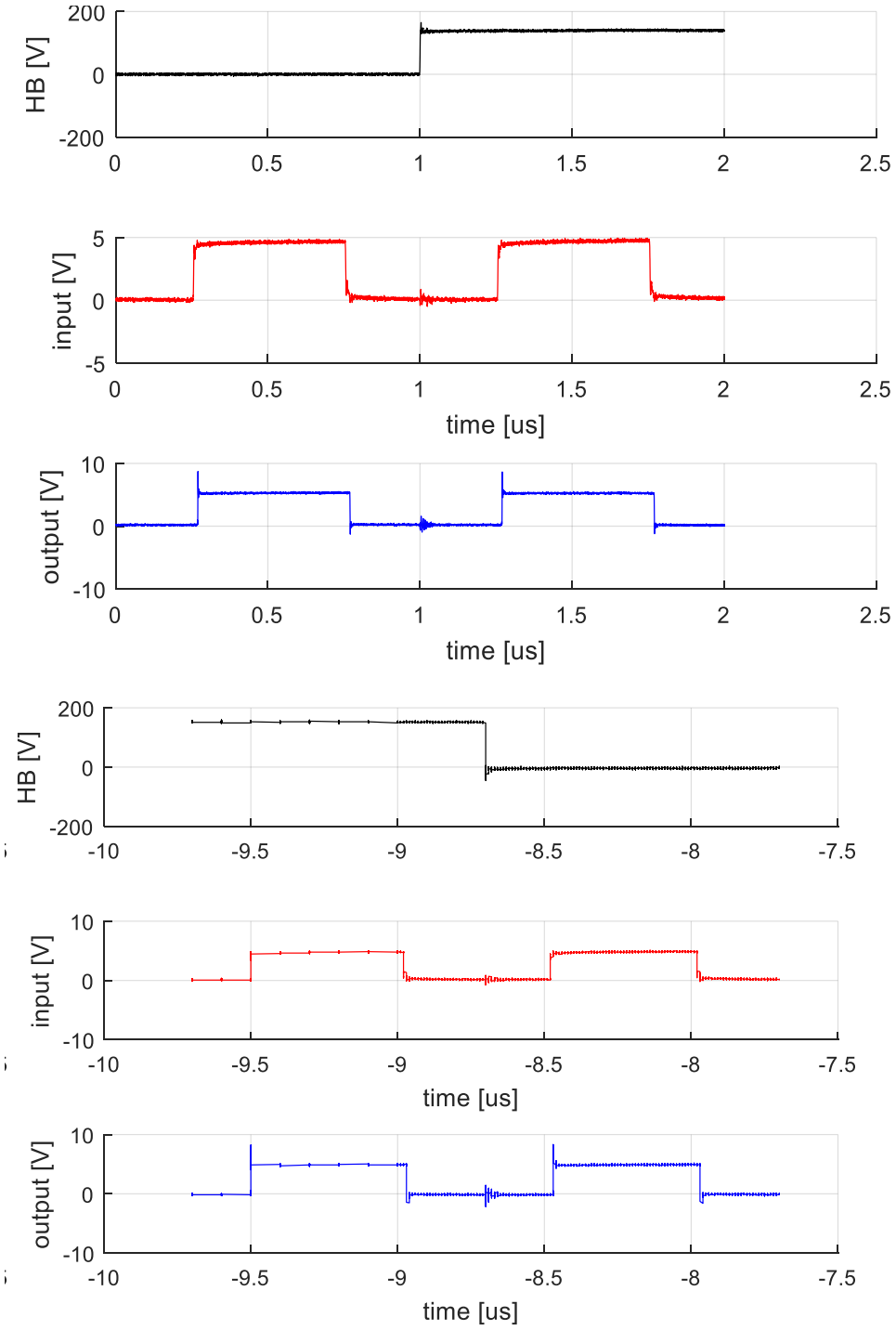

Figure 3-14 CMTI Measurement for Rising and Falling Transients

3.3 Fabrication and Measurement Results

The chip was fabricated in a 0.25 µm BCD process and co-packaged in a 16-pin SOIC Wide Body Package, as shown in Figure 3-10. The two chips within the system are identical, thus increasing the yield and reducing development costs when compared with

other proposed solutions [2,3]. In the presented measurements, the transmitter's two inputs (In+ and In-) are tied together so that the transmitter operates as a standard edge modulator that translates the input's rising and falling edges to positive and negative impulses, respectively.

3.3.1 Full-Channel Data Rate and Propagation Delay

A successful full channel communication at 300 Mb/s with a propagation delay of 5 ns can be seen from the measured unidirectional performance in Figure 3-11. Figure 3-12 shows the input and outputs of the measured BDGI during a 136Mbps bi-directional communication. Bi-directional operation with decoding is also shown in Fig 11(b). These characterizations prove successful communication of interleaved signal and, therefore bi-directivity of the presented BDGI.

3.3.2 Power Consumption

Power consumption has been measured during 50% duty cycle operation. At 5 V supply voltage, low-power consumption of 300 pj/b has been measured. At 4 V operation, total power consumption was further reduced to 180 pj/b. These results prove the efficacy of short pulse polarity modulation in combination with the implemented UWB transmitter

and high sensitivity low power receiver for offering significant power efficiency improvement.

3.3.3 Common-mode Transient Immunity and Isolation Rating

A 1-minute dielectric breakdown test has shown an 11 kV (7.8 kVrms) isolation rating, the highest reported to date for a fully CMOS isolator. CMTI was measured by applying HV transients with controlled slew rates across the grounds of the TX chip and RX Chip, and monitoring the digital output, to measure the highest slew rate that won't affect the output value. In order to ensure the safety of measurement equipment and oscilloscope operator, loop-back configuration shown in Figure 3-13 is used; thanks to the bi-directivity of the system, the feedback is shaped by self-feeding the output to the input of the secondary of the same GI. In this setup, the common-mode transient (Vcm) is applied at GND2 while the digital output is monitored. Measurement results for CMTI are shown in Figure 3-14 for different signaling scenarios, showing a consistent digital operation in the presence of 100 kV/μs HV Common-Mode transient.

Table 3-2 summarizes the presented system's performance and compares it to other state-of-the-art fully CMOS GI architectures.

3.4 Conclusion

A UWB CMOS BDGI is fabricated and measured. Table 3-2 summarizes the presented system's performance and compares it to other state-of-the-art, fully CMOS GI architectures. The presented system achieves the smallest total area per channel of 0.8 mm^2. Using the half-duplex topology allowed reducing the number of isolating transformers and bondwires by 50%. The double-isolated transformer enabled a 7.8 kVrms isolation rating,

TABLE 3-2: PERFORMANCE AND SUMMARY COMPARISON

Parameter	**This Work**		**[9]**	**[11]**	**AduM226N**
Technology(nm)	250		180	500	N.R.
Data-Rate(Mb/s)	300		500	250	150
Isolation Rating (kVrms)	7.8		7.5	2.5	5
Vdd(V)	5	4	N.R.	5	5
Total Power Consumption(pj/b)	300	180	200	650	550
Modulation Scheme	Pulse Polarity		OOK	Pulse Polarity	N.R.
Silicon Area(mm^2 /channel)	0.81		12.5	1	N.R.
Prop. Delay(ns)	5		-	5.5	7.2
CMTI(kV/us)	100		50	35	100
Bi-Directivity	Yes Shared GI Link		Yes Two GIs	No	Yes Two GIs
Standard Process/ Packaging	Yes		Yes	Yes	Yes

the highest isolation rating reported in fully CMOS, using less than 10% of the chip area of previously highest reported isolation [9]. Furthermore, the possibility of reaching an isolation rating two times of the rating allowed by the process's inter-metal dielectrics thickness without alternating the native process or adding additional steps to fabrication or packaging is demonstrated. The UWB transceiver presented in this work achieves the smallest propagation delay of 5 ns, with a lowest-power consumption of 180 pj/b. The implemented design also achieved an industry-leading CMTI of 100kV/us, one of the highest reported today for a bidirectional fully CMOS magnetic GI and two times higher than reported CMTI in [9]. This work also demonstrates that UWB TDD can achieve a high data rate of 300 Mb/s. Comparison of this work with state-of-art solutions clearly demonstrates the efficacy of presented circuits, design, and implementation technics in this work for achieving simultaneous robust, common-mode resilient, high data performance, energy-efficient compact solution using a fully CMOS process.

CHAPTER 4

Pulse Width Modulated Class-E PAs

In order to study class-E PAs, a mathematical ideal Class E behavioral model based on [38] is developed. This model allows for analysis and study of various attributes of a Class-E PA under PWM operation. Plots of Figure 4-1and Figure 4-2 show output power and input power of Class-E PA and drain efficiency versus duty cycle variation (ON time), respectively. From these figures, it is clear that with an increase of duty cycle from 0% to 50%, the output power, DC power consumption, and efficiency increases. After 50%, the

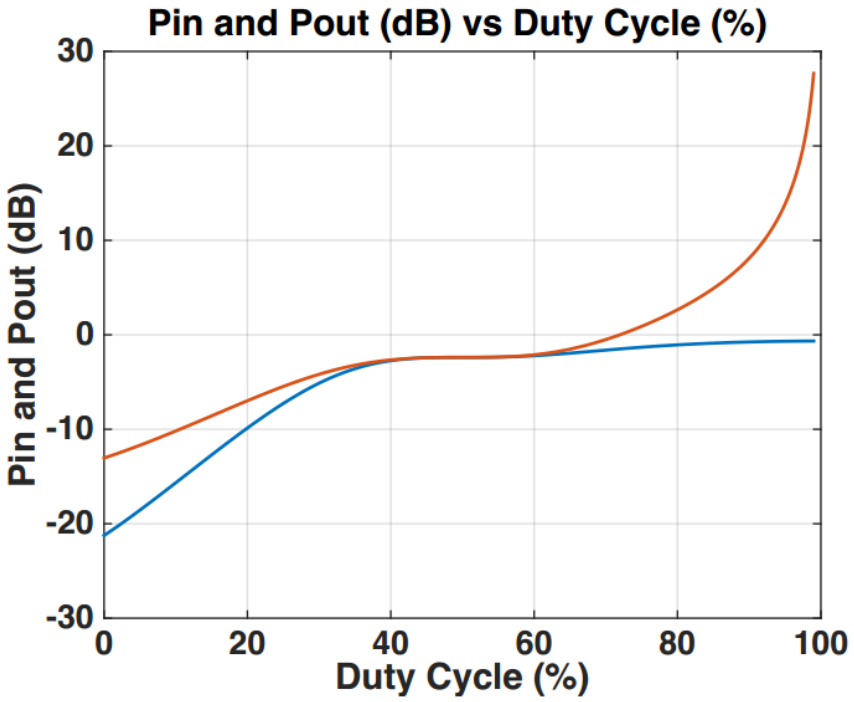

Figure 4-1 DC power consumption (orange) and RF output power in a PWM Class-E PA

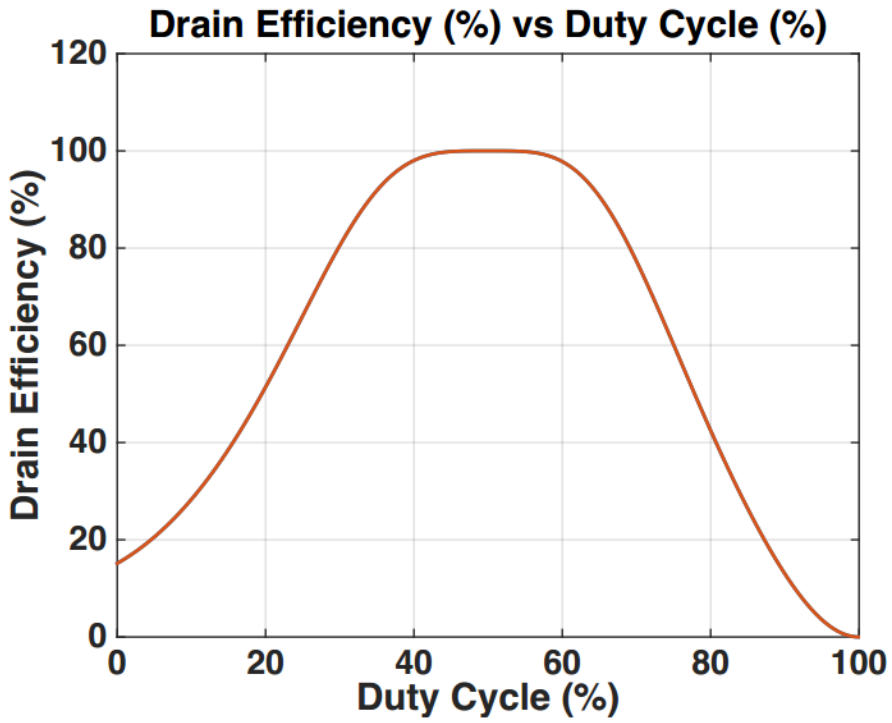

Figure 4-2 Efficiency vs. Duty Cycle in Class-E PAs

output power remains relatively constant while the DC power is increasing until the duty cycle reaches 100% at which the switch is always on; thus, the efficiency is zero. Figure 5-3 plots efficiency versus PBO for a duty cycles range of 0-50 percent, with an efficiency roll-off of 20% per first 3dB back-off, which is 30% lower (better) than 50% efficiency roll-off in the out phasing based works (Figure 4-5). However, as previously mentioned, due to the large input capacitance of the power transistors (GaN), the minimum duty cycle that can be generated at the input of the transistors are practically limited. In this work, we assume a 30% lower bound limitation for the duty cycle, which is an ideal Class-E PA means that dynamic range is practically limited to 3dB back off for fixed supply voltage.

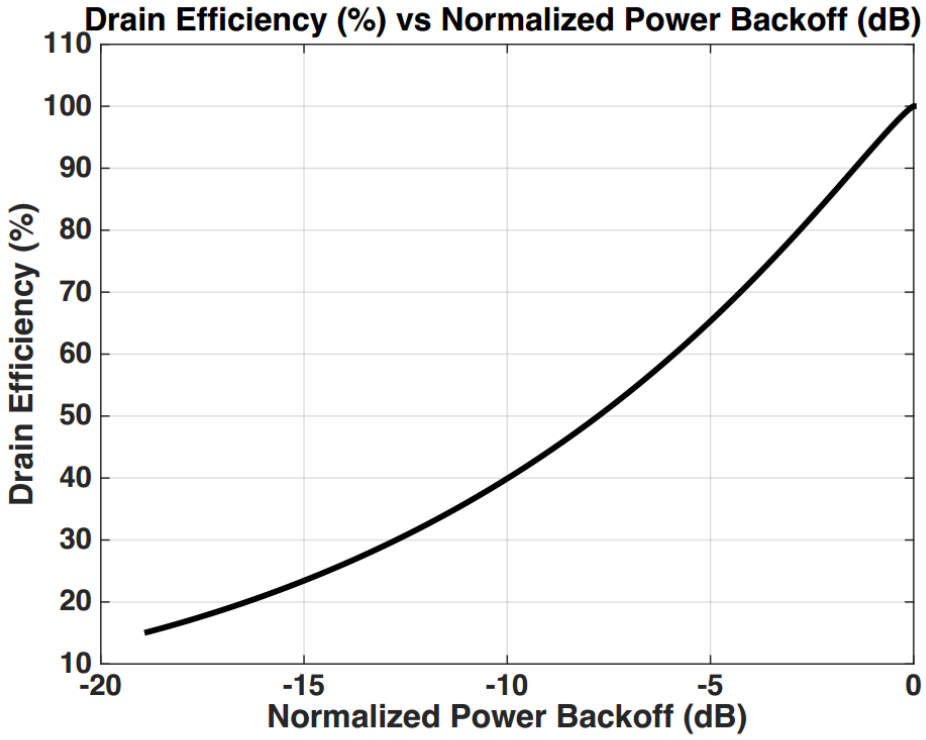

Figure 4-3 Efficiency vs PBO for Class-E PAs

4.1 Class-E PWM PA under Multilevel Supply variation

Figure 4-5 shows the efficiency versus PBO profile for PWM class-E, class-E in LINC, PWM class-E with multilevel supplies, and class-E in LINC with multilevel supplies. From Figure 4-5, the PWM class-E PA and class-E in LINC have the highest and lowest efficiency roll-off versus PBO, respectively. For the presented multilevel PWM class-E, the supply voltage is switched after the PA reaches its 3dB back-off associated with a 30% duty cycle. When this lower limit of duty cycle (e.g., 30%) is reached, the PA's supply is switched to a lower voltage value, and the PA's input duty cycle is switched back to 50%, thus allowing for another 3dB back-off using the adjusted lower supply voltage. A

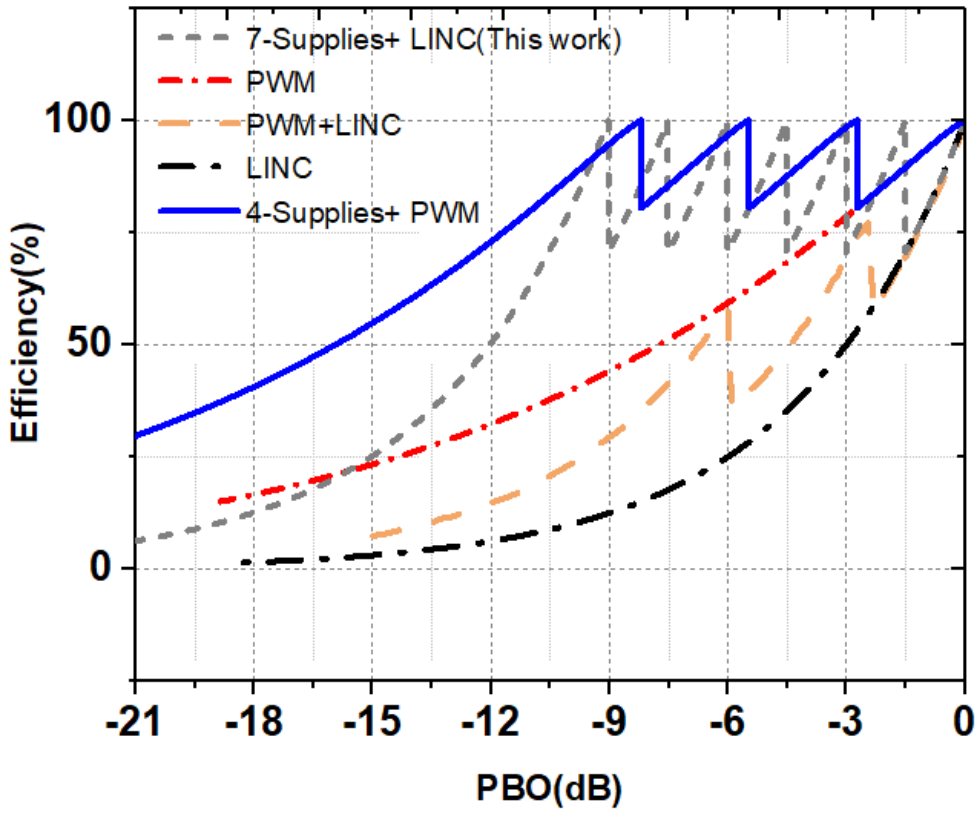

Figure 4-4 Ideal class-E power efficiency profile for various multilevel solutions

comparison between the results shows that PWM class-E has over 25% efficiency increase at 12dB PBO compared with the multilevel LINC. Furthermore, the presented architecture only requires 4 supplies, whereas previously proposed architectures need a larger number of supply voltage levels (e.g. 7 for this case) to achieve the same PBO dynamic range. Increased number of supply levels generally correlates to higher circuit complexity and lower efficiency in the supply regulator, as well as lower linearity for high PAPR communications signals. Therefore, class-E PWM is an excellent candidate with a multilevel operation to overcome the barrier associated with pulse-swallowing and enables substantially higher dynamic range and efficiency compared with prior works.

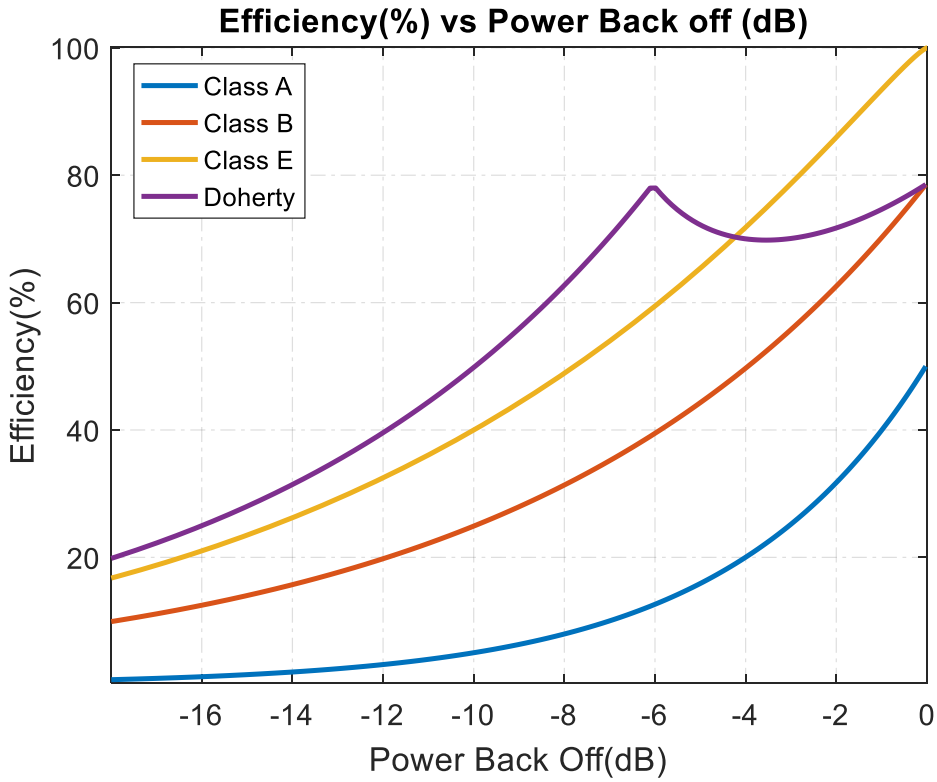

Figure 4-5 Efficiency vs. PBO comparison between current source PAs and proposed Class-E PWM PA

4.2 Efficiency Roll-off Comparison with linear PAs

In addition to the Class-G PWM performance comparison within SMPA topologies, in this section superiority of PWM class-E over flagship linear PA architectures is demonstrated. Figure 4-6, shows a comparison of efficiency versus PBO of Class A, B, and Doherty PAs with PWM-operated Class-E PAs. In the plot of Figure 5-10, all the efficiencies are normalized to 1 to allow for a comparison of the efficiency-PBO roll-off slopes. From these two plots, it can be seen that PWM Class-E shows the highest efficiency for the dynamic range of interest (first ~3dB power back off) and also a better efficiency

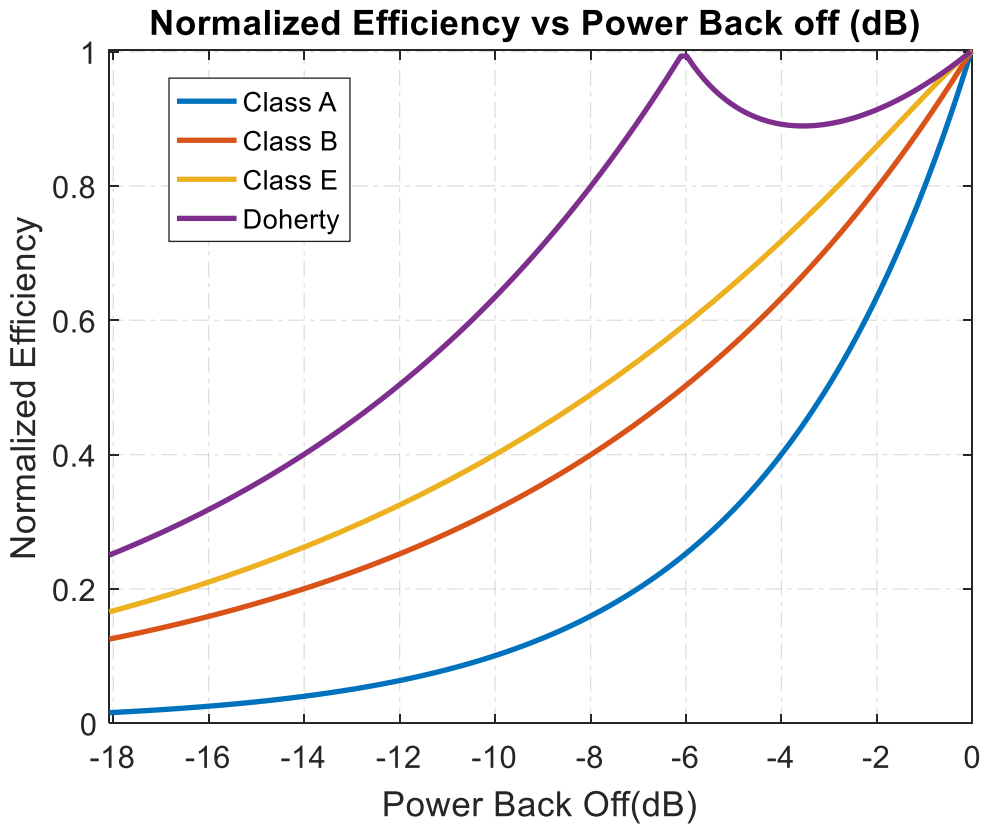

Figure 4-6 Efficiency vs. PBO comparison between current source PAs and proposed Class-E PWM PA

roll-off in comparison with Class-AB architectures. Although Doherty PA shows a slightly better efficiency roll-off in theory, however, in practice, the efficiency at the second high-efficiency point (the 6dB back off point in Figure 4-7) drops significantly in comparison with the peak power efficiency creating a higher roll-off slope. Therefore, the Class-E with PWM input signal (as fine control) is the best candidate for the multi-level operation.

4.3 Duty Cycle Sensitivity in Switch Mode PAs

Class-E and Class-D PAs both show output power sensitivity to modulation (variation) of their input's duty cycle. However, due to pulse swallowing, the SMPAs achievable

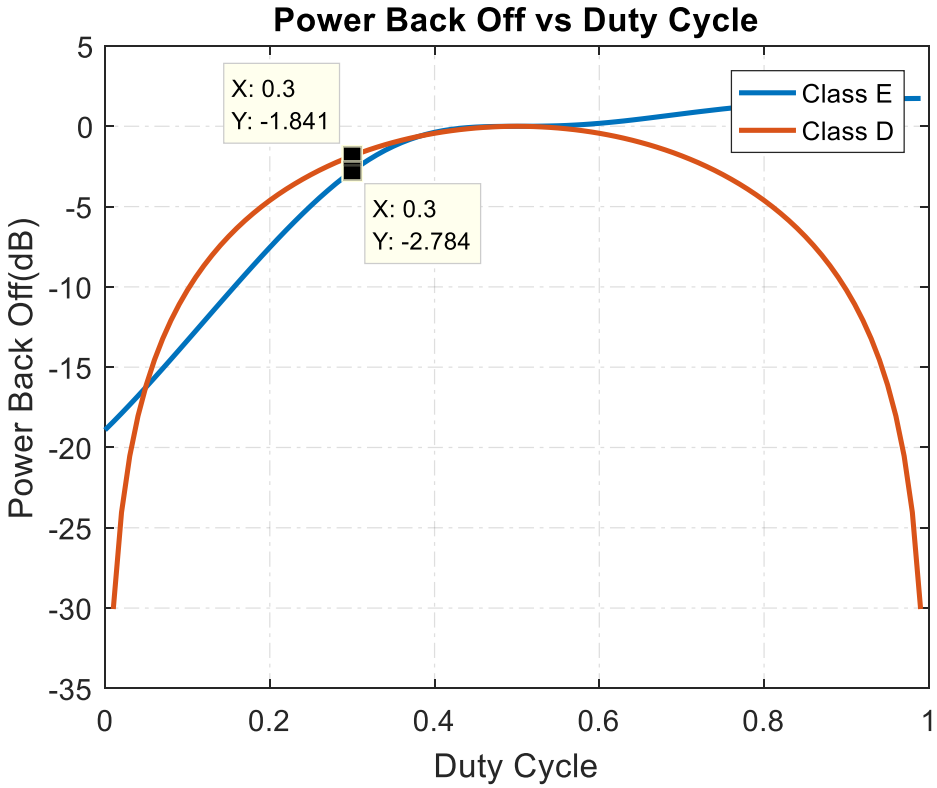

Figure 4-7 Output power to duty cycle sensitivity comparison for Class-E and Class-D PAs

dynamic range is limited; a PA Class is preferable that can achieve a higher dynamic range for a 50 to 30 percent duty cycle range. Figure 4-8 shows the overlaid plots of Class-E and Class-D PWM modulated output power back-off versus the input signal's duty cycle using mathematically modeled behavioral models. This plot clearly shows that Class-D PA's output power shows a lower sensitivity to duty cycle variation when compared with Class-E and its dynamic range becomes equal to class-E only after a low duty cycle of 5%. For example, this plot clearly shows that at 30% duty cycle, Class-E achieves 1 dB higher dynamic range than Class-D. Therefore when considering the pulse swallowing limitations for PWM PAs, Class-E PAs are a better candidate.

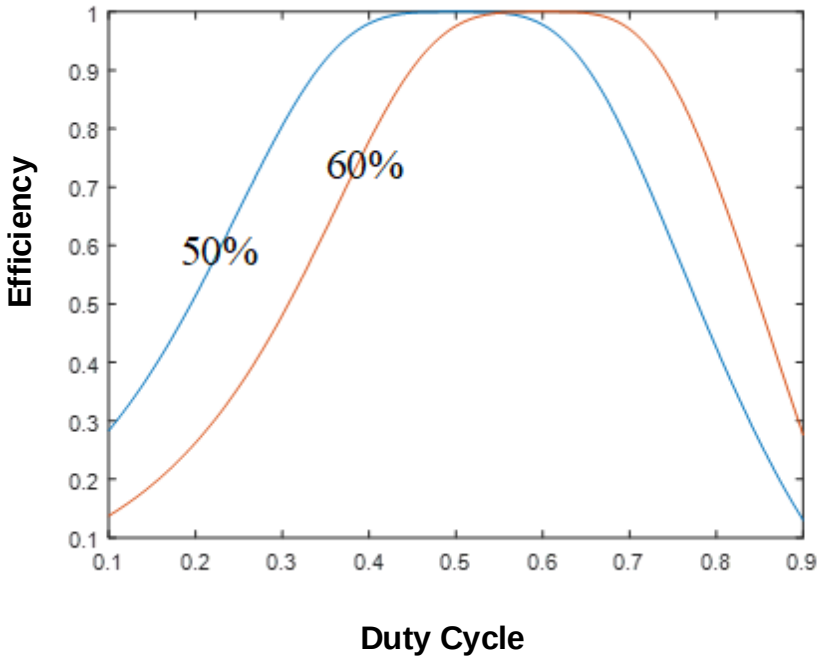

Figure 4-8 Class-E PA Efficiency vs. Duty Cycle for 50% and 60% optimized designs

4.4 Duty Cycle Sensitivity-Dynamic Range Enhancement

Although Class-E PAs, as shown in the previous section, naturally show a higher duty cycle sensitivity in comparison with Class-D PAs, however, in this research, we studied the possibility of further enhancement of output power's sensitivity to the duty cycle for class-E PAs to increase the associated dynamic range with the available practical duty cycle range. One of the limitations of the PWM class-E PAs has been their limited dynamic range in the nominal designs to less than 3dB. We propose an enhancement technique to address this issue and prove that the dynamic range can be enhanced through the optimization of network loads. In order to understand why the dynamic range is limited in class-E PAs, it should be noted that nominal class-E PAs (optimized to achieve the best performance at

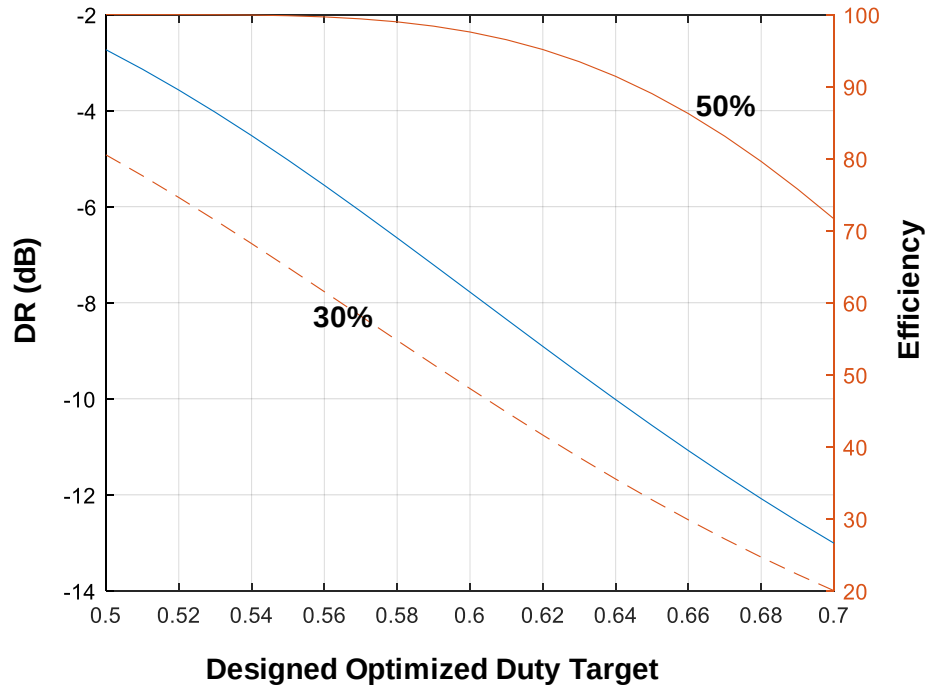

Figure 4-9 Dynamic range and efficiency at 50% and 30% duty cycle vs designed optimization target duty cycle.

50% duty cycle) experience a duty cycle de-sense around 50% to 40% duty cycle, which significantly limits the dynamic range. In order to address this issue, this work proposes that if the efficiency-pout vs. duty cycle profiles of the PA are shifted to the right side, the dynamic range and sensitivity to the PWM can be enhanced. In order to shift this profile, class-E PA can be optimized for a duty cycle higher than 50%. This has been demonstrated in Figure 4-10 for a class-E PA optimized for 60% duty cycle demonstrating significant sensitivity enhancement for the previously de-sensed 50%-40% duty range, pushing the de-sensed range toward the outside of the desired window With an increment of the optimized for duty cycle the dynamic range increases however the efficiency also starts to

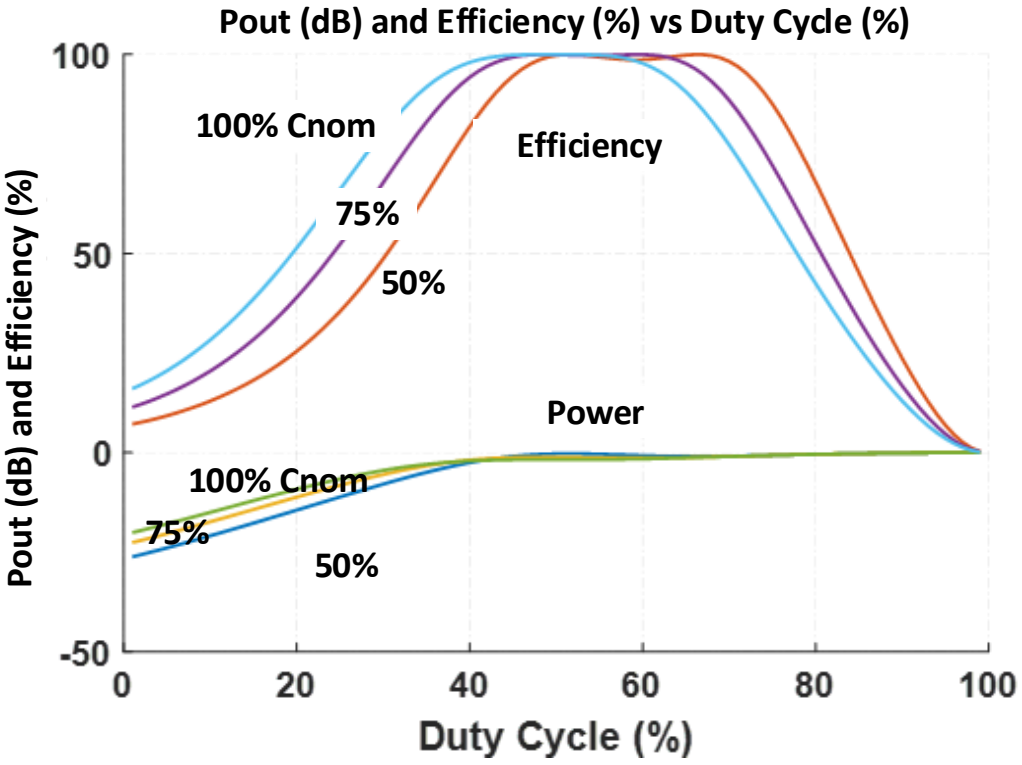

Figure 4-10 Class-E Pout and efficiency vs duty cycle for different shunt capacitance values with respect to nominal shunt capacitance (Cnom)

drop significantly. This shows that for a duty cycle target of 60%, the dynamic range can be enhanced from less than 3dB to about 8dB with almost no efficiency penalty, as shown in Figure 4-11.

4.5 Effect of Shunt Capacitance variation

Our study shows that reducing the shunt capacitance value slightly from the designed value can significantly increase the duty cycle sensitivity of the power amplifier. Figure 4-12 and 4-10 shows the efficiency and power profile versus duty cycle for nominal

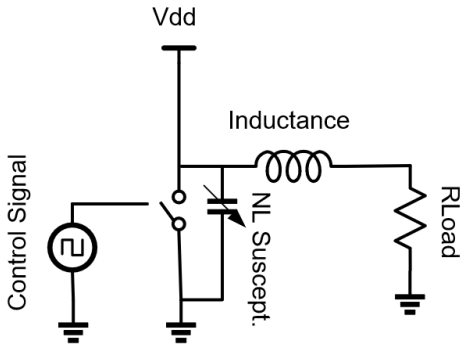

Figure 4-11 Conceptual Demonstration of a Class-E PA with a non-linear Output Capacitance

capacitance (C_{nom}), 25%, and 50% capacitance reduction from the nominal value. As can be seen, the dynamic range within 50 to 30 percent duty cycle has increased, and the flat portion of the efficiency profile is shifted toward duty cycles higher than 50%.

4.6 Effect of Shunt Capacitance Nonlinearity

To this point in this chapter, it was assumed that the shunt capacitance, parallel to the switching transistor is linear. However, in class-E PAs, using power transistors majority to all of the shunt capacitance of Cp is provided through parasitic capacitance of the switching transistor, which has a non-linear characteristic. Figure 4-17 shows parasitic parallel capacitance of a GaN transistor versus supply voltage. As this Figure shows, the capacitance value changes drastically with supply voltage variation and reduces the drain voltage increases. This non-linear behavior's effect on the performance of Class-E PAs has been the focus of various researches for a long time. However, in all these works, the effect of the aforementioned capacitance non-linearity is studied under *fixed duty cycle conditions*, and methods were proposed to neutralize or minimize this effect[63]–[65]. In this work, for the first time, we study the effect of non-linear parasitic capacitances in

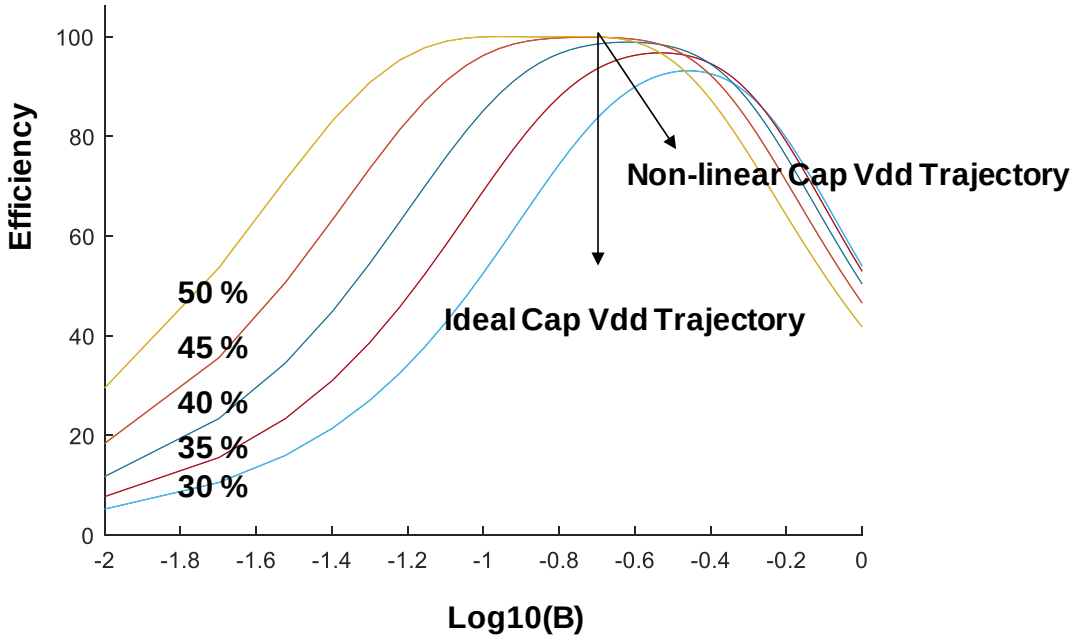

Figure 4-12 Class-E Efficiency vs Shunt susceptance for different duty cycles

Class-E PAs for a non-constant duty cycle operation (PWM). A conceptual class-E PA with non-linear parasitic capacitance is shown in Figure 4-11. In this research, to study the impact of non-linearity of parasitic capacitance, an ideal Class-E PA circuit model is developed, with a non-linear equation-based capacitance parallel to the ideal switch. A supply voltage sweep was done while plotting the efficiency and output power for two confining boundaries of practical duty cycle range (30% and 50%), using a circuit simulator. The results of these simulations are plotted in Figure 4-13 and Figure 4-14. The simulations are conducted for three cases: 1) linear capacitance (ideal case, constant with voltage) 2) non-linear capacitance with nominal value-effective capacitance at maximum supply voltage (the nominal supply the PA is designed to work for peak output power, e.g. 10V in this plot) 3) non-linear capacitance with less than nominal effective capacitance at maximum

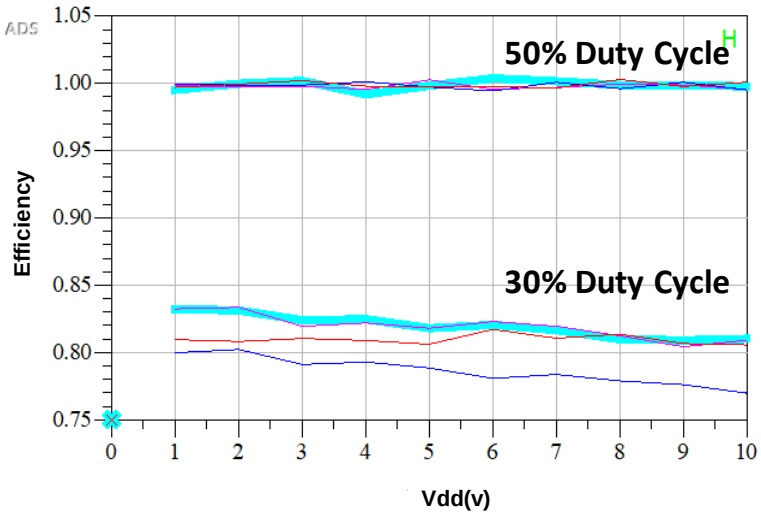

Figure 4-13 Efficiency vs Supply Voltage for Linear Cds (red), non-linear Cds designed with less than nominal effective capacitance value (dark blue) and non-linear capacitance with effective nominal capacitance (light blue)

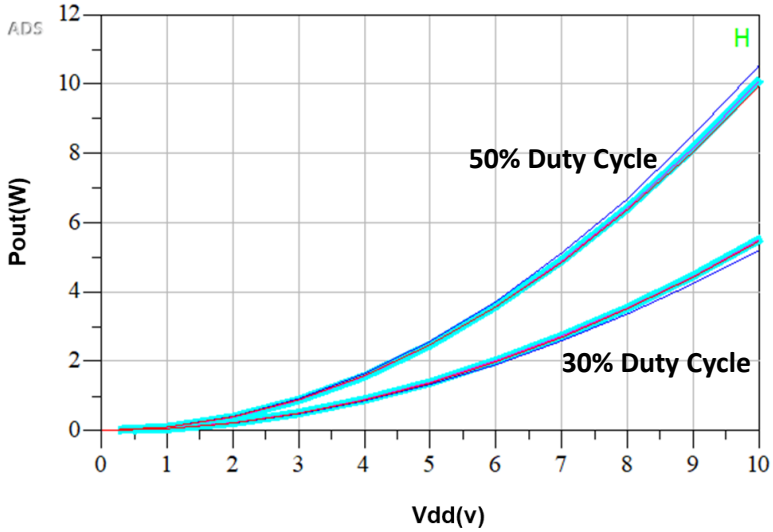

Figure 4-14 Pout vs Supply Voltage for Linear Cds (red), non-linear Cds designed with less than nominal effective capacitance value (dark blue) and non-linear capacitance with effective nominal capacitance (light blue)

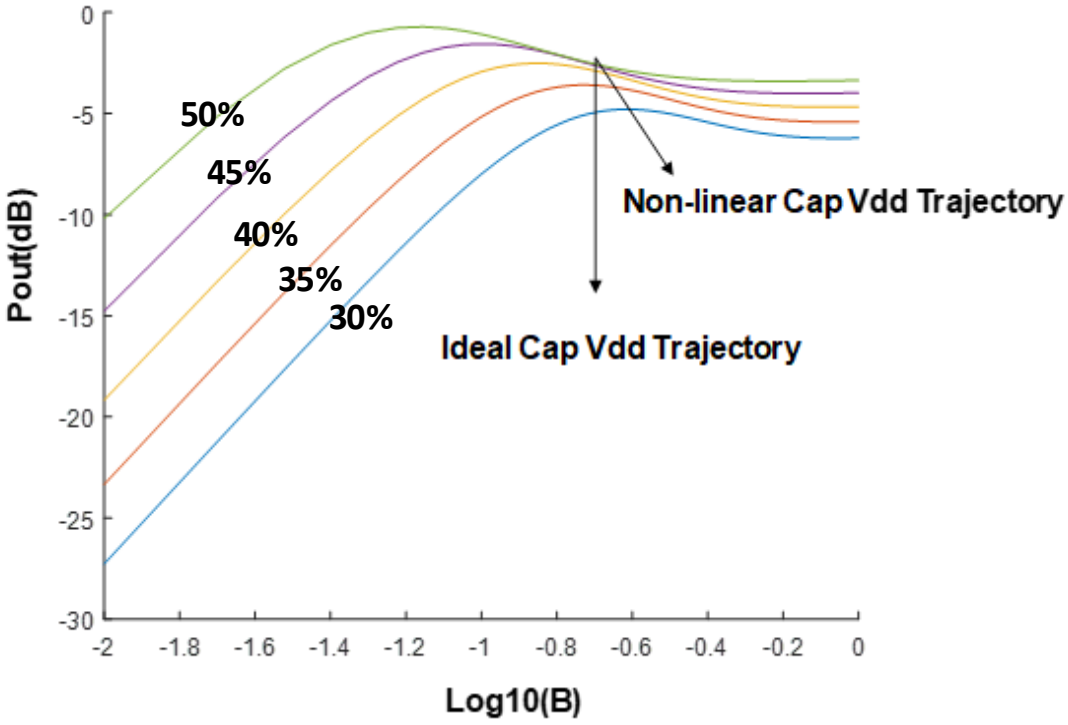

Figure 4-15 Class-E Pout vs Shunt suceptance for different duty cycles

supply voltage. The results show that for the linear efficiency, the efficiency is insensitive to the supply variation as expected. For both non-linear capacitance PAs, the efficiency plots show that while the efficiency for the 50% duty cycle remains flat and relatively insensitive to Vdd variation (and thus capacitor non-linearity), the efficiency at 30% duty cycle shows different behavior. At a 30 percent duty cycle, the efficiency is observed to be sensitive to the voltage variation and increase significantly with the reduction of the supply voltage. Thus the sensitivity of the PA efficiency to the Vdd variation increases with a decrease in duty cycle. At the same time, the output power versus supply voltage plots shows that at both 30 and 50 percent duty cycle output power profile is almost identical to a linear capacitance (ideal) design. Thus the output power is relatively incentive to the

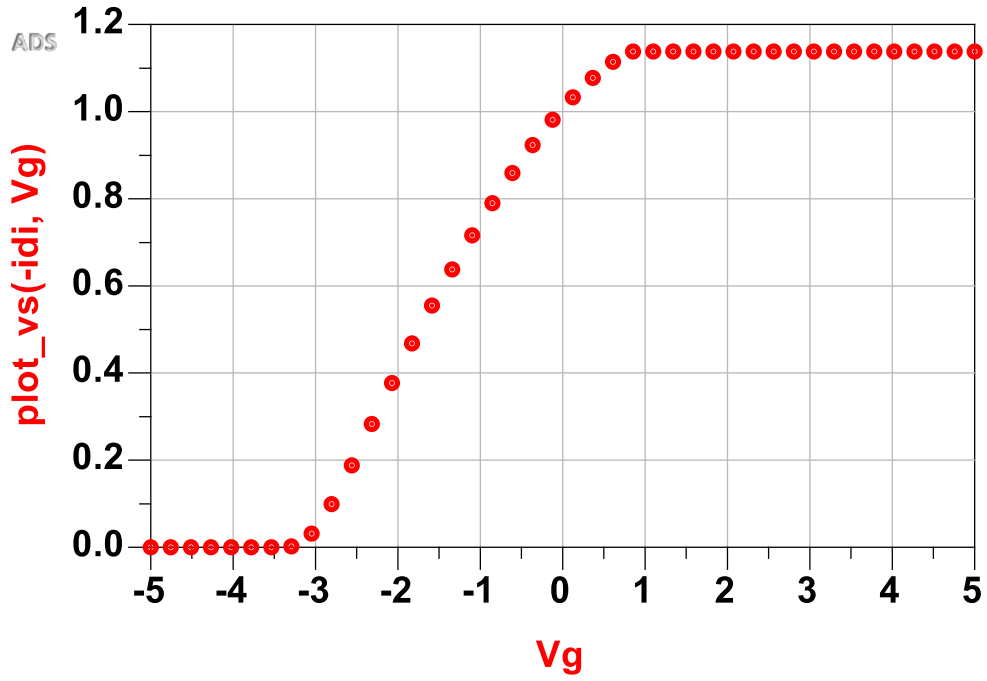

Figure 4-16 Ig_Vd Profile for the 8W Cree GaN (Bare Die)

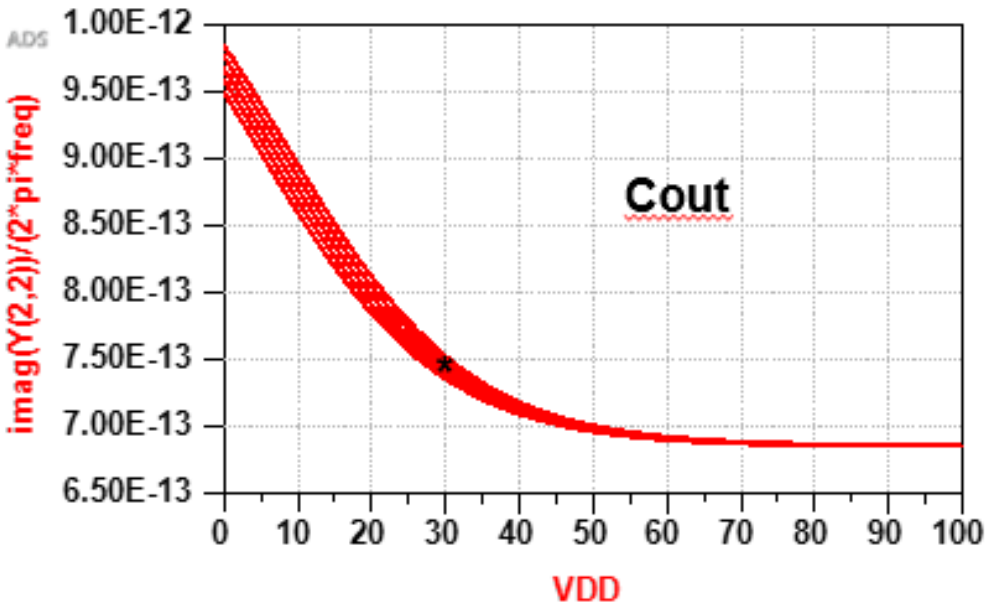

Figure 4-17 Output Capacitance (F) vs Supply Voltage (V) for the 8W Cree GaN (Bare Die)

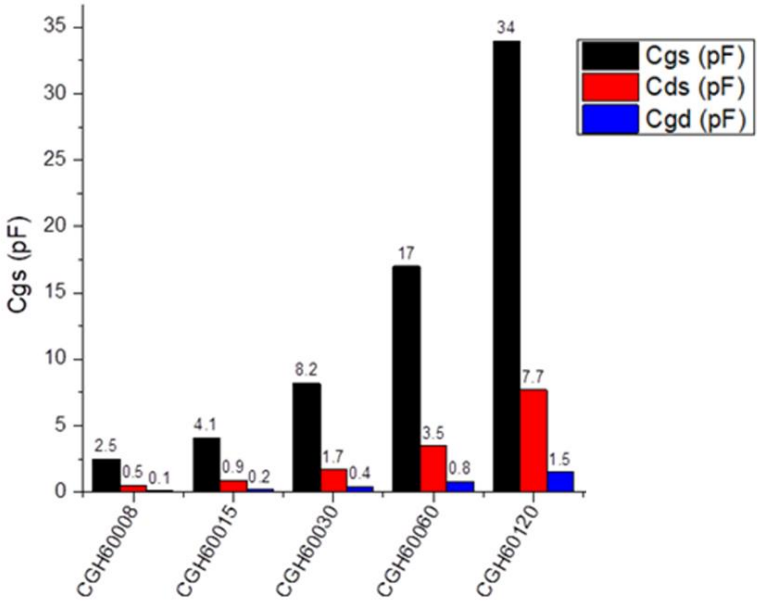

Figure 4-18 Parasitic Capacitance of GaN RF devices (from Cree) for different power ratings from 8W to 120W

capacitance non-linearity. Since the capacitance non-linearity leads to the efficiency increase with reduction of the supply voltage, this means that we can use this phenomenon in our advantage, enabling an auto-tuned (shunt capacitance) multi-level PWM Class-E PA solution that can break the well-known efficiency-power back off (PBO) trade-off.

The observed capacitance non-linearity affects the sensitivity of the class-E PA efficiency and output power to variation of the shunt capacitance is studied using the equation-based ideal PA model to validate and theorize. Figure 4-16 and Figure 4-17 show the efficiency and output power of ideal class-E PA versus shunt susceptance (B) for various duty cycles, where a nominal design has ~-8 dBohm shunt capacitance. The efficiency and output power trajectories are shown for Vdd variation for both the linear and non-linear capacitances. These figures visually demonstrate that in Class-E PAs the

efficiency sensitivity to the shunt susceptance increases with reducing the duty cycle. Thus, when the Vdd has reduced the shunt capacitance increases (Figure 4-17) and the efficiency and power follow the new trajectory associated with non-linear capacitance, causing a significant increase in the efficiency at lower practical duty cycle boundary (30%) and remains almost flat at 50% while at the same time at either duty cycle the output power doesn't change significantly as shown in Figure 4-15**.** This result from the ideal class-E mathematical model is in complete agreement with the ideal circuit simulation results for Vdd sensitivity from Figure 4-13 and Figure 4-14.

4.7 Driver Requirements

Since this work focuses on the power amplifier part and relies on external PA driving solutions, it's important to understand the driver requirements, specifications, limitations, and how the driver specifications can affect the PA design. Figure 4-18 shows the values of parasitic capacitance for different GaN transistors. This figure clearly shows that the input capacitance can be in a range of 2.5 pF to 8.2 pF transistor for an 8 to 30 watts device. Due to the large input capacitance of the power transistors such as GaN, a driver circuit is needed to generate the required square wave gate at the transistor's gate for different duty cycles[39][40][66]. A functional driver should be able to generate a large enough voltage swing to turn the device on and off, accounting for the voltage drop over the connection from driver to the PA, especially at higher frequencies since the loss over the Driver-PA interface increases. Furthermore, the driver should be able to switch at the expected design frequency. In addition to the switching frequency of the driver, the driver should be able to turn on and off the PA gate with minimum rise time and fall time (dv/dt), which means the driver should be able to charge the input capacitance of the PA in the shortest possible time

by providing enough current(Cdv/dt). Thus the practical frequency and duty cycle at which the driver can be used also depends on its charging capability.

4.8 Non-linear Input Capacitance in Switch-Mode Transmitters

4.8.1 Overview

In previous sections, we studied the effect of output capacitance non-linearity in digital transmitters and demonstrated its significance, especially in Class-E power amplifiers in the presence of duty cycle and supply voltage variation. This section presents results on the effect of input capacitance non-linearity in design requirements and performance of digital transmitters.

The capacitance of a capacitor is defined through the relation between the stored charge by the capacitor and the voltage across its terminals:

$$\mathbf{C}(\mathbf{v},\mathbf{t}) = \frac{\mathbf{q}(\mathbf{v},\mathbf{t})}{\mathbf{v}(\mathbf{t})} \qquad (4-1)$$

In a wide range of design circuit and analysis techniques, the above equation is assumed to be linear and thus results in C(v,t) becoming time and voltage invariable. However, in solid-state devices, the parasitic capacitance (e.g. MOS Cap and Junction Caps) are known to be variable with voltage, thus resulting in a non-linear behavior. In small signal applications, the small-signal capacitance at the dc voltage of operation can be calculated and used during the design and simulation. However, in power amplifiers, due to the large-signal operation, the parasitic capacitances not only are a function of biasing voltage but also a time-variable voltage, varying with the fluctuations due to input and output signals. Thus there is a need to understand how this voltage and time dependence can affect the

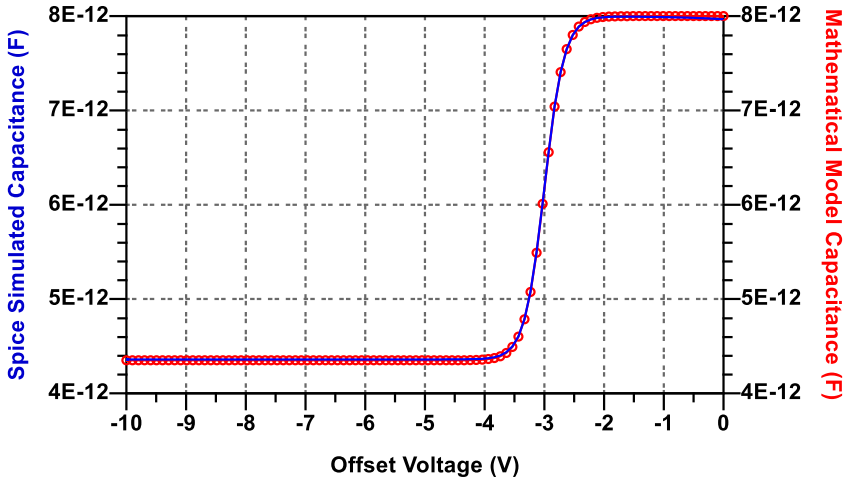

Figure 4-19 Small Signal Input Capacitance C(V)-V plot

(red=foundry model simulation, blue=mathematical model)

performance and design requirements of a digital transmitter. Input capacitance looking through the gate in amplifiers is of paramount importance, especially since the input gate capacitance shows a significant change with a hard transition around the transistor's threshold voltage, VT (e.g. -3 for the GaN HEMT used in this analysis). Figure 4-19 shows the C(V)-V relation for input capacitance of a GaN HEMT, which shows around up to two times of variation due to voltage dependency. The input capacitance value is key parameter to different performance and design requirements, including the overall input power consumption and required drive power, the peak current capability required from the driver, and also the PA input network of the power amplifier. It is desirable for designers to work with a time-independent capacitance for describing the power FET and also simplifying the design procedure and predicting the drive requirements. However, most data sheets report the off-state capacitance, which, when used, can lead to inaccurate results. This work studies how the input capacitance non-linearity does affect the above-

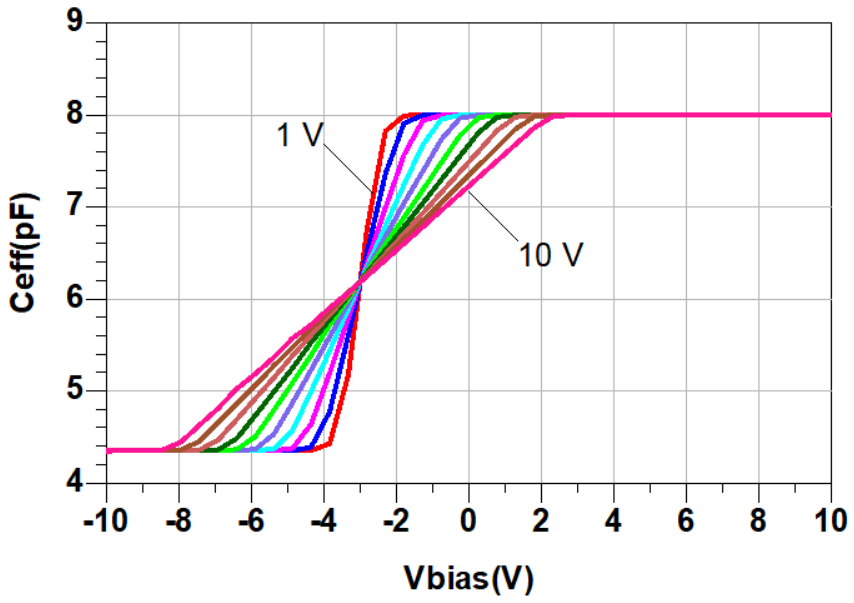

Figure 4-20 Effective Input Capacitance C(V)-V plot for a Square Wave with amplitudes varying from 1V to 10V

mentioned parameters and also presents a method for calculating effective capacitance for digital transmitter applications.

4.8.2 Effective Capacitance: Conventional Definition and Extraction Method

The current of a capacitor can be written as:

$$\mathbf{i(t)} = \frac{\mathbf{dq}}{\mathbf{dt}} = \overbrace{\frac{\mathbf{d\left(C(v,t)V(t)\right)}}{\mathbf{dt}}}^{\mathbf{(1)General\ Capacitance}} = \overbrace{\frac{\mathbf{Cd\left(V(t)\right)}}{\mathbf{d(t)}}}^{\mathbf{(2)Linear\ Capacitance}} \qquad (4-2)$$

For an amplifier driven with a sinusoidal signal, the effective capacitance can be written as:

$$C_{AVG} = \frac{rms(i)|_{f0}}{rms\left(\frac{dv(t)}{dt}\right)|_{f0}}$$

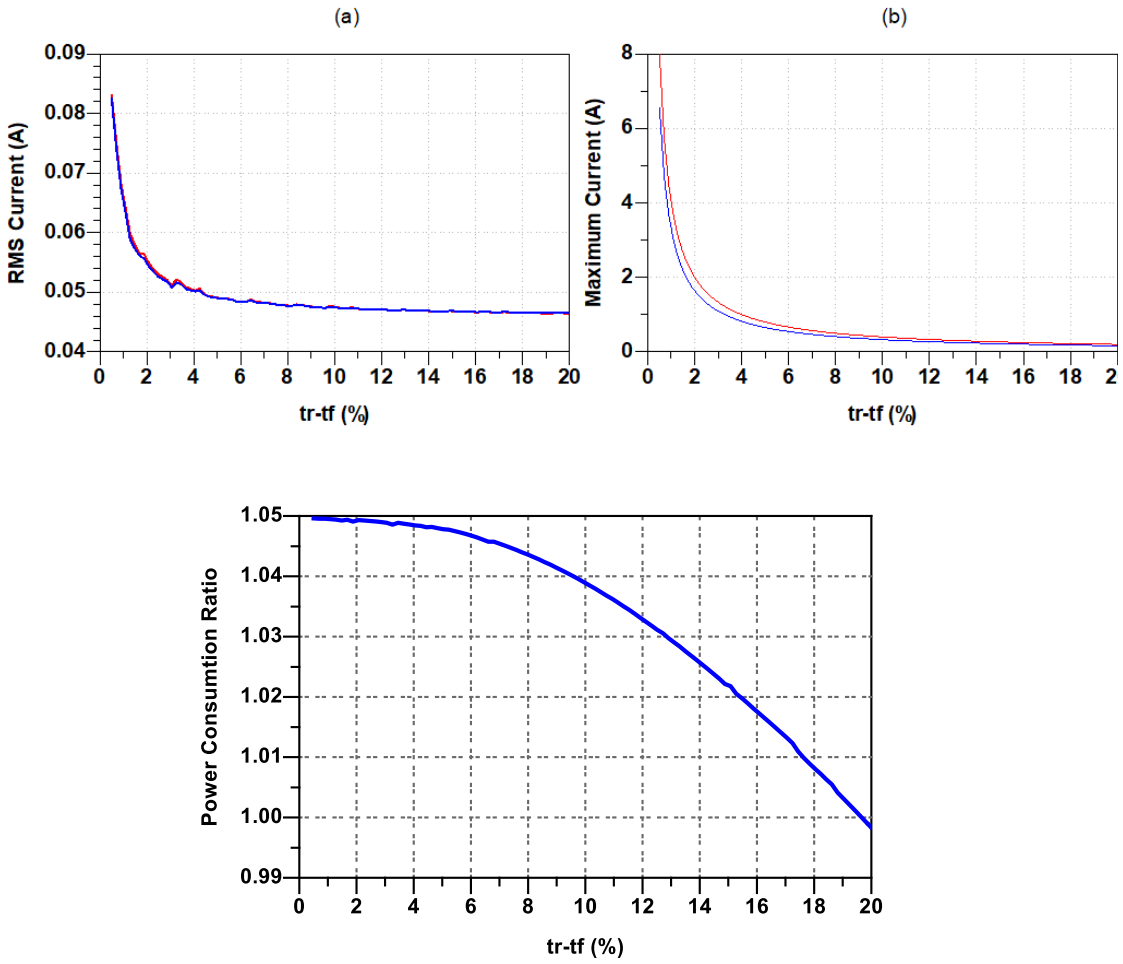

Figure 4-21 (a) RMS Current and (b) Peak Current variation (c) Power Consumption ratio vs. Transition time (% of period) (red=NL-Cap, blue=Ceff)

However, in digital transmitters, the power devices must be driven by square-wave signals, which are wideband signals that consist of numerous harmonics. Thus the traditional effective capacitance will not return an accurate result in large signal square-wave operation, and there is a need for defining a new metric.

4.8.3 Proposed Method: Effective Capacitance for a Square Wave Drive Signal

This work proposes a new method for the calculation of effective capacitance in the following:

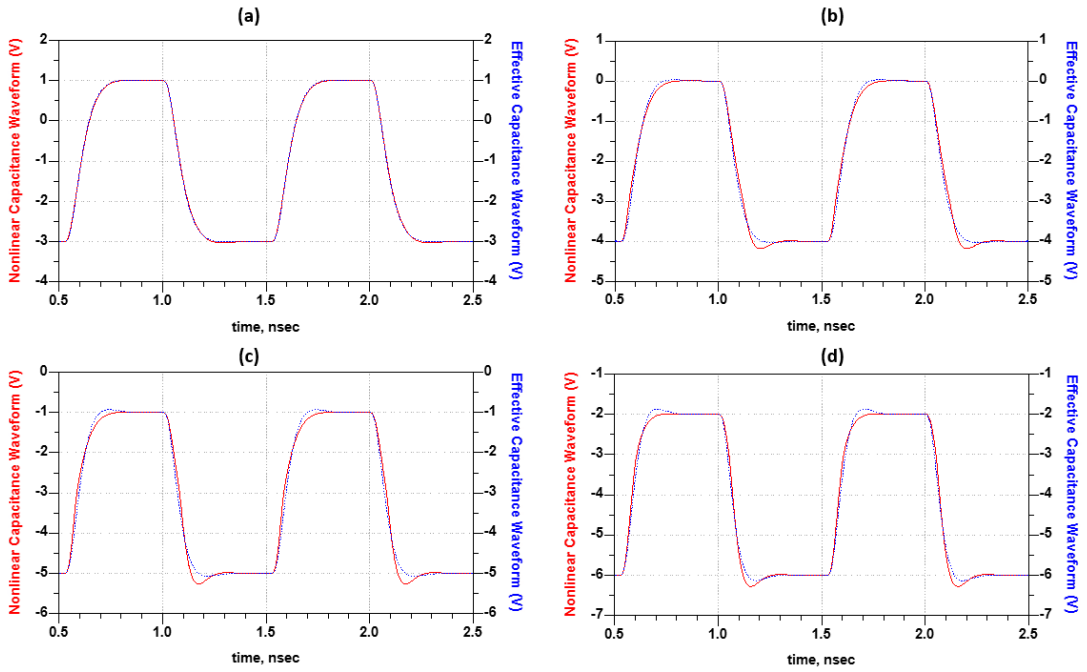

Figure 4-22 Voltage waveform across the input capacitance of PA, with input network for (a) -1V (b) -2V (c)-3V (d) -4V offset voltages @ 1GHz.

$$\mathbf{C_{eff}} = \frac{\mathbf{rms(i) for\ the\ DUT\ nonlinear\ capacitance}}{\mathbf{rms(i) for\ a\ linear\ 1F\ capacitance}} \qquad (4-4)$$

Where in both linear and non-linear cases, the transistors are driven with the same square-wave signal. This definition allows for a close match both in time-form wave shape and also in terms of drive power. In this work, we use an ideal drive signal for effective capacitance calculation and later show that the proposed definition with using the ideal signal holds valid and useful in the presence of an input network, rise-time, and fall-time, and duty cycle variation.

4.8.4 Modeling the Non-Linear Input Capacitance

In order to simulate and analyze the effect of non-linear capacitance, an equation-based mathematical model for the C(V)-V behavior of non-linear input capacitance of the FET simulated in Figure 4-19 has been developed.

$$\mathbf{C_{in}(V) = Cmin + (Cmax - Cmin) \times \frac{1 + \tanh\big(3 \times (V + VT)\big)}{2}} \qquad (4-5)$$

The result from the developed model and the simulation results from the foundry model is overlaid in Figure 4-20 and are in excellent agreement.

4.8.5 Effective Capacitance Simulation Results

Figure 4-20 depicts the effective non-linear capacitance for various amplitudes versus biasing (offset voltage) variation, utilizing the proposed method. This figure clearly shows that the effective capacitance deviates from the small-signal version shown in Figure 4-19 as the amplitude increases resulting in larger effective capacitance when biased less than the threshold voltage (-3V) and smaller effective capacitances when biased larger than the threshold voltage. This can be intuitionally expected since as the amplitude gets larger, the signal spends more time in the Cmax region when biased less than the threshold voltage. Similarly, the opposite takes place when biased at higher than VT, and the signals spend more time in Cmin region.

4.8.6 Peak Current Requirement and Sensitivity to Rise-Time/Fall-Time

In Figure 4-21(a), the RMS current is demonstrated across input signal rise time and fall time variation and compared between the non-linear case and effective capacitance case. This simulation results show that the effective capacitance is valid and insensitive for a wide range of transition time.

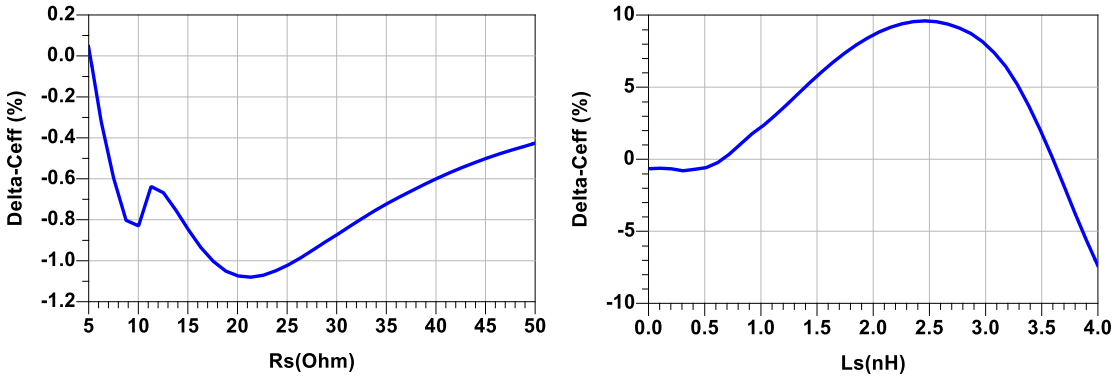

Figure 4-23 Nominal Capacitance deviation vs. input resistance and inductance of IC interface

Figure 4-21(b) also shows that while the effective capacitance can accurately predict the RMS current consumption, the maximum current that needs to be available by the driver is determined by the maximum capacitance seen by the signal during its transition. Thus for calculating the peak available current required by the driver, effective capacitance provides a very close estimation. However, it is the maximum capacitance seen by the driver during the transition that the peak current can be estimated with the best accuracy.

4.8.7 **Effective Capacitance in the presence of Input Network**

Figure 4-22 demonstrates four examples of the voltage waveforms across the non-linear input capacitance for various offset values from -1V to -4V, for a 4V driving signal, in the presence of an input network connecting the driver model to the non-linear capacitance model, consisting of an inductance (Ls) in series with a resistor (Rs), to take into account for connection's inductance and resistance, bondwire inductance, and damping resistance. These figures also show as the waveform starts to leave the flat part of effective capacitance (Figure 4-22 (a)) and experiences more dynamic capacitance deviation, the waveform becomes more asymmetric, e.g. experiencing different overshoots in falling transition from

rising transition. The waveform when the non-linear capacitance is replaced with effective capacitance is calculated from Figure 4-20, utilizing the proposed method in 4.8.3. As shown in Figure 4-22, the effective capacitance waveforms and non-linear capacitance waveforms are in great agreement in the presence of the input load networks and interconnect from the driver to the PA.

4.8.8 Sensitivity to Input Network

The nominal effective capacitance calculation presented in Figure 4-22 is done utilizing an ideal square-wave signal which is applied directly through a short wire to the non-linear capacitance, in the absence of the input network that interfaces the driver with the power device (non-linear capacitance here). Although the effective capacitance can be calculated using the formula from the proposed method, taking the input network effect into account, as shown in the previous session, the nominal effective capacitance is in good agreement with simulation results from the non-linear cases, in the presence of an input load. Figure 4-23 shows the deviation of the nominal effective capacitance from the effective capacitance calculated by taking the interface network into account. These results show that using the nominal effective capacitance can give results with excellent accuracy. The results are less sensitive to the resistance Rs since it mostly affects the rise-time and fall-time. However, the results are more sensitive to the series inductance Ls, since its increase distorts the signal to the point that it no longer has a square wave shape, which is expected to lead to larger errors from the nominal case.

4.8.9 Duty Cycle Sensitivity

The duty cycle variation does not change the transition trajectory of the driving signal's transition; thus, the overall driving rms current remains constant with duty cycle variation, and also the effective capacitance won't change with duty cycle, although the overall dc value of the driving signal reduces with duty cycle reduction. This is due to the fact that the effective capacitance is a function of amplitude and off-set voltage (y-axis symmetry line of the waveform) as shown in Figure 4-22. Thus despite the fact that duty cycle variation modifies the DC value (and also rms value) of the signal in proportion with the duty cycle since the offset voltage remains constant, the effective capacitance doesn't change with the duty cycle. Therefore general beliefs that the effective capacitance is a function of the rms value or dc value of the signal are probably mostly coming from the traditional effective capacitance for sine wave signals and do not hold in general and specifically for digital driver signals.

4.9 Design and Implementation

A proof of concept 1W class-E RF power amplifier (Figure 4-24) is designed with its schematic shown in Figure 4-26. The design uses a bare-die Cree GaN HEMT transistor and a finite choke inductance topology, with a maximum supply voltage of 9V. The presented PA is designed for a 50 MHz square wave input signal that is generated by an arbitrary wave generator (AWG) with 4Vpp amplitude and rise and fall times of 2.9ns. In this design, the output load network is optimized to maximize the output power sensitivity to duty cycle variation, thus extending the dynamic range to more than 7dB with 30% to 50% duty cycle variation compared to a typical class-E PA that has only 3dB dynamic range (Figure 4-1). A 50 ohm damping resistor (RDamp) interfaces the driver's (AWG)

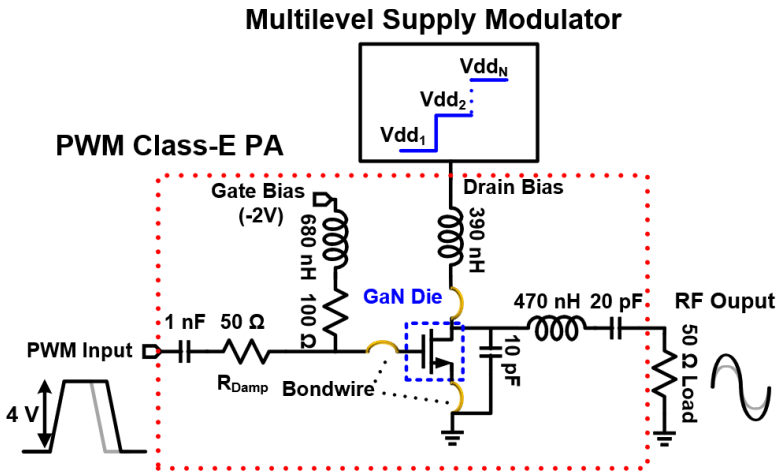

Figure 4-24 Implemented PWM Class-E PA

output with the GaN device's input gate terminal. RDamp forms a series RLC filter with the inductance and input capacitance to damp input signal oscillations.

4.10 Measurement Results I

The designed PA is measured using an AWG to generate the PA's input drive signal and a spectrum analyzer to measure the output spectrum and fundamental power, as illustrated in Figure 4-25. An attenuator is connected to the PA's output to minimize power reflections for instrument protection. The measurements are in complete agreement with design simulations. Figure 4-26 shows the measured output power and efficiency for varying input signal duty cycle with a fixed 9V supply voltage. The PA achieves more than 6dB dynamic range for 30% to 50% duty cycle variation, thus demonstrating successful class-E design optimization for PWM operation. Figure 4-27 shows measured efficiency versus output power for various supply voltages, where the change in output power is achieved through both duty cycle and supply voltage variation. These results display less than 15% efficiency roll-off per 3dB backoff, and the results validate the proposed concept of using

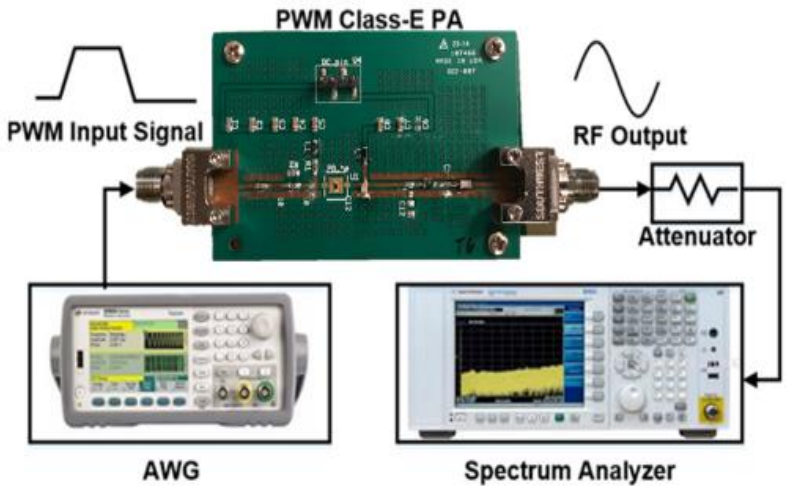

Figure 4-25 Measurement Setup

PWM in combination with multilevel supply voltages to increase average efficiency for high PAPR signals. A potential PWM and supply voltage trajectory has been highlighted (blue line) in Fig 4-27 to achieve more than 20dB PBO with only four supplies, and over 65% drain efficiency at 12.5dB PBO. Fig. 16 also shows that the implemented PA's drain efficiency increases with reduced drain voltage for a fixed duty cycle, thus creating a PA system that has increasing efficiency when controlling the PBO through supply voltage. In addition to output power measurements, phase measurements were also conducted. Figure 4-28 shows the output phase variation with respect to input phase, showing a linear relation and desirable phase controllability. In Figure 4-29 output phase measurement with respect to duty cycle is shown. The results are in good agreement with simulation results.

4.11 Discussion on Non-idealities

Two important phenomena can be observed from comparison of measured results in Figure 4-27 with Figure 4-5. The first observation is that the efficiency is compressed at 50% duty cycle with increase of the supply voltage and the second observation is that efficiency increases with reduction of supply voltage at 30% however with a more linear

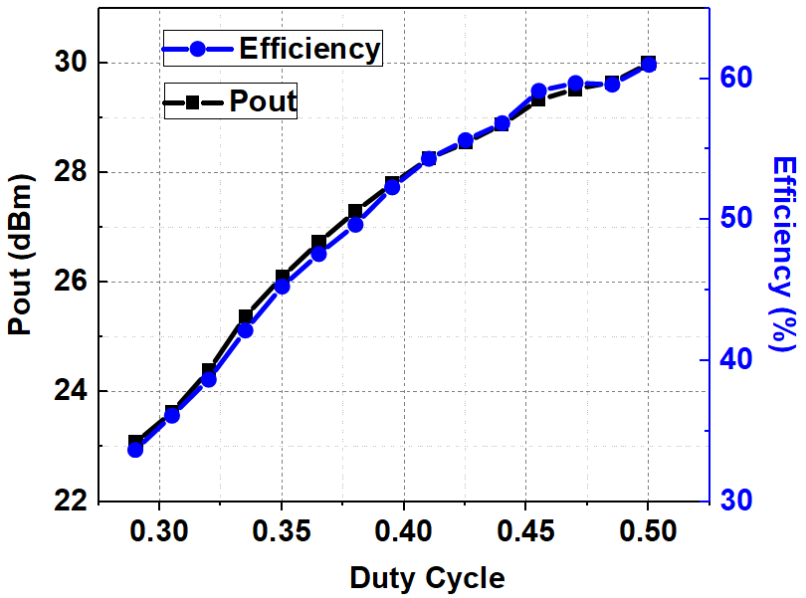

Figure 4-26 Measured Output Power and Drain Efficiency vs. Duty Cycle

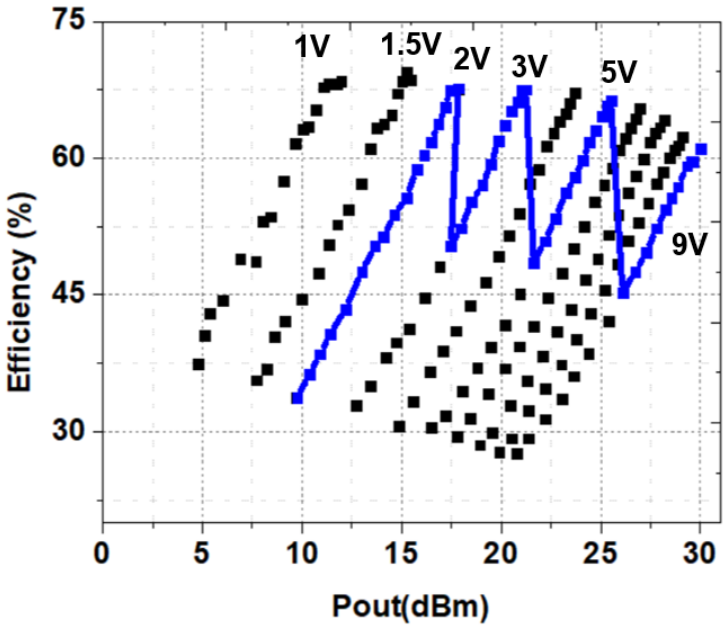

Figure 4-27 MEASURED efficiency versus output power (Pout) for various supply voltage levels (black). 4-level supply switching at 4dB backoff per supply (blue).

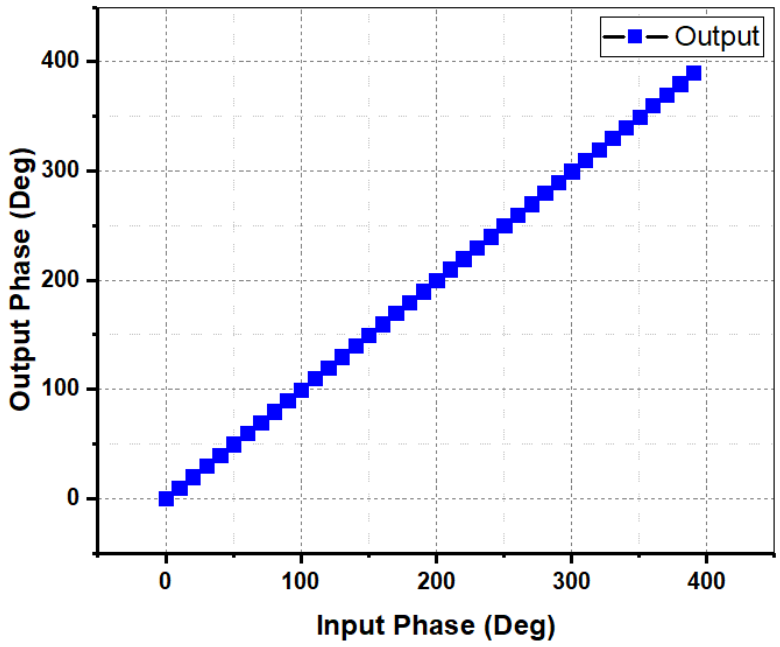

Figure 4-28 Normalized Output phase (y-axis) deviation (sensitivity) vs. Input phase

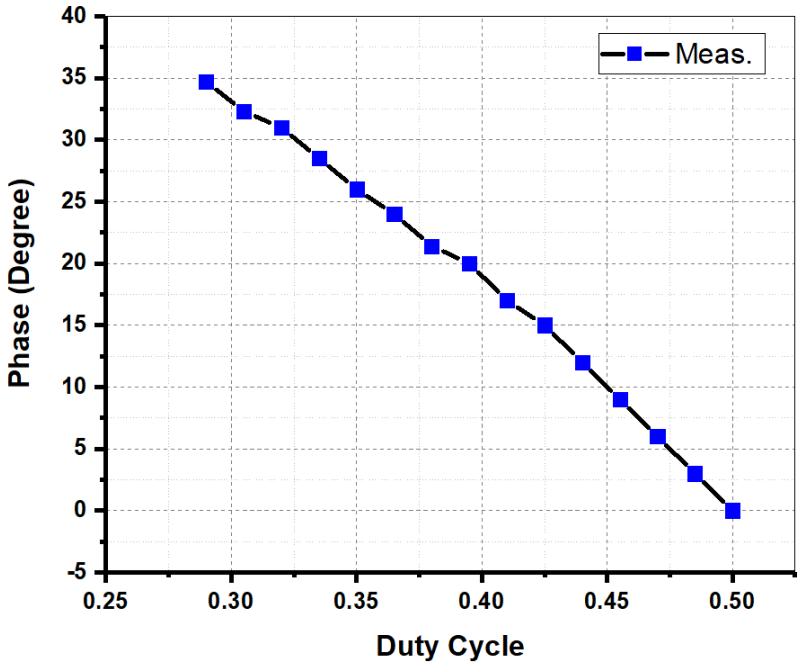

Figure 4-29 Output phase vs. Duty cycle

manner, unlike the constant efficiency plots vs. supply voltage that were expected from the ideal model. Our investigation shows that his behavior roots in self-heating and output capacitance non-linearity of the transistor, with the former being dominant at 50% duty cycle and the latter at 30% duty cycle. Self-heating is a phenomenon present in HEMT devices in which the heat dissipation in the device causes the junction temperature of the device to increase, hence reducing the device's physical parameters such as mobility and carrier saturation velocity. In power amplifiers, with an increase of power, the heat dissipation increases, and therefore the transistor's junction temperature rises. In switching GaN devices, this leads to a reduction of ON-resistance of the device and, thus, higher switching losses. In the next sections, we conducted simulations and designed an experiment to empirically investigate these behaviors.

4.12 Simulation Results

The class-E PA was simulated in four scenarios: No self-heating in room temperature, room temperature, 75°C, and -78.5°C. According to the studies presented, room temperature simulations when the self-heating model is deactivated show the efficiency degradation is eliminated at 50%, and the efficiency profile becomes flat since capacitance non-linearity is not significant at this duty cycle as expected from the earlier analysis in 4.6. At lower duty cycles such as 30%, efficiency degradation is present even with deactivated self-heating, and unlike 50% duty cycle, the efficiency profile has a negative slope, which proves the efficiency variation being majorly due to capacitance non-linearity at lower duty cycles. The simulations at room temperature are in agreement with the measurements demonstrating efficiency degradation with an increasing slope at both duty cycles. With temperature increase to 75°C, the self-heating is exacerbated and diminished

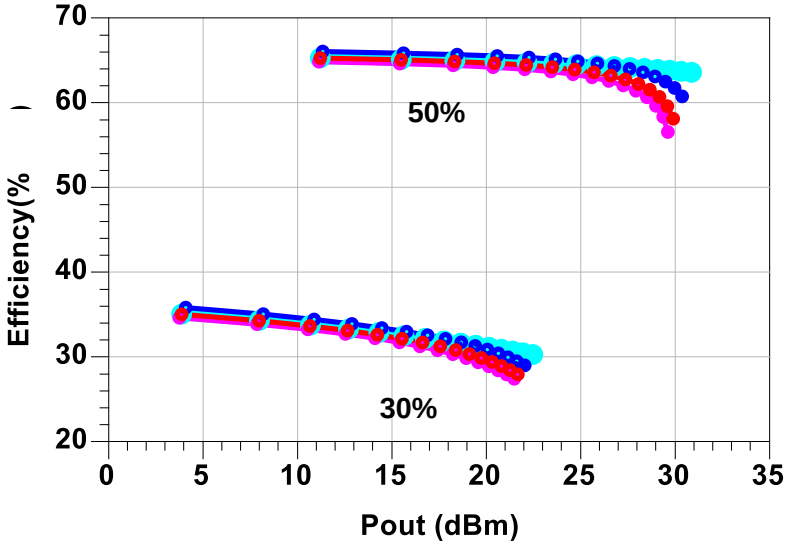

Figure 4-30 Efficiency vs output power for 50% and 30% pulse width for no self-heating (light blue), -78.5°C (dark blue) 25 °C (red) and 75°C (pink)

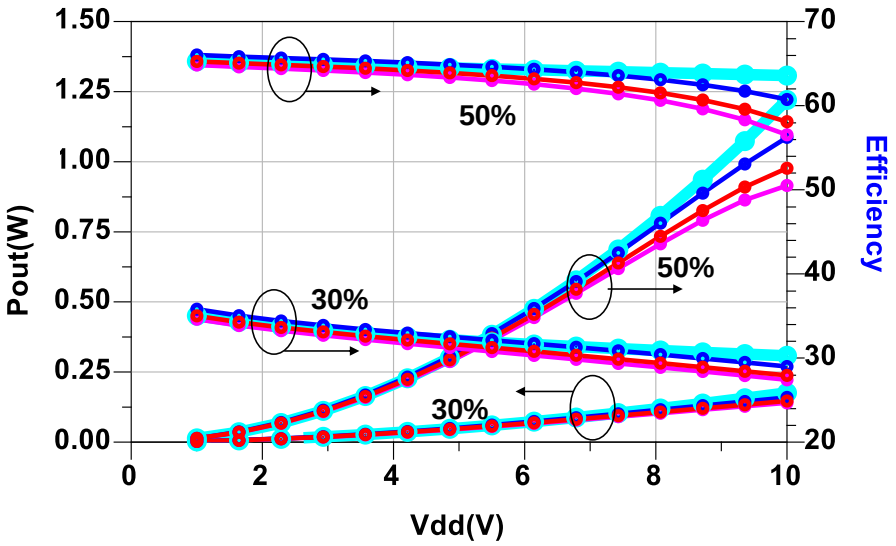

Figure 4-31. Simulated Output Power and Efficiency versus VDD for different temperatures

at negative temperatures (-78.5 °C), presenting a performance close to no-self heating. Figure 4-30 and Figure 4-31 show that the output power and efficiency at 50% and 30% duty cycles are plotted versus different supply voltages for no self-heating and different temperatures. This plot demonstrates that when self-heating is present, the efficiency reduces with supply voltage increase, and the output power is compressed at higher voltages. Furthermore, the pulse-width sensitivity of output power is reduced with increasing supply voltage (Vdd). A low-power, the efficiency profiles have the same slope as they have in the absence of self-heating since, at lower powers, self-heating is not dominant, and capacitance non-linearity is.

4.13 Measurement Results II: A Dry-Iced Experiment

4.13.1 Design of Experiment

To study the effect of self-heating, the measurements are repeated for two temperatures: 25C and with the board placed over dry-ice at -78.5 °C. To the best of the authors' knowledge, this is the first time that self-heating effects are studied for class-E PAs, including the effect of variable supply voltage and duty cycles (pulse widths), and also the first time that the dry-ice measurement technique has been used to investigate the role of thermal effects in an RF circuit. This experiment takes advantage of the knowledge from prior device studies that GaN HEMT devices parasitic capacitance are highly insensitive to temperature variation and simultaneously, transistor loss mechanisms are a strong function of temperature and therefore propose that extreme cooling of the device will enable the observer to eliminate or diminish the heating effect to filter the capacitive effects from the self-heating effects; therefore see clearly where and when each mechanism is present [67]. In order to achieve extremely low temperatures, this work proposes using

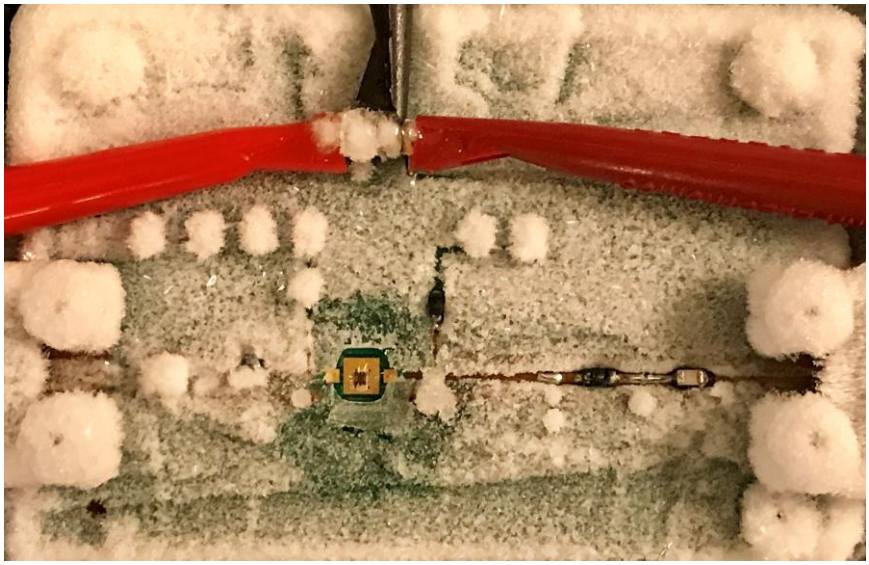

Figure 4-32 Implemented Class-E PA Board over Dry Ice (-78.5 °C)

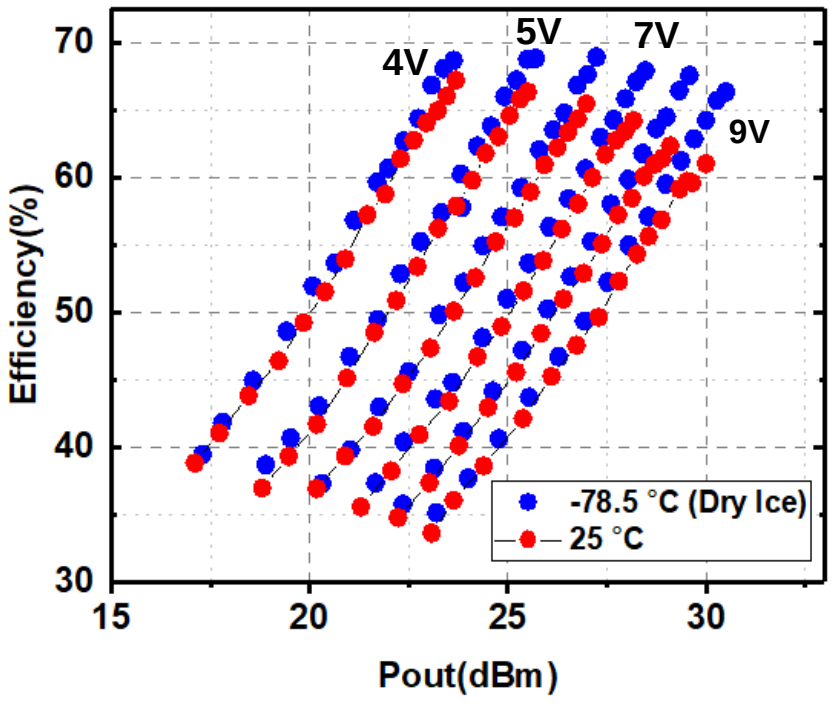

Figure 4-33. Output phase vs. Duty cycle

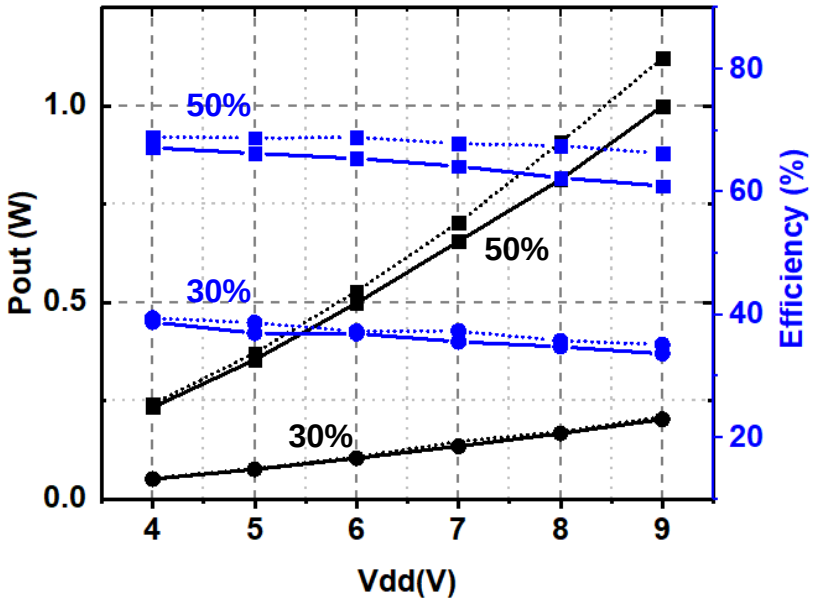

Figure 4-34 Measured Output Power and Efficiency, dry iced (dotted), room temperature (solid), the duty cycles are marked on the plots

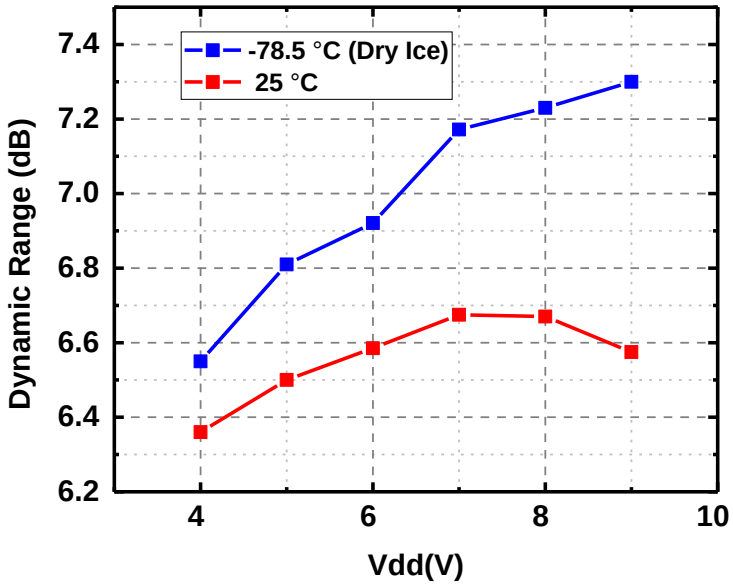

Figure 4-35 Measured PWM Dynamic Range (output power to pulse-width sensitivity)

dry-Ice as coolant agent. Dry-Ice is a solid form of carbon dioxide and sublimates at -78.5 Celsius. Dry-Ice is an advantageous cooling agent since it is commercially available at a low price. Thanks to its solid-form (comes in large chunks), it can be easily handled and placed under the device-under-test's substrate during the measurements. Fig 4-32 is a picture of the board during dry-ice measurements at peak power. It can be seen that the air over the board is frozen, except at the locations with the highest temperature and dense heat distribution. This figure shows that the majority of heat concentration is at the GaN device and the output load.

4.13.2 Results

Figure 4-33 shows the measured PWM PA's efficiency vs. output power for different supply voltages, while the pulse-width is varied between 50% to 30%. Figure 4-34 shows the efficiency and output power variation versus supply voltage at two bounds of the duty cycle (50% and 30%). The results demonstrate that at 50% duty-cycle over dry-ice, the efficiency is relatively constant with Vdd variation, and the output power linearly increases. The room temperature measurements demonstrate that the efficiency drops significantly from 70% to 60% with voltage increase, and the output power begins to compress. The efficiency and output power are almost equal at 4V in both temperatures and diverge with an increasing supply voltage. Thus, the power dissipation increases, proving that the observed efficiency and output power degradation is due to self-heating. At 30%, the duty cycle, the results at both temperatures are almost equal, and both showing efficiency increase with the reduction of the supply voltage. Since the output power is reduced at smaller duty cycles, the self-heating effects reduce with duty cycle reduction from 50% duty cycle in comparison with 30%. This is in agreement with theoretical

expectations: with the temperature increase, the switching loss increases. At higher duty cycles with an increment of ON time of the switch, the power losses increase with higher sensitivity than lower duty cycles. Furthermore, with the increment of duty cycle, the total current passing the switch increases, leading to a higher level of self-heating, thus more drop in conductivity of switch at 50% compared to 30% duty cycle.

Figure 4-35 shows the dynamic range during PWM operation, demonstrating dynamic range compression with an increase of Vdd at room temperature due to self-heating. The measurements at -78.5 °C show no compression and manifest a higher dynamic range with the reduced self-heating at this lower temperature. The increase of dynamic range is due to exploiting the non-linearity of the output capacitance. With the reduction of Vdd, the heating effect at room temperature is reduced, and the dynamic range converges with the iced measurements.

4.14 Conclusion

The concept of multilevel PWM class-E for base-station PAs is introduced and validated through simulation and measurement. This work demonstrates that the PWM class-E's superior efficiency roll-off with power backoff can be exploited to enhance the average efficiency and total dynamic range of multilevel SMPAs and identifies PWM class-E PAs as an excellent candidate for the multi-level operation. The presented concept allows a PWM class-E PA to achieve a higher dynamic range and efficiency by using a minimal number of discrete supplies and switching between them. For the first time, this work also presents an optimized class-E PA for PWM operation to achieve more than 6dB dynamic range in comparison with 2.5dB, 3dB, and 4.8dB from [68],[69] and [39] respectively. The presented PA [70] shows increasing drain efficiency with PBO when fixing the duty cycle

and reducing the supply voltage, thus making this topology a desirable candidate for high PAPR signals. The designed PA and provided measurement results by this work successfully validate the theory and simulations developed by this work. The effect of non-idealities was studied, including self-heating and non-linearity of parasitic capacitances. The self-heating effect on the class-E PAs is studied for different input duty cycles and supply voltage through theory and measurements. This work demonstrates that self-heating causes efficiency degradation and compression of output power and pulse-width sensitivity (i.e., dynamic range) in class-E power amplifiers. This work demonstrates that self-heating significantly increases as the supply voltage is increased from low voltages toward the nominal operating voltage. A comparison of self-heating effects for various duty cycles shows that increasing the duty cycle increases the self-heating in PWM class-E PAs. The presented measurement technique over dry ice demonstrates that the observed performance degradation in class-E PAs with supply voltage increase is due to self-heating. The results in this work suggest that superior thermal dissipaters can enhance the performance of class-E PWM PAs. This work also investigates the input capacitance nonlinearity in digital transmitters. The effect of output capacitance non-linearity on class-E PA performance was presented; this work demonstrated that the efficiency sensitivity to non-linearity of output capacitance decreases with the increment of the operating duty cycle. Finally, a mathematical model was developed for modeling the nonlinear behavior of power transistor input capacitance. The limitations and disadvantages of the traditional effective capacitance calculation method from a single tone system are discussed demonstrated, and a new effective capacitance method is proposed. The dependence of effective capacitance on large-signal input amplitude and offset was presented. Simulation results were used

utilizing the developed mathematical model to demonstrate that the proposed effective capacitance method can effectively predict the input power consumption and wave shape of the driver's signal at the gate both in the presence and absence of an interface network. Furthermore, it was demonstrated that the peak current capability is determined by the maximum capacitance seen by the driver's signal. The time-domain simulation shows excellent wave shape fitting from the nominal effective capacitance presented in this work. The y-asymmetry of the gate drive signal in the presence of non-linear capacitance has been explained. Also, this work shows that a nominal effective capacitance (proposed effective capacitance calculated for an ideal square wave with an ideal interface- short circuit- between the driver and power amplifier) can be used as a practical, effective capacitance, which can return excellent results and estimation of a non-linear capacitance even in the presence of a PA input network, connecting the driver to the PA. This work also shows that the proposed effective capacitance method holds for a wide range of digital transition speeds (slew rate) and input network loads demonstrated by analysis of sensitivity to equivalent inductance and resistance. This work also explains why duty cycle change does not lead to any change in the effective capacitance and emphasizes that for digital drive signals, it is the offset voltage and amplitude of the driver signal determine the effective capacitance seen by the driver signal, rather than the RMS of the input signal.

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