Diamond Schottky P-I-N Diodes for High Power RF Receiver Protectors

by

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ABSTRACT

Wide Bandgap (WBG) semiconductor materials are shaping day-to-day technology by introducing powerful and more energy responsible devices. These materials have opened the door for building basic semiconductor devices which are superior in terms of handling high voltages, power and temperature which is not possible using conventional silicon technology. As the research continues in the field of WBG based devices, there is a potential chance that the semiconductor industry can save billions of dollars deploying energy-efficient circuits in high power conversion electronics. Diamond, silicon carbide and gallium nitride are the top three contenders among which diamond can significantly outmatch others in a variety of properties.

This thesis describes a methodology to develop the 'Simulation Program with Integrated Circuit Emphasis' (SPICE) model for diamond-based P-I-N diodes. The developed model can predict the AC and DC response of fabricated P-I-N diodes. P-I-N diodes are semiconductor devices commonly used to control RF and microwave signals. It has found a very unique place in the list of available semiconductor devices in modern electronics which interestingly shows resistance modulation property in high frequency domain while handling a high-power signal at the same time. The developed SPICE model for the diamond-based P-I-N diode in this project is then used to evaluate the performance of a solid-state passive limiter in shunt configuration which protects the sensitive instruments in 'Radio Detection and Ranging' (RADAR) systems.

Dedicated to my parents and teachers

ACKNOWLEDGMENTS

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CHAPTER 1. INTRODUCTION

1.1Wide Band Gap Materials: Why Diamond?

Now a day's silicon technology is ceding its dominance in power devices to higher- efficiency alternatives called "Wide bandgap (WBG)" materials. *WBG semiconductors* show superior properties enabling power device functioning at very high operating voltages and extreme temperature environments. The use of new semiconductor material over traditional silicon technology will allow very efficient power conversion and electrical energy transformations. Diverse applications range from industrial functions, such as motor drives and power supplies, to automotive and transportation systems including hybrid and electric vehicles, aircraft, ships, and traction, to wireless communications, military systems, space programs, and clean energy generation from solar inverters and wind turbines.

Power electronics is a fundamental industry; absolutely everything that uses electricity employs power management devices of some kind. As such, advancements in power devices enable advancements in an unlimited number of applications. Conventional silicon-based power devices have limitations on maximum blocking voltage, operation temperature and switching frequency [1]. The reported highest Si IGBT breakdown voltage capability is 6.5 kV which is further restricted to operate below 200^0C for proper functioning. The new generation of WBG power semiconductors will allow increasing the efficiency of electric energy transformation by removing the barriers from silicon technology. The current state of the art wide bandgap materials can be compared with silicon technology for key metrics [2] on a spider chart as shown in Fig 1.1.

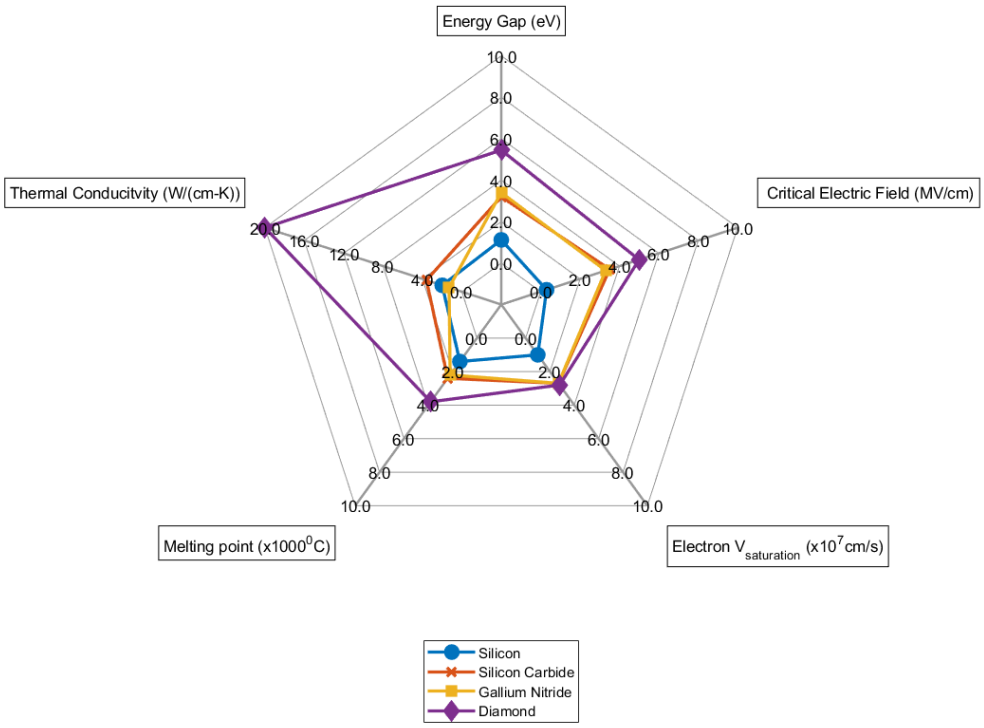

Figure 1.1: Radar Chart Showing Key Metric of WBG Materials.

The chart shown in Figure 1.1 gives a visualization of the superiority of diamond among all other contenders in terms of physical parameters. Table 1.1 shown below summarizes these key metric data:

	Silicon	**4H-SiC**	**GaN**	**Diamond**
Energy Gap (eV)	1.12	3.20	3.40	5.45
Thermal Conductivity ($W\ cm^{-1}K^{-1}$)	2.00	3.60	1.30	20
Critical Electric Field (MV/cm)	0.3	3.5	3.3	5.8-20
Electron Saturation Velocity (cm/s)	1×10^7	2.7×10^7	2.7×10^7	2.8×10^7
Melting point (^{0}C)	1400	2400	2200	3800

Table 1.1: Key Metrics of WBG Materials.

The related high critical field strength of wide bandgap semiconductors leads to devices with low area-specific on-state resistances and low switching capacitances [3] which is very much desirable from power electronics point of view. Diamond with very high critical electric field strength and excellent thermal conductivity is the best WBG material available. These promising properties are the motivation for ongoing research on diamond-based power devices. Diamond based Schottky and *P-I-N diodes* are already achieving remarkable performance during static and dynamic measurement setup shown in several literatures [4] [5].

Alongside the progress being made towards diamond electronics for DC power management, diamond devices are also being developed for high power RF applications. The two-dimensional hole gas (2DHG) formed at the surface of hydrogen-terminated diamond has been used for p-channel FETs with a cutoff frequency, f_T, and maximum oscillation frequency, f_{max}, of 41 GHz and 44 GHz respectively [6]. The 2DHG p-FETs are also capable of high current drive with drain current over 1A/mm [7]. Diamond MOSFET RF amplifiers with 3.8 W/mm of output power at 1 GHz have been demonstrated [8]. These results bode well for RF power amplifiers operating in high-temperature environments, or for high-performance applications that would benefit from the efficient heatsinking enabled by the high thermal conductivity of the diamond substrate.

1.2 Diamond Diodes in RADAR System

Diamond P-I-N diodes are one of the most advanced and promising devices for high power application. P-I-N diodes are also widely used in the RF and microwave domain as

a signal controlling device because of their unique characteristics to behave as bias current-controlled resistors for high-frequency signals. In RF communication systems (RADAR), limiters are a common block sitting in the receiver chain whose function is to protect the sensitive instruments from high power signals as shown in Fig 1.2.

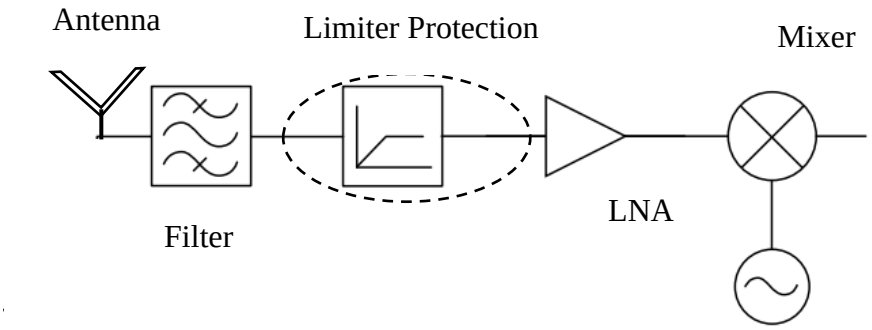

Figure 1.2: Limiter Application in a Simple Radar Receiver Frontend.

Diode receiver protectors can be operated as active attenuators [9] in which an external bias is used to switch the diode from a low insertion loss, off-state, to a highly attenuating conducting state, for which the input power is reflected. Alternatively, back-to-back diodes can be used as self-biased passive attenuators that turn on when high RF powers are present at the input of sensitive receiver elements. Commercial silicon P-I-N diode limiters are widely available for receiver protector applications [10]. Integrated GaAs P-I-N passive limiters have demonstrated for CW input powers of 4 W [11]. Achieving receiver protection for input RF powers in the range 10 – 100W is a challenge for existing semiconductor technologies, in part because of the difficulty in extracting the heat from the diodes caused by the absorbed power not reflected by the impedance

mismatch. Diamond, with the highest thermal conductivity of any known material, may offer a solution for high power receiver protector applications.

The aim of this thesis is to continue research into the characterization and modeling of the response of new diamond-based P-I-N diodes. The developed model is further used to simulate the performance of these diodes in the RF limiter circuits.

1.3 Outline of the Thesis

In Chapter 2, an introduction to the theoretical operation of PIN diodes and the processing steps that were performed at Nano fabrication lab in order to fabricate diamond-based PIN diodes are presented. At the end of this chapter the measurement methodology for the AC and DC characterization of the PIN diodes are discussed. The following thesis uses Keysight's ICCAP DUT modeling tool to acquire real time AC and DC characteristics of the DUT [12] . The DC data was originally acquired using HP semiconductor parameter analyzer 4156A and ***AC data using Agilent VNA [model number]*** and Keithley 236.

In Chapter 3, a generic industrial approach has been utilized to develop a SPICE model for the measured DC and AC characteristics of the diode. Developed model is also flexible enough to predict the diodes capacitance-voltage characteristics. Assuming a lumped model configuration of the diode, important model parameters are first extracted. Then ICCAP's inbuilt SPICE simulator allows the user to develop a complex sub-circuit-based models (using nonlinear elements) along with real time parameters fine-tuning

which updates the simulation data on the fly, giving an excellent way for the user to observe the fitting error.

Finally, in Chapter 4, a working operation and practical integration of the limiter circuit for an RF receiver is described and implemented in ADS. The developed SPICE model - which agrees with both measured AC and DC characteristics, is substituted for the diamond PIN diode in ADS which enables us to measure the performance of the diode for single and double stage limiting operation. Insertion loss, power dissipation and return loss are the important system level parameters that are being characterized and reported [13].

Lastly, Conclusions and future direction of research are presented in Chapter 5.

CHAPTER 2. P-I-N DIODE THEORY, FABRICATION AND CHARACTERIZATION

A semiconductor diode, the most commonly used type today, is a crystalline piece of semiconductor material with a P-N junction connected to two electrical terminals. This P-N junction is fundamental to the performance of function such as rectification and switching in electronic circuits. A P-I-N diode is very similar to a P-N diode, except an extra intrinsic layer (or I -layer) is introduced between the P and N layer as shown in Fig. 2.1. Generally, P and N layers are heavily doped (degenerate) and hence they are of very low resistance whereas I-layer has very low doping levels creating a highly resistive region sandwiched between P and N layers.

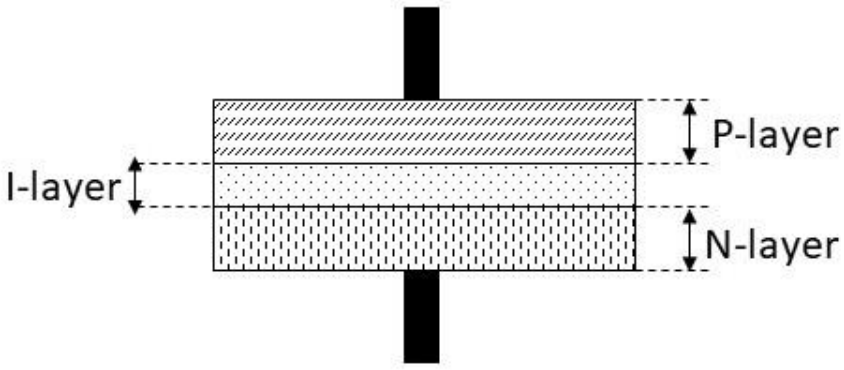

Figure 2.1: Structure of a P-I-N Diode.

This tweak in the design of P-I-N diodes allows it to operate as a variable resistor at microwave frequencies [14]. The PIN diode is often described as an “Incident-Power Controlled, Variable Resistor”. These diodes are optimized to achieve a wide and linear resistance range. Their ability to control high power RF signals makes them suitable for attenuation, modulation, and many other applications with much lower levels of DC excitations [15].

2.1 Device Operation

Figure 2.2 represents electrical symbol of a PIN diode . The P-layer (connected to the anode) and N-layer (connected to the cathode) are heavily doped with acceptor and donor impurities respectively while the I-layer is almost intrinsic in nature.

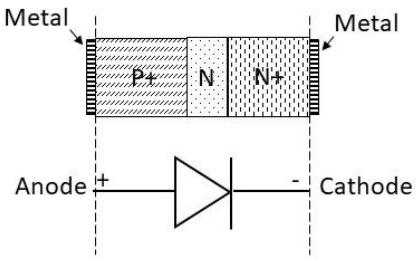

Figure 2.2: Schematic of a P-I-N Diode.

The operation of P-I-N diodes can be understood as follows: Based on the ionized impurity concentration in different regions, a different concentration profile of carriers (holes or electrons) results in the device. Under *zero external bias condition*, if we assume that the device is under thermal equilibrium, then at the interface (P-I and I-N), charge carriers will diffuse from higher concertation (P or N layer) to lower concentration region (I layer) leaving behind impurities which are depleted. This will setup an electric field in opposite direction and cause drift current which will exactly balance the diffusion current (because of concentration gradient) component under thermal equilibrium. It is to be noted that under thermal equilibrium, the potential on the electrode surface on the both sides of the device are equal. The potential difference created by the difference in concentration of impurities in the semiconductor does not appears outside (to the contact) and is often referred as built-in potential as shown in Fig. 2.3.

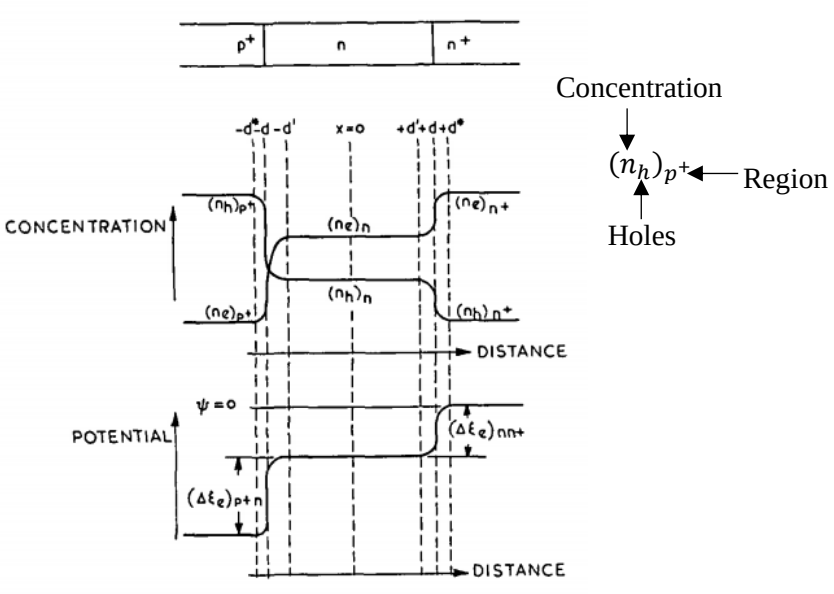

Figure 2.3: Potential Distribution and Carrier Concentration in P-I-N Diode under Thermal Equilibrium [16].

Under *forward bias*, the static characteristic of the diode is determined by the concentration of minority carriers present in any region of the semiconductor. When external bias is applied, the concentration of minority carriers in the all the regions (P-I-N) are affected because of injection which in turn affect the rate of generation and recombination of the carriers. In order to find the current voltage characteristics of the diode, one must consider three separate cases based on level of injection (or bias) as:

a) Low-level injection: When the concentration of injected carriers is less than the thermal-equilibrium value for majority carriers in any region, we have the conditions of low-level injection. Under such scenario the applied bias falls completely across p+n layer thereby reducing the overall potential barrier for charge carriers. Potential and carrier distribution of low-level injection case is shown in Fig. 2.4.

b) High level injection: When the concentration of injected carriers becomes comparable to that of the concentration of majority carrier in n-type region, we have the condition of high-level injection. Potential and carrier distribution of High-level injection case is shown in Fig. 2.5.

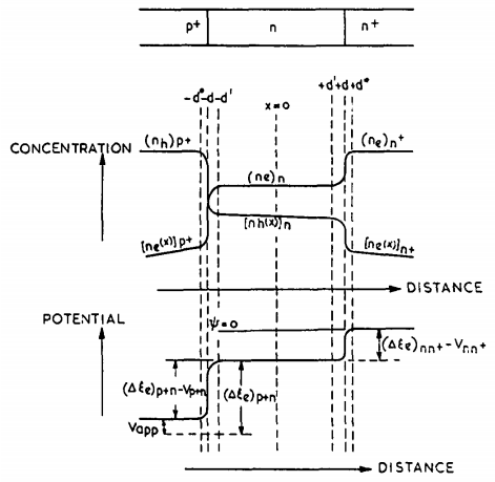

Figure 2.4: Low Level Injection [16].

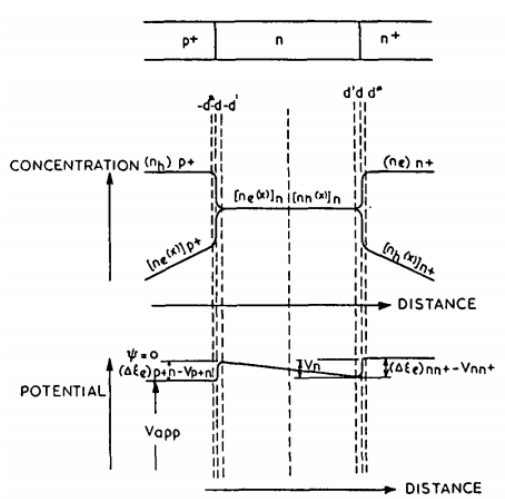

Figure 2.5: High Level Injection [16].

c) Very high-level injection: As shown in Fig. 2.6, when the injected carrier density becomes greater than the majority carrier concentrations in the n+ and p+ regions, we have conditions of very-high-level injection.

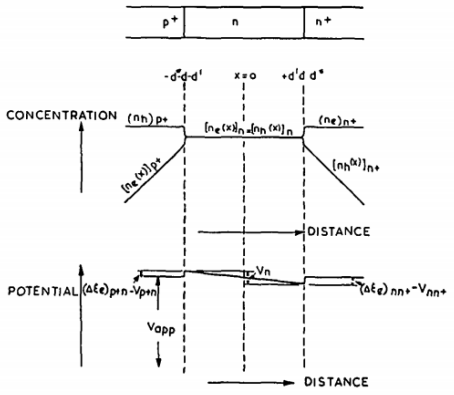

Figure 2.6: Very High-level Injection [16].

Given the potential distribution profile within the diode, one can derive the concentration profile using "*law of junctions"* in terms of the applied bias and equilibrium concentration. The excess carriers getting injected into the device under non equilibrium conditions recombines and give rise to the electric current. So, we can write the total current in the device :

$$\Gamma = \int (\text{Net generation} - \text{ Net recombination}) \times dv \tag{2.1}$$

There are several approximation functions available to describe the integrand of equation 2.1. One such expression is for the process when the electrons and holes recombines through a single recombination level then,

$$(\text{Net generation} - \text{ Net recombination}) = \frac{n_e n_h - n_i^2}{\frac{1}{\alpha_e n_T}(n_h + n_{h1}) + \frac{1}{\alpha_h n_T}(n_e + n_{e1})} \tag{2.2}$$

Where,

n_e: Concentration of electrons, n_h: Concentration of holes

n_i: Intrinsic carrier concentration

n_{e_1}| n_{h1}: constant of mass of mass action law for e and h.

α_e: recombination constant for free electrons

α_h: recombination constant for free holes

n_T: concetration of recombination centers

Thus, a knowledge of carrier concentration profile under non equilibrium conditions will enable us to write the expression 2.2 which in turn can be integrated to find the total current density as a function of applied bias. The Fig. 2.7 shows a generic IV characteristics of a PIN diode derived in [16] based on different levels of minority carrier injection calculated using equation 2.1.

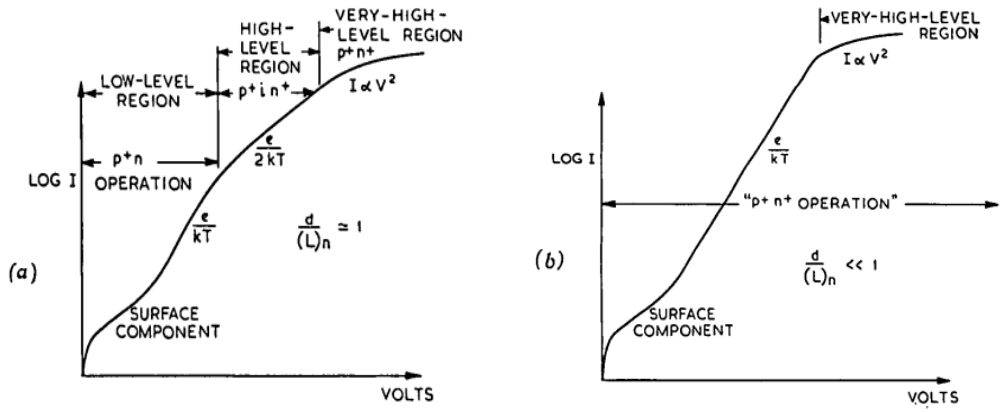

Figure 2.7: Theoretically Approximated IV Characteristics of P-I-N Diode [16]. (a) Device with Comparable Diffusion Length , (b) Thinner I Region and Higher Diffusion Length.

When a *reverse bias* is applied, a majority of the holes and electrons stored in the intrinsic region during forward bias return to the P and N layers. Almost no charge is stored in the depleted I region. Ideally this should result in infinite resistivity, however in reality the resistivity is finite which results in lossy I-region capacitance. At high frequency, device acts like a parallel plate capacitor whose value is almost independent of the applied reverse bias. The value of this capacitance is approximately given by:

$$C_{rev} = \frac{\epsilon \times \text{Area of cross section}}{\text{Width of Intrinsic region}} \tag{2.3}$$

2.2 Device Fabrication

The starting material for fabrication of P-I-N diodes are the commercially available High-pressure, high temperature diamond substrates. Some of the physical properties of HPHT diamond material are shown in Table 2.1 [17] :

Orientation	<111>
Background Doping type	P-type
Substrate dimension	3mm x 3mm
Thickness	$300\mu m$
Dopant	Boron
Peak Impurity concentration	$2 \times 10^{20} cm^{-3}$

Table 2.1: Process Parameters of HPHT Diamond

High-pressure, high-temperature (HPHT) <111> p-type doped diamond substrates with dimensions of 3mm x 3mm and a boron concentration of ~$2x10^{20}cm^{-3}$ were commercially obtained from the Technological Institute for Superhard and New Carbon Materials. The HPHT wafers have a thickness of ~ 300 µm.

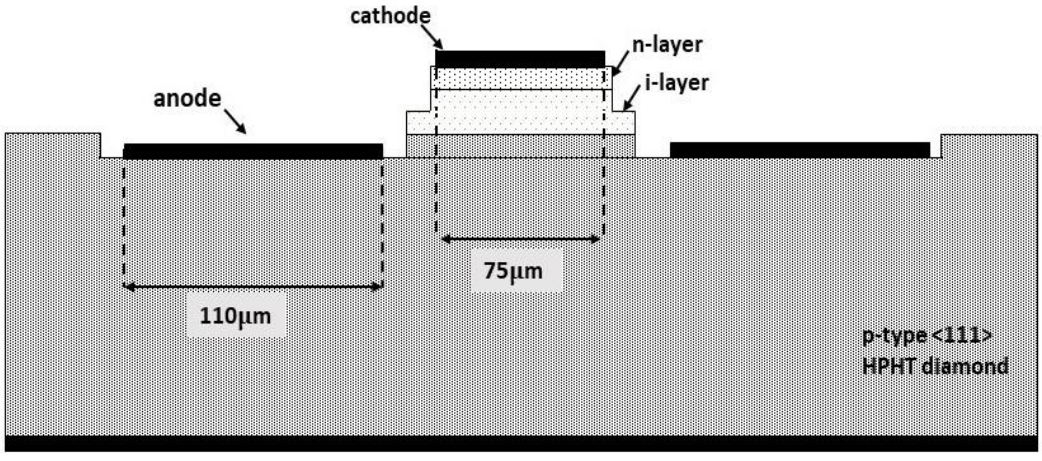

Figure 2.8: Cross Section of the Diamond Schottky P-I-N Diode.

At first, the epitaxial layers of boron doped (~ $10^{20}cm^{-3}$) diamond of thickness ~5μm were grown by Plasma Enhanced Chemical Vapor Deposition (PECVD) technique on the substrate material by Dr. Franz Koech from the physics department at ASU [31]. The intrinsic layer and finally the n+ layer was then grown on the boron doped (p+) layer to obtain a vertical structure of P-I-N diode as shown in Figure 2.8.

A 50nm thick phosphorus doped n-layer was deposited on top of the intrinsic region. The n-type layer has a nominal background doping of > $10^{18}cm^{-3}$and is thin enough to be completely depleted by the Schottky barrier height of the metal cathode. As a result, the diodes behave as a p-type Schottky junction with a lower turn-on voltage compared to P-I-N diodes with a thick n-type region that is only partially depleted at zero bias. These fabrication steps were performed by PhD student Harshad Surdi at ASU Nanofab.

A secondary ion mass spectroscopy (SIMS) analysis was performed on the completed wafer and the concentration of boron and phosphorus as a function of depth into the wafer is shown in Figure 2.9. The SIMS data confirms the high boron doping in the substrate, falling to ~$10^{16}cm^{-3}$ during the growth of the nominally undoped intrinsic i-layer. The phosphorus concentration in the n-layer steadily increases from a background below $10^{-15}\ cm^{-3}$ to a peak of $8 \times 10^{18}\ cm^{-3}$ at the surface. The depth at which the phosphorus concentration equals the boron background concentration gives an n-layer junction depth of 0.28μm, leaving an intrinsic region of approximately 0.22 μm. A peak in the boron concentration within the top 50 nm of the diamond surface suggests that the n-layer is partially compensated, perhaps due to boron dopants from the substrate floating on the growth front during the PECVD deposition.

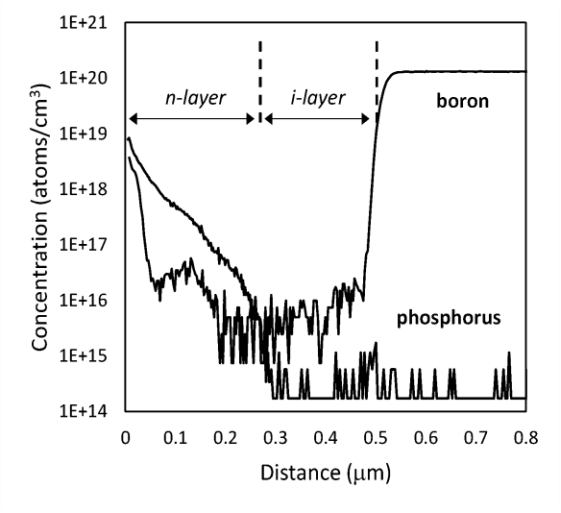

Figure 2.9: SIMS Profile of the Fabricated P-I-N Diode.

Electrical contacts suitable for on-wafer DC and RF probing of the diodes were fabricated as follows. The devices were electrically isolated from one another by a partial mesa etch through the n-type diamond and into the I-layer using O_2/SF_6 reactive ion-etching that defines the diode area. To allow contact to the p-type region from the top surface a second RIE step was used to etch through the I-layer and into the HPHT substrate. Metal layers of Ti/Ni/Au (50nm/50nm/300nm) were deposited by electron beam evaporation to form the cathode and anode contacts to the n- and p-layer diamond respectively. The metal layer to the anode forms an Ohmic contact due to the high doping concentration in the p-type diamond substrate. In contrast, a Schottky contact is formed on the n-type cathode, which is depleted at zero bias forming a so-called Schottky P-I-N diode. The electrical contacts were patterned with a ground-signal-ground (GSG) configuration as shown in Fig. 2.14. The active diode area of $100\mu m \times 75\mu m$ forms the central ground connection, and the center-center pitch between the ground-signal pads is $100\mu m$.

2.3 DC Characteristics and Measurement

The characteristics of P-I-N diode under several bias conditions can be derived with proper set of approximations (under several injection levels) and has been explained here [16]. However, it has been shown that the IV characteristics of a P-I-N diode [18] with relatively narrow I-region can be approximately written in the form:

$$I_d = I_0\left(e^{\frac{q(V-I_d r_s)}{nkT}} - 1\right) \tag{2.4}$$

Where,

n is ideality parameter that changes based on injection level or applied bias,

r_s is the series resistance of the diode,

I_0 is the saturation current,

q is the electronic charge,

k being the Boltzmann constants and

T is the operating temperature.

The electrical characteristics of the diodes were measured by on-wafer probing. The measured DC IV data characteristics are shown in Fig. 2.10. For reverse bias and forward bias up to 6V, the current was measured using an Agilent 4156 precision semiconductor parameter analyzer with a maximum current of 100 mA and a noise floor of ~ 0.1 pA. For higher currents the forward IV characteristics were recorded using a Keithley 2400 with a current limit of 1A. The current limit was reached at a forward bias of 9.2 V and corresponds to a current density of 12.1 kA/cm^2.

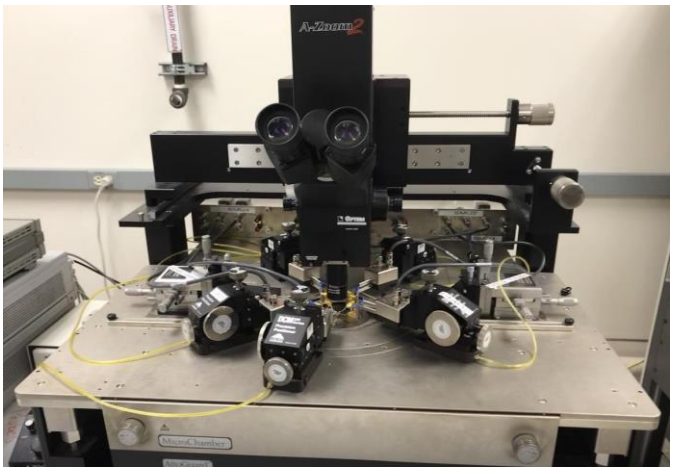

Figure 2.10: DC Probe Station Connected to Agilent 4156 Precision Semiconductor Parameter Analyzer.

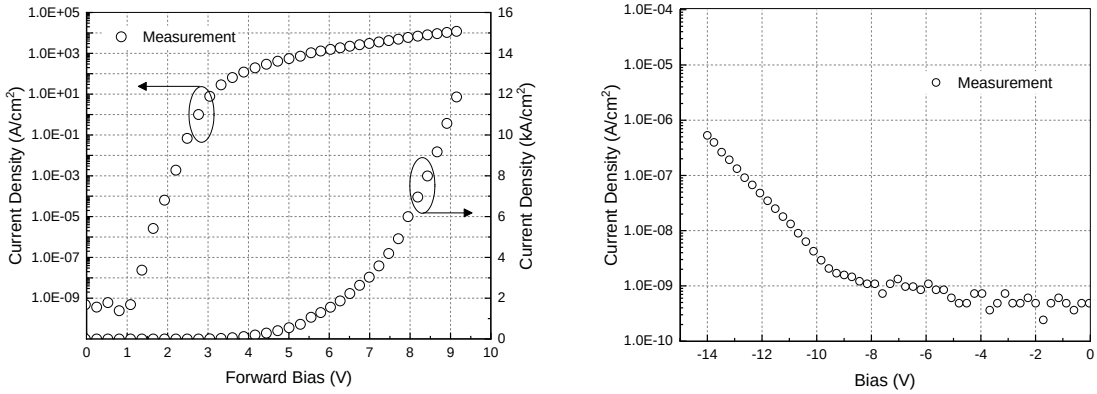

Figure 2.11: Measured DC IV Characteristic of the PIN Diode. Left: Forward Bias, Right: Reverse Bias

It is also important to derive the first order characteristics of the diode called as conductance, G_d. Diode conductance (dynamic) is obtained by differentiating the IV characteristics and is defined as :

$$G_d = \frac{dI_d}{dV} \approx \frac{I_d}{nV_t} = \frac{1}{R_j} \tag{2.5}$$

Where R_j is the junction equivalent resistance. The measured conductance of the diode is shown in Fig. 2.12.

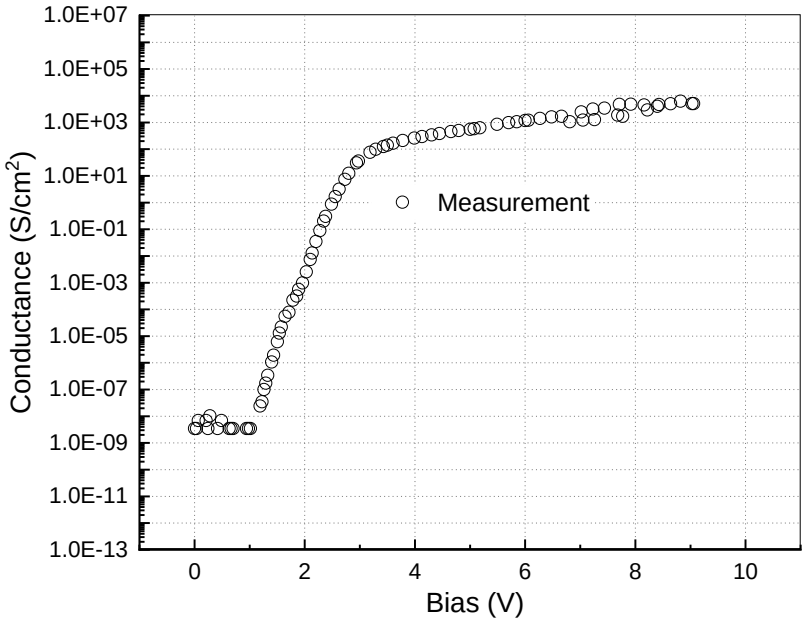

Figure 2.12: P-I-N Diode Conductance Obtained from Measured DC IV Characteristics.

2.4 AC Characteristics and Measurement

From RF point of view, a PIN diode basically acts as a variable resistor. The total resistance of the diode is the sum of resistances from P, I and N region respectively. Since P and N region are heavily doped, they contribute a very small portion to total resistance. However, the resistivity of the I region and thus the total diode resistance is determined by the total number of free carriers in the I region:

$$\rho_I = \frac{1}{q(u_N N + \mu_P P)} \tag{2.6}$$

Where q is the electronic charge and μ_N and μ_P are electron and holes mobility.

The amount of charge stored in the I-layer during forward bias depends on the diode current and the average carrier lifetime,τ. The following equation relates these parameters under steady state conditions:

$$\mathrm{I_d} = \frac{\mathrm{Q_d}}{\tau} \tag{2.7}$$

The average time it takes for the stored charge to decay by ~63% of its initial value is equal to carrier lifetime (recombination time). For a high frequency signal, the number of free charge carriers stored in the intrinsic region does not changes appreciably and remains almost the same as what is set by the DC bias current. If we assume that the width of the intrinsic region to be W, carrier mobility and lifetime be μ and τ respectively, then the value of resistance seen by AC signal can be approximately written as [14] :

$$\mathrm{R_j} = \frac{\mathrm{W^2}}{2\mu\tau\mathrm{I_d}} \tag{2.8}$$

Or this can be written into form:

$$\log R_j = -\log I_d + C \tag{2.9}$$

Finite element-based differential with very small voltage step would give a reasonable approximation of R_j. Hence the value of R_j is determined from Fig. 2.12 which has a monotonic behavior over measurement window. The measured data shows an almost linear relationship on a logarithmic scale between R_j and the diode current obtained from the DC measurements shown in Fig. 2.13.

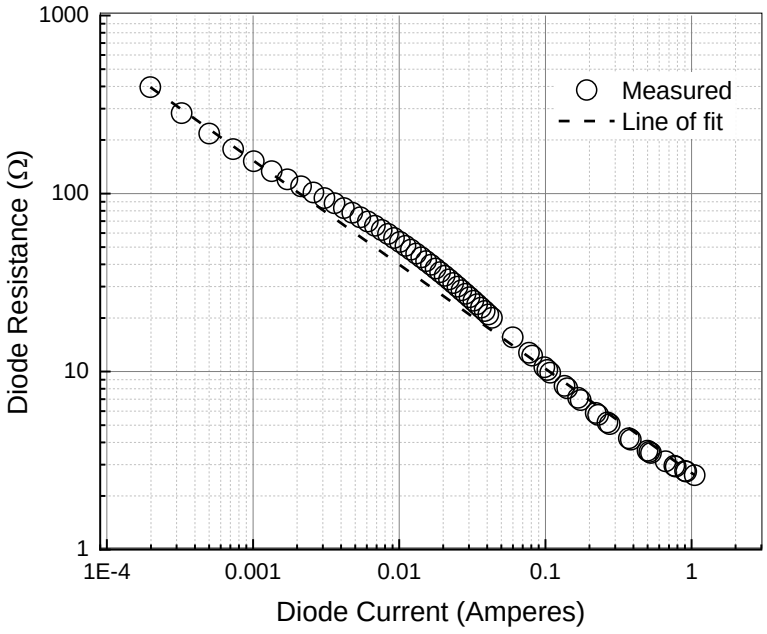

Figure 2.13: Plot of Dynamic Resistance vs Diode Current.

After calibration of the GSG probes (Fig. 2.14) using an impedance standard substrate the S-parameters of the diode were measured from 1G to 25 GHz for a range of DC forward biases as shown in the Smith chart representation of Fig. 2.15.

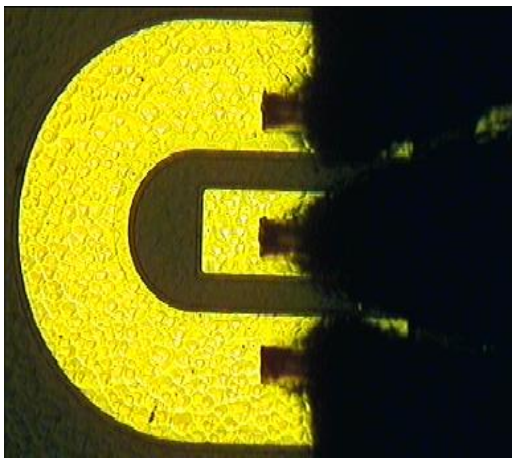

Figure 2.14: GSG Probe Touching the P-I-N Diode for S-parameter Measurement.

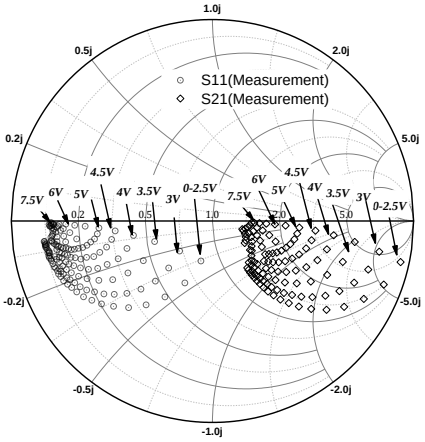

Figure 2.15: Measured S11 and S21 of the Device.

From the S-parameter data, the corresponding Z-parameters were extracted (not shown) using standard formulas [19]. The impedance data was then used to fit the simple lumped-element RC circuit in the inset to Fig. 2.16, using the Keysight parameter extraction software, IC-CAP [20]. In this way the total diode impedance, C_D, can be determined as a function of bias. The resulting CV curves are shown in Fig. 2.16 and are later used to extract the SPICE model capacitance parameters. At zero bias the capacitance of the diode is 16.8 nF/cm^2, and for a relative permittivity of 5.7 would correspond to an I-layer of thickness 300nm, in excellent agreement with the target growth thickness.

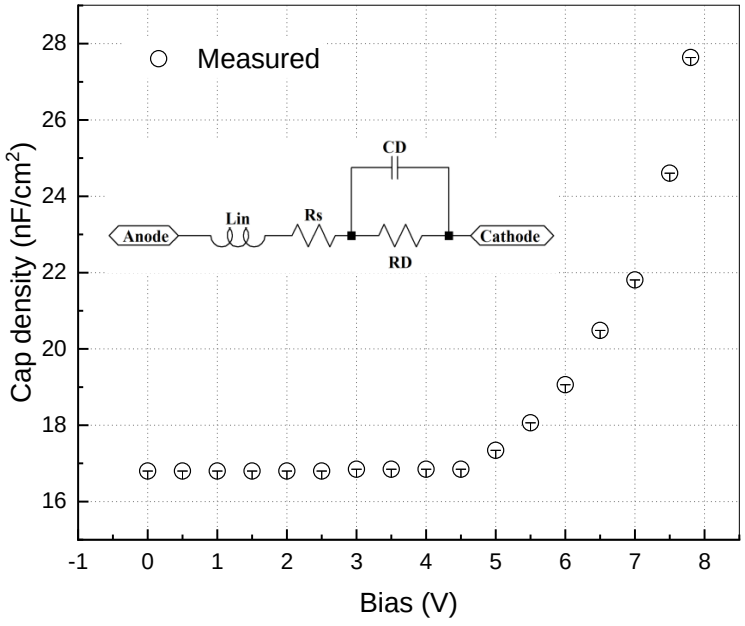

Figure 2.16: Extracted Diode Capacitance as a Function of Applied Bias.

CHAPTER 3. SPICE MODELLING OF THE DIAMOND SCHOTTKY P-I-N DIODE

SPICE is an open-source industry standard analog circuit simulator. It is used to predict the behavior of integrated circuits and integrity of circuit design. SPICE can perform nonlinear DC, nonlinear transient and linear AC analysis of complex circuits. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, lossless and lossy transmission lines (two separate implementations), switches, uniform distributed RC lines, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFETs [21].

SPICE models can predict the IV characteristics of a diode using inbuilt equivalent circuit representation as shown in the Fig. 3.1.

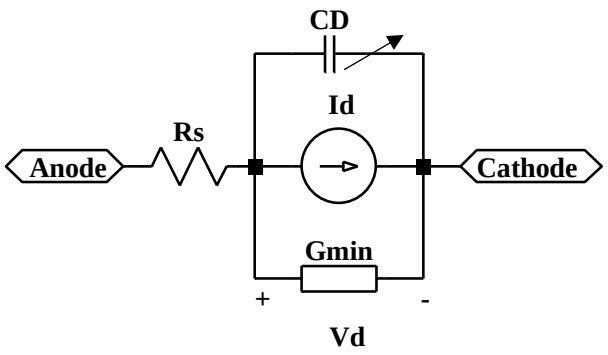

Figure 3.1: Diode Equivalent Circuit Representation in SPICE.

The parameters definitions in diode equations are tabulated in Table 3.1 :

N	Emission coefficient
Is	Reverse saturation Current
Gmin	Parallel transconductance
Rs	Series resistance
TT	Transit time
VJ	Junction Potential
CJ0	Zero Bias Junction cap
M	Grading coefficient
Gmin	Parallel transconductance
BV	Breakdown Voltage

Table 3.1: Diode SPICE Model Parameters.

Different regime of operation of diode in SPICE is shown in the Figure below with its corresponding equation:

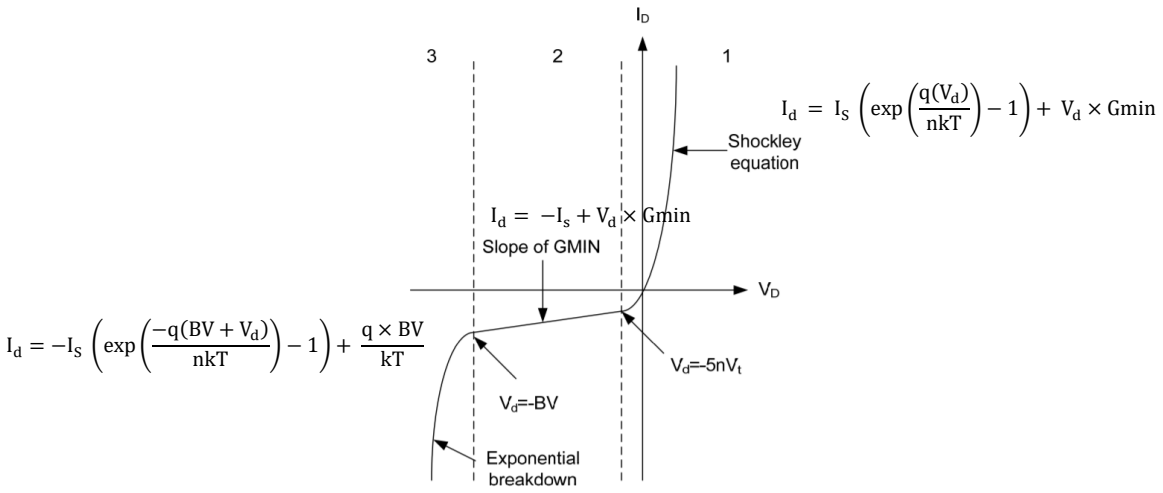

Figure 3.2: Different Regime of Operation of SPICE Diode Model [22].

At this point it can be noted that the diode model in SPICE allows only a fixed value of the emission coefficient, N. This is true when a diode operates in low injection regime. However, in general high-power devices (P-I-N diode for instance) operate in different injection regime and hence the IV characteristics exhibit high level injection behaviors as shown in Fig. 2.7. In practical scenario, to model such kind of non-idealities accurately using SPICE, often complex sub-circuit-based macro models are implemented [23]. We will follow this approach to model the DC and AC characteristics of a P-I-N diode.

3.1 DC Modelling of P-I-N Diode in SPICE

The measured IV characteristics of a PIN diode consists of several regimes of different slope. A subcircuit based modeling approach is required in order to extend the SPICE capabilities to predict the AC/DC characteristics of P-I-N diode. Many electronics devices are not represented by primitives but are still well suited as SPICE models. A SPICE subcircuit is built from a collection of devices that contain primitive models, voltage and/or current sources, and/or other SPICE subcircuits. A generic structure of a subcircuit is shown below :

```
.SUBCKT <SubcircuitName> <Node1> <Node2> <Node3> .. <Noden>
    …  circuit definition …
   .ENDS <SubcircuitName>
```

Figure 3.3: Structure of Sample SPICE Subcircuit.

The DC characteristic (on logarithmic y axis) which consists of multiple slope regions can be modeled by combination of series or parallel diodes by following two rules:

(a) Inclusion of parallel diode: If the measured IV characteristic have a higher current than the ideal diode at a particular voltage, then this behavior can be modeled by inserting a parallel diode to original ideal diode model accounting for higher current. This is shown in Fig. 3.4.

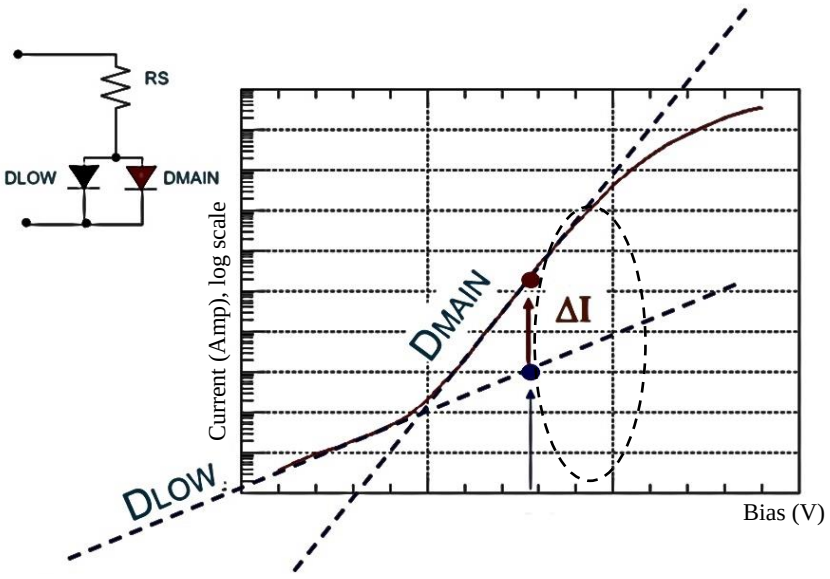

Figure 3.4: Higher Current at Given Diode Voltage is Achieved by Inserting DMAIN in Parallel to DLOW [23].

(b) Inclusion of Series diode: If the measured IV characteristics have a higher voltage than the ideal diode at a particular diode current, then this behavior can be explained by inserting a series diode to original ideal diode model. This is shown in Fig 3.5.

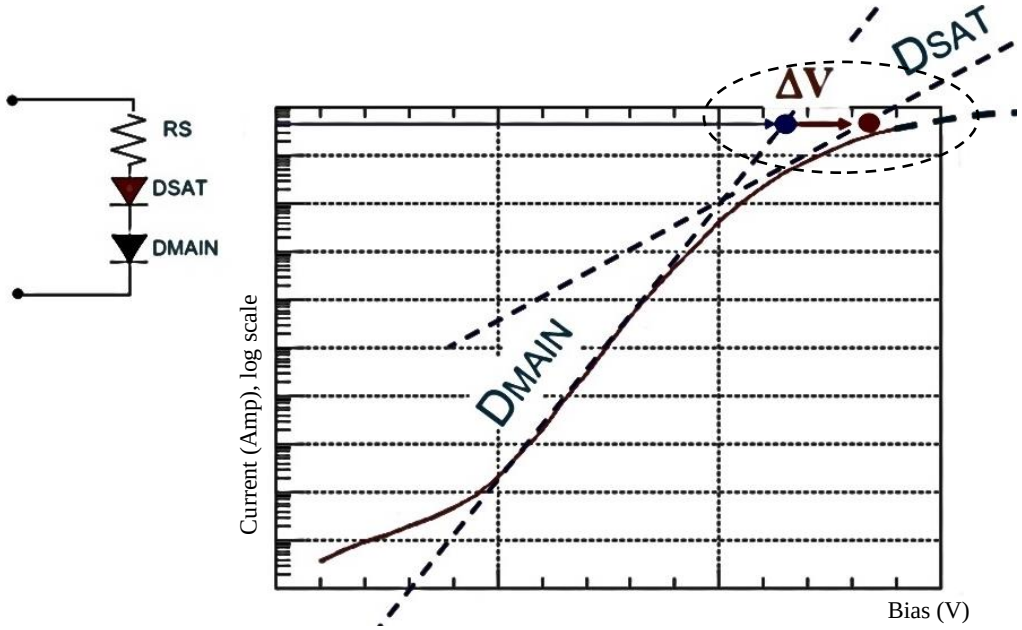

Figure 3.5: Higher Voltage at Given Diode Current is Achieved by Inserting DSAT in Series to DMAIN [23].

The measured IV characteristics of the P-I-N diode shown in Figure[] has evidently four distinct regimes in forward bias which can be modelled by a LOW current diode (DLOW), main diode (DMAIN), a saturation regime diode (DSAT) and finally a series resistance dominated region. The resulting subcircuit prototype which can predict the forward bias behavior is shown in Fig. 3.6.

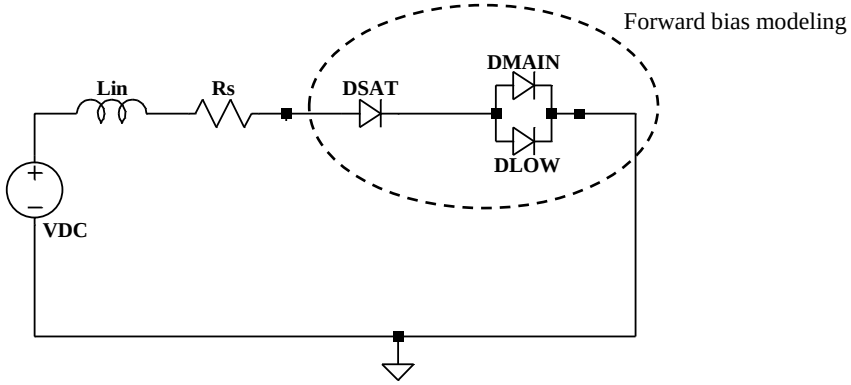

Figure 3.6: P-I-N Diode Subcircuit to Model the DC Forward Characteristics.

It can also be noted that the DC reverse IV characteristics of the diode in Fig. 2.11 consists of two different regimes which must be modeled by two parallel diodes. So, the subcircuit modifies to what is shown in Fig. 3.7.

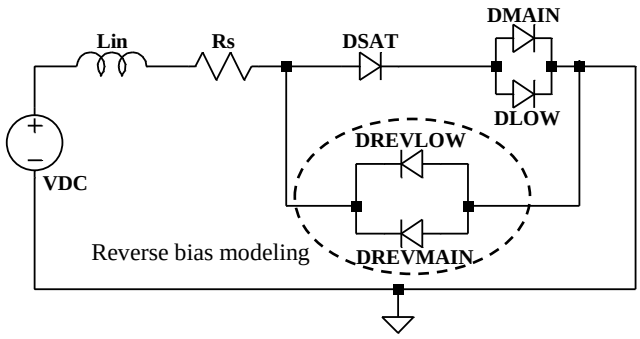

Figure 3.7: P-I-N Diode Subcircuit to Model the DC Forward and Reverse Characteristics.

The Fig. 3.8 shows the results of DC sweep in SPICE for the subcircuit shown in Fig. 3.7. By adjusting the saturation current, IS, and ideality factor, n, for each diode, an adequate fit to the DC characteristic is achieved as shown by the solid lines in Fig. 3.8.

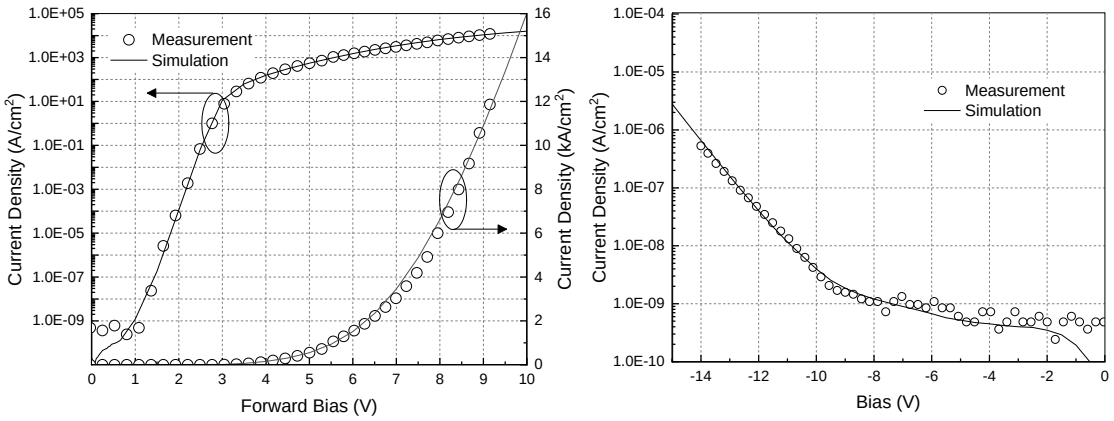

Figure 3.8: DC Fitting to the Measured Data in SPICE Using Subcircuit model. Left: Forward Bias , Right: Reverse Bias.

For diode voltages VD < ~1V the diode DLOW controls the current before the diode starts to turn on, and along with DREVLOW reflects the leakage paths due to defects and/or sidewalls. The diode DMAIN controls the exponential current in the range 1V < VD < ~3V. To reproduce the transition from exponential behavior to the quasi-linear saturation regime controlled by the diode series resistance, 'RS', we use the series connected diode DSAT0. The DSAT0 diode is used to reproduce transport mechanisms not captured by eq. (2.4), including effects due to non-linear p- and n-type contacts, carrier injection and space-charge conduction. The series resistance, 'RS', of the DSAT0 diode is set to be vanishingly small so that the on-resistance of the P-I-N diode is determined by overall 'Rs' as shown in Fig. 3.7. In the reverse bias regime, the parameters for the diode DREVLOW are adjusted to obtain the fit from 0 V to approximately 8 V, while DERVMAIN determines the current for higher reverse bias. Measurements of other diodes (not included here) show a reverse breakdown voltage, VBD, of approximately ~90V due to impact ionization, and we use that value here for the SPICE model.

	D_{LOW}	D_{MAIN}	D_{SAT}	D_{REVLOW}	$D_{REVMAIN}$
IS (A)	2.05×10^{-20}	6.06×10^{-20}	9.55×10^{-3}	2.96×10^{-19}	2.39×10^{-21}
N	8.28	3.01	34.6	29.4	23.8
RS (Ω)	0.001	0.001	0.001	0.001	0.001
CJ0	0	0	0	0	0
TT (ps)	0	0	1.4	0	0

Table 3.2: Diode Subcircuit Parameters for the DC Macro Model.

The diode small-signal conductance, $G_D = \partial I_D / \partial V_D$, is an important device metric that needs to be accurately reproduced by the compact model. Fig. 3.9 compares the

measured and simulated G_D as a function of forward bias diode voltage. The reasonable agreement between the measured and simulated diode conductance suggests the model is sufficiently accurate to reproduce first order differential behavior such as G_D.

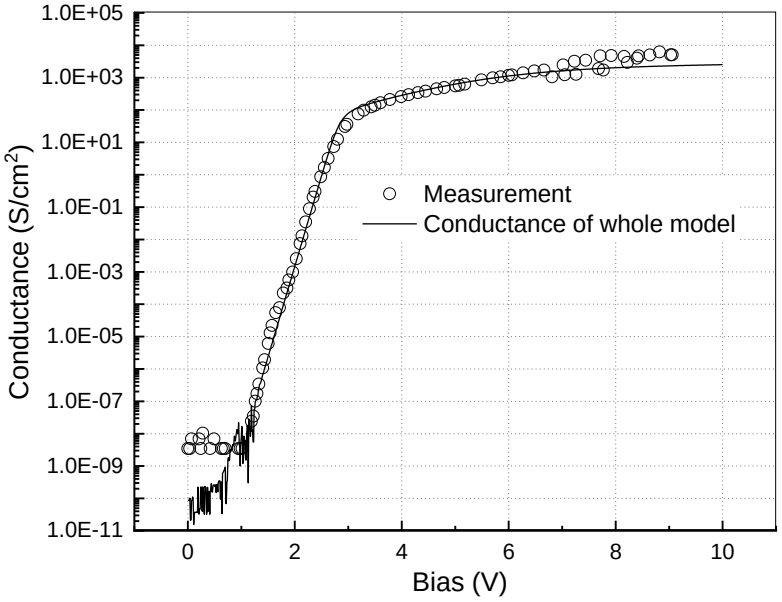

Figure 3.9: The Total Diode Conductance (Open Circles) as Determined by Differentiating the Measured Data in Fig. 2.11. The Solid line is the Diode Small Signal Conductance from the SPICE Model.

3.2 AC Modelling of P-I-N diode in SPICE

To model the small signal characteristics of the device, we must model the capacitance and first order characteristic of the device correctly as the frequency and bias changes. The total capacitance of a junction diode is the sum of the depletion capacitance, C_{DEP}, which dominates at low currents, and the diffusion capacitance, C_{DIFF}, that increases rapidly as the diode begins to turn on. Diode SPICE models use the product of

transit time, TT, and small signal conductance to simulate the diffusion capacitance, while C_{DEP} is derived from the depletion approximation.

$$C_D = C_{DEP} + C_{DIFF} \tag{3.1}$$

$$C_D = \frac{CJ0}{\left(1 - \frac{V_D}{VJ}\right)^M} + TT \times G_D \approx CJ0 + TT \times G_{DSAT} \tag{3.2}$$

Both terms are included in the expression for C_D given in eq. (3.1). From the data in Fig. 2.16, the diode capacitance is constant below ~ 4V indicating that the grading coefficient, m, in the depletion capacitance expression is approximately zero. For this reason, the depletion capacitance is represented by a constant value capacitance, CJ0, connected between the anode and cathode as shown in the circuit of Fig. 3.10.

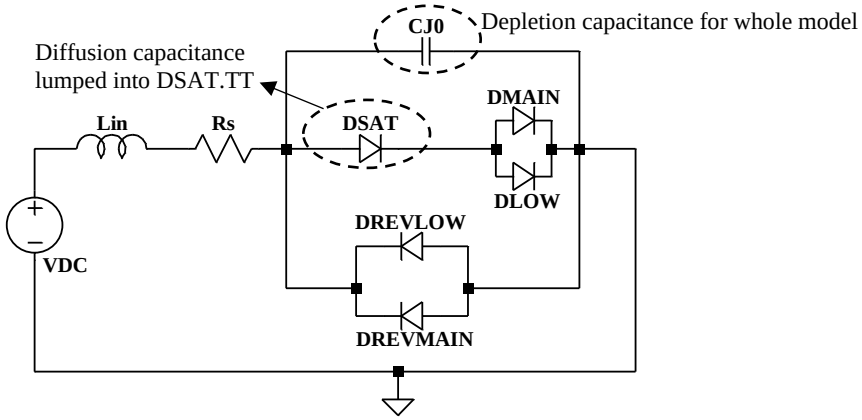

Figure 3.10: P-I-N Diode Subcircuit with Capacitances Modelled.

The increase in the total capacitance that is observed in Fig. 2.16 for VD > 4V corresponds with the turn-on voltage of the diode current seen in Fig. 3.11. In this 'ON' regime the diode conductance is controlled by DSAT, before it is ultimately limited by

the diode series resistance, Rs. For the model developed here the diffusion capacitance is associated entirely with diode DSAT, all the other diode transit times being set to zero. As a result, eq. (3.1) can be modified to the simplified form in eq. (3.2) which we use to fit the data in Fig. 3.11. A transit time of 1.4 ps for diode DSAT reproduces the rapid increase in CD using the diode conductance G_{DSAT}.

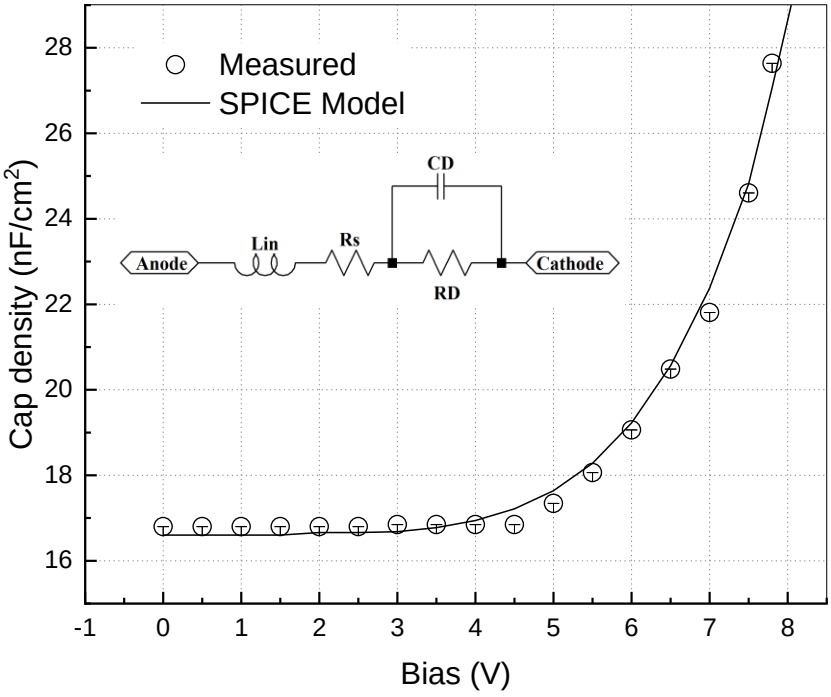

Figure 3.11: The Capacitance (Open Circles) of the Schottky P-I-N Diode Is Extracted as a Function of Bias by Fitting the RLC Model (Shown in the Inset) to the Z-parameters Derived from the Measured S-parameters in Fig. 2.15. (Solid Line Model Fit)

For AC conditions and DC bias VD > 4V the diode model of Fig. 3.10 is consistent with the RLC circuit in the inset of Fig. 3.11. The capacitance of diode DMAIN is set to zero such that it appears as an AC open circuit. At the same time, very little AC signal is dropped across DMAIN because the AC current is limited by the conductance of DSAT for VD > 4V. As a result, the capacitance of the diode sub-circuit is CJ0 in parallel with

$C_{DIFF} = TT \times G_{DSAT}$. The diode capacitance, C_D, of eq. 3.2 is in parallel with the small signal conductance of DSAT, and the total impedance includes the diode series resistance, Rs and negligible series inductance Lin.

The diode shunted co-planar waveguide was configured for two-port RF measurements as shown in the photograph of Fig. 3.12. The forward transmission, S21, and the input reflection, S11, were recorded from 1-25GHz with bias voltages of 0 – 7.8V applied to the diode.

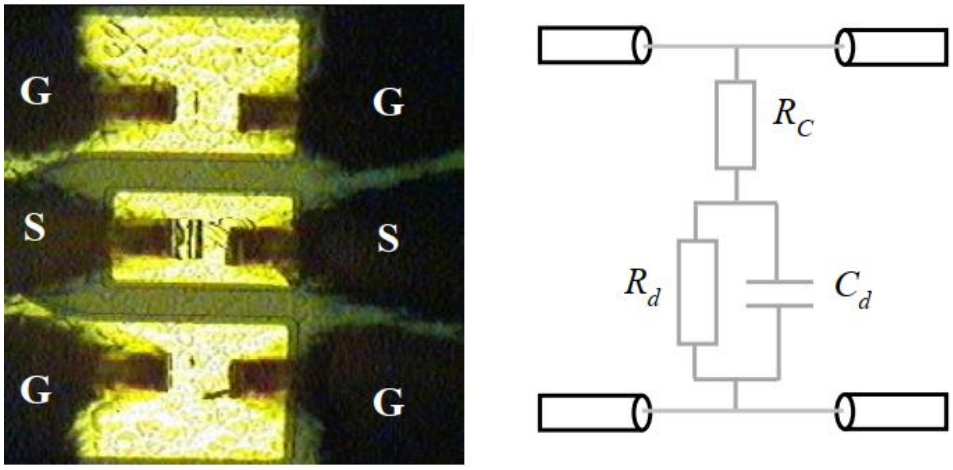

Figure 3.12: S-parameters Measurement Setup.

The s-parameter equation for the structure shown in the Fig. 3.12 can be written as:

$$S_{11} = \frac{Z_0 | \, | Z_d - Z_0}{Z_0 | \, | Z_d + Z_0} \tag{3.3}$$

$$S_{21} = 2\frac{Z_0 | \, | Z_d}{Z_0 | \, | Z_d + Z_0} \tag{3.4}$$

Where, Z_0 is the characteristics impedance of the system and Z_d is the diode impedance.

The measured data is shown as open symbols in Fig. 3.13 along with simulated values of S21 and S11 using the SPICE simulation of diode subcircuit.

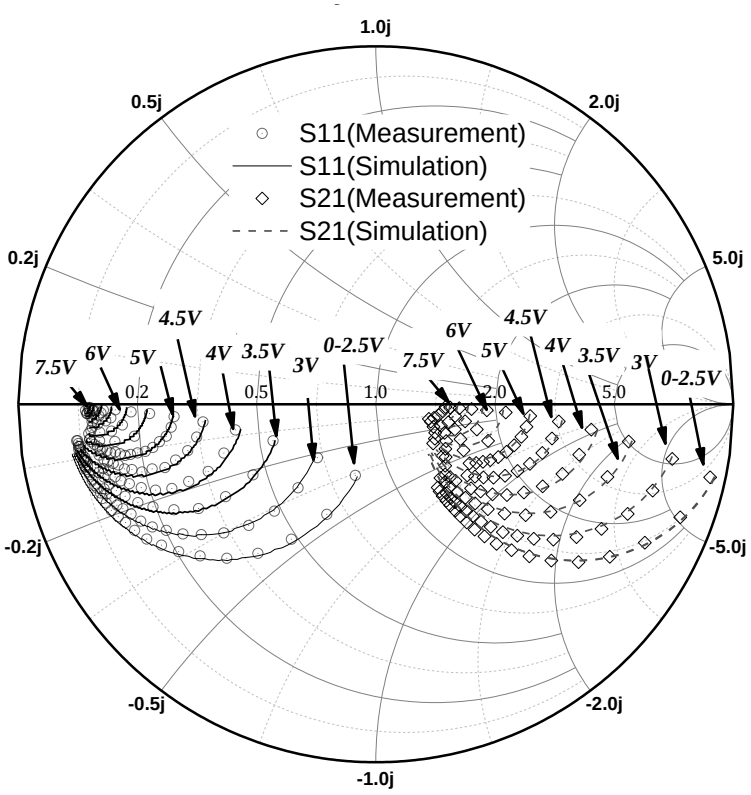

Figure 3.13: Measured and Simulated S-parameters.

When operated as biased controlled attenuators [9] a control voltage is used to switch the diode receiver protector from a low insertion loss, off-state, to a highly attenuating conducting state, for which the input power is reflected. With two GSG probes placed onto the pads the diode behaves as a shunt attenuator connected between the signal and ground lines of the RF transmission line formed by the GSG probes and the coaxial cables. In this fashion the insertion loss, S21, and the return loss, S11, have been measured as a function of diode voltage for a frequency of 1 GHz, see Fig. 3.14. The DC diode voltage is applied by means of a bias-T connected to port-1 of the 2-port measurement system.

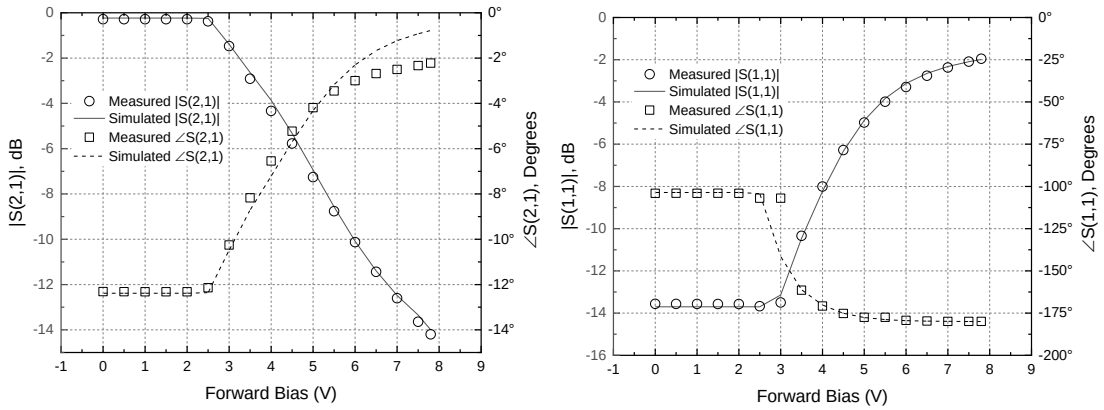

Figure 3.14: S-parameters Fit at 1GHz . Left: Mag , Right: Phase.

As shown in Fig. 3.14 the diode shunt contributes less than 0.3 dB insertion loss until the diode starts to turn on at ~ 2.5V of forward bias. For the highest bias of 7.8V at which the 100 mA current compliance occurs, the diode insertion loss is 14 dB and the return loss is 2 dB. The solid lines in Fig. 8 show the simulated magnitude and phase of S11 and S21 derived from the lumped-element sub-circuit. The good agreement between the measured and simulated insertion loss confirms that the SPICE model sub-circuit of Fig. 3.10 is sufficiently accurate for the design of diamond-based receiver protectors such as the two-stage, self-biasing circuit described in Chapter 4.

3.3 Parameter Optimization and Extraction in ICCAP

IC-CAP (Integrated Circuit Characterization and Analysis Program) is the industry standard for DC and RF semiconductor device modeling. IC-CAP extracts accurate compact models used in high speed/digital, analog, and power RF applications. The following set of steps gives a brief idea about creating and optimizing a SPICE model for P-I-N diode in ICCAP:

(a) To start with the tool, a new model must be created in main ICCAP window as shown in Fig. 3.15.

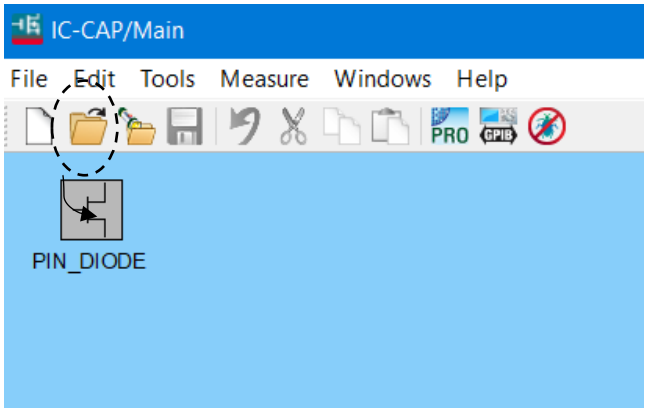

Figure 3.15: Creating New Model in ICCAP Main Window.

(b) For the newly defined model, we need to create several setups each corresponding to our measurement scenario as shown in Fig. 3.16. These are followed by input/output specifications.

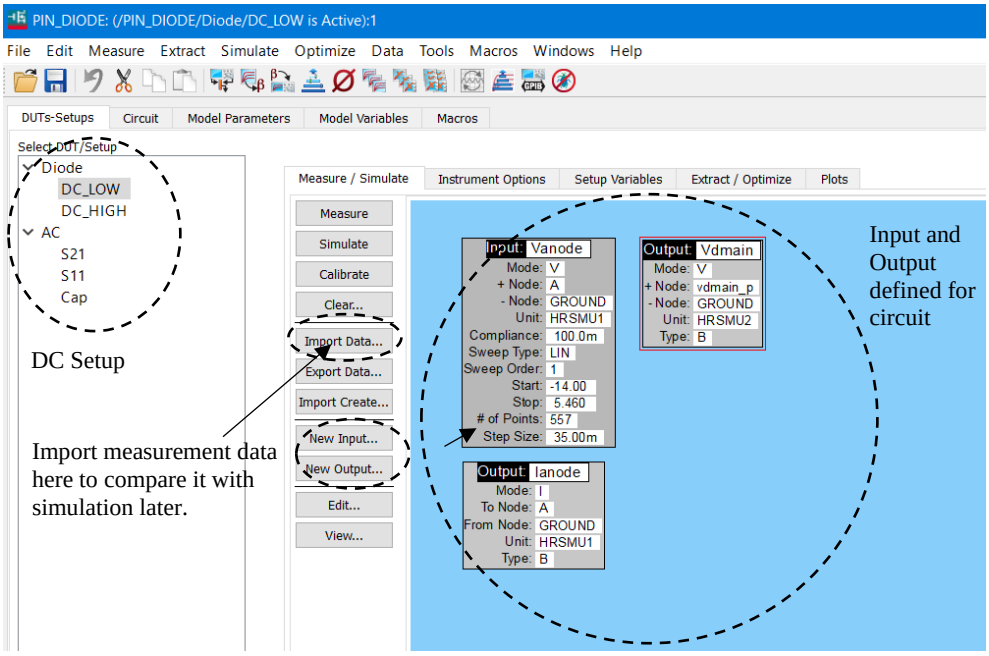

Figure 3.16: Creating New Setup and Defining Input and Output Variables in ICCAP DUT.

(c) After defining the top-level input and output specifications, a complete SPICE netlist with all the primitive elements is defined in Circuit section of the Setup. Note that this is a global definition, and it holds same for all the setup. The P-I-N diode model netlist developed for this work is shown below:

```
.OPTION limpts=3000 gmin=1e-14

*Initialize subcircuit with ports connected to what is defined in Input/Output specification at top
level
.subckt model_schottky_pin 1=A 2=C 12=vdmain_p

*Short port 1 to port 2 to create a Transmission line structure
Rshort 1 200 0.001
Lshort 200 2 1p

*port 1 model: port name: 1 with parasitic
Rin 1  10 5
Cdiode 10 0 1.4pf
Ccross 1 2 1f
*****************************************************************
* diode sub circuit
*****************************************************************
*forward bias modeling
DSAT0 10 12 DSAT0
DMAIN 12 0 DMAIN
DLOW 12 0 DLOW
*reverse bias modeling
DREV 0 10 DREV
DREV2 0 10 DREV2
*****************************************************************
*model cards (need to be optimized later)
.MODEL DMAIN D IS = 4f  N = 4.3 BV = 1000  IBV = 1m
+ RS = 1.1 CJO = 680f VJ = 2.164 M = 0.01  FC = 0.5 TT = 0
+ EG = 1.110  XTI = 3.0

.MODEL DLOW D IS = 10p N = 60 BV = 1000 IBV = 52E-3
+ RS = 0.1  CJO = 0 VJ = 2.164  M = 0.9 FC = 0.5 TT = 0
+ EG = 5 XTI = 3.0

.MODEL DSAT0 D IS = 15m N = 30 BV = 1000  IBV = 52E-3
+ RS = 0 CJO = 0  VJ = 2.164 M = 0.9  FC = 0.5  TT = 0
+ EG = 5  XTI = 3.0

.MODEL DREV D IS = 30a  N = 15.5  BV = 1000  IBV = 52e-4
+ RS = 2 CJO = 0 VJ = 2.164 M = 0.5 FC = 0.5 TT = 0
+ EG = 1.110 XTI = 3.0

.MODEL DREV2 D  IS = 30a N = 15.5 BV = 1000  IBV = 52e-4
+ RS = 2 CJO = 0 VJ = 2.164 M = 0.5  FC = 0.5 TT = 0
+ EG = 1.110  XTI = 3.0

.ends
```

(d) We can define additional variables in “Model variables” tab which are specific to the whole model and can be tuned in later optimization stage. In this case we are just defining the simulator to be used as SPICE (Available options are : LTSPICE, HSPICE, PSPICE etc). Once can also define parameters like TNOM to vary the nominal temperature during optimization process.

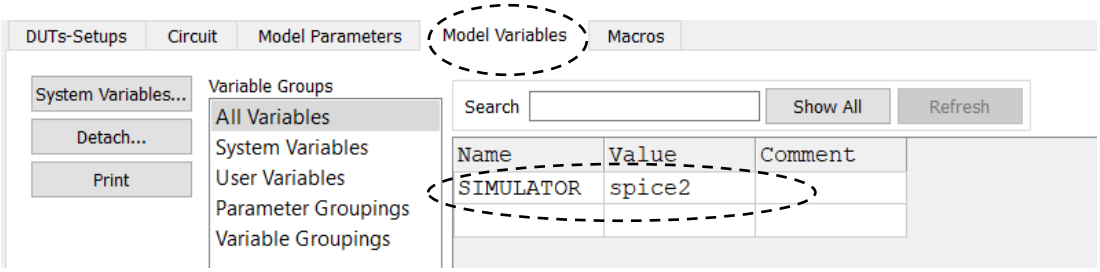

Figure 3.17: Defining Model Variables.

(e) The next step is defining all the plots. This will help us to visualize the output variable between measurement and simulation. The plot definition is straightforward as shown in Fig. 3.18.

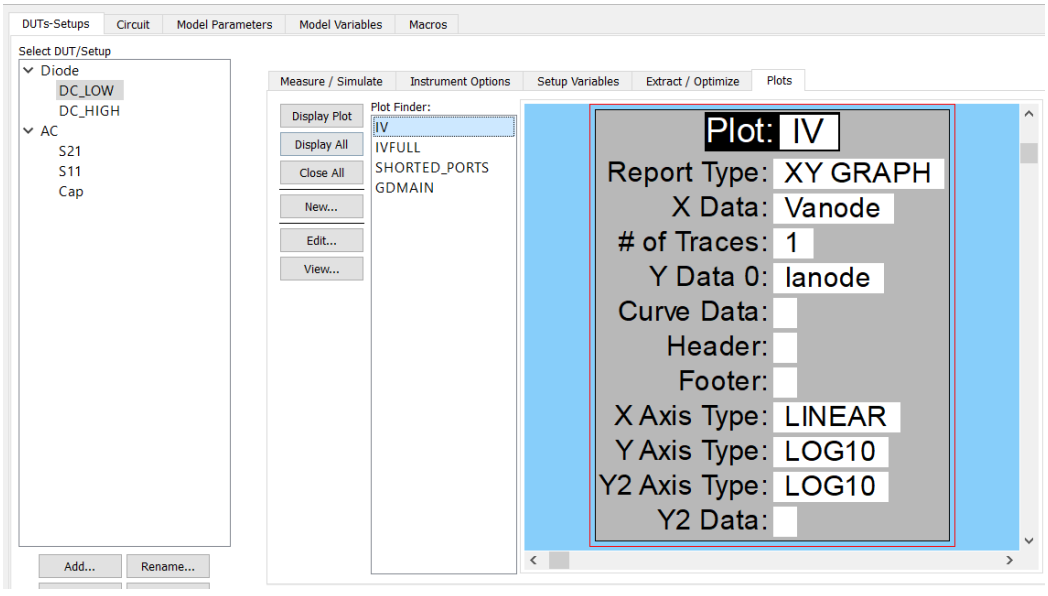

Figure 3.18: Plot Setup for Plotting DC IV.

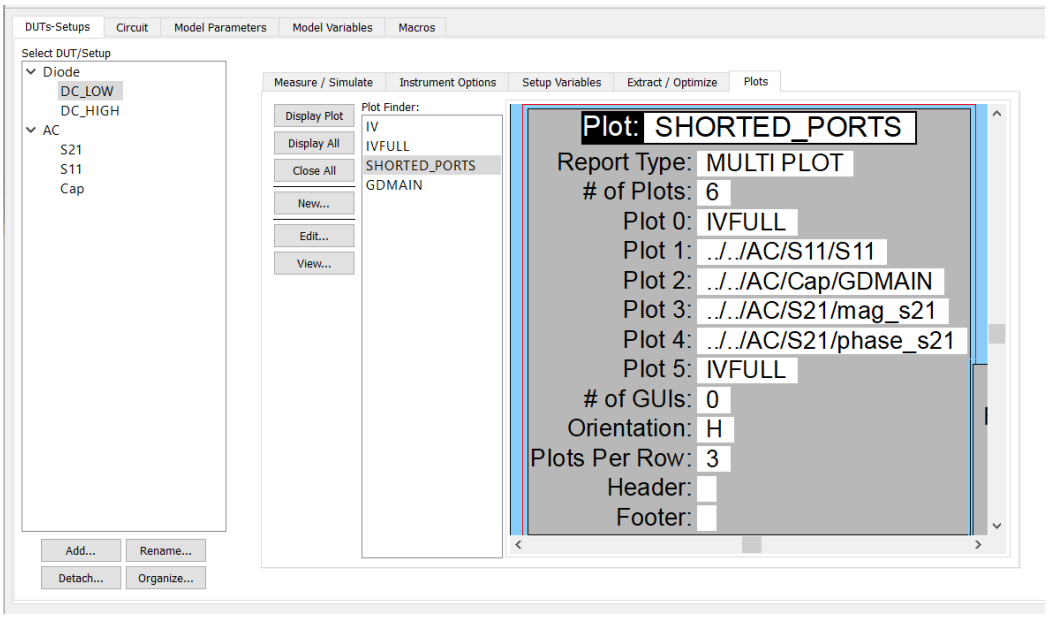

Figure 3.19: A Sample Multiplot Window to Plot all the Optimizing Output.

(f) Once the setup is done, we hit simulate button and open a particular plot that we want to optimize. In this case, the Fig. 3.20 is showing a multiplot where we want to optimize all the output variables at once, namely: DC-IV, S-parameters, and Capacitance vs Voltage.

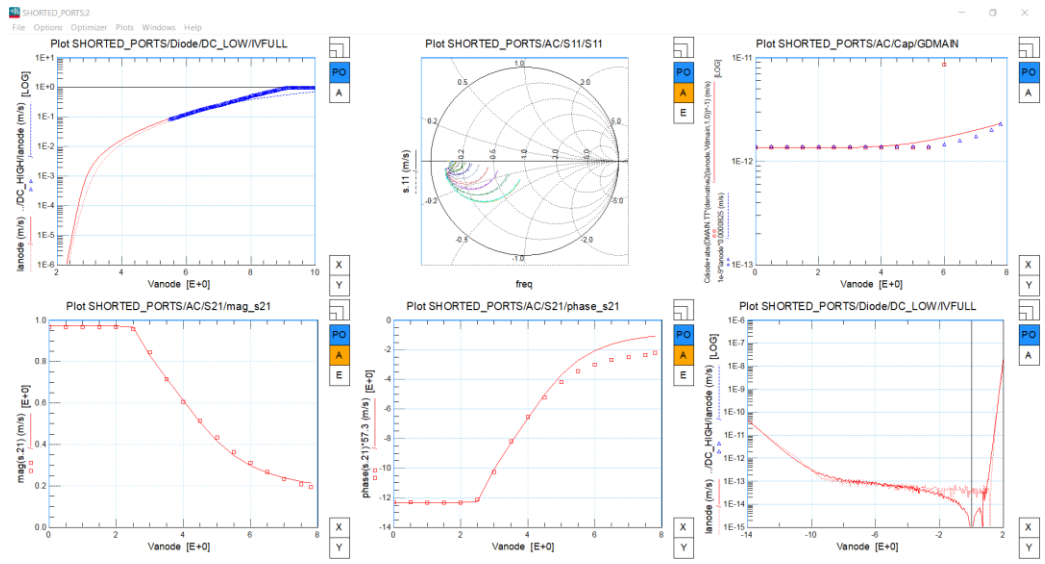

Figure 3.20: A sample Plot Window Showing Measurement and Simulation Data Fit.

(g) The plot obtained in step(f) shows the measurement data superimposed with simulation solid lines. Initially these traces will be way off (because we have no information about model parameters in the start) and optimization needs to be done in order to bring them closer and reduce the model error. The optimization task is invoked by choosing optimization as shown in Fig. 3.21.

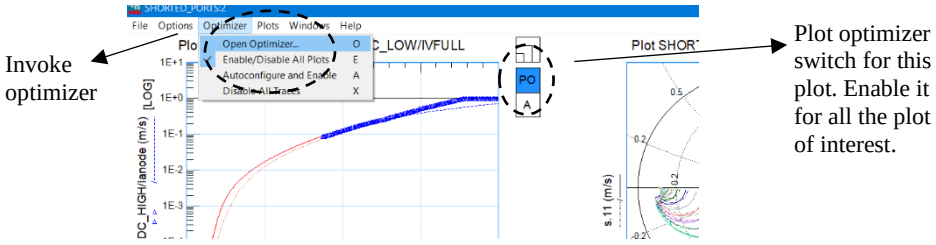

Figure 3.21: Invoking Optimizer.

(h) After launching the optimizer, we must add the parameters that needs tuning for the output plot. These parameters can come from subcircuit level, model level or user defined level as shown in the Fig. 3.22. We then launch tuner after adding relevant variables into the optimization list.

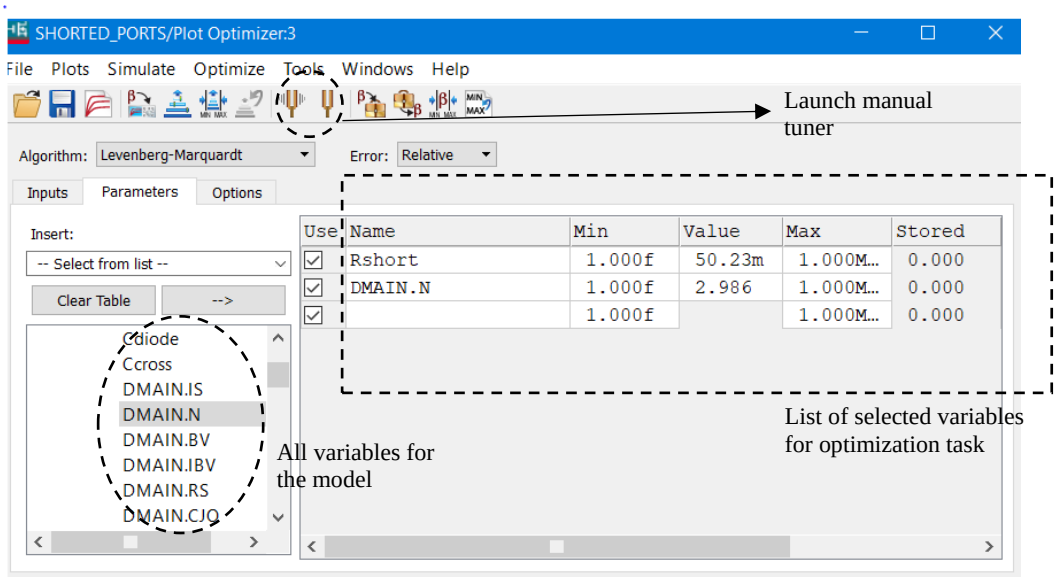

Figure 3.22: Adding List of Variables for Optimization.

(i) Upon executing tuner, ICCAP updates the simulation result in the plot immediately as soon as any parameter are tuned from the tuner tab. This is a manual process but allows us to observe the impact of model parameter on the output variables and help us to move in the direction where the model fits the measured data.

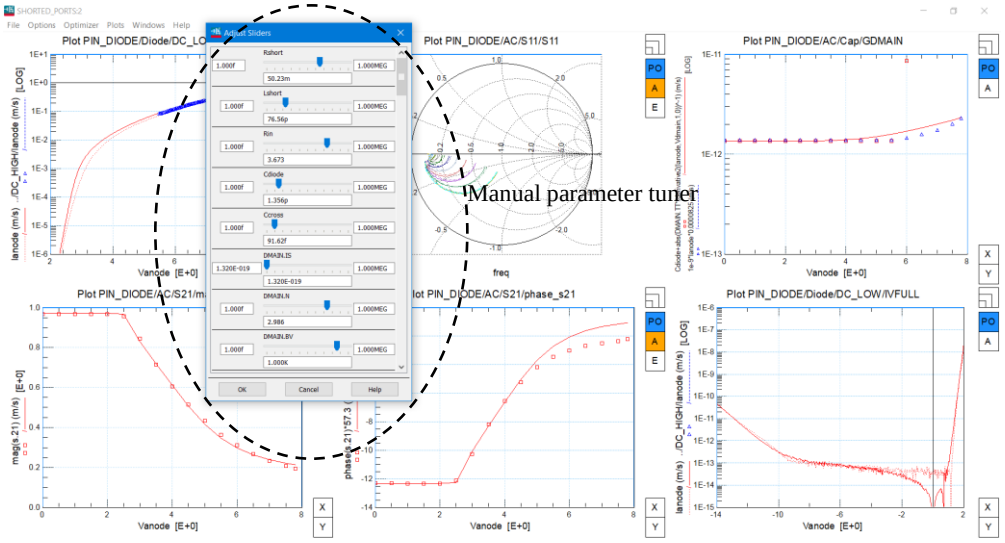

Figure 3.23: : Manual Tuning for Optimization.

(j) If the upper and lower limit of optimization parameters are known to some accuracy(step (h)), then one can launch the optimization task in ICCAP which finds the model fitting solution automatically with least square error as shown in Fig 3.24.

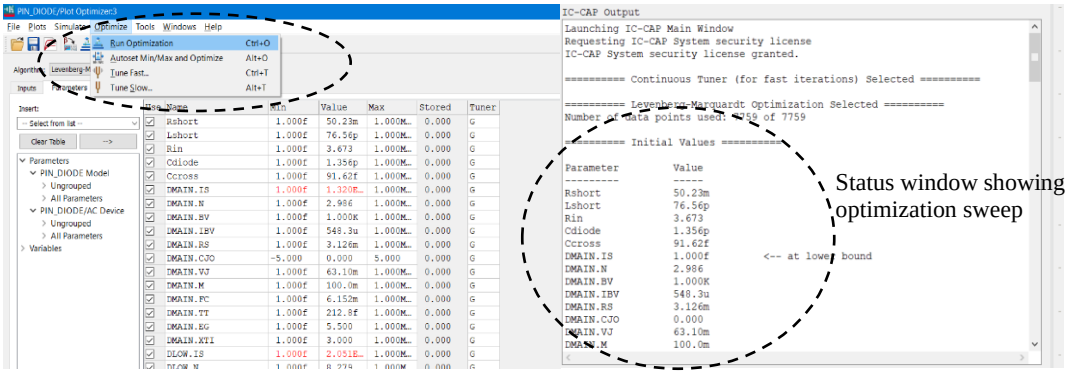

Figure 3.24: Running Automatic Optimization Task.

For the P-I-N diode used in this research, the optimized parameters are shown in Table 3.3 obtained after series of steps explained above.

	D_{LOW}	D_{MAIN}	D_{SAT0}	D_{REVLOW}	$D_{REVMAIN}$	D_{CJ0}
IS (A)	2.051E-020	6E-020	9.55e-3	2.959e-019	2.388e-021	1e-30
N	8.279	3.01	34.55	29.39	23.81	100
BV (V)	90	90	90	90	90	90
IBV (A)	5e-3	5e-3	5e-3	5e-3	5e-3	5e-3
RS (Ω)	1e-3	1e-3	1e-3	0.2	4.4e-005	1.37e-12
CJO (F)	0	0	0	0	0	2.26e-12
VJ (V)	11.08	11.08	11.08	11.08	11.08	11.08
M	1	1	1	1	1	0.159
FC	0.95	0.95	0.95	0.95	0.95	0.95
TT (s)	0	0.13e-12	0	0	0	0
EG (eV)	5.5	5.5	5.5	5.5	5.5	5.5
XTI						

Table 3.3: Final Optimized SPICE Model Parameters for the P-I-N Diode Subcircuit.

CHAPTER 4. P-I-N DIODE APPLICATION: RECEIVER PROTECTION

A typical receiver used in RADAR systems is designed to sense very small signal amplitude. The sensing circuitry often contains fragile semiconductor blocks which are very sensitive to electrical signals (can typically resolve ~μV). However, these systems must also be capable of handling huge signals incident on them. To make the receivers robust enough to handle large signal powers, receiver protection limiters are the ultimate choice. The receiver protection limiter, most often referred to simply as a limiter, can protect the receiver from large input signals and also allow the receiver to function normally when these large signals are not present [24].

Modern transceivers, whose transmitter and receiver blocks are tuned to same frequency, usually has limiter protection circuitry in them. The necessity of limiters can be best understood from the block level diagram shown in the Fig. 4.1.

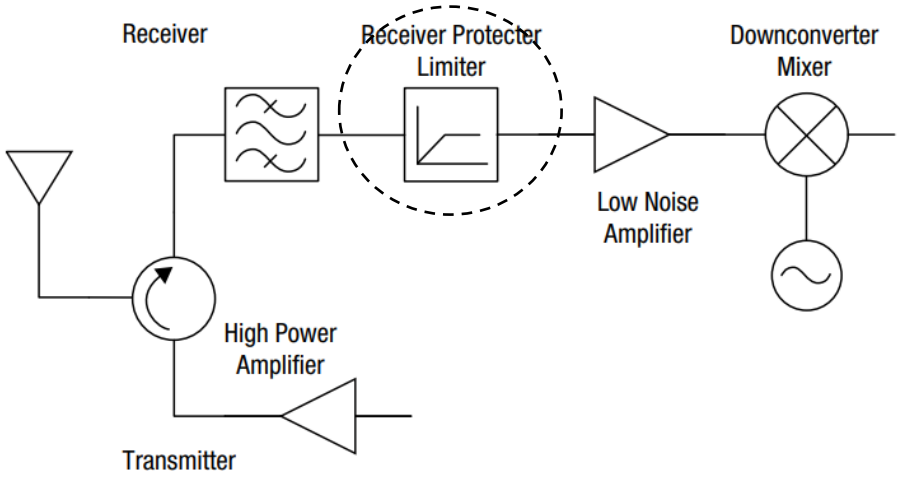

Figure 4.1 :An Overview of a Typical RADAR Transceiver with Limiter [25].

The architecture shown above has transmitter and receiver blocks sharing a common antenna. When operated in transmit mode, the antenna usually sends out a very strong signal (order of ~100 Watts to kWatts). On the other hand, the receiver circuit components are designed to handle very low signal levels being sensed by the antenna. The received signal is first processed by a low noise amplifier (LNA) where the signal first hits the gates of transistors. In the case of very high input power (when a small portion of transmit power that gets coupled to receiver) to the LNA, the transistor gates may get damaged and lead to permanent circuit failure. To prevent such a scenario, limiters are often employed which can protect the following sensitive circuits in the receiver chain.

Diamond PIN diodes are ideal for limiter circuit applications because of their low on resistance and extreme power handling capacity. The maximum power-handling capability of a limiter circuit is principally determined by the sizes of PIN diodes chosen for the design. A large diameter PIN diode is able to conduct more current than a smaller diameter diode and is therefore able to survive higher RF drive levels. However, the larger the diode size, the more shunt capacitance in the circuit and the less available bandwidth. The secret to optimum limiter design is selection of diode sizes to meet power handling capability without greatly exceeding this requirement. By choosing the correct diode size for the intended application, excess shunt capacitance will not be added, and insertion loss will be minimized.

4.1 Receiver Protection

A limiter controls maximum instantaneous voltage or current, never allowing it to exceed a certain value. Wide ranges of input voltage or current to this device produce output voltage or current varying over only a specified range. So, the primary objective of having a limiter is to have amplitude limitation (Current or Voltage).

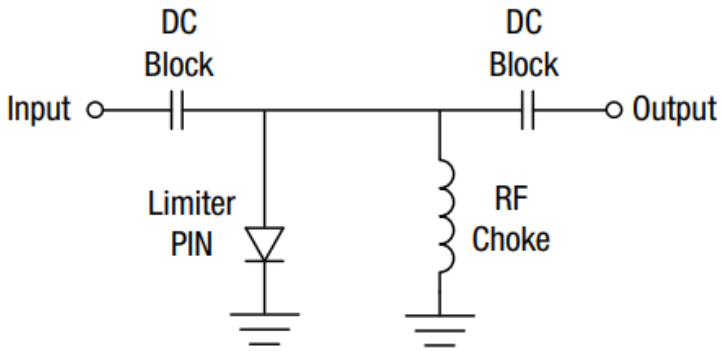

Figure 4.2: A Single Stage Limiter [25].

One of the simplest forms of limiter is shown in Fig. 4.2. The circuit comprises of a P-I-N diode and an RF choke in shunt to the main signal line. The limiter diode can be thought of as an incident power controlled variable resistor. So, when the input signal is very weak, diode presents its maximum impedance resulting in least insertion loss. If the input signal temporarily becomes huge, the diode is forced to move into a low impedance state producing an impedance mismatch at the line input. In this case the electric field of the signal temporarily forces positive charge carriers (holes) from the diode P layer and negative charge carriers (electrons) from the diode N layer into the nominally undoped, high impedance I layer, causing the impedance of the diode to be temporarily reduced to

a much lower value. This causes the majority of the incident signal to get reflected back to the source. An output characteristic of interest for this kind of limiter is shown in Fig. 4.3 where output power is plotted with respect to varying input power on logarithmic scale.

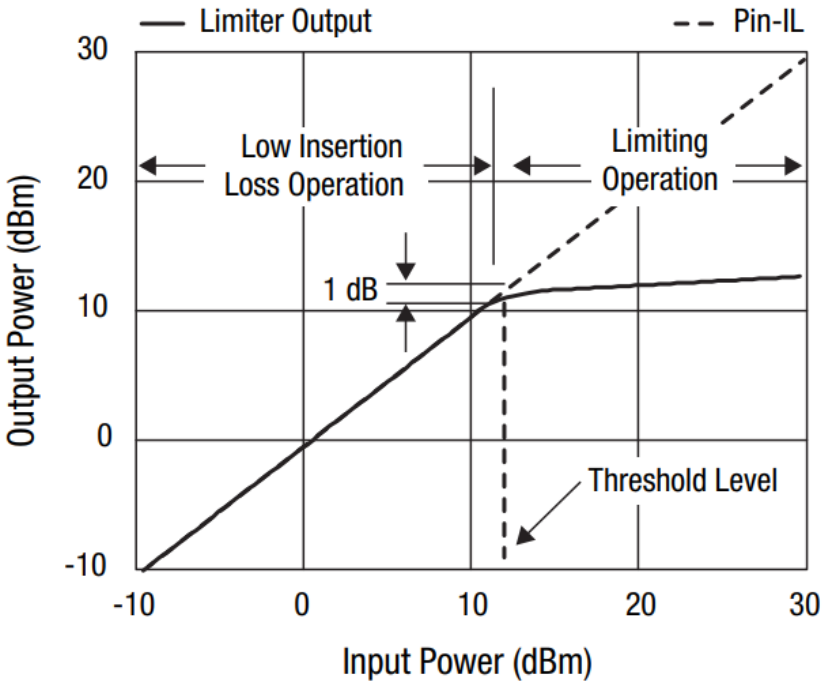

Figure 4.3: Transfer Characteristics of a Limiter [25].

When the large input signal is no longer present, the impedance of the diode reverts from a very low value to its maximum value after a brief delay. It is important to note that when a large input signal is present, the limiter diode reflects majority of the power, but some power gets dissipated in the diode itself. The main advantage of using diamond-based P-I-N diode is that one can go to very high input power level and the operation of limiter still remains intact as diamond substrate can easily handle high power level.

It is to be noted that the minimum and maximum impedances of the limiter PIN diode are determined by the geometry of the diode as well as the resistivity of the diode's I layer. In the simplest approximation, the PIN diode can be modeled as a right cylindrical section with three separate layers: The P layer, the I layer and the N layer, where the resistance of each layer is given by:

$$R_{layer} = \frac{Resistivity_{layer} \times Thickness_{layer}}{Area_{layer}} \tag{4.1}$$

4.2 ADS Simulation

To simulate and evaluate the performance of limiter circuits in ADS, an instance of diamond-based P-I-N diode is created as shown in Fig. 4.4 whose optimized SPICE model predicts the AC and DC behavior of the diode.

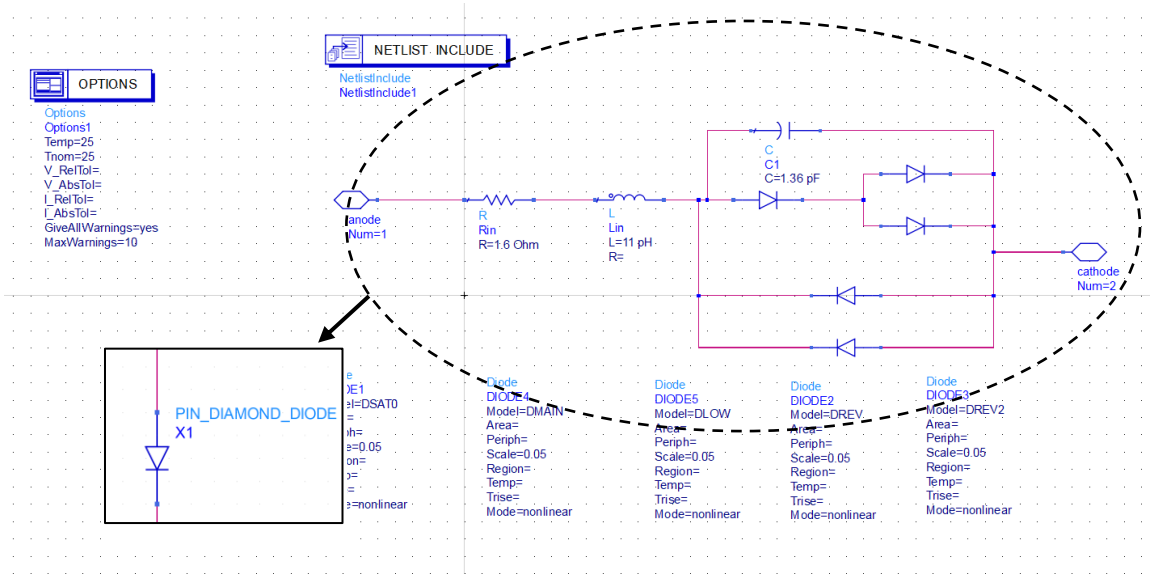

Figure 4.4: Diamond P-I-N Diode Instance Defined in ADS.

A two-stage limiter can be designed to maximize limiting, power-handling capability, and bandwidth [26]. Fig. 4.5 show schematics for a two-stage limiter. In this topology, at small signal drive levels the diodes and transmission lines form a low-pass filter structure. The transmission line length and impedance are used as series inductance with the diodes providing shunt capacitance.

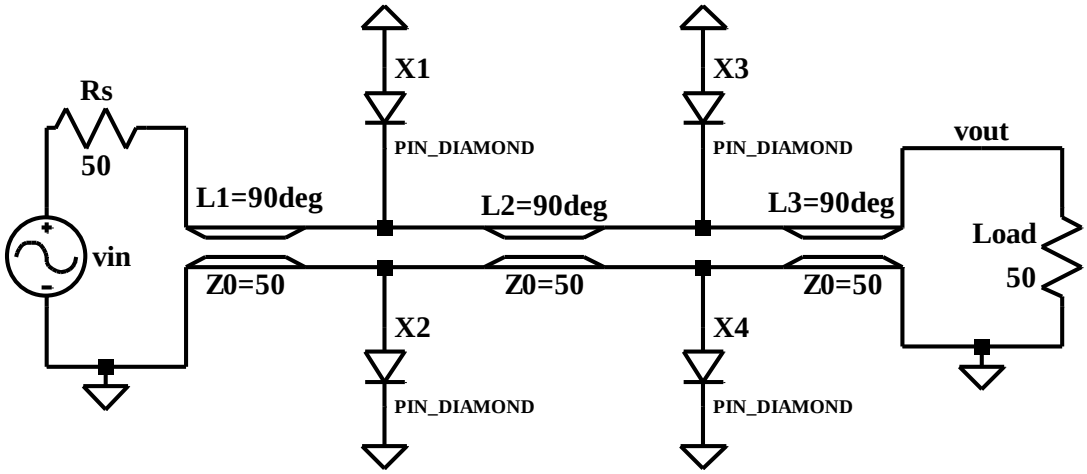

Figure 4.5: Two Stage Limiter Setup with λ/4 Transmission Line.

To evaluate the performance of a diamond-based receiver protector the sub-circuit of Fig. 4.4 is used to simulate the power transfer characteristics of the circuit in Fig. 4.5 operating at 1 GHz. The power delivered to a 50Ω load as a function of input power is plotted in Fig. 4.6 along with the total power dissipated in the receiver protector circuit. At input powers above 100 mW the output power starts to be attenuated. For Pin=100 W the power delivered to the load is 0.51 W, with 29 W dissipated in the diodes of the receiver protector and the rest being reflected at the input.

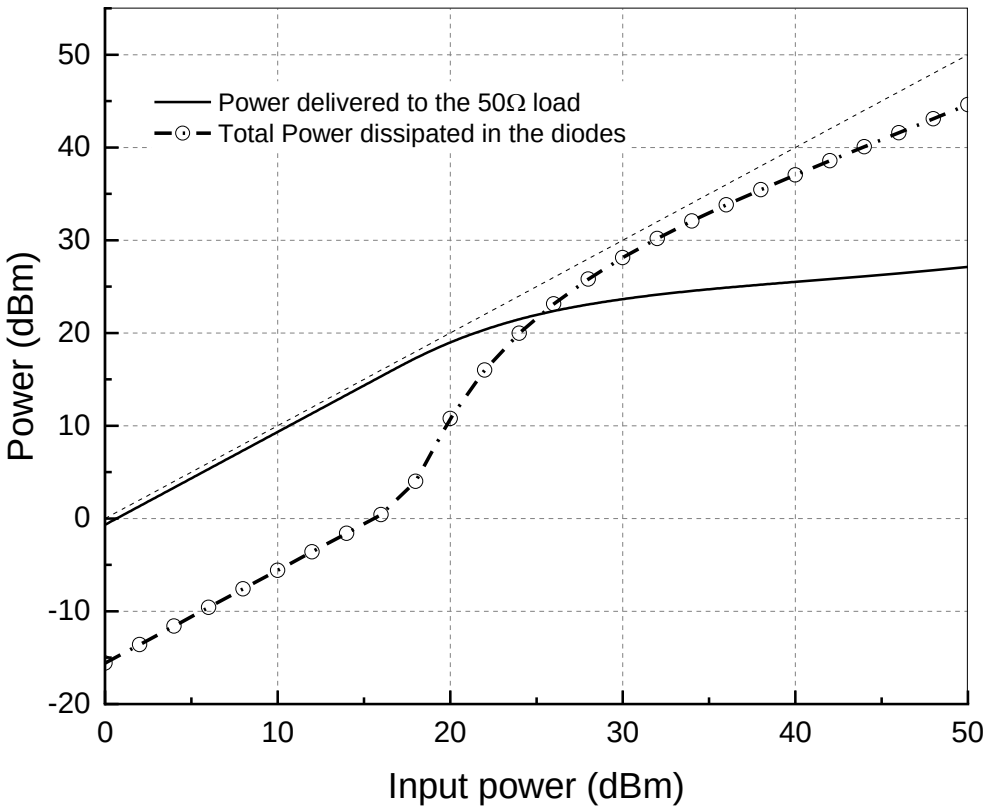

Figure 4.6: Simulated Power Attenuation of the Two-stage Diamond P-I-N Diode Limiter Circuit.

4.3 Performance Comparison

The power dissipated in the diodes of the receiver protector leads to Joule heating, and the resulting increase in temperature will ultimately limit the operation of the receiver protector. It is for these high-power applications that diamond substrates, with their high thermal conductivity, will provide important systems level benefits. To compare the increase in temperature for different substrate materials we use the 1D thermal transport equation :

$$\Phi = \kappa A \frac{dT}{dz} \tag{4.2}$$

Where Φ is the heat flux, κ is the thermal conductivity of the substrate and dT/dz is the temperature gradient in the direction z, normal to the substrate.

Reference	Material System	Thermal Conductivity at 300 K (W·cm-1·K-1)	Frequency (GHz)	Insertion Loss (dB)	Pin for 3dB attenuation in Pout (dBm)	Power Density for ∇T=100°C (dBm/mm^2)
[31]	Silicon	1.5 [36]	3	< 1	~ 20	47
[32]	GaAs	0.46 [35]	10	1.5	~ 20	42
[9]	GaAs	0.46 [35]	10	0.74	~ 18	42
[23]	GaAs	0.46 [35]	9.5	< 1	~ 18	42
[33]	4H-SiC	2.8 [35]	2 – 7	1.1 – 2.6	Not reported	50
This work	Diamond	> 20 [34]	1	0.3	~ 25	58

Table 4.1: Comparison of Diode Limiter Circuits for Different Semiconductor Materials.

The diodes in the first stage of the attenuator experience the largest RF voltage swing, and therefore the highest power dissipation. The power density dissipated in a single diode for a temperature drop of 100^0C across a substrate of thickness 300 μm is estimated using eq. (4.2) with the room temperature thermal conductivities appropriate for silicon, GaAs, SiC and diamond. The values are included in Table II along with other key materials parameters for receiver protectors made from these materials. At elevated temperatures the thermal conductivity of the substrates decreases with increasing temperature [27-30] making it harder to dissipate the heat generated in the diodes. As a result, the power densities in Table II are an over-estimate, and the devices would

experience a temperature increase greater than 100^0C. Nonetheless, the data in Table II confirms that compared to other semiconductor material systems diamond-based P-I-N diodes are ideally suited for high power RF receiver protector applications.

CHAPTER 5. CONCLUSION AND FUTURE WORK

Diamond Schottky P-I-N diodes have been grown by PECVD and integrated as a shunt impedance in co-planar striplines. The DC and AC characteristics of the diodes have been measured and used to extract a lumped element compact SPICE model. The model accurately reproduces the measured insertion and return loss up to 25 GHz. A passive 2- stage diode limiter circuit, simulated at a frequency of 1 GHz, provides receiver input protection up to 50 dBm of input power. At such high input powers significant diode self-heating is expected, increasing the risk of device failure. The high thermal conductivity of the diamond substrates ensures that the self-heating in diamond-based receiver protectors is kept to a minimum compared to other semiconductor device materials such as silicon, GaAs, and SiC.

Some of the milestones that are still under investigation for diamond-based P-I-N diodes and receiver protector application is listed below:

(i) Real time fabrication and characterization of multistage shunt configuration limiters and its performance correlation with the model predictions.

(ii) High Temperature characterization of the diodes and validity of SPICE models to predict the AC and DC behavior under such circumstances.

(iii) The reverse breakdown voltage and additional high temperature leakage currents are the main issues that are currently limiting the performance of the diamond P-I-N diodes. While the diodes show good rectifying behavior up to 600^0C, additional current leakage paths above 300^0C lead to deviations between the simulated and measured data (not mentioned in this thesis).

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