Diamond: An Ultra-Wide Band Gap Semiconductor for High Power Applications

by

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ABSTRACT

Wide Bandgap (WBG) semiconductor materials are shaping day-to-day technology by introducing powerful and more energy responsible devices. These materials have opened the door for building basic semiconductor devices which are superior in terms of handling high voltages, high currents, power, and temperature which is not possible using conventional silicon technology. As the research continues in the field of WBG based devices, there is a potential chance that the power electronics industry can save billions of dollars deploying energy-efficient circuits in high power conversion electronics. Diamond, silicon carbide and gallium nitride are the top three contenders among which diamond can significantly outmatch others in a variety of properties. However, diamond technology is still in its early phase of development and there are challenges involved in many aspects of processing a successful integrated circuit. The work done in this research addresses three major aspects of problems related to diamond technology. In the first part, the applicability of compact modeling and Technology Computer-Aided Design (TCAD) modeling technique for diamond Schottky p-i-n diodes has been demonstrated. The compact model accurately predicts AC, DC and nonlinear behavior of the diode required for fast circuit simulation. Secondly, achieving low resistance ohmic contact onto n-type diamond is one of the major issues that is still an open research problem as it determines the performance of high-power RF circuits and switching losses in power converters circuits. So, another portion of this thesis demonstrates the achievement of very low resistance ohmic contact ($\sim 10^{-4}\ \Omega\cdot cm^2$) onto n-type diamond using nano crystalline carbon interface layer. Using the developed TCAD and compact models for low resistance contacts, circuit level predictions show improvements in RF performance. Lastly, an initial study of breakdown

characteristics of diamond and cubic boron nitride heterostructure is presented. This study serves as a first step for making future transistors using diamond and cubic boron nitride – a very less explored material system in literature yet promising for extreme circuit applications involving high power and temperature.

Dedicated to my parents and teachers

ACKNOWLEDGMENTS

I would like to genuinely express my heartfelt gratitude to my advisor, Professor Trevor Thornton. He has been a constant source of guidance throughout my degree here at Arizona State University. I have been privileged to acquire knowledge, learn from his wealth of experience, and grow under his supervision over the past three years. His everlasting support, invaluable guidance and insightful motivation have been indispensable in helping me achieve my research goals. I would like to thank Professor Robert Nemanich and his team for providing excellent support with the availability of diamond substrates without which the research wouldn't have been possible. My sincere thanks to Professor Stephen Goodnick for guiding me through the TCAD model of diamond devices which turned out to be super helpful in terms of gaining insight into physics of operation of diamond devices. Special thanks to Professor Terry Alford for providing support on material characterizations techniques. Special thanks to the members of diamond team, Evangeline Amonoo, Frank Koeck, Eugene su, Kari Slotten for regular meetings and knowledgeable discussions. I would like to thank PhD student, Harshad Surdi for letting me research on his fabricated device for developing compact models.

The research for achieving low contact resistance on phosphorus doped diamond was done in collaboration with collaborators from Northrop Grumman and Michigan State University. Thanks to staff members from ASU Nanofab for illustrative cleanroom equipment training where all the devices were fabricated. Device characterization was done using equipment from Engineering Research Center 224 lab at ASU.

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CHAPTER 1.

INTRODUCTION

1.1 Wide Band Gap Materials and Diamond

Solid state materials are formed from densely packed atoms, which interact with each other intensely. The result of these interactions determines the mechanical, thermal, electrical, magnetic, and optical properties of solids. Depending on the material involved and the conditions in which it was formed, the atoms may be arranged in a regular, geometric pattern or irregularly which gives rises to various electronic structure within the solid. In solid-state physics, the band gap, also called an energy gap, is an energy range in a solid where no electronic states can exist. The band gap generally refers to the energy difference (in electron volts) between the top of the valence band and the bottom of the conduction band in insulators and semiconductors. It is the energy required to promote a valence electron bound to an atom to become a conduction electron, which is free to move within the crystal lattice and serve as a charge carrier to conduct electric current. Therefore, the band gap is a major factor determining the electrical conductivity of a solid.

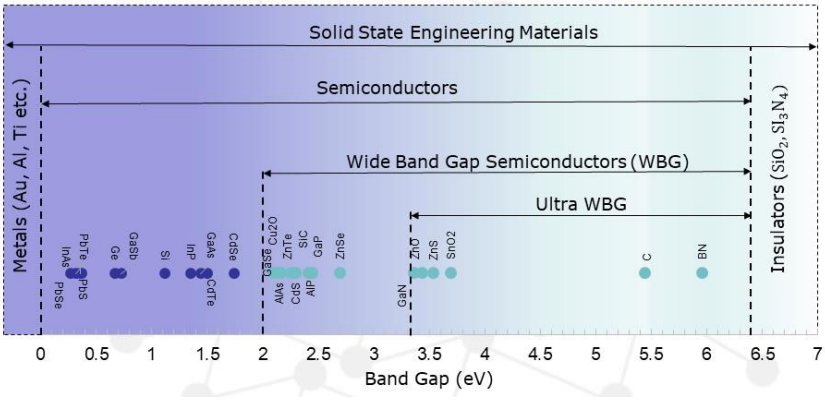

Figure 1.1 Classification of Solid-state Engineering Materials based on Band Gap [1.1]

Fig. 1.1 classifies some of the solid-state engineering materials based on their band gap. The left most extreme are called metals where conduction band and valance band are merged into each other and hence there are plenty of free electrons available for conduction at room temperature. A semiconductor is a material with an intermediate-sized, non-zero band gap that behaves as an insulator at T=0K but allows thermal excitation of electrons into its conduction band at temperatures that are below its melting point. Further in literature, semiconductors are categorized into Wide Band Gap (WBG) semiconductors and Ultra WBG semiconductors (UWBG) which have band gaps greater than 2eV and 3.4eV respectively. In contrast, a material with a large band gap (>6.5eV) is an insulator with negligible charge carriers at room temperature.

WBG semiconductors show superior properties enabling power device functioning at very high operating voltages and extreme temperature environments. The use of new semiconductor material over traditional silicon technology will allow very efficient power conversion and electrical energy transformation [1.2].

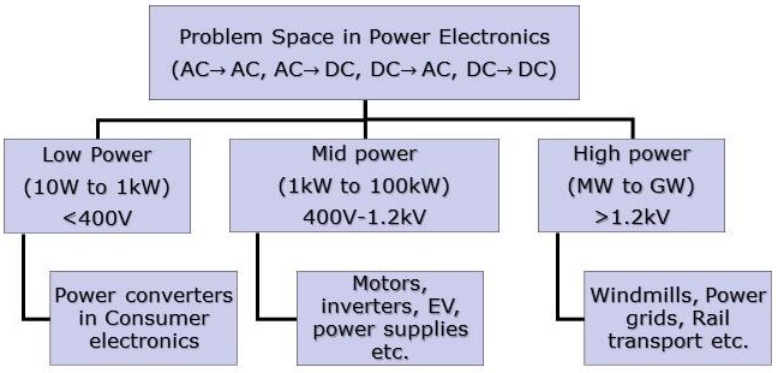

Figure 1.2 Product Space of WBG Materials in Power Electronics Industry.

The end market of WBG materials in power electronics space can be categorized into low, mid, and high-power conversion-based applications as shown in Fig. 1.2. Diverse applications range from industrial functions, such as motor drives and power supplies, to

automotive and transportation systems including hybrid and electric vehicles, aircraft, ships, and traction, to wireless communications, military systems, space programs, and clean energy generation from solar inverters and wind turbines.

Power electronics is a fundamental industry; absolutely everything that uses electricity employs power management devices of some kind. As such, advancements in power devices enable advancements in an unlimited number of applications. Conventional silicon-based power devices have limitations on maximum blocking voltage, operation temperature and switching frequency [1.3]. The reported highest Si IGBT (Insulated-Gate Bipolar Transistor) breakdown voltage capability is 6.5 kV which is further restricted to operate below 200°C for proper functioning. The new generation of WBG power semiconductors will allow increasing the efficiency of electric energy transformation by removing the barriers from silicon technology. The current state of the art wide bandgap materials can be compared with silicon technology for key metrics [1.4] on a spider chart as shown in Fig 1.3. It can be seen from the spider chart that the related high critical field strength of wide bandgap semiconductors leads to the possibility of making thinner devices with low area-specific on-state resistances and low switching capacitances [1.5] which is very much desirable from power electronics point of view. Diamond with very high critical electric field strength and excellent thermal conductivity is the best WBG material available. In the spider chart, all of the WBG material properties translate ultimately to benefits through improved efficiencies, decreased power losses through heat and reduced cost [1.6]. These promising properties are the motivation for ongoing research on diamond-based power devices.

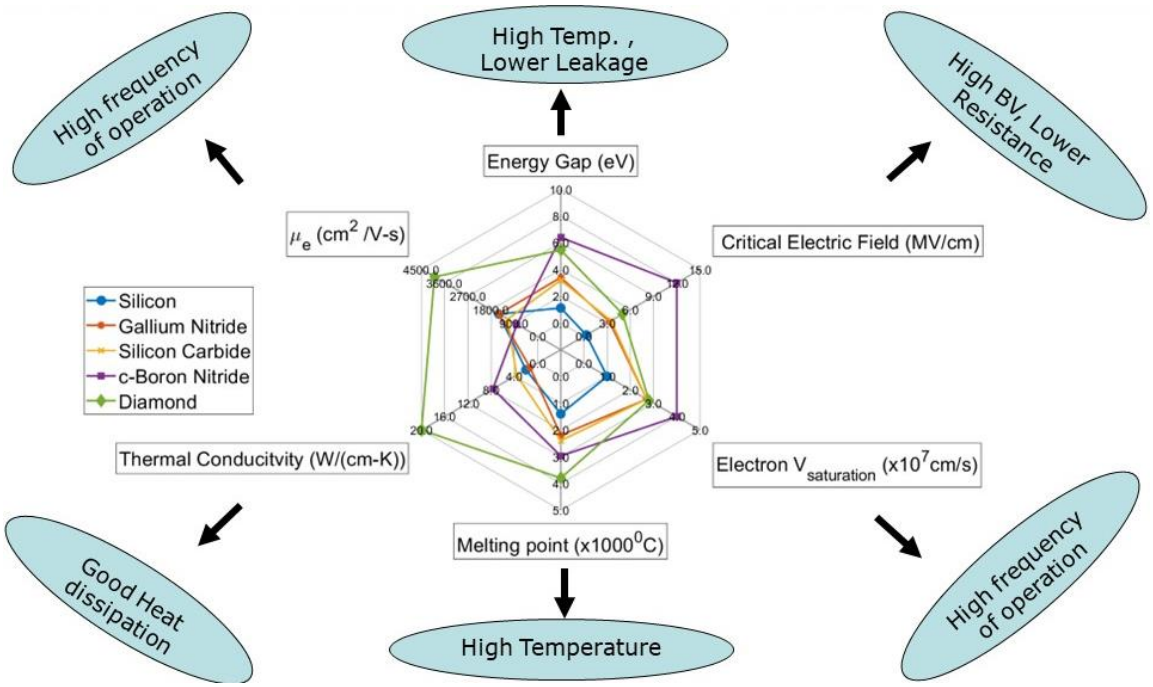

Figure 1.3 Spider Chart Comparing Interesting Properties of WBG Materials with Silicon.

Diamond based Schottky and P-I-N diodes are already achieving remarkable performance during static and dynamic measurement setup shown in several publications [1.7]. There has been a substantial increase in diamond power device research with various successes such as diamond Schottky barrier diodes with a breakdown voltage of 12.4 kV [1.8] has been reported. Fig. 1.4 shows some of the best reported maximum current density and breakdown voltage of Schottky barrier diodes fabricated on diamond in the last two decades. High current carrying capacity inherently requires understanding of the heat generation and dissipation in the power device, thanks to the very high thermal conductivity of diamond that allows it to operate at very high-power levels while dissipating the heat effectively.

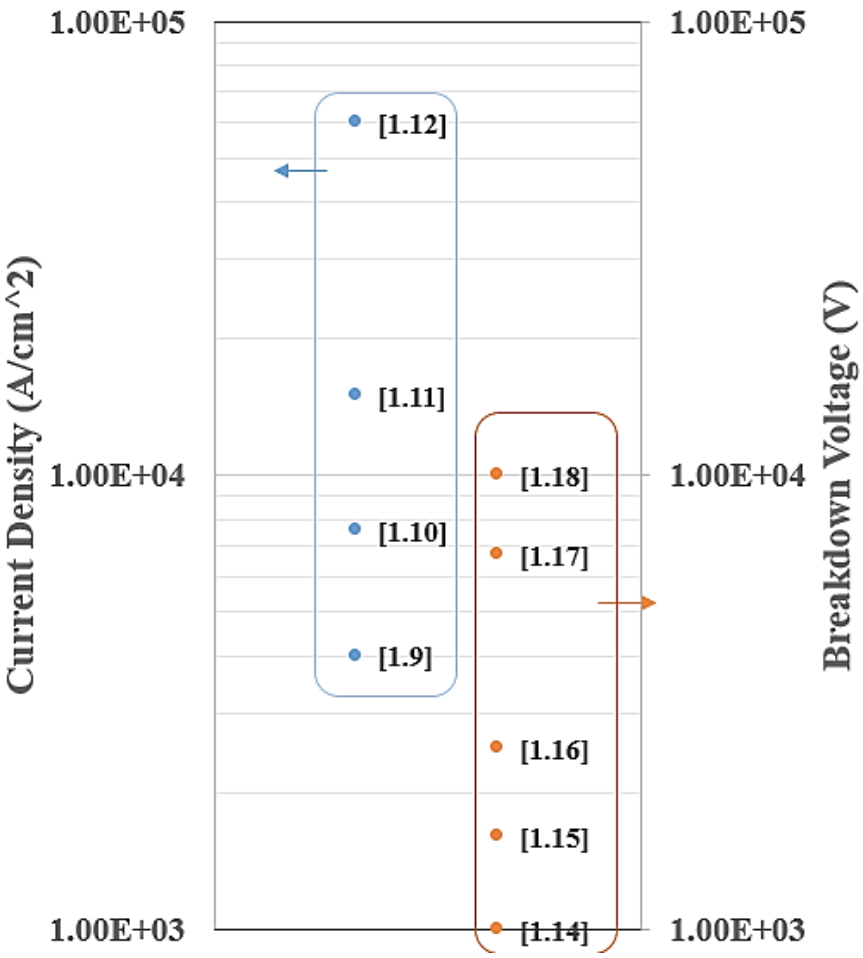

Figure 1.4 Progress Made in Diamond Diodes. Reported Values of Maximum Current Density and Breakdown Voltage.

Alongside the progress being made towards diamond electronics for DC power management, diamond devices are also being developed for high power RF applications. The two-dimensional hole gas (2DHG) formed at the surface of hydrogen-terminated diamond has been used for p-channel FETs with a cutoff frequency, f_T, and maximum oscillation frequency, f_{max}, of 41 GHz and 44 GHz respectively [1.19]. The 2DHG p-FETs are also capable of high current drive with drain current over 1A/mm [1.20]. Diamond MOSFET RF amplifiers with 3.8 W/mm of output power at 1 GHz have been demonstrated [1.21]. These results bode well for RF power amplifiers operating in high-temperature

environments, or for high-performance applications that would benefit from the efficient heatsinking enabled by the high thermal conductivity of the diamond substrate.

1.2 Research Possibilities and This Work

Diamond is a wide-bandgap semiconductor with tremendous potential as an electronic device material in both active devices, such as high-frequency field-effect transistors (FETs) and high-power switches, and passive devices, such as Schottky diodes. Its properties potentially enable devices that are beyond the scope of current systems in terms of operating frequency, power handling capacity, operating voltage, and operating environment. Fig. 1.4 shows key steps in building an integrated circuit on semiconductors. While diamond has significant potential, it possesses a number of features that present challenges in each of the steps during device processing.

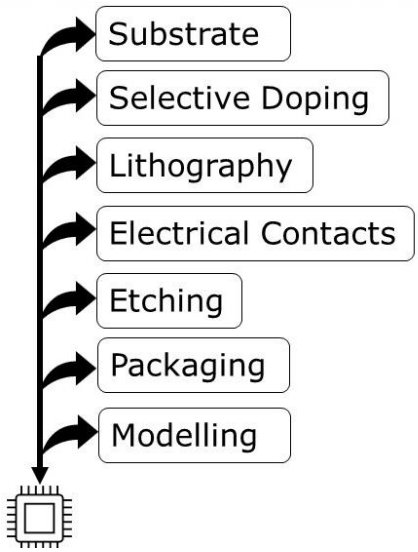

Figure 1.5 Key steps in Building Integrated Circuits on Semiconductors.

Starting from substrate availability, selectively doping the diamond, making good electrical contacts onto diamond surface, modeling the electrical characteristics of devices etc. are some of the fundamental unit processes that are currently very immature for

diamond technology [1.22] and hence in terms of research opportunities there are lots of open problems that need to be solved with innovative ideas.

Natural diamond is too variable in its properties to be considered as a viable electronic material for commercial applications [1.23]. Alternatively, a lot of growth techniques have been explored in the research community to artificially synthesize diamond in the lab. Currently a major issue for the use of diamond is the lack of inch-sized wafers compared with the availability of such wafers for other materials, including Si, SiC, GaN, and Ga_2O_3. The lab grown diamonds are typically classified into high-temperature high-pressure (HPHT) synthetic substrates or CVD grown diamonds. Larger substrates with the HPHT method may be difficult owing to the size restrictions of high-pressure fabrication methods. The bottleneck with HPHT process is increasing cost and defect density for large substrates [1.24]. Conversely, chemical vapor deposition (CVD) methods have fewer restrictions on apparatus size than those for the HPHT method, and research into the synthesis of single crystal diamond is progressing. Currently the largest size crystals of 2in. size has been reported using this method [1.25].

Diodes in power electronics are one of the two major components allowing industry to develop switching converters. They are often working with a transistor, and they are required to pass ever higher currents in the forward direction and to sustain ever higher voltages in the reverse direction. Such diodes will be used, for example, in high power switching DC/DC converters. An ideal device would offer very low on-resistance and very high blocking voltage. Theoretically, diamond offers large advantages in both the regimes owing to its very high thermal conductivity ($\kappa = 22 - 24$ W/cm. K) that can handle large amounts of current with minimal or no heatsinks and high breakdown field (10 − 20

MV/cm). Chapter 2 of this research work demonstrates the SPICE and TCAD modeling strategy of diamond Schottky p-i-n diodes fabricated at the ASU Nanofab. SPICE is used to model the terminal characteristics of the devices to check the integrity of circuit designs and to predict complex circuit behavior in a short amount of simulation time where TCAD offers more insight into physics of operation of the individual device but usually takes significant amount of time which might not be practical for complex circuit simulation.

In order to make efficient devices on p or n type semiconductors, electrical contact property is one of the key factors determining the device performance. Ideally one would want to have a zero voltage drop across the contact, i.e., perfectly ohmic contact. But in practice there exists a barrier between contact material and the semiconductor surface that inhibits the ideal current flow. As shown in Fig. 1.6, for boron doped p-type diamond a low-resistivity contact has been almost achieved by titanium (Ti)/ platinum (Pt)/ gold (Au) contact, approaching specific contact resistance (ρ_c) to order of 10^{-6} $\Omega \cdot cm^2$ [8].

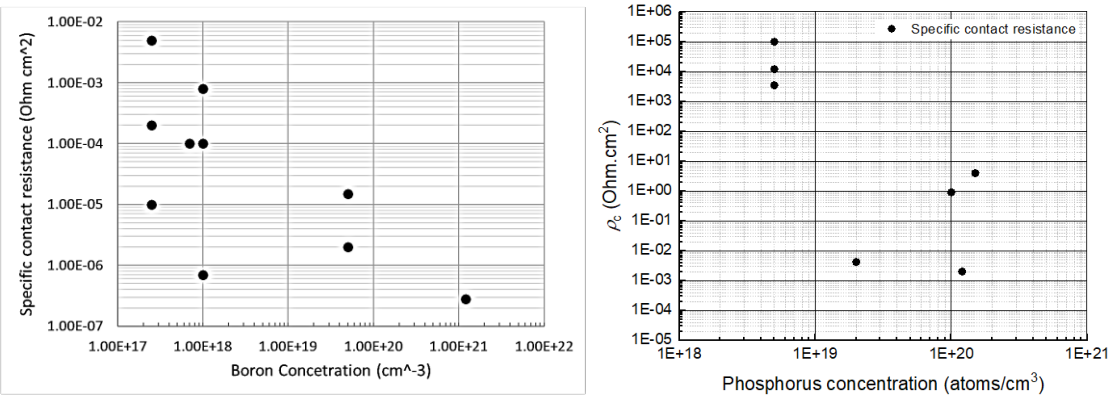

Figure 1.6 Specific Contact Resistance Plotted Against Doping Concentration from Literature. Left: Boron Doped Diamond, Right: Phosphorus Doped Diamond. (See Chapter 3 for Data References.)

On the other hand, for phosphorus-doped n-type diamond, a reliable contact with low resistance has not been achieved yet. Fig. 1.6 shows the specific contact resistance of (111)- Phosphorus doped diamond/metal interfaces from several references. The specific contact resistance is strongly dependent on the P concentration, which means that heavy P doping is effective for decreasing the value of ρ_c. In chapter 3 it has been demonstrated that, with selecting proper annealing temperature and conditions, Ti/Pt/Au metallization scheme onto heavily doped oxygen terminated n-type diamond can achieve low contact resistance to the order of 10^{-3} $\Omega \cdot cm^2$. We further succeed to reduce the contact resistance down to the order of 10^{-4} $\Omega \cdot cm^2$ (the lowest reported value till now) using an ultra-nanocrystalline diamond (UNCD) interface layer grown between the Ti/Pt/Au and the n-type diamond. Finally, the sheet resistance behavior at different temperatures is discussed.

As pointed out earlier, diodes and transistors are the key components in power conversion and power control circuits. Given a well calibrated TCAD/SPICE model is available, simulators can precisely predict the AC, DC, transients, and nonlinear behavior of complex circuits using available device models. In chapter 4 of this thesis, two important applications of diodes, receiver protector circuit and RF mixer, have been simulated using the device models developed in chapter 2. For high power RF applications and power conversion operations, the on-resistance plays a crucial role in determining the overall figure of merit of the device. Further, the strategy used in chapter 3 to reduce the contact resistance is used in the TCAD models to predict the performance improvements of receiver protection circuits.

Cubic boron nitride (c-BN) possesses a number of extreme properties rivaling or surpassing those of diamond. The large bandgap and high thermal conductivity of c-BN

make it an attractive candidate for applications with power electronic devices. Cubic boron nitride is similar to diamond, with sp3 hybridized bonds. However, realization of c-BN-based functional devices is still a challenging task due largely to the subtlety in the preparation of high-quality c-BN films with uniform thickness and controllable properties. In chapter 5, an initial study for the breakdown charateritics of c-BN film onto diamond has been done with help of MOSCAP structures. The results provide an important insight into dielectric breakdown and the current leakage mechanisms which will serve as a first step towards making transistors using diamond and c-BN heterostructure.

Lastly, conclusions and future direction of research are presented in chapter 6.

CHAPTER 2.

DIAMOND P-I-N DIODES: MODEL PARAMETER EXTRACTION

2.1 Introduction

A semiconductor diode, the most commonly used type today, is a crystalline piece of semiconductor material with a P-N junction connected to two electrical terminals. This P-N junction is fundamental to the performance of electrical functions such as rectification and switching in electronic circuits. A P-I-N diode is very similar to a P-N diode, except an extra intrinsic layer (or I -layer) is introduced between the P and N layer as shown in Fig. 2.1. Generally, P and N layers are heavily doped (degenerate) and hence they are of very low resistance whereas the I-layer has very low doping levels creating a highly resistive region sandwiched between P and N layers.

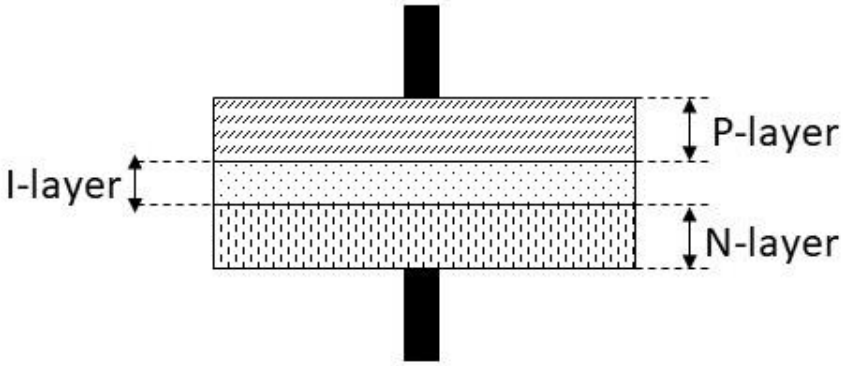

Figure 2.1: Structure of a P-I-N Diode.

This tweak in the design of P-I-N diodes allows it to operate as a variable resistor at microwave frequencies [2.1]. In the conducting state, holes and electrons are injected into the I-region. These charges do not immediately recombine; instead, they can exist for an average time called the carrier lifetime, τ. This results in an average stored charge, Q, which

lowers the effective resistance of the I-region to a value R_s (series resistance). The P-I-N diode is often described as an "Current Controlled Linear Resistor". These diodes are optimized to achieve a wide and linear resistance range. Their ability to control high power RF signals makes them suitable for attenuation, modulation, and many other applications with much lower levels of DC excitations [2.2].

A compact model is a virtual analog of a real device. The compact model includes a set of parameters used to simulate the device in different modes of operation: static (DC), dynamic (for transient analysis, TR) and frequency-response (in small signal mode, AC). In most SPICE-like programs for circuit simulation, the compact Schottky diode model is a variation of the conventional diode model of the p-n junction. The unified compact modeling strategy of a P-I-N diode consists of multiple diodes [2.11] as shown in Fig. 2.2, where different diodes in the model turn on in different regimes of operation.

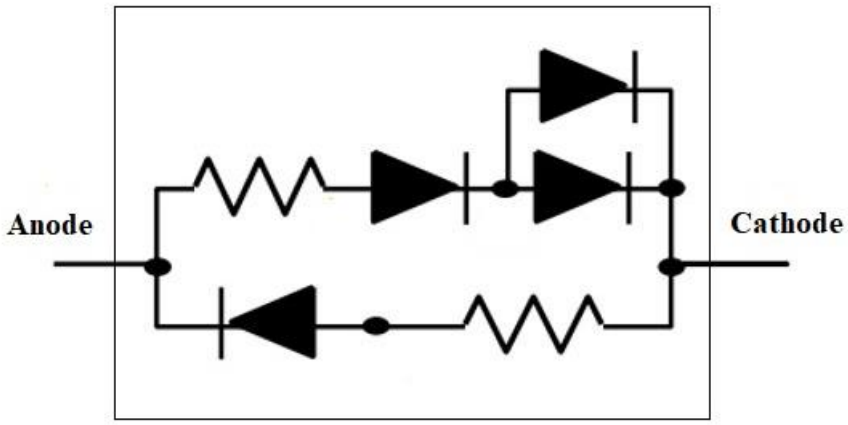

Figure 2.2 Unified Compact Modeling Strategy of P-I-N Diode. Multiple P-N Junction Diode and Its Parameters Are Tuned to Model the Overall Diode Behavior.

2.2 Theoretical Device Operation

Figure 2.3 represents the electrical symbol of a P-I-N diode. The P-layer (connected to the anode) and N-layer (connected to the cathode) are heavily doped with acceptor and

donor impurities respectively while the I-layer is almost intrinsic in nature. Under equilibrium conditions there exists no external potential difference between anode and cathode. During forward bias, the anode is tied to a higher potential than the cathode while during reverse bias the n-layer is at higher potential than p-layer.

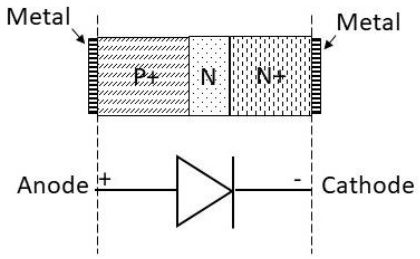

Figure 2.3: Schematic of a P-I-N Diode.

The operation of P-I-N diodes can be understood as follows: Based on the ionized impurity concentration in different regions, a different concentration profile of carriers (holes or electrons) results within the device. Under zero external bias condition, if we assume that the device is under thermal equilibrium, then at the interface (P-I and I-N), charge carriers will diffuse from higher concertation (P or N layer) to lower concentration region (I layer) leaving behind impurities which are depleted. This will setup an electric field in the opposite direction and cause drift current which will exactly balance the diffusion current (because of the concentration gradient) component under thermal equilibrium. It is to be noted that under thermal equilibrium, the potential on the electrode surface on both sides of the device is equal. The potential difference created by the difference in concentration of impurities in the semiconductor does not appear outside (to the contact) and is often referred to as the built-in potential as shown in Fig. 2.4.

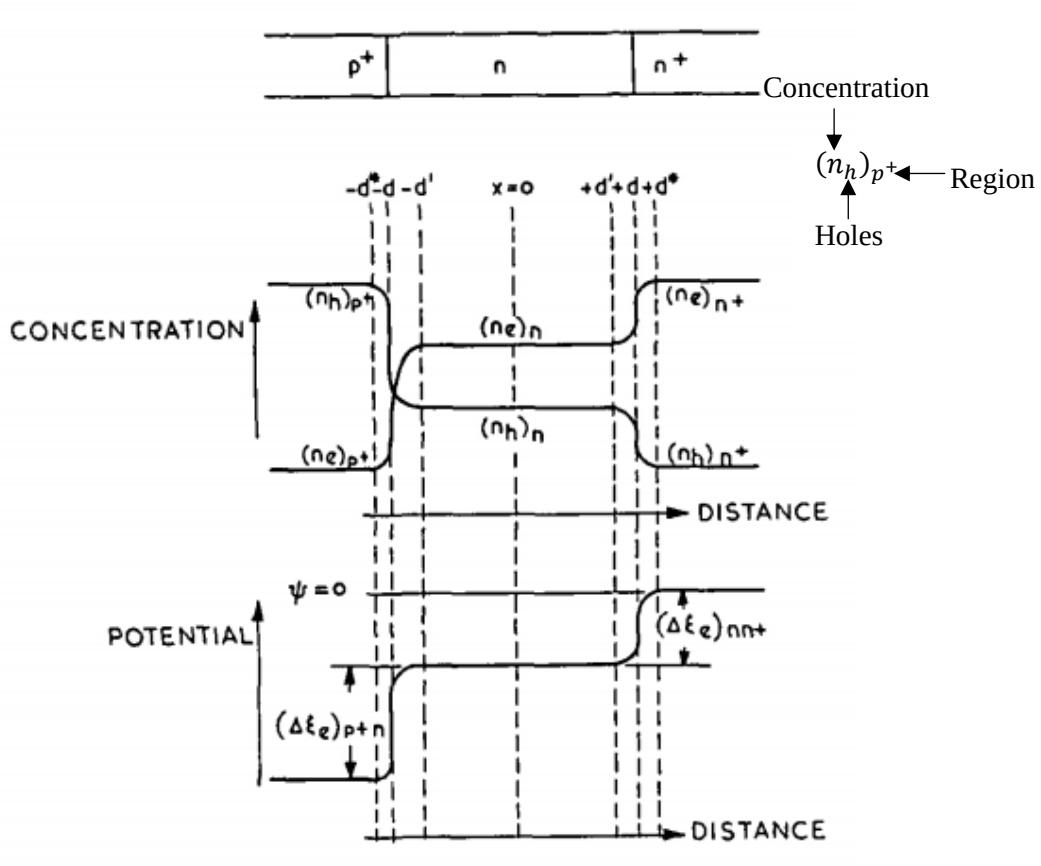

Figure 2.4: Potential Distribution and Carrier Concentration in P-I-N Diode under Thermal Equilibrium [2.3].

Under *forward bias,* the static characteristic of the diode is determined by the concentration of minority carriers present in any region of the semiconductor. When external bias is applied, the concentration of minority carriers in the all the regions (P-I-N) are affected because of injection which in turn affects the rate of generation and recombination of the carriers. In order to find the current voltage characteristics of the diode, one must consider three separate cases based on level of injection (or bias) as:

a) Low-level injection: When the concentration of injected carriers is less than the thermal-equilibrium value for majority carriers in any region, we have the conditions of low-level injection. Under such a scenario the applied bias falls completely across the p+n layer

thereby reducing the overall potential barrier for charge carriers. Potential and carrier distribution of low-level injection case is shown in Fig. 2.5.

b) High level injection: When the concentration of injected carriers becomes comparable to that of the concentration of majority carrier in n-type region, we have the condition of high-level injection. Potential and carrier distribution of high-level injection case is shown in Fig. 2.6.

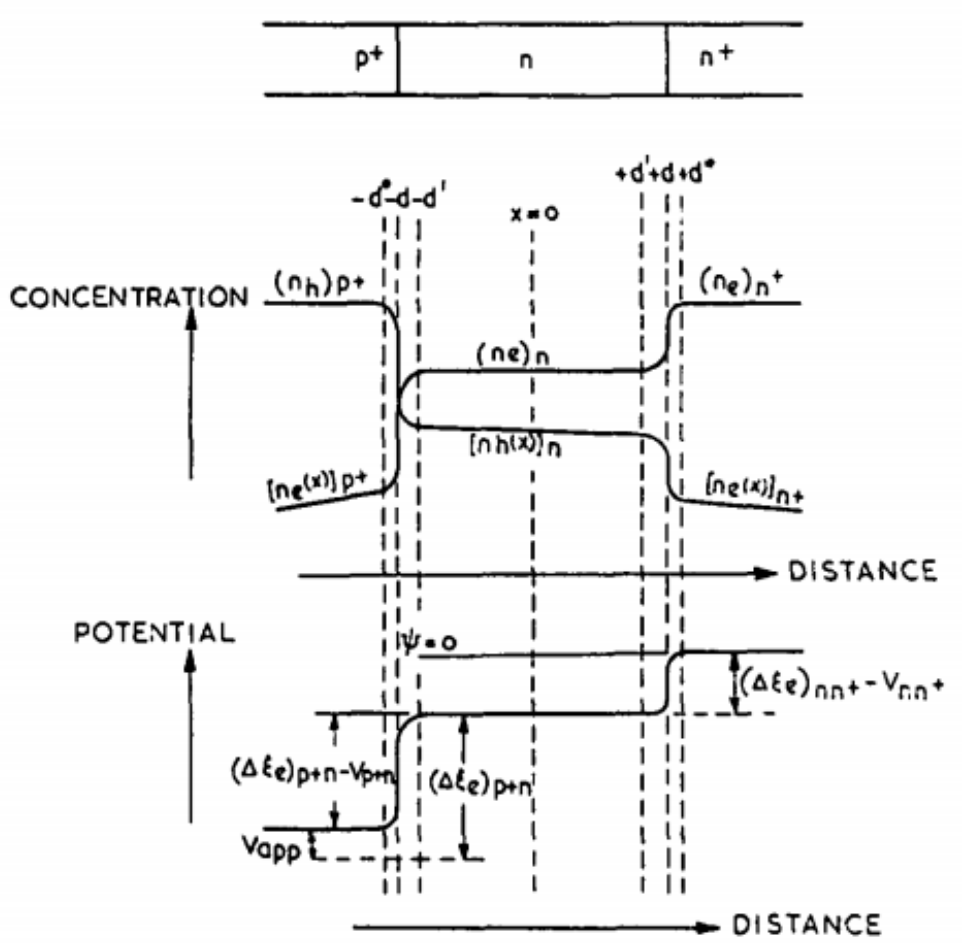

Figure 2.5 Low Level Injection [2.3].

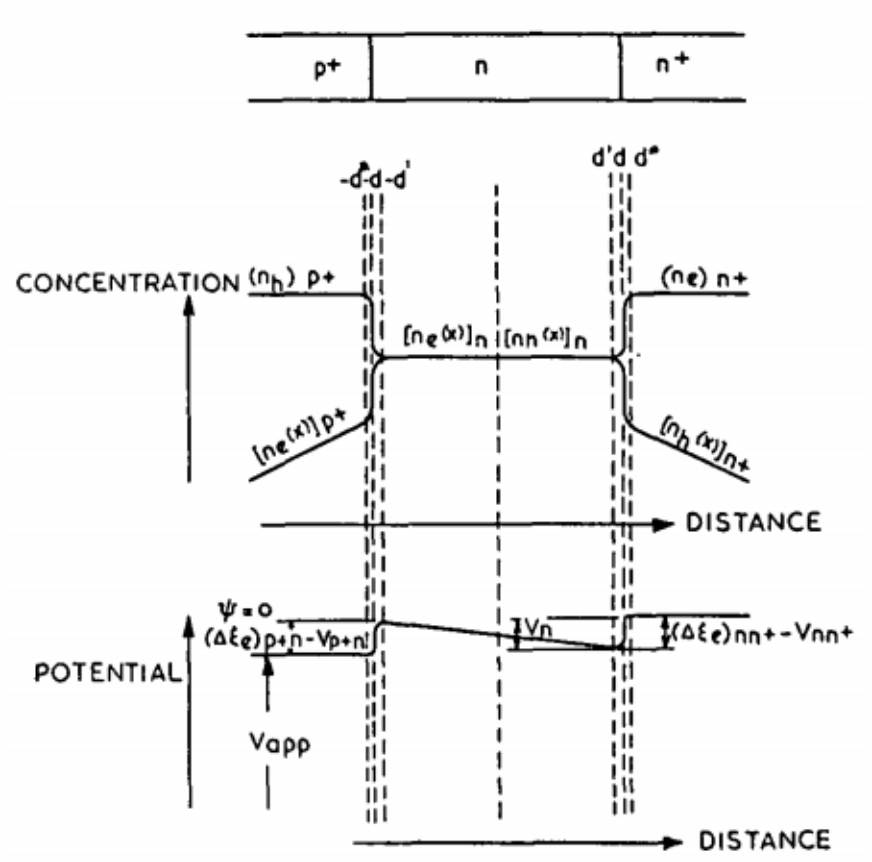

Figure 2.6 High level Injection [2.3]

c) Very high-level injection: As shown in Fig. 2.7, when the injected carrier density becomes greater than the majority carrier concentrations in the n+ and p+ regions, we have conditions of very-high-level injection.

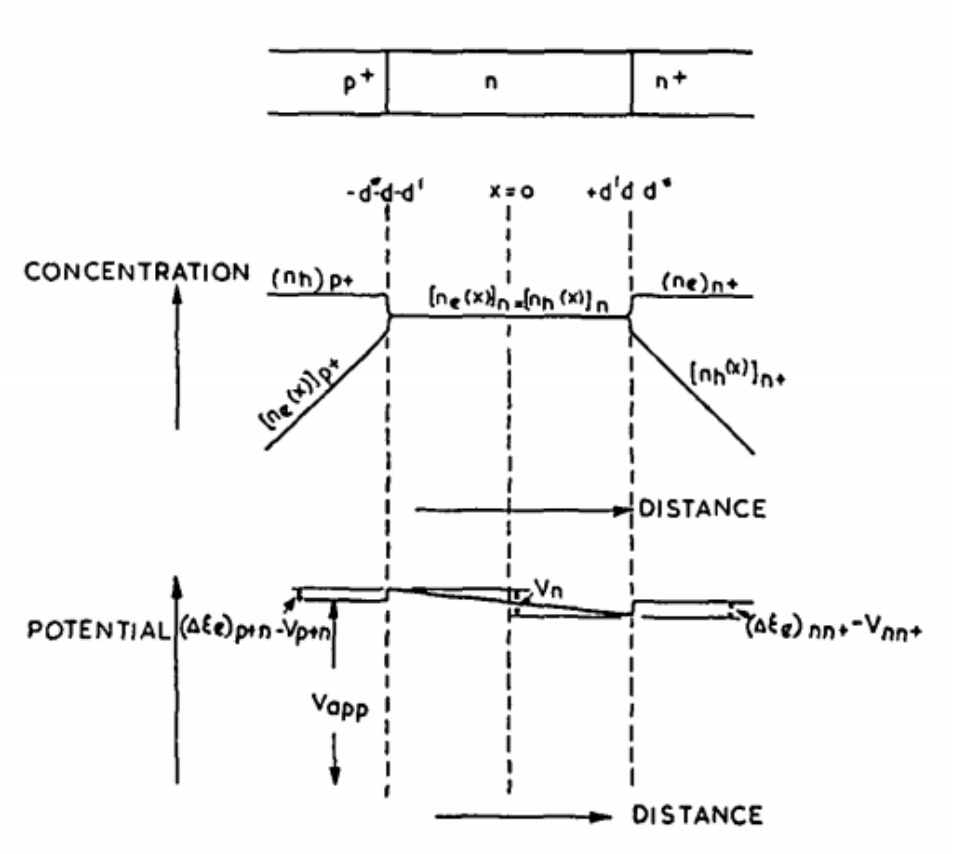

Figure 2.7: Very High-level Injection [2.3].

Given the potential distribution profile within the diode, one can derive the concentration profile using "*law of junctions"* in terms of the applied bias and equilibrium concentration. The excess carriers getting injected into the device under non equilibrium conditions recombine and give rise to the electric current. So, we can write the total current in the device :

$$\Gamma = \int (\text{Net generation} - \text{ Net recombination}) \times \text{dv} \qquad (2.1)$$

There are several approximation functions available to describe the integrand of equation 2.1. One such expression is for the process when the electrons and holes recombine through a single recombination level then,

$$(\text{Net generation} - \text{ Net recombination}) = \frac{n_e n_h - n_i^2}{\frac{1}{\alpha_e n_T}(n_h + n_{h1}) + \frac{1}{\alpha_h n_T}(n_e + n_{e1})} \qquad (2.2)$$

Where,

n_e: Concentration of electrons, n_h: Concentration of holes

n_i: Intrinsic carrier concentration

n_{e_1}| n_{h1}: constant of mass of mass action law for e and h.

α_e: recombination constant for free electrons

α_h: recombination constant for free holes

n_T: concetration of recombination centers

Thus, a knowledge of carrier concentration profile under non-equilibrium conditions will enable us to write the expression 2.2 which in turn can be integrated to find the total current density as a function of applied bias. Fig. 2.8 shows a generic IV characteristic of a P-I-N diode derived in [2.3] based on different levels of minority carrier injection calculated using equations 2.1 and 2.2.

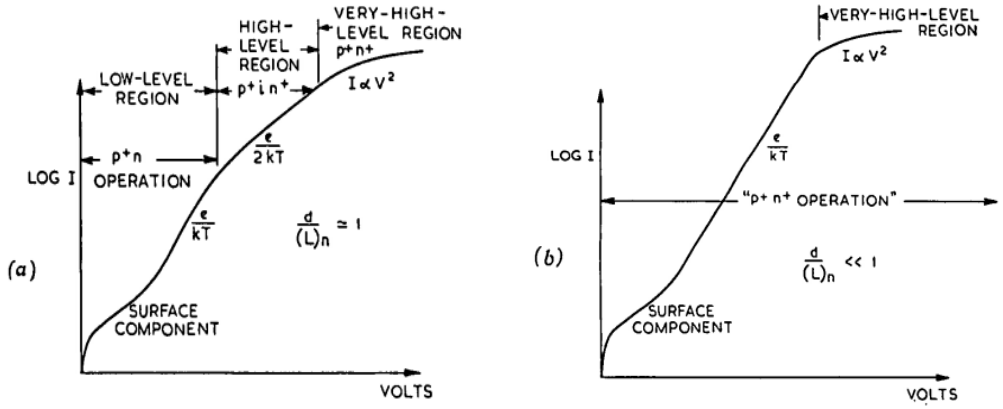

Figure 2.8: Theoretically Approximated IV Characteristics of P-I-N Diode [2.3]. (a) Device with Comparable Diffusion Length , (b) Thinner I Region and Higher Diffusion Length.

When a *reverse bias* is applied, a majority of the holes and electrons stored in the intrinsic region during forward bias return to the P and N layers. Almost no charge is stored in the depleted I region. Ideally this should result in infinite resistivity, however in reality the resistivity is finite which results in lossy I-region capacitance. At high frequency, the device acts like a parallel plate capacitor whose value is almost independent of the applied reverse bias. The value of this capacitance is approximately given by:

$$C_{rev} = \frac{\epsilon \times \text{Area of cross section}}{\text{Width of Intrinsic region}} \tag{2.3}$$

2.3 Device Fabrication

The starting material for fabrication of diamond P-I-N diodes are the commercially available high-pressure, high-temperature (HPHT) diamond substrates. Some of the physical properties of HPHT diamond material are shown in Table 2.1:

Orientation	<111>
Background doping type	P-type
Substrate dimension	3mm x 3mm
Thickness	300µm
Dopant	Boron
Peak Impurity concentration	$2 \times 10^{20} cm^{-3}$

Table 2.1: Process Parameters of HPHT Diamond

High-pressure, high-temperature (HPHT) <111> p-type doped diamond substrates with dimensions of 3mm x 3mm and a boron concentration of ~$2x10^{20}cm^{-3}$ were commercially

obtained from the Technological Institute for Superhard and New Carbon Materials [2.4]. The HPHT wafers have a thickness of ~ 300 μm.

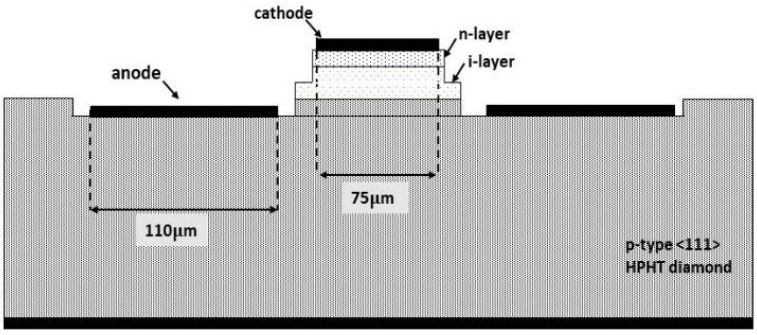

Figure 2.9: Cross Section of the Fabricated Diamond Schottky P-I-N Diode.

At first, the epitaxial layers of boron doped (~ 10^{20}cm^{-3}) diamond of thickness ~5μm were grown by plasma enhanced chemical vapor deposition (PECVD) technique on the substrate material by Dr. Franz Koeck from the Physics Department at ASU [2.5]. The intrinsic layer and finally the n+ layer was then grown on the boron doped (p+) layer to obtain a vertical structure of P-I-N diode as shown in Figure 2.9. The n-type layer has a nominal background doping of > 10^{18}cm^{-3}and is thin enough to be completely depleted by the Schottky barrier height of the metal cathode. As a result, the diodes behave as a n-type Schottky junction with a lower turn-on voltage compared to P-I-N diodes with a thick n-type region that is only partially depleted at zero bias. These fabrication steps were performed by PhD student Harshad Surdi at ASU Nanofab.

A secondary ion mass spectroscopy (SIMS) analysis was performed on the completed wafer and the concentration of boron and phosphorus as a function of depth into the wafer is shown in Fig. 2.10. The SIMS data confirms the high boron doping in the substrate, falling to ~10^{16}cm^{-3} during the growth of the nominally undoped intrinsic i-layer. The

phosphorus concentration in the n-layer steadily increases from a background below 10^{-15} cm^{-3} to a peak of 8×10^{18} cm^{-3} at the surface. The depth at which the phosphorus concentration equals the boron background concentration gives an n-layer junction depth of 0.28μm, leaving an intrinsic region of approximately 0.22 μm. A peak in the boron concentration within the top 50 nm of the diamond surface suggests that the n-layer is partially compensated, perhaps due to boron dopants from the substrate floating on the growth front during the PECVD deposition.

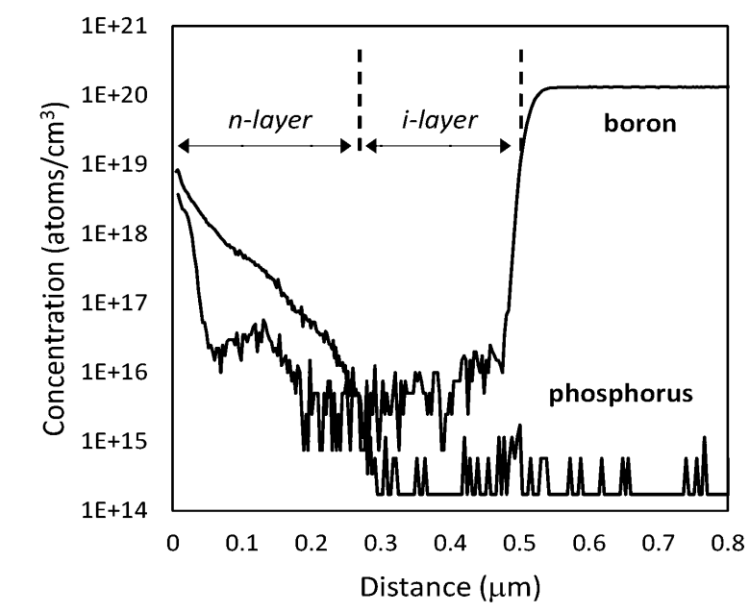

Figure 2.10: SIMS Profile of the Fabricated P-I-N Diode.

Electrical contacts suitable for on-wafer DC and RF probing of the diodes were fabricated as follows. The devices were electrically isolated from one another by a partial mesa etch through the n-type diamond and into the I-layer using O_2/SF_6 reactive ion-etching that defines the diode area. To allow contact to the p-type region from the top surface a second RIE step was used to etch through the I-layer and into the HPHT substrate. Metal layers of Ti/Ni/Au (50nm/50nm/300nm) were deposited by electron beam

evaporation to form the cathode and anode contacts to the n- and p-layer diamond respectively. The metal layer to the anode forms an Ohmic contact due to the high doping concentration in the p-type diamond substrate. In contrast, a Schottky contact is formed on the n-type cathode, which is depleted at zero bias forming a so-called Schottky P-I-N diode. The electrical contacts were patterned with a ground-signal-ground (GSG) configuration as shown in Fig. 2.15. The active diode area of $100\mu m \times 75\mu m$ forms the central ground connection, and the center-center pitch between the ground-signal pads is $100\mu m$.

2.4 DC Characteristics and Measurement

The characteristics of P-I-N diode under several bias conditions can be derived with proper set of approximations (under different injection levels) and has been discussed in section 2.2. However, it has been shown that the IV characteristics of a P-I-N diode [2.6] with relatively narrow I-region can be approximately written in the form:

$$I_d = I_0\left(e^{\frac{q(V-I_d r_s)}{nkT}} - 1\right) \tag{2.4}$$

Where,

n is ideality parameter that changes based on injection level or applied bias,

r_s is the series resistance of the diode,

I_0 is the saturation current,

q is the electronic charge,

k being the Boltzmann constants and

T is the operating temperature.

The electrical characteristics of the diodes were measured by on-wafer probing system shown in Fig. 2.11. Fig.2.12 shows the measured IV data of the diode. For reverse bias and

forward bias up to 6V, the current was measured using an Agilent 4156 precision semiconductor parameter analyzer with a maximum current of 100 mA and a noise floor of ~ 0.1 pA. For higher currents the forward IV characteristics were recorded using a Keithley 2400 with a current limit of 1A. The current limit was reached at a forward bias of 9.2 V and corresponds to a current density of 12.1 kA/cm^2.

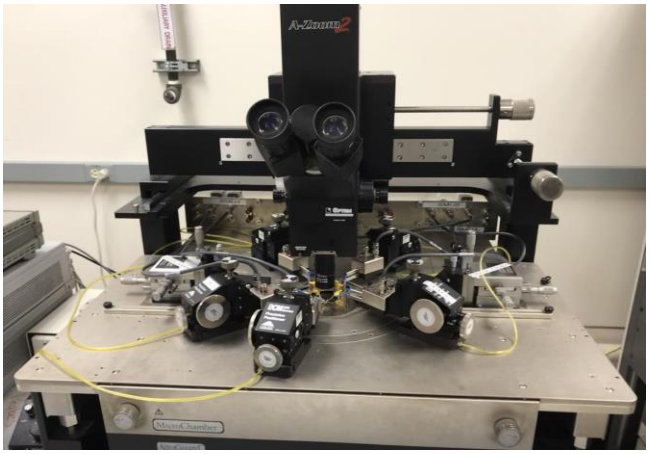

Figure 2.11: DC Probe Station Connected to Agilent 4156 Precision Semiconductor Parameter Analyzer.

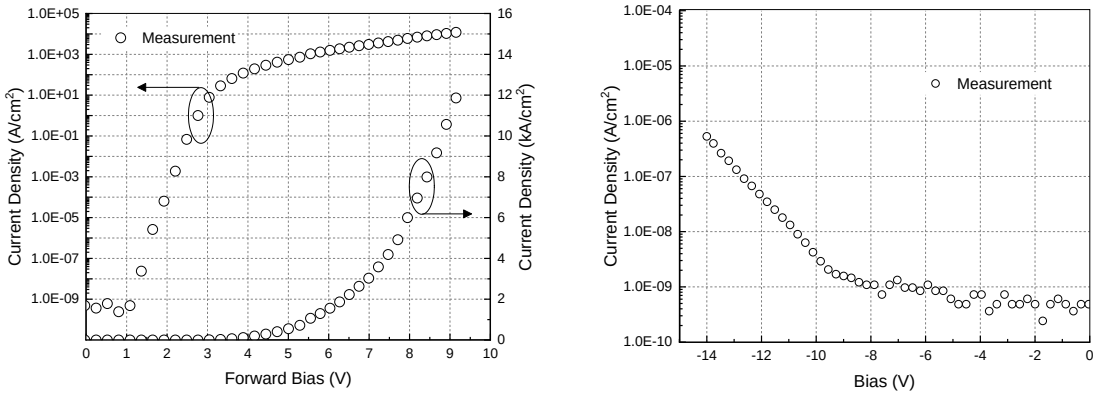

Figure 2.12: Measured DC IV Characteristic of the P-I-N diode. Left: Forward Bias, Right: Reverse Bias

It is also important to derive the first order characteristics of the diode called as conductance, G_d. Diode conductance (dynamic) is obtained by differentiating the IV characteristics in eq. 2.4 and is defined as :

$$G_d = \frac{dI_d}{dV} \approx \frac{I_d}{nV_t} = \frac{1}{R_j} \tag{2.5}$$

Where R_j is the junction equivalent resistance. The measured conductance of the diode is shown in Fig. 2.13.

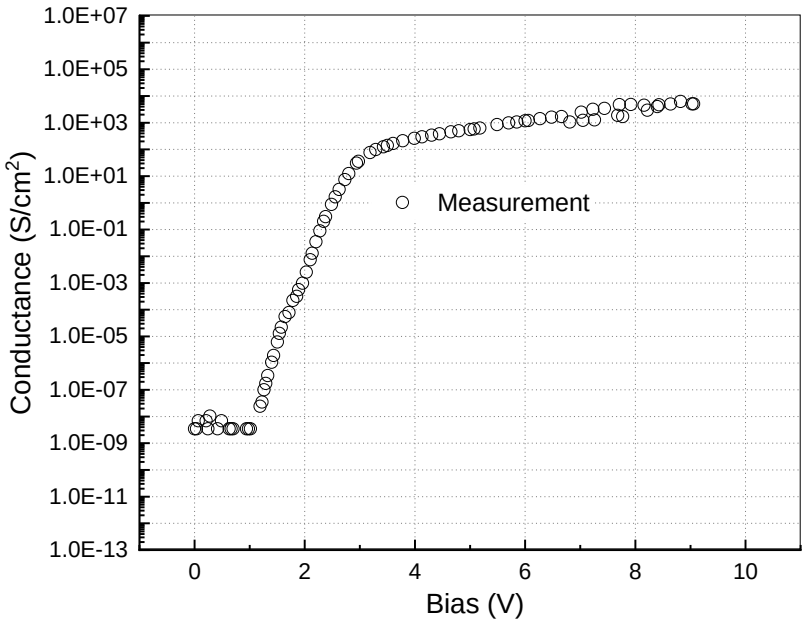

Figure 2.13: P-I-N Diode Conductance Obtained from Measured DC IV Characteristics.

2.5 AC Characteristics and Measurement

From a small-signal RF point of view, a P-I-N diode basically acts as a variable resistor. The total resistance of the diode is the sum of resistances from P, I and N region respectively. Since P and N region are heavily doped, they contribute a very small portion

to total resistance. However, the resistivity of the I region and thus the total diode resistance is determined by the total number of free carriers in the I region:

$$\rho_I = \frac{1}{q(u_N N + \mu_P P)} \tag{2.6}$$

Where q is the electronic charge and μ_N and μ_P are electron and holes mobility.

The amount of charge stored in the I-layer during forward bias depends on the diode current and the average carrier lifetime,τ. The following equation relates these parameters under steady state conditions:

$$I_d = \frac{Q_d}{\tau} \tag{2.7}$$

The average time it takes for the stored charge to decay by ~63% of its initial value is equal to carrier lifetime (recombination time). For a high frequency signal, the number of free charge carriers stored in the intrinsic region does not change appreciably and remains almost the same as what is set by the DC bias current. If we assume that the width of the intrinsic region to be *W*, carrier mobility and lifetime be μ and τ respectively, then the value of resistance seen by AC signal can be approximately written as [2.1] :

$$R_j = \frac{W^2}{2\mu\tau I_d} \tag{2.8}$$

Or this can be written in the form:

$$\log R_j = -\log I_d + C \tag{2.9}$$

Finite element-based differential with very small voltage step would give a reasonable approximation of R_j. Hence the value of R_j is determined from Fig. 2.12 which has a monotonic behavior over the measurement window. The measured data shows an almost

linear relationship (as in eq. 2.9) on a log-log scale between R_j and the diode current obtained from the DC measurements shown in Fig. 2.14 i.e., modulation of resistance with bias current.

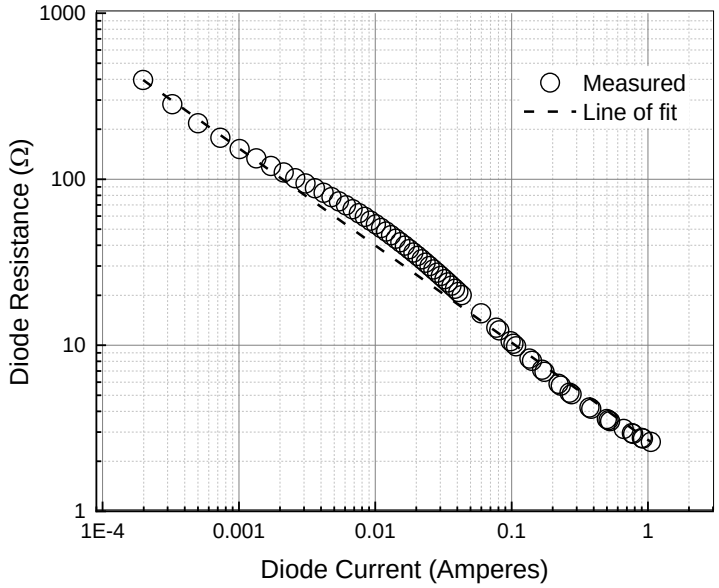

Figure 2.14: Plot of Dynamic Resistance vs Diode Current.

After calibration of the ground-signal-ground (GSG) probes (Fig. 2.15) using an impedance standard substrate, the S-parameters of the diode were measured from 1GHz to 25 GHz for a range of DC forward biases as shown in the Smith chart representation of Fig. 2.16.

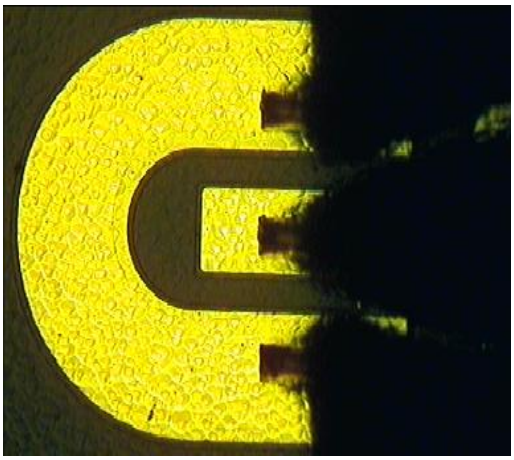

Figure 2.15 GSG Probe Touching the P-I-N Diode for S-parameter Measurement.

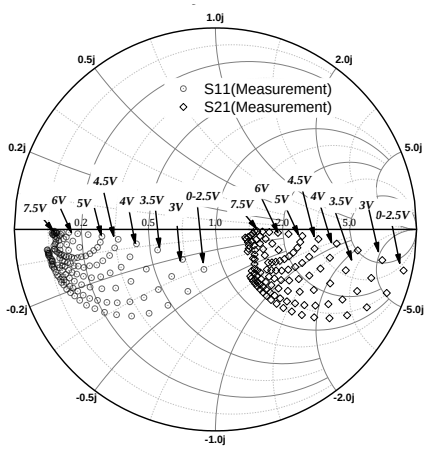

Figure 2.16 Measured S11 and S21 of the Device.

From the S-parameter data, the corresponding Z-parameters were extracted (not shown) using standard formulas [2.7]. The impedance data was then used to fit the simple lumped-element RC circuit in the inset to Fig. 2.17, using the Keysight parameter extraction software, IC-CAP [2.8]. In this way the total diode impedance, C_D, can be determined as a function of bias. The resulting CV curves are shown in Fig. 2.17 and are later used to extract the SPICE model capacitance parameters. At zero bias the capacitance of the diode is 16.8 nF/cm^2, and for a relative permittivity of 5.7 would correspond to an I-layer of thickness 300nm, in excellent agreement with the target growth thickness.

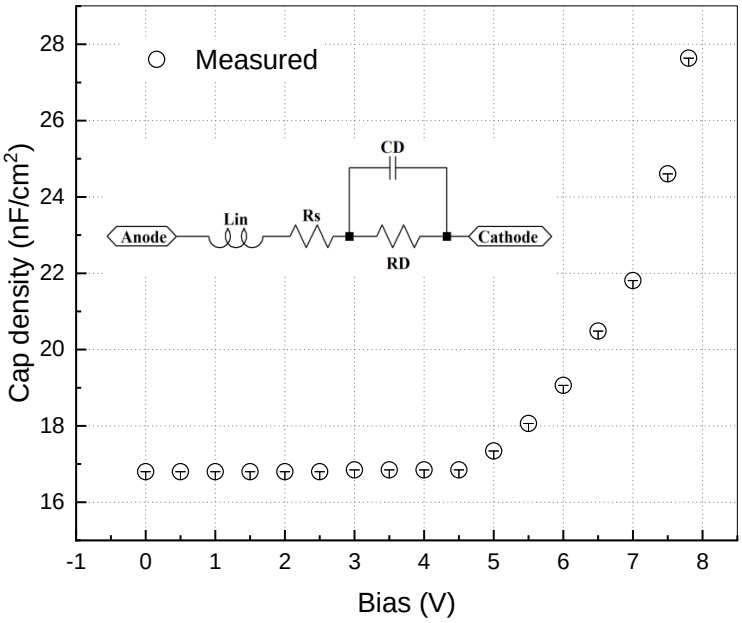

Figure 2.17: Extracted Diode Capacitance as a Function of Applied Bias.

2.6 SPICE Modelling

SPICE is an open-source industry standard analog circuit simulator. It is used to predict the behavior of integrated circuits and integrity of circuit design. SPICE can perform nonlinear DC, nonlinear transient and linear AC analysis of complex circuits. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, lossless and lossy transmission lines (two separate implementations), switches, uniform distributed RC lines, and the five most common semiconductor devices: diodes, BJTs, JFETs, MESFETs, and MOSFETs [2.9].

SPICE models can predict the IV characteristics of a diode using inbuilt equivalent circuit representation as shown in the Fig. 2.18.

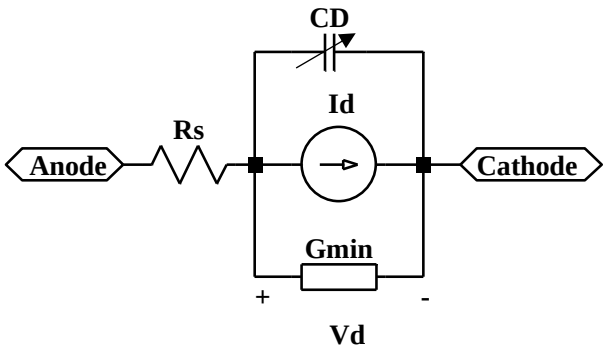

Figure 2.18: Diode Equivalent Circuit Representation in SPICE.

The parameters definitions in diode equations are tabulated in Table 3.1 :

N	Emission coefficient
Is	Reverse saturation Current
Gmin	Parallel transconductance
Rs	Series resistance
TT	Transit time
VJ	Junction Potential
CJ0	Zero Bias Junction cap
M	Grading coefficient
Gmin	Parallel transconductance
BV	Breakdown Voltage

Table 2.2: Diode SPICE Model Parameters.

Different regimes of operation of diode in SPICE is shown in the figure below with its corresponding equation:

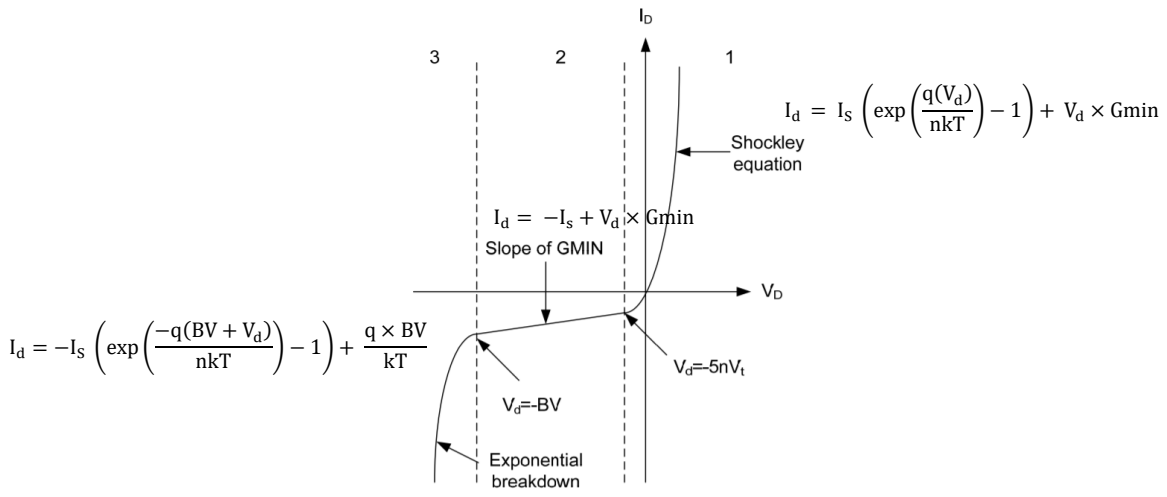

Figure 2.19: Different Regime of Operation of SPICE Diode Model [2.10].

At this point it can be noted that the diode model in SPICE allows only a fixed value of the emission coefficient, N. This is true when a diode operates in low injection regime. However, in general high-power devices (P-I-N diode for instance) operate in different injection regimes over a wide range of biases and hence the IV characteristics exhibit high level injection behaviors as shown in Fig. 2.7. In a practical scenario, to model such kind of non-idealities accurately using SPICE, often complex sub-circuit-based macro models are implemented [2.11]. We will follow this approach to model the DC and AC characteristics of a P-I-N diode.

2.6.1 DC Modelling of P-I-N Diode in SPICE

The measured IV characteristics of a P-I-N diode consists of several regimes of different slope. A subcircuit based modeling approach is required in order to extend the SPICE capabilities to predict the AC/DC characteristics of P-I-N diode. Many electronics devices are not represented by primitives but are still well suited as SPICE models. A SPICE subcircuit is built from a collection of devices that contain primitive models, voltage

and/or current sources, and/or other SPICE subcircuits. A generic structure of a subcircuit is shown below :

```
.SUBCKT <SubcircuitName> <Node1> <Node2> <Node3> .. <Noden>
    …  circuit definition …
   .ENDS <SubcircuitName>
```

Figure 2.20 Structure of Sample SPICE Subcircuit

The DC characteristic (on logarithmic y-axis) which consists of multiple slope regions can be modeled by combination of series or parallel diodes by following two rules:

(a) Inclusion of parallel diode: If the measured IV characteristic has a higher current than the ideal diode at a particular voltage, then this behavior can be modeled by inserting a parallel diode to the original ideal diode model accounting for higher current. This is shown in Fig. 2.21.

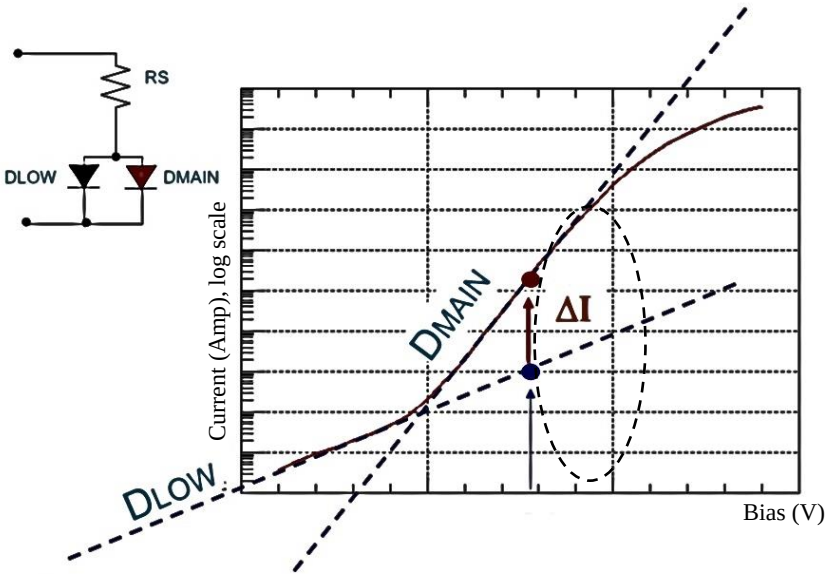

Figure 2.21: Higher Current at Given Diode Voltage is Achieved by Inserting DMAIN in Parallel to DLOW [2.11].

(b) Inclusion of series diode: If the measured IV characteristics have a higher voltage than the ideal diode at a particular diode current, then this behavior can be explained by inserting a series diode into the original ideal diode model. This is shown in Fig 2.22.

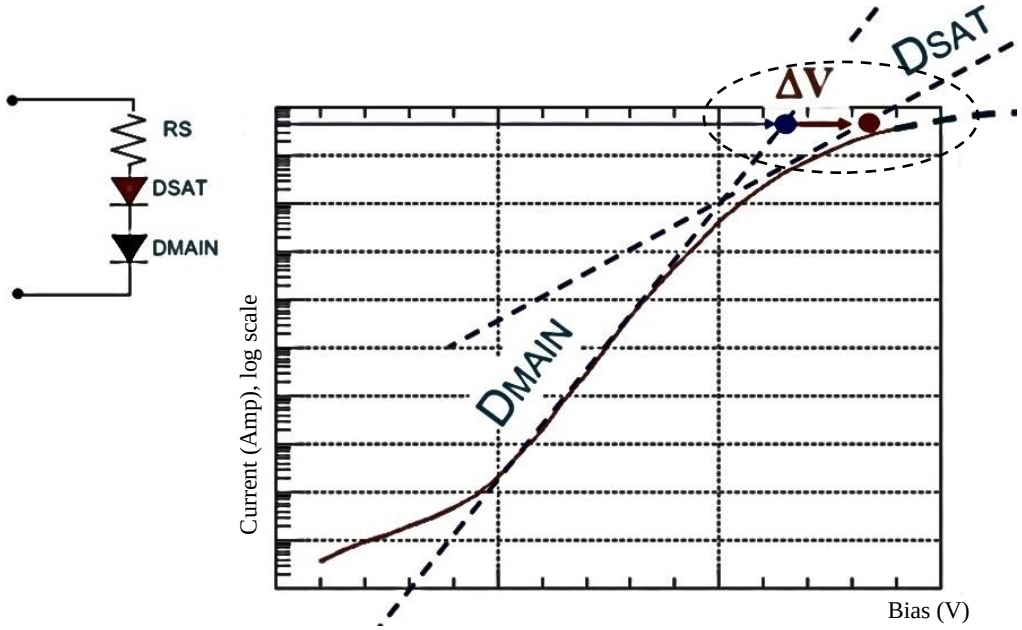

Figure 2.22: Higher Voltage at Given Diode Current is Achieved by Inserting DSAT in Series to DMAIN [2.11].

The measured IV characteristics of the P-I-N diode shown in Fig. 2.12 has evidently four distinct regimes in forward bias which can be modelled by a LOW current diode (DLOW), main diode (DMAIN), a saturation regime diode (DSAT) and finally a series resistance dominated region. The resulting subcircuit prototype which can predict the forward bias behavior is shown in Fig. 2.23.

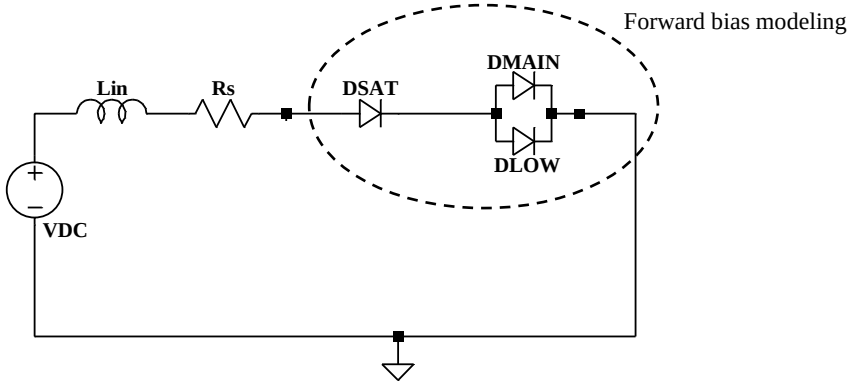

Figure 2.23: P-I-N Diode Subcircuit to Model the DC Forward Characteristics.

It can also be noted that the DC reverse IV characteristics of the diode in Fig. 2.11 consists of two different regimes which must be modeled by two parallel diodes. So, the subcircuit modifies to what is shown in Fig. 2.24.

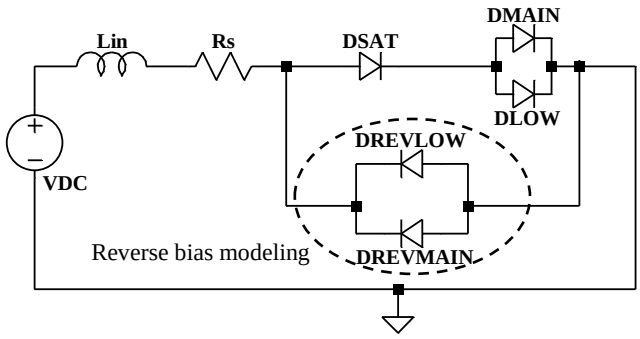

Figure 2.24: P-I-N Diode Subcircuit to Model the DC Forward and Reverse Characteristics.

The Fig. 2.25 shows the results of DC sweep in SPICE for the subcircuit shown in Fig. 2.24. By adjusting the saturation current, IS, and ideality factor, n, for each diode, an adequate fit to the DC characteristic is achieved as shown by the solid lines.

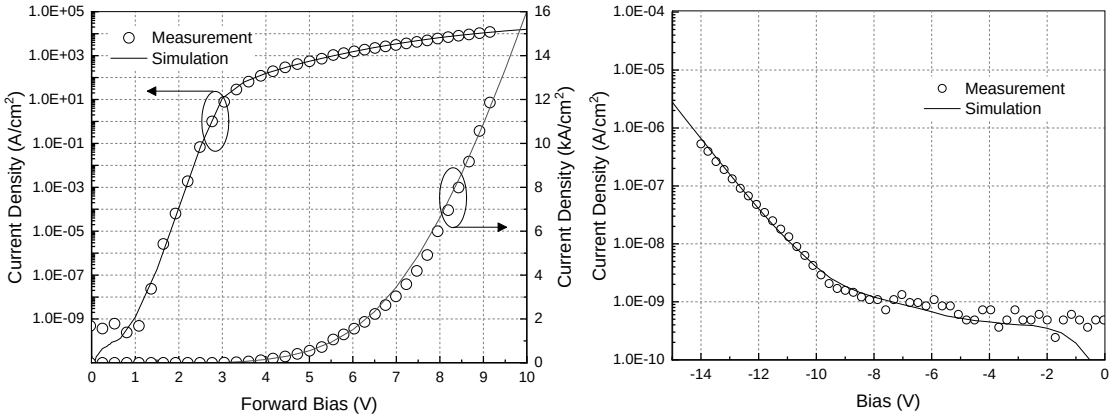

Figure 2.25: DC Fitting to the Measured Data in SPICE Using Subcircuit model. Left: Forward Bias , Right: Reverse Bias.

For diode voltages VD < ~1V the diode DLOW controls the current before the diode starts to turn on, and along with DREVLOW reflects the leakage paths due to defects and/or sidewalls. The diode DMAIN controls the exponential current in the range 1V < VD < ~3V. To reproduce the transition from exponential behavior to the quasi-linear saturation regime controlled by the diode series resistance, 'RS', we use the series connected diode DSAT0. The DSAT0 diode is used to reproduce transport mechanisms not captured by eq. (2.4), including effects due to non-linear p- and n-type contacts, carrier injection and space-charge conduction. The series resistance, 'RS', of the DSAT0 diode is set to be vanishingly small so that the on-resistance of the P-I-N diode is determined by overall 'Rs' as shown in Fig. 2.24. In the reverse bias regime, the parameters for the diode DREVLOW are adjusted to obtain the fit from 0 V to approximately 8 V, while DERVMAIN determines the current for higher reverse bias. Measurements of other diodes (not included here) show a reverse breakdown voltage, VBD, of approximately ~90V due to impact ionization, and we use that value here for the SPICE model.

	D_{LOW}	D_{MAIN}	D_{SAT}	D_{REVLOW}	$D_{REVMAIN}$
IS (A)	2.05×10^{-20}	6.06×10^{-20}	9.55×10^{-3}	2.96×10^{-19}	2.39×10^{-21}
N	8.28	3.01	34.6	29.4	23.8
RS (Ω)	0.001	0.001	0.001	0.001	0.001
CJ0	0	0	0	0	0
TT (ps)	0	0	1.4	0	0

Table 2.3: Diode Subcircuit Parameters for the DC Macro Model.

The diode small-signal conductance, $G_D = \partial I_D / \partial V_D$, is an important device metric that needs to be accurately reproduced by the compact model. Fig. 2.26 compares the measured and simulated G_D as a function of forward bias diode voltage. The reasonable

agreement between the measured and simulated diode conductance suggests the model is sufficiently accurate to reproduce first order differential behavior such as G_D.

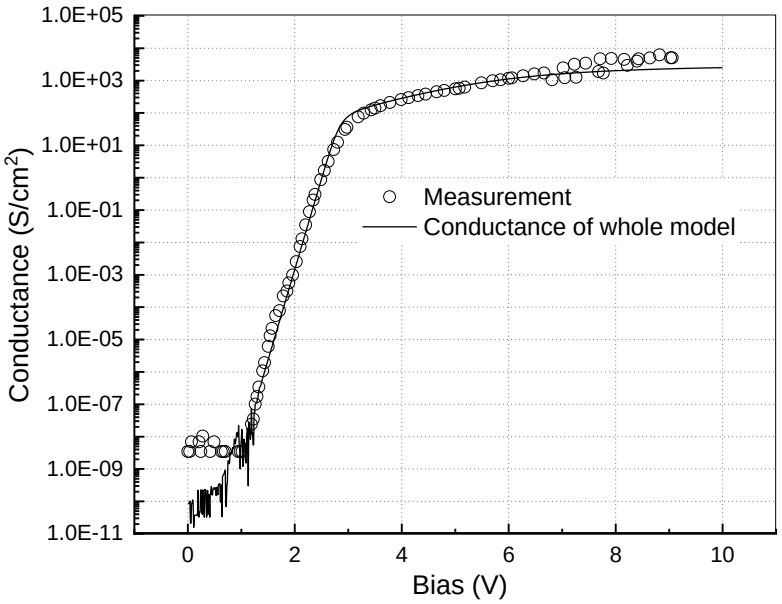

Figure 2.26: The Total Diode Conductance (Open Circles) as Determined by Differentiating the Measured Data in Fig. 2.12. The Solid line is the Diode Small Signal Conductance from the SPICE Model.

2.6.2 AC Modelling of P-I-N diode in SPICE

To model the small signal characteristics of the device, we must model the capacitance and first order characteristic of the device correctly as the frequency and bias changes. The total capacitance of a junction diode is the sum of the depletion capacitance, C_{DEP}, which dominates at low currents, and the diffusion capacitance, C_{DIFF}, that increases rapidly as the diode begins to turn on. Diode SPICE models use the product of transit time, TT, and small signal conductance to simulate the diffusion capacitance, while C_{DEP} is derived from the depletion approximation.

$$C_D = C_{DEP} + C_{DIFF} \tag{2.10}$$

$$C_D = \frac{CJ0}{\left(1 - \frac{V_D}{VJ}\right)^M} + TT \times G_D \approx CJ0 + TT \times G_{DSAT} \tag{2.11}$$

Both terms are included in the expression for C_D given in eq. (2.10). From the data in Fig. 2.17, the diode capacitance is constant below ~ 4V indicating that the grading coefficient, m, in the depletion capacitance expression is approximately zero. For this reason, the depletion capacitance is represented by a constant value capacitance, CJ0, connected between the anode and cathode as shown in the circuit of Fig. 2.27.

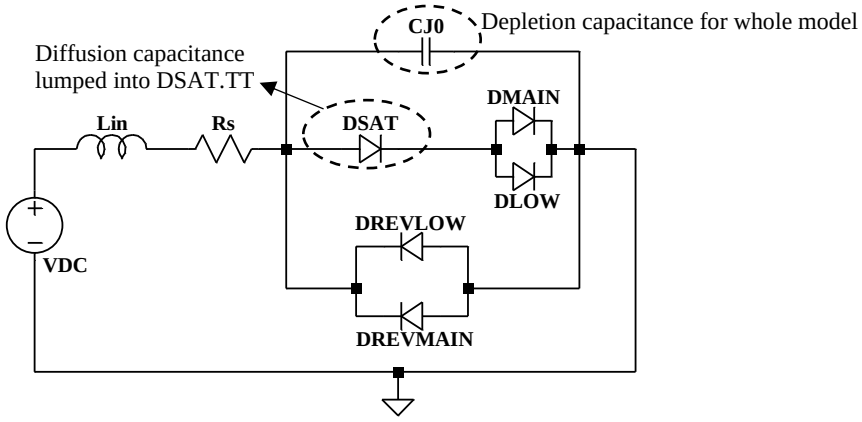

Figure 2.27: P-I-N Diode Subcircuit with Capacitances Modelled.

The increase in the total capacitance that is observed in Fig. 2.17 for VD > 4V corresponds with the turn-on voltage of the diode current seen in Fig.2.25. In this 'ON' regime the diode conductance is controlled by DSAT, before it is ultimately limited by the diode series resistance, Rs. For the model developed here the diffusion capacitance is associated entirely with diode DSAT, all the other diode transit times being set to zero. As a result, eq. (2.10) can be modified to the simplified form in eq. (2.11) which we use to fit

the data in Fig.2.28. A transit time of 1.4 ps for diode DSAT reproduces the rapid increase in CD using the diode conductance G_{DSAT}.

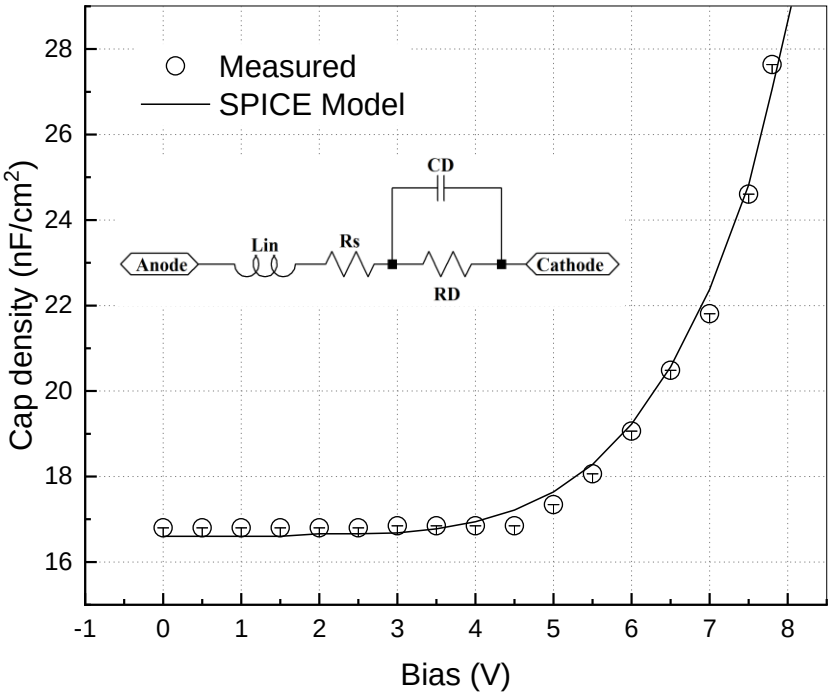

Figure 2.28: The Capacitance (Open Circles) of the Schottky P-I-N Diode Is Extracted as a Function of Bias by Fitting the RLC Model (Shown in the Inset) to the Z-parameters Derived from the Measured S-parameters in Fig. 2.16. (Solid Line Model Fit)

For AC conditions and DC bias VD > 4V the diode model of Fig. 2.27 is consistent with the RLC circuit in the inset of Fig. 2.28. The capacitance of diode DMAIN is set to zero such that it appears as an AC open circuit. At the same time, very little AC signal is dropped across DMAIN because the AC current is limited by the conductance of DSAT for VD > 4V. As a result, the capacitance of the diode sub-circuit is CJ0 in parallel with $C_{DIFF} = TT \times G_{DSAT}$. The diode capacitance, C_D, of eq. 2.11 is in parallel with the small signal conductance of DSAT, and the total impedance includes the diode series resistance, Rs and negligible series inductance Lin.

The diode shunted co-planar waveguide was configured for two-port RF measurements as shown in the photograph of Fig. 2.29. The forward transmission, S21, and the input reflection, S11, were recorded from 1-25GHz with bias voltages of 0 – 7.8V applied to the diode.

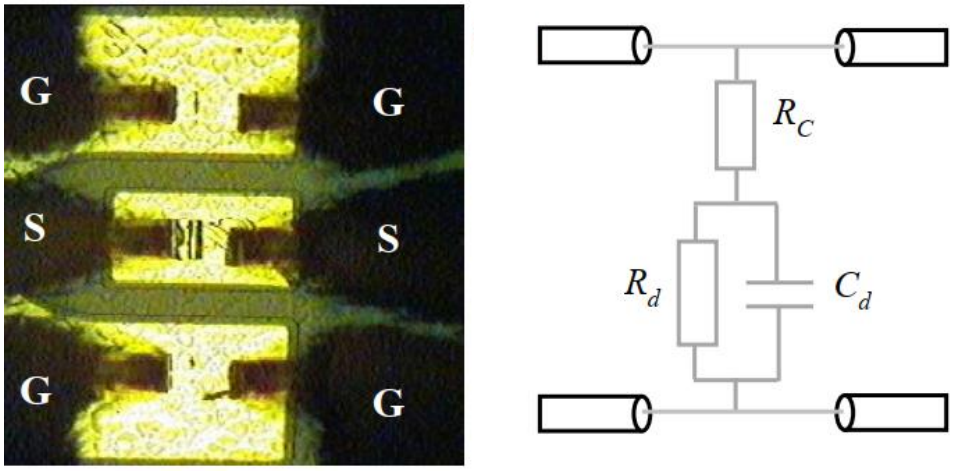

Figure 2.29: S-parameters Measurement Setup and the Equivalent Lumped Model of the Diode.

The s-parameter equation for the structure shown in the Fig.2.29 can be written as:

$$S_{11} = \frac{Z_0|\,|Z_d - Z_0}{Z_0|\,|Z_d + Z_0} \tag{3.3}$$

$$S_{21} = 2\frac{Z_0|\,|Z_d}{Z_0|\,|Z_d + Z_0} \tag{3.4}$$

Where, Z_0 is the characteristics impedance of the system and Z_d is the diode impedance. The measured data is shown as open symbols in Fig. 2.30 along with simulated values of S21 and S11 using the SPICE simulation of the diode subcircuit.

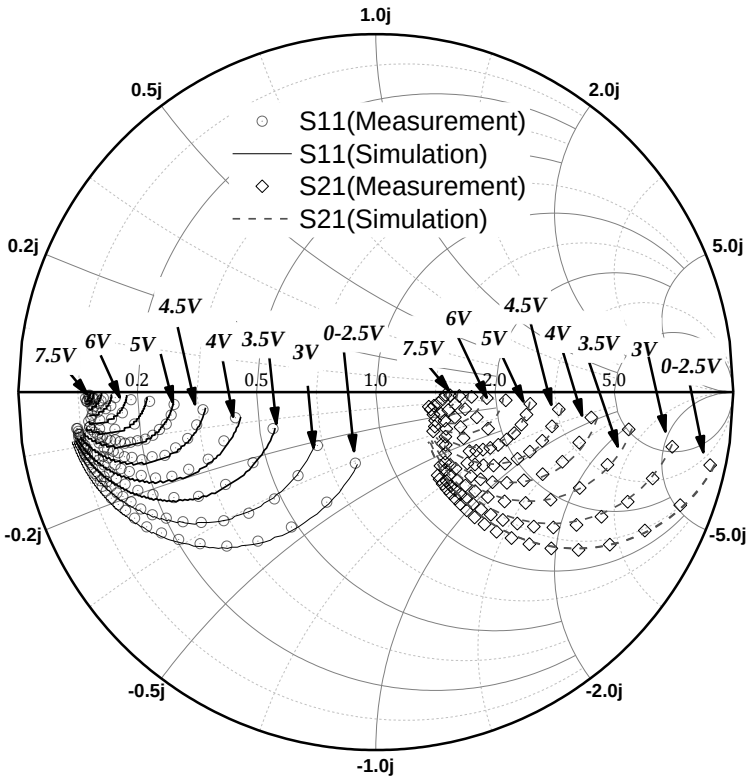

Figure 2.30: Measured and Simulated S-parameters.

When operated as biased controlled attenuators [2.12] a control voltage is used to switch the diode receiver protector from a low insertion loss, off-state, to a highly attenuating conducting state, for which the input power is reflected. With two GSG probes placed onto the pads the diode behaves as a shunt attenuator connected between the signal and ground lines of the RF transmission line formed by the GSG probes and the coaxial cables. In this fashion the insertion loss, S21, and the return loss, S11, have been measured as a function of diode voltage for a frequency of 1 GHz, see Fig 2.31. The DC diode voltage is applied by means of a bias-T connected to port-1 of the 2-port measurement system.

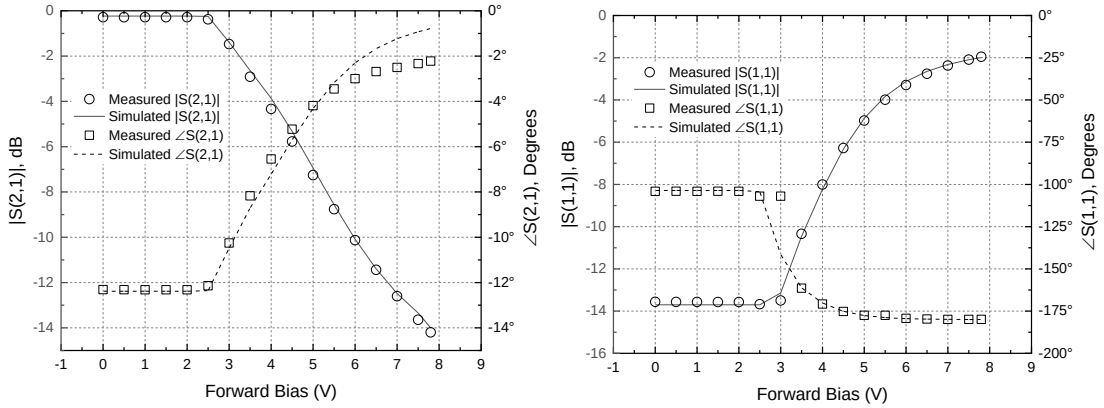

Figure 2.31: S-parameters Fit at 1GHz . Left: Mag , Right: Phase.

As shown in Fig. 2.31 the diode shunt contributes less than 0.3 dB insertion loss until the diode starts to turn on at ~ 2.5V of forward bias. For the highest bias of 7.8V at which the 100 mA current compliance occurs, the diode insertion loss is 14 dB and the return loss is 2 dB. The solid lines in the graph show the simulated magnitude and phase of S11 and S21 derived from the lumped-element sub-circuit. The good agreement between the measured and simulated insertion loss confirms that the SPICE model sub-circuit is sufficiently accurate for the design of diamond-based receiver protectors such as the two-stage, self-biasing circuit described in Chapter 4.

2.6.3 Parameter Optimization and Extraction in ICCAP

IC-CAP (Integrated Circuit Characterization and Analysis Program) is the industry standard for DC and RF semiconductor device modeling. IC-CAP extracts accurate compact models used in high speed/digital, analog, and power RF applications. The following set of steps gives a brief summary for creating and optimizing a SPICE model for P-I-N diode in ICCAP:

(a) To start with the tool, a new model must be created in the main ICCAP window as shown in Fig.2.32.

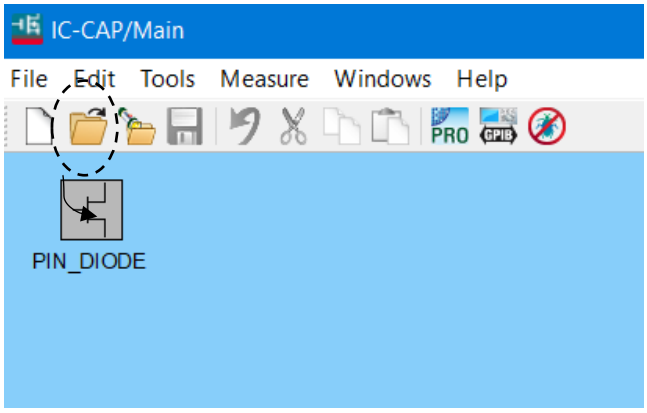

Figure 2.32: Creating New Model in ICCAP Main Window.

(b) For the newly defined model, we need to create several setups each corresponding to our measurement scenario as shown in Fig. 2.33. These are followed by input/output specifications.

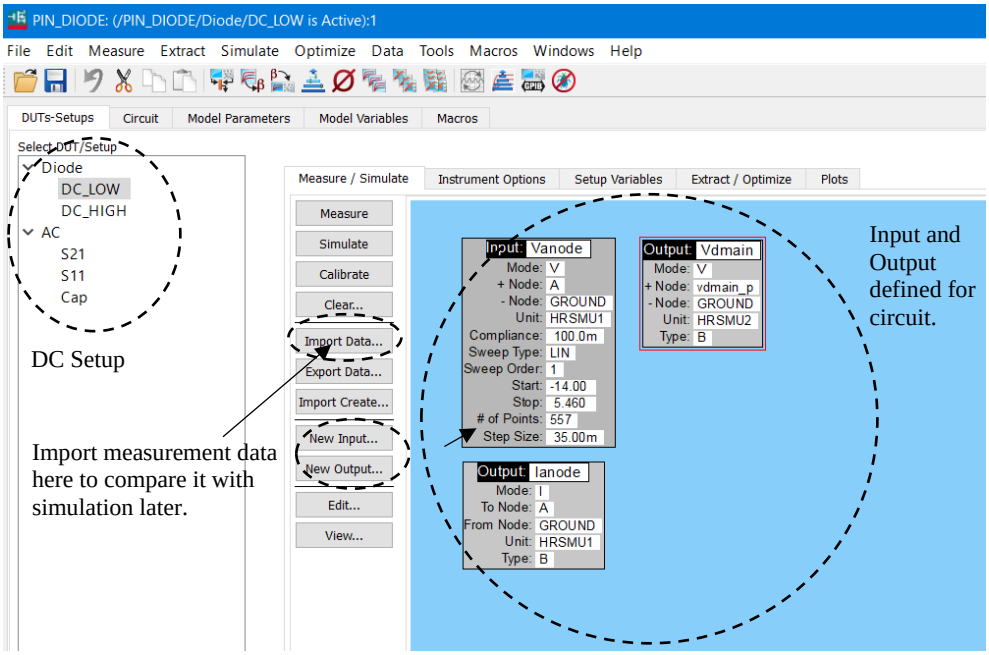

Figure 2.33: Creating New Setup and Defining Input and Output Variables in ICCAP DUT.

(c) After defining the top-level input and output specifications, a complete SPICE netlist with all the primitive elements is defined in Circuit section of the Setup. Note that this is a global definition, and it holds same for all the setups. The P-I-N diode model netlist developed for this work is shown below:

```
.OPTION limpts=3000 gmin=1e-14

*Initialize subcircuit with ports connected to what is defined in Input/Output specification at top
level
.subckt model_schottky_pin 1=A 2=C 12=vdmain_p

*Short port 1 to port 2 to create a Transmission line structure
Rshort 1 200 0.001
Lshort 200 2 1p

*port 1 model: port name: 1 with parasitic
Rin 1  10 5
Cdiode 10 0 1.4pf
Ccross 1 2 1f
*****************************************************************
* diode sub circuit
*****************************************************************
*forward bias modeling
DSAT0 10 12 DSAT0
DMAIN 12 0 DMAIN
DLOW 12 0 DLOW
*reverse bias modeling
DREV 0 10 DREV
DREV2 0 10 DREV2
*****************************************************************
*model cards (need to be optimized later)
.MODEL DMAIN D IS = 4f  N = 4.3 BV = 1000  IBV = 1m
+ RS = 1.1 CJO = 680f VJ = 2.164 M = 0.01  FC = 0.5 TT = 0
+ EG = 1.110  XTI = 3.0

.MODEL DLOW D IS = 10p N = 60 BV = 1000 IBV = 52E-3
+ RS = 0.1  CJO = 0 VJ = 2.164  M = 0.9 FC = 0.5 TT = 0
+ EG = 5 XTI = 3.0

.MODEL DSAT0 D IS = 15m N = 30 BV = 1000  IBV = 52E-3
+ RS = 0 CJO = 0  VJ = 2.164 M = 0.9  FC = 0.5  TT = 0
+ EG = 5  XTI = 3.0

.MODEL DREV D IS = 30a  N = 15.5  BV = 1000  IBV = 52e-4
+ RS = 2 CJO = 0 VJ = 2.164 M = 0.5 FC = 0.5 TT = 0
+ EG = 1.110 XTI = 3.0

.MODEL DREV2 D  IS = 30a N = 15.5 BV = 1000  IBV = 52e-4
+ RS = 2 CJO = 0 VJ = 2.164 M = 0.5  FC = 0.5 TT = 0
+ EG = 1.110  XTI = 3.0

.ends
```

(d) We can define additional variables in “Model variables” tab which are specific to the whole model and can be tuned in later optimization stage. In this case we are just defining the simulator to be used as SPICE (Available options are : LTSPICE, HSPICE, PSPICE etc). We can also define parameters like TNOM to vary the nominal temperature during optimization process.

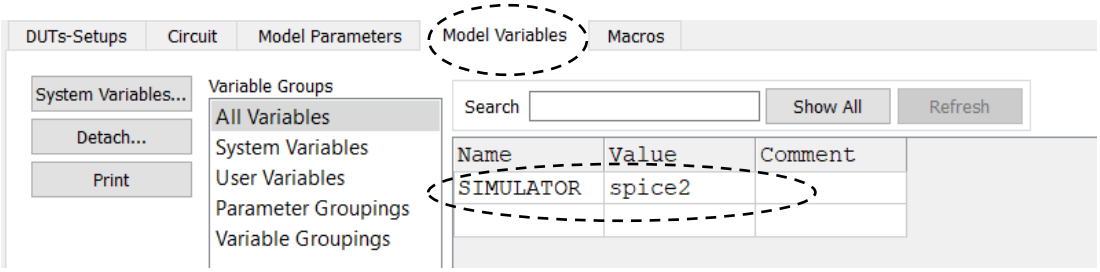

Figure 2.34: Defining Model Variables.

(e) The next step is defining all the plots. This will help us to visualize the output variable between measurement and simulation. The plot definition is straightforward as shown in Fig. 2.35.

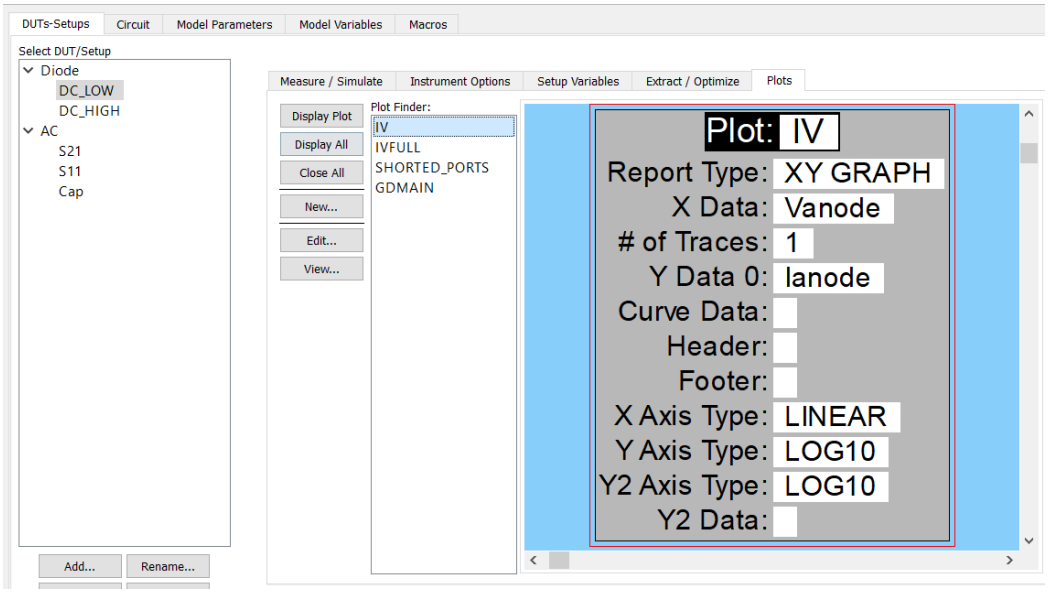

Figure 2.35: Plot Setup for Plotting DC IV.

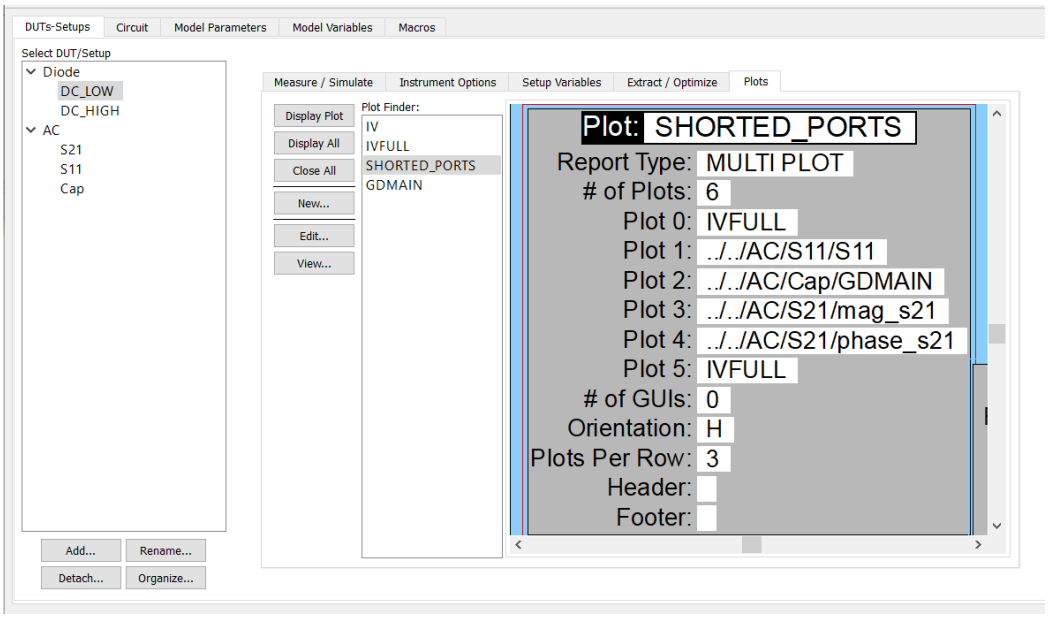

Figure 2.36: A Sample Multiplot Window to Plot all the Optimizing Output.

(f) Once the setup is done, we hit simulate button and open a particular plot that we want to optimize. In this case, Fig. 2.37 is showing a multiplot where we want to optimize all the output variables at once, namely: DC-IV, S-parameters, and Capacitance vs Voltage.

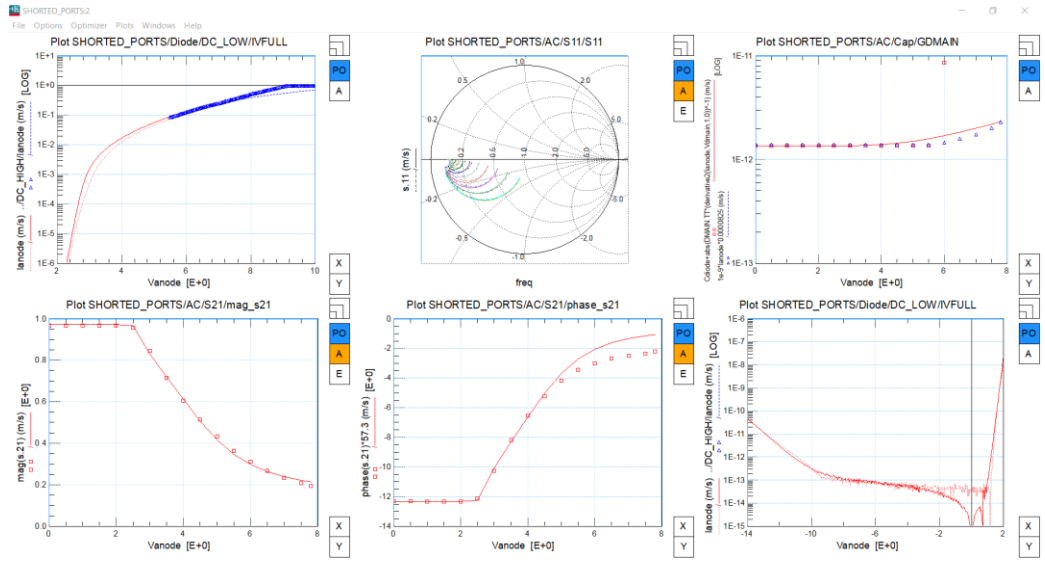

Figure 2.37: A sample Plot Window Showing Measurement and Simulation Data Fit.

(g) The plot obtained in step(f) shows the measurement data superimposed with simulation solid lines. Initially these traces will be way off (because we have no information about model parameters in the start) and optimization needs to be done in order to bring them closer and reduce the model error. The optimization task is invoked by choosing optimization as shown in Fig. 2.38.

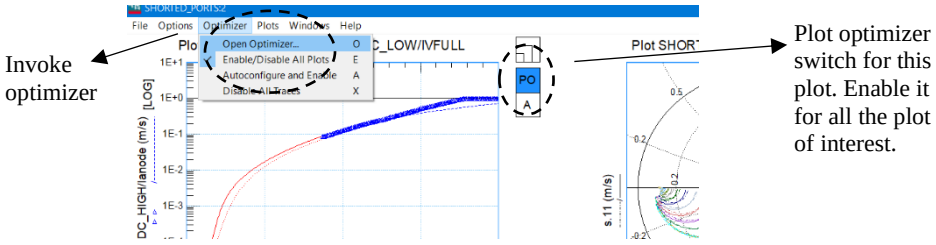

Figure 2.38: Invoking Optimizer.

(h) After launching the optimizer, we must add the parameters that need tuning for the output plot. These parameters can come from subcircuit level, model level or user defined level as shown in Fig. 2.39. We then launch the tuner after adding relevant variables into the optimization list.

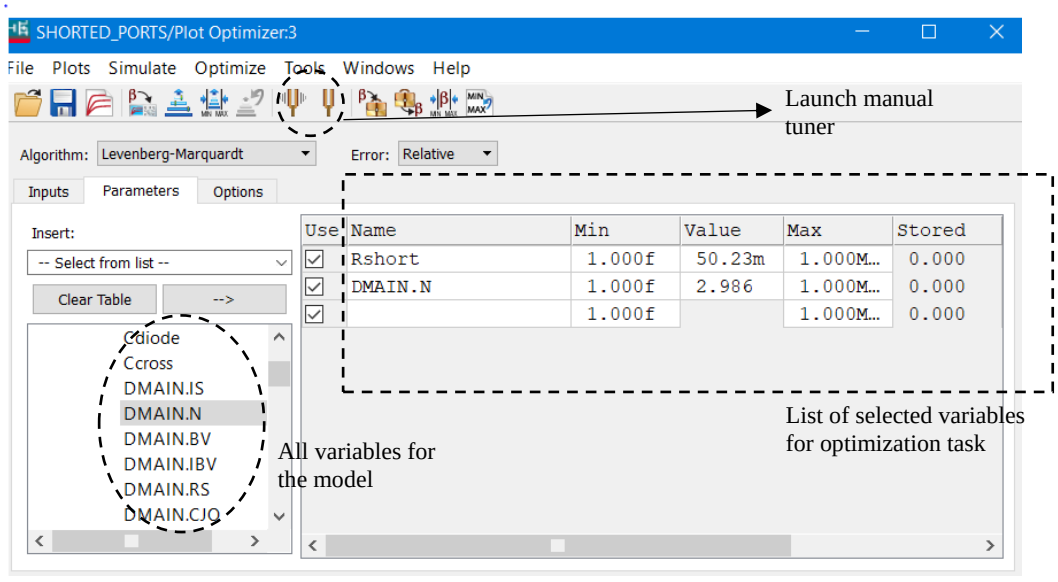

Figure 2.39: Adding List of Variables for Optimization.

(i) Upon executing tuner, ICCAP updates the simulation result in the plot immediately as soon as any parameters are tuned from the tuner tab. This is a manual process but allows us to observe the impact of model parameters on the output variables and help us to move in the direction where the model fits the measured data.

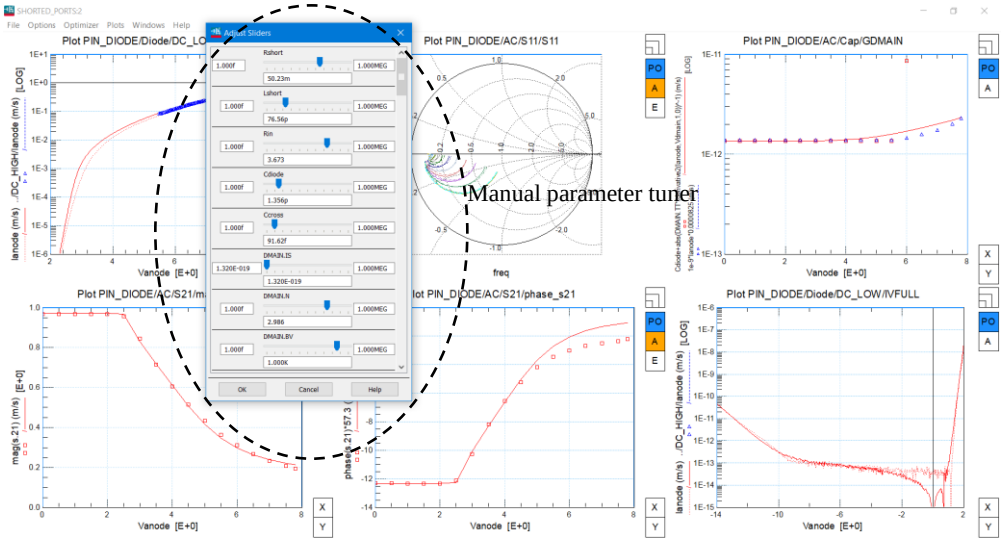

Figure 2.40: : Manual Tuning for Optimization.

(j) If the upper and lower limit of optimization parameters are known to some accuracy(step (h)), then one can launch the optimization task in ICCAP which finds the model fitting solution automatically with least square error as shown in Fig 2.41.

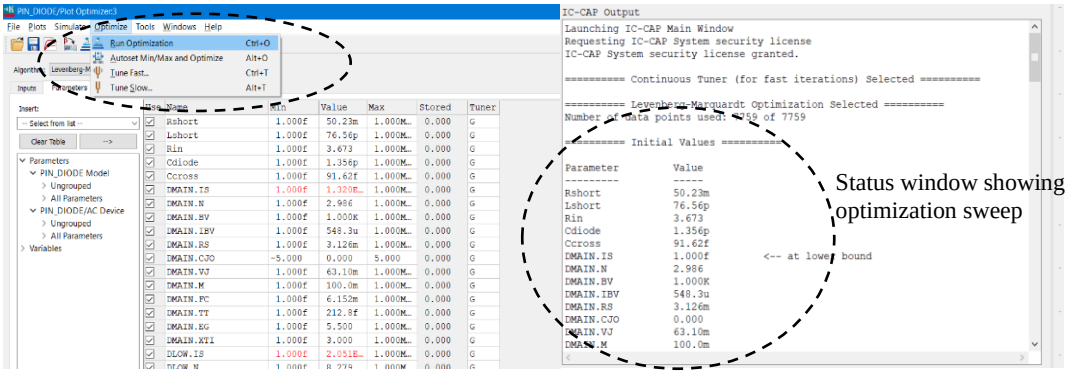

Figure 2.41: Running Automatic Optimization Task.

For the P-I-N diode used in this research, the optimized parameters are shown in Table 2.4 obtained after series of steps explained above.

	D_{LOW}	D_{MAIN}	D_{SAT0}	D_{REVLOW}	$D_{REVMAIN}$	D_{CJ0}
IS (A)	2.051E-020	6E-020	9.55e-3	2.959e-019	2.388e-021	1e-30
N	8.279	3.01	34.55	29.39	23.81	100
BV (V)	90	90	90	90	90	90
IBV (A)	5e-3	5e-3	5e-3	5e-3	5e-3	5e-3
RS (Ω)	1e-3	1e-3	1e-3	0.2	4.4e-005	1.37e-12
CJO (F)	0	0	0	0	0	2.26e-12
VJ (V)	11.08	11.08	11.08	11.08	11.08	11.08
M	1	1	1	1	1	0.159
FC	0.95	0.95	0.95	0.95	0.95	0.95
TT (s)	0	0.13e-12	0	0	0	0
EG (eV)	5.5	5.5	5.5	5.5	5.5	5.5
XTI						

Table 2.4: Final Optimized SPICE Model Parameters for the P-I-N Diode Subcircuit.

2.6.4 Spectrum Modeling

In the previous few sections, the DC and small signal modeling strategy of p-i-n diodes have been presented. However, when it comes to predicting crucial large-signal effects such as harmonic and intermodulation distortion, a good non-linear model is going to be needed instead. The main non-linear effects encountered in, the ON and OFF states, are

principally generated, when a relatively large RF signal is present, by two very different non-linear mechanisms inside the device:

i) Conductivity modulation of the charge, within the I-layer in ON state [2.13] and

ii) Capacitance modulation [2.14]

The advantage of using the model shown in fig. 2.27 is that it allows us to lump both of above-mentioned effects into DSAT diode whose conductance determines the overall capacitance (by TT parameters) and the excellent agreement of first order derivative. Apart from these, overall series inductance must be tuned to model the high order non-linearity.

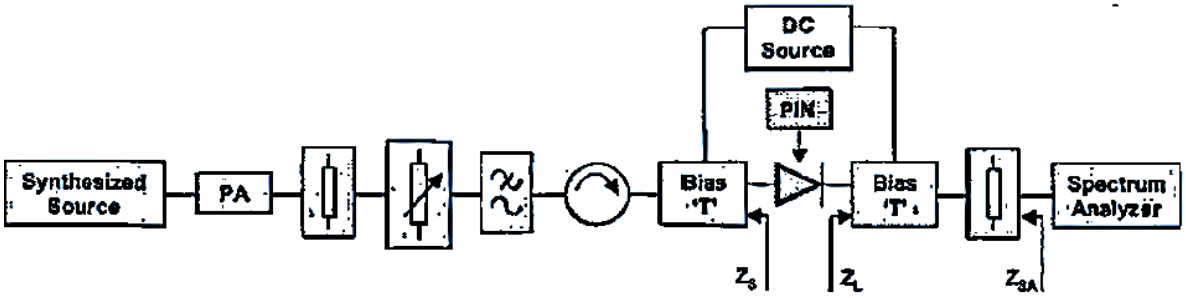

Figure 2.42 The Large Signal Measurement Setup Used to Characterize the Harmonic Distortion(HD) of P-I-N Diode [2.18].

The basic large signal measurement set-up is shown in Fig. 2.42. The accuracy and consistency of any HD measurement is very much dependent on the matching conditions in which the DUT is tested, at the fundamental as well as the harmonic frequencies. The synthesized source (Agilent's vector signal generator) generates low power signal which further gets amplified by highly linear power amplifier (noise filtered out) which is then fed into the matched input terminal of the diode and the output is connected to the matched load of spectrum analyzer.

Fig. 2.43 shows the harmonics that appear at the 50 Ω load for a 1 GHz single-tone input. From the graph, it is evident that for a low input power signal (<20dBm), there is no significant distortion in output signal as the diode is in completely off state. As the input power increases beyond +20 dBm, the second, third and fourth harmonics start to grow significantly in the output signal. The sub-circuit model of Fig. 6 predicts this non-linearity with reasonable agreement as shown by the solid lines.

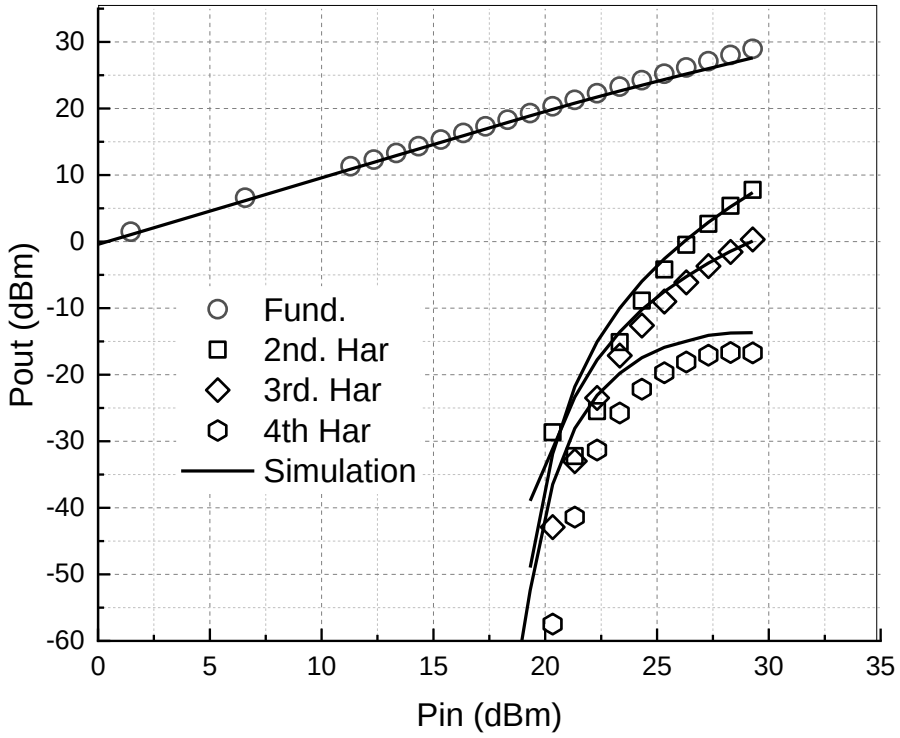

Figure 2.43 Measured and Simulated Harmonics for a Single Tone Input at 1GHz.

2.7 TCAD Modelling

TCAD device simulation tools simulate the electrical characteristics of semiconductor devices, as a response to external electrical, thermal, or optical boundary conditions imposed on the structure. The Silvaco Atlas simulator was used to simulate the electrical characteristics of diamond devices. The detailed simulation methodology has been

described in [2.15] and here we used a similar approach. Diamond being a new user defined material in the TCAD simulator requires calibration of material parameters, incomplete ionization parameters, mobility models and recombination models. Some of the material parameters used for diamond device simulation are listed in table 2.5.

Room temperature band gap	5.45 eV
Effective density of states for electrons	1.021e+19 cm^{-3}
Effective density of states for holes	2.166e+19 cm^{-3}
Electron Affinity	0.38eV
Electron saturation velocity	2.7e7 cm/s
Hole saturation velocity	1.2e7 cm/s

Table 2.5: Some Important Material Parameters of Diamond Used for TCAD Simulation.

At room temperature, the impurities in diamond have large activation energies which also depend upon their concentration. The TCAD simulator can account for impurity freeze-out with appropriate degeneracy factors GCB and GVB for conduction and valence bands. This effect has been modeled in TCAD using equations:

$$\frac{N_D^+}{N_D} = \frac{1}{1 + GCB \exp\left(\frac{E_{F_n} - \left(E_C - (A.EDB - B.EDB \cdot N_D^{\frac{1}{3}})\right)}{kT}\right)}$$

$$\frac{N_A^-}{N_A} = \frac{1}{1 + GVB \exp\left(\frac{-E_{F_p} + \left(E_V + ((A.EAB - B.EAB \cdot N_A^{\frac{1}{3}})\right)}{kT}\right)}$$

Where N_D and N_A are net compensated n-type and p-type doping. The above two equations handle the incomplete ionization in diamond for n and p type impurities respectively. The model parameters used for the simulation are tabulated below:

A.EDB	0.57eV
B.EDB	0
A.EAB	0.416eV
B.EAB	5.4329e-8
GCB	0.5
GVB	4

Table 2.6: Incomplete Ionization Parameters Used for TCAD simulation.

After incomplete ionization, mobility is another important parameter that influences the electrical charateritics of the device. There are a wide variety of mobility models available for silicon and other materials in Silvaco TCAD, however for diamond, electron and hole mobility is based on hopping mechanism. It has been reported that nearest neighbor hopping (NNH) and variable range hopping (VRH) are the major conduction mechanisms in moderate to highly doped n and p type diamond respectively. To model devices with both n-type and p-type diamonds therefore requires an accurate model of NNH and VRH conduction. These models have been implemented in Silvaco via a built-in C language interpreter. The detailed equations for mobility are outlined in [2.15].

The dependence of the diamond band gap with temperature can be modeled by using equation [2.16]:

$$E_g(T) = 5.45 + \frac{(1.01)(300^2)}{3.95 \times 10^6 + 300} - \frac{(1.01)(T^2)}{3.95 \times 10^6 + T}$$

Where temperature T is in Kelvin and 5.45eV represent the band gap at T=300K.

To calibrate the material parameters and models, a 3D resistor as shown in figure 2.44 with uniformly doped n-type or p-type diamond was simulated in Silvaco. Compensation of 10% was used for all doping concentrations in the substrate material. The resistance is extracted from the slope of the I-V curves (between a pair of ohmic contacts) for very low voltages. Figure 2 shows the fit between the resistivity obtained from Silvaco simulations and the experimental data [2.17] as a function of temperature.

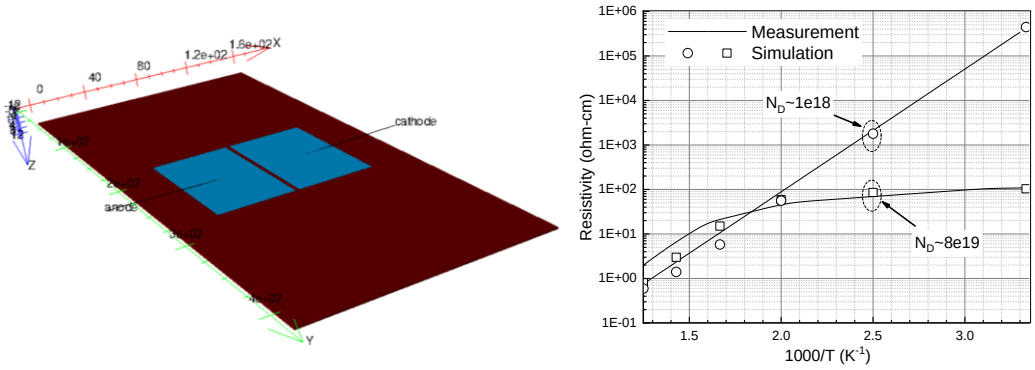

Figure 2.44 Left: 3D Resistor in TCAD, Right: Plot of Resistivity vs Temperature of N-Type Diamond Film for Various Doping Concentration

With the calibrated TCAD models, a 3D P-I-N diode structure was created in Silvaco atlas as shown in Fig. 2.45 (normalized view). The top metal contact to n type diamond was set to have a variable work function and finite contact resistance while the contact to p-type diamond was defined to be ohmic.

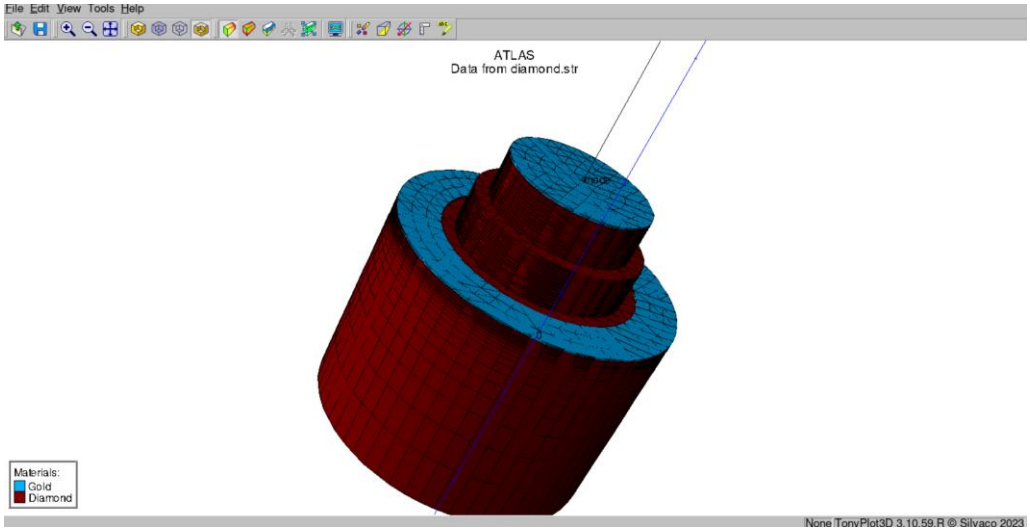

Figure 2.45 Normalized View of the Diode Built in TCAD Tool.

The mesh was initiated with doping profile as shown in Figure 2.17 with the help of an external file. In-built Shockley-Reed-Hall Recombination (SRH) model was used to model the recombination process in the device. As shown in Fig. 2.46, a good agreement between TCAD simulated IV data and measured data was obtained after tuning the simulation variables.

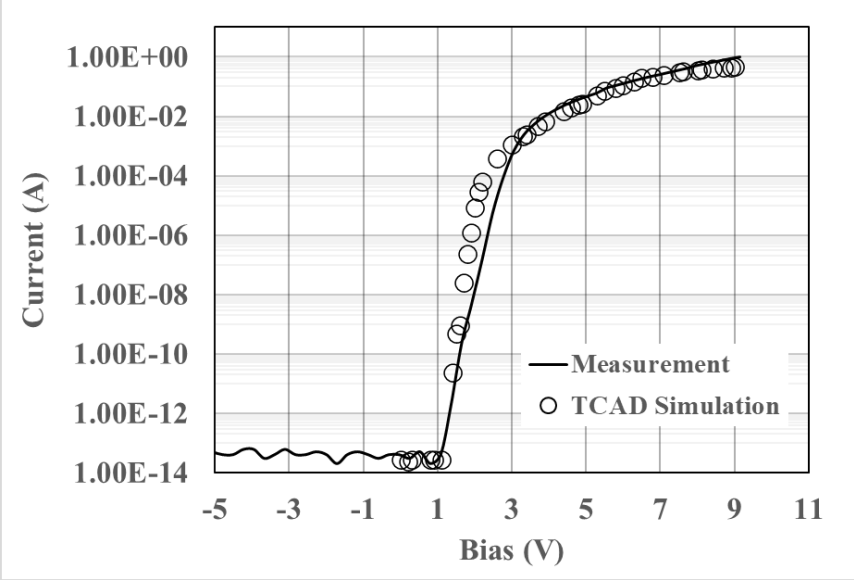

Figure 2.46 Fit Between TCAD Model and Measurement Data.

CHAPTER 3.

LOW RESISTANCE OHMIC CONTACT ON N-TYPE DIAMOND

3.1 Introduction

Diamond is an ultra-wide band gap material that can be doped to have p- or n-type characteristics. P-type diamond with boron impurities occurs naturally, with the boron forming an acceptor level that is 0.37eV above the valance band maxima [3.1]. Boron doped diamond can also be produced in the laboratory using high-pressure, high-temperature (HPHT) or chemical vapor deposition (CVD) growth techniques [3.2]. In contrast, n-type diamond is naturally rare and difficult to produce artificially.

Nitrogen is the most common group V donor element for the diamond lattice, but it occupies deep impurity states in the crystal [3.3]. Theoretical calculations have shown that phosphorus can be used as an n-type dopant with shallow donor states but imposes several challenges during doping because of the low solubility of phosphorus in the diamond lattice [3.4]. Despite the challenges involved in making n-type diamond, recent advances in CVD techniques have allowed researchers to grow phosphorus-doped epitaxial layers on (111) diamond substrates with the concentration of phosphorus atoms varying from 10^{16} cm^{-3} to 10^{20} cm^{-3} [3.5-3.7]. Achieving phosphorus concentrations beyond this range is an active area of research.

To make high efficiency devices on p- or n-type semiconductors, it is important to have a linear, low resistance current-voltage (I-V) characteristic across the contact, i.e., perfectly Ohmic behavior. But in practice there exists a barrier between the contact material and the semiconductor surface that inhibits ideal current flow, leading to non-linear, high resistance

contacts. For boron doped p-type diamond a low specific contact resistivity, ρ_c, of order 10^{-6} Ω.cm^2 can be achieved using a Ti/Pt/Au metal contact stack [3.8]. On the other hand, achieving low resistance contacts with linear I-V characteristics for phosphorus-doped n-type diamond is more challenging, and minimum values of ρ_c in the range 10^{-3} to 10^{-2} Ω.cm^2 are typically reported. Fig. 3.1 shows the specific contact resistivity of phosphorus doped (111) diamond/metal interfaces from several references.

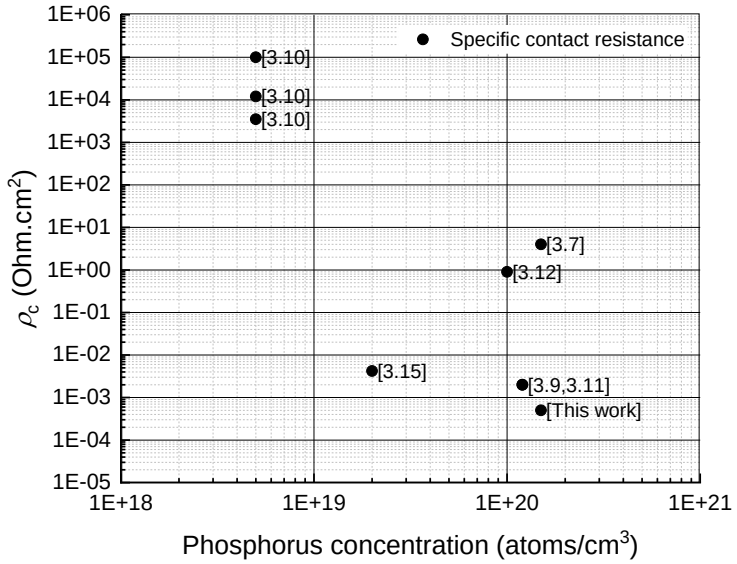

Figure 3.1 The Specific Contact Resistivity to N-Type Diamond as a Function of Phosphorus Concentration.

In this chapter we demonstrate the fabrication of high-linearity, low resistance Ohmic contacts on phosphorus doped (111) diamond substrates using a nano-crystalline (nano-C) interface layer between the crystalline diamond and the metal contacts. Transfer length method (TLM) test structures were fabricated using a Ti/Pt/Au metal stack with a 50 nm thick nano-C interface layer between the titanium and n-type diamond. Titanium serves as an adhesion layer with the potential to form a thin TiC interface layer after high temperature annealing. Platinum serves as a diffusion barrier to the final layer of gold which in turn

provides a high conductivity and ductile surface layer for electrical probing or wire bonding. After annealing at 700^0C the resulting contact structure demonstrates highly linear current-voltage characteristics with a specific contact resistance of $3x10^{-4}$ $\Omega.cm^2$, almost an order of magnitude lower than previous reports using Ti/Pt/Au alone.

The samples used for this study were single crystal high-pressure, high-temperature (HPHT) diamond substrates with cleaved (111) surfaces. An epitaxial layer of phosphorus doped diamond was grown on the nominally un-doped substrate using microwave plasma assisted chemical vapor deposition (MPCVD). Details of the MPCVD growth have been presented in [3.7]. An optical micrograph of the diamond sample is shown in Fig. 2.

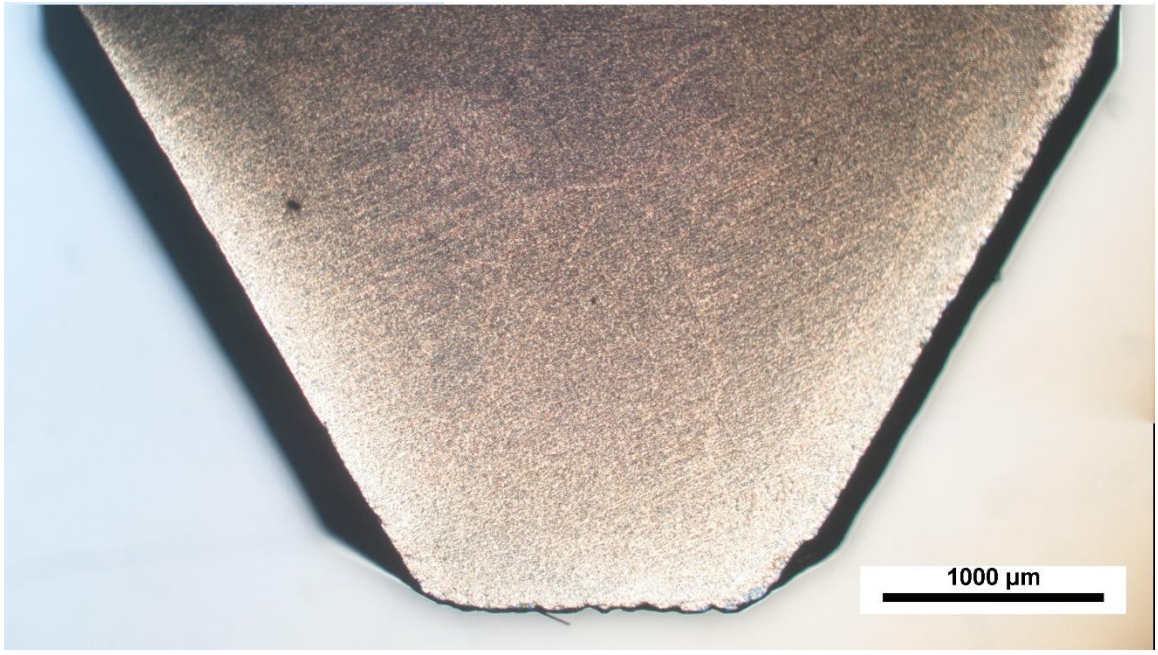

Figure 3.2 Diamond Substrate with Heavily Phosphorus Doped Epitaxial Layer Used for Contact Study.

The growth of the MPCVD epilayer is optimized to achieve high phosphorus doping concentrations. Secondary ion mass spectroscopy (SIMS) performed by Evans Analytical

Group (EAG) confirms a phosphorus concentration greater than 10^{20} atoms/cm^3 throughout the ~ 6.5 μm thick film, see Fig. 3.3.

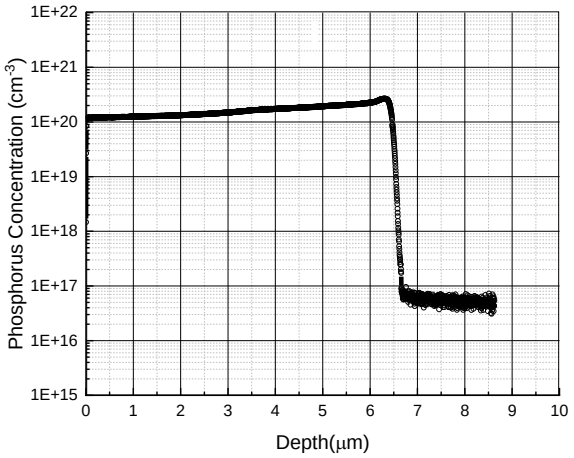

Figure 3.3 SIMS Data of the Obtained Sample Suggesting Heavy Phosphorus Doping.

3.2 Hall effect analysis

Hall voltage measurements are used to derive the type of semiconductor (n or p), the free carrier density, and the mobility. The van der Pauw method is used to measure sheet resistivity and Hall mobility of thin films. It was first reported in 1958 by Leo J. van der Pauw of Philips Research laboratories [3.18]. This four-wire method is used on small, flat shaped samples of uniform thickness with four terminals. Current is forced through two terminals on the sample, and the voltage drop is measured across the opposite two terminals. This measurement is repeated eight times around the periphery of the sample as shown in Fig. 3.4.

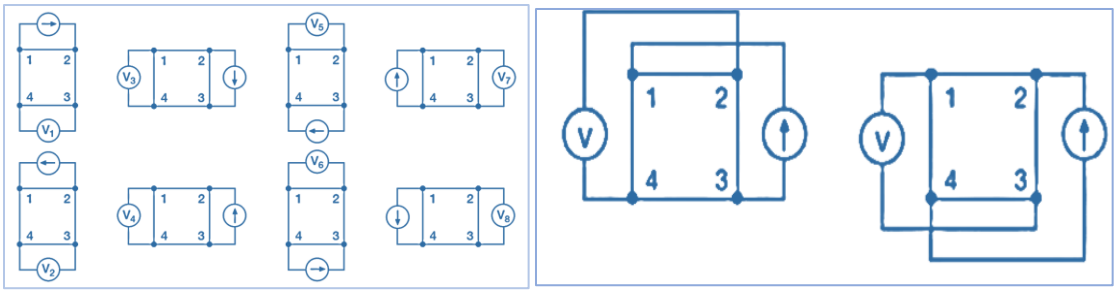

Figure 3.4 Left: Van Der Pauw Resistivity Measurement Conventions. Right: Hall Voltage Measurement Configurations.

Using those eight measurements, the average resistivity is determined using equation:

$$\rho_{avg} = \frac{\pi}{8\ln(2)} t_s (f_a(V_1 - V_2 + V_3 - V_4) + f_b(V_5 - V_6 + V_7 - V_8))$$

where:

t_s is sample thickness (cm),

V_1 -V_8 represent the voltages measured by the voltmeter (V),

I is the current through the sample (A),

f_a and f_b are the geometrical factors based on sample symmetry.

Hall voltage measurements are important to semiconductor material characterization because from both the Hall voltage and the resistivity, the conductivity type, carrier density, and mobility can be derived. With an applied magnetic field, the Hall voltage is measured using the I-V measurement configurations in Fig. 3.4. With a positive magnetic field, B, applied perpendicular to the sample, apply a current between terminals 3 and 1 (I31pBp) and measure the voltage drop (V24pBp) between terminals 2 and 4. Reverse the current (I31nBp) and measure the voltage drop (V24nBp) again. This current reversal method is done to correct for offset voltage. Next, apply current from terminal 2 to terminal 4 (I24pBp), and measure the voltage drop (V13pBp) between terminals 1 and 3. Reverse the current (I24nBp), and measure the voltage drop (V13nBp) again. Reverse the magnetic

field, Bn, and repeat the procedure again measuring the voltage drops V24pBn, V24nBn, V13pBn, and V13nBn. From the eight Hall voltage measurements, the average Hall coefficient can be calculated as follows:

$$R_{HC} = \frac{t_s}{4BI}(V24pBp - V24nBp + V24nBn - V24pBn)$$

$$R_{HD} = \frac{t_s}{4BI}(V13pBp - V13nBp + V13nBn - V13pBn)$$

where:

R_{HC} and R_{HD} are Hall coefficients (cm^3/C),

t_s is the sample thickness (cm),

B is the magnetic flux density in Tesla ($V*s/m^2$),

I is the current (A),

V represents the voltages (V).

Using the hall coefficients, average hall mobility can be determined using equation:

$$\mu Hall = \frac{|R_{HC} + R_{HD}|}{2\rho_{avg}}$$

Multiple Hall effect measurements on phosphorus doped diamond sample were done at room temperature using Ecopia HMS5000 system. Each corner of the diamond sample was attached to the gold leaf on the mounting board as shown in Fig. 3.5. During all the measurement a constant injection current of magnitude 1μA was used and generated voltages were recorded. Further with the application of 0.55T strength of magnetic field and same injection current, Hall voltages were recorded.

Figure 3.5 Hall Effect Measurement Board. The Contacts Were Placed onto 4 Corners of the Samples and Voltages were Recorded After Injecting Current into the Terminals.

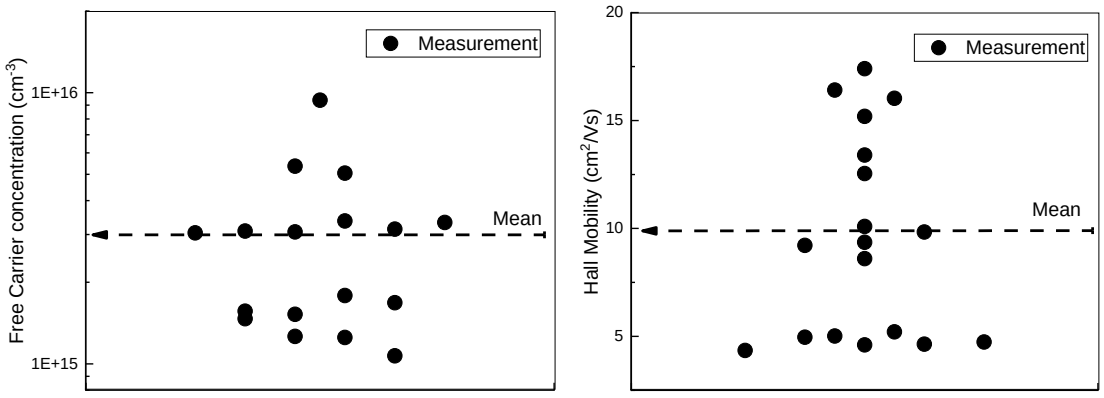

Figure 3.6 Left: Free Electron Hall Concentration from Repeated Measurements, Right: Hall Mobility from Repeated Measurements

The free electron concentration and carrier mobility were extracted from the measured voltages. As can be seen from the figures there is considerable variation in the measured values of the free electron concentration and mobility which we attribute to non-uniform current flow in the doped diamond epilayers. Each time the mechanical contacts were placed down to contact the diamond surface they would be located in different positions on the surface with differing magnetoresistance characteristics, R_{xy}, for a fixed magnetic field, B=0.55T. For this reason, multiple measurements were taken to determine the mean

values and variance in the data. The average free electron concentration across all measurements is ~$3x10^{15}$ cm^{-3} suggesting a dopant activation efficiency of 0.002%. The corresponding average free electron mobility is ~10 $cm^2V^{-1}s^{-1}$. The sheet resistance determined from the Hall effect measurements varies in the range 190 – 380 kΩ/square. Assuming a uniform electron concentration across the 6.5 μm thick epi-layer the corresponding resistivity is 124 – 247 Ω cm.

3.3 Contact Resistance Reduction by Annealing

The obtained sample was first cleaned using acid piranha, then HF dip and finally boiled in nitric acid and sulfuric acid mixture heated to about 150˚C solution temperature. After cleaning, the sample was directly spin coated with AZ3312 photoresist and rectangular TLM pad shapes of dimension 100µm×50µm with varying spacing from 5µm to 35µm was patterned using an OAI 808 aligner. After developing the TLM pads, the surface of the sample was exposed to oxygen plasma prior to metal deposition. The de-scumming property of oxygen plasma leads to good adhesion between metal and diamond surface which in turn helps to make a contact that remains stable after high temperature annealing. Finally a metal stack of titanium/platinum/gold of thickness 50nm/50nm/300nm were deposited onto the sample using an e-beam evaporator followed by a lift-off process leaving us with the desired metal stack as shown in Fig. 4. Electrical characterization of the sample was done using DC probe station and semiconductor parameter analyzer HP4156 and IV characteristics were recorded.

The initial IV measurement for this case is shown in Fig. 3.7. The IV data from the unannealed sample clearly shows the barrier at the interface. This is attributed to fact that

deposited titanium (Ti) is in unreacted state with oxygen terminated diamond and has significant barrier height inhibiting the current flow.

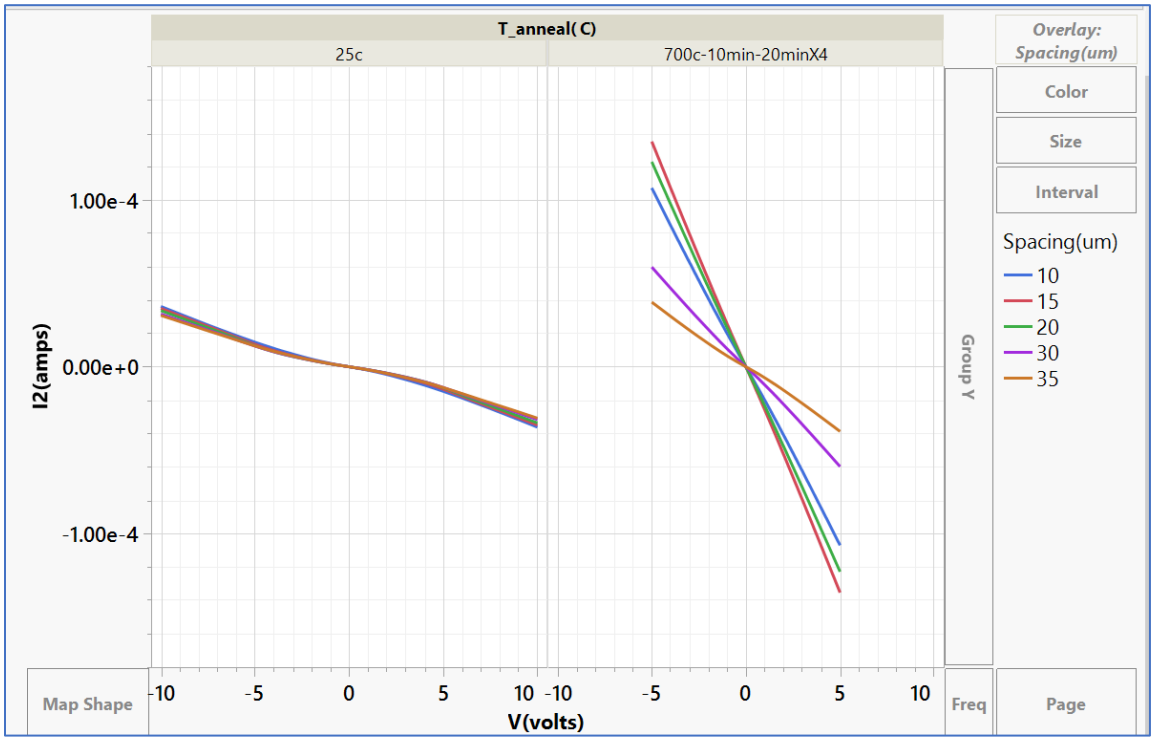

Figure 3.7 Measured IV Data from TLM. The Graph on the Left Represents Measurement Data on Unannealed Sample While the Right One Comes from Annealed Sample (700c for about 80mins).

Next we progressively annealed the sample from 400°C to 700°C in forming gas mixture and extracted the total resistance between each pad that is shown in Fig. 3.8 (left). It is evident that until 600°C there is a very slight change in the contact property. However, as we start annealing the sample after 700°C, the carbide formation starts to happen at the interface between Ti and diamond surface. The intermediate annealing at 700°C shows the sign of non-uniformity in the carbide formation between the interface until we annealed the sample for almost 80min and the variability of resistance between the pads reduces drastically and it becomes almost linear.

The transfer length method (TLM) is a commonly used approach to extract the specific contact resistance to a semiconductor material from measurements of the resistance between rectangular pads with varying spacing [3.19]. The total resistance between any two adjacent pads is given by:

$$R_T = R_s + 2R_c$$

where R_s is the resistance of the semiconductor material between the contacts and R_c is the resistance associated with metal/semiconductor contacts themselves. With the traditional TLM approach a plot of R_T vs TLM pad spacings, *d*, is used to extract the sheet resistance of the semiconductor, the contact resistance, and the transfer length, L_T, from the slope of the fit, and the y- and x-axis intercepts, respectively. Fits to the linear I-V curves measured between adjacent pads were used to develop the TLM plot. The data plotted in Fig. 3.8 (right) shows the corresponding specific contact resistance extracted from the line of best fit after each annealing runs. The graph suggests initially the room temperature ρ_c ~18 $\Omega \cdot cm^2$. With properly adjusted annealing time at 700°C we can achieve a better contact with ρ_c ~7×10^{-3} $\Omega \cdot cm^2$.

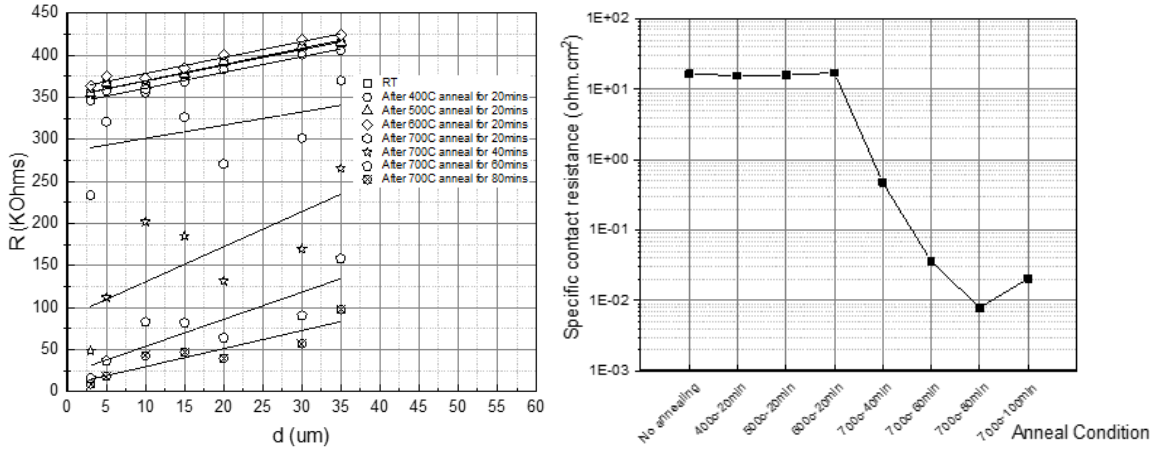

Figure 3.8 Left: Plot of Resistance Vs Spacing From Different Annealing Experiments, Right: Extracted Specific Contact Resistance

3.4 Contact Resistance Reduction by Nano Carbon

Ultra-nanocrystalline diamond (UNCD or simply nano-C) is an extremely fine-grained diamond film with most of the carbon atoms present in sp^3 hybridized state [3.13]. UNCD can be deposited by microwave PECVD technique and has many interesting properties. UNCD films can be doped with nitrogen to produce highly conductive n-type diamond [3.14], which is fully active at room temperature and demonstrates reasonable mobilities. To demonstrate this fact, we fabricated Ti/Pt/Au metal stack TLM onto heavily nitrogen doped nano-carbon layer as depicted in Fig. 3.9 (left).

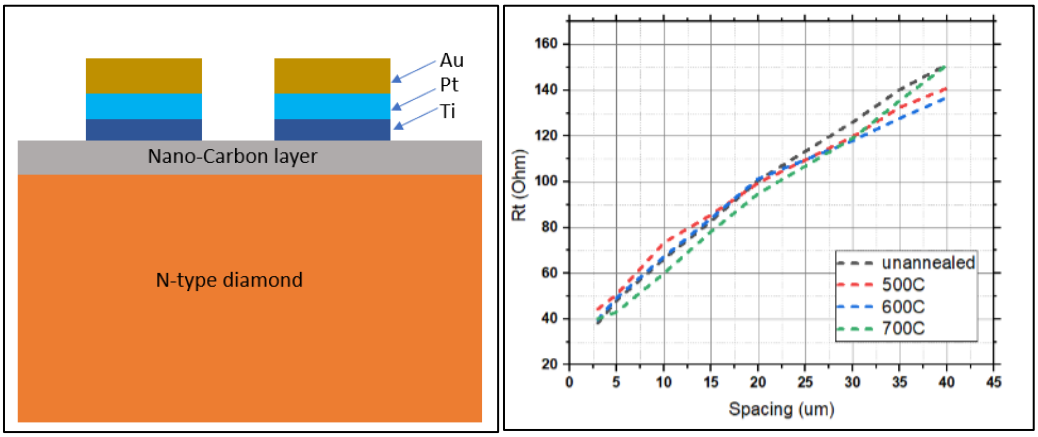

Figure 3.9 Left: Schematic Showing the Contact Made onto nanoC Layer, Right: Resistance vs Spacing Plot After Different Annealing Conditions. (Graph from [3.20])

TLM measurements were done at room temperature and the total resistance vs. spacing graph were plotted as shown in Fig. 3.9 (right). From the graph, we extracted $\rho_c \sim 9.8\times 10^{-5}\ \Omega\cdot cm^2$ and $R_s \sim 300\ \Omega/\square$ confirming a highly conductive layer. Further annealing the contacts to high temperature has little or no impact.

Upon depositing a thin layer of UNCD onto n-type diamond, the electronic states essentially get altered as shown in Fig. 3.10. Depositing directly metal onto the diamond surface results in finite Schottky barrier(SB) height because of the work function

difference. UNCD mitigates this issue by introducing a high density of states in the forbidden zone resulting mainly from distortions in bond geometries and the hybridization states of nitrogen with carbon atoms in the grain boundaries [3.15,3.16].

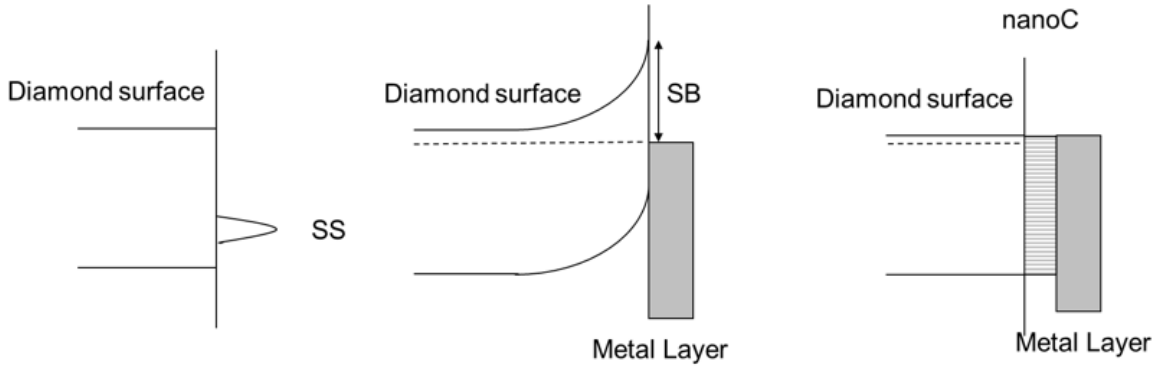

Figure 3.10 Introduction of nanoC Between Metal and Diamond Introduces Lots of States in Forbidden Gap that Facilitates Carrier Transport Across the Barrier.

Using the above remarkable bonding property of UNCD and its high conductivity, we experimentally measured the contact property of the stack shown in Fig.3.11. In contrast to Fig.3.9, additionally a reactive ion etch process using CF_4 and O_2 gas at a flow rate of 5:20 sccm under 10mT chamber pressure and 350W microwave power for about 3 minutes was used for the etch step. This essentially creates a Ti/Pt/Au contact to diamond surface via UNCD layer sandwiched in between them.

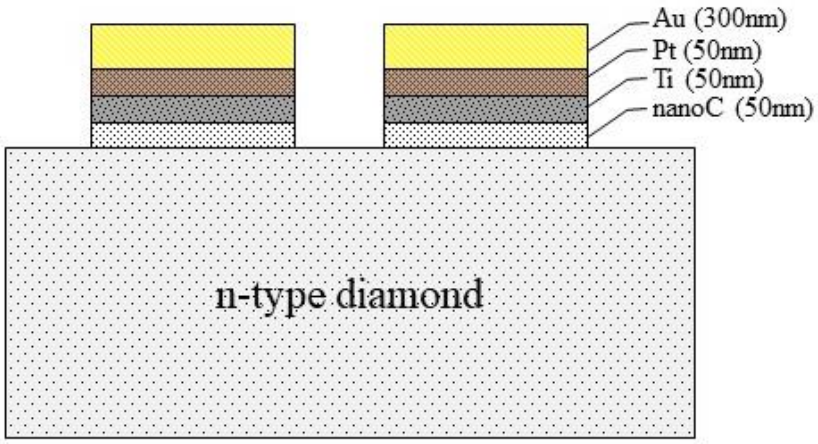

Figure 3.11 TLM Stack for Measuring Contact Resistance of Metal onto Diamond via nanoC Layer.

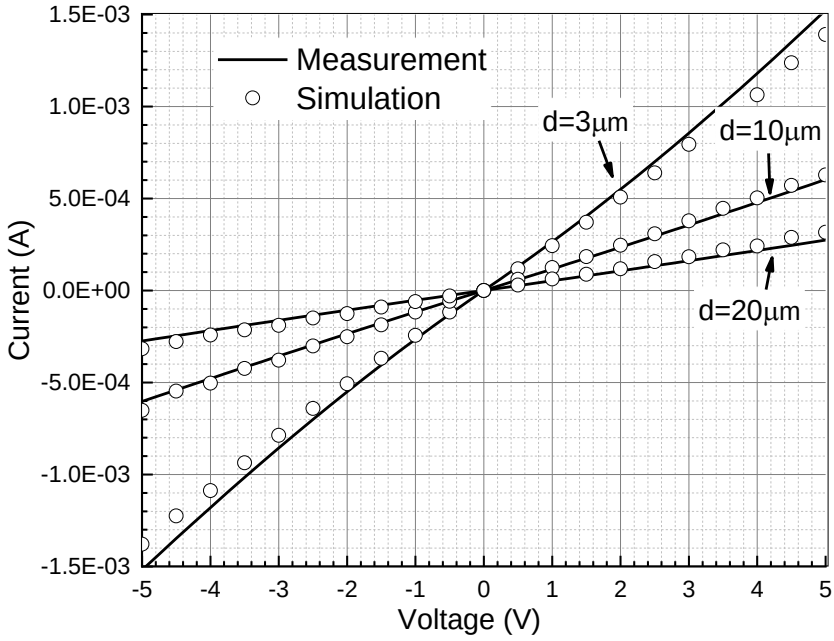

Figure 3.12 Measured IV Data for Few Spacings of Ti/Pt/Au/nanoC Stack.

The room temperature current-voltage (I-V) characteristics measured between pairs of contacts are shown in Fig. 3.12. It is evident that even with no high temperature annealing of the contacts the I-V curves are highly linear. Progressive annealing of the contacts up to 700° C had negligible impact on the I-V curves. From the IV curves we extracted the resistance vs. spacing as plotted in Fig. 3.13.

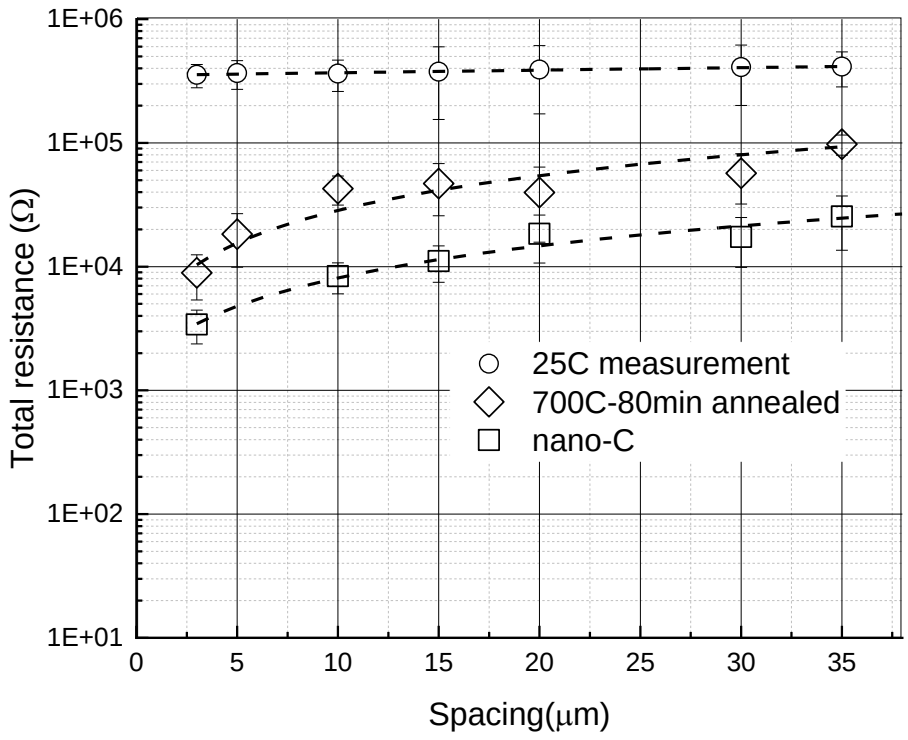

Figure 3.13 Specific Contact Resistance from Three Different Experiment Shows Significant Improvements and Reduction in ρ_c when nanoc is Used.

The TLM analysis described above assumes that the current flow is confined to a width, Z, defined, for example, by a mesa etch to restrict the current to parallel flow lines between the metal pads. However, for the diamond sample used here the 6.5 μm thick phosphorus doped layer was too thick to conveniently etch and instead the current was injected into the diamond film with no mesa isolation. As a result, additional current can flow along the fringing fields between the metal contacts, increasing the effective width of the metal contacts.

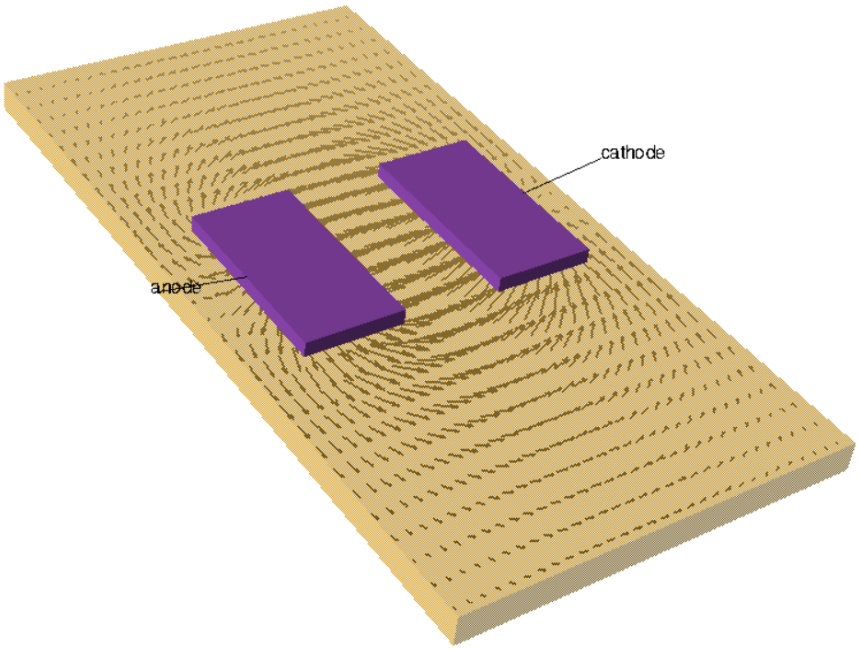

Figure 3.14 TCAD Simulation of TLM to Estimate the Fringe Current.

From the fit to the as-measured TLM plot (in Fig. 3.13) we determine a gradient of 700 Ω/μm, a contact resistance of 600 Ω, and a transfer length of 0.86 μm. Using the contact width as the value for Z = 100 μm, we obtain a sheet resistance of 70 kΩ/square and a specific contact resistance of 5.2×10^{-4} $\Omega.cm^2$. The measured sheet resistance is nearly three times smaller than the lowest value in the range determined from the Hall effect measurements. We attribute this discrepancy to the fringing currents present in this sample without mesa etch isolation, leading to a higher effective width than 100 μm, and a corresponding under-estimate of the sheet resistance. To correct the fringing currents, we used the correction factor by simulating the TLM structure in TCAD framework described previously in section 2.7. The current flow vectors shown in Fig. 3.14 show the detailed distribution of current between and outside of the contacts. The fringe current was estimated by integrating the current density vector that flows outside of the contacts. By subtracting this from the measured data we can calculate the resistance between a pair of

contacts that would have been measured if a mesa isolation etch had been used to confine the current. A fit to the corrected TLM data, shown in Fig. 3.15 as the solid symbols, gives a sheet resistance of 120 kΩ/square and a specific contact resistance of 2.1×10^{-4} Ω.cm^2.

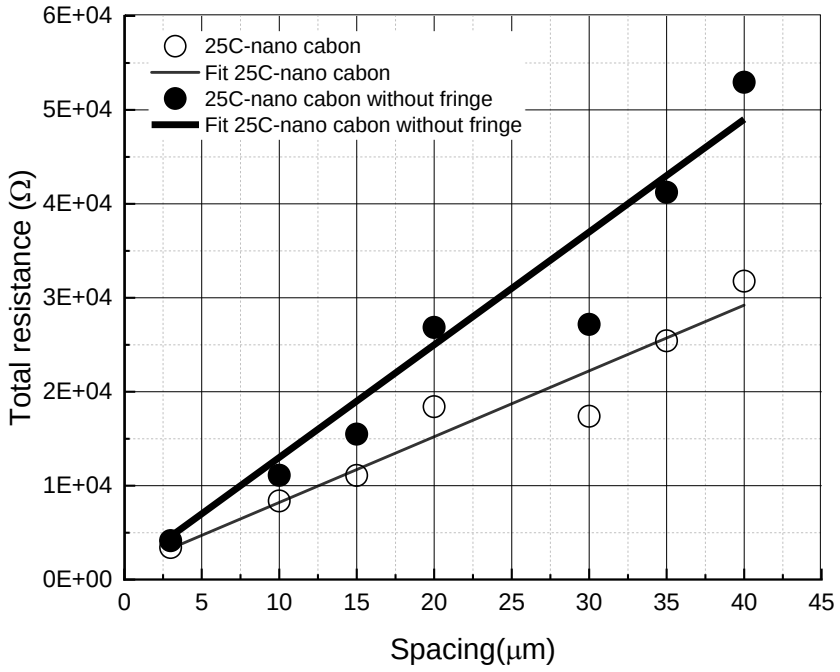

Figure 3.15 TLM Data Correction by Removing the Fringe Current from Measurement.

CHAPTER 4.

CIRCUIT APPLICATIONS

4.1 Introduction

A typical receiver used in RADAR systems is designed to sense very small signal amplitude. The sensing circuitry often contains fragile semiconductor blocks which are very sensitive to electrical signals (can typically resolve ~μV). However, these systems must also be capable of handling huge signal incidents on them. To make the receivers robust enough to handle large signal powers, receiver protection limiters are the ultimate choice. The receiver protection limiter, most often referred to simply as a limiter, can protect the receiver from large input signals and also allow the receiver to function normally when these large signals are not present [4.1].

Modern transceivers, whose transmitter and receiver blocks are tuned to the same frequency, usually have limiter protection circuitry in them. The necessity of limiters can be best understood from the block level diagram shown in Fig. 4.1.

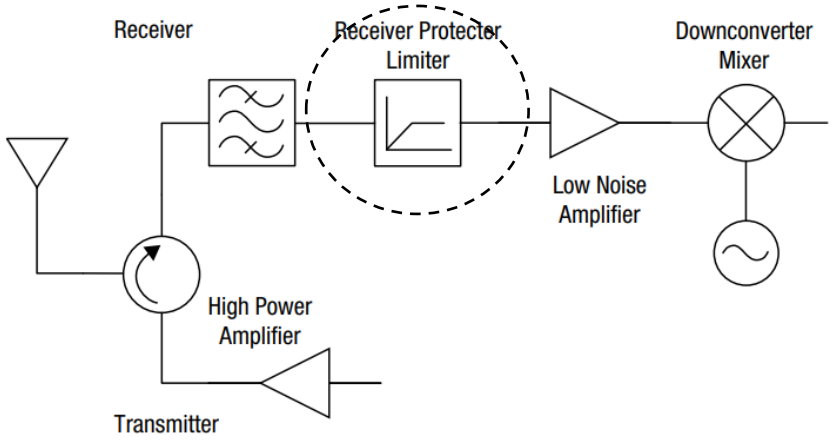

Figure 4.1 :An Overview of a Typical RADAR Transceiver with Limiter [4.1].

The architecture shown above has transmitter and receiver blocks sharing a common antenna. When operated in transmit mode, the antenna usually sends out a very strong signal (order of ~100 Watts to kWatts). On the other hand, the receiver circuit components are designed to handle very low signal levels being sensed by the antenna. The received signal is first processed by a low noise amplifier (LNA) where the signal first hits the gates of transistors. In the case of very high input power (when a small portion of transmit power that gets coupled to receiver) to the LNA, the transistor gates may get damaged and lead to permanent circuit failure. To prevent such a scenario, limiters are often employed which can protect the following sensitive circuits in the receiver chain.

Diamond P-I-N diodes are ideal for limiter circuit applications because of their low on resistance and extreme power handling capacity. The maximum power-handling capability of a limiter circuit is principally determined by the sizes of P-I-N diodes chosen for the design. A large diameter P-I-N diode is able to conduct more current than a smaller diameter diode and is therefore able to survive higher RF drive levels. However, the larger the diode size, the more shunt capacitance in the circuit and the less available bandwidth. The secret to optimum limiter design is selection of diode sizes to meet power handling capability without greatly exceeding this requirement. By choosing the correct diode size for the intended application, excess shunt capacitance will not be added, and insertion loss will be minimized.

A frequency mixer is a 3-port electronic circuit. Two of the ports are “input” ports and the other port is an “output” port [4.2] . The ideal mixer “mixes” the two input signals such that the output signal frequency is either the sum (or difference) frequency of the inputs. In other words:

$$f_{out} = f_{in1} \pm f_{in2}$$

In principle, any nonlinear device can be used to make a mixer circuit. As it happens, only a few nonlinear devices make “good” mixers. The devices of choice for modern mixer designers are Schottky diodes, GaAs FETs and CMOS transistors. The choice depends on the application. FET and CMOS mixers are typically used in higher volume applications where cost is the main driver and performance is less important. For the more challenging, high-performance applications, Schottky diode mixers are used almost exclusively. [4.3]

4.2 Receiver Protector

A limiter controls maximum instantaneous voltage or current, never allowing it to exceed a certain value. Wide ranges of input voltage or current to this device produce output voltage or current varying over only a specified range. So, the primary objective of having a limiter is to have amplitude limitation (current or voltage).

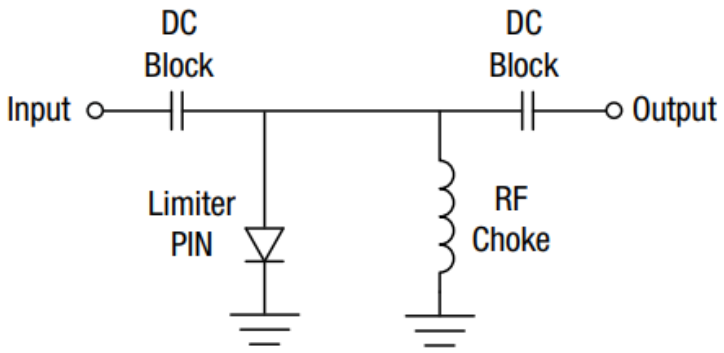

Figure 4.2: A Single Stage Limiter [4.1].

One of the simplest forms of limiter is shown in Fig. 4.2. The circuit comprises of a P-I-N diode and an RF choke in shunt to the main signal line. The limiter diode can be thought of as an incident power controlled variable resistor. So, when the input signal is very weak, the diode presents its maximum impedance resulting in least insertion loss. If the input signal temporarily becomes huge, the diode is forced to move into a low impedance state producing an impedance mismatch at the line input. In this case the electric field of the signal temporarily forces positive charge carriers (holes) from the diode P layer and negative charge carriers (electrons) from the diode N layer into the nominally undoped, high impedance I layer, causing the impedance of the diode to be temporarily reduced to a much lower value. This causes the majority of the incident signal to get reflected back to the source. An output characteristic of interest for this kind of limiter is shown in Fig. 4.3 where output power is plotted with respect to varying input power on logarithmic scale.

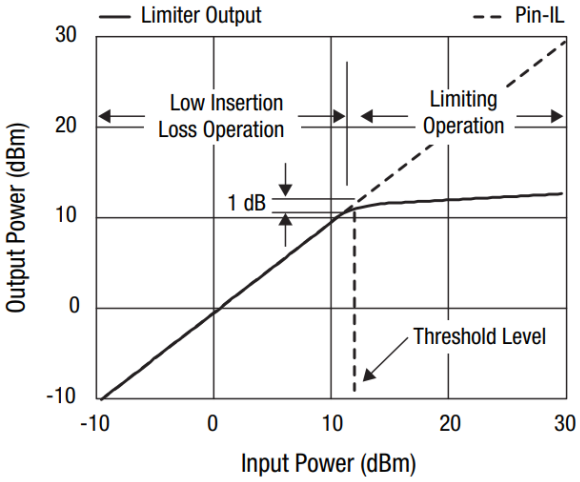

Figure 4.3: Transfer Characteristics of a Limiter [4.1].

When the large input signal is no longer present, the impedance of the diode reverts from a very low value to its maximum value after a brief delay. It is important to note that when a large input signal is present, the limiter diode reflects the majority of the power, but some

power gets dissipated in the diode itself. The main advantage of using diamond-based P-I-N diode is that one can go to very high input power level and the operation of limiter still remains intact as the diamond substrate can easily handle high input power levels.

It is to be noted that the minimum and maximum impedances of the limiter P-I-N diode are determined by the geometry of the diode as well as the resistivity of the diode's I layer. In the simplest approximation, the P-I-N diode can be modeled as a right cylindrical section with three separate layers: The P layer, the I layer and the N layer, where the resistance of each layer is given by:

$$R_{layer} = \frac{Resistivity_{layer} \times Thickness_{layer}}{Area_{layer}} \qquad (4.1)$$

To simulate and evaluate the performance of limiter circuits in ADS, an instance of diamond-based P-I-N diode is created as shown in Fig. 4.4 whose optimized SPICE model predicts the AC and DC behavior of the diode.

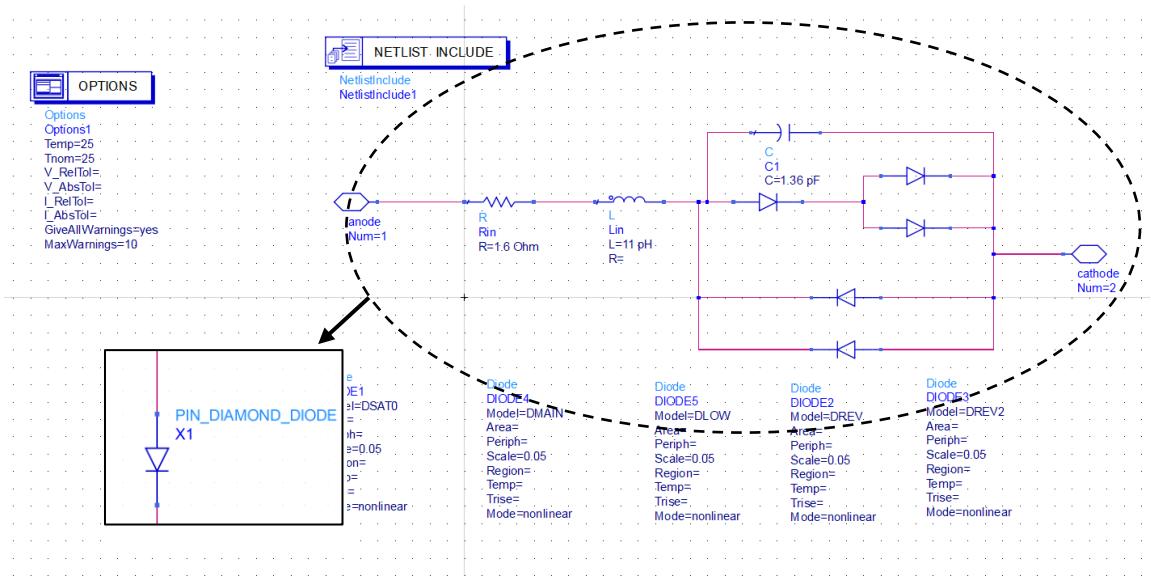

Figure 4.4: Diamond P-I-N Diode Instance Defined in ADS.

A two-stage limiter can be designed to maximize limiting, power-handling capability, and bandwidth [4.4]. Fig. 4.5 shows the schematic for a two-stage limiter. In this topology, at small signal drive levels the diodes and transmission lines form a low-pass filter structure. The transmission line length and impedance are used as series inductance with the diodes providing shunt capacitance.

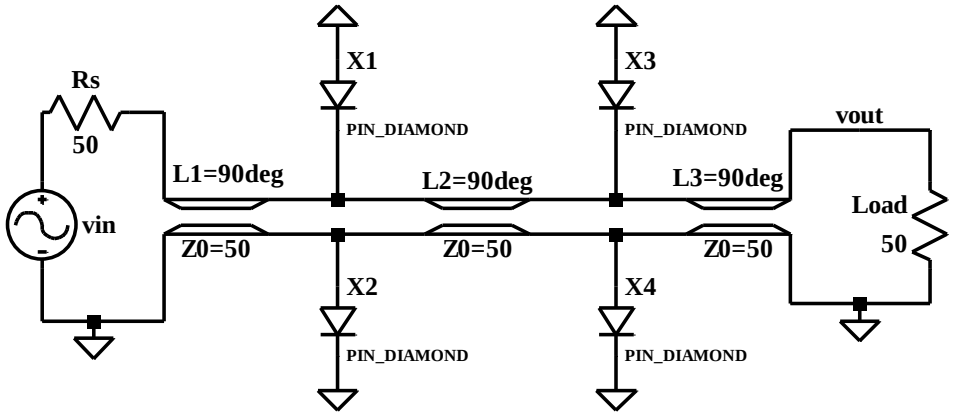

Figure 4.5: Two Stage Limiter Setup with λ/4 Transmission Line.

To evaluate the performance of a diamond-based receiver protector the sub-circuit of Fig. 4.4 is used to simulate the power transfer characteristics of the circuit in Fig. 4.5 operating at 1 GHz. The power delivered to a 50Ω load as a function of input power is plotted in Fig. 4.6 along with the total power dissipated in the receiver protector circuit. At input powers above 100 mW the output power starts to be attenuated. For P_{in}=100 W the power delivered to the load is 0.51 W, with 29 W dissipated in the diodes of the receiver protector and the rest being reflected at the input.

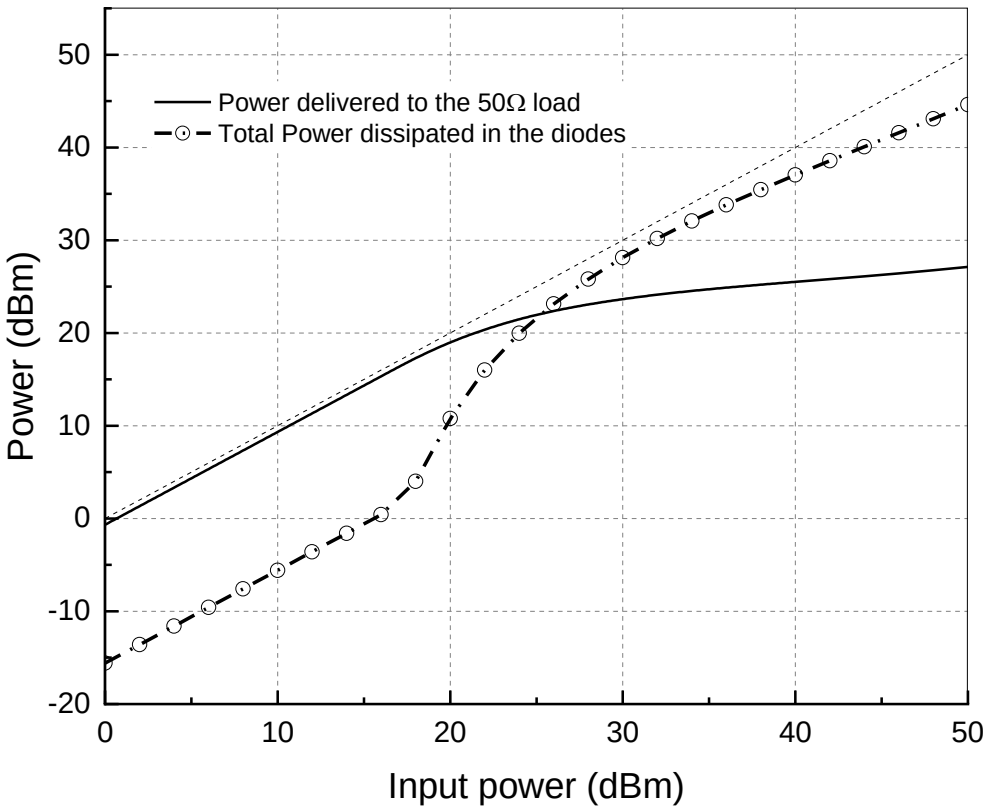

Figure 4.6: Simulated Power Attenuation of the Two-stage Diamond P-I-N Diode Limiter Circuit.

The power dissipated in the diodes of the receiver protector leads to Joule heating, and the resulting increase in temperature will ultimately limit the operation of the receiver protector. It is for these high-power applications that diamond substrates, with their high thermal conductivity, will provide important systems level benefits. To compare the increase in temperature for different substrate materials we use the 1D thermal transport equation :

$$\Phi = \kappa A \frac{dT}{dz} \tag{4.2}$$

Where Φ is the heat flux, κ is the thermal conductivity of the substrate and dT/dz is the temperature gradient in the direction z, normal to the substrate.

Reference	Material System	Thermal Conductivity at 300 K (W·cm-1·K-1)	Frequency (GHz)	Insertion Loss (dB)	Pin for 3dB attenuation in Pout (dBm)	Power Density for ∇T=100°C (dBm/mm^2)
[4.9]	Silicon	1.5 [4.14]	3	< 1	~ 20	47
[4.10]	GaAs	0.46 [4.13]	10	1.5	~ 20	42
[1.21]	GaAs	0.46 [4.13]	10	0.74	~ 18	42
[4.15]	GaAs	0.46 [4.13]	9.5	< 1	~ 18	42
[4.11]	4H-SiC	2.8 [4.13]	2 – 7	1.1 – 2.6	Not reported	50
This work	Diamond	> 20 [4.12]	1	0.3	~ 25	58

Table 4.1: Comparison of Diode Limiter Circuits for Different Semiconductor Materials.

The diodes in the first stage of the attenuator experience the largest RF voltage swing, and therefore the highest power dissipation. The power density dissipated in a single diode for a temperature drop of 100°C across a substrate of thickness 300 μm is estimated using eq. (4.2) with the room temperature thermal conductivities appropriate for silicon, GaAs, SiC and diamond. The values are included in Table 4.1 along with other key materials parameters for receiver protectors made from these materials. At elevated temperatures the thermal conductivity of the substrates decreases with increasing temperature [4.5-4.8] making it harder to dissipate the heat generated in the diodes. As a result, the power densities in Table 4.1 are an overestimate, and the devices would experience a temperature increase greater than 100°C. Nonetheless, the data in Table 4.1 confirms that compared to

other semiconductor material systems diamond-based P-I-N diodes are ideally suited for high power RF receiver protector applications.

4.3 High Power Signal Mixing

There are many ways to build a mixer. The simplest mixer consists of a single diode as shown in Fig. 4.7. A large signal local oscillator (LO) and a small signal RF combine at the anode of the diode. For an "ideal" single diode mixer, it is assumed that the LO is significantly stronger than the RF such that only the LO has the ability to affect the transconductance of the diode. We also assume that the diode switches instantaneously. Devices that possess such instantaneous transconductance switching are called ideal commutators and yield the theoretically optimal diode mixer performance.

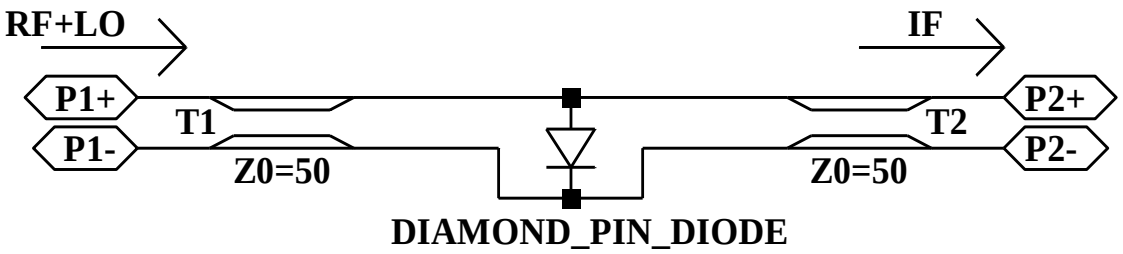

Figure 4.7 Single Ended Unbalance Diode Mixer

Diamond P-I-N diodes can be used for mixing two high frequency signals because of their inherent nonlinearity. A two-tone input comprising a local oscillator (LO) at 1.05 GHz and an RF signal at 0.95 GHz, results in down-conversion to an intermediate frequency (IF) at 100 MHz as shown in Fig. 4.8.

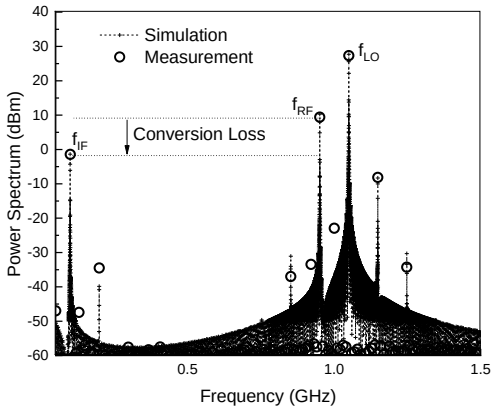

Figure 4.8 Measured and Simulated Output Power Spectrum of the Diode Mixer for an LO Power of +27dBm and RF Power of +9dBm.

The spectrum shows the presence of higher order mixing terms and intermodulation components that are well-reproduced by the model. The sub-circuit model was verified with the two-tone simulations and compared with the measured conversion loss as shown in Fig. 4.9.

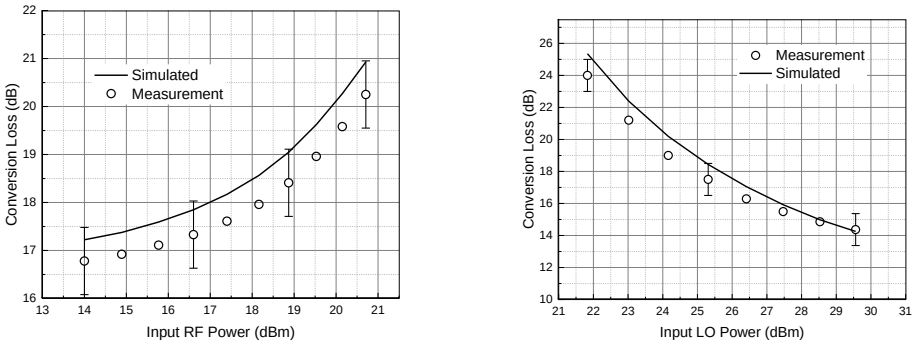

Figure 4.9 Conversion Loss at 100MHz IF, Left: LO Power Fixed at +26 dBm, Right: RF Power Fixed at +14dBm

Another two-tone measurement was used to find the third-order intermodulation intercept point (IIP3) by sweeping amplitude of closely spaced equal-power RF input signals at 1.045 GHz and 1.055 GHz as shown in Fig. 4.10. The extrapolated value for IIP3 was found to be 35 dBm, comparing well to the 31 dBm reported for a balanced SiC Schottky diode high power mixer [10].

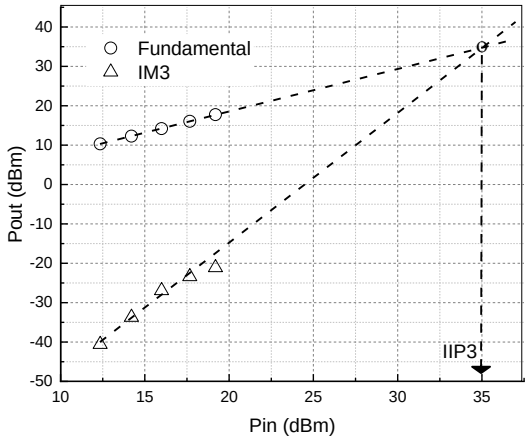

Figure 4.10 Determination of IIP3 Using Two Closely Spaced Two-Tone Input Signals at 1.045 GHz and 1.055 GHz.

To summarize, we demonstrated the design and performance of a two-stage limiter for high-power RF receiver protector applications. The limiter consists of diodes and transmission lines that form a low-pass filter structure at small signal drive levels. The power transfer characteristics of the limiter are simulated using a sub-circuit model. The power dissipated in the diodes of the receiver protector leads to Joule heating, and the resulting increase in temperature ultimately limits the operation of the receiver protector. Diamond substrates, with their high thermal conductivity, are shown to provide important systems level benefits for high-power applications. We also demonstrated the construction and performance of a simple mixer that uses a single diode. The diode is used to combine a large signal local oscillator (LO) and a small signal radio frequency (RF) at the anode. The down-conversion of a two-tone input signal and the presence of higher order mixing terms and intermodulation components are obtained by inherent non-linearity of the diode. The proposed sub-circuit model was verified with two-tone simulations and compared to the measured conversion loss.

CHAPTER 5.

DIAMOND-BORON NITRIDE HETEROSTRUCTURES

5.1 Introduction

In recent years, the development of diamond-based transistors is gaining popularity. Most of the successfully demonstrated transistors on diamond rely on hydrogen terminated surface which results in a 2D hole gas (2DHG) with a reasonable sheet carrier density. The mobility of these devices is usually limited because of surface impurities and roughness scattering processes [5.1]. The electrical properties of these devices are also not stable under high temperature conditions. Bulk conducting transistors seems to be better choices over H-terminated transistors that mitigate the above-mentioned problems. Transistors made from ultra-wide bandgap materials such as diamond and cubic boron nitride (c-BN) are expected to be an ideal candidate for high power applications in future. As shown in Figure 1.1, both the materials have exceptional thermal conductivity and large bandgap that enables them to dissipate heat effectively while operating at very high voltages.

The two most common polymorphs of boron nitride (BN) have hexagonal (h-BN) and cubic (c-BN) symmetries. As shown in Fig. 5.1, h-BN and c-BN are structurally analogous to graphite and diamond phases of carbon, respectively. It has been reported that h-BN is generally regarded as the most stable BN polymorph at ambient conditions while c-BN does not exist in nature [5.3], and its synthesis in laboratories requires high-temperature and high-pressure conditions, a very similar phenomenon happens with graphite and the diamond form of carbon respectively. Thermodynamically, under normal conditions c-BN is the stable form of boron nitride while transition from c-BN to h-BN might start happening at temperature as high as 1500K.

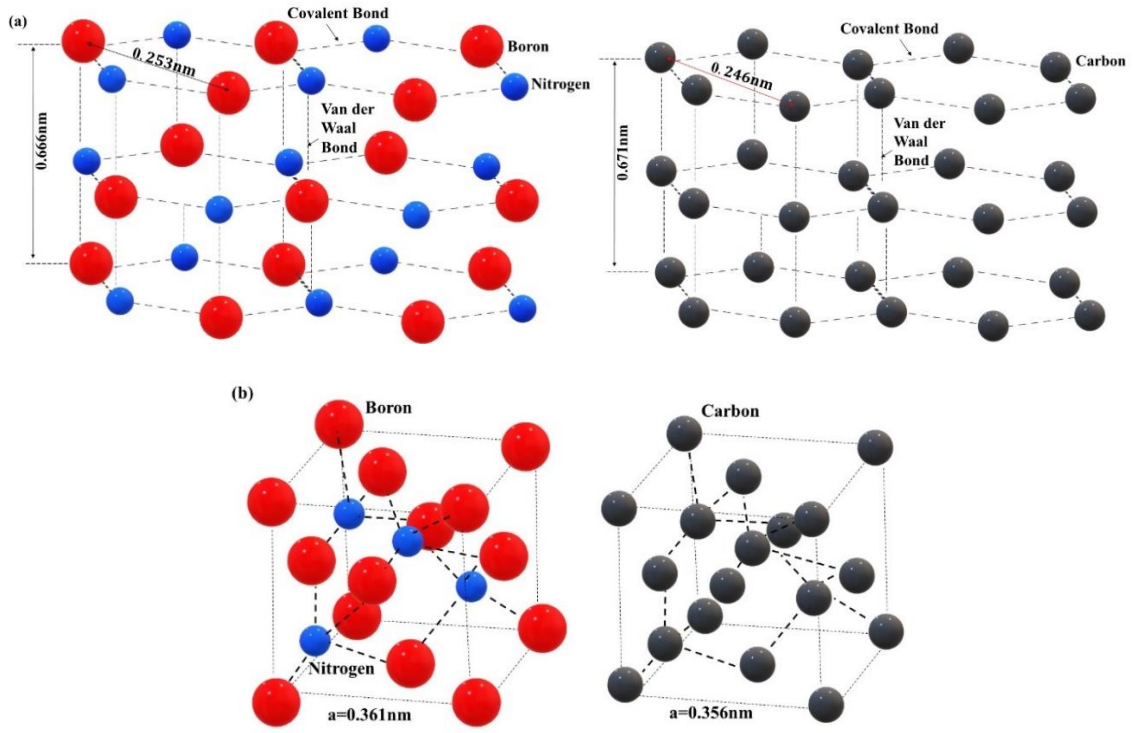

Figure 5.1 Structure Resemblance Between (a) h-BN and Graphite with sp^2 Bonding (b) c-BN and Diamond with sp^3 Bonding. Lattice Parameters Obtained from [5.3,5.4]

Heterostructures made by artificially depositing c-BN, which is structurally very similar to diamond (sp^3 bonded carbon atoms), exhibits a very small lattice mismatch at the interface [5.5]. Structures with high lattice mismatch has mismatching positions of the atoms in the crystal at the boundaries which can cause strain, leading to cracks or dislocations that propagate through the structure. Along with low lattice mismatch, a large thermal conductivity of diamond and c-BN heterostructure, seems promising to dissipate the heat effectively that will be generated from the high-power devices made using these materials.

The large band gap of boron nitride and diamond results in very high critical field (E_{BD}) for these materials. Different techniques have been used in the literature to measure the critical breakdown field of different polymorphs of boron nitride. As shown in Fig. 5.2, the

E_{BD} is different for h-BN and c-BN form and also dependent upon the direction of applied field relative to crystal plane in h-BN.

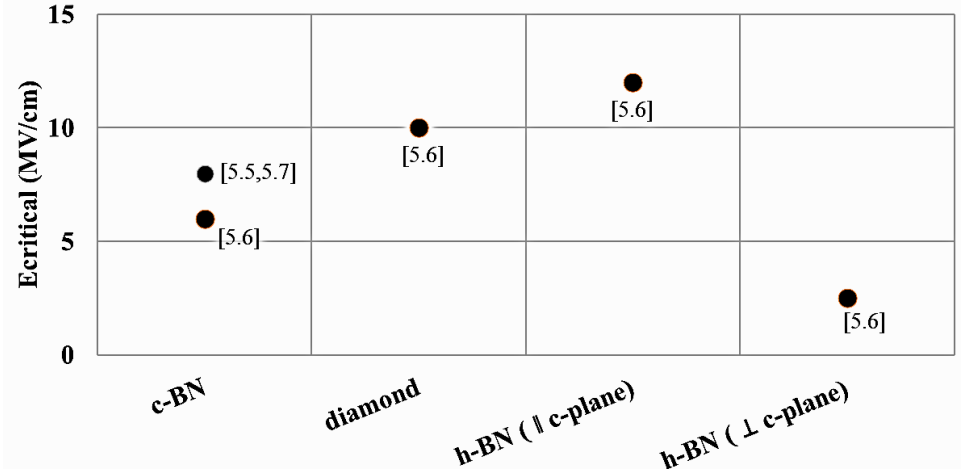

Figure 5.2 E_{BD} for h-BN, c-BN, and Diamond from Literature. The Critical Field for h-BN Depends on the Direction of Field Applied Relative to c-Plane.

The heterostructure consisting of c-BN and diamond is a less explored area and has not yet found the attention it deserves. In this chapter, we studied the electrical characteristics of a capacitor formed using mixed phase h-BN/c-BN dielectric layer deposited on heavily doped p-type polycrystalline diamond substrate. BN films of thickness roughly 200nm and 300nm were deposited via plasma-enhanced chemical vapor deposition (PECVD) on two different polycrystalline diamond samples. The I-V, C-V characteristics of the capacitor are presented, and the breakdown voltage of the dielectric film was deduced from measurements. The chapter serves as a very first step towards making transistors using diamond and c-BN heterostructures.

5.2 Device fabrication

Boron nitride layer of approximate thickness ~200nm and ~300nm were grown on heavily boron doped polycrystalline diamond substrate of dimension approximately 1cm x 1cm. The samples were labeled as AE2218 (~200nm BN) and AE2208 (~300nm BN). The details of the growth process have been outlined in [5.5]. In summary the epitaxial growth of c-BN was achieved using PECVD employing fluorine chemistry. XPS and TEM results indicated that h-BN regions formed at the interface, but c-BN growth dominated after growth of several nanometers. Hence the dielectric film of BN has the mixed phase composition.

The samples were then first cleaned using methanol. After cleaning, a thin layer of lift-off resist and AZ3312 photoresist was spin coated onto the samples.

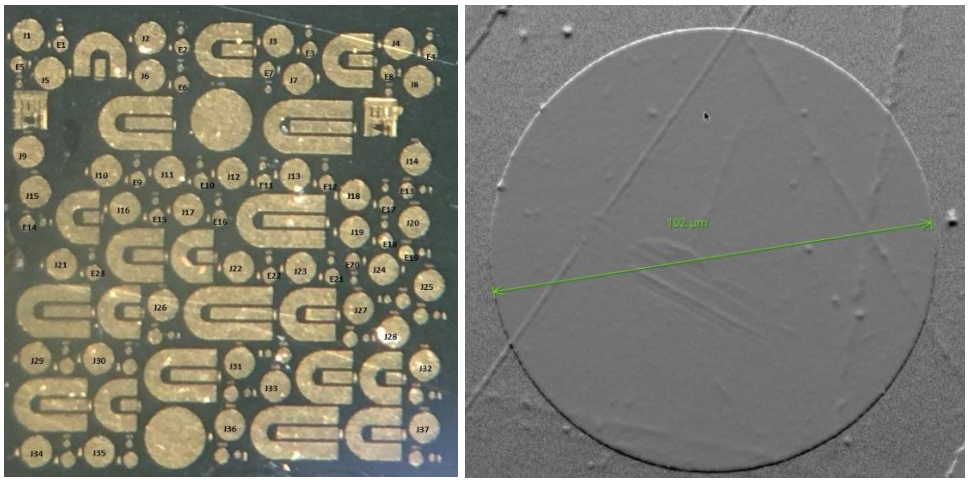

Figure 5.3 Left: An Optical Micrograph of the Sample after Its Full Fabrication. The Image Shows Circular Metal Pads of Different Diameter. Right: Sem Image of One of the Small Pads of Diameter ~100um. The Lines in Background on the Sample in SEM Image Seems to Be the Fault Lines on the Substrate.

Circular pads of diameter 100µm and 180µm were developed using contact-based lithography. Using e-beam metal deposition system, first front and then the back side of

the sample were coated with Ti/Pt/Au metal stack of thickness 50nm/50nm/200nm respectively. Fig. 5.3 shows the optical and scanning electron microscope image of the final pads that we obtained after the lift off process.

5.3 Electrical Characterization

DC characteristics of the circular pads of about 100μm and 180μm in diameter were measured at room temperature using high resolution source monitor units. The bottom side of the sample touching the chuck was grounded and the bias range at the top gate contact was varied during different sweep. Fig. 5.4 shows the measured current density for one of the contacts from AE2218 sample acquired during multiple sweeps. In sweep 1, the range of bias was set to -30V to 30V. The measured IV data shows exponential relationship between the measured current density and applied bias.

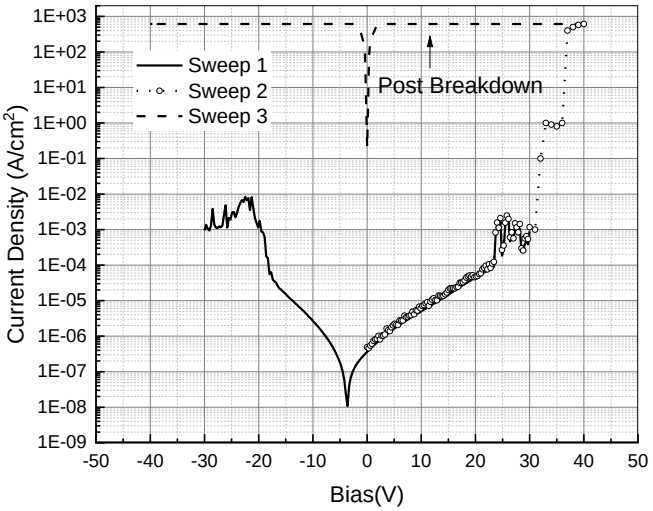

Figure 5.4 Plot of Current Density Vs Applied Bias from as Measured From 100um Circular Pad. Sweep 1 Represents Normal Measurement, Breakdown Happened During Sweep 2 While Sweep 3 Was Done to Confirm That the Breakdown Was Permanent.

During sweep 2, the voltage was ramped up from 0V to 50V to observe the breakdown. It is evident from the plot that the dielectric breakdown occurs when the bias reached

approximately 38V, and the measured current density reaches instrument compliance. Post breakdown measurement in sweep 3 shows the breakdown is permanent. The breakdown characteristics were measured for many other pads on both samples. Prior to the measurement, some of the metal pads on sample AE2208 were covered by depositing ~50nm PECVD SiO_2. This was done to reduce the effect of huge electric field component around the edges of pad thus inhibiting early breakdown.

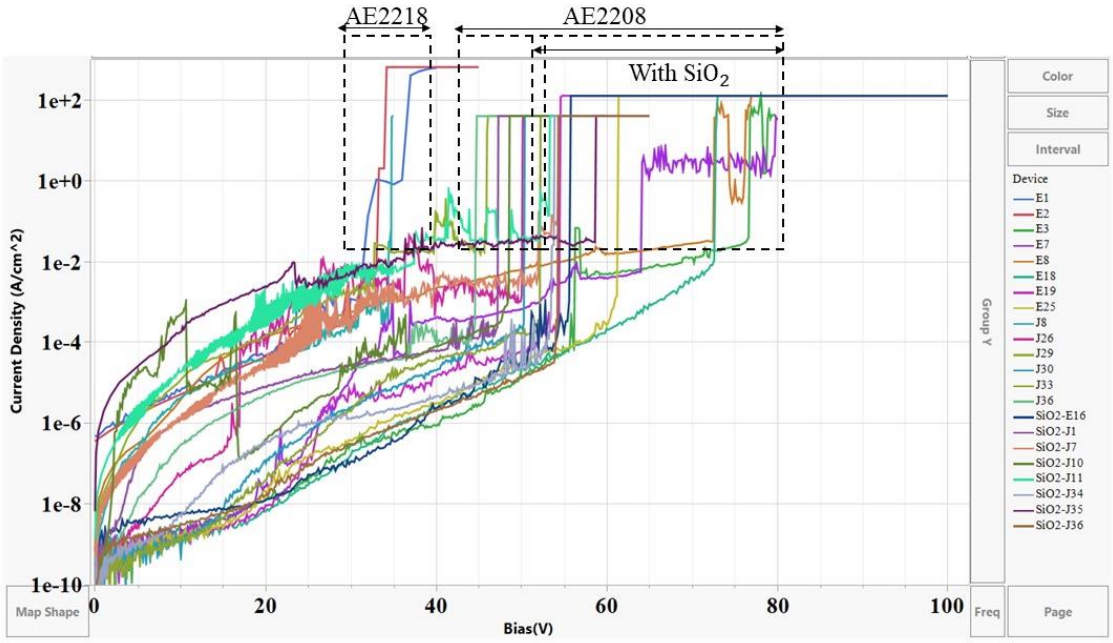

Figure 5.5 Breakdown Measurements from both Samples (AE2218 which has 200nm BN Layer and AE2208 with 300nm BN Layer) are Plotted Together.

The detailed IV breakdown measurements of many pads from these two samples are shown in Fig. 5.5. The measured exponential current (until breakdown) can be best explained by the fact that metal electrons first tunnels into dielectric traps, and then either they can hop from trap to trap within the thick dielectric layer or can tunnel through it until it reaches the dielectric-substrate interface where it recombines with the holes (majority

carrier). To further investigate the leakage mechanism, Fig. 5.6 presents the temperature dependent measurements of current density vs applied bias for some of the 180um diameter pads from sample AE2208. These measurements do not show significant dependence on the temperature.

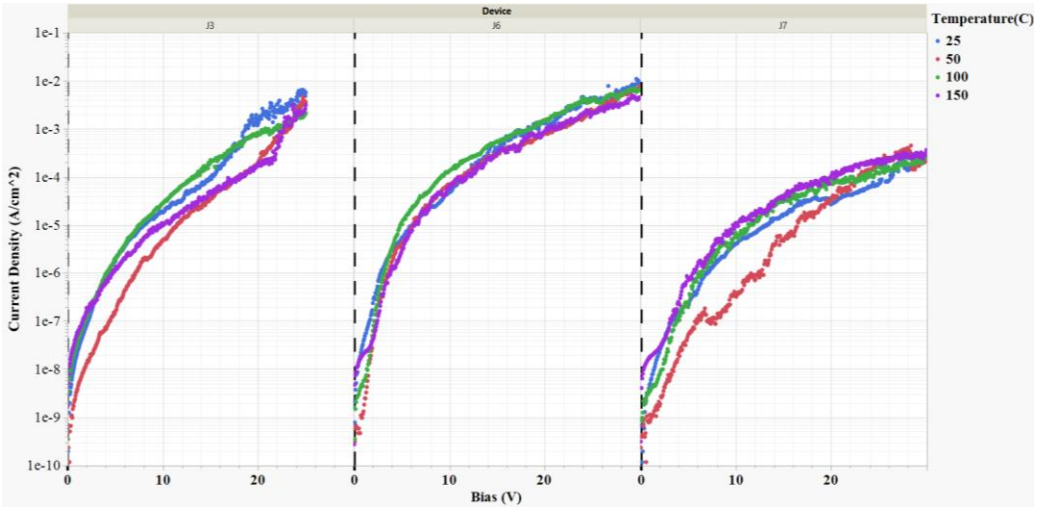

Figure 5.6 Plot of Measured Current Density Vs Applied Bias for Three Different Pads as Temperature Varies from 25C to 150C.

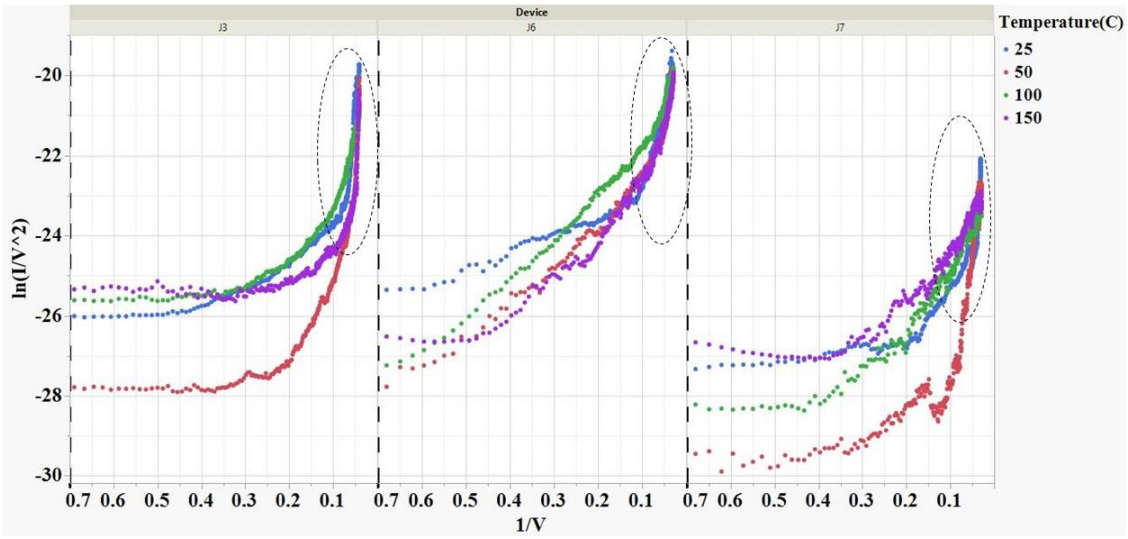

Figure 5.7 Data from Fig. 5.6 for Three Different Pads Plotted as ln (J/V^2) vs $1/V$. At very High Bias(circled region), FN Tunneling Indicated as Dominant Mechanism.

When plotted as ln (J/V^2) vs. $1/V$ in Fig. 5.7, different temperature curves for a given pad appears to become close to each other suggesting Fowler–Nordheim tunneling mechanism [5.8].

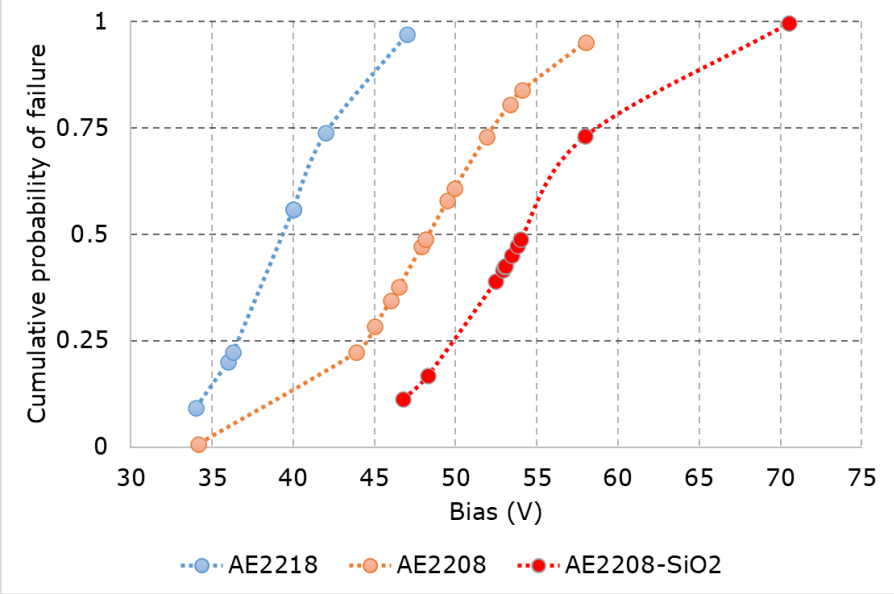

Figure 5.8 Cumulative Distribution of Breakdown Voltages from the Two Samples. The Breakdown Voltage Improves Slightly upon Depositing Silicon Dioxide over Metal Pads.

The sudden jumps in IV measurements at extreme bias as shown in Fig. 5.5 correspond to permanent breakdown of the pads and hence the current density reaching to instrument compliance. Upon extracting breakdown voltages of the pads from different samples, one can create a cumulative distribution plot as shown in Fig. 5.8. It's evident that the mean breakdown voltage from AE2218 sample which has BN layer thickness close to 200nm is about 38V or equivalently the distribution of critical field for the grown film on this sample was found to be in the range [1.7MV/cm, 2.4MV/cm] with mean value of 1.9MV/cm. Similarly, for AA2208 sample with 300nm dielectric layer has mean breakdown voltage of about 48V (when no SiO_2 and have the breakdown distribution in

the range [1.1MV/cm, 1.9MV/cm])and 54V (with SiO_2 layer present on top and has breakdown distribution in the range [1.6MV/cm, 2.4MV/cm]). It can be concluded that the use of silicon dioxide to mitigate the issue of high field around the edges enhance the breakdown field slightly while breakdown phenomenon is majorly controlled from the quality of deposited BN layer. The breakdown field strength obtained from this study is close to 2MV/cm for a mixed phase BN layer and the literature data from Fig. 5.2 suggests it to be as high as 8MV/cm. It is extremely important for the power devices utilizing BN as dielectric material should be able to tolerate very high voltage levels and hence a further investigation of breakdown field strength with better film quality on single crystal diamond is required.

Prior to permanent breakdown, capacitance voltage measurements for different diameter pads were done using an LCR meter. A small signal of amplitude 25mV was superimposed on to the DC bias during high and low frequency capacitance measurement. Fig. 5.9 plots the measured capacitance at different bias for 100μm pad diameter.

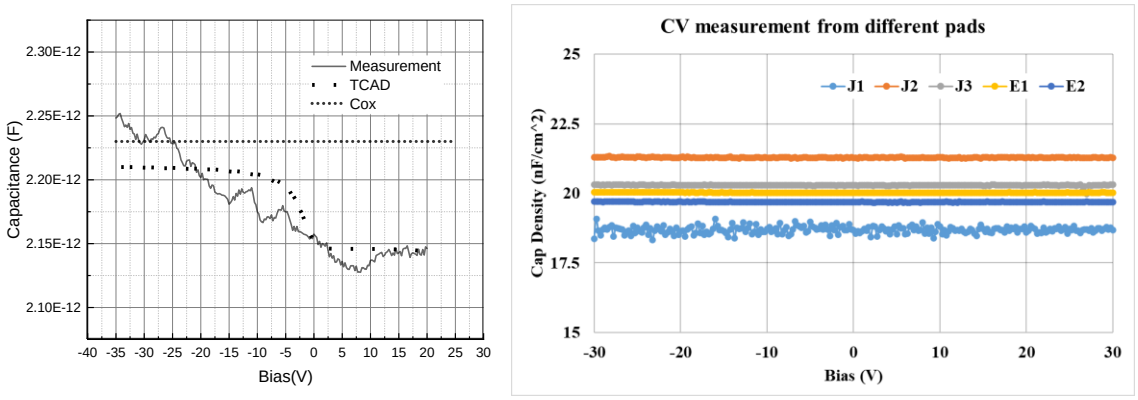

Figure 5.9 Left: CV Measurement Data for a Pad of Diameter 100um from AE2218. Cox Is Calculated Using Parallel Plate Formula, Right: Capacitance Density Plotted from 5 Different Pads of Different Diameters.

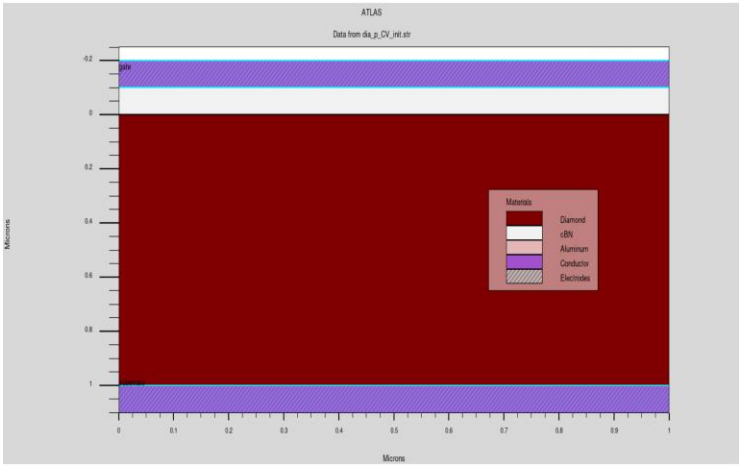

Figure 5.10 TCAD Structure to Simulate the CV Characteristics.

We can see in the accumulation region; the measured capacitance is very close to C_{ox}. As we move towards more positive bias (i.e., into depletion), the observed change in capacitance is minimal. This follows from the fact that the substrate is heavily doped p-type and hence during the positive bias, the depletion width near to the diamond surface is extremely small which in turn does not cause significant change in overall capacitance. The fabricated structure was simulated in Silvaco TCAD software (Fig. 5.10) to calibrate the capacitance as a function of bias. For the heavily doped substrate, the simulation confirms a depletion width of about 5nm resulting in a relatively large depletion capacitance compared to C_{ox}. By comparing the calculated C_{ox}, measured capacitance and simulated CV curve from TCAD, we obtain the relative permittivity of the cubic boron nitride to be 7.1 and dielectric layer thickness of about 210nm which is in good agreement with the grown layer thickness. Fig. 5.9 shows the measured capacitance of several other pads of diameter 100μm and 180μm. It can be seen that the measured capacitance density from different pads is very close each other. The slight variation in capacitance density can be attributed to non-uniformity in the film thickness.

CHAPTER 6.

CONCLUSION AND FUTURE WORK

This thesis first reviewed diamond technology in order to establish the context for the contributions presented in the subsequent chapters. The literature survey in the first chapter clearly showed that the unique combination of high thermal conductivity, high breakdown voltage, wide bandgap, chemical inertness, and high carrier mobility make diamond a highly attractive material for advanced electronic devices, especially for high-power, high-frequency, and high-temperature applications.

In the second chapter, the DC and AC characteristics of diamond Schottky P-I-N diodes have been measured and used to extract a lumped element compact model. The model accurately reproduces the measured insertion and return loss up to 25 GHz. A passive 2-stage diode limiter circuit, simulated at a frequency of 1 GHz, provides receiver input protection up to 50 dBm of input power. At such high input powers significant diode self-heating is expected, increasing the risk of device failure. The high thermal conductivity of the diamond substrates ensures that the self-heating in diamond-based receiver protectors is kept to a minimum compared to other semiconductor device materials such as silicon, GaAs, and SiC.

In chapter 3 of this thesis, we report the electrical characteristics of Ti/Pt/Au metal contacts to thick films of heavily doped n type diamond with a nano-C interfacial layer. The contacts are Ohmic, i.e., highly linear around 0V bias, without the need for a high temperature annealing step. A TCAD model is used to correct the fringing currents. The specific contact resistance was measured to be $2.1 \times 10^{-4}\ \Omega.cm^2$, almost an order of magnitude lower than previous reports. With further optimization, contact stacks of nano

C/Ti/Pt/Au suggest a promising approach for high power DC and RF diamond electronics. The future work that needs to be done in this direction of research is definitely the fabrication and characterization of multistage shunt configuration limiters onto the diamond in integrated form (Fig. 4.5) with low resistance Ohmic contact strategy proposed in this chapter and then its performance correlation with the model predictions (from chapter 2) should be investigated.

In chapter 5 of this thesis, the electrical property of metal insulator semiconductor (MIS) capacitors fabricated on heavily doped polycrystalline diamond. c-BN insulating layer has been deposited on p-type diamond body via plasma-enhanced chemical vapor deposition technique. Contacts on the front and back side were made using Ti/Pt/Au metal stack. The MOS capacitor showed a very small change in capacitance during inversion. Both high and low frequency CV measurements lead to almost the same characteristics revealing negligible minority carrier concentration in the WBG material as confirmed from TCAD simulation. Further the breakdown of the insulating film was found to be around 2MV/cm. The breakdown field showed very little improvement when the contacts were covered with an additional dielectric layer. This shows a negligible dependence of breakdown field on the high electric fields at contact edges. The field strength obtained from the study is lower by 4x factor which could be attributed to the quality of the BN film and the presence of unintentional defects in the polycrystalline diamond sample. Hence further study is required to determine the breakdown field strength of cBN film deposited onto lightly doped single crystal diamond. This will also allow us to measure the signification modulation of capacitance with voltage, critical for MOS applications.

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