Impact of Variations, Measurement Uncertainty, and Surface Roughness on High–Speed Interconnect Validation

by

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ABSTRACT

The rapid growth of emerging technologies is placing enormous demand on the seamless access to the extensive amount of data, which drives an unprecedented need for substantially higher data-transfer rates. As 1.6 Terabit Ethernet (TbE) specifications are being developed, high speed interconnects along with advanced materials and processes play a crucial role in technology enabling. However, validation of interconnect performance becomes increasingly challenging at these higher speeds.

High-speed interconnect behavior can be reliably predicted if interconnect models are successfully validated against measurements. In industry, it is still not common practice to perform validation at actual use conditions. Therefore, there is an urge for a restructured design methodology and metrology based on temperature and humidity, to set realistic specs for high speed interconnects and reduce probability of failure under variations.

Uncertainty quantification and propagation for interconnect validation is critical to assess the correlation quality more objectively, as well as to determine the bottleneck to improve the accuracy, repeatability and reproducibility of all the measurements involved in validation.

The purpose of this work is to create a methodology that is both academically rigorous and has a significant impact on industry. This methodology provides an accurate characterization of the electrical performance of interconnects under realistic use-conditions, accompanied by an uncertainty analysis to improve the assessment of correlation quality. Part of this work contributed to the Packaging Benchmark Suite developed by IEEE EPS technical committee on electrical design, modeling, and simulation.

DEDICATION

I would like to dedicate this dissertation to my children, Halil Emir and Eymen Kemal, and my wife, Meryem Burçin, with love. I am forever grateful for the ways in which you have improved my life beyond my wildest expectations, making me a more resilient, capable, and content person. This work is a tribute to the sacrifices you made, and the patience you showed.

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I would like to express my sincere gratitude to the following individuals and organizations without whose support, this dissertation would not have been possible.

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I am also indebted to the members of my dissertation committee, Zhichao Zhang, Sule Ozev, Lesley Polka, and my previous advisor Umit Ogras, for their insightful comments, thoughtful suggestions, and constructive criticisms. Their feedback helped me refine my research, and their enthusiasm for my work kept me motivated.

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Chapter 1

INTRODUCTION

"There are two kinds of designers, those with signal–integrity problems and those that will have them."
on a white board at a large systems company, as cited in [3]

The rapid growth of emerging technology superpowers such as artificial intelligence, ubiquitous computing, pervasive connectivity, and cloud-to-edge infrastructure has created a pressing need for seamless access to vast amounts of data. This demand is leading to an increased requirement for data rates that can accommodate the massive influx of data. To address this, IEEE and Optical Internetworking Forum (OIF) have already developed the electrical interface specifications for 400 GbE [4, 5] as illustrated in Figure 1.1, and are exploring possibilities 1.6 TbE and beyond [1].

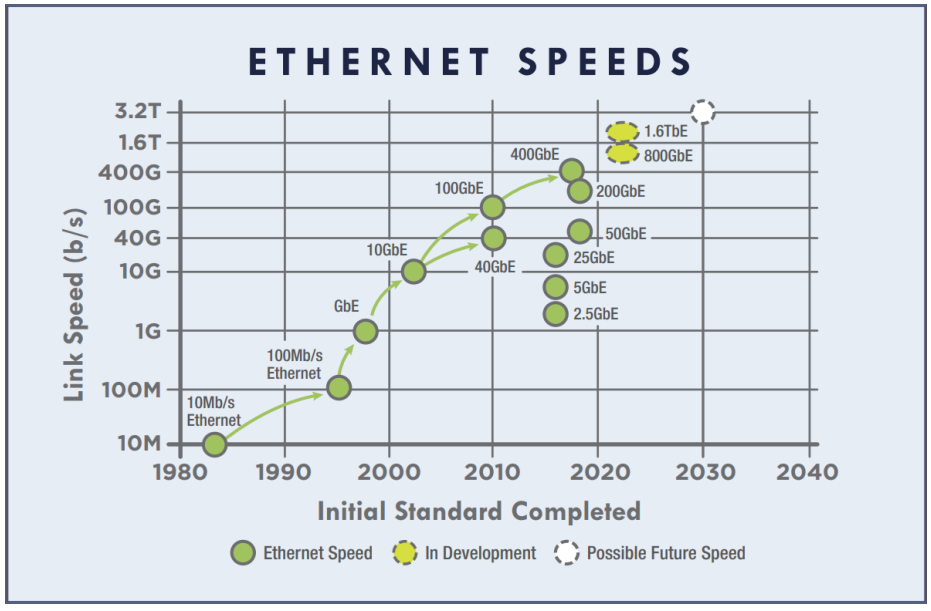

Figure 1.1: Ethernet Roadmap Showing the Evolution of Ethernet Speed over Time. Courtesy of Ethernet Alliance [1].

In the 1980s, for a system with 10 Mb/s data rate, the interconnect–the pathway transmitting the signals from the transceiver to the receiver, was not critical since it was essentially *"transparent to the signal"* and not affecting the system performance [3]. However, supporting a seamless connectivity at 400 GbE in the 2020s requires scalable, reliable, and high–performance interconnects between semiconductor chips. Figure 1.2 shows an example of an end-to-end channel topology which consists of a bi-directional package, a high density board, a cable with two connectors [2]. The link budget is breakdown among the system components, and these components are designed within their respective performance budgets. Basically, designers need to optimize i) signal quality of each net including attenuation, reflections and distortions from impedance discontinues in the signal and return path; ii) crosstalk between multiple nets including mutual capacitance and inductance coupling with non-ideal return paths [3]. Higher speeds bring numerous new challenges that have not yet been encountered, and existing problems will be more difficult to solve.

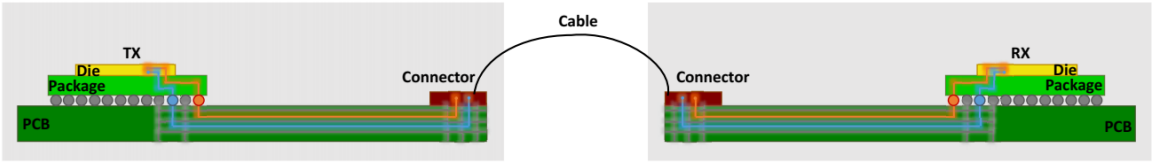

Figure 1.2: An Example of a Channel Topology for High–speed Interface Including Die, Package, Board, Connector and Cable. (After Figure 1 In [2]).

1.1 The Urge for a Restructured Design Methodology

At higher speeds, interconnects become major bottlenecks owing to significant increase in dielectric and conductor losses. One approach to reduce the loss is to utilize alternative package/system architectures, e.g., top-of-the package connection to flex circuits [6] or optical interconnects as in co-packaged optics [7]. The more direct approach, however, is the introduction of new materials and processes. Material

suppliers have been continuously improving their processes and chemistries to reduce the dielectric constant (Dk), dissipation factor (Df) and surface roughness while providing strong adhesion to the dielectrics [8].

Even when specifications are met in design with new low loss materials and better adhesion promoters, performance variation of the actual manufactured units is a major concern [9, 10]. Also the ever increasing demand for higher data rates with tighter design margins makes the systems more susceptible to variations. Without the means to evaluate signal behavior in a systematic manner as the physical and electrical characteristics of the system components vary, uncertainty may cause significant performance degradation and yield reduction There are two types of sources that lead to high-speed interconnect performance variation:

1. **Use-conditions:** Environmental conditions, e.g., temperature (T) and relative humidity (RH) can impact both the dielectric material [11] and conductor material properties [12]. This is not limited to the ambient temperatures and RH the system is being used in, but also include the temperature changes due to active components in package. For instance, active die could cause temperature increases in package substrate up to 90 - 110$^{\circ}C$ [13]. Such conditions can account for profound adverse effects on loss and diminishing returns for the new materials and processes unless they are temperature and RH insensitive. Since most systems are required to reliably operate over a wide range of use-conditions across the entire product lifespan, not accounting for this variation in link budget results in optimistic designs and can cause product failures. This places demands on accurate and reliable temperature and RH dependent methodologies in order to optimize high speed input/output (HSIO) designs for realistic use-conditions, which is covered in Chapter 2.

2. **Manufacturing processes:** There are many factors in a high-speed interconnect manufacturing process that can introduce variation. These factors can be split into 3 main segments: (i) raw materials, i.e., dielectric and conductor material properties, (ii) dimensions, i.e., stack-up and corresponding design rules, and (iii) surface roughness. These factors substantially impact the electrical performance of high-speed interconnects [14]. The challenge for designers is to ensure robust system performance under all operating conditions given the manufacturing process variations. Consequently, accurate quantification of the performance impact of uncertainty is necessary [15], which is covered in Chapter 3.

1.2 The Validation and Uncertainty Quantification

As data centers scale, interconnects along with advanced materials and processes play a crucial role in enabling faster data transfer rates. However, predictability of interconnect performance also becomes increasingly challenging at these higher speeds. High-speed interconnect behavior can be reliably predicted if interconnect models are successfully validated against measurements of manufactured test structures. A good measurement-to-modeling correlation is a key step to ensure a successful product design optimization for any new technology, material, or process. However, achieving good correlation for multiple metrics is not a simple task considering the large number of factors in the correlation flow, which influence the final performance.

Validation requires an understanding of the robustness of the measurement methods as well as the manufacturing process variations present in an imperfectly fabricated test structure. A measurement result is incomplete unless accompanied with an estimate of the uncertainty associated with the measurement [16]. There are many possible sources of measurement uncertainty, including the impact of environmental

conditions, bias in reading instruments, finite instrument resolution, or discrimination threshold, approximations, and assumptions incorporated in the measurement method [17]. Considering all the challenges in high-speed interconnect validation, it is not surprising that poor correlation occurs more often than is desirable. To ascertain whether a correlation is good or poor, one needs to understand how the uncertainty propagates to the outcome, and not just focus on the outcome itself. This places demand on a methodology for the uncertainty quantification of each measurement involved in high-speed interconnect validation, and their propagation to the final electrical performance metrics [15, 18, 19], which is covered in Chapter 4. It is worth noting that this is not the uncertainty coming from the manufacturing process variations in high volume manufacturing scenario, but the uncertainty coming from the measurement technique, and procedure utilized for the characterization in a single unit modeling-to-measurement correlation.

1.3 The Modeling and Measurement of Surface Roughness

Surface roughness is a physical quantity that is introduced intentionally in typical copper foil manufacturing processes to improve the adhesion of conductor to dielectric and avoid delamination. Although this increases the reliability of the substrate, it deteriorates the electrical performance by manifesting itself as higher loss and delay.

Surface roughness characterization remains as one of the challenging tasks in high–speed interconnect validation. Many different approaches have been proposed to predict this impact of surface roughness [20–26]. Models rely on parameters extracted from the copper surface; however, it is worth noting that the accuracy and reliability of the roughness parameters depend on the quality and quantity of the measured data, the complexity of the model, and the chosen method for finding the roughness parameters. This creates a nonideal situation where roughness models are treated as

purely mathematical functions. Therefore, instead of using actual extracted parameters, model inputs are determined by using an inverse modeling approach, where the roughness parameters are varied until the simulated results match the measured data. Chapter 5 explores new approaches to address these challenges.

1.4 The Key Contributions

The purpose of this work is to create a methodology that is both academically rigorous and has a significant impact on industry. This methodology will provide an accurate characterization of the electrical performance of interconnects under realistic use-conditions, accompanied by an uncertainty analysis to improve the assessment of correlation quality. The key contributions of this work include:

- Examining the impact of the use-conditions and manufacturing process variations on signal integrity performance,
- Quantifying measurement uncertainty for improved correlation quality,
- Investigating the effects of various adhesion promotion and copper surface roughness and developing a rigorous method for predicting loss.

In late 2018, the Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS) of the Electrical Packaging Society (EPS) collaborated with industry and academic experts to develop a series of contemporary benchmarks. Majority of this work contributed to one of the benchmarks the Packaging Benchmark Committee [27] elevated into the Suite [28].

Chapter 2

IMPACT OF USE CONDITIONS ON DIELECTRIC AND CONDUCTOR MATERIAL MODELS

Use conditions based on temperature and humidity can have a significant impact on the package material properties and loss, which is required to be included in modeling assumptions to be able to set realistic specifications. Dielectric loss is affected by both temperature and humidity through material properties. Conductor loss, however, is affected by only temperature explicitly through conductivity and implicitly through skin depth and surface roughness modeling. This chapter presents a systematic use condition dependent methodology for package high speed interconnects including a robust dielectric material characterization metrology. Correlation to high fidelity insertion loss measurements at different temperatures indicates that the roughness correction factor extracted at one temperature does not fit all and leads to underestimating the loss at higher temperatures. Without loss of generality due to unified form of correction factors of existing common roughness models, a modified version of Huray's *snowball* model with an explicit temperature dependence is proposed to achieve high quality on-package interconnect loss correlation at different temperatures.

Prior research has investigated temperature and RH impact on the performance of high speed interconnects pertaining to material properties, insertion loss, and channel metrics [29–40], but falls short of addressing the temperature impact on surface roughness modeling adequately. High temperature can account for both an increase in dielectric loss and a decrease in bulk conductivity. The latter has a larger loss impact at low frequencies while the high frequency conductor loss is influenced significantly by the surface roughness. Most of the existing surface roughness models [20–24, 26]

utilize a correction factor (K) as a function of skin depth (δ) to obtain effective conductivity (σ_{eff}) from bulk conductivity (σ_{bulk})

$$\sigma_{\text{eff}} = \sigma_{\text{bulk}}/K(\delta)^2 \text{ where } \delta = 1/\sqrt{\pi f \mu_r \mu_0 \sigma_{\text{bulk}}} \tag{2.1}$$

where f is the frequency, μ_r and μ_0 are the relative permeability of conductor and permeability of free space, respectively. For the roughness models not relying on a correction factor [25], σ_{eff} could still be derived. Temperature impact on σ_{bulk} inherently makes roughness models temperature dependent. Besides, K being a function of σ_{bulk} through δ makes σ_{eff} dependent on σ_{bulk} explicitly and implicitly, which leads to a nonlinear relationship with temperature.

This chapter investigates the impact of use conditions in a deterministic manner on package material characterization and presents a systematic correlation methodology to highlight the temperature impact on surface roughness modeling. The proposed methodology precisely defines the loss contribution of each factor, and measurements are substantiated by rigorous measurement capability analysis.

The rest of the chapter is organized as follows: Section 2.1 describes the use condition dependent methodology and correlation flow, followed by the review of measurement results and the measurement capability analysis for dielectric material characterization to determine the measurement uncertainty. Section 2.2 presents a method to predict material properties at any use condition. Section 2.3 examines the temperature impact on surface roughness modeling and loss correlation.

2.1 Use Condition Dependent Methodology

It is common practice to characterize the materials and measure the S-parameters in typical uncontrolled laboratory conditions, i.e., temperature ranges from $20°C$ to $25°C$ and RH ranges from 20% to 70%. However, often times realistic use conditions

are at high temperatures determined by the active die. This heat generated by the die along with the airflow by the cooler in actual systems may allow mitigating RH [10]. The gap between validation and actual use conditions, as shown in Figure 2.1, cannot be ignored owing to profound adverse effects on performance. It is imperative to include the effects of the active environment in which the system will be used in the modeling assumptions.

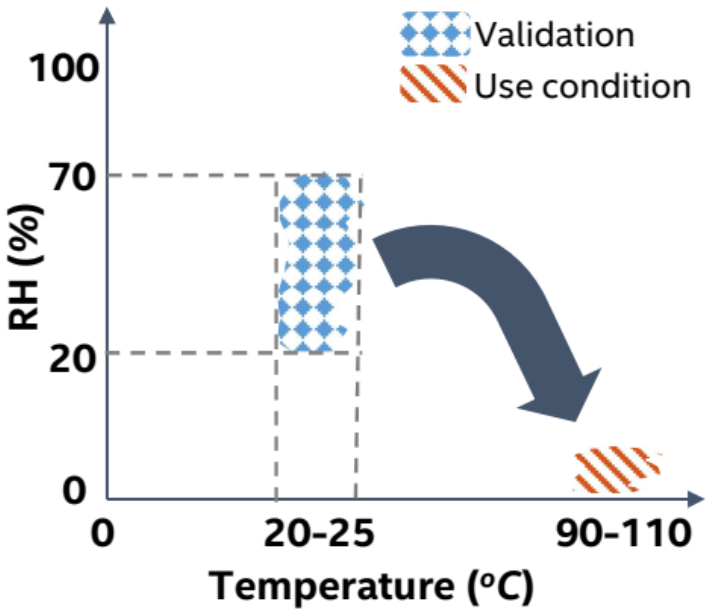

Figure 2.1: Typical Validation Conditions Illustrated Against Realistic Use Conditions.

Besides uncontrolled use conditions at the time of measurements, preexisting amount of moisture absorbed in materials and substrates can cause further deviation from the true values in both dielectric material characterization and S-parameter measurements. Considering any fluctuations occurred in the measurement as characterization tolerance or measurement uncertainty can lead overestimating the actual variation. This can result in expensive overdesigns. Prebaking the materials and substrates ensures all moisture absorbed are removed. Then, preconditioning guarantees the measurements are performed at the desired use conditions.

This section presents a systematic use condition dependent methodology for measurement-to-modeling correlation, as shown in Figure 2.2. In this flow, temperature dependence comes from both dielectric and conductor materials, whereas humidity dependence comes only from dielectric, since conductivity is insensitive to RH [30].

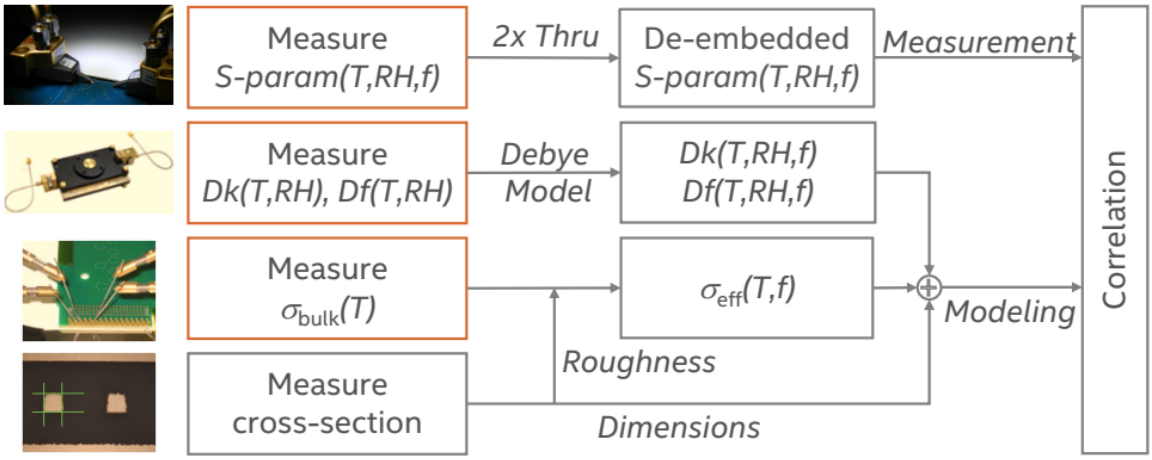

Figure 2.2: Use Condition Dependent Modeling and Correlation Flow. Red Boxes Indicate Temperature and/or RH Dependent Measurements.

Correlation flow has two main parts:

- **Measurement:** Performance network analyzer (PNA) measurements are performed in a temperature and humidity controlled environment. Prebaking and preconditioning of parts are critical to ensure repeatable and reproducible measurements at the desired use conditions. Measurement of S-parameters at varying use conditions are then followed by de-embedding to remove the unwanted artifacts of the system and fixtures to reveal the true characteristics of the transmission lines, e.g., loss and delay. Two-line de-embedding methodology is utilized [14] to post-process the S-parameter measurements of two transmission lines with different lengths, but having identical cross-sections and transitions to probes and connectors. De-embedding flow is depicted in Figure 2.3. Similar and alternative 2x-thru based de-embedding techniques exist in liter-

ature including Generalized S-parameters (GMS) [41], Automatic Fixture Removal (AFR) [42], Smart Fixture De-embedding (SFD) [43], and In-Situ De-embedding (ISD) [44].

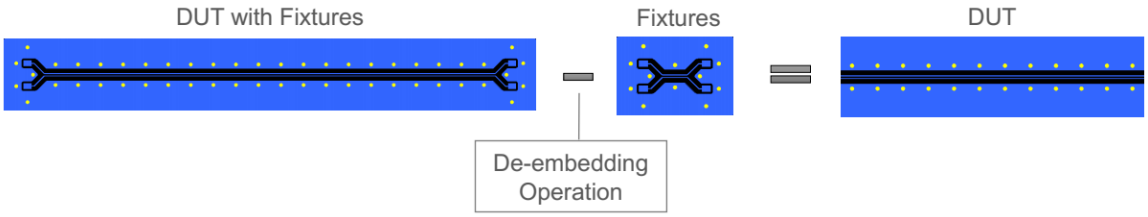

Figure 2.3: Illustration of De-embedding Process.

- **Modeling:** There are three steps to achieve accurate modeling of package electrical behavior: (i) Characterization of broadband frequency dependent effective conductor properties, (ii) characterization of broadband frequency dependent dielectric properties, and (iii) high fidelity representation of physical structures. Material characterizations are performed in a temperature and humidity controlled environment. Similar to PNA measurements, dielectric characterization requires prebaking and preconditioning, whereas bulk conductivity characterization does not. Frequency dependent broadband complex permittivity can be calculated utilizing wideband Debye models [45] by using the measured values of Dk and Df at a single frequency. On the other hand, frequency dependent effective conductivity is obtained by incorporating the surface roughness impact. The final high fidelity representation can be achieved by taking dimensional variations into account. Cross section pictures at multiple cut locations of any transmission line disclose dimensional variations. Especially, impedance and low energy metrics such as return loss are very sensitive to these dimensional variations.

The precision and robustness of the temperature and RH dependent metrology proposed in this paper is proven via a rigorous measurement capability analysis

(MCA) [46] to ensure high measurement repeatability and reproducibility. This is critical since it provides the necessary basis for separation of dielectric and conductor losses, and accurate surface roughness characterization at different use conditions.

2.1.1 S-parameter Measurements

Humidity impact of soak and bake out processes is investigated first for the device under test (DUT). Single-ended (SSL) and differential stripline (DSL) package traces routed on the layer below the surface with lengths of 10 and 20 mm are designed and manufactured. Figure 2.4 shows the routing and ground reference layers of SSL and DSL along with probe pads, transition regions and ground stitching vias. Using a precise analytical balance with readability of 0.1 mg, an experiment was set up to determine the rate of weight change over time, which depends on package substrate stack up, form factor and material set. DUT consisted of sixteen buildup layers and one core layer for a total of 18 metal layers, with a form factor of 37.5 x 42.5 mm and overall thickness of 1.5 mm.

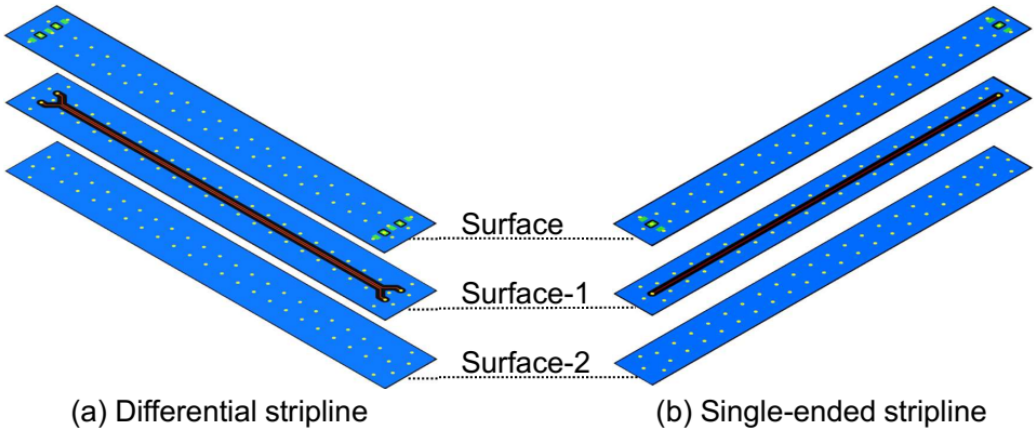

Figure 2.4: Differential and Single-ended Stripline Pictures on DUT.

The weight change of the packages normalized to its initial dry state while being soaked 90% RH at 25°C is shown in Figure 2.5. The initial high moisture absorption rate gradually saturates at 0.09% after 333 hours (∼2 weeks). It is worth to emphasize

that ∼70% of this moisture was absorbed within the first 24 hours. Succeeding baking process at 125°C after saturation leads to a rapid moisture removal rate, down to 0.01% within the first 24 hours. Weight gain returns to zero after ∼60 hours. Since the rate of weight change ceases in time, at least 3 days of baking process is selected as a requirement to ensure a dry state for this package.

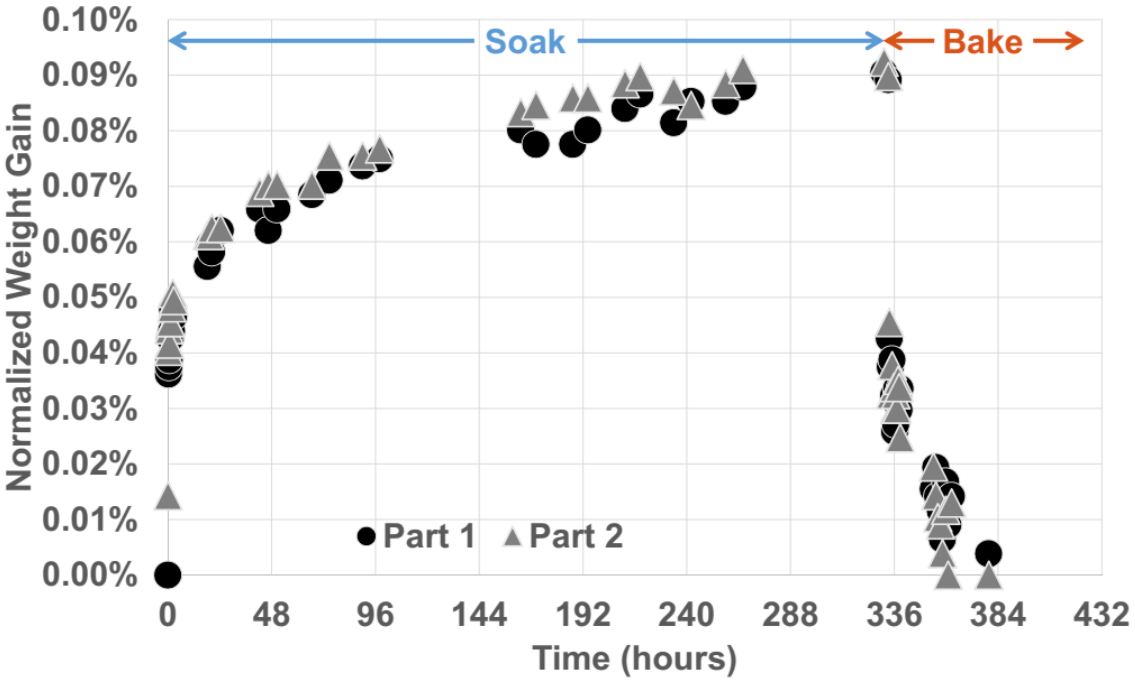

Figure 2.5: Weight Change of Two Parts of the Same Package During Soak and Bake Processes. Measurements Performed by ECC Lab.

PNA measurements are performed at several use conditions. To emulate one a typical use condition, 90°C and 0% RH is selected. In addition, 25°C and 60°C both at 0% RH are included to make a comparison and identify any trends. Humidity is excluded in PNA measurements and roughness extraction since the presence of moisture changes (accentuates) the temperature dependence of permittivity [29], but a more comprehensive study including humidity is performed for dielectric material characterization in Section 2.1.3. DUT is prebaked at 125°C for 3 days to remove moisture, cooled down in a nitrogen cabinet (0% RH) and measured on a temperature

chuck. Loss and delay increase with temperature for de-embedded SSL and DSL package traces with a length of 10 mm are shown in Figs. 2.6 and 2.7, respectively.

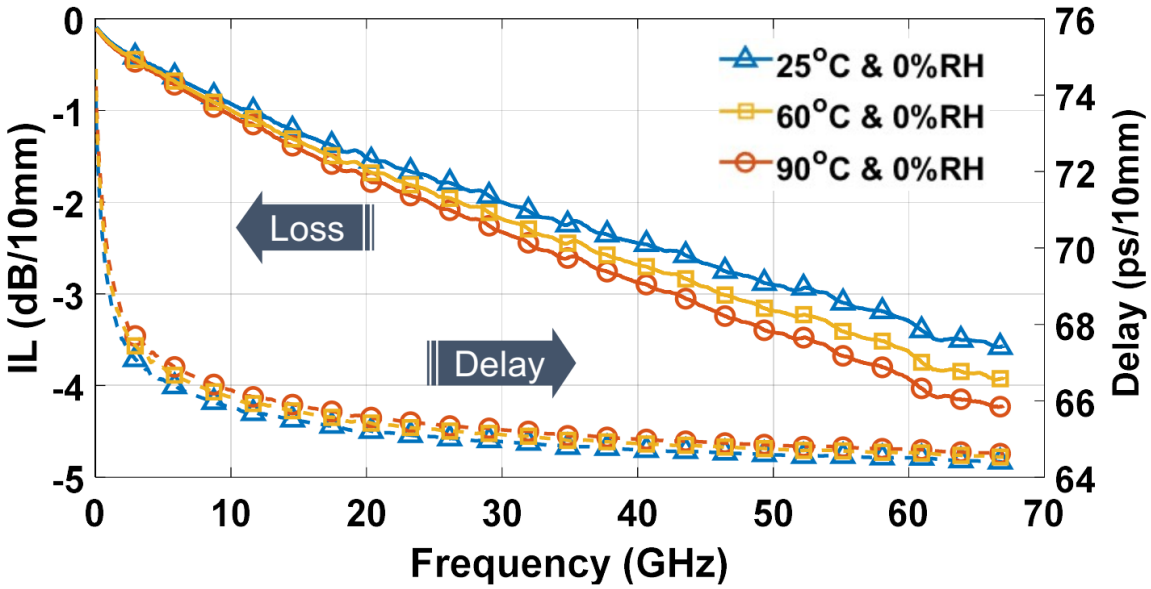

Figure 2.6: Temperature Impact on Single-ended IL (Solid Lines, Left Axis) and Delay (Dashed Lines, Right Axis) of SSL Package Trace. Measurements Performed by ECC Lab.

As temperature increases, both loss and delay increase, but the impact to former is more significant. Loss increase depends on multiple factors: σ_{bulk} reduction as detailed in Section 2.1.2, and Df increase as detailed in Section 2.1.3. It is also critical to see how surface roughness models changes with bulk conductivity, which is critical for correlation, as examined in Section 2.3.

Measured single-ended and differential loss as a function of temperature are shown in Figure 2.8 at multiple frequency points. It is clear that loss variation across temperature expands at higher frequencies. In other words, higher data rates suffer more from temperature dependent adverse effects. Loss increase at $90°C$ relative to $25°C$ rises from ∼0.1 dB/10 mm (1%) at 8 GHz to ∼0.6 dB/10 mm (7%) at 56 GHz.

Measured single-ended and differential delays as a function of temperature are shown in Figure 2.9 at multiple frequency points. Unlike loss variation across tem-

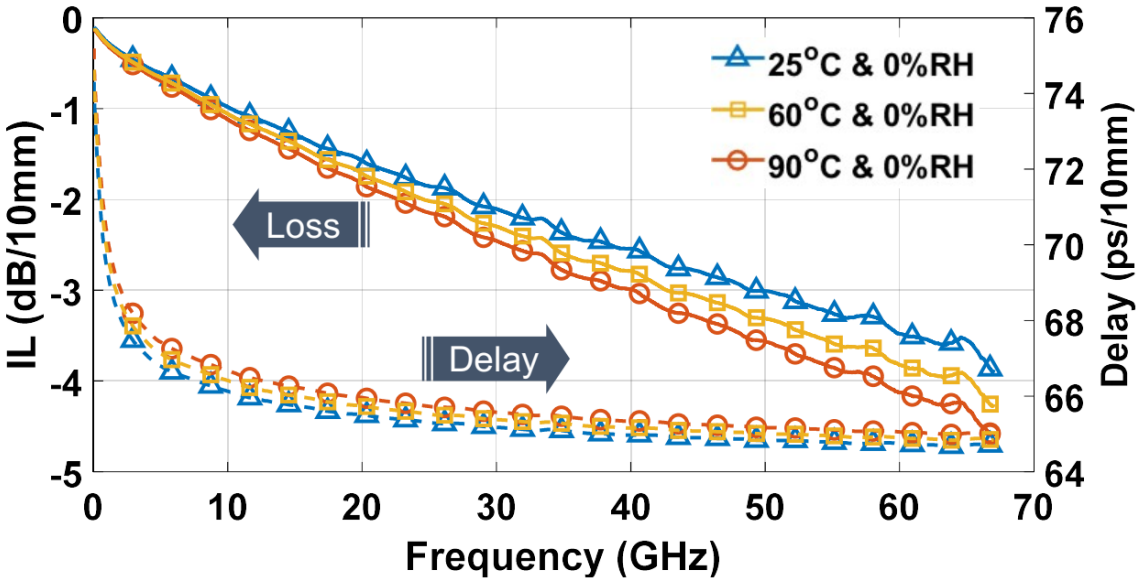

Figure 2.7: Temperature Impact on Differential IL (Solid Lines, Left Axis) and Delay (Dashed Lines, Right Axis) of DSL Package Trace. Measurements Performed by ECC Lab.

perature, delay variation across temperature shrinks at higher frequencies. Delay increase at 90°C relative to 25°C is ∼0.2 ps/10 mm (0.4%) for SSL and ∼0.3 ps/10 mm (0.5%) for DSL both at 56 GHz. DSL shows more sensitivity to temperature than SSL across frequency. Although this variation increases at lower frequencies, it remains less than 1 ps/10 mm.

2.1.2 Bulk Conductivity Measurements

DC resistivity (ρ_{DC}) of conductors depends on temperature and its purity level, but is insensitive to RH [30]. Pure copper characteristics are known as a function of temperature. However, since package conductors are not constructed of pure copper, low resistance (R) 4-wire measurements are performed on a temperature chuck at previously mentioned temperatures to determine the corresponding ρ_{DC} values.

After measuring R, DC resistivity of package conductor can be calculated as

$$\rho_{\mathrm{DC}} = R \cdot A/l \tag{2.2}$$

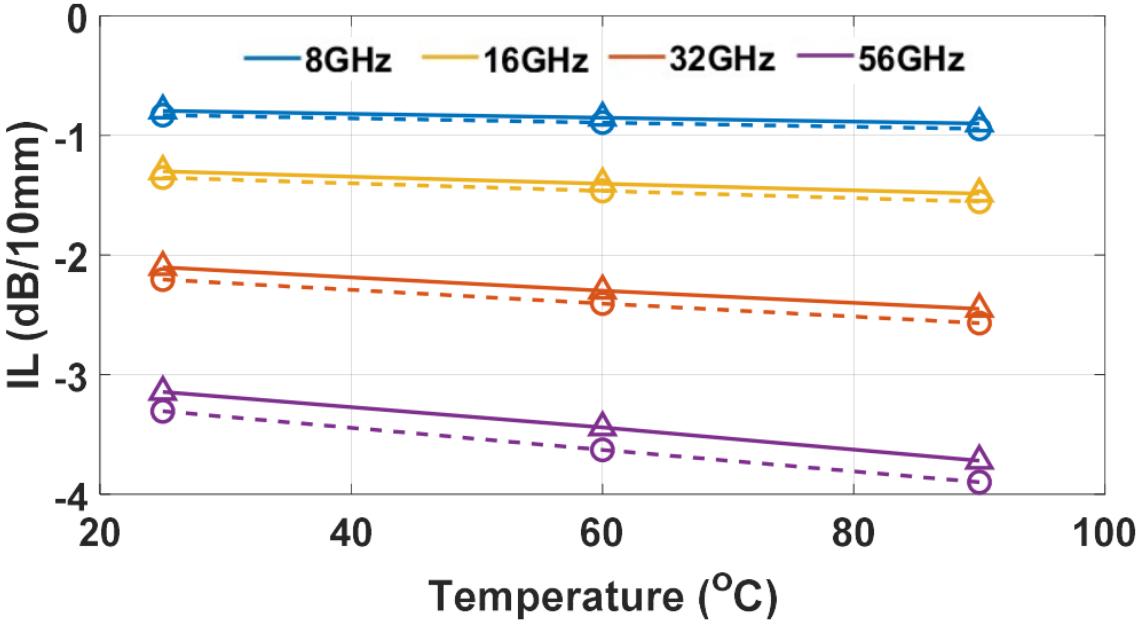

Figure 2.8: Loss of SSL (Solid Lines, Triangle) and DSL (Dashed Lines, Circle) as a Function of Temperature at Multiple Frequency Points. Measurements Performed by ECC Lab.

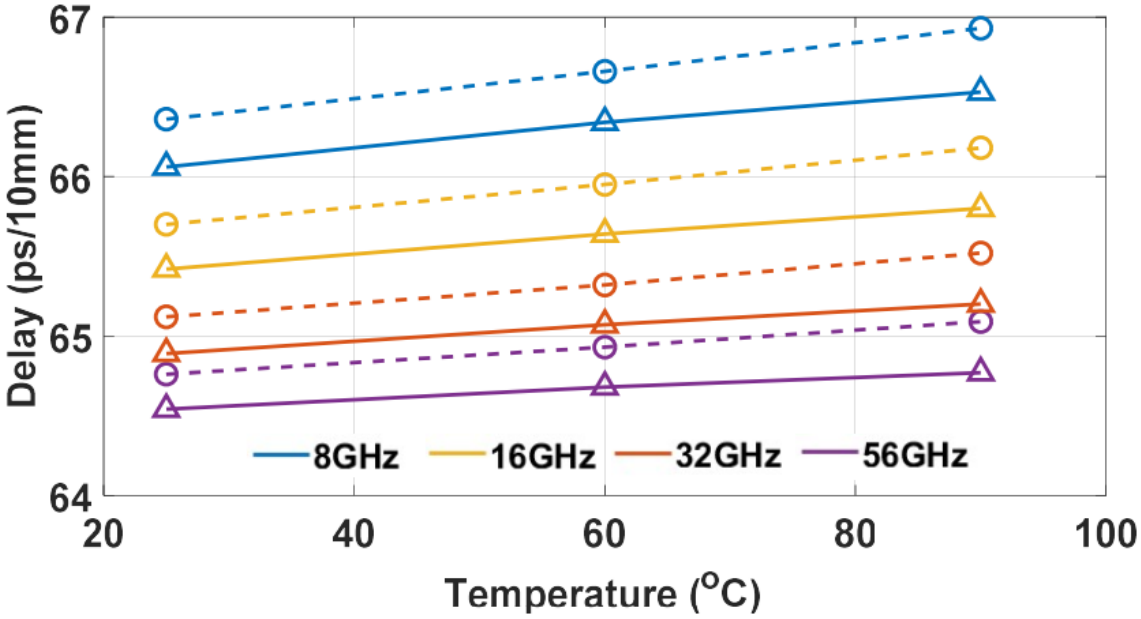

Figure 2.9: Delay of SSL (Solid Lines, Triangle) and DSL (Dashed Lines, Circle) as a Function of Temperature at Multiple Frequency Points. Measurements Performed by ECC Lab.

where l is the length and A is the cross section area of the trace. Both l and A are precisely measured for better accuracy. σ_{bulk} is simply the inverse of ρ_{DC}. Conductivity and resistivity normalized to room temperature are shown in Figure 2.10. Resistivity has a linear relationship with temperature and increases 27.4% at $90°C$ relative to $25°C$. This corresponds to 21.5% conductivity decrease. Package conductor temperature coefficient of resistance at $T_{\text{ref}} = 25°C$ is found to be $\alpha = 0.0043/°C$ given the relationship

$$R = R_{\text{ref}}[1 + \alpha(T - T_{\text{ref}})] \tag{2.3}$$

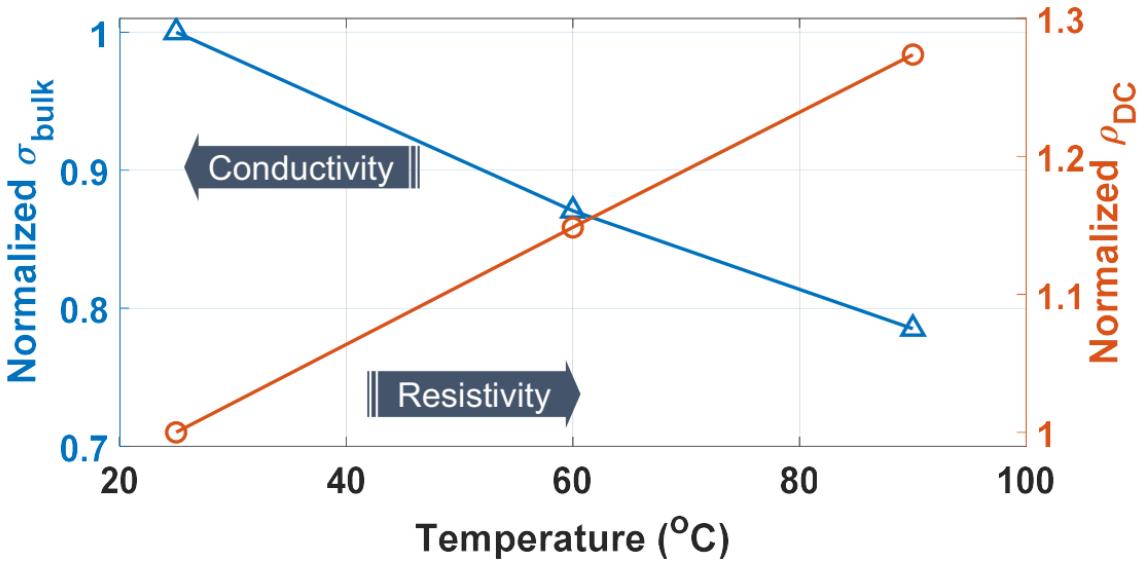

Figure 2.10: Temperature Impact on Normalized σ_{Bulk} (Triangle, Left Axis) and ρ_{Dc} (Circle, Right Axis) of Package Conductor. Measurements Performed by ECC Lab.

2.1.3 Dielectric Dk and Df Measurements

The proposed temperature and humidity dependent material measurement metrology follows that in [11] closely. Measurement setup as shown in Figure 2.11, is based on a split post dielectric resonator (SPDR) which provides accurate and repeatable measurement of Dk and Df at discrete frequencies [47]. SPDR is placed inside an en-

vironmental chamber to accurately control temperature and humidity, and connected to a PNA which is remotely controlled by a software tool to measure and collect characterization data.

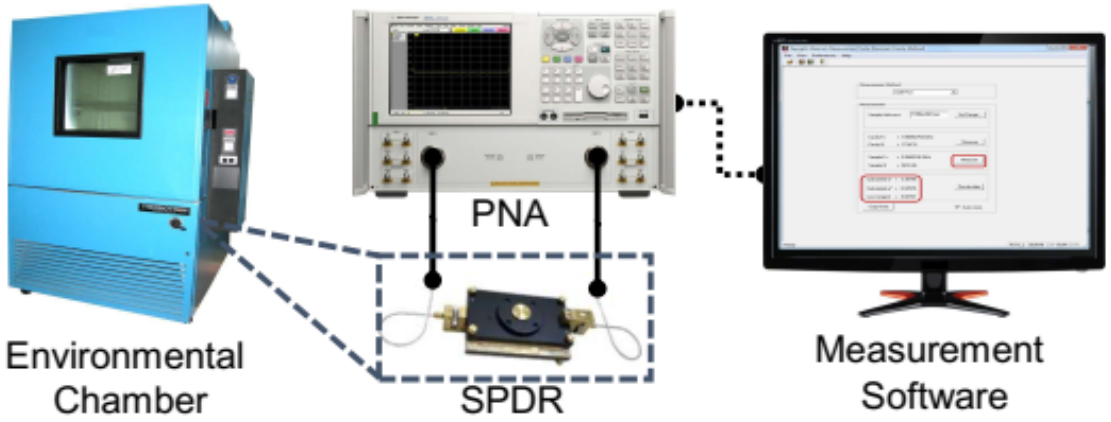

Figure 2.11: Dielectric Characterization Measurement Setup Based on SPDR.

Similar to Section 2.1.1, humidity impact of soak and bake processes is investigated for dielectric material samples. Each sample is prepared with the required thin film form factor. The weight change of package buildup and core samples normalized to their initial dry state while being soaked 90% RH at 25°C is shown in Figure 2.12. It is worth mentioning that the thickness (and weight) of buildup material sample is much smaller than of core material (∼5 - 10%). Buildup material absorbs 0.27% moisture of its weight within the first hour after dry state, which is ∼65% of all the moisture that it can possibly absorb. Core material has relatively slower moisture absorption rate, which saturates at 0.42% after 240 hours (10 days). Succeeding baking process at 125°C after saturation, leads to a rapid moisture removal rate for both, down to zero within a few hours. For buildup materials, at least 6 hours of baking process is selected as a requirement to ensure dry state for this package, which is significantly less than package substrate prebaking times.

In the procedure to characterize dielectric materials at varying use conditions,

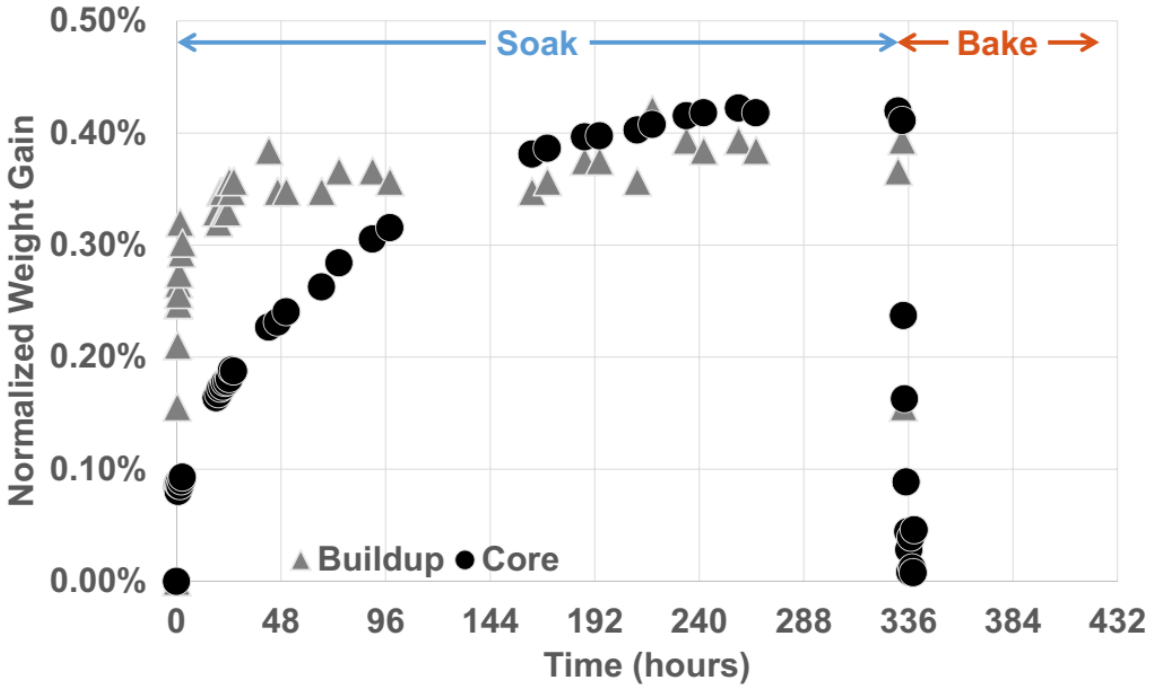

Figure 2.12: Weight Change of Package Buildup and Core Materials During Soak and Bake Processes. Measurements Performed by ECC Lab.

samples are prebaked for 6 hours at $125°C$ to remove any moisture, and then stored in a nitrogen cabinet to prevent absorption of moisture. Before measurement, samples are retained inside the environmental chamber at a specific temperature and RH level for a period of time that guarantees the samples reach the desired use condition. Depending on the sample thickness, this is typically achieved within 24 hours. Unloaded SPDR is measured at each condition to ensure the use condition effects are calibrated out during the sample measurement. Next, SPDR is loaded with the sample and measurement proceeds at 10 GHz for each condition.

A rigorous MCA with multiple packaging materials that are commonly used in industry has been performed to determine the tolerance limits of Dk and Df measurements at different use conditions. MCA consists of repeatability and reproducibility tests. In this paper, we discuss the reproducibility portion which examines the measurement variability introduced by all of the dynamic effects at a given use condition.

This includes repeated calibration performed by different operators over several days to capture operator-to-operator and day-to-day variations at different controlled use conditions.

In this MCA, four different kinds of materials were chosen including Teflon and package buildup, core and prepreg materials with varying thicknesses from 80 to $\sim$800 μm. Teflon was included in the MCA since package materials are not stable enough to make good accuracy standards. Samples are measured at three different conditions: (i) $25°C$ and 0% RH, (ii) $25°C$ and 90% RH, and (iii) $90°C$ and 0% RH. Several days of data collection from three operators gives reproducibility results as summarized in Table 2.1.

MCA results indicate highly reproducible measurements for this metrology. Relative standard deviation over multiple days and multiple operators is $3\sigma/\mu \leq 2.7\%$ for Dk and $3\sigma \leq 0.001$ for Df, where μ is the mean. It is important to note that, in addition to the variations due to multiple operators and several days of measurement, there is quantifiable inherent uncertainties in SPDR especially for the low loss material measurements [48]. When this is considered, precision of the proposed metrology reflects the state-of-the-art for both Dk and Df characterization at different use conditions.

The impact of nine discrete use conditions on package buildup Dk and Df are shown in Figs. 2.13 and 2.14, respectively. Conditions are selected within the safe measurement range defined in Section 2.2. Dk is the less sensitive material property to use conditions. Although it appears that there is a slight increase in Dk with temperature and RH, it is not possible to conclude this is an actual trend since the measurement uncertainty (2.7%) determined by the MCA is larger than the relative standard variation $3\sigma/\mu = 1.7\%$. Similarly, any impact on electrical impedance which directly depends on Dk is also expected to be very small. Df is the more sensitive

Table 2.1: Dielectric Dk and Df Measurement Reproducibility Results. Measurements Performed by ECC Lab.

			Dk		Df	
Sample	$T°C$	$RH\%$	**Mean**(μ)	$3\sigma/\mu$ %	**Mean**(μ)	3σ
Teflon	25	0	1.96	1.13	0.0003	0.0002
	25	90	1.96	0.68	0.0006	0.0012
	90	0	1.93	1.95	0.0003	0.0002
Buildup	25	0	3.28	1.32	0.0067	0.0005
	25	90	3.34	2.03	0.0107	0.0011
	90	0	3.30	1.63	0.0085	0.0001
Prepreg	25	0	3.11	1.57	0.0023	0.0005
	25	90	3.15	2.62	0.0048	0.0012
	90	0	3.11	1.39	0.0025	0.0001
Core	25	0	4.14	0.61	0.0090	0.0007
	25	90	4.17	0.39	0.0100	0.0004
	90	0	4.20	0.72	0.0101	0.0005

material property to use conditions. Relative to $25°C$ and 0 % RH, Df increases $\sim$31% at $90°C$ and 0% RH (exclusively due to temperature), and $\sim$56.4% at $25°C$ and 90% RH (exclusively due to humidity). A method to predict Dk and Df at any condition is presented next in Section 2.2.

2.2 Method for Dielectric Dk and Df Prediction

Complete measurement of all use conditions for each dielectric material is very time consuming. For design optimization at a desired use condition, one can use interpolated material properties generated from measured data at a discrete set of use conditions. In this section, a surface linear interpolation scheme based on measured

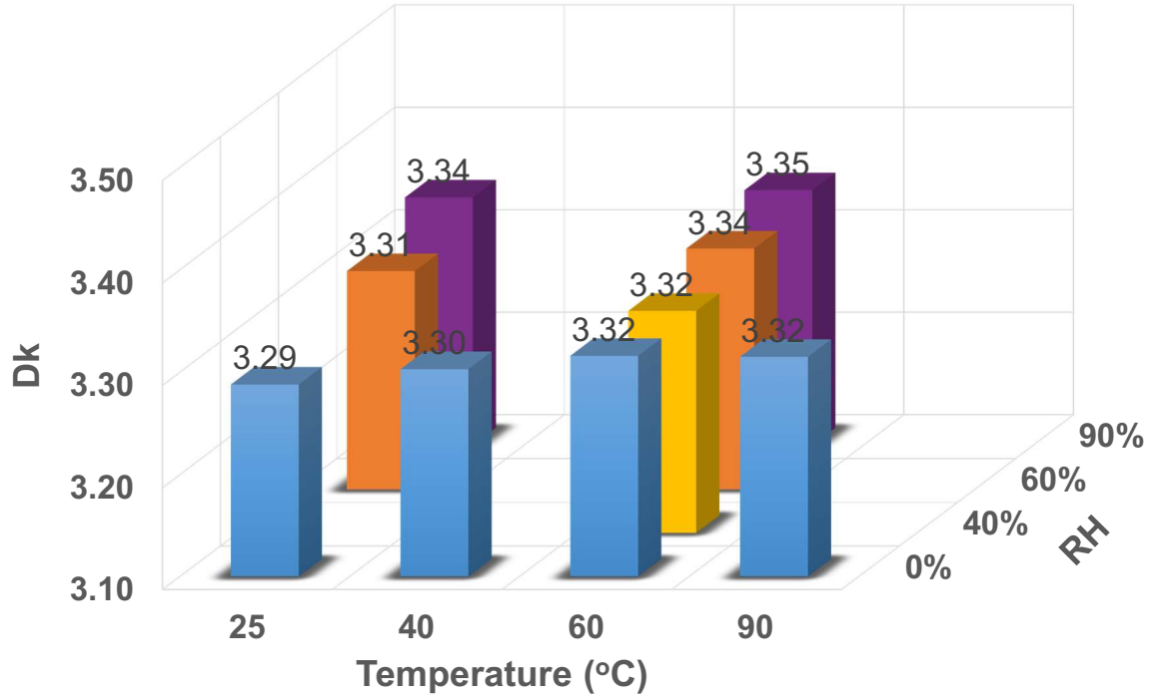

Figure 2.13: Use Condition Impact on Package Buildup Dk. Measurements Performed by ECC Lab.

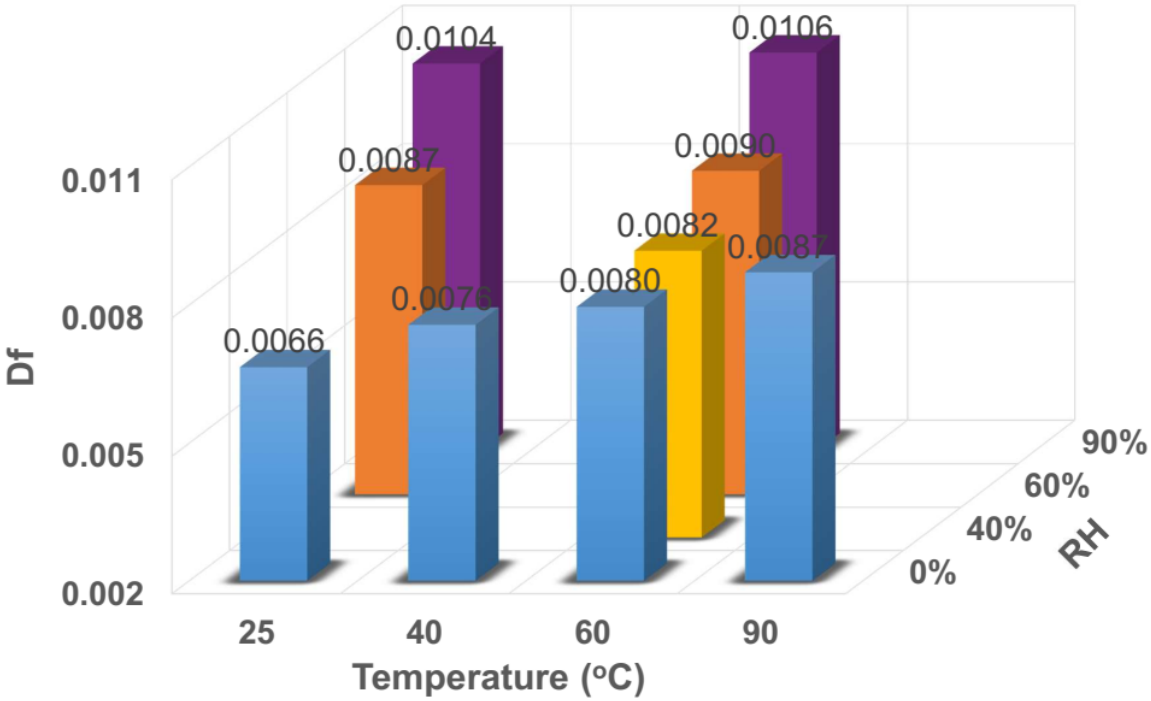

Figure 2.14: Use Condition Impact on Package Buildup Df. Measurements Performed by ECC Lab.

material properties at different temperature and humidity levels is applied to get Dk and Df of package materials at any use condition.

Dielectric material properties can be expressed as a function of temperature and RH using the method of linear least squares

$$\begin{aligned} Dk(T, RH) &= p_{00} + p_{10}T + p_{01}RH \\ Df(T, RH) &= q_{00} + q_{10}T + q_{01}RH \end{aligned} \tag{2.4}$$

where p and q are constant coefficients of Dk and Df, respectively.

In order to validate the interpolation scheme, the materials from the MCA are measured at nine different use conditions, as shown in Figure 2.15. Data collected at three use conditions indicated by marker $\star$ is used to generate a linear surface fit for temperature range from $25°C$ to $90°C$ and from 0% RH to 90% RH. Next, the interpolated data from the fit model and actual measurement at that use condition depicted by marker $\triangle$ is compared to determine the accuracy of the linear fitting. As an example, Dk and Df interpolation error is shown in Figure 2.15, which is smaller than MCA tolerance limits that demonstrate the goodness of the linear fitting.

Table 2.2 show the linear surface fit polynomial coefficients for each material used in MCA. By comparing the magnitudes of coefficients relative to Dk and Df, the sensitivity of the materials to temperature and humidity can be inferred. For all materials, p_{01} and p_{10} are smaller than Dk by four orders of magnitude (a factor of about 10^4). Considering the temperature and RH ranges from 0 to 100, this implies little impact to Dk, e.g., second significant digit after the decimal point. This is also observed in Figure 2.13. Df coefficients q_{01} and q_{10} are actually smaller than those of Dk, but their relative magnitudes (normalized to Df values) are higher. Teflon shows almost no dependency on temperature and humidity. Package buildup and core materials show both temperature and RH dependence, whereas prepreg material shows less sensitivity to temperature but more to RH.

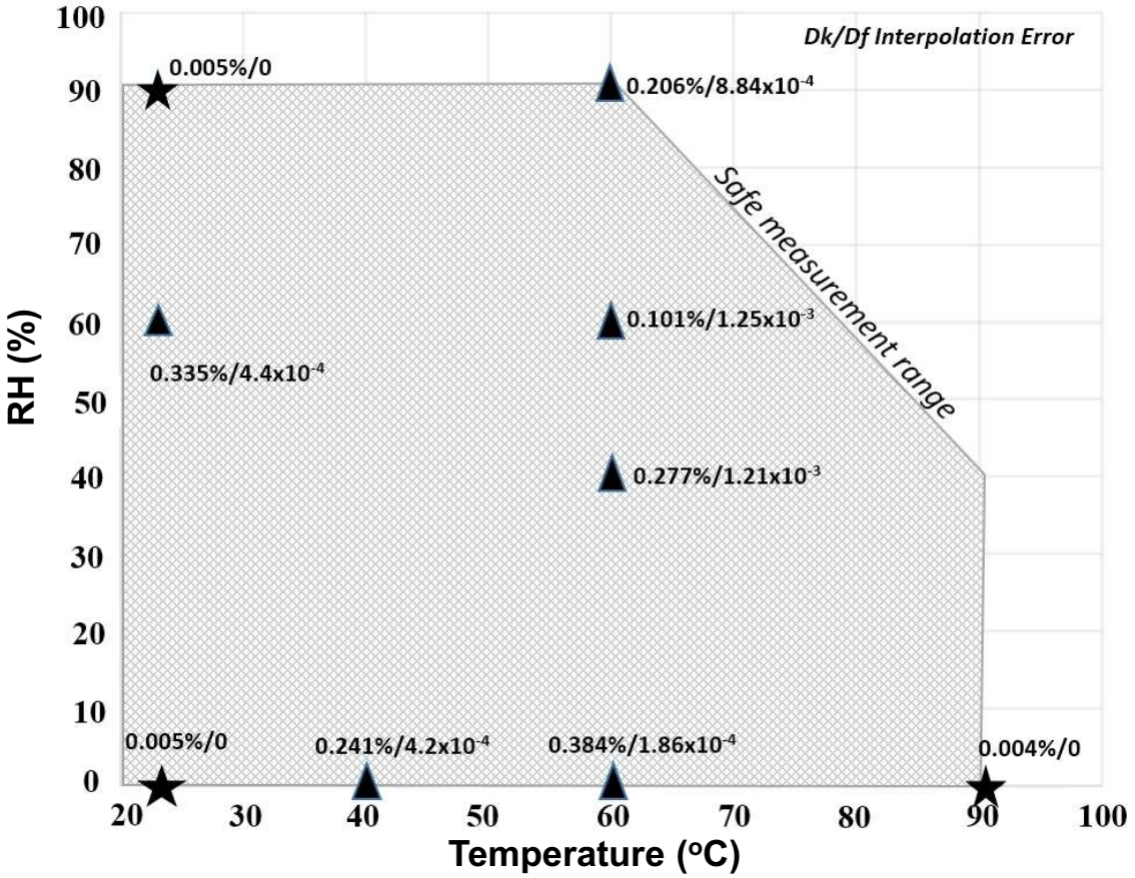

Figure 2.15: Dk and Df Interpolation Errors at Different Use Conditions. Measurements Performed by ECC Lab.

Table 2.2: Coefficients Used for Interpolation.

Sample	Dk			Df		
	p_{00}	p_{10}	p_{01}	q_{00}	q_{10}	q_{01}
Teflon	1.95	-1.05e-4	1.90e-4	0.0004	-2.54e-7	8.29e-7
Buildup	3.28	3.79e-4	4.69e-4	0.0065	2.03e-5	3.11e-5
Prepreg	3.09	1.84e-4	5.30e-4	0.0082	-9.11e-7	2.30e-5
Core	4.10	1.12e-4	3.45e-4	0.0086	2.53e-5	1.08e-5

Measured Dk and Df data points for selected use conditions and interpolated surface plots over 25 - 90°C and 0 - 90% RH are presented next. Note that this interpolation range includes outside of the safe measurement range, at which the accuracy is not verified. Dk and Df of package buildup material as a function of temperature and RH are depicted in Figs. 2.16 and 2.17, respectively. Dk is relatively smooth, whereas Df shows strong dependence to both, though the rate of change per $RH\%$ is larger than per °C, i.e., $q_{01} > q_{10}$. Dk and Df of package prepreg material as a function of temperature and RH are depicted in Figs. 2.18 and 2.19, respectively. Dk is again relatively smooth. Df shows higher RH dependence compared to package buildup. Df increases ∼85% as RH is changed from 0% to 90% at 25°C.

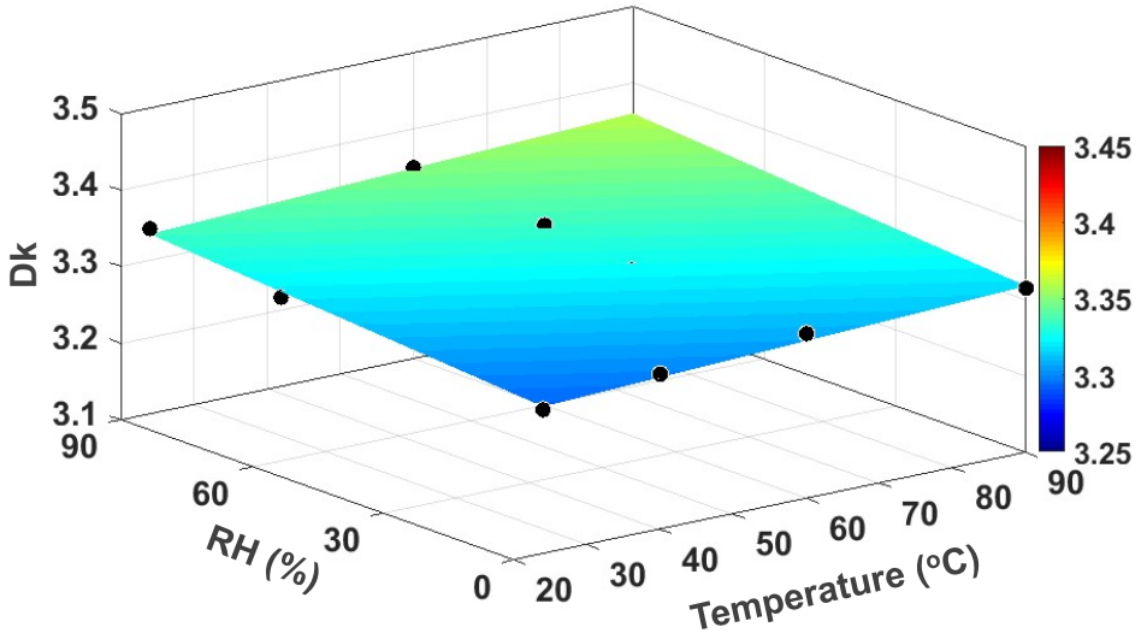

Figure 2.16: Package Buildup Measured (Circle, Black) and Curve Fitted (Surface, Color Coded) Dk as a Function of Temperature and RH.

2.3 Surface Roughness Modeling and Temperature Impact

The skin effect in rough conductor surfaces causes higher resistance and internal inductance, and manifests itself in not only higher loss but increased phase delay

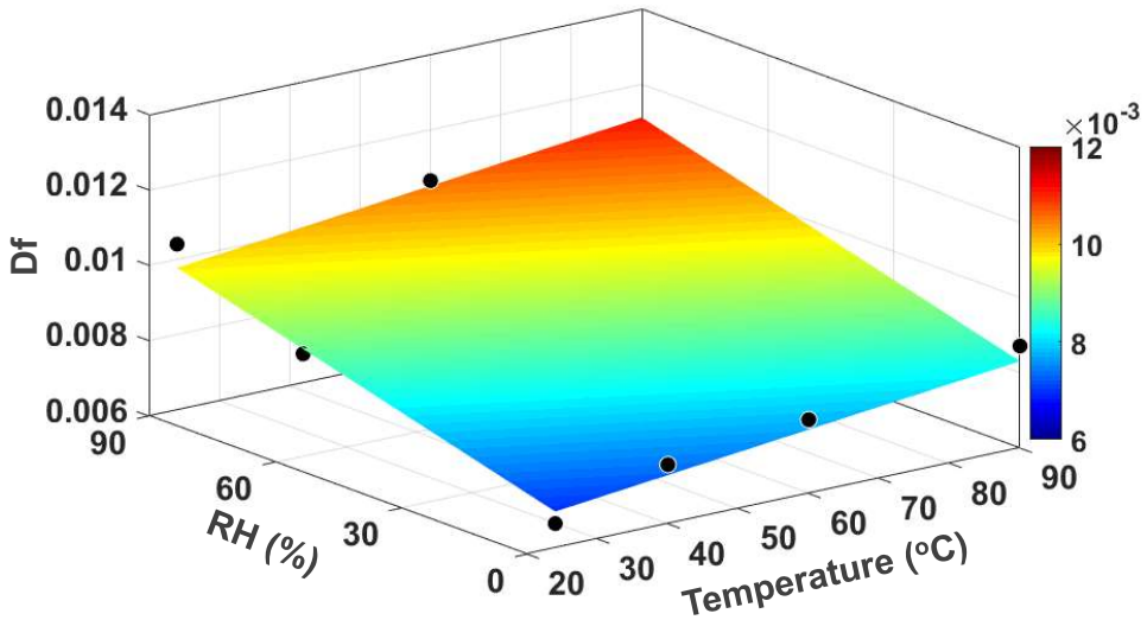

Figure 2.17: Package Buildup Measured (Circle, Black) and Curve Fitted (Surface, Color Coded) Df as a Function of Temperature and RH.

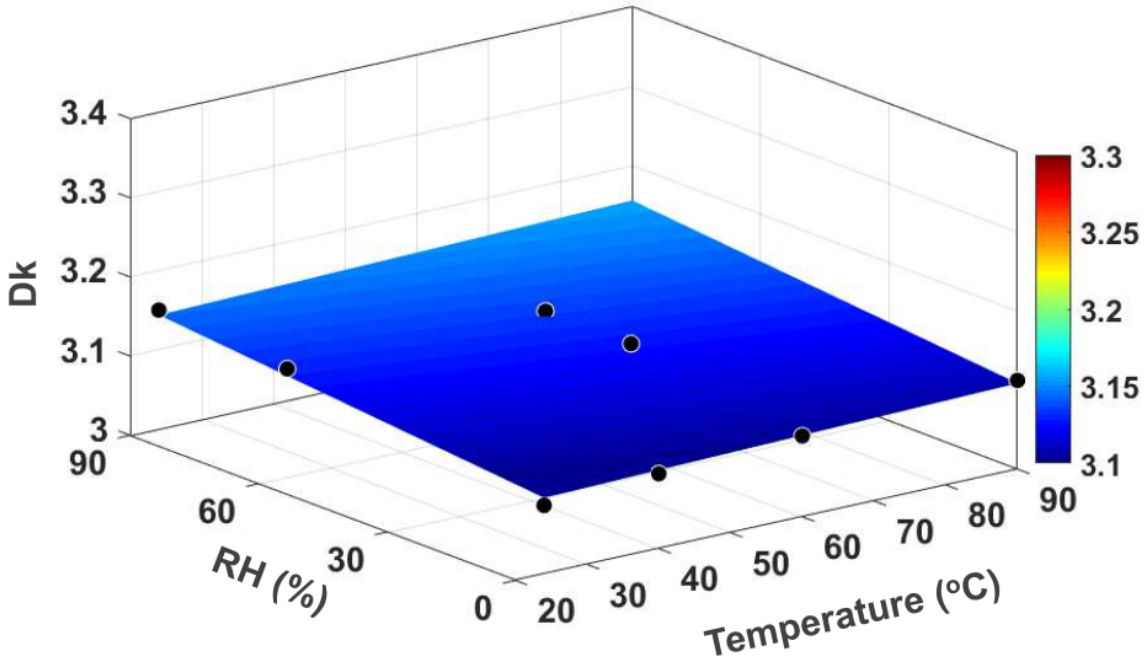

Figure 2.18: Package Prepreg Measured (Circle, Black) and Curve Fitted (Surface, Color Coded) Dk as a Function of Temperature and RH.

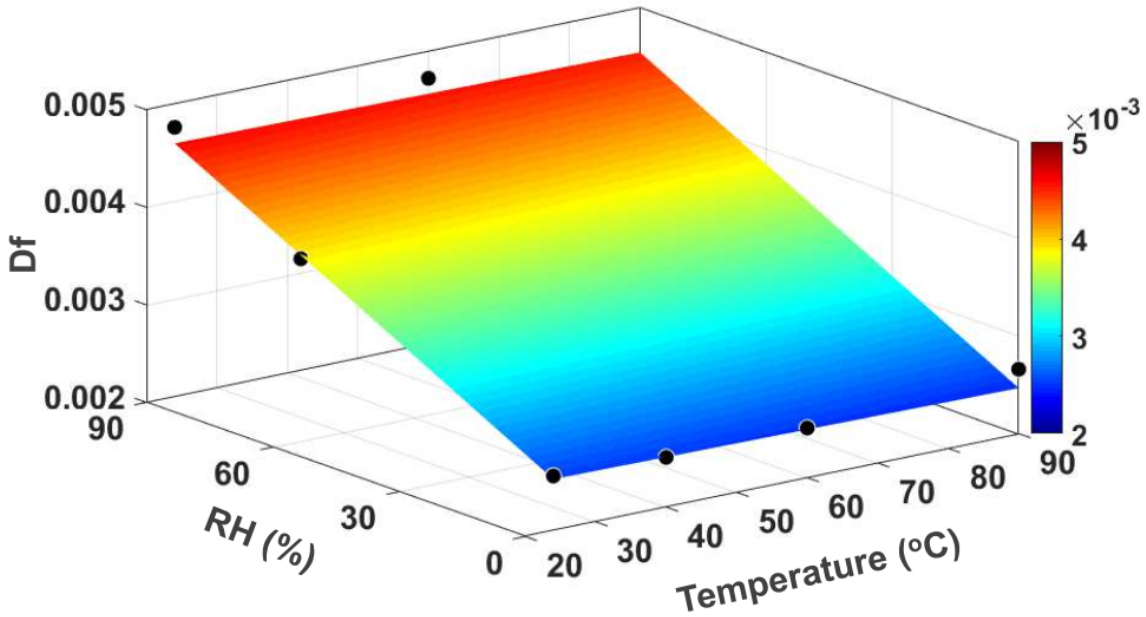

Figure 2.19: Package Prepreg Measured (Circle, Black) and Curve Fitted (Surface, Color Coded) Df as a Function of Temperature and RH.

to maintain causality [23, 25, 49]. This implies the correction factor K should be complex to *correct* both loss and phase due to skin effect, and causal versions of existing roughness models can be derived [50].

2.3.1 Correction Factor Temperature Profile

Surface roughness effect can be incorporated using either frequency dependent effective material properties or a surface impedance boundary condition. The former is convenient since (i) it can be readily applicable to any field solver without an increase in simulation time, (ii) increases fidelity of results by allowing solution of currents inside of conductors, and also (iii) the libraries for conductors with different adhesion promoters can be generated for third parties, which helps to reduce potential inconsistencies and errors during communication of this information.

Despite dissimilarity in surface roughness modeling, correction factors of existing

common approaches can be written in a unified form [51] as

$$K_U = 1 + (\zeta - 1) f(\xi, \delta) \tag{2.5}$$

where $\zeta > 1$ is the scalar factor that determines the maximum value of K_U (if f approaches to 1 at high frequencies), f is the roughness transition function and ξ is an input representing surface characteristics, e.g., surface basic element ball radius. It is worth mentioning that correction factors are typically a function of skin depth (δ). This gives the inherent temperature dependence to surface roughness models. In this section, temperature impact on surface roughness modeling is shown utilizing Huray's *snowball* model without loss of generality due to (2.5). Similar impact can be observed in other roughness models.

Correction factor for Huray's *snowball* model can be expressed as follows:

$$K_H(\delta, sr, a) = 1 + \frac{3}{2} sr \left(1 + \frac{\delta}{a} + \frac{\delta^2}{2a^2} \right)^{-1} \tag{2.6}$$

where sr and a are the surface ratio and effective radius of spheres, respectively. The implicit δ dependence of σ_{eff} as in (4.10) makes σ_{eff} dependent on temperature non-linearly. At higher temperatures, δ increases due to σ_{bulk} reduction (see Section 2.1.2 for more details). This leads to lower K_H at higher temperatures, for the same sr and a, as shown in Figure 2.20. This causes the absolute difference in σ_{eff} at different temperatures to become smaller, especially at higher frequencies. With this effect, it is not possible to achieve good correlation at all temperatures using the same roughness parameters, since variations in sr and a exert more influence on total loss than variations in σ_{bulk} or Df.

2.3.2 Measurement-to-Modeling Correlation

Following the methodology described in Section 2.1, sr and a can be synthesized at different temperatures accurately using the model dimensions obtained from the

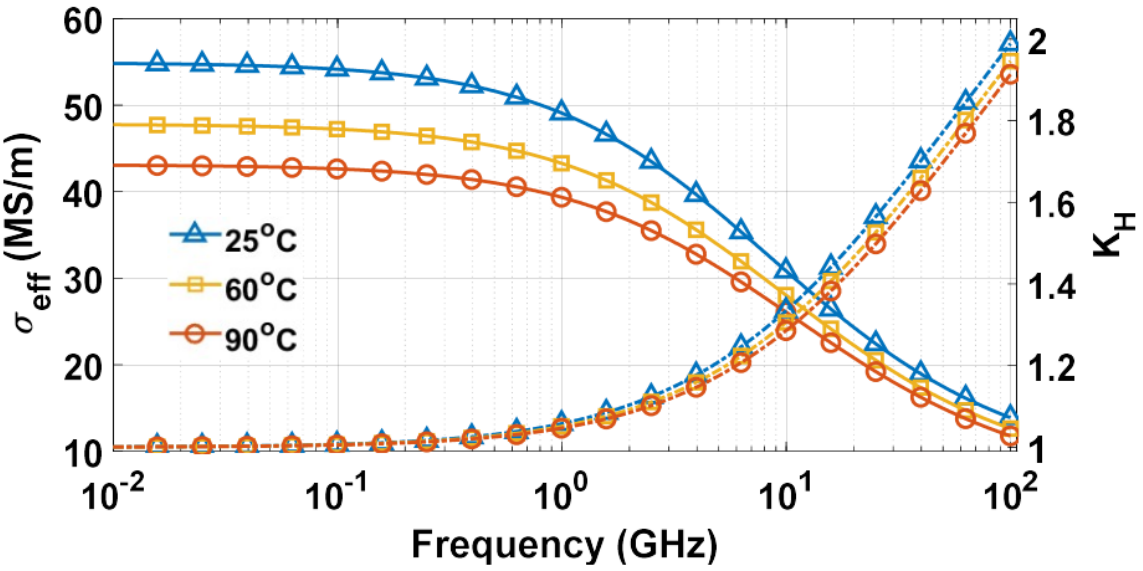

Figure 2.20: Temperature Impact on σ_{eff} (Solid Lines, Left Axis) and K_H (Dashed Lines, Right Axis) for the Same sr and a.

cross sectioning of the package trace. Intuition suggests that the same roughness parameters should be used at any temperature, since actual physical surface (and surface roughness) is assumed to remain unaffected. However, by careful investigation of the measurement-to-modeling correlation at different temperatures, we have concluded that the sr and a obtained at lower temperatures leads to underestimating the loss at higher temperatures. Figure 2.21 illustrates this with multiple modeling data showing the individual impact of each factor to total loss on top of measurements at $25°C$ and $90°C$ in dry state.

Roughness parameters are synthesized first for a good correlation at $25°C$ and 0% RH. Next, each temperature dependent factor (i.e., Dk, Df and σ_{bulk}) is replaced one at a time with their properties at $90°C$ and 0% RH, without changing the roughness parameters sr and a. This confirms that the total loss measured at $90°C$ cannot be predicted accurately until the roughness parameters are re-synthesized at $90°C$. The loss delta between the measurement at $90°C$ and the model with material properties at $90°C$ but roughness parameters extracted at $25°C$ (depicted by a

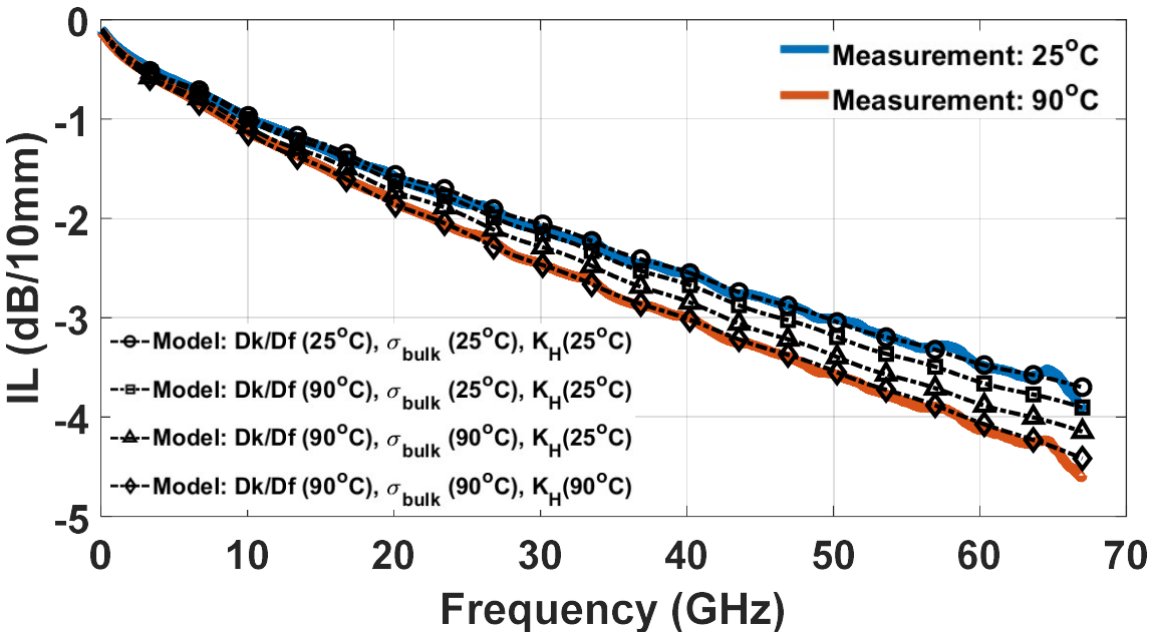

Figure 2.21: Measurement-to-modeling Correlation Using K_H Showing the Individual Loss Contributions of Each Temperature Dependent Factor. Measurements Performed by ECC Lab.

marker $\triangle$ in Figure 2.21) is growing exponential and consistent in log-scale.

2.3.3 Proposed Approach With Modified K_H

An explicit temperature dependence can be incorporated into K_H to account for the growing exponential loss delta which can be expressed as

$$K_H^{\text{mod}}(\delta, sr, a, T) = K_H(\delta, sr, a) + c_1(T - T_0)e^{-c_2\delta} \tag{2.7}$$

where c_1, c_2 are constant coefficients, and T_0 is the reference temperature. K_H^{mod} reduces to K_H at $T = T_0$. The correction factor in (2.7) can be used for modeling surface roughness at any temperature. For the package technology investigated, c_1 and c_2 are determined to be 0.0032 and 10^6, respectively. Temperature profiles of K_H^{mod} and σ_{eff} are shown in Figure 2.22.

K_H^{mod} in (2.7) with optimized parameters results in excellent measurement-to-modeling correlation in frequency domain at different temperatures, as illustrated in

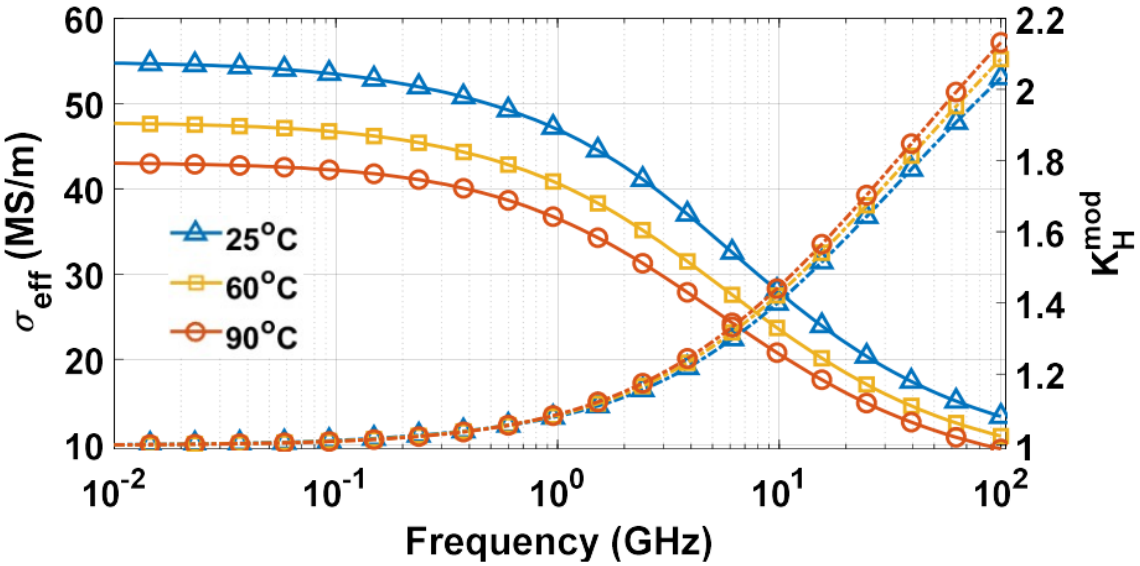

Figure 2.22: Temperature Impact on σ_{eff} (Solid Lines, Left Axis) and K_H^{od} (Dashed Lines, Right Axis) for the Same sr and a.

Figures 2.23 and 2.24 for single-ended and differential package traces, respectively. Also, these models can be seamlessly used in time domain such as SPICE-based transient analysis.

2.4 Summary

This chapter presents a novel systematic methodology that accurately captures the impact of use conditions on the dielectric and conductor models for package high-speed interconnects. First, a robust metrology is introduced to accurately characterize dielectric materials under various use conditions. Sample preconditioning requirements are detailed followed by an MCA study that demonstrates the precision of the metrology for different use conditions. A method for predicting the dielectric properties over continuous ranges of temperature and RH is proposed along with the results for typical types of package materials. Then, a comprehensive analysis is presented to show the inherent temperature dependence of correction factors of the existing surface roughness models. Correlation to high-fidelity insertion loss mea-

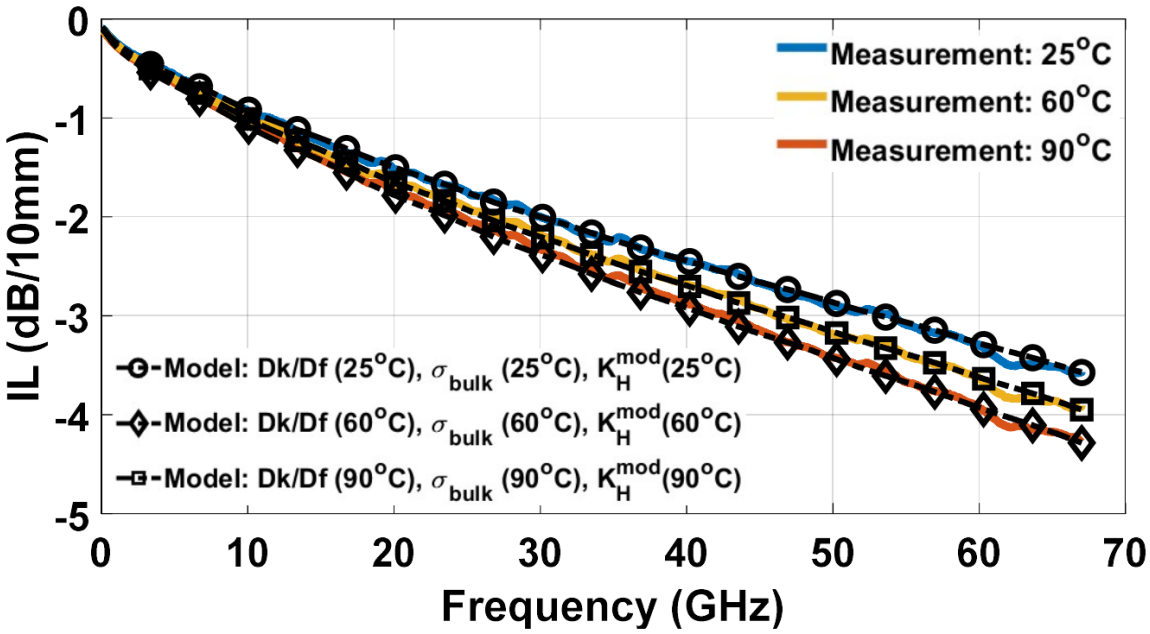

Figure 2.23: SSL Measurement-to-modeling Correlation Using K_H^{mod}. Measurements Performed by ECC Lab.

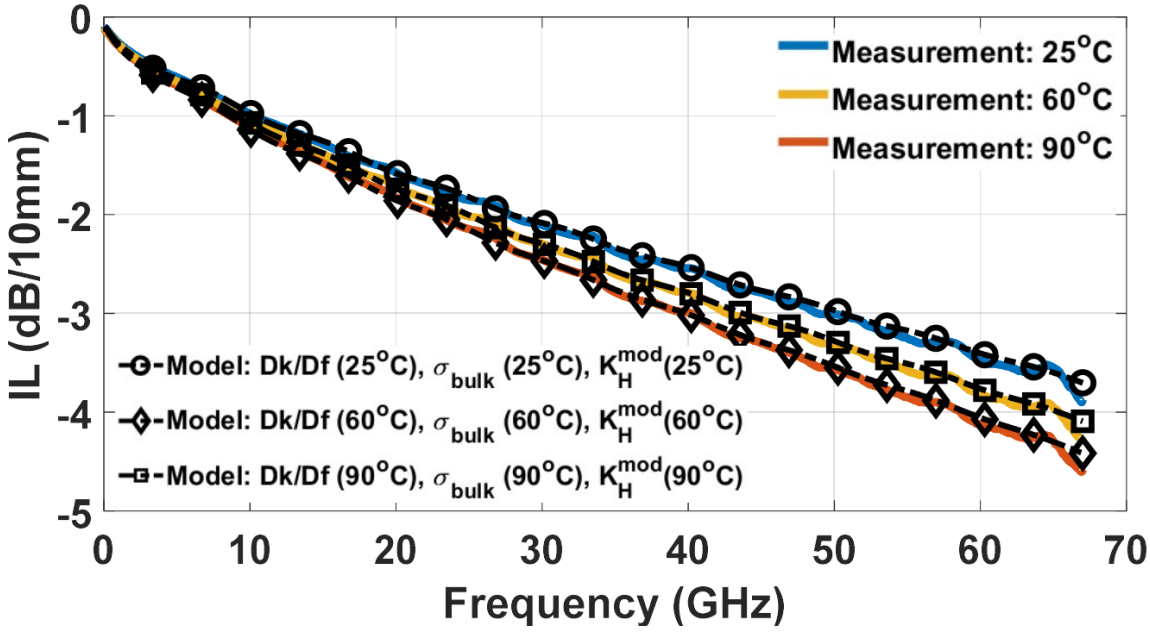

Figure 2.24: DSL Measurement-to-modeling Correlation Using K_H^{mod}. Measurements Performed by ECC Lab.

surements at different temperatures indicates that the correction factor synthesized at lower temperatures underestimates the loss at higher temperatures, necessitating an explicit temperature dependence for surface roughness models.

The proposed methodology ensures that the package design process can accurately account for the impact of product use conditions for emerging and future high-speed interfaces. The proposed methodology is considered to be general enough for the applications to other types of interconnects and use conditions. Such potential applications include but are not limited to board interconnects and characterization at manufacturing, assembly, or test environmental conditions. The validation of the method for these additional applications and more novel interconnect structures, such as tabbed transmission lines, is an important area for the future work.

Chapter 3

IMPACT OF MANUFACTURING PROCESS VARIATIONS

Variation in a high-volume manufacturing (HVM) process is a major concern in the design of high-speed interconnects [10, 52, 53]. The ever-increasing demand for higher bandwidth and lower loss with shrinking design margins makes system performance even more susceptible to uncertainty. Without the means to evaluate signal behavior in a systematic manner as the physical and electrical characteristics of the system components vary, variation may cause significant performance degradation and yield reduction or result in an overly designed system with increased design cycles and cost [10].

There are many factors in a high-speed interconnect manufacturing process that can introduce variation. These factors can be split into 3 main segments: (i) raw materials, i.e., dielectric and conductor material properties, (ii) dimensions, i.e., stack-up and corresponding design rules, and (iii) surface roughness, as illustrated in Figure 3.1. These factors substantially impact the electrical performance of high-speed interconnects [14]. Environmental conditions, e.g., temperature and humidity, are another source of variation, as explained in Chapter 2. Even if they do not directly affect the manufacturing process, environmental changes could trigger variations in performance of raw materials [13] and surface roughness [12]. The challenge for designers is to ensure robust system performance under all operating conditions given the manufacturing process tolerances and environmental changes.

Historically, statistical approaches have been primarily utilized for understanding the behavior of a complicated system so that the design can be adjusted to find a working solution. This process entails recognizing the key elements that exert the

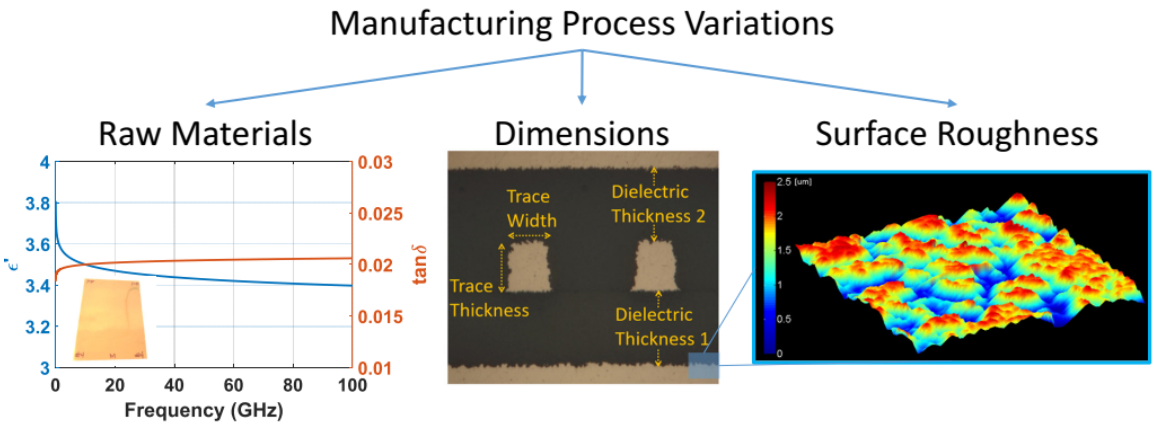

Figure 3.1: The Three Primary Areas Are Illustrated in Which Variations Can Occur Within the Manufacturing Process: Raw Materials, Dimensions, and Surface Roughness.

most significant impact on system performance, and modifying them to enhance the design's resilience, while adhering to the manufacturing constraints [10]. Response surface modeling is a technique widely used to find a predictive model by fitting polynomials to the data, and machine learning (ML) has recently gained a lot of attention in signal and power integrity optimization of nonlinear complex system [54–56]. This problem usually takes the form of a regression analysis using supervised learning and addresses the accurate quantification of the performance impact of uncertainty [15, 18, 57].

The rest of the chapter is organized as follows: Section 3.1 presents a machine learning based modeling methodology to analyze the impact of HVM process variations on electrical performance of high-speed interconnects, and compares with traditional approaches. Section 3.2 presents a novel methodology to determine corner case selection process based on maximum joint probability, which increases the accuracy of defect rate prediction which leads to cost saving through better designs or eliminating screening tests in vendors.

3.1 Machine Learning for Uncertainty Quantification

Monte Carlo analysis, being one of the traditional methods, relies on calculating the result over and over, each time using a different set of random values for any factor that has inherent uncertainty. As a result, Monte Carlo produces the distributions of possible outcome values. By the law of large numbers (LLN), observed expectation and variation of a certain outcome converge to the actual ones as more trials are performed. This large number of repetitions, e.g., 1 million or more, however, leads to a computationally expensive process, and a greater number of uncertain parameters exacerbates this cost. To reduce this overhead, a common approach is to derive a predictive model within a range per input, known as surrogate model, using design of experiments (DOE) [58]. Monte Carlo can then be performed using the predictive model, which will reduce the total number of actual simulations substantially and lead to huge reduction in computational resources and simulation time at the expense of accuracy.

Response surface modeling (RSM) is a commonly used method for predictive capability by fitting polynomials to the data. Conventionally, the least squares fitting using second-order combination of input variables is a good enough approximation for many disparate tasks including high speed signaling system performance [10]. Such a model is easy to estimate and apply, even when little is known about the actual relationships. However, it is presumed that the range of input parameters are small enough so that a quadratic (or low-order polynomial) model can fit the response. Therefore, each predictive model has an implicit tolerance limit on each uncertain variable. If the manufacturing process leads to a larger variation than this limit, the accuracy of the model is compromised. Another assumption is that the unknown nonlinear relationships can be reasonably approximated by polynomials, which may

not always be true.

To improve the accuracy and broaden the range inputs of surrogate models, ML provides promising techniques. This section focuses on the component level modeling of nonlinear relationship between uncertain parameters and electrical performance metrics in high-speed interconnects. The accuracy of more advanced ML algorithms is compared to RSM. Results show the proposed ML based methodology outperforms RSM and has the capability to model highly nonlinear structures.

3.1.1 Methodology

The impact of manufacturing variations on electrical performance metrics can be determined using the process flow shown in Figure 3.2. This detailed process flow comprises 3 major steps which can be interleaved iteratively: (i) sample selection, (ii) optimal surrogate model construction, and (iii) Monte Carlo analysis.

The accuracy of the methodology is highly correlated with the number and location of the samples in the design space. The significance of the number of samples is apparent owing to the data-driven nature of statistical modeling. Typically, if bias-variance trade-off is balanced, the more the samples are, the higher the accuracy is. The location of samples in the design space is also crucial to determine which variables affect the response and to identify the individual impacts of each variable. Often, better data is more useful than simply more data, i.e., quality over quantity. Consequently, random selection is unreliable, especially if the number of samples is small to reduce the computational costs. DOE addresses this problem by providing a means to collect the best data at minimal cost. DOE is a systematic process which improves the quality of information and eliminates redundant data. The method gives theoretical credence for choosing a set of points given a specific set of assumptions and objectives. The most used design is D-optimal (determinant) design which minimizes

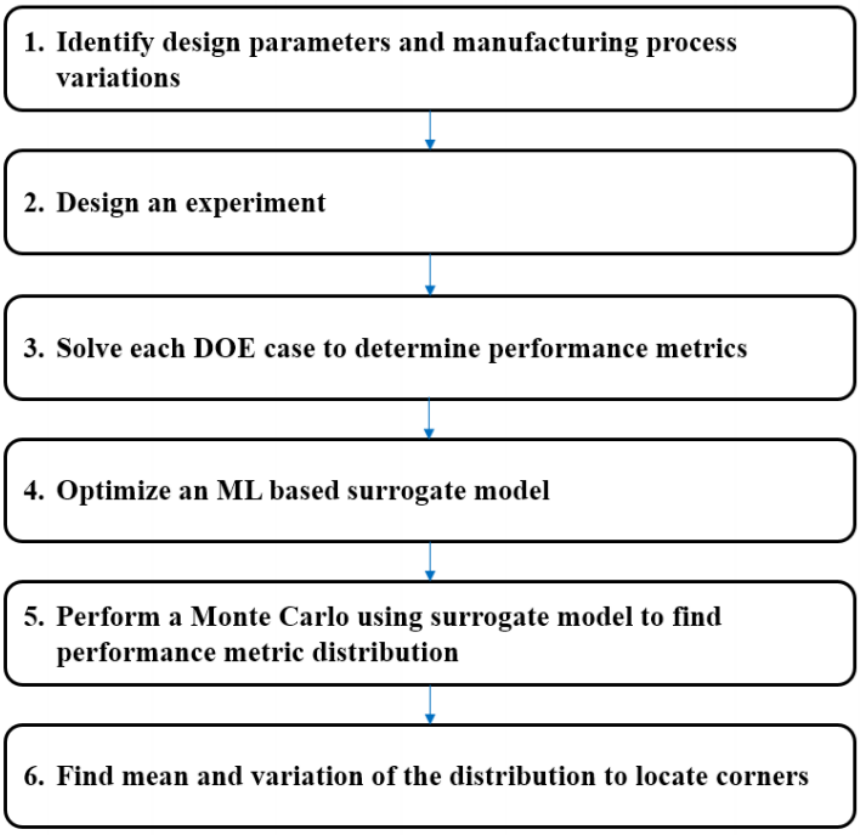

Figure 3.2: Uncertainty Quantification Process Flow.

the log determinant of error covariance matrix of the parameter estimates.

The traditional approach for predictive modeling is RSM. Its main virtues are simplicity of implementation and interpretability, whereas its main drawback is limited adaptability. If the relationship between input and output is not well approximated by a linear function, the model gives poor predictions.

Predictive model generation can also be defined as a regression problem via supervised learning. Support vector regression (SVR) and Gaussian process regression (GPR) are among the state-of-the-art ML algorithms for performing nonlinear regression [59]. SVR and GPR are based on the same probabilistic regressive model, but optimize different objective functions. SVR minimizes reconstruction error through convex optimization, and allows *kernel trick* to transform the data into a higher di-

mensional feature space with a nonlinear function to perform linear regression in the feature space. GPR provides a non-parametric kernel based Bayesian framework. Here, the goal is not only to predict the outcome of a simulation for a particular set of control parameters, but also to predict the distribution of the output, enabling the generation of confidence bounds around the predictions to assess the model quality. The prior beliefs, or domain knowledge, about the underlying function can be captured by choosing a descriptive kernel function. SVR and GPR both depend on the hyper parameters that need to be determined beforehand while training.

3.1.2 Benchmark Problem

A specific high-speed interconnect structure is selected as a benchmark problem: Differential stripline (DSL) package trace of a high-speed input/output (HSIO) interconnect. Electrical performance of HSIO interconnects is primarily determined by physical dimensions and dielectric and conductor material properties. A cross section picture of a DSL is shown in Figure 3.3.

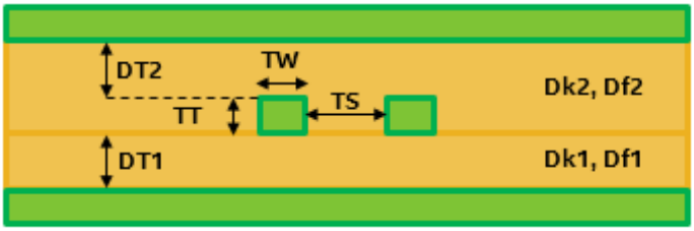

Figure 3.3: Cross-section Picture of a DSL along with Design Parameters.

Dielectric material properties, i.e., dielectric constant (Dk), dissipation factor (Df) are frequency, temperature, and humidity dependent; additionally, conductor material properties, i.e., conductivity, surface roughness are frequency and temperature dependent [13]. In this chapter, we focus on the variations in physical dimensions and dielectric material properties, excluding the variations in conductor material properties. Table 3.1 lists the input design parameters and the assumptions on their

nominal values and variations. It is worth noting that the variation assumptions of some parameters are excessively exaggerated in order to assess the capability of the methods at extreme conditions.

Table 3.1: Design Parameters with Nominal Values and Variation Assumptions. Variations of Some Parameters Are Exaggerated to Assess the Limits of Various Approaches.

Parameter	**Symbol**	**Nominal**	**Variation**
Dielectric Thickness	$DT1/DT2$	30 um	5 um
Trace Thickness	TT	15 um	5 um
Trace Width	TW	30 um	20 um
Trace Spacing	TS	60 um	40 um
Dielectric Constant	$Dk1/Dk2$	3.5	0.5
Dissipation Factor	$Df1/Df2$	0.02	0.01

Performance metrics are chosen to be the real and imaginary parts of the single-ended S-parameters. Differential lines have 2 signal traces which leads to a 4x4 S-parameter matrix with 32 real numbers (16 complex numbers) per frequency. Assuming that the network is passive, reciprocal, and symmetrical, reduces the number of performance metrics to 8 (4 complex numbers) per frequency as shown in Table 3.2.

Table 3.2: Electrical Performance Metrics.

Performance Metrics	**Real Part**	**Imaginary Part**
Return Loss	S_{11}^r	S_{11}^i
Insertion Loss	S_{12}^r	S_{12}^i
Near End Cross Talk	S_{13}^r	S_{13}^i
Far End Cross Talk	S_{14}^r	S_{14}^i

3.1.3 Numerical Results

The DSL described in Section 3.1.2 is used for the accuracy assessment of the algorithms including optimization and comparison. Linear regression is included as a baseline and ML based algorithms (SVR and GPR) are compared to RSM.

The objective of this section is to evaluate the capability of algorithms to explore the wide design space efficiently and accurately for the DSL. This is the reason behind selecting much wider ranges than typical for some design parameters (*TW, TS, Dk, Df*) as shown in Table 3.1. The training set consists of 200 cases with uniformly distributed input variables within their corresponding ranges, and the test set includes 1000 cases obtained by the same approach. A commercial 2D electromagnetic simulation tool is used to generate the performance metrics, for which a mapping function relating to design parameters is found.

Kernel Selection

GPR has 5 different kernel functions available with a separate length scale per predictor: *exponential, squared exponential, matern with parameters 3/2 and 5/2, and rational quadratic*. Each of these kernels are investigated in terms of training and test mean squared error (MSE) as shown in Figure 3.4. Hyper parameters are optimized per kernel using cross-validation. For a fair comparison, test MSE is better figure of merit for accuracy since test set is not seen by the optimized algorithms. Kernel *ardexponential* has the smallest training MSE but the largest test MSE, indicating an overfitting to training set despite the cross-validation step. Kernel *ardrationalquadratic* has the best accuracy for each performance metric, slightly better than *ardmatern52* and *ardsquaredexponential*.

SVR has 3 different kernel options: *linear*, *radial basis function (rbf)* and *poly-*

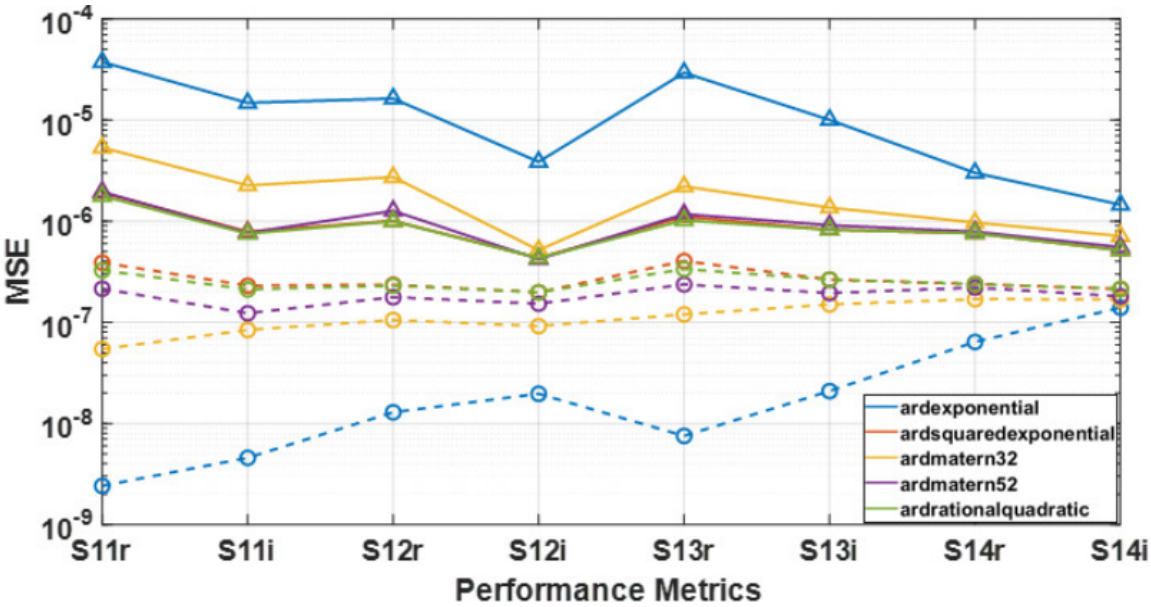

Figure 3.4: GPR Training (Circle, Dash) and Test (Triangle, Solid) MSE per Metric for Different Kernels.

nomial. The performance of SVR in terms of training and test MSE is shown in Figure 3.5. Similarly, hyperparameters are optimized using cross-validation per kernel. *Linear* kernel is the same as linear regression and has the worst performance overall. The accuracy of *polynomial* kernel with 2^{nd} and 3^{rd} order depends on the performance metric. 3^{rd} order is better than 2^{nd} order for S_{11} and S_{13}, on par for S_{14} and worse for S_{12}. It is also observed that *polynomial* can give a larger test MSE than *linear* regression for some metrics such as S_{12}, and S_{13}. The overall best accuracy is achieved with *rbf* kernel.

RSM we utilized in this paper relies on the least squares approach with quadratic combination of design parameters, as opposed to GPR and SVR which use the design parameters as they are shown in Table 3.1. The performance of RSM in terms of training and test MSE is shown in Figure 3.6. Here, we also included linear features to see the accuracy improvement by higher order terms. Quadratic features indicate linear, interaction and pure quadratic terms from design parameters. It increases the number of inputs but captures the covariance in between parameters. RSM provides

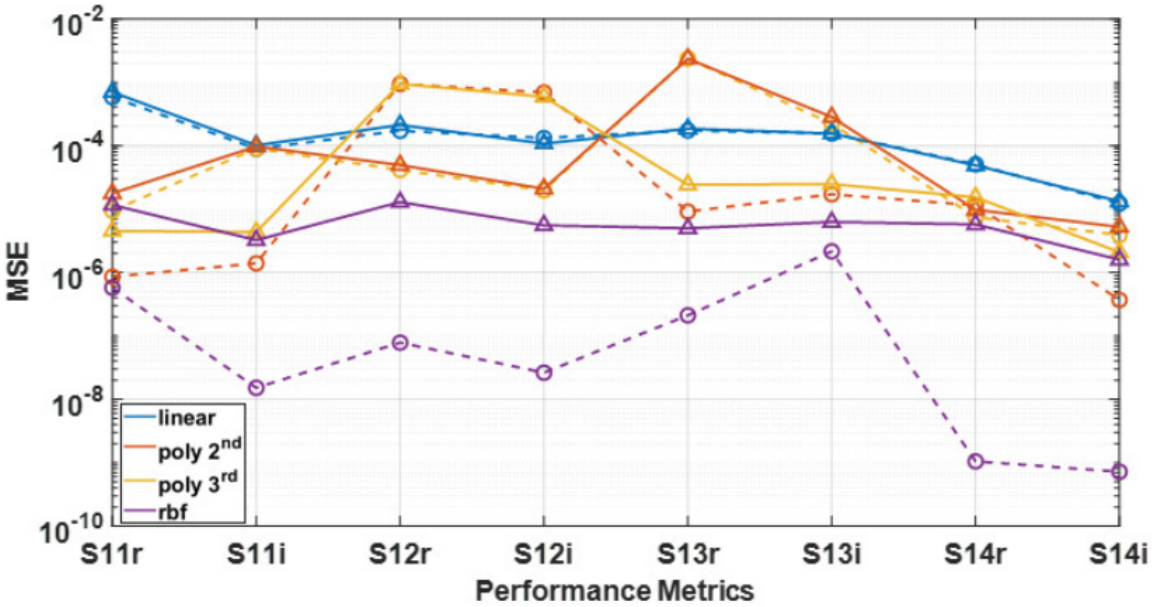

Figure 3.5: SVR Training (Circle, Dash) and Test (Triangle, Solid) MSE per Metric for Different Kernels.

accuracy improvement relative to linear regression by 1 order of magnitude (a factor of about 10).

Cross Comparison

After each regression method is optimized, their most accurate versions are compared across as shown in Figure 3.7. RSM has significant improvement over linear regression but is outperformed by ML based algorithms on each performance metric. GPR achieves the smallest error, hence provides the best performance.

One of the other advantages of GPR over other methods is that it provides confidence intervals for its prediction. Figure 3.8 illustrates an example of confidence intervals for one of the low energy metrics, S_{11} for 100 different cases. The small delta between 95% confidence intervals (CI) indicates high accuracy of predictions.

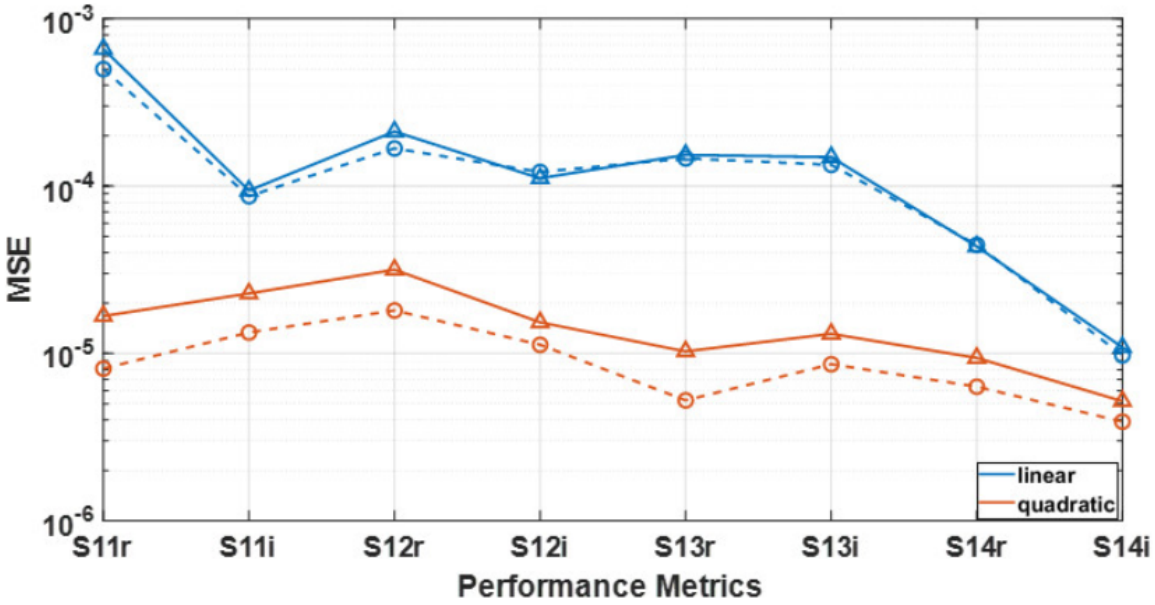

Figure 3.6: RSM Training (Circle, Dash) and Test (Triangle, Solid) MSE per Metric for Different Feature Sets.

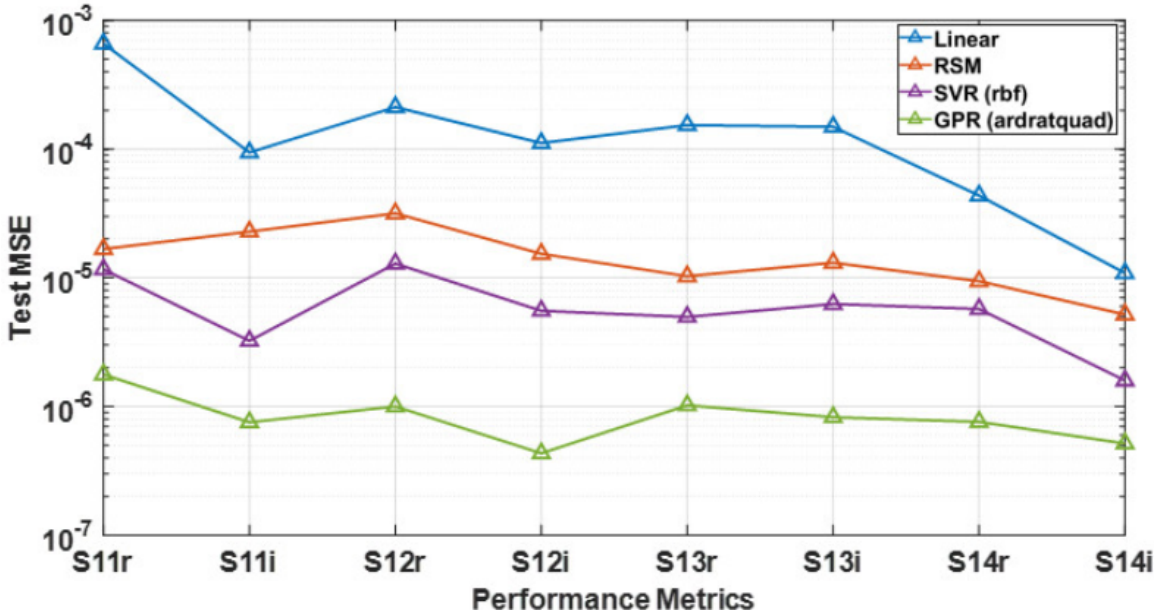

Figure 3.7: Across Method Test MSE Comparison Indicating GPR Outperforms on Each Metric.

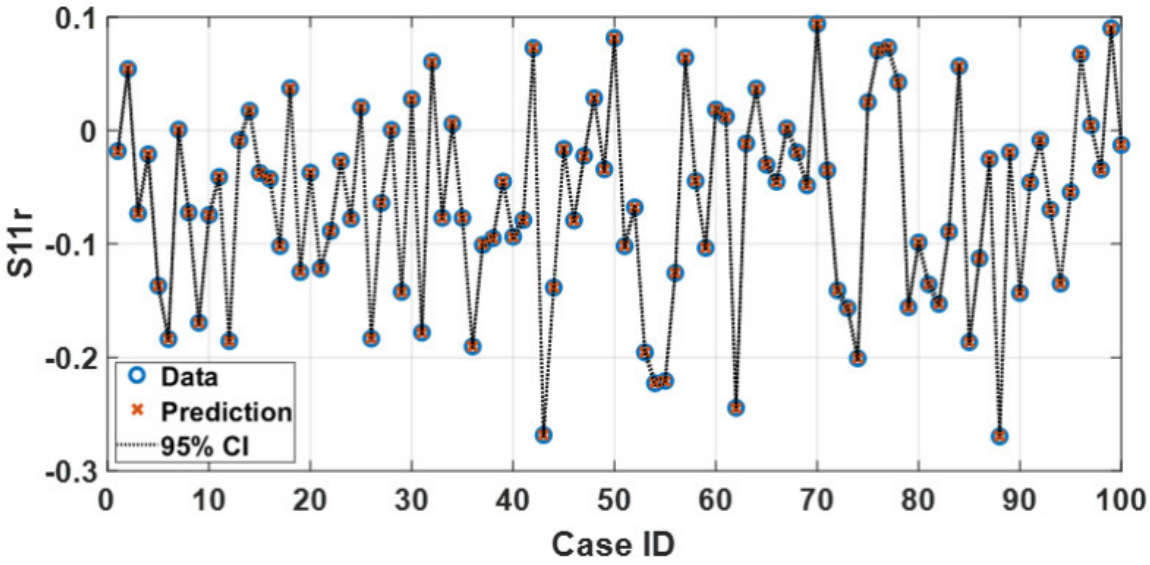

Figure 3.8: Actual Data and GPR Predictions with 95% Confidence Intervals (CI) for S_{11}^r.

3.2 Novel Corner Case Selection for More Accurate Defect Rate Prediction

As detailed in Section 3.1, statistical approaches are utilized along with design of experiments (DOE) to predict the electrical performance of channels, e.g., eye margin, as the physical and electrical characteristics of the system components vary. If this variation is not comprehended accurately in design and simulation, the platform DOE may not represent the accurate prediction of the performance, and leads to either over-design and cost adder or under-design and performance failure. The ultimate objective is to identify a working solution that comprehends the expected manufacturing variation through representative corner cases of components, and meets the expected defect rate with accuracy and cost efficiency.

Defect rate is a primary measure of quality and reliability of a process and therefore of critical importance in terms of cost. Its accuracy depends on corner case selection. Characteristic impedance of transmission lines rather than cross-sectional dimensions is used conventionally as a parameter in DOEs; however, this level of ab-

straction creates an ambiguity since there are many different transmission line model possibilities per impedance corner. This section proposes an novel corner case selection process based on maximum joint probability for more realistic high-speed IO channel performance and defect rate predictions.

3.2.1 Most Probable Corner (MPC)

Conventionally, corner models selection process involves user/algorithm-dependency that certain search directions are hard-coded. One approach is to skew design parameters from their nominal values towards the range limits observed in manufacturing by small amounts to move the impedance to the desired corner. A corner model is found as the impedance reaches its desired corner. Since mapping between the design parameters and impedance is not one-to-one, package and PCB models of the same impedance but with different loss and crosstalk performances will have distinct eye margin impact. This randomness involved in the corner model selection could have significant impact on defect rate predictions if a less probable model is selected. Also this leads to the lack of consistency in the process.

The proposed idea eliminates the possibility of having a pessimistic corner model which results in higher than actual defect rate. Furthermore, it provides consistency in model selection using maximum joint probability and the consistent process for multiple corner generation process (e.g. joint corner of loss, impedance, and crosstalk). This increases the accuracy of defect rate prediction which leads to cost saving through better designs or eliminating screening tests in vendors.

Consider designing a differential stripline similar to the one depicted in Figure 3.3, with 80 Ω target impedance for a typical organic package. After identifying nominal design parameters and corresponding substrate manufacturing tolerances for each parameter as described in Table 3.1, following the methodology detailed in Section 3.1,

electrical performance metric distributions can be estimated. Figure 3.9 illustrates the impedance variations caused by the uncertainty of design parameters and associated 3σ corner values. Each parameter is assumed to have a normal distribution around their nominal values.

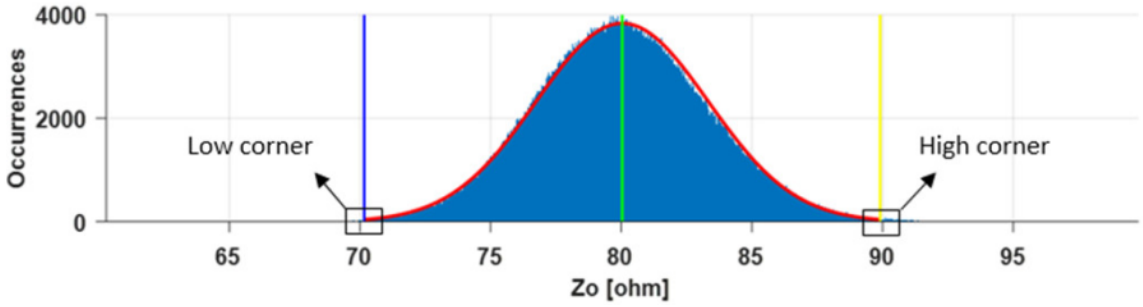

Figure 3.9: Impedance Variation of Package Differential Trace Based on Manufacturing Tolerance. Vertical Lines Show Mean and 3σ Variations (Corners).

Our objective is to find the most probable design parameters yielding the desired impedance corner. Since the same impedance can be achieved with different design rules within manufacturing tolerance, a set of design rules needs to be selected per impedance corner among many possible cases. In this example, there are more than 30,000 cases at low impedance corner (LZ) within 1% window size. Each case can be represented by one point in N-dimensional design space, where N is the number of design parameters. If the origin is defined at the nominal value for each design parameter, the closest point to the origin will have the maximum joint probability (or minimum Euclidean distance). Figure 3.10 shows sorted Euclidean distances to the origin for all cases at LZ. The case with min distance is referred to as the most probable corner (MPC), and two more cases are highlighted as least probable corner (LPC) and less probable corner (SPC) to see the impact on channel margin. Associated normalized design rules for MPC, LPC and SPC are shown in Figure 3.11. It is worth to note that SPC and LPC push some design parameters to their extreme values, whereas MPC keeps a balanced profile overall.

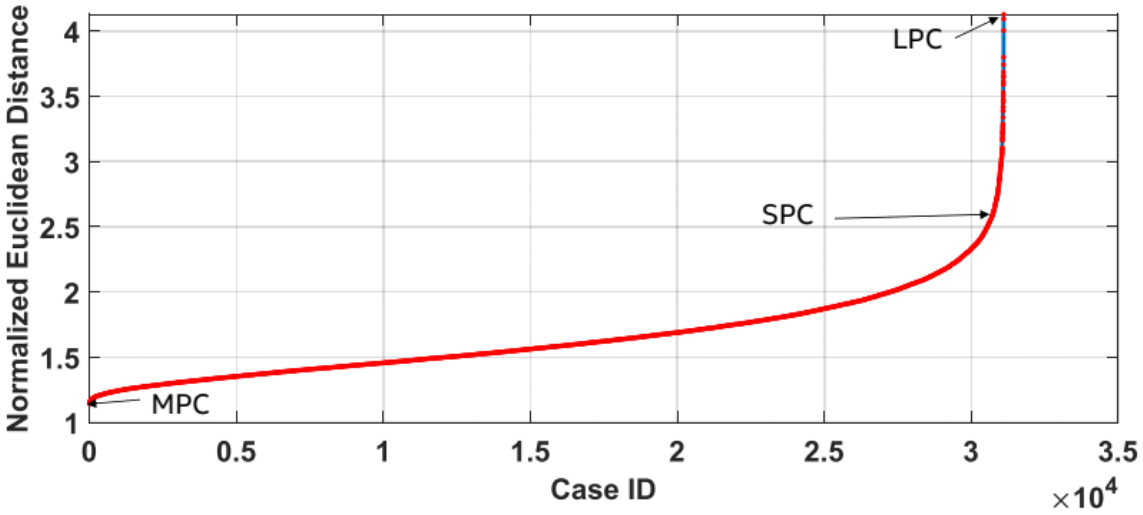

Figure 3.10: Sorted Euclidean Distance of Each Case at Low Impedance Corner.

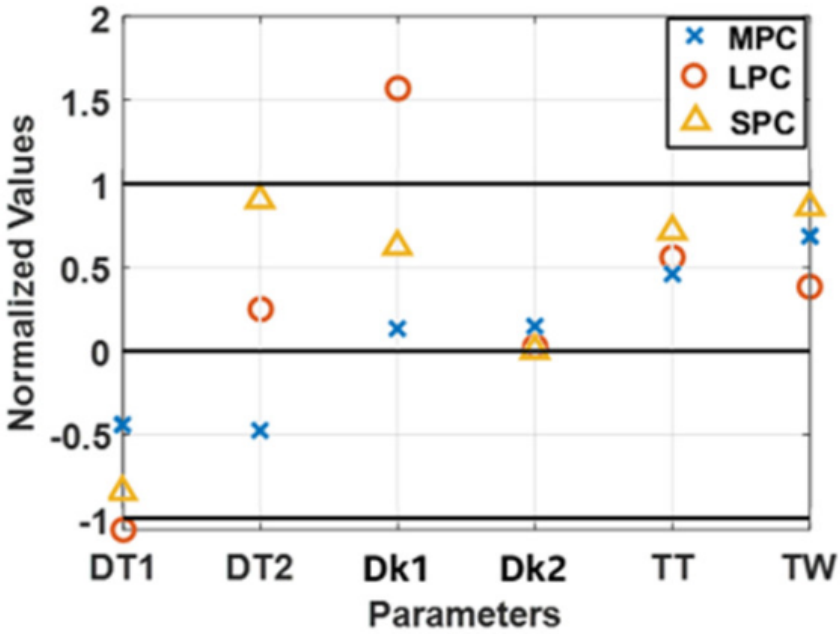

Figure 3.11: Normalized Design Rules Yielding MPC, LPC and SPC at Low Impedance Corner.

3.2.2 *Channel Margin Sensitivity*

Impact of corner model selection on channel margin is studied using 32 GT/s ultra path interconnect (UPI) topology with monolithic packages, as illustrated in Figure 3.12. MPC, SPC and LPC are utilized as the models selected for the impedance corners in the channel simulation. The Monte-Carlo simulation is performed assuming only impedance variation by package and PCB transmission lines. Table 3.3 shows the resulting eye margin summary over 1 million cases. It can be seen that eye margin is sensitive to joint probability of the corner case. The eye margin gap among the possible corner model selection cases can go up to 12% for eye height and 8% for eye width, which is significant. This as a result provides a reliable and accurate methodology for predicting and optimizing the electrical performance of high speed interconnects.

Figure 3.12: Ultra path interconnect (UPI) with a Transfer Speed of 32 GT/s.

Table 3.3: Eye Margin Summary Comparing Transmission Lines Based MPC, LPC and SPC Design Criteria. Channel Simulations Performed by Enterprise Platform SI Team.

	Eye Height (mV)	**Eye Width (ps)**
MPC	17.40	10.50
SPC	16.01	10.06
LPC	15.46	9.66

3.3 Summary

This chapter first presents an efficient and accurate modeling methodology to analyze the impact of manufacturing process variations on IO performance metrics. The proposed methodology outperforms conventional approaches such as RSM by incorporating ML based algorithms (SVR and GPR) and overcomes limitations such as the constraints on tolerance margins and the number of uncertain parameters. It is also capable of modeling highly nonlinear structures. This resulting methodology proves to be promising and can be applied to a broad range of applications involving HSIO interconnects. Second, a novel corner model selection methodology is presented. It is shown that eye margins are sensitive to the corner model selection, and it is proposed to select most probable corner via maximum joint probability for more accurate and realistic high speed IO channel performance and defect rate predictions.

Chapter 4

IMPACT OF MEASUREMENT UNCERTAINTY ON CORRELATION QUALITY

> "A theory is something nobody believes, except the person who made it.
> An experiment is something everybody believes, except the person who made it."
> *Albert Einstein*

Physical reality can be understood by the handshake of measurement and modeling, as illustrated in Figure 4.1. Comparison of measurement and modeling in high-speed interconnect validation is often the beginning (of a troubleshooting) rather than an end, since poor correlation occurs more often than is desirable considering all the challenges. Moreover this raises questions over what considered to be a good correlation. The ever-increasing demands for higher bandwidth and lower loss have only exacerbated the predictability issues of high-speed interconnect performance. Validating models against measurements of manufactured test structures requires not only accurate methodology but also understanding of the uncertainty impact. S-parameter measurements, characterization of materials, manufacturing processes, and models constructed based on measured inputs all cause uncertainty in the performance metrics of interest. Therefore, it is critical to anticipate the results with the associated uncertainty to assess the correlation quality more objectively.

This chapter investigates the reproducibility of measurements required for high-speed package interconnect validation through rigorous analysis and presents a methodology to quantify the impact of measurement uncertainty on commonly used performance metrics. In [15], among the factors affecting correlation quality; S-parameters, impact of dielectric constant (Dk), and bias in cross-section dimensional measure-

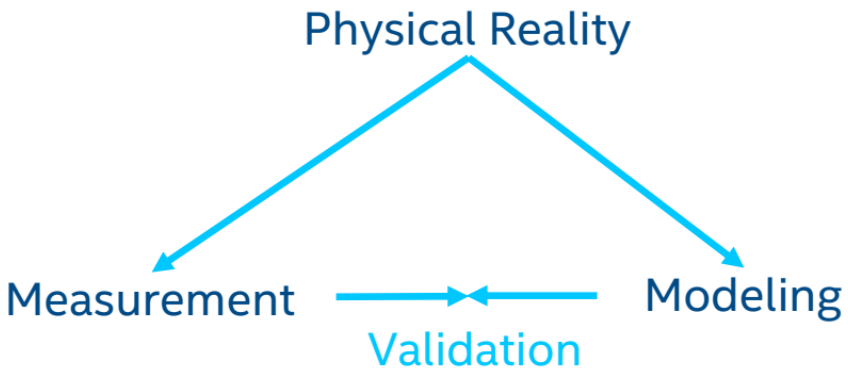

Figure 4.1: Validation Requires a Thorough Understanding of Measurement and Modeling, and the Uncertainties Around Each.

ments were prioritized and summarized. This chapter adds multiple new contributions to expand on the previous work: First, additional sources of uncertainties in the correlation flow are addressed including characterizations of bulk conductivity (σ_{bulk}), dissipation factor (Df) and dimensional variations along the routing. Second, existing S-parameter uncertainty analysis is illustrated with corresponding detailed figures of merit, and uncertainty of the dielectric constant characterization technique is investigated in detail and correlated to the dielectric sample thickness measurement uncertainty. Third, the sensitivity of dielectric and conductor models constructed based on these uncertain measured inputs are examined. Finally, new results are included for detailed analysis of measurement-to-modeling correlation. The evaluations in this chapter demonstrate that the proposed methodology is critical to decide on the goodness of the correlation quality in an objective technical fashion as opposed to using only one's empirical judgment. The methodology also helps to identify the uncertainty reduction opportunities. It is worth noting that even though the studies in this chapter are focused specifically on high-speed package interconnects, the proposed methodology can be applied to other types of interconnects as well.

The rest of this chapter is organized as follows: In Section 4.1, a statistical method

is described to quantify the measurement uncertainty for the correlation flow. Section 4.2 investigates the sensitivity of dielectric and conductor models based on the material characterization uncertainty. Section 4.3 presents test vehicle design and measurement results, and discusses the uncertainty propagation and analysis using the measurement-to-modeling correlation data. Section 4.4 investigates the impact of de-embedding on correlation quality.

4.1 Metrology Capability Analysis

All measurements are subject to uncertainty. Providing a quantitative estimate of measurement uncertainty is required to decide if the result is adequate for its intended purpose. Usefulness of any measurement is bounded by its accuracy, repeatability, and reproducibility, all of which can be assessed by metrology capability analysis (MCA) [47] as shown in Figure 4.2.

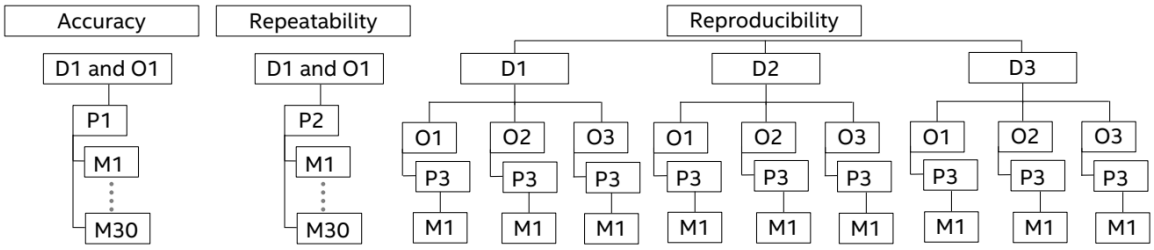

Figure 4.2: Illustrating Accuracy, Repeatability, and Reproducibility Sections of MCA. D, O, P, and M Stand for Day, Operator, Part and Measurement, Respectively.

An accuracy analysis is usually performed by repeatedly measuring National Institute of Standards and Technology (NIST) traceable standards using only one operator on one day, while minimizing the dynamics of the measurement including insertion of the device under test (DUT) and instrument calibration. This analysis provides information on how close the average value produced by an instrument comes to an accepted accuracy standard. The second part of the MCA examines the ability of a single operator to make repeated measurements on one day including the dynamics

of a measurement method such as DUT insertion and removal. Finally, the reproducibility portion of the MCA examines the closeness of the agreement between the results of measurements of the same measurand carried out under changed conditions of measurement [60]. The changed conditions include repeated DUT insertion and measurement instrument calibrations by multiple test equipment operators at different times. This process provides information on the measurement variability introduced by all temporal and spatial variations of any influence quantity.

In all cases, the assumption is made that the electrical properties of the test samples remain constant throughout the experiment. It has been shown that the environmental conditions, e.g., temperature (T) and relative humidity (RH), can have a profound adverse impact on the material properties, and loss [11, 13]. Therefore, these factors must be controlled in the MCA and considered when DUTs are characterized for model correlation.

Sources of uncertainty are often categorized as statistical or systematic. Any systematic error or bias can be sufficiently minimized by the accuracy part of the MCA through instrument calibration and consistency checks. The remaining uncertainty determined through repeatability or reproducibility are generally assumed to follow a normal distribution:

$$f(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-(x-\mu)^2/2\sigma^2} \tag{4.1}$$

where x is measurement quantity, μ and σ are expected value and standard deviation, respectively. The interval $\mu \pm 3\sigma$ encompasses approximately 99.73% of the distribution and is often referred to as the control limits.

4.1.1 S-parameter Measurements

A state-of-the-art four-port performance network analyzer (PNA) was utilized to measure the S-parameters of a differential stripline (DSL) package test structure up

to 67 GHz. DSL is frequently used in high speed systems since in many cases it provides better signal integrity performance compared to single-ended signaling, and other types of transmission lines [3, 10]. Details of the test structure are provided in Section 4.3. To assess reproducibility, three different operators collected data on three different days, calibrating the PNA before each measurement. This procedure yielded nine measurements of the DUT as shown in Figure 4.3 for differential reflection (SDD11) and transmission (SDD21) in dB scale. For these metrics, μ and σ are calculated in linear scale and then the upper and lower control limits $\mu \pm 3\sigma$ are converted back into dB scale. Although there are other choices that can be made, this method of quantification provides a clear and easy way to interpret the results.

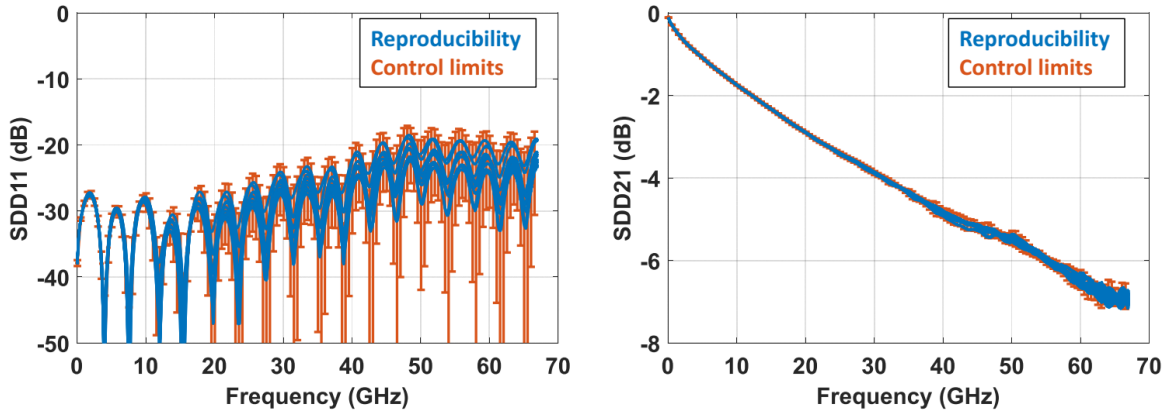

Figure 4.3: Reproducibility and Control Limits on Differential Metrics SDD11 and SDD21 in dB Scale. Measurements Performed by ECC Lab.

Reproducibility and control limits of SDD11 and SDD21 are shown in Figure 4.4 along with other linear metrics, time domain reflectometry (TDR) and phase delay (PD). Frequency domain metrics are referenced to 85 Ω and time domain metric uses $20-80\%$ rise time of 16 ps. It should be noted that the reflections are quite small (low SDD11) due to well-matched characteristic impedance of the DUT to the reference. As a result, SDD11 is observed to be a sensitive metric, since any small deviation from an already small reflection leads to high relative uncertainty. Other performance

metrics show excellent reproducibility.

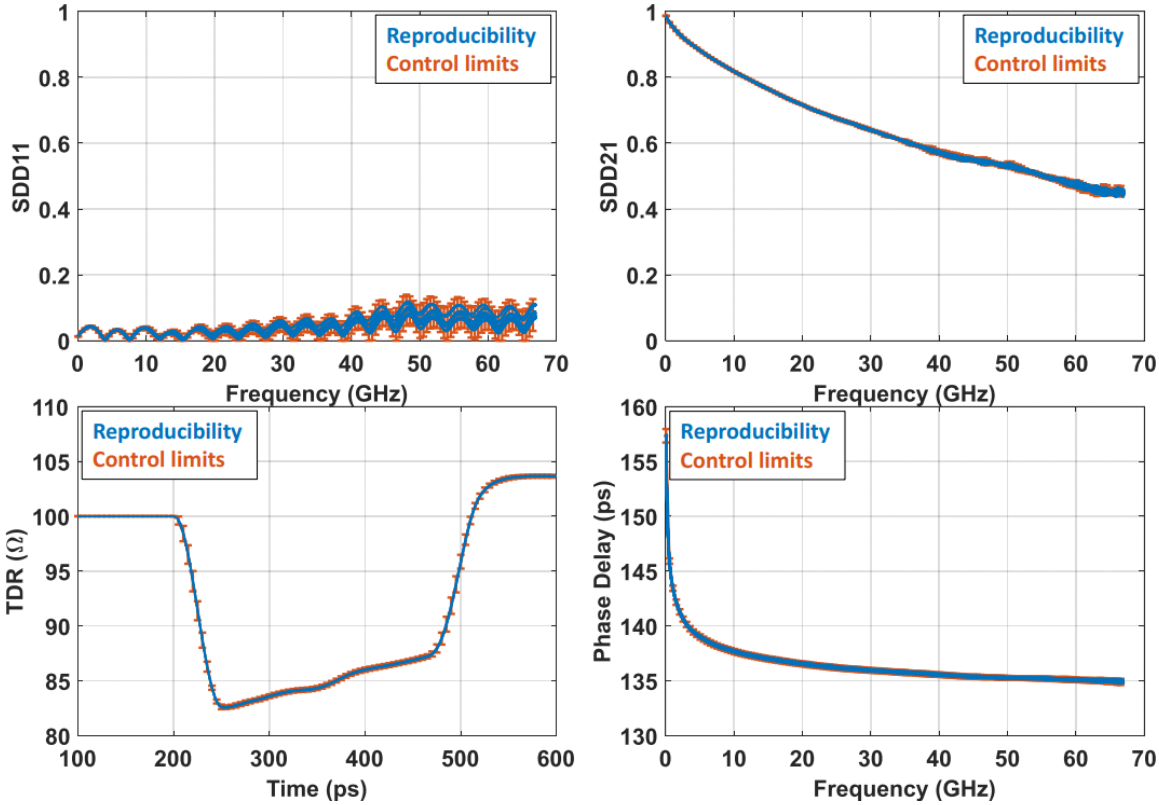

Figure 4.4: Reproducibility and Control Limits on Differential Metrics SDD11, SDD21, TDR and Phase Delay All in Linear Scale. Measurements Performed by ECC Lab.

Magnitude of μ and σ for each metric as shown in Figure 4.5 demonstrate the uncertainty of SDD11 and SDD21 increases with frequency. 3σ of SDD11 becomes comparable with its mean, whereas variation of SDD21 remains not significant compared to its mean. TDR has a small and practically constant variation over time except at the launches of the DUT. 3σ of TDR at the beginning and end of the DUT depends also on the rise time of the TDR pulse. Phase delay also has small and practically constant variation over frequency.

Relative standard variation ($3\sigma/\mu$) can be calculated for these metrics in addition to the absolute variation as shown in Figure 4.6. However, this quantity may not be useful for some performance metrics. For instance, SDD11 seems to yield higher than

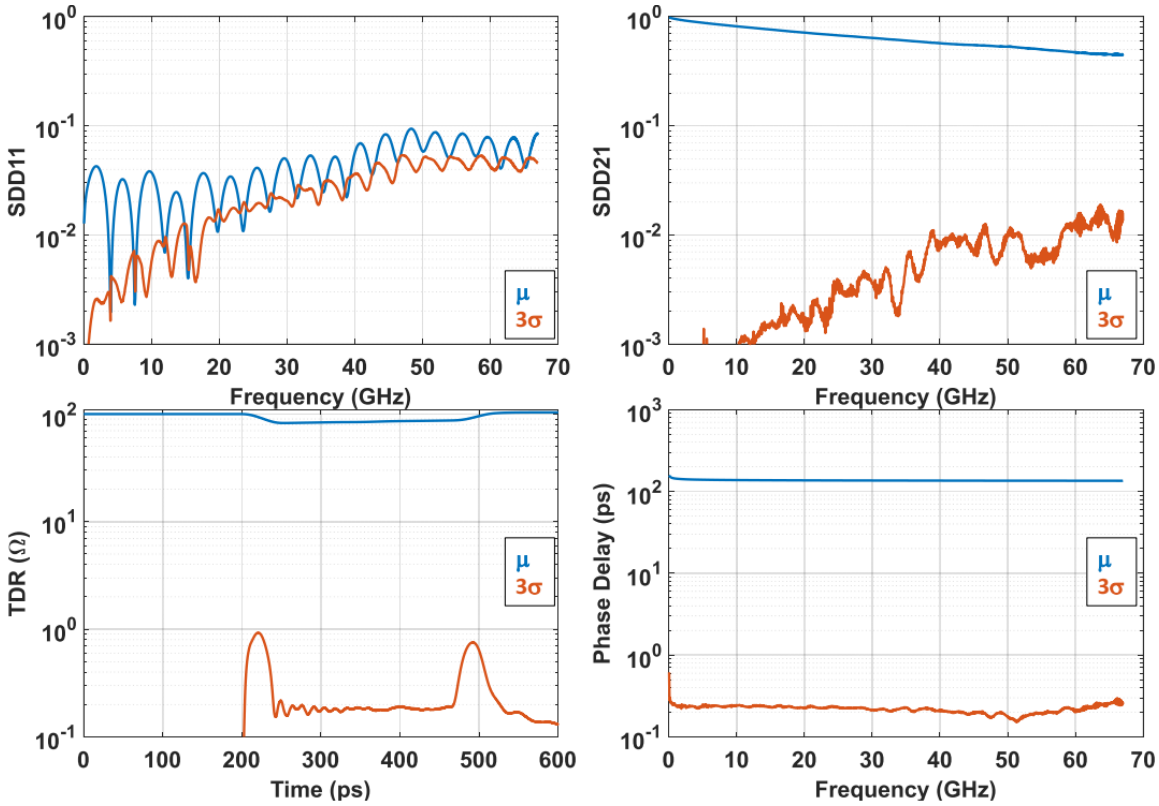

Figure 4.5: Magnitude of μ and 3σ for Each Differential Metric in Log Scale. Measurements Performed by ECC Lab.

100% relative standard variation for some frequencies, but the reason behind this is the phase shift occurring between SDD11 dips of reproducibility measurements. Absolute variation (3σ) would be a better figure of merit for SDD11. Variation in SDD21 remains under 3% up to 56 GHz and under 4% overall. Variations of TDR and PD are extremely low, i.e., less than $\sim 0.2\%$.

4.1.2 Bulk Conductivity Measurements

Copper conductivity is a key parameter for the electrical performance of electronic packages. Consequently, there have been extensive studies characterizing the bulk conductivity of the copper traces fabricated on package substrates. Although copper characteristics are well-known in literature, package conductors are not constructed

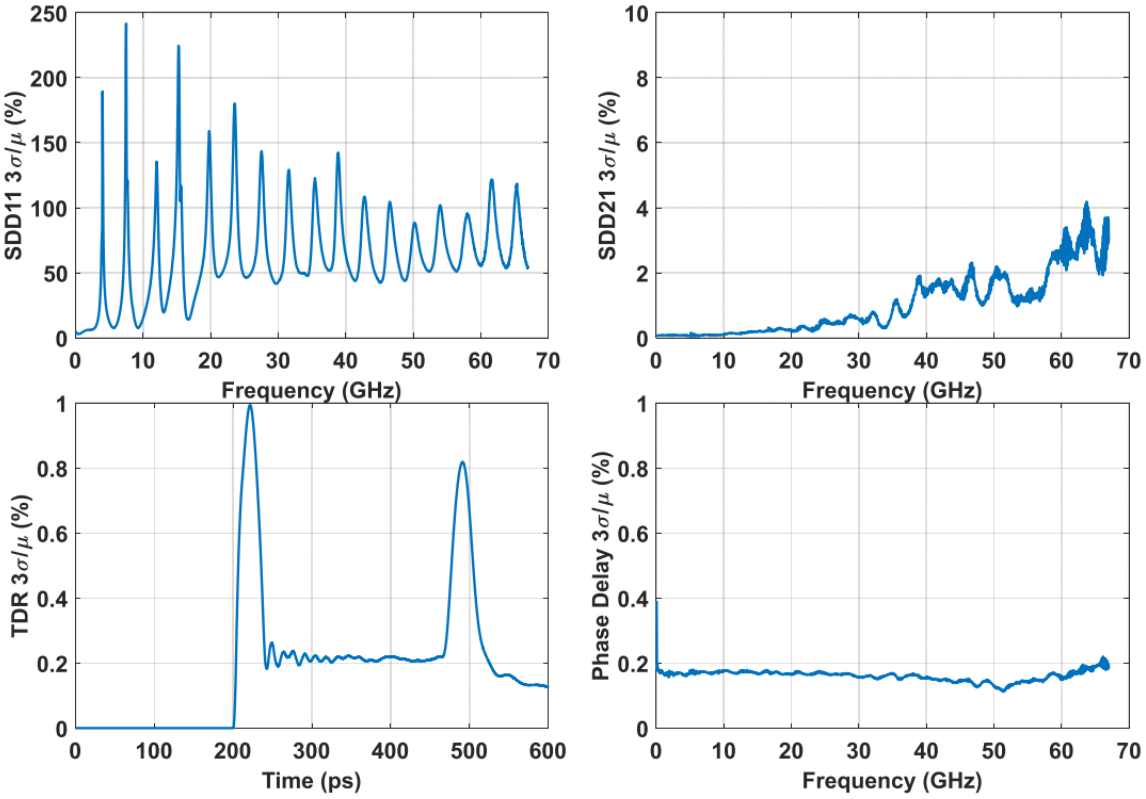

Figure 4.6: Relative Standard Variation ($3\sigma/\mu$) for Each Differential Metric. Measurements Performed by ECC Lab.

of pure copper, and hence need to be characterized empirically using low resistance 4-wire measurements. Typically, test coupons containing traces with Kelvin connections are used to provide a measured resistance value for a well-defined, wide, and long trace. A typical test structure for resistance measurements is shown in Figure 4.7. By measuring resistance (R) and knowing the cross-sectional conductor area (A) and length (l), the bulk material resistivity ρ_{DC} can be calculated as:

$$\rho_{DC} = RA/l \tag{4.2}$$

One challenge in characterizing the bulk conductivity from this resistance measurement is minimizing the impact of the variation in cross-sectional area due to fabricated trace thickness on the bulk material conductivity. For traditional bulk material measurements, a test sample is created that is dimensionally large in both

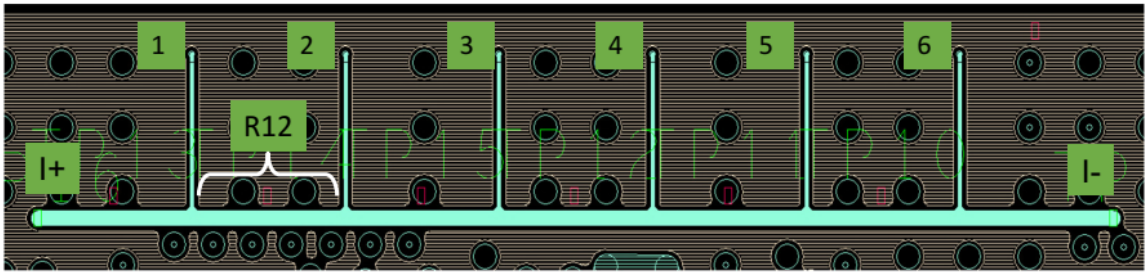

Figure 4.7: A Typical 4-wire Resistance Test Structure. Resistance Is Measured on Each Segment, e.g., R12.

cross-sectional dimensions such that the errors in conductor cross-sectional area due to surface roughness or dimensional equipment capability is a small fraction of the total area. For package traces, this approach is not generally possible as the thickness of the package metal is limited, and hence, the surface roughness is often not negligible compared to the trace thickness. To circumvent this issue, resistance measurements are collected on many structures across manufacturing lots and vendors, and those structures are then cross-sectioned at many locations to estimate the overall geometrical variation. This approach allows separation of the thickness variation from the bulk conductivity data.

Through these studies, the bulk conductivity of the copper used in the fabrication process of the structures in this chapter is known to be within $\pm 5\%$ for a given cross sectional thickness as shown in Figure 4.8 and has a measured temperature coefficient of $\alpha = 0.0043/^oC$ given the relationship

$$R = R_{ref}[1 + \alpha(T - Tref)] \tag{4.3}$$

where R_{ref} is the resistance at reference temperature T_{ref}.

4.1.3 Dielectric Permittivity Measurements

Dielectric properties of package materials can be characterized using resonators at a single frequency as a function of temperature and relative humidity. The split-post

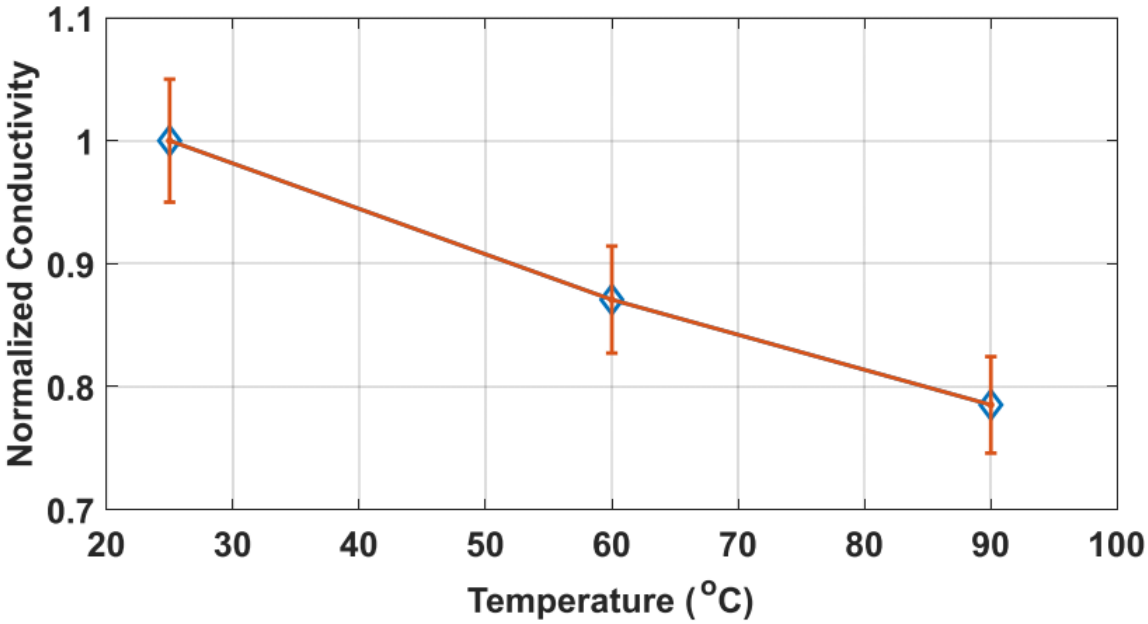

Figure 4.8: Reproducibility on Normalized Conductivity of Package Substrates. Error Bars Indicate $\pm 3\sigma$ Control Limits. Measurements Performed by ECC Lab.

dielectric resonator (SPDR) is a well-established technique for accurate measurements of the complex permittivity with quantifiable uncertainties [48]. An MCA is performed in [11] on the dielectric measurement metrology utilizing an SPDR. Reproducibility results indicate the relative standard deviation is $3\sigma/\mu \leq 2.1\%$ for Dk and $3\sigma \leq 0.001$ for Df for typical package materials. It should be emphasized that these uncertainties increase with decreasing values of dielectric loss and permittivity [48]. It is also found in the same study that the operator variation in the measurement of sample thickness (required to extract Dk from SPDR) is a key limiter to reproducibility. This is due to the direct correlation of errors in Dk to the relative errors in thickness measurements. Df uncertainty is predominantly limited by the Q-factor uncertainties of the resonator [48] and relatively insensitive to the sample thickness measurement uncertainty.

In [15], a separate MCA is performed on both typical package dielectric samples and a NIST traceable thickness gauge block using a high-performance micrometer. A

typical package dielectric sample is shown in Figure 4.9(a). Three different operators measured two samples with different thicknesses on three different days. The variations from mean value are shown in Figure 4.9(b). The thickness variations show small dependence on the mean considering one sample is more than twice as thick. As a result, reproducibility is expressed in absolute terms, i.e., $3\sigma \approx 4$ um. This result also indicates that the thicker samples would yield smaller relative variation in thickness, and hence smaller relative variation in extracted Dk. Gauge block measurements from this study demonstrate that the micrometer accuracy, i.e., average value of operator results compared to the traceable value, was significantly better than 4 um. Hence, it is only necessary to consider this value when computing thickness reproducibility effects.

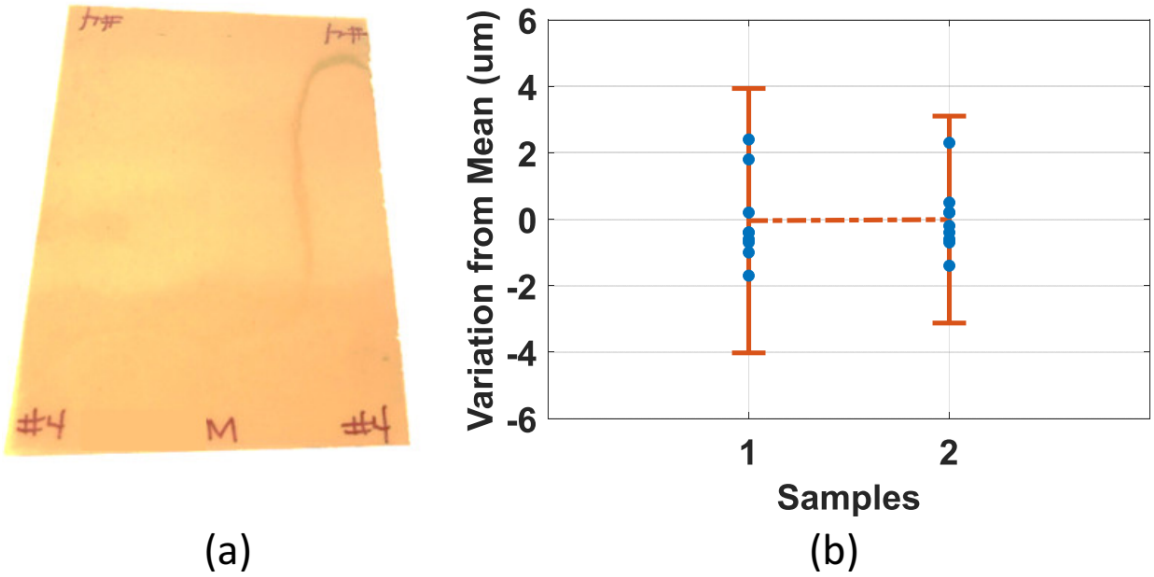

Figure 4.9: (a) A Typical Dielectric Sample Received from Vendors, and (b) Thickness Measurement Reproducibility Results. Error Bars Indicate $\pm 3\sigma$ Control Limits. Measurements Performed by ECC Lab.

Measurement dynamics and sample thickness variation lead to a combined uncertainty of $3\sigma/\mu \approx 3\%$ in Dk. This result implies that any simulation should be performed at both the upper and lower bounds from the dielectric characterization

to bound the expected impact of the measurement variability. In addition to uncertainty introduced by the sample thickness measurement uncertainty, the dielectric resonator hardware also introduces additional uncertainty into the dielectric material characterization because of imperfections in its construction. To address this issue, the SPDR used for characterizing the package buildup materials is used to measure a NIST traceable material sample [61]. This sample is approximately 750 um thick which allowed the error introduced by thickness uncertainty of the reference material to be minimized. This measurement was performed by three operators on three days and the average result compared to the NIST specified value. The result fell withing the $\pm 0.16\%$ uncertainty specified by NIST for the test material. Because this uncertainty is significantly lower than that introduced by the sample thickness assessment ($\sim 3\%$), the error introduced by SPDR is determined to be negligible compared to the error introduced by the thickness uncertainty.

4.1.4 Cross-section Dimensional Measurements

High fidelity geometrical representation of a transmission line can be achieved by cross-sectioning and is essential for a good correlation. Cross-section dimensional features become more critical because today's on-package high-speed interconnect loss is largely dominated by conductors due to thinner substrate and low loss dielectric materials [12]. Cross-section picture of a typical package trace along with dimensional features are shown in Figure 4.10(a).

An MCA was performed on a cross-section dimensional measurement utilizing a visualization software. Three different operators measured four separate dimensional features from the same cross-section picture on three different days to investigate reproducibility. The features are not measured at a single point, but averaged over many points. This is achieved by selecting an area around the feature of interest.

Then, the boundary between dielectric and conductor is auto-traced by the visualization software within that area, and the average dimension is provided.

The variation of each dimensional feature from its mean value is shown in Figure 4.10(b). The main source for uncertainty is the lack of clarity on where the features start and end due to manufacturing process variations and surface roughness. For larger design rules, this ambiguity might cause a relatively small uncertainty; however, for today's high-density package design rules, the resulting uncertainty is not negligible. Reproducibility results show that 3σ control limits for each dimensional feature can be as large as 0.7 um.

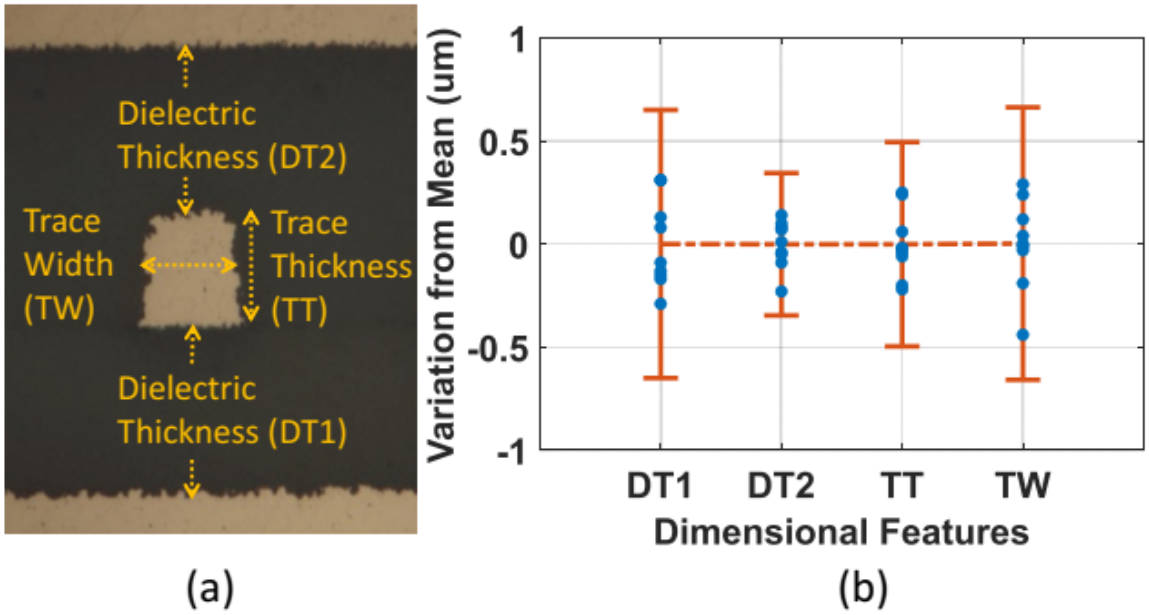

Figure 4.10: (a) Cross-section Picture of a Typical Package Trace with Dimensional Features Illustrated, and (b) Cross-section Dimensional Measurement Reproducibility Results. Error Bars Indicate $\pm 3\sigma$ Control Limits. Measurements Performed by ECC Lab.

It is worth noting that dimensional variations between differential traces and variations along the routing are independent from the MCA and investigated in Section 4.3.2 during measurement-to-modeling correlation. For the MCA, we select a representative case to quantify the metrology uncertainty. This manifests the inher-

ent uncertainty while determining the dimensions from a cross-section picture due to the sources of uncertainty highlighted in the introduction.

4.2 Dielectric and Conductor Models

The accuracy in the modeling of high-speed interconnect performance depends upon the accurate characterization of broadband dielectric materials and conductors with surface roughness. Proper modeling of physical structures requires broadband causal models satisfying Kramers-Kronig relationship. This section delves into the sensitivity of dielectric and conductor models to the parameter uncertainty of inputs.

4.2.1 Wideband Debye Model

Despite several existing causal broadband dielectric models, the Djordjevic-Sarkar (DS) model [45] is the one commonly used for materials in printed circuit boards and packages. DS model can only handle dielectric materials with lower Df than a specific threshold. Considering the model was initially developed for FR-4, the majority of today's package materials will meet this criterion. DS model uses an infinite distribution of poles to model the frequency response based on a single measurement:

$$\epsilon(f) = \epsilon_\infty + \frac{\Delta\epsilon}{\ln(f_B/f_A)} \ln \frac{f_B + jf}{f_A + jf} \tag{4.4}$$

where ϵ_∞ is the permittivity at very high frequency, $\Delta\epsilon$ is the magnitude of dispersion $\Delta\epsilon = \epsilon_\infty - \epsilon_{DC}$, if the DC permittivity is known, and f_A and f_B are the lower and upper frequency poles respectively. With the real permittivity ϵ_1, and loss tangent $tan\delta_1$ at the measurement frequency f_1, the lower pole can be expressed as:

$$f_A = \frac{f_B}{e^{\Delta\epsilon/K}} \text{ where } K = \frac{\Delta\epsilon}{\ln(f_B/f_A)} = \frac{\epsilon_1 tan\delta_1}{\arctan(f_B/f_A)} \tag{4.5}$$

The accuracy of the model at high frequencies depends on the upper pole f_B, which could be selected based on high frequency dielectric material characterization as sug-

gested by prior research [46].

To better understand the dependence of DS model to the measured ϵ_1 and $tan\delta_1$ at f_1, we can calculate the asymptotes on log-linear portions:

$$\epsilon(f) = \epsilon_1(1 + 2/\pi tan\delta_1 \ln(f_1/f)) \tag{4.6}$$

$$tan\delta(f) = tan\delta_1(1 + 2/\pi tan\delta_1 \ln(f_1/f)) \tag{4.7}$$

This indicates that any variation on $tan\delta_1$ affects the asymptote of relative permittivity, whereas any variation on ϵ_1 does not affect the asymptote of loss tangent.

For a typical package build up material, pairs of ϵ_1 and $tan\delta_1$ are generated based on reproducibility through a Monte Carlo analysis as shown in Figure 4.11. Each pair in this set are used to calculate a DS model. Resulting Dk and Df as a function of frequency are illustrated in 4.12.

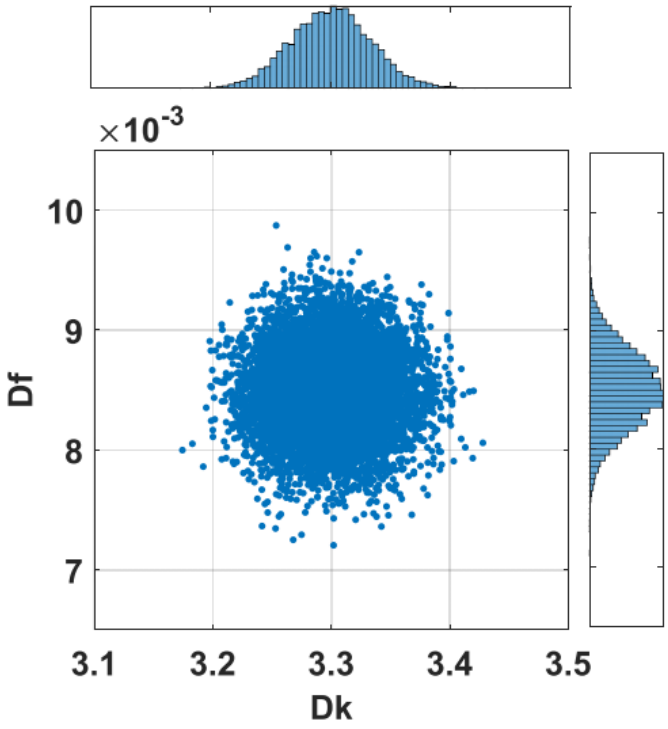

Figure 4.11: ϵ_1 and $tan\delta_1$ Pairs Obtained by a Monte Carlo Analysis Based on 3σ Control Limits from Reproducibility for a Typical Package Material.

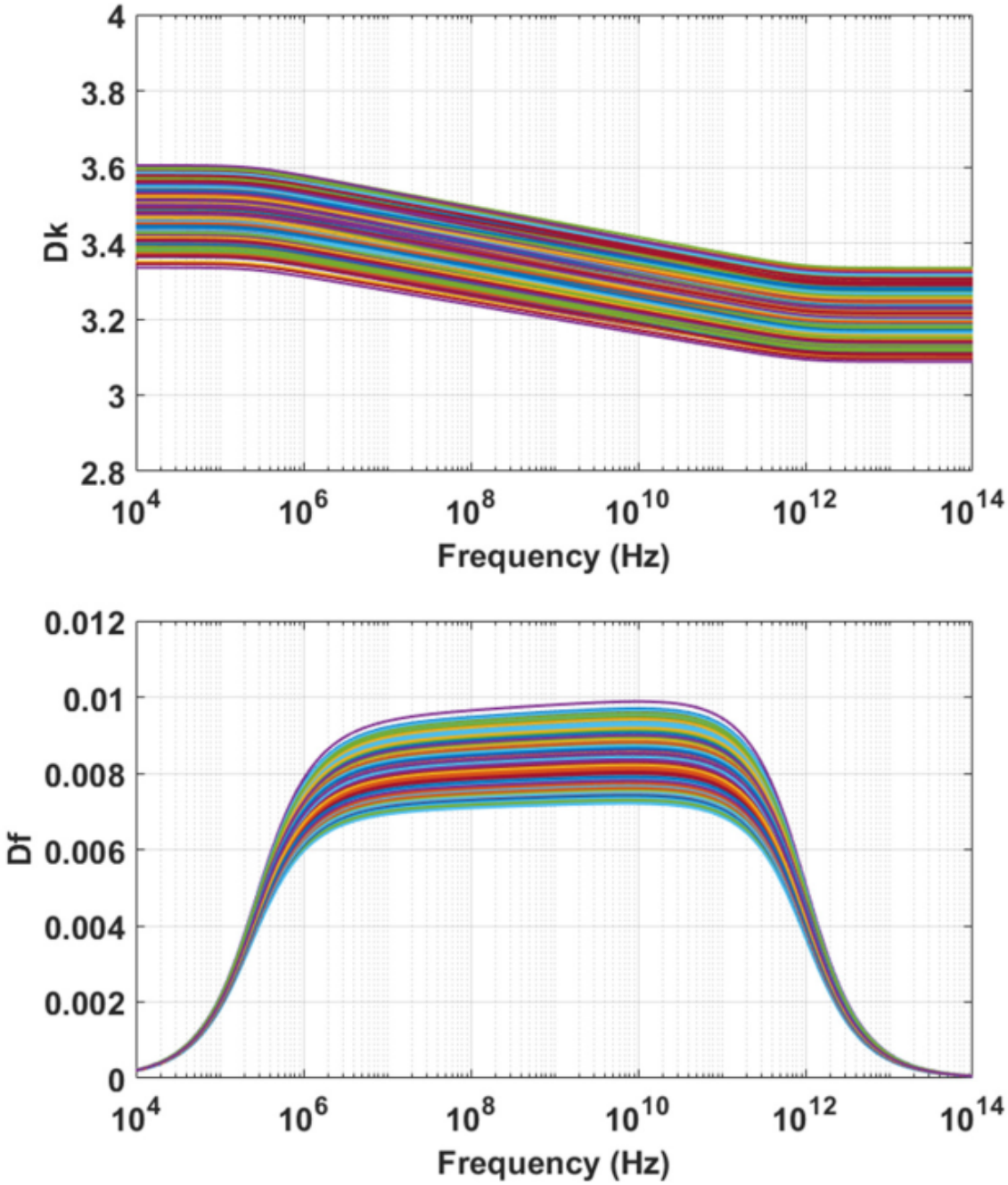

Figure 4.12: DS Model Illustrating the Variation in Broadband Response Based on Measurement Uncertainty.

4.2.2 *Effective Conductivity Model*

Surface roughness characterization and representation has been one of the challenging aspects of high-speed interconnect modeling. Many different approaches for roughness modeling exist in literature [20–26], and most of them utilize a correction factor (K) as a function of skin depth (δ). Despite dissimilarity, correction factors of existing common approaches can be written in a unified form [51].

Surface roughness effect can be incorporated using either frequency dependent effective material properties or a surface impedance boundary condition. The former is convenient due to being readily applicable to any field solver without an increase in simulation time. Moreover, it allows to generate material libraries for conductors with different roughening processes for ease of use. The skin effect in rough conductor surfaces causes higher resistance as well as internal inductance, and manifests itself in not only higher loss but increased phase delay to maintain causality [49, 50]. Causal versions of many existing roughness models have been derived [50], which can be critical for transient analysis. Roughness impact can be expressed with one frequency-dependent complex or two real effective material properties [25].

In this section, we present sensitivity analysis performed utilizing Huray's *snowball* model. Correction factor for causal Huray-Bracken model can be expressed as follows:

$$K_{HB}(\delta, sr, a) = 1 + \frac{3}{2} sr \left(1 + (1 - j) \frac{\delta}{2a} \right)^{-1} \tag{4.8}$$

where sr and a are the surface ratio and effective radius of spheres, respectively. Roughness impact on conductor loss can be calculated with the real part of K_{HB} and real effective conductivity as follows:

$$K_H(\delta, sr, a) = 1 + \frac{3}{2} sr \left(1 + \frac{\delta}{a} + \frac{\delta^2}{2a^2} \right)^{-1} \tag{4.9}$$

$$\sigma_{\text{eff}} = \sigma_{\text{bulk}} / K_H^2 \text{ where } \delta = 1/\sqrt{\pi f \mu_r \mu_0 \sigma_{\text{bulk}}} \tag{4.10}$$

As shown in Section 4.1.2, bulk conductivity measurement uncertainty is within ±5%. The impact of this uncertainty on correction factor and effective conductivity is shown in Figure 4.13. Correction factor uses the same sr and a, yet its frequency response is affected due to its dependence to bulk conductivity through skin depth. Propagated uncertainty to K_H remains under 1%. It should be noted that K_H converges to $1 + 3/2sr$ as $\delta \ll a$ at high enough frequencies, which reduces K_H uncertainty due to bulk conductivity measurement. Effective conductivity uncertainty is proportional to bulk conductivity uncertainty whenever K_H is constant, which happens either at low frequencies ($K_H \sim 1$) or high frequencies ($K_H \sim 1 + 3/2sr$). In mid-frequency range σ_{eff} uncertainty remains under 5%.

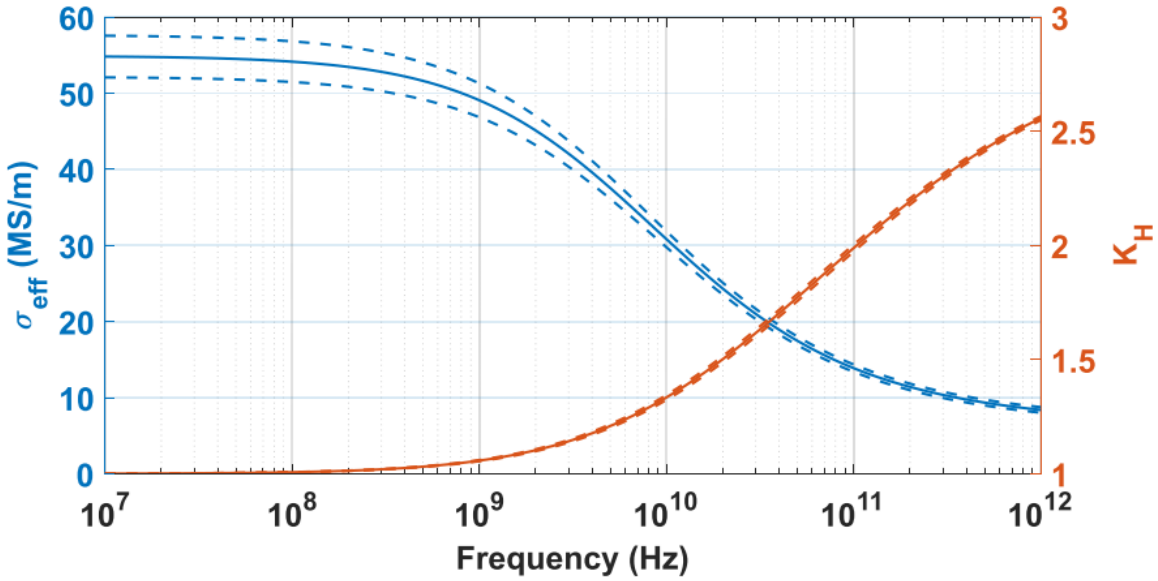

Figure 4.13: The Impact of ±5% Bulk Conductivity Variation on Correction Factor and Effective Conductivity. Solid and Dash Curves Indicate Nominal and $\pm 3\sigma$ Control Limits, Respectively.

It is obvious that K_H is more sensitive to sr and a compared to σ_{bulk}. Although Huray model input parameters have physical definitions, practically, effective parameters are used in modeling since it is very challenging to reliably extract these parameters from an actual package copper surface. Some of the challenges of parameter

extraction from the images of copper surface include but are not limited to the robustness of roughness measurement tools (either contact or non-contact based), process variations, limitations of commonly used roughness parameters to represent different roughening processes. For Huray model, surface ratio indicates how much surface area is increased after roughening process, which is relatively easy to calculate; however, sphere radius is not straightforward to extract since certain assumptions have to be made on the sphere arrangements to represent the copper surface. This challenge is exacerbated by the complex features formed on the actual surface after the roughening process. As a result, making many assumptions just to extract the sphere radius from the actual surface makes the process non-ideal and more alike to model synthesis.

Effective parameters are obtained through model synthesis, which is accomplished by fitting parameters so that a good measurement-to-modeling correlation is achieved. We assume that the best fit is achieved when the geometric distances from the S-parameter measurements to the fitting curve are minimized in the least squares sense. Even though uniqueness cannot be guaranteed, since sr and a values impact different frequency regions in the S-parameter data, practically, we expect the impact of non-uniqueness to be small. To illustrate the model sensitivity, it is assumed that parameters (sr and a) have 30% uncertainty, and the individual impacts on K_H and σ_{eff} are shown in Figure 4.14.

If the impact of combined uncertainty is considered as shown in Figure 4.15, K_H uncertainty remains under 18% and σ_{eff} uncertainty remains under 40%. Since the uncertainty in the surface roughness could not be reliably measured, Figs. 4.14 and 4.15 are provided merely as examples to show the sensitivity to surface roughness modeling parameters. Consequently, the impact of the uncertainty caused by surface roughness is not currently included in the results in Section 4.3.

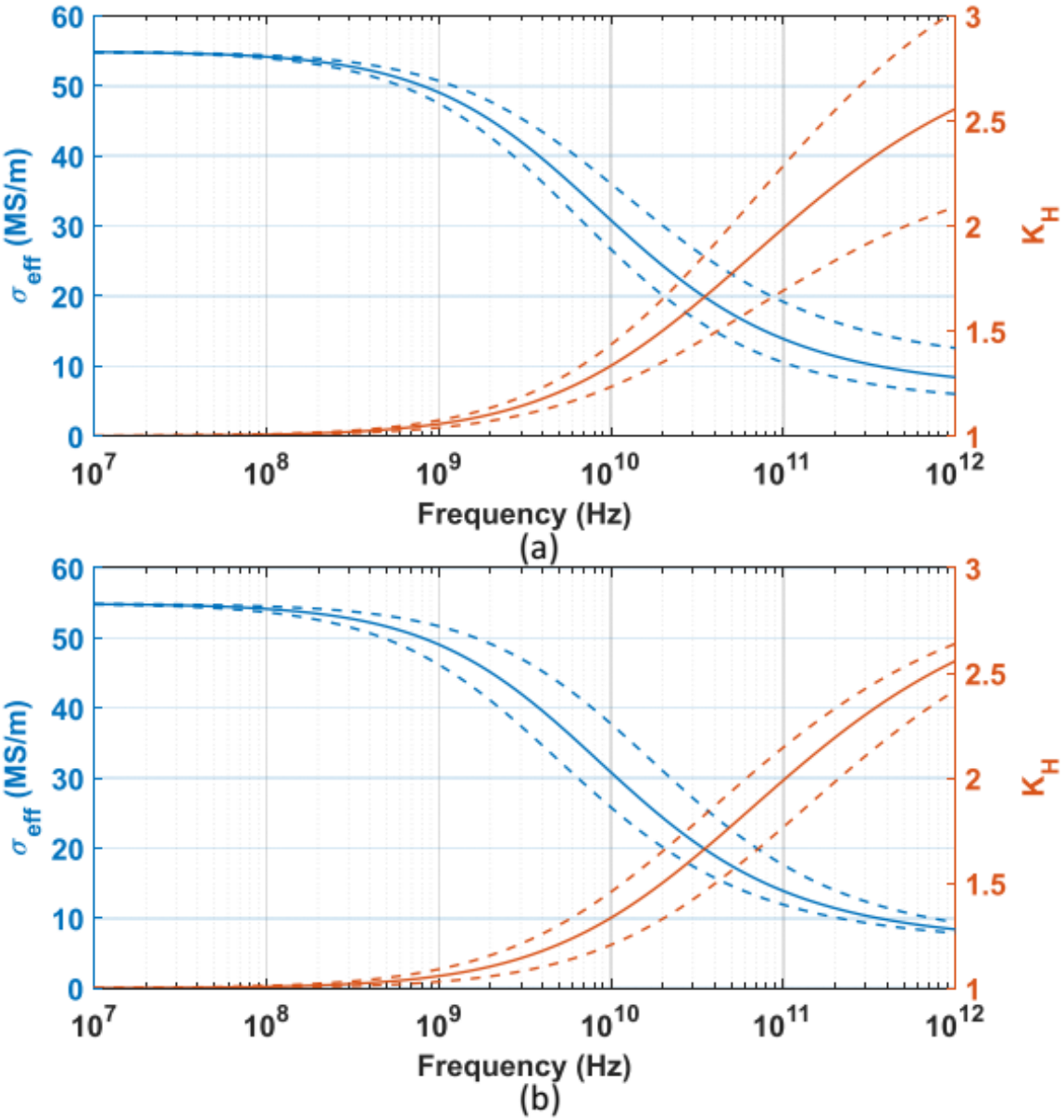

Figure 4.14: The Impact of 30% Assumed Variation of (a) *sr* Only, and (b) *a* Only, on Correction Factor and Effective Conductivity. Solid and Dash Curves Indicate Nominal and $\pm 3\sigma$ Control Limits, Respectively.

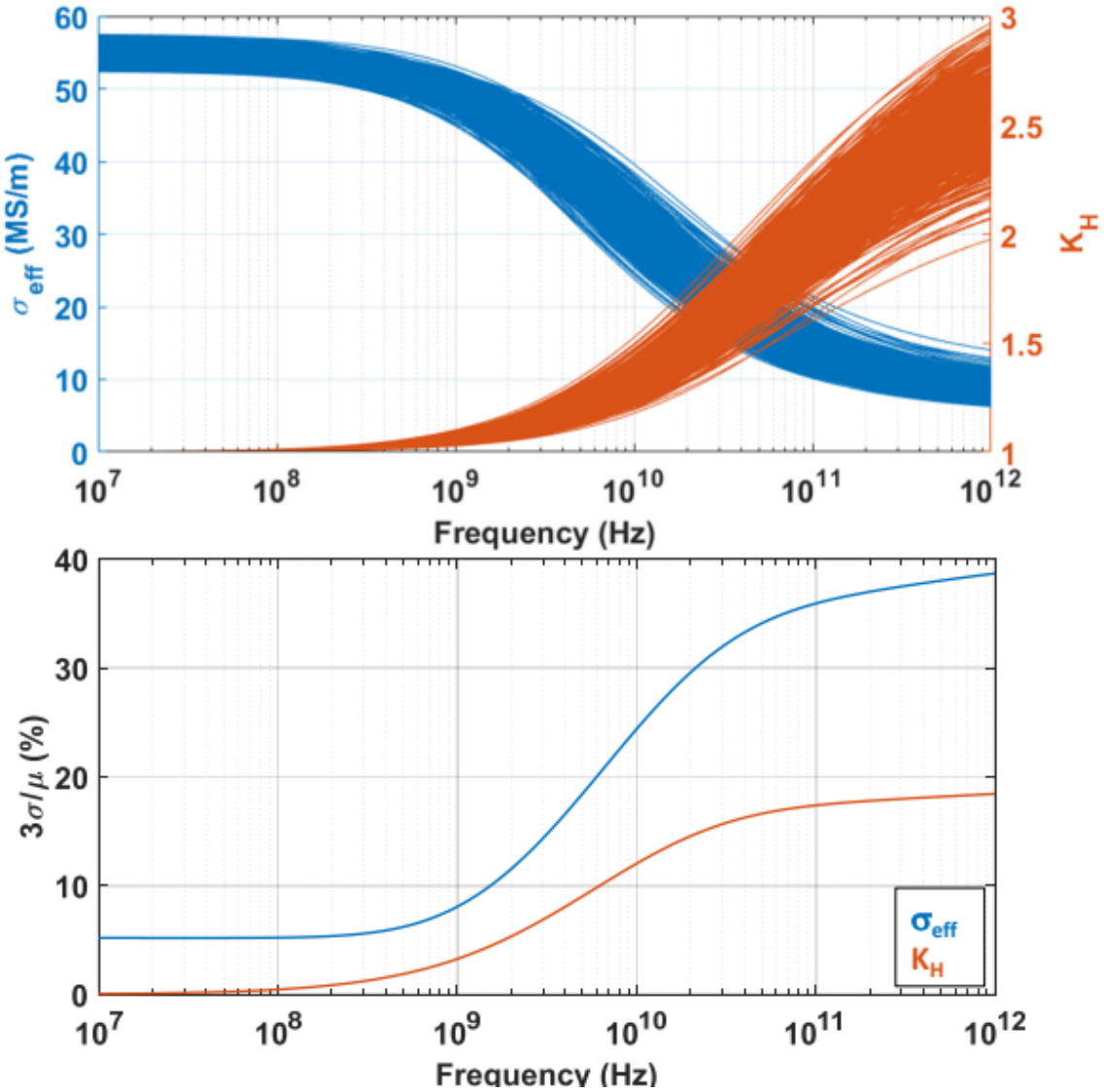

Figure 4.15: The Impact of Combined Uncertainty (σ_{Bulk}, sr, and a) on Correction Factor and Effective Conductivity.

4.3 Results

A package test vehicle was designed and manufactured including a DSL routed on the layer below the surface with a length of 20 mm as shown in Figure 4.16. The length was chosen based on certain physical constraints and the amount of real estate available in a typical package. The purpose is to have it practically long enough to clearly observe various characteristics of a transmission line. Even though the methodology should be generic enough to apply to other lengths as well, confirmation of this is a part of future work associated with de-embedding.

The measurement is performed with probes landing on the surface pads of the test structure. Pads are connected to the main routing on the layer below the surface through micro-vias and transition traces. Dielectric and conductor material characterization is completed for the material and surface roughness process bundle used in this test vehicle as described in Section 4.1. For the manufactured test vehicles, PNA and cross-section dimensional measurements are performed.

4.3.1 S-parameter Measurements

PNA measurements were performed after prebaking to ensure no moisture remained, and on a temperature chuck to achieve the controlled temperature condition to represent the typical package use condition [13]. The quality of measured S-parameters is evaluated with IEEE standardized metrics of passivity and reciprocity as shown in Table 4.1.

4.3.2 Cross-section Dimensional Measurements

Measured parts were then cross-sectioned to get the accurate dimensional characteristics. Multiple cut locations were selected to quantify dimensional variations

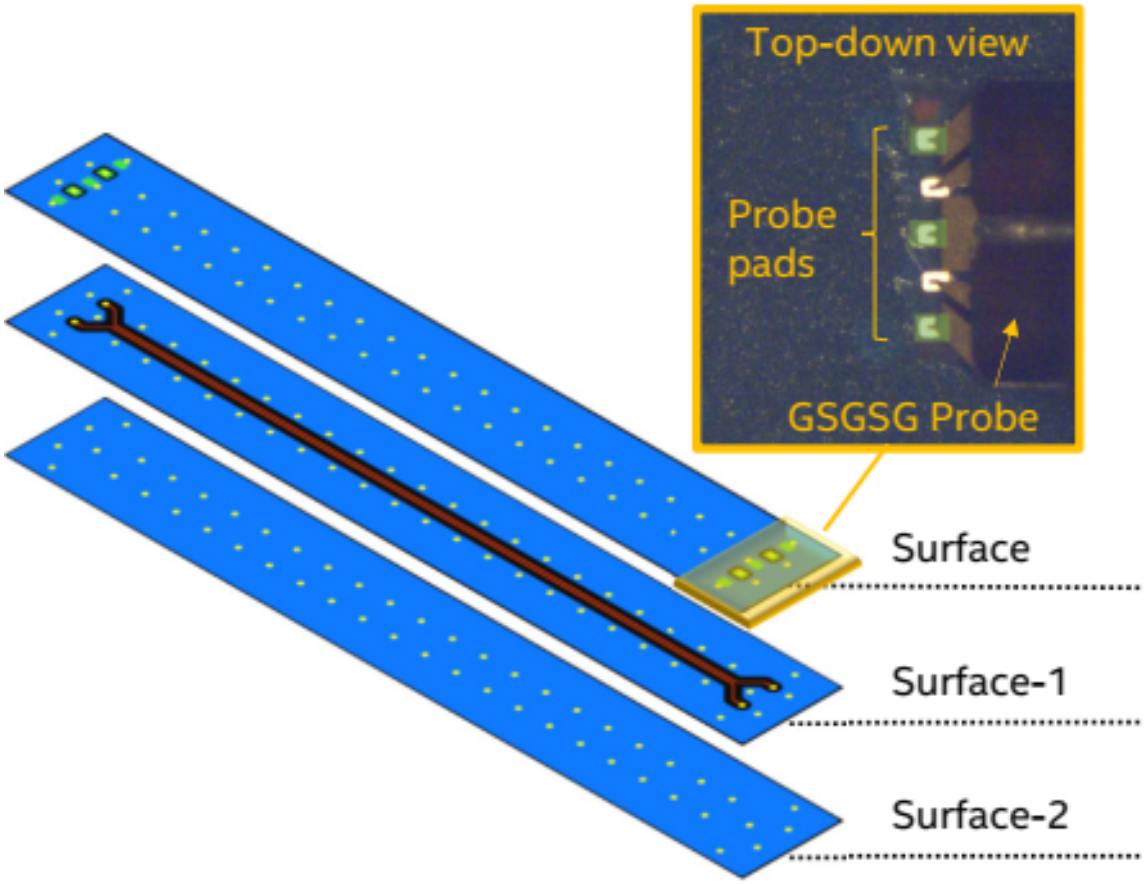

Figure 4.16: Differential Stripline Test Structure Illustrated by Layer with Main Routing, Transition, and Probe Landing Pads. Zoomed-in Picture Illustrates Probe Landing on Surface Pads from a Top-down Perspective.

Table 4.1: Quality of Measured S-parameters.

Design	Passivity	Reciprocity
A	100%	98.7%
B	100%	98.8%

along the routing. Figure 4.17 shows model cross-section, cut locations and cross-section pictures of DSL per location. It should be stressed that advanced processes used in high-density packages to enable fine line/spacing lead to considerably less etching factor than other processes used for coarser design rules. In a separate study performed to investigate the impact of etching factor in high density packages, results have demonstrated that rectangular traces as shown in the model cross-section, i.e., zero etching factor, yield very similar electrical performance compared to the models with expected etching factor for the packaging technology used here.

Dimensional measurements were taken on each picture in Figure 4.17. Mean values are listed in Table 4.2 and their variations from mean are summarized in Figure 4.18. It is observed that the 3σ variation remains less than 1.5 um for each design parameter. This uncertainty (σ_z) must be combined with the metrology uncertainty (σ_{xy}) presented in Section 4.1.4. By assuming these two uncertainty components are independent, combined uncertainty (σ_c) can be calculated with summation in quadrature [17]:

$$\sigma_c = \sqrt{\sigma_{xy}^2 + \sigma_z^2} \tag{4.11}$$

Table 4.2: Dimensional Mean Values Measured for Each Design Rule. All Units Are in um. Measurements Performed by ECC Lab.

Design	DT1	DT2	TT	TW	TS
A	25.73	25.60	16.99	15.37	34.91
B	25.82	26.56	14.24	14.69	36.50

For each design rule, combined uncertainty is used in modeling next, to account for cross-section dimensional uncertainty.

4.3.3 *Measurement-to-Modeling Correlation*

Modeling results were generated using dielectric and conductor material properties and surface roughness characterized at the same use condition along with cross-section dimensions. A commercial 3D simulation tool was utilized with the mean values of all measured inputs. Each component of uncertainty was propagated and overall uncertainty in standard deviation for each performance metric was quantified

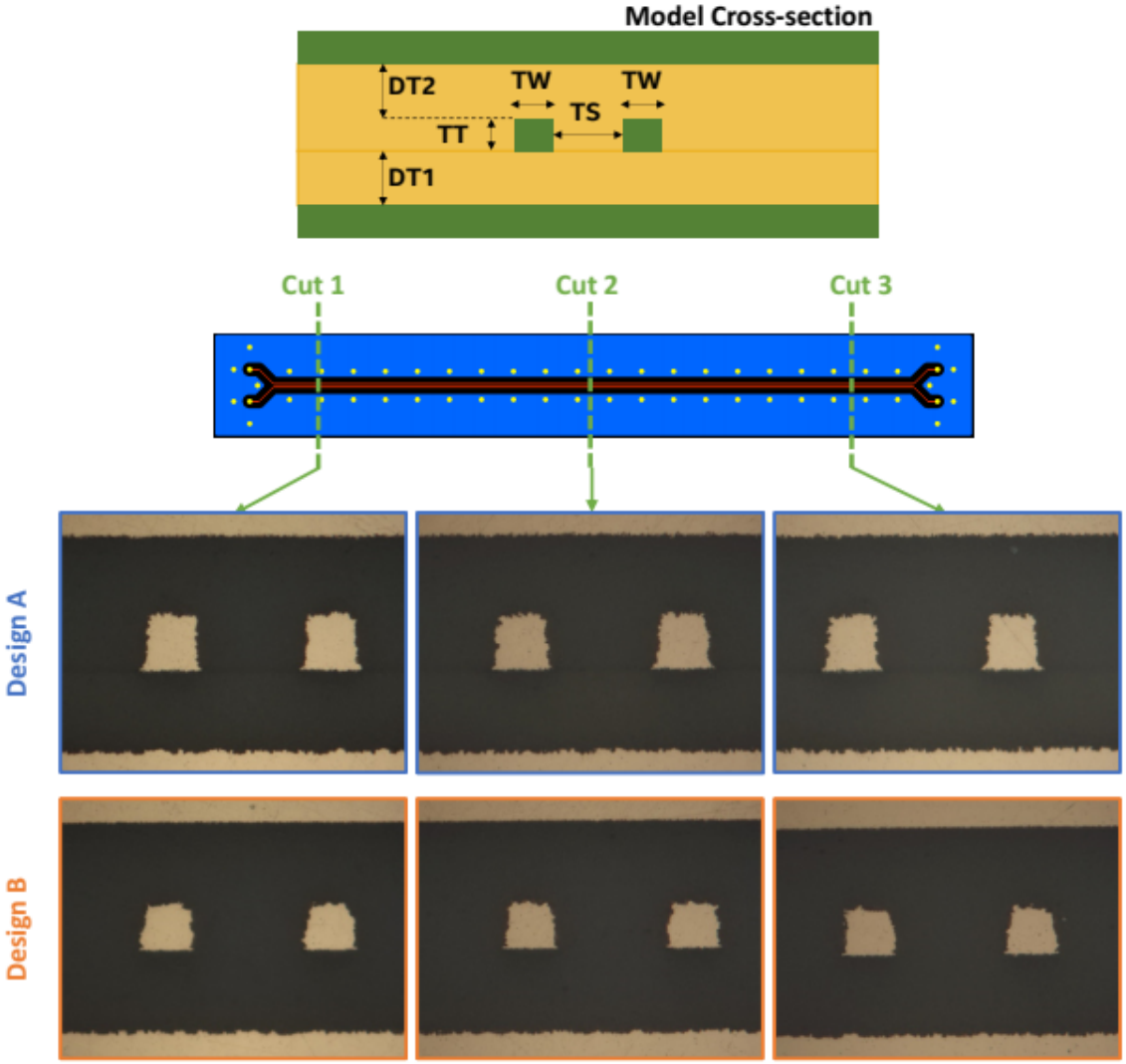

Figure 4.17: Model Cross-section, Cut Locations and Cross-section Pictures of DSL Are Shown. Cross-section Measurements Performed by ECC Lab.

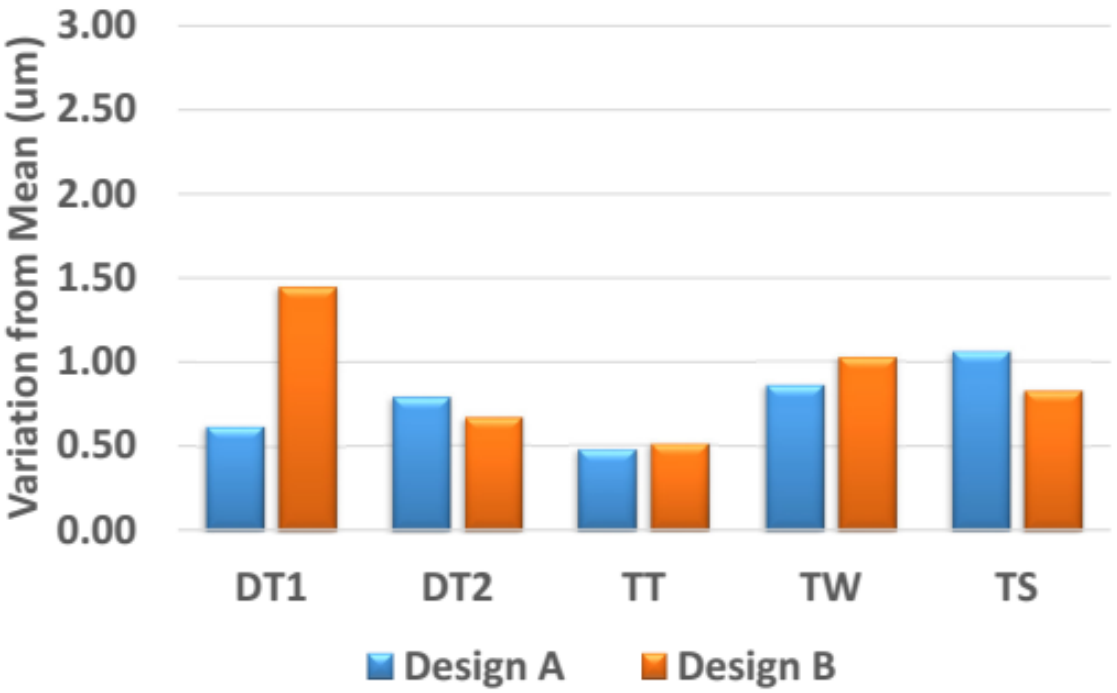

Figure 4.18: Dimensional 3σ Variations from Mean for Each Design Rule. Measurements Performed by ECC Lab.

using response surface methodology and statistical design of experiments [57]. Subsequently, a Monte Carlo analysis was performed to understand the impact of the variabilities on the modeling results.

Measurement-to-modeling correlation results of design A and B are shown at typical use condition for packages in Figs. 4.19 and 4.20, respectively. Simple visual assessment of measurement and modeling for design A (illustrated by blue and orange solid lines, respectively) indicate good correlation between measurement and modeling for all performance metrics except for the phase delay. However, a comparison of measured and modeled results without any sensitivity analysis is insufficient to assess the goodness of the correlation quality.

Propagation of the measurement uncertainty is required for an objective evaluation. Measurement uncertainty from Section 4.1.1 was incorporated into measured S-parameter data as a shaded area, i.e., measurement range. Measurement uncer-

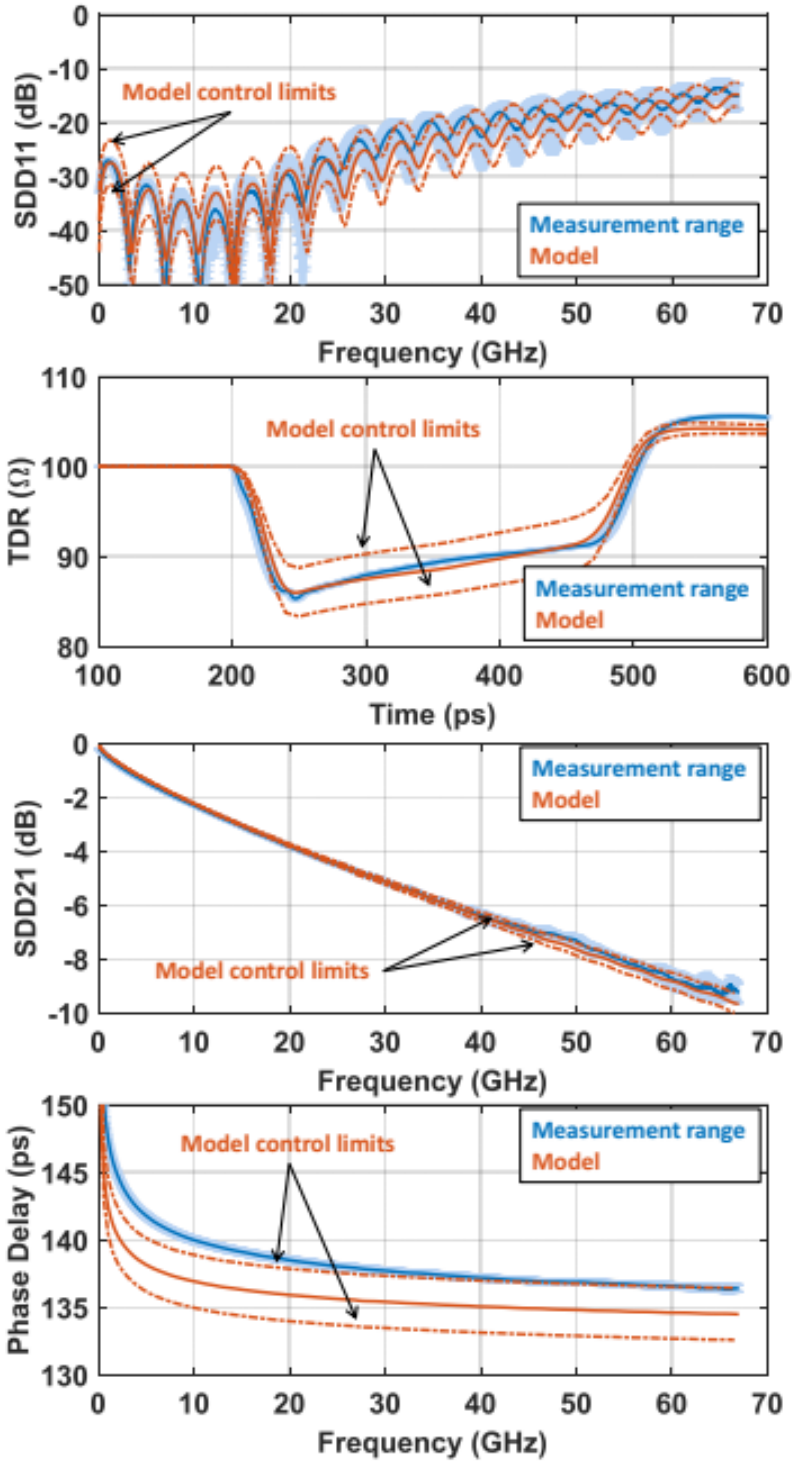

Figure 4.19: Measurement-to-modeling Correlation at Typical Package Use Condition for Design A. Uncertainty Incorporated into Measurement (Shaded) and Propagated to Modeling Outcome (Dash). Measurements Performed by ECC Lab.

tainty of bulk conductivity from Section 4.1.2, measurement uncertainty of Dk and Df from Section 4.1.3, and combined measurement uncertainty of cross-section dimensions from Sections 4.1.4 and 4.3.2 were incorporated into modeling data as model control limits. As can be seen, most of the correlation gap in the phase delay is accounted for. This result implies that the phase delay can also be considered to have a good correlation for $f > 30$ GHz.

Design B shows more dimensional variation along the routing than design A, as presented in Section 4.3.2. This manifests itself as a measured TDR deviation from modeled TDR but is enveloped by model control limits. Furthermore, design B measured SDD21 is enveloped by model control limits only for $f < 45$ GHz. The discrepancy for $f > 45$ GHz is expected to be caused by surface roughness variations, indicating the need for a reliable and accurate surface roughness measurement metrology.

As can be seen from Figs. 4.19 and 4.20, for certain frequency ranges and time instances, model control limits do not fully encompass the measurements. Before addressing possible reasons behind this, it is worth noting that adding uncertainties to the measurement-to-modeling correlations is a significant improvement to the conventional approach of comparing only two curves, i.e., one from measurement and one from model [14]. In this chapter, we are able to provide a systematic methodology to clearly state how much of the gap in performance metrics can be accounted for by the quantified measurement uncertainties. Having said that, we still cannot claim that all possible sources of uncertainties are included. As a result, we still cannot encompass all the measurement data across all frequency and time points using the calculated model control limits.

Regarding the phase delay measurement-to-modeling correlation limitations, there are several aspects we would like to highlight: i) Phase delay is very sensitive to

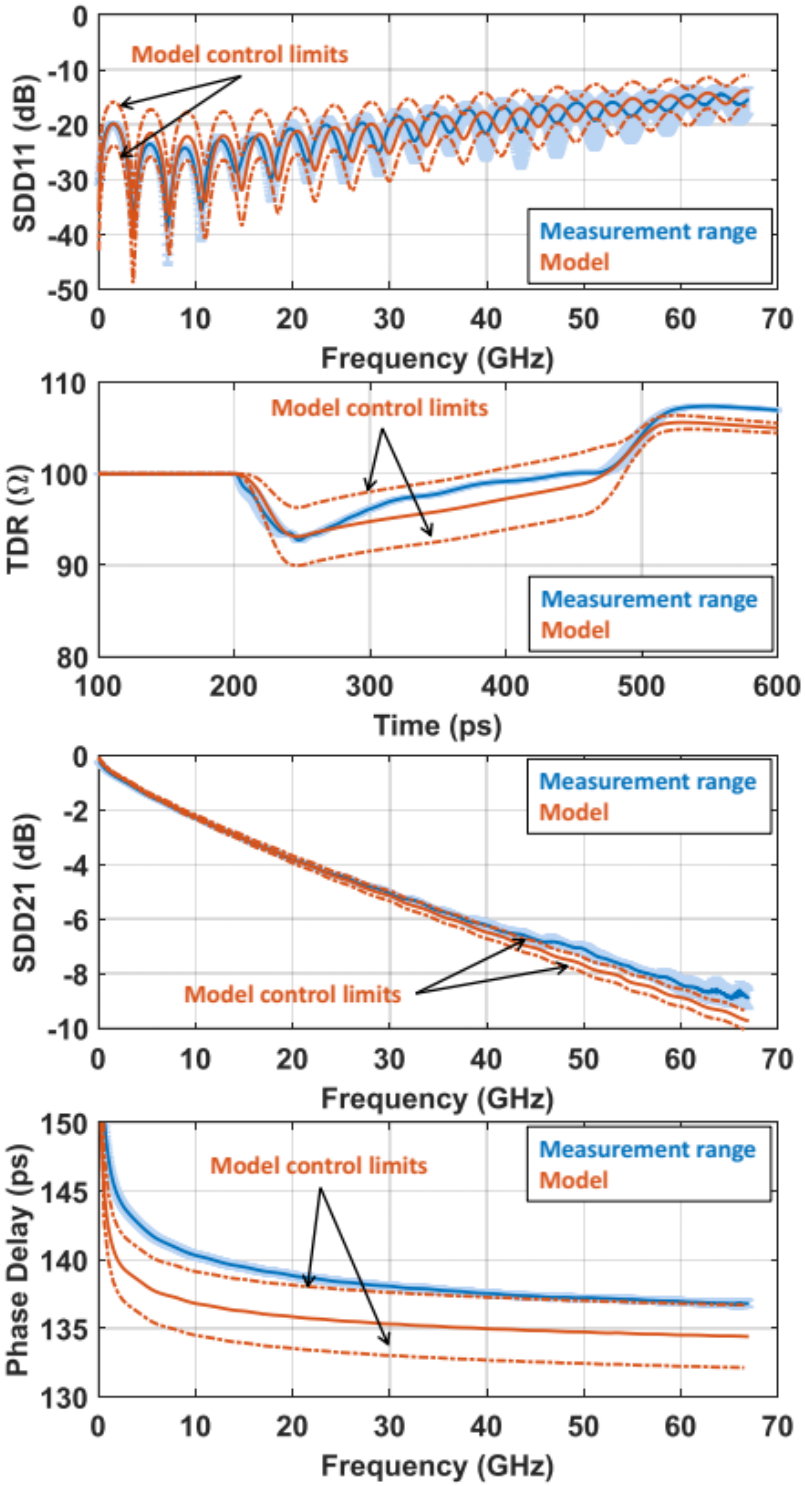

Figure 4.20: Measurement-to-modeling Correlation at Typical Package Use Condition for Design B. Uncertainty Incorporated into Measurement (Shaded) and Propagated to Modeling Outcome (Dash). Measurements Performed by ECC Lab.

the Dk value, and since dielectric material characterization is performed using a limited number of samples, this may result in under-estimating the actual existing variation. There is also the possibility of the material property shift between the material sheets that are characterized and those used in test vehicles. This impact could be further exacerbated due to part-to-part variations or various processes that packages experience during manufacturing, assembly or test. ii) Probe landing on the surface pads located on each end of the test structure can also affect the phase delay by changing the distance that signal has to travel. It should be noted that probes skate a certain distance after landing on the surface pads to ensure a good electrical contact. iii) Finally, causality of the roughness models could also have an impact. As indicated, the skin effect in rough conductor surfaces manifests itself in not only higher loss but also increased phase delay to maintain causality. This will influence relatively low frequencies more, where model control limits do not encompass the measurement data.

Regarding the insertion loss measurement-to-modeling correlations, as explained in Section III-B, the impact of the roughness variation has not been included in model control limits yet. It is expected that any discrepancy between insertion loss model control limits and measurement data will be further reduced by inclusion of this additional source of variation.

4.4 2x-Thru De-embedding

De-embedding plays a key role in removing the undesired impact of fixtures from S–parameters to achieve the actual device under test (DUT) performance. Fixtures are necessary for measurements of high speed transmission lines on a test vehicle and may include probe pads, microvias, and any sort of transition region before the DUT. Namely, the measurement reference plane already brought to the end of probes by

performance network analyzer (PNA) calibration, is moved to the end of transition region by de-embedding algorithms.

Any de-embedding process requiring identical designs with different lengths, e.g., 2x-Thru based [62], is inherently exposed to uncertainties due to manufacturing process variations and measurement reproducibility. Although the former has been studied in detail [63–67], prior research falls short of addressing the latter. Considering uncertainty quantification is critical to ascertain the quality of measurement-to-modeling correlation results [15, 18], the implications of de-embedding uncertainty deserve further exploring.

This section relies on the use condition dependent methodology which was introduced in [12] and thoroughly presented in [13]. The impact of measurement uncertainty without de-embedding was investigated in [15, 18]. Figure 4.21 illustrates the correlation flow highlighting the focus of this section with dash red lines. The major contributions of this section are as follows: (i) experimental evaluations of S-parameter measurement uncertainty with varying lengths for multiple metrics, (ii) a measurement-to-modeling correlation including de-embedding uncertainty using a 2x-Thru algorithm.

4.4.1 Reproducibility of S-parameter Measurements

Reproducibility examines the closeness of the agreement between the results of measurements of the same measurand carried out under changed conditions of measurement [60]. The changed conditions include repeated DUT insertion and measurement instrument calibrations by multiple test equipment operators at different times. This process provides information on the measurement variability introduced by all temporal and spatial variations of any influence quantity.

The impact of DUT length on S-parameter measurement reproducibility is eval-

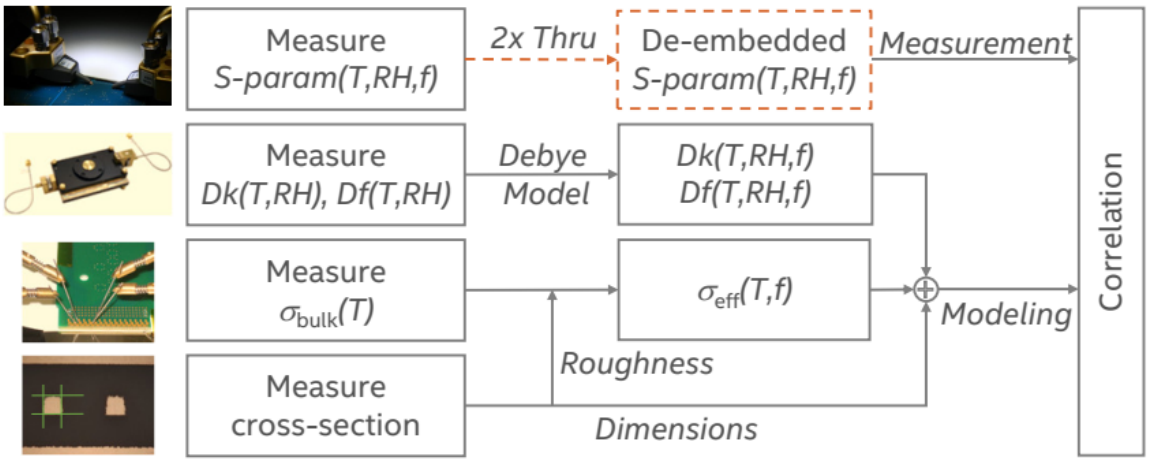

Figure 4.21: Correlation Flow. T, RH and f Indicate Dependence to Temperature, Relative Humidity and Frequency, Whereas σ_{bulk}, σ_{eff}, Dk, and Df Refer to Bulk and Effective Conductivity, Dielectric Constant and Dissipation Factor, Respectively. Dash Red Lines Highlights the Focus of This Section.

uated. A package test vehicle was designed and manufactured including four differential striplines (DSL) having the same design rules but varying routing lengths. Figure 4.22 illustrates all DUTs, and highlights the details like pads for probing, stitching microvias, ground plane and spacing on each layer.

To assess reproducibility, three different operators collected data on three different days, calibrating the four-port PNA before each measurement. Test vehicle was prebaked to ensure all the absorbed moisture was removed from the substrate and was kept in a nitrogen cabinet all the time except for active measurement [13]. Measurements were performed at $90°C$ up to 67 GHz on four different lengths, i.e., 5 mm, 10 mm, 15 mm, and 20 mm. This procedure yielded nine DUT measurements per length. Assuming the metrics are Gaussian variables, differential insertion loss (SDD21), phase delay (PD), and time domain reflectometry (TDR) are utilized to show relative standard deviation (RSD) $3\sigma/\mu$, where μ and σ are expected value and standard deviation, respectively.

As can be seen from Figure 4.23, SDD21 RSD increases with frequency, but there

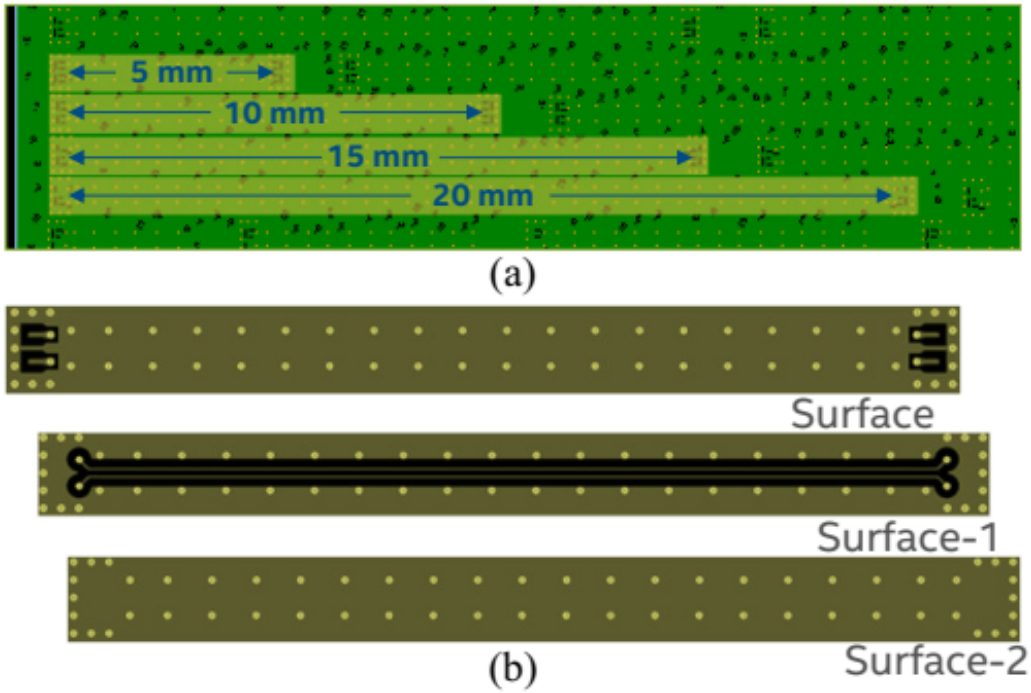

Figure 4.22: (a) Four DSL Structures on a Section of a Test Vehicle with Different Lengths Are Highlighted, (b) Features of One Structure Including Traces, Planes, Microvias, Probe Pads Are Illustrated per Layer.

is no clear trend observed with respect to length. In other words, similar RSD can be expected for any length or insertion loss of structure. Furthermore, overall RSD remains under 3% up to 67 GHz. The PD RSD shows little dependence on frequency—practically constant after a few GHz, but a clear trend on the length. RSD gets smaller for longer lines primarily due to higher delay. Probe landing on the surface pads located on each end of the test structure is the major factor affecting PD. It should be noted that probes skate a certain distance after landing on the surface pads to ensure a good electrical contact, which could unsurprisingly vary by operator and time. PD is also sensitive to Dk, but considering DUTs are closely located, Dk variation that DUTs see is expected to be minimal. TDR RSD has a small and practically constant variation over time. Except the shortest line, TDR RSD decreases with length, but all values are less than 0.4%. It is noteworthy that TDR plots only show the region

of interest for each length excluding initial delay and transition regions. Table 4.3 summarizes the key observations on the RSD impact of length and frequency/time over multiple performance metrics.

Table 4.3: RSD Impact of Multiple Factors Over SDD21, PD and TDR.

	SDD21	**PD**	**TDR**
Length	No clear trend	Decreasing	Mostly decreasing
Freq/Time	Increasing	Practically constant	Practically constant

2x-Thru de-embedding algorithms require two structures: i) DUT embedded between two fixtures (total), ii) two fixtures cascaded back-to-back without DUT (2x-Thru). Consider the 10 mm DSL as 2x-Thru, and 20 mm DSL as total from the set of structures shown in Figure 4.16. Nine distinct S-parameter measurements obtained from reproducibility in Section 4.4.1 for each 2x-Thru and total structures are de-embedded using all possible combinations. Therefore, the post de-embedding data include 81 distinct S-parameters for uncertainty quantification.

Figure 4.24 compares the uncertainty before and after de-embedding for multiple metrics. The frequency range ($f > 60$ GHz) where the IEEE P370 [68] fixture electrical requirements not conformed to are shaded, since de-embedding accuracy is not guaranteed. It is worth noting that Figure 4.24 does not compare the accuracy but the precision–how much data is spread with respect to its own mean μ, before and after de-embedding. Post de-embedding RSD for SDD21 and TDR indicates the uncertainty is pretty much comparable to the reproducibility before de-embedding despite the large amounts of data in de-embedded set. RSD of PD shows a bigger impact with de-embedding but overall RSD still remains below 1%.

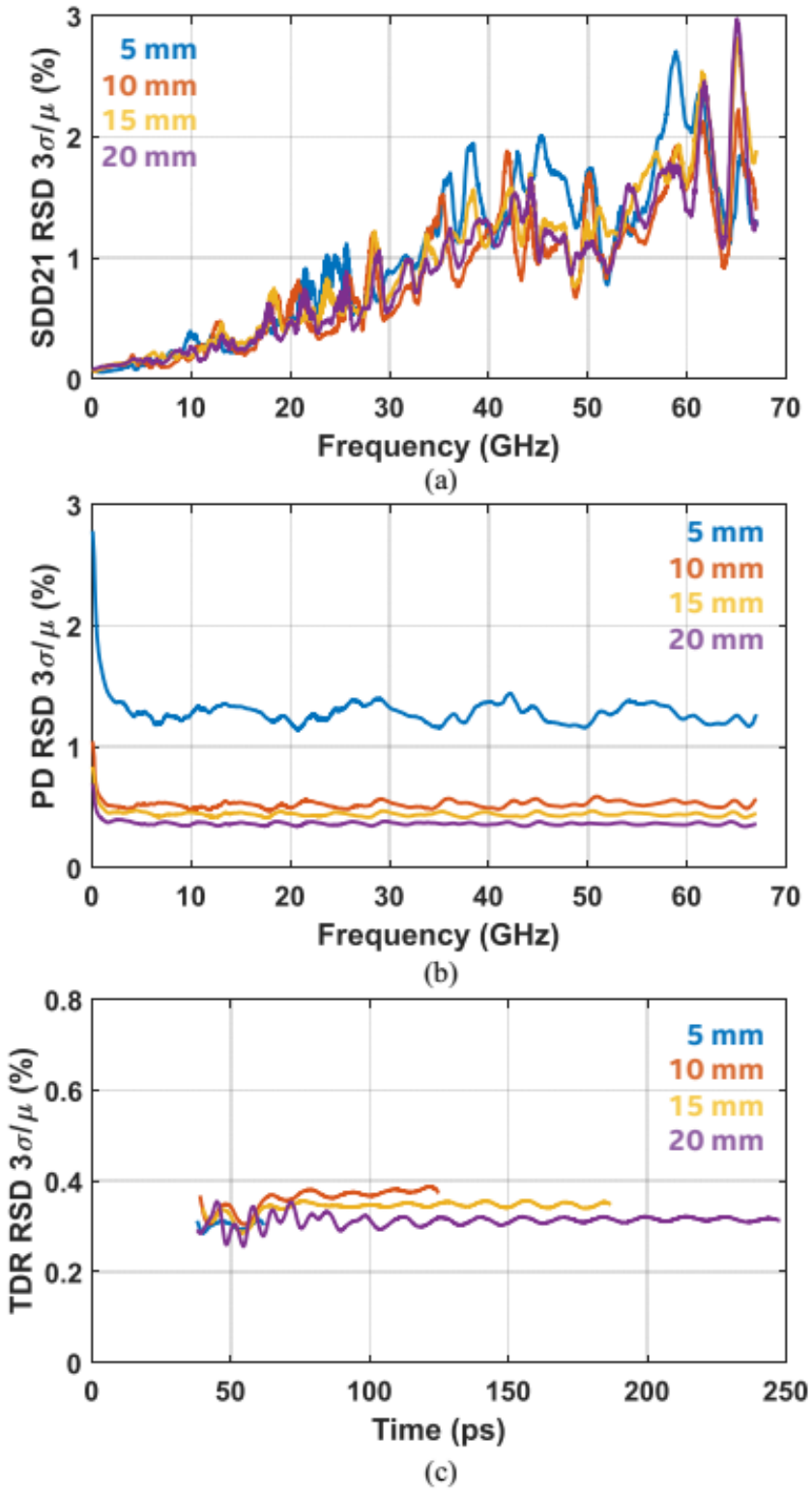

Figure 4.23: Relative Standard Deviation (RSD) ($3\sigma/\mu$) of Differential Metrics (a) SDD21, (b) PD, and (c) TDR. Lengths Are Color-coded. Measurements Performed by ECC Lab.

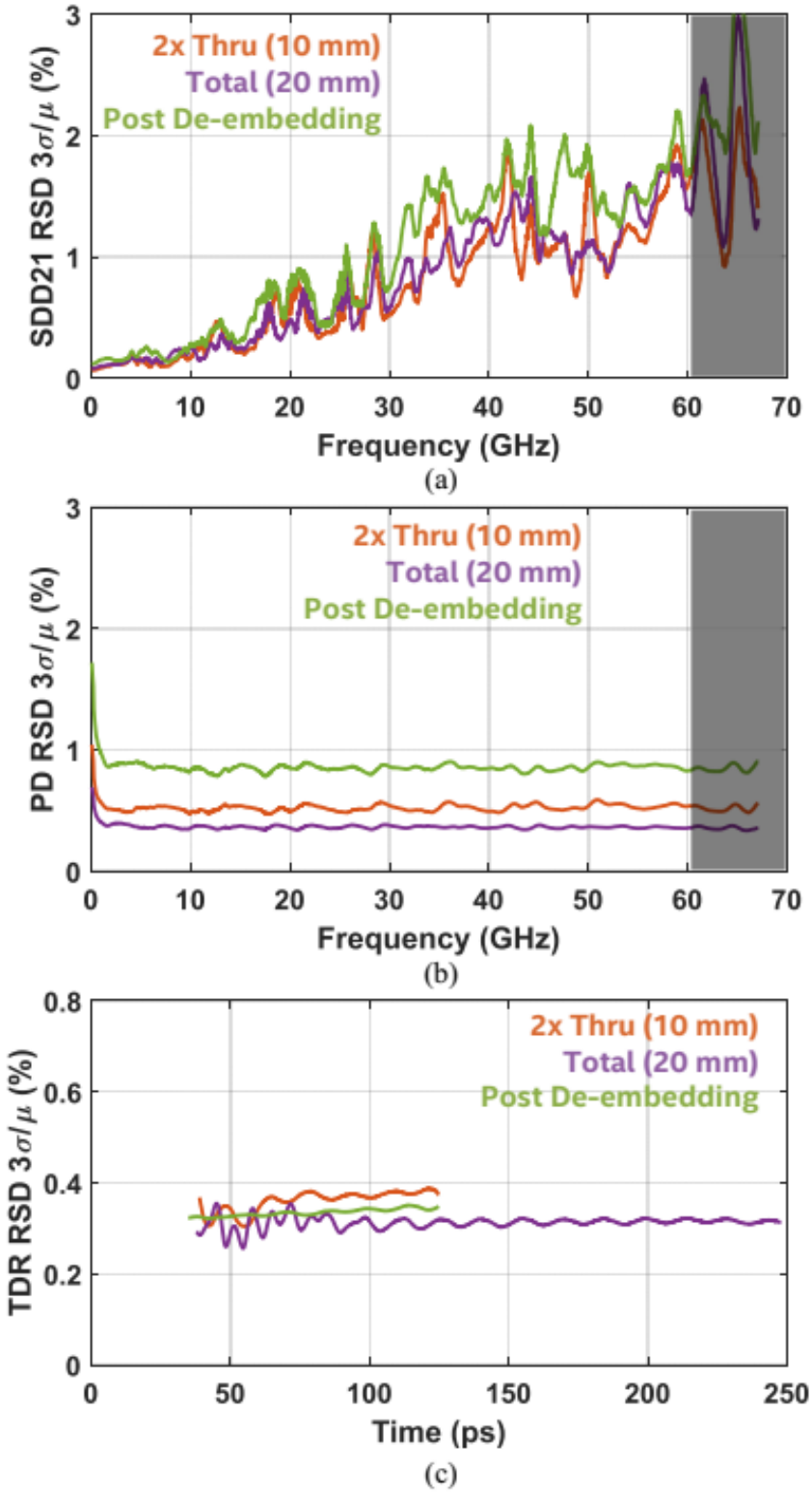

Figure 4.24: Before and after De-embedding RSD Comparison for Differential Metrics (a) SDD21, (b) PD, and (c) TDR. The Frequency Range Where the IEEE P370 Fixture Electrical Requirements Not Conformed to Are Shaded. Measurements Performed by ECC Lab.

4.4.2 Measurement-to-Modeling Correlation

This section follows [18] closely for uncertainty propagation methodology. Modeling results were generated using dielectric and conductor material properties and surface roughness characterized at the same use condition along with cross-section dimensions. A commercial 3D simulation tool was utilized with the mean values of all measured inputs. Each component of uncertainty was propagated and overall uncertainty in standard deviation for each performance metric was quantified using response surface methodology and statistical design of experiments [57]. Subsequently, a Monte Carlo analysis was performed to understand the impact of the variabilities on the modeling results.

Measurement-to-modeling correlation results are shown at $90°C$ in Figure 4.25. Measurement uncertainty was incorporated into de-embedded S-parameter data as a shaded area. Measurement uncertainty of bulk conductivity, Dk and Df, and cross-section dimensions were incorporated into modeling data as dashed lines. The impact of the uncertainty caused by surface roughness is not currently included in the results and will be addressed in future awaiting for a reliable roughness measurement metrology. This result implies that the most of the correlation gap in PD and TDR can be accounted for by the measurement uncertainties. It is also important to stress that de-embedding does not significantly increase measurement uncertainty.

4.5 Summary

This chapter presents a systematic methodology for measurement uncertainty quantification and propagation in high-speed package interconnect validation. Measurement uncertainty in S-parameters, dielectric permittivity, and cross-section dimensional measurements is examined. Variability in each measurement step of the

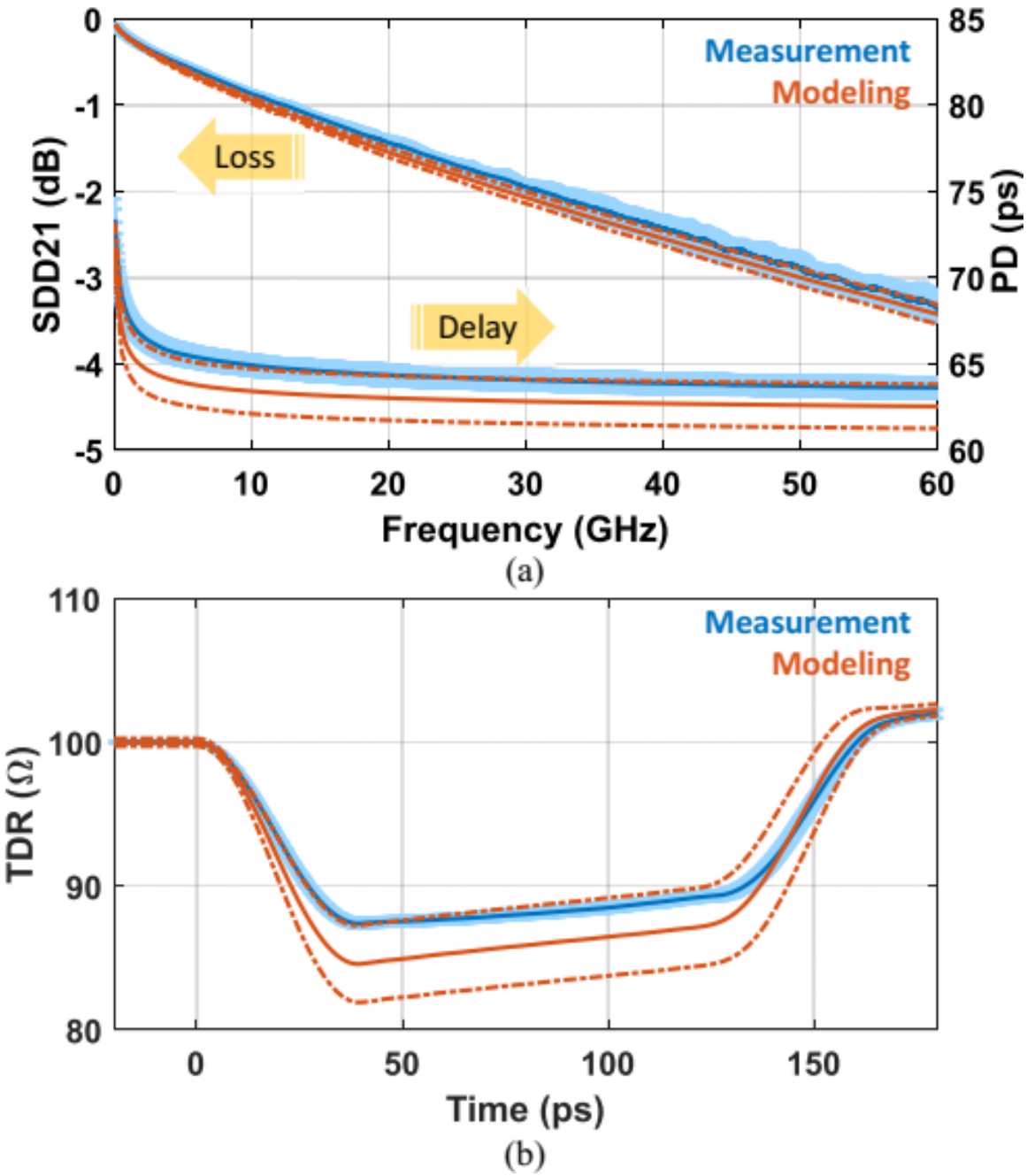

Figure 4.25: Correlation after De-embedding for Differential Metrics (a) SDD21, Pd, and (b) TDR. Uncertainty Incorporated into Measurement (Shaded) and Propagated to Modeling Outcome (Dash). Measurements Performed by ECC Lab.

use condition-dependent correlation flow is quantitatively determined through rigorous MCAs. Combined uncertainty propagated to the performance metrics increases the confidence in correlations by identifying control limits, and helps to more objectively interpret the correlation quality.

As de-embedding becomes increasingly central to high-speed interconnect validation, next the impact of de-embedding into measurement uncertainty was illustrated. Also, the experimental evaluations of S-parameter measurement uncertainty with varying lengths was presented for multiple metrics. By assessing the uncertainty impact of de-embedding, this study established that the de-embedding does not add significant uncertainty to the validation process.

Chapter 5

SURFACE ROUGHNESS CHARACTERIZATION

Surface roughness refers to the irregularities or deviations on the surface of a material from the ideal flat or smooth surface, as shown in Figure 5.1 In its pure form, copper has a relatively smooth surface; however, during manufacturing copper surface is intentionally roughened. This is desirable to promote adhesion between dielectric and conductor materials and avoid delamination in interconnects, but it dramatically increases insertion loss especially at high frequencies. This sensitive trade-off between electrical and mechanical demands makes it harder to optimize in a way that benefits both. Although some novel approaches proposed such as bypassing roughening process and introducing a thin layer of adhesion promoter [69], high volume manufacturing to-date commonly relies on copper etching. Therefore, surface roughness characterization is still critical to predict high-speed interconnect performance.

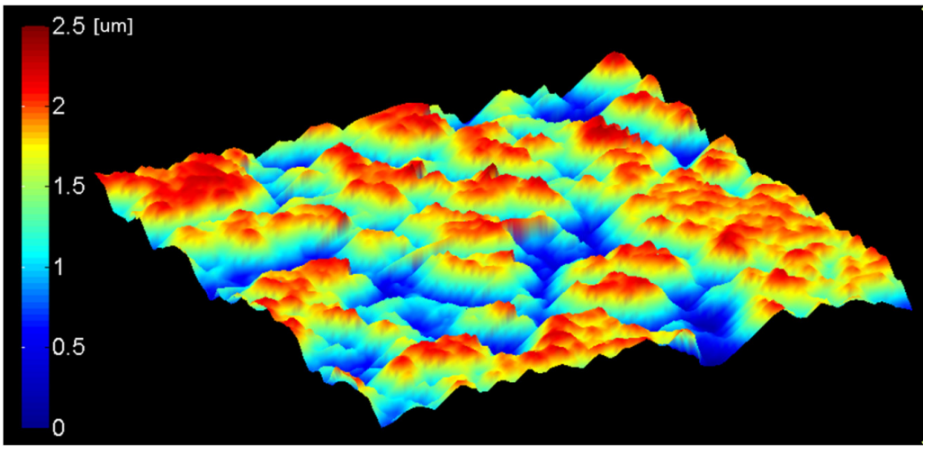

Figure 5.1: Surface Roughness Profile a Copper Foil.

5.1 Surface Roughness Metrology

There are various measurement instruments available for analyzing and evaluating surface roughness, which can be grouped under two methods:

- Contact profilometry: This measurement technique involves scanning a surface with a stylus or probe to obtain a three-dimensional profile of the surface. The stylus is typically a small, sharp tip that is mounted on a sensitive probe that can detect small vertical movements. As the stylus is moved along the surface, it traces the surface topography, and the vertical movements are recorded by the probe. One common instrument is Atomic force microscopy (AFM).

- Non-contact profilometry: This measurement technique does not require physical contact with the surface being measured. Instead of using a stylus or probe to scan the surface, non-contact profilometry typically uses light, laser, or other forms of electromagnetic radiation to measure the surface topography, such as white light interferometer and confocal microscopy.

Despite their differences, both of these methods provide information about the surface from top-down perspective. Therefore, one common shortcoming is that any surface feature invisible from top-down view cannot be captured, e.g., undercuts as shown in Figure 5.2. Alternative is the cross sectioning which is a powerful technique for roughness characterization that allows for a detailed examination of surface topography in a direction perpendicular to the surface. This method can provide valuable insights about any undercuts, but disclose features only over a line rather than an area.

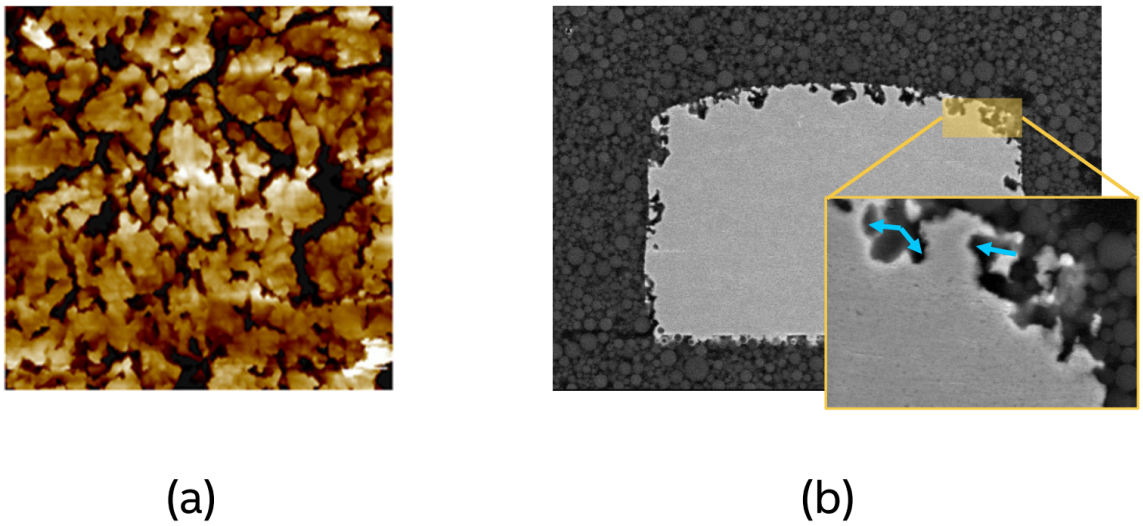

Figure 5.2: Surface Roughness Profiles from (a) Top-down View by AFM, and (b) Side-view by Cross-sectioning. Arrows Highlighting Undercuts Which Are Not Visible from Top-down View. Measurements Performed by LYA Lab.

5.1.1 Roughness Parameters

Once raw profile is measured, it is high-pass filtered to separate roughness (R) from waviness (W) as defined in surface metrology standards. 2-D roughness parameter names are preceded by a letter indicating the source profile, and 3-D roughness parameter names are preceded by letters 'S' or 'V' indicating surface and volume, respectively. The roughness profile is commonly described by the statistical distribution of height values, as some of them suumarized in Table 5.1.

Table 5.1: Commonly Used Statistical Roughness Parameters.

Rq	Root mean square height
Ra	Arithmetical mean height
Rsk	Skewness of height distribution
Rku	Kurtosis of height distribution
Rz	Maximum height

5.2 Surface Roughness Modeling Methodology

Copper surface roughness modeling is the process of mathematically describing the variations in the surface of a copper material. This can include factors such as the height of the surface's peaks and valleys, the distribution of those peaks and valleys, and the roughness of the surface at different scales. There are various methods for modeling copper surface roughness, as illustrated in Figure 5.3.

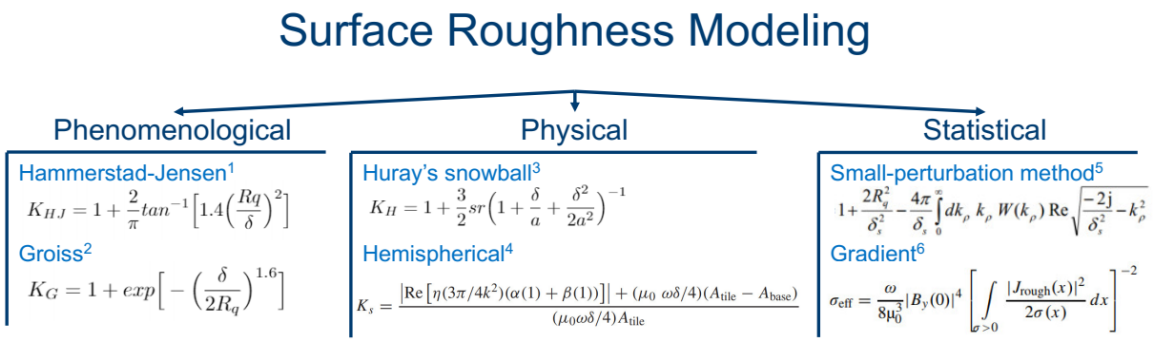

Figure 5.3: Existing Roughness Models.

There are several ways to find the roughness parameters for electrical roughness models:

- Experimentally: The roughness parameters can be determined experimentally by measuring the surface roughness using one of the aforementioned methods, and then fitting the measured data to an electrical roughness model.
- Inverse modeling: The roughness parameters can be determined by using an inverse modeling approach, where the roughness parameters are varied until the simulated results match the measured data.

It's worth noting that the accuracy and reliability of the roughness parameters depend on the quality and quantity of the measured data, the complexity of the model, and the chosen method for finding the roughness parameters.

5.2.1 Length Ratio

Today's on-package high speed interconnect loss is largely dominated by conductors due to thinner substrate, and high frequency conductor loss is considerably influenced by surface roughness. Currently roughness impact to loss is quantified by inverse modeling. Because there is no practical and reliable parameter(s) to extract from copper surface for estimating insertion loss. Commonly used parameters, e.g., Ra, Rq fails to differentiate surfaces especially when the roughness change is relatively small. Furthermore, contact or non-contact based surface profilometers used to calculate these roughness parameters suffer from the features not visible to detect from top-down view, e.g., undercuts. In this section, we propose an alternative to use a parameter extracted from cross-section images of the transmission line used for loss measurements.

This idea proposes to use the ratio of the length of rough trace perimeter to its smooth perimeter, indicating how much trace perimeter is increased after roughness process, as described in Equation 5.1.

$$L_r = \frac{\text{Rough counter length}}{\text{Smooth projected length}} \tag{5.1}$$

The proof of concept on this parameter is shown in Figure 5.4. Extracted L_r from the same test vehicle can predict slight loss increase that other parameters fall short of addressing.

The method provides a tool for suppliers to monitor roughness process stability quickly without the need for insertion loss measurements, which is very complex and error prone. This will ensure their process is stable and products will meet the loss targets committed.

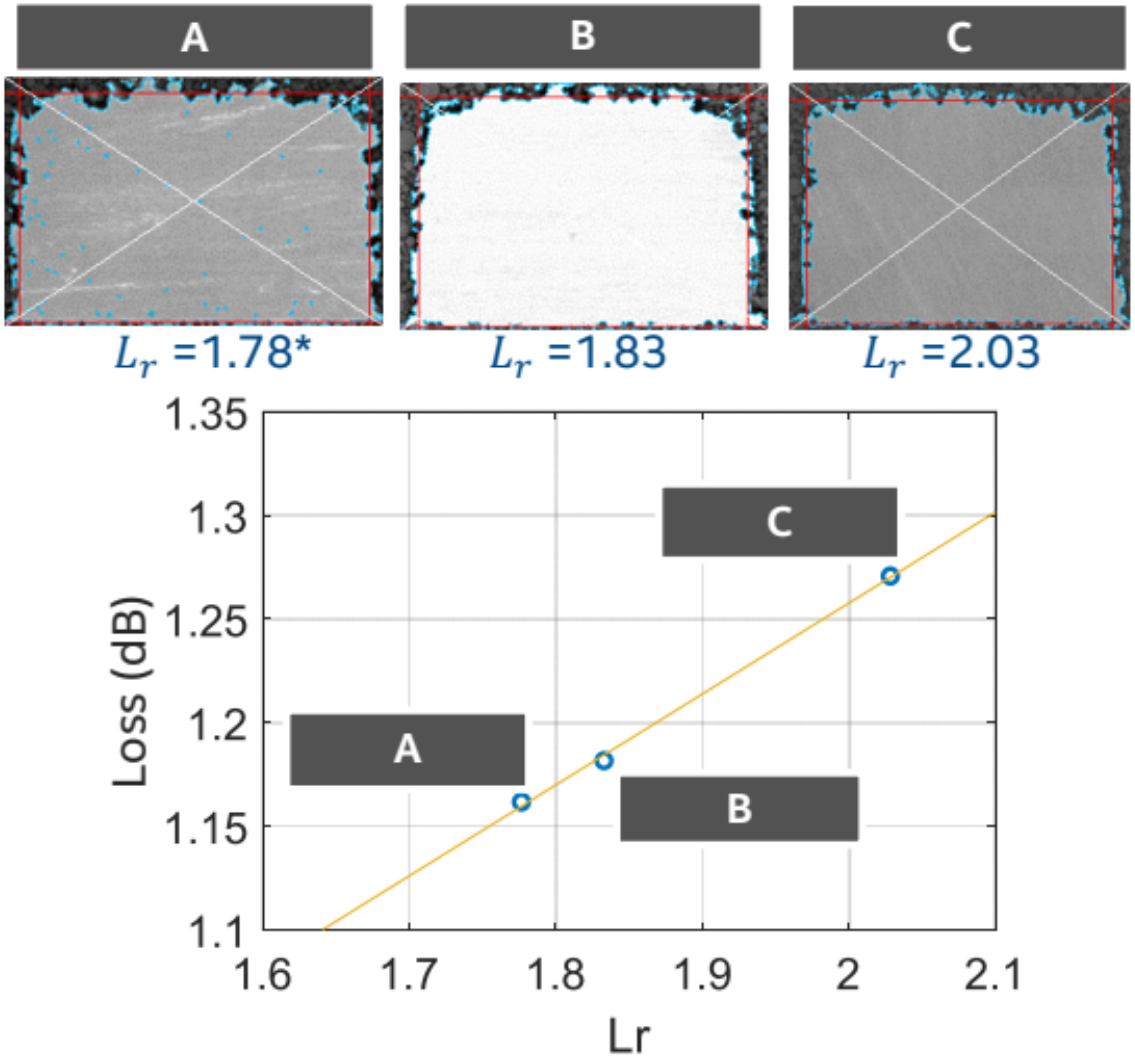

Figure 5.4: Length Ratio Proof of Concept. Loss and Cross-section Measurements Performed by ECC and LYA Labs, Respectively.

Chapter 6

CONCLUSION AND FUTURE WORK

The purpose of this work is to create a methodology that is both academically rigorous and has a significant impact on industry: A methodology providing an accurate characterization of the electrical performance of interconnects under realistic use-conditions, accompanied by an uncertainty analysis to improve the assessment of correlation quality. Majority of this work has already become a part of the Packaging Benchmark Suite developed by IEEE EPS TC-EDMS to provide information about the electromagnetic, electrical, and circuit modeling and simulation problems encountered, and the state-of-the-art solution methods used when analyzing and designing electronic packages [28]. Chapter 1 describes the motivation and summarizes the key contributions of this work as:

- Examining the impact of the use-conditions and manufacturing process variations on signal integrity performance,
- Quantifying measurement uncertainty for improved correlation quality,
- Investigating the effects of various adhesion promotion and copper surface roughness and developing a rigorous method for predicting loss.

Chapter 2 presents a novel systematic methodology that accurately captures the impact of use conditions on dielectric and conductor models for package high speed interconnects. First, a robust metrology is introduced to accurately characterize dielectric materials under various use conditions. Sample pre-conditioning requirements are detailed followed by an MCA study that demonstrates the precision of the metrology for different use conditions. A method for predicting the dielectric properties over

continuous ranges of temperature and RH is proposed along with results for typical types of package materials. Then, a comprehensive analysis is presented to show the inherent temperature dependence of correction factors of existing surface roughness models. Correlation to high-fidelity insertion loss measurements at different temperatures indicate that the correction factor synthesized at lower temperatures underestimates the loss at higher temperatures, necessitating an explicit temperature dependence for surface roughness models.

The proposed methodology ensures that the package design process can accurately account for the impact of product use conditions for emerging and future high speed interfaces. We consider the proposed methodology to be general enough for application to other types of interconnects and use conditions. Such potential applications include but are not limited to board interconnects and characterization at manufacturing, assembly, or test environmental conditions. Validation of the method for these additional applications and more novel interconnect structures such as tabbed transmission lines is an important area for the future work.

Chapter 3 first presents an efficient and accurate modeling methodology to analyze the impact of manufacturing process variations on IO performance metrics. The proposed methodology outperforms conventional approaches such as RSM by incorporating ML based algorithms (SVR and GPR) and overcomes limitations such as the constraints on tolerance margins and the number of uncertain parameters. It is also capable of modeling highly nonlinear structures. This resulting methodology proves to be promising and can be applied to a broad range of applications involving HSIO interconnects. Second, a novel corner model selection methodology is presented. It is shown that eye margins are sensitive to the corner model selection, and it is proposed to select most probable corner via maximum joint probability for more accurate and realistic high speed IO channel performance and defect rate predictions.

Chapter 4 presents a systematic methodology for measurement uncertainty quantification and propagation in high-speed package interconnect validation. Measurement uncertainty in S-parameters, dielectric permittivity, and cross-section dimensional measurements is examined. Variability in each measurement step of the use condition-dependent correlation flow is quantitatively determined through rigorous MCAs. Combined uncertainty propagated to the performance metrics increases the confidence in correlations by identifying control limits, and helps to more objectively interpret the correlation quality. Furthermore, although the work presented in this chapter covers frequencies up to 67 GHz, the methodology for achieving substrate measurement-to-modeling correlation has also been applied successfully to advanced substrate technologies spanning to 110 GHz.

Chapter 5 presents an overview of surface roughness characterization challenges including modeling, measurement and parameter extraction. Then, a new approach is introduced which can be used as an indicator to predict loss drifts. Although it is challenging to represent actual surface roughness with a single parameter, proposed method is able to capture loss variations in a small roughness window. For a wider window, or roughness processes leading to fundamentally different surface morphology, there might still be a need for more than a single parameter, which is an important area for future work.

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