Analyze of Total Ionizing Dose Effect in MOS/MNOS Capacitors

by

Ching-Tao Chang

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Graduate Supervisory Committee:

Hugh Barnaby, Chair
Keith Holbert
Sefaattin Tongay

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ABSTRACT

Metal-Oxide-Semiconductor (MOS) is essential to modern VLSI devices. In the past decades, a wealth of literature has been created to understand the impact of the radiation-induced charges on the devices, i.e., the creation of electron-hole pairs in the oxide layer which is the most sensitive part of MOS structure to the radiation effect. In this work, both MOS and MNOS devices were fabricated at ASU NanoFab to study the total ionizing dose effect using capacitance-voltage (C-V) electrical characterization by observing the direction and amounts of the shift in C-V curves and electron holography observation to directly image the charge buildup at the irradiated oxide film of the oxide-only MOS device.

C-V measurements revealed the C-V curves shifted to the left after irradiation (with a positive bias applied) because of the net positive charges trapped at the oxide layer for the oxide-only sample. On the other hand, for nitride/oxide samples with positive biased during irradiation, the C-V curve shifted to the right due to the net negative charges trapped at the oxide layer. It was also observed that the C-V curve has less shift in voltage for MNOS than MOS devices after irradiation due to the less charge buildup after irradiation.

Off-axis electron holography was performed to map the charge distribution across the MOSCAP sample. Compared with both pre-and post-irradiated samples, a larger potential drop at the Si/SiO_2 was noticed in post-irradiation samples, which indicates the presence of greater amounts of positive charges that buildup the Si/SiO_2 interface after the TID exposure.

TCAD modeling was used to extract the density of charges accumulated near the SiO_2/Si and SiO_2/ Metal interface by matching the simulation results to the potential data

from holography. The increase of near-interface positive charges in post-irradiated samples is consistent with the C-V results.

DEDICATION

Dedicated to my family in Taiwan.

ACKNOWLEDGMENTS

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I want to thank Dr. David Smith and Dr. Martha McCartney for developing the electron holography data and good hologram images that I use in my thesis. They also taught me the theory of electron holography and the phase reconstruction process and clarify the doubts I encountered. I would like to thank all the NanoFab staff and my great colleague Smitha for helping me with the sample fabrication in the cleaning room. They help me to overcome every issue I face during fabrication and provide me valuable feedback to optimize my process.

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CHAPTER 1

INTRODUCTION AND MOTIVATION

1.1 Introduction and Motivation

Metal-Oxide-Semiconductor (MOS) structures are essential to modern VLSI devices. In the past decades, a wealth of literature has been published to explain the impact of radiation-induced defects on these devices. The oxide insulating layer is the most sensitive part of the MOS structure to total ionizing radiation dose. When ionizing radiation (high energy charged particles or photons) interacts with MOS dielectrics, the deposited energy creates electron-hole pairs in the insulating layer [1], [2]. Generated electrons and holes are free to transport inside the insulator through diffusion and, primarily, electric field dependent drift, either toward the underlying silicon or toward the conducting gate. The high density of charge trapping centers located near the interfaces trap the radiation-induced carriers (electrons or holes) and thus generate fixed trapped charge in the insulator, which changes the electrical properties of the MOS system [2], [3].

Various techniques have been developed to study the effects of radiation exposure on MOS devices. The use of current-voltage (I-V) measurements or capacitance-voltage (C-V) measurements provides valuable information about the fixed charge buildup inside the oxide layer due to ionization [4-7]. More complex thermal, time, and frequency domain electrical measurements on MOS structures allow for the characterization of the spatial and energy distributions of radiation-induced oxide defects [8-10]. However, direct measurements of radiation-induced volumetric charge distributions in the oxide film have never been performed.

Off-axis electron holography is a novel metrology technique that allows for direct imaging of the electrostatic potential, prior to and after irradiation. Analysis of the potential profiles enables the net volumetric charge distribution inside the insulating film to be quantified. This technique uses a transmission electron microscope (TEM) equipped with a field-emission gun (FEG) to provide a steady coherent source of electrons. Besides FEG, biprism is also required. An electron biprism is a charged wire used to interfere with plane electron wave and reference wave, deflecting both waves toward each other until overlapping, which forms a hologram. This technique facilitates the production of an electrostatic potential mapping throughout the imaged sample [11] - [13]. Using TCAD simulation, the charge distribution can be extracted by matching the potential profile from the electron holography examination. Thus, with electron holography the difference in volumetric charge distributions inside the oxide layer between pre-and post-irradiated MOS capacitors can be quantified.

For oxide-only samples, the effect of ionizing radiation is traditionally explained, through the analysis of electrical data, by the trapping of holes near the Si-SiO_2 interface [2]. In this thesis, we confirm this explanation directly through the use of electron holography. We also show that for these samples, electron trapping occurs as well, but near the gate metal surface, where the effect of the negative charge is not observed electrically. It has been shown that oxide-nitride samples have better TID tolerance [14], especially at low irradiation biases. The theory developed to explain this effect is that more electron trapping occurs in the bulk of the film stack, which compensates for the effects of trapped holes [15]. Electron holography provides for the first time a method to confirm this theory.

This thesis does not report the results of holography on oxide-nitride films. However, it is planned in future work by this author.

1.2 Structure of the Dissertation

In Chapter 1, a brief background and history of research on total ionizing dose effects in the MOS capacitors is introduced and explained.

Chapter 2 describes the background of the total ionizing dose mechanism in the oxide film of MOS devices. Including the charge generation and recombination, transport, and the trapping charges in the dielectric. The charge separation technique and a brief introduction to Technology Computer-Aided Design (TCAD) are also mentioned in the chapter. There is also a section discussing the basics of electron holography in Chapter 2.

Chapter 3 describes the experimental methods, including fabrication processes of MOS and MNOS devices at the ASU cleaning room for the TID study, and TID experiment setup. It also mentioned the analysis method used in this thesis to study the TID effect on MOS and MNOS capacitors, including performing the C-V measurements and electron holography observations.

Chapter 4 presents and analyzes the results of the electrical measurements, mainly focused on the C-V curve shifts due to the TID effect. An increase in capacitance at inversion is also studied in Chapter 4.

Chapter 5 discusses the charge measured in the pre- and post-irradiated oxide films by holography. Also, TCAD simulations are performed to extract the total amount of charges built up in the irradiated oxide layer to quantify the TID effect.

Chapter 6 summarizes the work and draws conclusions and presents directions for future research.

CHAPTER 2

BACKGROUND

2.1 Total Ionizing Dose Effect

Long-term exposure to ionizing radiation can cause gradual degradation of MOS device performance. The cumulative damage caused by ionizing particles or high-energy photons is called Total Ionizing Dose (TID). The basic radiation-induced processes for TID in SiO_2 are: 1) electron-hole pair generation, 2) prompt recombination of a fraction of carriers, 3) transport of carriers, 4a) trapping of carriers, mostly holes near the Si/SiO_2 interface as shown in Figure 2.1, and 4b) de-passivation of dangling bonds by reactions involving holes and hydrogen [16]. When MOS capacitors are exposed to ionizing radiation, electron and hole pairs (ehps) are created by the interaction of radiation with the atoms in the oxide. The ionization damage is initiated when the ehps are generated by the energy deposited. The density of ehps is proportional to the energy absorbed [17]. A fraction of the generated carriers that transport towards the Si substrate will be trapped in defect precursors. Generally, most of the carriers that get trapped are holes, thus net trapped positive charges buildup near the $Si\text{-}SiO_2$ interface.

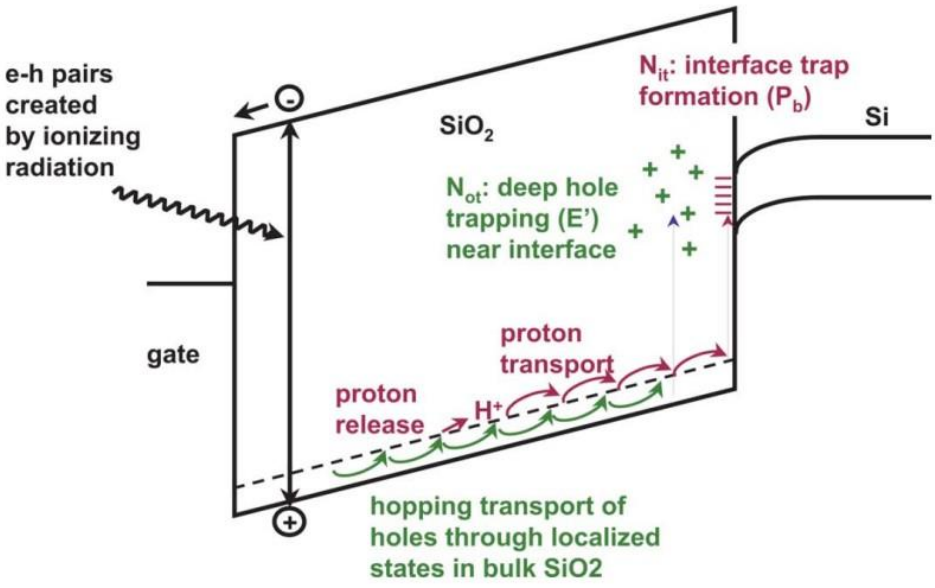

Figure 2.1 Schematic of Radiation Induce Processes with Band Diagram of MOS Capacitor Under
Positive Gate Bias [2].

Figure 2.1 plots the MOS band diagram under positive bias. Carrier generation and recombination process happen in picosecond time scales. The fraction of electrons and holes undergoing recombination depends on the electric field and radiation source. The remaining electrons escaping for recombination will move toward the gate in picoseconds due to their higher mobility in the oxide layer than holes. The holes move toward the Si/SiO_2 interface by polaron hopping through the defects and shallow traps present in the oxide film. Under positive bias applied to the gate, or for these devices due to the metal to semiconductor work function difference, when 0V bias is applied, the positive electric field will drive more holes towards the $Si\text{-}SiO_2$ interface. Near the interface, some fraction of holes falls in the deep trapping site, forming fixed positive charges (N_{ot}), which cause the negative voltage shift in C-V characteristics. Fixed trapped charge in the oxide will cause

shifts in the C-V curves. Some holes transported in the SiO_2 will release hydrogen ions through molecular interactions. Subsequent hydrogen ions that transport to the Si-SiO_2 interface will de-passivate silicon dangling bonds leading to the formation of the interface trap (N_{IT}) with energy levels located in the silicon bandgap. The occupancy of interface traps is dependent on the Fermi level at the interface, leading, as well, to C-V curve shifts and also a reduction in the slope of the capacitance transition from the accumulation to inversion capacitance. In this thesis, we will only consider the mechanisms of N_{OT} generation (i.e., not N_{IT}) and subsequent effects.

2.1.1 Generation and Recombination

The oxide layer in MOS structures is highly sensitive to ionizing radiation. When either photons or other ionizing particles, such as protons or electrons, interact with solid materials with enough energy, the energy deposited creates electron/hole pairs in the oxide [2], [17]. The average energy to create a single electron-hole pair is around 18 eV in SiO_2 [2]. The mechanism of carrier generation depends on the type of particles. This study primarily focused on photon-induced ionization. Ionizing radiation from high-energy photons can interact with target atoms through three different mechanisms: 1) photoelectric effect, 2) Thomson and Compton scattering, and 3) pair production shown in Figure 2.2. The photoelectric effect involves a low-energy photon interaction with the entire atomic electron cloud and knocks the inner core electrons, called photoelectrons. Photoelectrons produced by the primary photon are the primary products that generate ehps [20]. Thomson and Compton scattering involves higher energy of photons interacting with the target material and emitting a Compton electron and a photon with less energy to help

in e-h pair creation [20]. Pair production happens with high energy of photons interacting with the target materials and thus is able to create ehps [16,20]. In this study, a Co-60 γ source is used which emits photons around the energy of 1.25 MeV, where the main mechanism for carrier generation mechanism in target materials is Thomson and Compton scattering.

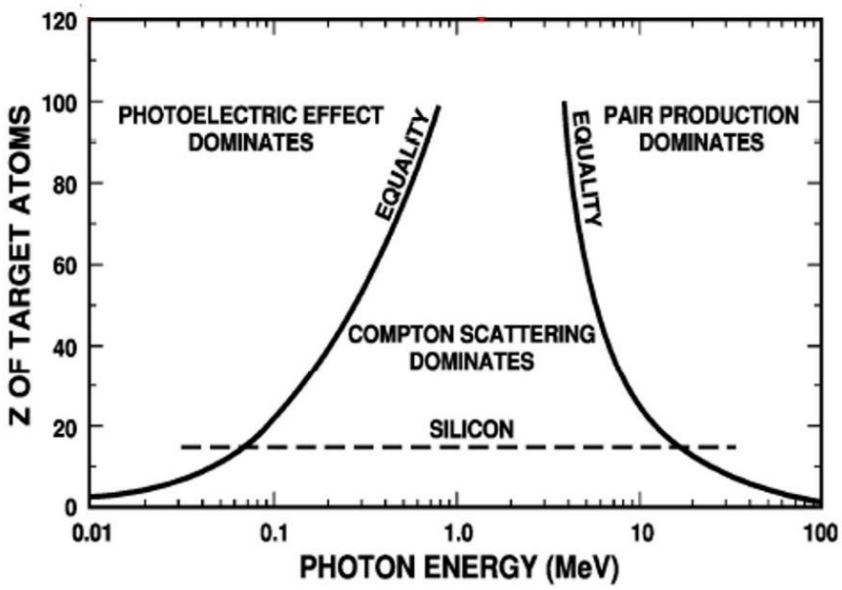

Figure 2.2 The Relationship Between Photon Energy and the Probability of Carrier Generating Mechanism Occurs [20].

After electron/hole pairs (ehps) are generated in the oxide layer due to ionizing radiation, some carriers recombine in a very short time period, typically in pico-seconds. The fraction of ehps that escape the initial recombination process, divided by the total number of ehps generated, is referred to as the charge yield. The fraction of holes that escape recombination depends on factors such as the energy of the radiation source and the strength of the electric field applied, as depicted in Figure 2.3. Highly ionizing particles such as α particles exhibit more prompt recombination compared to Co-60 photons.

Moreover, the recombination of ehp is a function of the electric field in the materials. A higher applied field reduces recombination since most of the ehps are separated before the recombination process occurs [19]. A fraction of the surviving holes may fall into deep traps near Si/SiO_2 interface after hopping transport into the oxide leading to the oxide-trapped charges buildup.

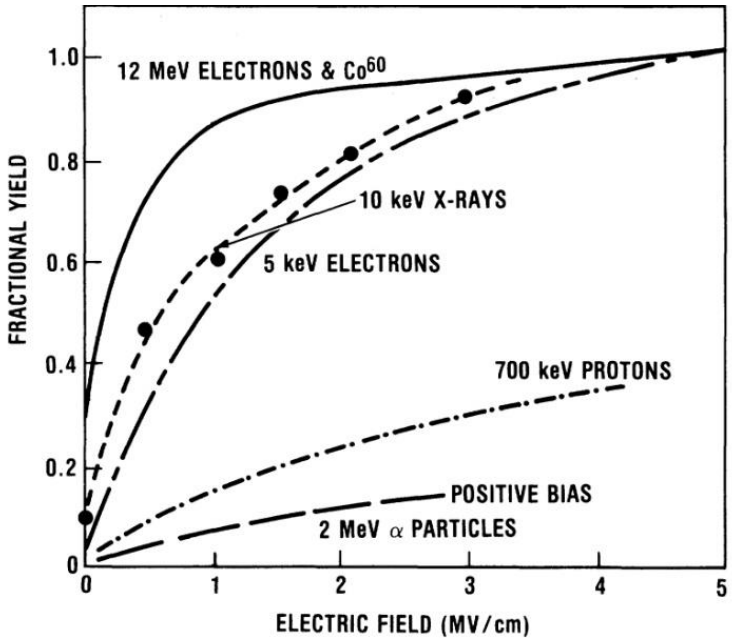

Figure 2.3 Fractional of Unrecombined Holes as A Function of Field with Different Radiation Sources [2].

2.1.2 Oxide Trapped Charge (N_{OT})

After irradiation, the oxide layer near Si/SiO_2 accumulates net positive trapped charges (N_{OT}). Holes typically get trapped in E' centers. There are two kinds of E' centers, E'_{γ} and E'_{δ}, which play an important role in the charge trapping near the interface of Si/SiO_2. The formation E'_{γ} center is due to the single oxide vacancy as shown in Figure 2.4 [21,22]. Two Si atoms are connected by a strained Si-Si bond, and each is backed bonded to three

oxygen atoms. When the devices are irradiated, the weak Si-Si bond is broken by capturing a hole causing an asymmetrical relaxation. The hole is localized at one of the Si atoms while the other threefold coordinate Si atom contains an unpaired electron. With the E'$_\delta$ center, an unpaired electron is shared by two Si atoms, and the Si-Si bond symmetrically relaxes upon capturing the hole [23], as shown in Figure 2.5.

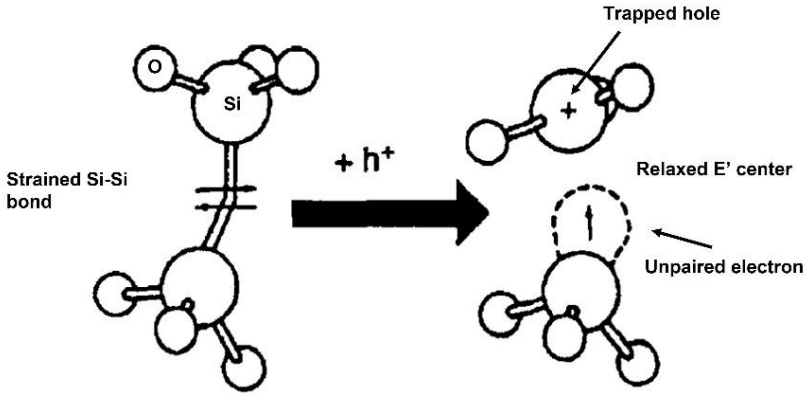

Figure 2.4 Formation of E' center in Amorphous SiO_2 [21].

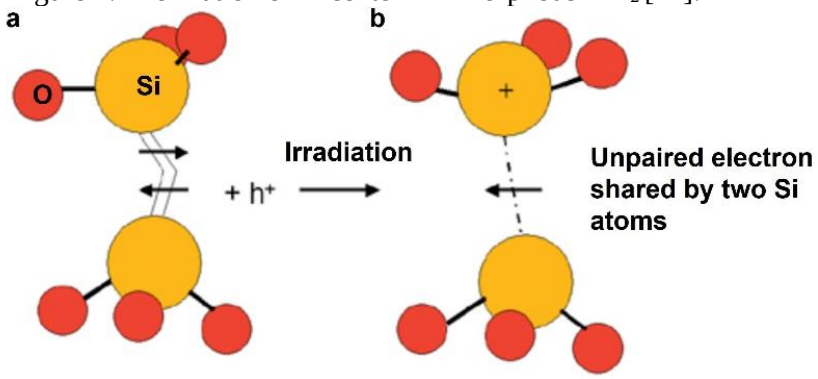

Figure 2.5 Schematic Showing the Formation of E'$_\delta$ center [23]. a. Shows the strained Si-Si bond b.
Shows the relaxed E'$_\delta$ center.

Both E' centers can exchange the charge with the adjacent Si layer via capture or emit carriers from the Si layer. The ability to communicate with the Si layer depends on their distance from the Si/SiO_2 interface. Defects that are located within 3nm of the Si/SiO_2

can exchange charges within a second via tunneling, and are called border traps, as shown in Figure 2.6. Those that are sited greater than 3nm from the interface have relatively slow charge exchange time (greater than 1 sec) and are treated as fixed positive oxide charges which make the C-V curves shift to the left [24,25].

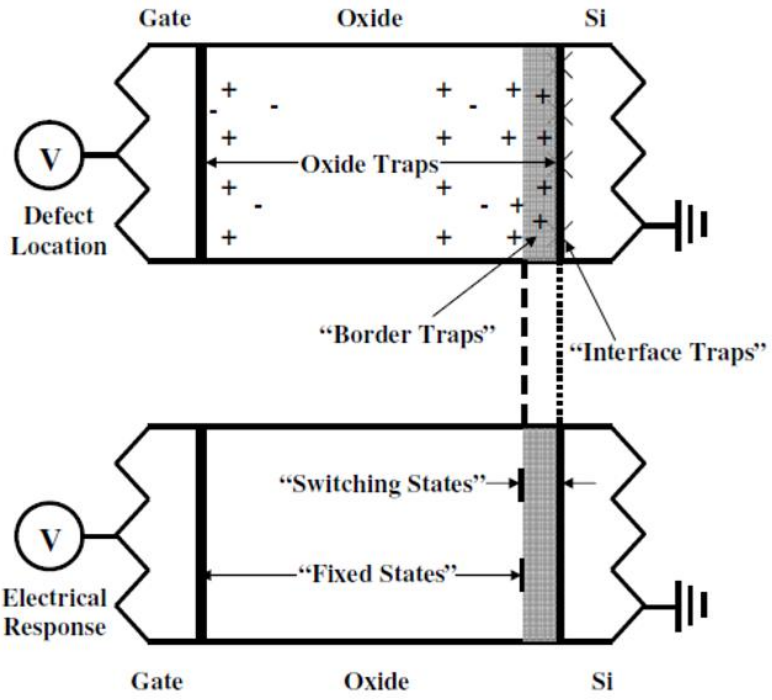

Figure 2.6 The Location and Electrical Respond of Trapped Charges in the MOS Capacitors [24].

2.1.3 Charge Separation Technology

To investigate the effect of N_{OT} buildup on MOS transistors using C-V measurements, it is necessary to quantify the buildup of oxide trap charges in the oxide film which causes the shift of the C-V curves after irradiation. The mid-gap charge separation technique allows us to calculate the density of the oxide trap charges buildup after irradiation by observing the shift of the C-V curve produced by these trap charges, as shown in Figure 2.7. When a gate voltage is applied to a MOS device and biased at a

specific depleting voltage, the shift of the C-V curve is solely due to the N_{OT} buildup [26]. This voltage is known as mid-gap voltage (V_{MG}). Therefore, the relationship between the shift of the V_{MG} and the voltage shift caused by N_{OT} can be expressed as [26],

$$\Delta V_{OT} = \Delta V_{MG} \tag{2.1}$$

where V_{OT} is the shift caused by the increase of N_{OT}. The density of the N_{OT} can be calculated as,

$$\Delta N_{OT} = -C_{OX} * \frac{V_{OT}}{q} \tag{2.2}$$

where C_{OX} is the oxide capacitance per unit area.

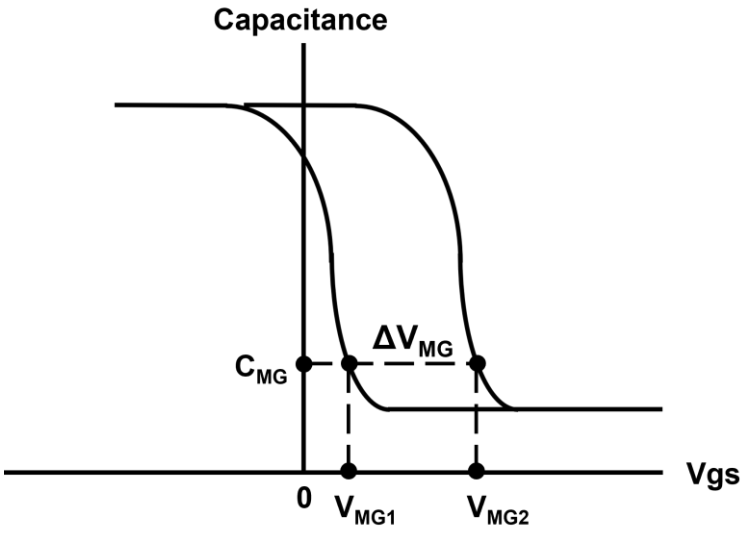

Figure 2.7 Schematic Illustration of Mid-Gap Charge Separation Technique.

2.1.4 Technology Computer-Aided Design (TCAD)

TCAD simulation is a powerful tool used in the semiconductor industry to model and analyze the behavior of electronic devices. In this work, TCAD simulation is

performed with one of the commercial Silvaco TCAD software tools, Atlas, to analyze the TID effect in MOS devices. Atlas provides general capabilities for physics-based 2D and 3D simulation of semiconductor devices. The inputs and outputs of the Atlas are shown in Figure 2.8. By defining the physical structure to be simulated and the device models to be used, it is able to specify the device simulation problems [27]. The physical structure could be created in the simulator by a CAD tool, DEVEDIT [28]. In order to have accurate simulation results, it is required to create a fine grid at the critical area of the structure. Atlas also provides many physical models, such as the impact ionization model [29], for us to study the physical behavior of a device due to the TID effect. One of the outputs from Atlas is the log file, which allows us to store the capacitance and voltage data. The structure file is another output from Atlas, which allows us to study the band diagram and charge distribution for the devices in this study.

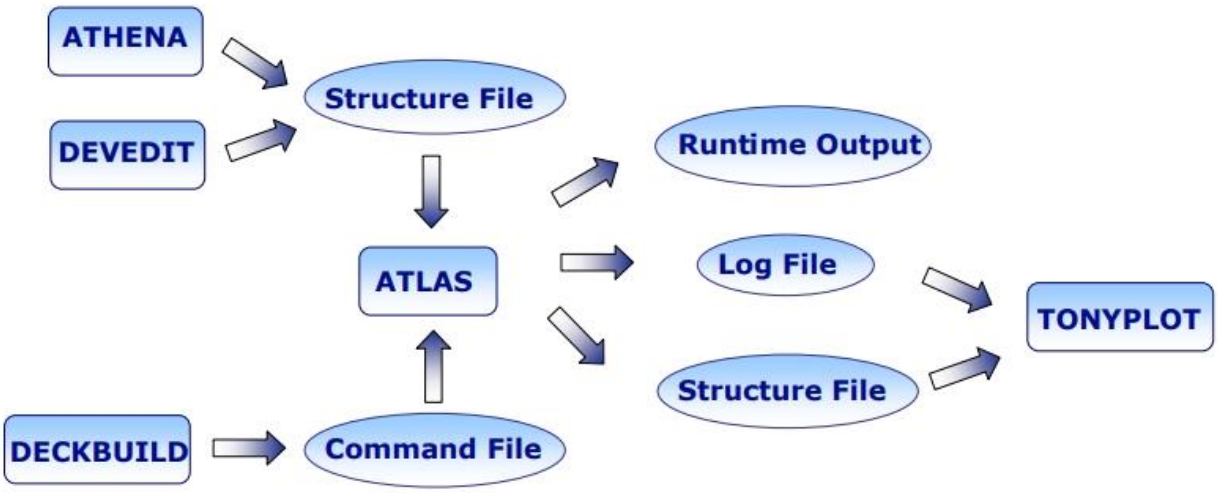

Figure 2.8 Inputs and Outputs of Atlas. [Source: Maria Concetta Allia]

2.2 Off-Axis Electron Holography

Off-axis electron holography is a powerful technique for characterizing electrostatic and electromagnetic fields with sub-nanometer resolution in the transmission electron microscope (TEM), by analyzing the phase shift of the electron wave deduced from the reconstructed electron hologram [30]. Rather than recording only the intensity information in the conventional TEM image, electron holography enables access to both the phase shift and the amplitude of the aberrated electron wave after it has traveled through the sample [31]. Although the concept is originally proposed by Gabor in 1949, it was not until the advent of the field emission gun (FEG), which provided a stable, coherent electron source, that the technique was successfully implemented in the TEM. The basic electron holography set-up in the TEM we use in this thesis is shown in Figure 2.9, and the functions of each of its key parts will be discussed in the following section.

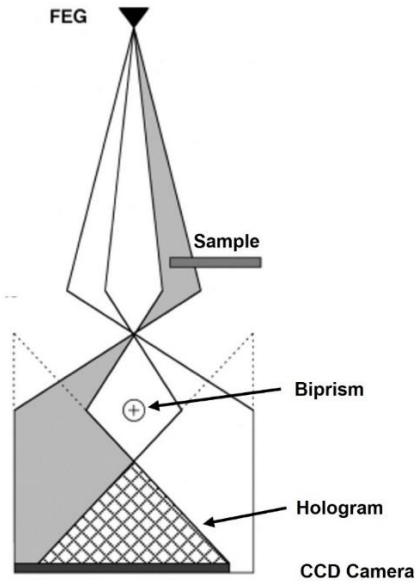

Figure 2.9 Schematic Illustration of the Set-Up in TEM for Off-Axis Electron Holography [31].

This geometry allows the electrons which have passed through the sample (sample wave) to be overlaid with electrons which have only passed through vacuum (reference wave).

2.2.1 Hologram formation

In order to form a hologram, it is required to equip the microscope with a field emission gun which will provide a steady and spatially coherent electron source. Since the resolution and linearity of the inference pattern is important the hologram must be recorded with a CCD or direct electron camera [12], [13]. Figure 2.10 shows the effect of limited spatial coherence on hologram images, where electrons emitted from two different positions separated by distance Δ u and form two inference patterns at different positions with a Δ x lateral shift [13].

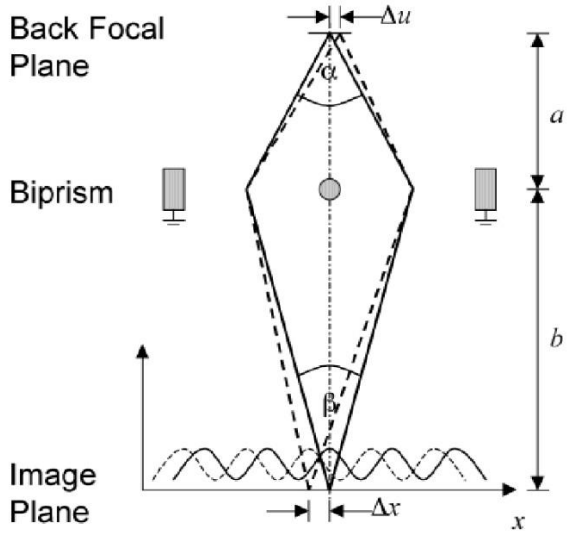

Figure 2.10 Illustration of the Effect of Limited Coherent Electron Source on Electron Hologram [13].

An electrostatic biprism located below the sample deflects both reference wave and objective wave together to form a hologram pattern that appears as interference fringes in the TEM image. To achieve greater resolution, it is desirable to maximize the width of the

interference pattern and minimize the spacing of the fringes by either applying a larger positive voltage to the biprism or reducing the radius of the biprism [12]. By increasing the positive potential applied to biprism, a larger space is created between two sources S1, and S2, and thus increases the interference region, W, with a larger deflection angle, α, shown in Figure 2.3. The relationship between the size of biprism (*R*) and interference width (*W*) could be expressed in Eq. 2.3 [32],

$$W = 2\left|\frac{a+b}{a}\right|\left(\alpha\frac{ab}{a+b} - R\right) \tag{2.3}$$

where a and b are the distance between the source, biprism, and hologram as shown in Figure 2.11, and α is the deflection angle of the source.

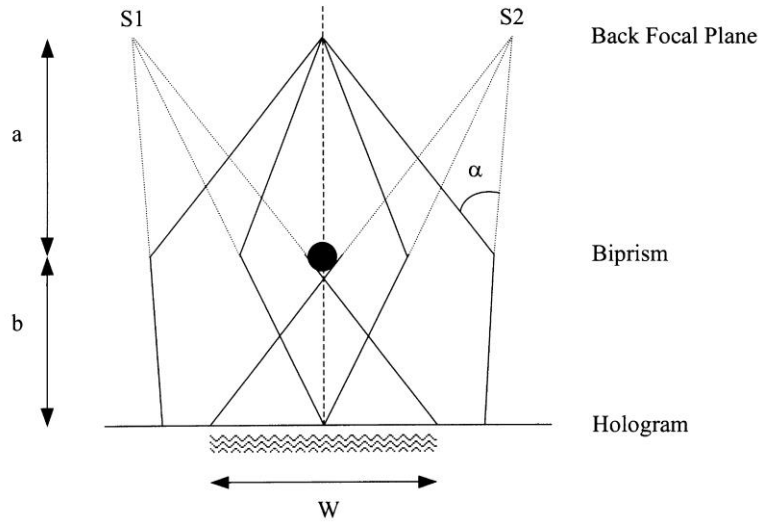

Figure 2.11 Schematic Diagram Illustrating the Role of the Biprism in Generating the Hologram [12].

The phase shift of an electron wave passed through the sample relative to the reference wave that has passed through the vacuum, is given in one dimension by equation 2.4 [30], [32],

$$\phi(x) = C_E \int V(x,z)dz - \frac{e}{\hbar}\iint B_\perp(x,z)dxdz \tag{2.4}$$

where z is the incident electron beam direction, x is a direction in the plane of the specimen, V is the mean inner potential (MIP) and the potential from electrostatic fields, $B_\perp$ is the component of magnetic induction perpendicular to the x and z, and C_E is the interaction action which depends on the energy of incident electron beam. Assuming that the sample thickness is uniform, neither V nor B varies with z within the sample thickness t. If one makes an assumption that any electric or magnetic fringing fields outside the sample can be neglected, a simplified expression for the relative phase change from Eq. 2.4 can be expressed as,

$$\phi(x) = C_E V(v)t(x) - \frac{e}{\hbar}\int B_\perp(x)t(x)dx \tag{2.5}$$

For the non-magnetic materials discussed in this thesis, the second term in Eq. 2.3 is zero. Differentiation from Eq. 2.5 with respect to x lead to an expression of phase gradient,

$$\frac{d\emptyset(x)}{dx} = C_E \frac{d}{dx}[V(v)t(x)] - \frac{e}{\hbar}B_\perp(x)t(x) \tag{2.6}$$

Both Eq. 2.5 and 2.6 are fundamental to the measurement and quantification of electric and magnetic fields using electron holography for phase imaging, as illustrated in Figure 2.12.

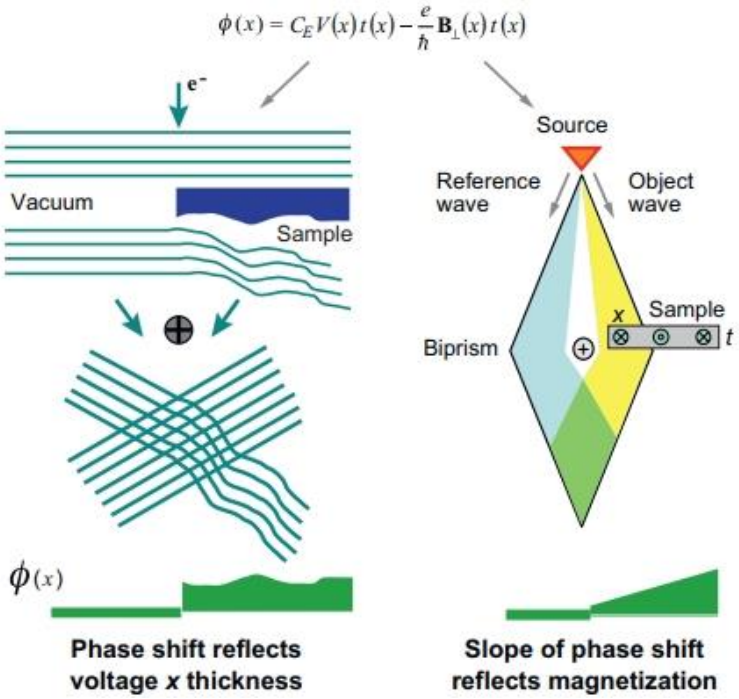

Figure 2.12 Schematic Illustration of the Origin of the Phase Shift to Quantify Electrostatic and Magnetic Potential [35].

In addition to FEG and biprism, a charge-coupled-device (CCD) camera is required in order to quantitatively analyze the electron phase shift. It allows holograms to be recorded by electron detectors that have linear output over a large dynamic range [33]. After the hologram was digitally recorded by a CCD camera, it was fed into the computer for phase reconstruction. The process of phase reconstruction to obtain amplitude and phase information in the hologram is shown in Figure 2.13 and will be discussed in the following section.

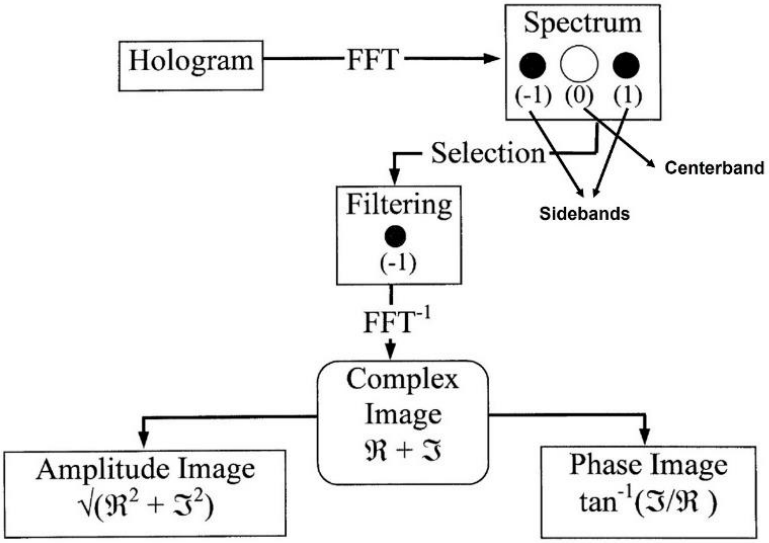

Figure 2.13 Schematic Illustration of the Phase Reconstruction Process [12].

2.2.2 Phase Reconstruction and Mapping

The electron wave from the hologram is restored as a numerical wave in the computer. The most common method for reconstructing the image wave is through the Fast Fourier transform (FFT) of the hologram, which creates a centerband and two sidebands. A centerband represents the diffractogram of a conventional electron micrograph, whereas sidebands correspond to the complex diffraction pattern which contains the information about the image phase that we need [13]. In order to eliminate the distortion-induced phase modulation during the reconstruction process caused by illumination, charging biprism, and CCD camera, another image from the vacuum was taken with the same parameters as the object hologram. This vacuum hologram serves as the reference hologram for the correction of the distortion-induced phase modulations. One of the sidebands from both the reference and sample FFTs is cut and moved to the center. After applying an inverse Fast Fourier transformation (IFFT), the information on the amplitude and phase can be

retrieved separately from the real and imaginary parts of the complex image. To achieve the distortion correction the IFFT of the object hologram is divided by the IFFT of the reference hologram, the wave transfer function of the complex image after IFFT is then given by [34],

$$ima(\vec{r}) = VA(\vec{r})e^{i\emptyset(\vec{r})}, \tag{2.7}$$

where V is the contrast of the fringe, $A(\vec{r})$ represents the amplitude image and $\emptyset(\vec{r})$ represents the phase image. The phase information from the complex image could be extracted with the following expression [34],

$$\emptyset(x, y) = \tan^{-1}\left[\frac{Im[ima]}{Re[ima]}\right], \tag{2.8}$$

where Im[ima] and Re[ima] are the imaginary and the real parts of the wave function, respectively. For phase images where the phase shifts are more than 2π due to the arctangent relationship between the imaginary and real wavefunction shown in Eq. 2.8, the phase is unwrapped with custom software. Using computer software, the reconstructed phase images can be expressed in the pseudo-color mode. Each color is cycled around 2π phase shift or arbitrary amounts if the phase is unwrapped.

CHAPTER 3

EXPERIMENT SETUP

In order to study the total ionizing dose effect in the MOS and MNOS devices, samples were fabricated at the ASU class 100 cleaning room. To conduct TID experiments, samples were packaged and exposed to radiation at the Gamma cell 220 irradiator facility at Arizona State University to reach a dose level of 500 krad. Capacitance-voltage (C-V) characteristics of the MOSCAP and MNOSCAP samples were measured after each dose step to measure the mid-gap voltage (V_{MG}) caused by TID. To map the charge distribution across the oxide layer of MOSCAPs, accurate measurements of electrostatic potentials by off-axis electron holography (EH) were carried out. Finally, charge distribution was extracted by performing 2D device simulations (TCAD) to match the potential profile for pre-and post-irradiated samples.

3.1 Sample Fabrication

Both MOSCAPs and MNOSCAPs were fabricated at ASU NanoFab, a class 100 cleaning room, on a 4-inch, thickness of 525 μm, P-type dope with Boron, and resistivity between 1 to 100. The structure for MOSCAP and MNOSCAP is illustrated in Figure 3.1.

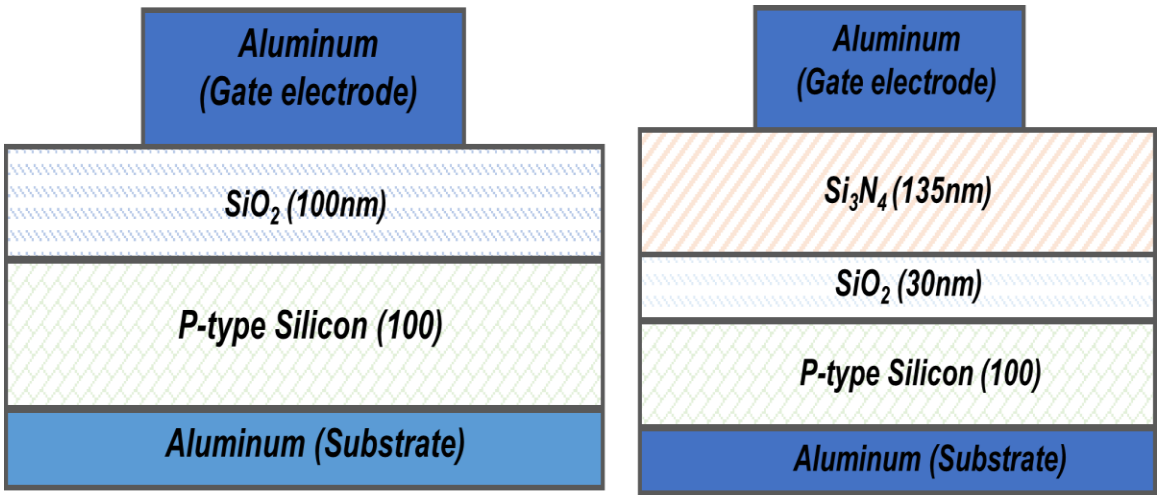

Figure 3.1 Schematic Structure of MOS (left) /MNOS (right) Capacitor.

All the wafers were cleaned by RCA to remove the native oxide and contaminations on the surface. Next, a layer of silicon dioxide was grown using the dry oxidation for MOSCAP, and a layer of Si_3N_4 was deposited on top of silicon dioxide using low-pressure chemical deposition (LPCVD) for the MNOSCAP samples. Soft baking was performed at 100°C for 5 mins to remove the moisture prior to the photolithography process. The process of photolithography is illustrated in Figure 3.2 Steps 1 to 3. A layer of lift-off resist (LOR) and a layer of positive photoresist (AZ4330) was coated on the top of the dielectric layer for 30 sec at 3500 rpm spin speed during the photolithography process. Samples were exposed under the light with a wavelength between 350 nm to 450 nm for 20 seconds. During exposure, a sheet of mylar mask, with patterns of different sizes and shapes, was covered on the top of the sample to define the gate area of the capacitors. Samples were developed with MIF 300 developer for 90 seconds to dissolve the photoresist that was exposed to the light directly. The chemical properties of AZ4330 will be changed after

exposed to light with a wavelength between 350nm and 450nm. Therefore, only the area that was exposed to the light could be dissolved with MIF 300 developer.

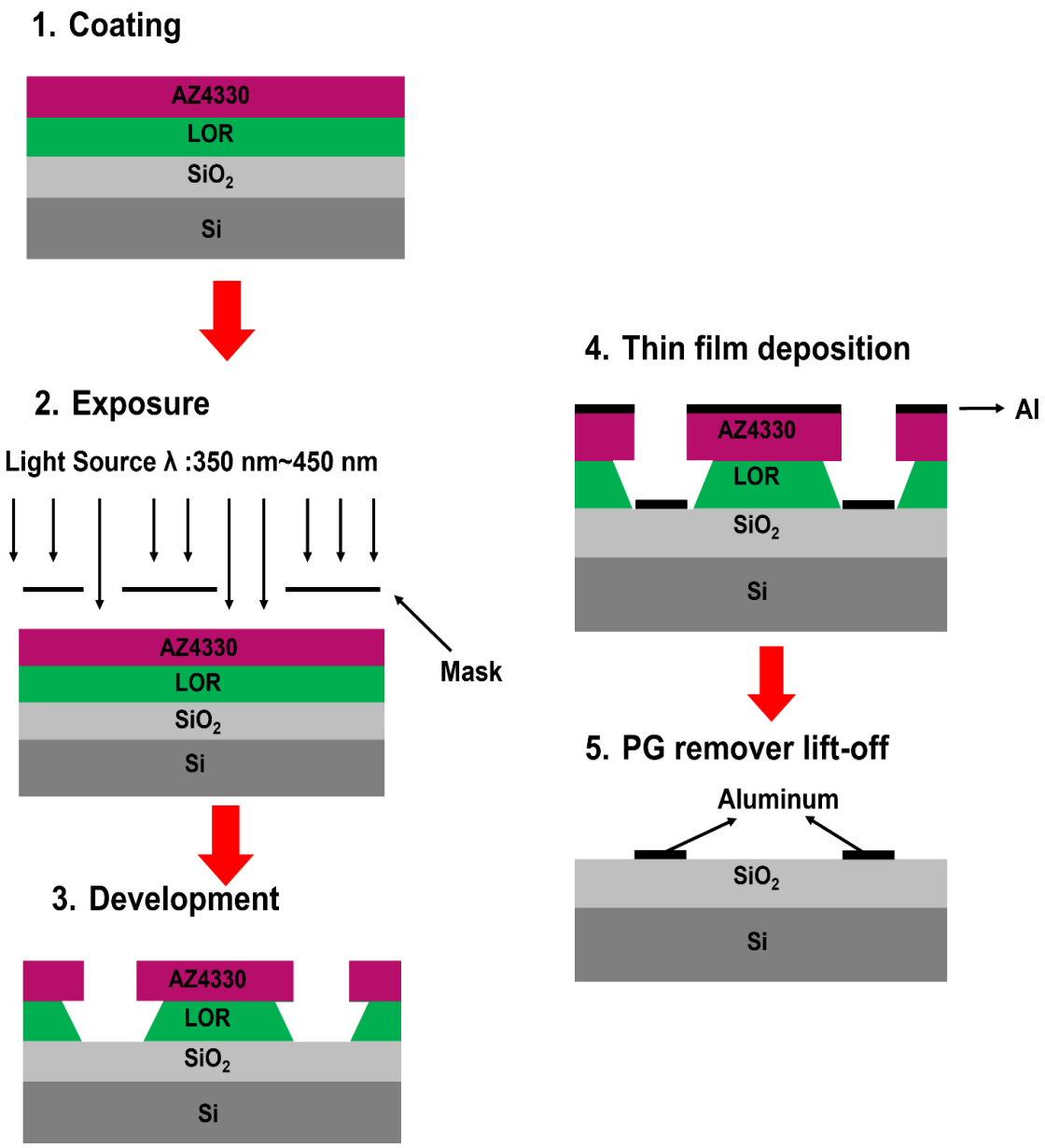

Figure 3.2 Schematic Illustration of Fabrication Process to Define Different Sizes of Gate Area.

A layer of aluminum of 150 nm was deposited on both sides of the sample using a Lesker e-beam evaporation tool as shown in Figure 3.2 Step 4. Aluminum was deposited

on the front side of the sample for the gate electrode and backside to form the p-silicon substrate contact. After the metal was deposited, the PG remover lift-off was performed to dissolve LOR, therefore, removing the aluminum that was not deposited on the patterns, as shown in Figure 3.2 Step 5. PG remover was heated to 80 ºC for two hours. With the help of LOR, by forming an undercut during the development process, a clean aluminum lift-off could be expected. At the last step of the fabrication process, rapid thermal annealing (RTA) at 380 °C for 2 minutes was performed in a forming gas environment to reduce the density of oxide charge (N_{OT}) and interface states (N_{IT}) in the samples.

To match the same equivalent oxide (SiO_2) thickness (EOT), the thickness of the Nitride-SiO_2 stack should be thicker than the oxide-only sample to get the same capacitance. This is because the permittivity of Si_3N_4 (7.5F/cm) is higher than that of SiO_2 (3.9F/cm). The equivalent oxide (SiO_2) thickness (EOT) for a given nitride thickness is given by,

$$T_{eq,oxide} = T_{nitride} * \frac{\varepsilon_{oxide}}{\varepsilon_{nitride}}, \tag{3.1}$$

where $T_{eq,oxide}$ is the equivalent SiO_2 thickness with the given Si_3N_4 thickness, $T_{nitride}$ is the Si_3N_4 thickness, ε_{oxide} is the permittivity for SiO_2, and $\varepsilon_{nitride}$ is the permittivity for Si_3N_4. The EOT for the SiO_2- Si_3N_4 stack is given by,

$$Total_{eq,oxide} = T_{eq,oxide} + T_{oxide}\,. \tag{3.2}$$

In this thesis, two different kinds of devices were fabricated and tested shown in Fig.3.1. Both of these devices have the same total EOT, which is 100 nm.

3.2 TID experiment setup

Radiation testing for all samples was performed at Arizona State University, using Gamma Cell 220 irradiator facility [By Dr. Keith Holbert]. Samples were exposed to Cobalt-60 gamma rays at a dose rate of 178 (rads/min) [SiO_2] until reaching a dose level of 500 krad at room temperature. During the radiation experiment, a 10 V gate bias was applied at the gate. Capacitors were diced and packaged into the dual in-line package to enable the application of gate bias during radiation. Each package contained eight dies and all of them were wire bonded to different pins. Packages for testing and a plane view of dies are shown in Figure. 3.3.

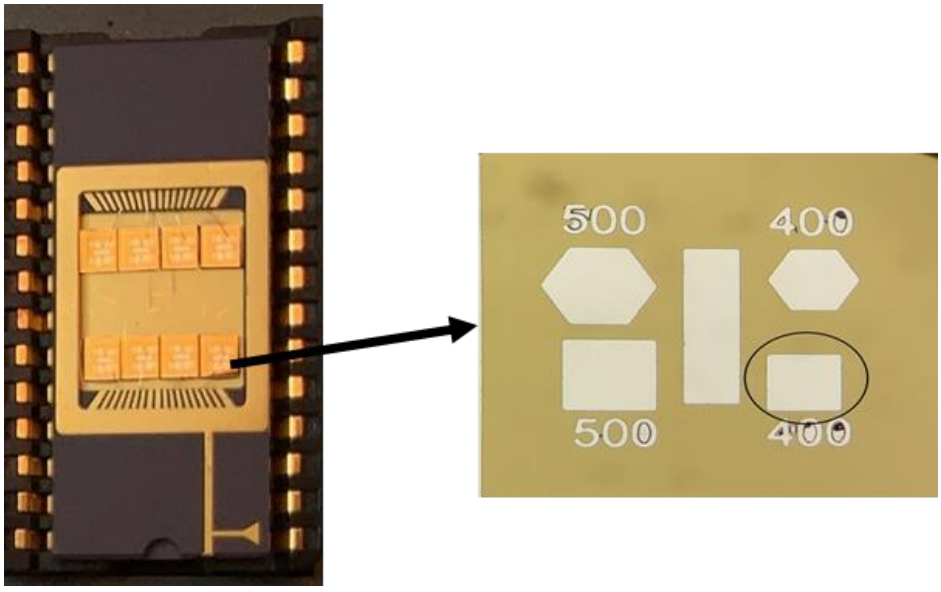

Figure 3.3 Packaged Device and Plane View of the Die.

3.3 Analysis Methods

The total ionizing dose effects in MOS and MNOS devices are studied through both electric and material analysis. CV measurements were performed to study the shift CV

curves after irradiation and electron holography and TCAD stimulation was performed to map the charge distribution across the pre-and post-irradiated oxide layer.

3.3.1 Capacitance-Voltage Measurements

In this study, we mainly focused on the shift of the mid-gap voltage (V_{MG}) caused by the TID effect. High-frequency capacitance-voltage (CV) characteristics at 1 MHz were carried out prior to irradiation and at dose steps of 50 krad, 100 krad, 250 krad, and 500 krad using an Agilent 4284A LCR meter and MDC software to collect the data, as shown in Figure 3.4, at room temperature under atmospheric pressure.

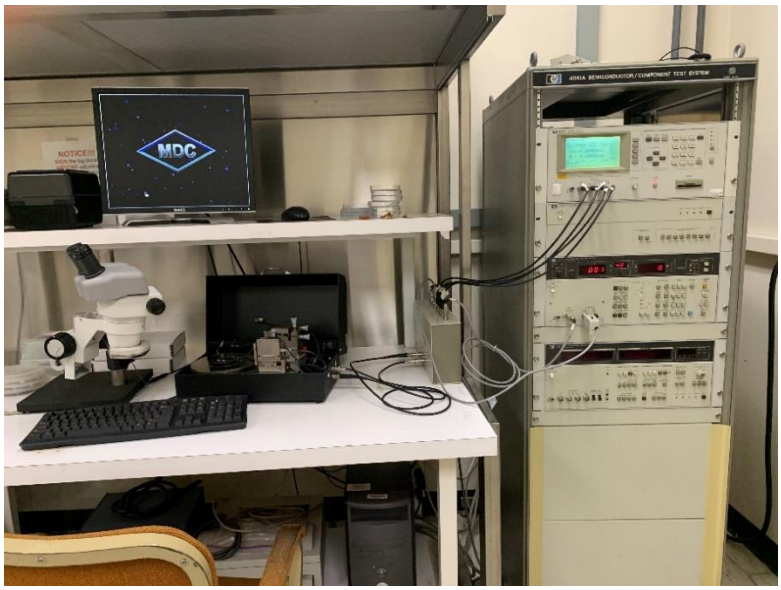

Figure 3.4 Capacitance-Voltage Measurements Setup.

3.3.2 Electron Holography Setup

In order to study the charges buildup in the oxide layer after irradiation, electron holography imaging was performed at ASU [by Dr. Martha McCartney]. The hologram was taken with the FEI Titan TEM equipped with a field emission gun, a biprism, and a

CCD camera at ASU Eyring Materials Center shown in Figure 3.5. To obtain accurate measurements of electrostatic potentials for the MOSCAPs using off-axis electron holography, sample preparation plays an important role. The sample needs to be prepared with uniform thickness to improve the accuracy of the interpretation of the reconstructed phase image. TCAD stimulation was performed to extract the charge density and distribution across the oxide film. Focused-ion-beam (FIB) milling was first performed to thin cross-sections of the samples. Before the milling process, the sample was deposited with platinum and carbon on top of the sample, as shown in Figure 3.6. Such cross-sectioning is essential when the device region or feature of interest is located below the sample surface. Furthermore, to prevent the sample from charging by induced electron beam emission of secondary electrons, the sample was coated with a layer of carbon before performing the electron holography (EH) study.

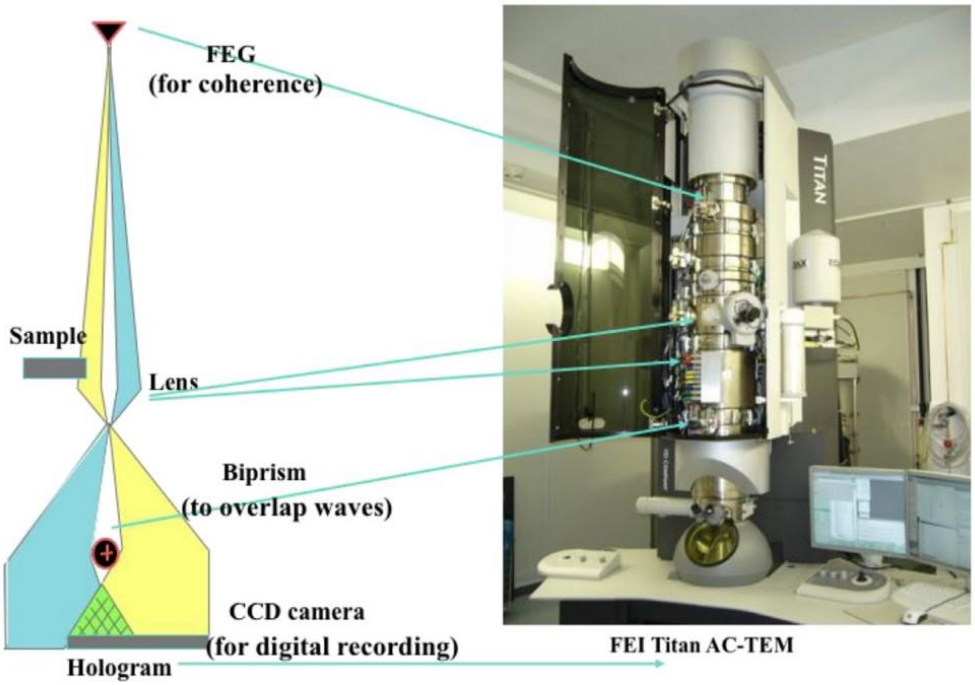

Figure 3.5 Electron Holography Setup for Titan TEM [11].

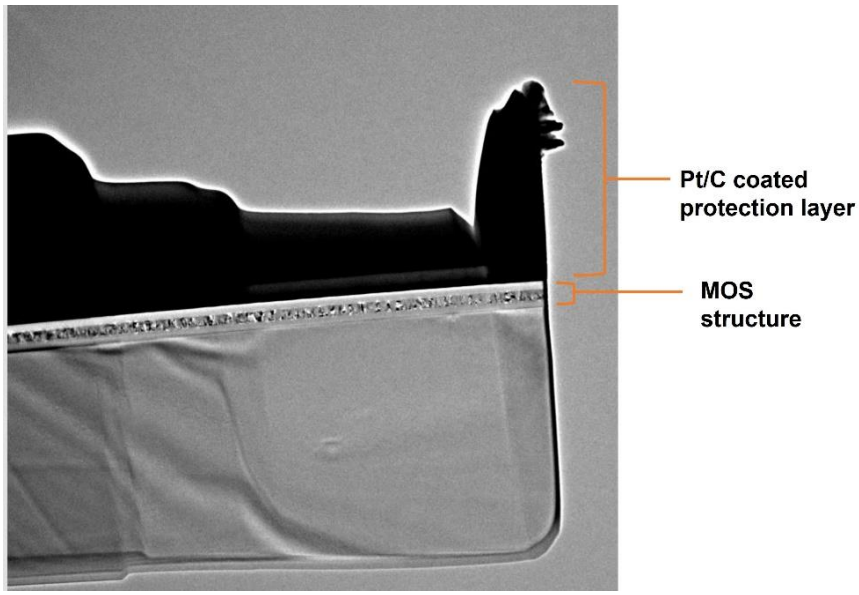

Figure 3.6 Cross-section of the MOS Sample before FIB Milling with Pt and C Deposited on Top of the Sample.

CHAPTER 4

RESULT AND DISCUSSION FOR ELECTRICAL CHARACTERIZATION

The work reported in this thesis can be divided into two main parts. The first part reports on the electrical characterization of TID effects focused on the shift of C-V curves for both MOSCAP and MNOSCAP devices. Shifts are observed in the CV curve after irradiation as expected. The second part reports on off-axis electron holography characterization and computer modeling will be discussed in the next chapter.

4.1 TID Experimental Result

4.1.1 Capacitance-Voltage measurements

Figure 4.1 and Figure 4.2 shows the normalized C-V curves for the MOSCAP and MNOSCAP samples with 0V and 10V bias during irradiation at different dose levels. The sample irradiated with 0V bias was reported previously in [36], [37]. The lines in different colors represent the CV measurements at each dose level. The TID response of the oxide-only sample shows a significant shift in the CV curve, to the left. Applying a 10 V bias during irradiation creates an even larger shift in the same direction. Moreover, the capacitance at the inversion region ($+V_{gs}$) increases for the condition with a 10 V bias. This increase did not show up for the 0V bias condition. The increase, discussed in section 4.1.3 below, may be due to the buildup of at or near interface traps that exchange charge with the underlying silicon when the surface is in inversion. Concerning the TID effects observed on nitride-oxide stack devices, with 0V bias, there is a negligible shift in the C-V curve. However, with a 10V bias during irradiation, the C-V curve shows a shift to the right. In addition, the capacitance at the inversion decreases as TID increases. At 500 krad,

the capacitance at the inversion reaches the theoretical minimum. The reasons for this reduction will also be discussed in section 4.1.3.

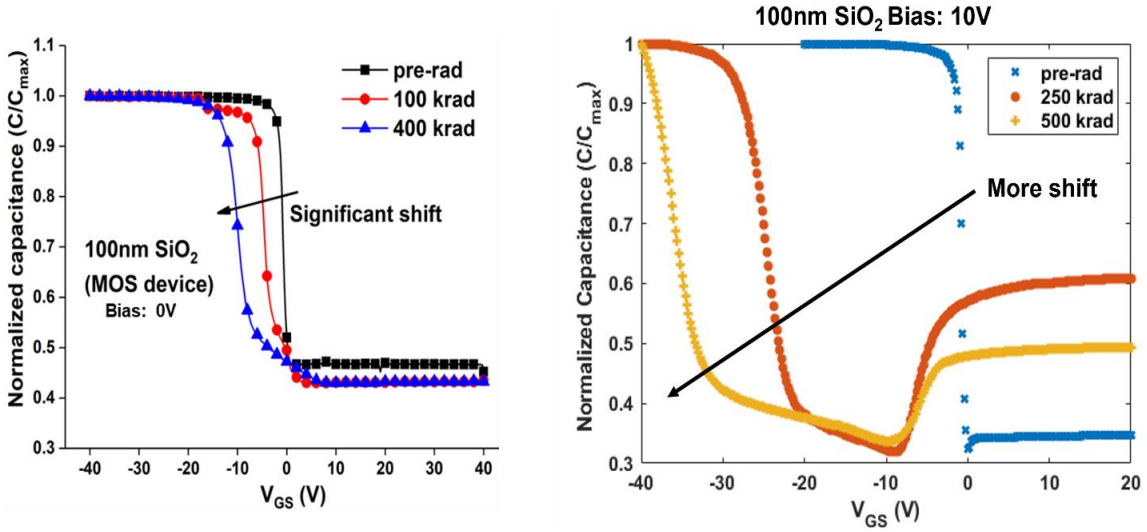

Figure 4.7 Schematic Structure of MOS (left) /MNOS (right) Capacitor.

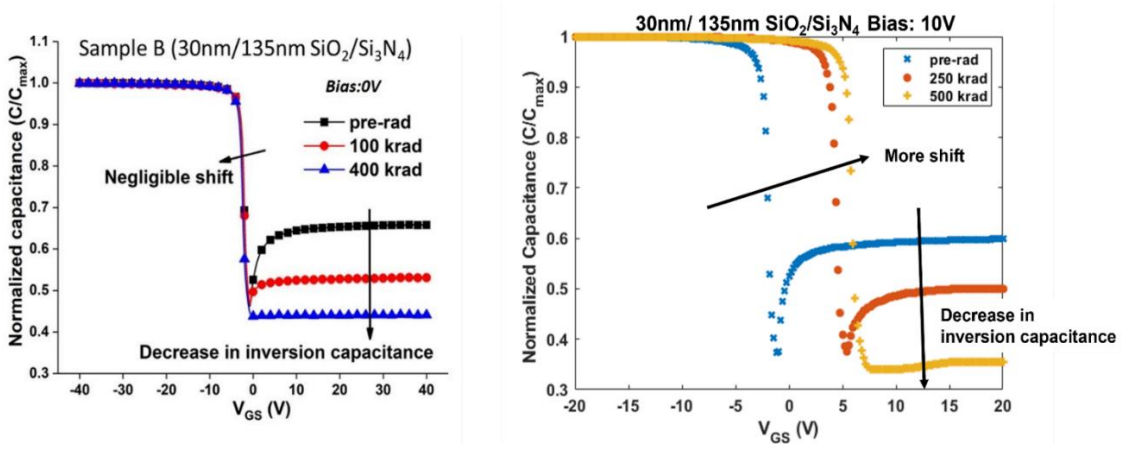

Figure 4.8 C-V Characteristics of MNOSCAPs for Different Dose Levels and Bias Conditions.

Figure 4.3 shows the voltage shift at the capacitance of 40 pF for MOSCAPs and MNOSCAPs with different bias conditions during irradiation. The data shows that the nitride layer provides better tolerance to the TID effect, resulting in less voltage shift. Moreover, with a 10 V bias applied for both oxide and oxide-nitride samples during

irradiation, there is a larger voltage shift compared with 0 V bias. For the case of oxide only samples, the total negative shift for a 0 V bias is around 9V, and it is around 37 V shift for a 10V bias condition. For the case of oxide-nitride stack samples, the total positive shift for the 10 V bias condition is around 6.5 V. Interestingly, the voltage shifts are in different directions for the two different samples. The oxide-only capacitor experiences a negative shift, whereas the oxide-nitride stack capacitor has a positive shift with positive bias during radiation testing. In the following two sections, the TID behavior of the capacitors will be discussed. TCAD simulations and off-axis electron holography are performed to support the discussion.

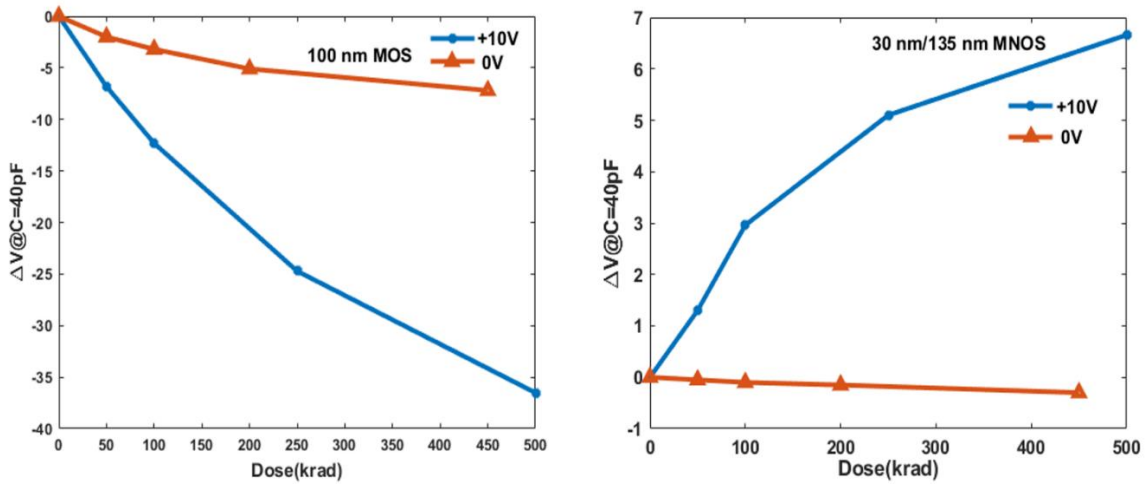

Figure 4.9 Voltage Shift for 100nm MOS and 30nm/135nm MNOS at C=40pf for 0V and 10V Gate Bias During Irradiation.

4.1.2 Effect of Trapped Charges (N_{OT})

When capacitors are exposed, electron-hole pairs will be induced into both oxide and nitride layers. Using the mid-gap voltage technique [26], the densities of N_{OT} created during irradiation can be extracted for each dose level. The schematic charge distribution

across the oxide layer after irradiation for both 0V and 10V bias conditions is shown in Figure 4.4. For the oxide only samples, net positive charges are trapped at the oxide layer for both 0 V and 10 V bias conditions. Electrons generated by the ionization of SiO_2 in the oxide layer will move toward the metal due to the presents of intrinsic and applied fields. On the other hand, holes generated in the oxide transport much slower than electrons through the oxide film, and toward the Si interface [36]. Due to the work function difference and applied voltage in the case of the 10V bias, the electric field points toward the Si substrate. Thus, positively charged holes move toward the Si. Near the Si/SiO_2 interface, a fraction of the holes is trapped at defect precursors, mostly likely oxygen vacancies [22]. Thus, fixed trapped charges near the Si/SiO_2 interface are positive after irradiation for MOS devices. The positive N_{OT} buildup causes the voltage shift of the C-V curve negatively. This is consistent with what we observed in Figure 4.1, showing negative shifts in the C-V curve for 100 nm MOS capacitors after radiation testing.

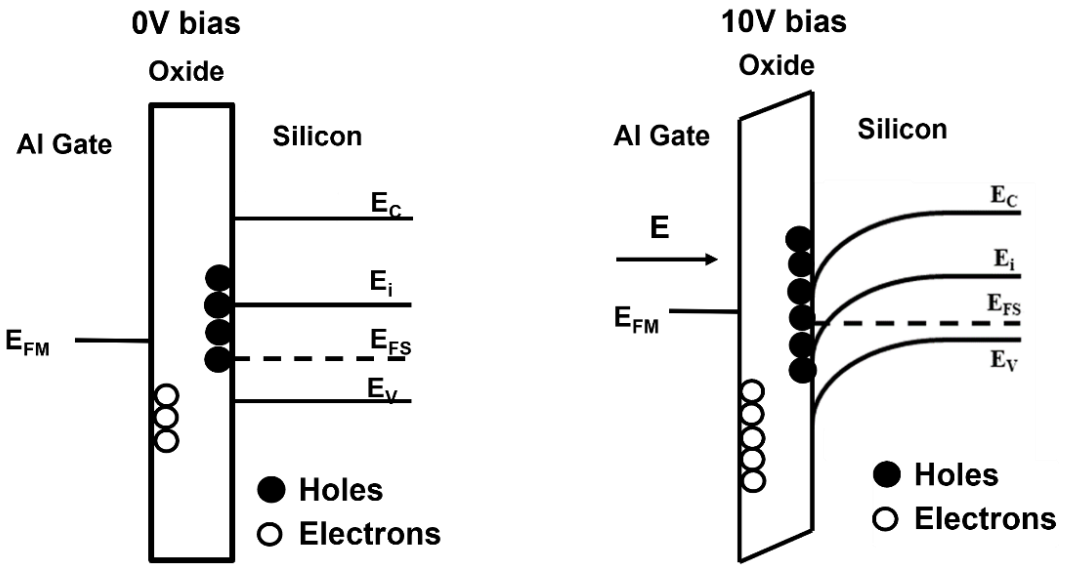

Figure 4.10 Schematic Illustration of Charge Distribution Across Irradiated Oxide Film for MOSCAPs Under 0V and 10V Bias Condition.

Compared with the 0V bias condition, there are more holes trapped in the oxide with the 10V bias condition shown in Fig. 4.5, which is not surprising since the external field created by the positive bias enables holes to avoid recombination in the oxide film. In Figure 4.5, the orange line represents the 0V bias condition, and the blue line represents the 10V bias condition. The number of holes that are trapped in the oxide film is dependent on the applied field. For the metal-gate capacitors, hole density increases with the increase of the electric field.

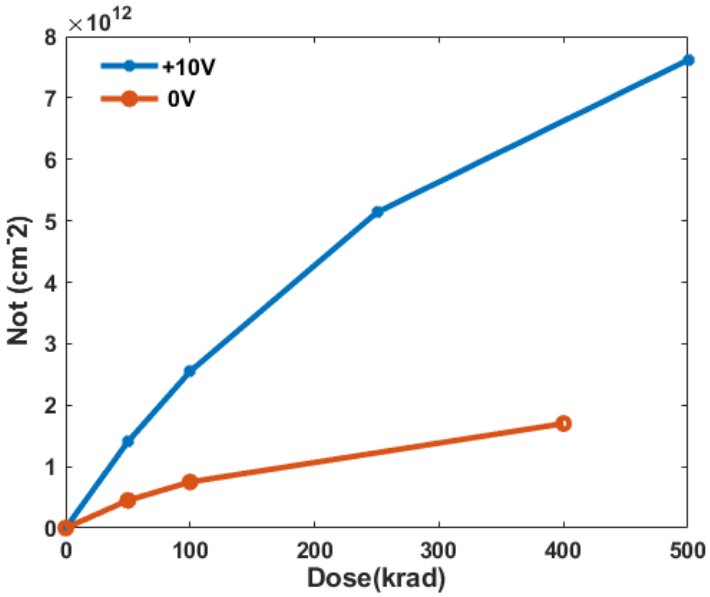

Figure 4.11 N_{OT} for 100 nm MOSCAPs at Each Dose Steps for 0 V and 10 V Bias

Figure 4.6 shows the N_{OT} buildup at each dose step for MNOS samples for 0V and 10V gate bias conditions during irradiation. For the 0V bias, we hypothesize that due to the work function difference between the Si substrate (4.85V) and the Aluminum gate electrode (4.1V), there is little intrinsic electric field pointing toward the gate. Little concentration of electrons and holes were trapped in the oxide layer, causing a negligible shift of the C-V curve. For the 10 V gate bias condition, electrons generated in the oxide will move toward the oxide-nitride interface and get trapped [14]. The holes generated in the nitride move toward the oxide/nitride interface and get trapped due to the presence of hole trapping precursors [14]. Holes generated in the oxide will move toward the Si substrate and be trapped near the bulk Si or Si/SiO_2 interface. We hypothesize that more electrons than holes get trapped; thus, the net charge for the trapped is negative for the MNOSCAPs with positive gate bias applied. Figure 4.7 shows a proposed illustration of the energy band diagram of MNOSCAPs with the positive bias condition. The figure shows

the balance of trapped charges for radiation-induced electrons and holes. The black circles represent the holes, and the white circles represent the electrons.

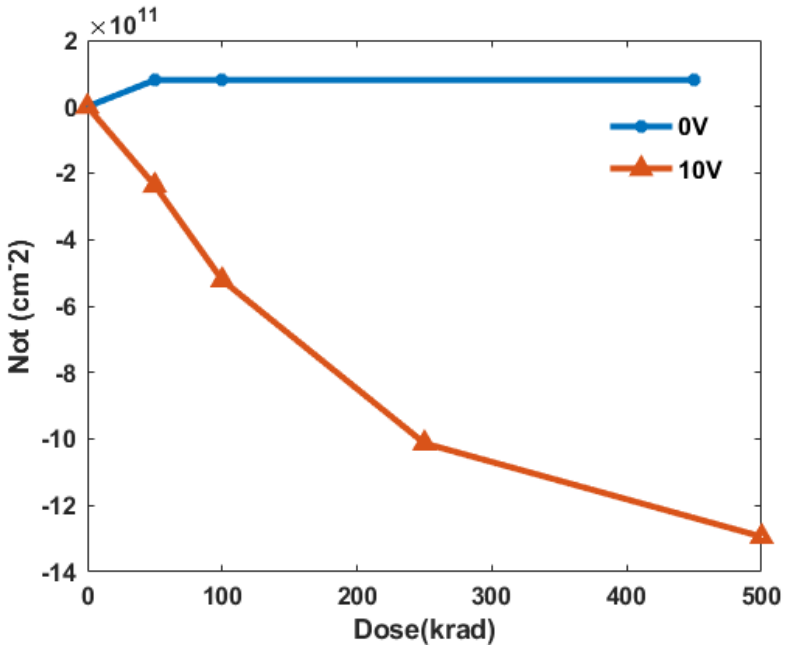

Figure 4.12 Oxide Trap Buildup for MNOSCAP with 0V and 10V Bias Conditions.

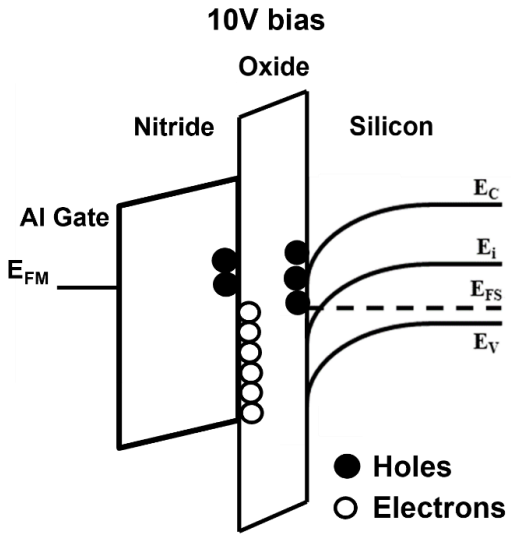

Figure 4.13 Energy Band Diagram for MNOSCAPs Under Positive Bias Condition and Electrons and Holes Distribution.

4.1.3 Effect of Shallow Traps

In Figure 4.2, we can also observe the capacitance increase at inversion (+Vgs) for the MNOSCAPs. Capacitance at inversion did not reach the theoretical minimum shown in Figure 4.8.

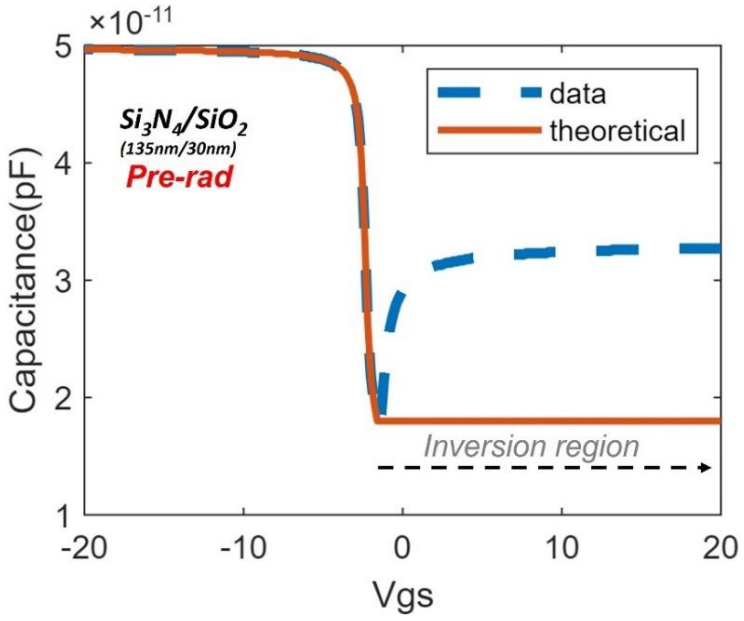

Figure 4.14 Comparison Between Measured Cmin and Theorical Cmin for MNOS Devices.

When the conduction band of Si is inverted, the increase of the capacitance could be caused by the high density of traps present in the upper part of the Si bandgap [38], a shallow trap. The capacitance due to traps charging (C_{IT}) will increase as the shallow trap density increase with function 4.1 [38],

$$C_{IT} = q * D_{IT,} \tag{4.1}$$

where D_{it} is the density of shallow traps. The additional C_{IT} was placed in parallel to the substrate capacity as shown in Figure 4.9. The total capacitance of the MNOS system, including the effect of shallow traps will be,

$$C_{total} = \frac{C_{ox}[C_s + C_{it}]}{C_{ox} + [C_s + C_{it}]} \tag{4.2}$$

C_{OX} is the oxide-nitride stack capacitance and C_S is the substrate capacitance formed across the maximum depletion width in silicon during inversion.

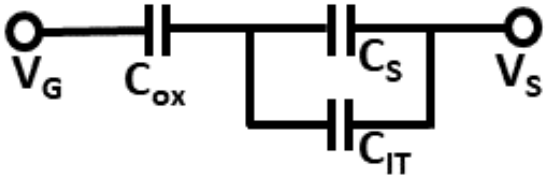

Figure 4.15 Schematic of Circuit Model Due to Additional Interface Traps Parallel to the Substrate
Capacity for MNOS Devices.

The increase of the capacitance at the inversion region could be simulated with the TCAD. The MOS capacitor structure built in the TCAD represents the fabricated device with the same structure, same doping concentration, and metal type shown in Figure 4.10.

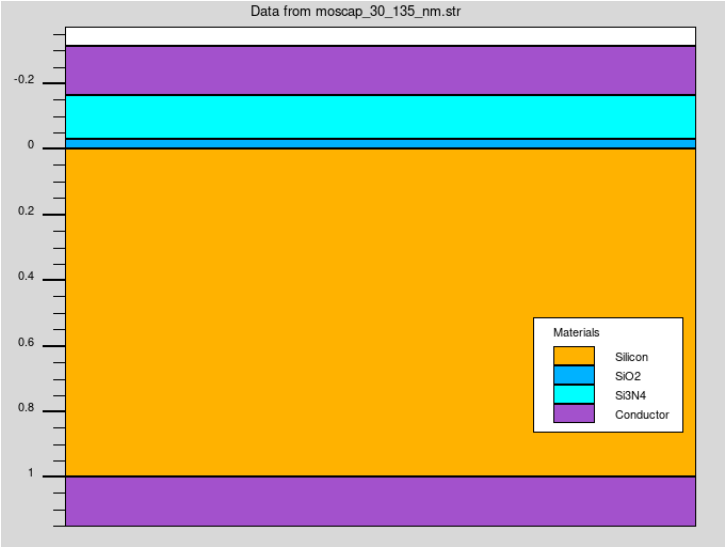

Figure 4.16 TCAD Structure for 135nm/30nm the MNOSCAP.

By adding acceptor-like interface traps at a discrete energy level near the conduction band with the Heiman model, the increase of capacitance at inversion could be observed [39], [40]. The Heiman model allows the electrons near the conduction band to fill the traps near the Si/ SiO_2 by tunneling mechanism when a high positive gate -source voltage was applied [41]. To match the data with TCAD simulation, a density of $8x10^{13}$ cm^{-2} spatially distributed acceptor-type interface traps was added to the interface of Si/SiO_2. Traps were located at the energy level of 0.01 eV below the conduction band energy. Figure 4.11 shows the terminology used to define the type of trap in TCAD.

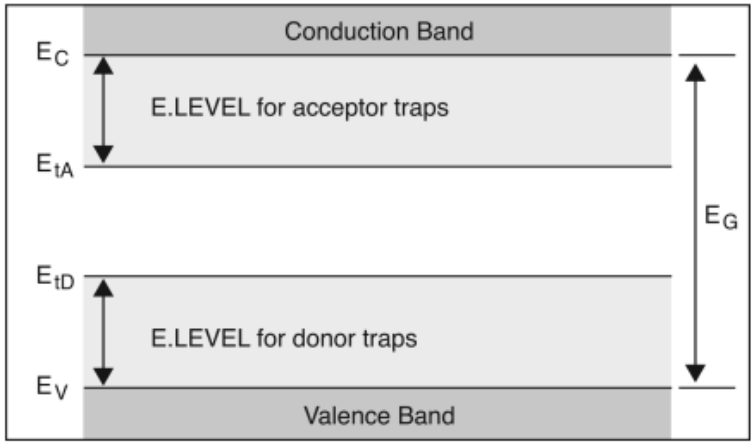

Figure 4.17 The Definition of the Trap Energy Level of Acceptor Traps in Reference to Conduction Band [39].

The simulation results shown in Figure 4.12 are overlaid with the data from CV measurements. In Figure 4.12, the blue dash line represents the TCAD modeling result using the Heiman model, and the orange dots represent the measurement data. With the Heiman model, we are able to closely match between the data and simulation. Therefore, it can be said that the increase of the capacitance at the inversion for MNOS capacitors is caused by the high density of spatially distributed shallow interface traps at the oxide layer.

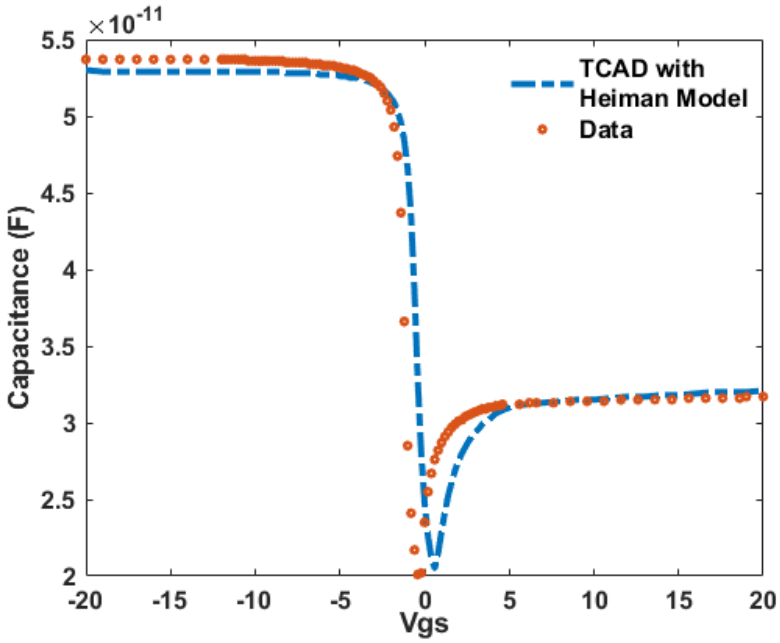

Figure 4.18 Pre-rad C-V Data for MNOSCAP and the Modeling Result with Heiman Model.

In Figure 4.2, it can be observed that the capacitance for the MNOSCAPs at inversion decreases with the increase of TID. This may be due to the decrease in shallow traps. The decrease in interface traps is the opposite of what is observed in the MOSCAPs, which shows that the increase in TID will lead to the buildup of shallows traps. This may be attributed to the de-passivation of Si dangling bonds at the interface [42], [43]. It should be noted that the probability of carrier capture and release is a function of the frequency of the CV measurement. Presumably at very high frequencies, i.e., above the standard 1MHz setting selected, there would be less of an increase in capacitance in inversion. This is because the voltage switching frequency would be much greater than the inverse time constant of carrier capture and emission.

CHAPTER 5

RESULT AND DISCUSSION OF ELECTRON HOLOGRAPHY

In this chapter, we report on off-axis electron holography characterization and computer modeling will be discussed in the next chapter. In the first part, traps built up in the oxide layer can be imaged by hologram. In the second part, the concentration of traps could be extracted through the use of TCAD simulation by matching the potential profile extracted from the electron holography.

5.1 Off-Axis Electron Holography Result

The off-axis electron holography technique uses a transmission electron microscope (TEM) to provide quantitative access to phase shifts experienced by an incident electron wavefront due to the interactions with the electrostatic and magnetic potentials with the sample. Electron holography was developed by Dr. Martha McCartney from ASU. In this study, measurements of electrostatic potential variation across the Si/SiO_2 for the pre-and post-irradiated devices were performed. A hologram is obtained by superimposing a reference wave on an object wave. This superimposition region is filled with interference fringes which contain both amplitude and phase information. Figure 5.1 (a) shows an example of a hologram obtained on the MOS capacitor. To eliminate the phase changes caused by the field emission gun (FEG) and charge-coupled device (CCD) camera, another hologram is recorded from the vacuum using the same conditions for the sample hologram, as shown in Figure 5.1 (b). The hologram is then digitally recorded by a CCD camera and a Fast Fourier Transformation (FFT) was carried out to produce a

central auto-correlation peak and two sidebands, shown in Figure 5.1 (c). One of the sidebands from Figure 5.1 (c) is extracted as both sidebands contain the same phase and amplitude information we need as shown in Figure 5.1 (d). The complex image was reconstructed by the Inverse Fast Fourier Transform (IFFT) of the sideband extracted. The IFFT was applied on both sidebands extracted from the FFT of the sample hologram and the FFT of the reference hologram. The resulting complex image was divided to subtract any phase shift caused by the biprism or the illumination. The phase image shown in Figure 5.1 (e) can be retrieved from the reconstructed complex image by Eq. 2.6, taking an arctangent of the imaginary and the real part of the complex image. The reconstructed phase image can be expressed in the pseudo-color mode by computer software as shown in Figure 4.14 (f). Each color cycle around 2π phase shifts due to the arctangent relationship in Eq 2.8. The constant of color across each layer indicates the evenness of thickness across the sample. The color of the metal gets brighter as it gets thicker.

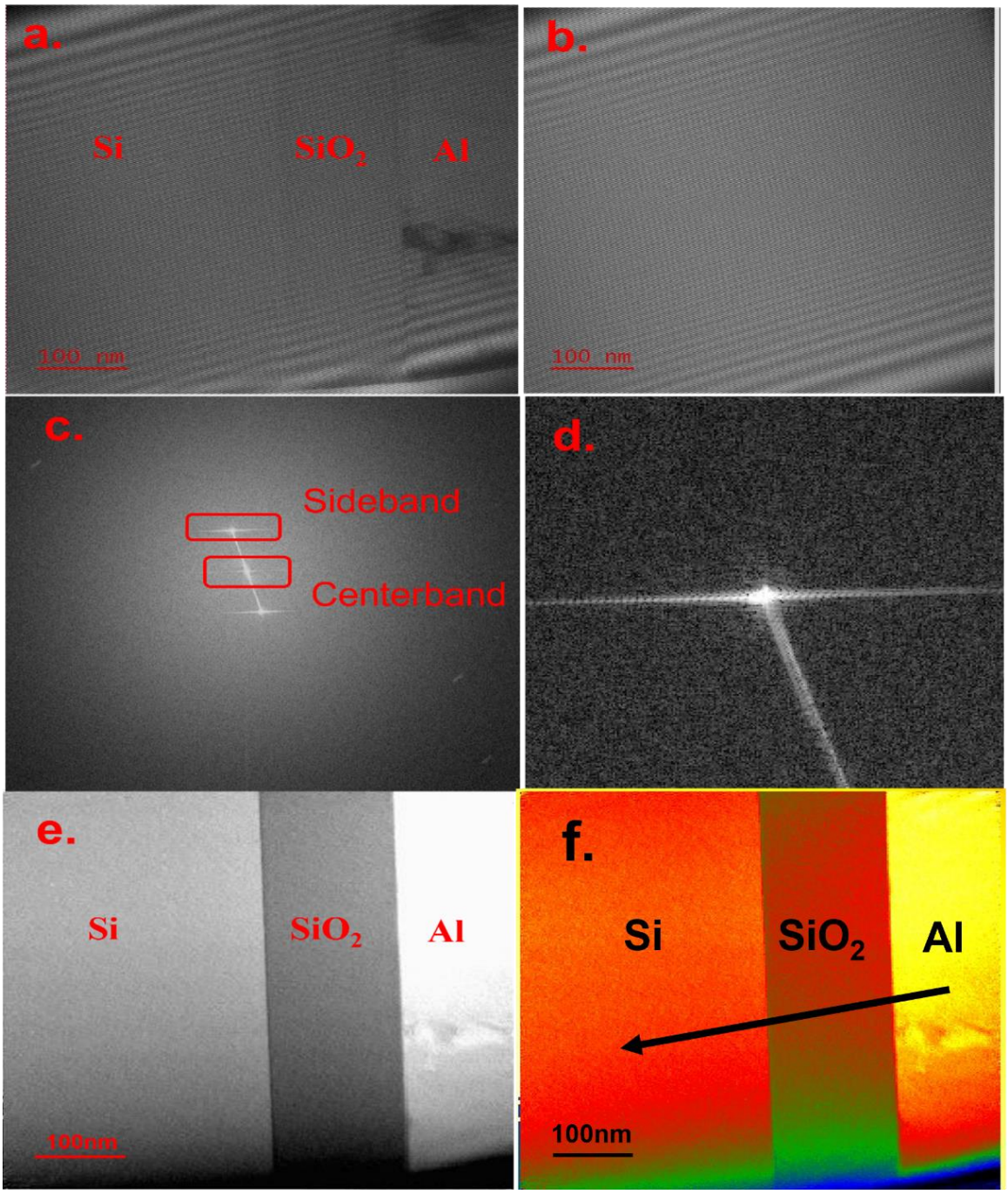

Figure 5.19 Image Reconstruction Process from Hologram Images to Extract the Phase Image of Pre-Irradiated Si/Sio_2 MOSCAP Sample. Arrow in (F) Indicates the Direction of Analysis.

The relationship between the holographic phase shift (ø) and the electrostatic potential (V), assuming that the sample under consideration is not strongly diffracting, is given simply by [35]

$$\Phi = C_E V t \tag{5.1}$$

where C_E is an interaction constant that depends on the energy of the incident electron beam, V is the electrostatic potential and t is the projected sample thickness. C_E has the value of 6.53 mrad/(V.nm) at a microscope accelerating voltage of 300 kV [35]. Figure 5.2 is the linear potential profile across the pre-irradiated sample extracted from the phase measurement.

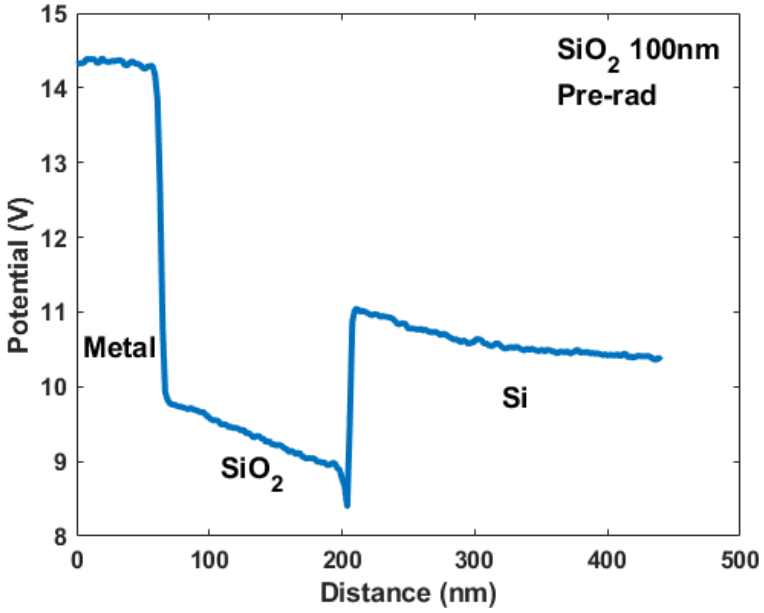

Figure 5.20 Potential Profile Measured Across the Pre-Irradiated Sample.

The mean inner potential of the Si is 12 V [44], whereas the potential observed for Si here is 11 V. This difference may be due to uncertainty in the Si thickness profile. The

potential drop across the SiO_2 layer is observed to be 0.7 V across the ~100nm film. The expected voltage drop for Si/SiO_2 interface is ~2 V [44]. The observed drop is 2.6 V. According to Poisson's equation, we can find the relation between the electrostatic potential (V) and charge distribution ($\rho(x)$) shown in Eq. 5.2,

$$-\frac{d^2V}{d^2x} = \frac{\rho(x)}{K_s \in_0} \tag{5.2}$$

where K_s is vacuum permittivity and $\in_0$ is the relativity permittivity of materials.

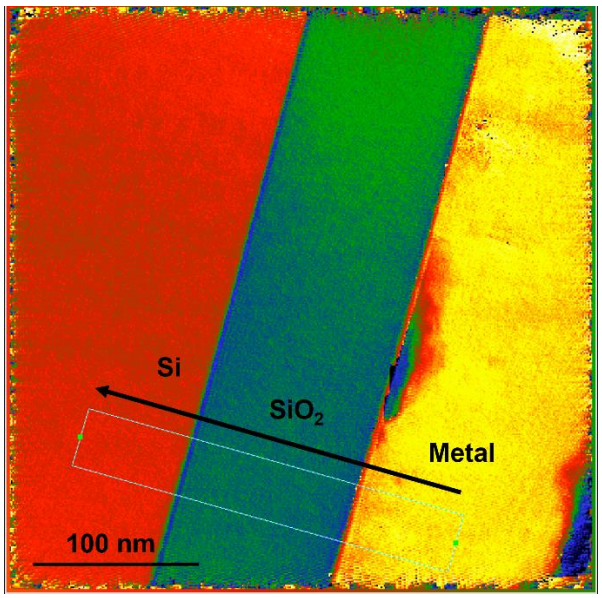

Figure 5.21 Phase Image of Irradiated Si/Sio_2 the MOSCAP Sample. Arrow Indicates the Direction
of Analysis.

Fig. 5.3 shows the reconstructed phase image of the irradiated sample and Fig. 5.4 plots the accompanying potential profile measured. By comparing Figs. 5.2 and 5.4, we observe that the potential drop across the SiO_2 layer has changed significantly after exposure. As will be discussed in the next section, the "flattening" of the potential indicates

that positive charges at Si/SiO_2 interface have increased, as expected, after TID. This correlates to results shown in the C-V data in Fig. 4.1 with 0V bias. Another interesting observation is the 2nd order reduction in the potential near the SiO_2/Metal interface. This is evidence of electron trapping on the metal side of the oxide film. This measure of trapped charge is mostly inaccessible in conventional I-V and C-V measurements due to its close proximity to the metal terminal relative to the semiconductor.

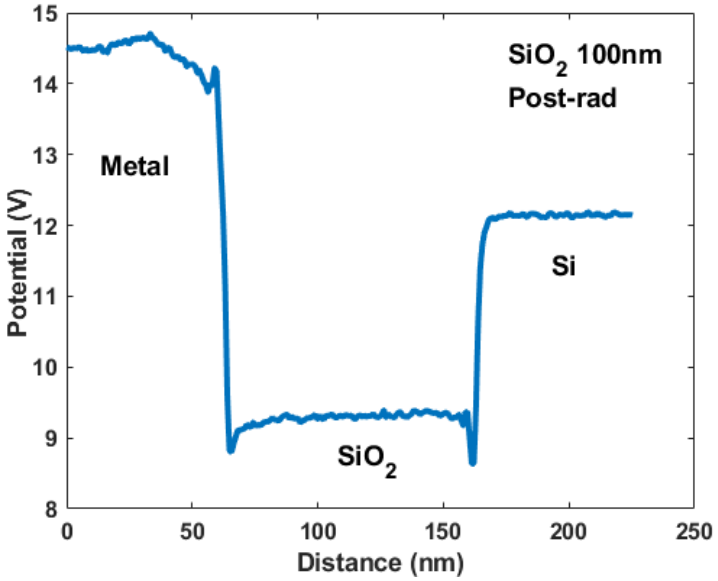

Figure 5.22 Potential Profile Measured Across the Irradiated Sample.

5.2 TCAD Device Stimulation

To validate these holography results 2D TCAD device simulations were performed on a MOSCAP structure representative of the fabricated device. This included matching the p-type Si doping concertation, oxide thickness, and metal type (Al) shown in Figure 5.5 (units μm). TCAD simulations were performed with Silvaco's Victory Device code [45].

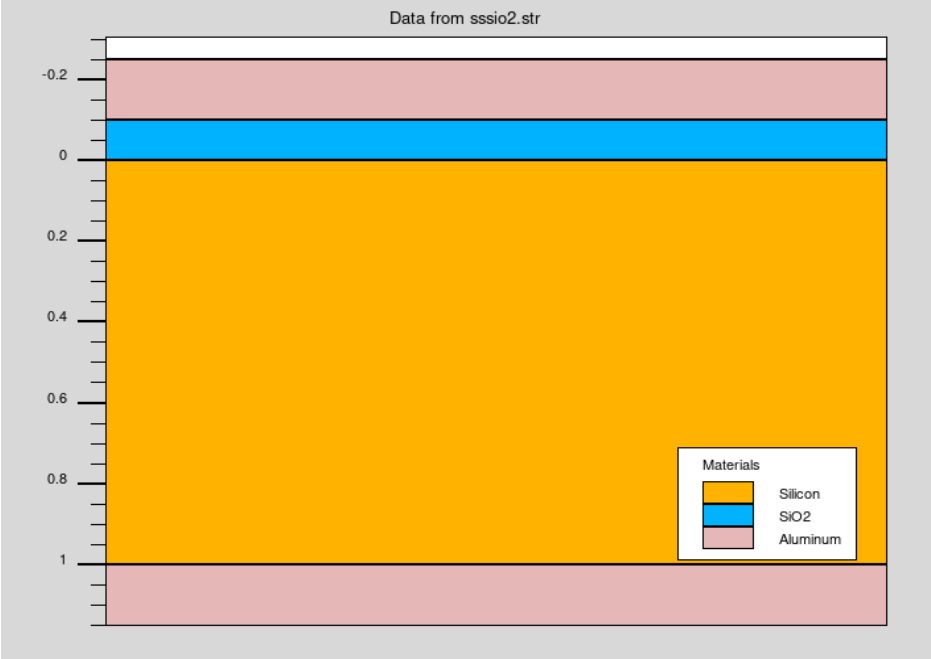

Figure 5.23 TCAD Structure for the 100 nm MOS Capacitor.

Figure 5.6 plots the potential profile in the p-silicon and, most importantly, the SiO_2 layer, obtained from the simulation (orange line). In order to match the holography data (blue symbols), a uniform volumetric layer of net positive charge of density $3x10^{18}$ cm^{-3} was added extending the Si/SiO_2 interface to a 5nm depth within the oxide. The charge profile (units cm^{-3}) for the pre-irradiation simulation is plotted in Fig. 5.7 (blue line).

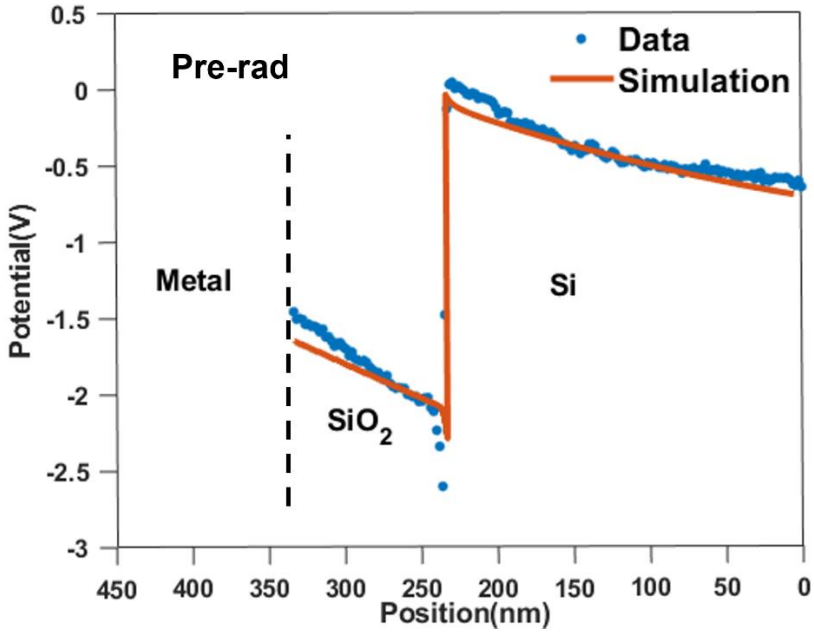

Figure 5.24 Overlay of Holography and TCAD Simulation Result of Pre-Irradiation 100nm MOSCAP Potential Profile.

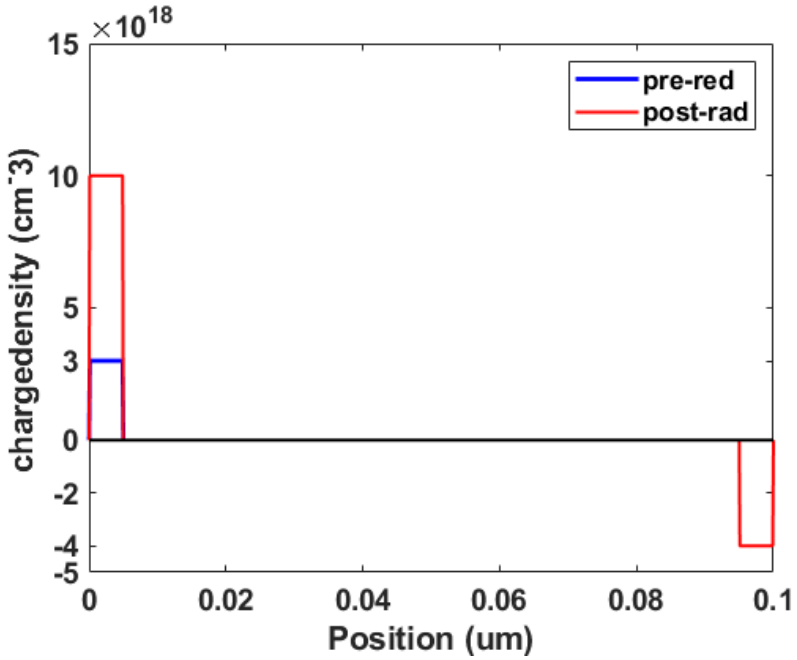

Figure 5.25 Charge Distribution Across 100 nm Sio_2 Used in the TCAD Simulations for Pre- and Post- Irradiation MOSCAPs.

Additional TCAD simulations were performed to match the 450 krad [Si] irradiated sample's holography data. Figure 5.8 plots the potential profile from the post-rad simulations (orange line) along with the data (blue symbols). To obtain good matching, a uniform layer of positive charge, 5nm from the Si/SiO_2 interface was increased to 10^{19} cm^{-3}. The increase in this near interface volumetric charge is consistent with the C-V results and causes the flattening of the potential in the oxide that was observed with holography. Additionally, the 2^{nd} order reduction in the potential near the metal interface was fit by adding net negative volumetric charge uniformly within 5nm from the gate metal. The density of this negative charge was $4x10^{18}$ cm^{-3}. The charge profile (units cm^{-3}) for the post-irradiation simulation is included in Figure 5.7 (red line). The good matching between data and model provides evidence of the efficacy of the electron holography technique in providing, for the first time, a direct image of charge buildup in irradiated oxides. In the future, we would like to perform electron holography with MNOS devices to map the charge distribution and compare pre-and post-irradiated devices, to verify our hypothesis on the charge distribution across the oxide/nitride layer.

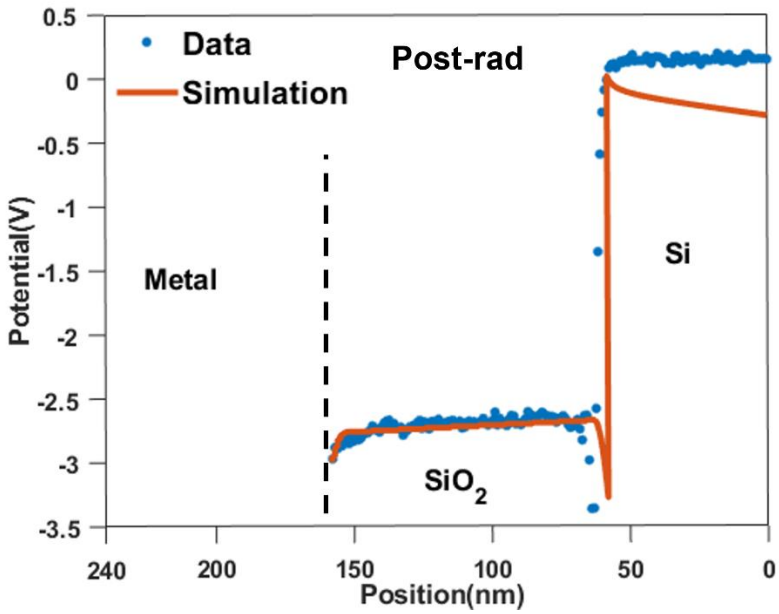

Figure 5.26 Potential Measurement and Modeling Across the Post-Rad Sample.

CHAPTER 6

CONCLUSIONS

This work presents test results and a new imaging methodology for total ionizing dose (TID) effects on Metal-Oxide-Semiconductor capacitor (MOSCAP) samples that use different dielectric stacks. All samples were fabricated in the ASU class 100 cleanroom and were exposed to ionizing radiation up to a target total dose of 500 krad [SiO_2] at the dose rate of 170 rad [SiO_2]/min using a Cobalt-60 source. Two different kinds of devices were fabricated: 1) a 100 nm SiO_2-only MOS capacitor (MOSCAP) and 2) a 30 nm SiO_2/ 135 nm Si_3N_4 stack MOS capacitor (MNOSCAP). The TID irradiations were performed with a positive bias applied at the gate terminal during exposure and at room temperature. To study the TID effect after irradiation, electric and materials analysis were performed. Capacitor-voltage (CV) measurements were performed at different dose steps to focus on the voltage shift caused by the total ionizing dose effect. Electron holography was performed to image the electrostatic potential across the MOS capacitors (MOSCAP) for pre- and post-irradiated samples of both types. A technology computer-aided design (TCAD) simulation was performed to analyze and validate the potential data from holography and also, to quantify charge distributions across the oxide layer prior to and after irradiation. The work reported here is the first time, electron holography analysis has been used to quantify the volume charge distribution in MOS dielectric films after irradiation. This is also the first time we are able to find the buildup of trapped electrons at the oxide film near the oxide/Al interface.

When the devices are exposed to ionizing radiation, electron-hole pairs are generated in the dielectric layer. For the oxide-only samples, the C-V curves shifted to the left after exposure (with a positive bias applied) because of the net positive charges trapped at the oxide layer. On the other hand, for nitride/oxide samples, the C-V curve shifted to the right due to the net negative charges trapped at the oxide layer. It was also observed that the C-V curve has less shift in voltage for MNOS than MOS devices after irradiation.

To quantify the number of charges induced after irradiation, charge separation techniques were performed. These techniques allow for the extraction of oxide trap concentrations (N_{OT}) across the oxide layer. When comparing the case of 0V bias and 10V bias during irradiation, after 500 krad [SiO2], both MOS and MNOS devices showed higher N_{OT} concentration when 10 V bias was applied. This is because a positive external bias from the gate to the silicon substrate during irradiation reduces electron-hole recombination, which allows holes generated in the oxide to escape capture and transport toward the interface where they can get trapped. For the MNOS case, more free electrons in the oxide layer get trapped at the oxide/nitride interface when a 10 V bias is applied.

In order to prove the charge build up in the irradiated oxide layer for MOSCAPs, the charge distribution across the oxide layer was mapped using off-axis electron holography and this helped in observing the electrostatics potential across the MOSCAP samples. For the pre-irradiated samples, a potential drop at the Si/SiO_2 interface was noticed, which indicates the presence of positive charge buildup at the Si/SiO_2 interface. A minor increase in potential across the Si layer revealed that there are some positive

changes created during processing. Analysis of the post-irradiated samples shows a larger potential drop at the Si/SiO_2 interface. This indicates that there are further positive charges that buildup after the TID exposure. In addition, there is also a small non-linear change in potential observed at the SiO_2/Metal interface, which is likely due to the accumulation of negative charges. TCAD modeling was used to extract the density of charges accumulated near the SiO_2 / Si and SiO_2 / Metal interface by matching the simulation results to the potential data from holography. The increase of near-interface positive charges in post-rad samples is consistent with the C-V results and causes the flattening of the potential in the oxide that was observed with holography.

This study demonstrates our ability to directly image the charge accumulation in the oxide film of MOS devices after irradiation. Future research will involve electron holography with MNOS devices to map the charge distribution and compare pre- and post-irradiated devices, with the aim of verifying our hypothesis on the charge distribution across the dielectric layer. These findings allow us to prove there is less charge buildup in the dielectric compared to MOS devices and thus, have a better tolerance to the TID effect.

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