Wide Bandgap Semiconductor Based Electric Vehicle Charging Systems: Modeling, Magnetics, and Control

by

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ABSTRACT

Adhering to an ever-increasing demand for innovation in the field of onboard electric vehicle (EV) charging, several technical aspects pertaining to the design and performance enhancement of integrated multi-port charger topologies are discussed in this study. This study also elucidates various research challenges pertaining to each module of the topology and elucidates technically validated solutions for each.

Firstly, targeting the input side totempole power factor corrector (TPFC) circuit, a novel digital filter based Active Mitigation Scheme (AMS) is proposed to curb the third harmonic component, along with a novel discretized sampling-based robust control scheme. Experimental verification of these techniques yields an enhanced Total Harmonic Distortion (THD) of 1.68%, enhanced efficiency of 98.1% and resultant power factor of 0.998 (lag).

Further, focusing on the bidirectional CLLC based DC/DC converter topology, a general harmonic approximation (GHA) based secondary side turnoff current minimization technique is discussed. Numerous fabrication and design-based constraints and correlations for parametric modelling of high frequency planar transformer (HFPT) are explained with analytical and 3D Finite Element Analysis (FEA) findings. Further, characterization of the plant transfer function of all-inclusive CLLC model is described along with hybrid Sliding Mode Control (SMC) based control scheme. The steady state experimental results at 1kW rated load show a peak efficiency of 98.49%, while the quantification of dynamic response portray a settling time reduction of 46.4% and an over/undershoot reduction of 33%.

Further, comprehensive modeling of triple active bridge (TAB) DC/DC converter topology is presented with special focus on the control scheme and decoupling capabilities to independently regulate the output bridges. With an objective to reduce the overall losses and to add a dimension of controllability, a three-loop control scheme is proposed with power flow optimization. Inculcating the benefits of multiport and resonant topologies, a comprehensive multi-variable loss optimization study of a Triple Active C^3L^3 (TAC^3L^3) converter is discussed. The performance of eight different hybrid modulation schemes is compared with respect to the developed global loss minimization objective function. Experimental validations for various loading conditions are presented for a wide-gain bidirectional operation (400V/500-600V/24-28V), portraying a peak converter efficiency of 97.42%.

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CHAPTER 1

INTRODUCTION

1.1 Overview of EV Charging Infrastructure

The consumption and creation of electric energy is undergoing a transformation that has never been seen before. The use of traditional energy sources such as coal is being phased out in favor of sustainable and renewable energy sources such as solar and wind. On the other hand, due to breakthroughs in the field of battery research and exponential technologies such as vehicle telematics, energy consumption, particularly in the sector of transportation, is shifting from petroleum-based to electricity-based fuel [1]. Electric Vehicle (EV) and Plug-in Hybrid Electric Vehicle (PHEV) technologies are gaining popularity due to their lower fuel consumption and greenhouse gas emissions. Since fuel is a secondary resource, PHEVs have a long driving range. Ancillary services, reactive power support, tracking the production of renewable energy sources, and load balancing are all possible with a connection to the electric power grid. Several organizations, including IEEE, the Society of Automotive Engineers (SAE), and others, are working on utility/customer interaction standards and norms. Electric vehicles have struggled to acquire widespread adoption. The high cost and cycle life of batteries, the complexities of chargers, and the lack of charging infrastructure are three major roadblocks [2]. Another disadvantage is that battery chargers can cause harmful harmonic effects on electric utility distribution networks, but this can be mitigated by chargers with an active rectifier front end [3].

In conjunction with charging station electrification of smart grids, renewable energy sources employed in distribution networks provide a choice for high power conversion efficiency and emission reduction [4]. The microgrid is made up of a collection of distributed energy sources and energy storage devices that are used locally by various types of loads and are connected to the grid or operated in an islanding mode [5]. Figure 1.1 depicts a typical EV charging station as part of a microgrid system. Large capacity penetration of EV charging points, on the other hand, increases demand for charging infrastructure, which raises demand on the utility grid [6]. Power generated locally from RES is combined with appropriate power converter topologies to alleviate concerns linked to power demand [7]. EV manufacturers provide charging station facilities as part of their charging infrastructure; for example, Tesla built a solar city and Nissan built a solar power plant [8]. However, charging stations built with renewable energy integration minimize the cost of charging and emissions while improving utility grid coordination [9,10].

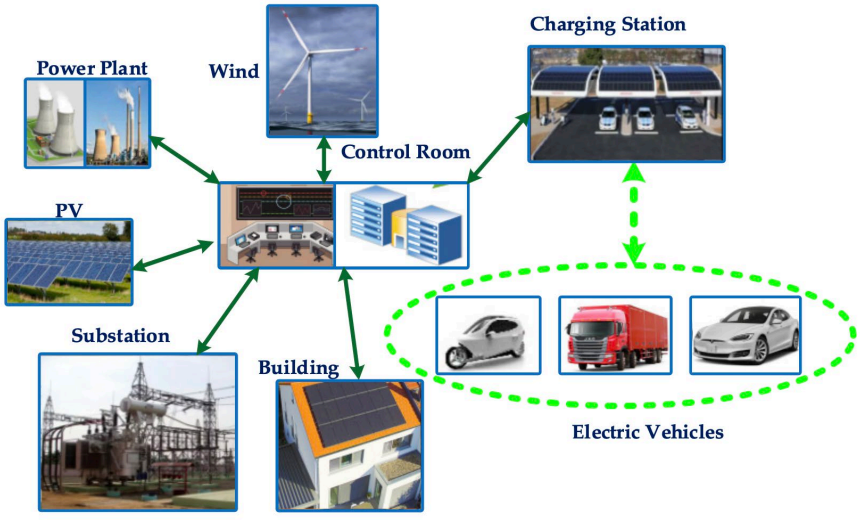


Figure 1.1: EV-charging Station as Part of the Microgrid Infrastructure [9]

Charging at work saves land and initial cost investment by using solar panels installed on the building's rooftop and parking lot [11]. According to a nationwide household survey, 90% of automobiles are parked in a parking lot for 5 to 6 hours, therefore workplace charging supports vehicle in grid (V2G) charging [12]. Figure 1.2 depicts charging stations in various locations. Automobile manufacturers must meet extremely high dependability standards regardless of the power source. Furthermore, some battery technologies' huge energy capacity and potentially volatile nature represent a severe safety danger. The key difficulties with charging stations are reliability, availability, and maintainability, which limit large-scale commercial use of these cars. The electric vehicle on the other hand depends on grid electricity and the charging system's reliability [13]. As a result, a model for grid-connected charging station reliability was developed. It aimed to look into the issues of EV charging station reliability, availability, and maintainability; investigate how fault events are logically related to one another, how these fault events influence a PEV's reliability, and how proper management strategies can improve a vehicle's availability [14]; and investigate the impact of a charging station on PEV availability. A modified probabilistic index was also presented to assess the reliability of the power supply. An IC was created to be controlled by an external BMS control unit via a serial peripheral interface (SPI), which also permitted data retrieval [15].

Charging at home Charging on public networks Charging at workplace

Figure 1.2: Charging Station in Different Locations [9]

1.1.1 Types of EV Charging Systems

Electric vehicle batteries are charged by conductive coupling, wireless charging, or battery swapping. Inductive or capacitive coupling is used to charge an electric vehicle wirelessly. The conductive coupling type uses an electrical outlet plug to charge the electric vehicles [16]. For power transmission, two distinct coils are used—one is put inside the vehicle and serves as the receiving coil, while the other is mounted on the parking slot and serves as the power transfer coil. Four capacitive plates are utilized to charge in capacitive charging [17]. By designing a level-based charging station, the cost of charging can be minimized. Battery switching technology reduces the time it takes to charge [11,18,19]. Table 1.1 lists the benefits and drawbacks of various charging methods. There are two types of electric vehicle chargers: off-board and on-board. An on-board charger is one that is housed inside the EV, whereas an off-board charger is one that is located outside the EV [20,21]. Figure 1.3 shows a block schematic of the many types of chargers. An on-board charger is mostly utilized for low-power applications, while an off-board charger is used for high-power DC fast charging [22]. EVs are charged from AC sources in an on-board charger; the primary challenges are power constraint and charging time [23]. Fast charging and vehicle-to-grid charging are also possible with off-board chargers. In that context, Table 1.2 shows the pros and drawbacks of chargers.

Table 1.1: Advantages and Disadvantages of Different Charging Systems

Charging Systems	**Advantages**	**Disadvantages**
Conductive Charging	• Suitable for slow and fast charging • High-efficiency charging • Multiple taping possible	• Need of standard connectors and cables. • Requires complex charging infrastructure
Wireless Charging	• No problems in standardization of connectors • Dynamic charging • Possible in all climate conditions	• Coil type needs to be standardized. • High cost and complexity. • Higher losses
Battery Swapping	• Battery replacement takes very less time • Higher range of the vehicle	• Standardized battery size and type • Battery maintenance • Special stations required.

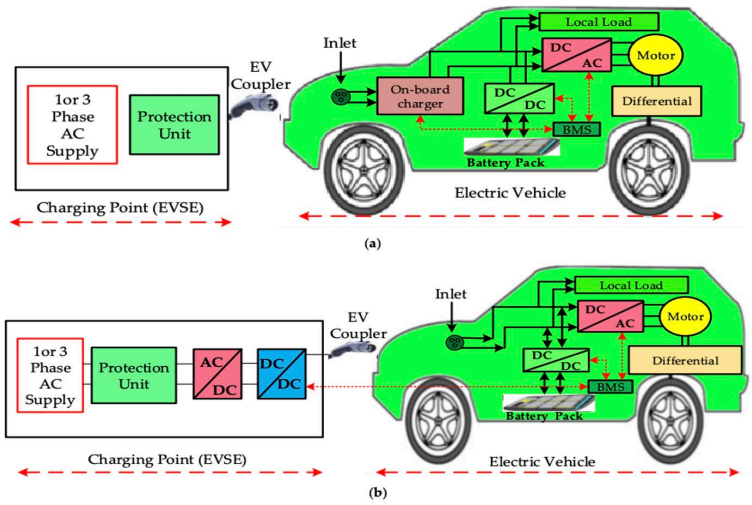


Figure 1.3: EV Charger Functional Schematic for (a) Onboard Charger, (b) Offboard Charger [9]

Table 1.2: Advantages and Challenges of Different Charging Types

Charger Type	**Advantages**	**Challenges**
Onboard Charging	• Charging possible at any location with an electrical outlet/ • Simple BMS can be used	• Slower charging, less power transfer at a time • Difficult to implement for V2G applications • Weight of the charger added to the EV
Offboard Charging	• Faster charging with higher power • Does not add to the weight of the EV	• Battery heating issue • Difficult to allocate charging locations. • Cost of charging is high

The majority of EV charging can be done overnight at home in a garage, where the vehicle can be hooked into a convenience outlet for Level 1 (slow) charging. Level 2 charging is the most common technique for both private and public facilities, and it necessitates a 240 V outlet. Future advances will concentrate on Level 2; semi-fast charging delivers sample power and can be used in a variety of settings. For Levels 1 and 2, single-phase solutions are typically employed. Level 3 and dc fast charging are designed for commercial and public use, similar to a gas station, and three-phase systems are typically used.

On-board and off-board EV battery chargers are available with unidirectional or bidirectional power flow [3]. Because it lowers hardware needs, simplifies interconnection concerns, and tends to lessen battery degradation, unidirectional charging is a sensible initial step. Charge from the grid, battery energy injection back to the grid, and power stabilization with proper power conversion are all supported by a bidirectional charging system. Because to weight, space, and cost considerations, most onboard chargers limit

high power. To circumvent these issues, they can be incorporated with the electric drive. Conductive or inductive on-board charger systems are available. Direct contact between the connector and the charge intake is used in conductive charging systems. A magnetic field is used to transfer electricity in an inductive charger. This type of charger has been explored for Levels 1 and 2 and maybe stationary or moving. An off-board battery charger is less constrained by size and weight.

1.1.2 Charger Power Levels and Infrastructure

Charger power levels are based on the following factors: power, charging time and location, cost, equipment, and grid impact. The deployment of charging infrastructure and electric vehicle supply equipment (EVSE) is critical since there are numerous factors to consider, including charging time, distribution, scope, demand policies, charging station standards, and regulatory procedures. The availability of charging infrastructure can be exploited to lessen the need for and expense of onboard energy storage.

The essential components of an EVSE include EV charge cords, charge stands (residential or public), attachment plugs, power outlets, vehicle connectors, and protection (see Figure 1.4) A specific cord set, and a wall or pedestal mounted box are the two most common options [3].

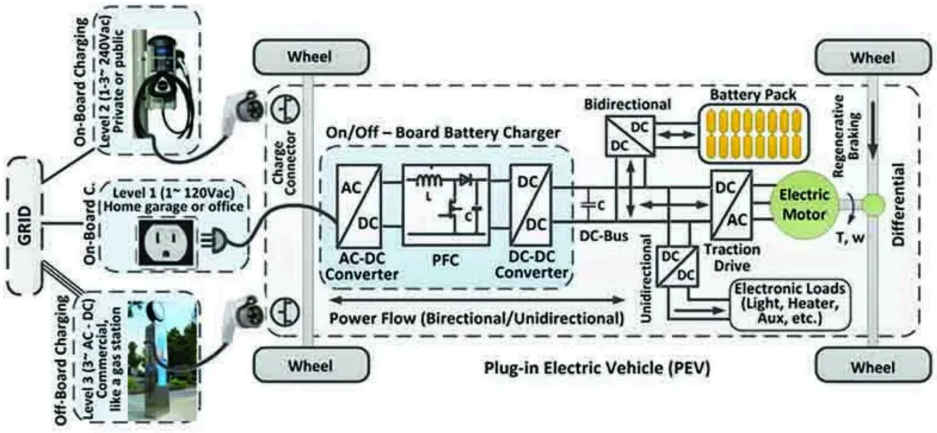


Figure 1.4: EVSE System Schematic [3]

Level 1 Charging is the slowest technique of charging. Level 1 uses a typical 120 V/15 A single-phase grounded outlet, such as the NEMA 5-15R, in the United States. A regular J1772 connector can be used to connect to the EV ac port. Although it is generally believed that this level will be integrated into the car, there are numerous existing installation costs of a residential Level 1 charging infrastructure.

Level 2 Charging: For dedicated private and public facilities, level 2 charging is the predominant way. To prevent redundant power electronics, this charging infrastructure can also be on-board. Level 2 equipment can be charged at 208 or 240 volts (at up to 80 A, 19.2 kW). For house or public units, dedicated equipment and a connection installation may be required, while automobiles like the Tesla have the power electronics on board and merely require an outlet.

Level 3 Charging: Level 3 commercial fast charging allows for charging in less one hour. Similar to petrol stations, it can be built in highway rest areas and city refueling sites. It requires an off-board charger to provide regulated ac–dc conversion and commonly runs

on a 480 V or higher three-phase circuit. Direct DC power may be used to connect to the car. In most cases, level 3 charging is not viable in residential settings.

Level 1 and Level 2 EVSE should be installed on the vehicle, while Level 3 should be installed outside the vehicle, according to the SAE J1772 connector for (PHEV and EV) standard. To enable quick charging in public settings, general public stations are planned to employ Levels 2 or 3. For utilities looking to reduce their on-peak effect, lower charge power is a plus. At peak times, high-power rapid charging can increase demand and potentially overload local distribution systems. Distribution transformer losses, voltage variations, harmonic distortion, peak demand, and thermal stress on the distribution system can all be exacerbated by level 2 and 3 charging. The use of a controlled smart-charging method can help to prevent the degradation of standard distribution equipment. A reliable communication network and control of public charging is needed to enable the successful integration of a large number of EVs. A comparison of all the EVSE types is shown in Table 1.3 [24].

Table 1.3: EVSE Level Classification

EVSE Type	Power Supply	Charging Power	Approximate Charging Time for a 24-kWh battery
Level 1: Residential	85V-265Vac, 12-16A, Single phase	1.44kW to 1.92kW	17 hours
Level 2 : Commercial	208Vac-240Vac, 15-80A, Single/split phase	3.1kW to 19.2kW	8 hours
Level 3 : Fast Charging	300-900Vdc, 400A max, poly phase	120kW to 350kW	24 minutes

1.2 EV Charging Topologies

A Level 1 EVSE uses generally available 120 VAC/230 VAC power sources, draws current in the 12 A to 16 A range, and can fully charge a 24-kWh battery in 12 to 17 hours. L1 chargers are used in residential applications and have a maximum capacity of 2 kW. A Level 2 EVSE (usually found in commercial settings such as malls, offices, and so on) employs poly-phase 240 VAC sources to power a more powerful vehicle charger, using anywhere from 15 to 80 A to fully charge a 24-kWh battery in around eight hours (power level up to 20 kW). A typical block diagram of an AC charging station is shown in Figure 1.5. On the other hand, the DC charging station is a Level 3 charger capable of handling very high-power levels ranging from 120 to 350 kW [25-26]. In approximately 24 minutes, the L3 chargers can charge batteries to 80% state of charge (SOC). Modular converters that may be stacked are employed to obtain such high-power levels. The inside of the car becomes bulky due to the stacking of converters. As a result, these stacking converters are mounted on the outside of the vehicle and serve as an EV charging station. The EV charging station connects directly to the vehicle's battery, bypassing the onboard charger. A typical block diagram of a DC charging station is shown in Figure 1.6.

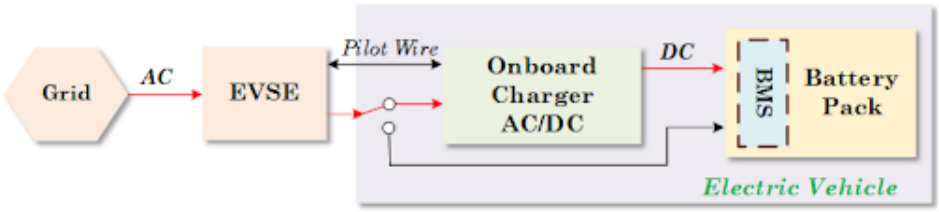


Figure 1.5: Level 1 and Level 2 EV Charger Schematic

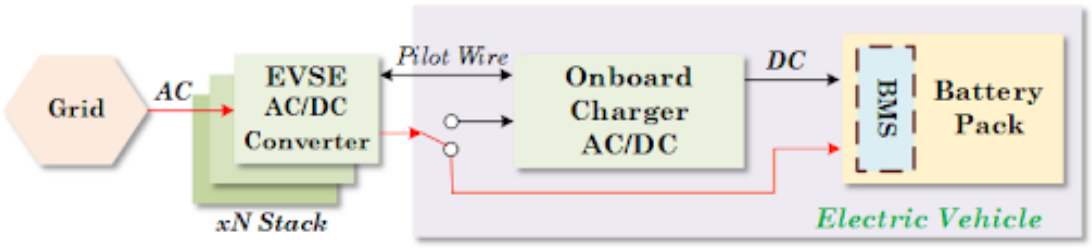


Figure 1.6: Level 3 EV Charger Schematic

High-power converters capable of charging to 80 percent SOC in under 24 minutes are required for DC charging stations. These fast-charging applications necessitate modular power converters that can be paralleled to cater to various power levels, allowing for rapid charging. The energy density and system efficiency are the most significant parameters. The quantity of energy that can be transferred for a given volume of converter is referred to as energy density. If we can double the power output for the same size, we can save a lot of money and speed up the charging process. This is performed by operating the converter at high switching frequencies, which helps achieve high power density by reducing the size of magnetics. For a given application, improved system efficiency means reduced losses and a smaller heat sink solution. It also minimizes temperature stress on electronics, resulting in longer part life expectancy.

The concept of Vehicle to Grid (V2G) is the most recent trend in automotive technology, which allows energy to flow from the battery to the grid for grid stability while the vehicle is parked or not in use. In order to accommodate such applications, both power stages must be bidirectional. Through a high-frequency transformer with the requisite voltage conversion ratio for the application, the converter must also be capable of providing galvanic isolation between the input and output stages. The converter must include inherent soft switching (like ZVS/ZCS) to function at high efficiency over a large input and output

voltage range. In an EV charging station, the AC/DC stage (also known as the PFC stage) is the initial level of power conversion. It transforms incoming grid AC power (380–415 VAC) into a reliable DC link voltage of roughly 800 V. As previously stated, the PFC stage is critical for maintaining sinusoidal input currents with a THD of less than 5%, providing controlled DC output voltage greater than the amplitude of the line-to-line input voltage, single-stage power conversion, no galvanic isolation, unidirectional and bidirectional power flow with (limited) reactive power compensation capability, simple circuit topology, simple modulation and control scheme, and the ability to. In an EV charging station, the DC/DC stage is the second level of power conversion. To charge the battery of an electric car, it converts the incoming DC link voltage of 800 V (in three-phase systems) to a lower DC voltage. Combined Charging System (CCS) and CHAdeMO are two protocols that control the charging of electric vehicles. The DC/DC converter must be able to deliver rated power to the battery over a wide voltage range, such as 50V-500V, to accommodate batteries ranging from 48V (e-bikes) to 400V (PHEV) and charge the battery in both constant current and constant voltage modes, depending on the battery's State of Charge (SOC).

1.2.1 Power Conversion Topologies for AC/DC Conversion

Passive, hybrid, and active power factor corrector (PFC) systems are the three types of topologies used for input AC/DC conversion. Single-phase and three-phase topologies are employed depending on the power level. Single-phase topologies are commonly used for power levels less than 3.3 kW, while three-phase topologies are utilized for power levels significantly higher than that. Single-phase PFC topologies, such as totem pole,

interleaved totem pole, and Neutral Point Clamped topology, and three-phase PFC topologies, such as Vienna PFC, Neutral Point Clamped (NPC) 3 level PFC, and T-type NPC [27] PFC are compared in Table 1.4 in terms of several technical metrics.

Table 1.4: Comparison of PFC Topologies

Metrics	**Totempole PFC**	**3-level NPC**	**3-level Vienna**	**3-Level TNPC**	**3-Level ANPC**
THD	High	Very low	Very low	Very low	Very low
Voltage Stress on Devices	High	Low	Low	Low	Lowest
Power Density	Medium	High	High	High	Highest
Bidirectional	Yes	Yes	Yes	Yes	Yes
Conduction Loss	Low	High	High	Medium	High
Switching Loss	Medium	Low	Medium	Medium	Low
Efficiency	High	Medium	High	High	Highest
Cost	Low	High	Medium	Medium	High
Control	Easy	Intermediate	Intermediate	Intermediate	Intermediate
Thermal Management	Easy	Difficult	Mild	Easy	Easy

1.2.2 Power Conversion Topologies for DC/DC Conversion

The LLC resonant converter, the Phase-shifted Full Bridge (PSFB), single-phase Dual-Active Bridge (DAB), and the Dual-Active Bridge in resonant CLLC mode are the four alternative topologies of high-power DC/DC converters that are compared in Table 1.5.

Table 1.5: Comparison of DC/DC Topologies

Metrics	**LLC**	**PSFB**	**DAB**	**CLLC**
Voltage Stress on Devices	High	Mid Low	Low	Mid Low
Transformer KVA	High	Medium	Low	High
Operation	Unidirectional	Unidirectional	Bidirectional	Bidirectional
Conduction Losses	High	Medium	Lowest	Lowest
Switching Loss	Low	High	High	Lowest
Controllability and Degrees of Freedom	Medium	Low	Medium	High
Efficiency	High	Medium	Medium	High
Switching Frequency	Fixed	High	High	Very High

1.2.3 V2G Capability Requirement

Vehicle to grid (V2G) technology allows energy stored in electric vehicles to be fed back into the national electricity network (or 'grid') to help supply energy during peak demand periods. This energy can be utilized to balance the grid, ensuring that we all have adequate electricity when we need it. As a result, bidirectional converters in EV charging stations are required. Figure 1.7 depicts an electric car connected to a charging station, where bidirectional converters allow the energy stored in the battery to be used to stabilize the intermittencies in the grid.

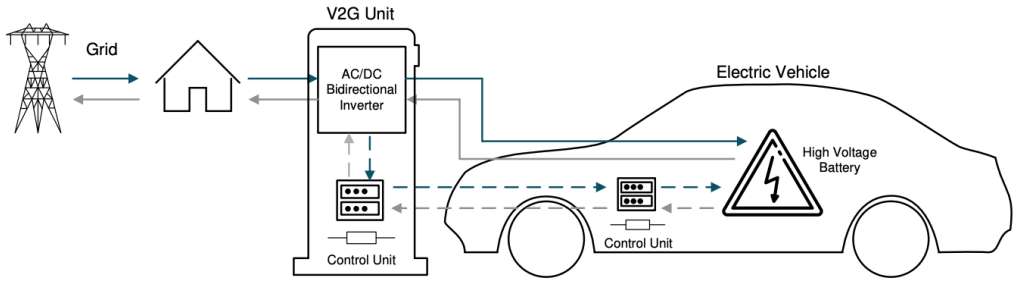


Figure 5-2. V2G Technology

Figure 1.7: V2G Power Transfer Schematic [22]

1.2.4 Proposed Dual Output Topology for Onboard EV Chargers

The work presented in this study focuses on Level 1 and Level 2 types of onboard EV chargers. All the existing on topologies implement a two-stage topology with a dedicated one port output for main battery charging. On the other hand, this work focusses on a design of a novel charging topology that is capable of not only charging the main battery, but also integrate a charging circuit for the auxiliary battery. The block diagram of the proposed topology with the selected terminal voltages is shown in Figure 1.8.

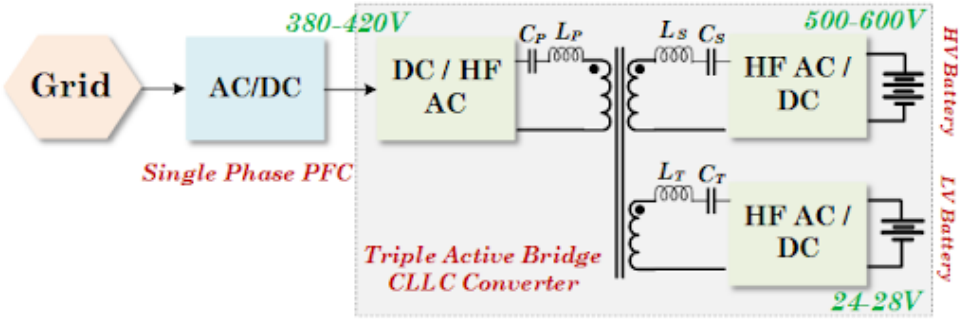


Figure 1.8: Block Diagram of the Proposed Topology

As observed in Figure 1.8, the terminal voltages are selected adhering to the typical battery voltages employed in ground military applications [28]. The high voltage (HV) battery is regulated at 600V [28] with a depletion threshold of 500V, while the low voltage (LV) battery level for auxiliary charging applications is 28V [29] with a depletion threshold

of 24V. However, the same topology can also be employed for a typical EV charger application by changing the transformer turns ratio and the relevant control parameters, where the conventional rated HV battery voltage is 400V [30] and the rated LV battery voltage is 48V. Further, adhering to the current shift in trend observed in the terminal battery pack voltages for EV charging systems, the HV terminal voltage can be regulated at 800V [31].

As observed, adhering to the benefits of low complexity design and ease of control, the input side PFC topology is chosen to be single phase totempole PFC (TPFC). With technical novelties in terms of improvement of power quality at the point of common coupling (PCC) and a sensorless control scheme aimed for cost reduction and superior dynamic control, the chosen TPFC topology proves to provide enhanced performance as compared to conventional topologies. Following the TPFC, a Triple Active Bridge C^3L^3 (TAC^3L^3) topology is implemented that portrays a coupled bridge structure, thus ensuring simultaneous charging solution for the HV and LV batteries (see Figure 1.9). Further, owing to the benefits of a bidirectional CLLC converter related to high power density, lower losses, and wide voltage range capabilities, the proposed topology uses CLLC converter in a multi-active bridge (MAB) fashion, thus ensuring efficient bidirectional charging solutions for the main and the auxiliary batteries. This topology is capable to work in 5 different operating modes, depending on the application as shown below:

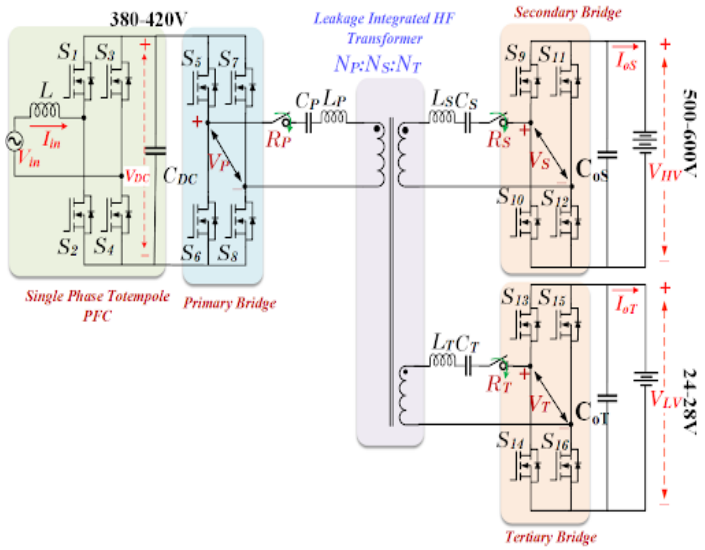


Figure 1.9: Proposed Multi-Output Onboard Charger Topology

1. Simultaneous Dual Port Battery Charging ($400V \rightarrow 600V, 28V$)

Adhering to the benefit of employing a TAC^3L^3 structure for the DC/DC converter, in this mode, both the HV and LV batteries are charged by the input mains (as seen in Figure 1.10). This is enabled by a novel decoupled power flow control technique (explained in Chapter 4), which allows independent power flow in both the output side bridges.

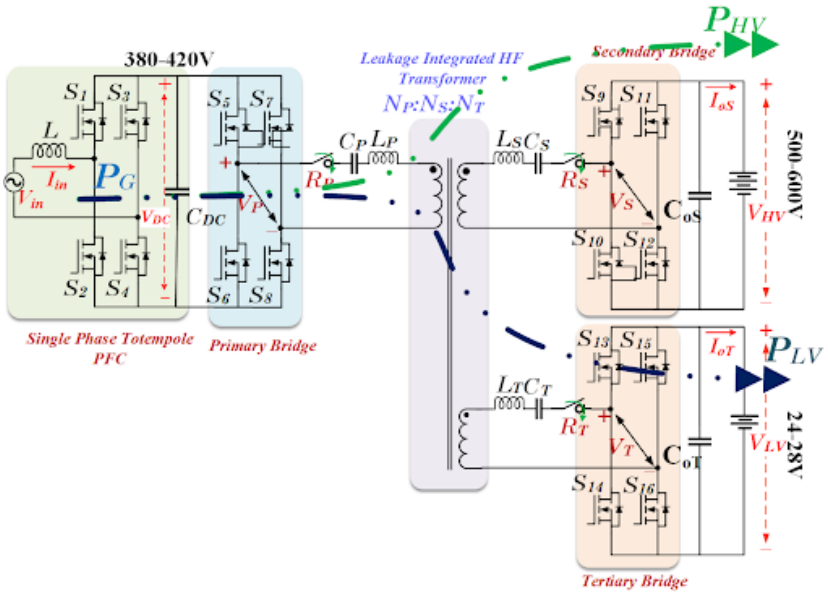


Figure 1.10: Mode – 1 Operation (Simultaneous Dual Port Battery Charging)

2. Simultaneous Reverse Power Flow ($600V, 28V \rightarrow 400V$)

During V2G mode of operation, both the main and auxiliary batteries are used to pump power back to the grid. This mode continues until the auxiliary battery is discharged to a certain SOC, after which the system operated in mode-3 as shown below:

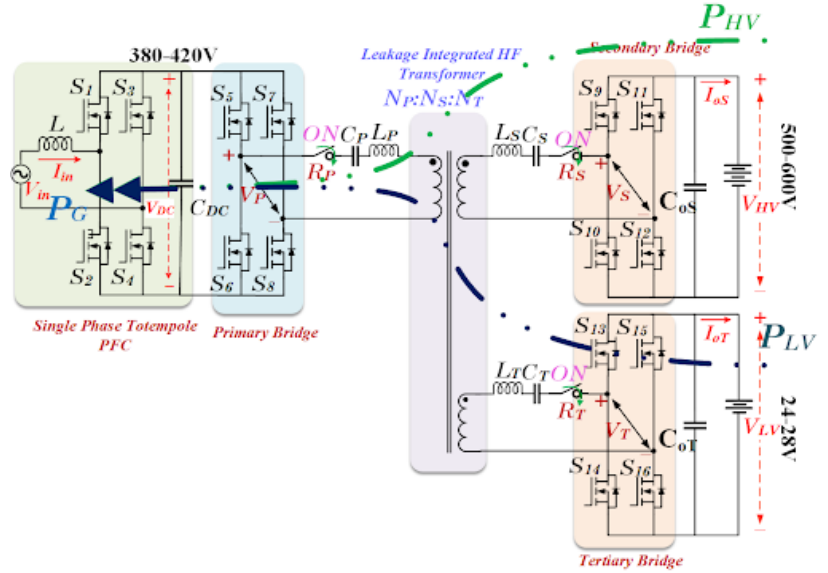


Figure 1.11: Mode – 2 Operation (Simultaneous Reverse Power Flow)

3. Bidirectional charging for the main battery ($400V \leftrightarrow 600V$)

In this mode of operation, the low voltage or the auxiliary battery is isolated and the power transfer happens between the grid power and the high voltage or the main battery (as shown in Figure 1.12). This mode can be bifurcated into two scenarios: (a) When the main battery is depleted (or has lower SOC), the main power supply draws power from the single-phase mains and charges it, (b) During V2G mode, the main battery necessitates reverse power flow to push power towards the grid.

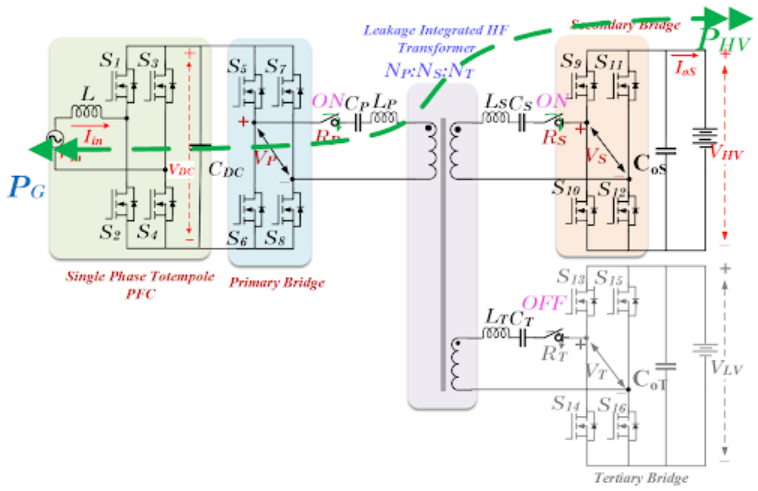


Figure 1.12: Mode – 3 Operation (Bidirectional Charging for the Main Battery)

4. Bidirectional Internal battery charging ($600V \leftrightarrow 28V$))

When the vehicle is in motion (grid is disconnected), the bidirectional charging capability enabled due to the CLLC converter topology ensures required power transfer between secondary and tertiary bridge (as seen in Figure 1.13). This is enabled by ensuring closed loop power flow optimization between the bridges, thus reducing any circulating power accounting for losses (as seen in Chapter 4).

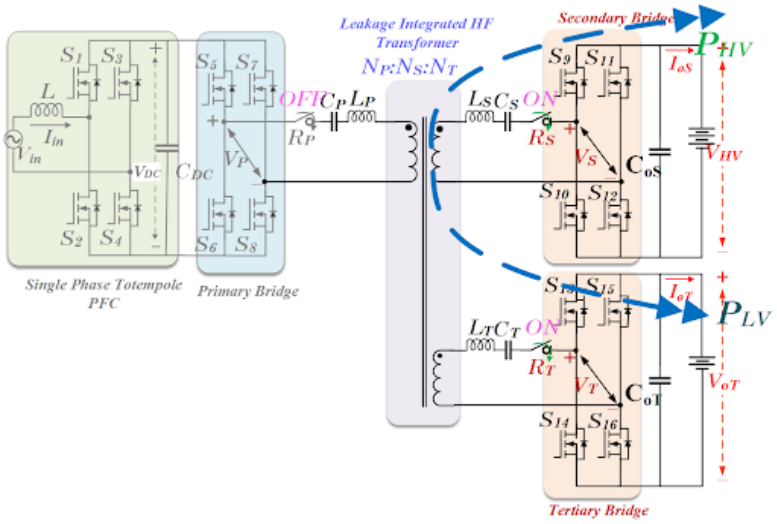


Figure 1.13: Mode – 4 Operation (Bidirectional Internal Battery Charging)

5. Unidirectional charging for the auxiliary battery ($400V \rightarrow 28V$)

During G2V charging mode, when the main battery is completely charged, it is then disconnected from the system and the auxiliary battery is charged through the mains. The breakers as shown in Figure 1.14 are controlled as per the battery SOC, that is given as an input to the digital controller.

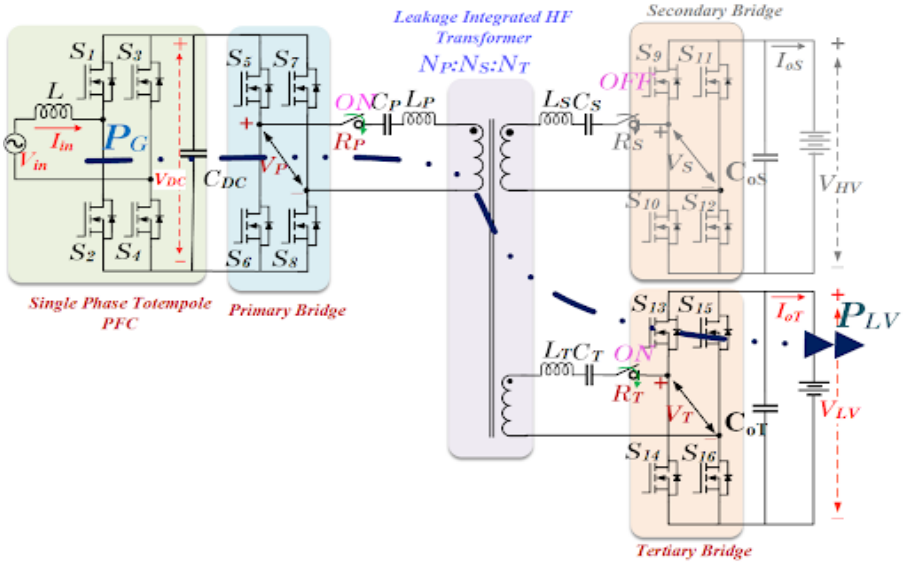


Figure 1.14: Mode – 5 Operation (Unidirectional Charging for the Auxiliary Battery)

Corresponding to the proposed topology of onboard EV charger, there are several research challenges pertaining to control, design and system modelling that are targeted for each module in this work and a detailed literature review with the required motivation is presented in the following sub-sections.

1.3 Input Side Power Factor Corrector (PFC) circuit

Adhering to the stringent power quality standards, power factor correction at the front end has become an indispensable feature for any plug-in power electronic device specifically used for electric vehicular applications. Several studies have been presented in the literature that aim at improving the performance of a PFC circuit [32]. Introduction of totem-pole structure to reduce the switching losses, interleaving of input side inductor to reduce the current ripple and other enhancements to reduce the overall size of the circuit have been discussed and well documented [33-34]. In this study, two of the most crucial research tasks related to a PFC are studied and appropriately addressed: (a) challenges pertaining to the power quality at the point of common coupling (PCC) due to the harmonic content of the input current and (b) enabling enhanced dynamic control without the use of a current sensor, thus resulting in superior power density and reduced cost.

1.3.1 Challenges Pertaining to Power Quality at the Point of Common Coupling (PCC)

Due to the ever-increasing number of electric vehicles (EVs) and their corresponding charging infrastructures, there has been a huge impact on the power quality of the utility grid [35]. All the commercially available OBCs include PFC circuits at the

front-end [36-37] that are responsible for maintaining the power quality at the point of common coupling (PCC).

A major concern in the PFC circuits is the existence of high magnitude higher-order harmonics (specifically the third harmonic component) in the input current [38]. Several studies have been proposed that aim at solving this issue by implementing design and/or control scheme variations. In [39] authors presented an input voltage sensorless control algorithm for boost PFC that reduces the input current harmonics converter by injecting an additional common-mode duty ratio term to the feedback controllers' outputs. The study proposed in [40] describes a power quality improvement technique for a boost PFC by mitigating line frequency instability using average current mode control [41]. A detailed analysis pertaining to the stability control scheme by adding a third current harmonic feedforward compensation and introducing a low-pass filter is explained, to enhance the overall THD. However, this work does not address and correlate the magnitude of the third harmonic component with the design parameters, thus leading to a complicated control system design. Moreover, the resultant THD is 15.58%, which is deemed unacceptable according to IEEE 519 [42].

Also, the proposed work in [43] presents a harmonic-reduction scheme that needs no extra hardware using a high-order digital filter that is challenging to be implemented in digital control platform. The work explained in [44] aims at reducing the third harmonic component from the input current by designing a compensation system for the higher order harmonic terms appearing in the switch node of the circuit, by adding a feed-forward path. However, the work lacks analyses pertaining to the current harmonic modelling for various loading conditions, thus limiting the scope of its application. Further, the study in [45]

explains an adaptive injection control scheme to cut down the resultant harmonics by reducing the ripple component appearing across the output capacitor of the PFC circuit, implemented using a low pass filter.

Considering the limitations pertaining to specific applications of the various studies presented in the literature, the study presented in this report (Chapter 2) aims at developing a thorough model to analyze and quantify the magnitude and phases of the higher order harmonic components present in TPFC input current and a novel technique to sufficiently attenuate them.

1.3.2 Review of the Existing Sensorless Control Schemes for PFC

For employing a closed loop control for a PFC circuit, conventionally, a two-loop control structure is implemented with an inner current control loop and an outer voltage loop, for which essentially three sensors are required – input voltage sensor, output voltage sensor and input current sensor. The most commonly used current sensing component is a current transformer (CT), placed in line with the high frequency switching MOSFET bridge. However, placing a CT in series with the switches increases the line inductance, which may cause high voltage spikes to appear across the switches, specifically during the switching instants. This also raises the requirement of resetting the magnetizing inductance in each switching cycle, which effectively reduces the maximum duty ratio of the converter [46]. On the other hand, in a Hall effect sensor, due to the remnant flux, a time-varying DC bias is introduced in the control system, which has the potential to destabilize overall control scheme. In addition to that, the bandwidth of a Hall-effect sensor is low, which leads to sluggish dynamic response of the converter. Resistor divider-based approach is

also one of the majorly used approach to sense current. However, it needs an additional high frequency, noise free and precise differential amplifier, which adds to the cost, complexity, and losses in the circuit [47]. Thus, to resolve the issues related to the use of a conventional current sensor and to reduce the overall cost of implementation and size of the converter, several research studies have been carried out to model the circuit alternatively, thus eliminating the current sensor.

An approach utilizing Kalman filters to obtain a system model using sensed voltages is proposed in [48]. In this method, two control loops – a real power loop and a power factor loop are implemented by sampling the system voltages using an extended Kalman filter (EKF). The plant is modelled with state variables corresponding to the peak of the input voltage, its phase angle, the output voltage magnitude and its peak-to-peak ripple, with a state estimator that uses the error feedback to correct the state estimates. However, due to high gain in the voltage control loop, the residual noise leads to distortion in the current waveform, thus degrading the overall power factor (to 0.985) with a THD of 10.6%, making its use infeasible in modern power supplies.

A more relevant approach is presented in [49], where the authors propose an adaptive inductor model method. In this technique, the sensorless control is achieved by extracting the inductor current reference from the sensed inductor voltage and processing it in an adaptive low pass filter. However, this method suffers with a major drawback pertaining to the estimation scheme used for calculating the inductance and its winding resistance, which primarily depends on an empirical equation derived in the paper (using output capacitor ripple information), with an unknown set of initial conditions. Additionally, as this method implements a component sensitive control scheme, any glitch

in the sensing and sampling module might lead to permanent damage of the inductor and the switches, the effect of which is not considered in the paper.

A more detailed approach is discussed in [50-52], where the PFC circuit is realized as a single switch model and is synthesized to obtain the necessary transfer function between the output voltage error and peak inductor voltage. This control technique provides a cost-effective and practically implementable solution for applications where the load variations are not very frequent [53]. This is because, the above- mentioned methods suffer with the issues of having high control loop execution times due to high degree of mathematical complexity of the proposed control schemes. Additionally, the dynamic response of these schemes is sluggish, typically taking 4-6 cycles (50-100ms) for the current to regain its stable state under any load disturbances.

With the aforementioned considerations and drawbacks of the SOA methods, a novel sensorless control approach is explained in this report (Chapter 2), that uses discretized sampling of system state variables and control variables. The proposed control scheme utilizes fundamental equations of instantaneous voltage across the input inductor using a switching cycle-averaged model and converts the logic into discrete domain for digital implementation.

1.4 Bidirectional CLLC Resonant DC/DC Converter

High frequency isolated resonant converters have found widespread application in the field of EV charging and aircraft power supplies, due to their higher power density and superior conversion efficiency [54]. Specific applications include auxiliary power units (APU) used in more electric aircrafts (MEA) that use fuel cell-based system at 400 DC

[55] to serve battery loads at 24-28V DC voltage levels at low load conditions, that in turn support the main supply during heavy loading conditions, thus demanding bidirectional power flow [56]. In that context, bidirectional CLLC resonant converter topology has proved to provide various advantages, such as reduced losses due to soft switching in the primary bridge [57] and synchronous rectification (SR) in the secondary bridge [58], no-load voltage regulation and wider gain range over narrow frequency modulation zone [59]. Additionally, with an aim to achieve superior power density for such converters, various research works have been published that aim at increasing the operational frequency of the converters, thus enabling reduction in size for magnetic components [60].

However, these advantages can only be redeemed by precise design and analysis of the equivalent parameters based on the physical design of the transformer winding arrangement [61], to obtain the desired gain characteristics, yet achieving the targeted efficiency and power density. In that context, it is thus important to parameterize the equivalent R-L-C parameters of the HFPT and understand their effect on the performance of the converter. Further, to enhance the efficiency of the converter, facilitating soft switching for the secondary side by enabling SR [80] is a necessity for efficient power conversion. In addition to that, from the control perspective, the aforementioned applications demand tight voltage regulation adhering to ever-changing load requirements based on the battery state-of-charge (SOC) and superior dynamic performance aiming better reliability of crucial battery-based loads, along with enhanced immunity against electromagnetic interference (EMI) [62]. A systematic two-fold controller design and modeling approach is quintessential for achieving the above-mentioned operational targets: (a) accurate characterization of the plant, with a target to intricately account for the non-

idealities and operational states, and (b) designing a robust controller in accordance with the developed plant model, capable to attain fast dynamic response. Referring to the research tasks aiming to optimize the steady state and dynamic performance of the resonant CLLC topology, a detailed literature review is presented herewith.

1.4.1 Characterization of R-L-C Parameters of the HFPT

Various studies have been proposed that aim at analyzing the operational behavior of HFPT under different operating conditions [63-64]. The implication of various winding structures and their configurations on the resultant flux linkages in the transformer and corresponding leakage inductances have been extensively researched [65]. Further, to analyze the effective AC resistance of the windings, several studies have been done improving Dowell's analysis [66] by introducing porosity factor η which have yielded results with maximum accuracy loss of 15%. The work in [67] implements an interleaved structure of winding arrangement with parallel secondary winding, aimed at reducing the winding losses occurring in the HFPT. A recent work on differential evolution algorithm (DEA) based approach in conjunction with finite element method (FEM) based analysis is presented in [63].

In addition to that, several studies have been published in the literature that provide detailed analysis on modelling the HFPT focusing on the aspects of reduced winding losses with interleaved arrangement [67], issues pertaining to electromagnetic interference (EMI) occurring due to stray capacitances and ways to reduce them [68-69]. The work presented in [63] focusses on the concept of paired interleaved windings that explains its implications related to reduced stray capacitance, at an expense of higher winding resistance. A detailed

design-based tradeoff analysis is presented in [65] with elaborate justification and verification of the HFPT components. However, all the above-mentioned works portray a very generalized model to characterize the HFPT with assumptions pertaining to uniform winding arrangements and correspondingly are unable to correlate the obtained equivalent parameters with the physical constraints of a PCB such as its thickness and corresponding insulation layer distribution, air gaps, and the conductor trace thickness.

Considering the above limitations, practical and realistic characterization of the leakage inductance, winding resistance and stray capacitance of a HPFT accounting for various intricate fabrication-based considerations and their effect on the system performance is explained in Chapter 3.

1.4.2 Turnoff Loss Minimization at the Secondary Side Using Synchronous Rectification (SR)

Several studies have been published in the literature that have implemented various techniques to correctly realize SR. A summarized comparison is presented in Table I.6 that qualitatively compares the most leading state-of-the-art works by elaborating on various metrics of performance and implementation. The method explained in [70] senses the voltage across the body diodes of the switches, based on the reverse current flow, to detect the turn-on instant. The study mentioned in [71] is based on resonant inductor voltage sensing which is used to formulate the instantaneous current flowing through it, which is used to actively detect the turn-on instants corresponding to current zero-crossings. Zhuoran et al. in their study [72] utilize a Rogowski coil and a zero-crossing detector (ZCD) to synthesize the switching instants. However, all the above-mentioned methods utilize an

extra voltage/current sensor to realize SR, which increases the overall cost and losses in the circuit. Further, in these cases, accuracy of SR highly depends on the sampling frequency of the sensor, which limits their use for high frequency application. In addition, intermediate failure in the auxiliary sensing circuit might adversely affect the power stage due to damage caused due to inaccurate phase tracking.

The studies presented in [73-76] provide an elaborated time-domain model highlighting the switching instants and formulating detailed system equations, to analytically calculate the required phase for enabling SR. These methods portray superior tracking accuracy, which is sufficiently backed by detailed sensitivity analysis corresponding to change in system parameters. However, these methods include relatively complex mathematical synthesis and solving complicated differential equations for each switching instants with several small signal approximations, limiting its widespread acceptance. In addition to that, these methods do not account for the stray components appearing in the resonant tank, thus rendering the work deficient.

Addressing the limitations of time domain models, the works in [77-79] utilize frequency dependent first harmonic approximation (FHA) model to synthesize the state equations and corresponding obtain the required phase to enable SR. However, FHA ignores the effect of higher order harmonics in formulating the system equations, thus limiting the accuracy of presented analysis. Further, inaccurate phase tracking based on FHA results in a degraded efficiency due to higher mismatch between the secondary current zero-crossings, leading to higher switching losses. To address the limitations of FHA, the study presented in [80] utilizes an extended harmonic approximation (EHA) strategy to synthesize the phase shift for ensuring minimal switching losses. In addition,

detailed sensitivity analysis is also presented which highlights the accuracy of the proposed method for significant changes in resonant tank parameters. However, this method, like all the previously referred works, does not account for the stray components: (a) winding resistance and (b) inter and intra-winding capacitance of the HFPT, leading to inaccuracy in terms of frequency modulation to achieve a particular gain, which significantly affects the resultant phase tracking accuracy.

Addressing the aforementioned limitations pertaining to the state-of-the-art methods of enabling SR, the study shown in this work (Chapter 3) elucidates a non-approximated frequency domain model-derived formulation of required phase shift enabling SR, accounting for the stray parameters and corresponding minimization of turnoff current based on multi-dimensional optimization approach.

1.4.3 Accurate Small-Signal Modeling and Closed Loop Control of CLLC Converter

Due to the inherent non-linear nature of the tank current and voltages and their large resonant swings around the operating points, traditional linear approximation based averaging approaches for CLLC converter topology are not feasible to obtain its small-signal model [81]. In that context, several studies have been published in the literature that elucidate various methods to extract the plant transfer function through empirical modeling techniques. The study in [82] models the load as a time-varying resistor using a frequency domain approach, where an iterative process formulates the phase and magnitude of the resistor, and the small signal model is derived using an empirical conversion matrix. Another set of studies [83-84] have employed time-domain low-frequency modeling of resonant topologies, by analyzing the converter at resonant frequency. However, the

accuracy of estimation and applicability of these studies show degrading trend at operational frequencies deviating from the resonant frequencies, thus rendering them infeasible for wide gain range applications. Aiming to tackle this problem, Mehdi et. al. [81] have proposed a novel homopolarity cycle based small-signal modeling of resonant topologies for below-, at- and above-resonant dynamic operations by establishing analytical relationships between bridge voltages and currents and implementing volt-amp-second balance principles for a half switching cycle.

Another well-known approach for characterizing the plant transfer function of resonant topologies is obtained by analyzing the large-signal dynamic behavior by expressing them through a set of non-linear discrete state-space equations [85-89]. These state-variables are linearized using extended describing function (EDF) [90] based technique that uses Fourier series expansion and first harmonic approximation (FHA) to obtain a set of matrices that are parameterized through equivalent circuit models. However, all the above-mentioned studies assume the converter to be an ideal system and fail to incorporate the effect of inherent parasitic components and corresponding higher order harmonic components in the obtained plant frequency response [91]. This raises a serious question: What effect do non-idealistic components present in the system have on the system small-signal response and controller design? The exclusion of parasitic components in the analysis not only leads to variation in the plant dynamics but also causes the corner frequencies to deviate, leading to inconsistencies in the controller design. In addition to that, the unaccounted poles, and zeros due to the parasitics might also lead to huge discrepancies in the obtained gain and phase margins, thus jeopardizing the closed loop stability of the system [92-93].

Further, to achieve stiffly regulated output voltage, several control techniques have been also discussed in the literature. Pulse Frequency Modulation (PFM) based proportional-integral (PI) controllers have proved to be the most suitable for controlling resonant DC/DC converters [94-95]. However, the design of such controllers requires rigorous trial and error-based time-consuming approach for tuning them for the desired response. In addition to that, due to parametric variation, non-linearity, and load disturbances, the PI controllers fail to regulate the converter at desired output voltage leading to significant steady state errors [96]. The study in [97-98] explains a constant current control based on a state trajectory model, which is implemented using a novel dead-band based control method and proves to have significant improvement over a conventional PI controller. Although, the study achieves a settling time reduction of approximately 56%, the proposed method does not account for the additional turn-off losses in the secondary side switches, leading to degraded steady state efficiency of the system. Another constant current control strategy for LEDs and ozone-driven systems was proposed in [99] implementing a PI controller without dynamic load change. A high dynamic parabolic current control based on the synchronization of zero-crossing current ripples was proposed for multi-phase buck converters [100]. However, due to the non-linear behavior of the resonant CLLC converter topology, the aforementioned control schemes were hard to implement.

SMC based control techniques have proved to provide significantly enhanced transient performance due to its easily tunable fast dynamic response and natural robustness [96]. Accounting for the commonly known drawback pertaining to the chattering phenomenon occurring around the sliding surface, methods have been discussed

in the literature that implement differential switching function in SMC where discontinuous terms are transferred to higher derivatives of the control input [101]. The work in [96] comprehensively describes the implementation of SMC controller in a CLLC converter topology. Although the study holistically covers the selection criteria based on the dynamic performance of the converter, it fails to account for the phase shift required for the secondary side bridge, thus incurring higher amount of switching losses.

Thus, considering the limitations of various research works to accurately characterize the plant and design a suitable robust controller, this work elucidates a detailed GHA [80] based small-signal model of the CLLC converter accounting for the system parasitics and higher order frequency components. A detailed comparison based on open loop frequency response is established between the proposed and the conventional method and is validated through comprehensive experimentally obtained results. Further, a hybrid SMC based control scheme is introduced with thorough quantification of the system dynamics concurrent with the controller design that portrays significant improvement in terms of voltage settling time and over/undershoot as compared to conventional PI controller. In addition to that, the proposed control scheme augments the frequency control with an additional phase shift in the secondary side gate pulses that significantly strengthens the objective of achieving superior steady state efficiency of the converter.

Table 1.6: Merit Review of Different State-of-the-art Works on SR Implementation

Criteria	**[70]**	**[71]**	**[72]**	**[73]**	**[74]**	**[75]**	**[76]**	**[77]**	**[78]**	**[79]**	**[80]**	**Proposed Method**
Method	Voltage Detection	Current Detection		Time Domain Modeling				FHA			EHA	GHA based optimization
Accuracy of Estimation	✧✧✧	✧✧✧✧	✧✧✧	✧✧✧✧	✧✧✧✧	✧✧✧	✧✧✧✧	✧✧	✧	✧	✧✧✧ ✧	✧✧✧✧✧
Computational Workload	✧✧	✧✧✧	✧	✧✧	✧✧✧✧	✧✧✧✧	✧✧✧	✧	✧	✧	✧✧	✧✧✧
Difficulty in Realization	✧✧✧	✧✧	✧✧✧	✧✧✧✧	✧✧✧✧	✧✧✧	✧✧✧	✧✧	✧	✧✧	✧✧	✧✧
Sensor Requirement	Yes	No (indirect)	Yes	Yes	Yes	No	Yes	No	No	No	No	No
Peak Efficiency	96.20%	~97.2%	98.30 %	~91%	97.05%	N/A	97.60%	~96.8 %	~95. 5%	97.50 %	97.24 %	98.49%

1.5 Power Flow Optimization and Decoupled Control of a Triple Active Bridge (TAB) Topology

Adhering to the ever-demanding innovation in the field of lighter EV and their charging infrastructure, specifically onboard charging systems for electric material handling equipment and airport ground support equipment [102], several converter topologies ensuring efficient battery charging solutions have been proposed in the literature [103-104]. These applications demand efficient charging solutions not only for the main battery, but also for the auxiliary batteries, typically rated at a lower voltage level. In order to cater to these applications, the TAB DC/DC converter topology has provided promising results, by providing simultaneous charging capabilities for both the main and the auxiliary battery units [105].

Due to the inclusion of the third bridge, as compared to a conventional dual active bridge (DAB) converter [106], there are several complex design challenges introduced pertaining to (a) degraded converter efficiency due to unavoidable power linkage between the two output bridges and (b) designing a three-winding transformer with leakage inductances corresponding to the required power demand at the output ports. In addition to that, the correlation between the control parameters responsible to modulate the output power and voltage, and their relative position increases the complexity in terms of control scheme formulation [107]. Several studies have been proposed in the literature that aim to resolve these challenges by optimizing the design and the control scheme, so as to achieve minimized losses.

The work proposed in [108] provides a detailed time-domain characterization of the modes of operation of the TAB topology. Moreover, it also provides insights about the leakage inductance modelling for reduced switching losses aiming at extended zero voltage switching (ZVS) range for the converter. A comprehensive loss model is presented in conjunction to optimum power flow trajectory leading to reduced switching losses. However, the paper does not address the issues related to the increase in the overall RMS current in the circuit, without any consideration given to the control parameters.

The work in [109] provides a detailed model of the TAB structure using the concept of GHA to obtain relations for the power flows in the system. Additionally, with an aim to minimize the switching losses by extending the ZVS range and to minimize the overall conduction losses, an optimization algorithm is developed involving the phase control parameters. The resultant efficiency with the optimized control scheme is 97.6%, which is higher than other claimed techniques [110-112]. However, interdependence and the effect of load change on either of the secondary or the tertiary side bridge resultant voltage and corresponding power level is not taken into consideration, which limits its application to a very specific objective, rather than a generalized solution.

A small signal-based modelling and intricate analysis of the dynamic performance of the formulated control scheme is presented in [113]. The authors have developed a decoupled control logic for the TAB topology by implementing the state space modelling approach that enables the designer to analyze the system performance in terms of its dynamic throughput by accounting for the overshoot/undershoot and settling time of the output parameters. However, no specific consideration in terms of enhancing the system

efficiency is explained, thus limiting the scope of analysis only referring to the control domain.

Further, the work presented in [114] provides time-domain based analysis of the TAB converter to derive and analyze the zero-voltage switching (ZVS) constraints and its feasible regions, thus accounting for the switching losses. The analysis also includes considerations pertaining to parasitics involved in the system, along with the leakage inductances, in order to account for the electromagnetic interference-based issues. To explore the ZVS operating points, the system is subjected to five degrees of freedom, which increases the complexity of design, yet achieving superior performance in terms of reduced switching losses. However, the authors fail to correlate the effect of ZVS operation on the resultant RMS values of the bridge currents and thus the conduction losses, which renders the analysis incomplete.

Pertaining to the shortcomings seen in the aforementioned works on the TAB topology, a decoupled power flow control strategy based on GHA modeling is explained in Chapter 4, that aims at providing seamless power transfer control for both the output bridges. Building on that basis, a novel three-loop control scheme along with a power flow optimization algorithm that includes a duty ratio control term in addition to the phase shift control parameters is proposed. Further, a multi-variable multi-constraint optimization algorithm is formulated with an objective to minimize the total losses in the system, while the algorithm also postulates design considerations pertaining to the required leakage inductance values to ensure desired power transfer between the bridges.

1.6. Multi-Variable Global Loss Optimization of Multi-Port Converters with Resonant Tanks

Owing to the target of achieving a power dense integrated solution and to provide simultaneous charging for the main and the auxiliary battery (typically at 12V or 28V), multi-port converters (MPC) have proved to be a promising solution. Based on that, several studies have been published on the modeling, design, control, and optimization of a Triple Active Bridge (TAB) converter [115], where the power flow between bridges is modelled using inductive impedances between them. Adhering to the performance-based advantages of the CLLC resonant topology and seamless integration achieved due to MPC based topologies, the investigation of an MPC following a resonant topology is of tremendous research interest. Thus, this work introduces a TAC^3L^3 converter topology with L-C resonant tanks on all three full-bridge ports and elucidates its modeling, analysis, and steady-state loss optimization techniques.

A few studies have been published that explore the possibility of implementing resonant topologies in MPCs. A resonant LCL immittance network based MPC is elucidated in [116], with a special impetus provided to its power decoupling capability. The requirements for achieving ZVS/ZCS using an enhanced phase shift modulation technique is explained along with analyzing the parameter sensitivity of the LCL immittance network. Further, a three-port resonant LLC converter for an intended use as a solid-state transformer is elucidated in [117]. This study characterizes the power sharing between the ports and analyzes the ZVS conditions for the explained topology, operated in DC-transformer mode, where two input ports simultaneously supply the load in the diode

bridge-driven third port. Although, the above-mentioned works diligently characterize the operation of the MPC topologies in their respective works, the presented analyses are limited to a particular set of operating conditions, where the effect of having different terminal voltages with various gains at corner conditions, and their dependence on the control parameters at different loading conditions is not studied. Overcoming this limitation, a three-port half bridge based CLL topology, its analysis for power flow controllability and its dependence on the operational duty and phase control parameter is explained in [118]. In this study, two input side half bridges are interfaced through a resonant tank and are connected to a common diode-based output side full-bridge. Further, a closed loop control scheme for output voltage regulation and power flow management is explained, where the system benefits from ZVS-ZCS for a wide load range. Y. Wang et. al. proposed a three-port bidirectional multi-element resonant converter (TPBMERC) with a detailed analysis explaining the dependence of power flow and resultant gains on the phase shift parameters between the three ports [119]. Further, a small signal model was developed to appropriately select the parameters for independent port control. However, the scope of efficiency improvement in these resonant MPC topologies by optimizing the control variables including the operational frequency and their effect on the power flow and voltage regulation remains relatively less explored.

In that context, a few works [120-123] have targeted to enhance the efficiency of MPCs by involving duty and phase control variables in the modulation schemes. However, these works characterize the converters and their loss models using complicated time-domain analysis of each operating point, thus resulting in a computationally expensive

solution. Further, as the time dependent state-equations involved in such analyses vary for different corner conditions, there is a lack of a generic approach for system loss synthesis. Complementary research works [124-125] targeting frequency-domain analysis of MPCs have also been published, that target global loss minimization by involving a five-dimensional control corresponding to the duty and phase shift variables. One of the most relevant works presented in [124], explains a conduction loss reduction strategy implemented on a TAB converter by developing detailed conduction and switching loss models and running an optimization routine to obtain the most optimum set of control parameters, adhering to the constraints of power flow between the ports.

However, as the proposed TAC^3L^3 converter includes an LC tank at each of its port following a resonant topology, the inclusion of frequency among the other control variables becomes essential for loss optimization, as the conduction and switching losses in the system portray a strong dependence on the operational frequency. Comprehensive comparison of various modulation schemes based on their merits/demerits related to soft-switching capability, complexity of implementation and gain range is elucidated in the review study presented in [126]. The concept of frequency-inclusive hybrid modulation to enhance the system efficiency of conventional resonant converters (LLC/CLLC) is elucidated in several works in the literature [127-130]. A. Awasthi et. al. proposed a hybrid frequency-duty modulation a low-Q LLC converter, utilized to improve the light load efficiency [128]. An approach to reduce the sum of RMS port current by implementing a phase shift and duty-based control, with detailed establishment of the power flow dependence on the control parameters, for a bidirectional resonant converter was described

in a recent study [129]. However, this study only focusses on a conduction loss minimization scheme and does not inculcate a global loss optimization algorithm involving the conduction, switching and resonant tank-based losses.

To overcome the above-mentioned challenges of several state-of-the-art (SOA) works in the field of multi-port converters and their control implemented using frequency, duty and phase shift control parameters, a multi-variable loss optimization for the proposed TAC^3L^3 is covered in Chapter 5.

1.7 Thesis Outline

As discussed in this chapter, various types of EV charging architectures are explained along with comparison of several topologies used in an onboard EV charger. Further, the proposed topology is elucidated with its different modes of operation highlighting the versatility of the proposed topology. A detailed literature review and motivation targeting several research tasks are laid out in this chapter. The rest of the thesis is organized as follows:

Chapter 2 focusses on detailed theoretical harmonic modelling of TPFC input current as a function of load power and input voltage levels. Further, thorough analysis and design of a novel digital filter based third harmonic Active Mitigation Scheme (AMS) scheme is explained that is aimed at subduing the third harmonic component appearing in the input current. Further, a novel sensorless control scheme is explained in this chapter along with exhaustive set of simulation and experimental validations.

Chapter 3 elucidates an intricately curated all-inclusive GHA based modeling of CLLC converter with asymmetric tank accounting for stray parameters and their effect on

the resultant gain trend, highlighting the experimental accuracy of the presented analysis. Further, graphically elucidated parametric trade-offs and guidelines related to conductor and insulator parameters employed for HPFT realization are explained in this chapter. Finally, a detailed GHA based small-signal modeling of the CLLC converter is presented with thorough modeling and design of a novel SMC based hybrid control scheme in association with efficiency enhancement objective obtained through secondary side turn-off current minimization.

Chapter 4 explains the modeling and system synthesis of a TAB converter along with design of an active cross-gain based decoupled power flow control scheme to eliminate interdependency between the output voltage control loops. In addition to that, a novel phase/duty modulated three loop control schemes based on power flow optimization to achieve enhanced converter efficiency is also presented in this chapter.

Chapter 5 provides detailed steady-state operational synthesis based on GHA to model the port voltages, currents, and powers, with their corresponding dependencies on the control variables – phase shifts between the ports, duty ratios and the operational frequency. Further, a multi-variable optimization function is developed to achieve global loss minimization of the proposed converter by imposing constraints to ensure soft-switching and desired power flow at the ports. The performance of eight different hybrid modulation schemes is compared with respect to the developed objective function and an optimal selection algorithm is elucidated to enable least algorithmic complexity based on implementation constraints, while ensuring maximum efficiency at different corner conditions of port powers and terminal voltages.

Finally, Chapter 6 puts forward some relevant conclusive points and summarizes the technical findings as a part of this work. In addition to that, it also lays down the future scope of work that proves to have significant research merit with regard to deeper analysis and implementation of multi-port resonant DC/DC converter topologies.

CHAPTER 2

PARAMETER VARIATION TOLERANT CURRENT SENSORLESS CONTROL OF A SINGLE-PHASE BOOST PFC WITH HARMONIC ACTIVE MITIGATION SCHEME (AMS)

2.1. Introduction

Referring to the challenges pertaining to degraded power quality on account of harmonics present in the input current of a Totempole Power Factor Corrector (TPFC), this chapter comprehensively explains the operational principles and control of a TPFC circuit along with novel concepts pertaining to the power quality improvement through the proposed Active Mitigation Scheme (AMS). The major technical contributions of this work are as follows: (a) Detailed theoretical harmonic modelling of TPFC input current as a function of load power and input voltage levels, (b) Comprehensive correlation established between the developed theoretical harmonic model with the simulation and experimental results, (c) Accurate analytical relationship between the harmonic amplitudes and closed loop controller coefficients, (d) Analysis and design of a novel digital filter based third harmonic AMS scheme aimed at subduing the third harmonic component appearing in the input current.

Further, as seen in Chapter 1, adhering to considerations and drawbacks of the SOA methods for employing a sensorless control scheme for TPFC, a novel control approach is described that uses discretized sampling of system state variables and control variables. The proposed control scheme utilizes fundamental equations of instantaneous voltage across the input inductor using a switching cycle-averaged model and converts the logic

into discrete domain for digital implementation. The fundamental contributions of this work are as follows: (a) owing to the simplicity of the proposed algorithm, the program execution time is considerably reduced compared to other sensorless control schemes, thus promoting the use of higher switching frequencies for a high-density power conversion, (b) the proposed control is proven to be immune to any variations in converter parameters, thus ensuring robust and reliable operation, (c) to account for EMI-induced noises in the sensed data, a discretized moving average sensing scheme is implemented to assure disturbance rejection, (d) the results show the ability of the proposed control scheme to achieve 25% faster dynamic response with respect to the SOA during a sudden load change.

The technical aspects included in this chapter are derived from the studies discussed in [131-133].

2.2. TPFC Topology and Modes of Operation

As seen in Figure 2.1, the TPFC consists of four active switches, out of which S_1 and S_2 are operated at the switching frequency (f_s) with a duty ratio δ, while the synchronous half-bridge employs active switches S_3 and S_4 that are operated at the grid frequency (60Hz), instead of using diodes. This is because diodes typically have high forward voltage drop leading to higher conduction and switching losses. On the other hand, engaging MOSFETs reduces the conduction losses due to relatively lesser $R_{DS,on}$, leading to lower $I_D^2 R_{DS,on}$ losses [134]. This arrangement facilitates in offering lower conduction losses compared to a conventional boost PFC and lower switching losses compared to a H-bridge PFC [32]. There are typically four modes of operation as seen in Figure 2.2.

As observed in Figure 2.2 with corresponding switching states as shown in Table 2.1, S_4 conducts when $V_{in}>0$ and similarly, S_3 conducts when $V_{in}<0$. During Mode – I, the input voltage is in its positive half cycle and S_2 and S_4 are switched on. Congruently, positive current ($i(t)$) magnetizes the input inductor, leading to the instantaneous voltage across it depending on V_{in} and the drop across the winding resistance ($i(t)r_{inductor}$). Similarly, in Mode – II, S_2 is turned off and S_1 is turned on, leading to the current flowing through the load. Thus, the instantaneous voltage across the inductor also includes the output voltage component along with the drop across its winding resistance (as seen in Table 2.1). Further, for Modes – III and IV, as $V_{in}<0$, S_3 is turned on, and switches S_1 and S_2 are triggered according to the configuration show in Table 2.1.

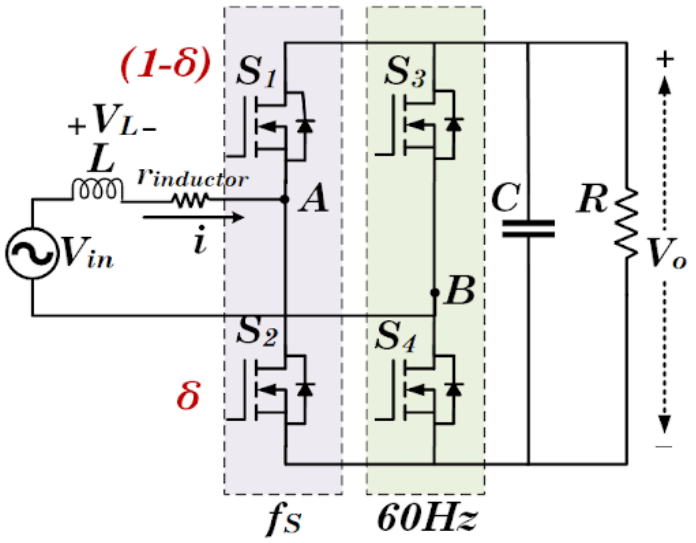


Figure 2.1: Single Phase Totem-pole Boost PFC

As observed in Figure 2.2, considering unity power factor operation, and referring to the voltage-second balance across the inductor for the modes of operation mentioned in Table 2.1, the duty ratio ($\delta(t)$) can be formulated as:

$$\delta(t) = \begin{cases} 1 - \frac{V_{in}(t)}{Vo}; \ \ for\ V_{in}(t) > 0 \\ -\frac{V_{in}(t)}{V_o}; for\ V_{in}(t) < 0 \end{cases} \tag{2.1}$$

With regard to the expression for duty ratio ($\delta(t)$), the on-time for switch S_2 can be defined as $\delta(t) * T_S$, while that for S_1 can be defined as $[1 - \delta(t)] * T_S$, where T_S denotes the switching period corresponding to a switching frequency f_s.

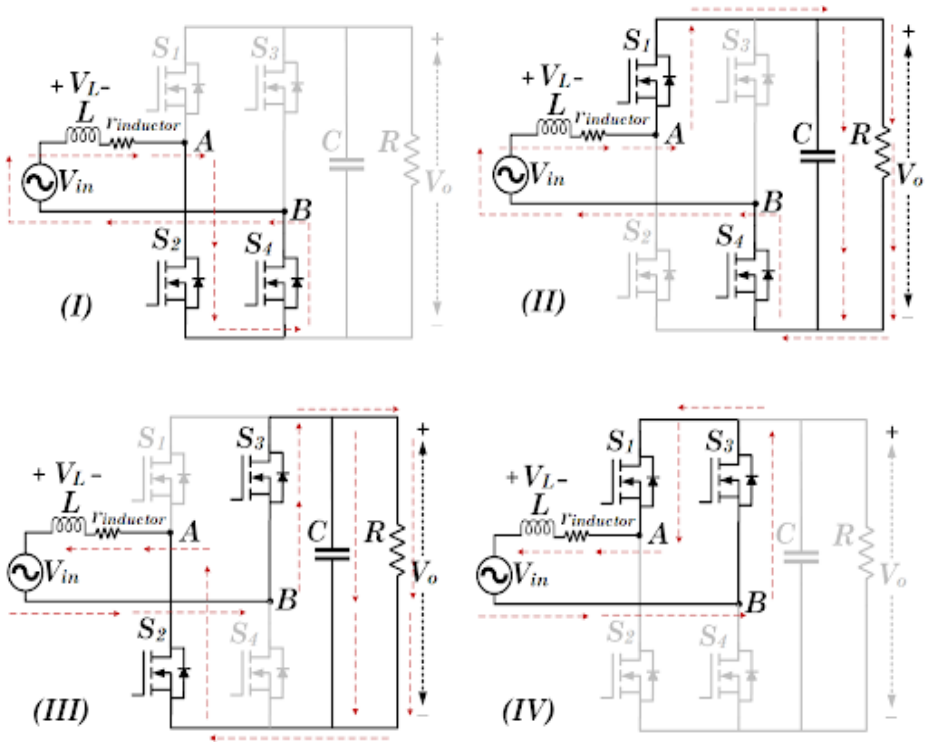


Figure 2.2:Modes of Operation of TPFC

Table 2.1: Modes of Operation and Instantaneous Inductor Voltages

Mode	Input Voltage (V_{in})	Switching States				Instantaneous Inductor Voltage (V_L)
		S1	*S2*	*S3*	*S4*	
I	$V_{in}>0$	OFF	ON	OFF	ON	$V_L(t) = V_{in}(t) - i(t)r_L$
II	$V_{in}>0$	ON	OFF	OFF	ON	$V_L(t) = V_{in}(t) + V_o - i(t)r_L$
III	$V_{in}<0$	OFF	ON	ON	OFF	$V_L(t) = V_{in}(t) + V_o - i(t)r_L$
IV	$V_{in}<0$	ON	OFF	ON	OFF	$V_L(t) = V_{in}(t) - i(t)r_L$

2.3. Analytical Modeling of Harmonics for TPFC

In order to obtain a model pertaining to the harmonic spectrum of the input current and its relation with the various design specifications, a comprehensive characterization of the various higher order frequency components is presented in this section by analyzing the conventional control scheme of a PFC circuit [33]. Figure 2.3 shows the control structure of TPFC including the outer voltage loop and inner current loop. The error (ΔV_o) between the reference (V_O^*) and sensed voltage (V_O) is processed in a PI controller to obtain the value of the transconductance term (g), which when multiplied with the sensed input voltage ($V_S \sin \omega t$), provides the reference input current (i^*). The sensed current (i) tracks the reference by synthesizing the value of δ in the PI controller and processing it for gate signal generation. To estimate the harmonics present in the sensed/actual input current, a time domain-based power transfer approach is used. The instantaneous power transfer in the PFC circuit can be described as the product of the supply voltage and supply current,

which is essentially the summation of all the harmonic components along with the fundamental frequency component, as depicted in (2.2).

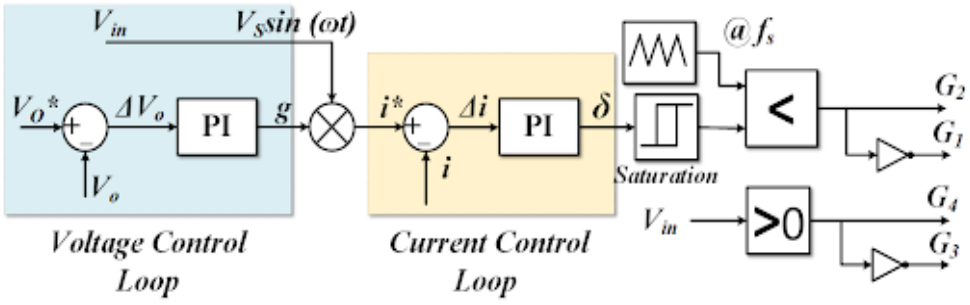


Figure 2.3: Conventional Control Scheme for TPFC

$$P(t) = V_S \sin \omega t \sum_{h=1}^{\infty} I_h \sin h\omega t \tag{2.2}$$

$$\sum_{h=1}^{\infty} I_h \sin h\omega t = A_1 \sin \omega t + A_3 \sin 3\omega t + A_5 \sin 5\omega t + \cdots \tag{2.3}$$

where ω is the grid frequency.

Using (2.2), and expanding the equation for $P(t)$, we obtain:

$$P(t) = \frac{V_S A_1}{2} + \frac{V_S(A_3 - A_1)}{2} \cos 2\omega t + \frac{V_S(A_5 - A_3)}{2} \cos 4\omega t + \frac{V_S(A_7 - A_5)}{2} \cos 6\omega t + \cdots \tag{2.4}$$

The output current gets bifurcated between the output load current (I_o) and output capacitor current (I_{Co}), as follows:

$$I_O(t) = \frac{V_S A_1}{2V_O} \tag{2.5}$$

$$I_{Co}(t) = \frac{V_S(A_3 - A_1)}{2V_O} \cos 2\omega t + \frac{V_S(A_5 - A_3)}{2V_O} \cos 4\omega t + \frac{V_S(A_7 - A_5)}{2V_O} \cos 6\omega t + \cdots \tag{2.6}$$

The higher frequency terms in the capacitor current essentially lead to the ripple component (ΔV_o) appearing at the DC link output voltage, which can be formulated as:

$$\Delta V_O(t) = \frac{1}{C}\int_0^t I_{Co} = \frac{V_S(A_3-A_1)}{4\omega V_O C}\sin 2\omega t + \frac{V_S(A_5-A_3)}{8\omega V_O C}\sin 4\omega t + \frac{V_S(A_7-A_5)}{12\omega V_O C}\sin 6\omega t \ldots \quad (2.7)$$

As observed in Figure 2.3, the error (ΔV_o) between the reference and the sensed output voltage constitutes the ripple component formulated in (2.7), which is passed through a PI controller to get the transconductance term (g), as shown below:

$$g(t) = \Delta V_O K_P + K_i \int \Delta V_O(t)dt \quad (2.8)$$

$$g(t) = \frac{V_S K_P(A_3-A_1)}{4\omega V_O C}\sin 2\omega t + \frac{V_S K_P(A_5-A_3)}{8\omega V_O C}\sin 4\omega t + \frac{V_S K_P(A_7-A_5)}{12\omega V_O C}\sin 6\omega t + \cdots \quad (2.9)$$

Further, to obtain the reference current ($i^*(t)$), the transconductance term is multiplied with the source voltage as shown below:

$$i^*(t) = g(t) * V_S \sin \omega t \quad (2.10)$$

$$i^*(t) = \frac{V_S^2 K_P(A_3-A_1)}{8\omega V_O C}\cos \omega t + \frac{V_S^2 K_P(2A_1+A_5-3A_3)}{16\omega V_O C}\cos 3\omega t +$$

$$\frac{V_S^2 K_P(3A_3+2A_7-5A_5)}{48\omega V_O C}\cos 5\omega t + \cdots + \frac{V_S^2 K_i(A_3-A_1)}{16\omega V_O C}\sin \omega t + \frac{V_S^2 K_i(4A_1+A_5-5A_3)}{64\omega V_O C}\sin 3\omega t +$$

$$\frac{V_S^2 K_i(9A_3+4A_7-13A_5)}{576\omega V_O C}\sin 5\omega t + \cdots \quad (2.11)$$

Combining all the similar frequency terms, a comprehensive model depicting the magnitude and phase of each harmonic component present in the input current waveform is obtained as shown below:

$$i^*(t) = M_1 \sin(\omega t + \varphi_1) + M_3 \sin(3\omega t + \varphi_3) + M_5 \sin(5\omega t + \varphi_5) + \cdots (2.12)$$

where, $M_1 = \frac{V_S^2(A_3-A_1)}{8\omega V_O C}\sqrt{K_P^2 + \frac{K_i^2}{4}}$ (2.13)

$$M_3 = \frac{V_S^2}{16\omega V_O C}\sqrt{K_P^2(2A_1 + A_5 - 3A_3)^2 - \frac{K_i^2(4A_1+A_5-3A_3)^2}{16}} \quad (2.14)$$

$$M_5 = \frac{V_S^2}{48\omega V_O C}\sqrt{K_P^2(3A_3 + 2A_7 - 5A_5)^2 - \frac{K_i^2(9A_3+4A_7-13A_5)^2}{144}} \quad (2.15)$$

$$\varphi_1 = \tan^{-1}\frac{2K_P}{K_i},\ \varphi_3 = \frac{4K_P(2A_1+A_5-3A_3)}{K_i(4A_1+A_5-5A_3)},\ \varphi_5 = \frac{12K_P(3A_3+2A_7-5A_5)}{K_i(9A_3+4A_7-13A_5)} \quad (2.16)$$

Using appropriate value of the current loop PI controller (as seen in Figure 2.3) to obtain the value of duty ratio term (δ), the resultant current (i) follows I_{ref}, which includes all the harmonic components as observed in (2.12), thus resulting in the source current to have harmonics imbibed along with the fundamental component.

2.3.1. Performance Verification of the Developed Harmonic Model

As observed in (2.12), the magnitude and the phase of the higher order harmonics present in the input current of a PFC depend extensively on the design specifications and corresponding control parameters. To correlate the developed model with the results obtained for different design specifications, a detailed comparative analysis between the analytically derived and simulated values at different load power and input voltage levels is presented. Figure 2.4(a) presents the third harmonic magnitudes for a range of load levels between 1 to 3.3 kW for two input RMS voltage levels of 115V and 230V. As observed, the magnitude of the third harmonic component tends to increase with increase in the load power, which adheres to the analytically developed model. Similarly, as shown in Figure 2.4(b), with the increase in the input voltage (in a universal single phase voltage range, i.e., 85-265V), the magnitude of the third harmonic component experiences a growing slope, which matches well with the developed model.

To compare the analytical values with the simulated values of third harmonic component, Figure 2.5 demonstrates the correlation between third harmonic amplitude and input voltage levels between 85 to 265V at various power levels. As observed in Figure 2.5(a), for a rated input voltage of 230V at various load power levels, the developed model matches the simulation results with an error of 3%. Similarly, as shown in Figure 2.5(b), for a rated load of 3.3kW at various input voltage levels, the difference between the developed and the simulation model is 8%, which affirms the accuracy of the presented analysis. The errors correspond to the power component non-idealities included in the simulation model to accrue realistic result.

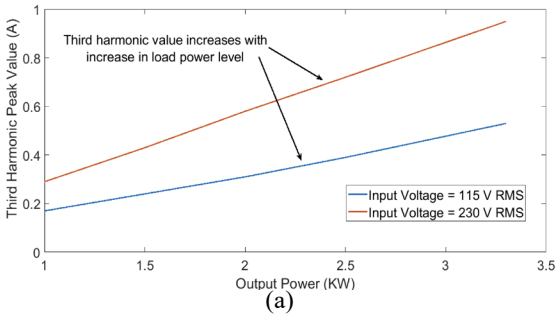


Figure 2.4: Third Harmonic Comparison with (a) Various Load Levels and (b) Input Voltage Levels

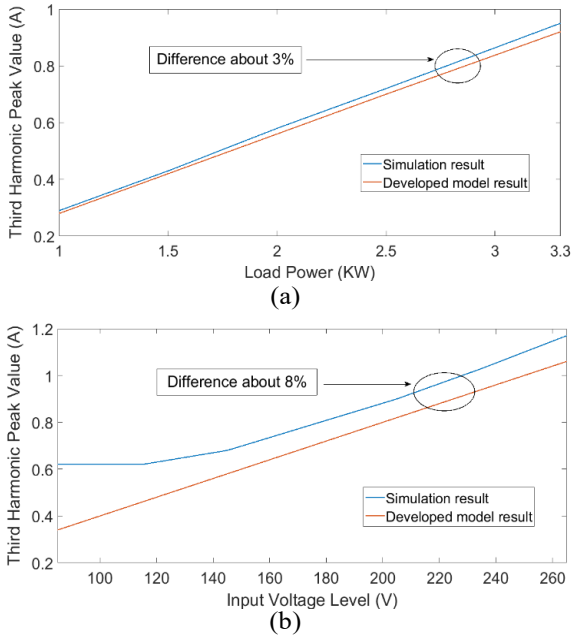


Figure 2.5: Performance of the Developed Model with (a) Various Load Levels and (b) Input Voltage Levels

2.4. Active Mitigation Scheme (AMS) for Third Harmonic Component

2.4.1. Comprehensive Two Stage Filter Design

As observed in (2.12), the magnitude of the third harmonic component can be reduced by oversizing the output capacitor, thus reducing ripple component. However, this passive approach leads to a bulky system, thus reducing the overall power density of the circuit. In order to subdue the third harmonic component, an active mitigation scheme is proposed herewith, that implements a digital filter to extract the third harmonic component from the sensed current, to provide active compensation, leading to reduced THD. To extract the third harmonic component from the sensed current, it is important to attenuate

its fundamental component to obtain a spectrum of only high frequency components. This can be achieved using a high pass filter designed as shown below:

$$G_{AMS,1}(s) = \frac{s^4}{(s+\omega_m)^4} \tag{2.17}$$

where, the design value of ω_m can be obtained using the relation: $\omega < \omega_m \ll 3\omega$, so that the filter only attenuates the fundamental component with minimum effect on the other harmonic components. Further, to specifically focus on eliminating the third harmonic component, a Notch filter [135] is designed that amplifies the third harmonic component, while attenuating the other higher harmonic components.

$$G_{AMS,1}(s) = \frac{s^4}{(s+\omega_m)^4} \tag{2.18}$$

where $\omega_n = 3\omega$ and $Q = 100$.

Thus, the overall filter design to eliminate the third harmonic component from the duty component (δ) is essentially a cascade combination of both – the high pass and the high-Q notch filter. The overall transfer function of the AMS filter can be written as:

$$G_{AMS}(s) = G_{AMS,1}(s) * G_{AMS,2}(s) = \frac{s^4\omega_n^2}{[s+\omega_m][s^2+\frac{2\omega_n}{Q}s+1]} \tag{2.19}$$

To implement this filter in a DSP, the transfer function in (2.19) is converted to discrete z-domain transfer function using $s = \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$ Thus, the resultant $G_{AMS}(z)$ can be written as:

$$G_{AMS}(z) = \frac{16(z-1)^4(z+1)^2T_s^2\omega_n^2}{\{16(z-1)^4+\omega_m^4T_s(z+1)^4+32\omega_mT_s(z-1)^3(z+1)+24\omega_m^2T_s^2(z-1)^2(z+1)^2+8\omega_m^3T_s^3(z-1)(z+1)^3\}} * \frac{1}{\left\{4(z-1)^2+\frac{\omega_n}{Q}T_s(z+1)+T_s^2(z+1)^2\right\}} \tag{2.20}$$

Expanding (2.20), we obtain a sixth order transfer function that can be shown as:

$$G_{AMS}(z) = \frac{p_6z^6+p_5z^5+p_4z^4+p_3z^3+p_2z^2+p_1z+p_0}{q_6z^6+q_5z^5+q_4z^4+q_3z^3+q_2z^2+q_1z+q_0} \quad (2.21)$$

where, the set of value for p_X and q_X ($x \in \{0,1 \dots 6\}$) for the design specifications mentioned in Table 2.3 are shown in Table 2.2. The filter characteristics of the design AMS filter is shown in Figure 2.6, which clearly portrays the gain (12dB) at the third harmonic component, with a major attenuation (-24dB) observed at the fundamental frequency component.

Table 2.2: Filter Coefficients for AMS

Numerator Coefficient	Denominator Coefficient
$p_0 = 4.55872\times10^{-5}$	$q_0 = 0.9989$
$p_1 = -3.99781\times10^{-5}$	$q_1 = -7.89221$
$p_2 = -4.55872\times10^{-5}$	$q_2 = 18.45873$
$p_3 = 12.44326\times10^{-5}$	$q_3 = -32.52085$
$p_4 = -4.55872\times10^{-5}$	$q_4 = 18.33473$
$p_5 = -3.99781\times10^{-5}$	$q_5 = -8.10026$
$p_6 = 4.55872\times10^{-5}$	$q_6 = 1.04528$

Table 2.3: Design Specifications for AMS Implementation

Parameters	Values
Input Voltage (V_{in})	85-120V RMS, 60Hz
Output Voltage (V_o)	400V
Output Power (P)	500W
Input Inductor (L)	500µH
Output Capacitor (C)	2mF
Switching Frequency (f_s)	100kHz

2.4.2. AMS Based Closed Loop Control Scheme

The third harmonic AMS based control scheme is shown in Figure 2.7. As observed, the sensed current (i) is processed in the AMS filter module to obtain its third

harmonic component (i_3), which is then multiplied with inverse plant transfer function to obtain the duty ratio term corresponding to the third harmonic component (δ_3). The obtained term δ_3 is subtracted from the synthesized duty control term δ, thus subduing the third harmonic term from the input current.

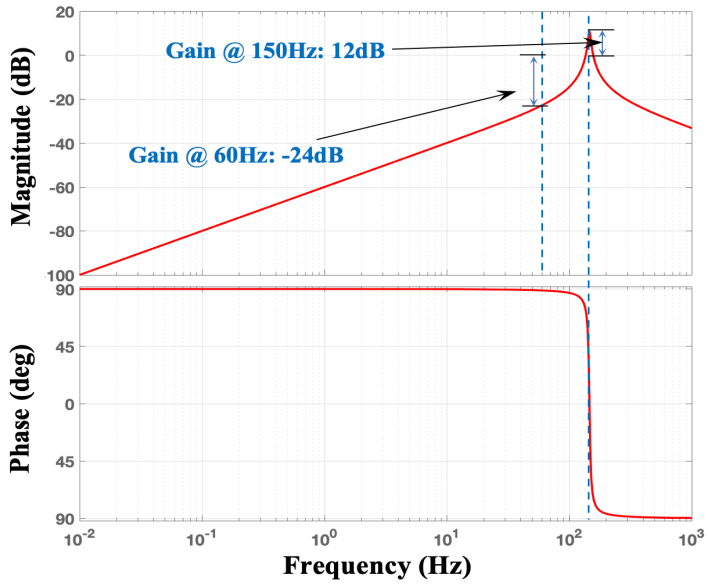


Figure 2.6: Filter Characteristics for AMS

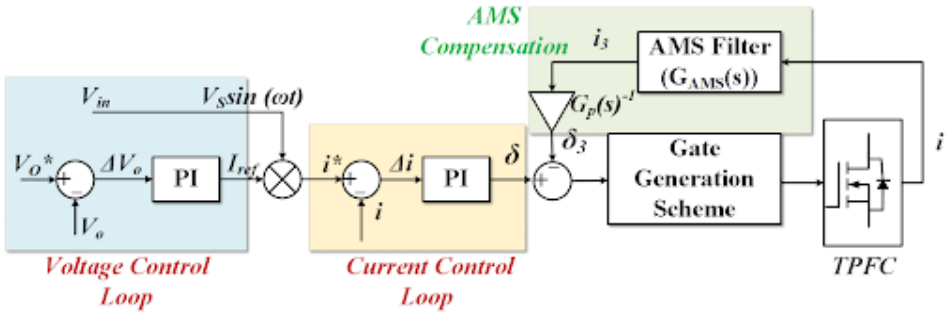


Figure 2.7: Proposed Control Scheme with Third Harmonic AMS

2.4.3. Simulation and Experimental Verification of AMS

To observe the performance of the developed harmonic analysis-based model and to elucidate the effectiveness of the proposed third harmonic AMS scheme, detailed

simulation and experimental results are presented in this section. Figure 2.8 shows the simulation results of the proposed third harmonic AMS. A comparison between the input current THD plot of a conventional control (as shown in Figure 2.9(a)) and the one for AMS (Figure 2.9(b)) shows a reduction in third harmonic component by 0.1072A, thus resulting in reduction in THD by 0.77%. Additionally, due to the reduction in the third harmonic component, the peak-to-peak ripple appearing across the output capacitor is also reduced to 1%, as seen in Figure 2.8.

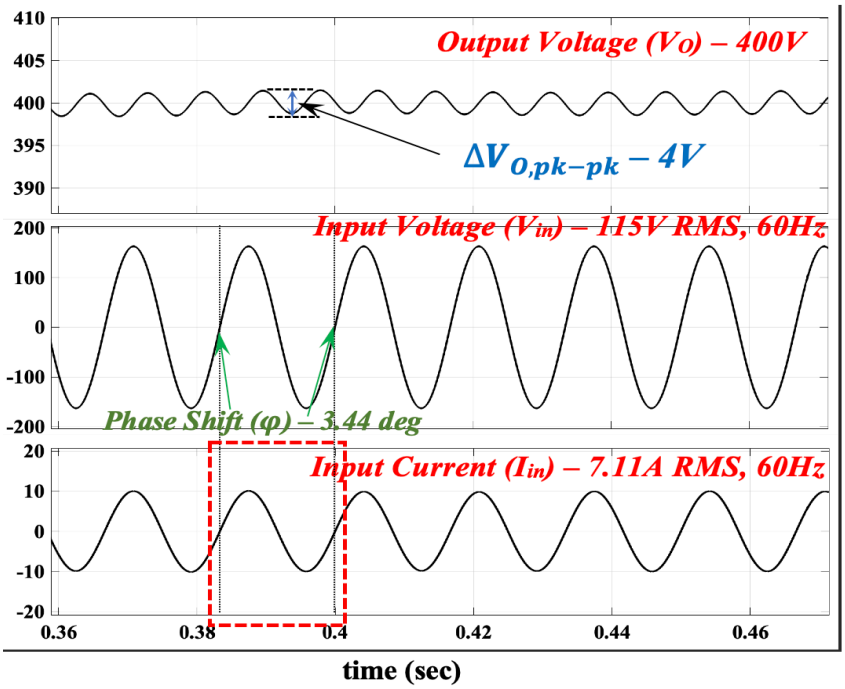
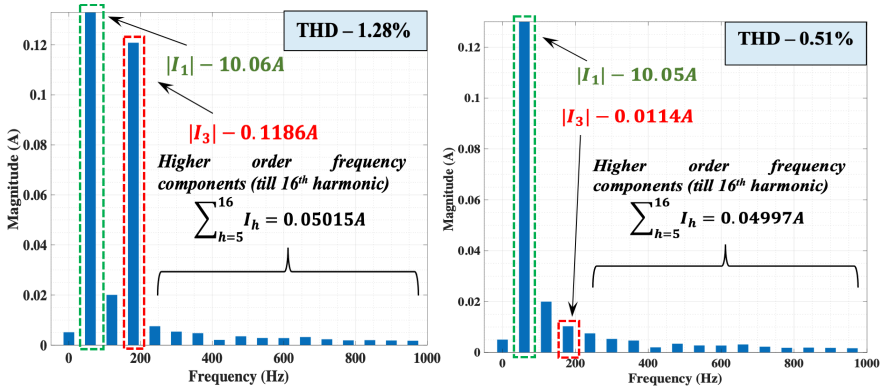


Figure 2.8: Simulation Results with Third Harmonic AMS (Y-axis: Output Voltage (V_o) – 5V/div, Input Voltage (V_{in}) – 100V/div, Input Current (I_{in}) – 10A/div; X-axis: Time - 20ms/div)



(a) (b)

Figure 2.9: Harmonic Spectrum (a) with Conventional Control Scheme (b) with Third Harmonic AMS

In order to validate the proof-of-concept of the proposed third order AMS, a laboratory prototype of TPFC (as shown in Figure 2.10) is designed and built with specifications listed in Table 2.3.

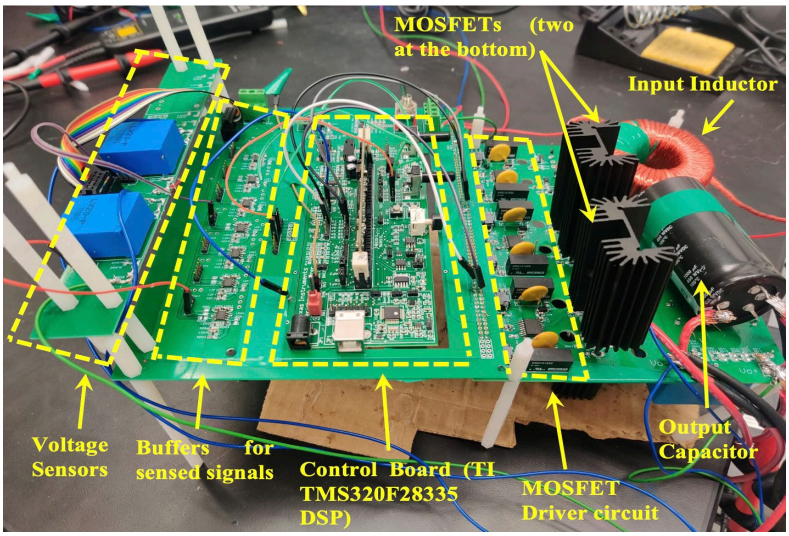


Figure 2.10: Developed Hardware Prototype for Implementation of Third Harmonic AMS for TPFC

Figure 2.11 shows the resultant input voltage, input current and output voltage waveforms obtained at 500W rated load. As observed, the current waveform follows the

input voltage with a phase lag of 9.24 degrees, thus achieving a power factor of 0.998 (lag). The proposed AMS leads to significant reduction in the third harmonic amplitude, thus resulting in a THD of 4.03% and an overall conversion efficiency of 97.4% at rated load.

Figure 2.12 illustrates the third harmonic magnitude at different power levels from 100W to 500W with/without AMS technique from analytical model, simulation, and hardware results. This figure shows that third harmonic component is reduced in all power levels even for very light loads. A minor deviation between the simulation and experimental results is seen is due to the additional parasitic capacitances and PCB trace inductances appearing in the hardware circuit, which are normally not accounted for simulation studies.

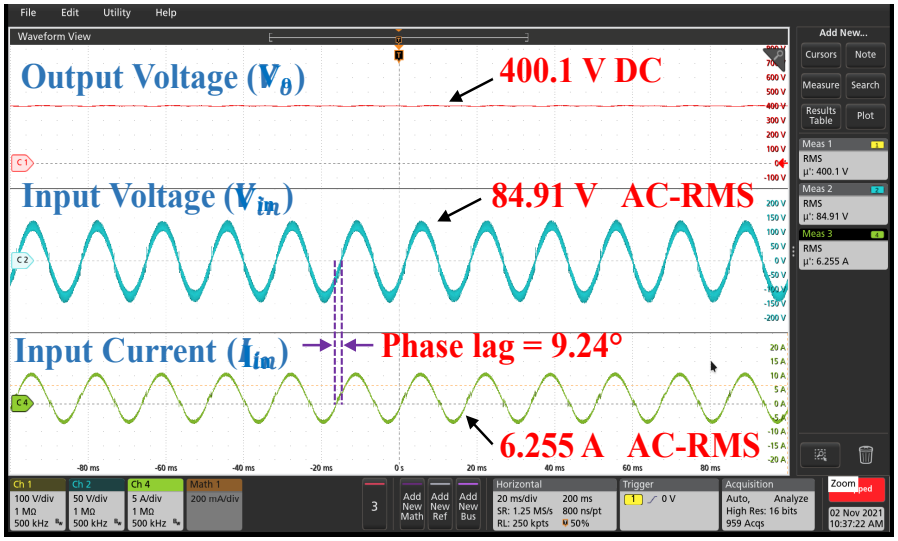


Figure 2.11: Experimental Waveforms with Implementation of AMS Technique (Y-axis: V_o=100V/div, V_{in}=50V/div, I_{in} = 5A/div; X-axis: Time=20ms/div)

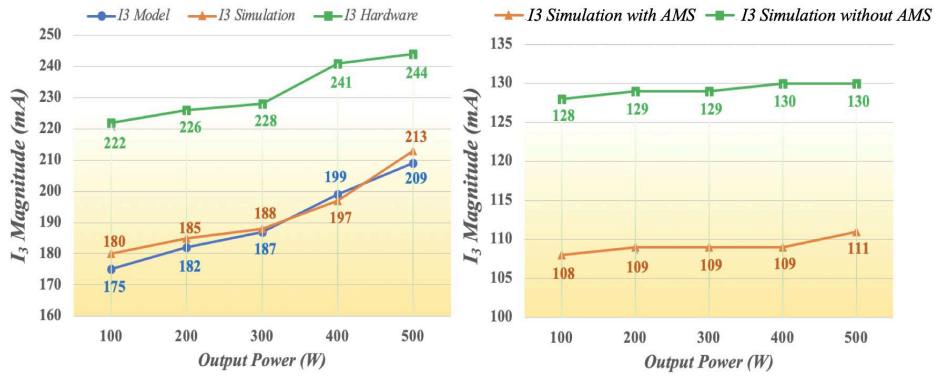
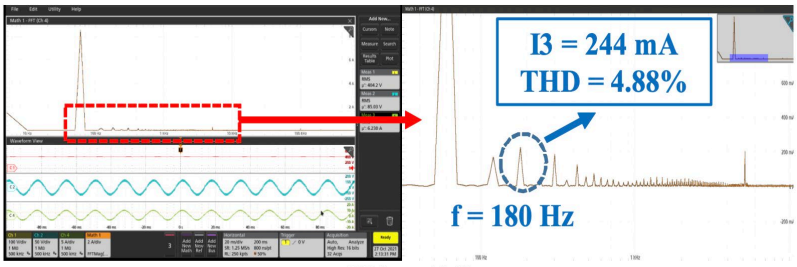
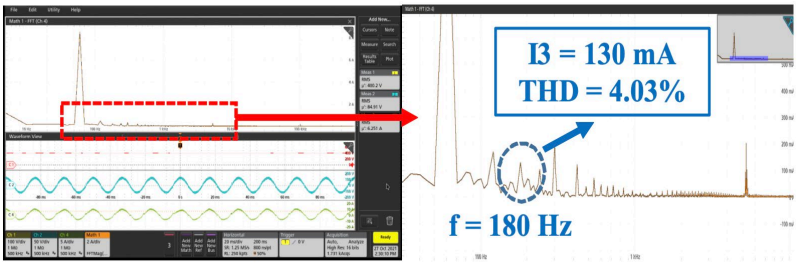


Figure 2.12: Third Harmonic Magnitude at Different Power Levels With/Without AMS Technique

Figure 2.13 depicts the FFT and steady state waveforms from experimental tests for two situations with/without implementing AMS technique. With conventional control scheme, third harmonic magnitude is 244 mA with an effective THD of 4.88% appearing in the input current. On the other hand, after implementing the AMS scheme to the control scheme, third harmonic magnitude decreases to 130 mA resulting in 4.03% THD in input current waveform.



Without AMS



With AMS

Figure 2.13: Experimental Results With/Without AMS Technique (Y-axis: V_o=100V/div, V_{in}=50V/div, I_{in} = 5A/div; X-axis: Time=20ms/div)

The FFT spectrum of input current with notch filter shows that there are some oscillations around third harmonic frequency. The reason is that the notch filter passes the frequencies in its band, so it affects the signal around the center frequency.

Comparison of the FFT of input current waveform from simulation and hardware tests for both situations with/without AMS implementation is presented in Figure 2.14. As observed, third harmonic magnitude is reduced by 46% as compared to its magnitude without the AMS scheme. Since the filter is designed for third harmonic mitigation, we expect it to have no effect on other frequencies. Findings also confirm this, and as Figure 2.14 shows, all higher order harmonics have similar magnitude for both with/without AMS situations.

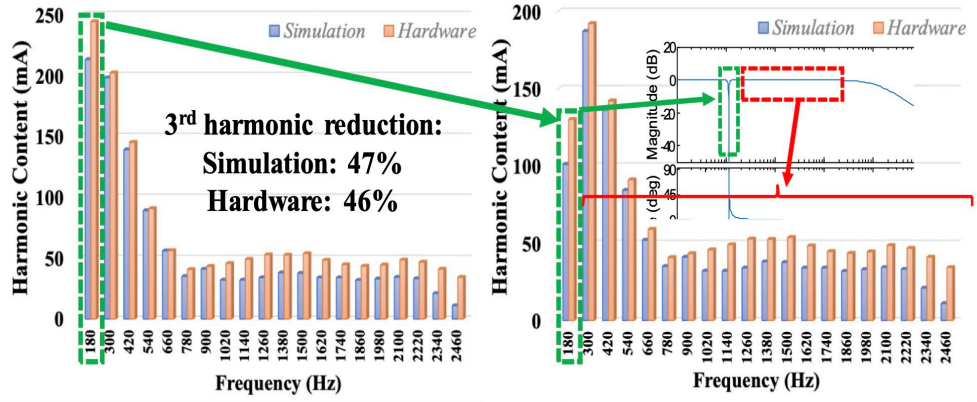


Figure 2.14: FFT Spectrum of Input Current from Simulation and Hardware Results With/Without AMS Technique

Table 2.4 investigates this effect and power factor for different power levels is calculated in this table. The resultant power factor in Table 2.4 is calculated as shown below:

$$\text{Resultant Power factor } (pf) = \cos \emptyset * DF \tag{2.22}$$

where, Distortion factor (DF) $= \frac{I_1}{\sqrt{\sum_{h=1}^{\infty} I_h^2}} = \frac{1}{\sqrt{1+THD_i^2}}$ (2.23)

Table 2.4: Power Quality for Different Power Levels

Load Power (W)	cos Ø	THD (%)	Power Factor
100	0.994	6.22	0.942
200	0.951	5.43	0.950
300	0.958	5.01	0.957
400	0.979	4.54	0.978
500	0.987	4.03	0.986

2.5. Current Sensorless Control Scheme for TPFC

The proposed sensorless control scheme uses fundamental concepts of volt-sec balance across the inductor in discrete domain to formulate the equation for current estimation. The control scheme formulation, along with the closed loop design and its stability analysis is presented in this section.

2.5.1. Control Scheme Formulation

Utilizing the system states and inductor voltages derived in Section 2.2, the equivalent circuit of the TPFC is shown in Figure 2.15 that analyzes the circuit in average domain. As observed in Table 2.1, the instantaneous inductor voltage includes a '$i(t)r_L$' drop to account for the resistance drop, thus providing a more realistic formulation of the TPFC topology. As seen in Figure 2.1, the inductor is represented as a series combination of inductor L and equivalent winding resistance r_L. Here, the component r_L is considered to be a lumped series model of the winding resistance and the channel resistance ($R_{DS,on}$)

of the two conducting MOSFETs, as highlighted in the modes of operation shown in Figure 2.2.

$$r_L = r_{inductor} + 2R_{DS,on} \tag{2.24}$$

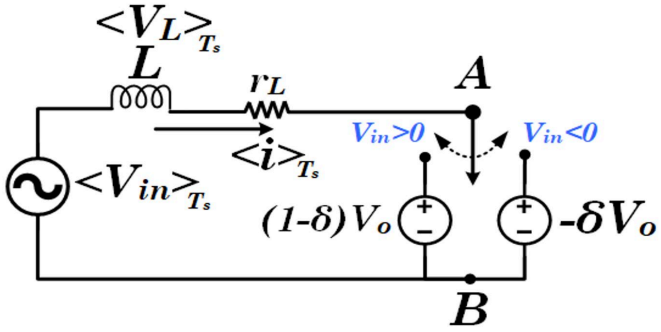


Figure 2.15: Equivalent Single Switch Circuit in Average Domain

As observed in the figure, V_{AB} toggles between 0 and V_o, depending on whether S_1 or S_2 is on. Therefore, the average of V_{AB} over a switching cycle can be expressed as: -

$$\langle V_{AB}\rangle_{T_s} = \begin{cases} (1-\delta)V_o & ; \quad V_{in} > 0 \\ -\delta V_o & ; \quad V_{in} < 0 \end{cases} \tag{2.25}$$

Thus, the average value of inductor voltage in steady state can be formulated as shown in (2.26): -

$$\langle V_L\rangle_{T_s} = L\,\langle \frac{di}{dt}\rangle_{T_s} = \langle V_{in}\rangle_{T_s} - \langle V_{AB}\rangle_{T_s} - \langle i\rangle_{T_s} r_L \tag{2.26}$$

Rearranging the terms, we obtain the expression for rate of change inductor current as shown in (2.27): -

$$\langle \frac{di}{dt}\rangle_{T_s} = \begin{cases} \frac{\langle V_{in}\rangle_{T_s} - (1-\delta)V_o - \langle i\rangle_{T_s} r_L}{L} & ; \quad V_{in} > 0 \\ \frac{\langle V_{in}\rangle_{T_s} + \delta V_o - \langle i\rangle_{T_s} r_L}{L} & ; \quad V_{in} < 0 \end{cases} \tag{2.27}$$

Discretizing (2.27) with a sampling frequency of f_n, we obtain the difference between the current sample and the previous sample of inductor current: -

$$i(n) - i(n-1) = \begin{cases} \left[\frac{V_{in}(n) - (1-\delta(n))V_o - i(n-1)r_L}{L}\right] T_n & ; \quad V_{in} > 0 \\ \left[\frac{V_{in}(n) + \delta(n)V_o - i(n-1)r_L}{L}\right] T_n & ; \quad V_{in} < 0 \end{cases} \tag{2.28}$$

where, *i(n)* denotes the nth sample of current *i* and $T_n \left(= \frac{1}{f_n}\right)$ is the sampling period. Rearranging the terms in (2.28), we obtain a closed form expression for the nth sample of *i,* as shown in (2.29).

$$i(n) = i(n-1) + Y(n-1) \tag{2.29}$$

$$Y(n-1) = \begin{cases} \left[\frac{V_{in}(n) - (1-\delta(n))V_o - i(n-1)r_L}{L}\right] T_n & ; \quad V_{in} > 0 \\ \left[\frac{V_{in}(n) + \delta(n)V_o - i(n-1)r_L}{L}\right] T_n & ; \quad V_{in} < 0 \end{cases} \tag{2.30}$$

Thus, as observed in (2.29-2.30), instead of sensing the input current, in this control scheme, the current reference signal is generated by utilizing the sensed values of input voltage, output voltage and the previous sampled value of current *i*, which is typically stored as an array in a microcontroller.

2.5.2. Closed Loop Stability Analysis

To understand the dynamic performance of the proposed sensorless control scheme, it is noteworthy to derive the closed loop transfer function of the PFC circuit, formulating the controller and plant transfer function in conjunction with the derived control scheme. Please note that as the current estimation scheme involves discretization of continuous variables with a defined sampling time, the closed loop transfer function is derived in z-domain (discrete) and then converted to s-domain (continuous) for evaluating the gain margin and phase margin of the overall plant. Formulating the small-signal z-domain equivalent of (2.29) for the case $V_{in}>0$, we obtain: -

$$\Delta i(z) - z^{-1}\Delta i(z) = \frac{T_n}{L} V_O \Delta\delta - \frac{T_n}{L} r_L z^{-1} \Delta i(z) \tag{2.31}$$

Simplifying (2.31), we get discrete feedback transfer function ($G_f(z)$) as:

$$G_f(z) = \frac{\Delta i(z)}{\Delta\delta(z)} = \frac{V_o T_n}{L + z^{-1} r_L T_n - z^{-1} L} \tag{2.32}$$

The plant transfer function ($G_p(s)$) of a practical TPFC can be written as:

$$G_P(s) = \frac{V_o}{sL + r_L} \tag{2.33}$$

Using bi-linear transformation to convert the system from continuous to discrete domain, s is replaced by $\frac{2}{T_n}\left[\frac{1-z^{-1}}{1+z^{-1}}\right]$ in (2.33), to obtain (2.34) and (2.35) as follows: -

$$G_C(z) = K_p + K_i \left[\frac{T_n}{2} \frac{1+z^{-1}}{1-z^{-1}}\right] \tag{2.34}$$

$$G_P(z) = \frac{V_o T_n (1+z^{-1})}{2(1-z^{-1}) + r_L T_n (1+z^{-1})} \tag{2.35}$$

where, $G_c(z)$ represents the PI controller transfer function. Using (2.32), (2.34) and (2.35), a closed loop discrete domain transfer function is developed (as shown in Figure 2.16). The closed loop small-signal transfer function $\frac{\Delta i(z)}{\Delta i^*(z)}$ can be shown as: -

$$\frac{\Delta i(z)}{\Delta i^*(z)} = \frac{G_C(z) G_P(z)}{1 + G_C(z) G_f(z)} \tag{2.36}$$

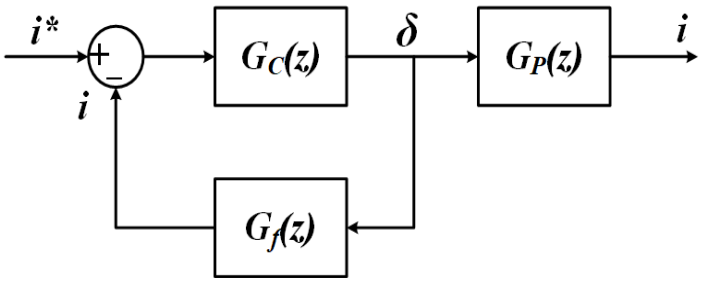


Figure 2.16: Closed Loop Discrete Domain Controller Scheme

Substituting the expressions for $G_C(z)$ and $G_P(z)$, the overall closed loop transfer function (obtained from Figure 2.16) in discrete domain is shown in (2.37). The frequency response of the transfer function obtained by discretizing the plant ($G_P(z)$), and that obtained by the discrete model of the TPFC ($G_f(z)$) are shown in Figure 2.17. As observed, the bode plots portray exactly similar characteristics, which validates the developed model with respect to the design specifications involved in the control scheme formulation.

Although the frequency characteristics of both the plants are the same, the methodologies to obtain the respective transfer functions are completely different. $G_P(z)$ is obtained by discretizing the small signal equivalent of a TPFC circuit, while $G_f(z)$ is obtained by analyzing the current ripple equations of a TPFC in discrete domain, by considering the state equations of the system along with the design specifications.

To provide stability analysis of the controller (for a sample time corresponding to 100kHz switching frequency), the frequency response of the closed loop transfer function as shown in (2.37) is described in Figure 2.18. As seen in the figure, the crossover frequency of the system is attained at 8.9 kHz, with a positive phase margin (PM) of 22.7^0, rendering it in the stable operating zone. Additionally, the gain of the system at 60Hz is 0dB or unity, thus signifying accurate reference tracking with ideally no estimation error. The phase remains negative (between 0^o and -180^o) in the operating zone, proving its robustness against any dynamic change.

$$\frac{\Delta i(z)}{\Delta i^*(z)} = \frac{z^{-2}\left[V_O K_i T_n^2 - 2K_P V_O T_n\right] + z^{-1}\left[2V_O K_i T_n^2\right] + \left[2K_P V_O T_n + V_O K_i T_n^2\right]}{2z^{-2}\left[L - T_n r_L\right] + z^{-1}\left[2T_n r_L - 4L - 2K_P T_n V_O + K_i T_n^2 V_O\right] + \left[2L + 2K_P T_n V_O + K_i T_n^2 V_O\right]} \quad (2.37)$$

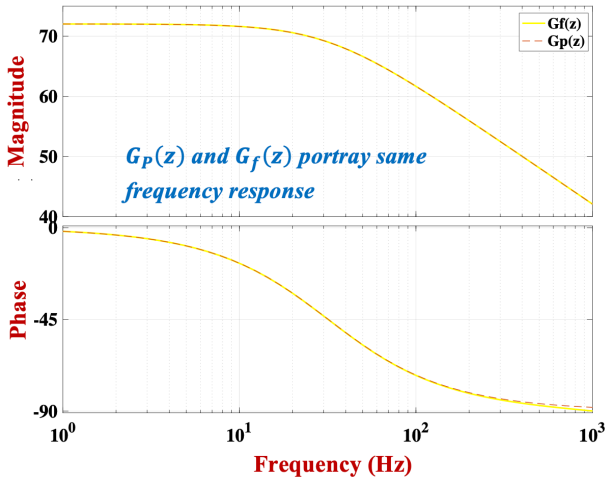


Figure 2.17: Frequency Response of $G_P(z)$ and $G_f(z)$

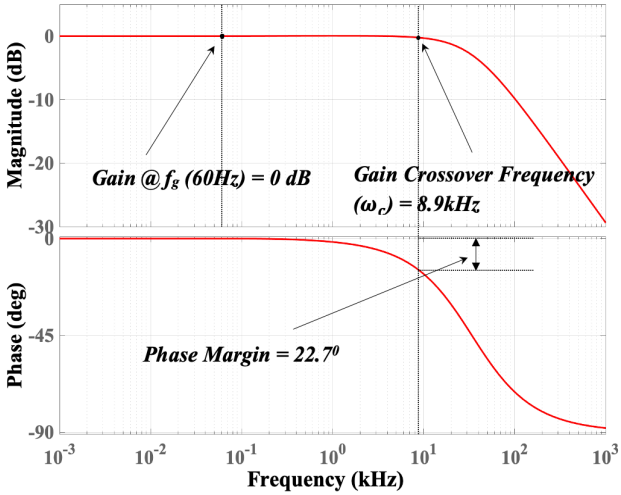


Figure 2.18: Bode Plot of the Closed Loop Transfer Function $\left(\frac{\Delta i(z)}{\Delta i^*(z)}\right)$

2.5.3. Closed Loop Control Scheme Schematic

As seen in (2.29), the current signal can be reproduced using the previous sampled value of *i* (i.e., *i(n-1)*) and voltage drop across the inductor at that sampling instant. The corresponding proposed control scheme is shown in Figure 2.19. The error (ΔV_o), obtained by comparing the actual sensed DC voltage (V_o) and reference DC voltage (V_o*), is passed

through a proportional integrator (PI) that provides the peak value of reference input current ($\hat{I}_{ref}$). This reference is multiplied by synchronously obtained $\sin \omega t$ to generate reference input current i^*. This reference signal is compared with the estimated current signal i, obtained using (2.29-2.30), to generate current error (Δi). This error is then processed in the current PI controller to generate the required duty signal (δ). A saturation block is usually used to limit the value of δ between 0 and 1. Finally, this generated duty signal is compared with carrier signal to generate the required gate pulses for switches S_1 and S_2.

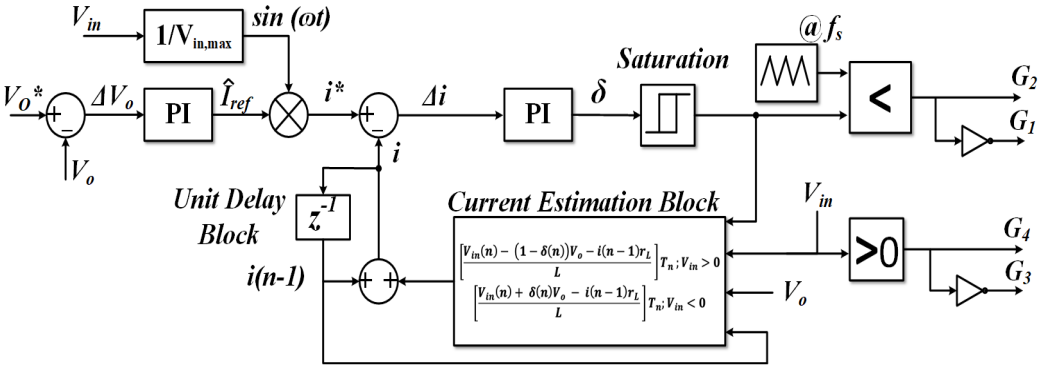


Figure 2.19: Proposed Discretized Sampling-Based Sensorless Control Scheme

2.5.4. Sensitivity Analysis for Parameter Uncertainty

The closed loop transfer function of the proposed control scheme is as shown in (2.37). Simplifying it for the purpose of this study, it can be alternatively written as (2.38) using control loop reconfiguration, which signifies the ratio between the small signal estimated current (Δi) and reference current (Δi^*).

$$T_{CL}(s) = \frac{\Delta i}{\Delta i^*} = \frac{sK_pV_o + V_oK_i}{s^2L + s(r_L + V_oK_p) + V_oK_i} = G(s) \tag{2.38}$$

$$G(\omega) = \frac{\sqrt{(V_o K_i)^2 + (\omega K_p V_o)^2}}{\sqrt{\omega^2 (r_L + V_o K_p)^2 + (V_o K_i - \omega^2 L)^2}} \tag{2.39}$$

The corresponding phase angle of the above-mentioned transfer function (2.38) can be written as: -

$$\angle T_{CL}(\omega) = \tan^{-1}[x] - \tan^{-1}[y] \tag{2.40}$$

$$\text{where, } x = \frac{K_p \omega}{K_i} \text{ and } y = \frac{(K_p V_o + r)\omega}{K_i V_o - \omega^2 L} \tag{2.41}$$

The closed loop transfer function shown in (2.37) aims to find the relation in terms of the gain and phase between the reference current signal and the synthesized input current signal. Considering appropriately tuned current controller, it is necessary that the estimated current signal accurately tracks the reference current signal, which essentially is in phase with the input voltage. Thus, any discrepancy in terms of tracking the reference will correspond to the gain difference and phase lag between $i^*$and i. As i^* follows the input voltage V_{in}, the cosine of angle shown in (2.42) principally portrays the power factor at the input.

$$PF(\omega) = \cos \angle T_{CL}(\omega) \tag{2.42}$$

$$= \cos[\tan^{-1}(x) - \tan^{-1}(y)] = \frac{1 + xy}{\sqrt{1 + x^2}\sqrt{1 + y^2}} \tag{2.43}$$

Substituting the expressions of x and y from (2.44), we get

$$PF(\omega) = \frac{1 + \frac{K_p \omega^2 (K_p V_o + r)}{K_i (K_i V_o - \omega^2 L)}}{\sqrt{1 + \left(\frac{K_p \omega}{K_i}\right)^2}\sqrt{1 + \left(\frac{(K_p V_o + r)\omega}{K_i V_o - \omega^2 L}\right)^2}} \tag{2.44}$$

At steady state, under nominal operation, the gain and the phase of the closed loop transfer function should be the following:

$$|G(\omega)|_{\omega=\omega_o} = G^* = 1 \tag{2.45}$$

$$\angle T_{CL}(\omega)|_{\omega=\omega_o} = 0^0 \tag{2.46}$$

$$PF(\omega)|_{\omega=\omega_o} = PF^* = 1 \tag{2.47}$$

where, ω_o is the synchronous grid frequency.

As observed in (2.39) and (2.44), both the gain and the phase of the proposed control scheme are dependent on the system (converter) design parameters (specifically L and r_L). However, these parameters have a tendency to shift from their nominal values due to several factors. These factors include temperature derating of the components, aging effect, ampere-turn (NI) variation in an AC line cycle, etc. Corresponding to the variation in these passive components, the gain and the phase of the control scheme are also bound to changes. These variations are highly undesirable as this might cause shift in the stable operating region of the converter and might result in loss of stability, leading to (a) loss of reference tracking and (b) increase in phase displacement angle (i.e., degradation of the power factor). Hence, it is very important to examine the robustness of the proposed control scheme with respect to the variations in L and r_L. To avoid any discrepancy between the volt-sec calculated using the digitalized plant $G_P(z)$ and plant obtained by discretizing the current ripple equations ($G_f(z)$), the sample time in both hardware and simulation analysis is taken to be similar to the switching frequency. As observed in Figure 2.17, the frequency response for both $G_P(z)$ and $G_f(z)$ portray similar characteristics yielding similar values of $\delta(z)$, thus avoiding any mismatch between the switching periods. Further, the factors that may cause discrepancies in terms of voltage balance, including non-idealities in the system

and variation in the design parameters are identified and their effect on the system performance is studied and supported by the findings in this section.

To evaluate the estimation accuracy of the proposed control scheme with respect to the designed component parameters, a 'sensitivity' term is defined here. The sensitivity of a variable M with respect to state variable N, is defined as the ratio between the relative change in M and that in N [136].

$$S_N^M = \frac{\frac{\partial M}{M}}{\frac{\partial N}{N}} \tag{2.48}$$

As observed in (2.48), if N deviates from its defined value by $p\%$, then the corresponding change in M can be calculated as $S_N^M * p\%$. To prove the robustness of the proposed control scheme against parameter variation, four different sensitivity metrics are defined, that explain the variation of gain and power factor with respect to L and r_L (as shown in (2.49)-(2.52)) and their corresponding relative variations with respect to the change in system parameters are obtained through comprehensive simulation analysis. As observed in Figure 2.20, the slopes of performance metrics precisely follow the analytical results obtained by substituting the nominal design values in (2.49)-(2.53) (as shown in Table 2.5). Further, the sensitivity quotients are derived for the nominal system parameters (mentioned in Table 2-6). The results shown in Table 2.5 strongly indicate the robustness of the proposed control scheme against the variation in system design parameters. For example, even with 25% parameter uncertainty of r_L, the gain of the control system deteriorates by less than 0.1%.

Sensitivity of Gain with respect to L:

$$(S_L^G) = \frac{\partial G}{\partial L}\Big|_{\omega=\omega_o} \frac{L^*}{G^*} = \left[\frac{\omega_o\sqrt{\left(K_pV_ow_o\right)^2+(K_iV_o)^2}\left(K_iV_o-\omega_o^2L\right)}{\left[\left(K_pV_o\omega_o+r_L\omega_o\right)^2+\left(K_iV_o-\omega_o^2L\right)^2\right]^{3/2}}\right]\frac{L^*}{G^*} \tag{2.49}$$

Sensitivity of Gain with respect to r_L

$$(S_{r_L}^G) = \frac{\partial G}{\partial r}\Big|_{\omega=\omega_o} \frac{r_L^*}{G^*} = \left[\frac{-\omega_o\sqrt{\left(K_pV_ow_o\right)^2+(K_iV_o)^2}(K_iV_o\omega_o+r_L\omega_o)}{\left[\left(K_pV_o\omega_o+r_L\omega_o\right)^2+\left(K_iV_o-\omega_o^2L\right)^2\right]^{3/2}}\right]\frac{r^*}{G^*} \tag{2.50}$$

Sensitivity of PF with respect to L

$$(S_L^{PF}) = \frac{\partial PF}{\partial L}\Big|_{\omega=\omega_o} \frac{L^*}{PF^*} = \left[-\frac{\omega_o^4(K_pV_o+r_L)(K_pL\omega_o^2+K_ir_L)}{K_i\sqrt{\left[\frac{K_p^2\omega_o^2+K_i^2}{K_i^2}\right]}\left[K_iV_o-L\omega_o^2\right]^2\left[\frac{\omega_o^2(K_pV_o+r_L)^2}{\left(K_iV_o-L\omega_o^2\right)^2}+1\right]^{\frac{3}{2}}}\right]\frac{L^*}{PF^*} \tag{2.51}$$

Sensitivity of PF with respect to r_L

$$(S_{r_L}^{PF}) = \frac{\partial PF}{\partial r_L}\Big|_{\omega=\omega_o} \frac{r_L^*}{PF^*} = \left[-\frac{\omega_o^2(K_pL\omega_o^2+K_ir_L)}{K_i\sqrt{\left[\frac{K_p^2\omega_o^2+K_i^2}{K_i^2}\right]}\left[K_iV_o-L\omega_o^2\right]^2\left[\frac{\omega_o^2(K_pV_o+r_L)^2}{\left(K_iV_o-L\omega_o^2\right)^2}+1\right]^{\frac{3}{2}}}\right]\frac{r_L^*}{PF^*} \tag{2.52}$$

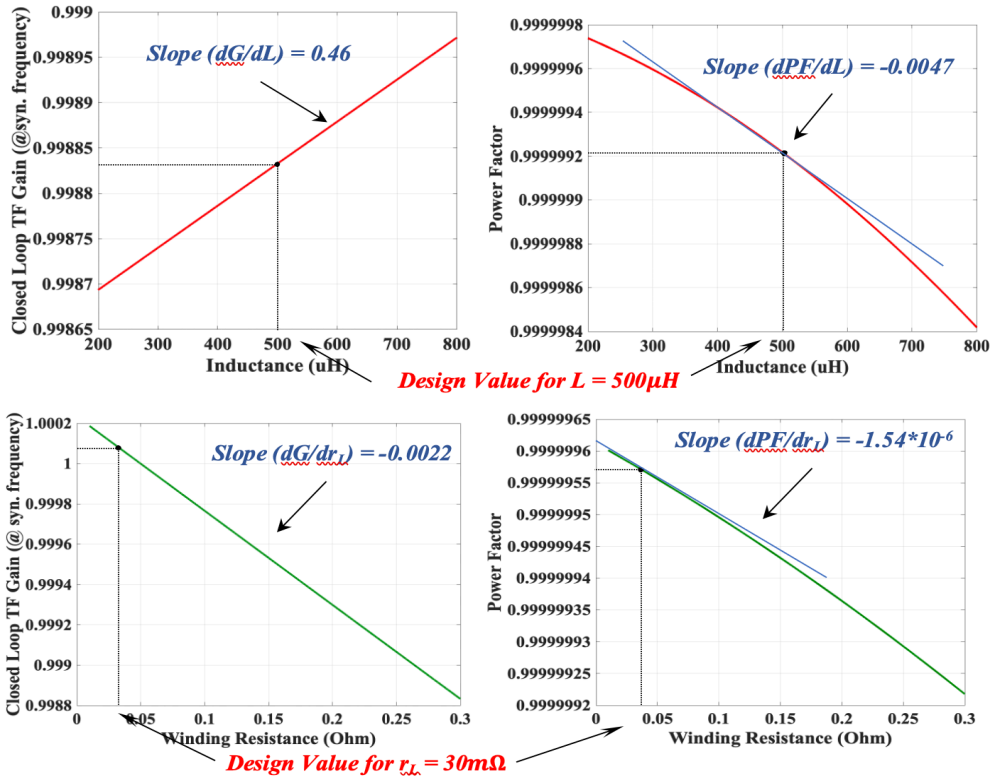


Figure 2.20: Relative Variation of Performance Metrics (Gain and PF) with Respect to System Parameters (L and r_L).

Table 2.5: Parameter Based Sensitivity Analysis

Variation in Estimation (M)	Change with respect to (N)	Relative Variation $\left(\frac{\partial M}{\partial N}\right)$	Sensitivity (S_N^M)
Gain (G)	L	$\frac{\partial G}{\partial L} = 0.46$	$S_L^G = 2.31 * 10^{-4}$
	r_L	$\frac{\partial G}{\partial r_L} = -0.0047$	$S_{r_L}^G = -0.0014$
Power Factor (PF)	L	$\frac{\partial PF}{\partial L} = -0.0022$	$S_L^{PF} = -1.15 * 10^{-6}$
	r_L	$\frac{\partial PF}{\partial r_L} = -1.54 * 10^{-6}$	$S_{r_L}^{PF} = -4.62 * 10^{-7}$

In addition to the analysis presented in terms of the individual effect of parameter uncertainty on system robustness, it is also critical to study the influence of coupled

variation of the system parameters (L and r_L) on the closed loop performance metrics for input current estimation (G and PF). Using the law of partial derivatives, at steady state, we can calculate the change in power factor (ΔPF) as shown in (2.53).

$$\Delta PF = \frac{\partial PF}{\partial L}\Delta L + \frac{\partial PF}{\partial r_L}\Delta r_L \tag{2.53}$$

Using the definition of sensitivity as derived in (2.51) and (2.52), we can restructure (2.53) as follows:

$$\Delta PF = S_L^{PF}\frac{PF}{L}\Delta L + S_{r_L}^{PF}\frac{PF}{r_L}\Delta r_L \tag{2.54}$$

Thus, the relative change in PF can be written as follows: -

$$\frac{\Delta PF}{PF} = S_L^{PF}\frac{\Delta L}{L} + S_{r_L}^{PF}\frac{\Delta r_L}{r_L} \tag{2.55}$$

Eq. (2.55) illustrates the relation between the relative variation of PF with respect to that of L and r_L (combined). If L experiences a change of p% and r_L changes by q%, then the relative variation in the PF can be calculated as $\{S_L^{PF}p + S_{r_L}^{PF}q\}$%.

Likewise, the relative change of gain can be also derived as:-

$$\frac{\Delta G}{G} = S_L^{G}\frac{\Delta L}{L} + S_{r_L}^{G}\frac{\Delta r_L}{r_L} \tag{2.56}$$

It is also noteworthy to understand the dependencies of each of the performance metric on the system parameters utilizing the correlations obtained in (2.55) and (2.56), to cognize which relative variation causes more dominant performance shift.

Referring to the results in Table 2.5, the effect of change in r_L on gain is more profound as compared to a change in L, as $S_{r_L}^{G} \approx 6 * S_L^{G}$. While the distortion in PF caused due to L is higher than that due to r_L, because $S_L^{PF} \approx 2.5 * S_{r_L}^{PF}$.

2.5.5. Moving Window Averaging Based Sampling for Disturbance Immunity

As seen in the previous sections, the stability of the current control loop majorly depends on the accurate estimation of the inductor current (i), which as seen in (2.29-2.30), depends on the sensed output voltage (V_o), input voltage (V_{in}), and the system parameters (L and r_L). As shown in the sensitivity analysis, the proposed control scheme is immune to variations in the system parameters. However, noises or glitches appearing in the sensed output or input voltage data caused due to undesired EMI noise coupling [137] or an erroneous voltage sensor can lead to inconsistencies in the inductor current reference estimation, leading to deviation from the stable operating region and hence resulting in the loss of PFC action. To account for these computational errors in the inductor current estimation, a moving point average-based output voltage sensor data computation methodology is proposed here. As shown in (2.28), the difference between the n^{th} and $(n-1)^{th}$ sample of the current can be expressed as a direct function of the sensed voltages:

$$\Delta i(n) = i(n) - i(n-1) = f(V_o(n), V_{in}(n)) \tag{2.57}$$

Any glitch or error (Δv) in the sensed output voltage, will directly affect the estimation, leading to a major deviation in the expected inductor current and output voltage profile as follows:

$$\Delta i(n)' = i(n)' - i(n-1) = f((V_o(n) + \Delta v), V_{in}(n)) \tag{2.58}$$

where $\Delta i(n)'$ is the modified value of estimated current due to the sensing error (Δv). To avoid the aforementioned deviation in the estimation, a 'K-point' average sensing method is proposed, that ensures suppression in the adversity caused due to the glitches.

For tracking the output voltage (with the proposed averaging scheme), the resultant n^{th} sample can be expressed as:

$$V_o(n) = \sum_{i=n-k}^{n} \frac{V_i}{K} \tag{2.59}$$

Implementing (2.59) in (2.58), the modified equation for current estimation can be expressed as follows:

$$\Delta i(n)'' = i(n)'' - i(n-1) = f((V_o(n) + \frac{\Delta v}{K}), V_{in}(n)) \tag{2.60}$$

As seen in (2.60), due to the modified sensing approach, the effect of the glitch (Δv) on the calculation of i(n) is reduced by a factor K. To verify the effectiveness of this technique, a simulation-based study is carried out to observe the effect of an unwanted glitch in the output voltage sensor data on the estimated inductor current and overall system performance. Figure 2.21 elucidates the resultant shift on the estimated inductor current, actual inductor current and output voltage for a sensorless PFC system for two cases: (a) without the 'K-point' averaging technique and (b) implementing the proposed technique with K = 50. To simulate an inconsistency in output voltage sensing, a glitch (having a duration of 100 μs) is superimposed with the sensed V_o data. In case (a), as observed in the figure, a sudden change in the output sensor data results in a sharp shift in the estimated current (i), leading to a fast change in the actual inductor current. On the other hand, in case (b), a similar change in output voltage sensor data results in a slower and suppressed variation in the estimated as well as the actual inductor current, which proves to be favorable for achieving stable operation. It is worth noting that as the value of 'K' is increased from 0 to 50, the system response is found to be slower. Thus, a suitable choice of the 'K' relies on the trade-off between noise immunity of the control loop and dynamic

response performance of the system. The K-point averaging scheme provides digital filtering against high frequency noise, specifically higher order switching frequency harmonics and/or other parasitic oscillations appearing in the sensed output voltage signal. Further, as seen in Figure 2.21, although selecting a higher value of K (i.e., oversampling) significantly reduces the effect of noise on the sensed signal, it reduces the system response time, and leads to loss of important ripple information.

In general, the output voltage contains combination of the 120Hz fundamental component and other higher order even grid-harmonic components (2k), that are responsible for the corresponding odd harmonic components (2k+1) present in the input current waveform [138]. Thus, filtering out the ripple component from the sensed signal will affect the system performance adversely due to absence of accurate error data between the reference and the sensed signal to be processed in the voltage controller loop. Thus, considering that constraint, the designer needs to appropriately select the value of K that ensures no loss of ripple information while attenuating only the higher order frequency noise from the sensed signal.

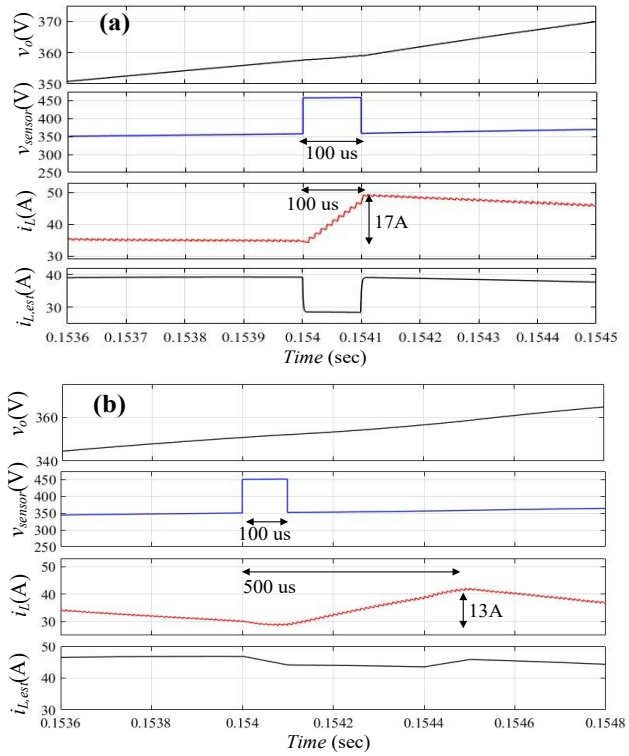


Figure 2.21: Effect of Implementing Moving Point Average on Sensed Output Voltage (V_o) (a) Without Moving Average or K = 0; (b) With Moving Average of K = 50.

2.5.6. Concept Verification Through Simulations and Experiments

Simulation based Analysis

To verify the system performance with the proposed control scheme, a simulation study is conducted in MATLAB/Simulink using the system parameters mentioned in Table 2.6. As seen in Figure 2.22, the input current (i) follows the input voltage (V_{in}) accurately (with a phase lag of 3.19^0, yielding a power factor of 0.998). The output voltage (V_o) reaches the set reference with a settling time of less than 10ms. Additionally, the output voltage ripple content is limited to 1% which avoids any undesired fluctuations during a steady state operation.

Table 2.6: Design Parameters for Sensorless Control Implementation

Parameters	Specifications
Input Voltage (V_{in})	110V RMS, 1-phase, 60Hz
Rated Load (P_o)	500W
Switching Frequency (f_s)	100kHz
Input Side Inductor (L)	500μH
MOSFET ($R_{DS,on}$)	65mΩ (TK39N60X,S1F)
Winding resistance (r_L)	30mΩ
Output Capacitor (C)	2mF
Sampling Time (T_n)	$10\mu s$
Output Voltage (V_o)	400V

To observe the dynamic performance of the control scheme, the system is subjected to a sudden change of load from 50W to 450W at t=0.4sec, portraying a 10% to 90% load change. As observed in Figure 2.23, the estimated current signal (i_L) (using the proposed scheme) accurately tracks the reference current (i^*) and correspondingly the measured input current waveform (i) follows a clean sinusoidal shape. Owing to the superior dynamic performance of the scheme, the system reaches the required stable operating point in less than 3 AC line cycles.

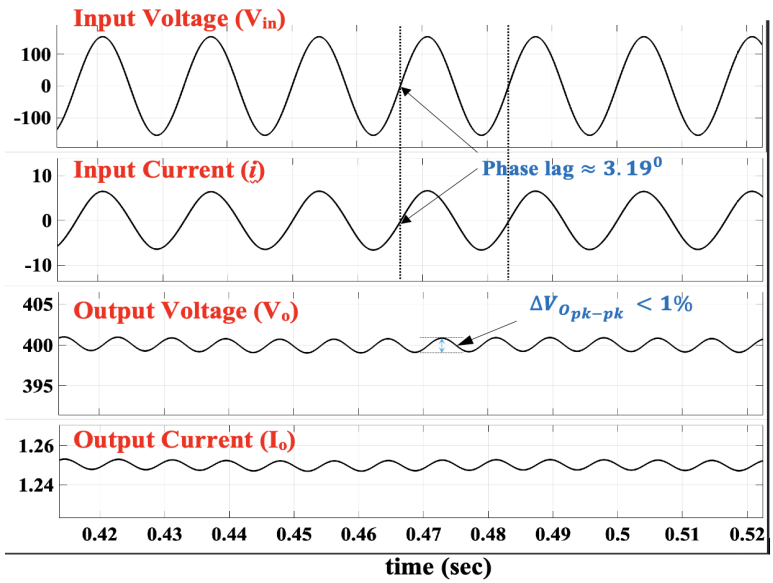


Figure 2.22: Steady State Simulation Results: Plot of Input Voltage (V_{in}) with Measured Input Current (i) and Corresponding Output Voltage (V_o) and Output Current (I_o) at Rated Load [Y-axis: V_{in} – 100V/div, i – 10A/div, V_o – 5V/div, I_o – 0.2A/div; X-axis: 10ms/div]

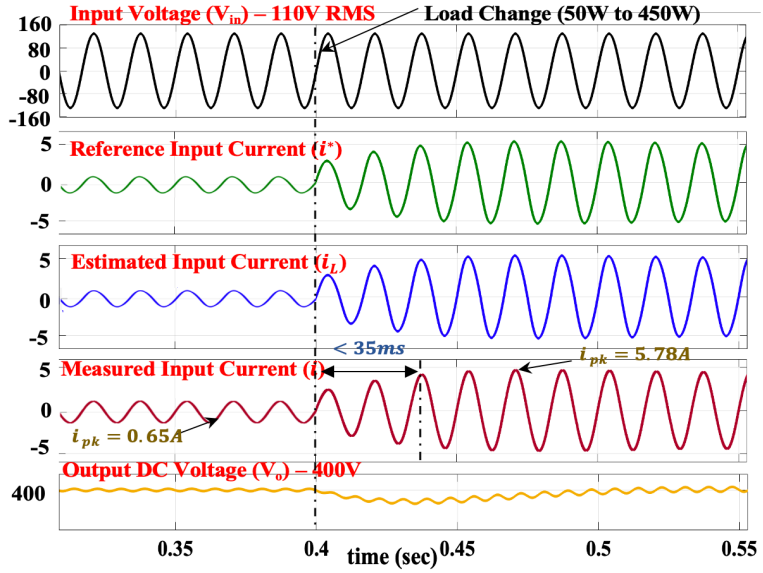


Figure 2.23: Dynamic Simulation Results of Input Voltage (V_{in}) with Reference Input Current (i_L^*), Estimated Input Current (i_L), Measured Input Current (i) and Corresponding Output Voltage (V_o) [Y-axis: V_{in} – 80V/div, i^*, i_L, i – 5A/div, V_o – 400V/div; X-axis: 50ms/div]

Experimental Analysis

To evaluate the performance of the proposed control scheme, a sensorless PFC proof-of-concept rated at 500W is developed as shown in Figure 2.10. The control algorithm is implemented using Texas Instruments (TI) TMS320F28335 DSP. The PWM triggered control is configured for 100kHz, which is the converter switching frequency. To ensure no signal aliasing effects, the sampling time (T_n) for the control loop (100kHz) is kept the same as the switching period i.e., 10µs, which is sufficient for accurate estimation of current with a line frequency of 60Hz. As observed from the experimental results in Figure 2.24, the system attains 400V constant DC voltage *(V_o)* at the output with <5% 120Hz ripple component. The phase current *(i)* tracks the input voltage *(V_{in}),* achieving a power factor of 0.998 and an efficiency of ~98.1%.

Further, to realize the dynamic performance of the proposed control scheme on the developed hardware, the load is stepped down from 450W to 50W, and then is stepped up back to 450W after a few cycles, thus elucidating a 10 to 90% load change. As observed in Figure 2.25, the settling time for the load transients is less than 6 AC-line cycles. Additionally, due to the robust design of the proposed control scheme, the DC link voltage regains its reference value after experiencing a 5% sag during the load change transient.

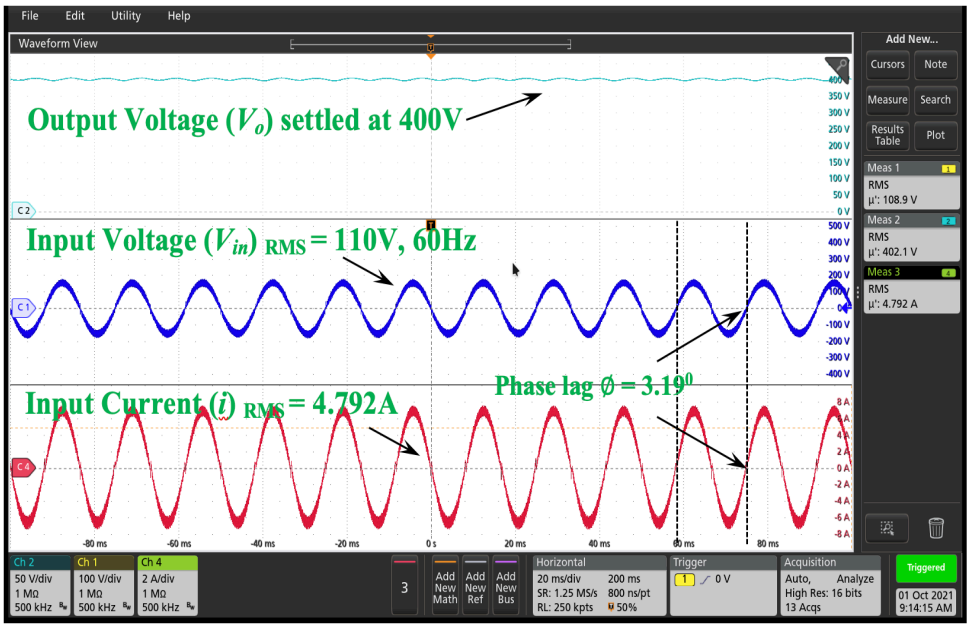


Figure 2.24: Static Load Experimental Results at 500W Load: Output Voltage (V_o), Input Voltage (V_{in}) and Input Current (i) [Y-axis: V_o – 50V/div, V_{in} – 100V/div, i – 2A/div; X-axis: Time – 20ms/div]

To account for the high frequency noise superimposed on the fundamental frequency component of input voltage, the following aspects of the system are reinforced. This also results in reduction in the resultant THD of the input current.

(a) Implementing a combined EMI filter at the input side:

To account for the EMI noise generated in the circuit and reflected at the input terminals of the PFC, a front-end single-stage EMI filter consisting of common mode (CM) and differential mode (DM) filtering stages is introduced between the AC grid and the converter where the boost PFC inductor acts as a DM inductive filter. The design considerations for this integrated EMI filter are explained in [139] for complying with FCC Class A/B conducted EMI standard [140]. The EMI filter implemented in the system is shown in Figure 2.26.

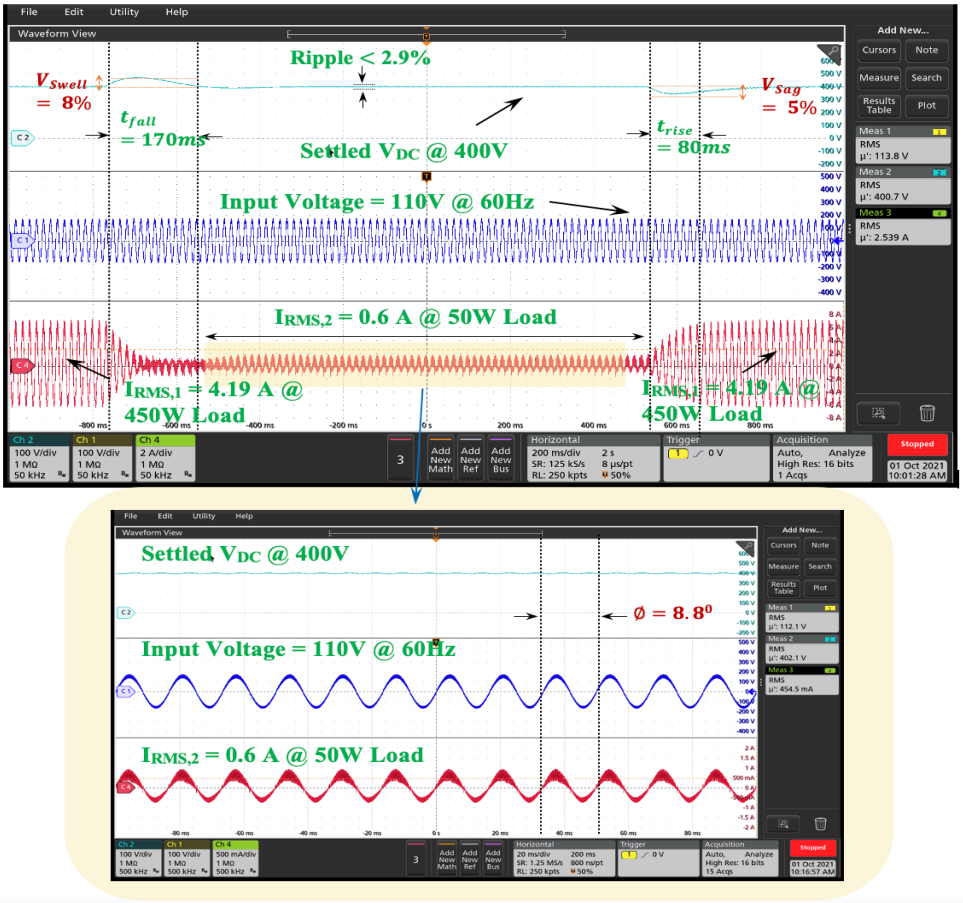


Figure 2.25: Dynamic Experimental Results at 450-50-450W Load Variation: Output Voltage (V_o), Input Voltage (V_{in}) and Input Current (i)) [Y-axis: V_o – 100V/div, V_{in} – 100V/div, i – 2A/div; X-axis: Time – 20ms/div]

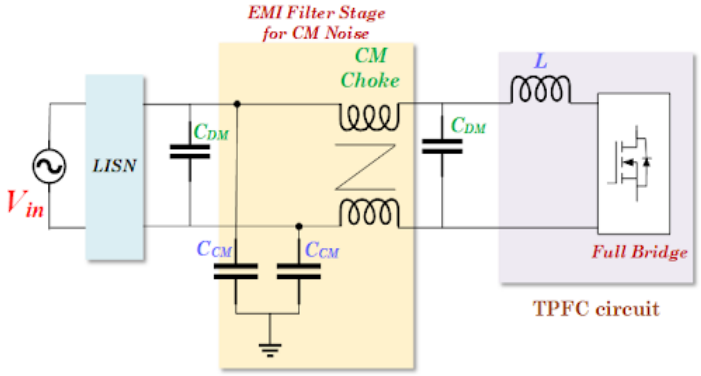


Figure 2.26: EMI Filter Schematic to Account for CM and DM Noise

(b) Introduction of a low pass filter at the output of the input voltage sensor buffer:

The microcontroller takes in the sensed value of input voltage (through ADC), and correspondingly generates the reference quantity for the input current, to be utilized for the inner current loop. However, since the input voltage consists of higher order frequency components, they likely propagate through the sensor to the microcontroller ADC and hence affect the reference current generation. Therefore, to ensure that the higher order frequency components are subdued, an additional filter capacitor (C_{FLT}) is used at the output of the input voltage sensor buffer, which is a high common voltage programmable gain difference amplifier (AD628 by Analog Devices for this application) [141]. This capacitor acts as a low pass filter in affiliation with the R_f resistor that is already present in the difference amplifier chip. For high-frequency attenuation, the filter capacitor is selected small enough to cause insignificant delay to the sensed grid-frequency voltage signal, so that the control loop design remains unaffected.

(c) Implementation of K-point moving average

In addition to the mentioned analog domain solutions to improve the input voltage quality, the K-point moving average based digital filtering scheme is implemented to account for any undesired noise from the output voltage sensing that might propagate to the ADC of the microcontroller unit.

Effect of parameter variation in experimental results

As observed in Table 2.5, the sensitivity indexes portray how the proposed control scheme proves to be resilient against changes in design parameters, rendering it to be parameter variation tolerant. To mimic a similar practical case, so as to observe the change

in the gain and power factor due to small change in the inductor's design specification, two scenarios are experimentally verified:

1. $(\{L, r_{inductor}\} = \{500\mu H, 30m\Omega\} \rightarrow \{L, r_{inductor}\} = \{600\mu H, 31.7m\Omega\}$

Using (2.52) and the sensitivity analysis mentioned in Table 2.5, the resultant power factor and gain at the updated values of design parameters can be calculated as:

$$\Delta PF = \frac{\partial PF}{\partial L}\Delta L + \frac{\partial PF}{\partial r}\Delta r = -2.226 * 10^{-7} \quad (2.61)$$

$$\Delta G = \frac{\partial G}{\partial L}\Delta L + \frac{\partial G}{\partial r}\Delta r = 3.801 * 10^{-7} \quad (2.62)$$

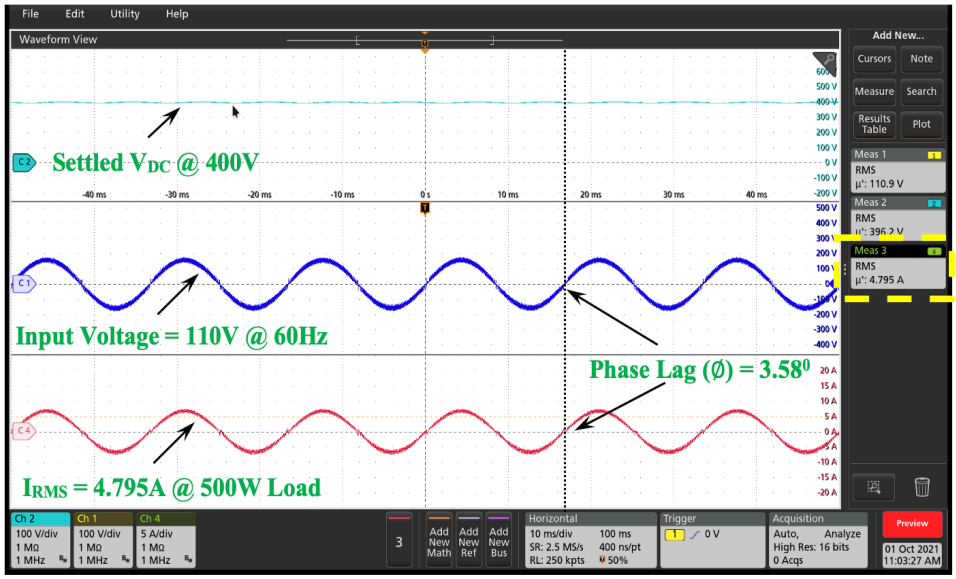


Figure 2.27: Static Load Experimental Results for $\{L, r_{inductor}\}$={600μH,31.7mΩ} : [Y-axis: V_o – 100V/div, V_{in} – 100V/div, i – 5A/div; X-axis: Time – 10ms/div]

As observed in Figure 2.27, as the values of L and $r_{inductor}$ are increased by 20% and 5.6% respectively, the steady state RMS value of the input current increases to 4.795A, indicating an increment of 3mA compared to the nominal case due to the increase in gain, that closely matches with the theoretical estimate. Additionally, the phase lag between the

input voltage and current, accounting for the power factor is increased to 3.580 with an increment of 0.390 compared to the nominal case.

2. $\{L, r_{inductor}\} = \{500\mu H, 30m\Omega\} \rightarrow \{L, r_{inductor}\} = \{450\mu H, 27.4m\Omega\}$

$$\Delta PF = \frac{\partial PF}{\partial L}\Delta L + \frac{\partial PF}{\partial r}\Delta r = 3.34 * 10^{-7} \quad (2.63)$$

$$\Delta G = \frac{\partial G}{\partial L}\Delta L + \frac{\partial G}{\partial r}\Delta r = -5.678 * 10^{-5} \quad (2.64)$$

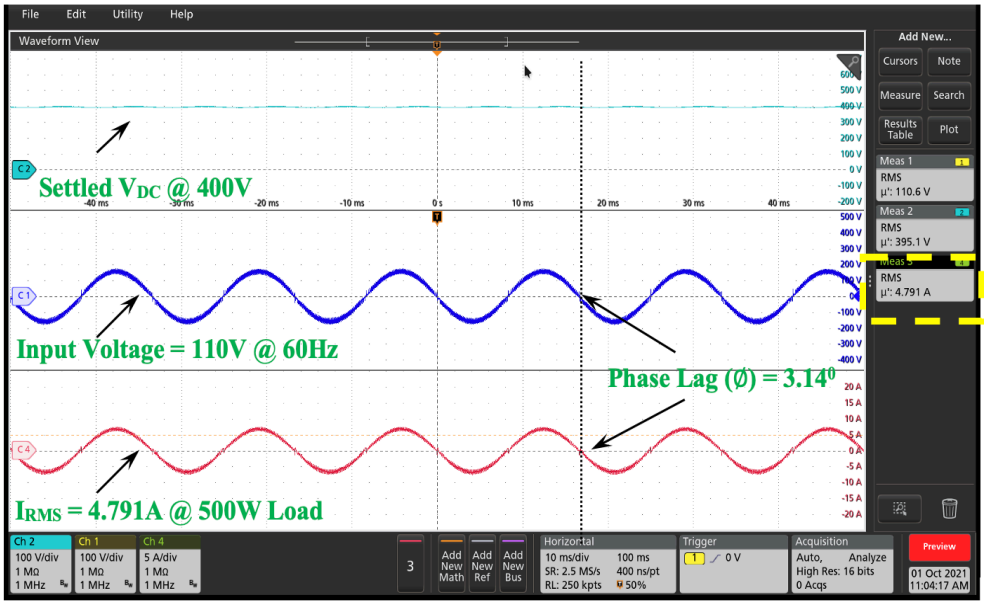


Figure 2.28: Static Load Experimental Results for $\{L, r_{inductor}\}$={450µH,27.4mΩ} : [Y-axis: V_o – 100V/div, V_{in} – 100V/div, i – 5A/div; X-axis: Time – 10ms/div]

Similarly, as observed in Figure 2.28, the values of L and $r_{inductor}$ are reduced by 10% and 8.6% respectively, and correspondingly the steady state RMS current value reduces to 4.791A, portraying a reduction of 1mA as compared to the nominal condition, resulting due to minor reduction in gain. Further, the phase lag between the input voltage and current reduces by 0.05^0, leading to a higher resultant power factor.

Table 2.7 shows the experimentally measured resultant power quality obtained at various loading conditions. As seen in the table, the THD at full load condition is 1.68%

and that at 10% load is 3.95%, proving the superiority of the proposed control scheme for all loading conditions. Additionally, Table 2.7 also mentions the achieved efficiency values for various loading conditions, achieving a peak efficiency of 98.1%.

Table 2.7: Power Quality Comparison at Various Loading Conditions

% of the rated load	THD (%)	Power Factor	Efficiency (%)
10%	3.95%	0.944	93.13%
25%	3.14%	0.961	95.78%
50%	2.43%	0.984	97.14%
75%	2.22%	0.992	97.33%
100%	1.68%	0.998	98.08%

A detailed loss distribution appearing in the circuit is also provided at rated load condition (as shown in Table 2.8) that diversifies the overall losses appearing in the circuit. Corresponding to that, Figure 2.29 shows the efficiency trend of developed circuit at various loads, highlighting the enhanced efficiency even at light load conditions. In addition to that, thermal images are captured using an infrared camera to highlight the hotspots appearing in the circuit at rated load condition with an ambient temperature of 22ºC. Figure 2.30 (a) and (b) describe the thermal image of the high frequency MOSFET (S_1) and synchronous MOSFET (S_3) respectively. As observed, the switches experience only 6ºC temperature rise at 500W steady operation, thus elucidating a thermally stable system. Additionally, Figure 2.30 (c) describes the thermal image of the entire system at rated load condition. The peak temperature of 72.5^oC occurs at the power supplies for the isolated gate drivers, which are rated to operate at 115^oC.

Table 2.8: Quantitative Loss Formulation at Rated Load

Loss category	Loss sub-category	Formulation	Resultant Losses
Semiconductor Losses	Switching Turn on losses	$P_{sw,on} = 2 * \frac{1}{2} V_{DS} I_D (t_{1,on} + t_{2,on}) f_{sw}$ Where, $t_{1,on} = R_g C_{in} \ln\left(\frac{V_{Dr} - V_{th}}{V_{Dr} - V_{pl}}\right)$ $t_{2,on} = \frac{C_{gd}(V_{DS} - I_D R_{on}) R_g}{V_{Dr} - V_{pl}}$	$P_{sw} = P_{sw,on} + P_{sw,off} = 5.4W$
	Switching Turn off losses	$P_{sw,off} = 2 * \frac{1}{2} V_{DS} I_D (t_{1,off} + t_{2,off}) f_{sw}$ Where, $t_{1,on} = R_g C_{in} \ln\left(\frac{V_{pl}}{V_{th}}\right)$ $t_{2,on} = \frac{C_{gd}(V_{DS} - I_D R_{on}) R_g}{V_{pl}}$	
	Conduction Losses	$P_{cond} = 2 * I_{RMS}^2 R_{ds,on}$	$P_{cond} = 1.05W$
	Gate Driving Losses	$P_{drive} = \frac{1}{2} C_{gs} V_{gs}^2 f_{sw}$	$P_{drive} = 0.18W$
Passive Component Losses	Capacitor ESR Losses	$P_{C,ESR} = I_{o,ripple\ (RMS)}^2 R_{C,ESR}$	$P_{C,ESR} = 0.24W$
Magnetics	Inductor Core Losses	$P_{core} = \frac{1}{T} \int_0^T k_i \left\lvert \frac{dB}{dt} \right\rvert^{\alpha} (\Delta B)^{\beta - \alpha} dt$ Where, $k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} \lvert \cos\theta \rvert^{\alpha} 2^{\beta-\alpha} d\theta}$	$P_{core} = 1.15W$
	Inductor Winding Losses	$P_{winding} = I_{RMS}^2 r_{inductor}$	$P_{winding} = 1.48W$

V_{Dr} = Driving gate voltage
V_{th} = Threshold voltage
V_{pl} = Gate plateau voltage
R_g = External gate resistance
C_{gd}= Gate to drain inherent capacitance
C_{in} = Input capacitance of the switch
C_{gs}= Gate to source capacitance
$R_{C,ESR}$ = ESR of the output capacitor
k, α, β = Steinmetz equation parameters
ΔB = peak to peak flux density
I_D = Drain current
V_{DS} = Drain to source voltage
$t_{1,on}$ = Time required for I_D to reach its rated value
$t_{2,on}$ = Time required for V_{DS} to drop down to zero
$t_{1,on}$ = Time required for V_{DS} to reach its rated value
$t_{2,on}$ = Time required for I_D to drop down to zero

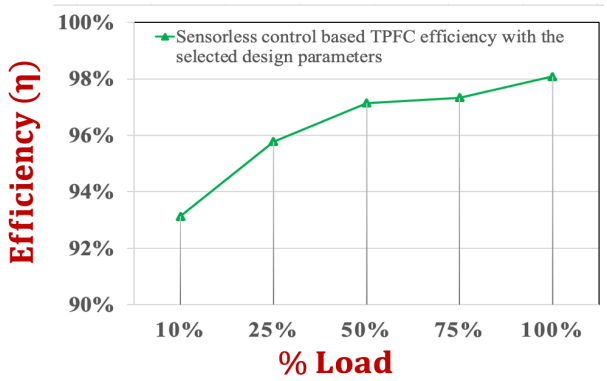


Figure 2.29: Efficiency Characteristics at Various Loading Conditions

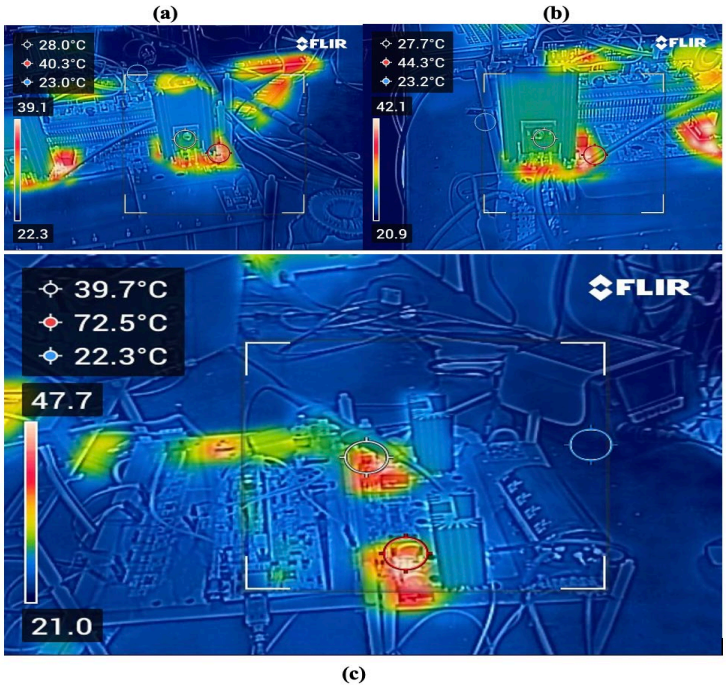


Figure 2.30: Thermal Image of the Experimental Set Up at Rated Load

2.5.7. Comparison with the State-of-the-art Methods

Most of the SOA methods for sensorless current control have used state estimation & observer models [46], Kalman filter [48] and voltage ripple based complex control approaches [51-52], which are of high-degree algorithmic complexity due to time-

expensive formulations of matrix inversions and trigonometric conversions, thus increasing the overall execution time of the control loop. In addition to that, issues related to degraded power quality at light load and poor dynamic performance for a major load change, most of these approaches have not achieved commercial acceptance. On the other hand, the proposed sensorless control scheme utilizes the switch-averaged model of the inductor voltage with basic mathematical formulations and a delay block (generally implemented using multi-variable array) to estimate the inductor current, thus proving it to be beneficial in terms of ease of implementation.

As seen in Figure 2.31, the execution time of the proposed control scheme is observed in TI TMS320F28335 MCU (by toggling a GPIO at the end of the control loop) and is compared with a SOA approach [52], which performs the power conversion at 40kHz switching frequency. As observed, the execution time for the proposed control scheme is reduced by 1.8 μs, which stresses on the fact that the proposed control scheme can be used for a system with significantly higher switching frequency (up to 300kHz), thus reducing the size of magnetics drastically, while SOA methods [51-52] are limited up to 170kHz switching operation.

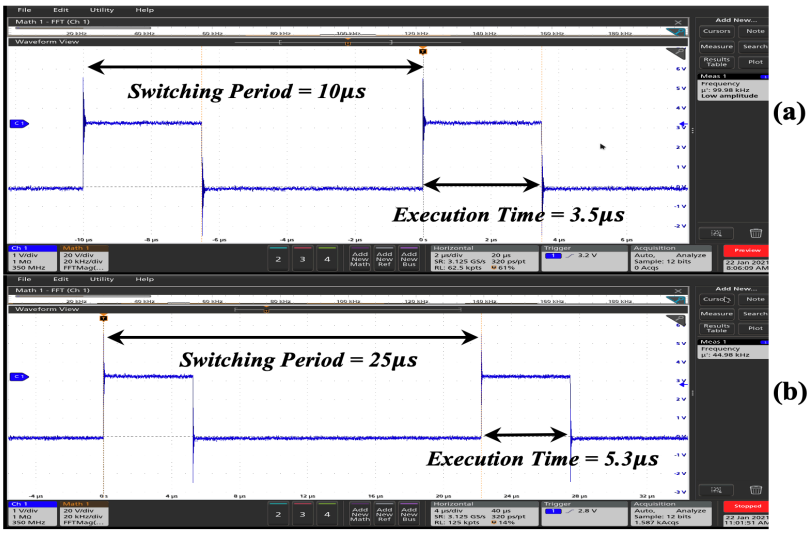


Figure 2.31: Control Loop Execution Times for (a) The Proposed Control Scheme @ fs=100kHz (b) SOA Approach@ fs=40kHz

As seen in (2.37), since the system is defined in discrete domain, it important to comprehend the effect of the system execution time and corresponding signal propagation delay on the estimation of input current. In addition, the overall propagation delay between the PWM generation port of the microcontroller unit (MCU) and the MOSFET gate terminal is not only dependent on the delay pertaining to the program execution time, but also due to the stray inductances and delay introduced by the gate driver circuitry. As observed in Figure 2.31(a), the execution time for the microcontroller unit in duty ratio generation and current estimation is approximately 3.5μs, which is lesser than the sampling period or the switching period ($T_n = T_S = 10\mu s$). Thus, the resultant power factor stays unaffected on account of the execution time of the microcontroller program. This concept is further described in Figure 2.32, which compares a generic current controller loop structure to the proposed scheme. As observed, the conventional control includes sensor delay in the feedback path that potentially affects the stability margin of the closed loop

control, while the proposed sensorless control scheme is executed in the MCU that updates the duty ratios in every switching/sampling period, hence introducing no feedback path delay. In addition to that, in order to characterize the delay introduced due to the driver circuit, an experimental result comparing the rise and fall time of the 3.3V PWM logic generated at the MCU PWM port and the 15V logic appearing at the gate terminal of the MOSFET is shown in Figure 2.33.

As observed in Figure 2.33, the delay pertaining to the gate driver circuit is approximately 256ns, i.e., ~2.5% of the switching time period, which, being consistent for all the four switches of the PFC topology, does not result in any asynchronous delay in the switching actions and does not cause any deviation in the resultant power factor. Also, please note that the gate driver path propagation delay is inevitably present in the conventional control schemes too. Further, the dead time for both the half-bridges in the circuit is selected to be 30ns, which renders it inconsequential to the obtained power factor.

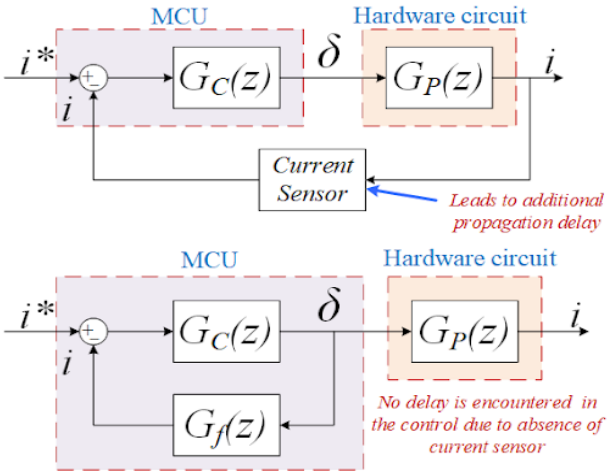


Figure 2.32: Comparison Between the Conventional Sensor-Based Control and Sensorless Control to Highlight the Propagation Delay

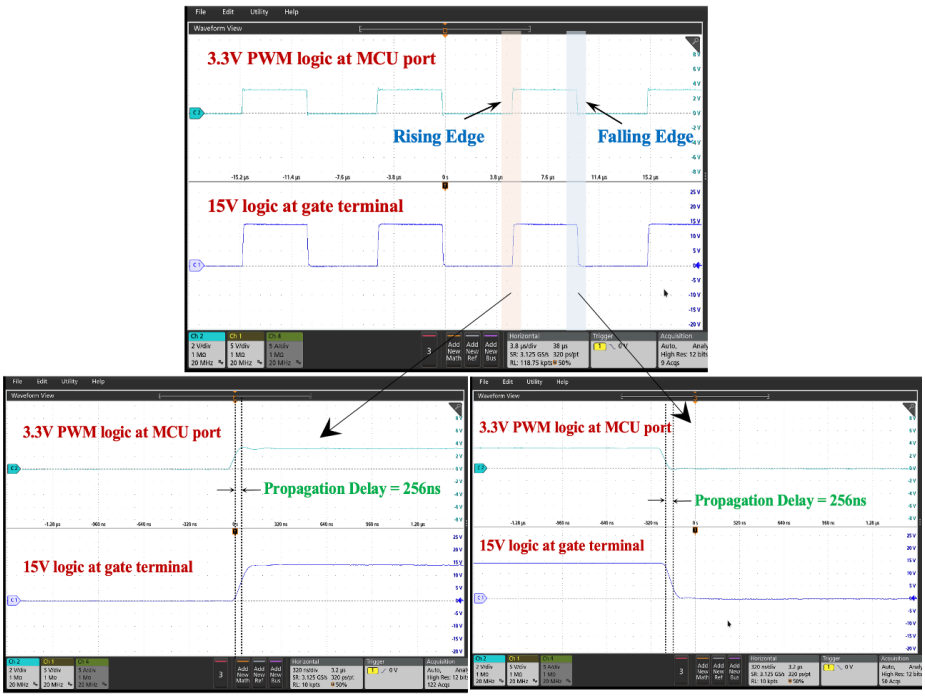


Figure 2.33: Experimental Results to Verify the Propagation Delay Between the Digital Logic Board and the Gate Terminal of the Switch

2.6. Chapter Summary

In this chapter, an accurate and detailed mathematical model is proposed for calculating the magnitudes and phases of the harmonic components appearing in input current of a TPFC topology. To validate the proposed model, a comprehensive correlation between the analyzed formulations and simulation/experimental results for various voltage and load power levels is presented that yields an accuracy of 97%. Further, to effectively mitigate the third harmonic component, a novel digital filter based AMS is proposed. To elucidate the effectiveness of the proposed AMS, detailed simulation and experimental results are presented in this work. The results portray 46% reduction in the third harmonic component magnitude, thus resulting in 17% improvement in the resultant THD at the

PCC. As a proof-of-concept verification to the proposed model, an 500W laboratory prototype TPFC is developed and tested for universal single phase input (85-265Vac) with a 400V DC stiff output. Meticulous results at various loading conditions with their resultant THDs and power factors are also included, that portray the significance of implementing the AMS, even at light load conditions. Additionally, due to its generic design approach, the AMS can also be extended for various other order of harmonics as per the requirement.

Further, a novel, easy-to-implement and reliable discrete sampling based current sensorless control for a totem-pole PFC is introduced and analyzed. As observed from the stability analysis and corresponding bode plot, the proposed control scheme provides a superior dynamic performance when subjected to sudden load changes. Further, to ensure accurate tracking of the phase current, with respect to gain and phase of the proposed control scheme, against the inherent uncertainty of the system parameters, a detailed sensitivity analysis is also presented. The results portray the robustness and tolerance of the control scheme against any variation of L and r_L, caused due to various detrimental effects on a typical power converter. To ensure immunity against any EMI noise that might appear in the sensed data, a 'K' point averaging is also proposed, and the results prove that as K increases, the effect of any unwanted noise is suppressed, resulting in a stable and robust performance. To verify the performance the proposed control scheme, detailed simulation studies are presented. The results show enhanced power quality with a resultant power factor of 0.998 (lag), at the rated load, with significantly improved quality metrics at light load as well. A 500W prototype is also built to illustrate the effectiveness of the proposed control technique, that yields a power factor of 0.998 (lag), with a resultant

efficiency of 98.1% and a THD of 1.68% at rated load. In addition to that, the results for a dynamic change in load also match the simulation results, yielding a settling time of less than 32ms. The proposed control scheme outperforms the SOA approaches with a lower execution time and hence higher switching frequencies (upto 300kHz). Due to its simplicity in terms of formulation and ease of implementation, the proposed control scheme can be utilized for any variant of PFC circuit, targeted to improve the input power quality of any power electronic converter, specifically used for EV applications.

CHAPTER 3

OPTIMAL DESIGN, CONTROL AND PARASITIC COMPONENT SYNTHESIS OF A BIDIRECTIONAL CLLC RESONANT DC/DC CONVERTER

3.1. Introduction

This chapter holistically covers the technical aspects to ensure optimal design, performance and parasitic synthesis of a bidirectional CLLC resonant converter. First, to ensure optimal tank selection with careful considerations of the parasitic components and their effect on the overall system performance, this chapter provides a detailed analytical formulation and validation of the R-L-C parameters of a HFPT. In that context, a practical and realistic characterization of the leakage inductance, winding resistance, and stray capacitance of a HPFT accounting for various intricate fabrication-based considerations and their effect on the system performance is elucidated in this chapter. Comprehensive graphically elucidated parametric trade-offs and guidelines related to conductor and insulator parameters employed for HPFT realization are explained that provide insightful design constraints, thus ensuring optimal selection of winding structures. In addition to that, a thorough comparison of the analytically derived model, with 3D FEA based simulations and experimental analysis is presented that validates the presented analysis.

Further, addressing the limitations pertaining to the state-of-the-art methods of enabling SR at the secondary side bridge to enhance the efficiency, the key contributions for enabling a novel modeling technique and turn-off current minimization approach are shown as follows: (a) Intricately curated all-inclusive GHA based modeling of CLLC

converter with asymmetric tank accounting for stray parameters and their effect on the resultant gain trend, highlighting the experimental accuracy of the presented analysis, (b) A non-approximated frequency domain model-derived formulation of required phase shift enabling SR, accounting for the stray parameters and corresponding minimization of turnoff current based on multi-dimensional optimization approach.

In addition to ensuring efficient steady state power flow, for ensuring superior dynamic performance a detailed GHA based small-signal modeling technique of the CLLC converter with intricate considerations of the parasitic components in the obtained small signal model is presented. Further, a comprehensive comparison of the plant frequency response elucidating the importance of inclusion of parasitics in the analysis and its relevance for a robust controller design ensuring superior immunity against EMI noise is explained. Further, thorough modeling and design of a novel SMC based hybrid control scheme in association with efficiency enhancement objective obtained through secondary side turn-off current minimization is presented with detailed experimental validation elucidating the effectiveness of the proposed hybrid controller over a conventional PI based controller.

The technical aspects included in this chapter are derived from the studies discussed in [142-145].

3.2. Frequency Domain GHA Based Equivalent Circuit Synthesis and Modeling for Asymmetric CLLC

Figure 3.1 shows the bidirectional CLLC DC/DC converter topology operating at a resonant frequency $f_r = \frac{1}{2\pi\sqrt{L_p C_p}} = \frac{1}{2\pi\sqrt{L_s C_s}}$, where C_p and C_s denote the resonant capacitors for the primary and secondary side, respectively and L_p and L_s denote the resonant inductors obtained as integrated leakages from the HFPT designed with a turns ratio of n: 1 and magnetizing inductance L_m. Please note the tank is considered asymmetric (i.e., $L_p \neq n^2 L_s, C_p \neq n^2 C_s$) to bring in more design flexibility in terms of supporting wider gain range. Further, to provide intricately curated realistic model highlighting the stray components, a comprehensive HFPT circuit representation is highlighted in Figure 3.1 and thoroughly explained in Section 3.4. As observed, R_p and R_s signify the effective winding resistances of the HFPT employed. Further, $C_{p_{in}}$ and $C_{s_{in}}$ denote the intra-winding capacitances of the primary and secondary windings of HFPT, while $C_{ps_{in}}$ signifies the inter-winding capacitance between the two windings.

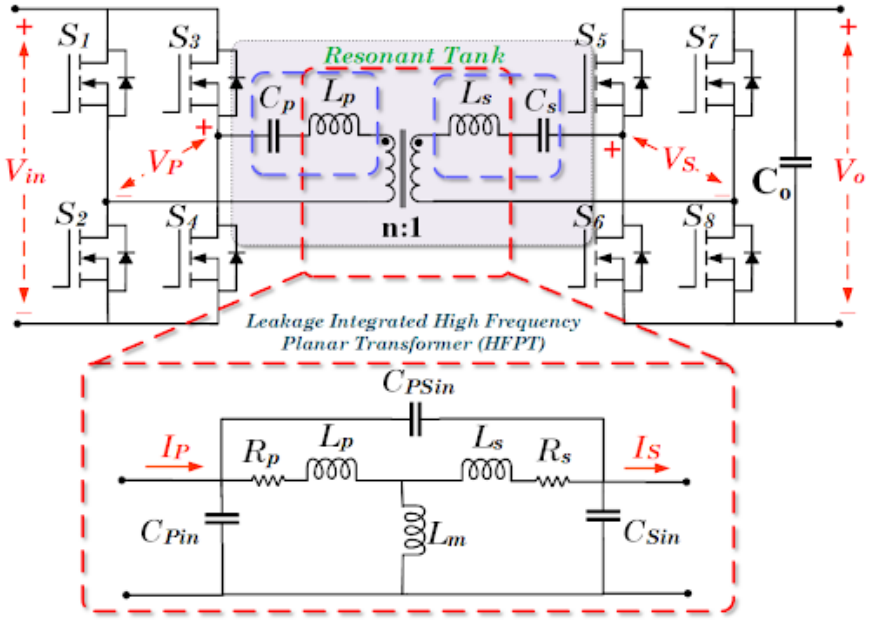


Figure 3.1: CLLC Topology with Zoomed in Comprehensive HFPT Circuit Model

To account for the influence of the above-mentioned stray components on the system performance, the equivalent tank structure shown in Figure 3.1 is remodeled using a series of star (Y)-delta (Δ) conversions to obtain the effective impedance parameters in equivalent Y and Δ models, as shown in Figure 3.2.

$$Z_p = R_p + j\omega L_p; Z_s = n^2[R_s + j\omega L_s]; Z_m = j\omega L_m \tag{3.1}$$

$$\left.\begin{aligned} Z_{pp} &= Z_p + Z_m + \frac{Z_p Z_m}{Z_s} \\ Z_{ps} &= Z_p + Z_s + \frac{Z_p Z_s}{Z_m} \\ Z_{ss} &= Z_s + Z_m + \frac{Z_s Z_m}{Z_p} \end{aligned}\right\} \tag{3.2}$$

$$\left.\begin{aligned} Z_{p,Y} &= X_{C_{p,in}} || Z_{pp} \\ Z_{ps,Y} &= X_{C_{ps,in}} || Z_{ps} \\ Z_{s,Y} &= X_{C_{s,in}} || Z_{ss} \end{aligned}\right\} \tag{3.3}$$

$$\left.\begin{aligned} Z_{\Delta,p} &= \frac{Z_{p,Y} Z_{ps,Y}}{Z_{p,Y} + Z_{ps,Y} + Z_{s,Y}} \\ Z_{\Delta,s} &= \frac{Z_{s,Y} Z_{ps,Y}}{Z_{p,Y} + Z_{ps,Y} + Z_{s,Y}} \end{aligned}\right\} \tag{3.4}$$

$$\left.\begin{aligned} Z_{eff,m} &= \frac{Z_{p,Y}Z_{s,Y}}{Z_{p,Y}+Z_{ps,Y}+Z_{s,Y}} \\ Z_{eff,p} &= Z_{\Delta,p} + X_{C_p} \\ Z_{eff,s} &= Z_{\Delta,s} + X_{C_s} \end{aligned}\right\} \tag{3.5}$$

$$\left.\begin{aligned} Z_{f,pp} &= Z_{eff,p} + Z_{eff,m} + \frac{Z_{eff,p}Z_{eff,m}}{Z_{eff,s}} \\ Z_{f,ps} &= Z_{eff,p} + Z_{eff,s} + \frac{Z_{eff,p}Z_{eff,s}}{Z_{eff,m}} \\ Z_{f,ss} &= Z_{eff,s} + Z_{eff,m} + \frac{Z_{eff,s}Z_{eff,m}}{Z_{eff,p}} \end{aligned}\right\} \tag{3.6}$$

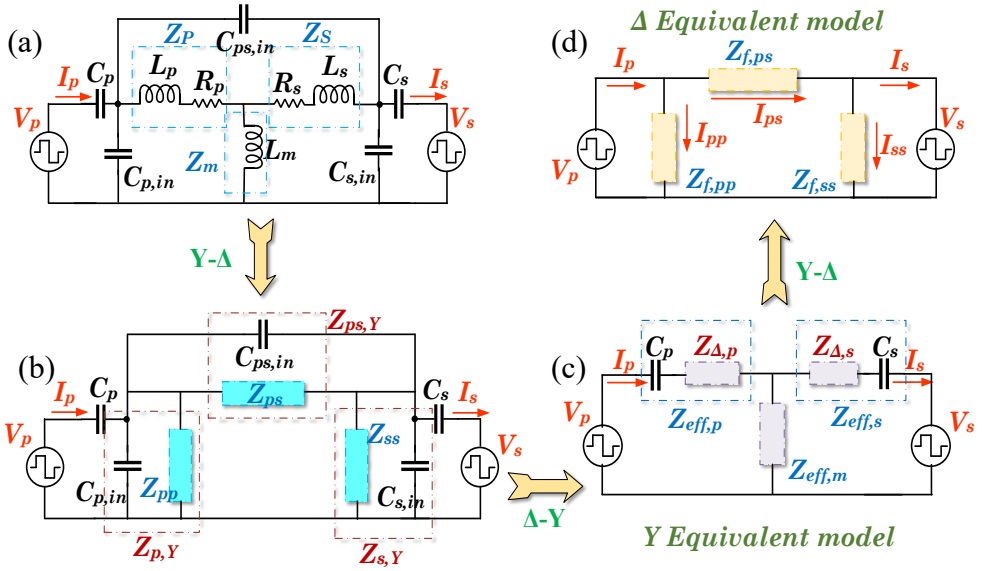


Figure 3.2: Reconfiguration of CLLC Equivalent Circuit Accounting for Stray Components

To formulate an all-inclusive GHA based gain equation, a detailed multi-harmonic AC equivalent impedance model based on the equivalent tank model is shown in Figure 3.3. The resonant tank is excited by a square-wave voltage of magnitude corresponding to the DC input that can be decomposed into a series of multiple sinusoidal voltage sources that essentially accounts for the fundamental and higher order harmonics. Considering G2V operation, with a constant input voltage source V_{in}, the reactive power flow in the

system can be considered zero and thus, the secondary side can be modelled as a load with equivalent resistance $R_{o,GHA}$ [80].

$$R_{o,GHA} = \frac{8n^2 R_o}{\pi^2} \sum_{k=1,3,5,\ldots}^{2n+1} \frac{1}{k^2} \tag{3.7}$$

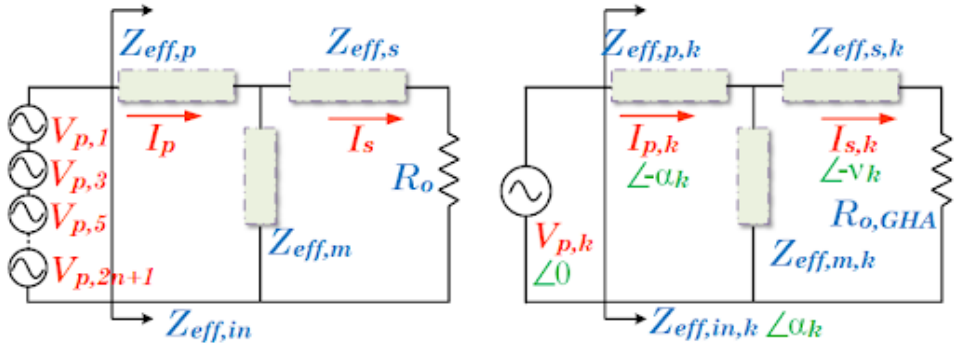


Figure 3.3: GHA Equivalent Model for CLLC Converter for Forward Power Flow

As observed in Figure 3.3, GHA enables the designer to analyze the effect of each harmonic component on the resultant gain by individually formulating the system equations for each component and superposing them to synthesize the equivalent gain. In that context, the input voltage ($V_p(t)$) and corresponding input current ($I_p(t)$) to the resonant tank can be written as summation of 'k' harmonic components as shown below:

$$V_p(t) = \sum_{k=1,3,5\ldots}^{2n+1} V_{p,k} \frac{\sin(k\omega_s t)}{k} = \frac{4V_{in}}{\pi} \sum_{k=1,3,5\ldots}^{2n+1} \frac{\sin(k\omega_s t)}{k} \tag{3.8}$$

$$I_p(t) = \sum_{k=1,3,5\ldots}^{2n+1} V_{p,k} \frac{\sin(k\omega_s t - \alpha_k)}{k} \frac{1}{|Z_{eff,in,k}|} \tag{3.9}$$

where, $Z_{eff,in,k} = Z_{eff,p,k} + Z_{eff,m,k} || (Z_{eff,s,k} + R_{o,GHA})$ denotes the input impedances and $\alpha_k = \angle Z_{eff,in,k}$.

Referring to (3.8-3.9), the cumulative power input accounting for the series connected voltage sources signifying summation of k harmonic components can be written as:

$$P_{in} = \frac{1}{2}\sum_{k=1,3,5\ldots}^{2n+1} V_{p,k}\, I_{p,k} \cos(\alpha_k) \tag{3.10}$$

Further, substituting (8-9) in (10), the input power is formulated as shown below:

$$P_{in} = \frac{1}{2}\sum_{k=1,3,5\ldots}^{2n+1} \frac{V_{p,k}^2}{|Z_{eff,in,k}|} \cos(\alpha_k) \tag{3.11}$$

$$= \frac{8V_{in}^2}{\pi^2}\sum_{k=1,3,5,\ldots}^{2n+1} \frac{1}{k^2}\frac{1}{|Z_{eff,in,k}|} \cos(\alpha_k) \tag{3.12}$$

The GHA based gain ($|G|\angle\varphi_g$) accounting for all the stray components is derived by equating (3.10) to $\frac{V_o^2}{R}$, invoking the power balance condition as shown below:

$$|G| = \frac{nV_o}{V_{in}} = \frac{2\sqrt{2}}{\pi} n \sqrt{R_o \sum_{k=1,3,5,\ldots}^{2n+1} \frac{1}{k^2}\frac{1}{|Z_{eff,in,k}|} \cos(\alpha_k)} \tag{3.13}$$

Figure 3.4 elucidates the gain versus frequency curves for first harmonic approximation (FHA), GHA [80], and the proposed gain model as shown in (3.13) with the experimentally obtained gain modulation trend for the design specifications mentioned in Table 3.9. As observed, due to intricately curated gain characteristics accounting for all the stray components in the asymmetric CLLC under study, the presented gain model follows the experimentally obtained gain model with an average mismatch of 0.44%, thus validating the exactitude of presented analysis.

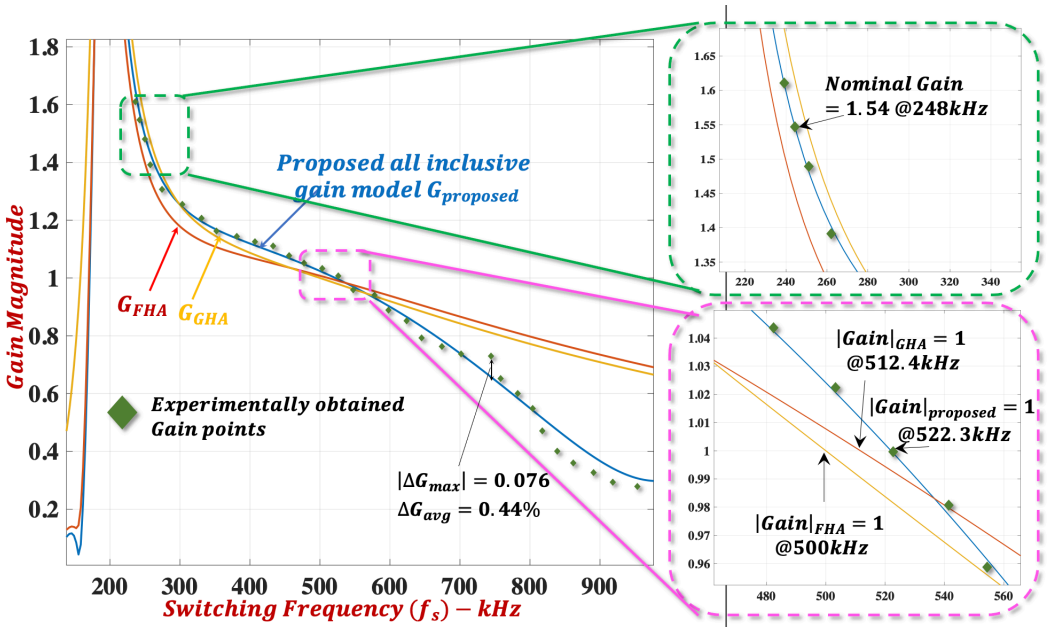


Figure 3.4: Gain Comparison of FHA, GHA, and Presented Gain Model, with Experimentally Obtained Gain Versus Frequency Trend.

Further, to prove the accuracy of the proposed all-inclusive gain model, zoomed in snapshots of two instances of the gain plot comparison are presented in Figure 3.4. As observed, implementing FHA based modeling, the unity gain point appears at operational switching frequency equal to the resonant frequency (500kHz). However, when verified experimentally, the unity gain point shifts to 522.3kHz, which matches the response portrayed by the proposed all-inclusive gain model. This occurs to due to the effect of parasitic components and higher order harmonics present in the system, which is encompassed by the proposed all-inclusive GHA based gain model. In addition to that, the nominal gain point ($|G|$=1.54) occurs at 248kHz switching frequency, which also coincides with the plot elucidated by the proposed gain model. The above two instances indicate that the inclusion of parasitic components in the gain modeling plays a crucial role to obtain accurate output voltage regulation.

3.3. Optimum Phase-Frequency Contour-Enabled SR Based Turnoff Current Minimization

With an objective to reduce the on-state conduction losses in conventional diode based secondary side bridge, the use of active switches operating with phase shift (ϑ) with respect to the primary side gate pulses facilitates accurate phase tracking with the switch voltage, resulting in reduced turn-off losses. Further, precise estimation of the mentioned phase shift is quintessential for enabling SR; the failure to do so results in significant turnoff losses which is directly proportional to the extent of error in phase tracking (ϑ_e). Figure 3.5 elaborates on this phenomenon by elucidating the turnoff losses due to inaccurate phase tracking for two cases: (i) $f_s < f_r$ and (ii) $f_s > f_r$ and compares it with an accurately estimated SR operation.

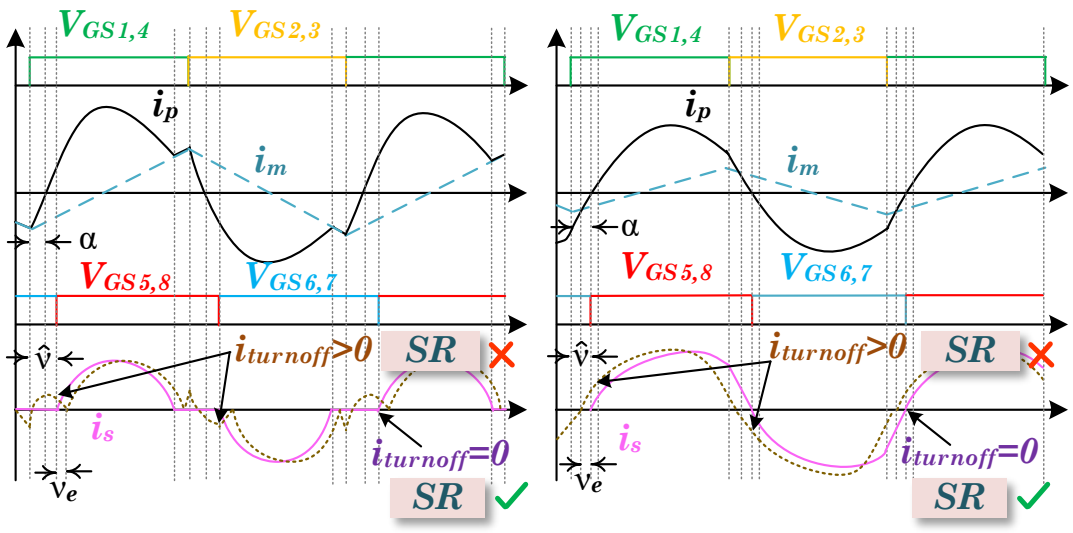


Figure 3.5: Waveform Comparison for (i) f_s<f_r and (ii) f_s>f_r.

As observed, due to inaccurate phase shift provided to switch S_5, the current at turnoff instant is not zero, leading to additional switching losses as seen in (3.14-3.15).

$$i_{turnoff} = |I_s| \sin \vartheta_\varepsilon \tag{3.14}$$

$$P_{turnoff} = 2 \cdot \frac{1}{2} V_o i_{turnoff} f_s t_{off} = V_o |I_s| f_s t_{off} \sin \vartheta_\varepsilon \tag{3.15}$$

In order to synthesize the required phase shift ($\hat{\vartheta}$) to alleviate the turnoff losses through SR, a detailed analysis elaborating on the system equations incorporating the effect of stray parameters is presented in this section. Referring to the Δ equivalent model as shown in Figure 3.2 (d), the secondary voltage can also be synthesized as a combination of 'k' voltage sources, each corresponding to the harmonic content of the quasi-square waveshape, as shown below:

$$V_s(t) = \sum_{k=1,3,5\ldots}^{2n+1} V_{s,k} \frac{\sin k(\omega_s t - \varphi_g)}{k} = \frac{4nV_o}{\pi} \sum_{k=1,3,5\ldots}^{2n+1} \frac{\sin k(\omega_s t - \varphi_g)}{k} \tag{3.16}$$

Utilizing (3.8) and (3.16), the current equations in the system can be formulated as follows:

$$i_{pp}(t) = \frac{4V_{in}}{\pi} \sum_{k=1,3,5\ldots}^{2n+1} \frac{\sin(k\omega_s t - \angle Z_{f,pp,k})}{k} \frac{1}{|Z_{f,pp,k}|} \tag{3.17}$$

$$i_{ss}(t) = \frac{4nV_o}{\pi} \sum_{k=1,3,5\ldots}^{2n+1} \frac{\sin(k(\omega_s t - \varphi_g) - \angle Z_{f,ss,k})}{k} \frac{1}{|Z_{f,ss,k}|} \tag{3.18}$$

$$i_{ps}(t) = \frac{4V_{in}}{\pi} \sum_{k=1,3,5\ldots}^{2n+1} \frac{\sin(k\omega_s t - \angle Z_{f,ps,k})}{k} \frac{1}{|Z_{f,ps,k}|} - \frac{4nV_o}{\pi} \sum_{k=1,3,5\ldots}^{2n+1} \frac{\sin(k(\omega_s t - \varphi_g) - \angle Z_{f,ps,k})}{k} \frac{1}{|Z_{f,ps,k}|} \tag{3.19}$$

Referring to Figure 3.2 (c), the secondary bridge current $i_s(t)$ can be synthesized (as shown in (3.21)) as a sinusoidal waveform having a zero crossing at $\omega_s t = \vartheta$, where ϑ accounts for the effect of additional phase shift required.

$$i_s(t) = i_{ps}(t) - i_{ss}(t) \tag{3.20}$$

$$i_s(t) = \frac{4V_o}{\pi} \sum_{k=1,3,5\ldots}^{2n+1} (A_k - B_k) \sin(k\omega_s t - \vartheta_k) \tag{3.21}$$

where, $\vartheta_k = \delta_k - \angle Z_{f,ps,k}$, $\delta_k = \tan^{-1}\frac{G\cos\beta}{1-G\sin\beta}$, $\beta_k = \frac{\pi}{2} - k\varphi_g$, $A_k = \frac{\sqrt{1+G^2-2G\sin\beta_k}}{k|Z_{f,ps,k}|}$ and $B_k = \frac{1}{k|Z_{f,ss,k}|}$.

Figure 3.6 portrays a phasor diagram elucidating the above-mentioned phase relationships between the port voltages and current for *'k^{th}'* harmonic component.

Figure 3.6: Phasor Diagram Explaining the Phase Relationship for k^{th} Harmonic Component

To obtain the required phase shift between the primary and secondary side gate pulses, the zero crossing of (3.21) is analyzed by numerically solving the equation by substituting the values of $\{\omega_s, \vartheta\}$ in an iterative loop. For a defined nominal voltage gain, the solution of $i_{turnoff} \rightarrow \boldsymbol{F}(i_s) = 0$ results in a contour of feasible solutions of $\{\omega_s^*, \vartheta^*\}$ corresponding to the rated load, all resulting in near-zero turnoff current. To elucidate this phenomenon, Figure 3.7 shows the set of possible combinations of $\{f_s^* = \frac{\omega_s^*}{2\pi}, \vartheta^*\}$ plotted for different load powers.

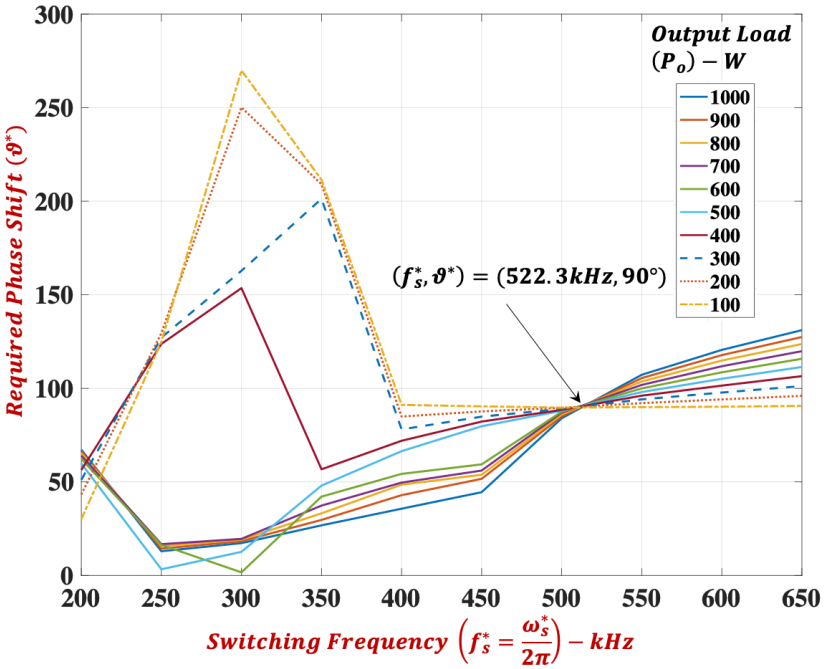


Figure 3.7: Plot of f_s^* Versus ϑ^* for Different Loading Conditions

However, to obtain the most optimum operating point resulting in minimum value of $i_{turnoff}$, an iterative multi-dimensional Newton method [146] using minimization approach with a residual error margin (ϵ) of 0.1%, as shown below:

$$\min i_{turnoff} \rightarrow \underset{\{\widehat{\omega_s}, \hat{\vartheta}\}}{solve} \boldsymbol{F}(i_s\{\boldsymbol{X}\}) = 0 \tag{3.22}$$

where, $\boldsymbol{X}$ denotes a matrix of all the feasible values of $\{\omega_s^*, \vartheta^*\}$ and $\boldsymbol{F}$ is the set of non-linear function depicting the values of i_s corresponding each possible value of $\{\omega_s^*, \vartheta^*\}$ as shown below:

$$X = \begin{bmatrix} \{\omega_{s,1}^*, \vartheta_1^*\} \\ \{\omega_{s,2}^*, \vartheta_2^*\} \\ \vdots \\ \{\omega_{s,n}^*, \vartheta_n^*\} \end{bmatrix}; \boldsymbol{F}(i_s\{\boldsymbol{X}\}) = \begin{bmatrix} i_{s,1}\{\omega_{s,1}^*, \vartheta_1^*\} \\ i_{s,2}\{\omega_{s,2}^*, \vartheta_2^*\} \\ \vdots \\ i_{s,n}\{\omega_{s,n}^*, \vartheta_n^*\} \end{bmatrix} \tag{3.323}$$

Iteratively solving (3.22) for u iterations, the $(u+1)^{th}$ solution set is formulated as shown below:

$$\boldsymbol{X}^{(u+1)} = \boldsymbol{X}^{(u)} - \boldsymbol{J}^{-1}(\boldsymbol{X}^{(u)}\boldsymbol{F}\left(i_s\{\boldsymbol{X}^{(u)}\}\right) \tag{3.24}$$

$$\boldsymbol{J}\left(\boldsymbol{X}^{(u)}\right)\epsilon\{\boldsymbol{F}\left(i_s\{\boldsymbol{X}\}^{(u)}\right)\} = -\boldsymbol{F}\left(i_s\{\boldsymbol{X}^{(u)}\}\right) \tag{3.25}$$

$$\text{where, } \boldsymbol{J}\left(\boldsymbol{X}^{(u)}\right) = \begin{bmatrix} \frac{\partial \boldsymbol{F}(i_{s,1})}{\partial \boldsymbol{X_1}} & \frac{\partial \boldsymbol{F}(i_{s,1})}{\partial \boldsymbol{X_2}} & \cdots & \frac{\partial \boldsymbol{F}(i_{s,1})}{\partial \boldsymbol{X_n}} \\ \frac{\partial \boldsymbol{F}(i_{s,2})}{\partial \boldsymbol{X_1}} & \frac{\partial \boldsymbol{F}(i_{s,2})}{\partial \boldsymbol{X_2}} & \cdots & \frac{\partial \boldsymbol{F}(i_{s,2})}{\partial \boldsymbol{X_n}} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial \boldsymbol{F}(i_{s,n})}{\partial \boldsymbol{X_1}} & \frac{\partial \boldsymbol{F}(i_{s,n})}{\partial \boldsymbol{X_2}} & \cdots & \frac{\partial \boldsymbol{F}(i_{s,n})}{\partial \boldsymbol{X_n}} \end{bmatrix} \tag{3.26}$$

$$\epsilon\{\boldsymbol{F}\left(i_s\{\boldsymbol{X}\}^{(u)}\right)\} = \boldsymbol{F}(i_s\{\boldsymbol{X}^{(u+1)}\} - \boldsymbol{F}\left(i_s\{\boldsymbol{X}\}^{(u)}\right) \tag{3.27}$$

$\boldsymbol{J}\left(\boldsymbol{X}^{(u)}\right)$ denotes the Jacobian matrix, while $\epsilon\{\boldsymbol{F}\left(i_s\{\boldsymbol{X}\}^{(u)}\right)\}$ represents the residual error of the u^{th} iteration. Further, applying the constraint $\epsilon\{\boldsymbol{F}\left(i_s\{\boldsymbol{X}\}^{(u)}\right)\} < 0.1\%$, results in optimum set of solution → $\{\widehat{\omega_s}, \hat{\vartheta}\}$.

Figure 3.8 graphically shows the contour of the minimization function by plotting $\boldsymbol{F}(i_s\{\boldsymbol{X}\})$ with respect to varying values of $\left\{f_s^* = \frac{\omega_s^*}{2\pi}, \vartheta^*\right\}$, highlighting the optimum operating point for a rated load of $P_o = 1kW$ for a voltage conversion of 400-28V. As observed, the global minima of the function lies at $\{i_{turnoff}, \hat{f_s}, \hat{\vartheta}\} = \{1.3A, 465.2kHz, 45.89°\}$ which ensures minimal switching losses due to implementation of SR.

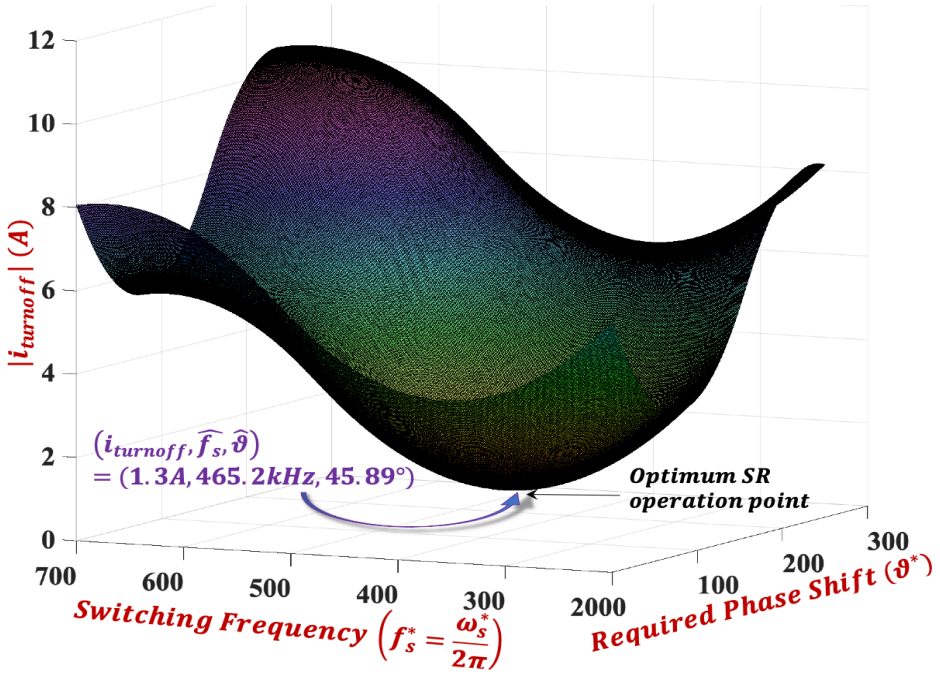


Figure 3.8: Plot of Turnoff Current Cost Function with Respect to f_s^* and ϑ^*

3.4. Analytical Modeling and Characterization of HFPT Parameters

Referring to the EV onboard charger-based application of (400-600V) to (24-28V) conversion, a turns ratio (n) of 22:1 is selected based on the trade-offs between the core loss and winding loss, to adhere to the unity nominal gain requirement of the CLLC converter resulting in efficient voltage regulation [147]. Corresponding to the selected *n*, the number of turns selected in each multi-layer PCB are selected as per IPC 2221 standard [148] that provides the minimum copper conductor width required to ensure the desired current flow for a defined copper conductor thickness adhering to a maximum temperature rise limit in the winding. The empirical formula to corelate the conductor width required with respect to temperature rise is shown as follows:

$$A_c = \frac{I_c}{(k*\Delta T^b)^{\frac{1}{c}}} \tag{3.28}$$

Using the area of the conductor calculated by (3.28), the width of the conductor is obtained as follows:

$$w_c = \frac{A_c}{h_t*1.378} \tag{3.29}$$

where, A_c is the area of the conductor in $mils^2$, w_c is the conductor width in mils, I_c is the current in the conductor in amperes, ΔT is the temperature rise in ℃, h_t is the thickness of the conductor used in ounces (oz.) of copper. The empirical constants k, b and c are obtained from curve fitting to the IPC 2221 current carrying standard curves and the numerical values are shown as follows: For external layers: $k = 0.048, b = 0.44, c = 0.725$, while for the internal layers: $k = 0.024, b = 0.44, c = 0.725$. Further, the spacing between the windings are decided by the voltage gradient between the two windings to ensure desired creepage to prevent any potential turn-to-turn short circuit.

To elucidate further, an analytical formulation for primary winding configuration is shown that depicts the maximum and minimum number of windings in the external and internal layers adhering to the specifications shown below:

- Magnetic core – FR45810EC planar ferrite core.
- Window width $(b_t) - 21.4mm \rightarrow 20mm$ (clearance from the core edges 0.7mm each side)
- $I_p\ (max) = 10A$
- Selected conductor thickness $(h_t) - 2\ oz.$ copper.
- Temperature rise (ΔT) limited to 40℃.

With h_t defined as 2oz., the minimum conductor width (w_{c_e}) for external layers is 1.76mm (selected to be 2mm for safety margin) and that for internal layers (w_{c_i}) is 3.49mm (selected to be 3.75mm for safety margin). Additionally, corresponding to per-turn voltage gradient $\left(\frac{V_p}{N} = \frac{600}{22} = 27V\right)$, the safe creepage between the windings is selected to be 0.5mm for external layers (c_e) and 0.25mm for internal layers (c_i).

Using the specifications for the winding thicknesses, the maximum number of turns in external layers ($N_{e,max}$) can be derived as follows:

$$b_t = N_{e,max} \times w_{c_e} + \left(N_{e,max} - 1\right) \times c_e \tag{3.30}$$

$$20mm = N_{e,max} \times 2mm + \left(N_{e,max} - 1\right) \times 0.5mm \tag{3.31}$$

$$N_{e,max} = 8.2 \sim 8 \tag{3.32}$$

As seen in (3.32), the maximum number of turns in external layer ($N_{e,max}$) is limited to 8. Similarly, for internal layers, the maximum number of turns in internal layers ($N_{i,max}$) can be derived as follows:

$$b_t = N_{i,max} \times w_{c_i} + \left(N_{e,max} - 1\right) \times c_i \tag{3.33}$$

$$20mm = N_{i,max} \times 3.75mm + (N_{i,max} - 1) \times 0.25mm \tag{3.34}$$

$$N_{i,max} = 5.06 \sim 5 \tag{3.35}$$

As seen in (3.35), the maximum number of turns in internal layer ($N_{i,max}$) is limited to 5.

Using the above-mentioned information, three non-interleaved winding configurations are studied in this work (explained in Table 3.1). In addition to that, to

explain the R-L-C modeling of an interleaved structure, one example of 8-layers {7P-1S*-1S*-4P-4P-1S*-1S*-7P}configuration is also explained.

Table 3.1: Winding Configurations Under Study

No.	No. of Layers per winding	Primary Winding (series)	Secondary Winding (*Layers are connected in parallel)	Turns Ratio
1	4 layers	8P-3P-3P-8P	1S*-1S*-1S*-1S*	22:1
2	4 layers	7P-4P-4P-7P	1S*-1S*-1S*-1S*	
3	4 layers	6P-5P-5P-6P	1S*-1S*-1S*-1S*	
4	8 layers	Interleaved: 7P-1S*-1S*-4P-4P-1S*-1S*-7P (*Layers 2,3,6,7 are connected in parallel)		

As observed in Table 3.1, for the non-interleaved winding configurations, the 4-layer primary winding consisting of 22 turns is realized using different number of turns in each layer. The winding structure and its PCB layout design for one such non-interleaved configuration {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]} is shown in Figure 3.9. As observed, the nomenclature of the primary winding: 7P-4P-4P-7P denotes that 7 turns of primary (P) winding are placed in the first layer, followed by 4 in the second layer, 4 in the third layer and the rest 7 turns in the fourth layer. The insulation between the copper layers is enabled by the prepreg and core layer of thicknesses h_{pr} and h_c, respectively. Further, the transition from one layer to the next one is realized using conventional vias in the PCB, with their hole dimensions matching the current carrying requirements of the windings as per IPC 2221. Similar, arrangement is observed for the other two non-interleaved winding configurations with different number of turns in each of the PCB layer. The secondary winding in the non-interleaved configurations is designed to portray a single turn, which is realized using one turn in each of the four layers and using vias at the winding terminals to

effectively connect them in parallel. The nomenclature 1S*-1S*-1S*-1S* (*Layers are connected in parallel) is used to highlight the parallel connection of the four layers, thus only extracting a single equivalent turn from a four-layer PCB. In addition to that, Fig. 3.10 shows the winding configuration of the interleaved winding structure. As observed, the notation for interleaved winding configuration (as seen in Table 3.1) corresponds to an 8-layer PCB denoted as 7P-1S*-1S*-4P-4P-1S*-1S*-7P. In this case, the PCB winding assembly is realized using 7 turns of primary winding in the first layer, followed by 4 turns of primary winding in the fourth layer, 4 turns in the fifth layer and finally 7 turns in the eighth layer, all connected through conventional vias. The secondary winding is realized using single turn in second, third, sixth and seventh layer, all connected in parallel through vias at their terminal points to realize one turn in the secondary winding.

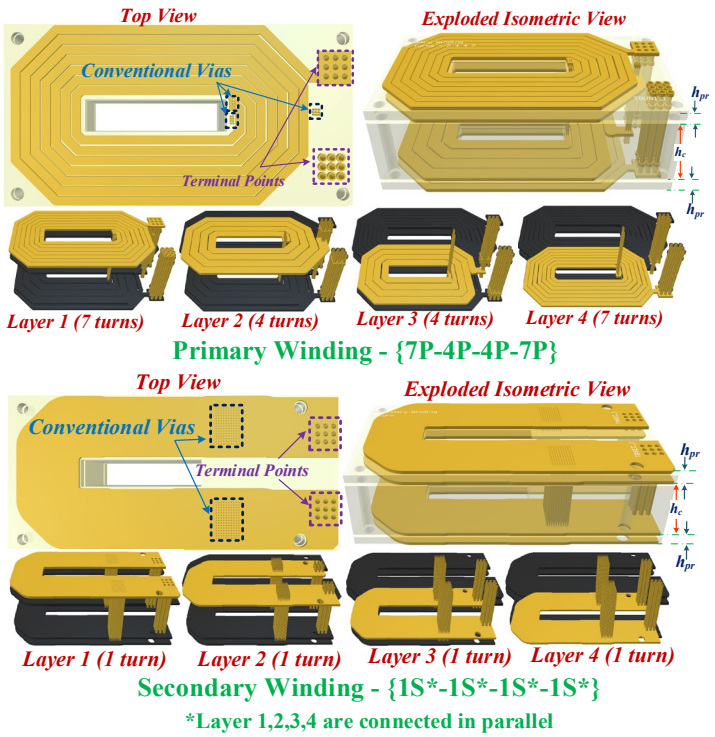


Figure 3.9: PCB Winding Arrangement for Non-interleaved {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]} Configuration.

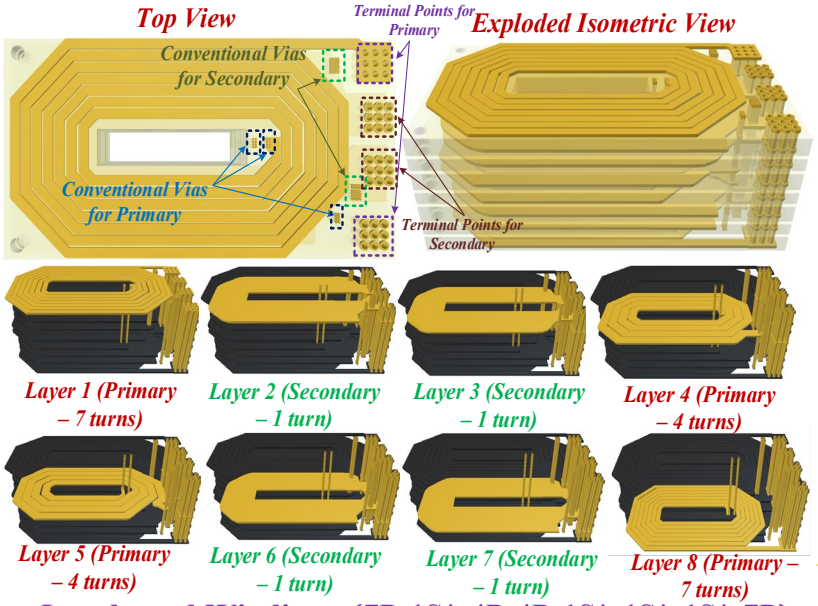


Figure 3.10: PCB Winding Arrangement for Interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P}) Configuration.

The respective 2D (front view) illustrations of the winding configurations mentioned in Table 3.1 are shown in Figure 3.11. Corresponding to the winding configurations as shown in Figure 3.11, this section characterizes the transformer components in detail and provides detailed tradeoffs pertaining to design and fabrication-based aspects by analyzing the model through 3D FEA simulations and analysis.

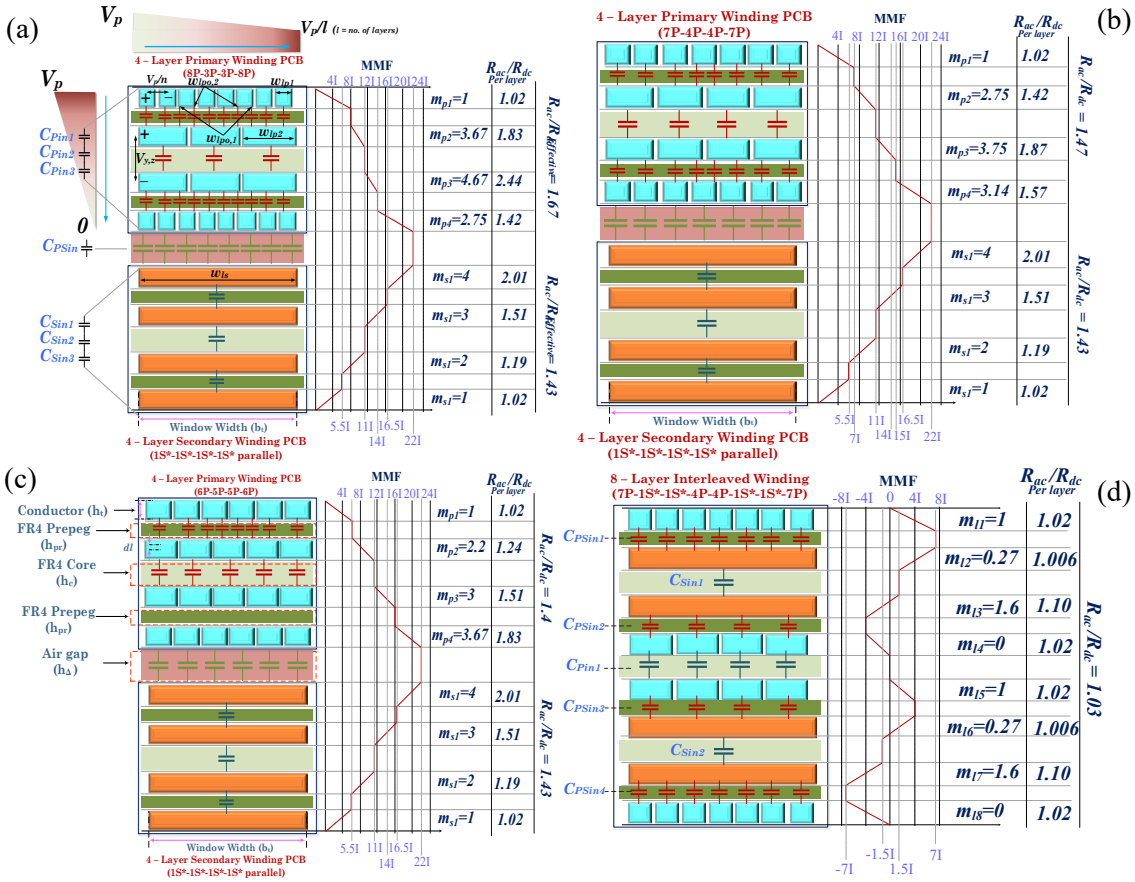


Figure 3.11: Structural Winding Configurations with Respective MMF Distributions for (a) Primary: 8P-3P-3P-8P (Series); Secondary: 1S*-1S*-1S*-1S*(Parallel) (b) Primary: 7P-4P-4P-7P (Series); Secondary: 1S*-1S*-1S*-1S*(Parallel) (c) Primary: 6P-5P-5P-6P (Series); Secondary: 1S*-1S*-1S*-1S*(Parallel) Configurations with 4-layer PCB and (d) Interleaved Winding Configuration: 7P-1S*-1S*-4P-4P-1S*-1S*-7P with 8-layer PCB.

3.4.1. Modeling and Controllable Synthesis of Leakage Inductance

Several studies have emphasized on the modeling and controllable reduction of leakage inductance focusing on the winding arrangement and interleaved structure [63,65]. However, with an objective to attain minimized switching losses (through ZVS) and yet achieve the required gain, this sub-section focusses on the fabrication-based trade-offs and

elucidates the dependencies on various factors pertaining to the orientation of the winding structures.

The configurations mentioned in Table 3.1 are assembled using EE type of ferrite core, as observed in Figure 3.12. To implement a leakage integrated HFPT design, an air gap (h_g) (as seen in Figure 3.12) is introduced between the cores, intentionally leading to flux leakage from the core with the return path through the gap, winding layers and the insulation layers. Based on this structure, as explained in [142], the magnetic energy (E_k) associated with the leakage flux is used to analytically formulate the leakage inductance, highlighting its dependency on the conductor thickness and insulator between them, as shown in (3.36).

$$E_k = \frac{\mu_o}{2} \sum \int_0^{h_t} H^2 l_t b_t dl = \frac{1}{2} L_k I_k^2 \; ; \; k \in \{P, S\} \tag{3.36}$$

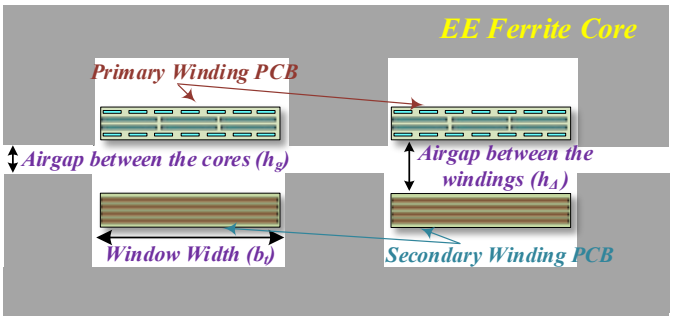


Figure 3.12: Arrangement of Transformer Windings in EE Ferrite Core Assembly.

where, μ_o represents the permeability of the core, H denotes the field strength, which is formulated by the ampere turns linked, l_t is the length of each winding, b_t is the window width of the core and h_t is the thickness of the conductor. Further, dl is the incremental thickness situated at a distance of l from the inner surface of the conductor, as observed in Figure 3.11. Referring to (3.36), equations (3.37-3.39) elucidate the

formulation of the magnetic energy corresponding to the primary winding, secondary winding, and the air gap respectively for a non-interleaved {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]} winding configuration.

$$E_P = \frac{\mu_o}{2} l_t b_t \left[22 \int_0^{h_t} \left(\frac{I_P l}{b_t h_t}\right)^2 dl + \left(\frac{7I_P}{b_t}\right)^2 \left(h_t + h_{pr} + h_\Delta\right) + \left(\frac{11I_P}{b_t}\right)^2 (h_t + h_c + h_\Delta) + \left(\frac{15I_P}{b_t}\right)^2 \left(h_t + h_{pr} + h_\Delta\right) + \left(\frac{22I_P}{b_t}\right)^2 (h_t + h_\Delta)\right] \quad (3.37)$$

$$E_S = \frac{\mu_o}{2} \frac{l_t b_t}{n^2} \left[22 \int_0^{h_t} \left(\frac{I_P l}{b_t h_t}\right)^2 dl + \left(\frac{22I_P}{b_t}\right)^2 (h_t + h_\Delta) + \left(\frac{\frac{33}{2} I_P}{b_t}\right)^2 \left(h_t + h_{pr} + h_\Delta\right) + \left(\frac{11I_P}{b_t}\right)^2 (h_t + h_c + h_\Delta) + \left(\frac{\frac{11}{2} I_P}{b_t}\right)^2 \left(h_t + h_{pr} + h_\Delta\right)\right] \quad (3.38)$$

$$E_{lk,air} = \frac{\mu_o}{2} l_t b_t \left[\left(\frac{22I_P}{b_t}\right)^2 (h_\Delta)\right] \quad (3.39)$$

Further, analytical expressions corelating the leakage inductances for the four winding structures with the conductor and PCB insulator thickness (h_{pr}: prepreg layer and h_c: core layer) are shown in Table 3.2.

Table 3.2: Leakage Inductance Analytical Model for Winding Configurations Under Study

Winding Configuration	**Primary Leakage Inductance (L_p) =**	**Secondary Leakage Inductance (L_s) =**	**Leakage in the air gap between the windings =**
{8P-3P-3P-8P}, {1S*-1S*-1S*-1S*}	$\frac{\mu_o l_t}{b_t}\left[\frac{2617}{3}h_1 + 260h_{pr} + 121h_c + 865h_\Delta\right]$	$\frac{\mu_o l_t}{n^2 b_t}\left[\frac{2745}{3}h_1 + \frac{605}{2}h_{pr} + 121h_c + \frac{1815}{2}h_\Delta\right]$	$\frac{\mu_o l_t}{b_t}\ [484h_\Delta]$
{7P-4P-4P-4P}, {1S*-1S*-1S*-1S*}	$\frac{\mu_o l_t}{b_t}\left[\frac{2659}{3}h_1 + 274h_{pr} + 121h_c + 879h_\Delta\right]$		
{6P-5P-5P-6P}, {1S*-1S*-1S*-1S*}	$\frac{\mu_o l_t}{b_t}\left[\frac{2713}{3}h_1 + 292h_{pr} + 121h_c + 897h_\Delta\right]$		
Interleaved {7P-1S*-1S*-4P-4P-1S*-1S*-7P}	$\frac{\mu_o l_t}{b_t}\left[\frac{217}{3}h_1 + 65h_{pr}\right]$	$\frac{\mu_o l_t}{b_t}\left[\frac{461}{6}h_1 + 65h_{pr} + \frac{18}{4}h_c\right]$	N/A

Referring to the interdependency of the leakage inductances on the structural arrangement and related hardware specifications of the windings, the designer has the flexibility to obtain the required leakage varying the air gap (h_Δ). Further, the leakage inductances also depend on the thickness of the conductor (h_1) used for the PCB fabrication that typically ranges between 35 to 140μm corresponding to 1 to 4 oz. of copper. To elucidate this dependency, Figure 3.13 portrays a plot of different values of leakage inductances obtained from 3D FEA simulations for the abovementioned four winding configurations. As observed, due to increased flux leakage with increasing values of air

gap between the winding, the resultant leakage inductances also see a linear rise. In case of interleaved winding structure, due to absence of airgap between the two windings, the leakage inductance depends only the conductor thickness, which results in a linearly increasing trend – matching well with the derived analytical expressions (as shown in Table 3.2).

Furthermore, as observed in Table 3.2, the effective value of leakage inductance also depends on the arrangement, width and thickness of the insulators used for PCB fabrication. This aspect generally depends on the PCB manufacturing capabilities and is defined according to the thickness of the fabricated PCBs [149]. The variation of the obtained leakage inductances with {[8P-3P-3P-8P],[1S*-1S*-1S*-1S*]}configuration fabricated using various PCB thicknesses (t) and corresponding thickness of insulation layers (h_{pr} and h_c) for a typical 4-layer PCB is illustrated in Figure 3.14. Please note that the solid lines show the trend of L_P and $L_S$with respect to variation in h_{pr}, while the dotted lines show the variation with respect to h_c. Further, it is worthwhile to point out that the flexibility provided due to the variation in h_{pr}, h_c and h_t is limited to the design phase of the PCB windings. Once the PCBs are fabricated, the control parameter to tightly modulate the leakage inductances is limited to h_Δ only.

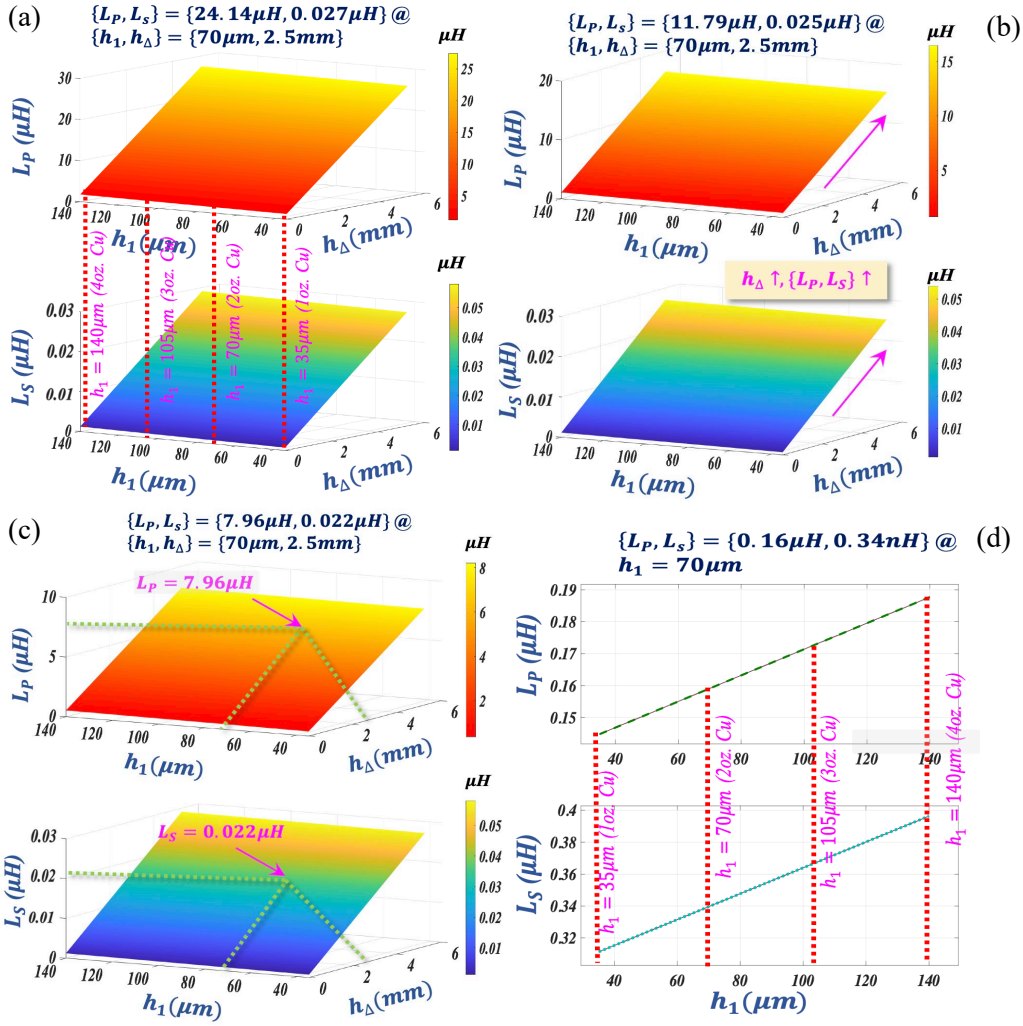


Figure 3.13: (a), (b), (c) 3D Plot Comparing Resultant Leakage Inductances for Different h_1 and h_Δ for Non-interleaved Winding Configurations; (d) Plot Corelating Leakage Inductances for Different h_1 for Interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P} Configuration.

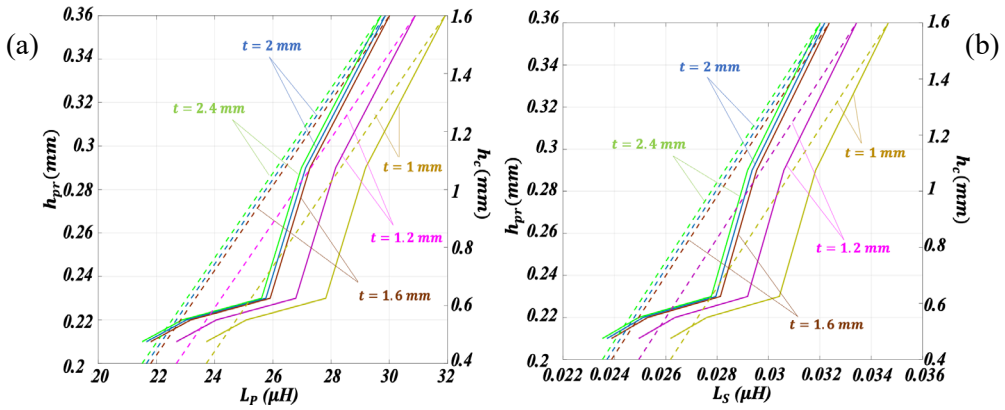


Figure 3.14: Plots Explaining the Relation Between (a) L_P and (b) L_S for Different h_{pr} and h_c Corresponding to Different PCB Thicknesses for {[8P-3P-3P-8P], [1S*-1S*-1S*-1S*]} Winding Configuration.

As seen in the above analysis, the leakage inductance obtained using interleaved winding is considerably smaller than that with non-interleaved winding. This is because the magnetic energy linked to leakage flux is significantly lesser due to absence of inter-winding air gap, leading to better flux linkage between the windings and the core. In that context, Figure 3.15 compares the MMF distribution and field linkage of each layer of non-interleaved {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]} and interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P}) winding structures, obtained through 3D FEA simulations. Relating these results to the MMF distribution shown in Figure 3.15, the resultant magnitude of H (A/m) is found to be increasing while moving from the primary layer-1 towards the air gap, reaching its peak for primary layer-4 and secondary layer-1, and consequently reducing at secondary layer - 4. With all the above-mentioned considerations, the optimal selection of fabrication parameters depends on the ZVS criteria and the application specific voltage gain requirement, which are covered in Section 3.4.

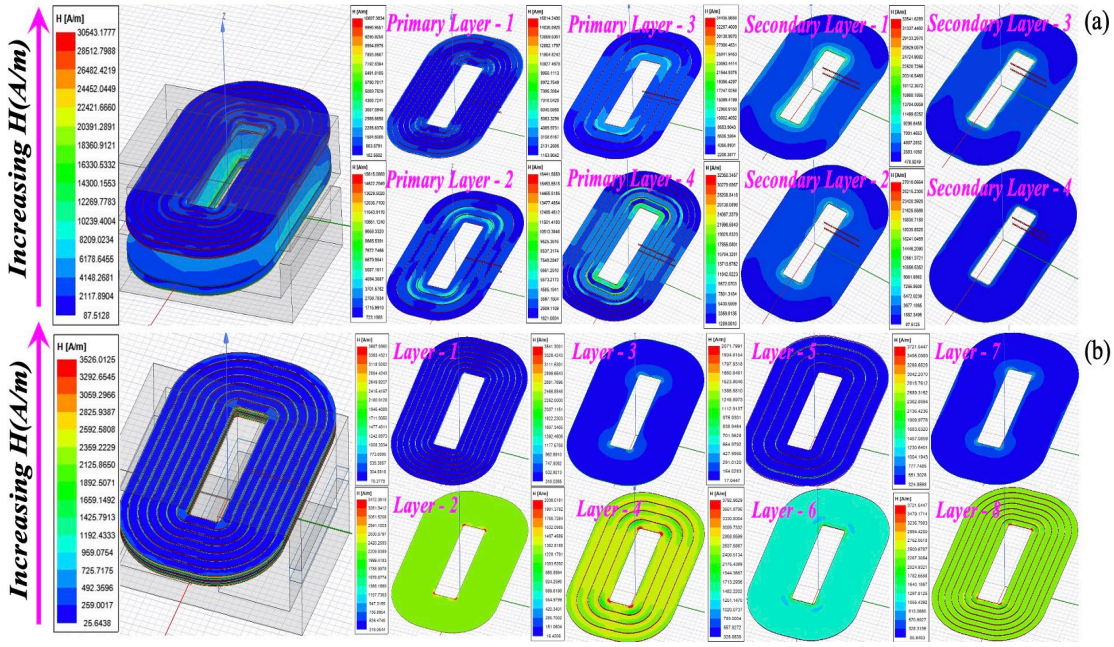


Figure 3.15: MMF Distributions Obtained from 3D FEA Simulation for (a) {[8P-3P-3P-8P],[1S*-1S*-1S*-1S*]}Winding Configuration and (b) Interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P}) Configuration.

3.4.2. Winding Resistance Modeling and Minimization

For applications targeting high switching frequency similar to the proposed CLLC DC/DC converter topology, winding losses pertaining to the effective AC winding resistance are found to be significantly high due to eddy current and skin effects [63]. Further, the HFPTs used for resonant converters experience non-uniform current density due to variable switching frequencies leading to winding losses due to proximity effect. Thus, accurate modelling of winding resistance for a wide frequency range with different transformer winding structures is quintessential for conduction loss optimization.

The effective winding resistance accounting for the skin effect of a foil conductor with sinusoidal excitation can be represented as the ratio of AC resistance (R_{ac}) to the

winding DC resistance (R_{dc}), as expressed in (3.40).

$$\frac{R_{ac}}{R_{dc}} = \frac{\gamma}{2}\left[\frac{\sinh\gamma+\sin\gamma}{\cosh\gamma-\cos\gamma}\right];\ R_{dc} = \frac{\rho l_t}{h_t b_t} \tag{3.40}$$

where, ρ is the resistivity of the conductor and $\gamma = \frac{h_t}{\delta}$, where δ is the skin depth. Utilizing (3.40), based on the fill factor of the conductor in the window width, porosity of the conductor and the switching frequency, the analytical expression for the effective winding AC resistance is obtained using the improved Dowell's equation [66] by extrapolating (3.40) for the current density field distribution in kth layer, as shown in (3.41).

$$\frac{R_{ac}}{R_{dc}} = \frac{\gamma}{2}\left[\frac{\sinh\gamma+\sin\gamma}{\cosh\gamma-\cos\gamma} + (2m-1)^2\frac{\sinh\gamma-\sin\gamma}{\cosh\gamma+\cos\gamma}\right] \tag{3.41}$$

$$m = \frac{MMF(k)}{MMF(k)-MMF(k-1)} \tag{3.42}$$

where, MMF(k) denotes the magnetomotive force of windings in layer k.

The losses due to proximity effect (depicted by the second term in (3.42)) majorly depends on the orientation of windings, which is dictated by the value of m for each layer. A comparative analysis elucidating the effective $\frac{R_{ac}}{R_{dc}}$ ratio for the four winding structures for 500kHz operational frequency and $h_1 = 70\mu m$ is shown in Figure 3.11. As observed, the effective ratio ($\left[\frac{R_{ac}}{R_{dc}}\right]_{eff}$) is 38.3% lower than for the interleaved structure as compared to the other three winding arrangements resulting in minimum AC resistance, thus significantly reducing the winding induced losses in the system. This concept is also verified by visualizing and comparing the current density distribution of {[7P-4P-4P-7P], [1S*-1S*-1S*-1S*]} and interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P}) winding

structures through 3D FEA analysis, as shown in Figure 3.16. As observed, the current density is higher near the edges for non-interleaved winding arrangements due to skin and proximity effects, which tend to distort the current distribution even further at higher frequencies, leading to higher winding losses. In that context, Figure 3.17 (a) shows the variation of the effective winding resistance for both the primary and secondary winding obtained from FEA simulations with respect to the excitation frequencies for the four mentioned winding configurations.

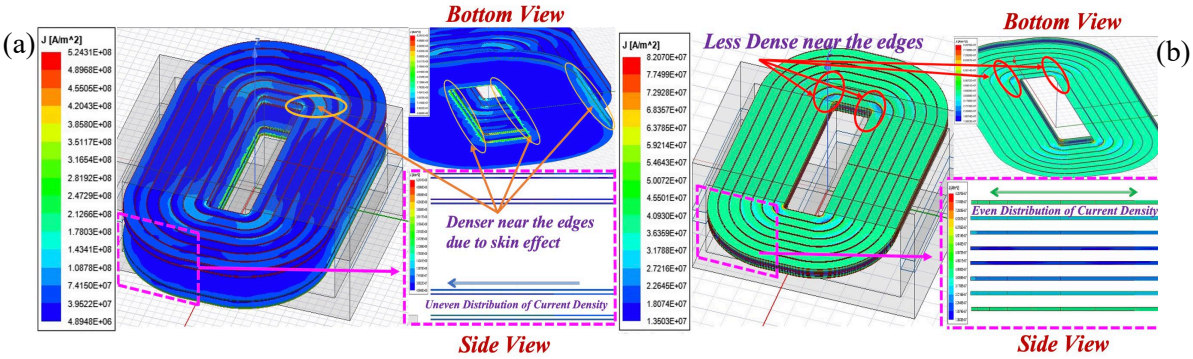


Figure 3.16: Current Density Distribution Obtained from 3D FEA Simulations for (a) ({[7P-4P-4P-7P], [1S*-1S*-1S*-1S*]}) and (b) Interleaved ({7P-1S*-1S*-4P-4P-1S*-1S*-7P}) Winding Distribution.

The $\frac{R_{ac}}{R_{dc}}$ ratio is not only dependent on m, but also on the value of γ that depends on the conductor thickness and the frequency of operation. To depict this relationship, Figure 3.17 (b) elucidates the plot of $\frac{R_{ac}}{R_{dc}}$ ratio with respect to variation in γ for different values of m. As observed, as the thickness of the conductor exceeds its skin depth ($h_t \gg \delta$), the $\frac{R_{ac}}{R_{dc}}$ ratio observes a drastic increase, resulting in higher winding resistance. Further, at a fixed frequency operation, reducing the conductor thickness results in lower value of AC

resistance, at an expense of increased DC winding resistance and hence a higher overall winding resistance, as observed in the trend shown in Figure 3.17 (b).

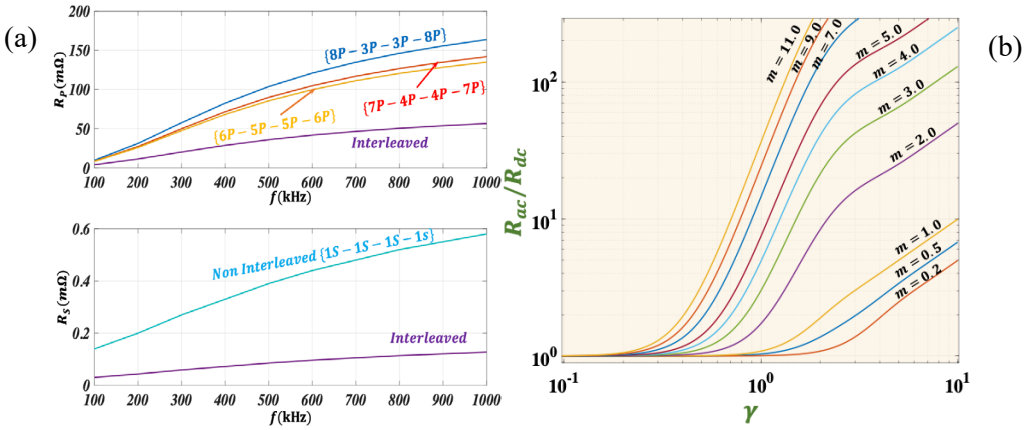


Figure 3.17: (a) Plot Depicting the Variation of R_P and R_S with Respect to Variation in Frequency (b) Plot Depicting Variation of the Ratio $\frac{R_{ac}}{R_{dc}}$ with Respect to k for Different Values of m Depending on the Winding Configuration.

The above analysis dissects the Dowell's equation to formulate the effective winding resistance for a HFPT. However, as suggested in [65], there are several assumptions pertaining to the Dowell's equation that are ignored for reduced analytical complexity. These factors include the porosity factor [150] (included when the conductor width is comparable to its thickness leading to proximity effect in horizontal direction), distance considerations between multiple conductors turns in a single layer, distance of conductor surface from the core, and sinusoidal excitation provided to the windings. Thus, to accurately characterize the winding resistance and to observe the losses due to skin and proximity effects, the 3D FEA simulation proves to be more reliable as presented in this work.

3.4.3. Stray Capacitance Modeling

The switching performance of the CLLC resonant converter majorly degrades due to presence of inter- and intra-winding capacitances in the HFPT. Several techniques have been discussed in the literature that focus on modelling these stray capacitances to enhance the EMI performance and voltage regulation of the converters under various loading conditions [63]. However, all the works have presented a generalized analysis to model these capacitors, with several assumptions pertaining to non-uniformity in the PCB insulation layers and winding configurations. For example, [63] considers the overlapping area for all the capacitors to be equal with equal spacing between the two layers. However, as observed in Figure 3.11, generally the winding arrangement dictates the resultant stray capacitance with varying winding widths adhering to PCB fabrication standards. Thus, with an intent to provide intricate modelling while accounting for the winding arrangement, insulation thickness, overlapping area and voltage gradient between the conductors, this section provides a detailed model to formulate the stray capacitances appearing in the primary and secondary windings.

Figure 3.11 (a) shows the voltage distribution of primary winding of {[8P-3P-3P-8P], [1S*-1S*-1S*-1S*]} winding configuration. The potential across the winding is assumed to vary linearly with the turns. Thus, the potential at each turn of the winding (V_y) can be written as:

$$V_y = \frac{(n+1)-y}{n} V_p; y \in \{1,2,3 \dots n\} \tag{3.43}$$

where n is the number of turns in the winding, and V_p is the primary voltage excitation. Thus, a voltage gradient ($V_{y,z}$) exists between the two adjacent windings and the

windings in two adjacent layers, which essentially leads to formation of virtual capacitors. This capacitance ($C_{y,z}$) can be formulated by analyzing the overlapping conductor area and the distance between the two subsequent conductors as shown in (3.44).

$$C_{y,z} = \frac{\varepsilon_o \varepsilon_r S_{y,z}}{d} \tag{3.44}$$

where, $\varepsilon_o$and ε_r denote the permittivity of air and relative permittivity of the dielectric material respectively, $S_{y,z}$ is the overlapping area between turns y and z as observed in (3.44) and d denotes the spacing between the two conductors.

$$S_{y,z} = \int_0^{l_t} w_o dl \tag{3.45}$$

where, w_o is the overlapping conductor width and dl_t represents an infinitesimally small sectional length of a turn, which is integrated over the entire circumference to form a complete turn of length l_t.

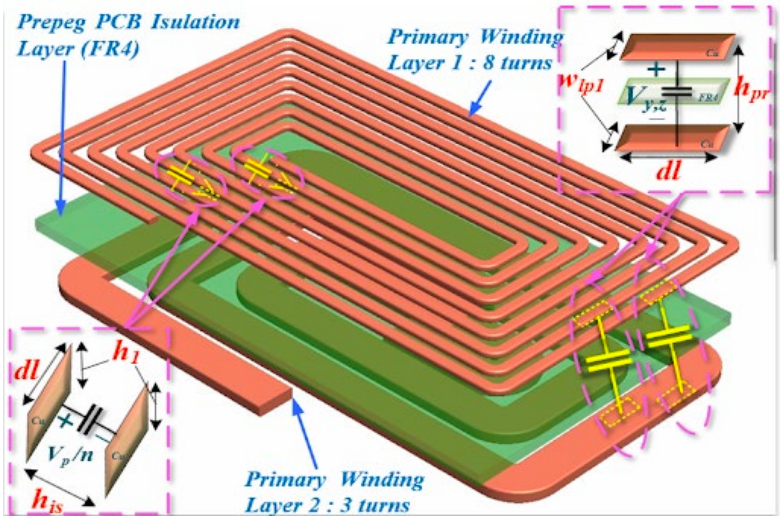


Figure 3.18: Intra-winding Capacitance Model for {[8P-3P-3P-8P], [1S*-1S*-1S*-1S*]} Winding Configuration.

Referring to Figure 3.18, since the overlap area $\left(\int_0^{l_t} h_1 dl\right)$ between the two turns is very small with air (distance between the conductors: h_{is}) being the dielectric medium

between them, the turn-to-turn capacitance is negligible and thus, its effect can be ignored. On the other hand, the capacitance between adjacent layers can be formulated by analyzing the total energy associated with the electric field between the two layers.

$$E_l = \sum_{l=1}^{l_n} \frac{1}{2} [C_{y,z} V_{y,z}^2]_{layer} \tag{3.46}$$

$$E_{l_t} = \sum_{l=1}^{l_n} E_l \tag{3.47}$$

where, $V_{y,z}$is the potential difference between two conductor surfaces, and E_l denotes the total energy in a layer l.

Thus, using (3.46-3.47), the effective inter or intra-winding capacitance can be formulated as:

$$C_{in} = \sum_{t=1}^{l_t(no.of\ layers)} \frac{2E_{l,t}}{V_{y,z}^2} \tag{3.48}$$

Referring to Figure 3.11(a), the intra-winding capacitance between first and second layer ($C_{Pin,1}$) is similar to that of between third and fourth layer ($C_{Pin,3}$) and can be formulated as:

$$C_{pin,1} = \frac{\varepsilon_o \varepsilon_r}{h_{pr}} \left[6w_{w_{l_{p^1}}} + 2w_{l_{P^o,_1}} + 2w_{l_{P^o,_2}} \right] \int_0^l dl = C_{pin,3} \tag{3.49}$$

Similarly, the intra-winding capacitance between second and third layer of primary PCB is formulated as:

$$C_{pin,2} = \frac{\varepsilon_o \varepsilon_r}{h_c} [3w_{l_p 2}] \int_0^l dl \tag{3.50}$$

All three capacitances are in parallel and thus can be added to formulate the overall primary intra-winding capacitance:

$$C_{Pin} = C_{p1} + C_{p2} + C_{p3} \tag{3.51}$$

Similarly, the intra-winding capacitance for the secondary winding can be formulated as:

$$C_{sin,1} = C_{sin,3} = \frac{\varepsilon_o \varepsilon_r}{h_{pr}} w_{l_s} \int_0^l dl \tag{3.52}$$

$$C_{sin,2} = \frac{\varepsilon_o \varepsilon_r}{h_c} w_{l_s} \int_0^l dl \tag{3.53}$$

$$C_{sin} = C_{s1} + C_{s2} + C_{s3} \tag{3.54}$$

Following the same method, the inter winding capacitance between primary and secondary board can be calculated as:

$$C_{PSin} = \frac{\varepsilon_o \varepsilon_r}{h_\Delta} [8 w_{l_p 1}] \int_0^l dl \tag{3.55}$$

A comprehensive comparison of the analytical formulation to determine the inter and intra winding capacitances for the four mentioned winding configurations referring to Figure 3.11 is presented in Table 3.3.

As observed in Table 3.3, the capacitances depend majorly on the overlapping area of the windings, airgap between the windings, thickness of the insulation between the layers and the length of a conductor turn. Out of the above-mentioned factors, the overlapping area is dependent on the winding configuration and relevant works [68] have provided methods to reduce it by modifying the arrangement of turns. Further, the length of the conductor also depends on the core geometry, which solely depends on the application specifications. To elucidate the dependency of the inter and intra-winding capacitances on the insulator layer thicknesses, Figure 3.19 shows the variation of intra-winding capacitances (C_{Pin} and C_{Sin}) for {[8P-3P-3P-8P], [1S*-1S*-1S*-1S*]}configuration, fabricated using various PCB thicknesses (t) with respect to change in

h_{pr} and h_c, obtained through 3D FEA simulations. Further, Figure 3.20 shows the variation of inter-winding capacitance for with respect to change in h_Δ for all the winding configurations. As observed, as the airgap increases, the interwinding capacitance observes a steep descent, and the trend becomes more flatter for higher values of airgap, which matches the analytical formulations presented in this section. Referring to the presented plots and analytical formulations shown in Table 3.3, it can be deduced that reduction in the intra-winding capacitance can be achieved either by increasing the insulator thicknesses or by reducing the overlap area of the conductors in two consecutive layers, as demonstrated in [69]. Both of these aspects of stray capacitance reduction can be exercised in the PCB design phase only. However, the inter-winding capacitance can be reduced externally by increasing the airgap (h_Δ) between the windings in the post-fabrication phase, adhering to the core dimensions.

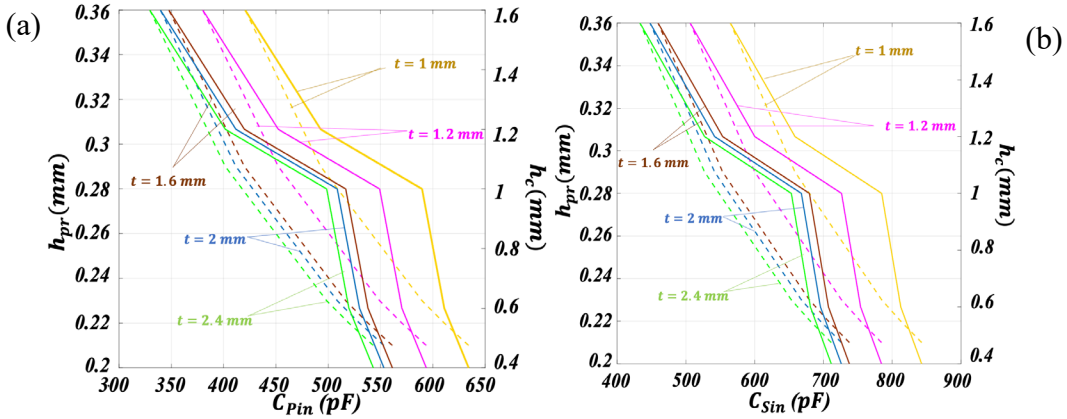


Figure 3.19: Plots Explaining the Relation Between (a) $C_{P_{in}}$ and (b) $C_{S_{in}}$ for Different h_{pr} and h_c Corresponding to Different PCB Thicknesses for {[8P-3P-3P-8P], [1S*-1S*-1S*-1S*]} Winding Configuration.

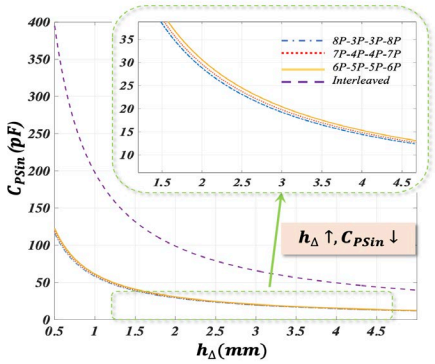


Figure 3.20: Plots Explaining the Relation Between $C_{PS_{in}}$ and Air Gap h_Δ.

Table 3.3: Stray Capacitance Analytical Model for Winding Configurations Under Study

Winding Configuration	**Primary Intra-winding Capacitance ($C_{P_{in}}$) =**	**Secondary Intra-winding Capacitance ($C_{P_{in}}$)**	**Inter-winding Capacitance ($C_{PS_{in}}$) =**
{8P-3P-3P-8P}, {1S*-1S*-1S*-1S*}	$\left[\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}\left[6w_{l_{P^1}} + 2w_{l_{P^o,1}} + 2w_{l_{P^o,2}}\right] + \frac{\varepsilon_o\varepsilon_r}{h_c}\left[3w_{l_{P^2}}\right]\right]\int_0^{l_t} dl$	$\left[\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}w_{l_S} + \frac{\varepsilon_o\varepsilon_r}{h_c}w_{l_S}\right]\int_0^{l_t} dl$	$\frac{\varepsilon_o\varepsilon_r}{h_\Delta}[8w_{l_{P^1}}]\int_0^{l_t} dl$
{7P-4P-4P-4P}, {1S*-1S*-1S*-1S*}	$\left[\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}\left[6w_{l_{P^1}} + 2w_{l_{P^o,1}}\right] + \frac{\varepsilon_o\varepsilon_r}{h_c}\left[4w_{l_{P^2}}\right]\right]\int_0^{l_t} dl$		$\frac{\varepsilon_o\varepsilon_r}{h_\Delta}[7w_{l_{P^1}}]\int_0^{l_t} dl$
{6P-5P-5P-6P}, {1S*-1S*-1S*-1S*}	$\left[\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}\left[4w_{l_{P^1}} + 2w_{l_{P^o,1}} + 2w_{l_{P^o,2}}\right] + \frac{\varepsilon_o\varepsilon_r}{h_c}\left[5w_{l_{P^2}}\right]\right]\int_0^{l_t} dl$		$\frac{\varepsilon_o\varepsilon_r}{h_\Delta}[6w_{l_{P^1}}]\int_0^{l_t} dl$
Interleaved {7P-1S*-1S*-4P-4P-1S*-1S*-7P}	$\frac{\varepsilon_o\varepsilon_r}{h_c}[4w_{l_{P^2}}]\int_0^{l_t} dl$	$\frac{2\varepsilon_o\varepsilon_r}{h_c}[w_{l_S}]\int_0^{l_t} dl$	$\left[\frac{2\varepsilon_o\varepsilon_r}{h_{pr}}\left[4w_{l_{P^1}}\right] + \frac{2\varepsilon_o\varepsilon_r}{h_{pr}}\left[4w_{l_{P^2}}\right]\right]\int_0^{l_t} dl$

3.4.4. Selection of Optimal Winding Configuration

Unlike a conventional CLLC converter model, where a lagging phase of primary current along with sufficient dead time intervals is sufficient to ensure ZVS [151-153], the inclusion of non-idealistic components in the CLLC converter model requires detailed investigation for understanding the conditions for achieving ZVS. Here, the drain-to-source capacitance of the MOSFET (C_{oss}) necessitates constraints in the form of minimum equivalent impedance required to facilitate ZVS commutation. In that context, an equivalent model is developed to comprehensively analyze the ZVS constraints for different conditions for each switch of the primary bridge as shown in Figure 3.21.

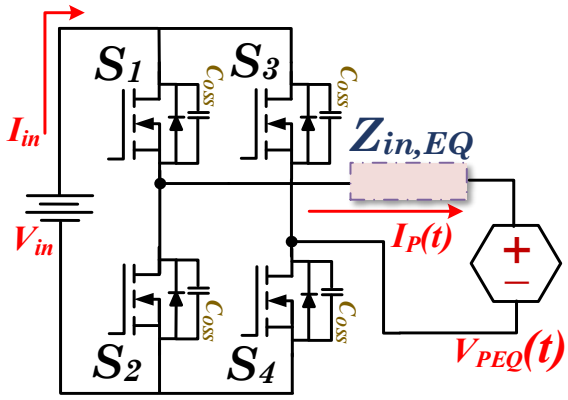


Figure 3.21: Equivalent Circuit for ZVS Investigation

As observed in Figure 3.21, $Z_{in,EQ}$ represents the equivalent input impedance of the CLLC converter whereas $V_{PEQ}(t)$ represents the equivalent voltage source, both referred to the primary side. The equivalent topological structure of the CLLC converter with the inclusion of parasitics is shown in Figure 3.22 obtained by reconfiguring the stray capacitance as a single lumped capacitance referred to the primary side [63,154].The equivalent value of $C_{str,P}$ can be formulated as follows:

$$C_{str,P} = C_{pstr} + C_{sstr} = C_{p,in} + (1-n)C_{ps,in} + n^2 C_{s,in} - n(n-1)C_{ps,in} \quad (3.56)$$

Utilizing the equivalent circuit shown in Figure 3.22, the analytical formulation of $Z_{in,EQ}$ is shown as follows:

$$Z_{in,EQ} = \frac{\left\{(1-f^2-f^2k_2)(1-f^2C-f^2)+f^2k_1(1+C)\left(\frac{f^2}{\omega}-1\right)-\frac{f^4}{m_2}(1+C)\left(\frac{1}{m_1}+\frac{1}{\omega}\right)\right\}+j\left\{f^2(1-f^2)\frac{(1+n_1)}{\omega m_1}-f^4k_2\frac{(1+n_1)}{\omega m_3}-\frac{f^2}{\omega m_2}\right\}}{\left\{\frac{f^6n_1}{\omega^2L_p}\left(\frac{1}{m_1}+\frac{k_2}{m_3}\right)-\frac{f^4}{\omega^2L_p}\left(\frac{n_1}{m_1}+\frac{1}{m_2}\right)\right\}-j\left\{\frac{f^6n_1}{\omega m_2L_p}\left(\frac{1}{m_1}+\frac{1}{\omega}\right)-\frac{f^4}{L_p}\left(1-\frac{n_1k_1}{\omega}\right)-\frac{f^2}{\omega L_p}(1-f^2-f^2k_2)(1-f^2n_1)\right\}} \quad (3.57)$$

where, $f = \frac{\omega}{\omega_r}$, $\omega_r = \frac{1}{\sqrt{L_pC_p}} = \frac{1}{\sqrt{L_sC_s}}$, $k_1 = \frac{L_m}{L_p}$, $k_2 = \frac{L_m}{L'_s}$, $m_1 = \frac{L_p}{R_p}$, $m_2 = \frac{L'_s}{R_{seq}}$, $m_3 = \frac{L_p}{R_T}$, $n_1 = \frac{C_{str,P}}{C_p}$, $R_{seq} = R'_{o,ac} + R'_s$, $R_T = R_p + R_{seq}$.

Further, following the derived equivalent circuit, the equivalent voltage $V_{PEQ}(t)$ can be derived as follows:

$$V_{PEQ}(t) = V_s(t)\left[\frac{Z_m\left(Z_{C_{str,P}}+Z_{C_P}\right)}{\left(Z_P+Z_{C_{str,P}}\right)(Z_m+Z_S)}\right] \quad (3.58)$$

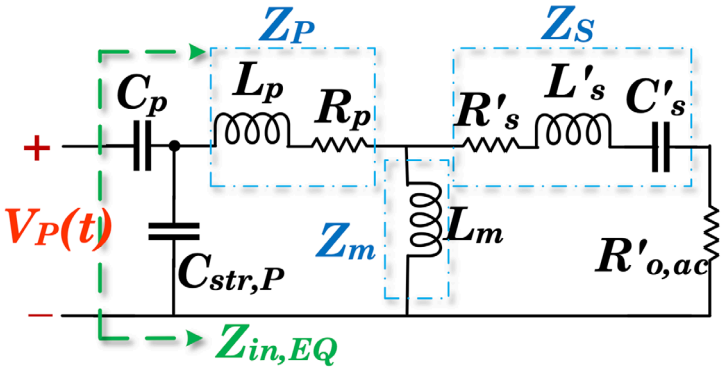


Figure 3.22: Equivalent Circuit with Reconfigured Stray Capacitors

Referring to the equivalent circuit shown in Figure 3.21, two commutation cases can be studied to examine the constraint for the value of L_p required to achieve ZVS as follows:

(a) When switch S_2 and S_3 turn on ($I_P(t) > 0$); as shown in Figure 3.23 (a).

(b) When switch S_1 and S_4 turn on ($I_P(t) < 0$); as shown in Figure 3.23 (b).

As the equivalent port voltage follows half wave symmetry, the condition $V_{PEQ}(t) = -V_{PEQ}(\pi + t)$ is implied. Thus, the analysis for both the cases proves to be similar for formulating the necessary constraint for ZVS. Focusing on the formulation for case (a) (for S_2 and S_3), the energy sunk by the sources can be formulated as follows:

$$E_{sunk} = \int_0^{\tau_d} \left(V_{PEQ} I_P(\zeta) - V_{in} i_{in}(\zeta)\right) dt = \int_0^{\tau_d} \left(V_{PEQ} \left(-2C_{oss} \frac{dV_{in}}{dt}\right)\right) dt$$

$$= 2C_{oss} V_{in} V_{PEQ}(\zeta) \tag{3.59}$$

where, τ_d is the dead time provided to the switches. Further, the total energy in the switch remains constant during the commutation interval, which helps formulate the necessary constraint for ZVS for this case, as follows:

$$E_{sourced} \geq E_{sunk} = \frac{1}{2} |Z_{in,EQ}| I_P^2(\zeta) \geq 2C_{oss} V_{in} V_{PEQ}(\zeta) \tag{3.60}$$

Thus, using (3.60), the minimum impedance for $V_{PEQ}(\zeta) > 0$ can be analyzed as:

$$|Z_{in,EQ}| \geq \left|\frac{4C_{oss} V_{in} V_{PEQ}(\zeta)}{I_P^2(\zeta)}\right| \tag{3.61}$$

where, ζ is the turn on instant of switch S_2 and S_3.

Solving the constraint in MATLAB for finding the constraints for L_P with respect to the magnitude of $Z_{in,EQ}$ for known values of other resonant tank parameters yields the minimum requirement of L_P for different winding configurations. To provide an instance of this evaluation, Table 3.4 shows the formulated values of minimum L_p required to ensure ZVS for all non-interleaved winding configurations at 1kW rated load.

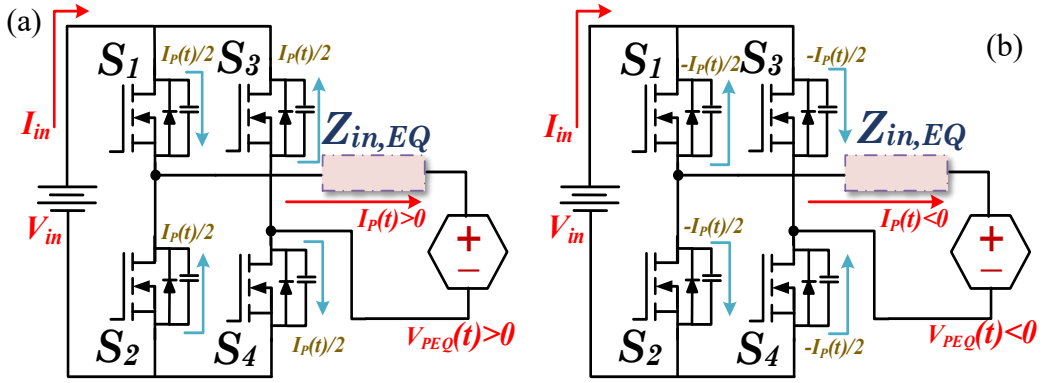


Figure 3.23: ZVS Turn on Cases (a) for Switch S_2 and S_3 (b) for Switch S_1 and S_4.

Table 3.4: Minimum Value of Primary Leakage Inductance Required to Ensure ZVS

No.	Winding Configuration	Minimum L_P required
1	{8P-3P-3P-8P},{1S*-1S*-1S*-1S*}	22.15µH
2	{7P-4P-4P-7P},{1S*-1S*-1S*-1S*}	11.08µH
3	{6P-5P-5P-6P},{1S*-1S*-1S*-1S*}	9.72µH

Further, to adhere to the cost-effectiveness for fabrication, power density constraints and the current carry capabilities, the conductor thickness is selected to be 2oz. copper ($h_1 = 70\mu m$). Moreover, the air gap between the cores is selected to be 1.9mm to obtain the required magnetizing inductance (L_m). Adhering to the supplementary ZVS criteria [151-153] of L_m with respect to the dead band time duration, and maximum switching frequency for achieving the desired gain, the maximum value of L_m is formulated to be $76.26\mu H$.

With the mentioned design criteria, the GHA [80] based gain curves achieved for all four winding configurations are shown in Figure 3.24(a). To adhere to the gain requirements, the relative variation of gain with frequency should follow : $\left[\frac{dG}{df}\right]_{min} \leq \frac{dG}{df} \leq \left[\frac{dG}{df}\right]_{max}$. The factor $\left[\frac{dG}{df}\right]_{\min}$ is decided based on the gain range requirement, which depends

on the Q factor selection for CLLC converter and its trade-offs [25]. Lower $\left[\frac{dG}{df}\right]_{\min}$ will lead to an operating range with higher switching frequencies, thus resulting in higher switching losses. On the other hand, higher $\left[\frac{dG}{df}\right]_{max}$ will lead to steeper gain curve, which might not be realizable by the frequency resolution (or least count) of the controller (TMS320F28379D) used for this application. To validate the accuracy and applicability of the analytical model, the resultant impedances for the primary (Z_P) and secondary (Z_S) side corresponding to all four fabricated windings structures are compared in Figure 3.24(b).

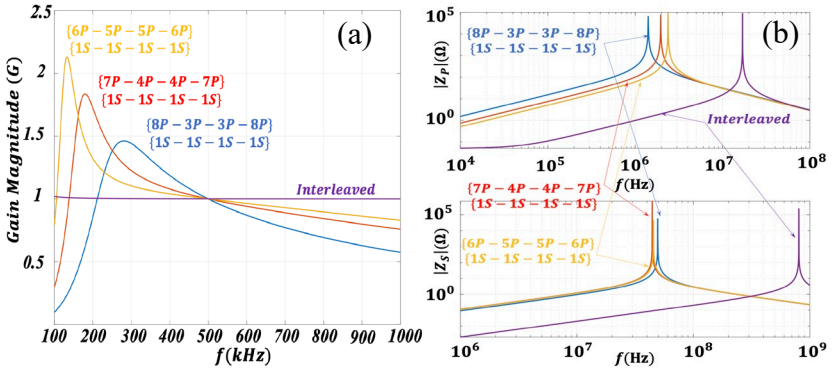


Figure 3.24: (a) Gain Plots for All Winding Configurations; (b) Plot of Equivalent Primary and Secondary Impedance Versus Operational Frequency.

Further, a detailed comparison of the resultant parameters obtained by simulation models and developed windings measured experimentally are shown in Table 3.5. For measuring the R-L-C parameters, GWINSTEK LCR8101G impedance analyzer is employed that has a frequency sweep range of 20Hz to 1MHz with a measurement accuracy of 0.1% and a resolution of 6 digital measurement units. The procedure follows several iterations of a standard open circuit/short circuit test implemented at the terminals of the HFPT, as shown below:

Table 3.5: Comparison of Analytical, Simulation and Experimental Results for Different Winding Configurations

Winding Configuration	Primary Leakage Inductance (μH) L_p			Secondary Leakage Inductance (nH) L_s			Effective Primary Winding Resistance ($m\Omega$) R_p			Effective Secondary Winding Resistance ($m\Omega$) R_s			Primary Intra-winding Capacitance (nF) C_{Pin}			Secondary Intra-winding Capacitance (nF) C_{Sin}			Inter-winding Capacitance (pF) $C_{PS_{in}}$		
	Anly.	**Sim.**	**Exp.**	**Anly.**	**Sim.**	**Exp.**	**Anly.**	**Sim.**	**Exp.**	**Anly.**	**Sim.**	**Exp.**	**Anly.**	**Sim.**	**Exp.**	**Anly.**	**Sim.**	**Exp.**	**Anly.**	**Sim.**	**Exp.**
{8P-3P-3P-8P}, {1S*-1S*-1S*-1S*}	25.887	24.142	25.845	17.63	19.58	14.55	102.683	91.776	121.866	0.819	0.814	1.144	0.509	0.582	0.526	0.668	0.701	0.712	23.102	23.985	25.195
{7P-4P-4P-7P}, {1S*-1S*-1S*-1S*}	12.113	11.794	11.828	17.63	19.94	18.32	82.59	87.254	92.735	0.819	0.843	1.022	0.555	0.618	0.558	0.668	0.673	0.702	23.747	24.553	25.577
{6P-5P-5P-6P}, {1S*-1S*-1S*-1S*}	8.524	7.961	7.825	17.63	19.11	17.62	72.634	82.534	93.216	0.819	0.827	0.981	0.552	0.592	0.561	0.668	0.686	0.698	24.527	25.553	26.731
Interleaved	0.109	0.157	0.211	0.239	0.218	0.324	46.438	49.583	44.356	0.312	0.227	0.236	0.544	0.591	0.561	0.117	0.121	0.121	790.081	791.252	812.252

(a) *Open circuit test with primary probing*: The HFPT equivalent circuit for open circuit test by probing the primary winding, while keeping the secondary side open is shown in Figure 3.25 (a). Please note, $C_{str,P}$ represents the lumped intra- and inter-winding capacitance referred to the primary side (as seen in (3.56)). Selecting the resistance mode measurement, for an excitation frequency of 500kHz (matching the resonant frequency), the value of R_p is obtained. Next, changing the mode to inductance mode calculation, the lumped value of inductance at the primary side is obtained as follows:

$$L_{eq,P} = L_P + L_m \tag{3.62}$$

Further, selecting the impedance measurement mode, the magnitude of $Z_{in,I}$ is measured, the analytical equivalent magnitude of which is formulated as follows:

$$\left|Z_{in,I}\right| = \text{mag}\left(\frac{R_p + j\omega\{L_{eq,P} - \omega^2 C_{str,P} L_{eq,P}^2 - C_{str,P} R_p^2\}}{1 - \omega^2\left(2C_{str,P} L_{eq,P} - C_{str,P}^2 R_p^2\right) + \omega^4 C_{str,P}^2 L_{eq,P}^2}\right) \tag{3.63}$$

(b) *Open circuit test with secondary probing:* Similar procedure of measurement is implemented referred to the secondary side, by keeping the primary side winding open (as seen in Figure 3.25 (b)). With an excitation frequency of 500kHz, the value of R_s is obtained with the resistance mode measurement. The inductance mode measurement provides the value of lumped inductance referred to the secondary side as follows:

$$L_{eq,S} = L_S + \frac{L_m}{n^2} \tag{3.64}$$

Following the same procedure of impedance measurement, the magnitude of $Z_{in,II}$ is measured and recorded.

$$\left|Z_{in,II}\right| = \text{mag}\left(\frac{R_s + j\omega\{L_{eq,S} - \omega^2 C_{str,S} L_{eq,S}^2 - C_{str,S} R_s^2\}}{1 - \omega^2\left(2C_{str,S} L_{eq,S} - C_{str,S}^2 R_s^2\right) + \omega^4 C_{str,S}^2 L_{eq,S}^2}\right) \tag{3.65}$$

where, $C_{str,S} = \frac{C_{str,P}}{n^2}$ is the lumped stray capacitance referred to the secondary side.

(c) *Short circuit test with primary probing:* In this step, the secondary side winding terminals are shorted, resulting in the equivalent circuit shown in Figure 3.25 (c). In this case, with the inductance mode measurement, the lumped inductance obtained is formulated as:

$$L_{eq,SC} = L_P + (L_m || (n^2 L_S)) \tag{3.66}$$

Further, the impedance measured at the primary winding terminal has a magnitude of $Z_{in,III}$ formulated in (3.67), where $C_{str,SC}$ represents the lumped stray capacitance excluding the value of $C_{s_{in}} \left(= C_{p_{in}} + (1 - n^2) C_{ps_{in}}\right)$.

$$Z_{in.III} = \text{mag}\left(\frac{R_p R_s' - \omega^2 \left(L_P L_{eq,S} + L_m L_S'\right) + j\omega\{L_m R_s' + L_{eq,S} R_p + L_P R_s'\}}{\left(R_s' + j\omega L_{eq,S}\right)\left(R_s - \omega^2 C_{str,SC}\left(L_m R_s' + L_{eq,S} R_p + L_P R_s'\right) + j\omega\left\{C_{str,SC}\left(R_p R_s' - \omega^2 \left(L_P L_{eq,S} + L_m L_S'\right)\right) + L_{eq,S}\right\}\right)}\right) \tag{3.67}$$

Once the measurements are recorded, (3.62), (3.64) and (3.66) are solved as simultaneous set of equations in MATLAB using *vpasolve* [155], to obtain the values of L_P, L_S and L_m. Further, substituting the obtained value of inductances and winding resistances in (3.63), (3.65), and (3.67), the set of equations are solved in MATLAB to obtain the values of $C_{str,P}, C_{str,S}$ and $C_{str,SC}$. Finally, using the values of stray capacitances obtained, the experimental values of $C_{p_{in}}, C_{s_{in}}$ and $C_{ps_{in}}$ are obtained by solving for three equations with three variables using *vpasolve*. To further validate the accuracy of the obtained parameters, the excitation frequencies are varied, and the same set of steps are repeated, thus establishing the repeatability (with a mismatch threshold of 5%) of the experimental procedure to obtain the R-L-C parameters of HFPT. As observed in Table

3.5, the FEA simulation and experimental results match the analytically calculated values with an average mismatch of 6.2% and 5.5% respectively, thus validating the model developed and analyses. Further, the experimentally measured values of winding resistance show a larger mismatch with the analytically calculated values due to the inconsistency introduced by the assumptions employed in Dowell's equation. As suggested in [65], there are several assumptions pertaining to the Dowell's equation that are ignored for reduced analytical complexity. These factors include the porosity factor [150] (included when the conductor width is comparable to its thickness leading to proximity effect in horizontal direction), distance considerations between multiple conductors turns in a single layer, distance of conductor surface from the core, and sinusoidal excitation provided to the windings. Thus, to accurately characterize the winding resistance and to observe the losses due to skin and proximity effects, the 3D FEA simulation proves to be more reliable as presented in this work. However, it is important to highlight the accuracy of the analytical calculations to obtain the values of leakage inductances and stray capacitance, as seen in Table 3.5. The accuracy obtained thereof essentially helps reduce the number of time and memory intensive iterations of FEA simulations for characterizing $L_p, L_s, C_{p_{in}}, C_{s_{in}}$ and $C_{ps_{in}}$ for different winding configurations.

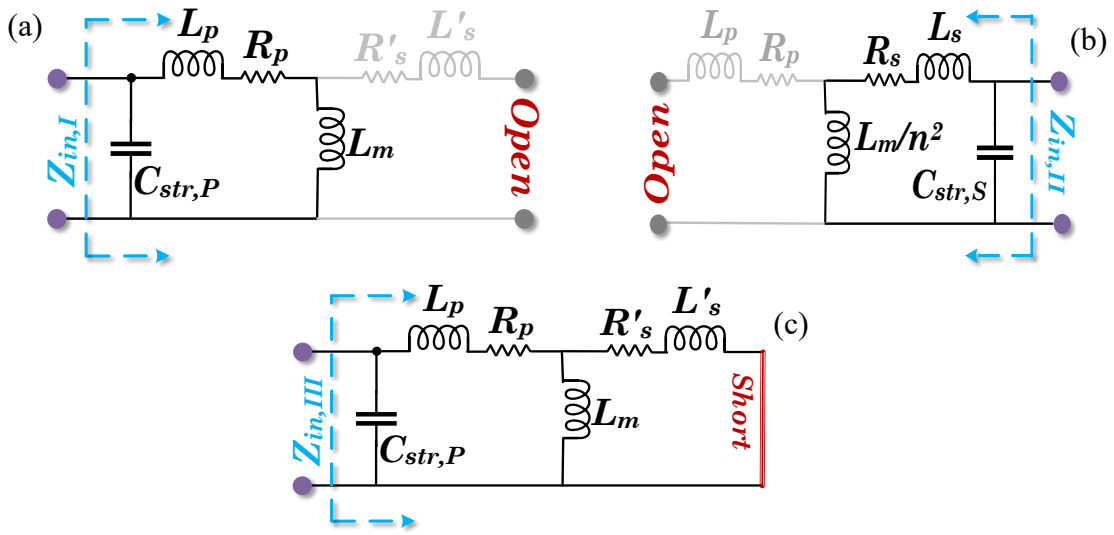


Figure 3.25: Open Circuit/Short Circuit Tests on HFPT to Experimentally Measure the R-L-C Parameters (a) Open Circuit Test with Primary Probing, (b) Open Circuit Test with Secondary Probing, (c) Short Circuit Test with Primary Probing.

Corelating the constraints for the optimum winding selection, Figure 3.26 elucidates a detailed flowchart depicting the iterative process of finding the most optimum winding configuration. As observed, based on the design specifications, the converter analysis and design phase include an iterative process of finding the optimum values of tank parameters based on factors like resultant gain dependencies, loss budget for resonant tank by enabling ZVS and SR, input impedance function and corresponding tank currents, etc. Following the design phase, as per the target tank parameters, a compatible magnetic core is selected, adhering to the requirements pertaining to rated power and the required magnetizing inductance (L_m).

The core selection follows a volumetric minimization based comparative analysis, where the following considerations pertaining to the gain-frequency trend, soft-switching criteria and dimensional constraints of the core are imposed for the design specifications mentioned in Table 3.9:

(a) The turns ratio needs to be $n = 22:1$, adhering to the near unity gain requirement at maximum operating voltages (for 600V-28V conversion). Corresponding to the current carrying capacity of a 2oz. copper trace for a 4-layer PCB, the window width should be at least 20mm with $N_{e,max} = 8$ and $N_{i,max} = 5$.

(b) Corresponding to the gain trend and ZVS requirements, the magnetizing inductance is calculated to be less than $76.26\mu H$. The airgap between the cores should be <2.5mm to prevent excessive leakage of flux from the cores.

(c) The B_{max} obtained corresponding to the turns ratio (n), area of the core (A_e), and excitation voltage should be less than the saturation flux density (B_{sat} value) of the core.

With the above-mentioned considerations, Table 3.6 compares five different planar cores [156] and analyzes the dimensions of the core, the airgap requirement to obtain the required L_m with n=22:1, corresponding B_{max} values and the core losses.

As observed in Table 3.6, the selected core FR45810EC proves to be the most ideal selection, adhering to the requirements corresponding to the window width and airgap to achieve the required L_m with n=22:1. Further, the selected core also provides an optimal tradeoff corresponding to the dimensions (the area and volume) of the core with respect to the B_{max} obtained thereof, resulting in the least amount of analytically calculated core losses**.** Please note that the comparison shown above is only targeted for the converter specifications for the presented work. However, as Figure 3.26 provides a generic flowchart for optimum HFPT design, the magnetic core selection is also included in the iterative design process.

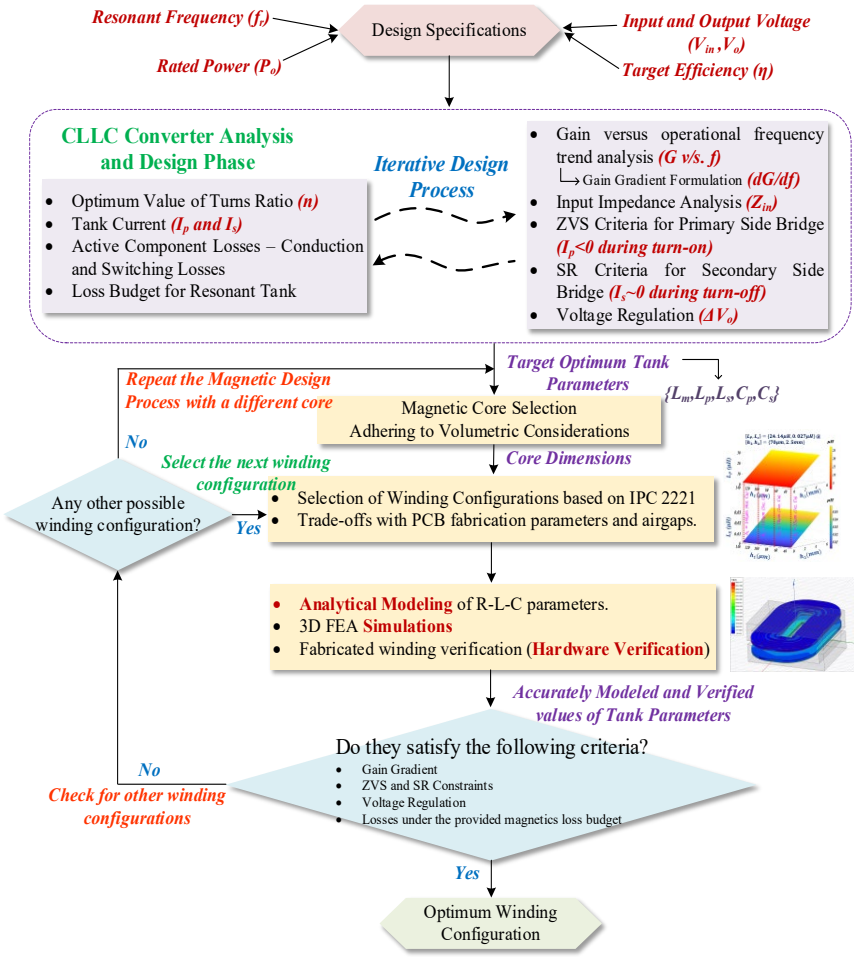


Figure 3.26: Flowchart Depicting the Process to Obtain the Most Optimum Winding Configuration.

Table 3.6: Comparison of Planar Cores for Volumetric Minimization

Relevant Ferrite Magnetic Planar Cores	Window Width (b_t)	Area of the core (A_e)	Volume of the core (V_e)	Air gap (h_g) for L_m = 76µH and n = 22:1	B_{max} for excitation voltage = 400V, and n = 22:1	Analytically calculated core loss [157]
FR43808EC	11.43mm	194mm^2	10200mm^3	1.5mm	46.8mT	5.287W
FR44310EC	13.2mm	229mm^2	13900mm^3	1.8mm	39.6mT	5.876W
FR45810EC	21.4mm	310mm^2	24600mm^3	1.9mm	29.5mT	5.221W
FR46410EC	21.8mm	516mm^2	41400mm^3	4.1mm	17.6mT	6.242W
0R49928EC	36mm	540mm^2	79800mm^3	4.25mm	16.8mT	8.385W

Further, as observed in (3.28)-(3.35), based on the core selection and the available window area, different winding configurations are formulated along with their trade-offs pertaining to the airgaps and PCB fabrication parameters. This process is followed by analytical modeling, FEA simulations and hardware verification to accurately characterize the obtained tank parameters. The optimal winding selection process is successful if the obtained tank parameters satisfy the constraints pertaining to gain gradients, soft-switching, and core losses. In addition to that, ideally for obtaining minimized winding losses, interleaved winding configurations proves to be the most feasible option. However, it is worthwhile to point out at the limitation of implementing an interleaved structure in a leakage integrated design of HFPT. As observed in the analytical calculations in Table 3.2, with verified resultant parameters shown in Table 3.5 and corresponding gain graphs in Figure 3.24(a), although the interleaved winding structure provides reduced effective winding resistance, due to negligible value of leakage inductances obtained thereof, the required gain is not achieved as required by the application. Thus, an additional inductor is required to meet the requirements of voltage gain and ZVS soft switching, which degrades the power density of the developed converter. This necessitates the criteria of checking the winding losses and ensuring them to be under the defined magnetic loss budget as seen in Figure 3.26.

If none of the possible winding structures satisfy the performance constraints, then the same process of R-L-C modeling is carried out for all possible winding configurations with different compatible magnetic cores. This iterative process facilitates the most

optimum HFPT design for a given set of design specification pertaining to a selected converter topology.

3.5. GHA Based All Inclusive Small Signal Modeling

To precisely characterize the dynamic performance of the CLLC converter model as shown in Figure 3.1 accounting for the parasitic components of the resonant tank, a comprehensive equivalent model for 'kth' harmonic is shown in Figure 3.27. This model is used to formulate the state-space equations for the circuit, which are split in their corresponding sine and cosine components using GHA based harmonic modeling. Further, the non-linear terms are linearized using the extended describing function (EDF) expansion accounting for the higher order harmonics and their effect on the system performance.

A flowchart depicting the entire small-signal modeling approach [90] is portrayed in Figure 3.28, and correspondingly detailed elucidation of system modeling is discussed as follows:

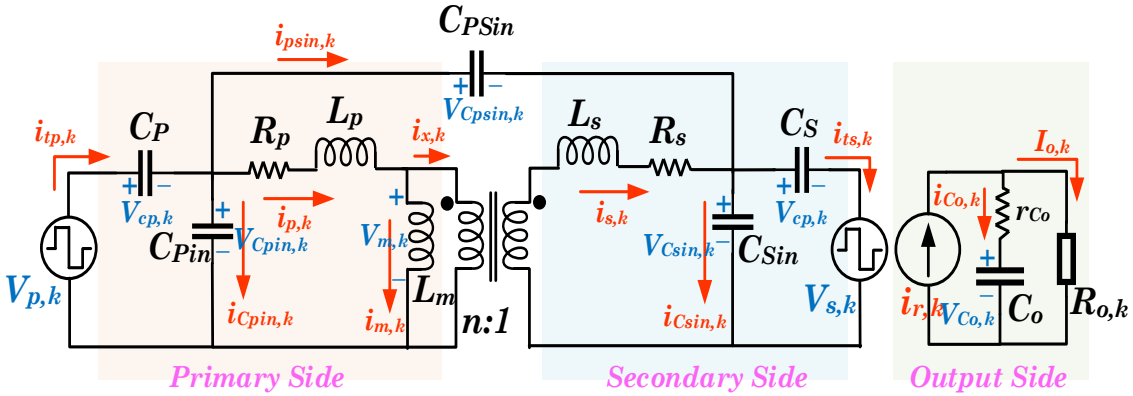


Figure 3.27: Equivalent Model of CLLC Converter Topology for k^{th} Harmonic

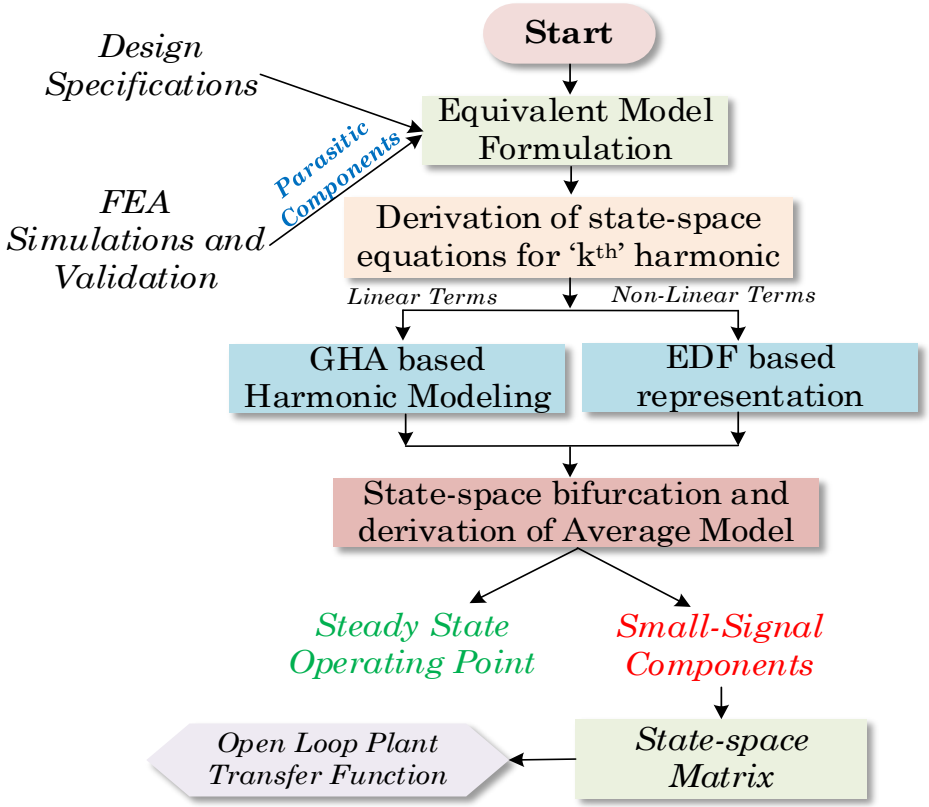


Figure 3.28: Flowchart Depicting the Small Signal Model Derivation Procedure

3.5.1. Derivation and Correlation of State-Space Equations

The set of non-linear state-space equations can be derived by utilizing the equivalent 'k^th' harmonic model.

Applying KVL in the primary side block as observed in Figure 3.27, the following relations are obtained.

$$V_{p,k}(t) = V_{C_p,k}(t) + V_{C_{p_{in}},k}(t) \tag{3.68}$$

$$V_{C_{p_{in}},k}(t) = L_p \frac{di_{p,k}(t)}{dt} + i_{p,k}(t)R_p + L_m \frac{d\left(i_{p,k}(t) - i_{x,k}(t)\right)}{dt} \tag{3.69}$$

$$\frac{1}{n}V_{m,k}(t) = i_{s,k}(t)R_s + L_s \frac{di_{s,k}(t)}{dt} + V_{C_{s_{in}},k}(t) \tag{3.70}$$

Maintaining the asymmetric nature of the tank (i.e., $L_p \neq n^2 L_s$), the following relation is obtained:

$$i_{x,k}(t) = \frac{i_{s,k}(t)}{n} \tag{3.71}$$

Further, applying KVL in the secondary side block (as seen in Figure 3.27), the following relation is obtained:

$$V_{C_{s_{in}},k}(t) = V_{C_s,k}(t) + V_{s,k}(t) \tag{3.72}$$

Simultaneously solving (3.68-3.72) and rearranging the terms, the state space equations for the primary and secondary tank current are obtained as follows.

$$\frac{di_{p,k}(t)}{dt} = \frac{V_{p,k}(t)}{L_{ss}} - \frac{i_{p,k}(t)R_p}{L_{ss}} - \frac{V_{C_p,k}(t)}{L_{ss}} + \frac{V_{s,k}(t)}{L_{mm}} - \frac{V_{C_s,k}(t)}{L_{mm}} - \frac{i_{s,k}(t)R_s}{L_{mm}} \tag{3.73}$$

$$\frac{di_{s,k}(t)}{dt} = \frac{V_{p,k}(t)}{L_{mm}} - \frac{i_{p,k}(t)R_p}{L_{mm}} - \frac{V_{C_p,k}(t)}{L_{mm}} - \frac{V_{s,k}(t)}{L_{pp}} - \frac{V_{C_s,k}(t)}{L_{pp}} - \frac{i_{s,k}(t)R_s}{L_{pp}} \tag{3.74}$$

In (3.73-3.74), the equivalent inductances can be referred as lumped primary, secondary and magnetizing forms, as follows.

$$L_{mm} = \frac{n^2 L_{es} L_{ep} - L_m^2}{nL_m} \tag{3.75}$$

$$L_{pp} = \frac{n^2 L_{es} L_{ep} - L_m^2}{n^2 L_{ep}} \tag{3.76}$$

$$L_{ss} = \frac{n^2 L_{es} L_{ep} - L_m^2}{n^2 L_{es}} \tag{3.77}$$

where, $L_{ep} = L_p + L_m$ and $L_{es} = L_s + \frac{L_m}{n^2}$

Applying KCL in Figure 3.27 to obtain the state-space equations for the resonant capacitor voltages, the following relations are obtained.

$$i_{t_p,k}(t) = C_p \frac{dV_{C_p,k}(t)}{dt} = i_{p,k}(t) + i_{ps_{in},k}(t) + i_{C_{p_{in}},k}(t) \tag{3.78}$$

$$i_{t_s,k}(t) = C_s \frac{dV_{C_s,k}(t)}{dt} = i_{s,k}(t) + i_{ps_{in},k}(t) - i_{C_{s_{in}},k}(t) \tag{3.79}$$

Further, to formulate the feasible state-space equations for the current through the parasitic capacitances ($C_{p_{in}}, C_{s_{in}}$and $C_{ps_{in}}$), trace inductances of negligible values ($L_{p_{in}}, L_{s_{in}}$and $L_{ps_{in}}$, respectively) are assumed to be connected in series [158]. Accommodating this modification in the model, the following relations are obtained:

$$i_{c_{p_{in}},k}(t) = C_{p_{in}} \frac{dV_{C_{p_{in}},k}(t)}{dt} \tag{3.80}$$

$$i_{c_{s_{in}},k}(t) = C_{s_{in}} \frac{dV_{C_{s_{in}},k}(t)}{dt} \tag{3.81}$$

$$i_{ps_{in},k}(t) = C_{ps_{in}} \frac{dV_{C_{ps_{in}},k}(t)}{dt} \tag{3.82}$$

$$V_{C_{p_{in}},k}(t) = V_{p,k}(t) - V_{C_p,k}(t) - L_{p_{in}} \frac{di_{C_{p_{in}},k}(t)}{dt} \tag{3.83}$$

$$V_{C_{s_{in}},k}(t) = V_{C_s,k}(t) + V_{s,k}(t) - L_{s_{in}} \frac{di_{C_{s_{in}},k}(t)}{dt} \tag{3.84}$$

$$V_{C_{ps_{in}},k}(t) = V_{C_{p_{in}},k}(t) + L_{p_{in}} \frac{di_{C_{p_{in}},k}(t)}{dt} - \frac{V_{C_{s_{in}},k}(t)}{n} - \frac{L_{s_{in}}}{n} \frac{di_{C_{s_{in}},k}(t)}{dt} - L_{ps_{in},k} \frac{di_{ps_{in},k}(t)}{dt} \tag{3.85}$$

Analyzing the output side block (as observed in Figure 3.27), the rectified current source can be written as follows using superposition theorem.

$$i_{r,k}(t) = \left|i_{s,k}(t)\right| = n\left|i_{x,k}(t)\right| = n\left|i_{p,k}(t) - i_{m,k}(t)\right| \tag{3.86}$$

$$i_{r,k}(t) = \frac{v_{C_o,k}(t)}{R_{o,k}} + \left(1 + \frac{r_{C_o}}{R_{o,k}}\right) C_o \frac{dv_{C_o,k}(t)}{dt} \tag{3.87}$$

Further, the output voltage equation can be formulated as follows.

$$v_{o,k}(t) = \frac{R_{o,k}}{r_{C_o} + R_{o,k}} v_{C_o,k}(t) + \left(\frac{r_{C_o} R_{o,k}}{r_{C_o} + R_{o,k}}\right) i_{r,k}(t) \tag{3.88}$$

Eq. (3.68)-(3.88) represent the set of intricately modeled state-space equations incorporating the effect of parasitic components in the system design. As observed, these equations include linear, non-linear and DC terms which can be represented using harmonic equivalent model and EDFs as shown in the following sections.

3.5.2. GHA Based Harmonic Modeling of Linear Terms in State-Space Equations

Representation of linear terms in the state-space equations like tank currents ($i_{p,k}(t)$ and $i_{s,k}(t)$), capacitor voltages ($V_{C_p,k}(t)$ and $V_{C_s,k}(t)$) and parasitic components (as shown in (13-18)) can be represented as summation of odd-order sinusoidal harmonic components. To portray the GHA based expansion of the aforementioned state-space variables, the harmonic modeling of a generic state variable $\alpha(t)$ is shown below.

$$\alpha(t) = \sum_{k=1}^{2n-1} \alpha_k(t) = \sum_{k=1}^{2n-1} \alpha_{s,k}(t) \sin k\omega_s t + \sum_{k=1}^{2n-1} \alpha_{c,k}(t) \cos k\omega_s t \quad (3.89)$$

where, $\alpha_{s,k}(t)$ and $\alpha_{c,k}(t)$ denote the sine and cosine components of harmonic expansion for the variable $\alpha(t)$. In addition to that, the term $\frac{d\alpha(t)}{dt}$ can be represented as follows:

$$\frac{d\alpha(t)}{dt} = \sum_{k=1}^{2n-1} \frac{d\alpha_k(t)}{dt} = \sum_{k=1}^{2n-1} \left(\frac{d\alpha_{s,k}(t)}{dt} - k\omega_s \alpha_{c,k}(t) \right) \sin k\omega_s t + \sum_{k=1}^{2n-1} \left(\frac{d\alpha_{c,k}(t)}{dt} + k\omega_s \alpha_{s,k}(t) \right) \cos k\omega_s t \quad (3.90)$$

Utilizing (3.89-3.90), the linear terms in state-space equations can be expanded to denote their sine and cosine components, thus elucidating their phase and magnitude for each k^{th} harmonic component.

3.5.3. Extended Describing Function (EDF) Based Representation of Non-Linear Terms in State-Space Equations

Due to the inherent non-linear behavior of state-variables - $V_{p,k}(t), V_{s,k}(t)$and $i_{r,k}(t)$, EDF based representation is used that essentially is depicted using Fourier series expansion. The primary bridge voltage $V_{p,k}(t)$ is assumed to be the main excitation source of the system and it is thus chosen as a reference for denoting the phase relation with respect to other state variables. Further, adhering to the quasi-square wave nature of $V_{p,k}(t)$, only odd-order harmonics are considered for EDF representation, as shown below:

$$V_{p,k} = \sum_{k=1}^{2n-1} \left|v_{p,k}\right| \sin k\omega_s t \tag{3.91}$$

where, $\left|v_{p,k}\right| = \frac{4V_{in}}{k\pi} \sin\left(\frac{\pi\delta}{2}\right)$ and δ is the operational duty ratio of the primary bridge.

Similarly, the secondary bridge voltage can be represented using the following describing function:

$$V_{s,k} = \sum_{k=1}^{2n-1} \left|v_{s,k}\right| \frac{\sin k(\omega_s t - \varphi_g)}{k} = \frac{4nV_o}{\pi} \sum_{k=1}^{2n-1} \frac{\sin k(\omega_s t - \varphi_g)}{k} \tag{3.92}$$

where, φ_g denotes the angle of voltage gain expression for the CLLC network.

However, on account of the synchronous rectification (SR) [80] algorithm to obtain turn-off current minimization (included as a part of the hybrid control scheme explained in Section – IV), it is observed that the magnitude of secondary bridge voltage is dependent on the polarity of the secondary tank current, which is depicted in the following relation:

$$V_{s,k} = \begin{cases} v_{o,k}; & i_{s,k} > 0 \\ -v_{o,k}; & i_{s,k} < 0 \end{cases} \tag{3.93}$$

Equation (3.93) can be rearranged to obtain the describing function for secondary bridge voltage as follows.

$$V_{s,k} = sgn(i_{s,k})v_{o,k} \tag{3.94}$$

$$V_{s,k} = \sum_{k=1}^{2n-1} v_{s,k}(t) = \sum_{k=1}^{2n-1} \frac{4}{\pi}\frac{i_{s_s,k}v_{C_o,k}}{ki_{sT,k}} \sin k\omega_s t + \sum_{k=1}^{2n-1} \frac{4}{\pi}\frac{i_{s_c,k}v_{C_o,k}}{ki_{sT,k}} \cos k\omega_s t \tag{3.95}$$

where, $i_{sT,k}$ denotes the cumulative peak value of secondary tank current, and can be depicted as follows:

$$i_{sT,k} = \sqrt{i_{s_s,k}^2 + i_{s_c,k}^2} \tag{3.96}$$

Further using (3.96), the non-linear rectified output current state-variable can be formulated as follows:

$$i_{r,k} = \sum_{k=1}^{2n-1} |i_{s,k}| = \frac{2}{\pi}\sum_{k=1}^{2n-1} i_{sT,k} \tag{3.97}$$

Using (3.91-3.97), the non-linear terms are converted to their equivalent system of approximated linearized equations. This is quintessential for carrying out the orthogonal component split (encompassing the information about the magnitude and phase) of the state-space variables.

3.5.4. Orthogonal Component Split-Based State-Space Harmonic Modeling

Utilizing the describing functions (3.91-3.93) to replace the non-linear terms and GHA based harmonic modeling (3.89-3.90) to replace the linear terms in the state-space equations derived in (3.68-3.88), the overall equivalent circuit can be written in the form

of sets of sine and cosine (s and c respectively) terms. For achieving orthogonal decomposition of state-space equations, the following variables are used:

$$\xi = [s, c] \tag{3.98}$$

$$\Upsilon = \begin{cases} 1; & \xi = s \\ -1; & \xi = c \end{cases} \tag{3.99}$$

$$\sigma = \begin{cases} 1; & \xi = s \\ 0; & \xi = c \end{cases} \tag{3.100}$$

Utilizing (3.98-3.100), the resultant linearized state-space equation set for primary and secondary block (referred to Fig. 2) can be expressed as follows:

$$\frac{di_{p_\xi}}{dt} = \sum_{k=1}^{2n-1} \frac{di_{p_{\xi,k}}}{dt} = -\frac{1}{L_{mm}} \sum_{k=1}^{2n-1} \left(\frac{4}{\pi} \frac{i_{s_{\xi,k}} v_{C_{o,k}}}{k i_{sT,k}} \right) - \frac{1}{L_{ss}} \sum_{k=1}^{2n-1} V_{C_{p_{\xi,k}}} -$$

$$\frac{1}{L_{mm}} \sum_{k=1}^{2n-1} V_{C_{s_{\xi,k}}} - \frac{R_p}{L_{ss}} \sum_{k=1}^{2n-1} i_{p_{\xi,k}} - \frac{R_s}{L_{mm}} \sum_{k=1}^{2n-1} i_{s_{\xi,k}} + \sigma \frac{1}{L_{ss}} \sum_{k=1}^{2n-1} \left| v_{p,k} \right| +$$

$$\Upsilon \sum_{k=1}^{2n-1} k\omega_s \, i_{p_{\xi,k}} \tag{3.101}$$

$$\frac{di_{s_\xi}}{dt} = \sum_{k=1}^{2n-1} \frac{di_{s_{\xi,k}}}{dt} = -\frac{1}{L_{pp}} \sum_{k=1}^{2n-1} \left(\frac{4}{\pi} \frac{i_{s_{\xi,k}} v_{C_{o,k}}}{k i_{sT,k}} \right) - \frac{1}{L_{mm}} \sum_{k=1}^{2n-1} V_{C_{p_{\xi,k}}} -$$

$$\frac{1}{L_{pp}} \sum_{k=1}^{2n-1} V_{C_{s_{\xi,k}}} - \frac{R_p}{L_{mm}} \sum_{k=1}^{2n-1} i_{p_{\xi,k}} - \frac{R_s}{L_{pp}} \sum_{k=1}^{2n-1} i_{s_{\xi,k}} + \sigma \frac{1}{L_{mm}} \sum_{k=1}^{2n-1} \left| v_{p,k} \right| +$$

$$\Upsilon \sum_{k=1}^{2n-1} k\omega_s \, i_{s_{\xi,k}} \tag{3.102}$$

$$\frac{dv_{C_{p_\xi}}}{dt} = \sum_{k=1}^{2n-1} \frac{dV_{C_{p_{\xi,k}}}}{dt} = \frac{1}{C_p} \sum_{k=1}^{2n-1} i_{p_{\xi,k}} + \frac{1}{C_p} \sum_{k=1}^{2n-1} i_{ps_{in_{\xi,k}}} + \frac{1}{C_p} \sum_{k=1}^{2n-1} i_{C_{p_{in_{\xi,k}}}} +$$

$$\Upsilon \sum_{k=1}^{2n-1} k\omega_s \, V_{C_{p_{\xi,k}}} \tag{3.103}$$

$$\frac{dv_{C_{s_\xi}}}{dt} = \sum_{k=1}^{2n-1} \frac{dV_{C_{s_{\xi,k}}}}{dt} = \frac{1}{C_s} \sum_{k=1}^{2n-1} i_{s_{\xi,k}} + \frac{1}{C_s} \sum_{k=1}^{2n-1} i_{ps_{in_{\xi,k}}} - \frac{1}{C_s} \sum_{k=1}^{2n-1} i_{C_{s_{in_{\xi,k}}}} +$$

$$\Upsilon \sum_{k=1}^{2n-1} k\omega_s \, V_{C_{s_{\xi,k}}} \tag{3.104}$$

$$\frac{dV_{C_{p_{in\xi}}}}{dt} = \sum_{k=1}^{2n-1} \frac{dV_{C_{p_{in\xi'},k}}}{dt} = \frac{1}{C_{p_{in}}} \sum_{k=1}^{2n-1} i_{C_{p_{in\xi'},k}} + \Upsilon \sum_{k=1}^{2n-1} k\omega_s V_{C_{p_{in_c},k}} \quad (3.105)$$

$$\frac{dV_{C_{s_{in\xi}}}}{dt} = \sum_{k=1}^{2n-1} \frac{dV_{C_{s_{in\xi'},k}}}{dt} = \frac{1}{C_{s_{in}}} \sum_{k=1}^{2n-1} i_{C_{s_{in\xi'},k}} + \Upsilon \sum_{k=1}^{2n-1} k\omega_s V_{C_{s_{in_c},k}} \quad (3.106)$$

$$\frac{dV_{C_{ps_{in\xi}}}}{dt} = \sum_{k=1}^{2n-1} \frac{dV_{C_{ps_{in\xi'},k}}}{dt} = \frac{1}{C_{ps_{in}}} \sum_{k=1}^{2n-1} i_{ps_{in_{\xi'},k}} + \Upsilon \sum_{k=1}^{2n-1} k\omega_s V_{ps_{in_c},k} \quad (3.107)$$

$$\frac{di_{C_{p_{in\xi}}}}{dt} = \sum_{k=1}^{2n-1} \frac{di_{C_{p_{in\xi'},k}}}{dt} = \sigma \frac{1}{L_{p_{in}}} \sum_{k=1}^{2n-1} |v_{p,k}| - \frac{1}{L_{p_{in}}} \sum_{k=1}^{2n-1} V_{C_{p_{\xi'},k}} -$$

$$\frac{1}{L_{p_{in}}} \sum_{k=1}^{2n-1} V_{C_{p_{in\xi'},k}} + \Upsilon \sum_{k=1}^{2n-1} k\omega_s i_{C_{p_{in\xi'},k}} \quad (3.108)$$

$$\frac{di_{C_{s_{in\xi}}}}{dt} = \sum_{k=1}^{2n-1} \frac{di_{C_{s_{in\xi'},k}}}{dt} = \frac{1}{L_{s_{in}}} \sum_{k=1}^{2n-1} V_{C_{s_{\xi'},k}} - \frac{1}{L_{s_{in}}} \sum_{k=1}^{2n-1} V_{C_{s_{in\xi'},k}} -$$

$$\frac{1}{L_{s_{in}}} \sum_{k=1}^{2n-1} \left(\frac{4}{\pi} \frac{i_{s_{\xi',k}} v_{C_{o,k}}}{k i_{sT,k}} \right) + \Upsilon \sum_{k=1}^{2n-1} k\omega_s i_{C_{p_{in\xi'},k}} \quad (3.109)$$

$$\frac{di_{ps_{in\xi}}}{dt} = \sum_{k=1}^{2n-1} \frac{di_{ps_{in\xi'},k}}{dt} = \sigma \frac{1}{L_{ps_{in}}} \sum_{k=1}^{2n-1} |v_{p,k}| - \frac{1}{L_{ps_{in}}} \sum_{k=1}^{2n-1} V_{C_{p_{\xi'},k}} -$$

$$\frac{1}{L_{ps_{in}}} \sum_{k=1}^{2n-1} V_{C_{ps_{in\xi'},k}} - \frac{1}{nL_{ps_{in}}} \sum_{k=1}^{2n-1} V_{C_{s_{\xi'},k}} - \frac{1}{nL_{ps_{in}}} \sum_{k=1}^{2n-1} \left(\frac{4}{\pi} \frac{i_{s_{\xi',k}} v_{C_{o,k}}}{k i_{sT,k}} \right) +$$

$$\Upsilon \sum_{k=1}^{2n-1} k\omega_s i_{ps_{in_{\xi'},k}} \quad (3.110)$$

Similarly, the DC terms obtained from the output side block can be formulated as follows:

$$C_o \sum_{k=1}^{2n-1} \frac{dv_{C_o,k}}{dt} = \frac{2}{\pi} \sum_{k=1}^{2n-1} i_{sT,k} \frac{R_{o,k}}{k(R_{o,k}+r_{C_o})} - \sum_{k=1}^{2n-1} \frac{v_{C_o,k}}{R_{o,k}+r_{C_o}} \quad (3.111)$$

$$V_o = \sum_{k=1}^{2n-1} v_{o,k} = \frac{2}{\pi} \sum_{k=1}^{2n-1} i_{sT,k} \frac{R_{o,k} r_{C_o}}{k(R_{o,k}+r_{C_o})} - \sum_{k=1}^{2n-1} v_{C_o,k} \frac{R_{o,k}}{R_{o,k}+r_{C_o}} \quad (3.112)$$

Using the orthogonally decomposed set of state-space equations, an all-inclusive small-signal model incorporating all the harmonic frequency components developed in the following section.

3.5.5. All-Inclusive Small-Signal Modeling

The set of linearized state-space equations can be analyzed in an average domain to yield the large signal model of the all-inclusive CLLC model, which includes the steady state operating point of the state-variable and a small-signal equivalent component [89-90].

$$\{\alpha_k(t)\}_{avg} = \alpha_k + \widehat{\alpha_k} \tag{3.113}$$

From (3.113), it is observed that the formulation of the average of state-variable $\alpha_k(t)$ corresponding to k[th] harmonic over a switching cycle (i.e., $\{\alpha_k(t)\}_{avg}$) can be written as a summation of a steady state operating point α and its small signal term ($\widehat{\alpha_k}$). Similarly, the average switching frequency can be also written as a combination of the steady state switching frequency (Ψ) and its small signal equivalent term ($\widehat{\omega_n}$).

$$\left\{\omega_{s,k}\right\}_{avg} = k\Psi + k\omega_o\widehat{\omega_n} \tag{3.114}$$

where, ω_o is the resonant frequency selected as per the design specifications. As observed in (3.101-3.102, 3.109-3.110), the non-linear terms can be further linearized around their averaged values as follows:

$$\frac{\left\{i_{s_\xi,k}\right\}_{avg}\left\{v_{C_o,k}\right\}_{avg}}{\left\{i_{sT,k}\right\}_{avg}} = \frac{I_{s_\xi,k}V_{C_o,k}}{I_{sT,k}} + \frac{I_{S_\xi}}{I_{sT,k}}\widehat{v_{C_o,k}} + \frac{I_{S_c,k}^2 V_{C_o,k}}{I_{sT,k}^3}\widehat{\imath_{s_\xi,k}} - \frac{I_{s_\xi,k}I_{s_{\xi'},k}V_{C_o,k}}{I_{sT,k}^3}\widehat{\imath_{s_{\xi'},k}} \tag{3.115}$$

$$\left\{i_{sT,k}\right\}_{avg} = I_{sT,k} + \frac{I_{s_S,k}}{I_{sT,k}}\widehat{\imath_{s_S,k}} + \frac{I_{s_C,k}}{I_{sT,k}}\widehat{\imath_{s_C,k}} \tag{3.116}$$

In addition to that, the small signal equivalent for the input voltage term can be written as follows:

$$\left|\widehat{v_{p,k}}\right| = \frac{4}{k\pi}\sin\left(\frac{\pi}{2}\delta\right)\widehat{V_{in}} + \frac{2V_{in}}{k}\cos\left(\frac{\pi}{2}\delta\right)\hat{\delta} \tag{3.117}$$

Using the above-mentioned modifications and extracting the small-signal dependent terms, the proposed all-inclusive GHA based small-signal model is obtained in the form of state-space equation pairs as follows:

$$\frac{d\hat{x}}{dt} = A_k \cdot \hat{x} + B_k \cdot \hat{u} \tag{3.118}$$

$$\hat{y} = C_k \cdot \hat{x} + D_k \cdot \hat{u} \tag{3.119}$$

$$\hat{x} = [\widehat{\imath_{p_s,k}}\ \widehat{\imath_{p_c,k}}\ \widehat{\imath_{s_s,k}}\ \widehat{\imath_{s_c,k}}\ \widehat{V_{C_{p_s},k}}\ \widehat{V_{C_{p_c},k}}\ \widehat{V_{C_{s_s},k}}\ \widehat{V_{C_{s_c},k}}\ \widehat{V_{C_{p_{in_s}},k}}$$

$$\widehat{V_{C_{p_{in_c}},k}}\ \widehat{V_{C_{s_{in_s}},k}}\ \widehat{V_{C_{s_{in_c}},k}}\ \widehat{V_{C_{ps_{in_s}},k}}\ \widehat{V_{C_{ps_{in_c}},k}}\ \widehat{\imath_{C_{p_{in_s}},k}}\ \widehat{\imath_{C_{p_{in_c}},k}}$$

$$\widehat{\imath_{C_{s_{in_s}},k}}\ \widehat{\imath_{C_{s_{in_c}},k}}\ \widehat{\imath_{ps_{in_s},k}}\ \widehat{\imath_{ps_{in_c},k}}\ \widehat{V_{C_o,k}}]^T \tag{3.120}$$

$$\hat{u} = [\widehat{\omega_n}\ \ \widehat{V_{in}}\ \ \hat{\delta}] \tag{3.121}$$

$$\hat{y} = \widehat{V_{o,k}} \tag{3.122}$$

Corresponding to all the 21 state variables, A_k represents the system matrix and portrays a 21x21 matrix structure incorporating relation between the small-signal representations of all the state-space variables and the system design parameters, where all the non-zero coefficients of the matrices are listed in the Appendix section. Please note, $A_{m:n,k}$ denotes the m^{th} row and n^{th} column coefficient of A_k matrix. Further, B_k denotes the input matrix and establishes the relation between the perturbation terms (shown in $\hat{u}$) and the state variables and C_k matrix represents the output matrix and denotes the relation between the output vector $\hat{y}$ and state-space variable vector $\hat{x}$. The coefficients of B_k and

C_k matrices are also shown in the Appendix section. Further, D_k is zero matrix with 3x1 structure.

The proposed small-signal model provides flexibility to the designer to achieve output voltage control by modulating not only the frequency (i.e., implementing PFM control), but also the primary bridge duty ratio through PWM control implementation [159-164]. However, the targeted controller application in this study is based on frequency modulation only; therefore, the open-loop plant transfer function corelating the small-signal perturbation in output voltage $\widehat{V_{o,k}}$ with respect to perturbation in operational frequency $\widehat{\omega_n}$ for a 'kth' harmonic can be expressed as follows.

$$G_{p,k}(s) = \frac{\widehat{V_{o,k}}}{\widehat{\omega_n}} = C_k(sI - A_k)^{-1}B_{k,(m:1)} \tag{3.123}$$

where, $B_{k,(m:1)}$ represents the first column of the B_k matrix as the perturbation is only realized for $\widehat{\omega_n}$ terms.

Pertaining to the GHA based small-signal modeling, the overall plant transfer function, denoting change in output voltage with respect to modulation in the switching frequency, can be modeled to be the summation of plant responses from k simultaneous plant gains as shown in Figure 3.29. As observed, GHA model considers all the frequencies ranging from its fundamental component (k=1) to (k=2n-1), thereby tracking the change in the output voltage using the summation of all the resultant output voltage perturbations corresponding to each harmonic component ($\widehat{V_{o,1}}, \widehat{V_{o,3}}, \dots, \widehat{V_{o,2n-1}}$), by processing the small signal perturbations in the corresponding order frequencies ($\widehat{\omega_n}, 3\widehat{\omega_n}, \dots, (2n-1)\widehat{\omega_n}$) through the plant transfer functions ($G_{p,1}(s), G_{p,3}(s), \dots, G_{p,2n-1}(s)$) respectively as

observed in (3.125-3.126). The resultant perturbation in the operational frequency can be decomposed as shown below:

$$\widehat{\omega_{n_{GHA}}} = \widehat{\omega_n} + 3\widehat{\omega_n} + \cdots + (2n-1)\widehat{\omega_n} \tag{3.124}$$

Utilizing (3.124), the effective perturbation in output voltage can be formulated as follows:

$$\widehat{V_o} = \widehat{V_{o,1}} + \widehat{V_{o,3}} + \cdots + \widehat{V_{o,2n-1}} \tag{3.125}$$

$$= \widehat{\omega_n} \cdot G_{p,1}(s) + 3\widehat{\omega_n} \cdot G_{p,3}(s) + \cdots + (2n-1)\widehat{\omega_n} \cdot G_{p,2n-1}(s) \tag{3.126}$$

On the contrary, an FHA derived model would have only considered the $G_{p,1}(s)$ plant response, which refers to the following formulation:

$$\widehat{V_o} = \widehat{\omega_n} \cdot G_{p,1}(s) \tag{3.127}$$

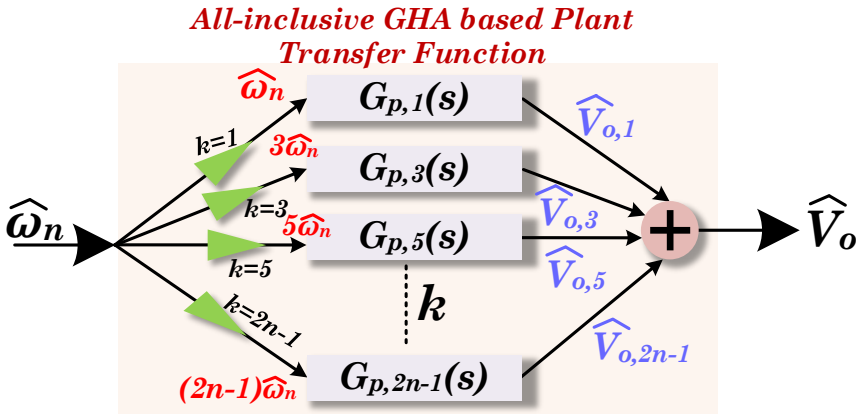


Figure 3.29: GHA Based Plant Transfer Block Diagram

Comparing (3.126) and (3.127), one can observe that the GHA based model involves significant contribution of higher order harmonic components in the modelling approach, thus providing the designer valuable insights on the selection of the corresponding controller parameters. Further, this influence is prominently explained with an illustrative comparison of the open-loop plant response, as seen in Figure 3.30 (a), that

compares the open loop frequency response obtained using the proposed all-inclusive GHA based plant model (number of harmonics: k=11) with the conventional FHA based plant model without parasitics.

As observed, the crossover frequency ω_c for an FHA based plant model (2MHz) is shifted by a factor of ~5 as compared to the proposed all-inclusive GHA based model (10.22MHz). Further, exclusion of the parasitics from the small-signal model restricts the designer to accurately attenuate the higher order frequency components due to incomplete information obtained with respect to the system practical crossover frequency. This concept is illustrated by Figure 3.30 (b), where the FHA open loop plant response is compared with its GHA counterpart obtained with/without inclusion of parasitic components in the model. Based on the response obtained in Figure 3.30 (b), the comparison of the crossover frequency shift due to adoption of the GHA approach in affiliation with the parasitics involved in the model is summarized in Table 3.7. As observed, as the model inculcates the GHA based approach, with increasing number of parasitics involved in the modelling, the crossover frequency tends to shift to a higher value, thus incorporating the effect of additional poles/zeros added thereof.

Table 3.7: Variation in the Crossover Frequency for Increasing Order of Parasitics Included in the Small-Signal Model

Model	Crossover frequency	% Variation from FHA derived model
FHA	2MHz	–
GHA without parasitics	4.98MHz	149%
GHA with R_p, R_s only	6.24MHz	212%
All-inclusive GHA	10.22MHz	411%

(a)

(b)

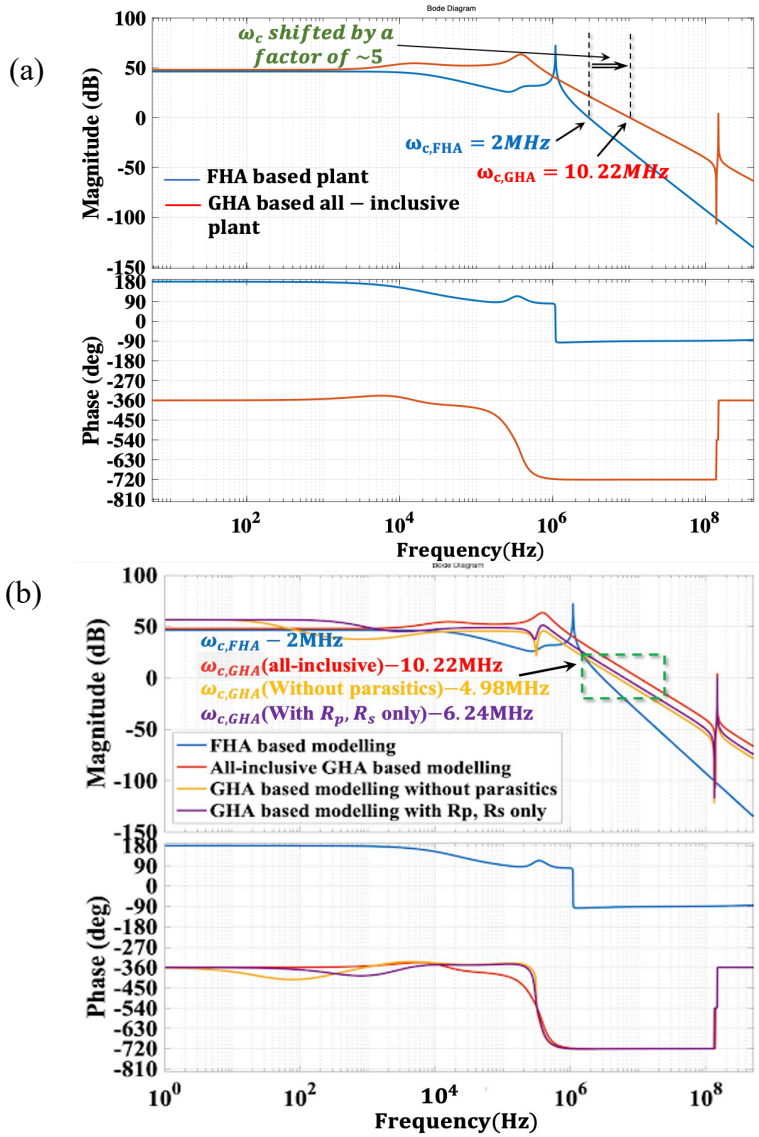


Figure 3.30: (a) Open Loop Frequency Response Comparison for Proposed GHA based All-Inclusive Plant and Conventional FHA Based Plant Without Parasitics (b) Open Loop Plant Response Comparison to Elucidate the Effect of Inclusion of Parasitic Components in the Small-Signal Model

Considering an instance for designing a compensator system using the FHA model, let us assume that the closed loop crossover frequency is selected to be 60kHz with an aim to attenuate the high frequency noise [81]. However, in practical scenario, due to the presence of parasitic components, the real value of ω_c for the compensator will also tend

to shift by a factor of 5, to approximately 300kHz. This shift in ω_c will cause the compensator to pick up high frequency noise, proving to be a potential cause of instability in the system. This phenomenon can be prevented by characterizing the system accurately using the proposed all-inclusive GHA based model. Although, the inclusion of higher order frequency components and the parasitics in a practical system makes the small signal model complex, the designer would be able to account for the mislaid corner frequencies and synthesize the corresponding controller adhering to the compensation required in a practical CLLC converter, thus resulting in a well-rounded robust system design.

To ascertain the accuracy of the GHA based all-inclusive small-signal model, a simulation study is carried out in MATLAB Simulink, where a chirp [165-166] frequency perturbation is superimposed to the operational frequency, and the perturbation observed in the output voltage ($\widehat{V_o}$) is recorded using frestimate function of MATLAB, as seen in Figure 3.31 (a). Further, the recorded values of $\widehat{V_o}$ in (dB) are plotted against the applied perturbations using logarithmic scale and compared with the all-inclusive GHA based small-signal frequency response, as shown in Figure 3.31 (b). Further, the recorded values of $\widehat{V_o}$ in (dB) are plotted against the applied perturbations using logarithmic scale and compared. As observed, the analytically derived model frequency response follows the simulated model very closely with an average mismatch of <2%, thus justifying the accuracy of the GHA model. This minor mismatch is primarily attributed toward the limitation in the order of harmonics considered for analytical modelling, where the harmonic order was restricted within k=11.

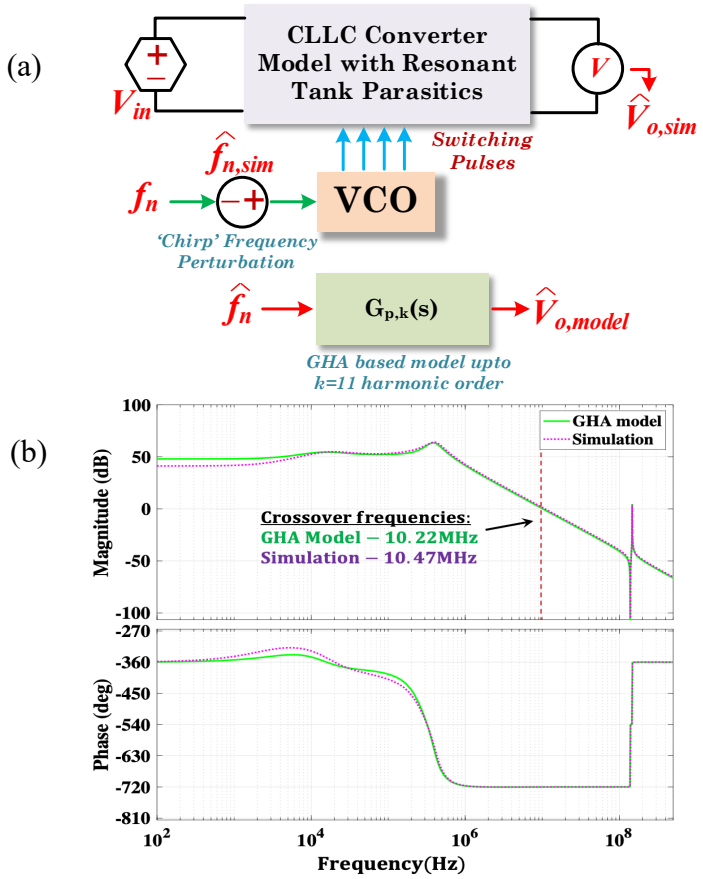


Figure 3.31: Simulation Based Verification of Derived Small Signal Model (a) Simulation Model (b) Plant Response Comparison

Further, the resonant parameters and the output capacitor ESR portray parameter variations due to their characteristics and observe a change in their resultant values with variations in temperature, operating conditions, core/winding air gaps, and PCB layout [142,167-168]. Thus, it becomes quintessential to analyze the effect of these parameter variations with respect to change in the open loop plant gain response obtained from the derived GHA based small-signal model. To elucidate this change, a sensitivity term ($S_N^{\omega_{C_f}}$) [131] is introduced herewith, that refers to the relative change in the crossover frequency with respect to relative variation in parameter N.

$$S_N^{\omega_{C_f}} = \frac{\Delta\omega_{C_f}/\omega_{C_f}}{\Delta N/N} \tag{3.128}$$

To elucidate this phenomenon, Figure 3.32 (a)-(e) shows the open-loop plant gain response of derived GHA based model by varying $L_m, L_p, L_s, C_p, C_s, R_p, R_s, C_{pin}, C_{sin}, C_{psin}, r_{C_o}$ by $\pm 10\%$ and compares their individual crossover frequencies with respect to the nominal parameters analyzed in Table 3.5. Further, based on the obtained plant responses, Table 3.8 computes the $S_N^{\omega_{C_f}}$ term for each case. The crossover frequency variations for a $\pm 10\%$ change in resonant tank parameters, as seen in Figure 3.32, portray maximum deviation of 1.71MHz (due to +10% variation in L_p) from the crossover frequency obtained by the nominally analyzed parameters. Further, to ensure robustness of the derived plant model and corresponding compensator, the closed loop SMC based controller is designed to adhere to the worst-case crossover frequency i.e, 8.51MHz, thus ensuring accurate compensation provided to attenuate the higher order frequency components, while maintaining a positive phase margin to ensure the closed loop stability and superior EMI performance.

Table 3.8: Selectivity of Crossover Frequency with Respect to Tank Parameters

N Sensitivity	L_m	L_p	L_s	C_p	C_s	R_p	R_s	C_{pin}
$S_N^{\omega_{C_f}}$	0.342	−1.673	0.254	−1.654	−0.025	−1.555	−0.024	−1.643

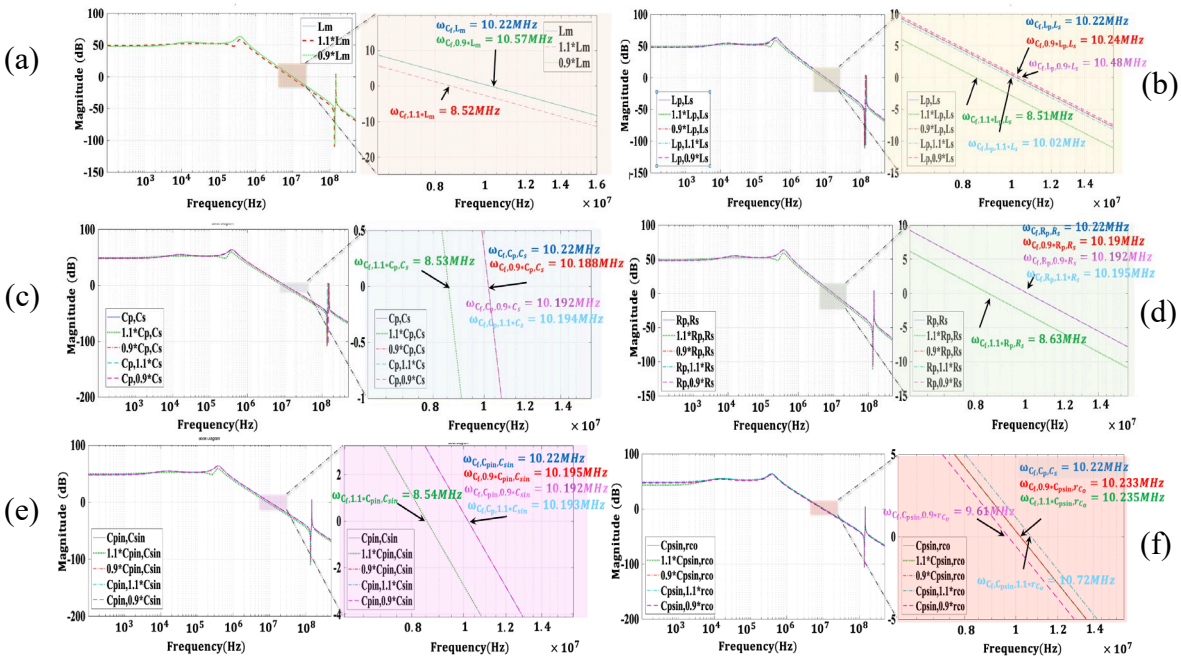


Figure 3.32: Gain Response for ±10% Variation in Stray Parameters (a) L_m, (b) L_p,L_s, (c) C_p,C_s, (d) R_p,R_s, (e) C_{pin},C_{sin}, (f) C_{psin},r_{C_o}

With the knowledge of the accurately model plant transfer function ($G_p(s)$), the closed loop controller design to provide the required compensation at the output, obtained through a hybrid SMC based controller is explained in the following section.

3.6. Proposed SMC based Hybrid Control Scheme

With an objective to attain tightly regulated voltage output yielding superior dynamic performance against sudden changes in load, along with an additional constraint of achieving significantly reduced turn-off losses in the secondary bridge, this section comprehensively elucidates the modeling and implementation of a SMC based hybrid control scheme.

3.6.1. Defining the Sliding Surface

To control the output voltage V_o, the sliding surface function can be defined as a linear combination of system variables as shown below:

$$S = M_1(V_{oe}(t)) + M_2 \int_0^t V_{oe}(t)\, dt \tag{3.129}$$

where, V_{oe} denotes the instantaneous error between the reference and the sensed output voltage and M_1 and M_2 are the sliding surface coefficients.

$$V_{oe}(t) = V_o^{ref} - V_o(t) \tag{3.130}$$

where, V_o^{ref} is the set reference voltage. The coefficients M_1 and M_2 are defined to provide the necessary bandwidth and phase margin offered by the controller at steady state operation, which necessitates the following relation:

$$\dot{S} = \frac{dS}{dt} = 0 \tag{3.131}$$

$$\dot{S} = -M_1\dot{V}_o + M_2 V_{oe} \tag{3.132}$$

where, $\dot{V}_o = \frac{dV_o(t)}{dt}$

Converting the sliding mode function in frequency *'s'* domain, the steady state value of output voltage (V_o^{SS}) and its correlation with the sliding mode coefficients is obtained as follows:

$$\dot{S}(s) = 0 = -M_1 s V_o^{SS}(s) + M_2 \frac{V_o^{ref}}{s} - M_2 V_o^{SS}(s) \tag{3.133}$$

$$V_o^{SS}(s) = \frac{M_2 V_o^{ref}}{s(M_1 s + M_2)} \tag{3.134}$$

Optimal selection of M_1 and M_2 with adequate consideration of system dynamic performance at a particular operational frequency ($s = j\omega$), (3.134) provides the

information regarding the magnitude and phase of the output voltage at steady state, thus indicating the steady state error of the controller, when compared to V_o^{ref}.

3.6.2. Practical Constraints of SMC Implementation

At steady state condition, the sliding surface functions (S and $\dot{S}$) are tuned to be zero, which forces the dynamic state of the converter to evolve around the sliding surface *S*. Correlating the desired steady state performance, the following constraint [169] is enforced to implement the sliding surface control:

$$S \cdot \dot{S} < 0 \tag{3.135}$$

Referring to the above-mentioned constraint, a control variable ζ is used for implementing the switching logic in a digital microcontroller unit (MCU). The conditions of switching are defined as follows.

$$\zeta = \begin{cases} 1; & S > 0 \\ 0; & S < 0 \end{cases} \tag{3.136}$$

When V_o is lesser than V_o^{ref}, the value of S is positive and correspondingly, the value of ζ is set to 1, which indicates a step size increase ($\Delta\omega$) in the switching frequency. Similarly, when V_o exceeds the reference V_o^{ref}, the sliding function S is negative and thus, the value of ζ is set to 0, indicating $\Delta\omega$ reduction in the operating frequency. However, in practical cases, it is important to restrict $\Delta\omega$ within reasonable boundaries, thus preventing a permanent damage on account of undesired noise and glitches in the feedback signals. Thus, a hysteresis-based controller logic is defined which replaces the previously framed condition (3.137), as shown below.

$$\zeta = \begin{cases} 1; & S > \rho \\ 0; & S < \rho \end{cases} \tag{3.137}$$

Where ρ represents the defined error band for the sliding surface. The sliding region is constrained between the defined limits (2ρ) that effectively corresponds to the acceptable steady state error of the output voltage. Corresponding to the referred application in this study, the value of ρ is selected to be 1% Further, the value of $\Delta\omega$ is selected based on the resolution of frequency modulation of the selected digital signal processor (DSP) based controller – TMS320F28379D, which is dependent on the ADC interrupt time duration and system clock synchronized output (which is a scalable factor of 200MHz system clock). In that context, a unitary change in the value of TBPRD register of EPWM sub-routine, the change in the operating frequency is observed to be 1.2kHz, which is selected to be the most appropriate value for $\Delta\omega$ with respect to each sensed sample.

3.6.3. Settling Time and Overshoot/Undershoot Constraints

For quantifying the SMC controller parameters to obtain a well-regulated output voltage, it is essential to necessitate boundary conditions for M_1 and M_2 based on the dynamic performance, corresponding to the settling time and overshoot error constraints imposed.

Figure 3.33 (a) shows a typical trend of output voltage settling observed during start-up or a dynamic load change, which portrays a settling time of τ_s and a peak overshoot of Δv_{os}. Please note that the definition of settling time in context of SMC based control is referred as the time taken by the average value of the voltage signal to settle back to its pre-defined acceptable band, that is decided by the designer. Corresponding to that, the

trend of $V_{oe}(t)$ with respect to time (t) as observed by the controller observes an exponentially decaying slope (Figure 3.33 (b)), which is formulated as follows:

$$V_{oe}(t) = V_{oe,initial} e^{-\frac{M_2}{M_1}t} \tag{3.138}$$

where, $V_{oe,intial}$ depicts the error at $t \to 0$, which can be either at the start-up or just before the load change. Dissecting (3.138) to obtain the relation between the required settling time τ_s and the SMC coefficients for x% settling band for the required output voltage, the following relation is obtained:

$$\frac{x}{100} V_o^{ref} > V_{oe,initial} e^{-\frac{M_2}{M_1}\tau_s} \tag{3.139}$$

$$\tau_s > \frac{M_1}{M_2}(4.605 - \log_e x) \tag{3.140}$$

Please note, the above constraint is only valid for asymptotically stable systems, portraying a decaying error characteristic.

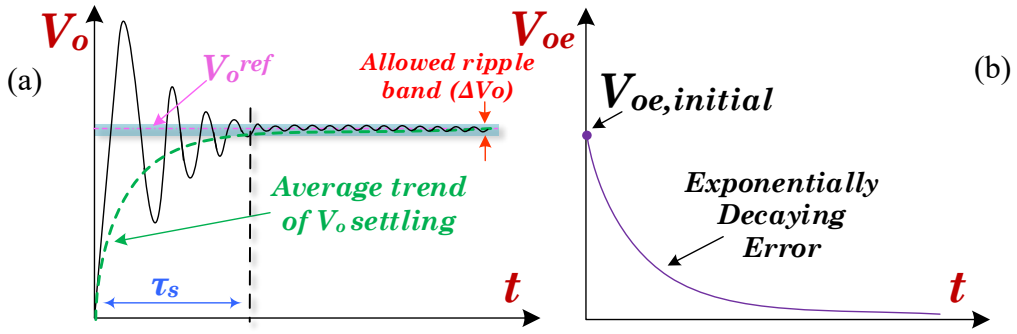


Figure 3.33: (a) Typical Voltage Start Up Trend (b) Exponentially Decaying Output Voltage Error Trend

Further, as observed in Figure 3.34, the constraints defined for the sliding surface ($S + \varrho$ and $S - \varrho$) dictate the overshoot/undershoot in the output voltage due to its proportionality with the deviation from the normalized sliding surface. Referring to the slope of sliding function, the traversal of 2ϱ is obtained during one switching cycle,

where$\dot{S} > 0$ corresponds to the conducting time interval (τ_c) of the secondary side switches S_5 and S_8, and $\dot{S} < 0$ corresponds to the blocking time interval (τ_b) of these switches, both of which are selected to be constant at 50% (i.e., operational duty ratio) of the switching time interval [96]. It can therefore be inferred that, the maximum slope magnitudes are observed for minimum values of τ_c or τ_b. Thus, the slope magnitude constraint of the sliding mode function can be written as:

$$\dot{S} = \left|\frac{dS}{dt}\right| = \left|-M_1\dot{V}_o + M_2 V_{oe}\right| < \frac{2\varrho}{\tau_c\ (or\ \tau_b)} \tag{3.141}$$

But as the $\tau_c/\tau_b$are constrained to 50%, we can substitute $\tau_c\ (or\ \tau_b) = \frac{\pi}{\omega_s}$ in (3.141) to obtain the following relation.

$$\dot{S} = \left|-M_1\dot{V}_o + M_2 V_{oe}\right| < \frac{2\varrho\omega_s}{\pi} \tag{3.142}$$

$$M_1\dot{V}_o + M_2 V_o < \frac{2\varrho\omega_s}{\pi} - M_2 V_o^{ref} \tag{3.143}$$

Integrating (3.143) for a switching cycle to obtain the correlation between τ_c (or τ_b) and ΔV_o, the following relation is obtained:

$$M_1\Delta V_o + M_2 V_o \tau_c < \left[\frac{2\varrho\omega_s - M_2 V_o^{ref}\pi}{\pi}\right]\tau_c \tag{3.144}$$

As the considerations of overshoot/undershoot are defined in large signal domain, following (3.112), V_o can be written as follows referring to the state-space model in large signal domain [90]:

$$V_o = V_{C_o} = \frac{2}{\pi}\sum_{k=1}^{2n-1} I_{sT,k} R_{o,k} \tag{3.145}$$

Substituting V_o from (3.145) in (3.144), the maximum overshoot is obtained as follows:

$$\Delta V_{o,max} = \frac{2\varrho\omega_s}{\pi}\tau_c - (p_x)\frac{M_2\tau_c}{M_1} \tag{3.146}$$

$$\text{where, } p_x = V_o^{ref} + \frac{2}{\pi}\sum_{k=1}^{2n-1} I_{sT,k}R_{o,k} \tag{3.147}$$

Careful considerations of (3.140) and (3.146) enable the designer to design the controller response as per the desired application specific requirements of settling time and maximum acceptable overshoot/undershoot.

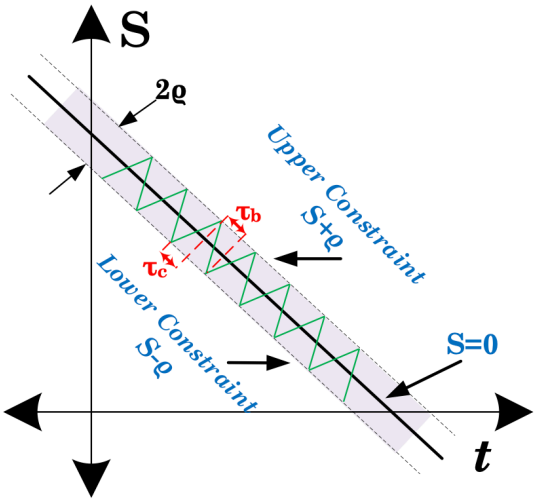


Figure 3.34: Sliding Surface Plot on Phase Plane

3.6.4. Closed Loop Stability of SMC and Comparison with Conventional PI Controller

The closed loop control system corresponding to the developed open-loop GHA based all-inclusive plant (as seen in (3.127)) is portrayed in Figure 3.35 and the corresponding closed loop transfer function can be written as follows:

$$TF_{CL}(s) = \frac{\left(M_1+\frac{M_2}{s}\right)G_p(s)}{1+\left(M_1+\frac{M_2}{s}\right)G_p(s)} \tag{3.148}$$

Utilizing the closed loop transfer function as shown in (3.148), and the controller coefficients obtained using the criteria mentioned in (3.140) and (3.146), the closed loop

frequency response of the designed SMC controller is shown in Figure 3.36. As observed, the closed loop gain crossover frequency is achieved at 38kHz, selected to ensure a ~1/225th order attenuation to the worst-case open loop plant crossover frequency – 8.51MHz, essentially mitigates all the high frequency components from the output voltage, thus ensuring a superior EMI performance. Additionally, the phase margin is achieved to be 138° that renders the closed loop system in the stable operating zone.

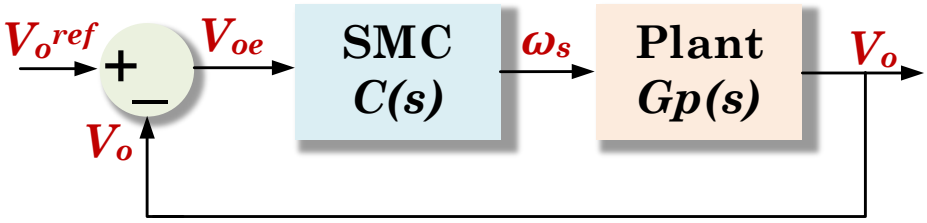


Figure 3.35: Closed Loop System Block Diagram with SMC Based PFM Controller

Further, to compare the performance of the designed SMC controller with the conventional PI controller, two instances of closed loop responses obtained from the derived plant transfer (3.127) are taken into consideration: (a) A PI (PI_a) controller with similar crossover frequency (38kHz) has a phase margin (PM) lesser than SMC controller ($PM_{SMC} > PM_{PI_a}$), and (b) Another PI (PI_b) controller with similar PM (141°) as SMC has 27dB lower attenuation (27dB lesser) as compared to SMC based controller. Following the above-mentioned comparison, the key take-aways in terms of dynamic performance of the system are as follows:

(a) The closed loop system experiences higher overshoot ($e^{-\frac{\pi\xi_d}{\sqrt{1-\xi_d^2}}}$) and becomes more oscillatory (due to lower damping ratio ξ_d and higher settling time, $t_s = 3/\xi_d\omega_n$ for a 5% tolerance band) as the PM decreases while approaching the stability limit. In that

context, as observed for the comparison case involving PI(a), due to higher PM, the overshoot with SMC controller is significantly subdued and results in faster settling time, thus portraying its superior dynamic characteristics.

(b) As observed in Figure 3.36, the PI_a controller portrays a positive gain (high 'Q') for certain frequencies (21kHz to 38kHz for PI_a), which might lead to instabilities due to unaccounted amplification of high frequency components that may be present in any of the feedback signals.

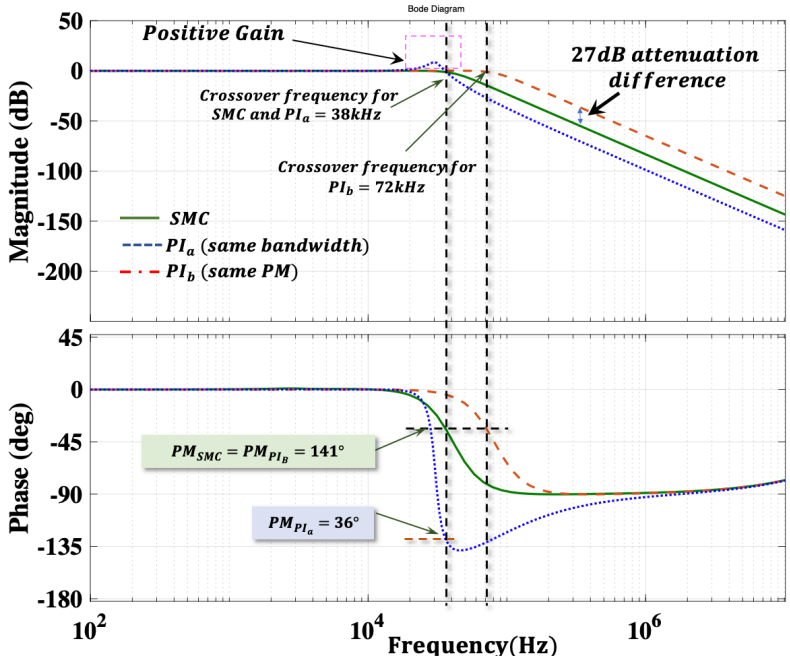


Figure 3.36: Closed Loop Frequency Response for (a) SMC Based Controller, (b-c) Conventional PI Controllers

3.6.5. Hybrid Control Scheme for Minimized Secondary Turn-off Current

Analyzing the controller dynamic constraints and adhering to the objective of attaining minimized turn-off losses at the secondary bridge (as explained in Section 3.2), the proposed hybrid control scheme is shown in Figure 3.37. As observed, the sensed value

of output voltage (V_o) is compared with its reference value (V_o^{ref}) to generate the error (V_{oe}), which is then passed through the SMC control block to obtain the value of ($\Delta\omega_s$). This obtained signal is then added to ω_s^*, which portrays an initial estimate of the switching frequency (generally obtained from open loop gain plots), to obtain the required modulated frequency ($\omega_s^* + \Delta\omega_s$). Further, a limiter is used to constrain the operational frequency ($200kHz < f_s^* \left(= \frac{\omega_s^* + \Delta\omega_s}{2\pi}\right) < 650kHz$) to stay in the limits based on the ZVS criteria [147], gain requirements and stress on the switches. A voltage-controlled oscillator (VCO) is then utilized to generate the required gating pulses for primary side switches ($S_1 - S_4$) corresponding to the modulated frequency signal. Further, to necessitate an additional phase shift (ν) facilitating the synchronous rectification operation, aimed at minimizing the turn-off losses, a look-up table is employed, that generates the required phase-shift with respect to the loading condition (obtained by sensing I_o) and is implemented using a variable delay block.

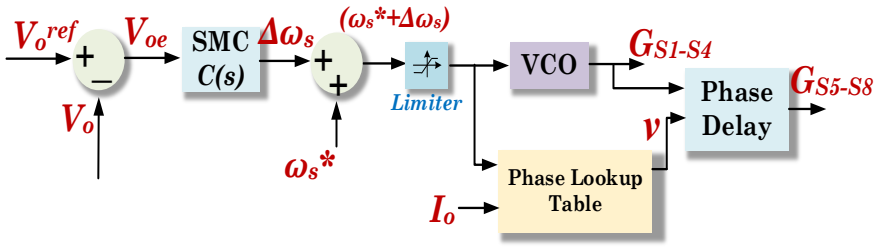


Figure 3.37: Proposed SMC Based Hybrid Control Scheme for Turn-off Current Minimization

3.7. Experimental Verification and Benchmarking

To validate the findings and analysis presented in the previous sections, an experimental prototype (as shown in Figure 3.38) is developed for the specifications mentioned in Table 3.9.

Table 3.9: Design Specifications for Bidirectional CLLC

Parameters	Values
Primary input voltage range (V_P)	400V
Secondary output voltage range (V_S)	24-28V
Rated Power (P_o)	1kW
Transformer Turns Ratio (n)	22:1
Tank Leakage Inductances (L_P, L_S)	11.8µH, 0.022µH
Magnetizing Inductance (L_m)	72µH
Tank Capacitors (C_P,C_S)	8.58nF, 5.06µF
Resonant frequency (f_r)	500 kHz

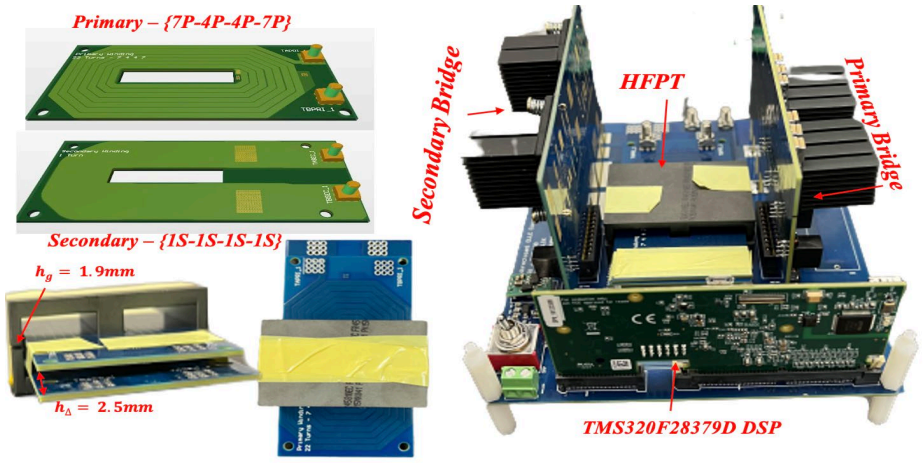


Figure 3.38: Experimental Proof-of-Concept for Developed CLLC Converter

3.7.1. HFPT Characterization

Utilizing the analysis and dependencies shown in the previous sections with considerations pertaining to the variation of transformer parameters with respect to change

in the winding arrangements, and other physical characteristics, the most optimum arrangement aimed at achieving the required specifications for the mentioned CLLC topology is selected. A 22:1 planar transformer with primary winding structure of {[7P-4P-4P-7P],[1S*-1S*-1S*-1S*]}using two 4-layer 1.6mm PCBs with a copper conductor thickness of 70μm is fabricated. Corresponding to the selected PCB arrangement: $h_{pr} = 0.23mm$ and $h_c = 1.19mm$ are selected. The air gap between the primary and secondary winding $h_\Delta = 0.5mm$ and that between the core $h_g = 2.5mm$ is selected to achieve the required L_P, L_S and L_m. The core used for this application is FR45810EC.

Referring to the material properties of R-material [157], it was observed that the sensitivity of μ_r with respect to frequency variation for the required gain range at all loading conditions ($G \in [0.88,1.232]$ for $f \in [297,702]kHz$) is $S_f^{\mu_r} = \frac{d\mu_r/\mu_r}{df/f} < 1.29\%$, leading to a sensitivity in resultant L_m with respect to μ_r to be $S_{\mu_r}^{L_m} = \frac{dL_m/L_m}{d\mu_r/\mu_r} < 1.62\%$. Utilizing this dependency, the gain trend for selected specifications experiences a variation of <1.85%, which validates the core selection with a negligible effect on the output voltage regulation.

Figure 3.39 shows the thermal images of the HFPT assembly, for a converter operation at its rated load of 1kW. As observed, the temperature of the winding is restricted within 40℃ adhering to the design constraints.

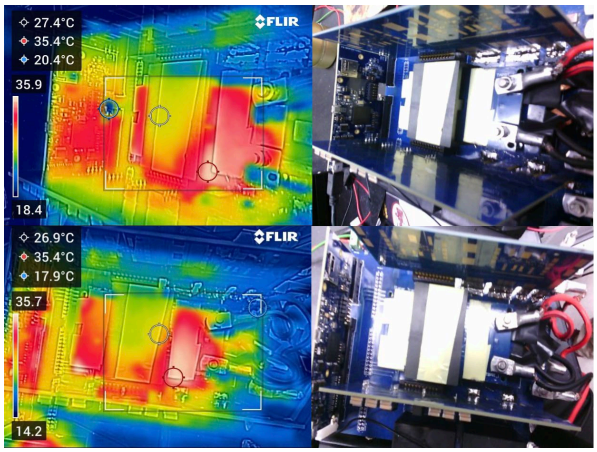


Figure 3.39: Thermal Image of the HFPT Assembly During Rated Load Operation.

3.7.2. Turnoff Current Minimization Using Novel SR Technique

Detailed analysis elucidating results obtained for both light and heavy loading conditions highlighting the synchronous rectification action are presented in this section. Further, following similar investigation pertaining to the gain and phase shift requirement, experimental results of reverse power flow are also presented accounting for the switching loss minimization objective. The required gate pulses with a phase shift enabling SR are provided using TMS320F28379D dual-core digital signal processor. The primary side bridge is realized using GaN Systems GS66508T ($650V, 30A, 50m\Omega$), while the secondary side consists of four EPC2020 ($60V, 90A, 2.2m\Omega$) switches connected in parallel, thus enabling an all-GaN power converter solution, ensuring a superior power density of 106 W/inch^3.

A comprehensive flowchart to elucidate the optimization approach and its implementation is presented in Figure 3.40. As observed, with the knowledge of the design specifications and HFPT parasitic components, an offline calculation of optimum operating

points is executed using multi-dimensional Newton optimization method. With respect to the cost function (min $i_{turnoff}$) defined, the function $F\left(i_s\left\{X^{(u)}\right\}\right)$ is solved iteratively and corresponding error $\epsilon\left\{F\left(i_s\{X\}^{(u)}\right)\right\}$ is calculated for every iteration. The algorithm converges when the criteria: $\epsilon\left\{F\left(i_s\{X\}^{(u)}\right)\right\} < 0.1\%$ is satisfied (which indicates that the function has reached its minimum value), resulting in operating points $\left\{\widehat{\omega_s}, \hat{\vartheta}\right\}$ that correspond to minimum turnoff current. To quantify the stop criteria for the optimization algorithm, Figure 3.41 portrays the plot of the error with respect to number of iterations. As observed, the function converges after 54 iterations, when the error values satisfy the convergent criteria ($\epsilon\left\{F\left(i_s\{X\}^{(u)}\right)\right\} < 0.1\%$). The number of iterations can be further reduced by adding a learning coefficient α_k in the optimum point tracking process [146]. These optimum points are stored along with the load information in the microcontroller (TMS320F28379D) as a lookup table. For real-time realization of the optimization algorithm, the load information is sensed, and corresponding gate pulses are given to switch S_1 to S_4 having a switching frequency of $\widehat{f_s} = \frac{\widehat{\omega_s}}{2\pi}$. In addition to that, the gate pulses are shifted by a phase of $\hat{\vartheta}$ and are applied to secondary side switches (S_5 to S_8) to obtain the required SR action.

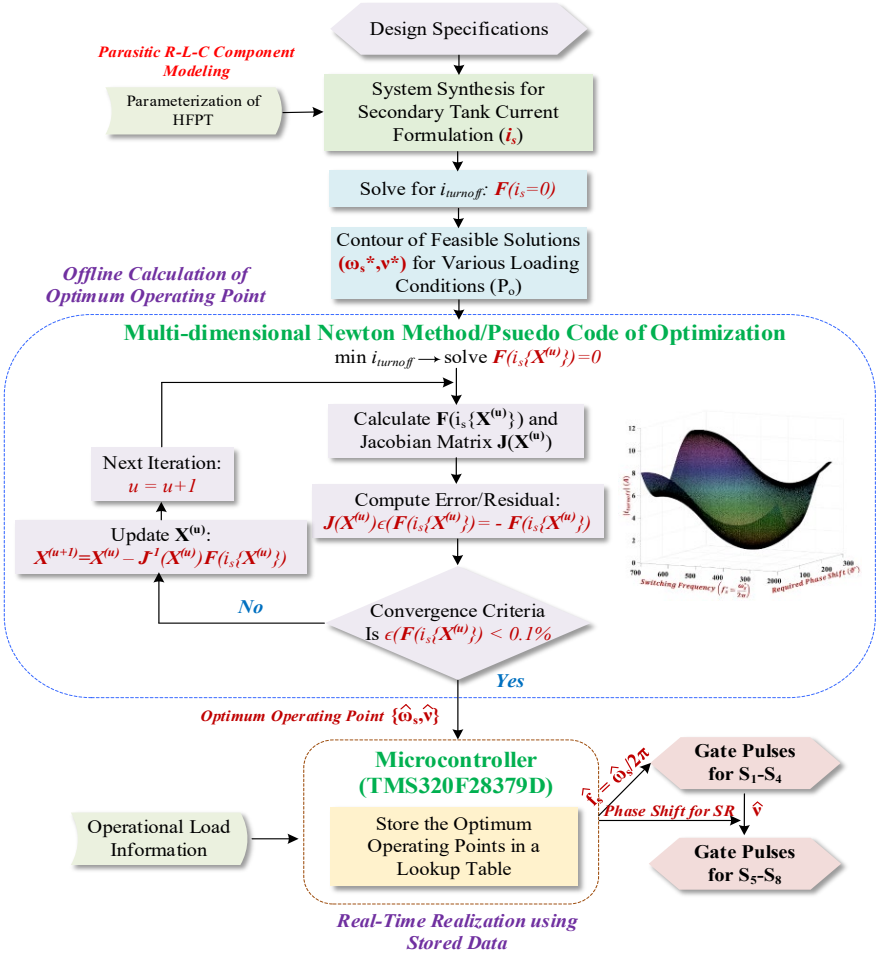


Figure 3.40: Implementation of the Proposed Algorithm for Turnoff Current Minimization

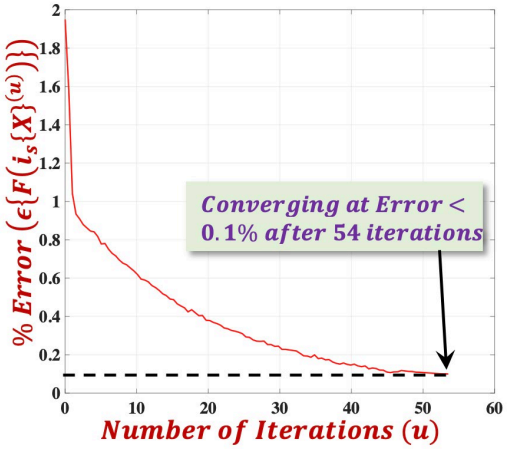


Figure 3.41: Function Convergence Plot with Respect to Number of Iterations

Please note, due to significantly high magnitude of I_s, the interface between the HFPT and secondary bridge PCB is made using 20 Litz wires of same specification, connected in parallel to (a) facilitate near-equal sharing of current amongst all the wires and (b) to minimize any additional stray inductance, thus ensuring optimal tank design. Relevant experimental results for I_s have been obtained by probing one of the Litz wire.

Figures 3.42-3.43 show the experimental results obtained for forward power flow for a voltage conversion of 400-28V, obtained at 462.9kHz with a SR phase shift of $\vartheta = 46.9°$, resulting in minimum switching losses (of 62mW), portraying a strong agreement with the presented analysis, having a mismatch of 0.29% only. As observed, the instantaneous current at turn-off instant is significantly less (~1.4A), which ensures ominously reduced turnoff losses for the secondary side switches. Further, as observed in Figure 3.43, the primary current lags the primary bridge voltage thus achieving ZVS operation [170] ($i_p < 0$ at turn-on), which matches the presented analysis and justifies the winding selection and ZVS based constraint.

$$P_{turnoff} = 2\frac{1}{2}V_o i_{turnoff} f_s t_{off} = 62mW \tag{3.149}$$

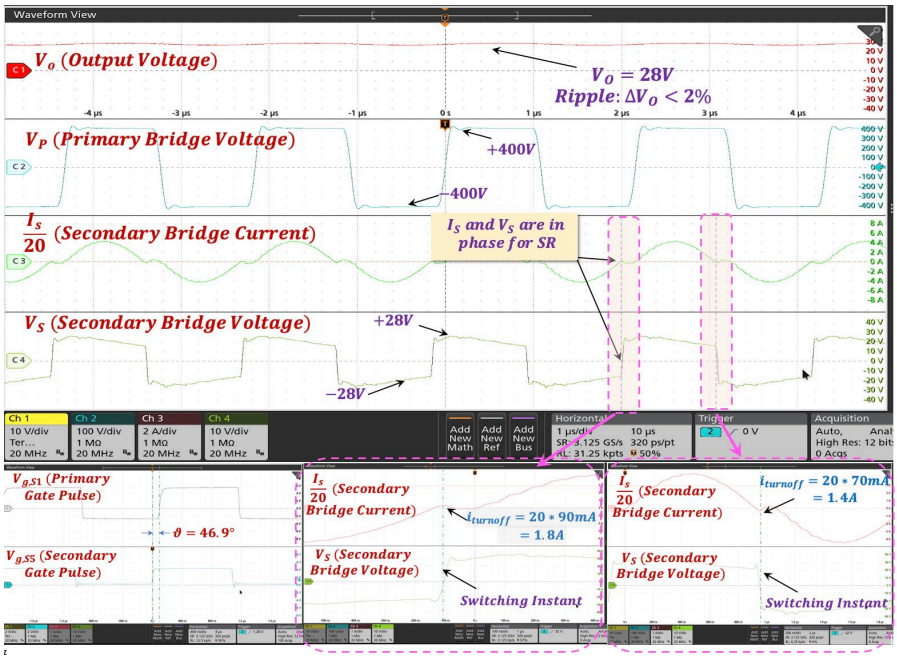


Figure 3.42: Experimental Waveforms for 400-28V Conversion at 1kW Elucidating SR (Y-axis: V_o=10V/div, V_P=100V/div ,V_s=10V/div, $\frac{I_S}{20}$=2A/div; X-axis: Time = 1µs/div)

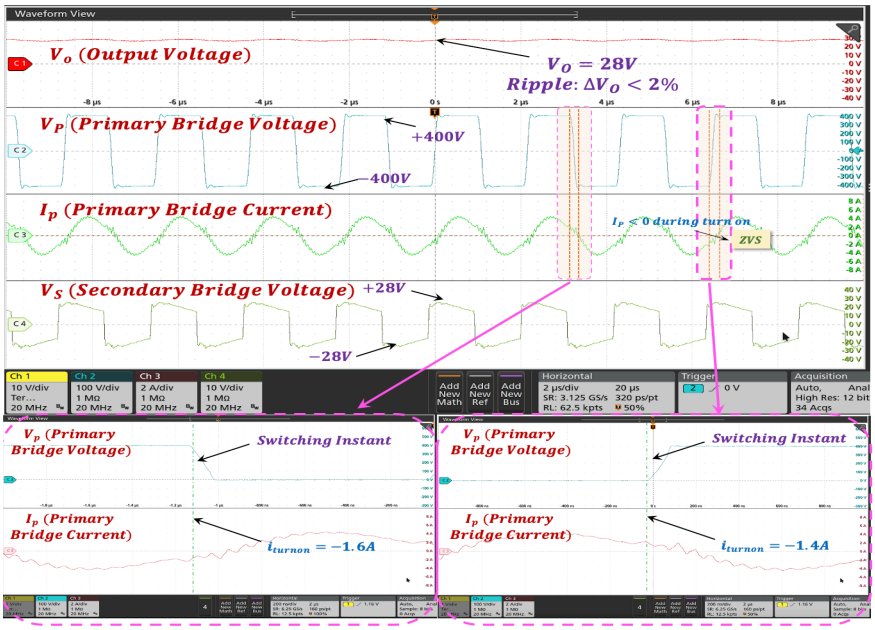


Figure 3.43: Experimental Waveforms for 400-28V at 1kW Elucidating ZVS (Y-axis: V_o=10V/div, V_P=100V/div ,V_s=10V/div, I_p=2A/div; X-axis: Time = 2µs/div)

To elucidate the wide-gain capability of the designed converter, Figure 3.44 shows experimentally obtained waveforms for 400-24V conversion, with its optimum operating point located at $\{f_s, \vartheta\} = \{452.5kHz, 42.2°\}$. As observed, the primary switches undergo ZVS turn-on, while the secondary side switches experience minimal switching losses (84mW) accounting for the comprehensive phase identification method used to enable SR.

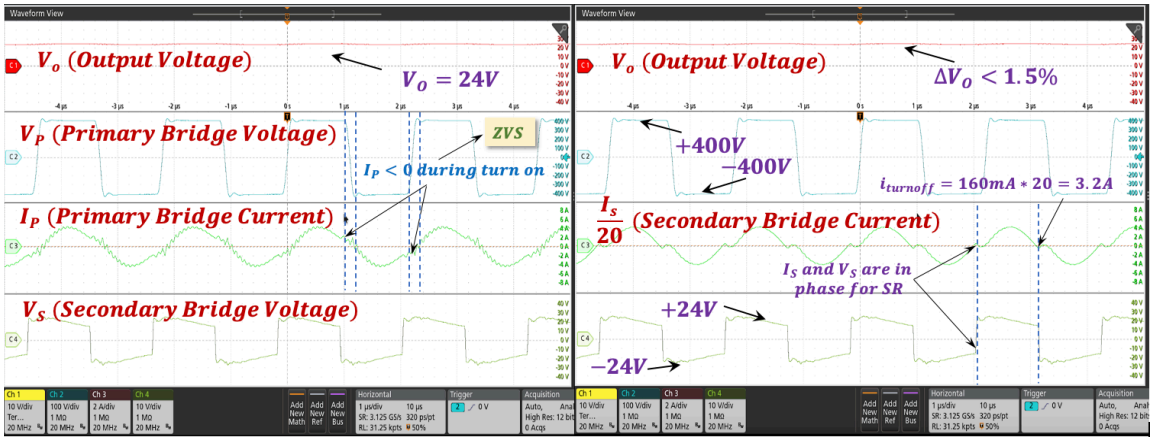
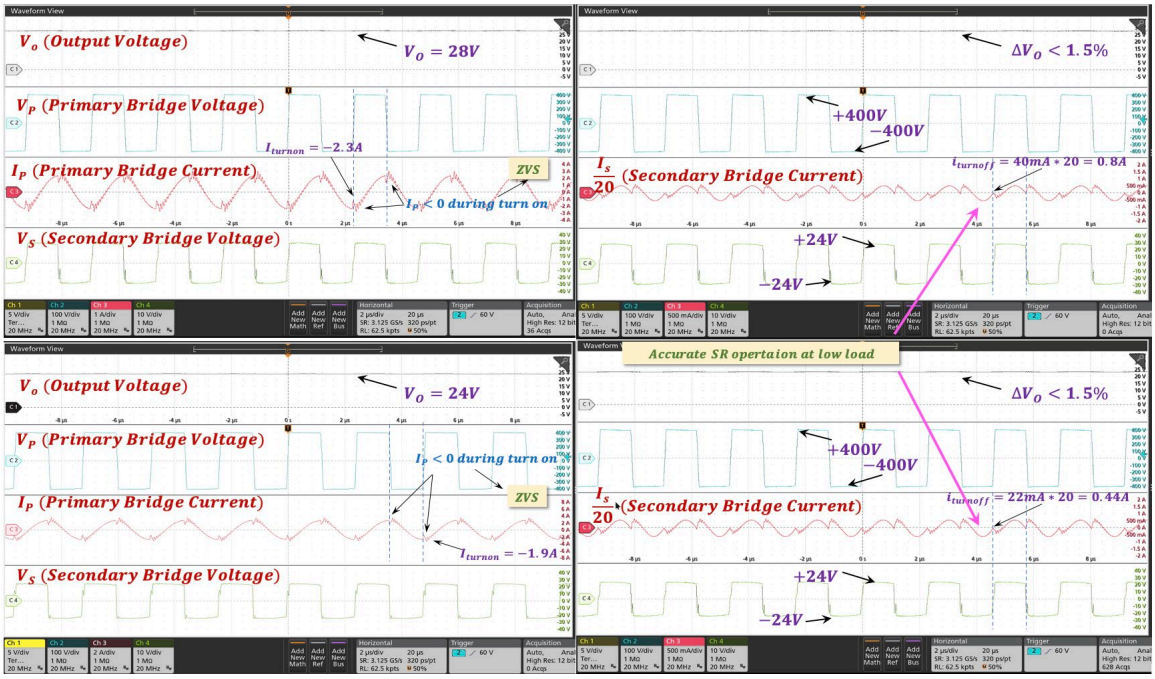


Figure 3.44: Experimental Waveforms for 400-24V Conversion at 1kW Load (Y-axis: V_o=10V/div, V_P=100V/div ,V_s=10V/div, I_p=2A/div, $\frac{I_s}{20}$=2A/div; X-axis: Time = 1µs/div)

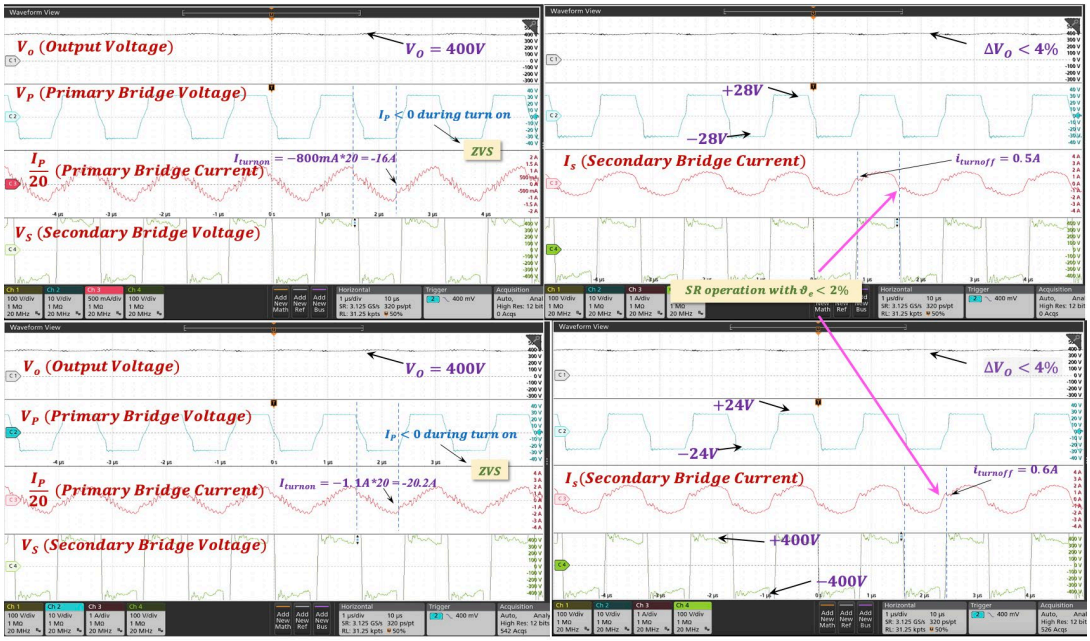
While adhering to the efficiency maximization objective by reducing the secondary side switching losses at higher loading conditions, the presented analysis also portrays its effectiveness in light loading conditions. Figure 3.45 (a-b) illustrates the converter operation at 10% load, while achieving the required gain range to obtain $V_o = 28V$ and $V_o = 24V$, respectively. As observed, ZVS operation is maintained, while the turnoff losses at the secondary side are limited to 59mW due to accurate SR tracking.

(a) 

(b)

Figure 3.45: Experimental Waveforms for (a) 400-28V (b) 400-24V Conversion at 100W (Y-axis: V_o=5V/div, V_P=100V/div ,V_s=10V/div, I_p=1A/div, $\frac{I_s}{20}$=0.5A/div; X-axis: Time = 2μs/div)

To portray the feasibility of efficient reverse power flow for V2G applications, Figure 3.46 shows experimentally obtained waveforms implementing the optimal phase detection method as explained in Section 3.3. As observed, the turnoff current is reduced to $\sim 0.5A$ that corresponds to switching losses of only 62mW in the secondary side, in addition to ZVS at the primary side, leading to reverse power peak efficiency of 96.2%.

(a) 

(b)

Figure 3.46: Experimental Waveforms for Reverse Power Flow for (a) 28-400V (b) 24-400V Conversion (Y-axis: V_o=100V/div, V_P=10V/div ,V_S=100V/div, $\frac{I_p}{20}$=0.5-1A/div, I_s=1A/div; X-axis: Time = 1µs/div)

To benchmark the efficiency improvement of the proposed SR method for 400-28V and 400-24V conversion, a detailed analytical loss breakdown at rated load of 1kW is provided in Table 3.10, that compares the various aspects of system losses for FHA, GHA, and the proposed method. Further, the loss breakdown for 400-28V and 400-24V conversion is graphically presented in Figure 3.47.

As observed, due to accurate tracking of phase shift required for SR and operating it at the optimum frequency obtained as a part of the optimization, the switching losses using the proposed method are considerably reduced. Further, as the tank currents are also relatively lesser due to optimum frequency operation, the conduction losses and transformer winding losses are also reduced, thus boosting the rated load efficiency of the system.

Further, Figure 3.48 compares the forward power flow efficiency trend at various loading conditions for (a) 400-28V and (b) 400-24V conversion. As observed, due to elaborate and precise modelling accounting for the stray components affecting the system operating point, the proposed model yields a peak efficiency of 98.49%, elucidating its superiority even at a high operational frequency.

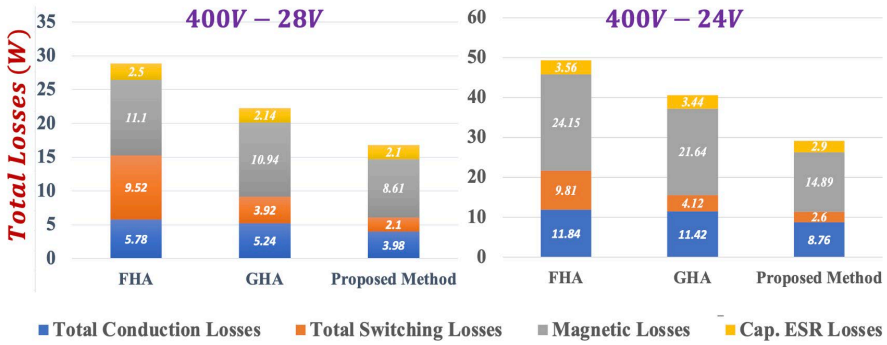


Figure 3.47: Loss Breakdown and Comparison of 400-28V and 400-24V Conversions

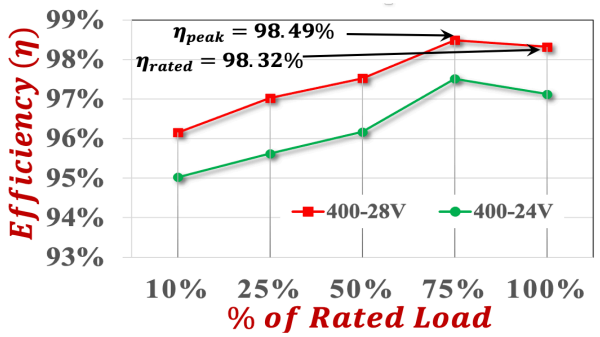


Figure 3.48: Efficiency Trend for Various Loading Conditions

Table 3.10: Comprehensive Loss Breakdown and Comparison for FHA, GHA and the Proposed Method.

Loss category	Loss sub-category	Formulation	Comments	FHA	GHA	Proposed Method
Semiconductor Losses	Switch Turn on losses	$P_{sw,on\,(S_X)} = \frac{1}{2} V_{DS\,(S_X)} I_{D\,(S_X)} \left(t_{1,on\,(S_X)} + t_{2,on\,(S_X)}\right) f_s$ Where, $t_{1,on\,(S_X)} = R_{g(S_X)} C_{in(S_X)} \ln\left(\frac{V_{Dr(S_X)} - V_{th(S_X)}}{V_{Dr(S_X)} - V_{pl(S_X)}}\right)$ $t_{2,on(S_X)} = \frac{C_{gd\,(S_X)}\left(V_{DS\,(S_X)} - I_{D(S_X)} R_{DS,on\,(S_X)}\right) R_{g(S_X)}}{V_{Dr(S_X)} - V_{pl(S_X)}}$	Primary Side Switches ($S_1 - S_4$) will undergo ZVS due to operation in inductive region. However, they will still incur turnoff losses. The secondary side switches ($S_5 - S_8$) will incur turnoff losses corresponding to the error in the phase calculation. For FHA and GHA based methods the inaccuracy in the phase estimation was ~4% and ~12% respectively, as compared to the proposed model, leading to higher switching losses.	9.52W (400-28V) 9.81W (400-24V)	3.92W (400-28V) 4.12W (400-24V)	2.14W (400-28V) 2.6W (400-24V)
	Switch Turn off losses	$P_{sw,off\,(S_X)} = \frac{1}{2} V_{DS\,(S_X)} I_{D(S_X)} \left(t_{1,off\,(S_X)} + t_{2,off(S_X)}\right) f_s$ Where, $t_{1,off(S_X)} = R_{g(S_X)} C_{in(S_X)} \ln\left(\frac{V_{pl(S_X)}}{V_{th(S_X)}}\right)$ $t_{2,off(S_X)} = \frac{C_{gd(S_X)}\left(V_{DC(S_X)} - I_{D(S_X)} R_{DS,on(S_X)}\right) R_{g(S_X)}}{V_{pl(S_X)}}$				
	Conduction Losses	$P_{cond\,(S_X)} = I^2_{D,RMS\,(S_X)} R_{DS,on\,(S_X)}$	The conduction losses in the switches depend on the tank currents, which are a function of the operating frequency and the phase shift.	5.78W (400-28V) 11.84W (400-24V)	5.24W (400-28V) 11.42W (400-24V)	3.98W (400-28V) 8.76W (400-24V)
Capacitor ESR Losses	-	$P_{Cap,ESR} = I^2_{O,ripple\,(RMS)} R_{C_O,ESR}$	The capacitor ESR losses remain relatively unchanged in all the cases.	2.5W (400-28V) 3.56W (400-24V)	2.14W (400-28V) 3.44W (400-24V)	2.12W (400-28V) 2.9W (400-24V)
Magnetics	Core Losses	$P_{core} = \frac{1}{T} \int_0^T k_i \left\lvert \frac{dB}{dt} \right\rvert^{\alpha} (\Delta B)^{\beta-\alpha} dt$ Where, $k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} \lvert\cos\theta\rvert^{\alpha} 2^{\beta-\alpha} d\theta}$	The RMS values of the tank current are different for FHA, GHA, and proposed method due to different operating frequencies. With the accurate phase and frequency calculated, the winding losses are least in the proposed method.	11.1W (400-28V) 24.15W (400-24V)	10.94W (400-28V) 21.64W (400-24V)	8.61W (400-28V) 14.89W (400-24V)
	Winding Losses	$P_{winding} = I^2_{p,RMS} R_p + I^2_{s,RMS} R_s$				

For any switch $S_{X;\, X \in \{1,2,\ldots 8\}}$: -

$V_{pl\,(S_X)}$ = Gate plateau voltage
$R_{DS,on\,(S_X)}$ = On-state resistance of the switch
$R_{g\,(S_X)}$ = External gate resistance
$I_{D\,(S_X)}$= Instantaneous drain current of the switch
$I_{D,RMS\,(S_X)}$= RMS drain current of the switch
$C_{gd\,(S_X)}$= Gate to drain capacitance of the switch
$C_{in\,(S_X)}$ = Input capacitance of the switch
$C_{gs\,(S_X)}$= Gate to source capacitance
$R_{C_O,ESR}$ = ESR of the output capacitor
$V_{th(S_X)}$ = Threshold voltage
k, α, β = Steinmetz equation parameters
ΔB = peak to peak flux density
$t_{1,on(S_X)}$ = Time required for I_D to reach its rated value
$t_{2,on(S_X)}$ = Time required for V_{DS} to drop down to zero
$t_{1,on(S_X)}$ = Time required for V_{DS} to reach its rated value
$t_{2,on(S_X)}$ = Time required for I_D to drop down to zero

3.7.3. All-inclusive Small Signal Model and Proposed SMC Hybrid Control Scheme

A noise immune operational amplifier (LT1368) based voltage sensing circuit with digitally implemented low pass filter is used to sense the output voltage at ADC port 3, with intricately quantified sensor gains and offsets.

To verify the preciseness of the derived GHA based all-inclusive small signal, the frequency response of the simulated plant transfer function is compared with the experimentally obtained gains at the rated loading conditions by perturbing the operational frequencies and measuring the resultant gain. To obtain the experimental results, a set of discrete frequency perturbations ranging from 100Hz to 5MHz (limited by the equipment used) were generated and correspondingly the perturbations in the output voltage magnitude and phase (with respect to V_p) were recorded. This data was then tabulated in MATLAB to find the gain according to (3.150) and were plotted as discrete points. Figure 3.49 elucidates the above-mentioned comparison by presenting the frequency sweep of the open-loop converter plant transfer function obtained at the rated load, where the x-axis denotes perturbations in frequency and the y-axis describes the magnitude of the small-signal output voltage-to-frequency ratio (measured in dB).

$$Gain\ (dB) = 20\log_{10}\frac{\Delta V_o}{\Delta f} \tag{3.150}$$

As observed, the experimentally obtained points show good agreement with the analytically generated plots for perturbations limited to 5MHz. The deviation becomes larger for higher frequencies due to aggravated effect of the ESR (r_{C_o}) of the output capacitors at higher frequency bands. As observed, due to precise considerations of the

parasitic components involved in the proposed model, the experimental results portray an average mismatch in gain of <4.2% with maximum deviation at 4MHz.

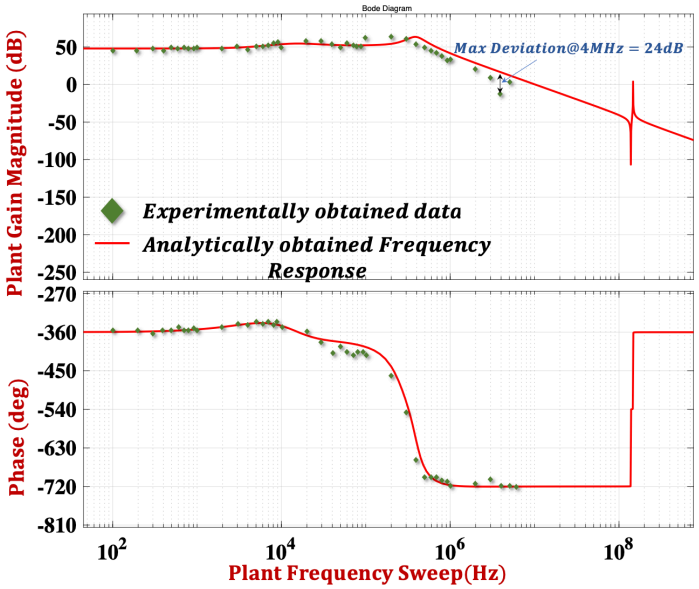


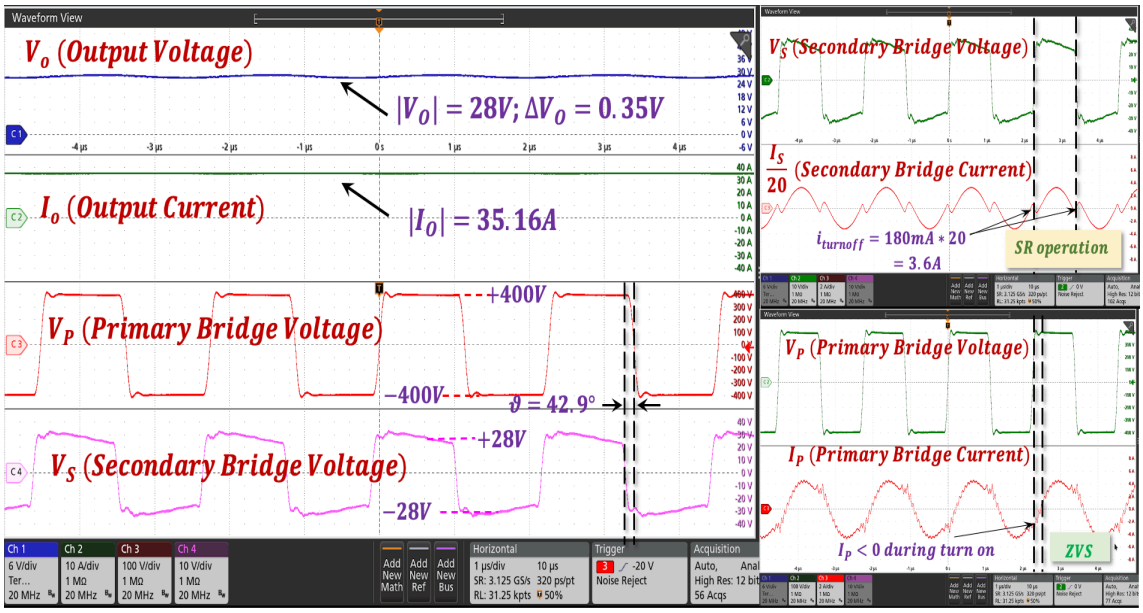
Figure 3.49: Experimental Validation of the Proposed All-Inclusive GHA Based Open Loop Plant Frequency Response

Corresponding to the steady-state performance of the proposed control scheme at the rated load, Figure 3.50 shows the experimental results of forward power flow for a voltage conversion of 400V-28V. As observed in Figure 3.50 (a), corresponding to the tuned sliding surface coefficient pertaining to the constraints in (3.140,3.144), the output voltage achieves a stiff regulated 28V output voltage with a peak-to-peak ripple (ΔV_o) of 0.35V. The steady-state operational frequency is obtained at 442.4kHz, with a required phase shift (ϑ) of 42.9° to facilitate minimum secondary bridge turn-off current (3.6A) (as shown in Figure 3.50 (a)), thus resulting significantly reduced turn-off losses (160mW). Further, as observed in Figure 3.50 (a), accounting for the operation in inductive region, the primary bridge achieves ZVS operation ($i_p < 0$ at switch turn-on).

Similarly, the set of results shown in Figure 3.50 (b) elucidate the steady state operation results for a 400V-24V conversion at 1kW rated load. As observed, the operational frequency is 463kHz with phase shift (ϑ) of 39.4°, yielding a turn-off current of 4.4A and an output voltage ripple of 0.29V.

Following the converter operation at rated load, Figure 3.51 shows the experimentally obtained results for 10% loading condition for a voltage conversion of 400-28V. As observed, the controller achieves the steady state output with operational frequency of 543.25kHz (>f_r (500kHz)), where the output voltage is settled at 28V with a peak-to-peak ripple of 0.19V. Soft-switching is ensured at the primary side through ZVS turn-on, while the secondary side switches observe SR action, thus resulting in a minimized turnoff current of 0.34A.

(a)



(b)

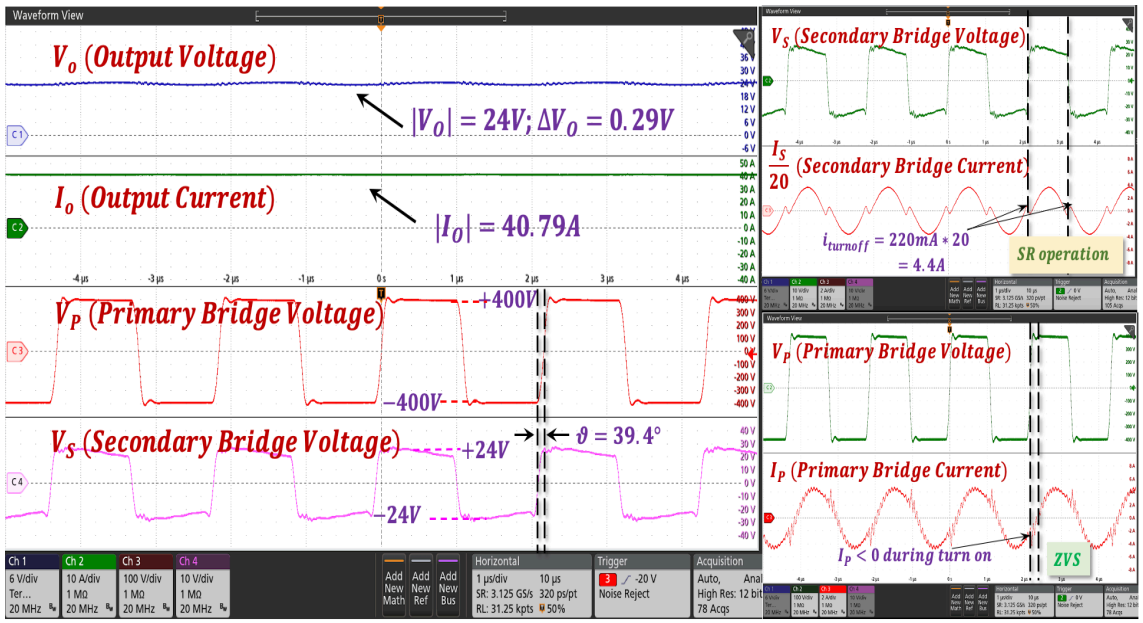


Figure 3.50: Steady State Experimental Results at 1kW Rated Power for (a) 400-28V Conversion and (b) 400-24V Conversion (Y-axis: V_o=6V/div, I_o=10A/div, V_P=100V/div ,V_s=10V/div, $\frac{I_s}{20}$=2A/div,I_p=2A/div; X-axis: Time = 1µs/div)

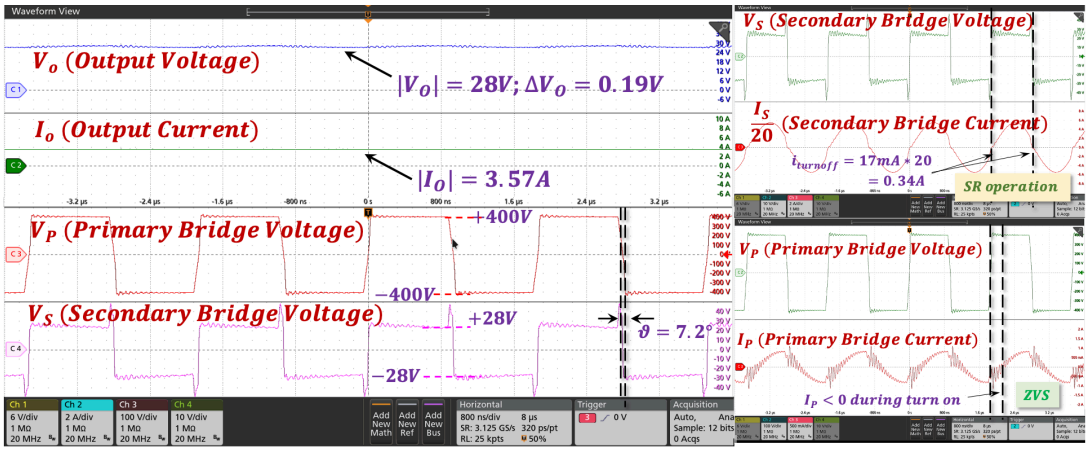


Figure 3.51: Steady State Experimental Results at 100W Rated Power for 400-28V Conversion (Y-axis: V_o=6V/div, I_o=2A/div, V_P=100V/div ,V_s=10V/div, $\frac{I_S}{20}$=2A/div,I_p=0.5A/div; X-axis: Time = 800ns/div)

In addition to the above shown findings elucidating the steady state operation, Figure 3.52 presents the dynamic load transient results for a step-change of 10% to 90% of the rated load implemented using the proposed control scheme. As observed, adhering to the settling time constraint imposed to attain output voltage in the acceptable ripple band $(28 \pm 5\%)V$, the resultant settling time (τ_s) is found to be $360\mu s$. Further, due to the robust design of the controller, the output voltage experiences an undershoot lower than 1.8V with a steady state error of <0.6%, rendering it suitable for crucial battery charging applications. A zoomed-in snapshot of waveforms obtained at 10% and 90% loading conditions are also presented to elucidate the relevance of ZVS and SR operation at both loading conditions, thus validating the efficiency maximization objective as a part of the hybrid control scheme. Similar set of results (as shown in Figure 3.53) are captured for a step-down load change from 90% to 10% of the rated load. The results portray good agreement with the

dynamic constraints imposed resulting in a settling time of $860\mu s$, overshoot of 2.4V and a steady state error of <0.4%. In addition to that, the voltage ripple is ascertained to be limited to <5% of the rated output voltage of 28V, thus validating the robustness and small signal stability of the proposed control scheme.

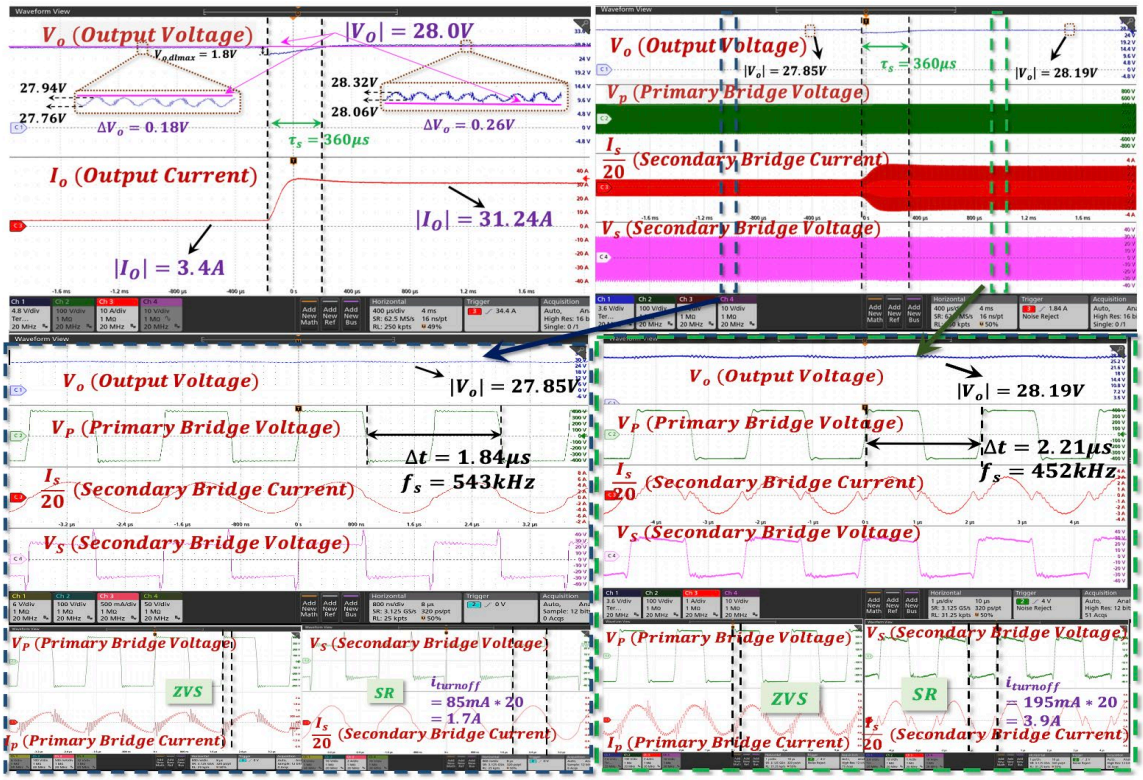


Figure 3.52: Experimental Results for Dynamic Load Change Using SMC Based Hybrid Control Scheme for 10% to 90% Load Step Up (Y-axis: V_o=4.8V/div, I_o=10A/div, V_p=200V/div, $\frac{I_s}{20}$=1A/div, V_s=10V/div; X – axis: Time = 400µs/div).

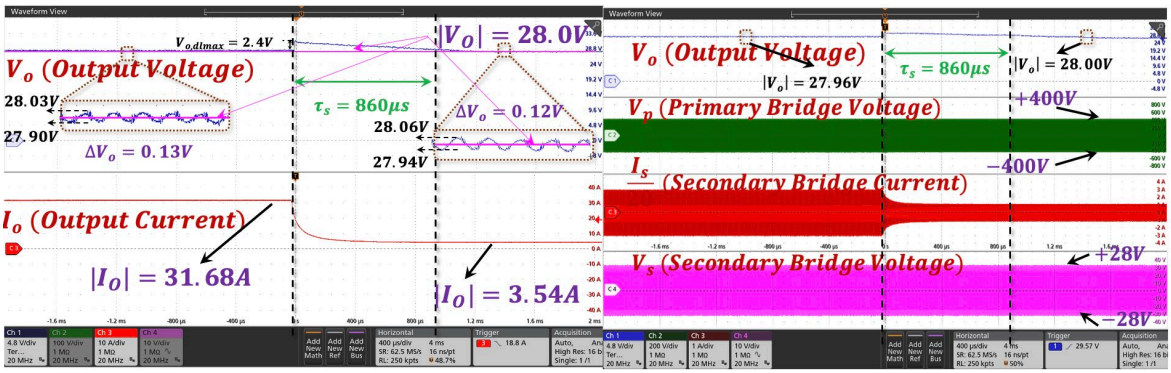


Figure 3.53: Experimental Results for Dynamic Load Change Using SMC Based Hybrid Control Scheme for 90% to 10% Load Step Down (Y-axis: V_o=4.8V/div, I_o=10A/div, V_p=200V/div, $\frac{I_s}{20}$=1A/div, V_s=10V/div; X – axis: Time = 400µs/div).

In addition to that, to provide experimental quantification of improvement with proposed control scheme implementation over conventional PI based controller, similar set of results pertaining to 10%-90% load step-up and 90%-10% step-down results are presented in Figure 3.54 and Figure 3.55 respectively. Further, a detailed quantitative comparison elucidating the settling time and overshoot/undershoot corresponding to the aforementioned two load step-change conditions are presented in Table 3.10. Following the detailed discussion in Section 3.6.3 regarding the quantification of overshoot and settling time on account of improved PM and higher attenuation provided by the SMC controller, the experimentally obtained results in Table 3.11 indicate that the proposed control scheme achieves 46.4% reduced settling time and under/overshoot is subdued by 33%, thus validating the superiority of the robustness and enhanced dynamic performance of the proposed SMC based controller. For the conventional PI based control scheme, due to the absence of the SR enabling phase shift in the control system, the turn-off losses dominate, leading to a degraded peak efficiency of 94.73%. On the other hand, due to the additional phase shift provided by the lookup table for globally enabling SR across the load

range to facilitate minimized switching losses, the efficiency of the converter with the SMC based hybrid control scheme at rated load is measured to be 98.32%, with a peak converter efficiency of 98.49%. The elucidation of this efficiency enhancement is shown in Figure 3.56, which presents a comparison of the efficiency trend of the SMC based hybrid control and conventional PI controller for a voltage conversion of 400V-28V.

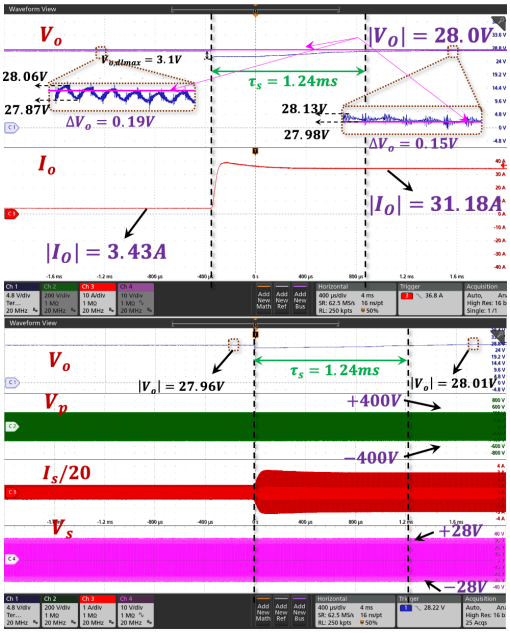


Figure 3.54: Dynamic Load Change Result – 10% to 90% Load Step Up with PI Controller (Y-axis: V_o=4.8V/div, I_o=10A/div, V_p=200V/div, $\frac{I_s}{20}$=1A/div, V_s=10V/div; X – axis: Time = 400µs/div).

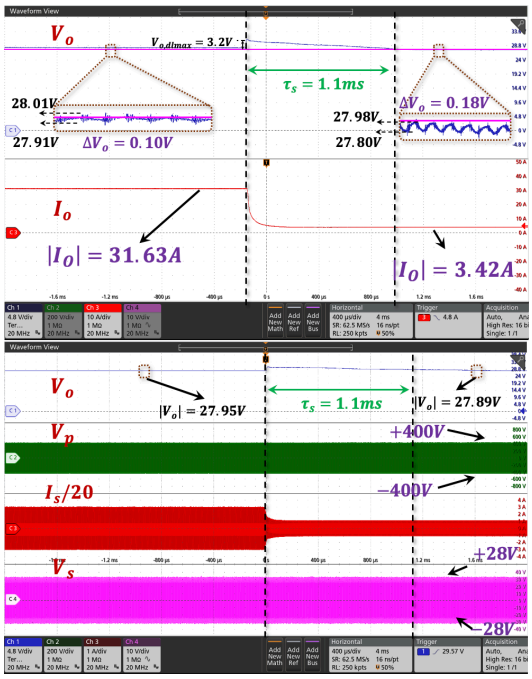


Figure 3.55: Dynamic Load Change Result – 90% to 10% Load Step Down with PI Controller (Y-axis: V_o=4.8V/div, I_o=10A/div, V_p=200V/div, $\frac{I_s}{20}$=1A/div, V_s=10V/div; X – axis: Time = 400µs/div).

Table 3.11: Dynamic Performance Comparison of PI Controller with Proposed SMC Based Hybrid Control Scheme

Load Change	Dynamic Performance Metrics	PI Controller	SMC based Hybrid Control Scheme
10%-90% (step-up)	Settling Time	1.24ms	$360\mu s$
	Overshoot/ Undershoot	3.1V	1.8V
90%-10% (step-down)	Settling Time	1.1ms	$860\mu s$
	Overshoot/ Undershoot	3.2V	2.4V

A comprehensive performance comparison of the various works implementing the SMC based control are elucidated in Table 3.12 to benchmark the proposed application of SMC based hybrid control scheme. Please note that the metrics shown in Table 3.12 are obtained from the experimental results provided in the referenced works [96,171-175],

which vary significantly in terms of the adopted topologies, nominal powers, voltage conversions and % load variations.

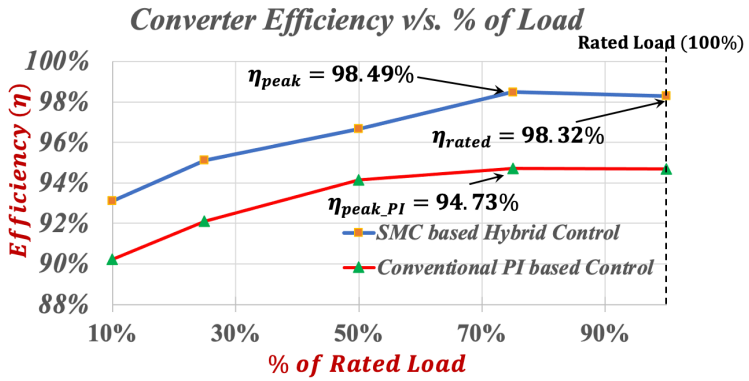


Figure 3.56: Efficiency Trend Comparison Between the Proposed SMC Based Hybrid Control Scheme and the Conventional PI Based Control Scheme

Table 3.12: Performance Comparison of Relevant Works on SMC Implementation with Proposed SMC Based Hybrid Control Scheme

References	Topology	Nominal Power and Voltages ($P_o/V_{in}/V_o$)	Reported % load variations	Dynamic Performance Metrics (Average for load step-up and step-down)	
				Settling Time	Overshoot/ Undershoot
[171]	LLC	972W/85V/175V	~60%	<1ms	<1.5V
[172]	LLC	1kW/180-200V/180-200V	10%	4.2ms	0.5V
[173]	Boost	96W/24V/48V	90%	4.4ms	3.4V
[174]	Quantum Resonant	62.5W/10-15V/25V	50%	1.5ms	3.5V
[175]	Boost	50W/30V/7.5-11V	31.8%	8ms	0.35V
[96]	CLLC	1kW/600V/400V	90%	0.9ms	8V
This work	CLLC	1kW/400V/24-28V	90%	$610\mu s$	2.1V

3.8. Chapter Summary

Meticulously considering the effect of stray parameters on the performance of a bidirectional asymmetric CLLC DC/DC converter, a comprehensive GHA based modeling and analysis is presented in this study. Stressing on the influence of the stray components, a detailed all-inclusive gain model is derived, which is further validated with several experimentally obtained gain points, portraying an average mismatch in gain modulation trend of 0.44% only, thus confirming its accuracy. Unlike other state-of-the-art methods focusing only on phase modulation or frequency modulation, the proposed SR phase detection technique provides a contour of feasible $\{\omega_s^*, \vartheta^*\}$ points for different gain/load operations. Further, a non-linear multi-dimensional minimization function for the secondary current zero crossing is defined with an error margin of 0.1%, that tracks the phase required to facilitate SR, and is experimentally verified elucidating a phase error of 0.29%.

To facilitate the proposed SR tracking method and to ensure optimum transformer design, a thorough parametric RLC modeling of HFPT aided with detailed 3D FEA analysis is presented. The characterization of four different winding structures is carried out comprehensively and corresponding results are verified using various 3D FEA models and experimental analysis, portraying an average mismatch of 6.2% and 5.5% respectively. Further, optimal selection trade-offs are presented pertaining to ZVS constraints, gain requirements and frequency dependencies referring to experimentally developed 1.6mm (2oz. copper) 4-layer PCBs for non-interleaved configurations and 1.6mm (2oz. copper) 8-layer for interleaved structure.

Further, this chapter comprehensively presents an effective and accurate way of modeling an asymmetric resonant CLLC DC/DC converter by involving the inherent higher frequency terms (using GHA) and parasitic components in the small-signal model. Several valuable design insights are deduced that enable the designer to effectively calibrate the compensator response accounting for the effect caused due to the non-idealistic components. Further, a detailed quantified approach to parameterize an SMC based controller is explained by dissecting the dynamic performance constraints, thus deriving the values of the controller coefficients according to the design requirements. Further, the robustness of the SMC based controller is established by extracting several comparisons with PI based controller and their corresponding frequency responses. A hybrid control scheme is also proposed that introduces an additional phase to the secondary side gating pulses, thus facilitating minimized switching losses.

To validate the presented model and SR phase detection method, exhaustive experimental analysis for a 1kW prototype operating at 500kHz resonant frequency with results at various corner conditions are presented. Experimental results for forward power flow for 400-28V and 400-24V are provided which portray a turnoff current of ~1.4A, highlighting reduction in switching losses, thus achieving a peak efficiency of 98.49%, which is ~1.5% over other state-of-the-art techniques. In addition to that, the reverse power flow capabilities of the designed converter are also verified for different conditions (28-400V and 24-400V), which due to accurate phase detection, portrays a peak converter efficiency of 96.2%. Further, the experimentally obtained open loop response portrays good agreement with the proposed GHA based all-inclusive small-signal model with an

average mismatch of <4.2%. Detailed results for dynamic load change (10-90% load step up and 90-10% load step down) are presented and compared for SMC and PI based controllers. Due to the robustness of the designed hybrid SMC based controller, the results portray an average settling time reduction of 46.4% and over/undershoot reduction of 33%, in addition to maintaining a superior steady state converter efficiency of 98.32% at the rated load, thus adhering to it additional objective of turn-off current minimization at the secondary bridge.

CHAPTER 4

PHASE-DUTY MODULATED LOOP DECOUPLING AND DESIGN OPTIMIZATION FOR A TRIPLE ACTIVE BRIDGE CONVERTER

4.1. Introduction

This chapter thoroughly explains the GHA based modeling technique of a TAB converter. Adhering to the limitations of the SOA works as seen in Chapter 1, the major contributions of this work are as follows: (a) accurate characterization of the TAB topology using frequency-domain GHA modeling to precisely formulate closed-form system design relations and constraints, (b) design of an active cross-gain based decoupled power flow control scheme to eliminate interdependency between the output voltage control loops, (c) implementation of a novel phase/duty modulated three loop control scheme based on power flow optimization to achieve enhanced converter efficiency, and (d) detailed loss modeling of the TAB topology with regard to the most optimum operating point, thus benchmarking the system performance as compared to the conventional control schemes.

The technical aspects covered in the chapter are derived from the study shown in [115, 176-177].

4.2. Design and Modeling of TAB Topology

The DC/DC TAB converter topology is shown in Figure 4.1, which comprises of three full bridges (primary bridge (B_P), secondary bridge (B_S) and tertiary bridge (B_T)), magnetically coupled with each other through a three-winding transformer. L_P, L_S, L_T are

controllable leakage inductances integrated with the transformer for primary, secondary, and tertiary winding, respectively. The transformer turns ratio is $N_P : N_S : N_T$, where N_P, N_S and N_T are the primary, secondary, and tertiary turns, respectively. Further, V_P, V_S, and V_T are midpoint bridge voltages of the primary, secondary, and tertiary bridge, respectively. As observed in Figure 4.1, the power flow polarities are defined for forward direction, i.e., P_P corresponds to the active power sent from the primary bridge, while P_S and P_T are active power flows towards the secondary and tertiary bridge, respectively. The output voltages of B_S and B_T are V_{OS} and V_{OT}, respectively.

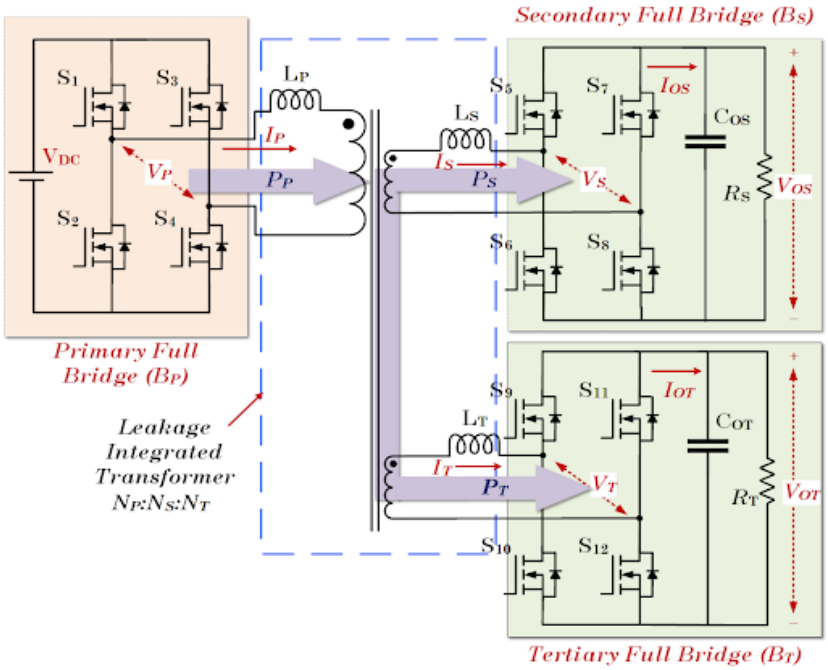


Figure 4.1: TAB Converter Topology

To model the TAB converter topology, with a target to obtain decoupled power transfer, the three bridges involved in the circuit can be portrayed as three individual voltage sources. Thus, with that objective, a three-port equivalent of the TAB topology is designed, with independent voltage sources and corresponding line inductances obtained

from the leakage inductances of the transformer for each winding. Referring to the concept of power flow on transmission lines, Figure 4.2 shows a star connected model of the three voltage sources V_P, V_S and V_T with their respective line inductances (L_P, $L'_S = \left[\frac{N_S}{N_P}\right]^2 L_S$ and $L'_T = \left[\frac{N_T}{N_P}\right]^2 L_T$) and magnetizing inductance (L_m) referred to the primary side. The waveforms of V_P, V_S and V_T resemble a quasi-square shape with their reference phases of 0, $\emptyset_{S,k}$ and $\emptyset_{T,k}$, respectively.

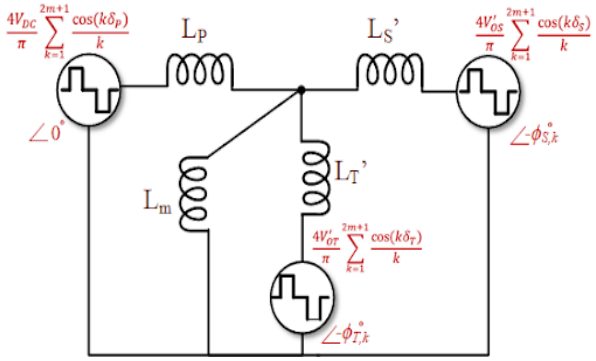


Figure 4.2: Star Equivalent Model of TAB

Additionally, the power flow is controlled by actively varying the duty ratios $\delta_{P,k}$, $\delta_{S,k}$ and $\delta_{T,k}$ corresponding to primary, secondary, and tertiary side full bridges, as depicted in Figure 4.3.

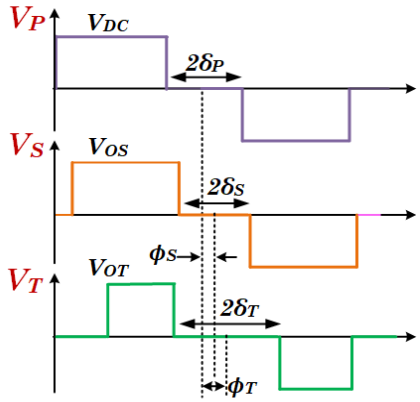


Figure 4.3: Correlation Between Bridge Voltages and Control Parameters

Due to numerous combinations of relations between the control parameters based on the system design specifications, a piecewise time domain analysis turns out multi-case dependent complex process to accurately model the TAB converter topology. Generally, to characterize PWM based converters, fundamental harmonic approximation (FHA) is widely used [178]; however, as the system waveforms deviate from sinusoidal waveshape, the accuracy of analysis obtained using FHA is significantly compromised. Therefore, to account for the higher order harmonics appearing in the port voltages (and currents) without losing generality, the GHA model is adopted in this work to model the system. Implementing GHA based modeling, the port voltage magnitudes can be written as:

$$\left|V_{P,k}\right| = \frac{4V_{DC}}{\pi}\sum_{k=1}^{2m+1}\frac{\cos(k\delta_P)}{k} \tag{4.1}$$

$$\left|V_{S,k}\right| = \frac{4V'_{OS}}{\pi}\sum_{k=1}^{2m+1}\frac{\cos(k\delta_S)}{k} \tag{4.2}$$

$$\left|V_{T,k}\right| = \frac{4V'_{OT}}{\pi}\sum_{k=1}^{2m+1}\frac{\cos(k\delta_T)}{k} \tag{4.3}$$

where, $V'_{OS} = \frac{N_S}{N_P}V_{OS}$ and $V'_{OT} = \frac{N_T}{N_P}V_{OT}$

Referring to Figure 4.2, the current flowing through the magnetizing branch is considerably low as compared to the winding currents. This is typically because the design of the transformer is made in such a way, that the magnetizing inductance (L_m) is 50-100 times larger in value as compared to the winding leakage inductances. Utilizing that design constraint, the magnetizing branch is neglected for obtaining the power flow equations. However, the star equivalent model (as observed in Figure 4.2) is not suited to analyze independent power flows to/from each port, as they are coupled with each other, resulting in a complex analysis. Thus, by implementing equivalent star-to-delta circuit conversion, a new equivalent model is derived and presented in Figure 4.4. Please note that the system is modeled with parameters referred to the primary side; thus, the line inductances placed between the two voltage ports can be formulated as follows:

$$L_{PS} = L_P + L'_S + \frac{L_P L'_S}{L'_T} \tag{4.4}$$

$$L_{ST} = L'_S + L'_T + \frac{L'_S L'_T}{L_P} \tag{4.5}$$

$$L_{PT} = L_P + L'_T + \frac{L_P L'_T}{L'_S} \tag{4.6}$$

Additionally, as observed in Figure 4.4, $P_{PS} = -P_{SP}, P_{ST} = -P_{TS}$ and $P_{PT} = -P_{TP}$ are the power flow between primary and secondary, secondary, and tertiary and primary and tertiary, respectively.

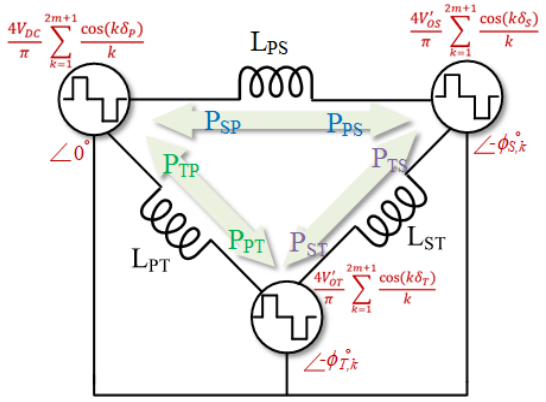


Figure 4.4: Delta Equivalent Model of TAB

The model described in Figure 4.4 can be further split into three independent two port networks, each consisting of two controllable voltage sources connected through a constant line impedance as shown in Figure 4.5. This transformation helps the designer to accurately calculate the RMS value of currents flowing between the ports that are essential for component selection and to characterize the conduction losses in the system. The corresponding phasor diagram for the formulated equivalent model of TAB, accounting for the phase angles between the port voltages and corresponding currents is shown in Figure 4.6. Here, $\theta_{PS,k}$ is the angle between port voltage $V_{P,k}$ and current flowing ($I_{PS,k}$) through the impedance $j\omega k L_{PS}$.

From the phase diagram shown in Figure 4.6, the angles $\theta_{PS,k}$and $\theta_{ST,k}$ can be formulated as follows. The angle information obtained from (4.7-4.8) help finding the instantaneous value of line currents at the switching instants, to accurately synthesize the switching losses in the devices.

$$\theta_{PS,k} = \cos^{-1}\frac{V_{S,k}\sin\emptyset_{S,k}}{V_{P,k}^2+V_{S,k}^2-2V_{P,k}V_{S,k}\cos\emptyset_{S,k}} \tag{4.7}$$

$$\theta_{ST,k} = \cos^{-1}\frac{V_{T,k}\sin\emptyset_{T,k}}{V_{S,k}^2+V_{T,k}^2-2V_{S,k}V_{T,k}\cos\emptyset_{T,k}} \tag{4.8}$$

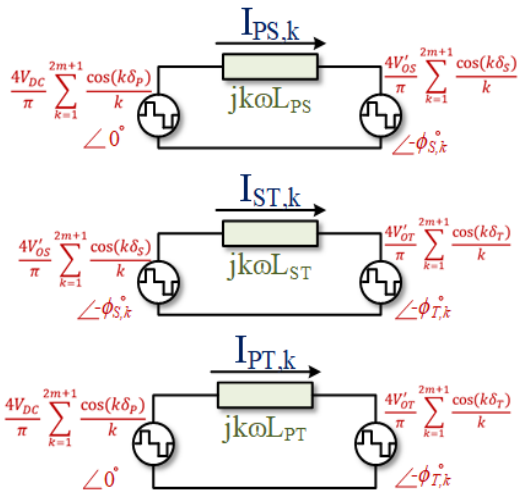


Figure 4.5: Decoupled Two-Port Networks Derived from Delta Equivalent Model

Further, using the independent circuit model described in Figure 4.5, the current amplitudes for the 'kth' order harmonic can be synthesized as:

$$|I_{PS,k}| = \frac{\sqrt{|V_{P,k}^2|+|V_{S,k}^2|-2|V_{P,k}||V_{S,k}|\cos k\emptyset_P}}{\omega k^2 L_{PS}} \tag{4.9}$$

$$|I_{ST,k}| = \frac{\sqrt{|V_{S,k}^2|+|V_{T,k}^2|-2|V_{S,k}||V_{T,k}|\cos(k\emptyset_S - k\emptyset_P)}}{\omega k^2 L_{ST}} \tag{4.10}$$

$$|I_{PT,k}| = \frac{\sqrt{|V_{P,k}^2|+|V_{T,k}^2|-2|V_{P,k}||V_{T,k}|\cos k\emptyset_T}}{\omega k^2 L_{PT}} \tag{4.11}$$

where, $\omega = 2\pi f_s$ and f_s is the switching frequency of the converter. Combining the magnitude and phases obtained using the phasor diagram as shown in Figure 4.6, the time domain expressions of port voltages and line currents can be written as:

$$V_P(t) = \sum_{k=1}^{2m+1}|V_{P,k}|\sin(k\omega t) \tag{4.12}$$

$$V_S(t) = \sum_{k=1}^{2m+1}|V_{S,k}|\sin(k\omega t - k\emptyset_S) \tag{4.13}$$

$$V_T(t) = \sum_{k=1}^{2m+1}|V_{T,k}|\sin(k\omega t - k\emptyset_T) \tag{4.14}$$

$$I_{PS}(t) = \sum_{m=1}^{2k+1} |I_{PS,k}| \sin(k\omega t - k\theta_{PS}) \quad (4.15)$$

$$I_{ST}(t) = \sum_{m=1}^{2k+1} |I_{ST,k}| \sin(k\omega t - k\theta_{ST} - k\emptyset_S) \quad (4.16)$$

$$I_{PT}(t) = \sum_{m=1}^{2k+1} |I_{PT,k}| \sin(k\omega t - k\theta_{PT}) \quad (4.17)$$

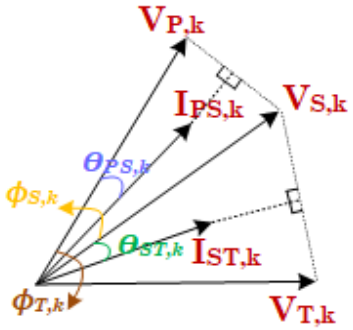


Figure 4.6: Phasor Diagram of TAB System

Corresponding to the time domain expressions as observed in (4.15)-(4.17), the RMS values of currents between two ports are formulated as:

$$I_{PS,k\,(RMS)} = \frac{1}{\sqrt{2}} \sqrt{\sum_{k=1}^{2m+1} |I_{PS,k}|^2} \quad (4.18)$$

$$I_{ST,k\,(RMS)} = \frac{1}{\sqrt{2}} \sqrt{\sum_{k=1}^{2m+1} |I_{ST,k}|^2} \quad (4.19)$$

$$I_{PT,k\,(RMS)} = \frac{1}{\sqrt{2}} \sqrt{\sum_{k=1}^{2m+1} |I_{PT,k}|^2} \quad (4.20)$$

Maintaining the forward power flow convention, the decoupled current equations for the three bridges can be written as:

$$I_P(t) = I_{PS}(t) + I_{PT}(t) \quad (4.21)$$

$$I_S(t) = -I_{ST}(t) + I_{PS}(t) \quad (4.22)$$

$$I_T(t) = I_{PT}(t) + I_{ST}(t) \quad (4.23)$$

To elucidate the correlation between the phase angles, an illustrative set of waveforms for $V_P > V_S > V_T$ is shown in Figure 4.7. As observed, the port voltages in affiliation with their dependency on phase and duty parameters and correspondingly the instantaneous voltages appearing across the leakage inductances dictate the current waveshapes.

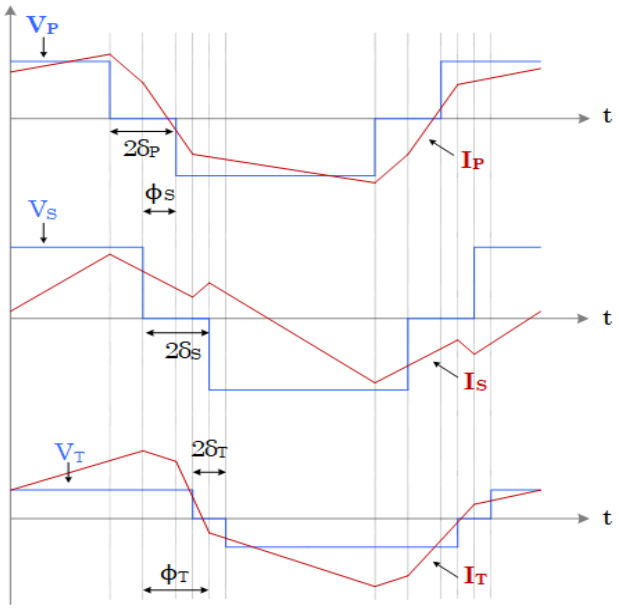


Figure 4.7: Illustrative Bridge Voltage and Current Waveforms of TAB (V_P>V_S>V_T)

Utilizing the magnitudes and phase differences between the node voltages, the power flow between the three nodes can formulated using the concept of power flow on a transmission line as follows:

$$P_{PS} = \frac{8V_{DC}V'_{OS}}{\pi^2\omega L_{PS}} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_P)\cos(k\delta_S)\sin(k\emptyset_S)}{k^3} \tag{4.24}$$

$$P_{ST} = \frac{8V'_{OS}V'_{OT}}{\pi^2\omega L_{ST}} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_S)\cos(k\delta_T)\sin(k(\emptyset_T-\emptyset_S))}{k^3} \tag{4.25}$$

$$P_{PT} = \frac{8V_{DC}V'_{OT}}{\pi^2\omega L_{PT}} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_P)\cos(k\delta_T)\sin(k\emptyset_T)}{k^3} \tag{4.26}$$

Thus, the resultant power flow between the three bridges (as seen in Figure 4.1) can be formulated as:

$$P_P = P_{PS} + P_{PT} \tag{4.27}$$

$$P_S = -P_{PS} + P_{ST} \tag{4.28}$$

$$P_T = -P_{PT} - P_{ST} \tag{4.29}$$

where, power flowing out of the node/bridge is expressed with negative sign convention.

4.3. Decoupled Power Flow Two Loop (DPFTL) Control Scheme

This section builds on the concept of decoupled control scheme to achieve independent power flow control at the two output bridges (B_S and B_P) by explaining the conventional phase shift control and decoupling the two loops by adding cross-gain terms.

4.3.1. Conventional Phase Shift Two-Loop (PSTL) Control Scheme

The conventional PSTL scheme for TAB converter topology is shown in Figure 4.8. This control method is based on phase angle modulation between the pole voltages of the three bridges to control the power flow between the three ports (as observed in (4.27)-(4.29)). In this control scheme, the power flow control is obtained considering $\delta_{X,\forall X\in\{P,S,T\}} = 0^o$, thus implying only phase shift-based control. As observed, the error signals (ε_S and ε_T) generated by comparing the reference output voltages (V_{OS}^* and V_{OT}^*) and the sensed output voltages (V_{OS} and V_{OT}) are passed through a PI controller to obtain the reference phase shifts between the primary and secondary, and primary and tertiary port

voltages respectively ($\emptyset_S$ and $\emptyset_T$). These phase shifts are utilized to generate the secondary and tertiary side half-bridge gate pulses (G_{BS} and G_{BT}) while keeping the primary bridge gate signals (G_{BP}) as reference.

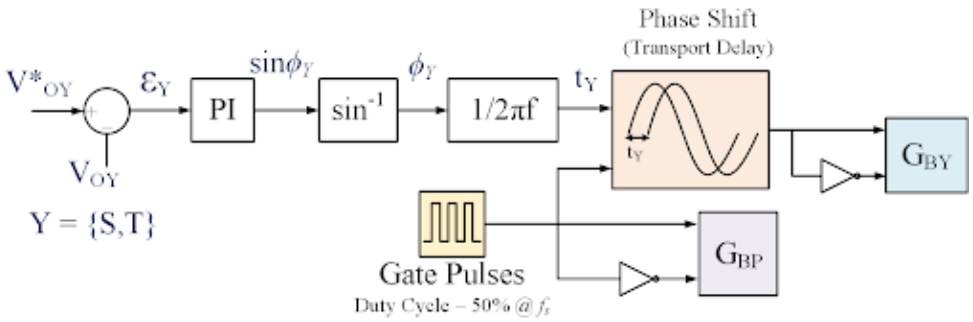


Figure 4.8: Conventional Phase Shift Two-Loop Control Scheme

4.3.2. Decoupled Power Flow Two-Loop (DPFTP) Control Scheme

The conventional PSTL control scheme (as shown in Figure 4.8) achieves voltage regulation at the two output ports by tuning the phase angles $\emptyset$ between the port voltages. However, as seen in (4.27)-(4.29), the power flows between the three ports have a dominant interdependency on the $\emptyset$ and δ of each bridge. For instance, a variation in the load of the secondary bridge results in change in the terminal voltage and correspondingly, the power delivered to the tertiary bridge, and vice-versa holds true.

In order to eliminate this interdependency, the DPFTP control scheme is proposed herewith that aims to eradicate the cross-coupling between the two voltage control loops. This method employs the fundamentals of a multi-input multi-output (MIMO) [179] system and establishes mathematical relationships between the various input and output signals. As shown in Figure 4.9, a MIMO system is developed using two control inputs

(W1(s) and W2(s)), corresponding to which the MIMO plant provides two outputs (Y1(s) and Y2(s)).

Figure 4.9: Figurative Representation of MIMO System

The input matrix W(s) and corresponding plant output matrix Y(s) can be denoted as follows:

$$W(s) = \begin{bmatrix} W_1(s) \\ W_2(s) \end{bmatrix} \tag{4.30}$$

$$Y(s) = \begin{bmatrix} Y_1(s) \\ Y_2(s) \end{bmatrix} \tag{4.31}$$

Further, using the concept of MIMO system, a control scheme (Figure 4.10) is devised to achieve the reference values of $Y_{x,ref}(s)$ by defining a plant, which involves a cross-coupling between the two control loops.

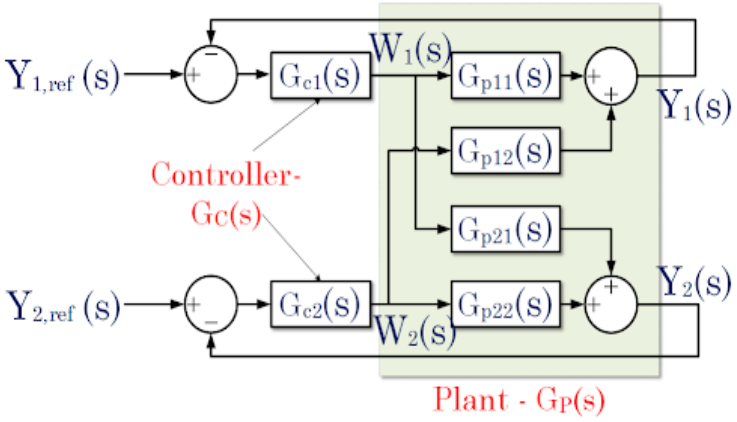


Figure 4.10: MIMO Based Closed Loop Control System

The plant transfer function $G_p(s)$, as observed in Figure 4.10, corresponding to the developed model for the referred MIMO system can be expressed as a 2x2 matrix, as shown below:

$$G_p(s) = \begin{bmatrix} G_{P11}(s) & G_{p12}(s) \\ G_{p21}(s) & G_{p22}(s) \end{bmatrix} \tag{4.32}$$

In addition to that, $G_C(s)$ is the controller transfer function for each loop that ensures active tracking of the defined reference quantity. As seen in (4.32), the diagonal coefficients i.e., the self-loop gains ($G_{P11}(s)$ and $G_{P22}(s)$), provide a relation between the inputs $W_1(s)$ and $W_2(s)$ in context to their corresponding outputs $Y_1(s)$ and $Y_2(s)$. On the other hand, the cross-coupling terms $G_{P12}(s)$ and $G_{P21}(s)$ are defined to establish the interdependence of $Y_1(s)$ on $W_2(s)$ and $Y_2(s)$ on $W_1(s)$, respectively. Employing the plant gains in the closed loop control system, as seen in Figure 4.9, the resultant output variables $Y_1(s)$ and $Y_2(s)$ can be formulated as:

$$Y_1(s) = G_{p11}(s)W_1(s) + G_{p12}(s)W_2(s) \tag{4.33}$$

$$Y_2(s) = G_{p21}(s)W_1(s) + G_{p22}(s)W_2(s) \tag{4.34}$$

For enabling a decoupled control, it is crucial to curb or eliminate the effect of cross-coupling terms by modifying the control loop, which can be executed by adding a counter-reactive cross gain term. Corelating this with the TAB converter system, as observed in the PSTL control scheme, the plant transfer functions of each voltage control loop are interdependent, which mimic a MIMO system. Thus, the formulation and design of DPFTP scheme is done in such a way that a cross-gain term is introduced in the closed loop system that cancels out the effect of relative change in the phase angle ($\emptyset$)

corresponding to a load change in any of the two output bridges. This facilitates individual power flow control for both the bridges, without any change in the steady state outputs of either of the bridges.

The power transfer to the secondary bridge, as seen in (4.28), can be written as:

$$P_S = -K_{PS} \sum_{k=1}^{2m+1} \frac{\sin(k\emptyset_S)\cos(k\delta_P)\cos(k\delta_S)}{k^3} - K_{ST} \sum_{k=1}^{2m+1} \frac{\sin(k(\emptyset_S-\emptyset_T))\ \cos(k\delta_S)\cos(k\delta_T)}{k^3} \quad (4.35)$$

where, $K_{PS} = \frac{8V_{DC}V'_{HV}}{\pi^2\omega L_{PS}}$ and $K_{ST} = \frac{8V'_{HV}V'_{LV}}{\pi^2\omega L_{ST}}$

The effective power transfer to the secondary bridge can be also written as the power output at that bridge, which is dependent on the load R_S. Considering no losses in the system, the expression for secondary bridge power P_S can be further expressed as:

$$P_S = \frac{V_{OS}^2}{R_S} \quad (4.36)$$

$$V_{OS} = \sqrt{P_S R_S} = -K_1\sqrt{\sum_{k=1}^{2m+1} \frac{\sin(k\emptyset_S)}{k}} + K_2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin(k(\emptyset_S-\emptyset_T))}{k}} \quad (4.37)$$

where, $K_1 = \sqrt{R_S K_{PS} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_P)\cos(k\delta_S)}{k^2}}$ and $K_2 = \sqrt{R_S K_{ST} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_S)\cos(k\delta_T)}{k^2}}$

Further, to define a correlation between the phase control parameters $\emptyset_S$ and $\emptyset_T$, identifying their effect on the secondary port voltage V_S, a small signal equivalent of the expression in (4.37) is formulated as follows:

$$\Delta V_S = -\frac{K_1 \sum_{k=1}^{2m+1} \cos(k\emptyset_S)}{2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin(k\emptyset_S)}{k}}} \Delta\emptyset_S + \frac{K_2 \sum_{k=1}^{2m+1} \cos(k(\emptyset_T-\emptyset_S))}{2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin\left(k(\emptyset_T-\emptyset_S)\right)}{k}}} (\Delta\emptyset_T - \Delta\emptyset_S) \quad (4.38)$$

Taking (4.38) as a reference, a small signal equivalent for formulating the dependence of V_T on $\emptyset_S$ and $\emptyset_T$ is shown as follows:

$$\Delta V_T = -\frac{K_3 \sum_{k=1}^{2m+1} \cos(k\emptyset_T)}{2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin(k\emptyset_T)}{k}}} \Delta\emptyset_T - \frac{K_4 \sum_{k=1}^{2m+1} \cos(k(\emptyset_T - \emptyset_S))}{2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin\left(k(\emptyset_T - \emptyset_S)\right)}{k}}} (\Delta\emptyset_T - \Delta\emptyset_S) \tag{4.39}$$

where, $K_3 = \sqrt{R_T K_{PT} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_P)\cos(k\delta_T)}{k^2}}$ and $K_4 = \sqrt{R_T K_{ST} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_T)\cos(k\delta_S)}{k^2}}$

Compiling (4.38) and (4.39), the small signal plant transfer function, as referred in Figure 4.10 for TAB, can be described in a gain-matrix format where the matrix entries are formulated using generalized harmonic approximation (GHA) model.

$$\begin{bmatrix} \Delta V_S \\ \Delta V_T \end{bmatrix} = \begin{bmatrix} A_1 & A_2 \\ B_1 & B_2 \end{bmatrix} \begin{bmatrix} \Delta\emptyset_S \\ \Delta\emptyset_T \end{bmatrix} \tag{4.40}$$

where,

$$A_1 = -\frac{K_1 \sum_{k=1}^{2m+1} \cos(k\emptyset_S)}{2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin(k\emptyset_S)}{k}}} - \frac{K_2 \sum_{k=1}^{2m+1} \cos(k(\emptyset_T - \emptyset_S))}{2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin\left(k(\emptyset_T - \emptyset_S)\right)}{k}}} \tag{4.41}$$

$$A_2 = \frac{K_2 \sum_{k=1}^{2m+1} \cos(k(\emptyset_T - \emptyset_S))}{2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin\left(k(\emptyset_T - \emptyset_S)\right)}{k}}} \tag{4.42}$$

$$B_1 = \frac{K_4 \sum_{k=1}^{2m+1} \cos(k(\emptyset_T - \emptyset_S))}{2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin\left(k(\emptyset_T - \emptyset_S)\right)}{k}}} \tag{4.43}$$

$$B_2 = -\frac{K_3 \sum_{k=1}^{2m+1} \cos(k\emptyset_T)}{2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin(k\emptyset_T)}{k}}} - \frac{K_4 \sum_{k=1}^{2m+1} \cos(k(\emptyset_T - \emptyset_S))}{2\sqrt{\sum_{k=1}^{2m+1} \frac{\sin\left(k(\emptyset_T - \emptyset_S)\right)}{k}}} \tag{4.44}$$

As observed in (4.40), the diagonal components of matrix A_1 and B_2 portray the self-dependence of V_S on $\emptyset_S$ and V_T on $\emptyset_T$ respectively. On the other hand, the cross-diagonal terms, i.e., A_2 and B_1 denote the cross-coupling terms referring to the cross-gains $G_{p12}(s)$ and $G_{p21}(s)$. To curb their effect on either of the loops, the updated MIMO system is depicted in Figure 4.11. It is further important to note that the gain coefficients depend on the operating point i.e., instantaneous phase and duty terms.

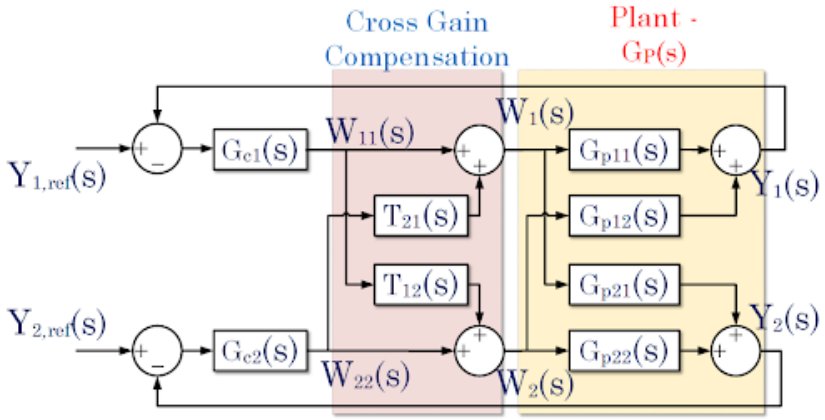


Figure 4.11: Updated MIMO Based Closed Control System with Cross Gain Terms

As observed in Figure 4.11, the cross-compensation terms $T_{12}(s)$ and $T_{21}(s)$ are derived in a way that the net contribution of one loop output to the other plant input becomes zero.

$$W_{11}(s)T_{12}(s)G_{p22}(s) + W_{11}(s)G_{p21}(s) = 0 \tag{4.45}$$

$$T_{12}(s) = -\frac{G_{p21}(s)}{G_{p22}(s)} \tag{4.46}$$

$$W_{22}(s)T_{21}(s)G_{p11}(s) + W_{22}(s)G_{p12}(s) = 0 \tag{4.47}$$

$$T_{21}(s) = -\frac{G_{p12}(s)}{G_{p11}(s)} \tag{4.48}$$

Referring to (4.45)-(4.48), the cross-gain terms for the TAB loop can be written as follows.

$$T_{12}(s) = -\frac{A_2}{B_2} \text{ and } T_{21}(s) = -\frac{A_1}{B_1} \tag{4.49}$$

Thus, using these cross-gain terms, the updated two-loop decoupled control system for a TAB is shown in Figure 4.12.

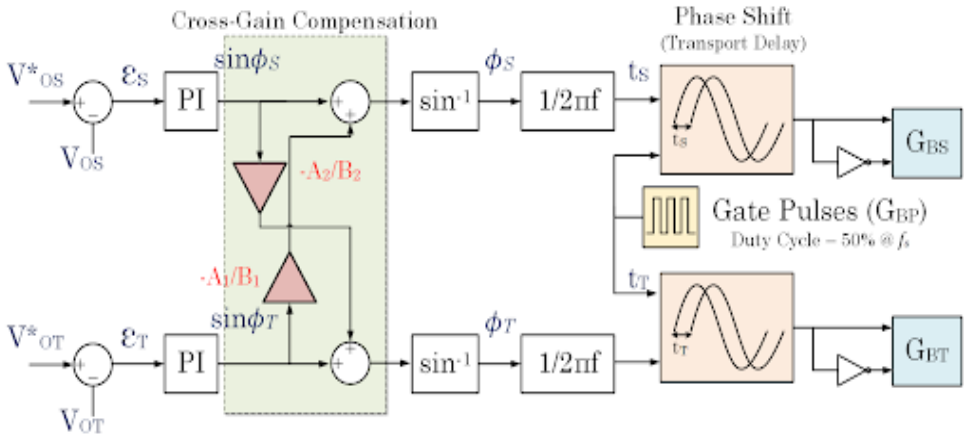


Figure 4.12: Decoupled Power Flow Two Loop Control Scheme

It is noteworthy that these cross-gain terms need to be adaptively updated after each execution cycle of the control loop. The execution time of each sample of sensed output voltage along with the cross-gain term updation in TMS320F28335 DSP is $4.2\mu s$, which is lesser than the program sampling time of $10\mu s$ to avoid any signal aliasing and distortions. As the DSP does not include a defined function for finding the inverse sine of any given input, a Taylor series based polynomial expansion of $\sin^{-1} x$ is defined in the controller, which is accounted for in the execution time calculation.

4.4. Phase/Duty Modulated Three Loop Control with Power Flow Optimization

The DPFTP control is implemented by taking all full-bridge duty ratios i.e., δ_X (X = P, S, T) to be zero. Even though the DPFTP achieves decoupled power flow at the two output bridges, it fails to account for the switching and conduction losses occurring in the active devices at that particular operating point. Thus, to expand the horizon of control of a TAB topology, with an objective to enhance the overall conversion efficiency, a comprehensive study is presented in this section, that evaluates the requirements and conditions of involving a third loop dependent on the duty control parameter. The motivation of introducing the third loop is to ensure the sum of three reference power transfer levels ($P_{PS}^*, P_{ST}^*, P_{TP}^*$) to zero, in order to achieve zero circulating active power loss. This is done by synthesizing an optimization algorithm that is defined with an objective to reduce the system losses and defining constraints that bound the solution data space (i.e., φ, δ) within reasonable limits, adhering to the system dynamics of the TAB topology. In addition to achieving the objective of minimized losses, the optimization algorithm also provides resourceful design insights in terms of choosing the optimum values of system parameters such as the primary/secondary/tertiary leakage inductances for ensuring desired power transfer between the bridges.

A flowchart depicting the overall optimization algorithm to obtain optimized values of δ_X (X = P, S, T), while accounting for the required leakage inductances is shown in Figure 4.13. The 'power transfer check' stage defines the constraint for power transfer between the three bridges by taking user-defined design specifications and targets. The power transfer constraints provide optimized values of leakage inductances, which corelate

to the power transfer capabilities of each bridge. Using the optimized leakage inductance along with the real-time sensed values of V_{OS} and V_{OT} and the synthesized phase shift parameters, the optimization program provides optimum values of δ_X, which are then utilized to calculate reference values of inter-port power transfer, ensuring minimum losses.

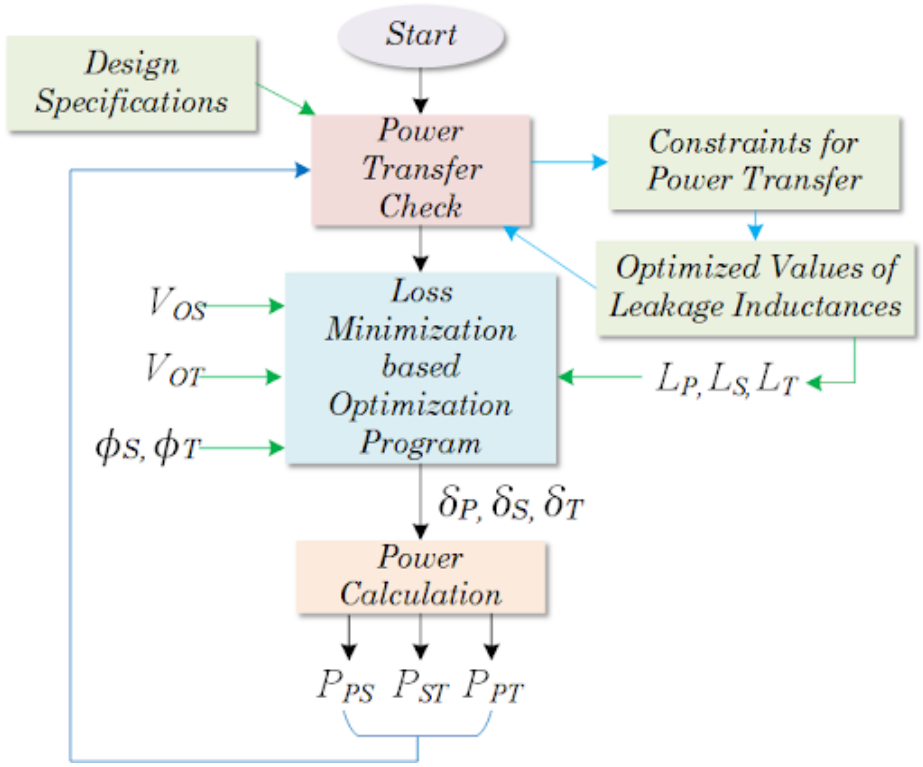


Figure 4.13: Loss Minimization-Based Optimization Algorithm

Corelating the power equations, as stated in (4.27)-(4.29), the optimization program for minimizing the overall losses in the system is defined as follow:

Objective: Min $\sum_{H=P,S,T} P_H$ (4.50)

Constraints:

The following constraints are formulated to account for the reference power calculations and to ensure that the desired power flow is achieved between the three bridges.

$$P_{PS}^{*} = -\frac{2}{3}P_S - \frac{1}{3}P_T \tag{4.51}$$

$$P_{ST}^{*} = \frac{1}{3}P_S - \frac{1}{3}P_T \tag{4.52}$$

$$P_{PT}^{*} = -\frac{1}{3}P_S - \frac{2}{3}P_T \tag{4.53}$$

The following constraints are laid to synthesize the values of the duty control parameters with a motive to establish a correlation between the system variables and the reference power transfer magnitudes.

$$\sum_{k=1}^{2m+1}\cos(k\delta_P) = \frac{P_{PS}^{*}}{K_P V_{DC} V'_{OS} \sum_{k=1}^{2m+1}\frac{(\sin(k\emptyset_S)\cos(k\delta_S))}{k^3}} \quad ; \text{where } K_P = \frac{8}{\pi^2\omega L_{PS}} \tag{4.54}$$

$$0 < \sum_{k=1}^{2m+1}\cos(k\delta_P) < 1 \tag{4.55}$$

$$\sum_{k=1}^{2m+1}\cos(k\delta_S) = \frac{P_{ST}^{*}}{K_S V'_{OS} V'_{OT} \sum_{k=1}^{2m+1}\frac{(\sin(k(\emptyset_T-\emptyset_S))\cos(k\delta_T))}{k^3}} ; \text{ where } K_S = \frac{8}{\pi^2\omega L_{ST}} \tag{4.56}$$

$$0 < \sum_{k=1}^{2m+1}\cos(k\delta_S) < 1 \tag{4.57}$$

$$\sum_{k=1}^{2m+1}\cos(k\delta_T) = \frac{P_{PT}^{*}}{K_S V_{DC} V'_{OT} \sum_{k=1}^{2m+1}\frac{(\sin(k\emptyset_T)\cos(k\delta_P))}{k^3}} \text{ ; where } K_T = \frac{8}{\pi^2\omega L_{PT}} \tag{4.58}$$

$$0 < \sum_{k=1}^{2m+1}\cos(k\delta_T) < 1 \tag{4.59}$$

The following constraints are framed to provide insightful design conditions to find the upper bounds of leakage inductances required to ensure desired power transfer at various ports.

$$P_P = \frac{8V_{DC}V'_{OS}}{\pi^2\omega L_{PS}} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_P)\cos(k\delta_S)\sin(k\emptyset_S)}{k^3} +$$

$$\frac{8V_{DC}V'_{OT}}{\pi^2\omega L_{PT}} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_P)\cos(k\delta_T)\sin(k\emptyset_T)}{k^3} \geq P_P^* \quad (4.60)$$

$$P_S = \frac{8V_{DC}V'_{OS}}{\pi^2\omega L_{PS}} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_P)\cos(k\delta_S)\sin(-k\emptyset_S)}{k^3} +$$

$$\frac{8V'_{OS}V'_{OT}}{\pi^2\omega L_{ST}} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_S)\cos(k\delta_T)\sin(k(\emptyset_T-\emptyset_S))}{k^3} \geq P_S^* \quad (4.61)$$

$$P_T = \frac{8V_{DC}V'_{OT}}{\pi^2\omega L_{PT}} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_P)\cos(k\delta_T)\sin(-k\emptyset_T)}{k^3} +$$

$$\frac{8V'_{OS}V'_{OT}}{\pi^2\omega L_{ST}} \sum_{k=1}^{2m+1} \frac{\cos(k\delta_S)\cos(k\delta_T)\sin(k(\emptyset_S-\emptyset_T))}{k^3} \geq P_T^* \quad (4.62)$$

The following constraints are formulated to ensure that the calculated losses are constrained within the objective function, thus adhering to the target of achieving minimized losses.

$$^{\#} \sum_{H=P,S,T} P_H \geq \sum P_{switching} + \sum P_{conduction} + P_{cap,ESR} + P_{Magnetics} \quad (4.63)$$

[#]Detailed formulation and classification of the mentioned losses is provided in Section 4.5. The third control loop, as shown in Figure 4.14 is designed to ensure that the power transfer between secondary and tertiary bridge (P_{ST}), calculated online through GHA modeling, tracks its reference value (P_{ST}^*). The secondary-side full-bridge duty ratio (δ_S) is modulated in the third loop, while keeping δ_P and δ_T to be zero for minimizing the objective function. It is noteworthy that the tertiary-side full-bridge duty ratio (δ_T) can also be the control variable in third loop because P_{ST} depends on both δ_S and δ_T. The generated error (ε_{PST}) is then processed in a PI controller to obtain the value of δ_S, by taking inverse cosine of the PI output. Finally, the modulated values of the control parameters are used to

generate the required gating pulses according to the phase relation as portrayed in Figure 4.3.

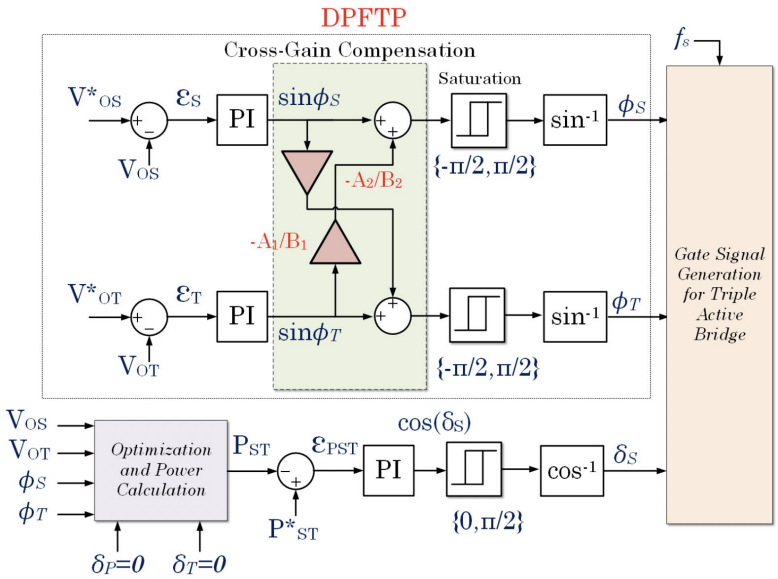


Figure 4.14: Phase/Duty Modulated Three Loop Control

4.5. Concept Verification Through Simulation and Experimental Analysis

This section focuses on quantifying the implications of the proposed three loop control scheme as compared to the PSTL and DPFTP control schemes. Figure 4.15 illustratively provides design considerations regarding the maximum allowable leakage inductance required to enable desired power flow at various bridges. Adhering to the load requirements as mentioned in Table 4-I, for $\{P_{OS}, P_{OT}\} = \{156,144\}W$, the optimized values of leakage inductances are $\{L_P, L_S, L_T\} = \{10.34\ \mu, 10.18\mu, 0.14\mu\}H$.

With respect to the TAB converter applications in onboard charging of light EV applications [102-103], a list of key design specifications for simulation and experimental analyses is shown in Table 4-I. To study the effectiveness of the optimization algorithm

for the TAB topology using the design specifications, the objective function is plotted with respect to the phase shift control parameters ($\emptyset_S$ and $\emptyset_T$), as shown in Figure 4.16. As observed, the global minima of the objective function, resulting in lower system losses is achieved at $\{\sum_{H=P,S,T} P_H, \emptyset_S, \emptyset_T\} = \{10.554W, 0.038\,rad, 0.152\,rad\}$.

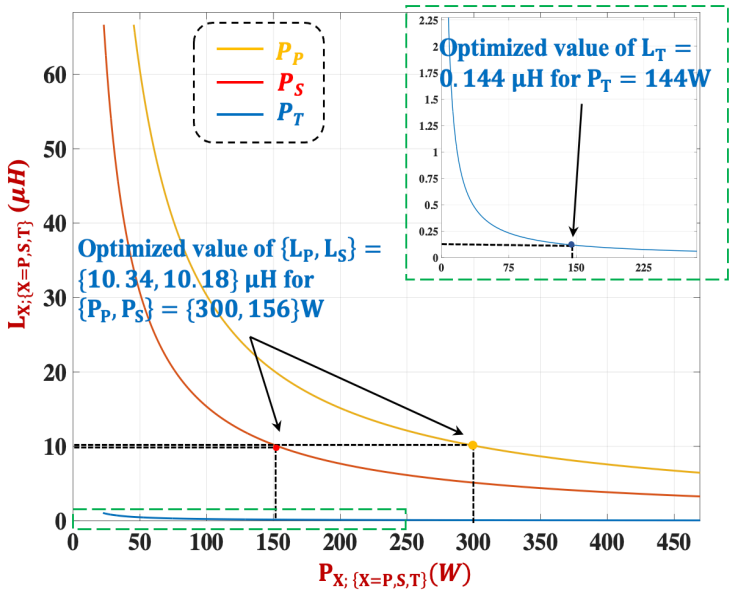


Figure 4.15: Plot to Determine the Optimized Value of Lx

Further, to analyze the effectiveness of the obtained operating points in terms of efficiency improvement, surface plots targeting total conduction and switching losses are provided in Figure 4.17 and 4.18. A comprehensive loss analysis based on the achieved operating points and corresponding values for the semiconductor losses is mentioned in Section 4.5. Figure 17 shows that at the optimum feasible operating point, the coordinates obtained for conduction losses involved in the system are $\{\sum P_{conduction}, \emptyset_S, \emptyset_T\} = \{5.69W, 0.038\,rad, 0.152\,rad\}$. Similarly, for the switching losses, the system performance at optimum operating points is obtained at $\{\sum P_{switching}, \emptyset_S, \emptyset_T\} = \{1.18W, 0.038\,rad, 0.152\,rad\}$.

Table 4.1: Design Specifications for TAB Converter

Parameters	Values
Input voltage (V_{DC})	80V
Secondary/Tertiary Output Voltage (V_{OS} /V_{OT})	80V/12V
Secondary/Tertiary Output Power (P_{OS}/P_{OT})	156W/144W
Transformer Turns Ratio (N_1, N_2, N_3)	8:8:1
Leakage Inductances (L_1,L_2,L_3)	10µH, 10µH, 0.14µH
Secondary Output Capacitor (C_{OS})	200µF
Tertiary Output Capacitor (C_{OT})	5mF
Switching frequency (f_s)	100 kHz

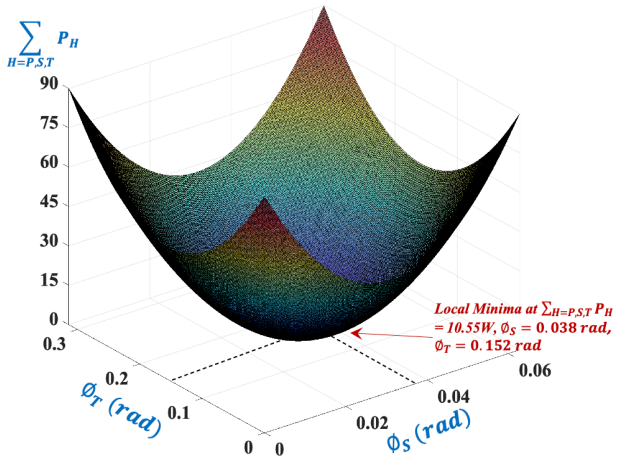


Figure 4.16: Surface Plot of the Loss Minimization Objective Function with Respect to $\emptyset_S$ and $\emptyset_T$

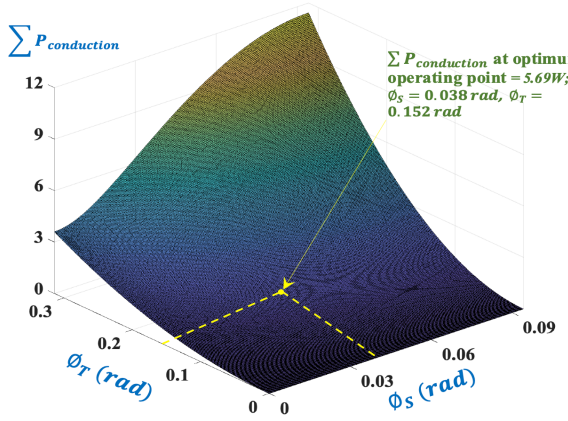


Figure 4.17: Surface Plot of the Conduction Losses at Optimum Operating Point with Respect to $\emptyset_S$ and $\emptyset_T$

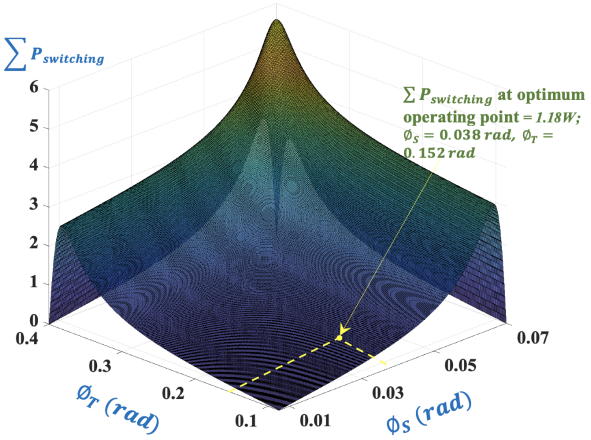


Figure 4.18: Surface Plot of the Switching Losses at Optimum Operating Point with Respect to $\emptyset_S$ and $\emptyset_T$

4.5.1. Simulation Analysis

Further, to provide proof-of-concept verification of the proposed DPFTP and the three-loop control in affiliation with the optimization module, an exhaustive simulation analysis, implemented in MATLAB Simulink environment is presented using the design specifications as mentioned in Table 4.1.

For the DPFTP control scheme, the duty control parameter $\delta_X (X = P, S, T)$ is taken to be zero for only engaging two loops in the control scheme. Here, the voltage regulation and power flow control are obtained using only phase shift modulation. As seen in Figure 4.19, the primary port voltage V_P, depicts a square waveshape (as $\delta_P = 0\, rad$) with its peak magnitude corresponding to the input DC voltage ($V_{DC} = 80V$). Corresponding to the transformer turns ratio, a square voltage waveform is also seen in at the secondary port (V_S) with a magnitude of 80V, corresponding to the secondary bridge load output voltage requirement, and a phase shift ($\emptyset_S$) of 11.94^o. The output voltage at the secondary bridge (V_{OS}) portrays a well-regulated DC output waveform, with a ripple content of less than 1%. Further, with respect to the voltage appearing across the primary leakage inductance, current I_P follows a trapezoidal waveshape with an RMS value of 4.05A.

Figure 4.20 shows the waveforms corresponding to the tertiary bridge. As observed, the tertiary bridge voltage V_T also follows a square waveshape with a magnitude of 12V, corresponding to the designed transformer turns ratio, with a phase shift of $52.7^0$with respect to the primary port voltage (V_P). The control scheme achieves the required regulated DC output (12V) at the tertiary output, with a ripple content of less than 2%.

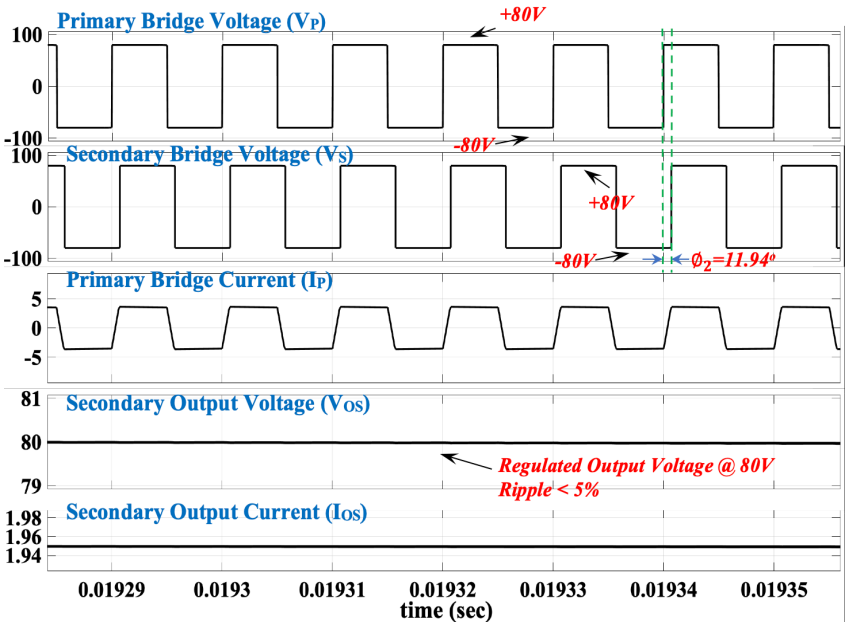


Figure 4.19: Steady State Simulation Waveforms [Y – axis: V_P – 100V/div, V_S – 100V/div, I_P – 5A/div, V_{OS} – 1V/div, I_{OS} – 20mA/div; X – axis: Time (t) – 10µs/div]

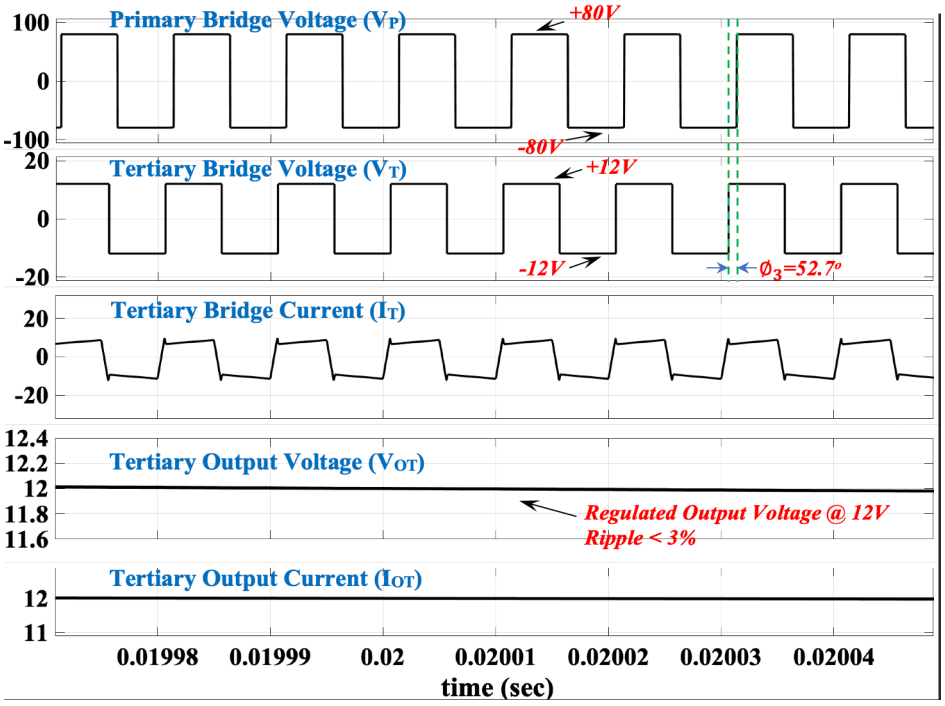


Figure 4.20: Steady State Simulation Waveforms [Y – axis: V_P – 100V/div, V_T – 20V/div, I_T – 20A/div, V_{OT} – 0.2V/div, I_{OT}– 1A/div; X – axis: Time (t) – 10µs/div]

To elucidate the effectiveness of the DPFTP control scheme, with a target to provide decoupled control of output voltages and load power, a simulation scenario with dynamic load change is presented in Figure 4.21. As observed, the load at the tertiary bridge is reduced to 50% of its rated capacity ($144W \rightarrow 72W$) at $t = 0.15\ sec$. Due to the active cross gain compensating blocks placed to nullify the coupling between the output voltage control loops, the load change at the tertiary bridge does not affect the dynamics of the secondary bridge output and vice-versa. As observed, during the load change instant, V_{OT} stays constant at 12V, while the load current reduces to 6A, corresponding to the 50% drop in load. However, the voltage fluctuation cause in V_{OS} is relatively negligible (<4%), which asymptotically decays in less than 15ms, thus keeping the output voltage and load current of the secondary bridge unaffected.

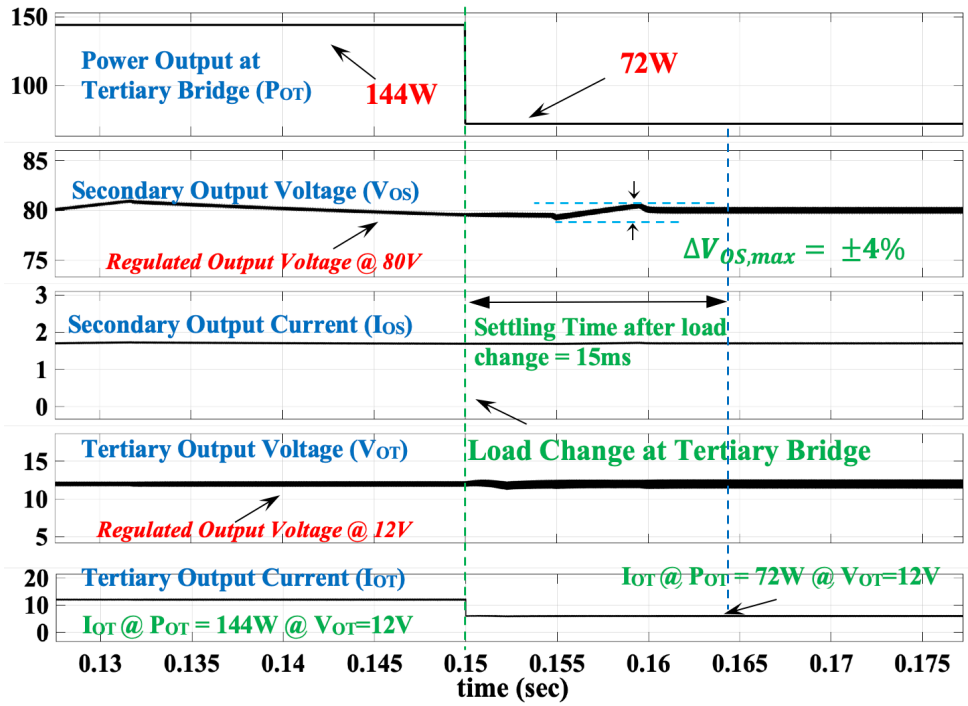


Figure 4.21: Dynamic Load Change Simulation Waveforms [Y – axis: P_{OT} – 50W/div, V_{OS} – 5V/div, I_{OS} – 1A/div, V_{OT} – 5V/div, I_{OT} – 10A/div; X – axis: Time (t) – 5ms/div]

Further, the three-loop control scheme (Figure 4.14), designed and implemented with respect to the specifications mentioned in Table 4.1, observes the benefit in the reduction in the sum of mean square current due to the inclusion of loss objective function in the loop design. Figure 4.22 shows simulation result of a case with δ_S included as the third control parameter. As observed, the value of δ_S obtained from the control scheme is 6.874^0, which matches with the theoretical outcome of the loss minimization block. An instance affirming this result can be pointed out by realizing the reduction in the RMS value of the primary current from 4.05A for DPFTP control scheme to 3.84A for the proposed three-loop control scheme.

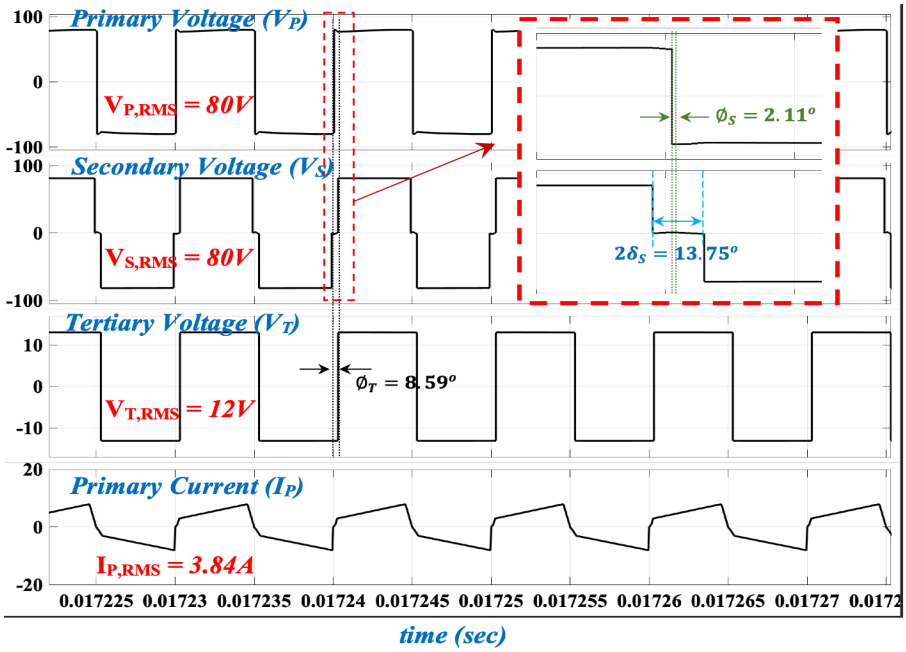


Figure 4.22: Simulation Results of Three Loop Control (Y-axis: V_P=100V/div, V_S=100V/div, V_T=10V/div, I_P=20A/div; X-axis: Time - 5µs/div)

4.5.2. Experimental Analysis

To further technically support the analyses presented in the simulation results, a hardware proof-of-concept circuit, shown in Figure 4.23 is developed for the same specifications.

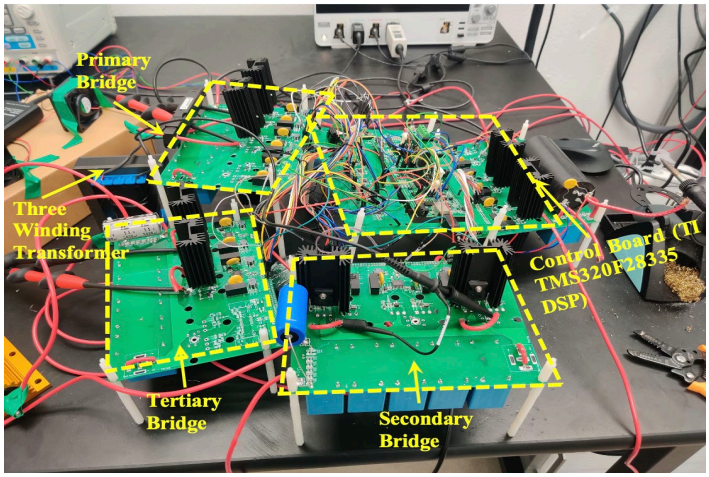


Figure 4.23: Experimental Set Up for TAB Converter

Figure 4.24 shows the experimental results obtained from the DPFTP control scheme adhering to the bridge load requirements. As observed, the phase shifts obtained at steady state operation are $\{\emptyset_s, \emptyset_T\} = \{14.79^0, 46.44^0\}$. Further, the primary bridge current (I_P) portrays a trapezoidal waveshape, with an RMS value of 3.95A that closely matches with the simulation results.

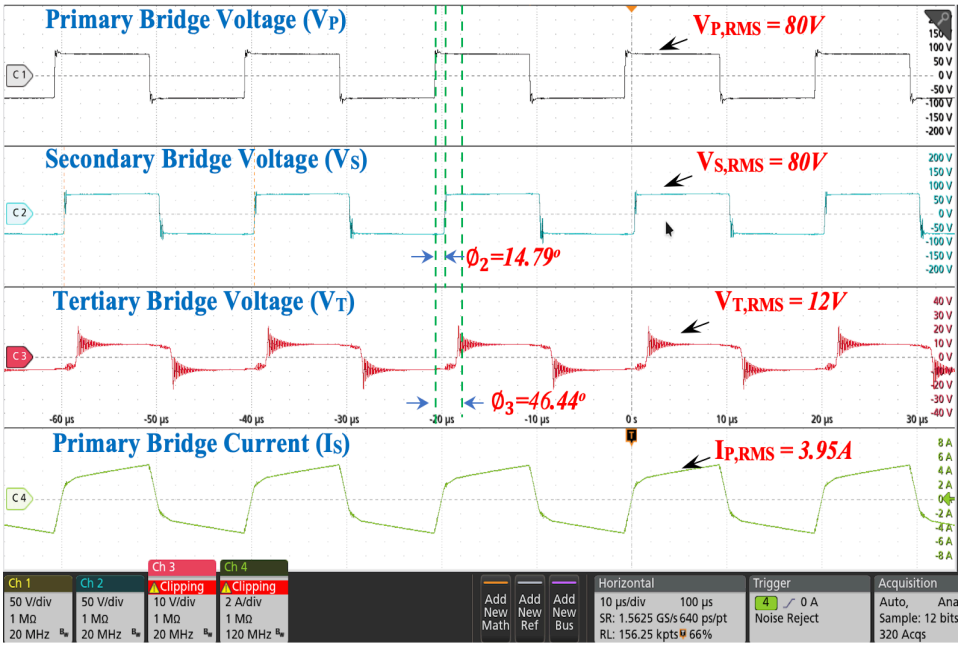


Figure 4.24: Steady State Experimental Results with DPFTL [Y – axis: V_P – 50V/div, V_S – 50V/div, V_T – 10V/div, I_P – 2A/div]

Further the steady state experimental results implementing the three-loop control scheme are shown in Figure 4.25. As observed, the optimized values of the three control parameters in steady state are $\{\emptyset_S, \emptyset_T, \delta_S\} = \{3.12^0, 8.92^0, 7.39^0\}$. The corresponding loss analysis at this rated load condition is described in Section 4.5, which depicts the efficiency improvement of 4.97% and 2.94% over the PSTL and DPFTP control schemes, respectively.

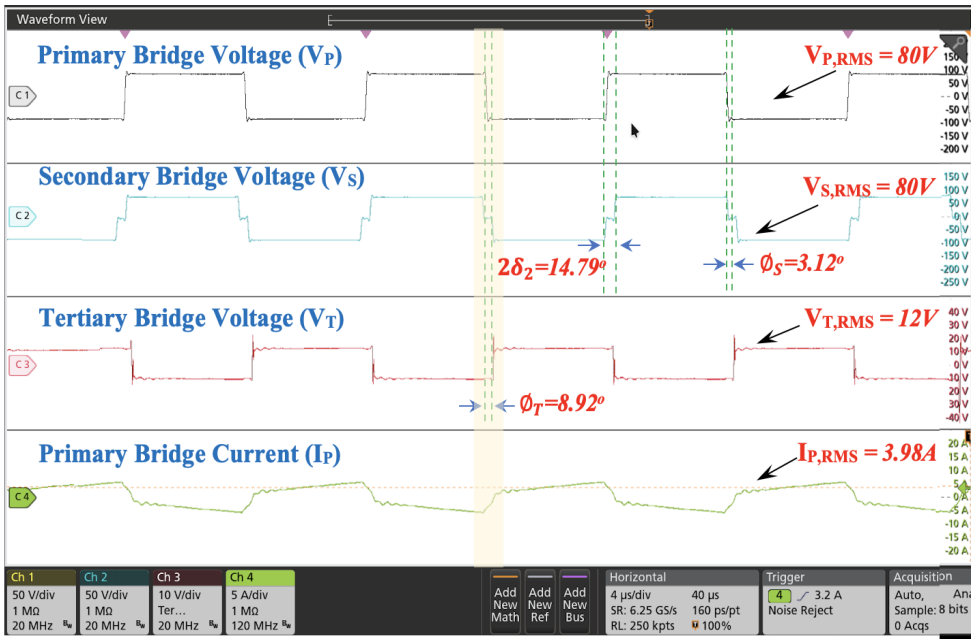


Figure 4.25: Steady State Experimental Results with Three Loop Control [Y – axis: V_P – 50V/div, V_S – 50V/div, V_T – 10V/div, I_P – 2A/div]

Further, to analyze the dynamic response and decoupling effect between the two voltage control loops using the three-loop control method, a load transient is performed on the tertiary side. The corresponding results are depicted in Figure 4.26. At the load change instant, V_{OT} observes an overshoot of 0.8V and settles down back to its reference value of 12V. On the other hand, corresponding to the tertiary side load change, the output current drops from 12A (at 144W rated load) to 6A (at 72W (50% of the rated load)). Due to loop decoupling, the secondary output (V_{OS}) does not experience any fluctuation, providing a stiffly regulated 80Vdc output voltage, thus proving a strong correlation between the theoretical analyses and experimental results.

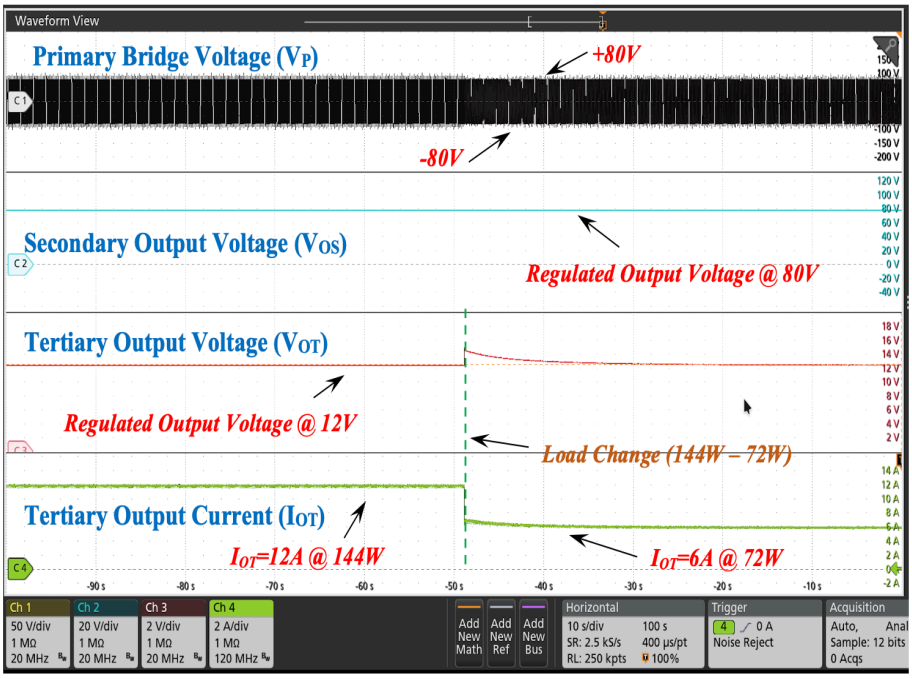


Figure 4.26: Dynamic Load Change Implemented with Three Loop Control [Y – axis: V_P – 50V/div, V_{OS} – 20V/div, V_{OT} – 10V/div, I_{OT} – 2A/div]

4.6. Loss Analysis and Efficiency Improvement Mapping

This section provides a complete loss model of the TAB topology and classifies the loss magnitudes by splitting them into various categories – semiconductor losses, capacitor ESR losses and losses pertaining to magnetics. A comparative study for each loss component is also presented for the three-loop control scheme with the PSTP and DPFTP control scheme, in order to quantify the efficiency improvement objective.

To understand the contribution of switching losses, it is important to analyze the current polarities during the switching instants. Figure 4.27 shows the waveforms of drain to source voltage with the drain current for switches in each bridge. As observed, the devices in primary and secondary bridge undergo ZVS ($I_D < 0$ at switching instants), and

thus, only incur turn-off losses. However, the tertiary bridge devices undergo hard switching ($I_D > 0$) and hence both turn-on and turn-off losses need to be accounted for.

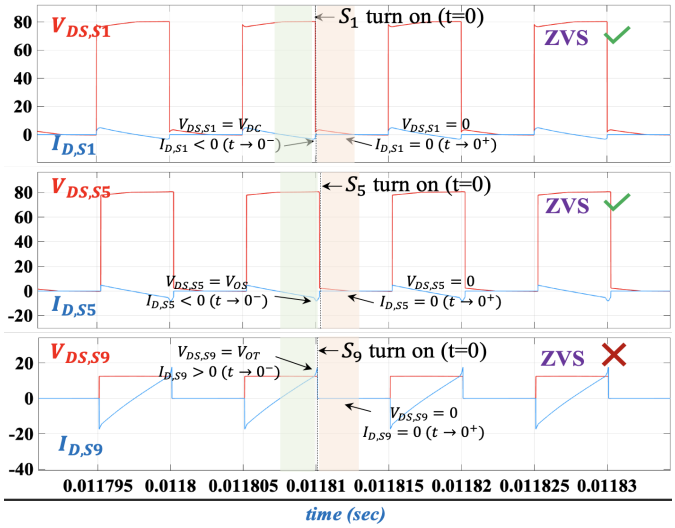


Figure 4.27: Simulation Results for Identifying ZVS Conditions (Y-axis: $V_{DS,S1}$=20V/div, $V_{DS,S5}$=20V/div, $V_{DS,S9}$=20V/div, $I_{D,S1}$=20A/div, $I_{D,S5}$=20A/div, $I_{D,S9}$=20A/div; X-axis: Time - 5µs/div)

The switching losses for each of the tertiary bridge switches ($P_{SW,T}$) can be accurately calculated by finding the drain current at the switching instant.

$$I_{T,sw} = I_T(t=0) = \sum_{m=1}^{2k+1} \left|I_{PT,k}\right| \sin(-k\theta_{PT}) - \sum_{m=1}^{2k+1} \left|I_{ST,k}\right| \sin(-k\theta_{ST} - k\emptyset_S) \quad (4.64)$$

$$P_{SW,T} = \frac{1}{2} V_{OT} I_{T,sw} (t_{1,on} + t_{2,on}) f_{sw} \quad (4.65)$$

As seen in (4.64)-(4.65), implementing GHA allows the designer to precisely model the losses with respect to system design and control parameters. On the other hand, time domain analysis adds to the complexity of such calculations, as the magnitudes of the drain current at switching instant depends on the relative values of control parameters ($\emptyset_S, \emptyset_T, \delta_S$) and sequence of different possible operating modes [108].

To characterize the various kinds of losses, Table 4.2 provides a comprehensive loss model with analytically and experimentally obtained values of various system parameters. Figure 4.28 compares the losses incurred in the TAB topology with implementation of various control schemes as discussed in the study. As observed, the three-loop control with optimization algorithm results in significantly lower amount of switching and conduction losses as compared to PSTL and DPFTL schemes.

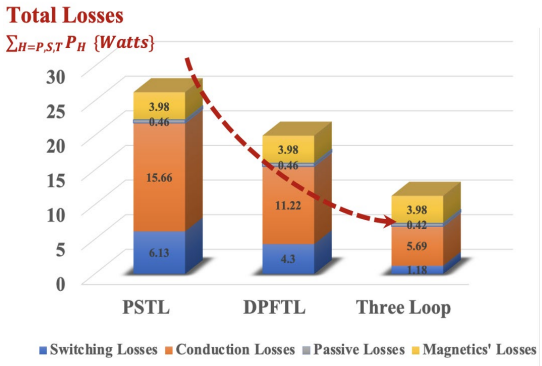


Figure 4.28: Loss Comparison Between Implementation of PSTL, DPFTL and Three Loop Control Schemes

Further, the efficiency curve of all the three control schemes at different loading conditions is presented in Figure 4.29, which indicates a peak efficiency of 96.24% using the three-loop control scheme.

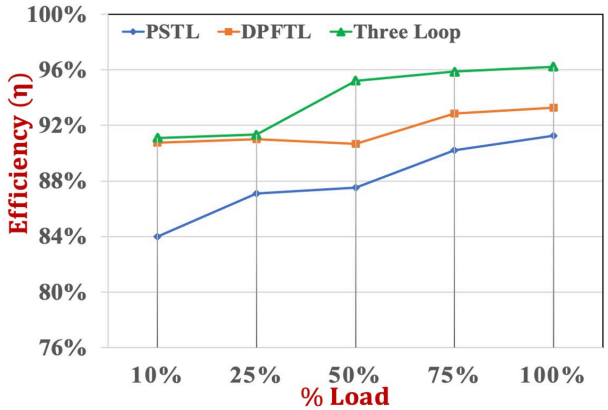


Figure 4.29: Efficiency Characterization at Various Loading Conditions

Table 4.2: Detailed Loss Model of the TAB Converter Topology with Quantified Loss Breakdown

Loss category	Loss sub-category	Formulation for one component	Comments	Components Involved (count)	Calculated Losses
Semiconductor Losses	Switching Turn on losses	$P_{sw,on\,(S_X)} = \frac{1}{2} V_{DS\,(S_X)} I_{D\,(S_X)} \left(t_{1,on\,(S_X)} + t_{2,on\,(S_X)}\right) f_{sw}$ Where, $t_{1,on\,(S_X)} = R_{g(S_X)} C_{in(S_X)} \ln\left(\frac{V_{Dr(S_X)} - V_{th(S_X)}}{V_{Dr(S_X)} - V_{pl(S_X)}}\right)$ $t_{2,on(S_X)} = \frac{C_{gd\,(S_X)}\left(V_{DS\,(S_X)} - I_{D(S_X)} R_{DS,on\,(S_X)}\right) R_{g(S_X)}}{V_{Dr(S_X)} - V_{pl(S_X)}}$	Switches in B_P and B_S undergo ZVS turn-on. However, they still incur turn-off losses. On the other hand, switches in B_T experience hard switching, incurring both turn-on and turn-off losses. $\sum P_{switching} = \sum P_{sw,on} + \sum P_{sw,off}$	$S_9, S_{10}, S_{11}, S_{12}$ (4) S_1 to S_{12} (12)	1.18W
	Switching Turn off losses	$P_{sw,off\,(S_X)} = \frac{1}{2} V_{DS\,(S_X)} I_{D(S_X)} \left(t_{1,off\,(S_X)} + t_{2,off(S_X)}\right) f_{sw}$ Where, $t_{1,on(S_X)} = R_{g(S_X)} C_{in(S_X)} \ln\left(\frac{V_{pl(S_X)}}{V_{th(S_X)}}\right)$ $t_{2,on(S_X)} = \frac{C_{gd(S_X)}\left(V_{DC(S_X)} - I_{D(S_X)} R_{DS,on(S_X)}\right) R_{g(S_X)}}{V_{pl(S_X)}}$			
	Conduction Losses	$P_{cond\,(S_X)} = I^2_{D,RMS\,(S_X)} R_{DS,on\,(S_X)}$	At any instant, two switches in any particular bridge experience conduction losses. $\sum P_{conduction} = \sum_{X=1}^{12} I^2_{D,RMS\,(S_X)} R_{DS,on\,(S_X)}$	S_1 to S_{12} (12*) *6 at a given instant	5.69W
Capacitor ESR Losses	-	$P_{Cap,ESR} = I^2_{OS,ripple\,(RMS)} R_{C_{OS},ESR} + I^2_{OT,ripple\,(RMS)} R_{C_{OT},ESR}$	The capacitor bank ESR losses are limited due to series/parallel combination of capacitors resulting in reduced effective ESR	C_{OS} and C_{OT} (2)	0.42W
Magnetics	Core Losses	$P_{core} = \frac{1}{T} \int_0^T k_i \left\lvert\frac{dB}{dt}\right\rvert^{\alpha} (\Delta B)^{\beta-\alpha} dt$ Where, $k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} \lvert\cos\theta\rvert^{\alpha} 2^{\beta-\alpha} d\theta}$	Total magnetic losses are summation of magnetic core loss and winding losses	-	2.11W
	Winding Losses	$P_{winding} = I^2_{P,RMS} R_{P,ac} + I^2_{S,RMS} R_{S,ac} + I^2_{T,RMS} R_{T,ac}$		-	1.64W

4.7. Chapter Summary

This work focuses on detailed modeling and analysis of a TAB DC/DC converter topology along with its various control mechanism to enhance the overall conversion efficiency of the system. Closed form equations for port voltages, line currents and inter-port power flows are derived using GHA based modeling technique corelating their dependency between the control parameters and voltage gains at different load levels. Further, a decoupled control scheme, specifically aimed at eliminating the interdependency between the two voltage control loops is formulated by introducing cross-gain terms derived from a MIMO based system. To minimize the system losses and to add another dimension of control, a phase/duty modulated three loop control scheme is proposed with power flow optimization algorithm. Several constraints are defined that find the most optimum operating point $\{\delta_S, \emptyset_S, \emptyset_T\} = \{0.119\, rad, 0.038\, rad, 0.152\, rad\}$ for a particular set of design specifications rated at 300W. The proposed optimization function also provides design insights pertaining to the leakage inductance optimization to ensure power flow requirement while achieving loss minimization. Finally, the work presents and experimentally validates loss comparison and efficiency mapping of the three control schemes that indicate that the three-loop control scheme achieves highest peak efficiency of 96.24% that is 2.94% and 4.97% higher than DPFTL and PSTL schemes.

CHAPTER 5

STEADY STATE MODEL DERIVED MULTI-VARIABLE LOSS OPTIMIZATION FOR TRIPLE ACTIVE C^3L^3 RESONANT CONVERTER

5.1. Introduction

Complimenting the varied research efforts on MPCs as reviewed in Chapter 1, their amalgamations with resonant structures, and the modulations schemes introduced to enhance the system efficiency, this study focusses on a holistic steady-state analysis and global loss minimization of the proposed TAC^3L^3 converter. The key contributions of this work are as follows: (a) Detailed GHA based steady-state converter model construction with accurate quantification of tank currents, power flows between the ports and voltage gain trends, (b) Comprehensive conduction and switching loss function formulations targeted to achieve global loss minimization based on multi-dimensional multi-variable constrained loss optimization, (c) Thorough strategical elucidation of algorithm to find the best hybrid modulation scheme, adhering to the implementation constraints of involving increasing order of control variables, (c) Meticulous experimental validation of the developed model and loss comparison of modulation techniques for wide range of power and voltage gain based corner conditions.

Please note that the transient analysis of the proposed converter is excluded from the scope of this work, thus focusing on its steady-state operational synthesis and loss optimization. The technical aspects covered in the chapter are derived from the study shown in [180].

5.2. GHA Based Modeling of TAC^3L^3 Converter

The proposed TAC^3L^3 converter topology is shown in Figure 5.1. As observed, three full bridge modules are coupled together through a three winding high frequency planar transformer (HFPT) with integrated leakage inductances (L_P, L_S, L_T denote primary, secondary, and tertiary side leakage inductances respectively), having a turns ratio of $N_P : N_S : N_T$ and magnetizing inductance of L_m. The system is designed for a resonant frequency $f_r = \frac{1}{2\pi\sqrt{L_P C_p}} = \frac{1}{2\pi\sqrt{L_S C_S}} = \frac{1}{2\pi\sqrt{L_T C_T}}$, where C_P, C_S and C_T denote the resonant capacitors for the primary, secondary and tertiary modules. To bolster the flexibility of design with its wide gain range capability, the resonant tank is considered to be asymmetric (i.e., $L_p \neq \left(\frac{N_S}{N_P}\right)^2 L_s \neq \left(\frac{N_T}{N_P}\right)^2 L_T$).

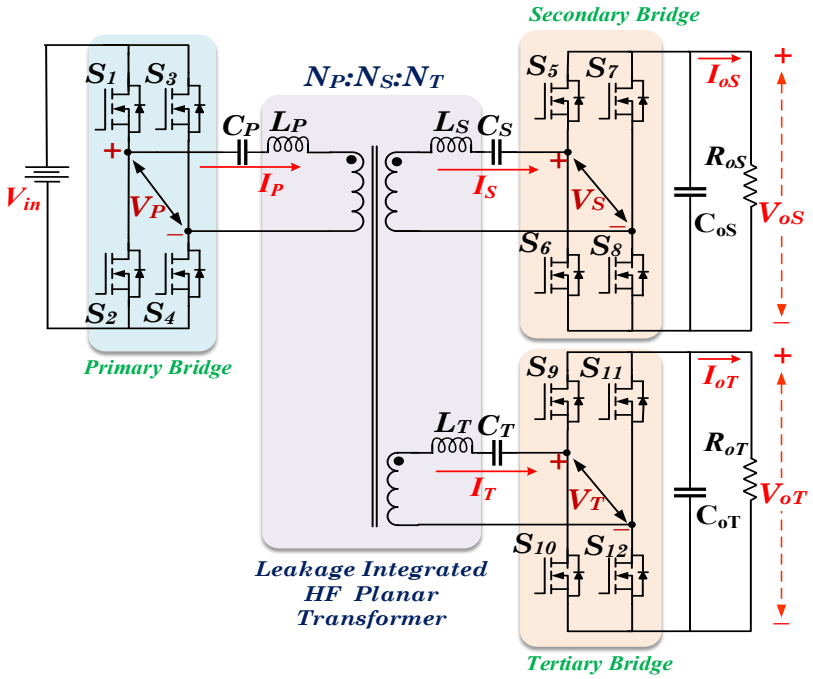


Figure 5.1:TAC^3L^3 Converter Topology.

For analyzing the power flow between the three modules and their interdependency, the TAC^3L^3 topology can be modelled as a three-port network as shown in Figure 5.2(a). Following the concept of GHA based modeling [115], each port can be shown as a quasi-square waveshape voltage source, which can be represented as a summation of *k* odd order sinusoidal voltage sources ($k \rightarrow 1$ to $2m+1$; $m \in [0, \infty)$), including the fundamental component and its higher order harmonics. Thus, the port voltages can be written as:

$$V_P(t) = \frac{4V_{in}}{\pi} \sum_{k=1}^{2m+1} \frac{\sin(k\omega_s t)}{k} \cos(k\delta_P) \tag{5.1}$$

$$V_S(t) = \frac{4V'_{oS}}{\pi} \sum_{k=1}^{2m+1} \frac{\sin(k(\omega_s t - \varphi_S))}{k} \cos(k\delta_S) \tag{5.2}$$

$$V_T(t) = \frac{4V'_{oT}}{\pi} \sum_{k=1}^{2m+1} \frac{\sin(k(\omega_s t - k\varphi_T))}{k} \cos(k\delta_T) \tag{5.3}$$

where, $\omega_s (= 2\pi f_s)$ is the operational switching frequency, $\delta_P, \delta_S, \delta_T$ are the duty control parameters of the primary, secondary and tertiary side and φ_S, φ_T are the phase shifts of secondary and tertiary side port voltages with respect to that of the primary side port. The relationship between the control variables and the port voltages and their effect on the waveshape is elucidated in Figure 5.3.

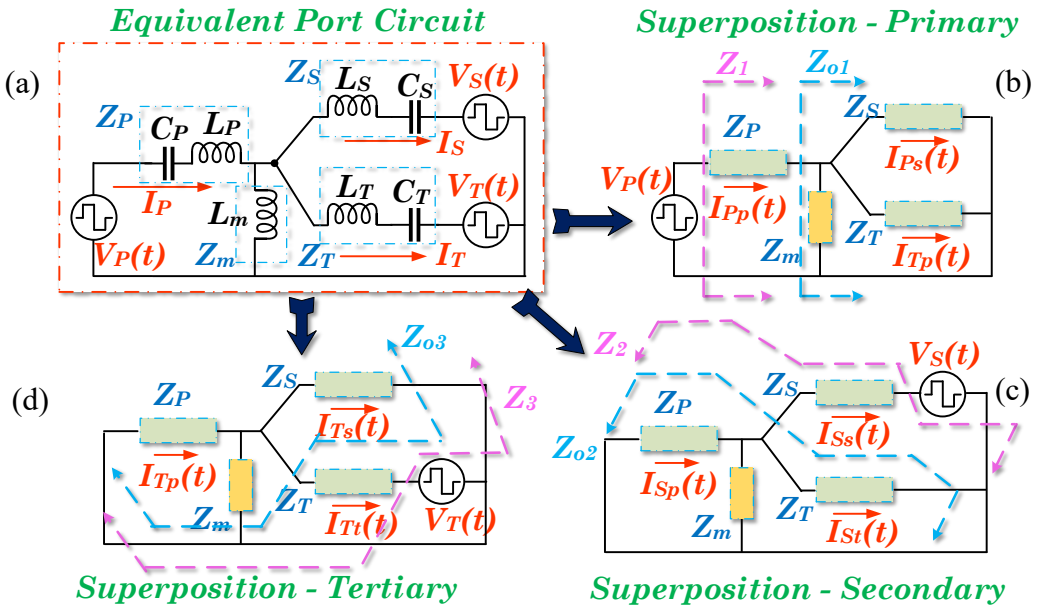


Figure 5.2: (a) Equivalent Port Representation for System Synthesis; (b),(c),(d) Equivalent Port Circuits Applying Superposition at Primary, Secondary and Tertiary Ports Respectively.

As the proposed TAC^3L^3 converter follows a resonant topology structure, the magnetizing inductance L_m takes part in the power flow between the bridges, unlike the conventional TAB topology [10,124-125], where its effect is ignored for power flow analysis due to very high value of L_m. Thus, a superposition-based port current formulation approach is elucidated, that facilitates accurate power flow modeling of the proposed TAC^3L^3 converter.

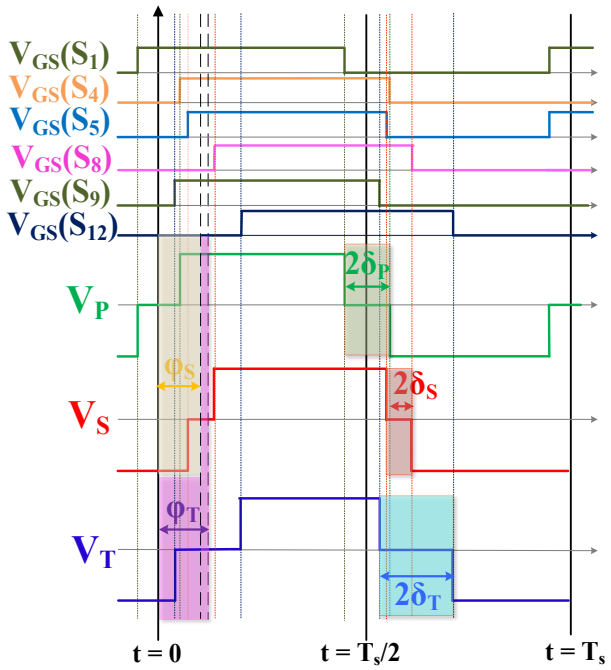


Figure 5.3: Phase Relationships Between Port Voltages and Corresponding Control Parameters

The equivalent port circuits utilizing superposition theorem is shown in Figure 5.2 (b)-(d), each representing the port circuits for individual port voltages. Using circuit restructuring and analysis, the cumulative port currents can be written as follows:

$$I_P(t) = I_{P_P}(t) + I_{P_S}(t) + I_{P_T}(t) \tag{5.4}$$

$$I_S(t) = I_{S_P}(t) + I_{S_S}(t) + I_{S_T}(t) \tag{5.5}$$

$$I_T(t) = I_{T_P}(t) + I_{T_S}(t) + I_{T_T}(t) \tag{5.6}$$

where, the analytical formulations of individual component of port currents are shown below. For the superposed primary equivalent circuit, the port currents can be written as follows:

$$\left.\begin{aligned} I_{P_P}(t) &= \frac{4V_{in}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(k\omega_s t-\alpha_{1,k})}{k}\frac{1}{|Z_{1,k}|}d_{P,k} \\ I_{S_P}(t) &= \frac{4V_{in}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(k\omega_s t-\alpha_{1,k}+\beta_{11,k})}{k}\frac{|Z_{x_{11},k}|}{|Z_{1,k}|}d_{P,k} \\ I_{T_P}(t) &= \frac{4V_{in}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(k\omega_s t-\alpha_{1,k}+\beta_{12,k})}{k}\frac{|Z_{x_{12},k}|}{|Z_{1,k}|}d_{P,k} \end{aligned}\right\} \quad (5.7)$$

where, $|Z_{1,k}|\angle\alpha_{1,k} = Z_{P,k} + Z_{o1,k}$; $Z_{o1,k} = Z_S||Z_T||Z_m$; $|Z_{x_{11},k}|\angle\beta_{11,k} = \frac{Z_{o1,k}}{Z_S}$; $|Z_{x_{12},k}|\angle\beta_{12,k} = \frac{Z_{o1,k}}{Z_T}$; $d_P = \cos(k\delta_P)$. Referring to the superposed secondary side, the port currents can be written as follows:

$$\left.\begin{aligned} I_{P_S}(t) &= \frac{4V'_{oS}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(k\omega_s t-k\varphi_S-\alpha_{2,k}+\beta_{21,k})}{k}\frac{|Z_{x21,k}|}{|Z_{2,k}|}d_{S,k} \\ I_{S_S}(t) &= -\frac{4V'_{oS}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(k\omega_s t-k\varphi_S-\alpha_{2,k})}{k}\frac{1}{|Z_{2,k}|}d_{S,k} \\ I_{T_S}(t) &= -\frac{4V'_{oS}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(k\omega_s t-k\varphi_S-\alpha_{2,k}+\beta_{22,k})}{k}\frac{|Z_{x22,k}|}{|Z_{2,k}|}d_{S,k} \end{aligned}\right\} \quad (5.8)$$

where, $|Z_{2,k}|\angle\alpha_{2,k} = Z_{S,k} + Z_{o2,k}$; $Z_{o2,k} = Z_P||Z_T||Z_m$; $|Z_{x_{21},k}|\angle\beta_{21,k} = \frac{Z_{o2,k}}{Z_P}$; $|Z_{x_{22},k}|\angle\beta_{22,k} = \frac{Z_{o2,k}}{Z_T}$; $d_{S,k} = \cos(k\delta_S)$. Similarly, the superposed tertiary side port current equations can be analyzed as follows:

$$\left.\begin{aligned} I_{P_T}(t) &= \frac{4V'_{oT}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(k\omega_s t-k\varphi_T-\alpha_{3,k}+\beta_{31,k})}{k}\frac{|Z_{x31,k}|}{|Z_{3,k}|}d_{T,k} \\ I_{S_T}(t) &= -\frac{4V'_{oT}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(k\omega_s t-k\varphi_T-\alpha_{3,k}+\beta_{32,k})}{k}\frac{|Z_{x32,k}|}{|Z_{3,k}|}d_{T,k} \\ I_{T_T}(t) &= -\frac{4V'_{oT}}{\pi}\sum_{k=1}^{2m+1}\frac{\sin(k\omega_s t-k\varphi_T-\alpha_{3,k})}{k}\frac{1}{|Z_{3,k}|}d_{T,k} \end{aligned}\right\} \quad (5.9)$$

where, $|Z_{3,k}|\angle\alpha_{3,k} = Z_{T,k} + Z_{o3,k}$; $Z_{o3,k} = Z_P||Z_S||Z_m$; $|Z_{x_{31},k}|\angle\beta_{31,k} = \frac{Z_{o3,k}}{Z_P}$; $|Z_{x_{32},k}|\angle\beta_{32,k} = \frac{Z_{o3,k}}{Z_S}$; $d_{T,k} = \cos(k\delta_T)$.

Further, utilizing the cumulative port currents, the average power flow from/to the three ports can be calculated as shown in (5.10)-(5.12). Please note, power flowing out of the port has a positive sign convention, while power flowing into the port has a negative sign convention.

$$P_P = \left(\frac{4V_{in}}{\pi}\right)^2 \left[M_{P1} + \frac{V'_{oS}}{V_{in}} M_{P2} + \frac{V'_{oT}}{V_{in}} M_{P3}\right] \tag{5.10}$$

$$P_S = \left(\frac{4V'_{oS}}{\pi}\right)^2 \left[-M_{S1} + \frac{V_{in}}{V'_{oS}} M_{S2} - \frac{V'_{oT}}{V'_{oS}} M_{S3}\right] \tag{5.11}$$

$$P_T = \left(\frac{4V'_{oT}}{\pi}\right)^2 \left[-M_{T1} + \frac{V_{in}}{V'_{oT}} M_{T2} - \frac{V'_{oS}}{V'_{oT}} M_{T3}\right] \tag{5.12}$$

where the coefficients M_{XY} $(X \in \{P, S, T\}, Y \in \{1,2,3\})$ are shown in the appendix section.

As the TAC^3L^3 converter follows a resonant topology, it is also important to formulate the gain dependency of the converter for the output ports. Thus, considering a forward power flow operation (primary port – input, secondary and tertiary port – outputs), the cumulative GHA based gain equation can be derived by equating the power equations in (5.11)-(5.12) with $\frac{{V'_{oS}}^2}{R_{oS}}$ and $\frac{{V'_{oT}}^2}{R_{oT}}$ respectively and solving a set of linear equation to obtain the gain equations as shown below:

$$G_S = \frac{V'_{oS}}{V_{in}} = \frac{G_{A2} - G_{A2}G_{B1} + G_{A3}G_{B2}}{(1-G_{A1})(1-G_{B1})(1-G_{A3}G_{B3})} \tag{5.13}$$

$$G_T = \frac{V'_{oT}}{V_{in}} = \frac{G_{B2} - G_{B2}G_{A1} + G_{B3}G_{A2}}{(1-G_{A1})(1-G_{B1})(1-G_{A3}G_{B3})} \tag{5.14}$$

where, $G_{A1} = -\left(\frac{4}{\pi}\right)^2 R_{oS}M_{S1}$; $G_{A2} = \left(\frac{4}{\pi}\right)^2 R_{oS}M_{S2}$; $G_{A3} = -\left(\frac{4}{\pi}\right)^2 R_{oS}M_{S3}$; $G_{B1} = -\left(\frac{4}{\pi}\right)^2 R_{oT}M_{T1}$; $G_{B2} = \left(\frac{4}{\pi}\right)^2 R_{oT}M_{T2}$; $G_{B3} = -\left(\frac{4}{\pi}\right)^2 R_{oT}M_{T3}$.

Following the gain equations mentioned in (5.13)-(5.14), the gain trends for the secondary and tertiary ports with respect to the switching frequency (f_s) for different loading conditions are shown in Figure 5.4.

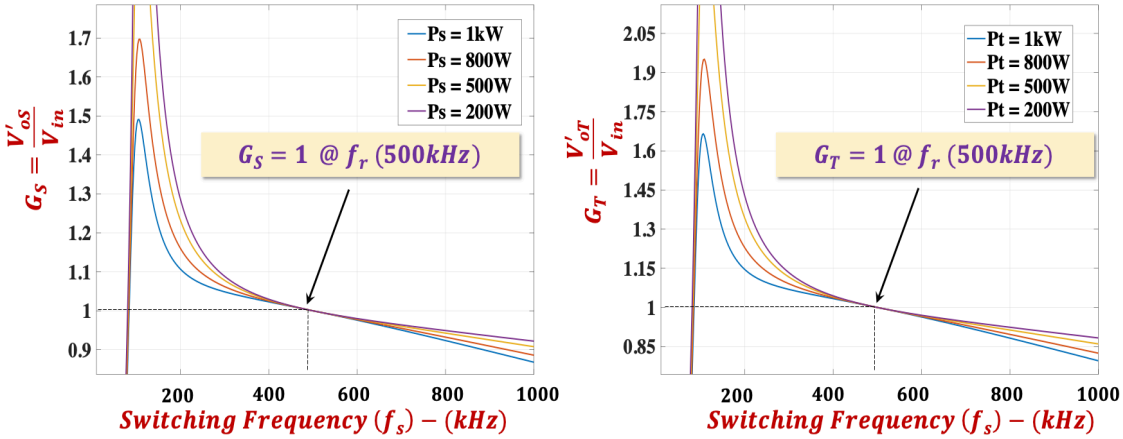


Figure 5.4: Secondary and Tertiary Port Gains (G_S, G_T) with Respect to the Switching Frequency (f_s) for Different Loading Conditions.

Further, as observed in (5.13-5.14), the gain trends tend to vary with variation of the selected duty and phase control parameters. This dependence introduces the concept of hybrid modulation for different set of port output voltages and powers involving different operating points with combination of control parameters, as explained in the following section.

5.3. Hybrid Modulation Techniques of TAC^3L^3 Converter

Following the gain-frequency dependence of the proposed TAC^3L^3 converter, the frequency modulation plays the most crucial role in achieving the desired power and voltage regulation at the output ports. Considering an instance where the duty control parameters are selected to be zero ($\delta_P = \delta_S = \delta_T = 0$), the required power flows for all the three ports (P_P, P_S, P_T) can be achieved by modulating at least three control parameters:

f_s, φ_S and φ_T for a particular set of port output voltages (V_{oS}, V_{oT}). This type of modulation technique that uses only the inter-port phase shifts and switching frequency as control variables is termed as frequency coupled dual phase shift (FDPS). In addition, solving three equations (10)-(12) with three unknown variables $\{f_s, \varphi_S, \varphi_T\}$ results in only one feasible operating point resulting in the desired power flow, thus leaving no scope for any performance optimization. For example, for design specifications mentioned in Table 5.3, for a set of requirements: $\{P_P, P_S, P_T, G_S, G_T\} = \{2kW, 1kW, 1kW, 1.09, 1.12\}$, the feasible operating point implementing FDPS occurs at $\{f_s, \varphi_S, \varphi_T\} = \{396.81kHz, -0.742, 0.197\}$. However, including a combination of duty and phase control variables along with the operational frequency in the power formulation function results in contour of multiple feasible operating points, which introduces a possibility of finding the most optimal operating point subject to a particular set of constraints. To testify this hypothesis, another case is considered with an additional duty control parameter - δ_S introduced in addition to $f_s, \varphi_S, \varphi_T$ to achieve the same set of port power and voltages. As observed in Figure 5.5, for case (a), the set of feasible operational $\{\varphi_S, \varphi_T\}$ points for $\{\delta_s, f_s\} = \{0.41, 372.12kHz\}$ is denoted by $\{FP_A\}$, while that for case (b) with $\{\delta_s, f_s\} = \{0.17, 347.76kHz\}$ is denoted by $\{FP_B\}$. As observed, adding a duty control parameter to FDPS expands the feasible set from a singular point to a contour of feasible points, which introduces the scope for implementation of a power flow optimization routine.

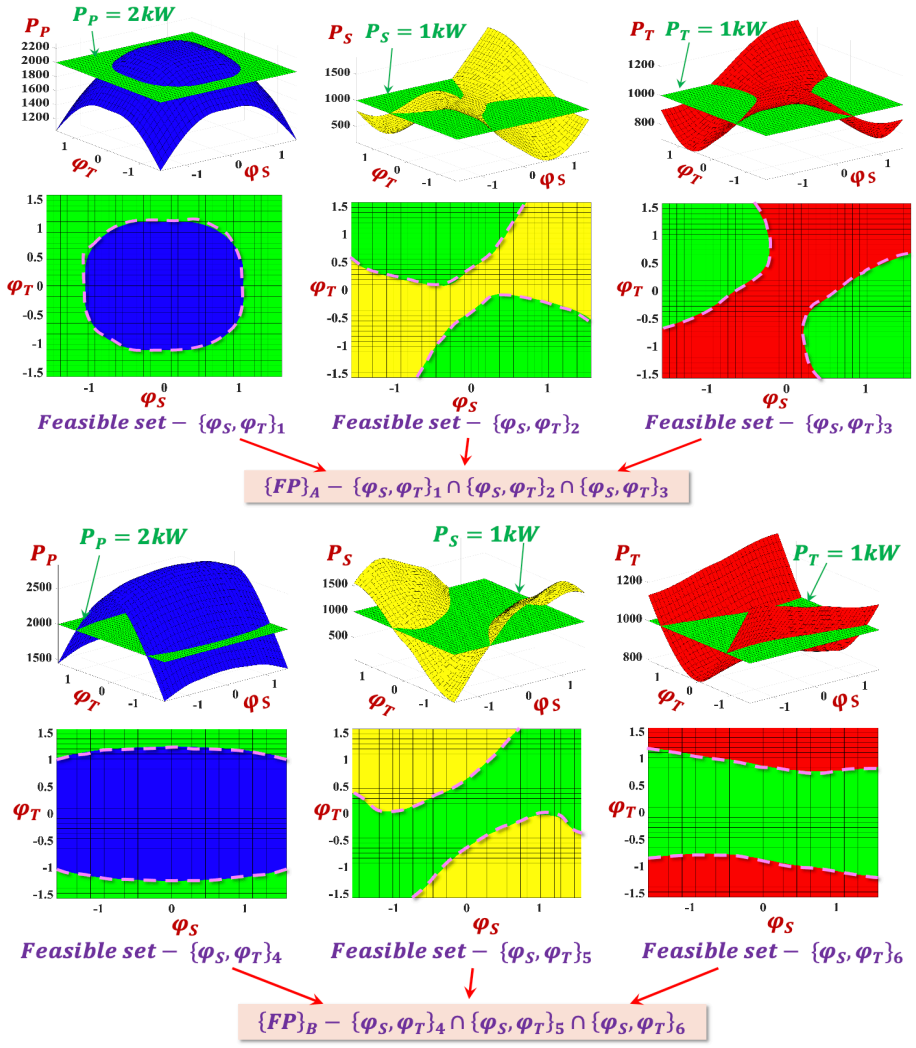


Figure 5.5: Contour Plot to Find the Feasible Operating Set Points - $\{\varphi_S,\varphi_T\}$ for (a) $\{\delta_s, f_s\}$={0.41,372.12kHz} and (b) $\{\delta_s, f_s\}$={0.17,347.76kHz}.

Based on this concept, the control degrees of freedom can be expanded to eight different hybrid modulation schemes depending on the combination of the various control parameters as shown in Table 5.1.

Table 5.1: Different Hybrid Modulation Schemes for TAC^3L^3 Converter

No.	Category of Hybrid Modulation	Nomenclature	Control Variables Involved
1	Frequency coupled Dual Phase Shift	FDPS	$\{f_s, \varphi_S, \varphi_T\}$
2	Frequency coupled Triple Phase Shift	FTPS-P	$\{f_s, \varphi_S, \varphi_T, \delta_P\}$
3		FTPS-S	$\{f_s, \varphi_S, \varphi_T, \delta_S\}$
4		FTPS-T	$\{f_s, \varphi_S, \varphi_T, \delta_T\}$
5	Frequency coupled Quad Phase Shift	FQPS-PS	$\{f_s, \varphi_S, \varphi_T, \delta_P, \delta_S\}$
6		FQPS-PT	$\{f_s, \varphi_S, \varphi_T, \delta_P, \delta_T\}$
7		FQPS-ST	$\{f_s, \varphi_S, \varphi_T, \delta_S, \delta_T\}$
8	Frequency coupled Penta Phase Shift	FPPS	$\{f_s, \varphi_S, \varphi_T, \delta_P, \delta_S, \delta_T\}$

As observed, for the FPPS modulation, six control parameters are involved, which on one hand provides more degrees of control freedom, but on the other hand proves to be expensive in terms of computational workload. Analyzing this trade-off, the following section formulates the cumulative loss function of the TAC^3L^3 converter with detailed constraints to find an optimal operating point with a target of loss minimization. Further, a methodology to select the best modulation technique is also mentioned based on the selected design parameters and corresponding optimized loss functions.

5.4. System Loss Modeling and Global Loss Objective Function Formulation

The loss functions for the TAC^3L^3 converter are derived for conduction losses (F_{cond}), switching losses (F_{sw}) and the high-frequency planar transformer (HFPT) losses ($F_{wind} + F_{core}$) with their relevant operational constraints.

5.4.1. Conduction and HFPT Winding Losses

The RMS values of tank/port currents in the TAC^3L^3 converter portray a strong dependence on the operational load, frequency, and selected control variables, which are essentially used to calculate the conduction losses in the system. To analytically demonstrate this correlation, the mathematical models of the port RMS currents are formulated by simplifying (5.4)-(5.6) as follows:

$$I_X(t) = \sum_{k=1}^{2m+1} A_{k,X} \sin(k\omega_s t) + B_{k,X} \cos(k\omega_s t) \tag{5.15}$$

$$I_{X,RMS} = \frac{1}{\sqrt{2}} \sqrt{\sum_{k=1}^{2m+1} (A_{k,X}^2 + B_{k,X}^2)} \tag{5.16}$$

where, $X \in \{P, S, T\}$ and the coefficients ($A_{k,X}$ and $B_{k,X}$) corresponding to each port currents are shown in the Appendix section. Utilizing the RMS current formulations, the objective function for conduction loss characterization is shown in (5.17).

$$\boldsymbol{F_{cond}}\{\boldsymbol{G_S}, \boldsymbol{G_T}, \boldsymbol{P_P}, \boldsymbol{P_S}, \boldsymbol{P_T}\} = \sum_{X=P,S,T} I_{X,RMS}^2 R_{ds_{on},X}, \text{where } X \in \{P, S, T\} \tag{5.17}$$

where, $R_{ds_{on},X}$ are the on-state resistances of the switches in the full bridges of each port. The information of the RMS values of the port currents also helps formulate the HFPT winding loss function. Referring to applications targeting high frequency switching, winding losses pertaining to the effective AC resistance are found to be significantly high

due to eddy current and skin effects. Thus, based on accurate characterization of the effective winding resistances of all the three windings of the developed HFPT, the winding loss function can be expressed as follows:

$$\boldsymbol{F_{wind}}\{\boldsymbol{G_S}, \boldsymbol{G_T}, \boldsymbol{P_P}, \boldsymbol{P_S}, \boldsymbol{P_T}\} = \sum_{X=P,S,T} I_{X,RMS}^2 R_{eff,X} \tag{5.18}$$

where, $X \in \{P, S, T\}$.

5.4.2. Switching Losses

As the TAC^3L^3 converter follows a resonant CLLC topology, the switching loss model is developed with a target to achieve ZVS turn-on at the primary and secondary port, while achieving synchronous rectification (SR) based turn on/off at the tertiary port. The loss functions and soft-switching constraints are derived for various conditions of operational data points of the optimized control parameters, as follows:

(a) ZVS turn on for primary and secondary ports

Unlike a conventional CLLC converter, where a lagging phase of primary current along with sufficient dead time intervals is sufficient to ensure ZVS, the TAC^3L^3 requires detailed investigation for understanding the conditions for achieving ZVS. Here, the drain-to-source capacitance of the MOSFET (C_{oss}) necessitates constraints in the form of minimum instantaneous port current required to facilitate ZVS commutation [125]. In addition to that, the inclusion of duty control variable also alters the ZVS range due to inconsistency caused in the switching instants. Thus, an equivalent model is developed to comprehensively analyze the ZVS constraints for different conditions for each switch of the primary and secondary port. Figure 5.6 shows the generic Thevenin equivalent circuit

of the TAC^3L^3 converter referred to primary/secondary side. As observed, the equivalent impedance (Z_{XEQ}) and voltage source (V_{XEQ}) correspond to primary and secondary side port ($X = \{P, S\}$) and are derived as follows:

$$Z_{PEQ} = Z_P + (Z_{l1}); Z_{SEQ} = Z_S + (Z_{l2}) \tag{5.19}$$

$$V_{PEQ} = V_S(t)\left[\frac{Z_S + Z_P Z_{l1}}{Z_T || Z_m} - \frac{Z_P}{Z_S}\right] + V_T(t)\left[\frac{Z_T + Z_P Z_{l1}}{Z_S || Z_m} - \frac{Z_P}{Z_T}\right] \tag{5.20}$$

$$V_{SEQ} = V_P(t)\left[\frac{Z_P + Z_S Z_{l2}}{Z_T || Z_m} - \frac{Z_S}{Z_P}\right] + V_T(t)\left[\frac{Z_T + Z_S Z_{l2}}{Z_S || Z_m} - \frac{Z_S}{Z_T}\right] \tag{5.21}$$

where, $Z_{l1} = Z_m || Z_S || Z_T$ and $Z_{l2} = Z_m || Z_P || Z_T$

Further, the switch notations used in the generic equivalent circuit (Figure 5.6), correspond to the primary ($S_1 - S_4$) and secondary ($S_5 - S_8$) switches, as follows:

$$S_J = \begin{cases} S_1 \\ S_5 \end{cases}; S_K = \begin{cases} S_2 \\ S_6 \end{cases}; S_L = \begin{cases} S_3 \\ S_7 \end{cases}; S_M = \begin{cases} S_4 \\ S_8 \end{cases} \tag{5.22}$$

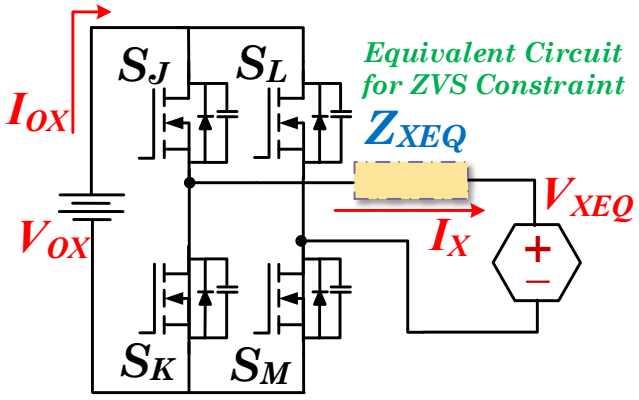


Figure 5.6: Equivalent Circuit for ZVS Investigation

Considering the equivalent circuit shown in Figure 5.6, two distinctly identified commutation cases for ZVS criteria are explained below:

(a) <u>*Case I*</u> ($\delta_X = 0$): $I_X(t) > 0, S_K$ and S_L turn on *OR* $I_X(t) < 0, S_J$ and S_M turn on

Following the instantaneous circuit structure as shown in Figure 5.7(a) for S_K and S_L turn on, the total energy sunk by the Thevenin equivalent source can be expressed as follows:

$$E_{sunk} = \int_0^{\tau_d} \left[V_{XEQ} I_X(\zeta) - V_{OX} I_{OX}(\zeta)\right] dt$$

$$= \int_0^{\tau_d} \left[V_{XEQ}\left(-2C_{oss}\frac{dV_{OX}}{dt}\right) - 0\right] = 2C_{oss} V_{XEQ} V_{OX} \tag{5.23}$$

where, τ_d is the deadtime interval.

Further, the total energy in the switch remains constant during the commutation interval, which helps formulate the necessary constraint for ZVS for this case, as follows:

$$E_{sourced} \geq E_{sunk} = \frac{1}{2} Z_{XEQ} I_X(\zeta)^2 \geq 2C_{oss} V_{XEQ}(\zeta) V_{OX} \tag{5.24}$$

Thus, to achieve ZVS turn on, the minimum port current constraint for $V_{XEQ}(\zeta) > 0$ can be expressed as follows:

$$\underline{\text{Constraint:}}\ |I_X(\zeta)| \geq 2V_{OX}\sqrt{\frac{C_{oss} V_{XEQ}}{Z_{XEQ} V_{OX}}} \tag{5.25}$$

where, the turn on instant ζ for S_K and S_L under $\delta_X = 0$ is $t = \pi + \varphi_X$. As the port voltage follows half-wave symmetry, the following condition is implied for the equivalent port voltage for both the primary and secondary side ports: $V_{XEQ}(t) = -V_{XEQ}(\pi + t)$. Thus, similar analysis can be performed to yield the ZVS constraints ($V_{XEQ}(\zeta) < 0$) at the turn on instants of switch S_J and S_M with opposite current polarity ($I_X(t) < 0$), as shown in Figure 5.7 (b):

$$\underline{\text{Constraint:}}\ |I_X(\zeta)| \geq 2V_{OX}\sqrt{-\frac{C_{oss} V_{XEQ}}{Z_{XEQ} V_{OX}}} \tag{5.26}$$

where, the turn on instant ζ for S_J and S_M for $\delta_P = 0$ is $t = (0\ or\ 2\pi) + \varphi_X$.

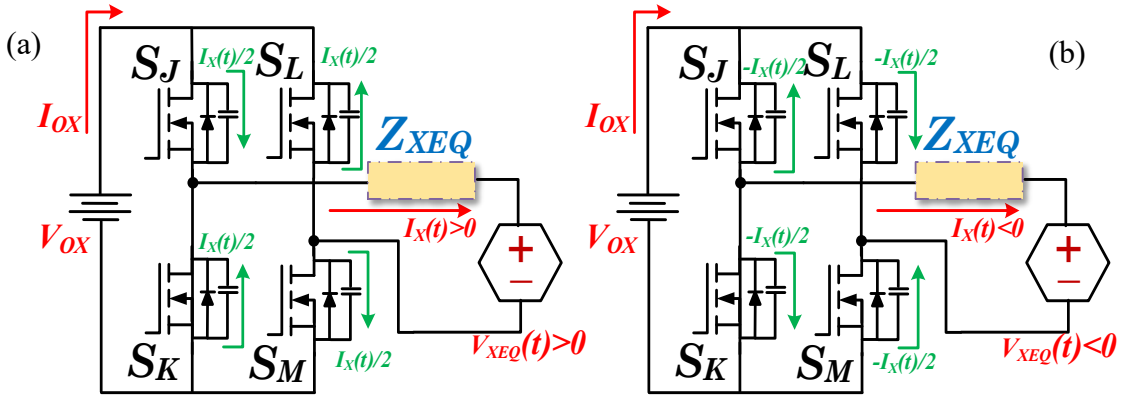


Figure 5.7: Equivalent Circuit for Formulation ZVS Constraints for δ_X=0; (a) Switch S_K and S_L, (b) Switch S_J and S_M.

Inclusion of duty control variable for the primary and secondary port, due to non-consistent switching instants imposes non-uniform constraints for ZVS turn-on for each switch. Thus, individual investigation targeting the ZVS criteria for each switch is presented in Case II.

(b) Case II $(\delta_X \neq 0)$: $I_X(t) > 0, S_K$ turn on *OR* $I_X(t) < 0, S_J$ turn on

Following the equivalent circuit configuration shown in Figure 5.8 (a) for $\delta_X \neq 0$, for the turn on instance of switch S_K, the total sunk energy can be expressed as follows:

$$\begin{aligned} E_{sunk} &= \int_0^{\tau_d} \left[V_{XEQ} I_X(\zeta) - V_{OX} I_{OX}(\zeta)\right] dt \\ &= \int_0^{\tau_d} \left[V_{XEQ}\left(-2C_{oss}\frac{dV_{OX}}{dt}\right) - V_{OX}\left(-C_{oss}\frac{dV_{OX}}{dt}\right)\right] dt \\ &= 2C_{oss}V_{XEQ}V_{OX} - C_{oss}V_{OX}^2 \end{aligned} \quad (5.27)$$

Utilizing (5.27), the necessary constraint for achieving ZVS for S_K can be formulated as follows:

$$\frac{1}{2} Z_{XEQ} I_X(\zeta)^2 \geq 2C_{oss}V_{XEQ}V_{OX} - C_{oss}V_{OX}^2 \quad (5.28)$$

where, $\zeta = \varphi_X - \delta_X$ denotes the turn-on instant of switch S_K. Further, as port voltages and current follow half-wave symmetry, the condition (5.28) for ZVS can be extended for S_J turn on (shown in Figure 5.8 (b)) for opposite current polarity ($I_X(t) < 0$), as shown below:

$$\frac{1}{2} Z_{XEQ} I_X(\zeta)^2 \geq -2C_{oss} V_{XEQ} V_{OX} - C_{oss} V_{OX}^2 \tag{5.29}$$

where, $\zeta = \pi + \varphi_X - \delta_X$ is the turn on instant for S_J.

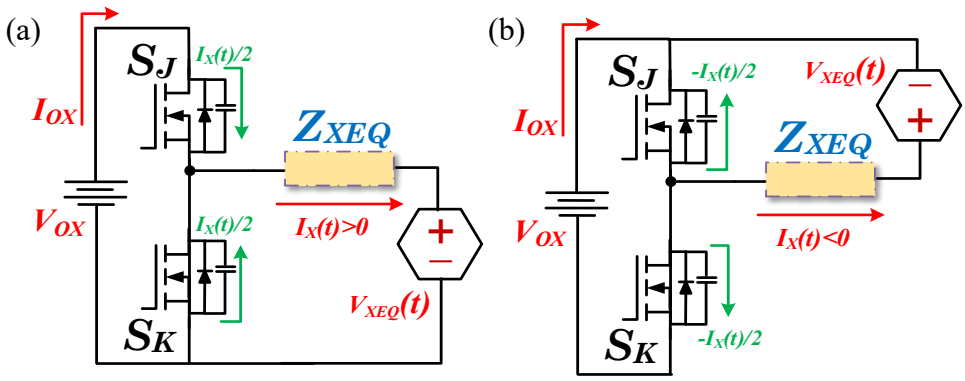


Figure 5.8: Equivalent Circuit for Formulation ZVS Constraints for $\delta_X \neq 0$; (a) Switch S_K (b) Switch S_J

Similar analysis can be performed for switches $S_M (I_X(t) > 0)$ and S_L $(I_X(t) < 0)$ with their turn-on instants $\zeta = \varphi_X + \delta_X$ and $\zeta = \pi + \varphi_X + \delta_X$ respectively. Adhering to the study shown in the above two cases, Table 5.2 summarizes the ZVS constraints for all the switches in the primary and secondary bridge.

Table 5.2: ZVS Constraints for Different Cases

Case	Switch turning on	ZVS Constraints	Switching Instant (ζ)
$\delta_X = 0$	S_K and S_L, $I_X > 0$	$\lvert I_X(\zeta)\rvert \geq 2V_{OX}\sqrt{\frac{C_{oss}V_{XEQ}}{Z_{XEQ}V_{OX}}}$ for $V_{XEQ} > 0$	$\pi + \varphi_X$
	S_J and $I_X < 0$	$\lvert I_X(\zeta)\rvert \geq 2V_{OX}\sqrt{-\frac{C_{oss}V_{XEQ}}{Z_{XEQ}V_{OX}}}$ for $V_{XEQ} < 0$	(0 or 2π) $+\varphi_X$
$\delta_X \neq 0$	$S_J, I_X < 0$	$\lvert I_X(\zeta)\rvert \geq 2V_{OX}\sqrt{-\frac{C_{oss}V_{XEQ}}{Z_{XEQ}V_{in}} - \frac{C_{oss}}{2Z_{XEQ}}}$ for $V_{PEQ} < -\frac{V_{in}}{2}$	$\pi + \varphi_X - \delta_X$
	$S_K, I_X > 0$	$\lvert I_X(\zeta)\rvert \geq 2V_{OX}\sqrt{\frac{C_{oss}V_{XEQ}}{Z_{XEQ}V_{OX}} - \frac{C_{oss}}{2Z_{XEQ}}}$ for $V_{XEQ} > \frac{V_{OX}}{2}$	$\varphi_X - \delta_X$
	$S_L, I_X > 0$	$\lvert I_X(\zeta)\rvert \geq 2V_{OX}\sqrt{\frac{C_{oss}V_{XEQ}}{Z_{XEQ}V_{in}} + \frac{C_{oss}}{2Z_{XEQ}}}$ for $V_{XEQ} > -\frac{V_{OX}}{2}$	$\pi + \varphi_X + \delta_X$
	$S_M, I_X < 0$	$\lvert I_X(\zeta)\rvert \geq 2V_{OX}\sqrt{-\frac{C_{oss}V_{XEQ}}{Z_{XEQ}V_{OX}} + \frac{C_{oss}}{2Z_{XEQ}}}$ for $V_{XEQ} < \frac{V_{OX}}{2}$	$\varphi_X + \delta_X$

As the ZVS constraints are enforced for the primary and secondary side switches, the solution set obtained as a part of the optimization function results in zero turn-on losses accounting for soft turn-on of the switches. The corresponding loss function for the primary and secondary is then limited to turnoff losses only as shown below:

$$\boldsymbol{F_{sw,pri\_sec}}\{\boldsymbol{G_S}, \boldsymbol{G_T}, \boldsymbol{P_P}, \boldsymbol{P_S}, \boldsymbol{P_T}\} = \sum_{X=P,S} V_{OX}|I_X(\zeta)|f_{sw}(t_{off}) \tag{5.30}$$

where, $t_{off} = t_{rv} + t_{fi} = \frac{C_{gd}R_g(V_{OX} - I_D R_{on})}{V_{pl}} + R_g C_{in} \ln\frac{V_{pl}}{V_{th}}$ and the corresponding parameters ($C_{gd}, R_g, V_{pl}, R_g, C_{in}, V_{th}$) can be obtained from the relevant datasheets of the MOSFETs used for the individual ports and be referred from [131].

(b) Synchronous Rectification for tertiary port

With an objective to reduce the switching losses to accurately track the phase of the tertiary bridge voltage, with respect to the phase shift φ_T, analytical considerations for

achieving SR are discussed in this section. The time dependent equation of tertiary side port current (5.6) can be written in terms of a sinusoidal term with complex magnitude and phase variables (ϑ_T) as shown below:

$$I_T(t) = |I_T| \sin\left(k\omega_s t + \vartheta_{T,X}\right) \tag{5.31}$$

$$= \sum_{k=1}^{2m+1} \sqrt{(A_{k,T}^2 + B_{k,T}^2)} \sin(k\omega_s t + \vartheta_{k,T}) \tag{5.32}$$

where $\vartheta_{k,T} = \tan^{-1} \frac{B_{k,T}}{A_{k,T}}$

Further, precise estimation of the optimal $\vartheta_{k,T}$ is quintessential for enabling SR; the failure to do so results in significant switching losses which is directly proportional to the extent of error in phase tracking (ϑ_e). Figure 5.9 elaborates on this phenomenon by elucidating the turnoff losses due to inaccurate phase tracking for $f_s < f_r$ for two cases: (a) $\delta_T = 0$ and (b) $\delta_T \neq 0$ and compares it with an accurately estimated SR operation.

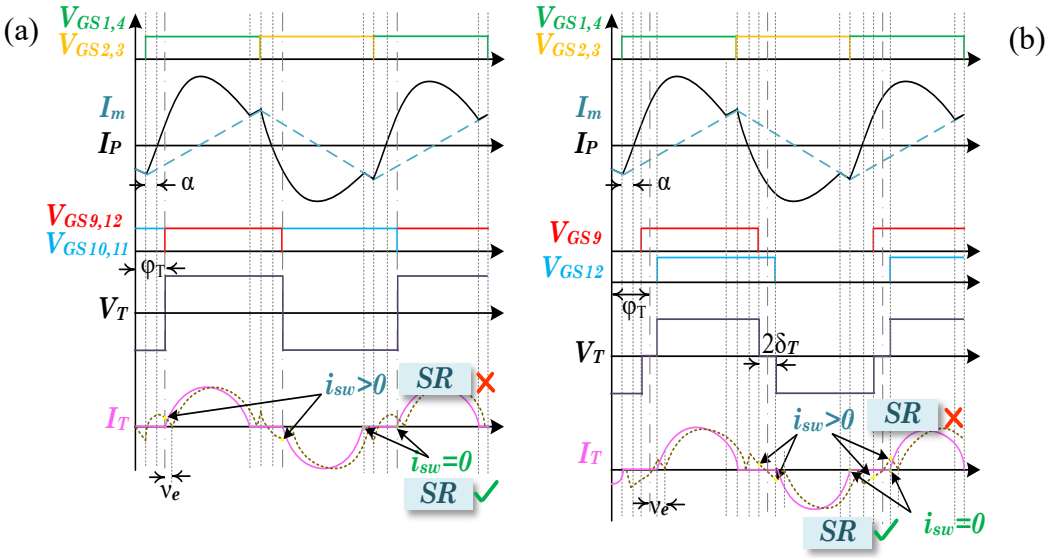


Figure 5.9: Waveforms to Elucidate SR Based Switching: Case (a) - δ_T=0 and Case (b) - δ_T≠0

As observed for Figure 5.9(a), due to inaccurate estimated phase provided to S_9 and S_{12} and their complementary pairs in waveforms (ii), the current at the turnoff/turn-on instant is not zero, leading to switching losses in all four switches, that can be calculated as follows:

$$i_{sw} = |I_T| \sin \vartheta_e \tag{5.33}$$

$$P_{sw,total} = 2 \cdot \tfrac{1}{2} V_{oT} |i_{sw}| f_s t_{off} + 2 \cdot \tfrac{1}{2} V_{oT} |i_{sw}| f_s t_{on} \tag{5.34}$$

where, $\vartheta_e = \vartheta_{k,T} - k\varphi_T$.

Similarly, for case (b) (as shown in Figure 5.9 (b)), considering waveform (i) to be the port current waveform, the current at the switching instants is zero, due to the accurate phase tracking with respect to the port voltage. However, for waveform (ii), the phase error of ϑ_e exists, resulting in $|i_{sw}| > 0$, thus incurring increased switching losses. Thus, maintaining symmetricity with port current following the phase of the port voltages is essential for accurate SR action. In that context, the phases of the port currents and voltages should precisely match, which enforces the following constraint:

Constraint: $\vartheta_{k,T} - k\varphi_T = 0$ (5.35)

Adhering to the constraint mentioned, the switching loss function occurring due to incorrect phase matching for tertiary side switches can be written as follows:

$$\boldsymbol{F_{sw,tri}\{G_S, G_T, P_P, P_S, P_T\}} = V_{oT} |i_{sw}| t_{on} f_{sw} + V_{oT} |i_{sw}| t_{off} f_{sw} \tag{5.36}$$

5.4.3. Global Loss Minimization for Different Switching Schemes

Following the loss functions derived above with their respective constraints, the global loss function of the TAC^3L^3 converter can be written as follows:

Objective: *Minimize* $F_{global} = F_{cond} + F_{sw,pri\_sec} + F_{sw,tri} + F_{wind} + F_{core}$

(5.37)

where, F_{core} denotes the magnetic core losses referred from Steinmetz equation [181], and can be formulated as follows:

$$\boldsymbol{F_{core}\{f_s\}} = kf^a\hat{B}^b \tag{5.38}$$

where, $\hat{B}$ denotes the magnetic flux density corresponding to the excitation provided and k, a and b are Stienmetz constants, obtained from the core material datasheets.

To obtain the optimized set of solutions for the objective function shown in (5.37), the following constraints for power flow and control variables are imposed in addition to the ones for ZVS turn-on and accurate SR action:

Constraint: For obtaining desired power flow at individual ports, the following conditions must hold:

$$\left.\begin{aligned} P_P^* - P_P &= 0 \\ P_S^* - P_S &= 0 \\ P_T^* - P_T &= 0 \end{aligned}\right\} \tag{5.39}$$

where, P_P^*, P_S^*, P_T^* are the desired port power references.

Constraints: The following limits are applied adhering to the control parameters used in the power flow analysis:

$$-\frac{\pi}{2} < \varphi_S, \varphi_T < \frac{\pi}{2} \tag{5.40}$$

$$0 < \delta_P, \delta_S, \delta_T < \frac{\pi}{2} \tag{5.41}$$

$$f_{s,min} < f_s < f_{s,max} \tag{5.42}$$

where, $f_{s,min}$ and $f_{s,max}$ depend on the gain trend with respect to output voltages at the secondary and tertiary port.

To elucidate the comparison of various modulation schemes and their performance with respect to the resultant value of the objective function (F_{global}), Figure 5.10 shows the correlation of objective function for different loading conditions (light, medium and heavy) with respect to different port gains for all the modulation schemes. As observed, in all the conditions, the FPPS modulation schemes proves to provide the least losses, thus yielding highest steady-state efficiency. Further, conventionally, as seen in [19], as the lower order modulation schemes are essentially a subset of the higher order ones, the objective functions portray a degrading trend with reduction in the control variables involved. However, for the TAC^3L^3 converter, due to the inclusion of operating frequency as a crucial optimization parameter and its corresponding resolution selected in the optimization routine, it is also observed that lower order modulation schemes render better performance than the higher order ones. One such instance is presented for the case involving the tertiary port at high power 1kW (as seen in Figure 5.10). As observed, for $G_T = 1.04$, the order of performance observed $FPPS < FQPS - TP < FTPS - S$, which follows the conventional trend. However, for $G_T = 1.12$, the order is changed to $FPPS < FTPS - T < FQPS - TP$, which might seem counterintuitive, but is verified by the experimental results shown in Section 5.6.

Adhering to the above-mentioned scenario, the implementation constraints imposed due to inclusion of higher control parameters enforces the investigation of an algorithm to optimally choose the switching scheme, as described in the following section.

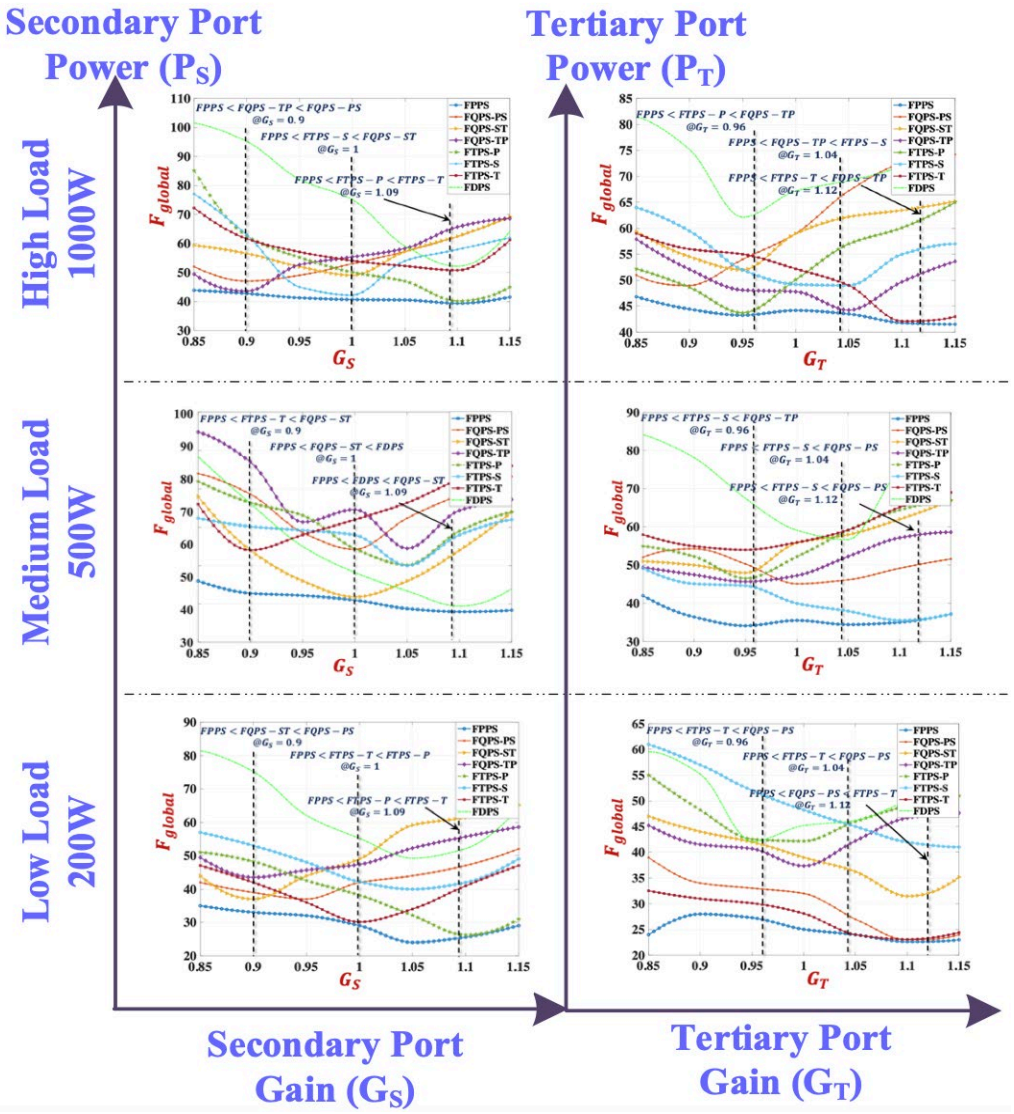


Figure 5.10: Performance Comparison of Various Modulation Schemes with Respect to the Defined Optimization Routine

5.5. Identification of Modulation Scheme Based on Implementation Constraints

Although FPPS modulation scheme results in the least value of global loss function (F_{global}) for almost all the corner conditions, its practical implementation scheme poses a challenge due to computationally expensive look up tables and larger memory blocks

involved. Thus, to find the optimum modulation scheme, an algorithm to compare the output of the objective functions for different modulation schemes is implemented. This algorithm is based on the concept of relative benefit provided by engaging an incremental number of control parameter to reach the optimal operating point. Therefore, in order to restrict rapid mode transitions unless a significant benefit is foreseen, a criterion is defined that quantifies the benefit in the objective function with respect to FPPS scheme with a threshold of 5% in the value of F_{global}, which translates to ~0.12% variation in the resultant efficiency. For elucidating this algorithm, the selection of optimal modulation scheme for the tertiary port for low loading (200W) condition is considered (as shown in Figure 5.11). For $G_T = 0.96$, the value of $F_{global}(FPPS)$ is 26.9, while the second-best modulation scheme ($FTPS-T$) results in $F_{global}(FTPS-T) = 30.1$. Comparing the resultant values of objective function, the condition $1.05\left(F_{global}(FPPS)\right) < F_{global}(FTPS-T)$ forces the selection of FPPS to be the most optimum modulation scheme in this case. However, for $G_T = 1.04$, the following is observed $1.05\left\{\left(F_{global}(FPPS)\right) = 24.2\right\} > \left\{\left(F_{global}(FTPS-T)\right) = 24.7\right\}$, which enables the selection of FTPS-T as the most optimal scheme for that particular gain/load condition. Further, for $G_T = 1.12$, we get $1.05\left\{\left(F_{global}(FPPS)\right) = 22.8\right\} > \left\{\left(F_{global}(FQPS-PS)\right) = 23.4\right\}$, however a low order modulation scheme (FTPS-T) also satisfies $1.05\left\{\left(F_{global}(FPPS)\right) = 22.8\right\} > \left\{\left(F_{global}(FTPS-T)\right) = 23.8\right\}$, thus making FTPS-T the most optimum modulation scheme for this gain/load condition, adhering the higher order modulation implementation constraints.

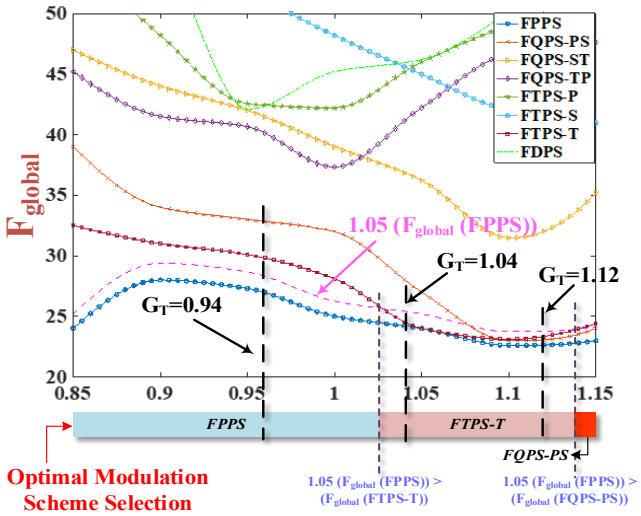


Figure 5.11: An Instance of F_{global} Performance to Show the Optimal Modulation Scheme Selection.

The corresponding generic flowchart to find the most optimum modulation scheme based on the loading and gain conditions is shown in Figure 5.12. Based on rigorous analysis and iterative process to solve the objective function for different corner conditions, and adhering to the algorithm for easing the implementation, Figure 5.13 presents the operating zone matrix that elucidates the optimal modulation scheme adhering to the implementation-based tradeoffs, which infer the following outcomes:

(a) At lighter load and low gain conditions, FPPS proves to be the most optimum modulation scheme.

(b) As the loading is increased, the lower order modulation schemes perform almost as efficiently as the FPPS.

(c) The presented analysis can be extrapolated for other loading and gain conditions ($\{P_S, P_T, G_S, G_T\}$), forming a 4D array of optimum operating schemes.

(d) If there is a clash for the optimum modulation selection in the operating zone matrix, the value of resultant objective function would be the deciding factor. For example, at $\{P_S, P_T, G_S, G_T\} = \{1kW, 1kW, 1.09, 1.12\}$, two modulation schemes – FTPS-P and FTPS-T – satisfy the criteria based on implementation constraints. In this case, as $\{F_{global}(FTPS-P)\} = 41.4 < \{F_{global}(FTPS-T)\} = 42.6$, the selected modulation scheme for optimal operation would be FTPS-P.

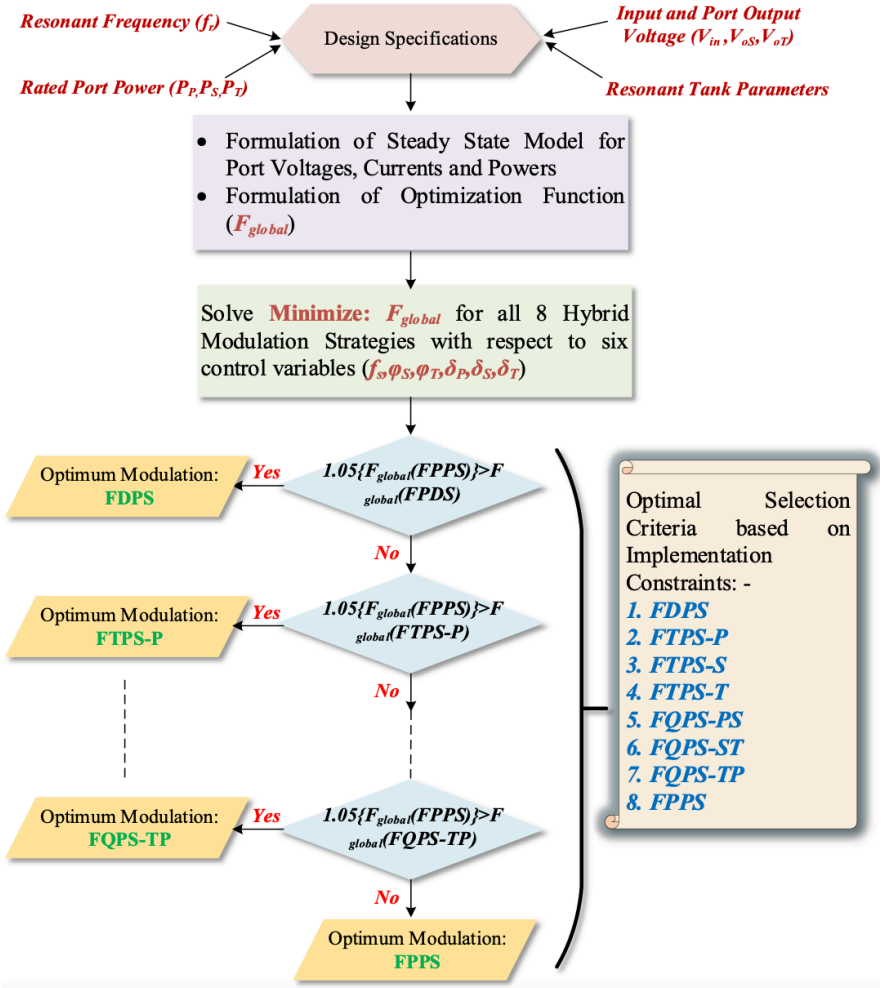


Figure 5.12: Algorithmic Flowchart to Obtain the Most Optimum Modulation Scheme Adhering to Implementation Constraints

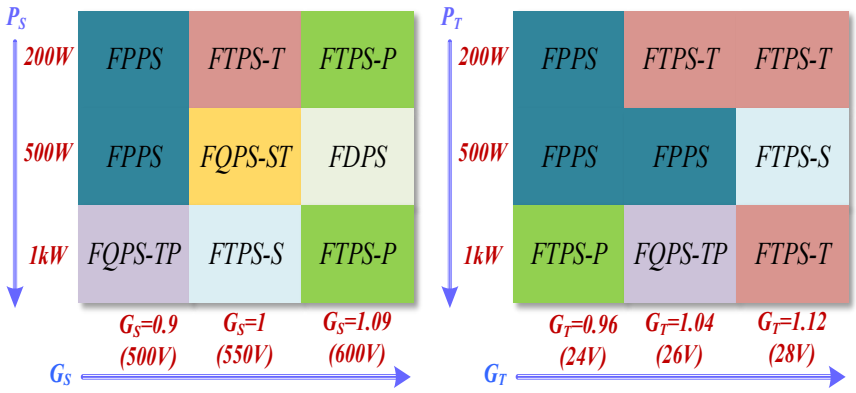


Figure 5.13: Operating Zone Matrix of the Designed TAC^3L^3 Converter Based on Port Gains and Power Requirements.

Based on the numerous findings and optimal modulation selection criteria presented, the following section aims at experimental validations for different loading and gain conditions.

5.6. Experimental Verification and Benchmarking

To thoroughly validate the analysis and findings presented in the previous sections, an experimental prototype (as elucidated in Figure 5.14) is developed for the design specifications mentioned in Table 5.3. Different corner conditions corresponding to the design requirements are verified with appropriate modulation schemes to ensure optimal efficiency operation. The proof-of-concept is developed with a targeted application of a multi-port EV charger, where the input side corresponds to a DC link voltage of 400V nominal, with the secondary and tertiary ports corresponding to the main and auxiliary batteries at 600V and 28V nominal, with a depletion threshold of 500V and 24V respectively. The gate control signals inculcating the phase, duty, and frequency parameters are fed to the power stage using TMS320F28379D dual-core digital signal

processor. The primary bridge consists of GaN Systems GS66508T $(650V, 30A, 50m\Omega)$, while the secondary side is realized using Transphorm TP90H050WS (900V, 22A, $63m\Omega$) cascode GaN-FETs and each of the tertiary side switching blocks consists of four EPC2020 $(60V, 90A, 2.2m\Omega)$ devices connected in parallel, thus enabling an all-GaN power converter solution, ensuring a superior power density. Magnetic planar EE core FR45810 from Mag Inc. is used to realize the HFPT with planar windings fabricated on a 4-layer PCB.

Please note, due to significantly high magnitude of I_T, the interface between the HFPT and tertiary bridge PCB is made using 10 Litz wires of same specification, connected in parallel to (a) facilitate near-equal sharing of current amongst all the wires, and (b) to minimize any additional parasitic inductance. Relevant experimental results for I_T have been obtained by probing one of the Litz wire.

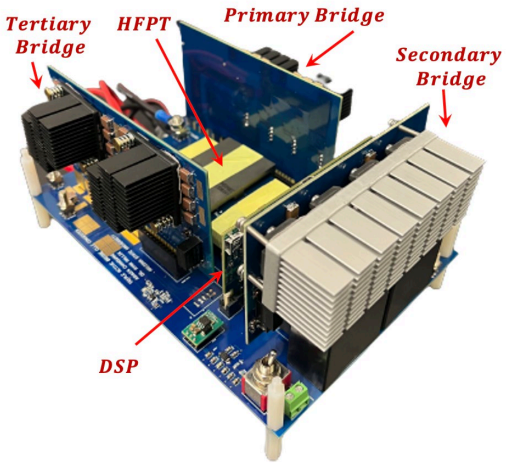


Figure 5.14: Hardware Prototype of the Developed TAC^3L^3 Converter

Table 5.3: Design Specifications for TAC^3L^3 Converter

Parameters	Values
Primary input voltage (V_{in})	400V
Secondary output voltage range (V_{OS})	500-600V
Tertiary output voltage range (V_{OT})	24-28V
Rated Port Power (P_P, P_S, P_T)	2kW,1kW,1kW
Transformer Turns Ratio (N_P, N_S, N_T)	16:22:1
Tank Leakage Inductances (L_P, L_S, L_T)	4.45μH, 12.89μH, 0.031μH
Magnetizing Inductance (L_m)	85.427μH
Tank Capacitors (C_P, C_S, C_T)	22.76nF, 7.85nF, 3.24μF
Resonant frequency (f_s)	500 kHz

Following the analysis presented in the previous sections, a detailed comparison is presented in Figure 5.15 with experimental results for the converter operation implementing all the 8 modulation schemes for the rated load operation – 2kW/1kW/1kW with rated terminal voltages of 400V/600V/28V. The following points are the takeaways from the experimental comparison:

(a) Adhering to the constraints enforced in the optimization routine, ZVS based soft turn-on for primary and secondary bridges and SR operation for the tertiary bridge is obtained for all the modulation schemes. ZVS turn-on instants for switches S_2 and S_6 under FPPS mode are illustrated in Figure 5.16.

(b) Referring to the objective function plot (Figure 5.10), the port RMS currents for FPPS modulation are found to be the least with minimum SR phase error (ϑ_e), thus resulting in the end-to-end conversion efficiency of 97.09%.

(c) The second-best performance metrics are obtained with FTPS-T and FTPS-P modulation schemes with converter efficiencies of 96.48% and 96.74%, respectively. The trade-off of ~0.35% efficiency reduction at the benefit of reduced order modulation

implementation justifies the selection of FTPS-P as the most optimal modulation scheme under this particular loading and port gain condition.

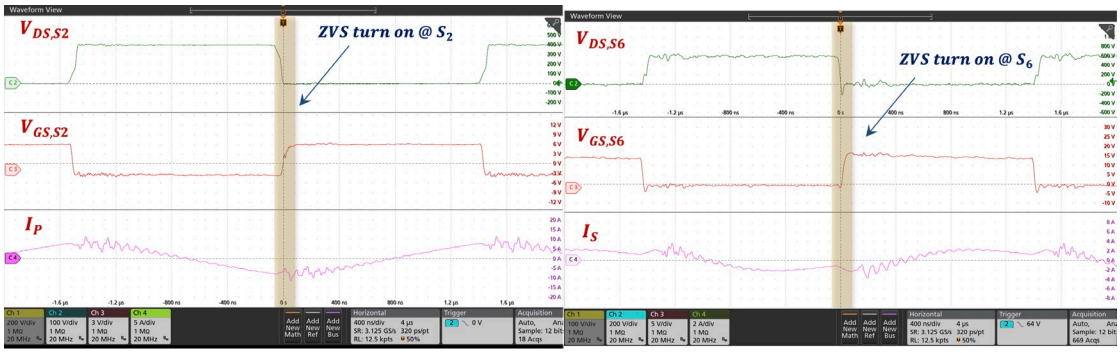


Figure 5.15: Experimental Investigation to Check the ZVS Turn-on for S_2 and S_6.

Figure 5.16: Experimental Results for $\{P_P, P_S, P_T, G_S, G_T\}$={2kW,1kW,1kW,1.09,1.12} With the Following Switching Schemes: (a) FDPS, (b) FTPS-P, (c) FTPS-S, (d) FTPS-T, (e) FQPS-PS, (f) FQPS-ST, (g) FQPS-TP and (h) FPPS.

To portray the operational versatility of the TAC^3L^3 converter in corner conditions, various loading and gain operating conditions are verified. Experimental waveforms for light loading conditions – $\{P_P, P_S, P_T, G_S, G_T\} = \{400W, 200W, 200W, 1.09, 1.12\}$ implemented with FPPS modulation scheme are shown in Figure 5.17. As observed, with the optimized operating control parameters $\{f_s, \varphi_S, \varphi_T, \delta_P, \delta_S, \delta_T\} =$ {393.7kHz, 0.36, -0.44, 0.29, 0.38, 0.17}, the converter achieves soft switching for all the ports, while portraying a light load efficiency of 93.2%. Further, to emulate depleted state of charge (SOC) of the batteries at the secondary and tertiary ports, Figure 5.18 shows the experimental results for $\{P_P, P_S, P_T, G_S, G_T\}$={2kW,1kW,1kW,0.9,0.96}, implemented with FQPS-TP modulation scheme, complying to the operating zone matrix.

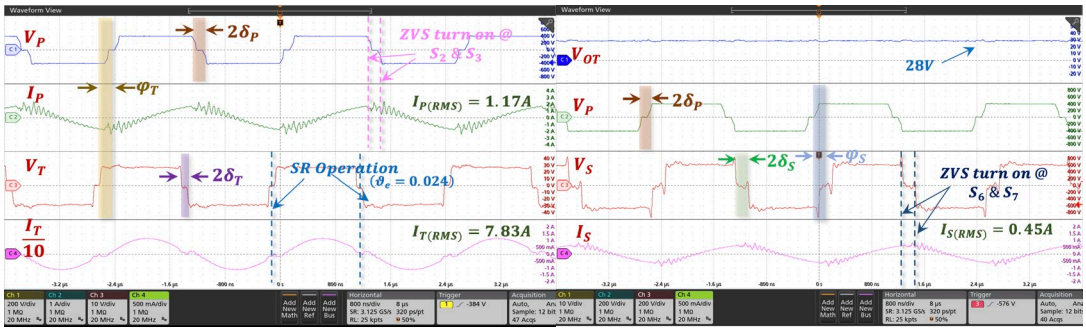


Figure 5.17: Experimental Results for $\{P_P, P_S, P_T, G_S, G_T\}$ = {400W,200W,200W,1.09,1.12} Implemented with FPPS Modulation.

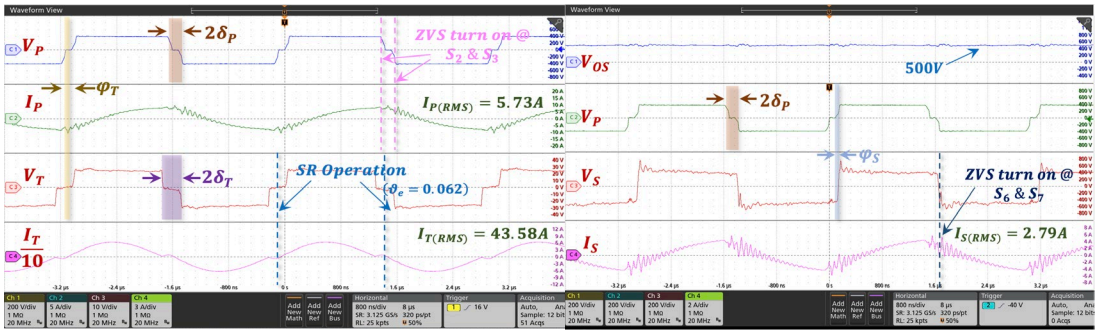


Figure 5.18: Experimental Results for $\{P_P, P_S, P_T, G_S, G_T\}$ ={2kW, 1kW, 1kW,0.9, 0.96}, Implemented with FQPS-TP Modulation Scheme.

The bidirectional power flow capability of the converter is also verified, where the tertiary side port acts as the input for the primary and secondary ports. Figure 5.19 elucidates the experimental results for reverse power flow condition $\{P_T(input), P_P, P_S, V_{OP}, V_{OS}\} = \{1\text{kW},\ 500\text{W},\ 500\text{W},\ 400\text{V},\ 600\text{V}\}$ implemented with FTPS-T modulation scheme. Please note, in this case, the ZVS turn-on constraints are expanded to all the ports, which results in the converter efficiency to be 91.3% for this operating condition.

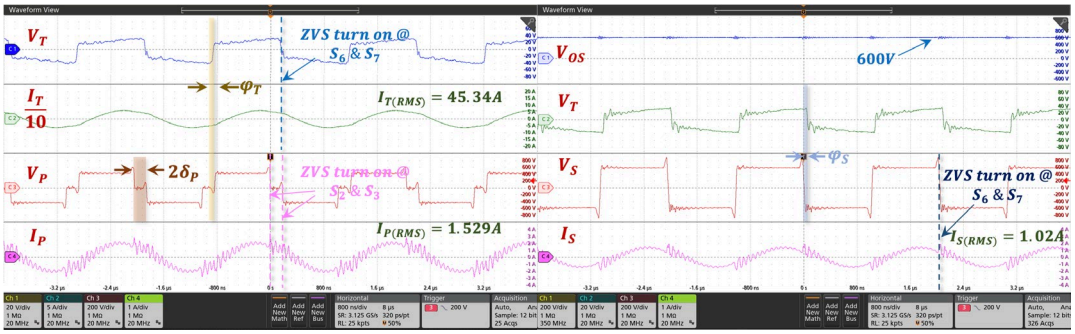


Figure 5.19: Experimental Results for Reverse Power Flow condition $\{P_T(\text{input}), P_P, P_S, V_{OP}, V_{OS}\} = \{1\text{kW}, 500\text{W}, 500\text{W}, 400\text{V}, 600\text{V}\}$ with FTPS-T Modulation Scheme.

To benchmark the performance of the TAC^3L^3 converter, an analytical comparison is provided with a conventional TAB converter implementing the Penta Phase Shift (PPS) modulation strategy [125]. The analytical comparison of losses in the system is shown in Figure 5.20. As observed, the implementation of PPS modulation in the TAB converter ensures reduction in the conduction losses in the system. However, due to partial soft switching occurring at various corner conditions results in non-ZVS turn-on of some of the switches, leading to higher switching losses (~45%) as compared to the TAC^3L^3 converter.

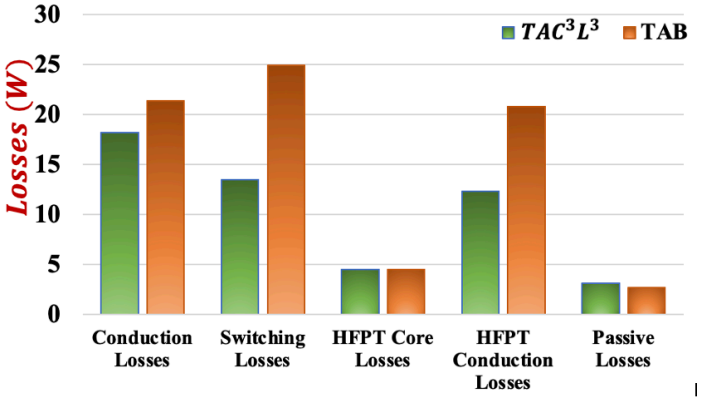


Figure 5.20: Analytical Loss Comparison of the Proposed TAC^3L^3 Converter with State-of-the-art TAB Converter with PPS Modulation.

Further, Figure 5.21 compares the efficiency trend for three cases: (a) 400V to 600V/28V conversion, (b) 400V to 500V/24V conversion and reverse power flow (c) 28V to 400V/600V. As observed, the TAC^3L^3 converter yields a peak efficiency of 97.42% and a rated efficiency of 97.09%.

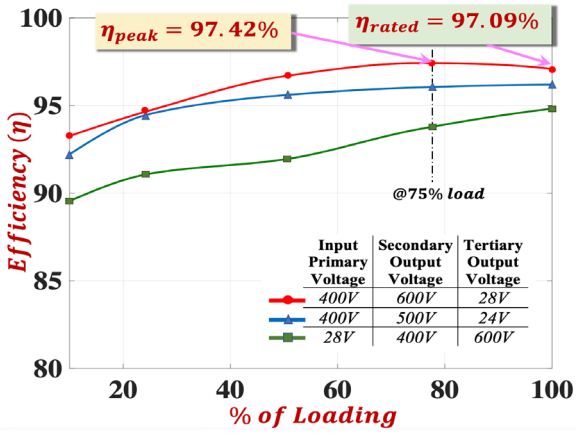


Figure 5.21: Efficiency Trend for TAC^3L^3 Converter at Different Loading Port Gain and Loading Conditions.

Please note that the efficiency graph shown in Figure 5.21 corresponds to the experiments done in a laboratory environment, with an ambient temperature of 24℃. However, it is important to note that the peak efficiency will observe a degrading trend in a higher ambient temperature environment dur to non-linear degradation of $R_{ds,on}$ of the

semiconductor devices, resulting in higher losses. Further, it is also worthwhile to note that the reliability analysis in a relevant on-board charger environment (with higher ambient temperature) will require a detailed modelling of the thermal management solution for the developed converter, which is not included in the current scope of work.

5.7. Chapter Summary

Based on the GHA model-based analysis of the TAC^3L^3 converter and its dependency on the control parameters – switching frequency, inter-port phase shifts and their respective duty ratios, a detailed multi-variable loss minimization objective function is developed to minimize the total power loss. The performance of different hybrid switching schemes is evaluated for the different loading and port gain conditions, with respect to constraints targeting soft-switching and desired power flow at the ports. Further, an algorithm is proposed, based on relative benefits with lower order modulation schemes, to enable optimal modulation scheme selection, with a loss function difference threshold of 5%. Various experimental results at different port gain corner conditions are presented to emulate different conditions of battery voltages at the secondary and tertiary ports (400V/500-600V/24-28V) at a power level of $\{P_P, P_S, P_T\} = \{2kW, 1kW, 1kW\}$. Verification for reverse power flow is also presented to elucidate the versatility of the TAC^3L^3 converter. Finally, the loss comparison with the state-of-the-art method is presented, elucidating ~45% reduction in the switching losses, with ~1.2% improvement in the end-to-end efficiency at the rated loading condition. The TAC^3L^3 converter portray a peak efficiency of 97.42% with a rated load efficiency of 97.09%.

CHAPTER 6

CONCLUSIONS AND FUTURE SCOPE OF WORK

This study holistically covers various modules of the multi-port resonant converter based onboard EV charger topology, elucidating the challenges pertaining to optimal design and effective control scheme, and provides detailed technically validated solutions.

An accurate and detailed mathematical model is proposed for calculating the magnitudes and phases of the harmonic components appearing in input current of a TPFC topology, along with a novel digital filter-based AMS to subdue the third harmonic component. Exhaustive simulation and experimental validation yielded in 46% reduction in the third harmonic component magnitude, thus resulting in 17% improvement in the resultant THD at the PCC. Further, a novel, easy-to-implement and reliable discrete sampling based current sensorless control for a TPFC was proposed and verified against the inherent uncertainty of the system parameters using a thorough sensitivity analysis. A 500W prototype is also built to illustrate the effectiveness of the proposed control technique, that yields a power factor of 0.998 (lag), with a resultant efficiency of 98.1% and a THD of 1.68% at rated load. The proposed control scheme outperforms the SOA approaches with a lower execution time and hence higher switching frequencies (upto 300kHz).

Following the AC/DC conversion, to characterize the CLLC DC/DC converter accurately, stressing on the influence of the stray components, a detailed all-inclusive gain model is derived. A non-linear multi-dimensional minimization function for the secondary current zero crossing is defined with an error margin of 0.1%, that tracks the phase required

to facilitate SR, and is experimentally verified elucidating a phase error of 0.29%. In addition to that, a thorough parametric RLC modeling of HFPT aided with detailed 3D FEA analysis is presented, for four different winding structures. Further, a detailed quantified approach to parameterize an SMC based controller is explained by dissecting the dynamic performance constraints, thus deriving the values of the controller coefficients according to the design requirements. Comprehensive experimental analysis for a 1kW prototype operating at 500kHz resonant frequency with results at various corner conditions are presented. Results portray a peak efficiency of 98.49%, which is ∼1.5% over other state-of-the-art techniques. Detailed results for dynamic load change (10-90% load step up and 90-10% load step down) are presented and compared for SMC and PI based controllers. Due to the robustness of the designed hybrid SMC based controller, the results portray an average settling time reduction of 46.4% and over/undershoot reduction of 33%,

Referring to the multi-port converter topologies, in order to precisely model the TAB converter adhering to the effect of higher order harmonics in the system, closed form equations for port voltages, line currents and inter-port power flows are derived using GHA based modeling technique corelating their dependency between the control parameters and voltage gains at different load levels. A decoupled two loop control scheme and a phase/duty modulated three loop control scheme is explained with a comprehensive power flow optimization objective defined with system design and performance constraints. The work presents and experimentally validates loss comparison and efficiency mapping of the three control schemes that indicate that the three-loop control scheme achieves highest peak efficiency of 96.24% that is 2.94% and 4.97% higher than DPFTL and PSTL schemes.

Finally, to elucidate the benefits of implementing a resonant topology in a multi-port converter for simultaneous charging for EV, a comprehensive loss optimization study of a TAC^3L^3 converter is presented in this study. Several hybrid switching schemes are introduced, and their comparative analysis is presented to achieve global loss minimization. Further, an optimal selection algorithm is elucidated to enable least algorithmic complexity based on implementation constraints, while ensuring maximum efficiency at different corner conditions of port powers and terminal voltages. Experimental validations for various loading conditions are presented for a wide-gain bidirectional operation (400V/500-600V/24-28V), portraying a peak converter efficiency of 97.42%.

The work presented in this study can be extended to different aspects of research areas, that constitute the future scope of work as shown below:

(a) Study on the gain interdependency of the output bridges and relevant decoupling formulated with the inclusion of parasitics in the system.

(b) Deeper analysis of three winding planar transformer in terms of characterizing the leakage inductances and stray capacitances in all the windings and establishing correlations with respect to fabrication-based considerations.

(c) Implementation of a closed loop control strategy to implement the algorithm for most optimum switching scheme for the TAC^3L^3 converter.

(d) Analysis on the EMI spectrum of the developed converters and corresponding EMI mitigation techniques.

(e) Reliability and failure mode analysis of the developed converter in a relevant on-board charger environment with higher ambient temperature.

(f) Integration of all the developed modules as a single solution for simultaneous battery charging which will include a cascaded closed loop control system structure to (i) regulate the PFC output voltage along with maintaining the sinusoidal current at the input and (ii) regulate the secondary and tertiary output voltages and port powers adhering to efficiency maximization objective.

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APPENDIX A

SUPPLEMENTARY EQUATIONS FOR FORMULATING THE ALL-INCLUSIVE SMALL-SIGNAL MODEL OF CLLC CONVERTER

The matrix coefficients for the all-inclusive small-signal model of CLLC converter (referring to Section 3.5.5, equations (3.118)-(3.122)) are shown below:

$$Z_1 = \frac{4}{k\pi}\frac{I_{Sc,k}^2 V_{Co,k}}{I_{sT,k}^3}; Z_2 = \frac{4}{k\pi}\frac{I_{Ss,k} I_{Sc,k} V_{Co,k}}{I_{sT,k}^3}; Z_3 = \frac{4}{k\pi}\frac{I_{Ss,k}}{I_{sT,k}}$$

$$Z_4 = \frac{4}{k\pi}\frac{I_{Sc,k}}{I_{sT,k}}; Z_5 = \frac{4}{k\pi}\sin\left(\frac{\pi}{2}\delta\right); Z_6 = \frac{2V_{in}}{k}\cos\left(\frac{\pi}{2}\delta\right)$$

$$A_{1:2,k} = -A_{2:1,k} = A_{5:6,k} = -A_{6:5,k} = A_{7:8,k} = -A_{8:7,k}$$

$$= A_{9:10,k} = -A_{10:9,k} = A_{11:12,k} = -A_{12:11,k} = A_{13:14,k}$$

$$= -A_{14:13,k} = A_{15:16,k} = -A_{16:15,k} = A_{17:18,k}$$

$$= -A_{18:17,k} = A_{19:20,k} = -A_{20:19,k} = k\Psi$$

$$A_{1:1,k} = A_{2:2,k} = -\frac{R_p}{L_{ss}}; A_{1:3,k} = A_{2:4,k} = -\frac{R_s + Z_1}{L_{mm}}$$

$$A_{1:4,k} = A_{2:3,k} = \frac{Z_2}{L_{mm}}; A_{1:5,k} = A_{2:6,k} = -\frac{1}{L_{ss}}$$

$$A_{1:7,k} = A_{2:8,k} = A_{3:5,k} = A_{4:6,k} = -\frac{1}{L_{mm}}$$

$$A_{1:21,k} = -\frac{Z_3}{L_{mm}}; A_{2:21,k} = -\frac{Z_4}{L_{mm}}; A_{3:1,k} = A_{4:2,k} = -\frac{R_p}{L_{mm}}$$

$$A_{3:3,k} = A_{4:4,k} = -\frac{R_s + Z_1}{L_{pp}}; A_{3:4,k} = k\Psi + \frac{Z_2}{L_{pp}}$$

$$A_{4:3,k} = -k\Psi + \frac{Z_2}{L_{pp}}; A_{3:7,k} = A_{4:8,k} = -\frac{1}{L_{pp}}$$

$$A_{3:21,k} = -\frac{Z_3}{L_{pp}}; A_{4:21,k} = -\frac{Z_4}{L_{pp}}$$

$$A_{5:1,k} = A_{5:15,k} = A_{5:19,k} = A_{6:2,k} = A_{6:16,k} = A_{6:20,k} = 1/C_p$$

$$A_{7:3,k} = -A_{7:17,k} = A_{7:19,k} = A_{8:4,k} = -A_{8:18,k} = A_{8:20,k} = 1/C_s$$

$$A_{9:15,k} = A_{10:16,k} = 1/C_{p_{in}}; A_{11:17,k} = A_{12:18,k} = 1/C_{s_{in}}$$

$$A_{13:19,k} = A_{14:20,k} = 1/C_{ps_{in}}$$

$$A_{15:5,k} = A_{15:9,k} = A_{16:6,k} = A_{16:10,k} = -\frac{1}{L_{p_{in}}}$$

$$A_{17:7,k} = -A_{17:11,k} = A_{18:8,k} = -A_{18:12,k} = \frac{1}{L_{s_{in}}}$$

$$A_{17:3,k} = A_{18:4,k} = -\frac{Z_1}{L_{s_{in}}} \; ; A_{17:4,k} = A_{18:3,k} = \frac{Z_2}{L_{s_{in}}}$$

$$A_{17:21,k} = -\frac{Z_3}{L_{s_{in}}} \; ; A_{18:21,k} = -\frac{Z_4}{L_{s_{in}}}$$

$$A_{19:3,k} = A_{20:4,k} = -\frac{Z_1}{nL_{ps_{in}}} \quad ; A_{19:4,k} = A_{20:3,k} = \frac{Z_2}{nL_{ps_{in}}}$$

$$A_{19:5,k} = A_{19:13,k} = A_{20:6,k} = A_{20:14,k} = -\frac{1}{L_{ps_{in}}}$$

$$A_{19:9,k} = A_{20:8,k} = -\frac{1}{nL_{ps_{in}}}$$

$$A_{19:21,k} = -\frac{Z_3}{nL_{ps_{in}}} \qquad ; A_{20:21,k} = -\frac{Z_4}{nL_{ps_{in}}}$$

$$A_{21:3,k} = \frac{2}{k\pi C_o}\frac{R_{o,k}}{R_{o,k}+r_{C_o}}\frac{I_{s_S,k}}{I_{sT},k} \; ; A_{21:3,k} = \frac{2}{k\pi C_o}\frac{R_{o,k}}{R_{o,k}+r_{C_o}}\frac{I_{s_C,k}}{I_{sT},k}$$

$$A_{21:21,k} = -\frac{1}{C_o}\frac{1}{R_{o,k}+r_{C_o}}$$

$$C_{3,k} = \frac{2}{k\pi}\frac{R_{o,k}r_{C_o}}{R_{o,k}+r_{C_o}}\frac{I_{ss,k}}{I_{sT,k}} \; ; C_{4,k} = \frac{2}{k\pi}\frac{R_{o,k}r_{C_o}}{R_{o,k}+r_{C_o}}\frac{I_{sC,k}}{I_{sT,k}} \; ; C_{21,k} = \frac{R_{o,k}}{R_{o,k}+r_{C_o}}$$

$$B_k = \begin{bmatrix} k\omega_o I_{p_c,k} & \frac{Z_5}{L_{ss}} & \frac{Z_6}{L_{ss}} \\ -k\omega_o I_{p_s,k} & 0 & 0 \\ k\omega_o I_{s_c,k} & \frac{Z_5}{L_{mm}} & \frac{Z_6}{L_{mm}} \\ -k\omega_o I_{s_s,k} & 0 & 0 \\ k\omega_o V_{C_{p_c},k} & 0 & 0 \\ -k\omega_o V_{C_{p_s},k} & 0 & 0 \\ k\omega_o V_{C_{s_c},k} & 0 & 0 \\ -k\omega_o V_{C_{s_s},k.} & 0 & 0 \\ k\omega_o V_{C_{p_{in_c}},k} & 0 & 0 \\ -k\omega_o V_{C_{p_{in_s}},k} & 0 & 0 \\ k\omega_o V_{C_{s_{in_c}},k} & 0 & 0 \\ -k\omega_o V_{C_{s_{in_s}},k} & 0 & 0 \\ k\omega_o V_{C_{ps_{in_c}},k} & 0 & 0 \\ -k\omega_o V_{C_{ps_{in_s}},k} & 0 & 0 \\ k\omega_o I_{C_{p_{in_c}},k} & \frac{Z_5}{L_{p_{in}}} & \frac{Z_6}{L_{p_{in}}} \\ -k\omega_o I_{C_{p_{in_s}},k} & 0 & 0 \\ k\omega_o I_{C_{s_{in_c}},k} & 0 & 0 \\ -k\omega_o I_{C_{s_{in_s}},k} & 0 & 0 \\ k\omega_o I_{C_{ps_{in_c}},k} & \frac{Z_5}{L_{ps_{in}}} & \frac{Z_6}{L_{ps_{in}}} \\ -k\omega_o I_{C_{ps_{in_s}},k} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

APPENDIX B

SUPPLEMENTARY EQUATIONS FOR FORMULATING THE PORT POWER EQUATIONS FOR TAC^{3}L^3 CONVERTER

The following coefficients are used to formulate the port power equations, as referred in (5.10)-(5.12).

$$M_{P1} = \sum_{k=1}^{2m+1}\left\{\frac{1}{2\mathrm{k}^2|Z_{1,k}|}\cos(\alpha_{1,k})\, d_{P,k}^2\right\}$$

$$M_{P2} = \sum_{k=1}^{2m+1}\left\{\frac{|Z_{x_{21},k}|}{2\mathrm{k}^2|Z_{2,k}|}\cos(k\varphi_S + \alpha_{2,k} - \beta_{21,k})\, d_{S,k}d_{P,k}\right\}$$

$$M_{P3} = \sum_{k=1}^{2m+1}\left\{\frac{|Z_{x_{31},k}|}{2\mathrm{k}^2|Z_{3,k}|}\cos(k\varphi_T + \alpha_{3,k} - \beta_{31,k})\, d_{T,k}d_{P,k}\right\}$$

$$M_{S1} = \sum_{k=1}^{2m+1}\left\{\frac{1}{2\mathrm{k}^2|Z_{2,k}|}\cos(\alpha_{2,k})\, d_{S,k}^2\right\}$$

$$M_{S2} = \sum_{k=1}^{2m+1}\left\{\frac{|Z_{x_{11},k}|}{2|Z_{1,k}|}\cos(\alpha_{1,k} - \beta_{11,k} - k\varphi_S)\, d_{P,k}d_{S,k}\right\}$$

$$M_{S3} = \sum_{k=1}^{2m+1}\left\{\frac{|Z_{x_{32},k}|}{2\mathrm{k}^2|Z_{3,k}|}\cos(k\varphi_T + \alpha_{3,k} - \beta_{32,k} - k\varphi_S)\, d_{T,k}d_{S,k}\right\}$$

$$M_{T1} = \sum_{k=1}^{2m+1}\left\{\frac{1}{2\mathrm{k}^2|Z_{3,k}|}\cos(\alpha_{3,k})\, d_{T,k}^2\right\}$$

$$M_{T2} = \sum_{k=1}^{2m+1}\left\{\frac{|Z_{x_{12},k}|}{2\mathrm{k}^2|Z_{1,k}|}\cos(\alpha_{1,k} - \beta_{12,k} - k\varphi_T)\, d_{P,k}d_{S,k}\right\}$$

$$M_{T3} = \sum_{k=1}^{2m+1}\left\{\frac{|Z_{x_{22},k}|}{2\mathrm{k}^2|Z_{2,k}|}\cos(k\varphi_S + \alpha_{2,k} - \beta_{22,k} - k\varphi_T)\, d_{S,k}d_{T,k}\right\}$$

APPENDIX C

SUPPLEMENTARY EQUATIONS FOR FORMULATING THE RMS VALUES OF PORT CURRENTS FOR TAC^{3}L^3 CONVERTER

The following coefficients ($A_{k,X}$ and $B_{k,X}$for $X \in \{P, S, T\}$) are used to formulate the RMS values of port currents in (5.15)-(5.16):

$$A_{k,P} = \frac{4V_{in}}{\pi k|Z_{1,k}|}\cos(\alpha_{1,k})\cos(k\delta_P) + \frac{4V'_{oS}}{\pi k|Z_{2,k}|}|Z_{x21,k}|\cos(k\varphi_S + \alpha_{2,k} - \beta_{21,k})\cos(k\delta_S) +$$

$$\frac{4V'_{oT}}{\pi k|Z_{3,k}|}|Z_{x31,k}|\cos(k\varphi_T + \alpha_{3,k} - \beta_{31,k})\cos(k\delta_T)$$

$$B_{k,P} = -\left\{\frac{4V_{in}}{\pi k|Z_{1,k}|}\sin(\alpha_{1,k})\cos(k\delta_P) + \frac{4V'_{oS}}{\pi k|Z_{2,k}|}|Z_{x21,k}|\sin(k\varphi_S + \alpha_{2,k} -\right.$$

$$\left.\beta_{21,k})\cos(k\delta_S) + \frac{4V'_{oT}}{\pi k|Z_{3,k}|}|Z_{x31,k}|\sin(k\varphi_T + \alpha_{3,k} - \beta_{31,k})\cos(k\delta_T)\right\}$$

$$A_{k,S} = -\frac{4V'_{oS}}{k\pi|Z_{2,k}|}\cos(k\varphi_S + \alpha_{2,k})\cos(k\delta_S) + \frac{4V_{in}}{k\pi|Z_{1,k}|}|Z_{x11,k}|\cos(\alpha_{1,k} -$$

$$\beta_{11,k})\cos(k\delta_P) - /\frac{4V'_{oT}}{k\pi|Z_{3,k}|}|Z_{x32,k}|\cos(k\varphi_T + \alpha_{3,k} - \beta_{32,k})\cos(k\delta_T)$$

$$B_{k,S} = \frac{4V'_{oS}}{k\pi|Z_{2,k}|}\sin(k\varphi_S + \alpha_{2,k})\cos(k\delta_S) - \frac{4V_{in}}{k\pi|Z_{1,k}|}|Z_{x11,k}|\sin(\alpha_{1,k} - \beta_{11,k})\cos(k\delta_P) +$$

$$\frac{4V'_{oT}}{k\pi|Z_{3,k}|}|Z_{x32,k}|\sin(k\varphi_T + \alpha_{3,k} - \beta_{32,k})\cos(k\delta_T)$$

$$A_{k,T} = -\frac{4V'_{oT}}{\pi k|Z_{3,k}|}\cos(k\varphi_T + \alpha_{3,k})\cos(k\delta_T) + \frac{4V_{in}}{\pi k|Z_{1,k}|}|Z_{x12,k}|\cos(\alpha_{1,k} -$$

$$\beta_{12,k})\cos(k\delta_P) - \frac{4V'_{oS}}{\pi k|Z_{2,k}|}|Z_{x22,k}|\cos(k\varphi_S + \alpha_{2,k} - \beta_{22,k})\cos(k\delta_S)$$

$$B_{k,T} = \frac{4V'_{oT}}{\pi k|Z_{3,k}|}\sin(k\varphi_T + \alpha_{3,k})\cos(k\delta_T) - \frac{4V_{in}}{\pi k|Z_{1,k}|}|Z_{x12,k}|\sin(\alpha_{1,k} - \beta_{12,k})\cos(k\delta_P) +$$

$$\frac{4V'_{oS}}{\pi k|Z_{2,k}|}|Z_{x22,k}|\sin(k\varphi_S + \alpha_{2,k} - \beta_{22,k})\cos(k\delta_S)$$