Time Division Synchronization For Distributed Transceiver Architectures

by

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ABSTRACT

Data transmission and reception has become an important aspect in day-to-day communication. With advancement in technology, it dictates the need for accurate data transmission and reception. For this very reason, wireless transceivers are employed in almost every industrial domain for numerous applications. A special concept of distributed transceivers is proven to be extremely useful in the latest technologies like Internet of Things. As the name suggests, this is a collaborative communication technique where multiple transceivers are synchronized for faster and much more reliable communication. This imposes a major challenge while designing this kind of a transceiver, as all the transceivers should be operating with carrier synchronization to maintain the proper collaboration.

While there are several ways to establish this sync, this thesis emphasizes one of those techniques and tries to resolve the issue in design. The carrier synchronization is achieved using time division synchronization technique. Several challenges in implementing this technique were addressed using various models simulated in MATLAB Simulink and Keysight ADS. An in detail analysis has been performed for all the techniques used for this implementation to provide a diverse perspective.

DEDICATION

Dedicated to my parents Boorela Venkata Ramadas and Ganduri Padmavathi, my beloved sister Boorela Venkata Sriharshini and my dear relatives and friends who constantly supported me at all times

ACKNOWLEDGMENTS

Firstly, I would like to express my deepest gratitude to my faculty advisor, Professor Saeed Zeinolabedinzadeh, who extended his constant support throughout my years of study. His ideas and knowledge inspired me to take up thesis and helped me to successfully finish my work. It was a great opportunity collaborating with him and to gain this research experience under his guidance.

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INTRODUCTION

1.1 Distributed Transceiver Systems

Wireless networks have received a great deal of interest in recent years because of their application, particularly in distributed radar networks. Distributed transceivers provide a cooperative communication technique as shown in Figure 1.1, where different transceivers commonly transmit the same message, by aligning their phases while transmitting the signal[7].

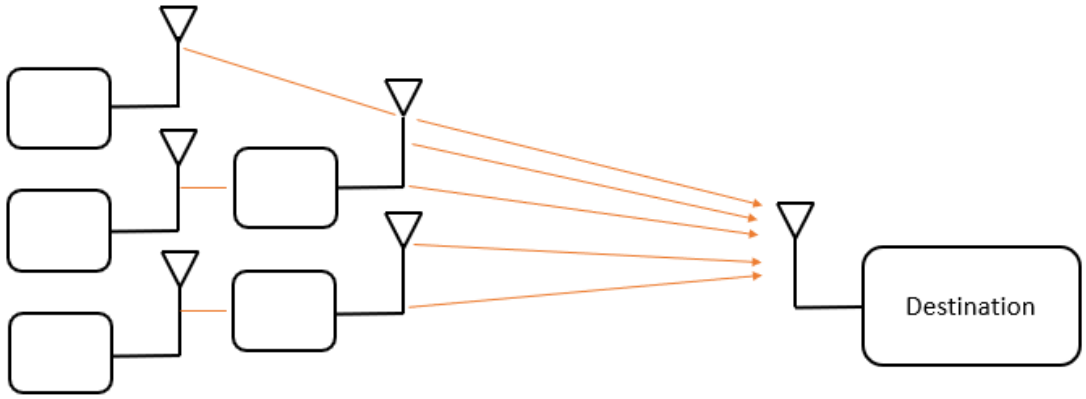

Figure 1.1: Distributed Transceiver Beamforming [7]

One of the major challenges is to make sure that the transceivers are synchronized with time and with carrier frequencies, to allow an organized exchange of data. Because each source in the distributed network has its own oscillator, the oscillators' frequencies will deviate from one another due to a variety of conditions, destructing the purpose of operation. Furthermore, when the sources are installed inside moving platforms such as airplanes, the frequency stability performance will be severely impacted. In order to combine the signals effectively at the destination, each transceiver

must transmit a common message signal at the same time, and monitor the phase of the carrier signals by synchronizing them continuously. As a result, this facilitates a need for developing distributed transceiver systems for information sharing, timing synchronization, and carrier synchronization to make this concept a reality.[7]

A wide range of frequency/phase synchronization schemes have been proposed over the years[3]. Instead of taking advantage of the wireless channel's broadcast characteristics, most of these alternatives use point-to-point transmission. The receiver must be in a location that allows it to establish line-of-sight contact with the transmitter in order to receive the direct-path signal. As a result, to eliminate or minimize the frequency offset, establishing novel frequency synchronization techniques is important from both a practical and theoretical standpoint, and it demands attention on its own.

1.2 Methods of Synchronization

In the distributed transceiver network, a master-slave architecture can be employed where one transceiver acts as a master transceiver that sets an order and alignment for the other transceivers acting as slaves. In order to achieve phase synchronization between the master and the slave transceivers and also among the slave transceivers, the two fundamentally used methods are: Closed loop synchronization and open loop synchronization [12].

In the closed loop synchronization technique, the destination, a master transceiver, checks the frequency/phase offset of the signals sent by the slave transceivers, and quantizes the offset. It then provides the phase correction data back to the respective sources in the form of a digital feedback signal. This can be seen in Figure 1.2. The interaction between the source transceivers is minimum since the destination coordinates the synchronization process.

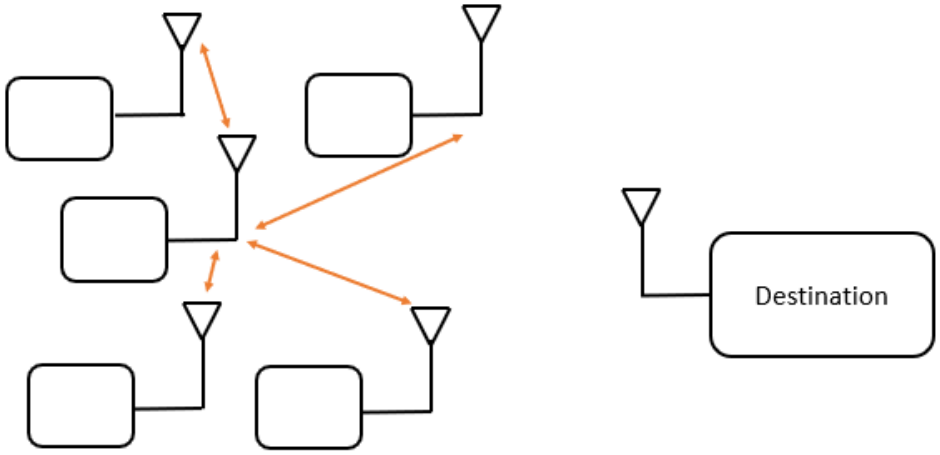

Figure 1.2: Closed Loop Synchronization [7]

Whereas in the open loop technique, the destination broadcasts a reference signal to the sources. Transceivers will utilize this reference signal, as well as information transmitted within themselves, to align the phases of their signals and combine them at the destination as shown in Figure 1.3. This emphasizes on local interactions between the sources and reduces the interaction with the destination far away. When the number of transceivers is considerably large, the time slot employed in this method might become very sophisticated, limiting the system's scalability and reliability.

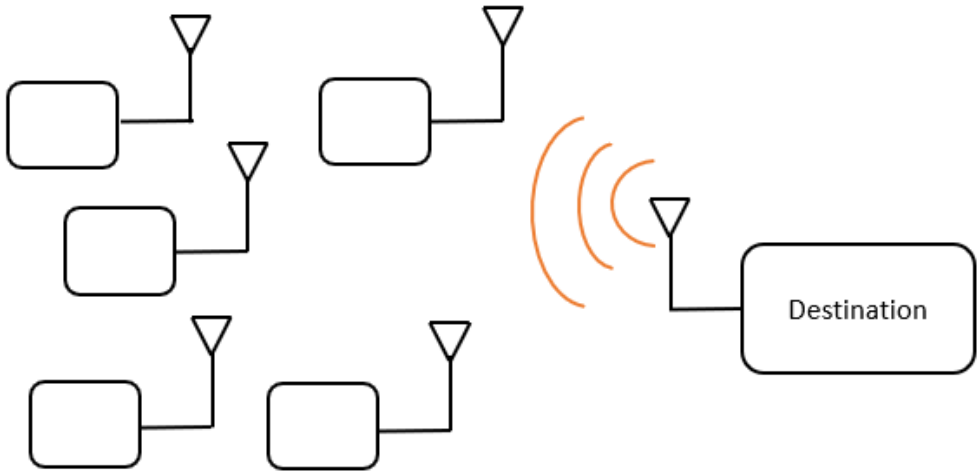

Figure 1.3: Open Loop Synchronization [7]

To create frequency-synchronized carrier signals, the slave transmitters can employ phase locked loops to lock to a reference carrier signal transmitted by the master transmitter.[7] However, due to uncertain propagation delays in wireless channels and Doppler effects, this approach leaves undetermined phase offsets between the carrier signals, for which time synchronization is absolutely necessary.

Based on the type of signal transmitted to provide synchronization, there are two different carrier frequency synchronization techniques. The first is continuous duplex synchronization, in which the synchronization signal is continuously transmitted by both the transmitter and the receiver. Synchronization and communication is done simultaneously in this method. The system hardware must be able to transmit and receive data at the same time, and the signals must be properly isolated.

The second type of synchronization technique is pulsed alternative synchronization, in which the synchronization and communication is performed in a periodic pattern by both the transmitter and receiver. Full-duplex system hardware is not required in this instance, and the signals are intrinsically separated, allowing for the use of a single carrier frequency.

1.3 Thesis Motivation

The aim of this thesis is to develop a time division carrier synchronization system that can be applicable to any distributed transceiver application. To achieve this, a PLL is employed in the receiver that locks to the unmodulated carrier signal sent by the transmitter. The message signal and unmodulated carrier are transmitted in time divisions. The major contributions of this work can be described as follows:

- Developed a Simultaneous Synchronization and Communication technique for BPSK communication using PLL

- Proposed a solution to alleviate the issue of toggling reference input signal
- Designed an RC Filter and Simple Sample and Hold circuit to maintain the PLL's control voltage
- Conducted experimental and comparative analysis of the proposed design on synchronization and communication

1.4 Thesis Organization

The remaining sections of this document are organized as follows. Chapter II consists of a brief introduction to the distributed transceiver architecture and how BPSK is useful in achieving the desired properties. Chapter III discusses the carrier frequency synchronization approach using PLL in detail. It contains elaborate information about phase locked loops and some of its blocks and their characteristics along with equations. The practical implementation of the time division synchronization, problems encountered and proposed solutions are specified. This is followed by performance analysis of the proposed design in Chapter IV. Conclusion, future work and references are provided in Chapter V.

Chapter 2

TRANSCEIVER DESIGN

2.1 Transceiver Model

In single carrier or multi carrier systems, carrier synchronization is a critical component of coherent communication transceivers. Carrier frequency offset is unavoidable due to non-ideal phenomena such as Doppler effect and mismatching of local oscillators between transmitter and receiver. Phase Locked Loops (PLLs) are one of the most useful traditional approaches for performing carrier synchronization.

There are several other techniques that provide phase/frequency synchronization [8] to the oscillators that influence the operation of the transceivers. In this thesis, the idea is based on utilizing the concept of time division synchronization which involves a periodic synchronization routine to keep the transmitter and receiver in continuous sync. The transceiver architecture employing time division carrier synchronization is shown by the Figure 2.1.

The transmitter consists of a modulator with a message signal and a high frequency carrier signal generated by a local oscillator. BPSK (Binary Phase Shift Keying) modulation technique has been used for a simple demonstration of this technique. The receiver on the other hand contains a demodulator with a synchronizing PLL (described in Chapter 3) which is used to synchronize the receiver to the carrier signal at the receiver.

The transmitter sends out the carrier signal first in order to perform the synchronization duty. When the receiver is ready, the modulated signal is then transmitted and the synchronized carrier frequency is used to retrieve the message signal at the

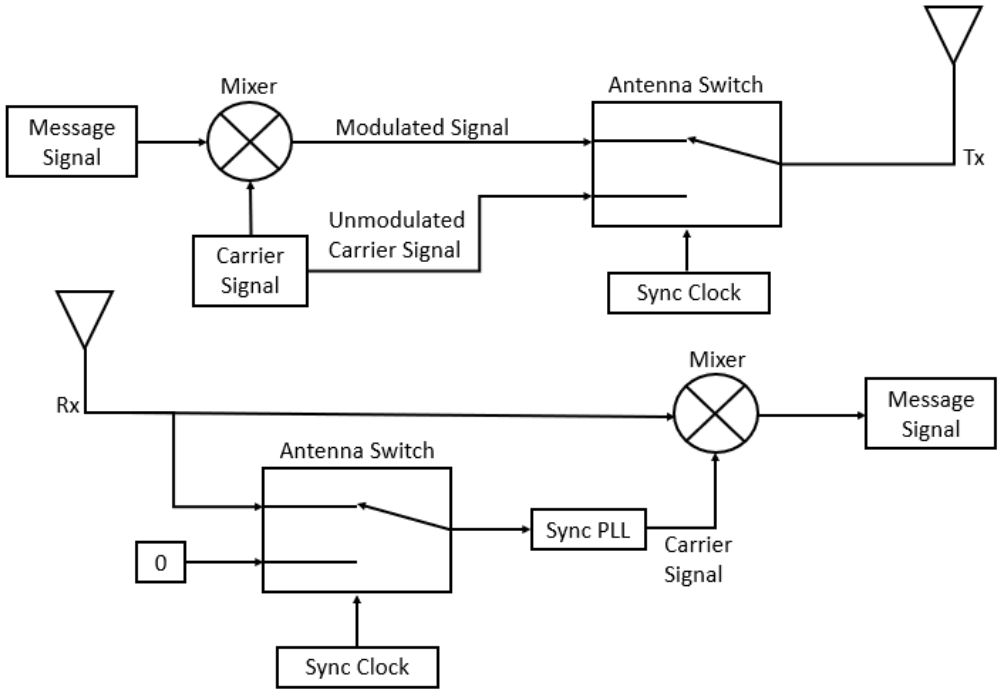

Figure 2.1: Transceiver Architecture

receiver. In order to achieve this type of time division synchronization, the transmitter has to periodically transmit the unmodulated carrier signal which will be used by the receiver to be in sync as shown by the Figure 2.2. [13]

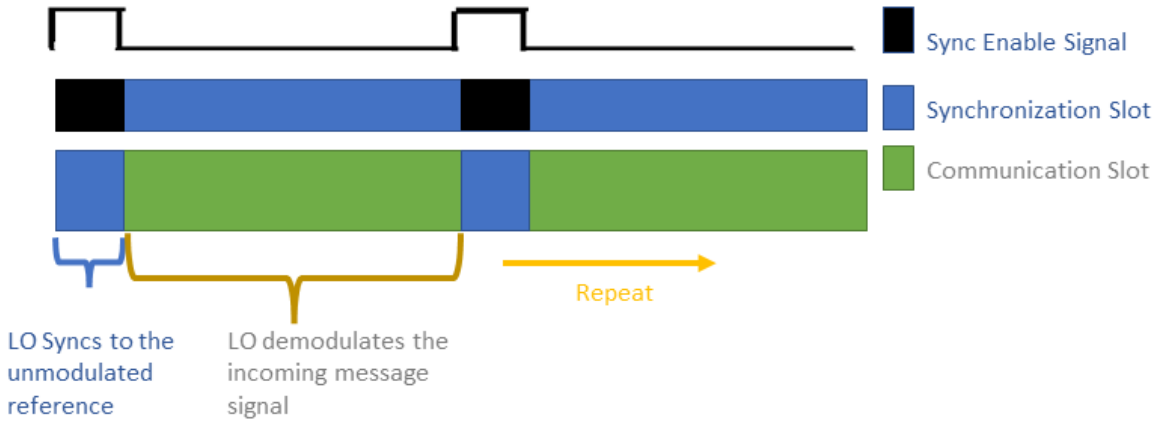

Figure 2.2: Transceiver Synchronization Timing

This can be achieved by assigning the message data bits to '1' for a specific time period at the transmitter. When the carrier signal is multiplied with a constant (=1),

the modulated signal will be the same as the carrier signal.

This time is utilized by the PLL to receive the carrier signal and lock the oscillator to the high frequency signal without being subjected to phase or frequency variations. When the PLL is locked and in sync with the carrier frequency, it acts as a local oscillator to demodulate the upcoming data till the next routine. This sync routine is monitored using a sync enable signal, a clock signal locally generated at the transmitter and receiver, which can be instantiated by a square pulse with its amplitude varying from 0 to 1 volts, as shown in the figure. The duty cycle and time period specifications of this signal determine the refresh rate and duration of the synchronization.

Chapter 3

TIME DIVISION SYNCHRONIZATION

3.1 Understanding PLL

PLLs (phase locked loops) are common circuits found in wide range of communication and engineering applications. To attain high frequency accuracy, most synthesizers utilize the concept of "phase-locking." A PLL is a non-linear negative feedback loop comprising a voltage controlled oscillator (VCO), a loop filter or a low pass filter (LPF) and a phase detector (PD) that locks the phase of the oscillator to a reference signal. A phase locked loop tries to keep the phase and frequency of the input signal and the voltage/current driven oscillator as constant as possible. [9]

Capture range and locking range: The capture range is the frequency range for which the loop locks from an initially unlocked state. On the other hand, the locking range can be defined as the range of frequencies for which the PLL stays locked. The capture range is smaller than the locking range.

The block diagram of a typical analog PLL is shown below:

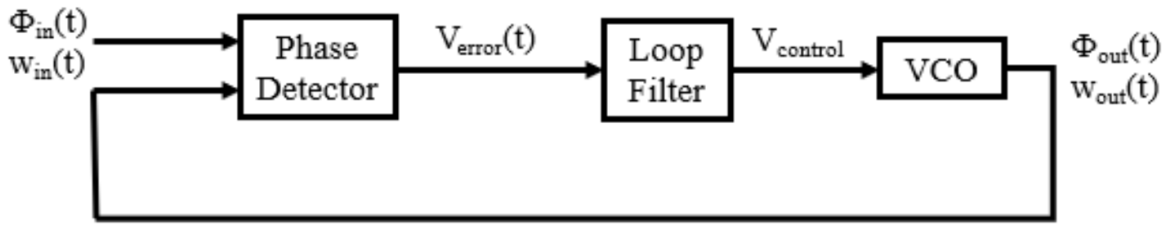

Figure 3.1: PLL Block Diagram [9]

3.2 PLL operation

The loop filter's output determines the angular frequency of the periodic signal generated by the VCO. The phase detector compares the phase of the output signal to the phase of the input periodic signal, resulting in an output proportional to the phase difference between the input and output. The output from the phase detector has a DC component and an AC component which can be eliminated by the loop filter. If a phase error mismatch develops, the system tries to minimize it by repeating the same procedure.

$$\phi_{out} - \phi_{in} = constant$$

$$\frac{d\phi_{out}}{dt} - \frac{d\phi_{in}}{dt} = 0$$

$$\omega_{in} = \omega_{out}$$

The operation of the PLL system is divided into three blocks:

Phase Detector: A phase detector (PD) or a phase/frequency detector (PFD) is the first component of the PLL. The phase detector provides an error signal which is equivalent to the phase difference between its two inputs, one of which is the reference signal and the other one being the feedback VCO output signal. For high frequency applications, a divider is sometimes employed to divide the VCO output frequency before it reaches the phase detector. The phase detector develops an output by comparing the phase of the output signal and the reference signal.

$$V_{error} = K_{PD}\Delta\phi$$

where,

K_{PD} represents the gain of Phase Detector

$\Delta\phi$ is the phase error

The AC component present in Verror(t) is eliminated by the loop filter. When KPD is at its ideal value, i.e. 1, the phase detector does not amplify the error signal and the output is proportional to the phase/frequency difference between the input and output.

An analog multiplier/mixer can also be used as a phase frequency detector.[1] [5]

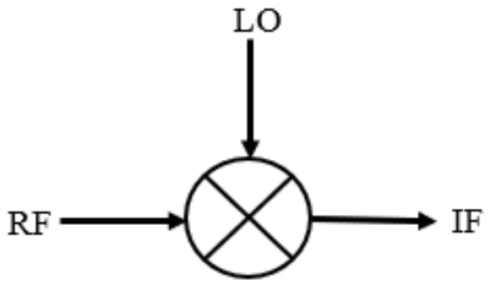

Figure 3.2: Mixer As Phase Detector [1]

Mixer operation: A mixer combines the message RF signal and the carrier LO signal in such a way that the amplitude of the resultant signal is obtained by product of amplitudes of RF and LO signals and the frequency component contains a sum of frequencies and a difference between the RF and LO frequencies.

In order to understand this better, let the signals multiplied by the mixer be $A\cos(wt)$ and $B\cos(wt+\phi)$. The resultant signal can be defined as:

$$V_{error} = A\cos(wt) * B\cos(wt+\phi)$$

After passing through the loop filter, the high frequency component is removed and the remaining error component can be written as:

$$V_{error}(t) = \frac{AB}{2}\cos\phi$$

An error signal is generated which is proportional to the phase difference between PLL input and output signals. If the signals are in phase, the output error signal is

constant. The error signal varies as long as the signals are out of phase. A negative feedback is generated across the loop that keeps generating the error voltage until the phases match.

Loop Filter: The loop filter is the system's second component. It specifies the capture range (bandwidth) and tracking range, as well as it helps in determining the dynamic features of PLL. Though a higher cutoff frequency allows for faster frequency shifts, it is critical to remove high frequency components at the phase detector's output, as they may emerge as spurious signals at the VCO input. These signals are then converted to a control voltage that is utilized to bias the VCO by the loop filter. The VCO oscillates at a higher or lower frequency depending on the control voltage, affecting the phase and frequency of the feedback. If the PFD generates an up signal, the VCO frequency is increased. The VCO frequency is lowered by a down signal.

Loop filters can be implemented using active or passive elements. In analog PLLs, the loop filter is used to remove the high frequency components at the PFD's output. In digital PLLs, they operate as an averaging filter, averaging the PFD's output. The loop filter is also necessary for maintaining loop stability. When driven by a phase detector with a voltage output, a loop filter behaves differently from when controlled by a charge pump phase detector with a current output.

VCO: The Voltage Controlled Oscillator (VCO) is the third block in the PLL, which functions as a positive feedback amplifier. The VCO's output varies with the input control voltage (generated by the loop filter) until the input reference frequency and the output frequency are equal. Until an input signal is applied, the VCO oscillates at its own frequency - the free running frequency, also called the quiescent frequency.

The response of the VCO to the error signal generated by the phase detector is as shown in Figure 3.3.

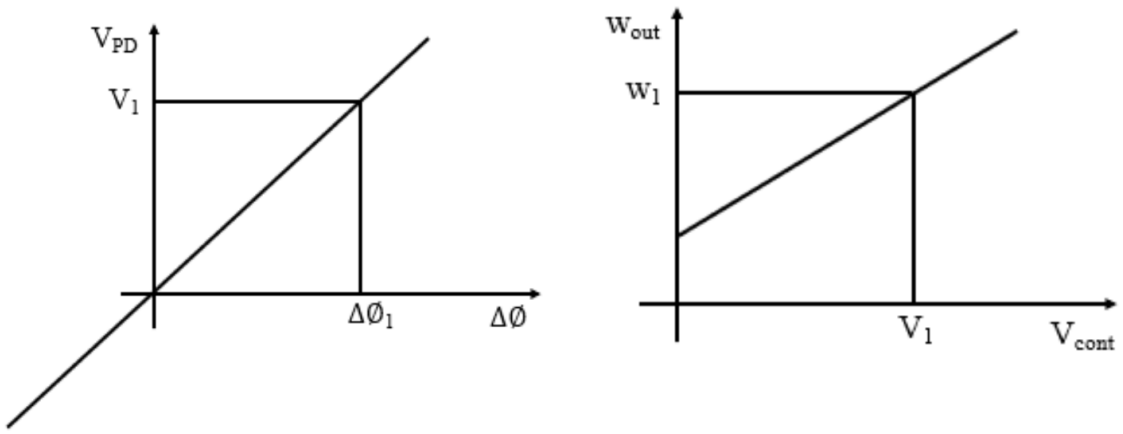

Figure 3.3: VCO Response To Phase Detector [10]

The Phase Detector generates a dc value equal to V1 if $\Delta\phi = \Delta\phi_1$ which is called the static phase error. When $V_{cont} = V_1$, VCO operates at frequency ω_1.

The output frequency can be obtained as follows:

$$\phi_{out} = K_{VCO} \int_{-\infty}^{t} V_{cont} dt$$

$$\omega_{out} = \omega_0 + K_{VCO} * V_{cont}$$

where,

K_{VCO} is the sensitivity of the VCO

ω_0 is the quiescent frequency of the VCO

V_{cont} is the control voltage fed into the VCO

ω_{out} is the generated output frequency by the VCO

VCOs have tank circuits and oscillate owing to noise from the amplifier's noise figure. The VCO reaches a stable state as soon as the amplifier approaches saturation. As a result, the VCO's output spectrum is said to contain a bandpass amplified noise response. The loop filter's output is a fluctuating voltage that forces the VCO to respond quickly in order to minimize the frequency difference between the output

and the input frequency. When the two frequencies are matched, the loop goes into a locked condition.

PLL regions of operation:

Lock range: It is the frequency range of the input signal for which the loop remains locked once it's been captured. The time it takes for a PLL to create the desired frequency with phase matching is known as lock time.

Hold Range: The frequency range in which the PLL can sustain phase tracking is referred to as the hold range. It is determined by measuring the frequency offset at the reference input, where phase error is greatest, and varies depending on the type of phase detector employed.

Pull-in range: The pull-in range is the whole frequency range, centered on the VCO center frequency, across which the PLL eventually achieves phase lock and manages to stay locked. As a result, the PLL can lock as long as the reference input is inside the pull-in range.

Pull-out range: The pull-out range is a metric for the PLL's dynamic response. The frequency step applied to the reference signal that causes the PLL to unlock is defined based on the pull-out range. The PLL will remain locked if the reference signal provided to it is smaller than the pull-out range. As soon as the frequency step exceeds the pull-out, the PLL will slide off. The PLL can certainly revert to its locked state, but the sole disadvantage is that it will take a lot longer.

3.3 PLL Model

To understand the loop parameters of the PLL, its behaviour is analyzed in phase domain as shown in Figure 3.4.[11] The input can be defined as a reference input phase ϕ_{ref} which is compared to the output phase ϕ_{out} of the signal generated by the VCO, whose phase domain transfer function is given by $\frac{K_{VCO}}{s}$. The gain factor of the

phase detector is given by K_{PD} and the transfer function of the loop filter is defined as H(s). The feedback factor is given by $\frac{1}{N}$ i.e. the frequency divider ratio.

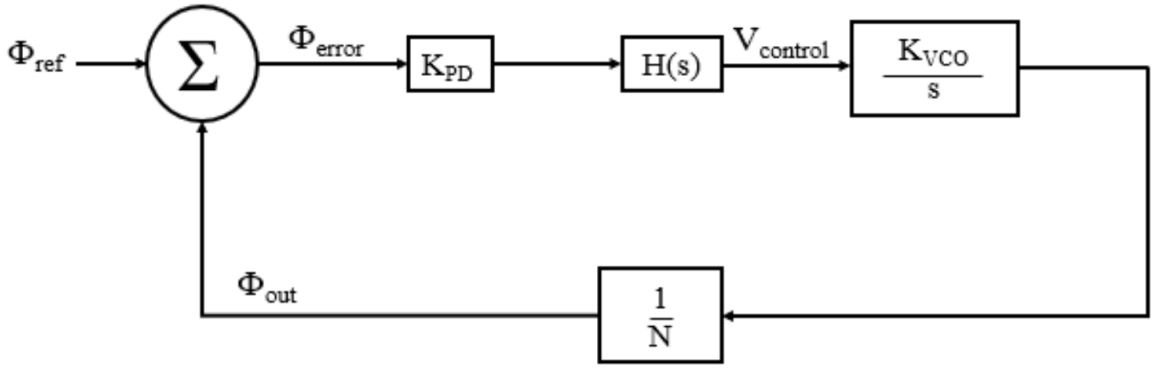

Figure 3.4: PLL Model In Phase Domain [11]

Open Loop gain can be written as:

$$A_{open}(s) = \frac{K_{PD}H(s)K_{VCO}}{Ns}$$

Closed Loop gain can be written as:

$$A_{closed}(s) = \frac{A}{1+A\beta} = \frac{K_{PD}H(s)K_{VCO}}{1+\frac{K_{PD}H(s)K_{VCO}}{N}}$$

H(s) depends on the type of filter used.

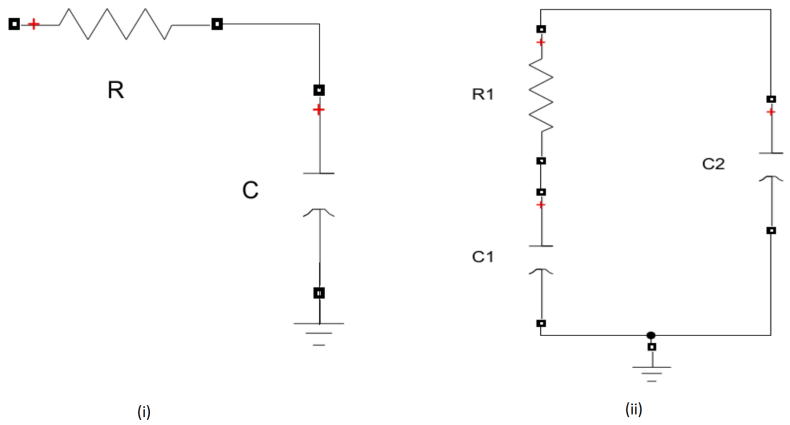

Figure 3.5: RC Filter (i)Single Pole RC Filter (ii)Pole Zero RC Filter

For a simple RC filter with a single pole:

$$H_{singlepole}(s) = \frac{1}{1 + \frac{s}{\omega_{LPF}}}$$

where,

$$\omega_{LPF} = \frac{1}{RC}$$

For a pole zero RC filter:

$$H_{polezero}(s) = \frac{sR1C1 + 1}{s[sR_1C_1C_2 + C_1C_2]}$$

Design Implementation: The basic PLL model has been implemented using Keysight ADS as shown in the Figure 3.6. An analog PLL has been modeled to work with a 24GHz reference signal with no frequency divider, while maintaining a loop bandwidth of 8MHz and phase margin of 75^0.

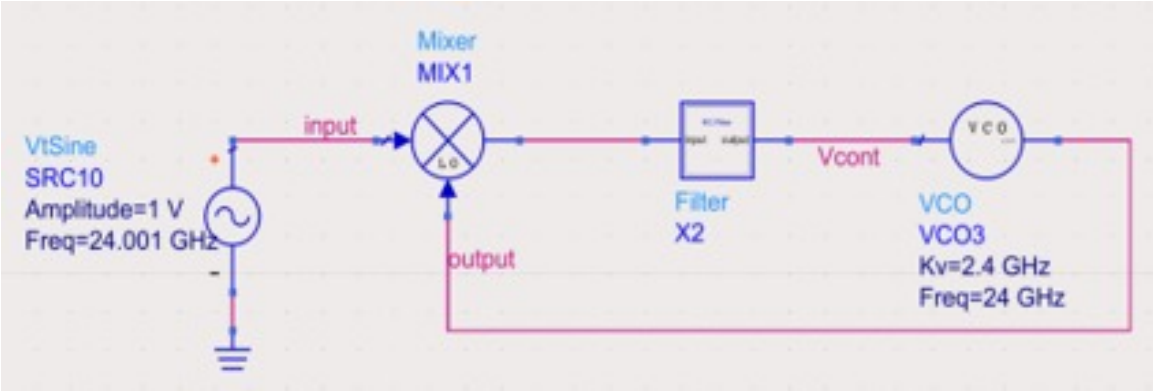

Figure 3.6: Basic PLL Implementation

Filter design used: In order to suppress the ripple caused by the $2f_0$ signal, a typical low pass filter requires at least a filter order greater than or equal to four. But, by increasing the order of the filter, the number of poles increases thereby affecting the stability of the PLL's loop response. In order to alleviate this problem, a third order pole-zero filter is used as the loop filter. This design has three poles and a zero which not only suppresses the ripple but also gives the best phase margin. Figure 3.7 shows the proposed design for the RC filter.

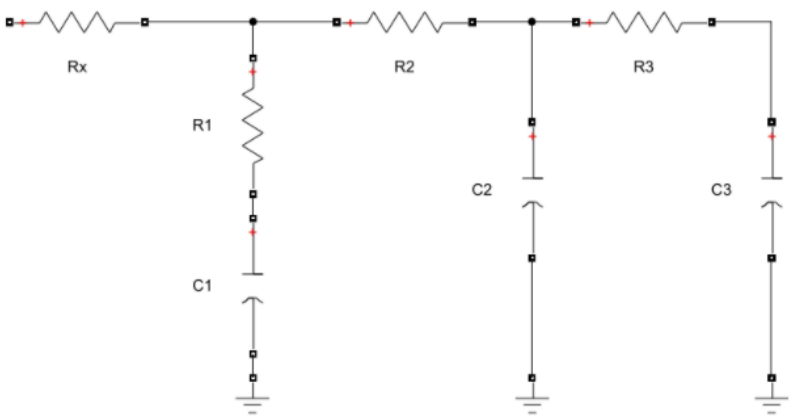

Figure 3.7: RC Filter Used

$$H(s) = \frac{sR_1C_1 + 1}{(1 + s(R_1 + R_x)C_1)(1 + sR_2C_2)(1 + sR_3C_3)}$$

where the zero and pole frequencies are given by,

$$\omega_{p1} = \frac{1}{(R_1 + R_x)C_1}$$

,

$$\omega_{p2} = \frac{1}{R_2C_2}$$

,

$$\omega_{p3} = \frac{1}{R_3C_3}$$

,

$$\omega_z = \frac{1}{R_1C_1}$$

,

The properties of the loop filter determine the settling time of the PLL as well as the amount of suppression of the $2f_0$ ripple on the control line.

The open loop and closed loop responses of this system are as shown in the Figures 3.8 and 3.9 respectively.

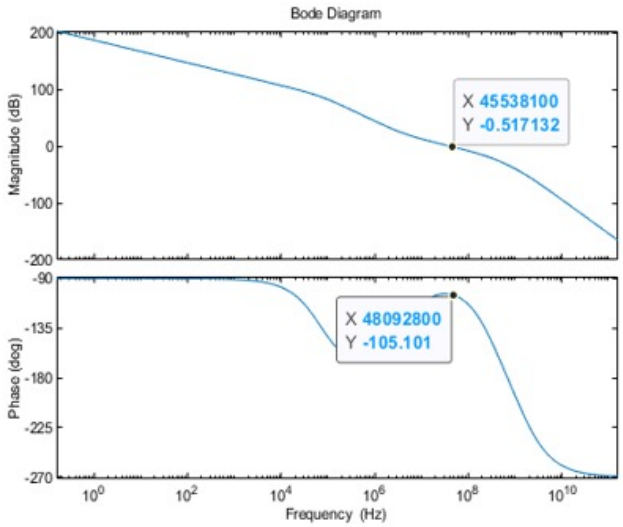

Figure 3.8: PLL Open Loop Response

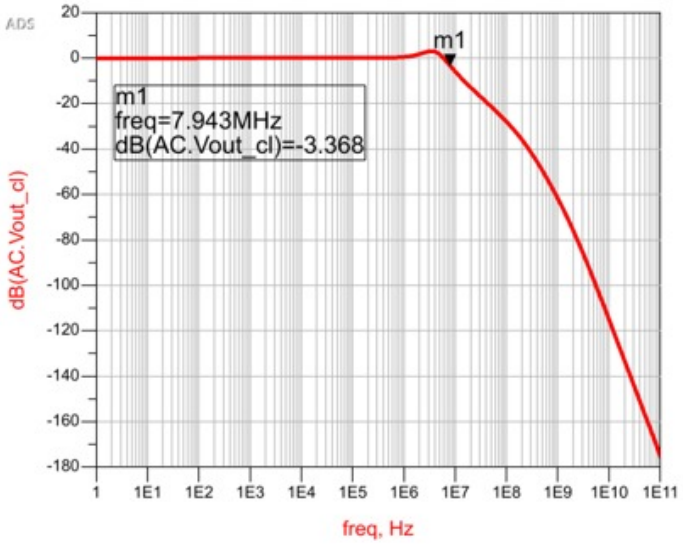

Figure 3.9: PLL Closed Loop Response

The plot of control voltage of the PLL with 24.005GHz input reference signal is shown by the Figure 3.10. The loop locks at 2mV within 30 nano seconds.

Since, a mixer is used as a phase detector, the error signal contains a high frequency $2f_0$ signal along with the low frequency component. The loop filter suppresses the amplitude of this $2f_0$ signal, which can be seen as a ripple on the control voltage line as shown in Figure 3.11.

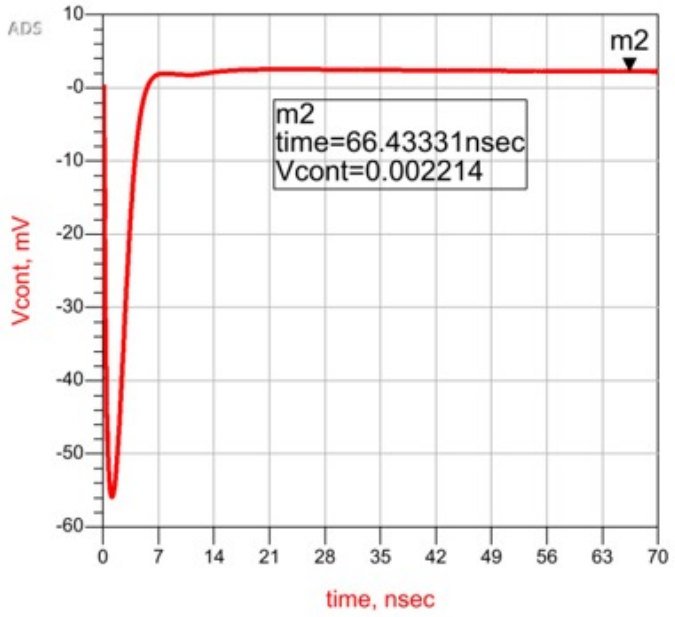

Figure 3.10: Control Voltage

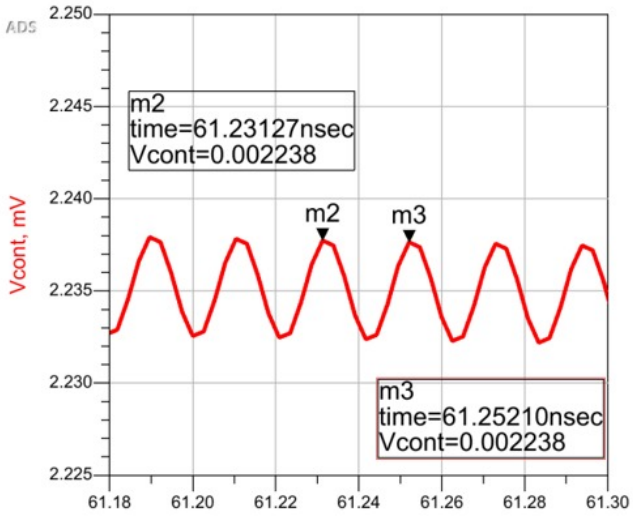

Figure 3.11: Ripple On Control Voltage Line

The locking range of this PLL is 24GHz +/- 10MHz which can be seen by the Figure 3.12.

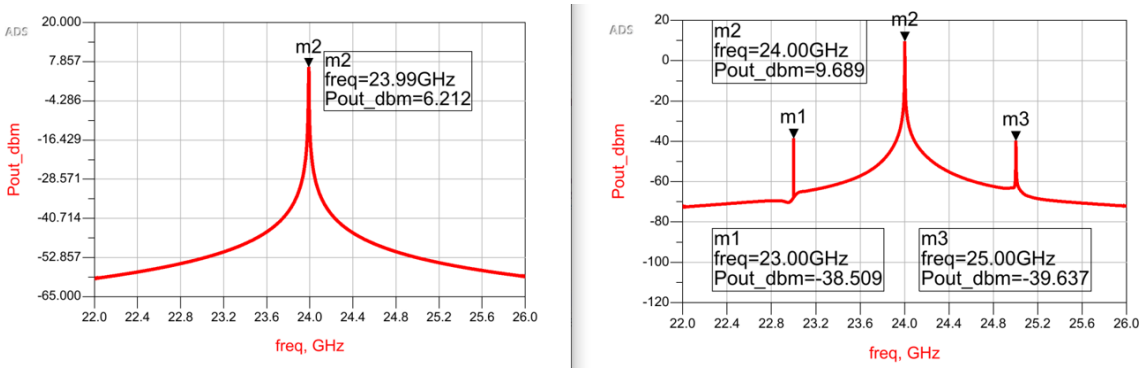

Figure 3.12: PLL Output Response At 10MHz And 1GHz Offset From Reference

3.4 PLL for Synchronization

In a basic point of view, a PLL is a device which can ensure a synchronization between two oscillators (reference and VCO). This property of the PLL can be utilized in the distributed transceivers to maintain the carrier synchronization. With this in mind, if we supply an unmodulated carrier signal to the receiver/slave PLL, it can adjust the VCO to the required frequency and act as the local oscillator. For this, we will be using the carrier broadcast technique that has been discussed in Chapter 1, where we periodically broadcast the unmodulated carrier signal from the master transmitter to maintain the sync.

3.4.1 Problem With Toggling Reference

A PLL that can ensure the sync with the unmodulated carrier for sure can establish the transceiver synchronization. However, the loop dynamics of a generic PLL demands the presence of a reference signal at all times. As we cannot use a modulated signal for synchronization, the unmodulated carrier will be stripped from the incoming signal and is supplied as a reference to the PLL. This raises the question of loop dynamics in the generic PLL. If we are stripping the unmodulated signal, we should replace the missing part with a DC zero volt signal(toggling reference) as

shown in the Figure 3.13.

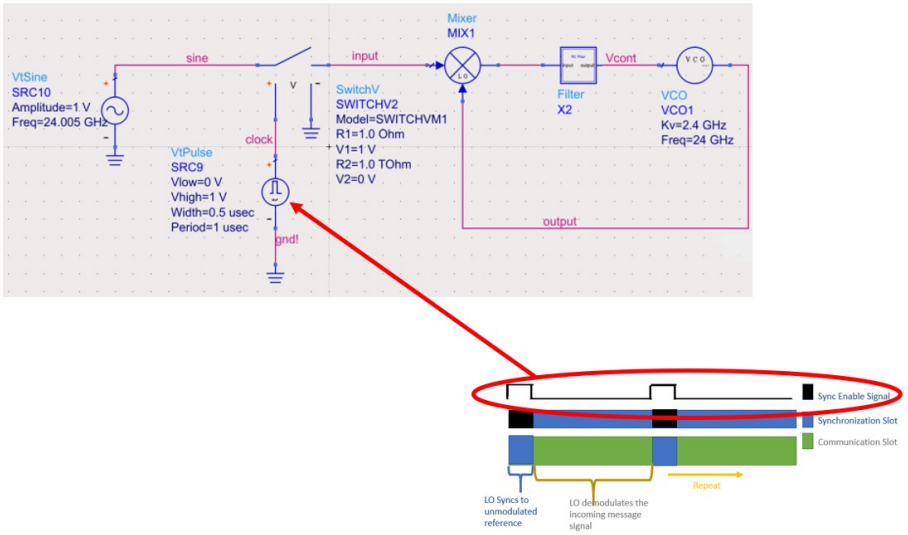

Figure 3.13: Toggling Reference Model

This disturbs the control line voltage as the phase detector (mixer) is comparing the 24GHz VCO output signal with a DC incoming signal. If the VCO has been pulled away from the required oscillating frequency, the PLL may never attain the lock even during the presence of the unmodulated carrier reference.

3.4.2 Proposed Solution

In order to alleviate the issue of toggling reference, the loop dynamics of the generic PLL must be altered in such a way that it does not respond to the undesired reference signal. If we take a closer look at the loop functioning, we just need to make sure that the VCO does not change its current operating frequency when there is no/undesired reference signal. So if the control voltage that determines the output frequency of the VCO stays constant during the undesired reference signal, or in other words, if the responses of the phase detector are ensured to not reach the control line of the VCO, we will be able to hold the local oscillator at the previously locked carrier frequency.

This can be done by installing a sample and hold circuit on the control line, after the loop filter. Using the sync enable signal as a clock signal to the sample and hold block, we can hold the control line to its current value before the reference signal changes, as shown in Figure 3.14 [4].

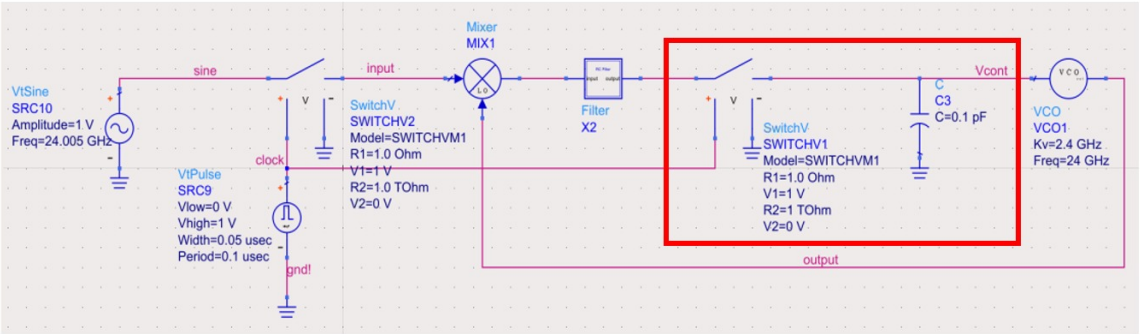

Figure 3.14: PLL With Sample And Hold Block

Once the unmodulated carrier signal is received as the reference, the PLL will be able to re-calibrate the operating frequency. This switching in the control line is basically restarting the PLL which means there is a locking time which the PLL takes to settle the control line. This is observed as periodic spurs on the VCO control line which in turn contributes to the phase noise that is discussed in the following chapter.

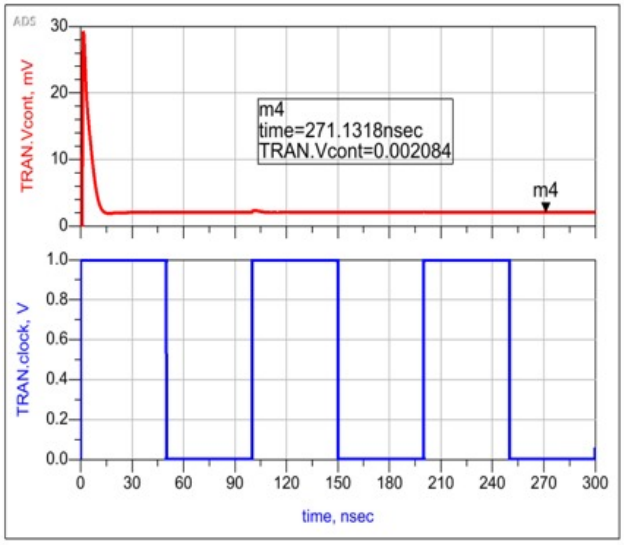

Figure 3.15: Control Voltage With Sample And Hold Block

Chapter 4

ANALYSIS AND SPECIFICATIONS

Although the sample and hold technique provides a solution to the synchronization problem, it comes with its own limitations and complexities which will be addressed in this chapter. Staring for a while on this idea, one can come up with several questions like: what are the upper and lower limits of the time interval of the sync pulses? How long do we have to maintain a single sync pulse? How is this going to affect the phase noise advantage provided by a typical PLL? Does the spurs on the control line caused by sample and hold switching have any effect on the phase noise or is it mitigated by the loop dynamics? If so, what are its limits? Several of these questions are answered by a quantitative analysis on experiments performed on the proposed design. We can understand the results from four different perspectives described below.

4.1 Phase Noise Analysis

The output phase noise profile of a phase-locked oscillator changes. In addition, phase noise in the PLL's reference input corrupts the output.[10]

VCO Phase Noise: The output phase of a PLL is always attempting to match the input phase. Even if the VCO has its own phase noise, the PLL tries to reduce the output phase noise to zero if the reference input has no phase noise. The loop identifies a considerable phase mismatch when the VCO phase noise develops and orders the PFD to rectify it.

Assuming H(s) to be the transfer function of a simple RC filter:

$$-\phi_{out}(K_{PD}(R+\frac{1}{sC}))\frac{K_{VCO}}{s}+\phi_{VCO}=\phi_{out}$$

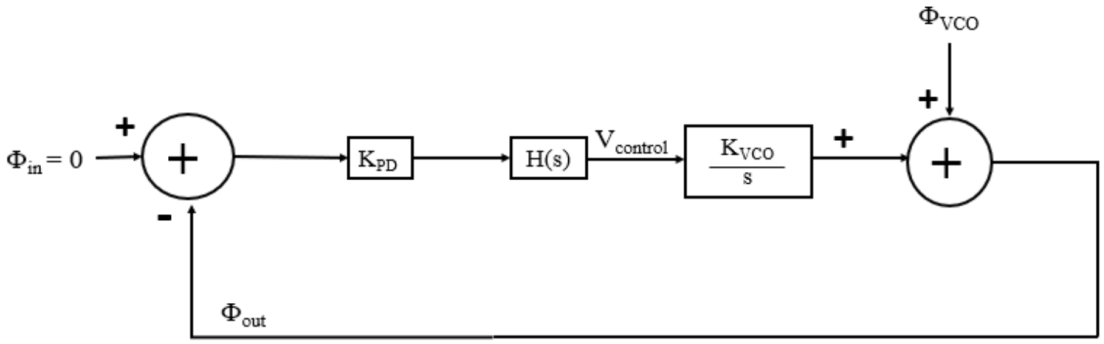

Figure 4.1: VCO Phase Noise Model [10]

$$\frac{\phi_{out}}{\phi_{VCO}} = \frac{s^2}{s^2 + 2s\zeta\omega + \omega^2}$$

The response of ϕ_{out} contains two poles and two zeros at origin exhibiting a high-pass behavior as shown in Figure 4.2. This suggests that the PLL suppresses slow phase variations in the VCO but is unable to compensate for quick variations. The VCO phase is compared to the input phase in lock, and the resulting error is injected into the loop filter to generate a voltage, which is then supplied to the VCO to counteract phase variation. For slow phase fluctuations, the negative feedback remains significant. On the other hand, for quick fluctuations, the loop gain decreases and the feedback gives less correction.

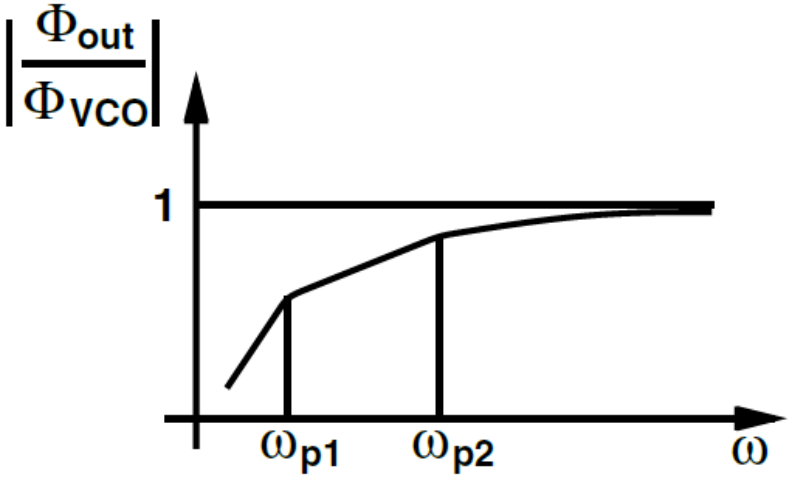

Figure 4.2: High Pass Response Of Phase Noise Due To VCO [10]

Reference Phase Noise The response of phase noise behavior that is caused by the reference input signal is shaped by the input/output transfer function of the PLL as shown by Figure 4.3.

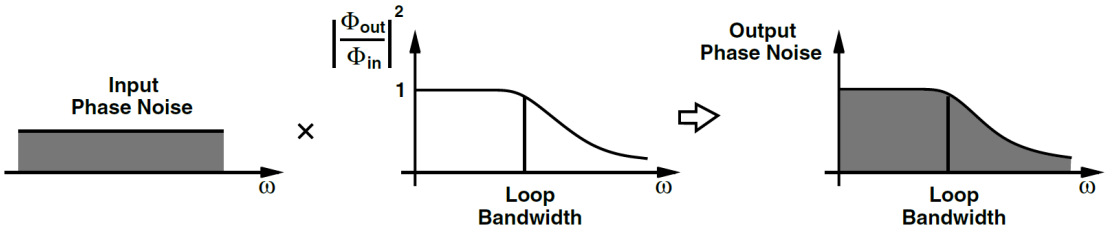

Figure 4.3: Phase Noise Due To Input Reference Signal [10]

Increasing the PLL's loop bandwidth can lead to a greater phase noise at the output, which is contrary to the VCO phase noise behavior. In other words, the loop bandwidth selection involves a trade-off between the reference input signal and VCO phase noise contribution.[2]

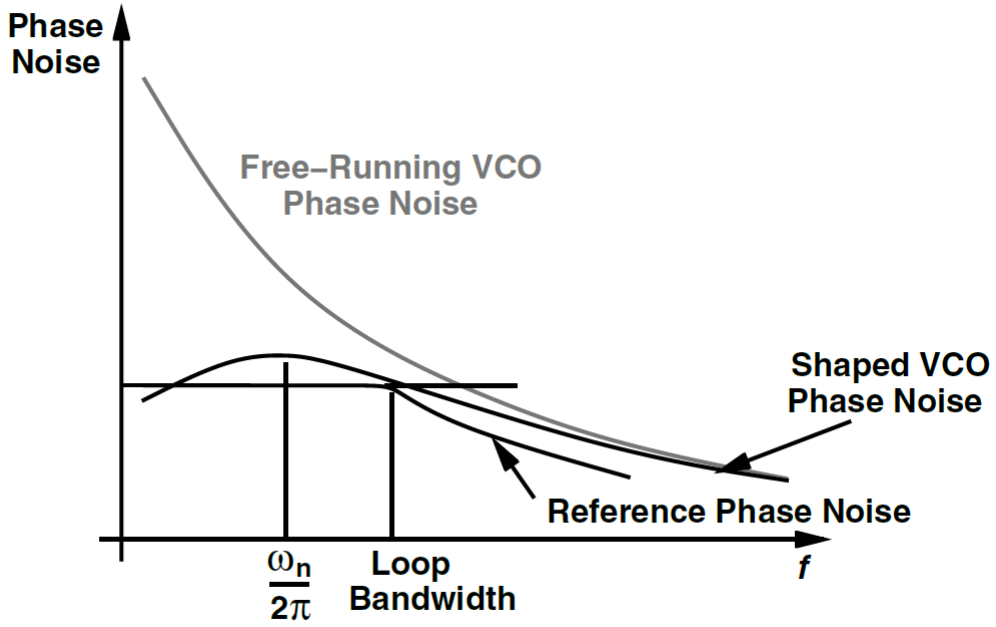

Figure 4.4: Overall Phase Noise Response [10]

To implement the phase noise model, noise from an external source is introduced

onto the control line of the PLL. VCO converts this noise into phase noise whose spectrum is shown in Figure 4.5. The phase noise spectrum of the VCO is as shown in Figure 4.6.

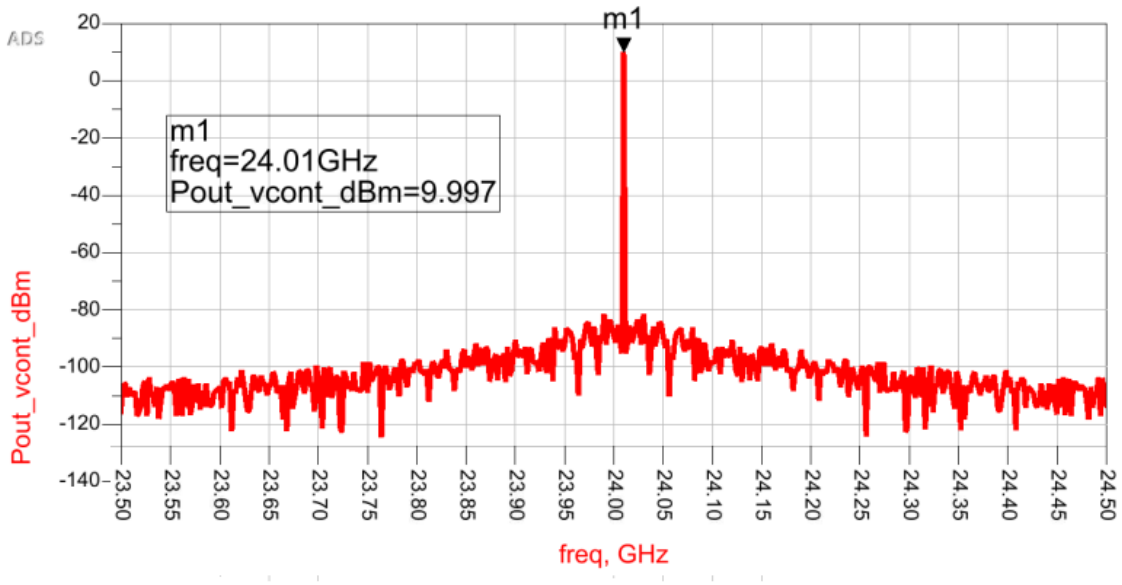

Figure 4.5: PLL Phase Noise Response

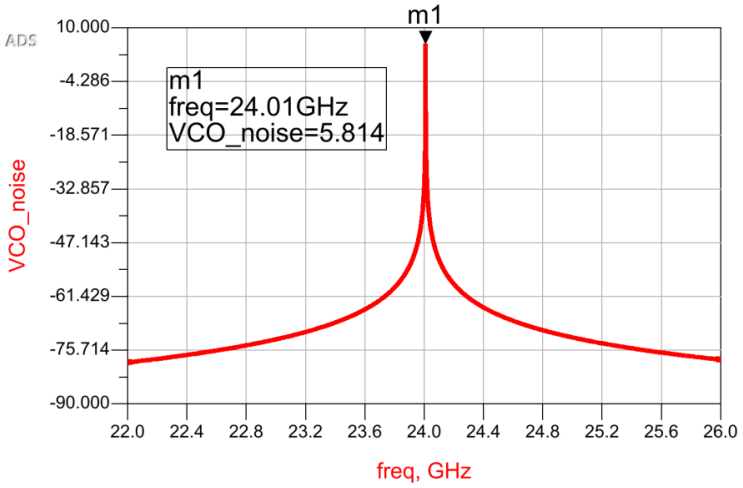

Figure 4.6: VCO Phase Noise Response

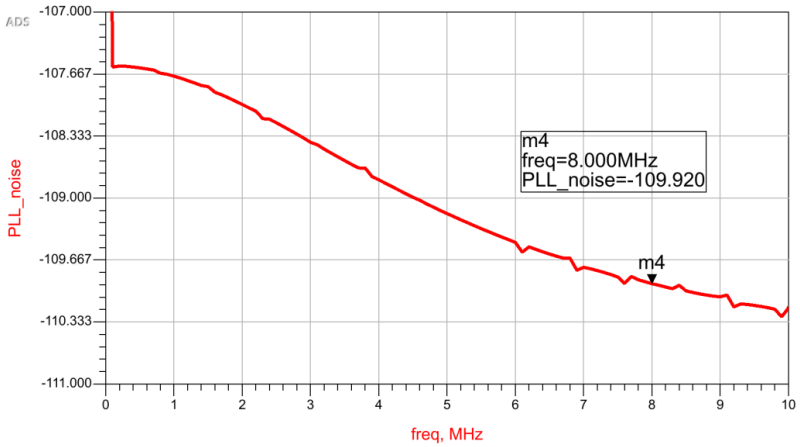

Figure 4.7: PLL Phase Noise Response To Loop Bandwidth

4.2 Spur Analysis

As we discussed earlier, the switching due to a sample and hold will re-calibrate the entire loop making it to stabilize itself. This is observed as undesired spurs on the control line of the VCO. These spurs will have a similar effect as a noise on the control line as shown in Figure 4.8. The power of these spurs is relative to the locking time of the PLL which is basically determined by the loop gain (K_{vco} and H(s)).

4.3 Specification

One can intuitively see that the sample and hold technique that is being used is basically cutting open the PLL loop at periodic intervals. This means that when the VCO is acting as the local oscillator, it will output a phase noise switching between that of a standalone VCO and a locked PLL. Both the phase noise and spur analyses are majorly dependent on the properties of the sync enable signal (period and duty cycle).

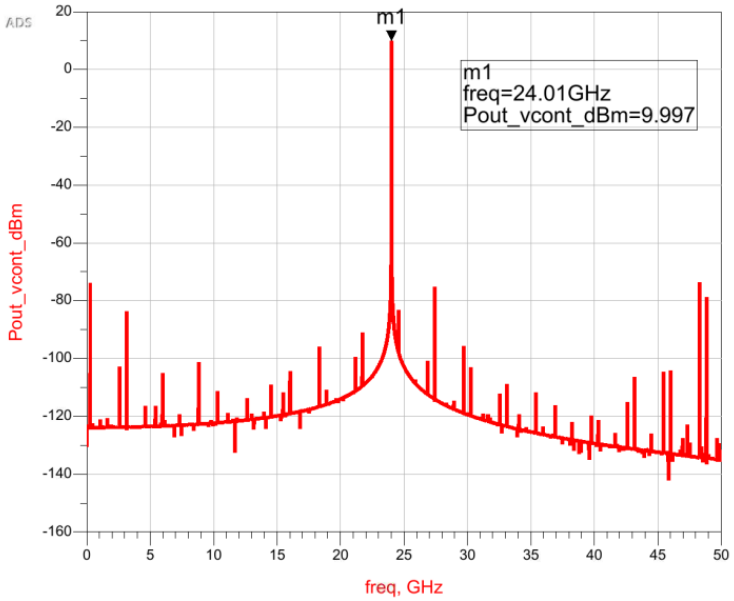

Figure 4.8: Spurs On PLL Output Spectrum At 1MHz Refresh Rate With 0.5 Duty Cycle

4.3.1 Refresh Rate

Refresh rate is the period of the sync enable signal. The Figures 4.9, 4.10 and 4.11 show the effect of the refresh rate on the spurs of the PLL's output spectrum. For all these simulations, the clock's duty cycle has been set to 50 percent. From this analysis, we can observe that higher the clock frequency is (higher refresh rate), higher the noise floor power is observed, consuming the spurs.

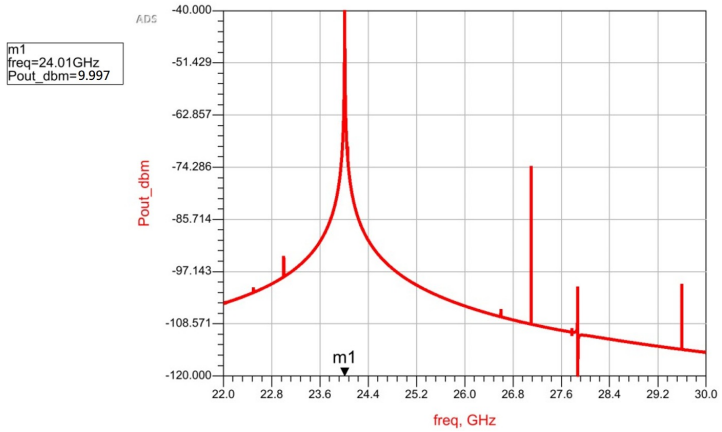

Figure 4.9: PLL Output Response At 10MHz Refresh Rate With 0.5 Duty Cycle

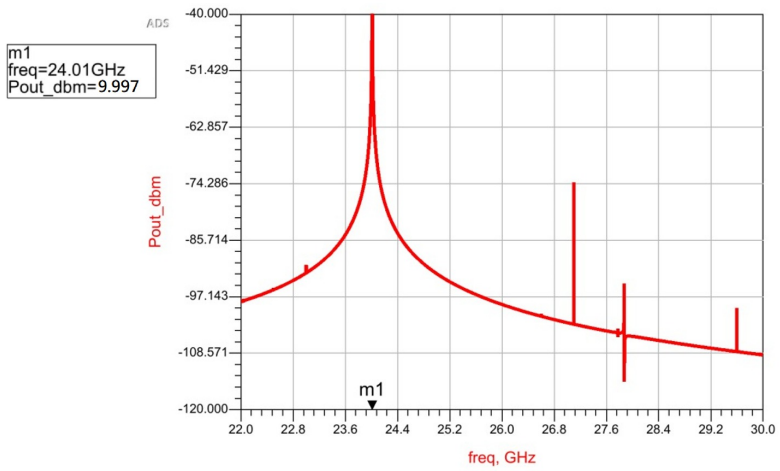

Figure 4.10: PLL Output Response At 50MHz Refresh Rate With 0.5 Duty Cycle

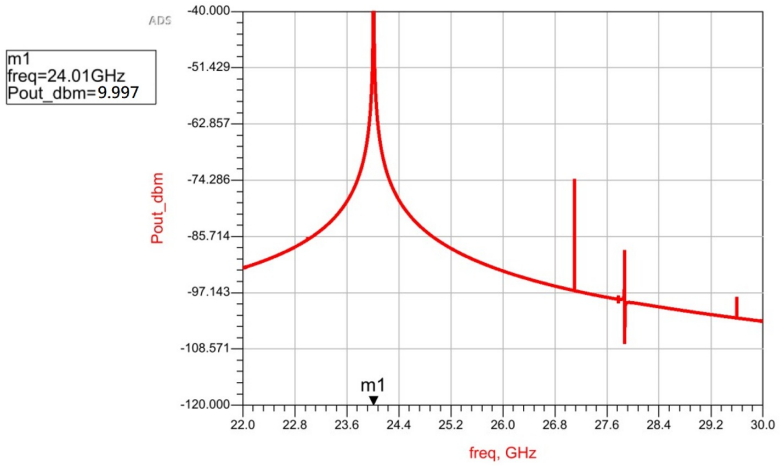

Figure 4.11: PLL Output Response At 100MHz Refresh Rate With 0.5 Duty Cycle

4.3.2 Duty cycle

Duty cycle is defined as the amount of time for which the sync enable signal is switched on for a given time period. The Figures 4.12, 4.13 and 4.14 show the effect of the duty cycle on the phase noise behavior of the switching PLL. For all these simulations, the period has been set to 1MHz for sync enable signal. From this analysis, we can state that the duty cycle has no impact on the overall phase noise performance of the PLL.

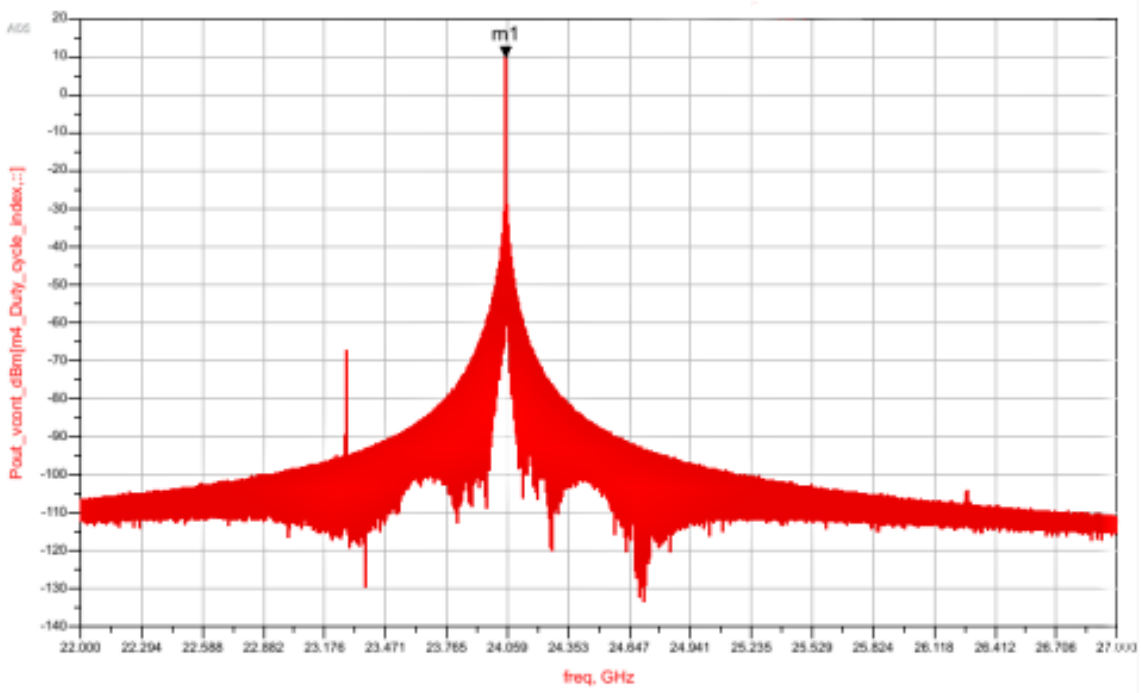

Figure 4.12: PLL Phase Noise Response At Duty Cycle = 0.2 For 1MHz Refresh Rate

From the analyses of spurs and phase noise, we can see that the duty cycle has minimal effect on the phase noise performance of the PLL. Signal quality decreases as the refresh rate increases. Thus, this PLL locks with a lower duty cycle and lower refresh rate without deviating from its performance.Hence the radios in the distributed system can be synchronized using a small fraction of the communication time slot for synchronization allotting the rest of the time for communication.

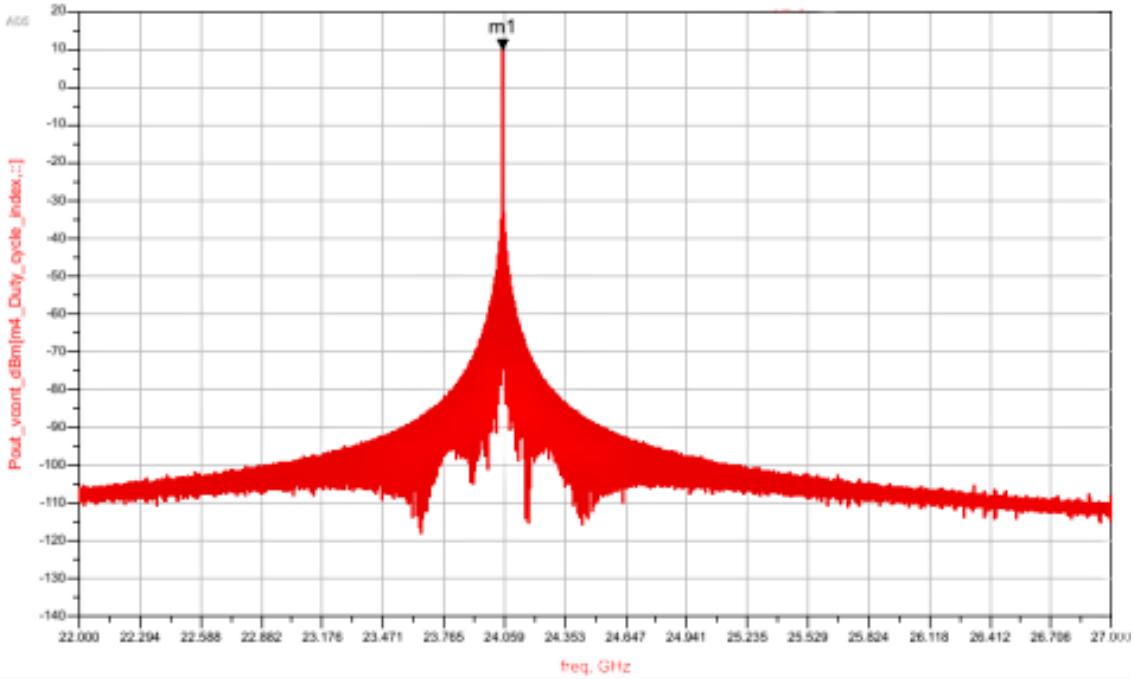

Figure 4.13: PLL Phase Noise Response At Duty Cycle = 0.5 For 1MHz Refresh Rate

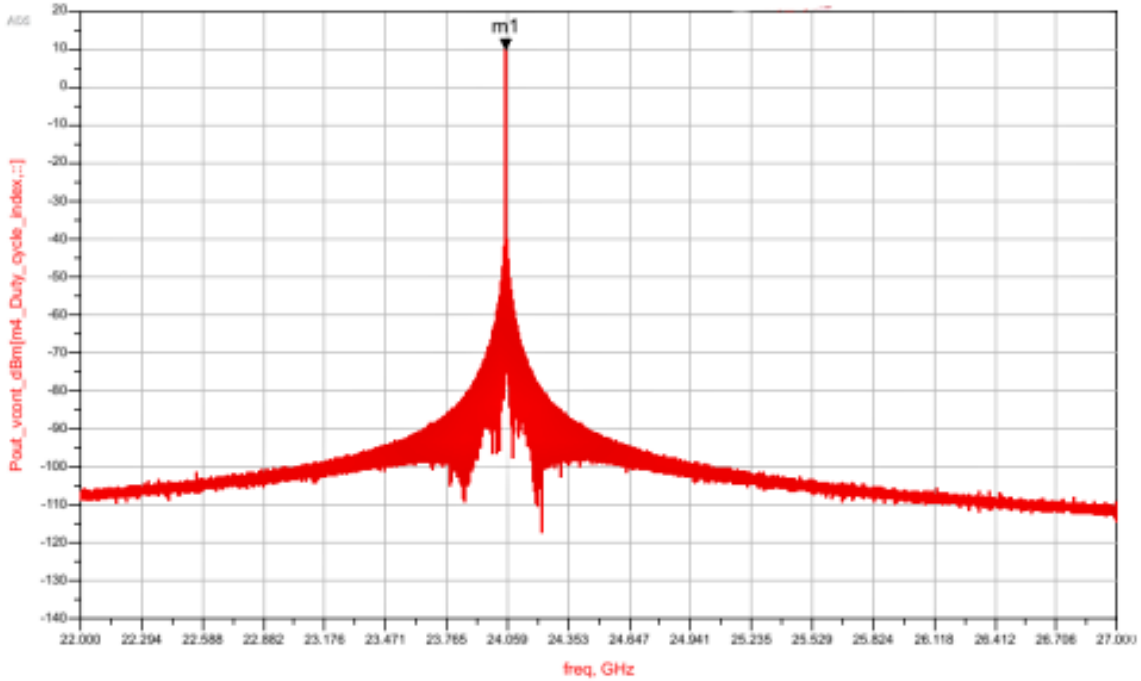

Figure 4.14: PLL Phase Noise Response At Duty Cycle = 0.8 For 1MHz Refresh Rate

Chapter 5

SUMMARY AND FUTURE WORK

5.1 Summary

Advancements in communication technologies demand more innovation. These advancements need more accurate and fast data transmission. For this very reason, wireless transceivers are employed in almost every domain for numerous applications. A special concept of distributed transceivers is proven to be extremely useful in the latest technologies like Internet of Things. This is a collaborative communication technique where the transceivers must be synchronized for faster and much more reliable communication. This is a challenge in design as all the transceivers should be operating in carrier synchronization to maintain the proper collaboration.

In this thesis the carrier synchronization has been established using time division synchronization technique. Several challenges in implementing this technique were addressed using various models simulated in MATLAB Simulink and Keysight ADS. A sample and hold model of the phase locked loop made sure to maintain the sync when the enable signal is off. This fix has its own complexities as it induces spur on the control line of a phase sensitive VCO. An in depth understanding of the impact of this technique on the phase noise of the PLL which acts as a local oscillator has been portrayed in this thesis. A detailed analysis has been performed for all the techniques used for this implementation to provide a diverse perspective. The utility of this technique in real time communication has been discussed with a relatively idealistic model of an example BPSK communication technique.

5.2 Future Work

To further ease up the implementation of this technique, few of the following topics need to be addressed. All the models that are discussed in this thesis were considered in an idealistic environment. In order to understand performance of this technique with noisy components, a noise source has been introduced on the control line of the VCO. The sweep of this noise power versus the phase noise performance of the PLL, shown in Figure , implementing this technique might give us a brief understanding of the noise performance. However, components like the sample and hold will have a separate impact on the PLL performance like altered lock time and spurs. This effect can be minimized by laying off some guard time on the sync enable signal, allowing the control line to settle in between the communication.

We also need to consider that, since the incoming signal and the local oscillator are operating at the same frequency, several effects like spectral leakage and injection pulling come into play, considering that the VCO is basically free running during the demodulation and susceptible to push and pull. To have a broader understanding of these effects it is important to implement this system in a transistor level design. [6]

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