Spin-on Glass and LOR 3A Resist-based Planarization Technique for Neuromorphic CMOS Chips

by

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ABSTRACT

Most hardware today is based on von Neumann architecture separating memory from logic. Valuable processing time is lost in shuttling information back and forth between the two units, a problem called von Neumann bottleneck. As transistors are scaled further down, this bottleneck will make it harder to deliver performance in computing power. Adding to this is the increasing complexity of artificial intelligence logic. Thus, there is a need for a faster and more efficient method of computing. Neuromorphic systems deliver this by emulating the massively parallel and fault-tolerant computing capabilities of the human brain where the action potential is triggered by multiple inputs at once (spatial) or an input that builds up over time (temporal). Highly scalable memristors are key in these systems- they can maintain their internal resistive state based on previous current/voltage values thus mimicking the way the strength of two synapses in the brain can vary. The brain-inspired algorithms are implemented by vector matrix multiplications (VMMs) to provide neuronal outputs. High-density conductive bridging random access memory (CBRAM) crossbar arrays (CBAs) can perform VMMs parallelly with ultra-low energy.

This research explores a simple planarization technique that could be potentially extended to integrate front-end-of-line (FEOL) processing of complementary metal oxide semiconductor (CMOS) circuitry with back-end-of-line (BEOL) processing of CBRAM CBAs for one-transistor one-resistor (1T1R) Neuromorphic CMOS chips where the transistor is part of the CMOS circuitry and the CBRAM forms the resistor. It is a photoresist (PR) and spin-on glass (SOG) based planarization recipe to planarize CBRAM electrode patterns on a silicon substrate. In this research, however, the planarization is only

applied to mechanical grade (MG) silicon wafers without any CMOS layers on them. The planarization achieved was of a very high order (few tens of nanometers). Additionally, the recipe is cost-effective, provides good quality films and simple as only two types of process technologies are involved- lithography and dry etching.

Subsequent processing would involve depositing the CBRAM layers onto the planarized electrodes to form the resistor. Finally, the entire process flow is to be replicated onto wafers with CMOS layers to form the 1T1R circuit.

To my ever-loving parents and late grandparents

ACKNOWLEDGMENTS

I still remember the first conversation I had with my mentor Dr. Hugh Barnaby. After listening to my prior research experience, he said, and I quote 'You are very cocky. I had another student before you who was also very cocky. He was exceptional and later went on to study at MIT. I am going to give you chance. Don't disappoint me'. I will always be very grateful for that one opportunity that helped me set foot in graduate-level research. Since then, he has continued to guide and push me every day to be the best I can be both as a researcher and as a person. I am also very grateful to Dr. Michael Kozicki who recognized my acumen in the field of semiconductor processing and gave someone like me with absolutely no prior experience in the same field to pursue graduate-level research. He is an exceptional teacher with vast knowledge and experience and for the last two years has always provided me with invaluable insights whenever I hit a wall in my research work. I am also thankful to Dr. Yago Gonzalez Velo for providing me with the appropriate research-related resources during the initial days of my research work.

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1 INTRODUCTION

1.1 Motivation

There has been a consistent growth in the number of electronic components on a complementary metal oxide semiconductor chip (CMOS) over the past two decades. And in fact, that number has doubled every two years (Fig. 1.1) as forecasted by Gordon E. Moore, the co-founder of Intel in 1965 [1]. Concurrently, the critical dimension of device-level features continues to shrink by about 13% each year [2]. This in turn has led to increased packing density and complexity of chip design and fabrication. And such a high level of integration and miniaturization requires hundreds of fabrication steps with excellent repeatability and precision. A smooth surface of the processed material layers on topography in each process step becomes imperative especially in lithography otherwise it can result in issues like non-conformal coating of PR, buildup of surface topography as multiple non-conformal layers are stacked upon one another, etc.

For more than 30 years, a technology called Chemical Mechanical Polishing (CMP) has been successfully implemented to achieve ultra-smooth surfaces. CMP is a very powerful fabrication technique that uses chemical oxidation and mechanical abrasion to remove material and achieve very high levels of planarity [3]. But as with any technology, it has some demerits too, which include difficulty of cleaning the wafer, relatively high cost, limited productivity, and unavailability of single-pass system and end-point detection [4]. Among these, the costly nature of the process deters many university-level researchers from employing this technique.

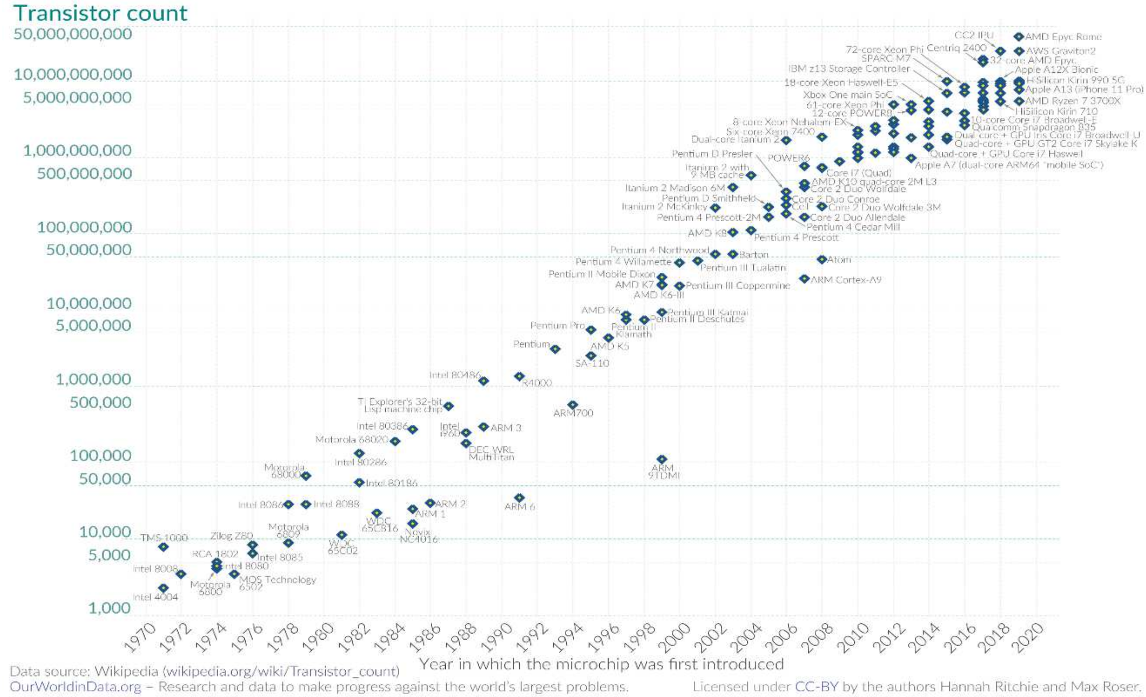

Figure 1.1: A semi-log plot of transistor counts in microprocessors against their dates of introduction. Reprinted with permission from the author Hannah Ritchie (https://ourworldindata.org/technological-progress).

Instead, a more cost and time-efficient solution can be to add simple steps to the full fabrication process. Here, the deposited layers though not perfectly planar are uniform enough such that the topography carried over to the subsequent device layers to be deposited is acceptable. As such, this thesis introduces a SOG and PR-based planarization recipe for hybrid integrated circuits that combine FEOL CMOS with BEOL resistive memory (RRAM) technologies. The RRAM devices are non-volatile programmable

metallization cells (PMCs), also known as CBRAM*. Wafers containing the CMOS circuitry which perform neuromorphic operations are modified by adding CBRAM to the top BEOL layer. To accomplish this, the wafers must be planarized first. After that, the CBRAM will be deposited in a series of steps that require photolithographic masks to pattern the device layers onto the wafers. These masks and the CBRAM deposition techniques will also be discussed in this thesis.

1.2 Thesis outline

This thesis presents a planarization technique that could be extended to combine FEOL processing of CMOS circuitry with BEOL processing of CBRAM for neuromorphic chips. After completion of the final processing of CBRAM layers on the chips, the bio-inspired circuitry is designed to perform VMM on a single-layer perceptron, which is one of the fundamental processing elements in deep neural network (DNN) architectures. This research demonstrates the process on a MG silicon wafer with no CMOS circuitry. The thesis is laid out as follows: - Chapter 2 gives an overview of lithography, one of the two sub-process technologies used in this research while the other technology, dry etching is discussed in Chapter 3. Chapter 3 also discusses different planarization techniques with a focus on SOGs. Chapter 4 discusses PMC technology, the neuromorphic chip layout and the photolithographic mask to be used to process the CBRAM layers. Chapter 5 discusses the fabrication process for planarizing MG silicon substrates with CBRAM electrode

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* CBRAM is a registered trademark of Adesto Technologies Corporation which is now part of Dialog Semiconductor

patterns using SOG and a lift-off resist (LOR). Finally, Chapter 6 summarizes the work and offers the future prospect for this research.

2 LITHOGRAPHY

Lithography in chip fabrication is the process of printing patterns on wafers. The steps involved in a typical lithography process are listed in the flow diagram below (Fig. 2.1). The first step, adhesion promotion, refers to the treatment of wafers before deposition with PR to improve the adhesion between the PR and the wafer. The second step as the name suggests involves coating the wafer with liquid PR uniformly. This is done by dispensing enough PR on the wafer such that at least 80% of the wafer is covered with it and then spinning the wafer at a specific spin speed to spread the resist uniformly over the wafer until the desired PR film thickness is achieved. Variables controlling the film characteristics at this step are spin speed (sets the film thickness), spin time (determines the extent of solvent evaporation from the film), spin speed acceleration (affects film uniformity) and spin chamber exhaust (controls solvent vapor pressure in the spin chamber). To result in solid adhesion of the PR to the wafer, during the third step, a soft bake is performed to densify the film and drive off any remnant solvents. The baking temperature and time and the nature of the bake (constant or ramped) control the extent and rate of solvent evaporation and the stress generated in the film. Lithography is often followed by other processes like etching, ion implantation or another lithography step as part of a multi-layer PR coating process. So, it is imperative that correct alignment (step 4) is ensured with specialized equipment while creating new patterns on top of existing ones. The baked PRs (PRs that undergo chemical reaction when exposed to light) are exposed to light to render positive PRs soluble to chemicals called PR developers and negative PRs insoluble in the same. In step 5, selective exposure is accomplished using sheets of glass covered by opaque materials called photomasks allowing only selective areas of the PR to

be exposed thus creating a pattern when dissolved in the PR developer. While step 6, the post-exposure baking is optional, it is performed to drive additional chemical reactions or diffusion of components within the PR film [5] and is the most common method for reducing the effect of standing waves [6], [7]. The development phase (step 7) involves the removal of the exposed or non-exposed sections of the deposited PR using a PR developer. Inspection of the wafer and measurements, where possible, is performed in step 8 before the last step (step 9) where an optional hard baking subjects the PR to very high temperatures to drive out any volatile components and render the PR photochemically inactive. Therefore, hard baking is always the final step and never executed before the development step.

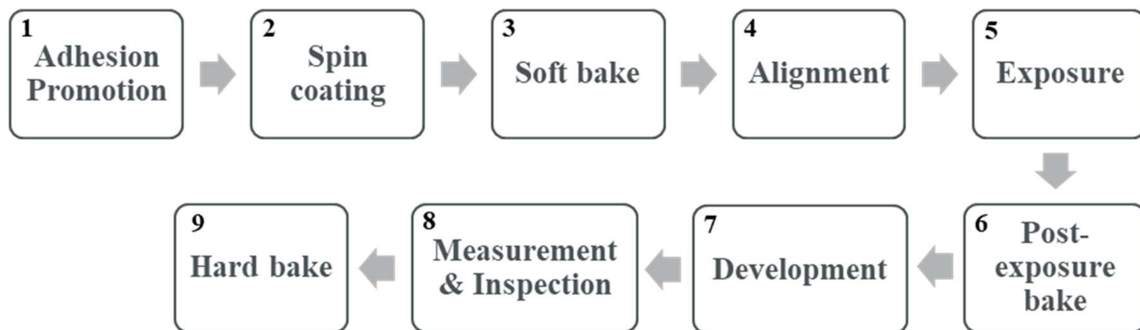


Figure 2.1: Steps in the lithographic process.

2.1 Photoresists (PR)

PRs can be broadly classified into two types based on their response to light, positive tone PRs and negative tone PRs. Positive PRs become soluble in developer chemicals after exposure to light of the right wavelength. This means a layer of positive PR on a wafer will leave behind patterns for the sections of the PR that have not been exposed to light. On the

other hand, negative PRs become insoluble to developers in presence of light and thus leave behind patterns on the wafer for the regions that have been exposed to light.

A typical PR comprises of four basic components: the polymer or binder polymerizes, forms crosslinks or photo-solubilizes upon exposure to light [8] thereby changing the photochemical nature of the entire PR. The solvent keeps the PR in a liquid form allowing it to be spun onto a substrate and also determines its viscosity; Photosensitizers are used to control or cause polymer reactions resulting in photo-solubilization or crosslinking of the polymer [8], modify the wavelength range of light to which the PR responds and also the fraction of photons needed to cause the photochemical reaction also termed as PR quantum efficiency and finally, additives are introduced as required by the specific application, for example, to increase photon absorption or to control light within the PR film [8].

2.2 Lift-off process and resist

A lift-off process involves exposing and developing a stencil layer to form an inverse image of the desired pattern and then depositing the layer to be patterned over this stencil layer. In this way, the layer gets deposited directly over the wafer in the locations where the pattern ought to exist while the same gets deposited on top of the stencil film in locations where it undesirable. Finally, the wafer is immersed in a chemical to dissolve away the stencil film and the material layer deposited on top of it gets 'lifted-off' leaving behind the material layer in areas where it is in direct contact with the wafer. For a successful lift-off it is key to ensure that there exists a distinct break between the deposited material layer on top of the stencil and the same on the wafer. This is so that the dissolving chemical can reach the underlying stencil layer and etch it.

There are a variety of ways of performing a lift-off: - single layer PR processing, for example, using a single positive PR mask layer but this suffers from the presence of graded side-walls that get coated with the material layer to be patterned and thus preventing the dissolver from reaching the PR. Using a negative PR instead gives retrograde side-walls and requires fewer process steps [9], [10], [11]; bi-layer techniques that use a combination of a PR and LOR [9], [12], aluminum [9] or polymethyl methacrylate (PMMA) [13] where the former is deposited on top of the latter allowing as much undercut in the latter layer as desired. This allows the developer to easily reach the PR from underneath and provides a clean lift-off; tri-level/ four-level layer techniques, for example, a four-layer stack of aluminum, a thick PR, an intermediate layer like tungsten and finally, another thin PR layer [9], [14], [15]; (4) surface modified resist processing [16], [17] involves soaking the wafer in chlorobenzene or toluene so that the top surface of the PR layer develops slowly as compared to the PR in the bulk of the layer thus producing a hook structure with an undercut profile.

LORs also called polydimethylglutarimide (PMGI) resists are a line of resists developed by Kayaku Advanced Chemicals for lift-off applications. LOR layers have superior planarizing properties [17], [12] and show excellent top surface uniformity thus making them a very cost-effective solution to planarization related applications. Additionally, they have very high thermal stability [12] making them appropriate to be used in conjunction with SOG as the latter requires high baking temperatures. LORs are also optically transparent materials [12]. This is desirable as the processing of subsequent CBRAM layers requires the patterns underneath the planarizing layers to be visible for

correct alignment during the exposure step. Besides, LORs can give film thicknesses as low as below 20 nm meaning that many layers can be stacked on top of one another thereby imparting exceptional uniformity to the top surface of the stack.

2.3 Multi-layer resist systems

Strictly speaking, any wafer with more than two layers of different stacked materials is a multi-layer (MLR) system. However, MLR systems commonly refer to a different approach. The first or the bottommost layer on the wafer is made thick enough to planarize the entire topography on the wafer while the subsequent second or third layers (depending on whether it is a bi-layer or tri-layer process) on top of the first layer are made much thinner. The same approach is used in this research where the thick bottommost layer is the LOR capped off by a thin SOG layer. Any subsequent layers deposited on this MLR system must have a different chemistry than that of the topmost layer of the MLR system to prevent issues at their interface, for example, the solvent of the former material dissolving any of the other planarizing layers.

3 MATERIAL LAYER PLANARIZATION

Planarization in the context of semiconductor processing is the process of increasing the flatness or planarity of the surface of a semiconductor wafer through various methods known as planarization techniques [18]. The starting wafer is blank and ideally planar. However, layers of various materials, shapes and depths are deposited over the wafer as it moves through various processing steps during device fabrication. Additionally, portions of these deposited materials are removed from the wafer either locally or globally through subtractive process steps leading to the formation of patterns with differing geometries. So, as layers keep stacking up the overall planarity of the wafer surface worsens as the residual roughness from the previous layers gets compounded. Two very generic issues that arise from such a scenario are ensuring the planarization layer provides ample step coverage and this becomes even more difficult as the aspect ratio between various patterned layers increase and ensuring that the planarization is good enough to provide a higher depth of focus that is better for the imaging of finer features on the wafer.

There can be two kinds of planarization depending on the area of coverage. Local planarization refers to smoothening techniques over short distances and global planarization refers to techniques that smoothen topography over long-range distances. Local planarization is illustrated in the fourth subfigure in Fig. 3.1 where the planarizing layer completely planarizes the three stacks (local topography) but slopes down with an angle θ beyond that and thus any patterns beyond the three stacks remain unplanarized. The degree of planarization refers to the extent a deposited layer can planarize the existing topography and is measured as Eq. 3.1. Fig. 3.1 shows the difference between a completely

non-planarized layer and a perfectly planarized layer. In reality, the outcome is neither as perfect as shown in either the first or fifth subfigures of Fig. 3.1 but rather closer to the second or third subfigure.

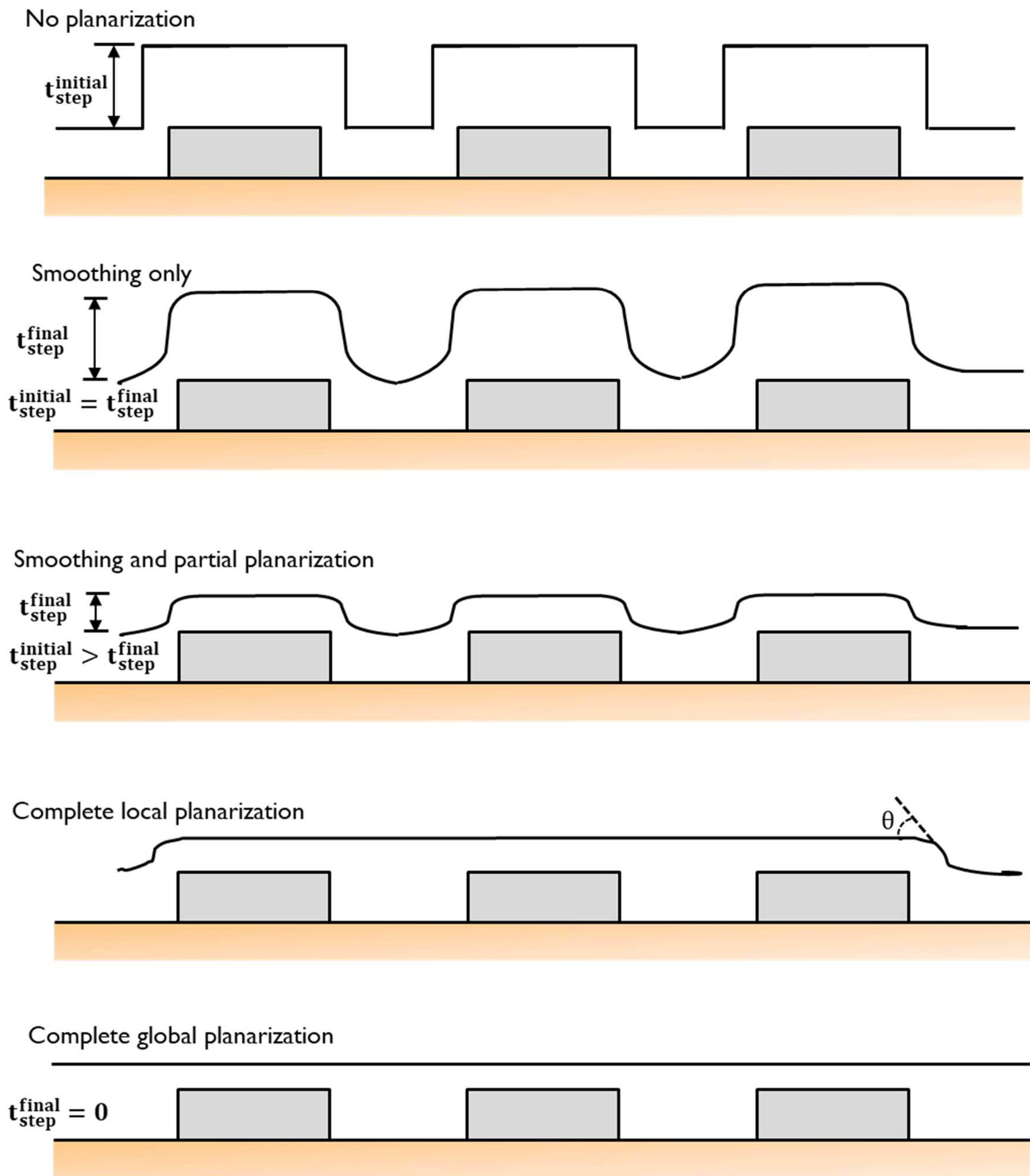


Figure 3.1: Degree of Planarization

$$Degree\ of\ Planarization = 1 - \frac{t_{step}^{initial}}{t_{step}^{final}} \qquad 3.1$$

where

$t_{step}^{initial}$ = step height difference of the topography being planarized.

t_{step}^{final} = step height difference after depositing the planarizing layer.

3.1 Planarization techniques

Planarization techniques include plasma etching and ion milling, ion implantation, reflow of SiO_2 doped with phosphorus or boron glass, reflow of metal, smoothening deposited films by re-sputtering them, chemical mechanical planarization (CMP), spin-on materials (glasses, resists, polymides, resins, low viscosity liquid epoxies, etc.).

Plasma etching refers to the use of a stream of high-speed glow discharge (plasma) of an appropriate gas mixture to bombard the surface of a sample. This plasma source serves as the etch species and is composed of both charged particles (ions) and neutral particles (atoms and radicals). The ions being reactive in nature impart the chemical etching effect, i.e., combining with surface molecules, converting them into the gas phase to be pumped away via the vacuum system. The atoms and radicals accelerated by the electronic potential physically bombard the layer surface at high energy and sputter or knock surface atoms off into the gas phase. The latter process is also called ion milling. Since the composition of the plasma is uniform throughout the etch chamber, the etch rate is also uniform in a specific direction. Additionally, the etching process can either be isotropic where material is etched from all directions or anisotropic where the etching is prominent in only one

direction. Before being replaced by CMP, plasma etch-back was quite typical for planarization applications. It was primarily being used as a standalone technique but in more recent sub-micron applications, it is used in combination with CMP [19]. CMP processes despite providing high throughput can leave non-uniformities and surface damage. This necessitates the use of plasma etching as a post-CMP topography refinement technique. Contrastingly, pure ion milling is more commonly used for polishing surfaces [19], [20] [21], [22] as the process can be better controlled through the ion beam angle and the ion energy.

Ion-implantation refers to the technique of injecting energetic ions into the surface of a target material layer to modify its near-surface chemical characteristics or its defect state. In the semiconductor industry, the most common application of ion implantation is doping material layers with electrically active ions although some literature also explains its potential in planarization applications. The process in the latter involves some way of modifying the ion-implanted layer to impart planarization to the system [23], [24]. For example, the depth of penetration of the energetic ions can be controlled so the resulting boundary separating the doped layer from the undoped layer is very planar. This means that the top surface of the layer left behind after removing this doped layer is also very planar [23]. (2) The other way does not involve removal of the doped layer but rather simply alters its chemical properties such that the resulting top layer is planar [24].

Silicon dioxide (SiO_2) doped with phosphorus called phosphosilicate (PSG) or boron called borosilicate glass (BSG) or a combination of both called borophosphosilicate glass (BPSG) have been used extensively for shallow trench isolation, inter-metal dielectric

isolation, spacer isolation, device passivation, etc. [25]. The planarization process typically involves depositing the glass using a variety of chemical compound combinations and Chemical Vapor Deposition (CVD) methods followed by subjecting the glass to its transition temperature (800°C-1100°C) such that the deposited glass reflows over the pattern to planarize it. The driving force behind reflow is a reduction in surface energy [26]. But such high transition temperatures can also cause increased lateral or vertical dopant diffusion, shifting of p-n junctions in device layers and degradation of silicide junctions. Other disadvantages include cusping (the deposited glass forms kinks across steps in the patterns) and void formation in the glass layer. Note that there is also a spin-on variety of silicate glasses that utilizes lithography for depositing the planarizing layer instead of CVD. More on this will be provided when SOG planarization is discussed later in this thesis.

Instead of depositing a secondary material over interconnect layers and then reflowing it, the interconnect metal itself can be reflowed to fill gaps, voids and create a more even top metal layer. For example, a wafer heated at 450°C-550°C can help in reflow of aluminum contact layers and vias. A reflow technique for copper can be found in [26].

Resputtering also called bias sputtering is the technique of applying a small negative potential to the substrate to continuously resputter some of the material being deposited. In a typical sputtering process, the sputtered material is deposited uniformly thus translating any topography on the target layer to the sputter-deposited layer. But this pattern translation can be avoided by continuously bombarding the deposited layer with ions to eject it while

being deposited such that the final layer is conformal. This technique has found applications in planarizing insulating layers [27], [28], [29] and metals [30].

CMP involves chemical reactions on the top uneven surface of a deposited layer followed by its removal mechanically to planarize the layer. The wafer is pressed face down against a rotating polishing pad with a slurry containing abrasive particles and chemical additives. The mechanical action is the controlling of torque and pressure while allowing the wafer to graze against the slurry on the pad whereas the chemical counterpart is the reaction between chemical reagents in the slurry and the film on the wafer thereby modifying the wafer surface to enhance its removal. CMP is a very popular technique, but expensive technique, which has been the subject of many publications [31], [32], [33], [34].

Spin-on materials typically refer to materials used for planarizing substrate topography through lithography. Typically, the process involves spinning the planarizing liquid onto the wafer to the desired thickness followed by baking/curing to evaporate the solvent in the spun film thereby hardening it and finally etching or polishing it to impart further planarity. The use of lithography-based planarization techniques is used extensively in the semiconductor industry as it is easier to control and implement and also cost-effective. Thus, there is an ample amount of good literature with comprehensive information on planarization using polyimides and resists [35], [36], resins [37] and low viscosity materials [37].

3.2 SOGs

Sol-gel based planarization technology uses sol-gel solutions containing the desired oxide or non-oxide precursor to planarize substrate topography by dipping, spinning,

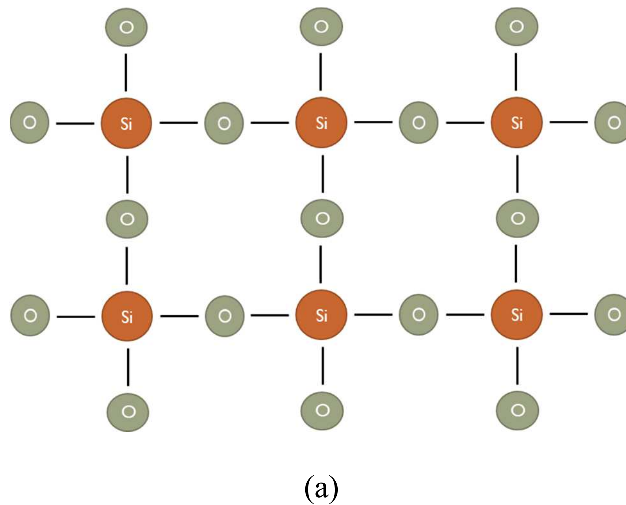
draining, or spraying. SOGs are just sol-gel solutions comprised of Si-O network polymers in organic solvents to deposit SiO_2 films on wafers. SOGs can be divided into three types based on their chemical composition as silicate SOGs, organosilicon compounds or siloxane SOGs and doped organic SOGs. This section will only talk about the chemical composition of each of the SOG types. SOG planarization techniques will be explained along with the process flow in the next section.

3.2.1 Silicates

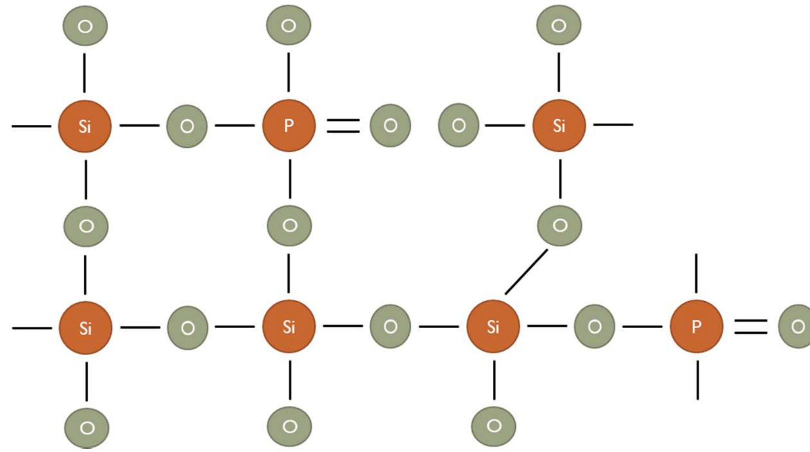
These SOGs are created from a condensation reaction of $Si(OH)_4$ by losing water and they lose the hydroxyl group (-OH) when cured/hard-baked to form strong Si-O bonds. A rough description of the molecular structure for an undoped and doped silicate SOG is shown in Fig. 3.2. But this also creates significant tensile stress and may even crack the film. A very good way to solve this cracking issue is to ramp bake the spun film instead of subjecting it to a constant high temperature. Ramp baking involves baking the film by slowly ramping up the temperature continuously or in steps until the target baking temperature is reached followed by ramping down the temperature in a similar fashion until the temperature is low enough to keep the film stable. After spinning and baking, silicates condense but remain thermally stable and do not react with plasma or moisture. But, if aluminum interconnects are used then the maximum curing temperature of spin-on dielectrics cannot exceed 450°C. This is too low to condense the film and it may contain significant amounts of silanol (≡Si-OH) and absorbed moisture thus degrading the dielectric quality. But this issue can be alleviated by choosing other metal types such that the curing can be performed at temperatures ≥800°C. Also, the silicates have low viscosity

and poor planarity compared to the other types of SOG. This means that silicate films are thin and require multiple coats to achieve the desired thickness and planarization.

Silicate SOGs can also be used as diffusion sources and are also spin-on dopants (SODs). An example of a phosphorus-doped silicate SOD is given in Fig. 3.2(b). The dopant atom modifies the Si-O network in the baked film thereby reducing the film stress and reducing the chances of cracking. But, if the dopant concentration exceeds a certain limit (varies depending on the type of dopant), the film becomes hygroscopic in nature, i.e., the film surface adsorbs water molecules. In case of boron-doped SODs, B_2O_3 reacts with adsorbed water at room temperature to form boric acids as shown in equations 3.2 and 3.3. Since HBO_2 and $H_3 BO_3$ are volatile compounds, boron present in boric acids is lost and will not contribute to silicon doping.



(a)



(b)

Figure 3.2: Molecular structures (after curing) of (a) Undoped silicate SOG and (b) phosphorus-doped silicate SOG.

$$B_2O_3 + H_2O \Longrightarrow 2\ HBO_2 \qquad 3.2$$

$$B_2O_3 + 3\ H_2O \Longrightarrow 2\ H_3BO_3 \qquad 3.3$$

Boron-doped SODs suffer from boron skin formation in addition to the moisture adsorption effect. When the silicon substrate with the B_2O_3 is subjected to diffusion temperatures, the boron diffuses into bulk silicon leaving behind a SiO_2 film on the surface-

$$2\ B_2O_3 + Si \Leftrightarrow 3\ SiO_2 + 4\ B \qquad 3.4$$

The concentration of boron at the surface of the silicon substrate is at its solid solubility limit allowed by the temperature at which diffusion is occurring. But the excessive amount of B_2O_3 at the wafer surface can also lead to the formation of SiB_x species which is called boron skin. This skin can be several hundred angstroms thick and is difficult to remove chemically.

3.2.2 Organosilicon compounds or Siloxanes

As the name suggests, these are SOGs doped with organic compounds like -CH_3, -C_2H_5, etc. as shown in Fig. 3.3. Similar to phosphorus or boron-doped SODs, these organic groups modify the Si-O network lowering film stress and thereby improving crack resistance and film planarity. These are heavier and more viscous than silicates and give thicker films at the same spin speed. Despite these advantages, siloxanes suffer from several issues that limit their usage. The organic group in siloxanes undergoes thermal decomposition even at low curing temperatures particularly in presence of oxygen plasma. The Si-R and Si-OR ('R' represents the organic group) bonds break to form Si-OH bonds and this -OH content increases the dielectric constant thereby degrading the device performance in addition to creating reliability issues. Since exposure to oxygen plasma is unavoidable in multi-step processing, siloxanes are commonly used as temporary planarizing materials to be removed by etching in subsequent process steps. Siloxane films also adsorb atmospheric water and have low mechanical strength.

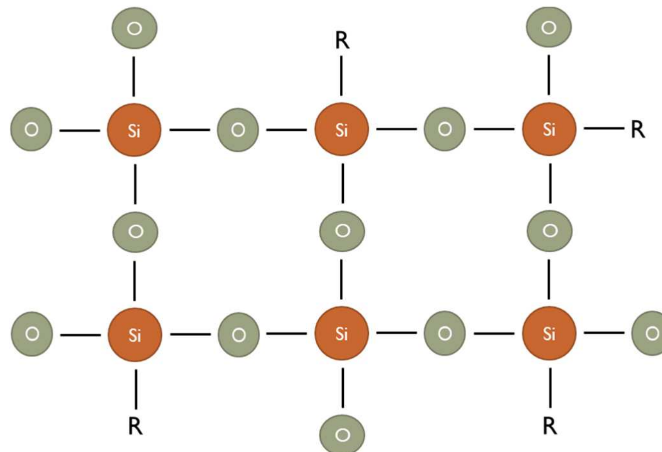


Figure 3.3: Molecular structure of Siloxane SOG

3.2.3 Dopant organic SOG

These SOGs are an amalgamation of silicate SODs and organic siloxanes. They have the advantages of SODs and siloxanes such as low stress, uniformity and low viscosity, while at the same time being resistant to moisture adsorption and non-volatile. Additionally, these SOGs have higher shelf life (more than a year at room temperature). This SOG is based on a boron-nitrogen backbone polymer dissolved in toluene synthesized from a class of boron nitrogen compounds called borazole (or borazine) [38]. Upon curing, these borazole polymers decompose into boron-nitrogen-hydrogen moieties which then react with oxygen from the organic groups and adsorbed water or oxygen from the furnace ambient to form B_2O_3. This then reacts with silicon in a similar fashion as described by equation 3.4 to diffuse boron in bulk silicon.

4 PMCs and Neuromorphic Chip Layout

4.1 PMC Technology

The PMC technology encompasses the family of devices that leverage electrochemical reduction of an active metal between two electrodes [39]. Put simply, a PMC is an electrochemical cell that consists of three material layers: - an active anode that serves as a source of metal ions, an inert cathode and a solid electrolyte layer doped with metal sandwiched between the two electrodes. Typically, when a potential is applied across the cell, the active metal anode oxidizes to supply metal cations that 'dissolve' into the solid electrolyte. These cations then travel through the electrolyte along the potential gradient, get reduced at the cathode and form a metallic electrodeposit on the inert cathode. Further application of forward bias will allow the electrodeposit to grow finally forming a filament connecting the two electrodes. Conversely, the electrodeposit can be dissolved back into the electrolyte by applying a reverse bias. Depending on its geometry, a PMC can be vertical, lateral or radial.

The vertical PMC due to its application as a non-volatile memory device is also called CBRAM and has potential to replace the current NAND Flash memory because of its low power, non-volatile and fast switching properties. CBRAM is a type of RRAM where the memory state changes with the resistance of the electrochemical cell upon application of electronic potential. Fig. 4.1 shows the CBRAM structure and the formation of filament that switches the device state from high resistance to low resistance. The electrolyte is doped with the anode metal ions to assist in the formation of the filament. If after formation of the filament, the potential is turned off, the filament does not dissolve. This means that

information is not lost upon turning off the power thus granting CBRAM its non-volatile nature.

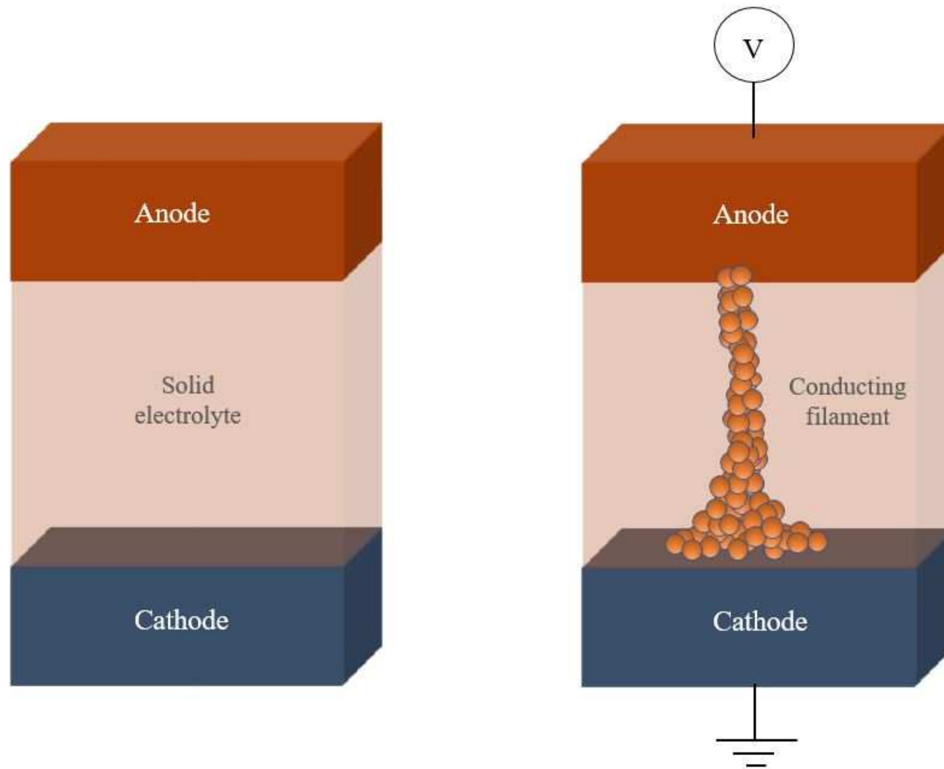


Figure 4.1: Vertical PMC in (a) high resistance and (b) low resistance states [40].

Unlike vertical PMCs where the electrolyte is sandwiched between the electrodes, lateral PMCs have both the electrodes on top of the electrolyte as shown in Fig. 4.2. In a lateral PMC, the distance between the electrodes is much larger than a vertical device (microns compared to nanometers), thus the electric field is smaller between anode and cathode. The filament is also thicker and can grow either on the surface or in the bulk of the electrolyte. The operating principles remain the same however. Lateral PMCs find applications as radio frequency (RF) switches, timers and microfluidic valves.

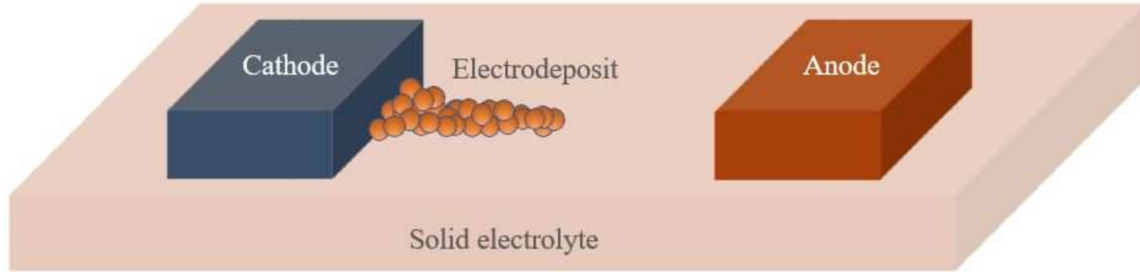


Figure 4.2: Lateral PMC structure [40].

The only similarity between radial PMCs and the other PMC types is that they operate on the same principle of growing a metallic electrodeposit. Radial PMCs are planar with a circular anode, a point cathode at the center and the solid electrolyte encompassing the area between the electrodes as shown in Fig. 4.3. Since the anode is circular, the electric field converges from all directions to the point cathode, unlike in the other PMC types where it is always unidirectional. This means that the electrodeposit has an equal probability to grow randomly in any direction. This randomness enables their application as physical unclonable functions (PUFs) [41].

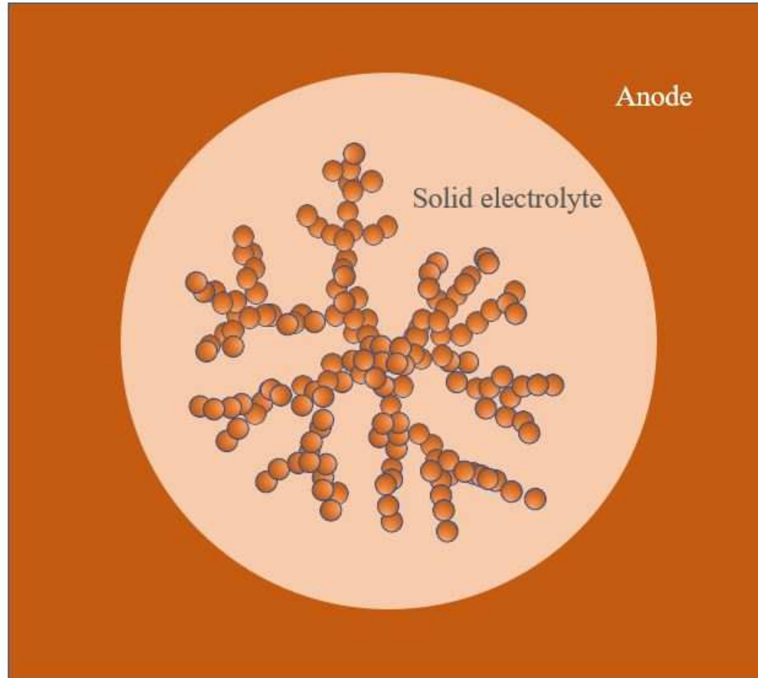


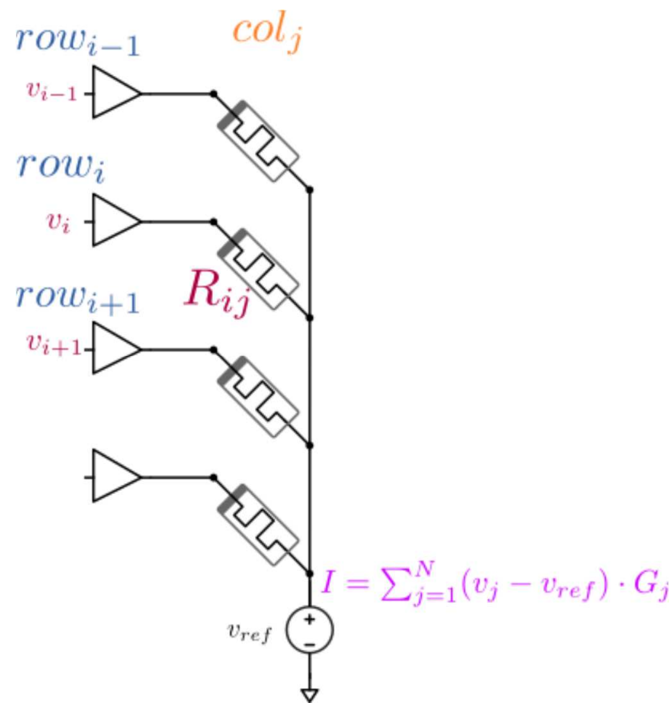
Figure 4.3: Radial PMC structure [40].

4.2 Neuromorphic Circuits

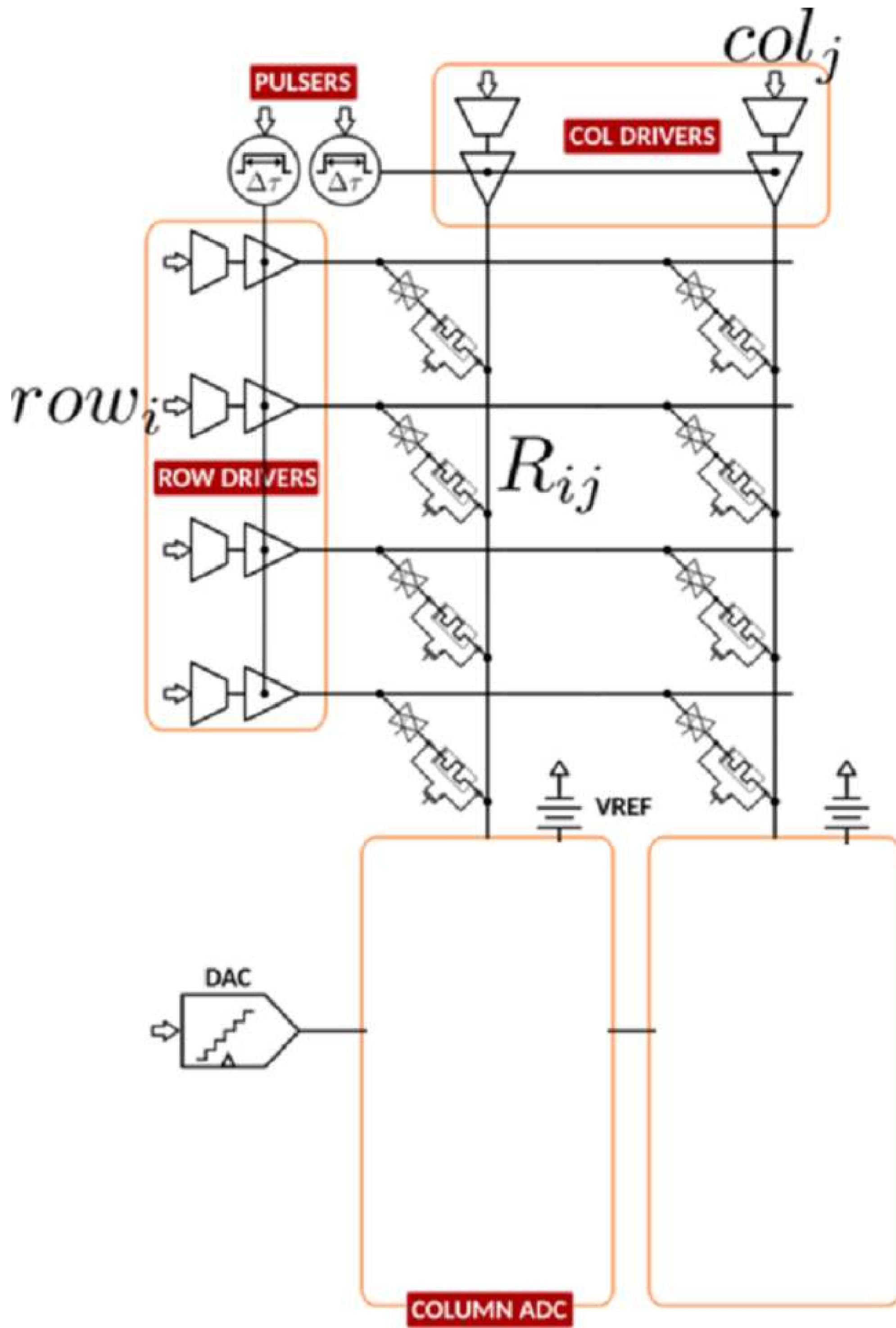
Of all the various types of neuromorphic circuits, the architecture that this thesis considers is a CMOS-based perceptron that performs a VMM operation by implementing a controlled pulsed write into and digital readout of an 8x7 integrated nonvolatile RRAM array. The VMM column read operations sum the currents created from input voltages impressed across a set of RRAM cells sharing a common lead as shown in Fig. 4.4 (a). The dot product sums are converted to a 10-bit digital word using an on-chip analog-to-digital converter (ADC). Each row or column in the array can be individually addressed and isolated to either be included or excluded for any given read or write operation. Also, on-chip is a variable width pulse generator used to control the width pulses that alter the array's RRAM conductance during write operations. The arrangement is depicted in Fig. 4.4.

Configuration of the control bits for array addressing, transimpedance gain, and test modes are all done through a simple shift-register chain which is part of the ADC circuitry.

The embedded RRAM array is divided into 8 columns. A VMM operation is just 8 dot product operations performed in parallel. Every row or column in the array has 2 mode bits that control how it is hooked up to the shared row and column drivers. This flexibility allows for subsets of the array to be targeted for a set of operations while floating or "idling" the other ones. The 8th column is populated with fixed poly resistors instead of RRAM devices and serves as a test column to evaluate the rest of the readout circuitry. This means there are only 8 rows and 7 columns of RRAM devices.



(a)



(b)

Figure 4.4: (a) dot product in a VMM operation and (b) on-chip VMM arrangement.

The RRAM in the 8x7 device array is a vertical PMC or CBRAM. Its structure consists of 3 layers (Ag/Ag-$GeSe_3$/Ti)- a silver (Ag) anode, a germanium selenide chalcogenide doped with silver (Ag-$GeSe_3$) as electrolyte and a titanium (Ti) cathode. The electrodes are to be deposited in an 8x7 array of BEOL metal stacks. And each unit in this 8x7 electrode stack consists of top-level metal electrodes: - a top electrode (TE) acting as the anode contact and the bottom electrode (BE) acting as the cathode contact for the RRAM cell. In ascending order, the top-level metal stacks are composed of a 15 nm thick titanium layer, a 25 nm thick titanium nitride (TiN) layer, a 675 nm thick aluminum-copper alloy which is capped off by a final 25 nm thick layer of TiN acting as an anti-reflective coating (ARC) as shown in Fig. 4.5. Thus, the electrodes are Ti/TiN/Al-5Cu/TiN ARC stacks where the bottommost Ti layer is an inert electrode material, Al-5Cu is an alloy of aluminum (Al) with 5% copper (Cu) by weight and the TiN ARC prevents reflection of light from the underlying highly reflective metal layers during photolithography. Each stack is 740 nm thick and has the same composition of materials that is Ti/TiN/Al-5Cu/TiN ARC. The TE and the BE have different shapes as seen in Fig. 4.6. The TE and BE stacks are 2 μm apart from each other and the BE of one array column is 23.75 μm from the nearby metal routing which in turn is 68.6 μm away from the TE of the subsequent array column of electrode stacks.

In Fig. 4.5, the blue-colored Ag layer forms the active anode and the pink-colored Ag doped $GeSe_3$ layer forms the electrolyte. Note that the BE never touches the Ag anode layer to prevent short-circuit. There is a need to planarize the stacks to avoid the deposited CBRAM layers from falling off from the edges of the TE and BE stacks. This is achieved

using a combination of SOG named NDG 7000R by Desert Silicon, Inc. and LOR 3A by Kayaku Advanced Materials, Inc. Ideally just the SOG would have sufficed as a planarizer but due to two limitations the LOR 3A had to be used in conjunction with the SOG. Firstly, the SOG needs to be spun at a spin speed <2000RPM to avoid severe non-uniformities in the top layer of SOG thus limiting the maximum possible height per SOG layer. Secondly, no more than 2 layers of SOG can be stacked on top of each other as the baking process for the third layer cracks the SOG layers underneath. Consequently, according to the film thickness versus spin speed curve in [42] and taking into account film shrinkage after curing, the total thickness of the dual layer SOG spun at 2000 RPM is limited to about 1100 nm. This is nowhere near enough to planarize 740 nm of topography. Thus, the LOR 3A resist, being an excellent planarizer can be stacked up to several thousands of nm in thickness without cracking. So, it is used as a buffer between the SOG and the wafer to allow for a taller planarization layer.

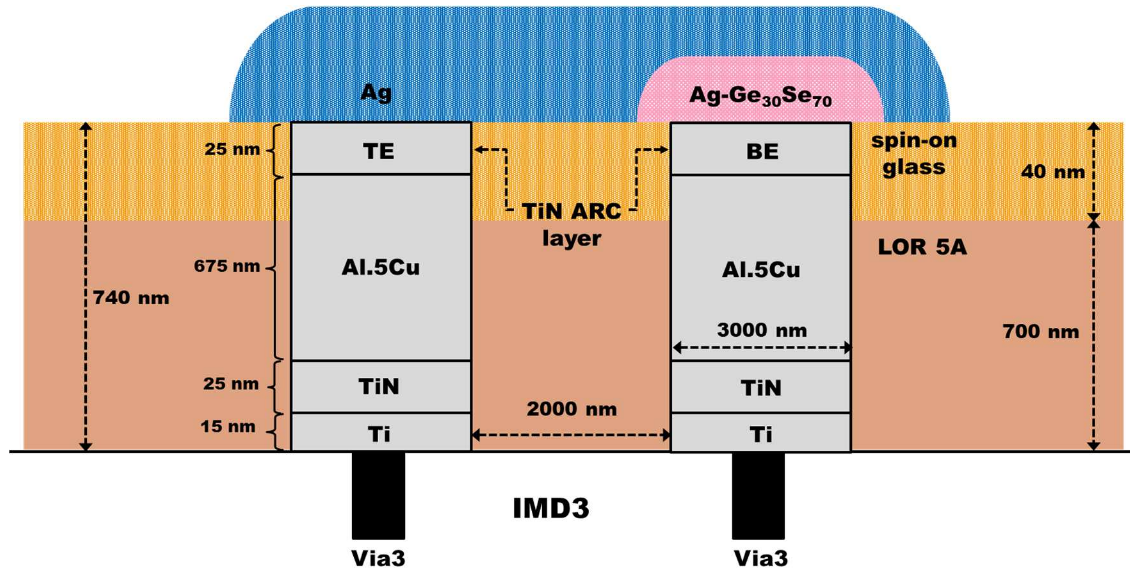


Figure 4.5: Cross-section of one CBRAM and its electrodes.

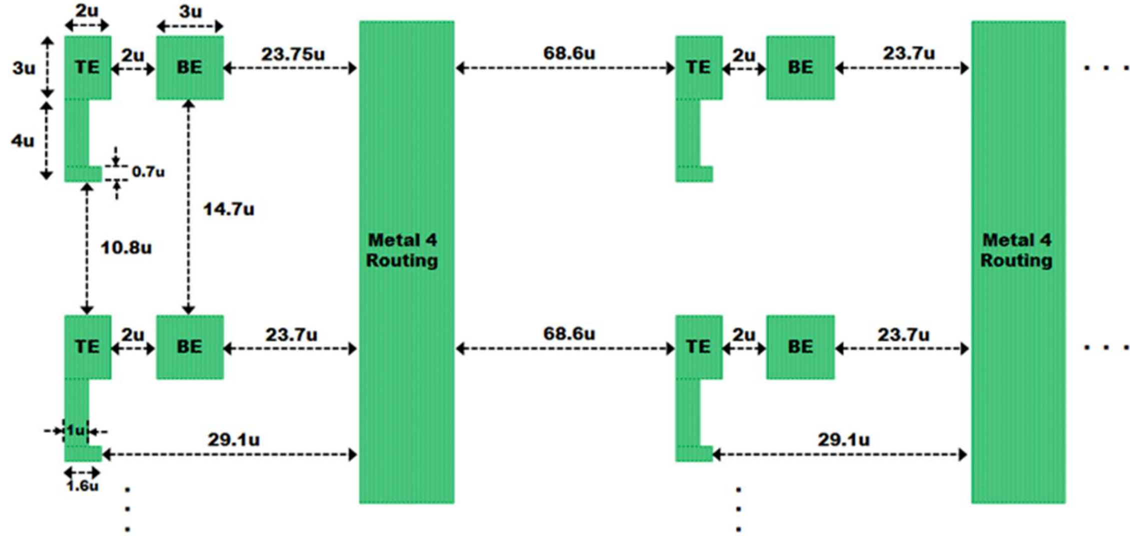


Figure 4.6: Top view of a 2x2 subset of the 8x7 CBRAM array outlining the TE, BE and the metal routing.

4.2.1 CBRAM Layout in the Neuromorphic CMOS Chips

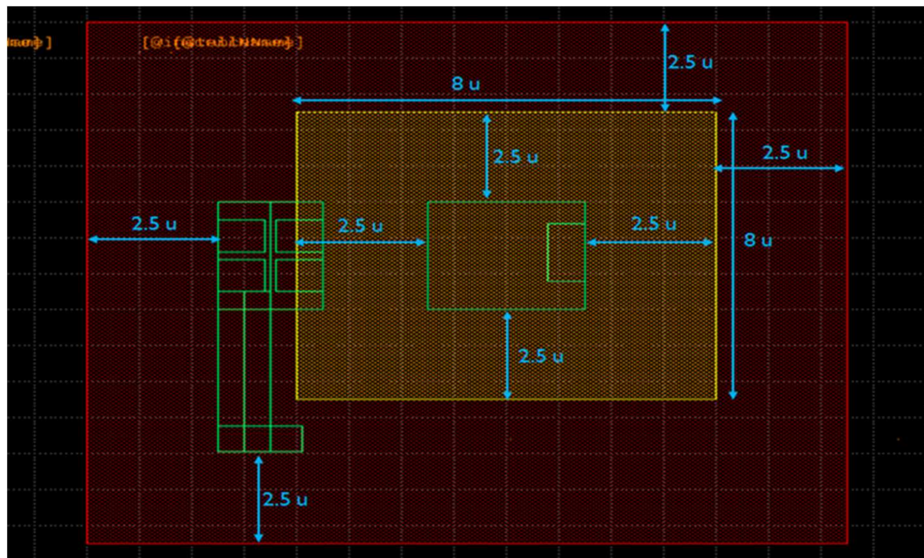
This work requires the deposition of only two CBRAM layers- *Ag* anode and *Ag-*$GeSe_3$ electrolyte. Hence, only two masks are needed for patterning as shown in Fig. 4.7 (a). In the same figure, the green outlines represent the TE and BE electrode outlines. The first mask outlined by a yellow square in Fig. 4.7 (a) patterns the $GeSe_3$ chalcogenide layer and a thin *Ag* photo dopant layer on top of the chalcogenide. The second mask outlined by a red square in Fig. 4.7 (a)patterns the *Ag* anode layer. After the completion of deposition, the latter diffuses into the chalcogenide through a process called photo-dissolution. Photo-dissolution involves the use of light energy greater than the optical gap of the glass to create charged defects at the interface of the thin Ag photo doping layer and the $GeSe_3$ chalcogenide. The electrons so created diffuse into the $GeSe_3$ layer while the holes are trapped by Ag. The resulting built-in electric field is enough to force the Ag^+ ions across

the interface energy barrier into the chalcogenide. Thus, an Ag^+ rich interfacial monolayer [43], [44] is created that supplies metal ions deep into the bulk of $GeSe_3$ through drift and diffusion.

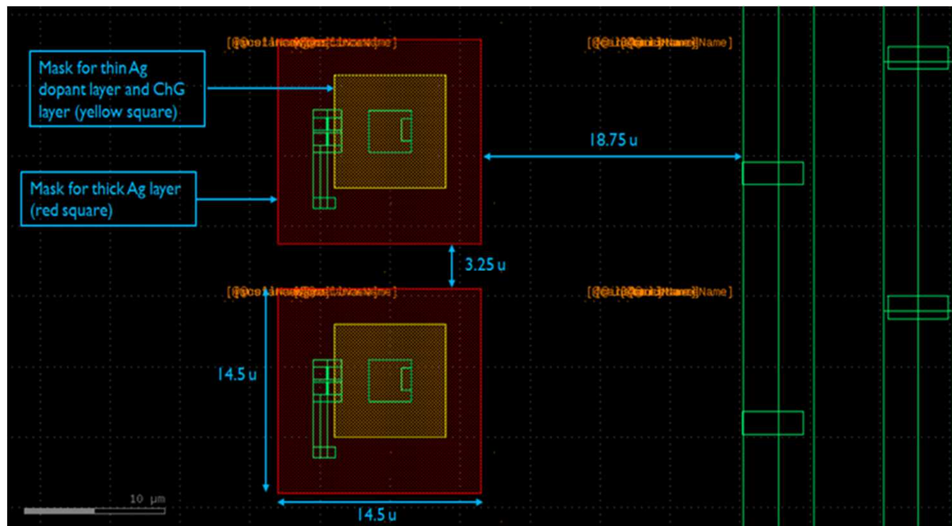
The masks were designed to fulfill three conditions: - the *Ag-GeSe₃* mask must completely cover the BE so that the Ag anode layer does not come in contact with it and short circuit the device, the *Ag* anode mask must completely cover the TE and the *Ag-GeSe₃* layer and since the aligner to be used for patterning the PR in the device deposition process flow (a lift-off process is used for depositing the CBRAM layers) is manually operated there is a predicted margin for error of ±2.5 µm. This means that the exposure of the PR can be off by ±2.5 µm. This means that the final layers can be misaligned by a maximum of ±2.5 µm after lift-off. Considering all the three conditions, the *Ag-GeSe₃* mask dimensions are made 2.5 µm larger than the BE outline and the *Ag* anode mask dimensions are 2.5 µm away from the TE and *Ag-GeSe₃* mask outline, i.e., the left and bottom dimensions of Ag anode mask are 2.5 µm away from TE outline and the right and top anode mask dimensions of the same are 2.5 µm away from the Ag-$GeSe_3$ mask outline as shown in Fig. 4.7 (a) and (b). Under these design rules, the *Ag-GeSe₃* mask is 8x8 μm^2 and the *Ag* anode mask is 14.5x14.5 μm^2 in area. Fig. 4.5 (c) shows the 10x10 sets of die on the coupon as designed in the mask with each die area being 2138x2248 μm^2 and the inter die distance being 90 µm.

Since the margin of error (±2.5 µm) is larger than the separation between TE and BE (2 µm), one obvious issue that emerges is the overlap between the *Ag-GeSe₃* layer and the TE which should not be a problem so long as the *Ag-GeSe₃* layer does not completely cover the TE. This means that in the worst scenario, the final deposited *Ag-GeSe₃* layer cannot

exceed its dimensions by 1.5 μm towards the left or bottom sides than what is outlined by its mask. Fig. 4.7 (b) shows the side-by-side comparison of masks for 2 sets of TE and BE stacks. Here, the inter-mask spacing between the *Ag* anode layers of two consecutive stacks is only 3.25 μm and thus care must be taken to prevent overlap. There are 8x7 such masks each for the *Ag* anode and the *Ag-GeSe₃* layers per die.



(a)



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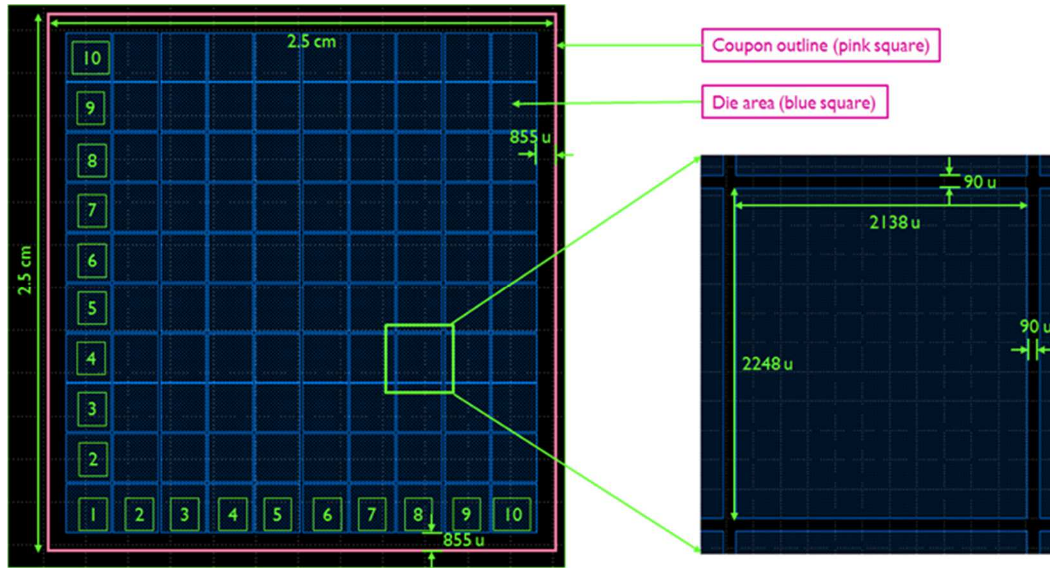


(c)

Figure 4.7: Photolithography mask layouts for CBRAM: (a) mask layout for the Ag anode layer (red square), thin Ag dopant layer (yellow square), and the $GeSe_3$ layer (yellow square); (b) mask dimensions with respect to the metal routing; (c) coupon layout with the scribe, die and coupon dimensions.

5 PLANARIZATION PROCESS FLOW AND CHARACTERIZATION

The processing was carried out on 1-inch by 1-inch square coupons diced from round MG wafers with a 6-inch diameter. MG wafers are the lowest grade wafers available and are only used for testing purposes. As such, these MG wafers do not have any FEOL CMOS and lower-level metal; only the top level. The processing work was carried out at the Nanofabrication facility of Arizona State University. The process flow for the planarization recipe is discussed in upcoming subsections.

5.1 LOR 3A and SOG process flow

5.1.1 Wafer scribing and dicing

The 8-inch mechanical wafers were first scribed into 4 quarters before dicing into coupons. This is because the dicer available can only dice a wafer with a maximum diameter of 4 inches. Upon dicing, 8 1-inch by 1-inch coupons were obtained from each quarter. So, for one 6-inch wafer, 32 coupons can be obtained.

5.1.2 Wafer cleaning and treatment

Ideally, an acid-based cleaning technique like Piranha clean or RCA clean is best for removing any metal ions or organic particles. But since the coupons contain metal layers on them as part of the TE and BE, acids would corrode the metal. Thus, a simpler clean is performed using Acetone, Methanol and Isopropyl alcohol (AMI).

Since the cleanroom has high humidity (>40%), a dehydration bake is performed over a hot plate immediately before spinning at a temperature of 140°C for 10 minutes. The substrate is cooled to room temperature before starting the spin process and takes between 3-5 minutes for the 1-inch by 1-inch Si coupons.

For the SOG, the cooling process should occur in an environment with low humidity (<40%) due to the hygroscopic nature of the wafer. It is also recommended that the spin cup humidity be maintained below 40% for the same reason, i.e., moisture adsorbed by the wafer surface can prevent the SOG from sticking properly to the wafer surface. The LOR 3A exhibits good adhesion to Si substrates and thus the cooling environment need not be a low humidity environment.

5.1.3 LOR 3A Spin Casting

The final coating profile after spinning and baking is influenced by many factors: - material properties like planarizing liquid's surface tension, viscosity, solvent evaporation rate; shrinkage due to high-temperature curing and defects on wafer are all key in determining whether the SOG or LOR process fills gaps and gives a planar surface. Similarly, spin speed, settling time, spin acceleration, the manner of dispensing, and the ambient during the coating process determine the quality and thickness of the coat on the substrate. But, unlike the SOG, the LOR is not a very difficult material to process and is designed to give very low defect coatings in addition to providing exceptional planarity.

As shown in Fig. 5.1, the overall LOR and SOG process flow has 6 main steps (not considering the wafer cleaning and treatment): - LOR 3A spinning, LOR 3A baking, LOR 3A dry etching, SOG spinning, SOG baking and SOG dry etching.

According to the thickness versus spin speed curve in [12], the LOR 3A film is about 225 nm thick when spun at 3000 RPM. Note that the film height is of no concern here as long as the LOR film is thick enough to reduce the step coverage to about 100 nm across the TE and BE. Accordingly, a technique is employed to increase the LOR settling time.

After spinning each layer of LOR 3A, the substrate is left on the spin chuck for 5 minutes to allow for the spun LOR layer to 'settle'. During this time, the LOR 3A layer is still fluidic in nature due to the presence of solvents and is thus vulnerable to external factors. One such factor is the cleanroom airflow that can ruin the planarity of the spun resist layer. To avoid this, the substrate is covered with a beaker for the 5 minutes of 'settling' time.

It was found that 15 layers of LOR 3A (each layer is spun at 3000 RPM to a height of 225 nm) can be stacked on top of one another when individual films are baked at a constant high temperature. Any attempts to spin subsequent layers crack the layers at the bottom. But, if ramped baking (ramping the temperature up in steps over time) is used, even 20 layers can be stacked without cracking the film. Since this recipe uses ramped baking 18 stacked layers were spun (total predicted height is 4050 nm). But spinning such a huge number of layers is a time-consuming procedure, approximately 20 minutes per layer with a total of 6 hours for all 18 layers. It is worth noting that the LOR 10A (each layer is 1100 nm thick at 3000 RPM [12]) by Kayaku Advanced Chemicals was considered as a substitute to lessen processing time but the results were highly unfavorable. The LOR 10A film cracked after the 9th layer (total film thickness was about 10 μm) and despite the high thickness the film non-uniformity across the TE and BE stacks was still about 200 nm (twice of that for LOR 3A). This proves that just increasing the total planarizer height thickness does not give better planarity; the number of layers also plays an important role.

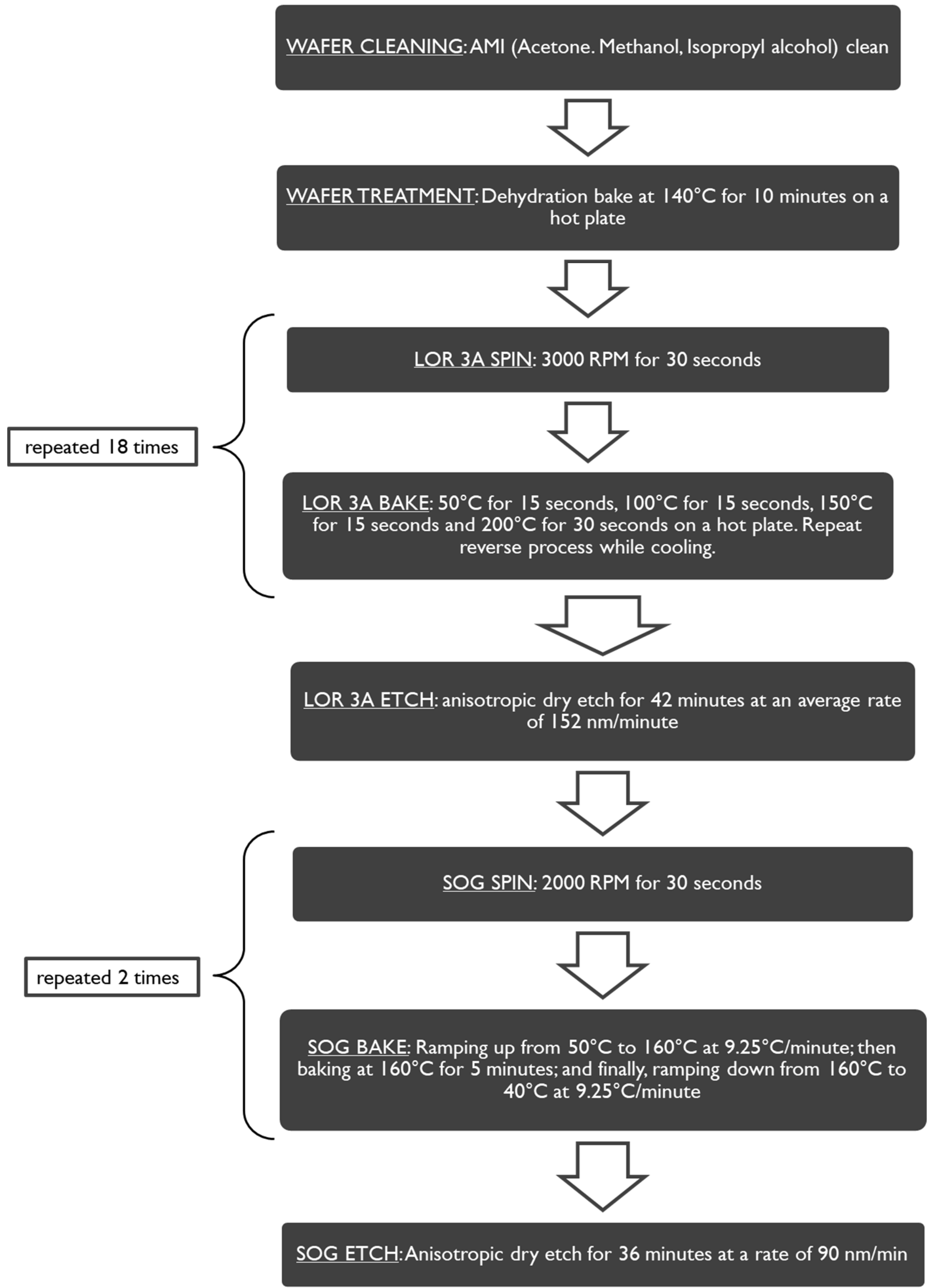


Figure 5.1: SOG and LOR planarization process flow on MG Si wafers.

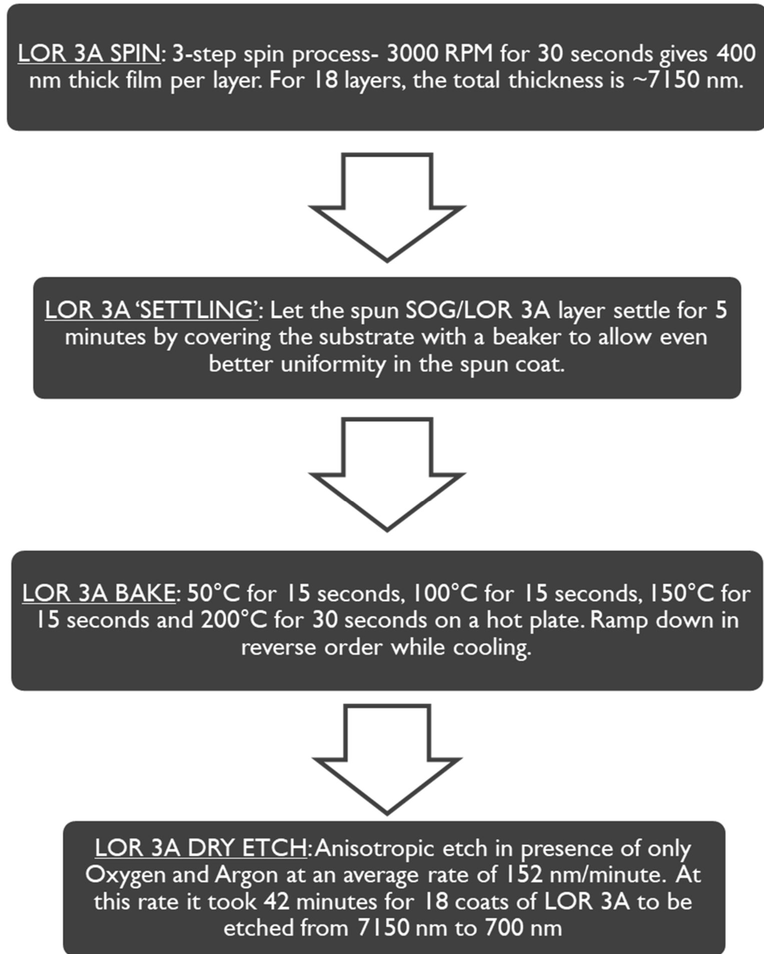


Figure 5.2: LOR 3A process flow.

As shown in Table 5.1, the LOR 3A spin recipe is a 4-step process: - the dispense step, the spread/flow-in step, the spin-off step and finally, a decelerating step. The dispense step as the name suggests is when the LOR 3A is dispensed onto the substrate. It can be dynamic where the LOR 3A is dispensed while the substrate spins at a low speed of 100-300 RPM or static where the substrate does not spin. The spin coater tool used in this work does not allow dynamic dispensing. It should be noted that dynamic dispense gives more uniform and planar film for patterned wafers with 125mm or larger diameter whereas static dispense

produces higher quality films on smaller wafers. This is because static dispense would require larger dispense time on larger wafers and PR sitting on a static wafer for long periods results in solvent evaporation causing spin defects. The substrates used in this work being 1-inch by 1-inch, static dispense works better. The spread/flow-in step causes the dispensed LOR 3A to spread over the entire wafer evenly by pushing the excess LOR 3A to the edges. The flow-in step is short (5-7 seconds) and slow (500-1000 RPM/second) acting as a transition between dispense and spin-off. The spin-off step allows the excess resist to be spun off the edge of the substrate leaving a more planar layer of desired thickness. This step runs at a much higher speed (determined by the film thickness versus spin speed chart in [12]) and for a longer time than the previous two steps. Finally, the deceleration step is an intermediate step before the spin process comes to a halt. A solvent-rich environment is needed in the spin cabinet for good film uniformity and to prevent the spun layer from drying too fast. Squirting about half a pipette's worth of LOR 3A into the cabinet right before spinning is adequate.

Table 5.1

LOR 3A spin recipe

Steps	**Spin Speed (RPM)**	**Ramp rate (RPM/second)**	**Time (seconds)**	**Exhaust**
Dispense	0	0	< 20	-
Spread/Flow in	500	500	5	5%
Spin-off	3000	500	30	80%
Deceleration	300	500	7	80%

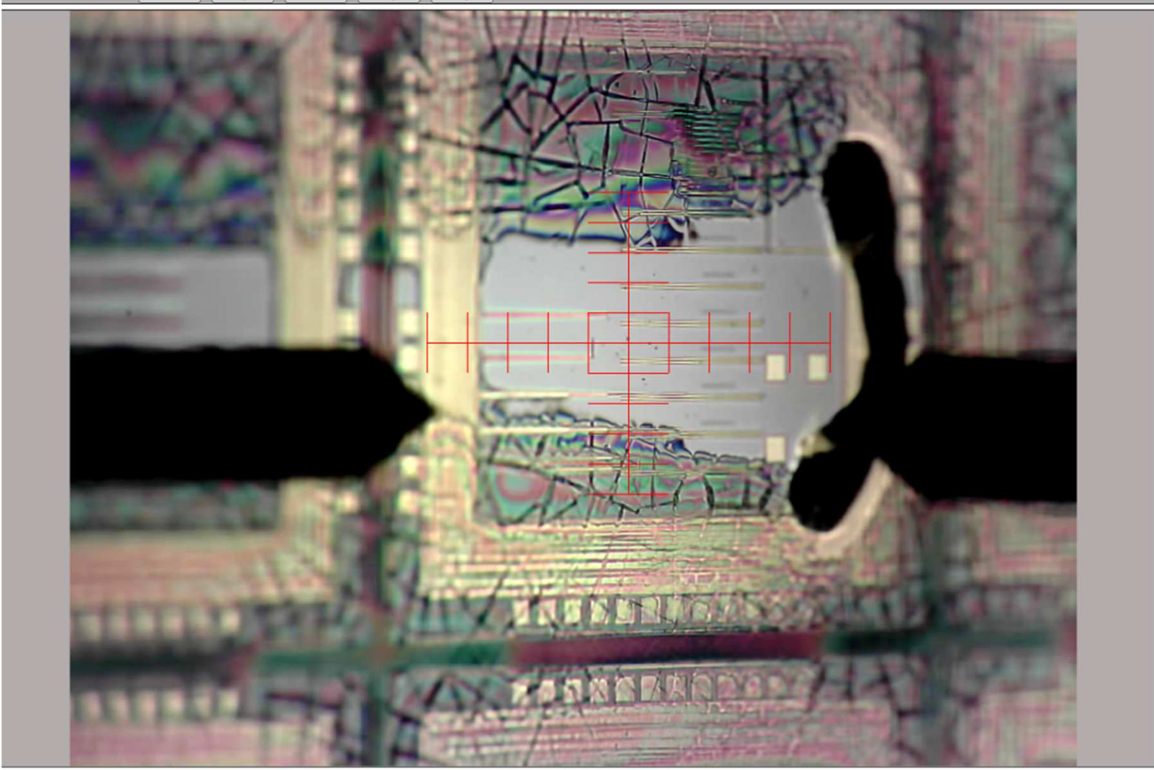
Another step is usually included between the spin-off and deceleration steps to push away the edge beads off the edge or at least as close to the coupon edge as possible. This recipe does not use one because edge beads are not of primary concern. Besides since a square coupon is used it is impossible to eliminate edge beads as there will always be some left at the square corners. Edge bead formation is a build-up of spun liquid along the outer edge of a wafer caused by surface tension during spin coating. In this step, the substrate is spun at speeds much higher than spin-off (~6000-10,000 RPM) for a short time (~5-7 seconds). Alternatively, an Edge Bead Remover (EBR) solvent can be used to manually strip off any edge beads.

5.1.4 LOR 3A Post-spin bake

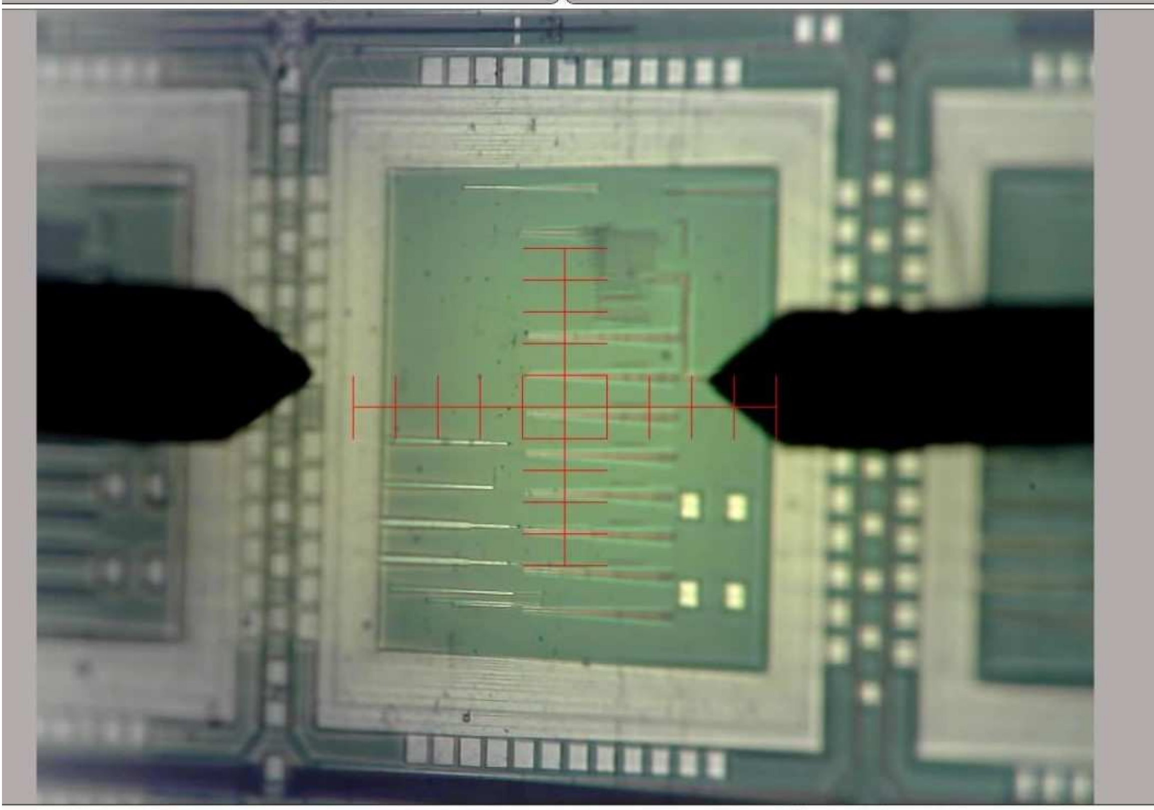
Owing to the propensity of cracking after a high number of spun-on layers, a ramped bake is performed for LOR 3A where the temperature was ramped from 50°C to 200°C in 4 steps and again back down to 50°C in 3 steps. The steps are: - after letting the substrate 'settle' for 5 minutes it was first subjected to 50°C for 15 seconds, then 100°C for 15 seconds, followed by 150°C for 15 seconds and finally, the target temperature of 200°C for 30 seconds. The steps were retraced in the same manner for cooling: - 150°C for 15 seconds, 100°C for 15 seconds and finally, 50°C for 15 seconds. The reason for choosing a target temperature of 200°C is that it renders the LOR 3A optically undevelopable. This means that any subsequent exposure and resist development process steps as part of CBRAM deposition will not affect the film stack in any way.

This method of baking enabled a completely crack-free film stack. This is because the lower the LOR 3A layer sits in the film stack, the greater number of times it gets subjected

to baking; the bottommost layer gets baked 18 times, the layer above it gets baked 17 times and so on. The heat travels through the bottom layers every time to be able to bake the topmost layer subjecting them to unnecessary stress. To make matters worse, it is imperative that the bottom 2-3 layers of LOR 3A remain in perfect condition because the top 15-16 LOR 3A layers are to be etched away and only serve to provide the desired planarity to the topography. Fig. 5.3 (a) shows a LOR film that cracked and 'peeled-off' after etching due to stress when the films were baked at a constant high temperature whereas the film in Fig. 5.3 (b) is completely crack-free due to ramped baking.



(a)



(b)

Figure 5.3: 18-layer LOR 3A film stack when baked at (a) constant temperature of 200°C and (b) ramped temperatures.

It was found that each LOR layer was about 400 nm thick after baking instead of the predicted 225 nm. This is because of the ‘settling’ process, i.e., as some of the resist liquid from the thicker edge beads flow inward while ‘settling’ thereby increasing the film thickness. Thus, the total thickness of the 18-layer film stack is 7150 nm as shown in Fig. 5.4.

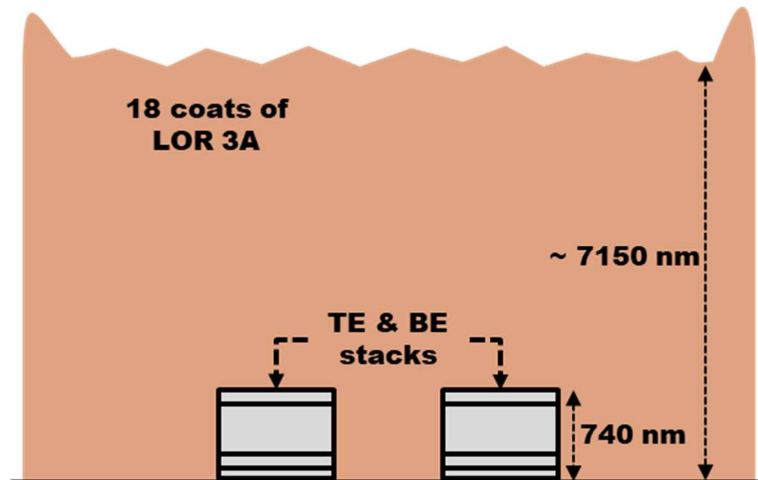


Figure 5.4: LOR 3A film stack after baking

It should be noted that even though ramped baking in discrete steps of temperature increment works fine, the best way is to continuously increase the temperature slowly from 50°C to 200°C and back down to 50°C again. But since it would take an enormous amount of time to perform the bake for 18 layers, this is not done.

5.1.5 LOR 3A etch-back

After baking, the 7150 nm thick LOR 3A film stack was etched for 42 minutes in presence of oxygen and argon gases to bring the thickness down to 700 nm as shown in Fig. 5.5. Now, the etch time of 42 minutes means that the etch rate is 152 nm/minute. But it was found that this etch rate varies between 150 minutes to 165 minutes and thus a fixed etch time does not exist. The best way is to perform the etch in 2 steps. Firstly, perform an initial etch for a 'safe' time such that over etching is impossible, calculate the etch rate and measure the thickness of the LOR 3A left. Secondly, perform a final etch-back based on the time needed to bring down the thickness to 700 nm at the calculated etch rate. The etch time can differ between etching tool types and etch chamber conditions. The etch time is

‘safe’ when it is minimum due to the etch rate being maximum. Thus, the ‘safe’ time assuming a maximum etch rate of 165 minutes is 39 minutes for the Plasmatherm 790 Reactive Ion Etch (RIE) tool in the ASU NanoFab. This is an anisotropic etch meaning that the LOR 3A etches only in the direction of the gas flow. Other parameters of importance are the chamber pressure of 11 mTorr, dc bias of 515 V and the forward and reflected powers of 175 W and 3W respectively. Table 5.2 shows the entire etch recipe.

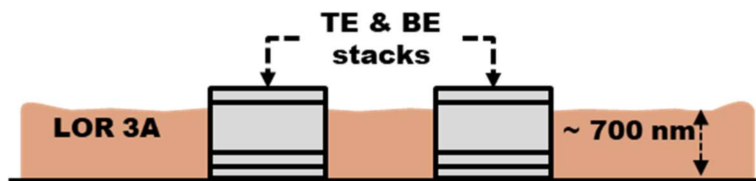


Figure 5.5: LOR 3A film stack after dry etching

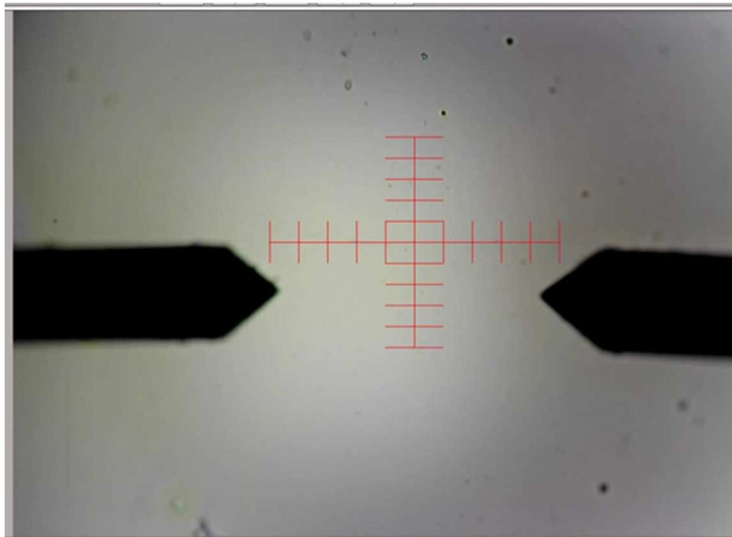
Table 5.2

LOR 3A dry etch process parameters

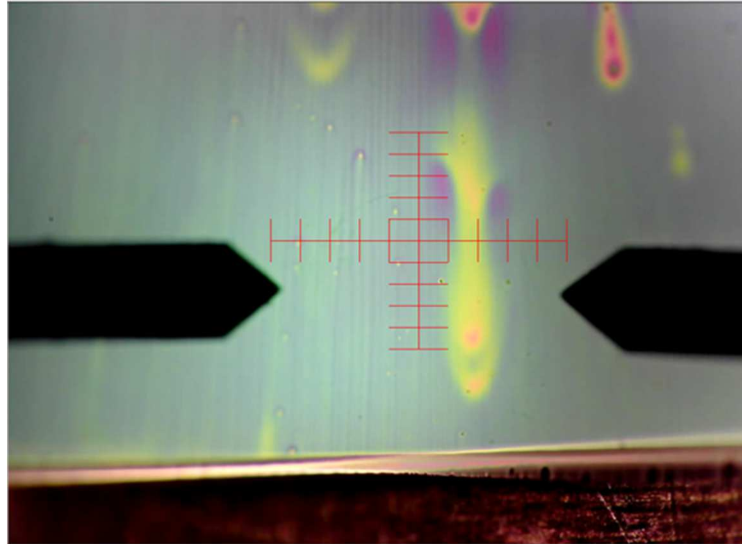
Gas	Oxygen (O_2)	Argon (Ar)
Gas flow rate	8	8
Etch time (minutes)	42	
Etch rate (nm/minute)	152	
Forward Power (W)	175	
Reflected Power (W)	3	
DC Bias (V)	515	
Chamber Pressure (mTorr)	11	

5.1.6 SOG Spin Casting

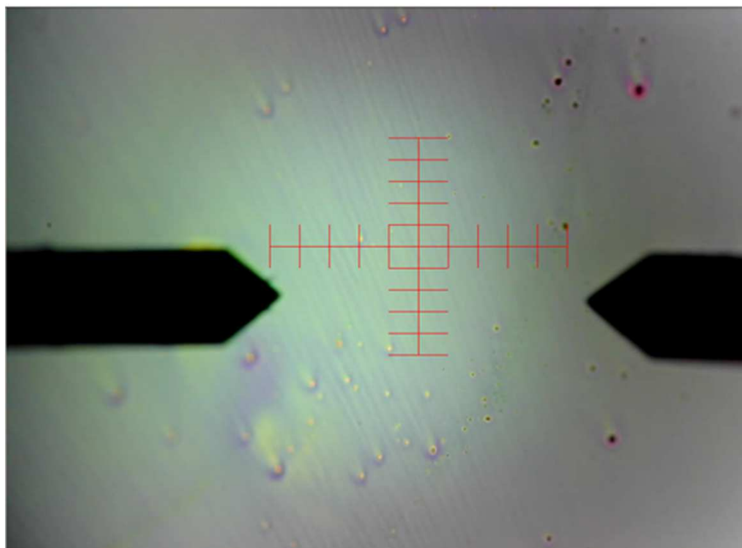
The SOG is a very difficult material to process due to several issues like film cracking, defects, film hazing, etc. Thus, before describing the spin process, certain precautions are to be followed for best SOG coats. It is recommended to store the SOG at 4°C to prolong its shelf life. If done so, the SOG needs to be warmed to room temperature before spinning it onto substrates. This is to be done by allowing the SOG to settle for about 24 hours at room temperature. Cold SOG can give poor quality films with high particle levels and form haze on the spun film thereby making the film cloudy as shown in Fig. 5.6 (a).



(a)



(b)



(c)

Figure 5.6: Image of a SOG film under a microscope: (a) a cloudy SOG film due to high humidity, (b) and (c) particles on a substrate causing the SOG to accumulate around the particles while spinning giving a comet-like appearance.

The SOG can be rinsed and removed by isopropyl alcohol (IPA), denatured alcohol or ethyl acetate as long as the SOG solvent has not completely evaporated. But, once the solvent evaporates and the SOG layer sets in, only hydrofluoric acid (*HF*) or Buffered Oxide Etchant (BOE) can etch it. And the SOG dries very fast so all equipment that is prone to exposure to the SOG must be made from polyvinyl or polypropylene as these materials wet well with rinsing solvents. Good wetting ensures complete removal of residual SOG thereby preventing them from being a source of particles in future processing work. In this process, IPA was used for rinsing and it worked well given that the equipment was rinsed immediately after spinning.

A plastic pipette was used for dispensing the SOG onto the substrate. The dispensing should be done immediately after taking the pipette out of the SOG bottle as the solvent dries very fast and can cause particles to form within the pipette. These particles would then transfer to the SOG layer on the substrate while dispensing. The same can happen if the pipette tip touches the SOG layer while dispensing and so sufficient distance must be maintained. Similarly, to avoid the transfer of the same particles to the SOG solution in the bottle, the pipette is to be disposed of after using only once and along with the SOG that may remain unused in the pipette. Fig. 5.6 (b) and (c) show the effect of particles on the spun and dried SOG layer.

At least 80% of the substrate must be covered with SOG while dispensing so that the spun layer gives uniform coverage over the substrate. It is recommended to complete the dispensing within 5 seconds and start the spin process immediately after. A longer dispense time can cause the layer to be thicker at the substrate center due to solvent evaporation.

Note that in subsection 5.1.5 ‘LOR 3A etch-back’, 700 nm of the topography is covered by LOR 3A while only 40 nm is left to be planarized by the SOG. The reason for this is two-fold. Firstly, the SOG can only be stacked up to 2 layers for a maximum total height of 2200 nm [42] at a spin speed of 2000 RPM before the film cracks. And secondly, SOG layers are prone to defects that come from the material itself and thus are impossible to eliminate meaning that the more the layers are stacked, the more is the defect count in the film stack. Unlike LOR 3A spin casting, a 3-step spin recipe is used here as shown in Table 5.3. The spin-off step spin speed was chosen to be 2000 RPM because going any higher would only decrease total film thickness thereby increasing non-uniformity due to bad step coverage and going any lower also decreases film planarity. Any significant uniformity variation is easily visible to the naked eye in the form of color variation along the plane of the film as shown in Fig. 5.7.

Table 5.3

SOG spin recipe

Steps	**Spin Speed (RPM)**	**Ramp rate (RPM/seconds)**	**Time (seconds)**	**Exhaust**
Dispense	0	0	< 10	-
Spread/Flow in	500	500	5	5%
Spin-off	2000	1000	30	80%

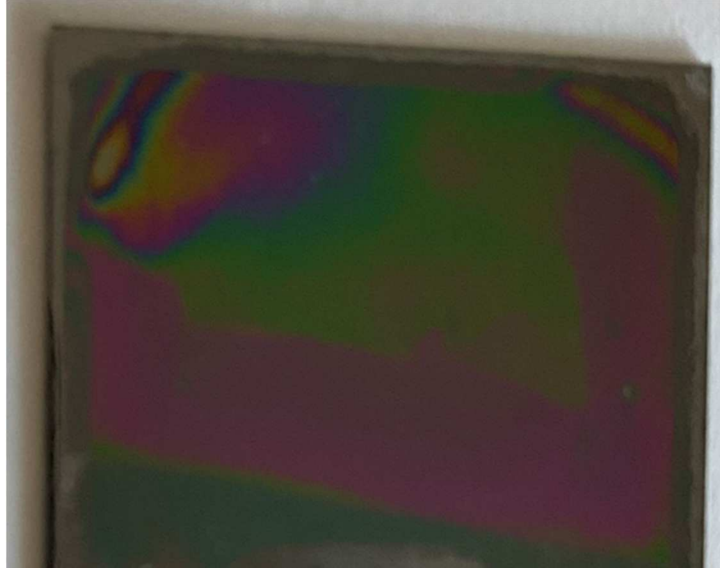


Figure 5.7: Visible color variation in SOG film due to non-uniformity.

Even though [12] predicts the SOG film thickness to be 1100 nm per layer at 2000 RPM, the final SOG layer is somewhat higher, 1225 nm per layer. Again, similar to the SOG, this is because of the 'settling' process as some of the resist liquid from the thicker edge beads flow inward while 'settling' thereby increasing the film thickness. The spin time depends on the humidity level of the cleanroom. If the cleanroom humidity is less than 35%, a spin time of 30 seconds is sufficient. Otherwise, a higher spin time between 30 seconds to 1 minute is required to allow for more solvent evaporation while spinning. This is because if the environment is too humid, the SOG absorbs water while performing post-spin bake and the film becomes cloudy.

The SOG tends to form a mist of liquid droplets above the substrate while spinning which produces particles or bubble-like defects in the films. Sufficiently high exhaust can evacuate the solvent vapor and keep the mist level below the plane of the wafer surface. Besides this, it was noticed that using insufficient exhaust causes non-uniformity in the

spun film. Thus, the exhaust must be turned on and maximized during all process steps. In this work, the exhaust was kept at 80% because that was the maximum allowable limit. Besides the exhaust, a solvent rich environment is also needed within the spin cabinet for film uniformity and to prevent the SOG layer from drying too fast. For best results, squirting about one pipette's worth of SOG into the cabinet is recommended. But, since the SOG can be costly using one of the component casting solvents of the SOG instead would suffice. Accordingly, in this process, IPA was sprayed in the cabinet as it is one of the casting solvents of the Desert Silicon NDG-7000R SOG and is readily available in a cleanroom. Also, while dispensing with a pipette, care should be taken such that no air bubbles form on the dispensed SOG film otherwise, defects will form in the baked layer in the form of voids. It is recommended to use the highest possible acceleration for the spin step that sets the SOG thickness. Due to being limited by the lithography capabilities of ASU NanoFab, one second is the minimum possible spin speed ramp rate that could be achieved. The entire process flow of SOG processing is outlined in Fig. 5.8.

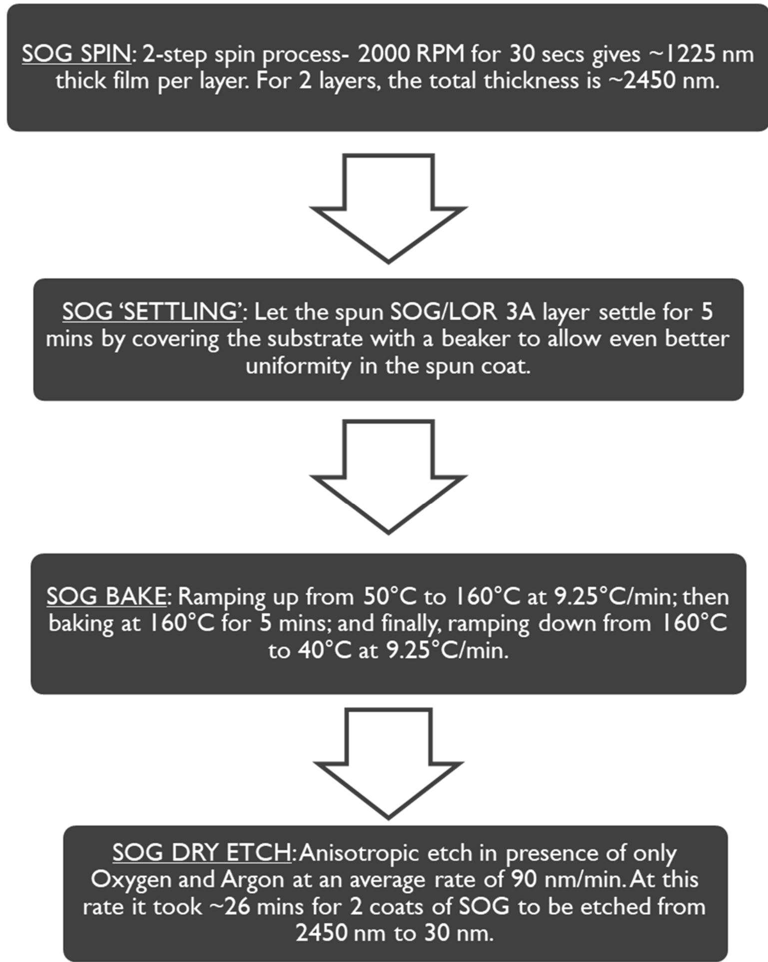


Figure 5.8: SOG process flow

5.1.7 SOG Post-spin bake

The vendor recommended maximum bake temperature for a double coat of NDG-7000R SOG is 225°C when spun at 2000 RPM. But this SOG is highly sensitive to temperature and may crack at 225°C when spun at lower spin speeds (thicker films). The SOG is also very moisture sensitive and clouds up in highly humid environments (>35%) if not immediately baked (humidity level in the ASU NanoFab cleanroom is >40%). And similar to LOR 3A, the SOG film cracks when subjected to a constant high temperature

due to induced film stress. In fact, the situation is even worse as performing a ramped bake in steps is not enough but rather a continuous ramped bake is needed. Despite this, the film still cracks if a third layer is stacked. Considering all these factors, the coupon is placed onto a hot plate immediately after spinning the SOG and the temperature is ramped continuously from 50°C to 160°C at a constant rate of 9.25°C/minute; the substrate then sits at 160°C for 5 minutes before ramping down the temperature at the same rate of 9.25°C/minute to 50°C.

Usually, post-spin baking is followed by curing the SOG film at a very high temperature of around 400°C or higher to remove any remnant solvents and further densify the film. But, since the Desert Silicon NDG-7000R can only withstand a temperature of 225°C before cracking, curing is not feasible. Hence, to maximize solvent evaporation the baking temperature is kept as close to the upper limit as possible given that it does not crack the film. The final double layer SOG coat is around 2450 nm after baking is shown in Fig. 5.9.

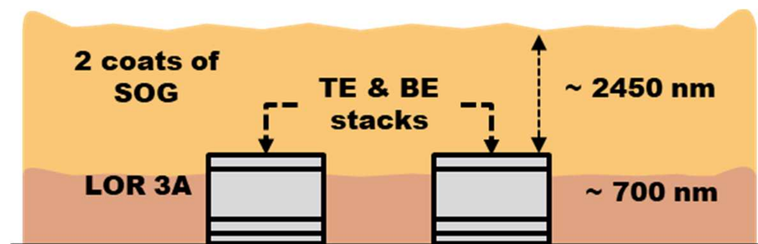


Figure 5.9: 2-layer SOG stack

5.1.8 SOG etch-back

After baking, the 2450 nm thick LOR 3A film stack was etched anisotropically for 27 minutes in presence of oxygen (O_2) and fluoroform/trifluoro methane (CHF_3) gases to

bring the thickness down to 40 nm as shown in Fig. 5.10. The etch time is 27 minutes which means that the etch rate is around 90 nm/minute. But the etch rate, similar to the situation for LOR 3A, can vary by ±10 minute and so the best way is to first perform the 'safe' etch considering the maximum possible etch rate of 100 minutes for 24 minutes (specific to Plasmatherm 790 RIE tool in the ASU NanoFab), then calculate the new etch rate, and perform the final etch for the time needed to make the SOG 40 nm thick based on the new etch rate. Etch time can differ between etching tool types and etch chamber conditions. Other parameters of importance are the chamber pressure of 41 mTorr, dc bias of 543 V and the forward and reflected powers of 246 W and 1 W respectively. Table 5.4 shows the entire etch recipe.

Table 5.4

SOG dry etch recipe

Gas	Oxygen (O_2)	Fluoroform (CHF_3)
Gas flow rate	3	40
Etch time (minutes)	27	
Etch rate (nm/minute)	90	
Forward Power (W)	246	
Reflected Power (W)	1	
DC Bias (V)	543	
Chamber Pressure (mTorr)	41	

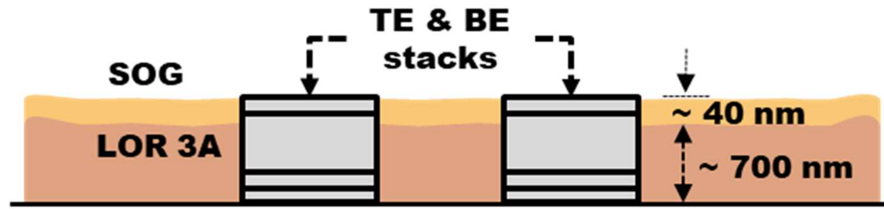


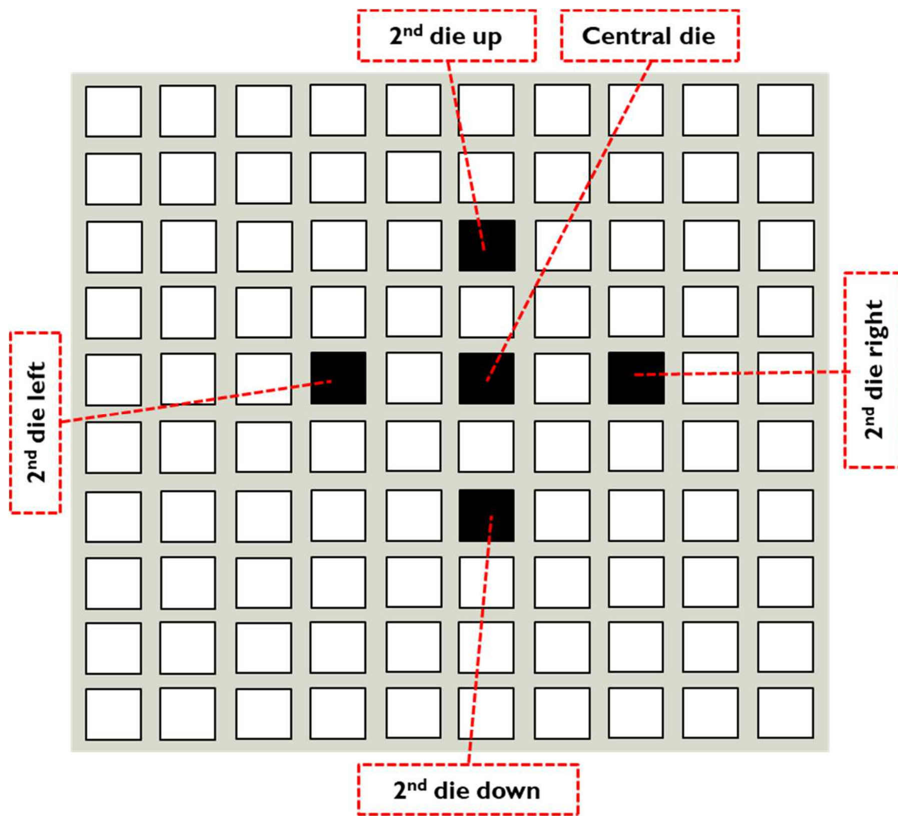
Figure 5.10: SOG film stack after dry etching

5.2 LOR 3A and SOG film characterization

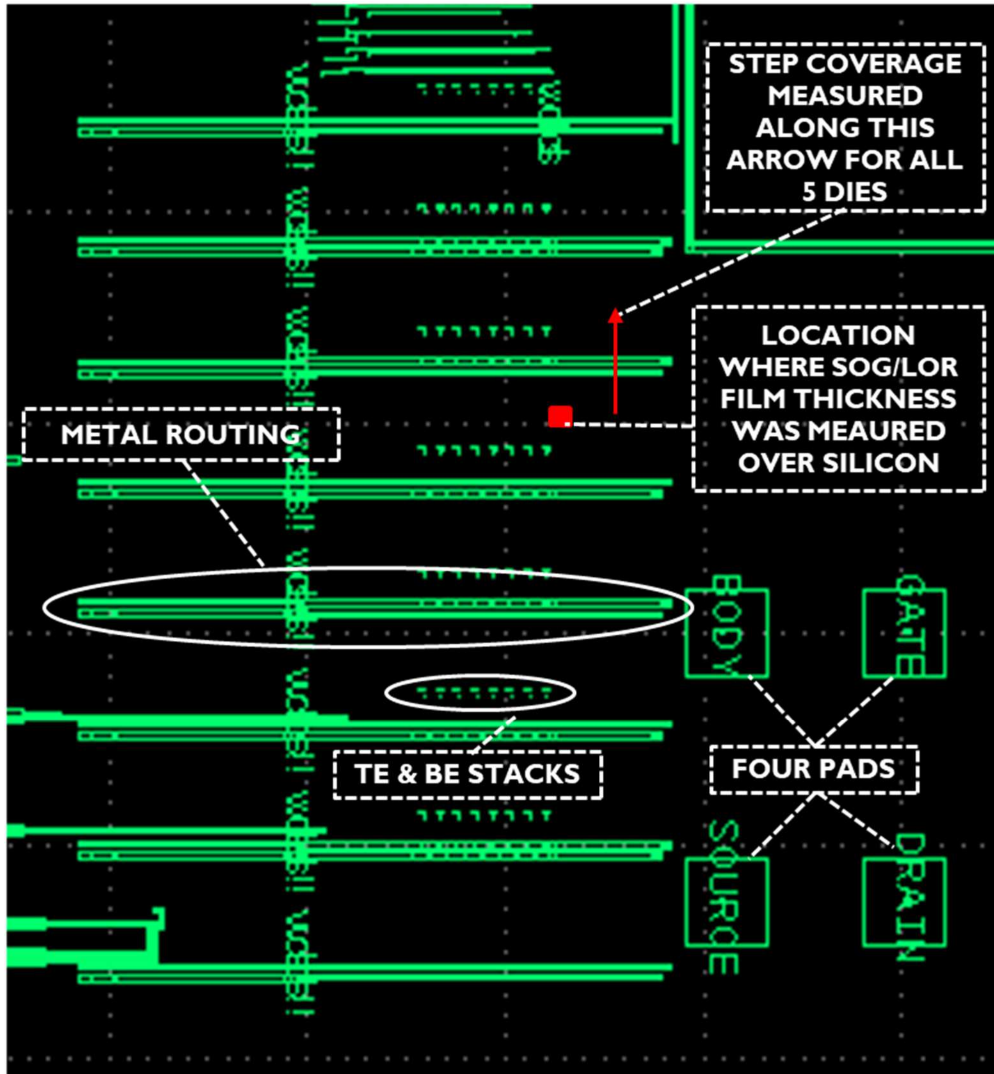
Material characterization is done using profilometry (Bruker Dektak XT Stylus profilometer in ASU NanoFab) and spectroscopic reflectometry (Filmetrics F40 in ASU NanoFab). Profilometer as the name suggests measures the surface profile of films. Here, the profilometer tool Bruker Dektak XT is a contact-based profilometer meaning it has a very sharp stylus that measures the 'hills' and 'valleys' as it runs over the film.

Spectroscopic reflectometry, on the other hand, uses reflection of light waves at film surfaces and interfaces to characterize film thicknesses. When light is incident on a film, some of it is reflected from the surface and some transmit across the film. This same happens to this transmitted light at the interface between this film and another film of a different material sitting underneath. This keeps going until the bottommost layer is reached. Depending on the phase difference between the light reflected from the film surface and the interface between the films, the combined light can create varying levels of constructive and destructive interference. This phase difference depends on the light wavelength and the optical distance the light travels. Finally, a model is fit to the reflected intensity versus light wavelength data to extract the film thickness. Here, the film thickness is varied in the model to minimize the error between the fitted model and measured data.

Note that the accuracy of spectroscopic reflectometry deteriorates after more than three layers of different materials are stacked. Spectroscopic ellipsometry is a better option if the optical properties of the film material are known. Even though the optical constants of the LOR 3A were known, that for the SOG were not known and ellipsometry could not be used.



(a)



(b)

Figure 5.11: (a) dies used for measurement and (b) location of measurement on a die is marked in red color (thickness is measured over the red square and step coverage is measured the red arrow).

To get accurate and consistent results, the location of measurement on a coupon was kept constant. Out of the 100 dies on a coupon, both film thickness and profile were measured at 5 locations: - the centermost die and 2nd die up, down, left and right of it as

shown in Fig. 5.11 (a). This is because the dies around the center have the least non-uniformity as will be discussed later in this section. But the die dimensions are in thousands of microns while the profilometer measures film profile accurately over only a few hundreds of microns. Thus, the measurement can only be taken over a small location on a die. This location is near the 4th row from the bottom and 8th column from the left of the TE and BE stacks when the coupon is oriented such that the four pads in any die are at the bottom right corner as shown in Fig. 5.11 (b).

Fig. 5.12 shows the film thickness measured on the five die locations after post-spin bake or before etching and Fig. 5.13 shows the same after etching of LOR 3A. Fig. 5.14 (a) shows the 18-layer LOR 3A film stack profile on the centermost die right after baking or before etching and Fig. 5.14 (b) shows the step height difference for all 5 dies. Fig. 5.15 (a) and (b) depicts the same information but after etching. Similar to LOR 3A, the SOG film thickness as measured by Filmetrics F40 before and after etching is shown in Fig. 5.16 and Fig. 5.17 respectively. And Fig. 5.18 (a), (b), (c), (d) and (e) shows the 18-layer LOR 3A film stack profile before etching whereas Fig. 5.19 (a), (b), (c), (d) and (e) shows the LOR 3A stack profile right after etching. In Fig. 5.19 (a), the step height was measured at the lower hill right over TE and BE and not on the higher hill to the left because that is where the TE and BE lie. In Figs. 5.14, 5.15 and 5.18, however, the profilometer could not detect the step over TE & BE and thus the measurement was taken in the location indicated by the red arrow in Fig. 5.11 (b).

Note that a SOG film thickness of 40 nm is quite thin compared to the 700 nm of LOR 3A film sitting underneath it. So, an obvious concern is that the SOG top layer non-

uniformity might be larger than 40 nm. In such a case, some areas of the SOG will be completely etched away and the LOR 3A underneath will be exposed. But averaging the non-uniformity values for the 5 dies in Fig. 5.19 (b), the average film non-uniformity comes out to be 22.7 nm. Thus, an extra 18 nm of leeway is left since after etching the SOG film stack it needs to be at least 40 nm thick to cover the TE and BE stacks perfectly. Additionally, if the SOG film non-uniformity was so high that it was completely etched away in certain locations, then the Filmetrics F40 would not have been able to measure the thicknesses correctly in those locations. This is because the model fitting in F40 requires that the layer materials and their estimated thicknesses be specified beforehand. If the SOG was completely etched due to high non-uniformity but was specified in the F40 model, the goodness of fit (GOF) of the model would be very low. But despite taking multiple measurements across various locations across the 5 dies and even other dies, the GOF remained above 98% consistently.

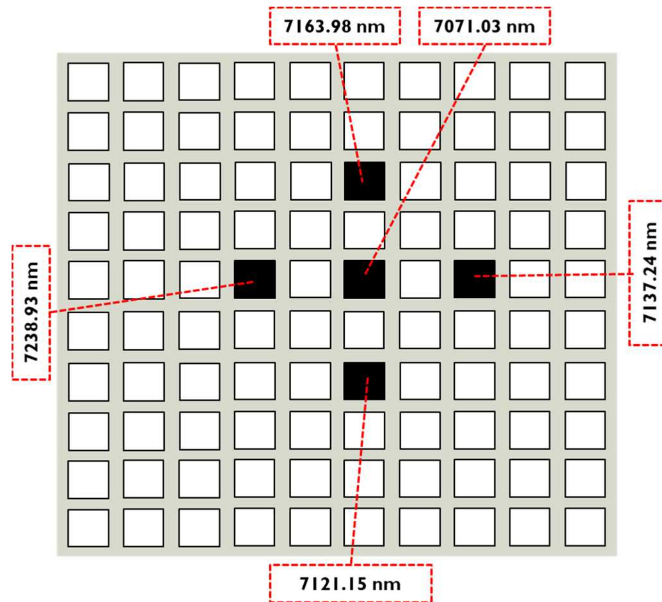


Figure 5.12: LOR 3A film thicknesses on 5 dies before etching.

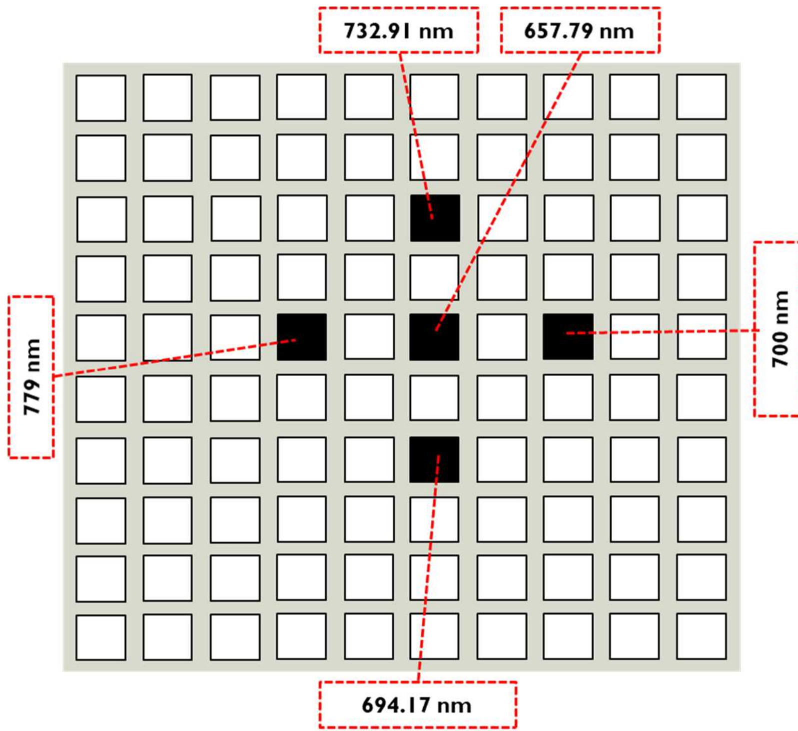
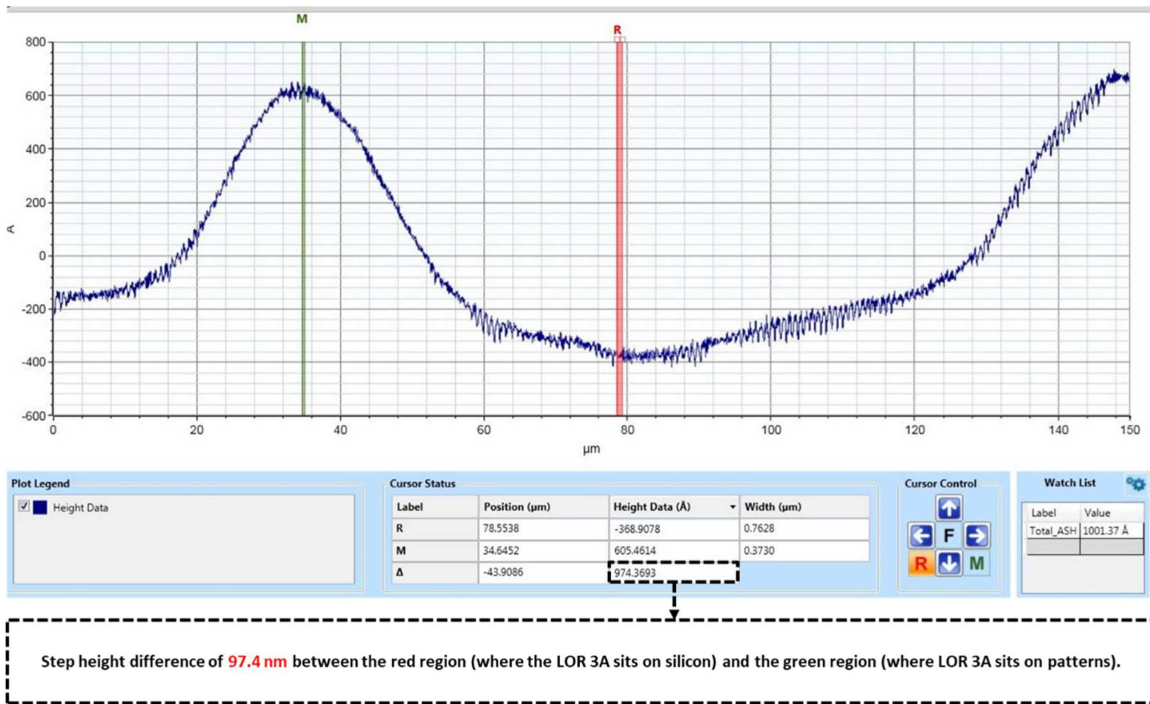
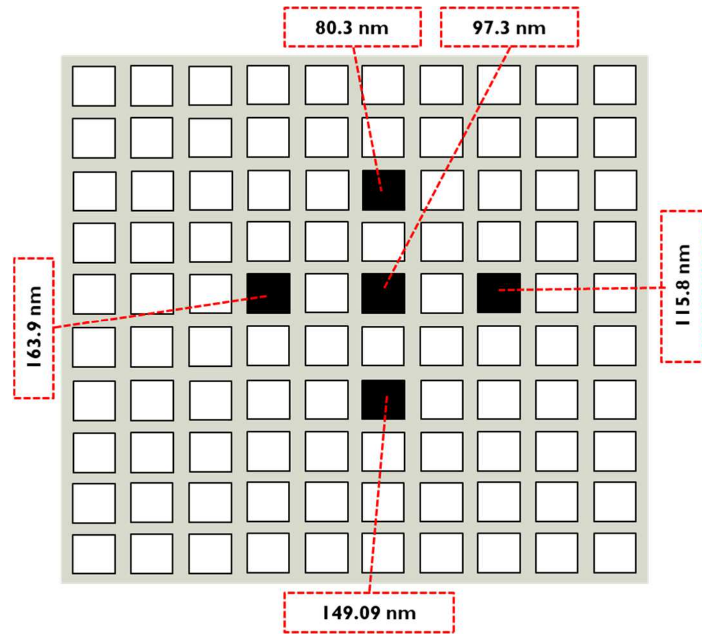


Figure 5.13: LOR 3A film thicknesses on 5 dies after etching.

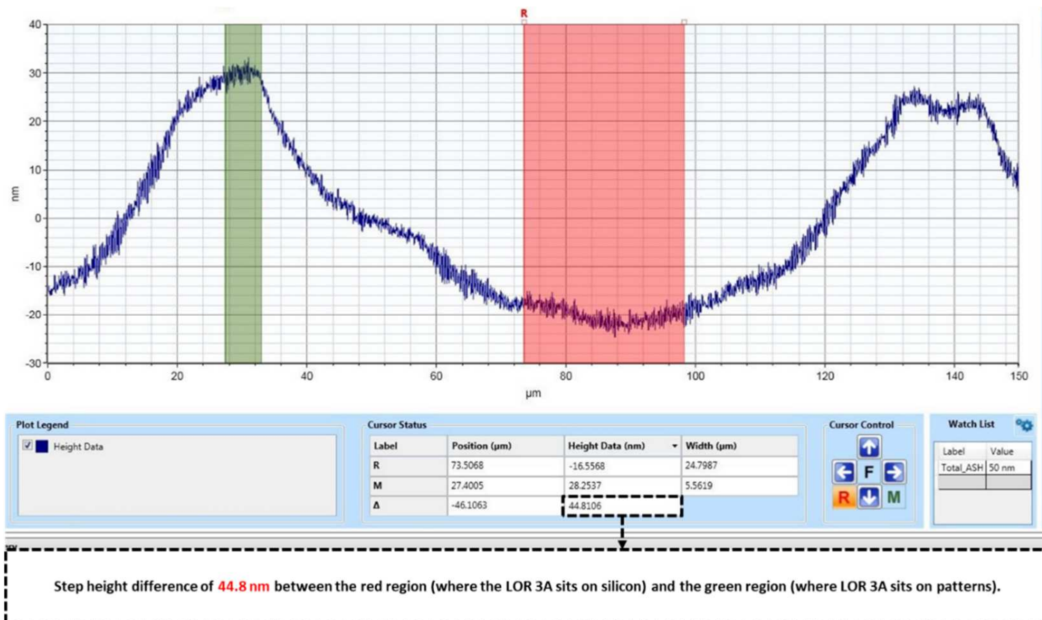


(a)

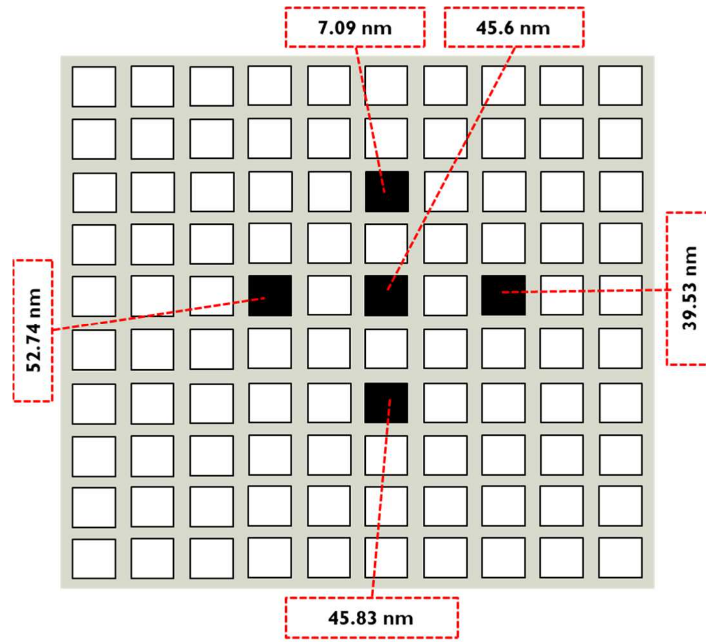


(b)

Figure 5.14: LOR 3A film profile before etching on the (a) centermost die, (b) LOR 3A film profile for all 5 dies- centermost die and 2nd dies to the right, left, above and below it.



(a)



(b)

Figure 5.15: LOR 3A film profile after etching on the (a) centermost die, (b) LOR 3A film profile for all 5 dies- centermost die and 2nd dies to the right, left, above and below it.

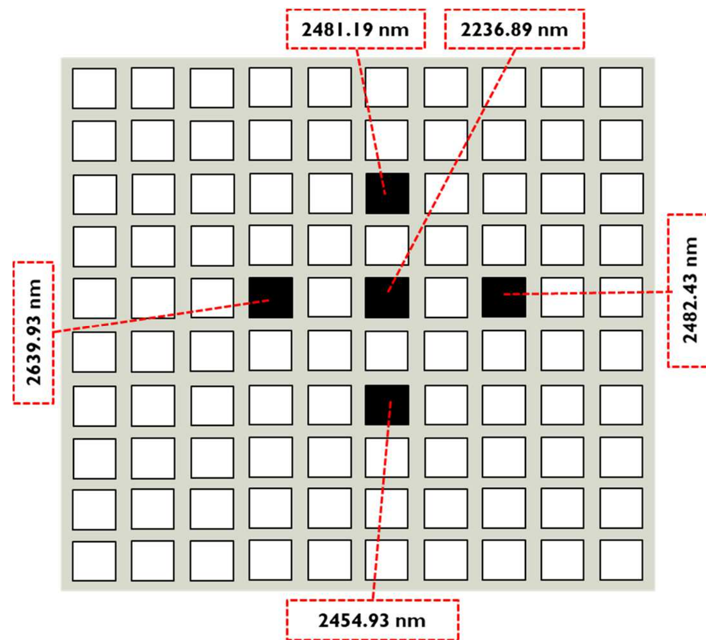


Figure 5.16: SOG film thicknesses on 5 dies before etching.

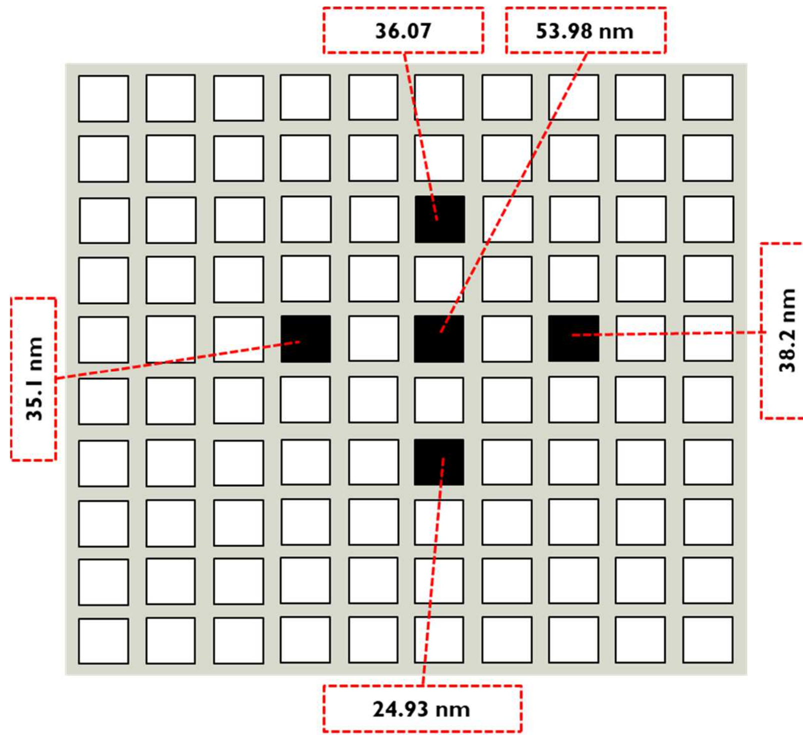
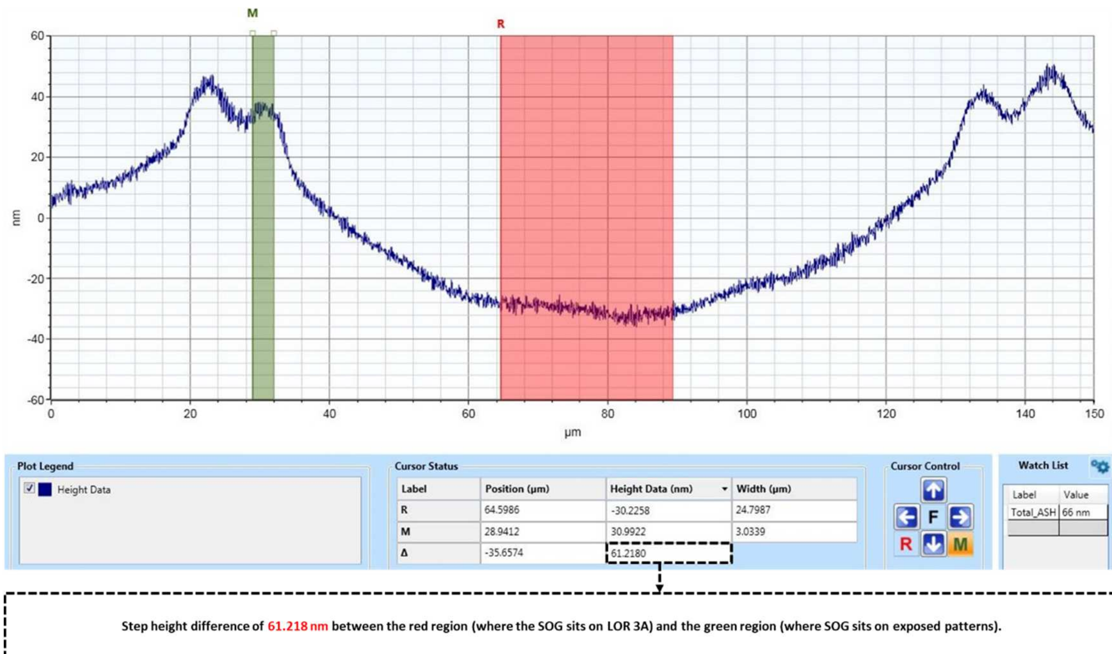
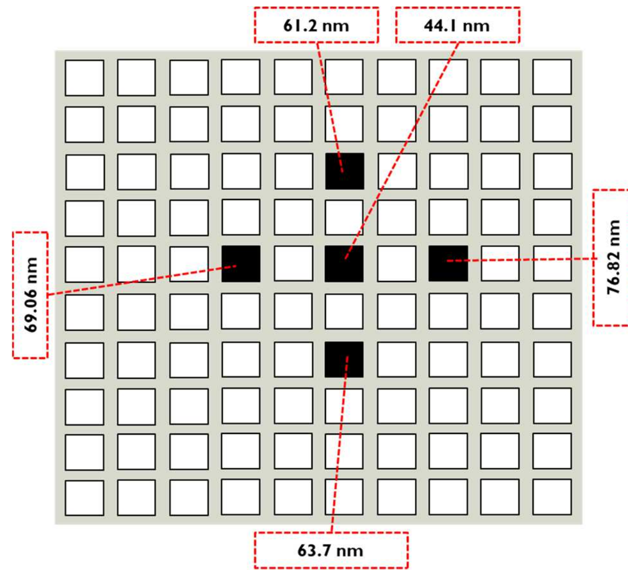


Figure 5.17: SOG film thicknesses on 5 dies after etching.

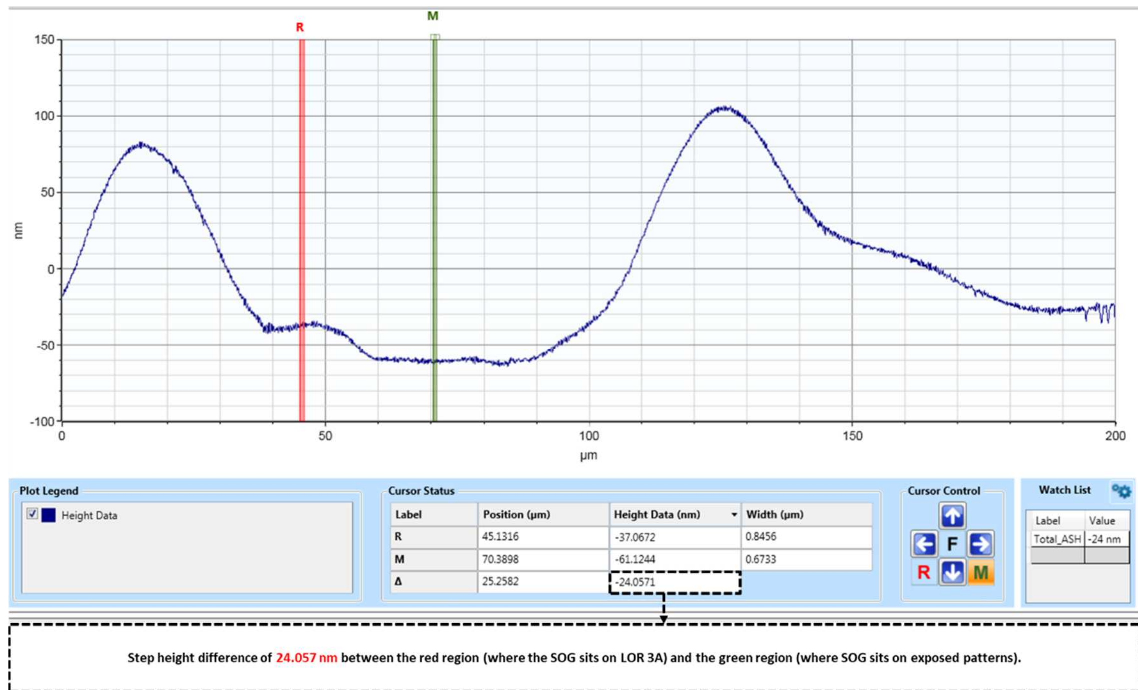


(a)

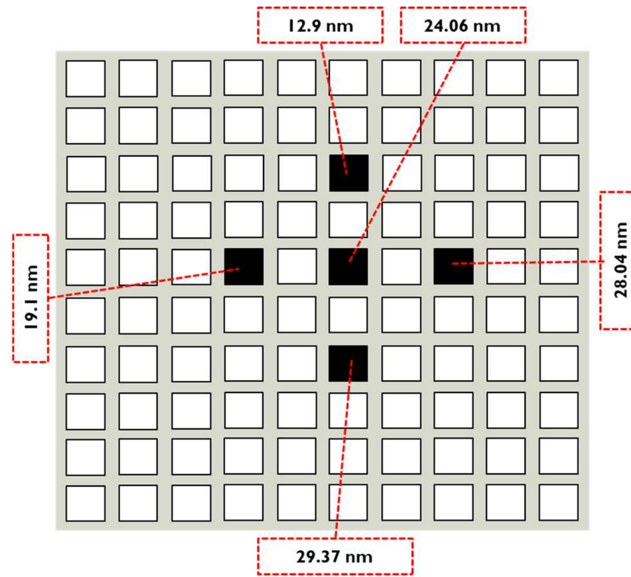


(b)

Figure 5.18: SOG film profile before etching on the (a) centermost die, (b) SOG film profile for all 5 dies- centermost die and 2nd dies to the right, left, above and below it.



(a)



(b)

Figure 5.19: SOG film profile after etching on the (a) centermost die, (b) SOG film profile for all 5 dies- centermost die and 2nd dies to the right, left, above and below it.

Another point to note is that it is only possible to measure SOG and LOR 3A thickness in locations where the layers sit right over the silicon and not over the metal patterns because of two reasons. Firstly, if the polished silicon wafer underneath is not the only reflector and if there are patterns in the area where the thickness is measured then the TiN ARC, Al-5Cu, Ti and the silicon wafer all act as perfect reflectors thereby making it difficult to measure the layer thicknesses. Secondly, considering each of the layers in the patterns there are a total of 6 layers that are measured and reflectometry fails for more than 3 layers. But, the SOG thickness over electrode patterns can be calculated analytically using equations 5.1 and 5.2 before SOG etch-back. The variables in equations 5.1 and 5.2 are depicted in Fig. 5.21.

$$h_{over\ metal\ stack} = \left(h_{step} + h_{over\ Si}\right) - h_{stack} \quad 5.1$$

$$h_{over\ Si} = (h_{LOR\ 3A\ over\ Si} + h_{SOG\ over\ Si}) \quad 5.2$$

where

$h_{over\ metal\ stack}$ = SOG film stack thickness over metal patterns.

h_{step} = step coverage across metal pattern as measured by profilometer.

$h_{over\ Si}$ = SOG and etched LOR 3A total thickness over Si wafer.

h_{stack} = height of the patterns from the Si substrate (740 nm).

$h_{LOR\ 3A\ over\ Si}$ = etched LOR 3A thickness over Si wafer.

$h_{SOG\ over\ Si}$ = SOG thickness over Si wafer.

Now, if $h_{over\ metal\ stack}$ is calculated after SOG etch-back and comes to be negative, this means that the electrode is exposed as distance cannot be a negative value.

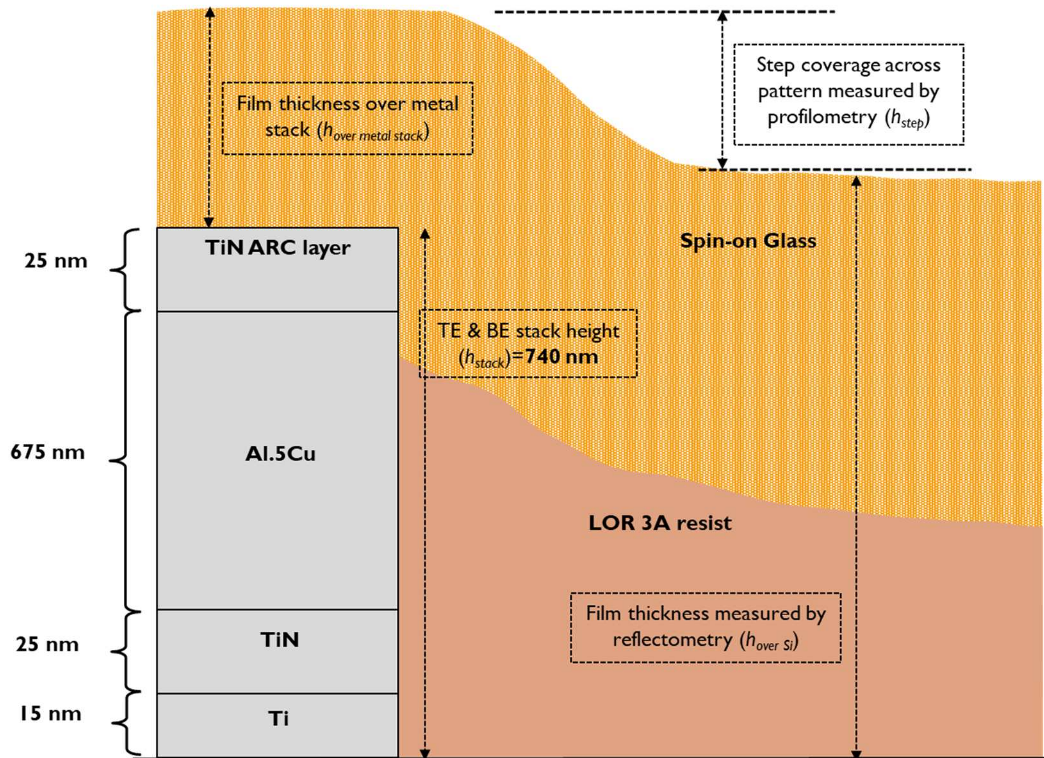


Figure 5.20: SOG and LOR 3A profile over a pattern before performing SOG etch-back.

6 CONCLUSION AND FUTURE WORK

In this thesis, a resist and SOG based planarization recipe was developed for planarizing Neuromorphic CMOS Chips with a TiN/Ti/Al-5Cu/TiN ARC topography of height 740 nm. Only lithography and dry etching were used in the processing of this recipe. Firstly, LOR 3A was spun at 3000 RPM for 30 seconds and baked by ramping the temperature from 50°C to 200°C in 4 steps and then cooling down the substrate in the exact reverse order to reach a height of 400 nm per layer. 18 such layers of LOR 3A were stacked on top of one another up to a maximum height of 7150 nm. Then, the LOR 3A film stack was etched back anisotropically in the presence of oxygen and argon plasma for 42 minutes (varies with etch rate) to reach a height of 700 nm. This was followed by spinning SOG on top of the etched LOR 3A at a speed of 2000 RPM for 30 seconds. Then, the SOG film was baked by ramping the temperature from 50°C to 160°C at a rate of 9.25°C/minute and letting it bake at 160°C for 5 minutes before finally ramping down the temperature in exactly the reverse manner to reach a height of 1225 nm per layer. 2 such SOG layers were stacked on top of one another up to a total height of 2450 nm. Finally, the SOG film stack was etched back anisotropically using oxygen and fluoroform gases for 24 minutes (varies depending on etch rate) to reach a height of 40 nm just exposing the top of the TiN ARC layer in the TiN/Ti/Al-5Cu/TiN ARC electrode stack. The material characterization was carried out between each process step using reflectometry to measure film thickness and profilometry to measure the step coverage across patterns. It was found that the final LOR 3A plus SOG film stack had a total non-uniformity of approximately 22.7 nm. Additionally, the photolithographic mask needed to expose the CBRAM layers to be

deposited on the planarized metal stacks has also been designed. There are two masks, one for the Ag anode and the other for the Ag-$GeSe_3$ chalcogenide.

Future work would involve forming the Ag/$GeSe_3$/Ti CBRAM device on these planarized electrodes. This would require processing three CBRAM layers in this order- the chalcogenide electrolyte ($GeSe_3$), a thin dopant layer (Ag) and a thick anode layer (Ag). The existing CBRAM deposition recipe might need to be tweaked to avoid too much mechanical or thermal stress on the SOG film. Once this is completed, the same planarization plus CBRAM recipe can be processed onto wafers with CMOS layers to form a 1T1R configuration.

However, a few challenges remain that need to be overcome for the final RRAM processing on top of the CMOS chips to work. An obvious and immediate challenge is the adjustment of the established CBRAM processing recipe to accommodate the SOG layer. The SOG is very susceptible to cracking upon application of mechanical and thermal stress. Additionally, the SOG can serve as a significant source of defects for the $GeSe_3$ layer to be deposited on top of it. Similarly, the CBRAM layers are deposited using lift-off method which would involve using chemical etchants. These chemical etchants must not etch the LOR 3A or SOG layers.

REFERENCES

[1] G. M. Moore, “Cramming more components onto integrated circuits With unit cost,” *Electronics*, vol. 38, no. 8, p. 114, 1965, [Online]. Available: https://newsroom.intel.com/wp-content/uploads/sites/11/2018/05/moores-law-electronics.pdf.

[2] J. Lai, “Mechanics, mechanisms, and modeling of the chemical mechanical polishing process,” Massachusetts Institute of Technology, 2001.

[3] K. C. Cadien and L. Nolan, *Chemical Mechanical Polishing Method and Practice*. Elsevier Inc., 2018.

[4] V. C. Venkatesh, I. Inasaki, H. K. Toenshof, T. Nakagawa, and I. D. Marinescu, “Observations on Polishing and Ultraprecision Machining of Semiconductor Substrate Materials,” *CIRP Ann. - Manuf. Technol.*, vol. 44, no. 2, pp. 611–618, 1995, doi: 10.1016/S0007-8506(07)60508-3.

[5] H. J. Levinson, “Overview of Lithography,” in *Principles of Lithography (3rd Edition)*, Third., 2011, p. 2.

[6] E. J. Walker, “Reduction of Photoresist Standing-Wave Effects by Post-Exposure Bake,” *IEEE Trans. Electron Devices*, vol. 22, no. 7, pp. 464–466, 1975, doi: 10.1109/T-ED.1975.18162.

[7] T. Batchelder and J. Piatt, “Bake effects in positive photoresist,” *Solid State Technol.*, vol. 26, no. 8, pp. 211–217, Jan. 1983, doi: 10.1016/0026-2714(84)90567-5.

[8] A. R. Barron, “Photoresist composition,” in *Chemistry of Electronic Materials*, 2011, pp. 150–151.

[9] S.-C. Chang and J. M. Kempisty, “Lift-off Methods for MEMS Devices,” *MRS Proc.*, vol. 729, p. U2.3, Feb. 2002, doi: 10.1557/PROC-729-U2.3.

[10] B. Loechel and Maciossek Andreas, “Surface microcomponents fabricated by UV depth lithography and electroplating,” in *Micromachining and Microfabrication Process Technology*, 1995, p. 174, doi: 10.1117/12.221275.

[11] K. Y. Lee *et al.*, “Micromachining applications of a high resolution ultrathick photoresist,” *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct. Process. Meas. Phenom.*, vol. 13, no. 6, pp. 3012–3016, 1995, doi: 10.1116/1.588297.

[12] Kayaku Advanced Materials, “LOR and PMGI Resists for Bi-layer Lift-off Processing.” pp. 1–8, 2020, [Online]. Available: https://kayakuam.com/products/pmgi-lor-lift-off-resists/.

[13] Kayaku Advanced Materials, "PMMA and Copolymer." pp. 1–7, 2020, [Online]. Available: https://kayakuam.com/products/pmma-positive-resists/.

[14] J. M. Moran and D. Maydan, "High resolution, steep profile resist patterns," *J. Vac. Sci. Technol.*, vol. 16, no. 6, pp. 1620–1624, 1979, doi: 10.1116/1.570256.

[15] J. H. Bruning, "Optical Imaging for Microfabrication," *J. Vac. Sci. Technol.*, vol. 17, no. 5, pp. 1147–1155, 1980, doi: 10.1116/1.570631.

[16] M. Hatzakis, B. J. Canavello, and J. M. Shaw, "Single-step optical lift-off process," *IBM J. Res. Dev.*, vol. 24, no. 4, pp. 452–460, 1980, doi: 10.1147/rd.244.0452.

[17] J. Salmi, J. Knuutila, H. Seppä, and P. Immonen, "Thin film process for Nb/NbOx/(Pb-In-Au) Josephson junction devices," *Thin Solid Films*, vol. 126, no. 1–2, pp. 77–81, Apr. 1985, doi: 10.1016/0040-6090(85)90178-6.

[18] "Planarization." https://www.eesemi.com/planarization.htm (accessed Apr. 04, 2021).

[19] M. Shen *et al.*, "Etch planarization - A new approach to correct non-uniformity post chemical mechanical polishing," in *25th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC 2014)*, 2014, pp. 423–427, doi: 10.1109/ASMC.2014.6846968.

[20] W. W.-Y. Lee, "Global planarization method using plasma etching," US5953578A, 1999.

[21] A. (Gatan I. . Pakzad, "Argon ion polishing of focused ion beam specimens in PIPS II system." https://www.gatan.com/argon-ion-polishing-focused-ion-beam-specimens-pips-ii-system (accessed Apr. 05, 2021).

[22] W. (Leica M. Grünewald, "Ion Beam Polishing of Sample Surfaces - Sample Preparation for SEM," 2016. https://www.leica-microsystems.com/science-lab/ion-beam-polishing-of-sample-surfaces-sample-preparation-for-sem/.

[23] V. V. Wong, A. Yasaka, and H. I. Smith, "Resist planarization over topography using ion implantation," *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct. Process. Meas. Phenom.*, vol. 13, no. 6, pp. 2797–2800, 1995, doi: 10.1116/1.588268.

[24] S.-C. Chien, C.-C. Hsue, and Y.-J. Liu, "Spin-on-glass planarization process with ion implantation," US5429990A, 1995.

[25] V. Y. Vasilyev, *Borophosphosilicate glass thin films in electronics*. Nova Science Publishers, 2013.

[26] D. S. Gardner, "Copper Reflow Process," US6599828B1, 2003.

[27] H. T. Baker, M. Ghafghaichi, R. C. Stevens, and H. Wimpfheimer, "Planarizing insulative layers by resputtering," US4007103A, 1977.

[28] B. Singh, O. Mesker, and D. Devlin, "Deposition of planarized dielectric layers by biased sputter deposition," *J. Vac. Sci. Technol. B Microelectron. Process. Phenom.*, vol. 5, no. 2, pp. 567–574, 1987, doi: 10.1116/1.583950.

[29] T. Mogami, M. Morimoto, H. Okabayashi, and E. Nagasawa, "SiO2 planarization by two-step rf bias-sputtering," *J. Vac. Sci. Technol. B Microelectron. Process. Phenom.*, vol. 3, no. 3, pp. 857–861, 1985, doi: 10.1116/1.583116.

[30] Y. Homma, S. Tunekawa, A. Satou, and T. Terada, "Planarization Mechanism of RF□Biased Al Sputtering," *J. Electrochem. Soc.*, vol. 140, pp. 855–860, 1993, doi: 10.1149/1.2056173.

[31] F. Atiquzzaman, "Chemical Mechanical Planarization of Electronic Materials," University of South Florida, 2012.

[32] B. Suryadevara, Ed., *Advances in Chemical Mechanical Planarization (CMP)*, 1st ed. ProQuest Ebook Central, 2016.

[33] J. Seo, "A review on chemical and mechanical phenomena at the wafer interface during chemical mechanical planarization," *J. Mater. Res.*, pp. 1–23, Sep. 2020, doi: 10.1557/jmr.2020.215.

[34] M. Krishnan, J. W. Nalaskowski, and L. M. Cook, "Chemical mechanical planarization: Slurry chemistry, materials, and mechanisms," *Chem. Rev.*, vol. 110, no. 1, pp. 178–204, 2010, doi: 10.1021/cr900170z.

[35] L. K. White, "Planarization Properties of Resist and Polyimide Coatings," *J. Electrochem. Soc.*, vol. 130, no. 7, pp. 1543–1548, 1983, doi: 10.1149/1.2120029.

[36] P. Chiniwalla *et al.*, "Multilayer planarization of polymer dielectrics," *IEEE Trans. Adv. Packag.*, vol. 24, no. 1, pp. 41–53, 2001, doi: 10.1109/6040.909624.

[37] K. Nishimura, L. Stecker, T. Afentakis, and K. Ulmer, "Organic semiconductor transistor with epoxy-based organic resin planarization layer," US9023683B2, 2014.

[38] S. W. Kirtley and G. S. Wooster, "Polymeric boron nitrogen dopant," US4578283A, 1984.

[39] M. N. Kozicki and W. C. West, "Programmable metallization cell structure and method of making same," US5896312A, 1999.

[40] N. Chamele, "Lateral Ag Electrodeposits in Chalcogenide Glass for Physical Unclonable Function Application," Arizona State University, 2017.

[41] M. N. Kozicki, “Dendritic structures and tags as physical unclonable function for anti-counterfeiting,” EP2998949A1, 2018.

[42] “Spin-on Glass NDG-7000R.” Desert Silicon, p. 2, 2000, [Online]. Available: http://desertsilicon.com/spin-on-glass/.

[43] J. M. Oldale, J. Rennie, and S. R. Elliott, “A comparative study of silver photodoping in chalcogenide films by means of extended X-ray absorption fine structure and kinetics measurements,” *Thin Solid Films*, vol. 164, pp. 467–473, 1988, doi: 10.1016/0040-6090(88)90178-2.

[44] D. Y. Cho, I. Valov, J. Van Den Hurk, S. Tappertzhofen, and R. Waser, “Direct observation of charge transfer in solid electrolyte for electrochemical metallization memory,” *Adv. Mater.*, vol. 24, no. 33, pp. 4552–4556, 2012, doi: 10.1002/adma.201201499.