Thin Silicon Heterojunction Solar Cells

By

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ABSTRACT

Crystalline silicon (c-Si) covers more than 85% of the global photovoltaics (PV) industry and has sustained a nearly 30% year-over-year growth rate. Continued cost and capital expenditure (CAPEX) reductions are needed to sustain this growth. Using thin silicon wafers well below the current industry standard of 160 μm can reduce manufacturing cost, CAPEX, and levelized cost of electricity. Additionally, thinner wafers enable more flexible and lighter module designs, making them more compelling in market segments like building-integrated photovoltaics, portable power, aerospace, and automotive industries. Advanced architectures and superior surface passivation schemes are needed to enable the use of very thin silicon wafers. Silicon heterojunction (SHJ) and SHJ with interdigitated back contact solar cells have demonstrated open-circuit voltages (V_{OC}) surpassing 720 mV and the potential to surpass 25% conversion efficiency. These factors have led to an increasing interest in exploring SHJ solar cells on thin wafers.

In this work, the passivation capability of the thin intrinsic hydrogenated amorphous silicon layer is improved by controlling the deposition temperature and the silane-to-hydrogen dilution ratio. An effective way to parametrize surface recombination is by using surface saturation current density (J_{0S}). A notable J_{0S} of 0.6 fA/cm^2 is achieved on textured wafers for wafer thicknesses ranging between 40 and 180 μm which is an order of magnitude lesser compared to the prevalent industry standards. Implied open-circuit voltages over 760 mV were accomplished on SHJ structures deposited on n-type silicon wafers with thicknesses below 50 μm. An analytical model is also described for a better understanding of the variation of the recombination fractions for varying substrate thicknesses. The potential of using very thin wafers is also established by manufacturing SHJ solar cells, using industrially pertinent

processing steps, on 40 μm thin standalone wafers while achieving maximum efficiency of 20.69%. It is also demonstrated that 40 μm thin SHJ solar cells can be manufactured using these processes on large areas (>120 cm^2). An analysis of the percentage contribution of current, voltage, and resistive losses are also characterized for the SHJ devices fabricated in this work for varying substrate thicknesses.

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1. INTRODUCTION

Global energy production and storage are some of the most important issues of the current age. The standard of living is directly proportional to the amount of energy consumed per capita which necessitates more energy production. This demand is constantly rising due to the growth in population and improvement in the standard of living in the developing world and is expected to increase by 60% by 2040 when compared to the demand in 2015 [1]. Fossil fuels are still the primary source of energy resources. They contribute to over 63% of the world's electricity production and greater than 84% for world energy production, figure 1 (a) [2]. Fossil fuels are constantly depleting due to exhaustive usage and their use for the production of energy creates carbon dioxide which is one of the main greenhouse gas contributing to global warming [3]. Global warming has extremely detrimental effects on our planet and there is an immediate need for alternative renewable and sustainable resources. A pathway for decarbonizing the energy production sector is to deploy economically feasible technologies to enable a sustainable and clean energy future. Although the demand has risen for all sources of energy over the years scaling up electricity production through renewables is crucial towards meeting the aims outlined in the Paris Agreement [4].

Solar energy is one such inexhaustible resource and photovoltaics (PV) is an elegant and sustainable method that has the potential to replace fossil fuels for energy production and cut down on greenhouse gas emissions [5]. Solar energy production is expected to contribute around 30% of the global electricity demand produced by renewables by 2050 [5]. Some outlooks even predict 20% of global primary energy demand will be generated by photovoltaics (PV) by 2050 [6].

PV technology was very small and developed slowly at the beginning, even though the technology was robust, reliable, and long-lasting. It is only in recent years that the PV industry has experienced an enormous change, with a remarkable increase in manufacturing capacities. The total installed capacity for Photovoltaics has grown at an average rate of greater than 30% per year in the last several years [1], [6]. Market prices for PV modules have almost reduced by 10% and solar cell costs have reduced by 20% in the year 2019 [6]. PV technology is constantly evolving with the main emphasis being on improving energy conversion efficiency

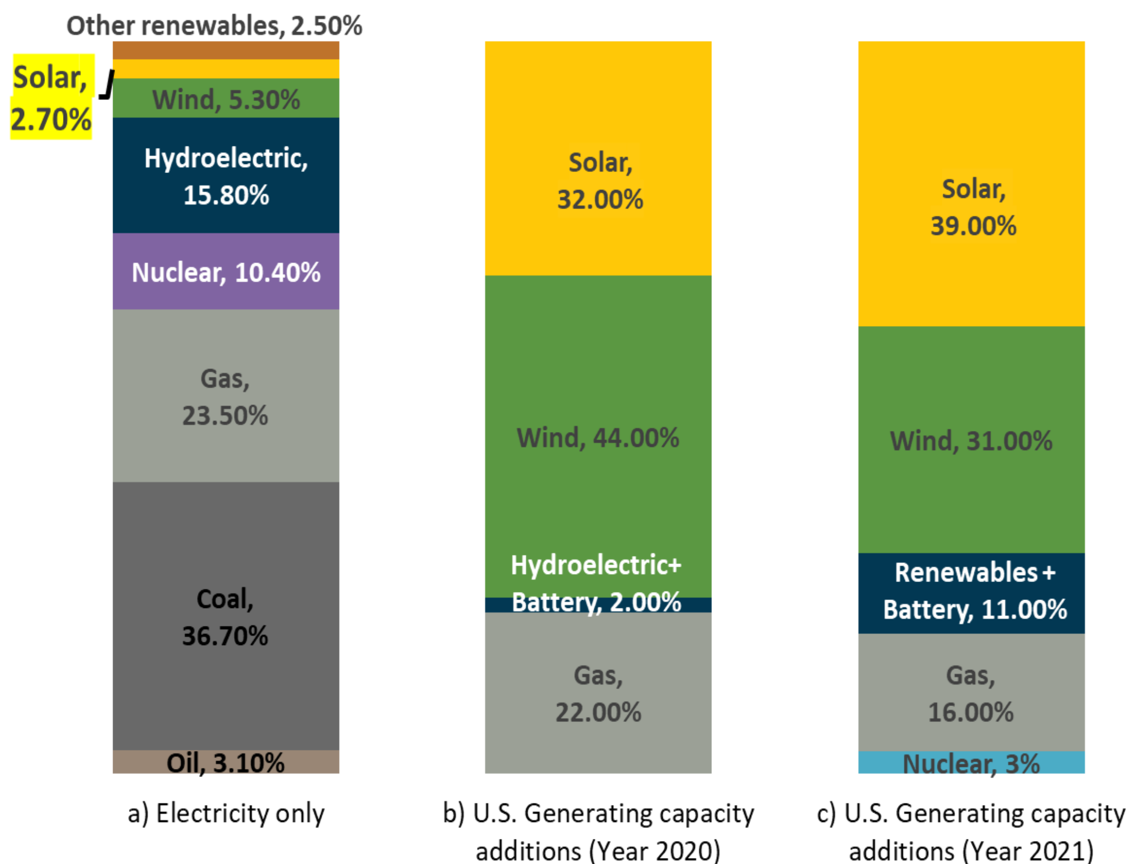

Figure 1 a) Contribution of Various Conventional and Renewable Sources of Energy for Global Electricity Production. Source: BP Statistical Review of World Energy (2020). *Other Renewables Include Geothermal, Biomass, Wave, and Tidal Energy. b), c) Net US Electricity Generating Capacity Additions for year 2020 and 2021. Source: U.S. Energy Information Administration, Annual Energy Outlook 2020 and 2021.

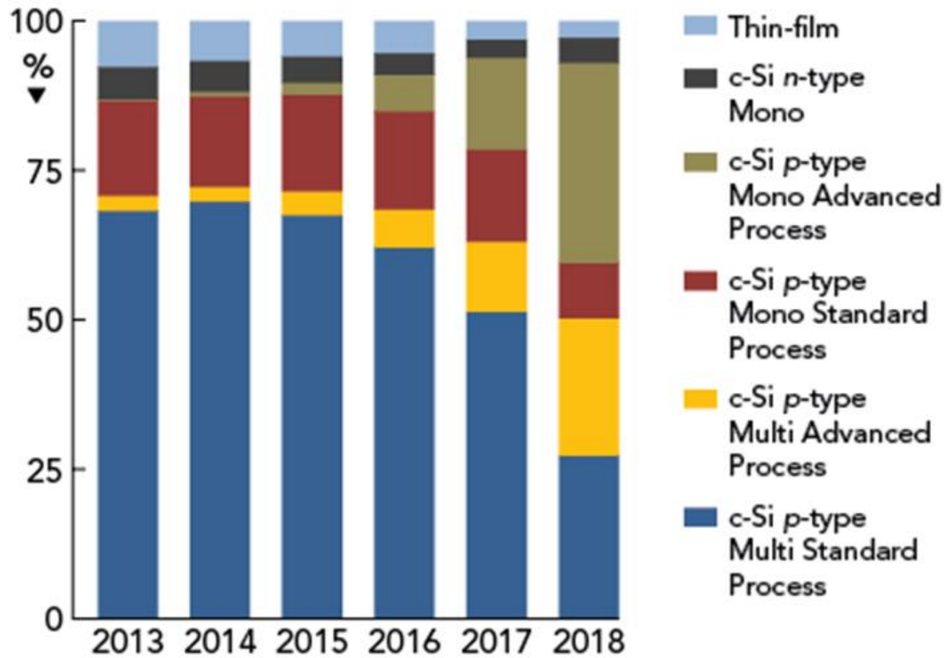

Figure 2: Annual PV Production Share by Different Categories of Solar Cell Technologies, Processes and Wafer Types Used. Silicon Solar Cells Have Greater than 90% of the Market Share. Source: PV-TECH & Solar Media Ltd, Oct 2018.

and manufacturing cost reduction. Out of the many different PV technologies that exist, silicon based solar cells are considered the most mature and have been established as the most dominant technology, figure 2.

1.1 Crystalline Silicon Solar Cells

Crystalline silicon (c-Si) currently dominates the PV market with a greater than 90% share in total production and particularly mono-crystalline technology contributes to around 66% of total production, figure 3 [6]. The properties of crystalline silicon and the idea for silicon based photovoltaic devices were first discovered in 1941 at Bell Laboratories [7]. The first c-Si solar cell was developed at the lab in New Jersey, where conversion of solar energy to electricity was demonstrated on silicon p-n junctions [8]. The solar cells developed could

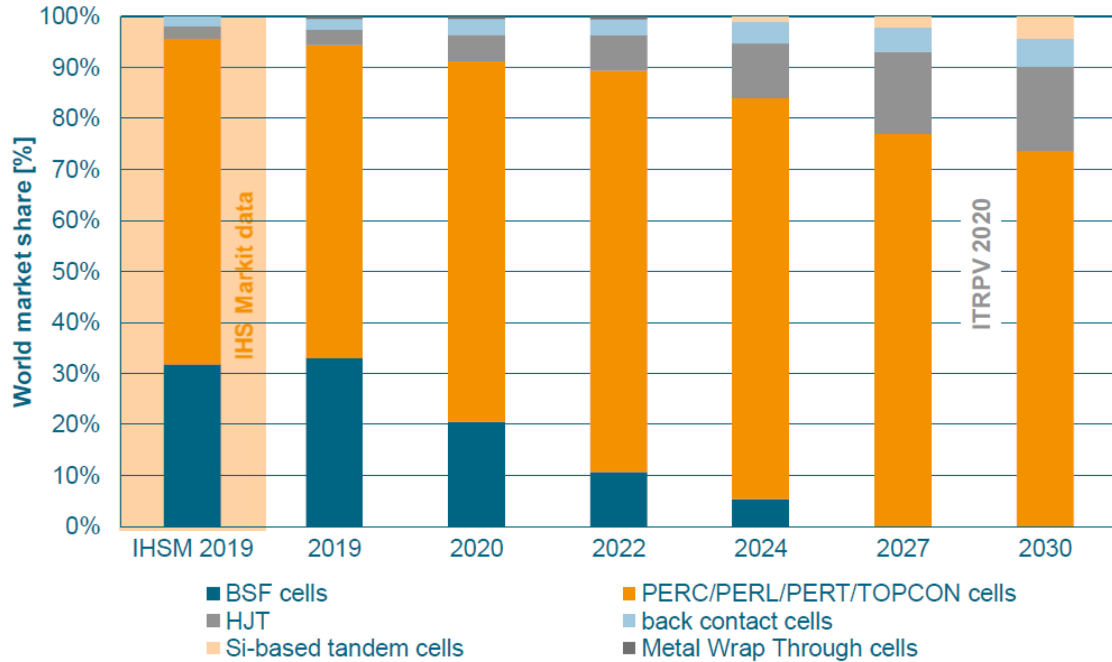

Figure 3: World Market Share for Different c-Si Solar Cell Technologies and Extrapolation of Demand to Year 2030. Source: ITRPV 2020 [6].

deliver power at a rate of 60 watts per square meter of the silicon surface, which is about 6% efficiency [8]. Ever since then there has been a rapidly rising interest in solar cell manufacturing using c-Si. The best commercially available c-Si modules can now achieve 24.4% efficiency and manufacturers, like Kaneka, are targeting even higher targets by 2030 [9]. The main reason for the dominance of c-Si based solar cells is the stability and abundance of silicon. The physical properties of silicon have also been well established due to its extensive use by the electronics industry for high-grade semiconductor devices, which helps reduce the price of solar cells. Due to these favorable properties of silicon, there is a high interest in c-Si based solar cells.

1.2 Motivation

During the last several decades novel technological advancements played a key role in improving the c-Si solar cell power conversion efficiencies. For solar energy to be more competitive compared to conventional and other renewable energy sources, there is a constant need to drive the production costs lower to enable large-scale industrialization of c-Si PV. Traditional multi and mono-crystalline silicon solar cells still form the major part of industrial production and have achieved 19% and >20% respectively in these production lines [6]. Research and development are being continuously carried out to further enhance solar cell efficiencies, reduce manufacturing costs, and achieve PV grid parity. The first ever silicon solar cell structure to break the 20% conversion barrier was achieved by UNSW back in the late 1980s [10]. This record efficiency has been boosted to 26.7%, which was achieved by Kaneka corporation, Japan in 2017. This acceleration of technological progress to improve conversion efficiency is one of the keys to reducing the cost of power generation.

Many c-Si solar cell architectures are currently being pursued to achieve very high efficiencies. In January 2019, LONGi Solar, China announced that it has achieved monocrystalline silicon passivated emitter rear cell (PERC) conversion efficiency that exceeds 24 percent for the first time using commercial wafer (M2) dimensions [11]. A conversion efficiency of 25.1% was achieved by Kaneka Corporation, Japan using Silicon Heterojunction (SHJ) (pseudonyms – HIT, HJT) solar cell technology in 2015 [12]. The combination of this SHJ technology and interdigitated back contact (IBC) has resulted in a new world record efficiency of 26.7% by Kaneka Corporation in 2017 [13]. Researchers at ISE, Germany have reported an efficiency of 25.8% using a new solar cell structure that uses tunnel oxide

passivated contacts (TOPCon) [14]. An efficiency of 26.1% was also achieved at ISFH, Germany by using polycrystalline Si (poly-Si) on oxide junctions (POLO) as an approach for passivating contacts [15]. Table 1 shows a detailed comparison of various device characteristics for different solar cell architectures that have very high conversion efficiencies (>25%). According to the latest International Technology Roadmap for Photovoltaics, SHJ technology will gain significant market share over back surface field (BSF) cells, figure. 3. SHJ and IBC solar cells will become more important as they lead to new opportunities in realizing silicon based tandem cells which show great potential for achieving even higher conversion efficiencies.

Table 1: Comparison of Device Characteristics of Different c-Si Solar Cell Architectures Measured Under the Global AM1.5 Spectrum (1000 W/m^2) at 25°C.

	PERC [16]	**POLO-IBC** [15]	**TOPCON** [17]	**TOPCON** [17]	**SHJ** [12]	**IBC** [13]
Voltage (mV)	687.9	727	732.3	724.1	738	738
J_{SC} (mA/cm^2)	41.81	42.6	42.05	42.87	40.8	42.65
Fill Factor (%)	82.83	84.3	84.3	83.1	83.5	84.9
Efficiency (%)	23.83	26.1	26	25.8	25.1	26.7
Area (cm^2)	244.43	4	4	4	151.9	79
Wafer type	P-type	P-type	P-type	N-type	N-type	N-type
Surface passivation	SiN_x	SiN_x, Al_2O_3	Al_2O_3	Al_2O_3	i-a-Si	i-a-Si

1.2.1 Silicon Heterojunction Solar Cell

Standard SHJ solar cell, like any other solar cell consists a combination of p-type and n-type materials. Amorphous and crystalline silicon are the main materials used in this device. The

first heterojunction device using amorphous silicon (a-Si) and c-Si stacked solar cell was designed in 1983 having efficiencies more than 12% [18]. The cell has a wide bandgap material at the top and a narrow bandgap at the bottom and triggered further investigation into the incorporation of a-Si in solar devices. A major milestone was achieved by Sanyo when it introduced a thin undoped buffer layer of a-Si between the doped emitter and the substrate, the Heterojunction with Intrinsic Thin-layer (SHJ/HIT) to reduce the surface defects. Efficiencies as high as 18% were achieved by these structures [19]. To reach the full device potential of the SHJ cell, the surface recombination must be minimal. Insertion of a wide band gap material like a-Si separated the highly recombinative metal contacts from the crystalline surface. Intrinsic hydrogenated amorphous Silicon (i-a-Si:H) of only a few nanometer thickness was found to be a promising candidate because of its low concentration of defects. These results motivated a lot of research groups to develop Sanyo's SHJ structure. The best efficiencies were obtained when a similar buffer layer was used as a passivating back contact. The introduction of the buffer layer improvised on every important parameter for a solar cell, but the open-circuit voltage (V_{oc}) benefitted the most. It was the use of a-Si that led to record values for V_{oc} and high efficiencies of SHJ cells.

SHJ solar cells have been attracting a growing amount of interest year over year due to the following advantages:

(1) Very high open-circuit voltage: both the large band bending between amorphous Si and crystalline Si and the excellent surface passivation of crystalline Si surface by intrinsic amorphous Si result in a high open-circuit voltage and a high conversion efficiency.

(2) low temperature process: low temperature process can not only save energy, but also prevent any degradation of bulk quality that happen with high temperature cycling process in low-quality silicon materials such as solar grade crystalline Si.

(3) good stability: n-type silicon wafers are used as the substrate without light-induced degradation. Additionally, a much better temperature coefficient can be obtained for HIT solar cells compared with conventional diffused cells.

(4) structural symmetry: compared to conventional crystalline silicon solar cells, the symmetrical structure reduces the mechanical stress, and therefore the thickness of the cell and the production cost can be reduced greatly. Meanwhile, the bifacial modules consisting of such symmetrical HIT cells can absorb light from double sides and thus improve the generating capacity.

Due to these benefits, there has been a marked increase in the research and development of SHJ solar cells. An analysis of the production costs of this technology has also been reported which sheds more light on various areas that can be improved [20]. The division of various solar cell architecture production costs can be seen in figure 4. A silicon wafer costs around 0.23 USD per Watt-peak (W_P) for a standard diffused junction solar cell [20]. This is greater than 60% of the total solar cell production costs. For a standard SHJ cell, the silicon wafer cost has been estimated to be around 0.19-0.22 USD per Watt-peak (W_P) which is around 55 to 65 % of the total solar cell production costs [20].

A recent study in 2020 [21] reported the cost of making PV Modules normalized to its power output. Specific contributions in the supply chain of PV manufacturing are broken down into: poly Si production, ingot growth and wafering, cell processing and module assembly, figure 5. They report that the combined capex contribution of the poly-Si and wafering processes have persistently been above 50% over the past eight years and over 30% of the total module cost. One way to further reduce the costs of c-Si wafers is to reduce the current standard thickness of around 170 – 180 μm down to 80-100 μm range [6], [20]. It has also been reported that using advanced device concepts and 50 μm thin silicon wafers, manufacturing capital expenditure can be reduced by 48% and the total module cost by 28% [21]. According to the latest international technology roadmap for photovoltaics (ITRPV)

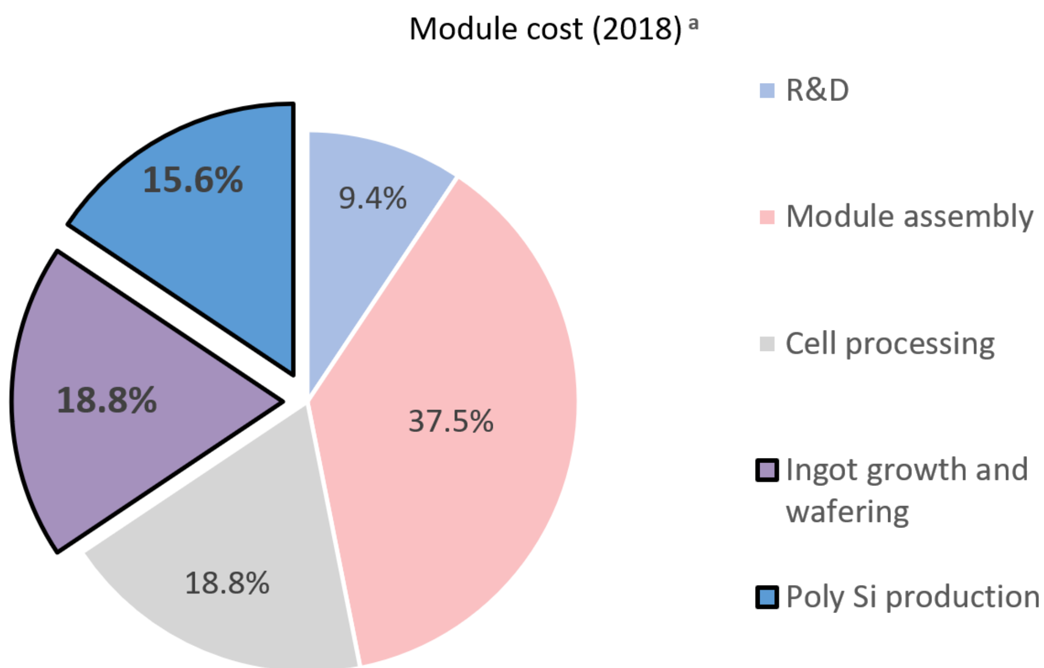

Figure 4: Module Cost for Monocrystalline Si PV Modules for 2018. Price Contributions for PV Manufacturing Are Broken down into Five Main Categories: Poly Si Production, Ingot Growth and Wafering, Cell Processing and Module Assembly. Data for Plot from [16].

there was 175 GW_P of global PV installation in 2019. 4% of this market share was made up of n-type CZ wafers which accounts for 7 GW_P [6]. A cell wafer cost of 0.22 USD/W_p leads to a market share of 1.54 billion USD. A 25% reduction in silicon wafer thickness leads to a cost reduction of 0.02-0.03 USD/Wp which can potentially lead to a market capitalization of 175 million USD. Additionally, thinner wafers enable more flexible and lighter module designs, making them more compelling in market segments like building integrated photovoltaics (BIPV) [22], portable power applications [23], [24] and aerospace and automotive industries [25]. These factors have led to an increasing interest in exploring SHJ solar cells using thin wafers.

Production of very thin silicon wafers also has setbacks due to kerf loss and yield of production. The current silicon wafer kerf loss of 75 μm is expected to reduce to 50 μm by 2030 [6]. Parallel improvement in the efficiencies of these SHJ solar cells can also drive down the total costs with respect to the total power generated. SHJ solar cells also require the use of

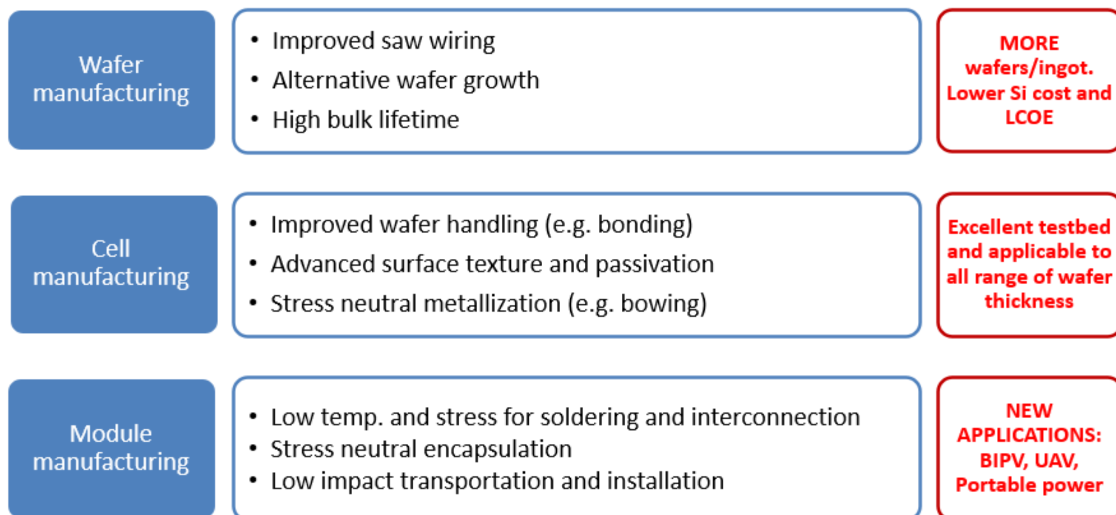

Figure 5: Specific Areas of Manufacturing That Require Considerable Improvement to Achieve High-efficiency Thin-PV Modules and Their Benefits in the Red Box Are Outlined.

specialized equipment. The use of transparent conductive oxides and low temperature silver paste adds to the cost of the SHJ solar cell. This leads to an increase in capital cost and the cost of PV modules. Multiple technology research and developments are required to enable the use of thin c-Si substrates for large-scale PV deployment. Some of the details with regards to manufacturing and their benefits are outlined in figure 5. Although there are multiple pathways to achieve economically sustainable production of SHJ cells, this thesis mainly concentrates on the objectives detailed below.

1.3 Research Objectives

As discussed in the previous sections a reduction in silicon wafer usage and improvement in the efficiency of SHJ solar cells to increase the power delivered per unit area per unit mass occupied by the PV system are a couple of ways to drive down production costs.

The main objectives of this thesis are to:

- Improve the surface passivation properties of the intrinsic amorphous silicon layer in silicon heterojunction solar cells to:
    - Enable very low surface saturation current density and high open-circuit voltages
    - Enable high efficiency on thin c-Si solar cells over large areas
- Evaluate the impact of these improvements for a wide range of substrate thicknesses
- Characterize the percentage contribution of device losses in comparison to the theoretical limit

The approach taken to achieve these objectives are:

- Develop a fabrication process for large area silicon heterojunction solar cells using substrate thicknesses down to 40 μm
- Explore certain factors influencing the device performance

1.4 Outline

This thesis developed the SHJ fabrication flow on large and small area 40 μm thick wafers which allowed SHJ solar cells to achieve > 740 mV and >20% efficiency. It was also demonstrated that the state-of-the-art a-Si process can be developed to achieve surface saturation current densities which are lower than 1 fA/cm^2. This work also explored the practical efficiency limit of silicon solar cells using thin solar-grade substrates and establishes that for surface saturation current densities below 0.2 fA/cm^2, the optimum wafer thickness is between 40 to 60 μm. This work also used a non-destructive diagnosis of bare-silicon wafers using a photoluminescence tool which can be used as a quality control step to verify the effectiveness of the surface cleaning process. An in-depth study was also done on the influence of laser-induced defects, treated as high recombination areas on the surface of SHJ solar cells, and their impact on the Current-Voltage (I-V) characteristics.

2. ASSESSING N-TYPE SILICON EFFICIENCY LIMIT

2.1 Recombination Mechanisms in Silicon

Recombination and generation of electron hole pairs is a continuous process in semiconductors, both optically and thermally. Thermodynamics defines that at equilibrium the generation and recombination rates are balanced so that the net charge carrier density of the semiconductor remains constant. The resulting probability of occupation of energy states in each energy band is given by Fermi–Dirac statistics.

An electron recombines with a hole and the energy is either released in the form of heat or light. The fundamental recombination mechanisms in crystalline silicon are:

- Radiative recombination
- Auger recombination

which cannot be mitigated by improving the material quality of Silicon or by optimizing the processing steps to fabricate a solar cell. In addition to these, we have defect assisted recombination in silicon

- Recombination due to traps/defects in the bulk
- Surface recombination

Trap assisted recombination in the bulk of the material can be greatly reduced by controlling the concentration of impurities in the silicon ingot or by reducing the thickness of the silicon wafer. Surface recombination, due to dangling bonds at the silicon surface, is generally reduced by the deposition of a surface passivation layer which deactivates the recombination-active defects due to the disruption of the material crystallinity. Reducing these

two recombination rates is one of the major challenges for improving the device characteristics of the SHJ solar cell.

When there is an excess of carriers the rate of recombination becomes greater than the rate of generation, driving the system back towards equilibrium. Carrier lifetime is defined as the average time it takes for a minority carrier to recombine and is the ratio of excess charge carrier density (Δn) and the net recombination rate (R). The effective lifetime (τ_{eff}) of a charge carrier is derived from the recombination processes listed above, which depend mainly on the nature and quality of the semiconductor (direct versus indirect band gap), doping level, and cell irradiance, and can be generally expressed as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{ta}} + \frac{1}{\tau_{S}} \tag{1}$$

where $\tau_{Auger,}$ $\tau_{Rad,}$ τ_{ta} and τ_{S} are the carrier lifetimes associated with Auger, Radiative, trap-assisted and surface recombination.

2.1.1 Radiative Recombination

Radiative recombination is a dominant mechanism observed in direct bandgap semiconductors. It is essentially the opposite process of photon absorption in which the energy of an electron-hole pair is lost as a photon of the same energy, figure 6. For silicon solar cells, which is an indirect bandgap semiconductor, a phonon is required in the radiative recombination process which makes it less probable to happen compared to the other recombination mechanisms. The recombination rate (R_{rad}) is directly proportional to the density of the free holes times free electrons and is given by:

$$R_{rad} = B(np - n_0 p_0) = B(np - n_{i,eff}^2) \tag{2}$$

where B is the coefficient of radiative recombination, n_0 and p_0 are the hole and electron density respectively in thermal equilibrium and $n_{i,eff}$ is the effective intrinsic carrier density. n and p is the total carrier density in the non-equilibrium state and is given by:

$$np = (n_0 + \Delta n)(p_0 + \Delta p) \tag{3}$$

where Δn and Δp is the electron and hole excess carrier density. Considering charge neutrality ($\Delta n = \Delta p$), the τ_{Rad} is then given by

$$\tau_{\text{Rad}} = \frac{\Delta n}{R_{rad}} = \frac{\Delta n}{B((n_0+\Delta n)(p_0+\Delta p)-n_i^2)} = \frac{1}{B(n_0+p_0+\Delta n)} \tag{4}$$

2.1.2 Auger Recombination

Auger recombination refers to a process involving three particles. In this mechanism an electron-hole pair recombine, and the energy generated is either transferred to an electron (eeh process) or a hole (ehh process), figure 6. The excess energy transferred to the particle is released as heat in the lattice (phonon) to achieve equilibrium. The Auger recombination rate R_{Auger} can be expressed as:

$$R_{Auger} = C_p\left(np^2 - n_{i,eff}^2 p_0\right) + C_n\left(n^2 p - n_{i,eff}^2 n_0\right) \tag{5}$$

where C_p and C_n are the Auger coefficients for ehh and eeh processes respectively. Because R_{Auger} is dependant on the cube of carrier concentration, it should become performance-limiting at high carrier injection rates. For high injection levels, where $\Delta n \gg N_d$, τ_{Auger} can be approximated to:

$$\tau_{Auger,hi} = \frac{1}{(C_n+C_p)\Delta n^2} \tag{6}$$

And for low injection levels, where $\Delta \ll N_d$, $\tau_{Auger,li} = \frac{1}{C_n N_d^2}$ for n-type silicon and $\tau_{Auger,li} = \frac{1}{C_p N_d^2}$ for p-type silicon

This traditional Auger theory is in good agreement with measured lifetimes of highly doped silicon (N_d >5×10^{18} cm^{-3}). For lower dopant concentrations, however, the predicted lifetimes significantly exceed the measured lifetimes.

A more recent recombination model is described below to present a more consistent picture of Auger recombination which is valid for all carrier densities [26]. It is based on the inclusion of the Coulomb attraction and repulsion, respectively, of electrons and holes and of electrons and electrons in calculating the Auger recombination rate. Further assessment by P. Altermat et al. [27] and Richter et al. [28] led to a better parametrization, which includes the radiative recombination component, and provides excellent accuracy to describe the upper limit of the minority carrier lifetime in crystalline silicon for a wide range of dopant densities, as well as a broad range of carrier injection levels. This parameterization also includes the more extensive model for band gap narrowing (BGN) that was published by Schenk in 1998 [29]. Its derivation is based on quantum mechanics and it accounts for dopant concentrations, carrier concentrations, and temperature.

The fundamental lifetime is given by:

$$\frac{\Delta n}{\tau_{fund}} = \frac{\Delta n}{\tau_{Auger}} + \frac{\Delta n}{\tau_{Rad}} = \frac{\Delta n}{(np - n_{i,eff}^2)(2.5\times10^{-31} g_{eeh} n_0 + 8.5\times10^{-32} g_{ehh} p_0 + 3\times10^{-29} \Delta n^{0.92})} + \frac{\Delta n}{\left(np - n_{i,eff}^2\right)(B_{rel} B_{low})} \quad (7)$$

with the enhancement factors

$$g_{eeh}(n_0) = 1 + 13\left\{1 - \tanh\left[\left(\frac{n_0}{N_{0,eeh}}\right)^{0.66}\right]\right\} \quad (8)$$

and $$g_{ehh}(p_0) = 1 + 7.5\left\{1 - \tanh\left[\left(\frac{p_0}{N_{0,ehh}}\right)^{0.63}\right]\right\} \quad (9)$$

and $N_{0,eeh} = 3.3 \times 10^{17} cm^{-3}$ and $N_{0,ehh} = 7 \times 10^{17} cm^{-3}$ and B_{low} is the radiative recombination coefficient for lowly doped and lowly injected silicon, 4.73×10^{-15} cm^3 s^{-1} [30] and B_{rel} is the relative radiative recombination coefficient [31], all derived for a temperature of 300 K.

2.1.3 Trap-Assisted Recombination in the Bulk

Trap-assisted recombination, in the bulk mainly occurs due to the presence of defects in the material which give rise to defect levels. An electron in transition between the valence and conduction band encounters a defect energy state in the forbidden region. A hole can then recombine with the electron at this level before the electron moves up into the conduction band, figure 6. The analysis of the dynamics involved in this process, the recombination rate involved with traps is dependent on the volume density of trapping defects and the energy of the trapping level and is given by:

$$R_{ta} = \frac{np - n_{i,eff}^2}{\tau_{n0}\,(p_0 + p_1 + \Delta n) + \tau_{p0}\,(n_0 + n_1 + \Delta n)} \quad (10)$$

where n_0 and p_0 are the equilibrium concentration of electrons and holes respectively, and τ_{n0} and τ_{p0} are lifetime parameters (for holes and electrons respectively) whose values depend on the type of trap and the volume density of trapping defects. The quantities n_1 and p_1 are parameters that introduce the dependency of the recombination rate on the trapping energy level (defect energy level) E_t as shown below:

$$n_1 = N_c e^{\left(\frac{E_t - E_c}{kT}\right)} \quad (11)$$

$$p_1 = N_v e^{\left(\frac{E_v - E_t}{kT}\right)} \quad (12)$$

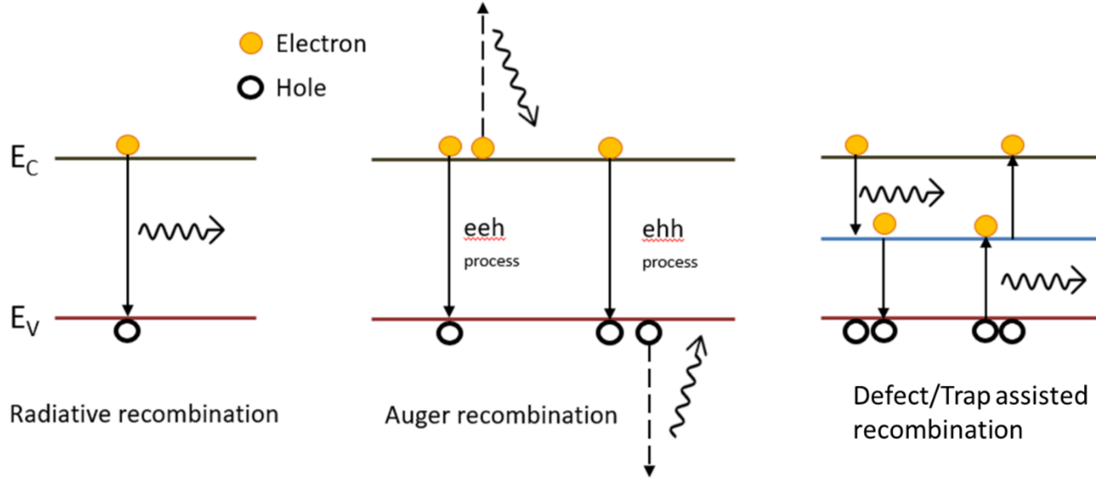

Figure 6: Schematic Illustration of the Different Recombination Mechanisms in Silicon Solar Cells - Radiative Recombination, Auger Recombination and Trap-Assisted Recombination

E_c and E_v are the energies of the conduction and the valence band edge, respectively, and N_c and N_v are the effective densities of states in the conduction and the valence band respectively. The time constants τ_{n0} and τ_{p0} for the capture of electrons and holes in the trap state is given by $\tau_{n0} = \frac{1}{N_t \sigma_n v_{th}}$ and $\tau_{p0} = \frac{1}{N_t \sigma_p v_{th}}$, where N_t is the defect concentration and σ_n and σ_p is the capture cross sections for electrons and holes respectively. The rate at which either carrier moves into a defect energy level is dependent on the difference of that level from either of the band edges. If the trap energy is close to either band edge, recombination is less likely as the carrier is likely to be re-emitted to the band edges rather than recombining. Therefore, trap energy levels near mid-gap act as very effective recombination centers. This can be modeled by using $E_t = (E_v - E_c)/2$ which leads to reduction of equation (11) and (12) to $n_1 = p_1 = n_{i,eff}$. The trap assisted effective lifetime for a mid-gap defect is given by:

$$\tau_{ta} = \frac{\Delta n}{R_{ta}} = \frac{\Delta n(\tau_{no}\left(p_0 + p_{i,eff} + \Delta n\right) + \tau_{po}\left(n_0 + n_{i,eff} + \Delta n\right))}{np - n_{i,eff}^2} \quad (13)$$

2.1.4 Surface Recombination

There is an abundance of defect levels at the surface of a semiconductor as the crystal lattice ends abruptly leading to surface dangling bonds. Large densities of surface states are continuously distributed in the forbidden gap. Similar to recombination statistics via a defect energy level in the bulk, the recombination rate at the surface can be expressed by the same. Since we have a large distribution of defect states spread over the band gap, the surface recombination rate for a particular energy level ($R(E)_S$) can be expressed as:

$$R(E)_S = \frac{(n_S p_S - n_i^2)dE}{\tau_{n0s}\,(p_S + p_1(E)) + \tau_{p0s}\,(n_S + n_1(E))} \tag{14}$$

where $\tau_{n0s} = \frac{1}{D_{it}(E)\sigma_n v_{th}}$, $\tau_{p0s} = \frac{1}{D_{it}(E)\sigma_p v_{th}}$, $D_{it}(E)$ is the defect energy dependent interface defect density and, n_s and p_s are the carrier concentrations at the surface. The total surface recombination (R_S) rate can be further reduced and expressed as an integral according to the equation:

$$R_S = v_{th}(n_S p_S - n_i^2) \int_{E_c}^{E_v} \frac{D_{it}(E)dE}{\frac{(p_S + p_1(E))}{\sigma_n} + \frac{(n_S + n_1(E))}{\sigma_p}} \tag{15}$$

The surface acts as a localized region of low carrier concentration which causes the carriers from the surrounding higher concentration regions to flow into this region. The surface recombination rate is thus limited by the rate at which minority carriers move towards the surface as expressed above. Generally, a parameter called the surface recombination velocity (S_{eff}), expressed in cm/s is used to specify the recombination at a surface and can be expressed as follows:

$$S_{eff} = \frac{R_S}{\Delta n} = \frac{1}{\Delta n} \int_{E_c}^{E_v} \frac{D_{it}(E)dE}{\frac{(p_{tot}(E))}{S_n} + \frac{(n_{tot}(E))}{S_p}} \tag{16}$$

where n_{tot} and p_{tot} is the total density of electrons (holes) at the interface, and S_p and S_n are the energy dependent S_{eff} for holes and electrons, respectively.

An alternative to S_{eff} is the use of a term called surface saturation current density (J_{0s}) introduced by Mcintosh et al. [32] which is analogous to the emitter saturation current density (J_{0e}) term used to model heavily doped emitters of diffused junction solar cells [33]. The surface recombination current is determined by:

$$J_{Surface,rec} = J_{0s}\left(\frac{n_s p_s}{n_{0s} p_{0s}} - 1\right) \tag{17}$$

where n_s and p_s are the concentration of electrons and holes at the surface in steady state conditions and n_{0s} and $n_{i,eff}$ p_{0s} are the concentrations at equilibrium. As an approximation we assume $n_{0s}p_{0s} = n_{i,eff}^2$. Similar to trap-assisted recombination statistics J_{0s} can be determined for a single defect level as:

$$J_{0s} = \frac{q n_{i,eff}^2}{\frac{p_s + p_1}{S_{n0}} + \frac{n_s + n_1}{S_{p0}}} \tag{18}$$

where S_{n0} and S_{p0} are the surface recombination velocity parameters given by $S_{n0} = D_{it}\sigma_n v_{th}$ and $S_{p0} = D_{it}\sigma_p v_{th}$ and $n_1 = n_{i,eff} e^{\left(\frac{E_t - E_c}{kT}\right)}$ and $p_1 = n_{i,eff} e^{\left(\frac{E_v - E_t}{kT}\right)}$ for a single defect energy level as described previously. The surface recombination rate can also be derived using J_{0s} in the form of the diode equation as:

$$qWR_S = J_{0s}\left[exp\left(\frac{V_d}{V_t}\right) - 1\right] \tag{19}$$

where V_d is the voltage bias. $V_t = \frac{k_b T}{q}$, where k_b is the Boltzmann constant and T is the temperature. Voltage bias or excess carrier density can be used as the parameter to vary to determine the effective minority carrier lifetime. To extract the excess carrier density Δn we vary the voltage bias parameter V_d by the equation:

$$np = (n_0 + \Delta n)(p_o + \Delta p) = n_{i,eff}^2 exp\left(\frac{qV_d}{k_bT}\right) \quad (20)$$

For n-type silicon wafer $n_0 = N_D$ and $p_0 = n_{i,eff}^2/N_D$. $n_{i,eff}$ is calculated by the equation:

$$n_{i,eff} = n_{i,0} exp\left(\frac{\Delta E_g}{2k_bT}\right) \quad (21)$$

where $n_{i,0}$ is intrinsic carrier concentration for Si at 300 K given by Altermatt et al. [34] and ΔE_g is the band gap narrowing derived according to Schenk [29]. This relation is solved iteratively, by varying voltage step by step, to determine Δn (V,n_0,p_o) and the corresponding radiative, auger, trap assisted and surface recombination rates according to equations (7), (13) and (19). Minority carrier lifetime can also be modeled similarly using the equations described in the above sections for varying excess carrier density as:

$$\frac{1}{\tau_{eff}} = \frac{\Delta n}{R_{Rad}} + \frac{\Delta n}{R_{Auger}} + \frac{\Delta n}{R_{ta}} + \frac{\Delta n}{R_S} \quad (22)$$

A comparison of the calculated minority carrier lifetime vs excess carrier density for two different wafer thicknesses, of 170 μm and 40 μm is illustrated in figure 7. The comparison is done by calculating the minority carrier lifetime for these two different substrate thicknesses by keeping the same bulk and surface recombination properties by keeping certain parameters constant. The fundamental lifetime is given by the black solid line in figure 7. The trap assisted recombination lifetime is obtained by setting the electron and hole capture lifetimes $\tau_{n0} = \tau_{p0} = 10\ ms$ in equation (13) so that the wafers with two different thicknesses have the same bulk characteristics. Minority carrier lifetime due to surface recombination is calculated by setting J_{0S} = 1 fA/cm^{-2}. As a result of the dependence of the total recombination rate on substrate thickness, the structure with a thickness of 40 μm thickness shows higher effect of

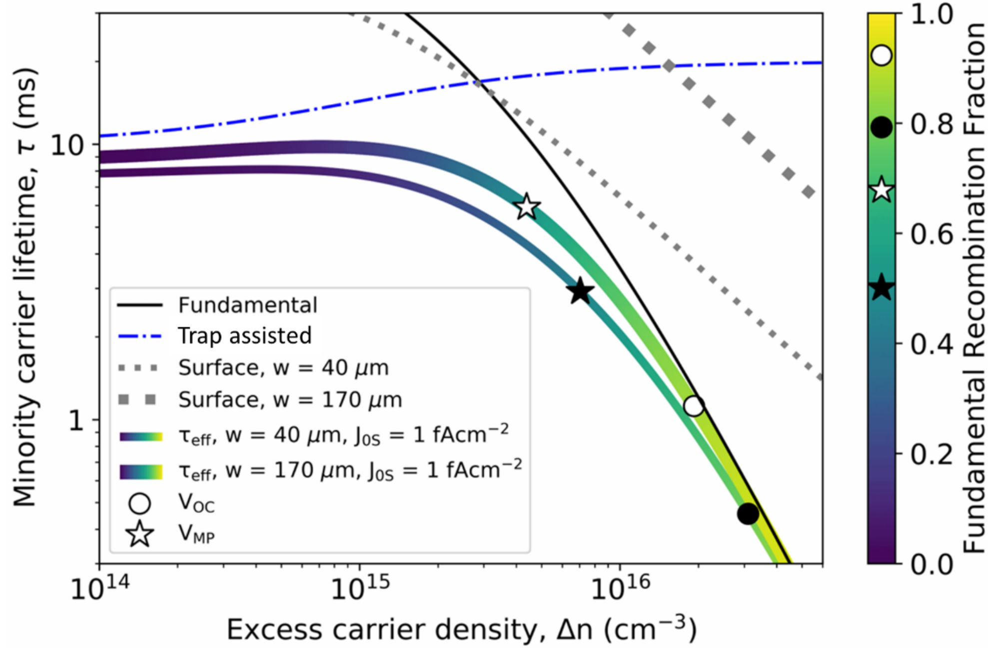

Figure 7: Effective Minority-carrier Lifetime of N-type Silicon Wafers of 170 µm and 40 µm Thickness, Trap-Assisted Lifetime of 10 ms and Bulk Resistivity of 3.55 Ω cm (1.3 x 10^{15} cm^{-3} dopant concentration), and Total J_{0S} (from both surfaces) of 1 fA cm^{-2}. Each Curve on the Plot Corresponds to a Different Recombination Mechanism as Mentioned in the Legend. The Color Bar Represents the Fraction of Fundamental (Auger + Radiative) Recombination. The Markers in the Color Bar Indicate the Fundamental Recombination Fraction at Maximum Power and Open-circuit Injections, Details of Which Will Be Discussed in Chapter 4.

surface recombination on the total recombination rate than the one with 170 µm. The impact of the surface is mainly observed at the maximum power point injection level, where the fundamental recombination fraction, represented by the color bar in figure 7, becomes less dominant.

2.2 Fundamental Efficiency Limit for Silicon

The maximum efficiency of silicon solar cells limited by the fundamental recombination properties of silicon was modeled by Richter et al. [35] The main variations in the work of

Richter et al. compared to the work of Kerr et al. [36] are the introduction of the new solar spectrum, updated optical properties of silicon, new parameters for free carrier absorption, improved parameterization of radiative and Auger recombination and also the effect of BGN. The general approach of modeling ideal silicon solar cell efficiency limits is to assume cells without surface and defect recombination, ideal front-side antireflection coating and ideal rear reflecting surfaces leading to no absorption or transmission losses [35]–[39]. The current density of an ideal silicon solar cell can be expressed as:

$$J = J_{ph} - J_{rec} \tag{23}$$

where J_{ph} is the photogenerated current density, J_{rec} is the recombination current density and for an ideal solar cell with the assumptions described in the above sections and considering no recombination from bulk and surface, J_{rec} can be expressed as

$$J_{rec} = qWR_{fund} \tag{24}$$

where q is the electronic charge, W is the thickness, and $R_{fund} = \Delta n/\tau_{fund}$ under the assumption of a narrow base, details of which are derived by Green [37].

J_{ph} for a particular thickness of silicon and for AM1.5G spectrum can be determined using the analytical solutions for the Lambertian light trapping scheme described by Green [40]. Richter et al. in their work for assessing the efficiency limit of silicon [35] also included free carrier absorption into account, as weakly absorbed sub-bandgap photons have a certain probability of being absorbed free carriers [38], to calculate the maximum possible J_{ph}. A phenomenon called photon recycling was also incorporated in as each radiative recombination event that generates a photon, has a probability of being reabsorbed by band-to-band transitions in case of very effective light-trapping [36]. Maximum efficiency can be calculated

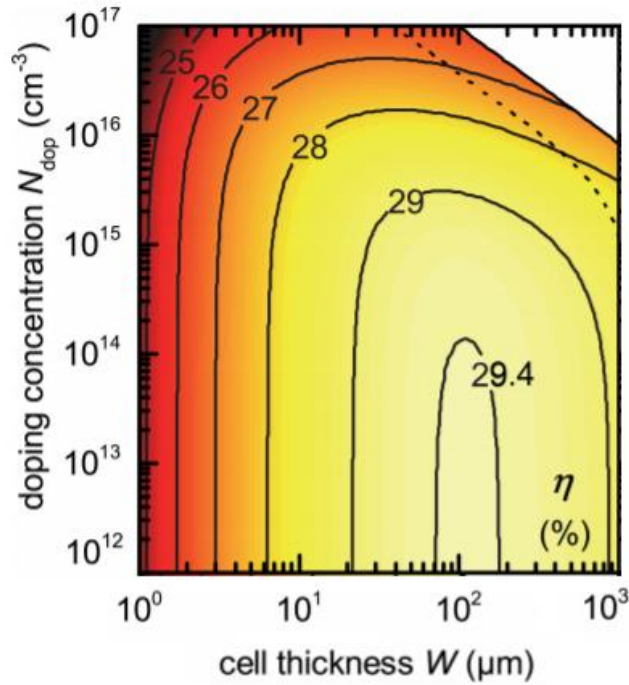

Figure 8: Limiting Efficiency of N-type Silicon Wafer for Varying Substrate Doping Concentration and Thickness. Figure Extracted from Reference [27]

from the expressions listed above by solving for the maximum power point which will determine the Fill Factor (FF) and V_{OC} and J_{SC} are calculated when J=0 and V=0, respectively. Applying these modeling parameters a maximum theoretical efficiency of 29.43% for a 110-μm-thick cell made of undoped Si was calculated by Richter et al.[34]. The variation of efficiency limit of n-type silicon with respect to its thickness and doping concentration can be seen in figure 7.

2.3 Efficiency Limit of Solar Grade Silicon Wafers

2.3.1 Trap-Assisted and Surface Recombination

Monocrystalline silicon wafers (mono c-Si) used for fabricating silicon solar cells are manufactured using the Czochralski (CZ) technology. As silicon growth technology keeps improving the number of defects present in silicon wafers can be reduced which will lead to

lower trap assisted recombination rates. A record 225 ms minority carrier lifetime has already been reported on an n-type float zone (FZ) silicon wafer [41]. The contribution of trap assisted recombination to the total recombination can also be reduced by decreasing the wafer thickness. For calculating the limiting efficiency for commercially viable solar-grade silicon we set the electron and hole capture lifetime $\tau_{n0} = \tau_{p0} = 10\ ms$ respectively in the trap assisted recombination equation that was described in equation (13). The recombination current for a particular thickness can be calculated as

$$J_{ta,rec} = qWR_{ta} = qW\frac{\Delta n}{\tau_{ta}} \tag{25}$$

where τ_{ta} is the trap assisted minority carrier lifetime. As detailed in the previous sections the surface recombination current can be modeled by defining a parameter called surface recombination velocity (S_{eff}):

$$J_{Surface,rec} = qS_{eff}\Delta n_d \tag{26}$$

where Δn_d is the excess carrier concentration near the surface. The recombination current can also be re-written using equation (19) as:

$$J_{S,rec} = J_{0s}\left[exp\left(\frac{V_d}{V_t}\right) - 1\right] = qWR_S \tag{27}$$

The total effective recombination current in a silicon solar cell can now be described as the sum of all the recombination currents discussed above:

$$J_{rec} = qW(R_{fund} + R_{ta} + R_S) \tag{28}$$

The total recombination for a particular voltage bias can be solved using the above equation. The maximum power point is obtained by iteratively solving for $P_{max} = max\ (J * V)$ which also gives us the efficiency of the solar cell. Figure 9 shows the conversion efficiency of silicon solar cells using n-type Si solar wafers and bulk resistivity of 3.55 Ω cm (1.3 x 10^{15} cm^{-3} dopant concentration) with varying surface saturation current density. Here J_{0s} is the total contribution from both front and back sides of the silicon wafer. For the n-type solar cells the optimum thickness is 100 to 110 μm when trap assisted recombination is excluded and 40 to 60 μm when it is included, for obtaining the highest power conversion efficiencies with J_{0s}<0.2 fA/cm^{-2} [42]. Ultra-high surface passivation improvement is the key to achieve high conversion efficiency using solar-grade silicon substrates.

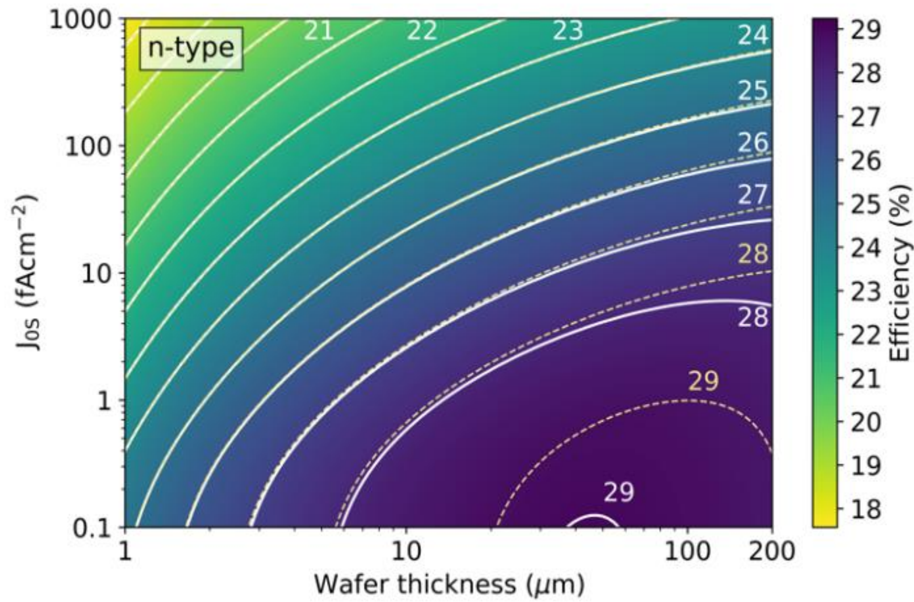

Figure 9: Conversion Efficiency of N-type Si Solar Cells ,with Bulk Lifetime of 10 ms, as a Function of Wafer Thickness and J_{0S}. The Dashed Lines Consider Only Surface Recombination, and Auger and Radiative Recombination in the Bulk. The Solid Lines (and the Color Map) Consider All Recombination Mechanisms, Including Bulk Lifetime. The Generation Current Is Defined by the Lambertian Light-trapping Limit for Each Thickness, Assuming the AM1.5g Spectrum at 25°C and Normalized to an Illumination Intensity Of 0.100 W cm^{-2}. [37]

3. PROCESSING AND CHARACTERIZATION

3.1 Device Processing

All the process development work for the fabrication of thin SHJ cells were done at Solar Power Lab, Arizona State University. The main fabrication steps can be divided into five broad sections as depicted in figure 10. SHJ samples were fabricated on n-type CZ wafers, with a starting thickness of 200 μm, bulk resistivity between 2 to 4 Ω-cm and <100> orientation. The wafers were thinned to different thicknesses from 180 to 40 μm using potassium hydroxide (KOH) solution. The samples were textured using alkaline wet etching (KOH and GP Solar additive), followed by an acidic cleaning process [43]. The total wet chemical process involves six steps and the recipes of the chemical solutions prepared, temperature and time are provided in table 2. Each wet chemical process is followed by rinsing the samples in de-ionized (DI) water until the resistivity of the water reaches 9 MΩ. This step is extremely important to make sure that contaminants are completely rinsed to achieve good surface cleans and avoid cross-contamination between the tanks. A high level of cleanliness of acid hood/baths is required for achieving repeatable results. Each cassette can hold 25 silicon samples, whereas only a maximum of 7-8 samples can be loaded for processing very thin wafers (<80 μm). Yield improvement was achieved by processing 3 to 4 lots of 8 silicon wafers each in freshly prepared solutions according to the recipes provided in table 2.

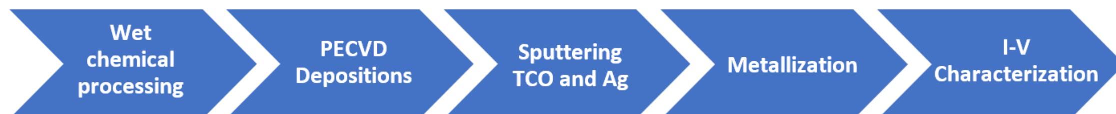

Figure 10: Broad classification of processing steps involved in the fabrication of silicon heterojunction solar cells.

Table 2: Wet Chemical Processing Steps and Corresponding Recipes for Solutions.

Wet chemical process	Purpose	Recipe for solution	Temperature (°C), time
1. Saw damage removal	Thinning of wafers	15.14L of 45% KOH + 3.785L of H_2O	80, variable
2. Texturing	Introducing random pyramids	18L of H_20 + 800 ml of 45% KOH, 50 ml of GP solar additive	80, 30-40 min
3. RCA-B	Metal ionic clean	13.2L H_20 + 2.2L of HCl + 2.2L of	74, 10 min
4. Dilute HF	Oxide removal	400ml of 45% HF + 10L of H_2O	RT, 10 min
5. Piranha	Oxidation of organic contaminants	15.142L of 95% H_2SO_4 + 3.785 L of H_2O	110, 10 min
6. Dilute HF	Oxide removal	400ml of 45% HF + 10L of H_2O	RT, 10 min

RT – indicates room temperature between 20 to 21 °C

After going through all the processing steps listed in table 2, the wafers are immediately transferred to a three-chamber plasma enhanced chemical vapor deposition (PECVD) cluster tool called P-5000 manufactured by Applied Materials for deposition. PECVD tool is used to deposit 6-15 nm thick intrinsic and n-/p-doped hydrogenated amorphous silicon (n-/p-/i-) (a-Si:H) layers, forming a p-i/c-Si/i-n stack. Immediate transfer to the tool is necessary to avoid native oxide formation and achieve high quality surface passivation. The p-i stack was first deposited on one side of the wafer followed by the i-n stack on the other side. The intrinsic a-Si:H was treated with an in-situ hydrogen plasma to improve the chemical passivation [44]. To improve the passivation properties of the intrinsic a-Si:H layer, we varied the PECVD susceptor temperatures and silane (SiH_4)-to-hydrogen (H_2) dilution ratios. PECVD is one of the most, if not the most, critical step for achieving good surface passivation

and high-performance devices. The details of these experiments are provided in the next chapter. The doped a-Si:H layers deposition parameters (susceptor temperature and gas flows) were also varied in certain devices to achieve better device efficiencies by controlling the doping level of the layers. PECVD tool is also used at SPL to deposit silicon nitride (SiN_x), silicon oxide (SiO_2), and other dielectric layers. The robot arm of the PECVD tool which handles the silicon wafers is vacuum operated and can lead to the breakage of wafers below 120 μm. This was overcome by designing SiN_x coated carriers that hold the wafers to be deposited and thus improve the yield of the SHJ devices.

Indium tin oxide (ITO) was deposited on both front and rear surfaces using a DC sputtering technique. The MRC 944 sputter tool can be used to deposit many dielectrics, metal films, and conductive oxides. Thin film depositions are performed by accelerating argon ions or an argon-oxygen mixture onto the surface of a sputter target, which is made of the material to be deposited onto the sample, mainly ITO and silver (Ag) in this study. ITO layers were optimized both electrically and optically to achieve better device efficiencies. The details of these experiments are provided in further chapters. The placement of thin wafers on the pallet used in the sputtering tool damages the underlying a-Si layers leading to a loss in surface passivation. This is overcome by placing the samples on a metal frame which provides a gap between the pallet and the samples to be deposited. This is also critical to improve yield and achieve repeatable results. A silver contact, also acting as a reflective mirror, was sputtered on the rear side of the SHJ solar cell. To mitigate the parasitic absorption of the front ITO layer, silicon oxide (SiO_x) layer was deposited by PECVD. This leads to an enhancement in the short circuit current density (J_{SC}) of the devices. As shown in figure 11, two different anti-reflective coatings (ARC) were fabricated. Front metal contacts were screen printed with the silver paste

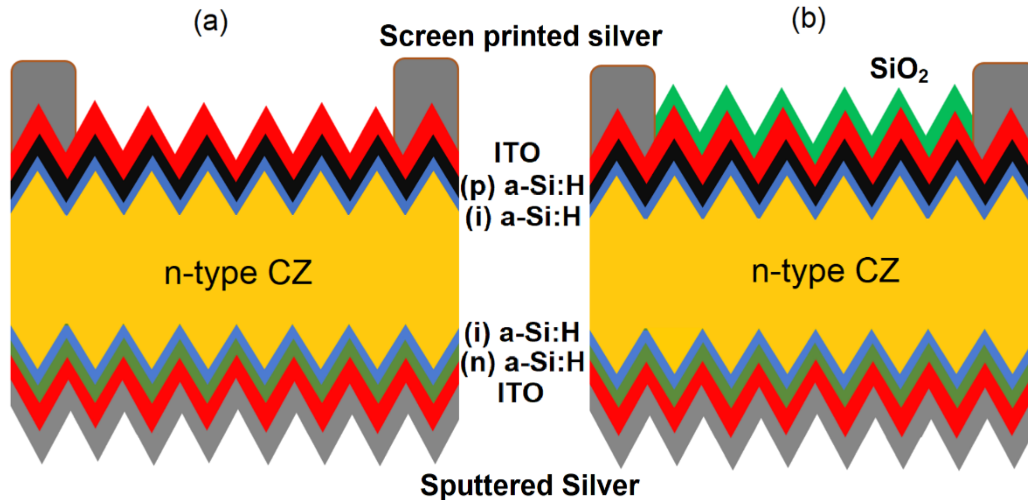

Figure 11: Illustration of SHJ Solar Cells Fabricated with Two Different ARC Structures: a) ITO and b) SiO_x and ITO Stack.

using the Baccini tool. The Baccini tool is an integrated, fully automated line for crystalline silicon PV cell production designed and manufactured by Applied Materials. The bulk conductivity of the paste used to form front metal contacts is limited by the conductivity of the polymer material present in it. The screen-printed cells were cured for 30 mins at 200 °C in a muffle furnace and ambient air conditions.

3.2 Characterization Tools

A Photoconductance decay tool (WCT-120) is used to measure the minority carrier lifetimes of semiconductor materials by implementing the photoconductance technique [39]. This tool is a contactless technique to measure current-voltage characteristics and was developed by Sinton in 1996. This measurement tool is extensively used in this thesis for the characterization of the minority carrier lifetime of various silicon samples. The tool measures τ_{eff} by exposing the samples to a flash of light produced by a xenon flash lamp. The flash generates excess carriers in the sample which recombine until equilibrium. The

Figure 12: The Thickness of the Wafers Was Measured after Texturing, at Five Different Points, Using a Digital Thickness Gauge with 1 μm Resolution. Photo Shows the Measurement Tool.

photogenerated excess electron and hole densities also increase the conductivity of the sample. An RF coil in the tool, directly underneath the sample, measures the decay of these charge carriers by measuring the change in photoconductivity. The excess photoconductance is given by:

$$\sigma_L = qW\Delta n_{av}(\mu_n + \mu_p) \tag{29}$$

where σ_L is the light generated conductance, W is the sample thickness, Δn_{av} is the average excess minority carrier density. A generalized way to determine the effective lifetime can be derived from the continuity equation as given by [45] as follows:

$$\tau_{eff} = \frac{\Delta n(t)}{G(t) - \frac{d\Delta n(t)}{dt}} \tag{30}$$

Where $\Delta n(t)$ is measured by the change in conductance as described above and the generation rate, $G(t)$, is measured by a reference cell in the tool. All the measurements in this

work were done using transient measurements where the incident flash duration is less than 0.2ms which is much shorter than the excess carrier decay lifetime (1-10 ms). In the transient measurement case, the generation rate is neglected to determine the excess minority carrier lifetime. Further parameters such as implied open-circuit voltage (iV_{OC}), implied FF (iFF) and surface saturation current density (J_{0S}) can be derived from the photoconductance decay measurement. Implied open circuit voltage is given by:

$$iV_{OC} = \frac{kT}{q}\ln\left(\frac{(\Delta n + N_{A,D}) * \Delta n}{n_i^2}\right) \quad (31)$$

The total surface saturation current density (J_{0S}) is estimated from a linear fit to the Auger-corrected (τ_{corr}) inverse effective minority carrier lifetime data as a function of excess carrier density, where $\Delta n \gg N_{A,D}$, as follows:

$$\frac{1}{\tau_{corr}} = \frac{1}{\tau_{eff}} - \frac{1}{\tau_{fund}} = \frac{1}{\tau_{bulk}} + \frac{2J_{0S}}{qW}\left(\frac{\Delta n + N_{A,D}}{n_i^2}\right) \quad (32)$$

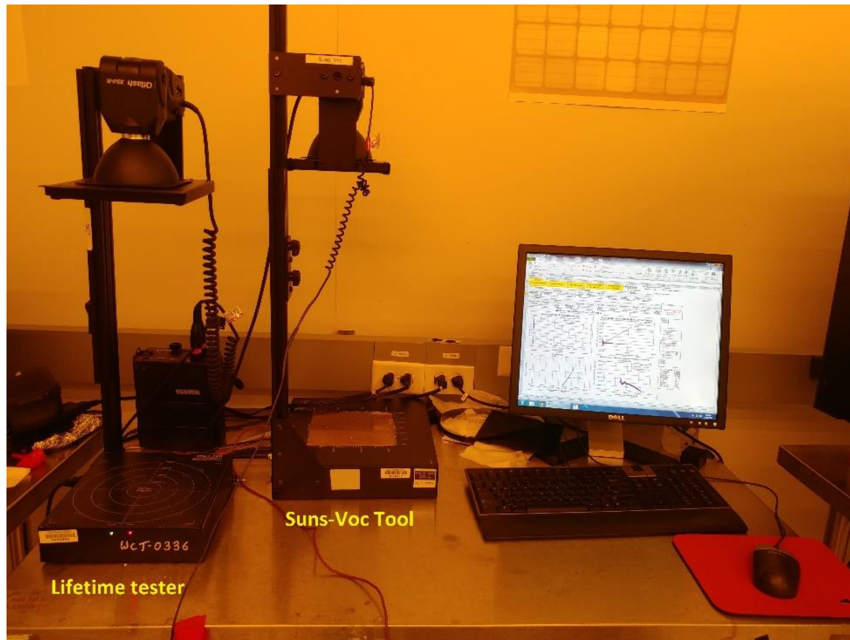

Figure 13: Photo of the WCT-0336 Photoconductance Measurement Tool on the Left and the Suns-V_{OC} Measurement Tool next to It as Setup in SPL.

To determine J_{0S} accurately will require using an effective intrinsic carrier density, which is a function of band gap narrowing provided by the Schenk band gap narrowing model described in [29].

A photoluminescence (PL) imaging tool can be used for spatially resolved characterization of effective minority carrier lifetime in silicon samples was well established by Trupke et al [46]. The silicon samples are illuminated by a light source and the generated photoluminescent signal due to radiative recombination is detected by an infra-red camera. The measured PL signal is proportional to the rate of spontaneous emission, which is proportional to the excess carrier density and the net background doping of the sample. It is also inversely proportional to defect density and impurity concentration. PL tool can also be used as an inline process monitoring tool as it provides fast spatial imaging of silicon samples, can measure solar wafers at any stage of processing, and can forecast the resulting cell efficiency. Similar to the PL tool, the electroluminescence (EL) tool can be used for the spatial characterization of metalized SHJ samples. In this technique instead of charge carriers generated by a light source, the solar

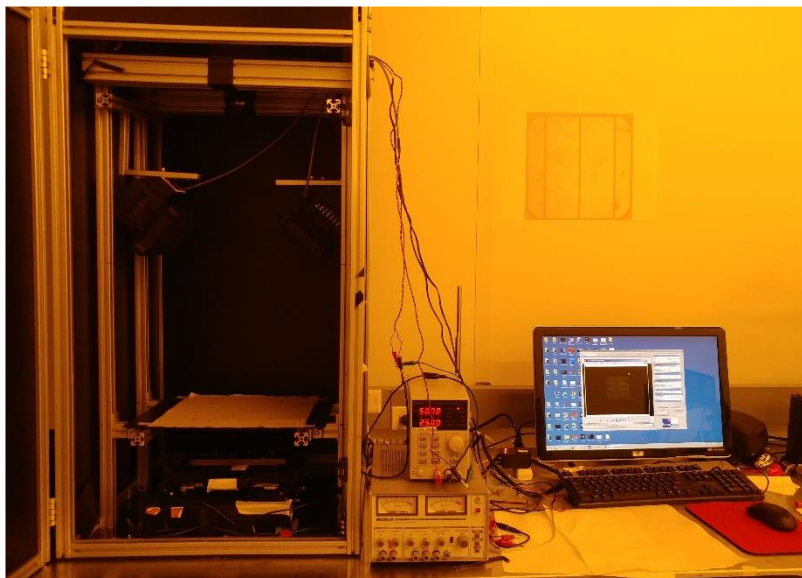

Figure 14: Photo of the PL and EL Characterization System at SPL

cell is forward biased using a power supply and subsequently, an IR camera is used to detect the emitted photons. PL and EL have been extensively used to generate spatial maps of series resistance [47], shunt resistance [48], [49], defect detection [50], [51], dark saturation current [52], [53] and minority carrier diffusion lengths [54], [55] and local efficiency mapping [56].

A flash tester (FCT-450), developed by Sinton Instruments, was used to measure the current-voltage (I-V) characteristics of all the SHJ solar cells in this thesis, figure 15. The tester has a xenon flash bulb that produces a spectrum very close to AM1.5 G. The tester is calibrated by Sinton instruments and later in this study a screen printed cell was measured at NREL to verify this calibration. The flash tester provides the short circuit current density (J_{SC}), open-circuit voltage (V_{OC}), Fill factor (FF), and efficiency (η). The tool is supplemented with the

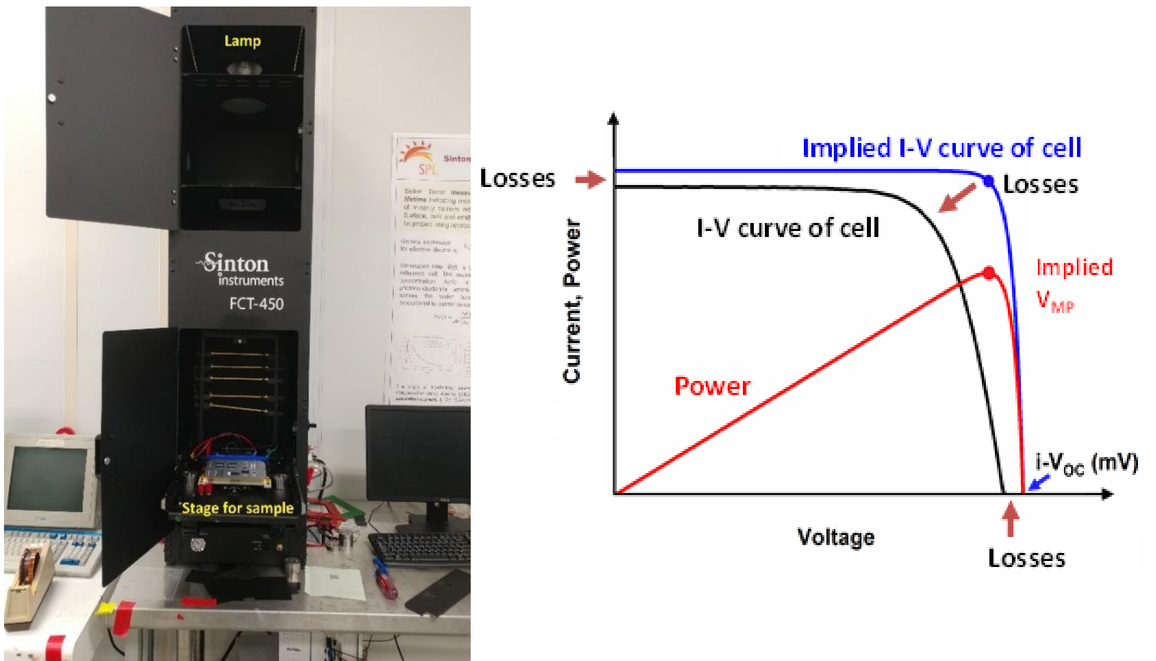

Figure 15: (Left) Photo of FCT-450 Instrument Used to Measure the I-V Characteristics of the SHJ Solar Cells Fabricated in This Study. (right) Example of the I-V Curve Measured by the System. Blue Curve Represents the Pseudo I-V Curve Measured by the Suns-V_{OC} System. Black Curve Represents the I-V curve, and the Red Curve Represents the Power Curve of the SHJ Solar Cell.

Suns-V_{OC} analysis which provides the pseudo I-V characteristics using which we can precisely measure the series (R_s) and shunt resistance (R_{sh}) of the solar cell and indicate the source of power losses. The slope of the I-V curve at low voltages provides the shunt resistance of the solar cell. Series resistance can be extracted by comparing the pseudo I-V curve to the actual I-V curve [57]. The tool can also provide measurements of saturation current density (J_0), bulk lifetime, lifetime at maximum power, substrate doping concentration and I-V characteristics at multiple intensities.

The Quantum efficiency of the solar cell is measured by the QEX10 tool, figure 16. The Quantum efficiency of a solar cell is defined as the ratio of the number of carriers collected by the solar cell to the number of photons of any given energy incident on the solar cell. All QE curves reported in this thesis are obtained after the metallization of the front and back of the SHJ solar cells. The incident light beam of the tool is focused in between two metal fingers and close to the metal busbar of the cell for optimum current collection. Reflectance

Figure 16: Photo of QEX10 Quantum Efficiency Measurement Tool

measurement can also be performed using this tool and was frequently used to optimize the anti-reflective coatings on the front of the SHJ samples.

Ellipsometry is a characterization technique that measures the change in polarization of incident light by the reflection from a sample. A variable angle spectroscopic ellipsometer (VASE) developed by J.A. Woollam ellipsometry solutions, was used to measure the thickness and optical constants of various thin films and also the thickness uniformity across a sample [58]. The raw ellipsometry data provides the amplitude component and the phase difference component of the reflected incident wave. To obtain this the measurement was done in the wavelength range of 300-1100 nm and at three different incident angles: 70, 75 and 80 degrees. The data was fitted to obtain various thin film characteristics by building the optical models using the CompleteEASE program developed by J.A. Woollam.

Fourier transform infrared spectroscopy was used to measure the material properties of thin intrinsic a-Si layers which were deposited on polished silicon substrates. The transmission infrared spectroscopy technique was used to measure the sample. The sample is placed directly into the infrared (IR) beam and as the IR beam passes through the sample, the transmitted energy is measured. An absorption spectrum is generated by calibrating the tool with a polished silicon substrate that has no layer deposited on it. The integrated intensity of the absorption peaks can be used to determine the microstructure fraction and hydrogen content in the intrinsic a-Si layers as given by the equation:

$$I_i = \int \frac{\alpha(\omega) d\omega}{\omega} \tag{33}$$

3.3 Process Control and Characterization

The photoluminescence tool can be used as an inline process monitoring tool to detect bad surface cleans that have led to areas of high surface recombination on the surface of the silicon samples. Wafers that have undergone any phase in the wet chemical processing steps described in table 2 can be dipped in an HF solution to generate an empirical image of the effective carrier lifetime, figure 17. Surface recombination velocity of silicon and germanium surfaces dipped in various acids was explored by Yablonovitch et al and they found HF solution to provide the least surface recombination velocity [59]. Subsequent infrared spectroscopy done shows that the surface was covered with covalent silicon-hydrogen (Si-H) bonds leaving no surface dangling bonds as recombination centers [59]. Characteristic and recurring defects are observed in PL images of wafers that have undergone saw damage removal and texturing, even after subsequent RCA-B and Piranha wet chemical cleaning, figure 17.

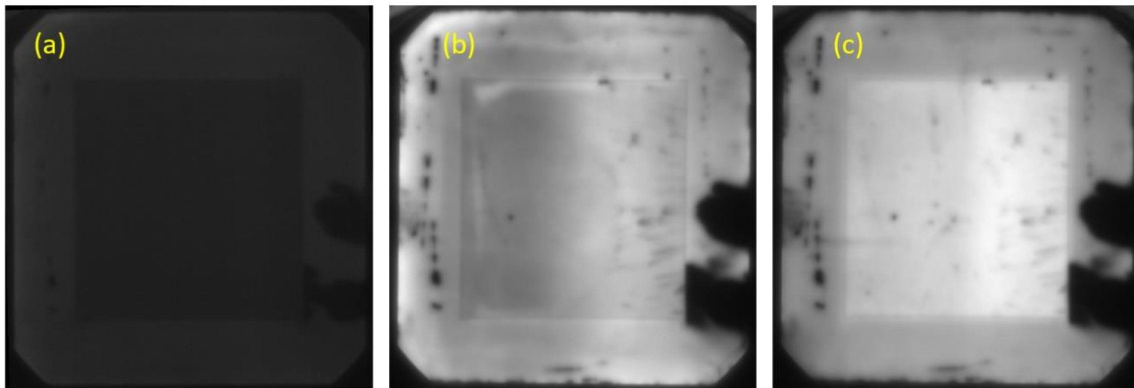

Figure 17: Photoluminescence Images of Silicon Samples after Chemical Process (a) Saw Damage Removal and Texturing. (b) after RCAB Clean. (c) after Piranha Clean. PL Can Be Used as an Inline Process Monitoring Tool to Obtain an Empirical Value for the Effective Minority Carrier Lifetime. Images Taken with Samples Dipped in Dilute HF Solution. Bulk/Handling Defects Can Be Seen in the Bottom Right Corner of the Samples. The Camera Settings like Gain, Exposure Time, and Pixel Binning Are Kept Constant Between Images.

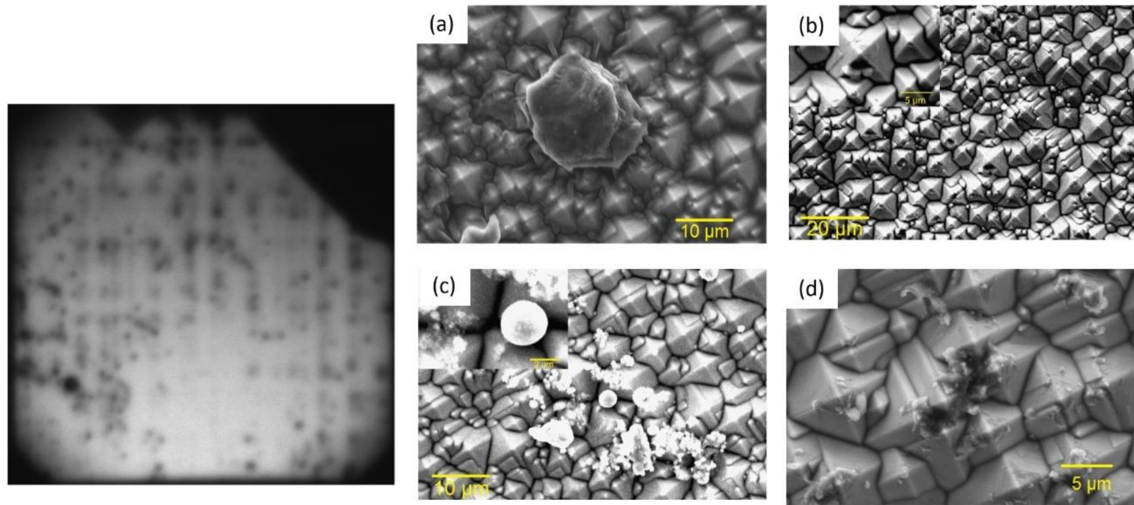

Figure 18: (Left) Photoluminescence Image of Defect Rich Sample Used for SEM Analysis. (Right) (a) Non-etched Silicon Particles (b) Damage on Deposited a-Si Layers (c) Various Debris Particles (d) Damaged Pyramids Seen on c-Si

Various kinds of defects, figure 18 are observed on c-Si wafers as seen in the SEM images. User handling of the wafers, the use of carriers for deposition of a-Si layers in the PECVD tool, and other uncontrollable processing variables play a major role in creating these areas of high recombination.

The PECVD deposition chambers must be cleaned and conditioned before the deposition of the a-Si layers to avoid debris particles on the surface of the wafer. Routine process control measurements to study the deposition rates of a-Si layers were performed by using VASE, Figure 19. Nine-point uniformity measurements of amorphous silicon films deposited without a hydrogen plasma etch step were also generated using VASE throughout this thesis. As can be seen in figure 19, the deposition range and the sample uniformity alters frequently compared to the baseline measurement taken on 9/15/17. These changes might be attributable to wafer-to-wafer repeatability, the way the carrier wafer lands in the susceptor pocket, the regular change of hydrogen cylinders for the P-5000, or some other factor that is

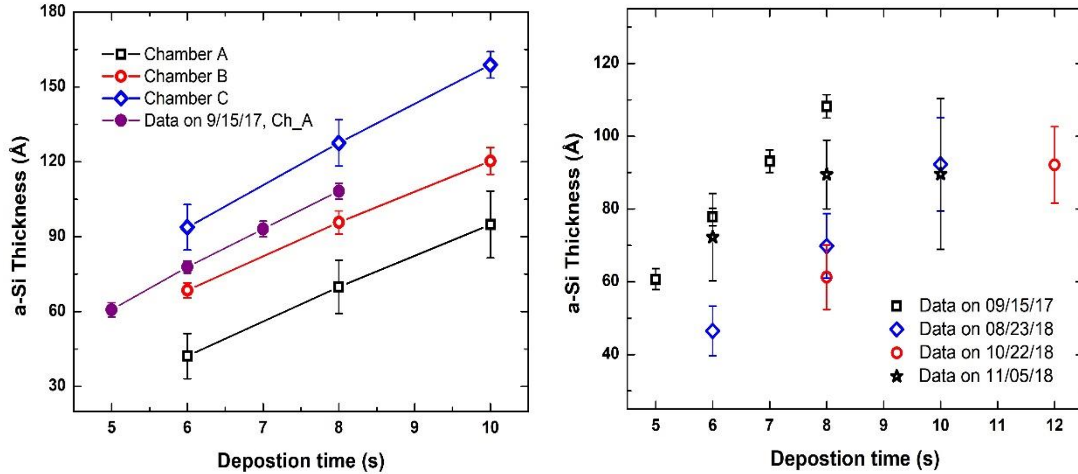

Figure 19: Intrinsic a-Si Layer Thickness vs Deposition Times Taken on: (Left) Three Different Chambers (Right) Different Occasions - and Compared to the Historic Data Taken on 9/15/17.

not yet determined. Contour maps generated using the VASE data indicate that a non-uniformity of only 3.4% exists on the baseline sample, figure 20 (left). The non-uniformity of a sample from 8/23/18 was very high at 13%, figure 20, (right). Nine-point uniformity measurements of p-type a-Si layers exhibited an average non-uniformity around 10.5 % and the n-type a-Si layers had an average of 22.7%.

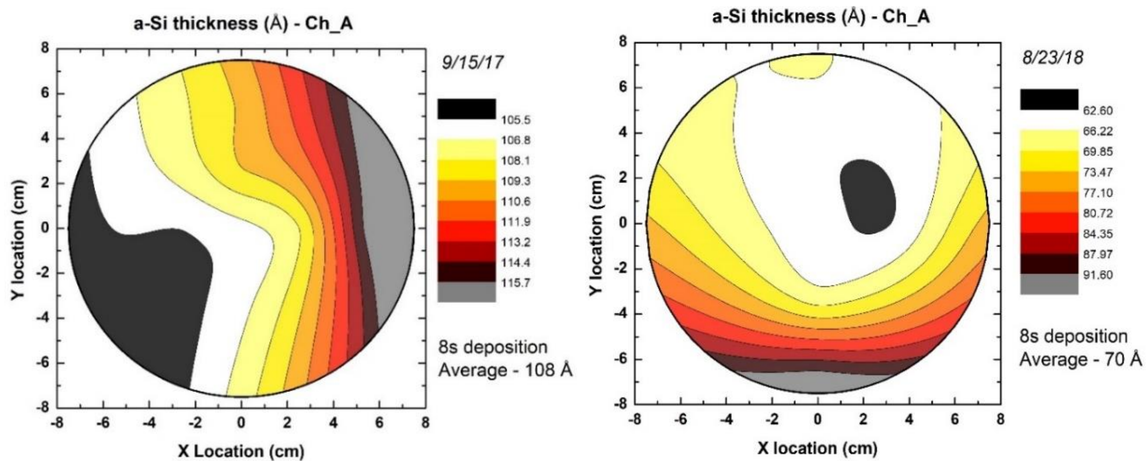

Figure 20: Contour Map of a-Si Layer Deposited in Chamber

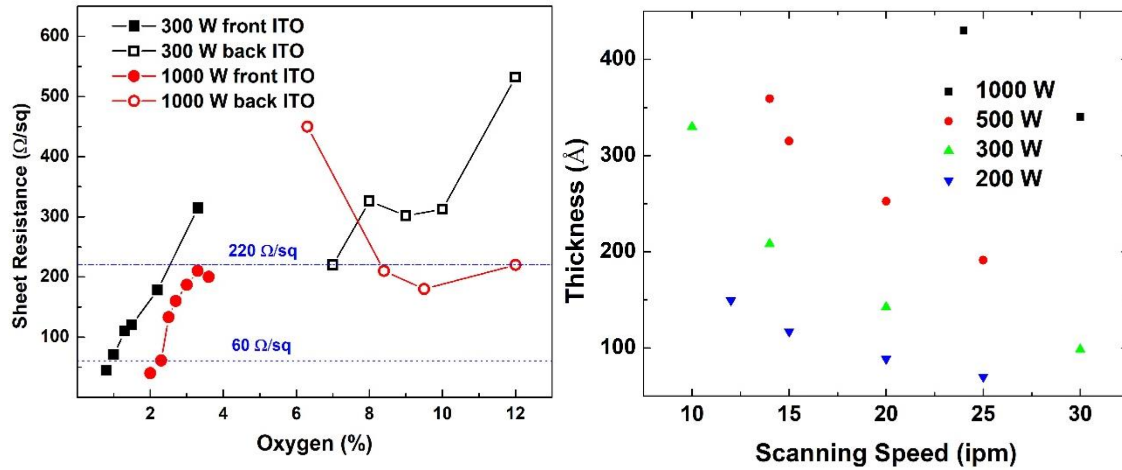

Figure 21: (Left) Sheet Resistance of Different ITO Layers of the Same Thickness as a Function of Oxygen Percentage Used During the Plasma Sputtering Process. This Was Measured Using Four-point Probe (FPP). (Right) Thickness of ITO Layers as a Function of Various Plasma Power and Scanning Speed of the Pallet Used for Deposition. The Deposition Was Carried on Polished Silicon Substrates and Thickness Was Measured Using VASE.

The deposition of the ITO layer must also be constantly monitored as it acts both as a conductive layer and an anti-reflective coating. The electrical and optical response of ITO thin films deposited using different conditions were measured. A sheet resistance of 60 Ω/sq for the frontside ITO and 220 Ω/sq for the backside ITO was targeted for various deposition conditions, figure 21. The thickness and deposition rate of ITO thin films deposited using different plasma power was measured using VASE. The reflectance of the ITO front surface layer was measured using the QE tool. The plasma generated in the tool was relatively less stable for very low-power density operation, which can lead to different microstructural, electrical, and optical properties [60]. All the processing techniques described above have parameters that are critical for the yield improvement of thin silicon wafers, some of which are described in table 3.

Table 3: Description of Yield Problems for Various Processing Steps and the Solution Developed to Overcome Them.

Process step	**Problems for yield**	**Solution**
Wet chemical processing	Wafers sticking to each other	Spacing required between placement of wafers in cassette
	Breakage of wafers during transfer of cassette between solution tanks	Avoid any agitation in solution while transferring cassette
	Spin rinse dry	Very low RPM (~500) and no N_2 gas flow
PECVD	Tool robot arm (vacuum)	Design of elevated SiN coated carriers
Sputtering	Pallet placement	Use elevated carriers
Screen printing	Vacuum, Pressure and Speed	Use carriers, pressure below 60 N and speed below 15 ipm

4. SURFACE PASSIVATION BY AMORPHOUS SILICON

The efficiency of silicon solar cells continues to be limited by the recombination of photogenerated electron-hole pairs. Various physical processes, like deposition of dielectric layers, and chemical processes that are used to limit the surface recombination rate are collectively termed surface passivation. Two main principal effects are used to achieve low surface recombination rates; Chemical passivation is achieved by eliminating the surface dangling bonds by the introduction of hydrogen or oxygen species and reduce the recombination centers. Field-effect passivation is achieved by using a built-in electric field to repel the generated carriers away from the surface and thereby preventing recombination at the surface defects. This built-in electric field can be achieved by a doping profile below the interface or by the presence of electrical charges at the interface [61]. Surface passivation is one of the main factors limiting solar cell efficiency as described in chapter 2. In the past, we have demonstrated open-circuit voltages over 760 mV and J_{0S} below 1 fA/cm^2 on 50 μm thick SHJ structures [62]. Those structures were designed to maximize surface passivation and voltage by using a thick (15 nm) intrinsic hydrogenated amorphous silicon (a-Si:H) layer on non-textured surfaces. Both implied (iFF) and pseudo fill factors (pFF) were greater than 85%. However, the use of a very thick intrinsic layer led to fill factors (FF) below 60%. Various groups have reported intrinsic a-Si:H layers in the range of 5-7 nm thickness to deliver efficiencies greater than 20% [63]–[65].

4.1 Plasma Chemistry and Growth Kinetics

Hydrogenated amorphous silicon (a-Si:H), which involves about 10 at% hydrogen in its material structure, was shown to have a low dangling bond-defect density in 1975 [66] and

also control the doping of p- or n-type material while growing the a-Si layer by Boron or Phosphorus respectively. In contrast to diffused junction solar cells a-Si:H layer is deposited using plasma enhanced chemical vapor deposition (PECVD) and needs only temperatures up to 300 ^{0}C. The growth mechanism of a-Si:H from a silane (SiH_4; source gas molecule) plasma has been investigated using a variety of process-diagnostic techniques [67].

Electron collision on monosilane (SiH_4) molecules is the primary event in the plasma. Electronically excited states of silane molecules are dissociative states, meaning that spontaneous dissociation occurs from those electronically excited states to a variety of radicals such as SiH_3, SiH_2, SiH, Si, and H [66]. Various parameters, like deposition temperature,

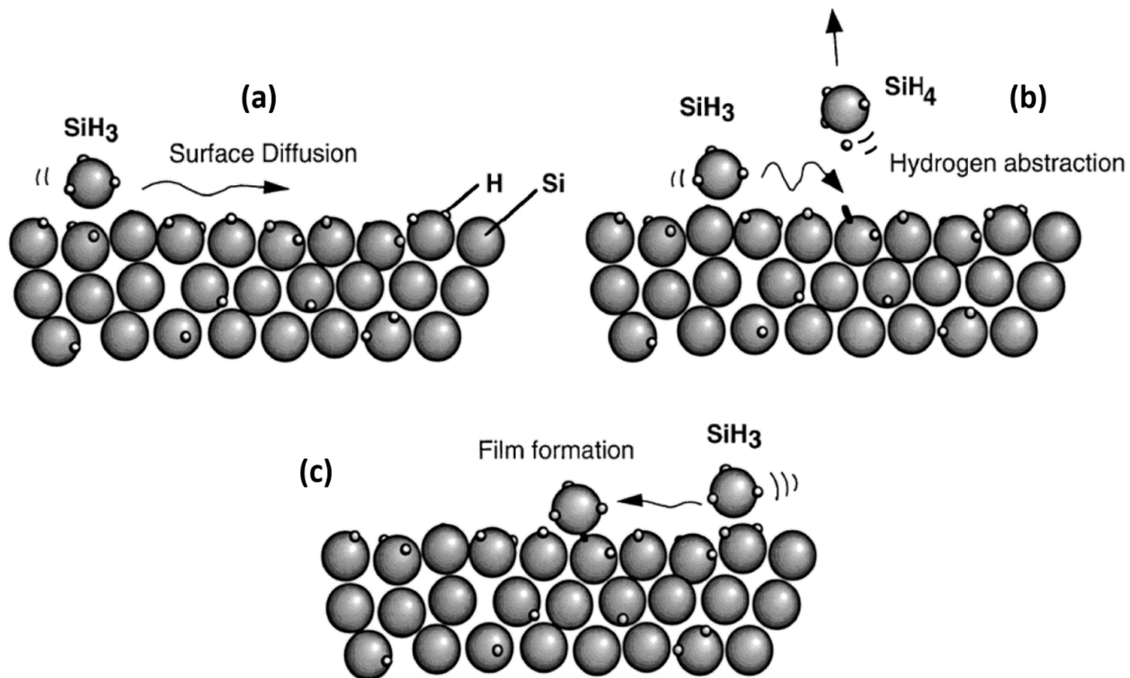

Figure 22: Extracted from [66] - Surface Reaction Model of Radicals as Established by Matsuda *et al*. (a) SiH_3 Reaches the Film Growing Surface and Diffuses Along the Surface (b) Surface Diffusing SiH_3 Abstracts Hydrogen Forming SiH_4 and Leaving Behind Si-dangling Bond (c) Another SiH_3 Radical Attaches to the Dangling Bond Forming Si-Si Bonds Leading to Film Formation.

pressure, frequency, gas flows, dilution ratios, plasma power, susceptor to showerhead distance, control the electrical, optical, and structural properties of the intrinsic a-Si layer deposited using the PECVD tool [66]–[68]. This work mainly concentrates on susceptor temperature and silane to hydrogen dilution ratio.

During the deposition process, hydrogen radicals terminate Si dangling bonds which are controlled by the amount of hydrogen gas in the plasma. Therefore, hydrogen dilution controls the rate and density of hydrogen radicals terminating dangling bonds. Hydrogen dilution has been demonstrated to result in materials with improved order [68]. Beyond a certain threshold, the transition from amorphous to the microcrystalline phase takes place and the density of defects starts to increase with increasing gas flow. Then, SiH_3 radicals rapidly diffuse across the surface leading to hydrogen abstraction and the remnant dangling bond leads to subsequent chemisorption of SiH_3 radicals, leading to the growth of the intrinsic a-Si layer. Substrate temperature controls the rate of diffusion by providing kinetic energy to the SiH_3 radicals and also controls the amount of density of defects present in the intrinsic a-Si layer [66]–[68]. Low temperatures lead to greater defects due to the presence of voids and very high temperatures lead to an increase in the number of vacancies [69]. Substrate temperature also provides kinetic energy for breaking Si-H bonds – hydrogen effusion [66]. Thus, a balance between ordered structure and hydrogen-terminated dangling bonds is needed for effective surface passivation.

4.2 Impact of Susceptor Temperature and Silane-to-Hydrogen Dilution Ratio

A standard baseline deposition process for intrinsic a-Si:H baseline deposition process at SPL is established where the PECVD susceptor temperature is 250 ^{o}C and silane-to-hydrogen

dilution ratio is 20% [70]. A deposition temperature setpoint of 250 °C has been previously reported to deliver an intrinsic layer with good passivation properties [71], [72]. Different temperatures may be desirable as they impact the hydrogen content and microstructure of the film [73], [74], which controls the passivation properties of the a-Si:H layer. In this study, we used textured thin wafers (~40 μm) as a testbed to increase the sensitivity to the surface passivation. Distribution of effective minority carrier lifetime (left) and implied open-circuit voltage (iV_{OC}) (right) for depositions of intrinsic a-Si:H at different setpoint temperatures and with a silane-to-hydrogen dilution ratio of 20% is plotted in figure 23. As the deposition rate is temperature dependent, the deposition time was adjusted to achieve the same thickness of

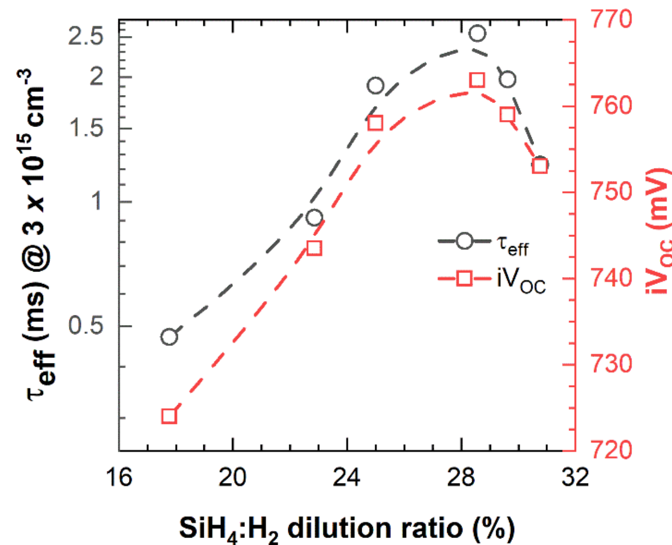

Figure 23: Effective Minority Carrier Lifetime and iV_{OC} of 42±2 μm Thick Wafers as a Function of Different Silane-to-Hydrogen (SiH_4:H_2) Dilution Ratios for a Susceptor Temperature of 275 °C. p-i and i-n a-Si:H Layers Were Deposited on These Wafers. Each Data Point Represents an Average Effective Minority Carrier Lifetime and iV_{OC} Obtained From Two Wafers. The Dashed Lines are a Guidance to the Eye Obtained Using B-Spline Smoothing Function to Fit the Data. The Average Thickness of a-Si:H Doesn't Vary Significantly Between Different Dilution Ratios. An Injection Level of $3x10^{15}$ cm^{-3} Represents the Maximum Power Point for 42±2 μm Thick Wafers.

a-Si:H (6 nm) for all samples. The average effective minority carrier lifetime is comparable for 250 ºC and 275 ºC, approximately 1.5 ms, but considerably lower for 300 ºC, 0.6 ms. Lower effective minority carrier lifetimes at 300 ºC can be due to the amorphous-to-crystalline transition of the a-Si:H layer at higher temperatures [72]. The wafer temperature is varied in the PECVD tool by controlling the susceptor temperature. The temperature is measured on the bottom of the susceptor, and the software incorporated in the tool and developed by the PECVD manufacturer estimates the wafer temperature. For susceptor temperatures of 250 ºC, 275 ºC, and 300 ºC, the estimated wafer temperatures are 233 ºC, 244 ºC, and 265 ºC, respectively. These wafer temperatures are within the range of optimum deposition temperatures reported by other groups [71], [72], [75].

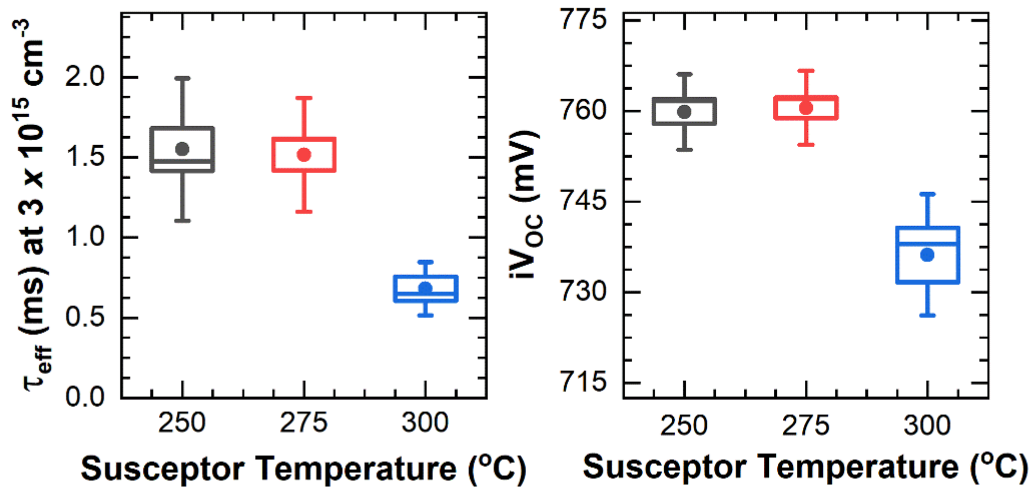

Figure 24: Measured Effective Minority Carrier Lifetime (at $3x10^{15}$ cm^{-3} Injection Level) and Implied Open Circuit Voltage (iV_{OC}) of p-i/c-Si/i-n Structures Deposited on 42±2 μm Thick Wafers. The Deposition Temperature of the Intrinsic Layer was Varied by Controlling the Susceptor Temperature. The Intrinsic Layer Thickness (6 nm) and Silane-to-Hydrogen (SiH_4:H_2) Dilution Ratio (20%) is Kept Constant for All Samples in This Plot. The P and N Doped Layers Were the Same for All Samples. Ten Samples Were Measured for Each Deposition Condition.

The hydrogen content of the intrinsic a-Si:H layer is also controlled by the silane-to-hydrogen dilution ratio during the deposition. The variation of effective minority carrier lifetime and iV_{OC} for different dilution ratios and a susceptor temperature of 275 °C is plotted in figure 24. As the dilution ratio increases from 17.8% to 28.6%, the effective minority carrier lifetime increases from 0.5 ms to 2.4 ms around the maximum power point injection level. A further increase in the dilution ratio to 30.8% leads to about a 1 ms loss in the effective minority carrier lifetime. The best effective minority carrier lifetime and iV_{OC} were obtained for a dilution ratio of 28.6%. For a 42±2 μm thick wafer, we measured an effective minority carrier lifetime and iV_{OC} of 2.4 ms and 763 mV, respectively.

4.3 Uniformity of i-a-Si Layer

Thickness uniformity of the intrinsic a-Si:H layer across the wafer area is a required condition to deliver high efficiencies on commercial size SHJ solar cells. The thickness

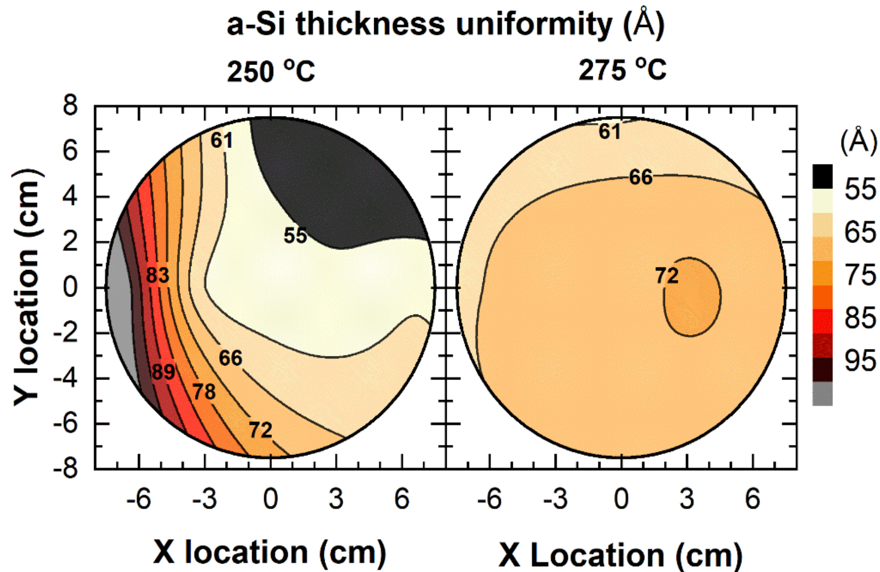

Figure 25: Variation of a-Si Thickness Deposited on a 150 mm Polished Wafer for Two Different Susceptor Temperatures Measured Using VASE. The Average Thickness is 6.5 nm for Both Deposition Conditions. The Non-Uniformity is 5.1% at 275 °C and 34.6% at 250 °C.

uniformity of the a-Si:H films deposited at 250 ºC and 275 ºC were measured on 150 mm polished wafers using variable angle spectroscopic ellipsometry (VASE). As shown in figure 25, the thickness uniformity improves when samples are deposited at 275 ºC. The non-uniformity, for the same intrinsic layer thickness, was 34.6% for samples deposited at 250 ºC and 5.1% for samples deposited at 275 ºC. The deposition of the intrinsic a-Si:H layer is not only controlled by temperature but also by multiple other parameters [76]. Previous studies on gas-phase reaction and transport phenomenon for PECVD processes illustrate wafer temperature regulation, within a range of 7 ºC, along concentric zones have sizable impact (>10%) on thickness uniformity [77]. Targeting very thin layers and creating abrupt junctions to avoid epitaxial growth, leads to constraints in process parameters and usage of extremely short deposition times, in the order of 5-7 seconds. Over this temporal range, seemingly subtle differences in plasma ignition time and incipient plasma uniformity can have a sizable impact on film reproducibility. The susceptor temperature of 275 ºC was the condition that delivered the best reproducibility and uniformity for the desirable film thickness, figure 25.

4.4 Implied Voltage Characteristics at Maximum Power and Open Circuit

A comparison of effective minority carrier lifetime between the baseline and optimized processes is shown in figure 26. The difference in lifetime between the fundamental and the experimental data decreases with increasing carrier density, indicating that the fundamental recombination plays a larger role at open circuit than at maximum power injection. For 40 µm thick samples, the optimized process shows voltage improvements of 20 mV at implied maximum power (iV_{MP}) and 5 mV at implied open circuit (iV_{OC}). The implied fill factor (iFF) improves over 1% absolute. The improvement of voltage at the maximum power is larger than at open circuit, as surface recombination plays a larger role at maximum power [78].

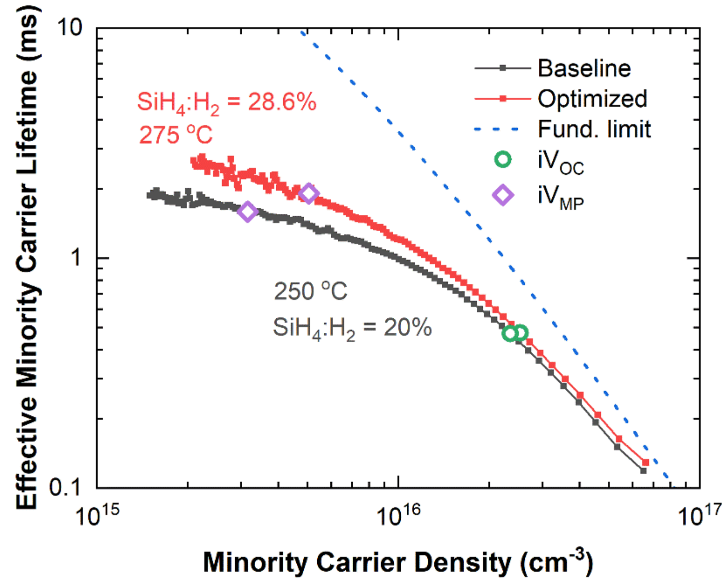

Figure 26: Comparison of τ_{eff} vs Minority Carrier Density on 42±2 μm Thick Wafers for the Baseline and Optimized Process. iV_{OC} and iV_{MP} are Indicated as Seen in the Graph. The Dashed Blue Line Represents the Fundamental (Auger and Radiative) Minority Carrier Lifetime Limit Calculated According to Richter et. al Parameterization [23].

4.5 FTIR Spectroscopy of a-Si Layers

The content of hydrogen in the a-Si:H layer is one of the critical factors to achieve high effective minority carrier lifetime [74]. Hydrogenation of silicon dangling bonds reduces the density of defects at the interface leading to higher effective minority carrier lifetimes [74]. In figure 27 we measure the hydrogen content and the microstructure fraction coefficient (R*) [73] of the intrinsic a-Si:H films deposited at different susceptor temperatures using Fourier transform infrared (FTIR) spectroscopy in transmission mode. The samples measured in figure 27 were prepared by depositing 100-110 nm of intrinsic a-Si:H layer on single side polished wafers. Similar thicknesses were achieved by controlling the deposition time for different susceptor temperatures. The in-situ hydrogen plasma treatment parameters were kept constant for the different susceptor temperatures.

Silicon hydride (Si-H_x) bond vibrations have been extensively studied and determined to have three characteristic absorptions: a wagging mode at 640 cm^{-1}, a bending scissor mode at 840–890 cm^{-1}, and a stretching mode between 1980-2160 cm^{-1} [79]. Stretching modes can be further divided into a low stretching mode (LSM) at 1980–2030 cm^{-1} and a high stretching mode (HSM) at 2060–2160 cm^{-1} [79]. Previous results have shown the LSM to be associated with monohydride (Si-H) bonds; similarly, the HSM is attributed to dihydride (Si-H_2) bonds [80]. The total hydrogen content (C_H %) was obtained by the integration of the Si-H absorption

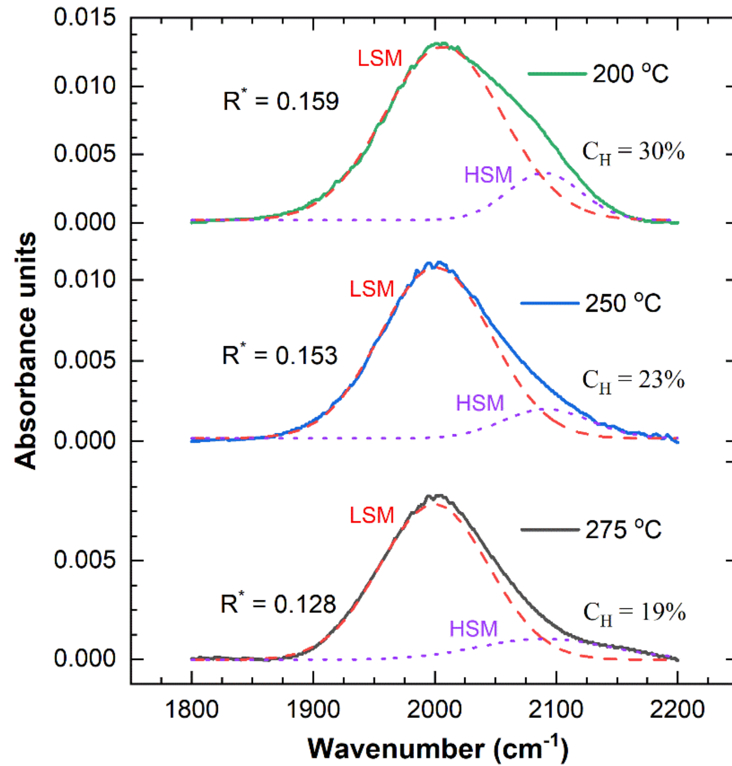

Figure 27: Comparison of FTIR Spectra for Different Susceptor Temperatures in Transmission Mode. The Solid Lines Represent the Absorbance. The Dashed Lines Indicate the LSM Peak Fits Done Between 1900-2010 cm^{-1}. The Dotted Lines Indicate the HSM Peak Fits Done Between 2090-2110 cm^{-1}. R* for Each Peak is Calculated According to [45]. C_H is Calculated According to [53]. The Intrinsic a-Si:H Thickness of 110 nm and In-Situ Hydrogen Plasma Time was Kept Constant for All Samples.

peak at 640 cm^{-1} [81]. An increase of the R* value has been correlated with a decrease in density of the a-Si:H film due to the presence of vacancies and voids and hydrogen content as well [69]. A high R* value has been also attributed to higher disorder in the film [69].

Higher susceptor temperatures show lower and broader HSM absorbance peaks (Figure 27) resulting in lower R* values and more ordered films. However, higher temperatures also result in lower hydrogen content. The passivation capability of the a-Si:H layer benefits from a more ordered and hydrogen-rich film [74]. The a-Si:H shows better R* for the 275 °C process and incorporates lesser hydrogen than films deposited at lower temperatures. From this point further, the process to deposit films using a susceptor temperature of 275 °C and a dilution ratio of 28.6% will be named as the optimized process.

4.6 Impact on Varying Substrate Thicknesses

To evaluate the benefits of the optimized process for different wafers thicknesses, we manufactured p-i/c-Si/i-n structures on textured wafers with thicknesses between 40 and 175 μm. Figure 28 shows how voltage is impacted by the two processes as the wafer thickness changes. The fundamental limits of V_{OC} and V_{MP} were calculated using the method previously described in [62]. In figure 28 the optimized process delivers higher iV_{MP} and iV_{OC} than the baseline process, independent of the wafer thickness. At iV_{OC} for the optimized process, the fundamental recombination is the dominant contributor to the total recombination. As the thickness of the wafer decreases the contribution of fundamental recombination decreases whereas the contribution of surface recombination increases, resulting in a larger deviation from the fundamental limit for thinner wafers (<80 μm). At iV_{MP}, both trap assisted and surface recombination play an important role. As we reduce the thickness of the wafer, the

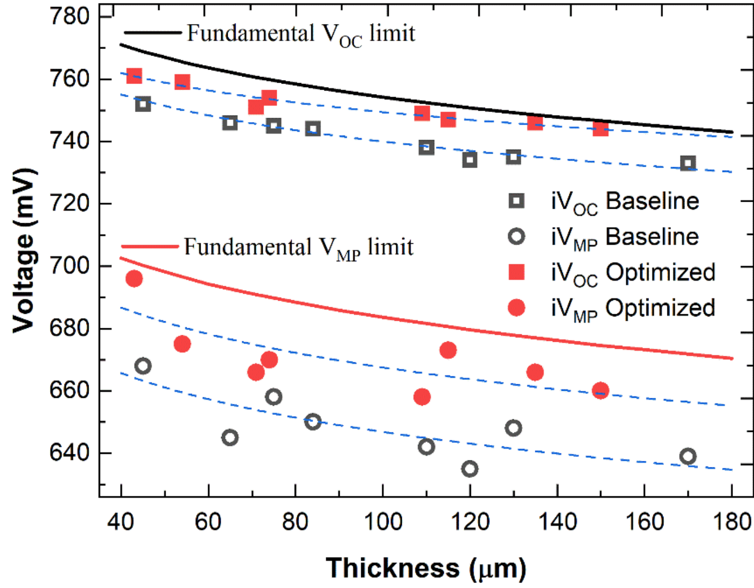

Figure 28: Comparison of iV_{OC} and iV_{MP} of the Optimized and Baseline Processes for Textured Wafers of Different Thicknesses. The Solid Black and Red Lines Represent the Fundamental V_{OC} and V_{MP} Limits. The Dashed Lines Indicate Logarithmic Fits to the Data. Implied Voltages are Obtained for the Wafers Using the Sinton Lifetime Tester, After Depositing i-p and i-n Layers on Them.

contribution of the surface to the total recombination increases, whereas the trap-assisited recombination decreases. As a result, the total contribution of these two recombination mechanisms at iV_{MP} seems to balance each other for different wafer thicknesses. This will be further explored by modeling the recombination fractions in the upcoming sections.

The total surface saturation current density (J_{0S}) was estimated from a linear fit to the Auger-corrected inverse effective minority carrier lifetime data as a function of excess carrier density in the range of 8 $x10^{15}$ and $1.3x10^{16}$ cm^{-3} [82]. Figure 29 shows the total J_{0S} values using the two processes for different wafer thicknesses. Average J_{0S} of 0.6 fA/cm^2 was accomplished using the optimized process. Previously [62], we demonstrated J_{0S} close to 0.1 fA/cm^2 by depositing a 15 nm thick layer of intrinsic a-Si:H on untextured wafers. The thick layer prevented us to

obtain a fill factor (FF) greater than 60%. This work demonstrates similar levels of passivation by using a layer that is more than two times thinner compared to previous work done at SPL [62]. Moreover, all the J_{0S} and implied voltage characteristics presented here are on textured wafers which have a significantly higher density of defect states on the surface compared to flat/non-textured wafers. We accomplished J_{0S} below 1 fA/cm^2 and implied open-circuit voltage (iV_{OC}) of 764 mV on 40 μm thick textured wafers by developing a 6 nm thick intrinsic a-Si:H layer.

To better explain the above results, the effective minority carrier lifetime, τ_{eff}, is modeled into its component recombination mechanisms using equations (7), (13), and (19) described in chapter 2. Each recombination fraction at a certain injection level is obtained by dividing the individual recombination lifetime by the total effective lifetime.

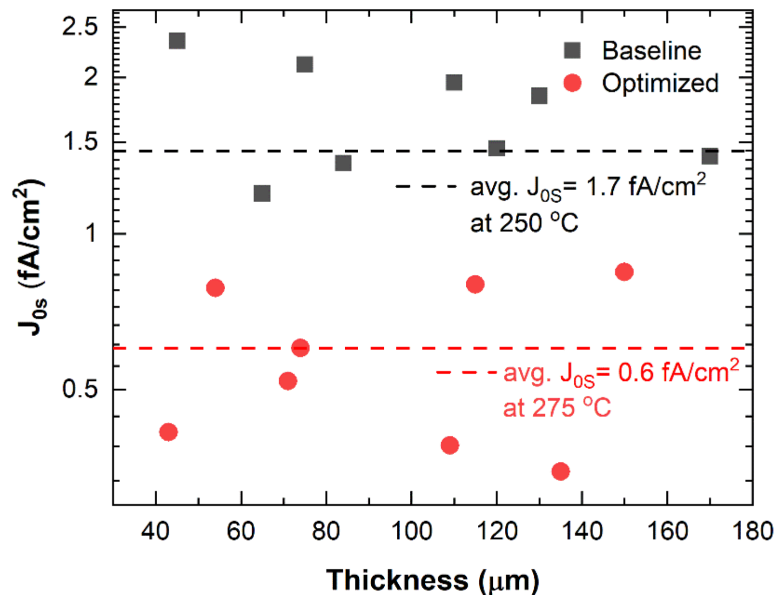

Figure 29: The J_{0S} for Different Wafer Thickness for Optimized and Baseline Processes. The Dashed Lines Indicate the Average J_{0S} Obtained from all the Data Points for Different Thicknesses. A Base-10 Log Scale is Used for the Y Axis.

$$Recombination\ fraction\ = \frac{\tau_i}{\tau_{eff}}$$

where i = Auger, Radiative, Trap assisted, Surface recombination lifetime. As a result of the dependence of total recombination rate on substrate thickness, the structure with a thickness of 40 μm thickness shows a higher effect of surface recombination on the total recombination rate than the one with 170 μm. The impact of the surface recombination is mainly observed at the maximum power point injection level. The fundamental recombination fraction (Auger and radiative), represented by the colored bars in figure 30, becomes less dominant at open-circuit (V_{OC}). The fraction of fundamental recombination is close to 90% for the thicker and the thinner wafer for a J_{0S}=0.5 fA/cm^2, figure 30 (a). This changes to close to 80% for the

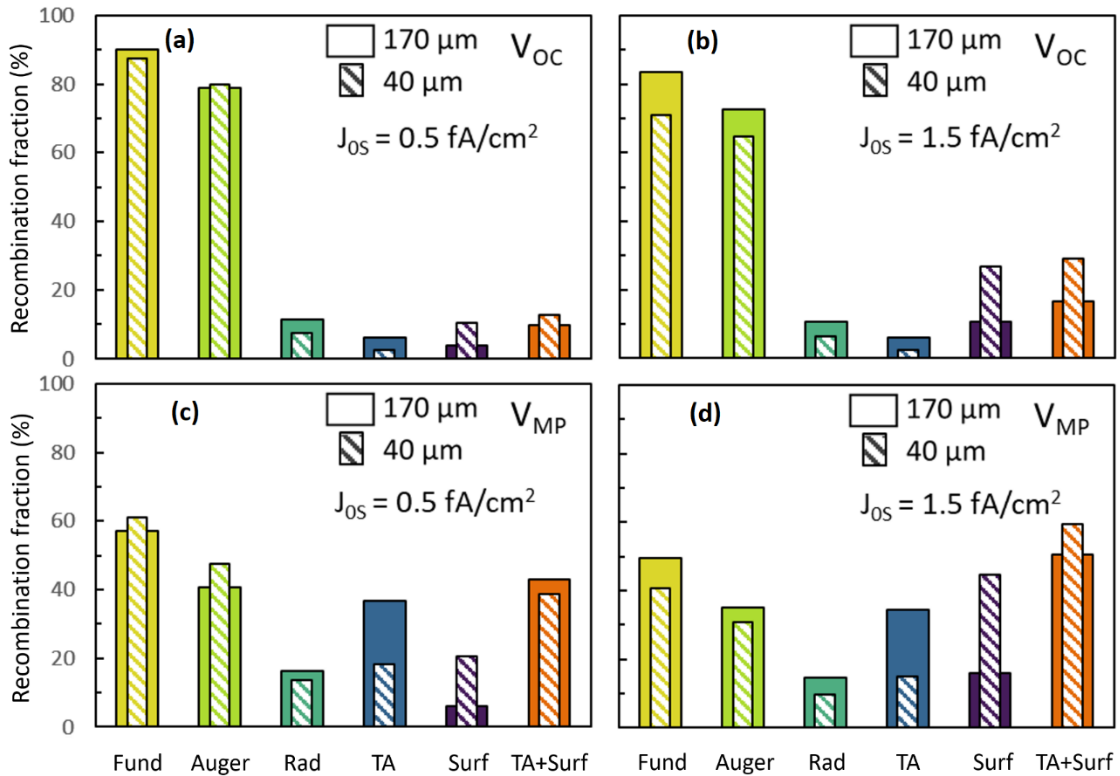

Figure 30: Recombination Fraction Details for Each Recombination Mechanism for 40 μm and 170 μm-Thick Samples for at V_{OC} for (a) J_{0S}=0.5 fA/cm^2 (b) J_{0S}=1.5 fA/cm^2 and at V_{MP} for (c) J_{0S}=0.5 fA/cm^2 (d) J_{0S}=1.5 fA/cm^2

thicker wafer and 70% for the thinner wafer for a J_{0S}=1.5 fA/cm^2, figure 30 (b). The fraction of the trap-assisted and surface recombination is only 10% for J_{0S}=0.5 fA/cm^2 and increases to 20% for the thicker wafer and almost 30% for the thin wafer with an increase of 1 fA/cm^2 in J_{0S}. In contrast, at maximum power voltage (V_{MP}), surface and trap-assisted recombination have considerably higher impact, reducing the overall fraction of fundamental recombination to nearly 60% for the thicker cell and thinner cell for a J_{0S}=0.5 fA/cm^2, figure 30(c). It can also be seen that the fraction of the fundamental recombination is higher for the thinner one when compared to the thinner one due to the improvement in surface saturation current density. For J_{0S}=1.5 fA/cm^2, the fraction of the fundamental recombination is around 50% for the thicker wafer and 40% for the thinner wafer, as shown in figure 30 (d). The total fraction of the trap-assisted and surface recombination is greater than the fundamental recombination for both the thick and thin wafer, figure 30(d). This is expected as the thick wafer is influenced by the higher trap assisted recombination in the bulk whereas the reduction of surface passivation influences the thinner wafer more significantly. There is a 22% decrease in the contribution of surface recombination for the thinner wafer with a change in surface saturation current density from 1.5 fA/cm^2 to 0.5 fA/cm^2 at V_{MP}, figure 30(c) and (d). Although, only an 11% change is observed for the thin wafer at V_{OC} with the decrease J_{0S}. This shows that surface recombination improvements can lead to higher V_{MP} gain than V_{OC} gain as seen in figure 28.

4.7 Accuracy of Lifetime Measurements

Recent work by Black et. al [83] discusses how parameters extracted from lifetime measurements, e.g. J_{0S} and iV_{OC}, can be incorrectly estimated when using an inductively coupled photoconductance decay method [39]. The relative sensitivity of the inductive coil used to measure the sample conductance appears to depend on the silicon wafer thickness. A

linear relationship between the dark voltage measured by the coil and the sample conductance measured by a four-point probe is a good indicator of lifetime measurement accuracy [83].

The variation of sheet conductance varies with excess carrier density and wafer thickness is seen in figure 31(a). For wafer thicknesses between 20 to 160 µm our experimental setup must measure sheet conductance accurately between 0.005 S to 0.09 S. These values correspond to the excess carrier densities of interest to measure the voltage at maximum power and open circuit voltages. To estimate these excess carrier densities, we assumed the fundamental limit of recombination. Samples with a wide range of sheet conductance values were manufactured. Samples with sheet conductance between 0.003 to 0.005 S were manufactured by varying the thickness of bare silicon wafers; for higher values of sheet conductance, we sputtered different

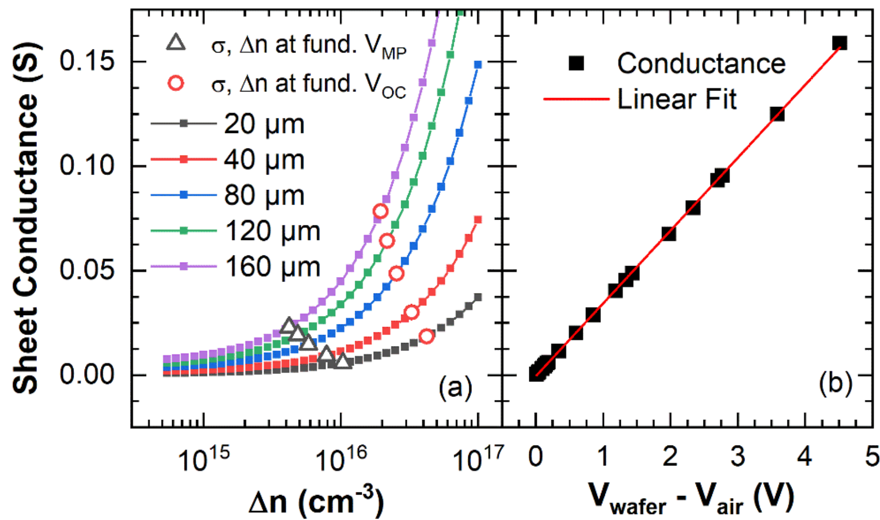

Figure 31: (a) Variation of Sheet Conductance Calculated for N-type Silicon Wafers of Different Thicknesses with a Base Doping of 1.5x10^{15} cm^{-3} at Different Excess Carrier Density. The Triangular Markers Represent The Sheet Conductance Calculated vs Excess Carrier Density (Δn) of Wafers at Their Fundamental V_{MP} Limit and the Red Circular Markers Represent the Same at Their Fundamental V_{OC} Limit. (b) Sheet Conductance Measured by Four-Point-Probe Versus Voltage Measured by the Inductive Coil of the WCT-120 System Obtained Using Samples with Various Resistivities and Thicknesses.

film thicknesses of ITO and aluminum on glass slides. In Figure 31(b), we show that the dark photovoltage measured by the lifetime testers has a linear relationship with the sheet conductance measured using the four-point probe. This is a good indication that the parameters derived from the lifetime measurements are accurate.

5. SHJ SOLAR CELL DEVICE RESULTS

5.1 Baseline vs optimized Process

SHJ solar cells were manufactured using the two intrinsic layers previously described in chapter 4. The I-V characteristics are shown in figure 32. All I-V parameters improved by using the deposition conditions for the intrinsic a-Si:H layer that was described in the previous chapter. The V_{OC} , J_{SC}, FF, and efficiency increase by 5mV, 0.5 mA/cm^2, 2% absolute, and 1% absolute, respectively. The optimized process improves the V_{MP} which also influences the

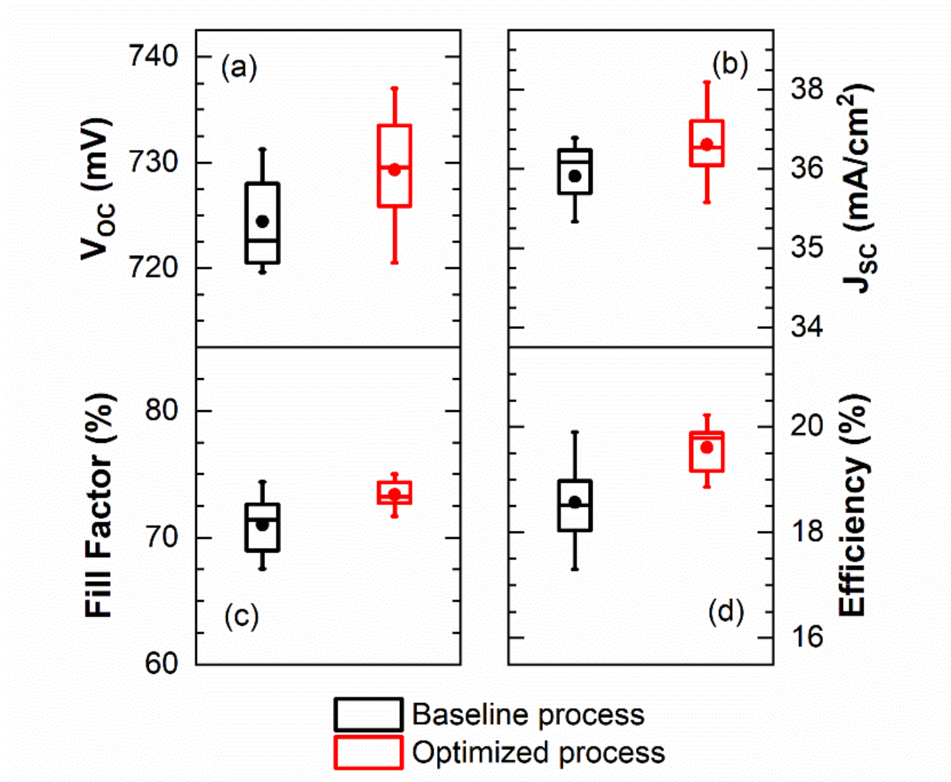

Figure 32: I-V Characteristics of 42±2 μm Thick, 4 cm^2 SHJ Solar Cells Manufactured Using the Intrinsic a-Si:H Layer Baseline and Optimized Processes. The Thickness of Intrinsic a-Si:H Layer is 6 nm for Both the Cases. The V_{OC} (a), J_{SC} (b), FF (c), and Efficiency (d) are Improved with the Optimized Process. The Structure of These Cells is as Represented in Fig. 1(a). The Sample Size was Greater Than 10 for Each Process.

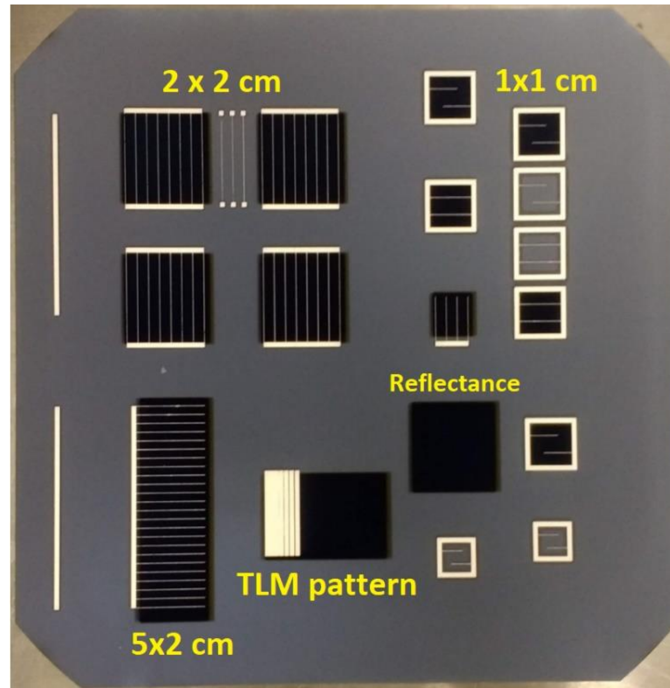

Figure 33: Top View Photo of a Metalized 40 μm Thin SHJ Sample Fabricated on 156 mm Standalone Wafer. The Screen-Printed Devices Have Multiple Patterns and Cells with Different Areas are Fabricated. These Patterns Can Also be Used to Measure the (a) TLM Pattern: Contact Resistance of the Underlying Layers in the Devices and (b) Reflectance of the ARC Layer Deposited on the Top of the SHJ Device to Optimize the Electrical and Optical Properties of the Devices.

gain seen in FF when compared to the baseline process. The variation in J_{SC} can be attributed to non-uniformities in the ITO layer, wafer thickness, variations in the texturing process, and slight deviation in alignment between screen printed samples due to handling. The photo of the metallized SHJ cell pattern is shown in figure 33.

5.2 SiO_x and ITO Stack for Increased Photogeneration

TCO requirements for SHJ solar cells usually include the following [84], [85]: refractive index close to 2.0 to serve as an ARC; transparency from 350 to 1200nm; provide lateral conductivity; achieve ohmic contact with metal electrodes and doped a-Si films; deposition

should not damage the surface passivation; should not cause reliability issues; should not contribute to the degradation and failures in the field. ITO is commonly used on top of doped a-Si:H layers to promote lateral carrier transport, good ohmic contact to metal electrodes, and serve as an antireflective layer. However, ITO also absorbs light in the ultraviolet regime due to its wide bandgap and the infrared regime due to free carrier absorption [86]. By using a stack of thinner-ITO and SiO_2, we can decouple to some extent the antireflective and conductive properties that were provided before by just a single thick, highly absorbent layer of ITO. When compared with ITO, the SiO_2 with an optimal refractive index and thickness has already been established to have low parasitic absorption and good antireflective properties [87]. A thin layer of ITO is enough to provide the necessary carrier transport and ohmic contact, and SiO_2 can be used to complement the antireflective properties.

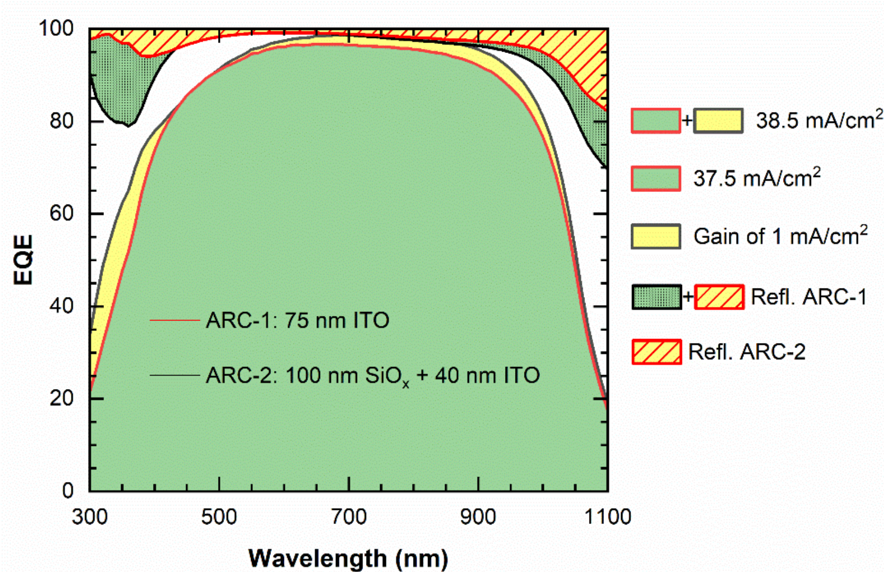

Figure 34: EQE of Representative Samples for the Two Types of Solar Cell Structures Shown in Fig. 11 Using 42±2 μm Thick Textured Wafers. J_{gen} of 37.5 mA/cm^2 Achieved Using 75 nm ITO and 38.6 mA/cm^2 Using SiO_x:ITO Stack. The Optimized Process was Used to Deposit the Intrinsic a-Si:H Layer for These Samples. The Patterned Green and Yellow Shaded Areas on Top of the EQE Curve are the Reflectance Measurements of the Respective ARC Layers.

SHJ solar cells with two anti-reflective coating stacks as shown in figure 11, chapter 3, were manufactured. To mitigate the light absorption, we reduced the thickness of ITO and added a silicon oxide layer to preserve the anti-reflective properties of the cell [85]. In Figure 34, the SiO_x:ITO stack shows an improvement (yellow shaded area) of 1 mA/cm^2 in photogeneration current density (J_{gen}). The J_{gen} for the device was calculated by measuring the external quantum efficiency (EQE). The SiO_x:ITO stack shows a gain in current across a wide range of wavelengths. As compared to the structure (a) of Figure 11, there is an absolute gain of 0.6 mA/cm^2 in the wavelength range of 300-450 nm and an increase of 0.3 mA/cm^2 in the wavelength range of 800-1050 nm by using structure (b) of Figure 11. A comparison between the reflectance measurements, figure 34, shows that the using SiO_x:ITO stack mitigates losses due to ITO, indicated by the patterned green area, mainly 300-400 nm and 900-1100 nm regime.

5.3 Impact of Varying a-Si and Substrate Thickness

A thicker intrinsic a-Si:H layer is expected to deliver better surface passivation leading to higher minority carrier lifetime and open circuit voltage [88]. It has been reported that for thin i-a-Si:H layers, minority carrier lifetime is mainly limited by recombination at the external surfaces whereas for thick layers both the defect density in the substrate as well as the i-a-Si:H layer will limit the minority carrier lifetime [88]. A thick intrinsic a-Si:H layer deposited using two steps to form a bilayer was successfully demonstrated in the past [62]. The idea is to deposit a thin layer, perform the hydrogen plasma treatment and then deposit the rest of the stack. This could promote a better diffusion of hydrogen to the intrinsic a-Si:H/c-Si-interface, enhancing the surface passivation [65]. In this work, a bilayer of intrinsic a-Si:H was formed

by first depositing a 6 nm of intrinsic a-Si:H, followed by hydrogen plasma, and finally a 7 nm of intrinsic a-Si:H was deposited. Figure 35 shows the I-V characteristics of the SHJ solar cells as a function of intrinsic a-Si:H thickness. The best efficiency on a 40±2 μm thick wafer using the optimized process and SiO_x:ITO ARC stack was 20.48%. The V_{OC} of the cells increases with an increase of intrinsic a-Si:H thickness, figure 35 (a). The difference between iV_{OC} and V_{OC} is mitigated when we use a thicker intrinsic layer, figure 35 (a), as the interface is likely to be partially shielded from sputtering damage [89]. The short circuit current density (J_{SC}) decreases slightly as the absorption increases with layer thickness, figure 35 (b). Figure 35 (b) also shows slightly different values of J_{SC} between the 14 nm thick layer and the bilayer (6+7 nm). This slight difference could be related to the fact that the number of samples processed with the bilayer was less than half of any other type of samples since we didn't expect sizable differences between the thick intrinsic a-Si:H and the bilayer samples. Implied fill factors (iFF) greater than 84% were attained for all the SHJ solar cells used in the study. The pseudo fill factor (pFF) increases by 1.3% absolute when a thicker intrinsic layer is deposited. However, thicker layers lead to higher series resistance [90], as seen in figure 35 (c). The fill factor reduces to less than 60% for a thick layer of intrinsic a-Si:H. Implied efficiency (iEff) of the SHJ solar cells was calculated by using the product of iV_{OC}, iFF and J_{gen}, figure 35 (d). Using the recombination limit and the light trapping characteristics of our cells, i.e., the implied voltage parameters and the generation current of our stacked ARC structure respectively, we get implied efficiencies greater than 24% and pseudo efficiencies greater than 23% for all the samples, figure 35 (d). Improvement in carrier selectivity of doped layers, increasing the mobility of the ITO layer, mitigating sputter damage and better front metallization scheme are

some of ways to reduce the difference between pseudo efficiency and the actual efficiency for the SHJ solar cells fabricated in this work.

Although using SiO_x:ITO stack leads to gain in generation current, FF losses were seen due to the reduction of ITO thickness which leads to an increase in sheet resistance of ITO. Thus, three different front ARC structures for SHJ solar cells was re-investigated:

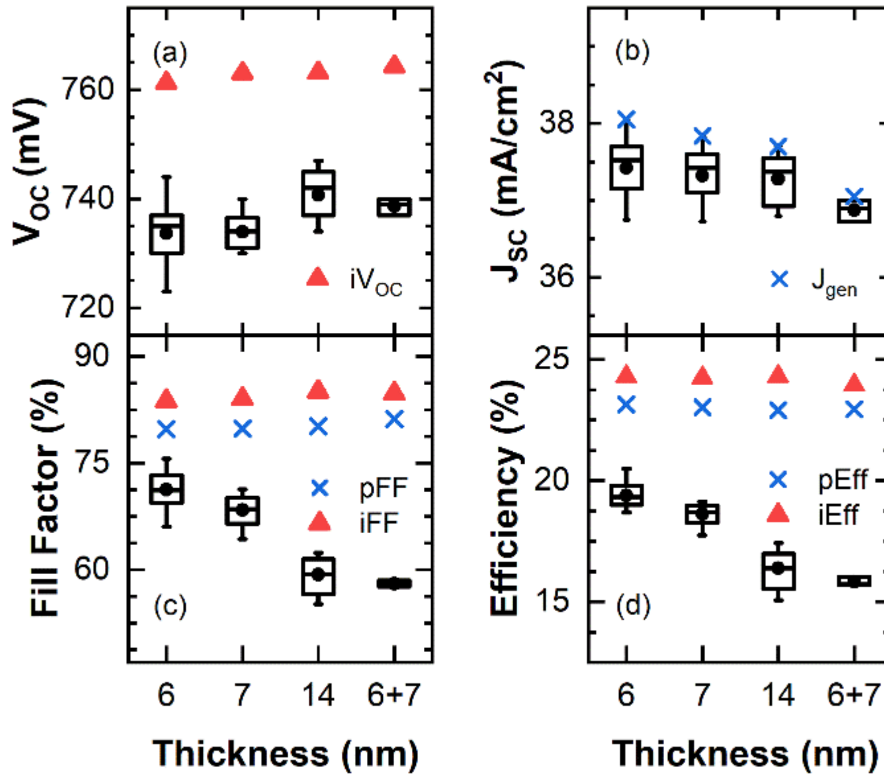

Figure 35: I-V Characteristics of 42±2 µm Thick, 4 cm^2, SHJ Solar Cells as a Function of Intrinsic a-Si:H layer Thickness: a) $V_{OC,}$ the Markers Represent iV_{OC} ; b) J_{SC}, the Markers Represent J_{gen}; c) FF, Where the x Marks Indicate the pFF, the Triangles Indicate Implied Fill Factor (iFF); and d) Efficiency, Where the X Marks Indicate the Average Pseudo Efficiency (pEff) and the Triangles Indicate Implied Efficiency (iEff). The Optimized Process was Used to Deposit Intrinsic a-Si:H for All the Samples. The Structure of These Cells is as Represented in Fig. 11(b). The Sample Size is Greater Than 10 for 6,7, and 14 nm Thick Intrinsic a-Si:H Layer and greater than 4 for a bilayer intrinsic a-Si:H layer Respectively.

- ARC type 1 - 78 nm of ITO
- ARC type 2 - 70 nm of ITO + 50 nm of SiO_2
- ARC type 3 - 40 nm of ITO + 100 nm of SiO_2

A comparison of the EQE of SHJ solar cells with these three different types of ARC structures is shown in figure 23 By using ARC type 2 we gain 0.4 mA/cm^2 in photogeneration current (J_{gen}). With this improvement, we were able to reach an efficiency of 20.69%. SHJ cells with ARC type 3 had an additional gain of 0.75 mA/cm^2 in J_{gen}. As compared to ARC Type 1, there is an absolute gain of 0.647 mA/cm^2 in the wavelength range of 300-450 nm and an increase of 0.334 mA/cm^2 in the wavelength range of 800-1050 nm by using an ARC Type 3 structure.

Table 4 shows a comparison of the best performing 40 µm thin SHJ solar cells using the three different types of ARC structures described above. The efficiency using the ARC type 3

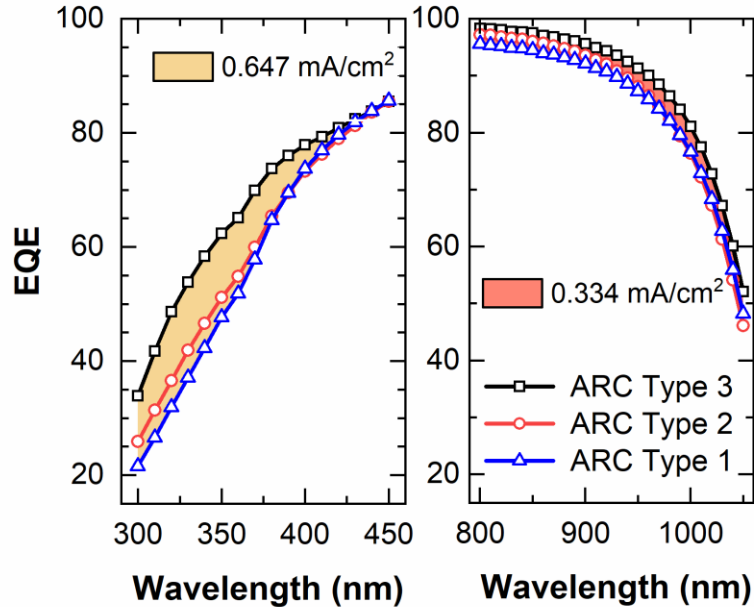

Figure 36: EQE of SHJ Solar Cells with Three Different ARC Structures. Each Type of SHJ Solar Cell is Classified According to Their ARC Structure as Mentioned Before.

structure was 20.48%, which is 0.2% absolute lower efficiency when compared to the ARC type 2 structure as a result of a lower FF (72.3%). There was an increase in J_{SC} (38.26 mA/cm^2), and the V_{OC} was 741 mV. The sheet resistance of ITO changes with film thickness and the

Table 4: Comparison of the I-V Characteristics of the Best SHJ Solar Cells with Three Different Front ARC Structures.

SHJ Cell type	V_{OC} (mV)	J_{gen} (mA/cm^2)	J_{SC} (mA/cm^2)	FF (%)	pFF (%)	η (%)
ARC Type 1	737	37.2	36.5	75.2	81.1	20.25
ARC Type 2	737	37.8	37.17	75.6	80.3	20.69
ARC Type 3	741	38.5	38.26	72.3	81.4	20.48

lower FF can be explained by the higher sheet resistance for a 40 nm thick ITO (90 Ω/•) when compared to the 75 nm thick ITO layer (60 Ω/sqr). Oxygen content in the ITO film can be reduced further to achieve similar sheet resistance as thick ITO films. Hydrogen doped SiO_2 layers can also be used to address the FF losses [85].

To control the accuracy of in-house measurements and to avoid the error introduced in the short circuit current density due to spectral mismatch, a 40 µm thin SHJ calibration solar cell was shipped to NREL. The efficiency measured at NREL was 18.49% and the in-house measurements showed an efficiency of 18.26%. There is a difference of 0.2 mA/cm^2 in J_{SC} (0.2%), 3 mV in V_{OC} (0.4%) and 0.8% in FF (1%) between the NREL and the in-house measurement, figure 37. These errors are within the tolerance limits of the Sinton FCT-450 flash I-V tester. Figure 37 also shows the I-V curve of the best cell measured at SPL with an efficiency of 20.69%.

SHJ cells were also fabricated on substrates with varying substrate thicknesses to examine the trend in I-V characteristics figure 38. The open circuit voltage of the devices increases with decreasing substrate thickness. Comparing the mean values of the distribution of the data points shows a logarithmic increase in V_{OC}. The short circuit current density decreases monotonically with the decrease in substrate thickness. The short circuit current density as described before is limited by the parasitic absorption in the intrinsic and doped a-Si:H layers, the ITO, and Ag layers of the SHJ devices. There is no significant trend observed in the FF of the SHJ devices for varying substrate thicknesses. The average of the distribution rises from 69% to 71% for a substrate thickness of 120 μm to 40 μm, which is largely due to the variations in the uniformity of the underlying a-Si:H and ITO layers, variations in screen printing, and general process variability. There is no significant difference between the efficiencies of 160 μm and 140 μm thick substrates. The average efficiencies of the devices

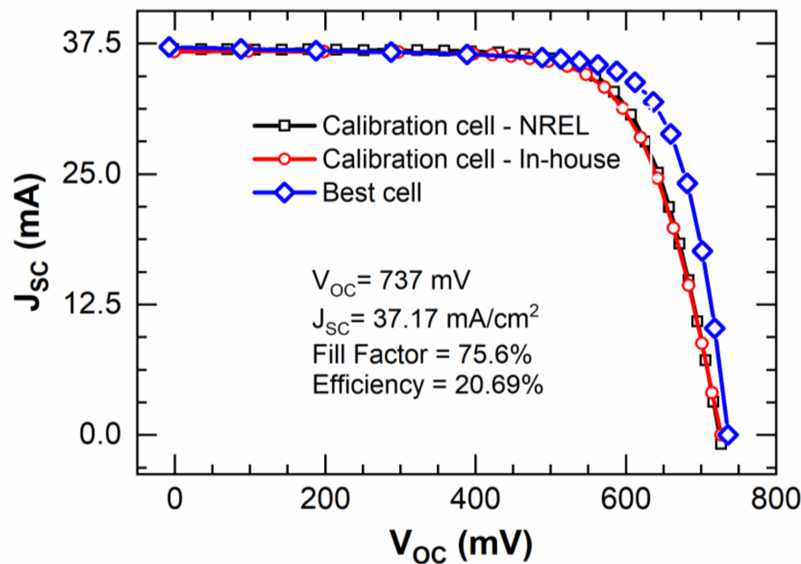

Figure 37: I-V Curves of 40 μm-Thin SHJ Solar Cells. SHJ Calibration Cell Measured at NREL (Eff. 18.49 %) and In-House (Eff. 18.26 %). Blue Curve Shows the I-V Curve of Our Best 40 μm-Thin SHJ Solar Cell with an Efficiency of 20.69 % Measured In-House.

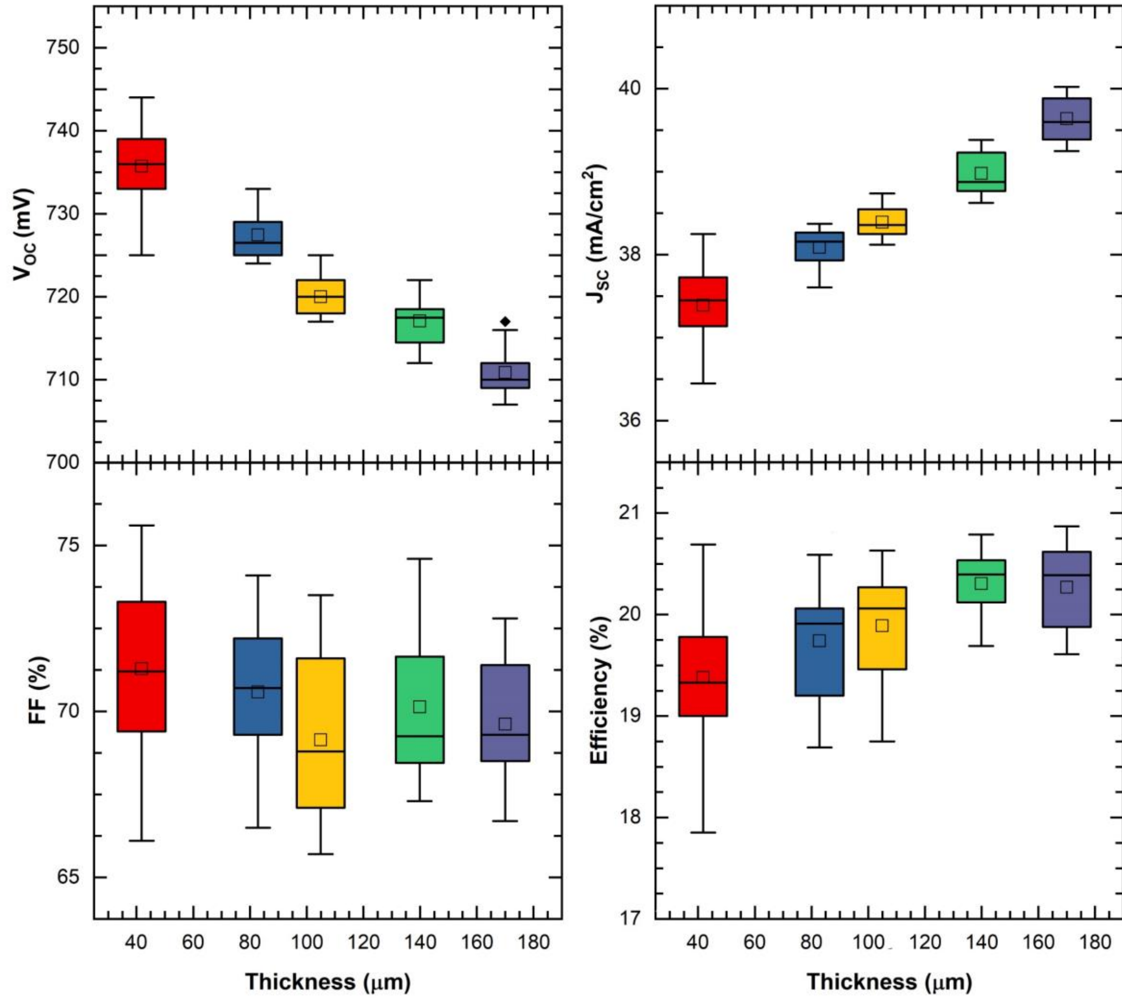

Figure 38: I-V Characteristics of 4 cm^2, SHJ Solar Cells as a Function of Substrate Thickness: (a) V_{OC}, (b) J_{SC}, (c) FF, (d) Efficiency

reduce monotonically with a reduction in substrate thickness. Further analysis and characterization of the device losses are explored in the upcoming chapter.

6. LOSSES IMPACTING DEVICE PERFORMANCE

6.1 Characterization of Losses Due to Varying Substrate Thickness

To enable a better understanding of how these devices perform under real-world conditions, the various energy conversion losses for fabricated SHJ solar cells were quantified for varying substrate thicknesses. The performance of these devices was discussed in the previous chapter. A pathway to make these SHJ devices for varying substrate thickness more efficient, less expensive, and more durable is also outlined at the end of this chapter. A comparison between the fundamental V_{OC}, implied V_{OC} and the actual device V_{OC} is presented in Figure 39 (a). Open circuit voltage of final SHJ devices follows an exponential decay similar to the implied open circuit voltage and the fundamental voltage. The fundamental V_{OC} limit for silicon is calculated according to the details provided in chapter 2. Implied voltages of the devices are obtained using the Sinton lifetime tester, after depositing i-p and i-n a-Si:H layers as seen in section 4.4, chapter 4. A loss of 22 mV at 180 μm and a loss of 30 mV at 40 μm is seen when device V_{OC} is compared to the fundamental limit. The final device current density has a sharper loss compared to the Lambertian limit [40] or the generated model using PV lighthouse. This is expected due to the transmission losses in longer wavelengths and absorption from the ITO layers. Owing to these losses there is a constant decrease in the efficiency with reducing thickness. In figure 39(c), the limiting efficiency of silicon is estimated by setting the FF at 82% (black curve) and 76% (red curve) and a comparison is made to the device limit that can be achieved by the best voltage, current density and fill factors obtained for SHJ devices for different substrate thicknesses fabricated in this work.

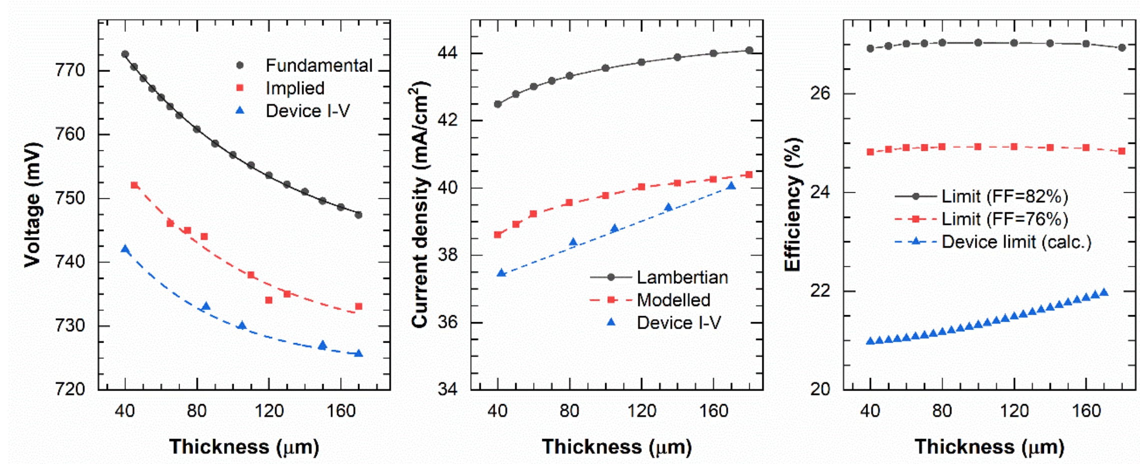

Figure 39: (Data of Cells with Best Efficiencies Only) (a) Comparison of V_{OC}, iV_{OC} and Fundamental V_{OC} of SHJ Devices for Varying Substrate Thickness. The Solid Black Line Represents the Fundamental V_{OC} Limit for Silicon. The Dashed Lines Indicate Logarithmic Fits to the Data to the Implied and Final Device Voltages. (b) Comparison of Short Current Density Obtained by Lambertian Limit, Modeled Using PV-Lighthouse Wafer Ray Tracer and Measurements of the Final SHJ Devices. The Dashed Blue Line Indicates a Linear Fit to the Data. (c) Comparison of Theoretical Efficiency Limit of Silicon for Fill Factors Set at 82 and 76% and Calculated Efficiency Limit for In-House SHJ Devices.

Optical, voltage, and resistive losses were characterized for the SHJ devices fabricated using multiple substrate thicknesses. Voltage losses compared to the fundamental silicon limit are obtained by the difference between the equations obtained by fitting for the data provided in figure 39 (a). Similarly, optical losses compared to the Lambertian limit are obtained by the difference between the fitted equations of the data provided in figure 39 (b). Fill factor (FF_0) is calculated by using well-known empirical equations (34) and (35) where the V_{OC} is the implied V_{OC} obtained as described in previous chapters [91]. To calculate the percentage losses due to series resistance (R_s) and shunt resistance (R_{sh}), we calculate the fill factors FF_s and FF_{sh} according to analytical expressions (38) and (39) [92] and compare it to FF_0. An average

Implied FF (iFF) of 83.5% , measured using the Suns-V_{OC} system, is a better estimate for calculating the device losses for the silicon substrates used to fabricate SHJ cells in this work.

$$v_{OC} = \frac{V_{OC}}{(nkT/q)} \tag{34}$$

$$r_s = \frac{R_s}{V_{OC}/J_{SC}} \tag{35}$$

$$r_{sh} = \frac{R_{sh}}{V_{OC}/J_{SC}} \tag{36}$$

$$FF_0 = \frac{v_{OC} - \ln(v_{OC} + 0.72)}{v_{OC} + 1} \tag{37}$$

$$FF_s = iFF(1 - 1.1r_s) + \frac{{r_s}^2}{5.4} \tag{38}$$

$$FF_{sh} = iFF\left(1 - \left(\frac{v_{OC} + 0.7}{v_{OC}}\right)\left(\frac{FF_0}{r_{sh}}\right)\right) \tag{39}$$

$$FF_T = FF_s\left(1 - \left(\frac{v_{OC} + 0.7}{v_{OC}}\right)\left(\frac{FF_s}{r_{sh}}\right)\right) \tag{40}$$

Voltage losses for SHJ devices fabricated at SPL contribute around 3.8% losses for 170 μm devices and around 3.8% for 40 μm samples. Optical losses contribute around 7.9% for 170 μm devices and increases to 9.9% for 40 μm samples, figure 40. These losses indicate that better optical schemes are required to address the optical losses due to parasitic absorption and transmission losses for very thin silicon substrates than the conventional random pyramid textured scheme. Figure 41 shows the comparison of the EQE data for varying substrate thicknesses. The curves indicate that the monotonous decrease in the short circuit current density is mainly due to the loss of absorption between 850 to 1200 nm regime (IR response). Detailed analysis of the optical loss mechanisms due to the heterojunction layers can be found elsewhere [86]. Very small differences are noticed in the EQE for the range of 300-350 nm,

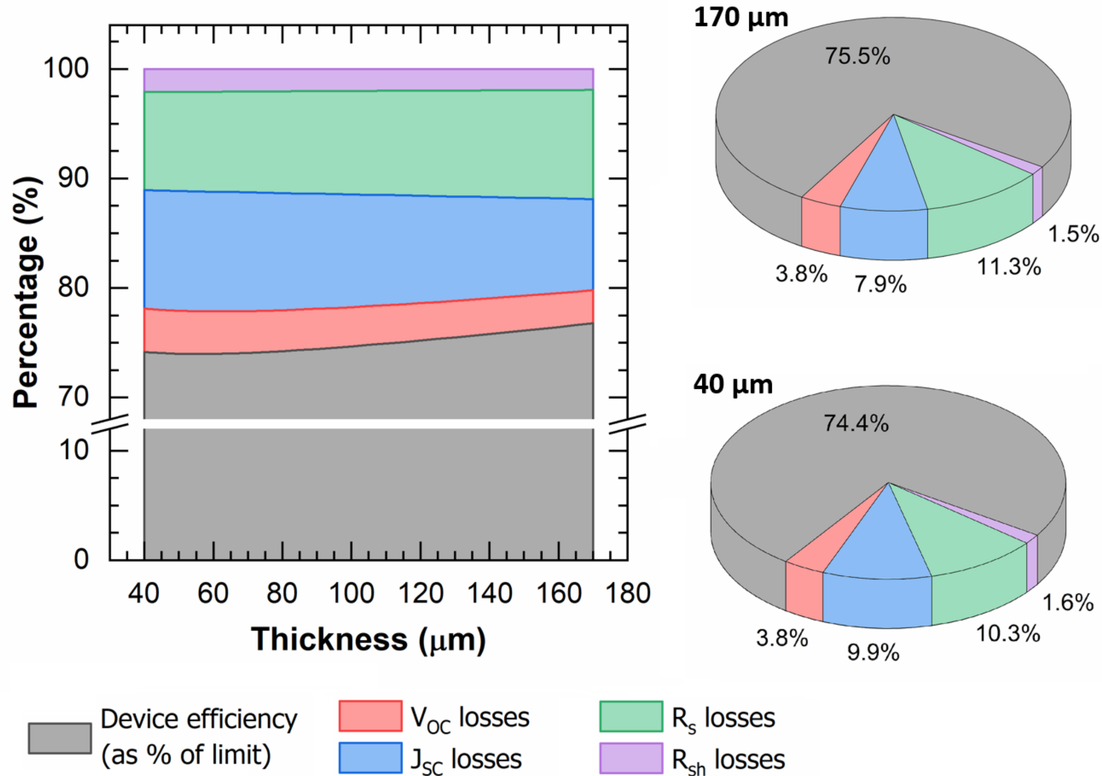

Figure 40: Percentage of Various Device Losses in Comparison to the Silicon Efficiency Limit Calculated Using [11]. The Inset Pie Chart Shows the Device Losses for a 170 and a 40 μm Thin SHJ Solar Cell. The Grey Area Indicates the Current Device Efficiency as a Percentage of the Theoretical Silicon Efficiency Limit for Varying Substrate Thicknesses.

which is mostly due to the non-uniformities introduced in the a-Si:H and ITO layers during the deposition process. One way to mitigate these losses was explored in the previous chapter by using SiO_2:ITO stacks. The impact of the increase in minority carrier injection levels, at the maximum power point, for reducing substrate thicknesses is mostly observed in the losses contributed due to series resistance. The resistance losses decrease from 11.3% for 170 μm devices to 10.3% for 40 μm samples. The losses due to shunt resistance are the least among the factors contributing around 1.5% for 170 μm devices and around 1.6% for 40 μm thin devices.

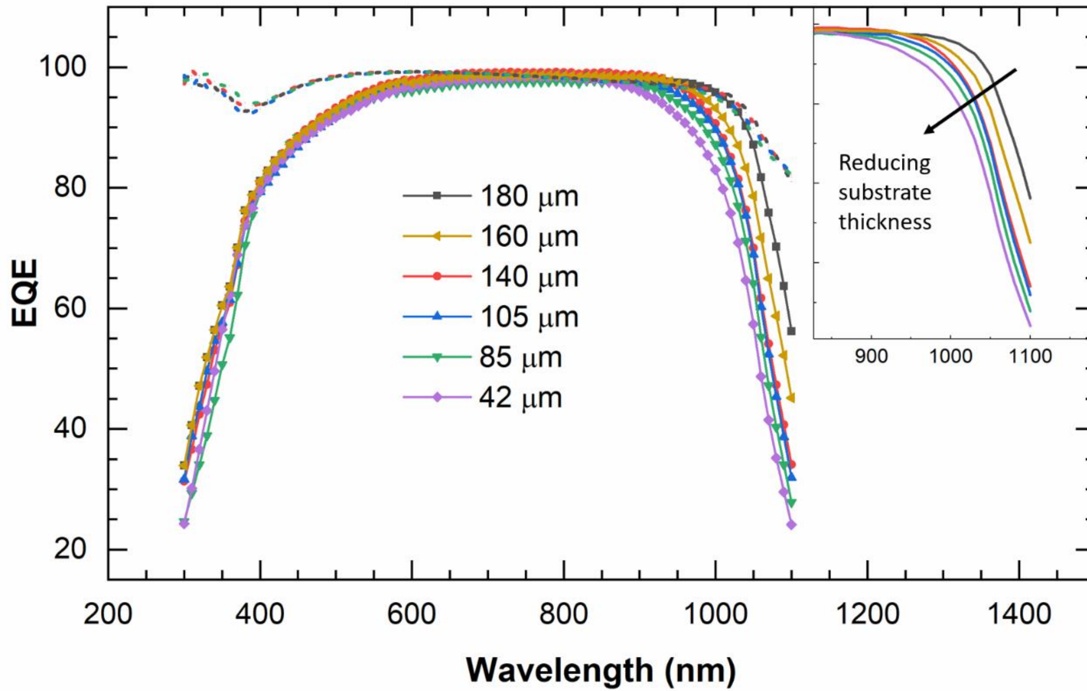

Figure 41: Comparison of EQE of SHJ Devices for Varying Substrate Thicknesses. The Dashed Curves are the Reflectance Measurements of the Devices. ITO is Used as an ARC Layer and the Deposition Conditions are Kept Constant Across These Devices. Inset Graph Shows the Comparison of the Same EQE Measurements for a Wavelength Range of 850-1150 nm Indicating the Absorbance Losses for Reducing Substrate Thickness.

6.2 Impact of Cell Area

The top efficiencies on SHJ solar cells are typically reported on large area solar cells [13], [20], [93], [94]. The reported results of SHJ solar cells in figures in the previous chapters are 4 cm^2 in area. Figure 33 shows the photo/schematic of the SHJ cells that were fabricated. Although we use an opaque mask to avoid illuminating the adjacent area of the cell which is defined by the mask, there exists an electronically active peripheral region within the cell where carrier recombination occurs, figure 42. This active region leads to losses in voltage that impact the overall performance of the SHJ cell. We manufactured solar cells with two different areas

and similar implied I-V parameters to evaluate the impact of the area on the cell performance, and the results are provided in Table 5. The larger cell shows lower V_{OC} loss and higher pFF. Since both the cells experienced the same manufacturing process, the only difference is the ratio of cell perimeter to the cell area. This seems to indicate that smaller cells, that is, those with a larger perimeter-to-cell-area ratio, have larger edge recombination, similar to other work found in the literature [95]. The difference in iV_{OC} and V_{OC} can also be attributed in part to the sputtering damage which results in the loss of surface passivation [89]. According to the values shown in Table 5, about 87% of the difference between the pFF and FF is caused by the series resistance. The R_S values are obtained from the Sinton I-V measurement tool.

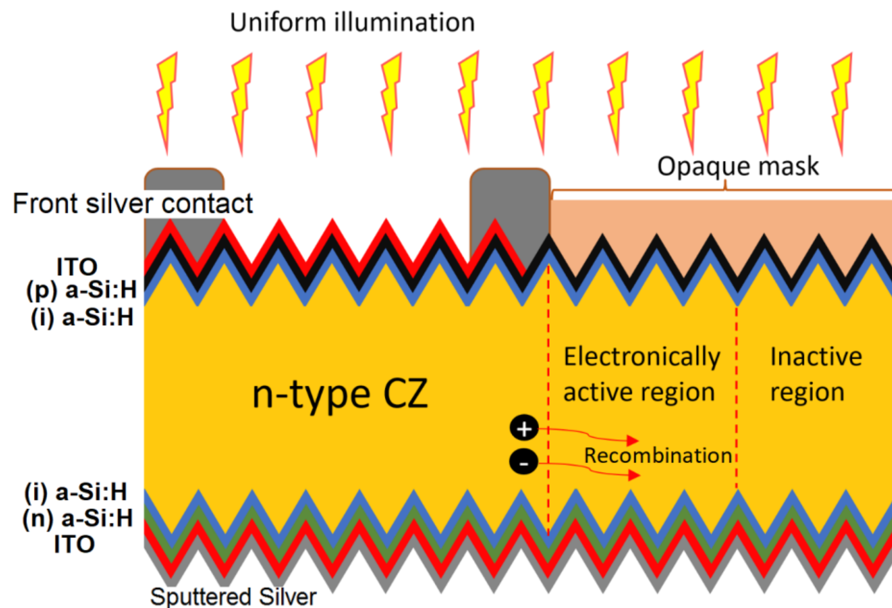

Figure 42: Schematic of the 4 cm^2 SHJ Cells That are Fabricated on 156 mm Wafers. An Opaque Mask Which has an Area of 4 cm^2 is Used to Cover the Area from Illumination. Recombination is Possible in the Peripheral Area as Shown Leading to Voltage Losses.

Photoluminescence imaging of solar cells at short-circuit conditions can also be used to measure the diffusion of carriers at the edge of the cell area. PL counts (C_{PL}) are directly proportional to the np-product and thus related to the diode voltage (V_d) as:

$$C_{PL} \propto np \propto \Delta\mathrm{n}(\Delta\mathrm{n} + N_d) \propto n_{i,eff}^2 \exp\left(\frac{qV_d}{kT}\right)$$

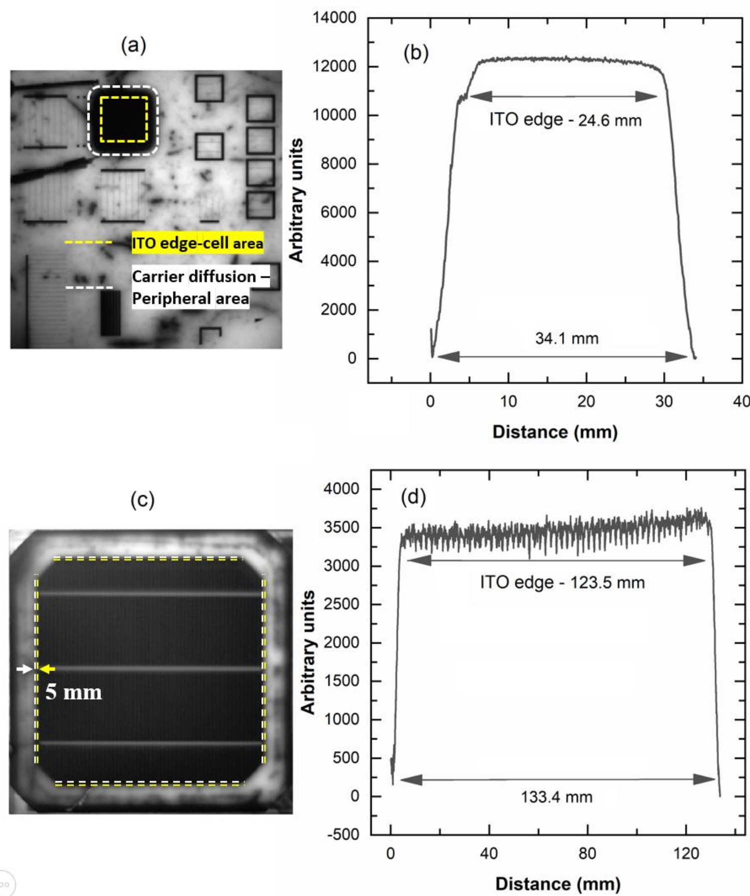

Figure 43: PL Image of 6 cm^2 SHJ Solar Cell Under Short Circuit Condition. (b) Representative PL Intensity Linescan Across the 6 cm^2 Device Which Shows Minority Carriers Diffuse at Least 5 mm from the Edge of the Device. (c) PL Image of 150.3 cm^2 SHJ Solar Cell Under Short Circuit Condition. (d) Representative PL Intensity Linescan Across the 150.3 cm^2 Device has Minority Carriers that Diffuse at Least 5 mm from the Edge of the Device. It is to be Noted that PL Linescans, (b) & (d) have Undergone Translational Transformation.

where the details of these parameters are provided in chapter 2. Figure 43 (a), (c) represents a PL image of the 6 cm^2 device and 150.3 cm^2 device under short-circuit conditions, respectively. Figure 43 (b), (d) is a representative linescan of PL intensity across the devices respectively and we see carriers diffusing at least 5 mm for both cases when compared to the edge of the ITO layer on the device. The section of the PL linescan till the edge of the ITO, is proportional to the V_{OC} measured when the entire substrate is illuminated. When using a measurement mask, there is the diffusion of carriers along the edges which is proportional to the diffusion of carriers at the edges under short circuit conditions. The loss of voltage due to the diffusion of carriers around the edge of the solar cell can be estimated using calibrated PL images.

Measured V_{OC} values for a 6 cm^2 square SHJ solar cell with and without masking are 725 mV and 735 mV respectively. Measured V_{OC} values for a 150.3 cm^2 pseudo-square SHJ solar cell with and without masking are 742 mV and 739 mV respectively. These results are a good indication that smaller cells that have a larger cell perimeter-to-area ratio, have larger edge recombination [95]. We demonstrate that the edge losses decrease with the decrease in the ratio of cell perimeter-to-area. A change in the cell area from 6 cm^2 to 150.3 cm^2 led to a voltage gain of 7 mV. When measuring voltage with and without a mask, a difference of 10 mV is seen for 6 cm^2 SHJ solar cells. This reduces to 3 mV for an area of 150.3 cm^2. It is demonstrated that PL imaging at short-circuit conditions is a promising technique to quantify the voltage losses from the edge of solar cells. Figure 44 also shows a comparison between the masked and unmasked measurements for thick and thin SHJ cells for varying illumination intensities. We see an average voltage difference of 5 mV for 160 μm cells and an average voltage difference of 10 mV for 40 μm cells at an illumination intensity of 1 sun. This voltage

Table 5: Comparison of 42±2 μm Thick SHJ Solar Cells of Different Areas but with Similar Effective Minority Carrier Lifetimes at $3x10^{15}$ cm^{-3}. τ_{eff}, iV_{OC} and iFF Were Measured on p-i/c-Si/i-n Structures. V_{OC}, pFF, FF, J_{SC}, R_S and Efficiency Were Measured on Completed SHJ Solar Cells. The J_{SC} Values for the First Two Solar Cells Shown Here are Lower Than in Figure 35 Because the SiO_x:ITO Stack Was Not Incorporated in This Experiment.

Cell area (cm^2)	**τ_{eff} (μs)**	**iV_{OC} (mV)**	**iFF (%)**	**V_{OC} (mV)**	**pFF (%)**	**FF (%)**	**J_{SC} (mA/cm^2)**	**R_S (Ω cm^2)**	**Eff (%)**
153.9	1440	764	83.7	747	82.4	75.7	34.0	1.57	19.22
4	1432	764	83.7	740	80.8	73.5	36.4	1.60	19.80
4*	1767	761	85.0	741	81.4	72.3	38.3	1.99	20.48

*Represents the best SHJ solar cell using SiO_x:ITO ARC stack figure 11(b).

difference increases to an average of 7 mV for 160 μm cells and 12 mV for 40 μm cells at an illumination intensity of 0.1 suns. An illumination intensity of 0.1 suns is close to the injection

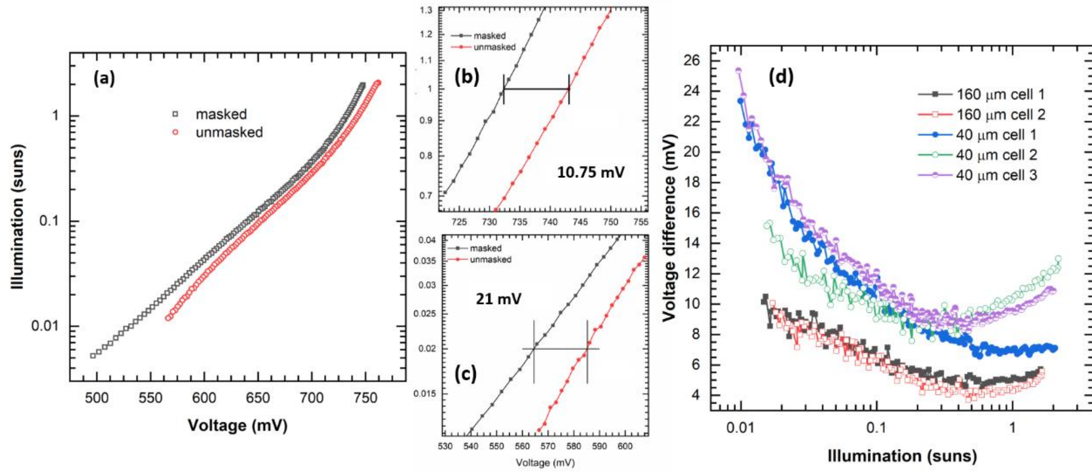

Figure 44: (a) Illumination vs Voltage Measurement of 40 μm Thin Cell with and Without a Mask, Measured Using the Suns-V_{OC} System. (b) Difference in Voltage Between the Measurements at an Illumination of 1 sun. (c) Difference in Voltage Between the Measurements at an Illumination of 0.02 sun. (d) Comparison of the Voltage Differences Observed for 160 and 40 μm Thick Cells for Varying Illumination Intensities.

level at maximum power point. This trend can be explained by the recombination fractions that were modeled in section 4.8, chapter 4. Thinner wafers operating at V_{MP} are more susceptible to peripheral recombination when compared to thicker wafers. A 5mV difference for 160 μm thick cell contributes to around 21% of the V_{OC} losses and 0.65% to the total efficiency losses seen in figure 40. A 10mV difference contributes to around 33% of the V_{OC} losses and 1.35% to the total efficiency losses seen in figure 40 for a 40 μm thick cell.

6.1 Sputtering Damage to Surface Passivation

The τ_{eff} of passivated wafers decreased drastically after sputtering, regardless of different intensities of DC plasma power, Figure 45 (b). One of the reasons could be that there is a threshold of energy required to break bonds, and higher energies have no additional impact [74]. To determine if the ITO layer affects τ_{eff} measurement, some of the samples were dipped in 15% HCl to etch the ITO away before remeasuring τ_{eff}. Acquiring PL images after each processing step showed the changes in τ_{eff} over the entire wafer, Figure 45. Since τ_{eff} did not

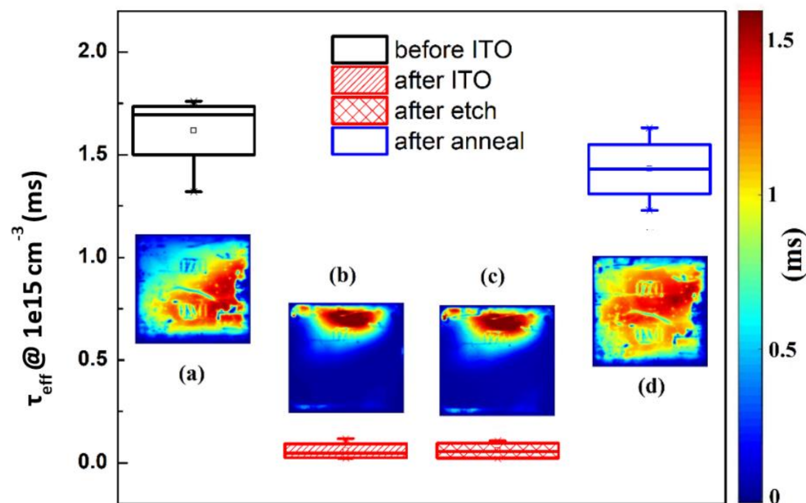

Figure 45: Carrier Lifetime and PL Images (a) Before ITO, (b) After ITO, (c) After HCl Dip and (d) After Annealing.

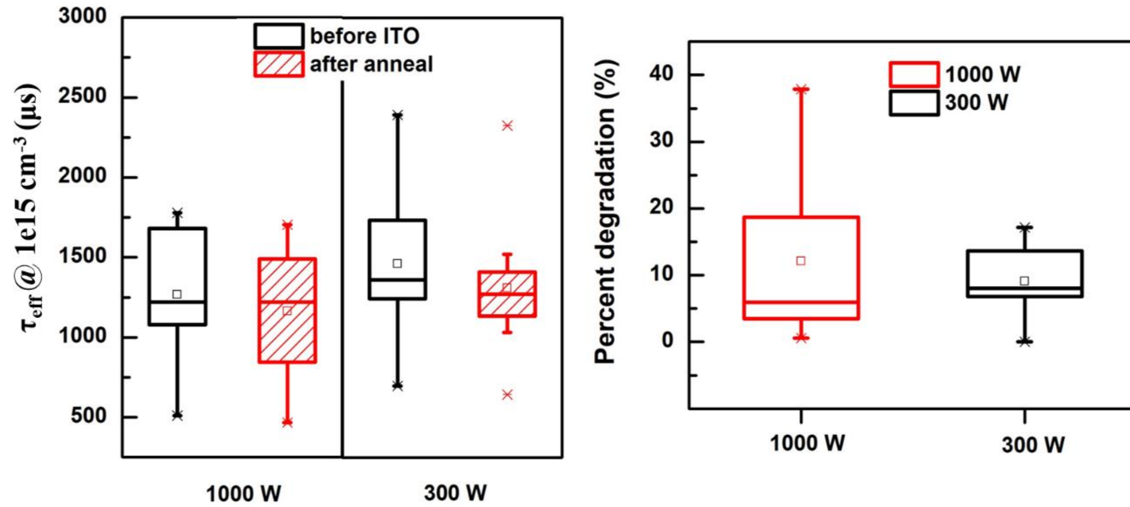

Figure 46: (Left) τ_{eff} of Wafers Before and After ITO Sputtering for Two Different DC Plasma Powers. (Right) Percentage Degradation in τ_{eff} Before Sputtering ITO and After Annealing Them to Recover τ_{eff}.

change after the etch, it was determined that this parameter can be measured accurately even with the presence of ITO layers. Although, τ_{eff} can be recovered partially by annealing we still see a discernible degradation Figure 48. The use of DC plasma power >1 kW showed higher degradation in minority carrier lifetime when compared to plasma power <300 W, Figure 48. The exposure time to the plasma also plays an important factor in reducing the damage on these wafers [96]. By 70% reduction in the DC plasma power, we can mitigate the sputtering damage, from a maximum of 38% down to 17%, and increase the reliability of the process.

6.2 Impact of Controlled Laser Induced Defects

Although a lot of care is taken to achieve high quality silicon surfaces for fabricating SHJ solar cells, areas of high recombination are not unavoidable. To study the effect of these high recombination areas on device performance, a quantitative investigation was carried out by comparing the characteristics of devices with no induced defects and devices with controlled

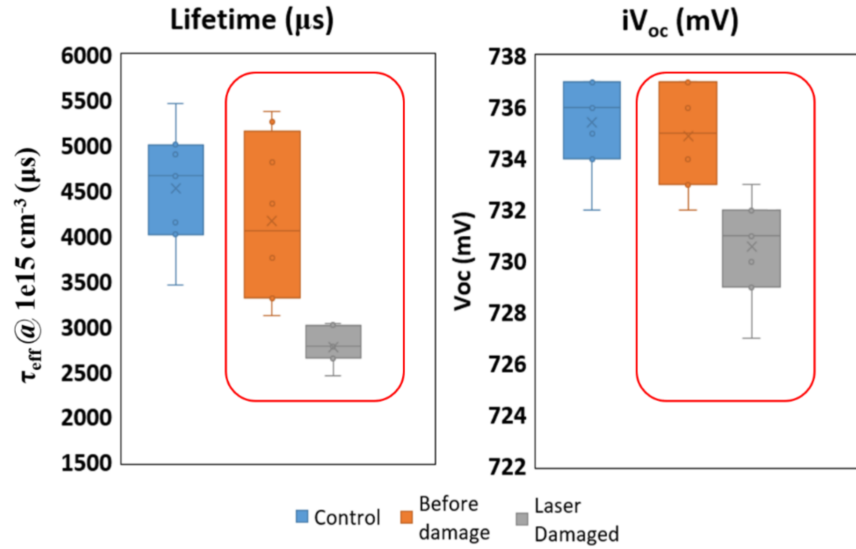

Figure 47: Minority Carrier Lifetime of p-i/c-Si/i-n Deposited Samples Using 170 µm Thick Substrates and iV_{OC} of Wafers Before Metallization

distribution of laser induced defects. SHJ cells were fabricated using a 170 µm thick substrate for these experiments. The area of these laser induced defects which mimic the areas of high recombination can be determined through PL images. Seven samples went through the standard silicon heterojunction solar cell process as described above and seven other wafers went through the process with laser induced defects on their surfaces. The effective minority carrier lifetime and implied open circuit voltage (iV_{OC}) of these sets of wafers are all in the same order, Figure 47, of 4.5 ms and 735 mV respectively before damage at an injection level of 10^{15} cm^{-3}. The average lifetime and iV_{OC} of the wafers decrease to 2.8 ms and 731 mV respectively after laser induced damage. A change in 1.7 ms lifetime corresponds to almost 37% change from the initial value. The average emitter saturation current density (J_{0e}) increased from 1.8 fA/cm^2 to 3.1 fA/cm^2. Sputtering of ITO is known to induce damage on the surface of wafers reducing the carrier lifetimes [97]. Minority carrier lifetimes were recovered by annealing the samples at 200 °C for 30 minutes. Areas of high recombination, when quantified

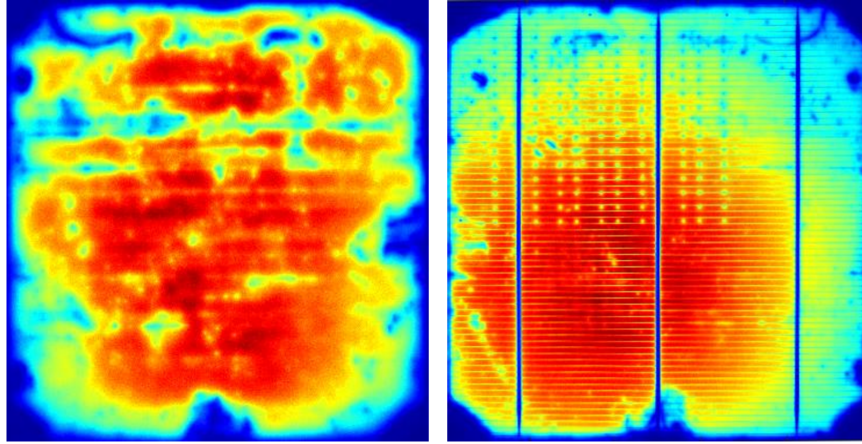

Figure 48: Representative PL Images of The Samples That Were Used for This Study (left) Passivated Wafer (right) Metalized Wafer with Laser Induced Defects.

using PL images, tend to reduce significantly after the deposition of ITO, Figure 48. Lateral transport of photogenerated carriers in the ITO layer can be the reason for this [98]. After metallization, parameters such as short circuit current density J_{SC}, open circuit voltage, voltage and current at maximum power point, fill factor, were extracted for each cell. Figure 49 shows a comparison of these parameters for control samples and the induced damaged devices.

The average efficiency of the control samples was at 18.6% and the average of the damaged ones was at 18.1%, i.e., a relative decrease of 2% in the efficiency. It is evident from the I-V characteristics that the induced defects did not have any considerable change on the short circuit current density of the wafers, which can be expected since the damaged area is around 1% of the total area. There is a relative change of only 0.5% or 4mV on the V_{OC}. The biggest impact of the damages was seen at V_{MP}, with a difference of 13 mV, i.e. a relative change of 2%, although there was no appreciable change in the J_{MP} of the cell. There was an absolute 2% loss in the fill factor between them. These factors correspond to an absolute loss of 0.12 W per cell, a relative loss of 8% per cell. Using calibrated photoluminescence images we can

spatially resolve lifetime, V_{OC}, and J_{0e} images of cells at various stages of processing, which can be further used to model and predict the efficiencies of wafers before metallization [55], [97]. An area of 2% of defects on a silicon wafer can lead to an 8% relative loss in power generated from the device. Also, V_{MP} shows a drop of 13 mV and negligible change in J_{SC} after the induced damages. These results indicate that each damaged area can be treated as diodes connected in series that bring down the total voltage at open circuit and maximum power point across the device. As shown in section 4.8 chapter 4, thinner cells are much more susceptible to surface recombination which leads to the conclusion that differences observed for these devices will be much more pronounced for thinner SHJ cells.

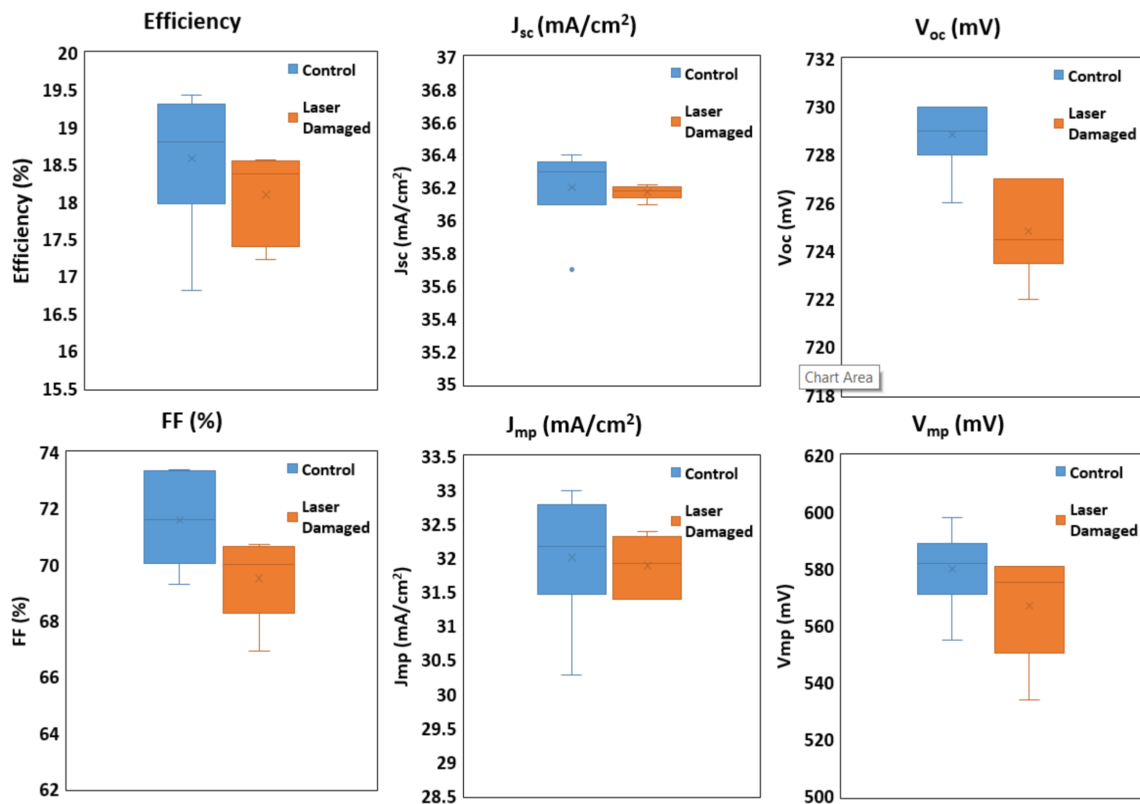

Figure 49: I-V Characteristics of the Metallized Samples. The Blue Box Plot Represents Cells That Did Not Undergo Laser Induced Defects and the Orange Box Represents the Samples That Did Undergo the Induced Defects.

7. SUMMARY AND CONCLUSIONS

In this work, the potential of very thin SHJ solar cells was examined both experimentally and through analytical modeling. It was demonstrated by modeling that for commercially viable solar-grade silicon with the total surface saturation current density $J_{0S} < 0.5$ fAcm^{-2} and n-type bulk minority-carrier lifetime of 10 ms, the calculated optimum wafer thickness is between 40–60 μm. Modifying the deposition parameters of the intrinsic a-Si:H led to improvements in surface saturation current density, implied voltages at maximum power, and open circuit across the entire range of wafer thicknesses considered in this study.

An average surface saturation current density of 0.6 fA/cm^2 was accomplished using the new process, reducing the surface saturation current density by half compared to the baseline process. The implied voltage at maximum power and open circuit improved by an average of 21 mV and 8 mV, respectively. Implied open circuit voltage over 760 mV and implied fill factors above 85% were measured on i-p/i-n stacks deposited on 40 μm thick wafers. It was successfully demonstrated experimentally the potential to exceed 21% efficiency using screen printed 40 μm thick silicon heterojunction solar cells. It was also established that standard industrial processes can be used to manufacture large area (>120 cm^2) SHJ solar cells using 40 μm silicon wafers.

Further efficiency improvements need to address losses in open circuit voltage and fill factor. The edge losses decrease with the decrease in the ratio of cell perimeter-to-area. A change in the cell area from 6 cm^2 to 150.3 cm^2 led to a voltage gain of 7 mV. The results also suggest that losses are in part related to the damage induced during the sputtering process of ITO. Lowering the power while sputtering can only lead to a controlled recovery of minority carrier lifetime and not complete recovery. A 2% area of high surface recombination can lead

to a relative decrease of 2% in the cell efficiency and a relative loss of 8% in power for a 170 μm thick SHJ solar cell. The FF losses are largely driven by the series resistance that can be partially improved by a better metallization design and improving the mobility of the ITO layer. The contact resistance between the p-type a-Si layer and the ITO layer should also be addressed for further efficiency improvements.

REFERENCES

[1] R. G. Newell, D. Raimi, S. Villanueva, and B. Prest, "Global Energy Outlook 2020: Energy Transition or Energy Addition?," p. 58.

[2] B. Looney, "Statistical Review of World Energy." 69th edition, 2020.

[3] S. Solomon, G.-K. Plattner, R. Knutti, and P. Friedlingstein, "Irreversible climate change due to carbon dioxide emissions," *PNAS*, vol. 106, no. 6, pp. 1704–1709, Feb. 2009, doi: 10.1073/pnas.0812721106.

[4] "The Paris Agreement." United Nations, Dec. 2015. [Online]. Available: https://unfccc.int/sites/default/files/english_paris_agreement.pdf

[5] "International Energy Outlook 2019," p. 85.

[6] J. Trube, "International Technology Roadmap for Photovoltaic (ITRPV)." VDMA Photovoltaic Equipment, Apr. 2020. [Online]. Available: itrpv.vdma.org

[7] R. Ohl, "Light-sensitive electric device," U.S. Patent No. 2,402,662, Jun. 25, 1946

[8] D. M. Chapin, C. S. Fuller, and G. L. Pearson, "A New Silicon p-n Junction Photocell for Converting Solar Radiation into Electrical Power," p. 3.

[9] M. A. Green, E. D. Dunlop, J. Hohl-Ebinger, M. Yoshita, N. Kopidakis, and X. Hao, "Solar cell efficiency tables (version 56)," *Prog Photovolt Res Appl*, vol. 28, no. 7, pp. 629–638, Jul. 2020, doi: 10.1002/pip.3303.

[10] A. W. Blakers, A. Wang, A. M. Milne, J. Zhao, and M. A. Green, "22.8% efficient silicon solar cell," *Appl. Phys. Lett.*, vol. 55, no. 13, pp. 1363–1365, Sep. 1989, doi: 10.1063/1.101596.

[11] "LONGi Solar 2019." [Online]. Available: https://en.longi-solar.com/home/events/press_detail/id/89.html

[12] D. Adachi, J. L. Hernández, and K. Yamamoto, "Impact of carrier recombination on fill factor for large area heterojunction crystalline silicon solar cell with 25.1% efficiency," *Appl. Phys. Lett.*, vol. 107, no. 23, p. 233506, Dec. 2015, doi: 10.1063/1.4937224.

[13] K. Yoshikawa *et al.*, "Silicon heterojunction solar cell with interdigitated back contacts for a photoconversion efficiency over 26%," *Nat Energy*, vol. 2, no. 5, p. 17032, May 2017, doi: 10.1038/nenergy.2017.32.

[14] A. Richter, J. Benick, F. Feldmann, A. Fell, M. Hermle, and S. W. Glunz, "n-Type Si solar cells with passivating electron contact: Identifying sources for efficiency

limitations by wafer thickness and resistivity variation," *Solar Energy Materials and Solar Cells*, vol. 173, pp. 96–105, Dec. 2017, doi: 10.1016/j.solmat.2017.05.042.

[15] C. Hollemann, F. Haase, S. Schäfer, J. Krügener, R. Brendel, and R. Peibst, "26.1%-efficient POLO-IBC cells: Quantification of electrical and optical loss mechanisms," *Progress in Photovoltaics: Research and Applications*, vol. 27, no. 11, pp. 950–958, 2019, doi: 10.1002/pip.3098.

[16] R. Chen *et al.*, "23.83% efficient mono-PERC incorporating advanced hydrogenation," *Prog Photovolt Res Appl*, vol. 28, no. 12, pp. 1239–1247, Dec. 2020, doi: 10.1002/pip.3243.

[17] A. Richter *et al.*, "Design rules for high-efficiency both-sides-contacted silicon solar cells with balanced charge carrier transport and recombination losses," *Nat Energy*, vol. 6, no. 4, pp. 429–438, Apr. 2021, doi: 10.1038/s41560-021-00805-w.

[18] K. Okuda, H. Okamoto, and Y. Hamakawa, "Amorphous Si/Polycrystalline Si Stacked Solar Cell Having More Than 12% Conversion Efficiency," *Jpn. J. Appl. Phys.*, vol. 22, no. Part 2, No. 9, pp. L605–L607, Sep. 1983, doi: 10.1143/JJAP.22.L605.

[19] M. Tanaka *et al.*, "Development of New a-Si/c-Si Heterojunction Solar Cells: ACJ-HIT (Artificially Constructed Junction-Heterojunction with Intrinsic Thin-Layer)," *Japanese Journal of Applied Physics*, vol. 31, no. Part 1, No. 11, pp. 3518–3522, Nov. 1992, doi: 10.1143/jjap.31.3518.

[20] A. Louwen, W. van Sark, R. Schropp, and A. Faaij, "A cost roadmap for silicon heterojunction solar cells," *Solar Energy Materials and Solar Cells*, vol. 147, pp. 295–314, Apr. 2016, doi: 10.1016/j.solmat.2015.12.026.

[21] Z. Liu *et al.*, "Revisiting thin silicon for photovoltaics: a technoeconomic perspective," *Energy & Environmental Science*, vol. 13, no. 1, pp. 12–23, 2020, doi: 10.1039/C9EE02452B.

[22] P. Heinstein, C. Ballif, and L.-E. Perret-Aebi, "Building Integrated Photovoltaics (BIPV): Review, Potentials, Barriers and Myths," *Green*, vol. 3, no. 2, Jan. 2013, doi: 10.1515/green-2013-0020.

[23] "SBM Solar." http://sbmsolar.com/home/sbm_solar-home.php

[24] "Solbian Solar." http://www.solbian.eu/index.php?lang=en

[25] A. R. Bhatti, Z. Salam, M. J. B. A. Aziz, and K. P. Yee, "A critical review of electric vehicle charging using solar photovoltaic: A critical review of PV-EV charging," *Int. J. Energy Res.*, vol. 40, no. 4, pp. 439–461, Mar. 2016, doi: 10.1002/er.3472.

[26] A. Hangleiter and R. Häcker, "Enhancement of band-to-band Auger recombination by electron-hole correlations," *Phys. Rev. Lett.*, vol. 65, no. 2, pp. 215–218, Jul. 1990, doi: 10.1103/PhysRevLett.65.215.

[27] P. P. Altermatt, J. Schmidt, G. Heiser, and A. G. Aberle, "Assessment and parameterisation of Coulomb-enhanced Auger recombination coefficients in lowly injected crystalline silicon," *Journal of Applied Physics*, vol. 82, no. 10, pp. 4938–4944, Nov. 1997, doi: 10.1063/1.366360.

[28] A. Richter, S. W. Glunz, F. Werner, J. Schmidt, and A. Cuevas, "Improved quantitative description of Auger recombination in crystalline silicon," *Physical Review B - Condensed Matter and Materials Physics*, vol. 86, no. 16, 2012, doi: 10.1103/PhysRevB.86.165202.

[29] A. Schenk, "Finite-temperature full random-phase approximation model of band gap narrowing for silicon device simulation," *Journal of Applied Physics*, vol. 84, no. 7, pp. 3684–3695, Oct. 1998, doi: 10.1063/1.368545.

[30] T. Trupke *et al.*, "Temperature dependence of the radiative recombination coefficient of intrinsic crystalline silicon," *J. Appl. Phys.*, vol. 94, no. 8, p. 4930, 2003, doi: 10.1063/1.1610231.

[31] P. P. Altermatt, F. Geelhaar, T. Trupke, X. Dai, A. Neisser, and E. Daub, "Injection dependence of spontaneous radiative recombination in c-Si: experiment, theoretical analysis, and simulation," in *NUSOD '05. Proceedings of the 5th International Conference on Numerical Simulation of Optoelectronic Devices, 2005.*, Berlin, Germany, 2005, pp. 47–48. doi: 10.1109/NUSOD.2005.1518128.

[32] K. R. McIntosh and L. E. Black, "On effective surface recombination parameters," *Journal of Applied Physics*, vol. 116, no. 1, p. 014503, Jul. 2014, doi: 10.1063/1.4886595.

[33] J. A. del Alamo and R. M. Swanson, "The physics and modeling of heavily doped emitters," *IEEE Transactions on Electron Devices*, vol. 31, no. 12, pp. 1878–1888, Dec. 1984, doi: 10.1109/T-ED.1984.21805.

[34] P. P. Altermatt, A. Schenk, F. Geelhaar, and G. Heiser, "Reassessment of the intrinsic carrier density in crystalline silicon in view of band-gap narrowing," *Journal of Applied Physics*, vol. 93, no. 3, pp. 1598–1604, Feb. 2003, doi: 10.1063/1.1529297.

[35] A. Richter, M. Hermle, and S. W. Glunz, "Reassessment of the limiting efficiency for crystalline silicon solar cells," *IEEE Journal of Photovoltaics*, vol. 3, no. 4, pp. 1184–1191, 2013, doi: 10.1109/JPHOTOV.2013.2270351.

[36] M. J. Kerr, A. Cuevas, and P. Campbell, "Limiting efficiency of crystalline silicon solar cells due to Coulomb-enhanced Auger recombination," *Prog. Photovolt: Res. Appl.*, vol. 11, no. 2, pp. 97–104, Mar. 2003, doi: 10.1002/pip.464.

[37] M. A. Green, "Limits on the open-circuit voltage and efficiency of silicon solar cells imposed by intrinsic Auger processes," *IEEE Trans. Electron Devices*, vol. 31, no. 5, pp. 671–678, May 1984, doi: 10.1109/T-ED.1984.21588.

[38] T. Tiedje, E. Yablonovitch, G. D. Cody, and B. G. Brooks, "Limiting efficiency of silicon solar cells," *IEEE Trans. Electron Devices*, vol. 31, no. 5, pp. 711–716, May 1984, doi: 10.1109/T-ED.1984.21594.

[39] R. A. Sinton and A. Cuevas, "Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data," *Appl. Phys. Lett.*, vol. 69, no. 17, pp. 2510–2512, Oct. 1996, doi: 10.1063/1.117723.

[40] M. A. Green, "Lambertian light trapping in textured solar cells and light-emitting diodes: analytical solutions," *Prog. Photovolt: Res. Appl.*, vol. 10, no. 4, pp. 235–241, Jun. 2002, doi: 10.1002/pip.404.

[41] T. Niewelt *et al.*, "Taking monocrystalline silicon to the ultimate lifetime limit," *Solar Energy Materials and Solar Cells*, vol. 185, pp. 252–259, Oct. 2018, doi: 10.1016/j.solmat.2018.05.040.

[42] A. Augusto, J. Karas, P. Balaji, S. G. Bowden, and R. R. King, "Exploring the practical efficiency limit of silicon solar cells using thin solar-grade substrates," *Journal of Materials Chemistry A*, vol. 8, no. 32, pp. 16599–16608, 2020, doi: 10.1039/D0TA04575F.

[43] S. Herasimenka *et al.*, "Surface preparation and optimization of amorphous silicon deposition for silicon heterojunction solar cells," *Twenty-eighth European Photovoltaic Specialists Conference*, pp. 1943–1946, 2013, doi: 10.4229/28thEUPVSEC2013-2DV.3.39.

[44] M. Mews, T. F. Schulze, N. Mingirulli, and L. Korte, "Hydrogen plasma treatments for passivation of amorphous-crystalline silicon-heterojunctions on surfaces promoting epitaxy," *Appl. Phys. Lett.*, vol. 102, no. 12, p. 122106, Mar. 2013, doi: 10.1063/1.4798292.

[45] H. Nagel, C. Berge, and A. G. Aberle, "Generalized analysis of quasi-steady-state and quasi-transient measurements of carrier lifetimes in semiconductors," *Journal of Applied Physics*, vol. 86, no. 11, pp. 6218–6221, Dec. 1999, doi: 10.1063/1.371633.

[46] T. Trupke, R. A. Bardos, M. C. Schubert, and W. Warta, "Photoluminescence imaging of silicon wafers," *Appl. Phys. Lett.*, vol. 89, no. 4, p. 044107, Jul. 2006, doi: 10.1063/1.2234747.

[47] J. Haunschild, M. Glatthaar, M. Kasemann, S. Rein, and E. R. Weber, "Fast series resistance imaging for silicon solar cells using electroluminescence: Fast series resistance imaging for silicon solar cells using electroluminescence," *phys. stat. sol. (RRL)*, vol. 3, no. 7–8, pp. 227–229, Oct. 2009, doi: 10.1002/pssr.200903175.

[48] O. Breitenstein, J. Bauer, T. Trupke, and R. A. Bardos, "On the detection of shunts in silicon solar cells by photo- and electroluminescence imaging," *Prog. Photovolt: Res. Appl.*, vol. 16, no. 4, pp. 325–330, Jun. 2008, doi: 10.1002/pip.803.

[49] D. Hinken, K. Ramspeck, K. Bothe, B. Fischer, and R. Brendel, "Series resistance imaging of solar cells by voltage dependent electroluminescence," *Appl. Phys. Lett.*, vol. 91, no. 18, p. 182104, Oct. 2007, doi: 10.1063/1.2804562.

[50] D.-M. Tsai, S.-C. Wu, and W.-C. Li, "Defect detection of solar cells in electroluminescence images using Fourier image reconstruction," *Solar Energy Materials and Solar Cells*, vol. 99, pp. 250–262, Apr. 2012, doi: 10.1016/j.solmat.2011.12.007.

[51] J. Haunschild, I. E. Reis, J. Geilker, and S. Rein, "Detecting efficiency-limiting defects in Czochralski-grown silicon wafers in solar cell production using photoluminescence imaging: Detecting efficiency-limiting defects in Czochralski-grown silicon wafers in solar cell production using photoluminescence imaging," *Phys. Status Solidi RRL*, vol. 5, no. 5–6, pp. 199–201, Jun. 2011, doi: 10.1002/pssr.201105183.

[52] M. Glatthaar *et al.*, "Spatially resolved determination of the dark saturation current of silicon solar cells from electroluminescence images," *Journal of Applied Physics*, vol. 105, no. 11, p. 113110, Jun. 2009, doi: 10.1063/1.3132827.

[53] A. Delamarre, L. Lombez, and J.-F. Guillemoles, "Contactless mapping of saturation currents of solar cells by photoluminescence," *Appl. Phys. Lett.*, vol. 100, no. 13, p. 131108, Mar. 2012, doi: 10.1063/1.3697704.

[54] T. Fuyuki, H. Kondo, T. Yamazaki, Y. Takahashi, and Y. Uraoka, "Photographic surveying of minority carrier diffusion length in polycrystalline silicon solar cells by electroluminescence," *Appl. Phys. Lett.*, vol. 86, no. 26, p. 262108, Jun. 2005, doi: 10.1063/1.1978979.

[55] T. Trupke, B. Mitchell, J. W. Weber, W. McMillan, R. A. Bardos, and R. Kroeze, "Photoluminescence Imaging for Photovoltaic Applications," *Energy Procedia*, vol. 15, pp. 135–146, 2012, doi: 10.1016/j.egypro.2012.02.016.

[56] C. Shen, M. A. Green, O. Breitenstein, T. Trupke, M. Zhang, and H. Kampwerth, "Improved local efficiency imaging via photoluminescence for silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 123, pp. 41–46, Apr. 2014, doi: 10.1016/j.solmat.2014.01.003.

[57] S. Bowden and A. Rohatgi, "Rapid and Accurate Determination of Series Resistance and Fill Factor Losses in Industrial Silicon Solar Cells," presented at the 17th European Photovoltaic Solar Energy Conference, Munich, Germany, 2001.

[58] C. M. Herzinger, B. Johs, W. A. McGahan, J. A. Woollam, and W. Paulson, "Ellipsometric determination of optical constants for silicon and thermally grown

silicon dioxide via a multi-sample, multi-wavelength, multi-angle investigation," *Journal of Applied Physics*, vol. 83, no. 6, pp. 3323–3336, Mar. 1998, doi: 10.1063/1.367101.

[59] E. Yablonovitch, D. L. Allara, C. C. Chang, T. Gmitter, and T. B. Bright, "Unusually Low Surface-Recombination Velocity on Silicon and Germanium Surfaces," *Phys. Rev. Lett.*, vol. 57, no. 2, pp. 249–252, Jul. 1986, doi: 10.1103/PhysRevLett.57.249.

[60] A. Kosarian, M. Shakiba, and E. Farshidi, "Role of sputtering power on the microstructural and electro-optical properties of ITO thin films deposited using DC sputtering technique," *IEEJ Transactions on Electrical and Electronic Engineering*, vol. 13, no. 1, pp. 27–31, Jan. 2018, doi: 10.1002/tee.22494.

[61] B. Hoex, J. J. H. Gielis, M. C. M. van de Sanden, and W. M. M. Kessels, "On the c-Si surface passivation mechanism by the negative-charge-dielectric Al2O3," *Journal of Applied Physics*, vol. 104, no. 11, p. 113703, Dec. 2008, doi: 10.1063/1.3021091.

[62] A. Augusto, S. Y. Herasimenka, R. R. King, S. G. Bowden, and C. Honsberg, "Analysis of the recombination mechanisms of a silicon solar cell with low bandgap-voltage offset," *Journal of Applied Physics*, vol. 121, no. 20, p. 205704, May 2017, doi: 10.1063/1.4984071.

[63] T. Matsui *et al.*, "High-efficiency amorphous silicon solar cells: Impact of deposition rate on metastability," *Appl. Phys. Lett.*, vol. 106, no. 5, p. 053901, Feb. 2015, doi: 10.1063/1.4907001.

[64] S. D. Wolf, A. Descoeudres, Z. C. Holman, and C. Ballif, "High-efficiency Silicon Heterojunction Solar Cells: A Review," *Green*, vol. 2, no. 1, Jan. 2012, doi: https://doi.org/10.1515/green-2011-0018.

[65] Hitoshi Sai, Po-Wei Chen, Hung-Jung Hsu, Takuya Matsui, Shota Nunomura, and Koji Matsubara, "Impact of intrinsic amorphous silicon bilayers in silicon heterojunction solar cells," *Journal of Applied Physics*, vol. 124, no. 10, p. 103102, Sep. 2018, doi: 10.1063/1.5045155.

[66] A. Matsuda, M. Takai, T. Nishimoto, and M. Kondo, "Control of plasma chemistry for preparing highly stabilized amorphous silicon at high growth rate," *Solar Energy Materials and Solar Cells*, vol. 78, no. 1–4, pp. 3–26, Jul. 2003, doi: 10.1016/S0927-0248(02)00431-2.

[67] J. Ramanujam and A. Verma, "Photovoltaic Properties of a-Si:H Films Grown by Plasma Enhanced Chemical Vapor Deposition: A Review," *Mat Express*, vol. 2, no. 3, pp. 177–196, Sep. 2012, doi: 10.1166/mex.2012.1073.

[68] S. Guha, J. Yang, A. Banerjee, B. Yan, and K. Lord, "High quality amorphous silicon materials and cells grown with hydrogen dilution," *Solar Energy Materials and Solar Cells*, vol. 78, no. 1–4, pp. 329–347, Jul. 2003, doi: 10.1016/S0927-0248(02)00441-5.

[69] A. H. M. Smets, W. M. M. Kessels, and M. C. M. Van de Sanden, "Vacancies and voids in hydrogenated amorphous silicon," *Applied Physics Letters*, vol. 82, no. 10, pp. 1547–1549, 2003, doi: 10.1063/1.1559657.

[70] S. Y. Herasimenka *et al.*, "Large area ultrapassivated silicon solar cells using heterojunction carrier collectors," Arizona State University, 2013. [Online]. Available: https://repository.asu.edu/items/20907

[71] M. Jeon, S. Yoshiba, and K. Kamisako, "Hydrogenated amorphous silicon film as intrinsic passivation layer deposited at various temperatures using RF remote-PECVD technique," *Current Applied Physics*, vol. 10, no. 2, pp. S237–S240, Mar. 2010, doi: 10.1016/j.cap.2009.11.059.

[72] J. Ge, Z. P. Ling, J. Wong, T. Mueller, and A. G. Aberle, "Optimisation of Intrinsic a-Si:H Passivation Layers in Crystalline-amorphous Silicon Heterojunction Solar Cells," *Energy Procedia*, vol. 15, pp. 107–117, 2012, doi: 10.1016/j.egypro.2012.02.013.

[73] E. Bhattacharya and A. H. Mahan, "Microstructure and the light-induced metastability in hydrogenated amorphous silicon," *Applied Physics Letters*, vol. 52, no. 19, pp. 1587–1589, 1988, doi: 10.1063/1.99089.

[74] M. Z. Burrows, U. K. Das, R. L. Opila, S. De Wolf, and R. W. Birkmire, "Role of hydrogen bonding environment in a-Si:H films for c-Si surface passivation," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 26, no. 4, pp. 683–687, 2008, doi: 10.1116/1.2897929.

[75] H. Sai, T. Oku, Y. Sato, M. Tanabe, T. Matsui, and K. Matsubara, "Potential of very thin and high-efficiency silicon heterojunction solar cells," *Prog Photovolt Res Appl*, vol. 27, no. 12, pp. 1061–1070, Dec. 2019, doi: 10.1002/pip.3181.

[76] J. Ganji, A. Kosarian, and H. Kaabi, "Mathematical Evaluation of a-Si:H Film Formation in rf-PECVD Systems," *Silicon*, vol. 12, no. 3, pp. 723–734, Mar. 2020, doi: 10.1007/s12633-019-00167-9.

[77] M. Crose, J. Sang-Il Kwon, M. Nayhouse, D. Ni, and P. D. Christofides, "Multiscale modeling and operation of PECVD of thin film solar cells," *Chemical Engineering Science*, vol. 136, pp. 50–61, Nov. 2015, doi: 10.1016/j.ces.2015.02.027.

[78] A. Augusto, P. Balaji, J. Karas, and S. G. Bowden, "Impact of substrate thickness on the surface passivation in high performance n-type solar cells," in *2018 IEEE 7th World Conference on Photovoltaic Energy Conversion (WCPEC) (A Joint Conference of 45th IEEE PVSC, 28th PVSEC & 34th EU PVSEC)*, Waikoloa Village, HI, Jun. 2018, pp. 2792–2794. doi: 10.1109/PVSC.2018.8548174.

[79] H. Shanks, C. J. Fang, L. Ley, M. Cardona, F. J. Demond, and S. Kalbitzer, "Infrared Spectrum and Structure of Hydrogenated Amorphous Silicon," *phys. stat. sol. (b)*, vol. 100, no. 1, pp. 43–56, Jul. 1980, doi: 10.1002/pssb.2221000103.

[80] A. H. M. Smets and M. C. M. V. D. Sanden, "Relation of the Si H stretching frequency to the nanostructural Si H bulk environment," *Physical Review B - Condensed Matter and Materials Physics*, vol. 76, no. 7, 2007, doi: 10.1103/PhysRevB.76.073202.

[81] W. Beyer and M. S. A. Ghazala, "Absorption Strengths of Si-H Vibrational Modes in Hydrogenated Silicon," *MRS Proceedings*, vol. 507, p. 601, 1998, doi: 10.1557/PROC-507-601.

[82] A. Kimmerle, P. Rothhardt, A. Wolf, and R. A. Sinton, "Increased Reliability for J0-analysis by QSSPC," *Energy Procedia*, vol. 55, pp. 101–106, Jan. 2014, doi: 10.1016/j.egypro.2014.08.087.

[83] L. E. Black and E. Kessels, "Dependence of coil sensitivity on sample thickness in inductively coupled photoconductance measurements," *AIP Conference Proceedings*, vol. 2147, no. 1, p. 020002, Aug. 2019, doi: 10.1063/1.5123807.

[84] D. Zhang *et al.*, "Design and fabrication of a SiOx/ITO double-layer anti-reflective coating for heterojunction silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 117, pp. 132–138, Oct. 2013, doi: 10.1016/j.solmat.2013.05.044.

[85] S. Y. Herasimenka, W. J. Dauksher, M. Boccard, and S. Bowden, "ITO/SiOx:H stacks for silicon heterojunction solar cells," *Solar Energy Materials and Solar Cells*, vol. 158, pp. 98–101, Dec. 2016, doi: 10.1016/j.solmat.2016.05.024.

[86] Z. C. Holman *et al.*, "Current Losses at the Front of Silicon Heterojunction Solar Cells," *IEEE J. Photovoltaics*, vol. 2, no. 1, pp. 7–15, Jan. 2012, doi: 10.1109/JPHOTOV.2011.2174967.

[87] A. Atzek, J. Capart, R. Carabb, K. Heffels, and G. Seibert, *in Proceedings of the International Colloquium ECOSEC, Toulouse, 1970*. Gordon and Breach New York, 1971.

[88] D. Deligiannis, V. Marioleas, R. Vasudevan, C. C. G. Visser, R. A. C. M. M. van Swaaij, and M. Zeman, "Understanding the thickness-dependent effective lifetime of crystalline silicon passivated with a thin layer of intrinsic hydrogenated amorphous silicon using a nanometer-accurate wet-etching method," *Journal of Applied Physics*, vol. 119, no. 23, p. 235307, Jun. 2016, doi: 10.1063/1.4954069.

[89] T. Konishi and K. Ohdaira, "Indium tin oxide sputtering damage to catalytic chemical vapor deposited amorphous silicon passivation films and its recovery," *Thin Solid Films*, vol. 635, pp. 73–77, Aug. 2017, doi: 10.1016/j.tsf.2017.01.021.

[90] R. Gogolin *et al.*, "Analysis of Series Resistance Losses in a-Si:H/c-Si Heterojunction Solar Cells," *IEEE Journal of Photovoltaics*, vol. 4, no. 5, pp. 1169–1176, Sep. 2014, doi: 10.1109/JPHOTOV.2014.2328575.

[91] M. A. Green, *Solar cells : operating principles, technology and system applications*. Prentice-Hall, Englewood Cliffs, NJ, USA, 1982.

[92] M. A. Green, "Accuracy of analytical expressions for solar cell fill factors," *Solar Cells*, vol. 7, no. 3, pp. 337–340, Dec. 1982, doi: 10.1016/0379-6787(82)90057-6.

[93] D. D. Smith, G. Reich, M. Baldrias, M. Reich, N. Boitnott, and G. Bunea, "Silicon solar cells with total area efficiency above 25 %," in *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*, Portland, OR, USA, Jun. 2016, pp. 3351–3355. doi: 10.1109/PVSC.2016.7750287.

[94] M. A. Green *et al.*, "Solar cell efficiency tables (Version 53)," *Progress in Photovoltaics: Research and Applications*, vol. 27, no. 1, pp. 3–12, 2019, doi: 10.1002/pip.3102.

[95] P. P. Altermatt and G. Heiser, "Numerical Quantification and Minimization of Perimeter Losses in High-eficiency Silicon Solar Cells," *Progress in Photovoltaics: Research and Applications*, vol. 4, pp. 355–367, 1996, doi: https://doi.org/10.1002/(SICI)1099-159X(199609/10)4:5%3C355::AID-PIP145%3E3.0.CO;2-X.

[96] B. Demaurex, S. D. Wolf, A. Descoeudres, Z. C. Holman, and C. Ballif, "Damage at hydrogenated amorphous/crystalline silicon interfaces by indium tin oxide overlayer sputtering," *Applied Physics Letters*, vol. 101, no. 17, 2012, doi: 10.1063/1.4764529.

[97] K. Kuwano and S. Ashok, "Investigation of sputtered indium-tin oxide/silicon interfaces: ion damage, hydrogen passivation and low-temperature anneal," *Applied Surface Science*, vol. 117–118, pp. 629–633, Jun. 1997, doi: 10.1016/S0169-4332(97)80155-9.

[98] M. Filipič, Z. C. Holman, F. Smole, S. De Wolf, C. Ballif, and M. Topič, "Analysis of lateral transport through the inversion layer in amorphous silicon/crystalline silicon heterojunction solar cells," *Journal of Applied Physics*, vol. 114, no. 7, p. 074504, Aug. 2013, doi: 10.1063/1.4818709.