# GaAs Thermophotovoltaic Cells with Patterned Dielectric Back Contact

by

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ABSTRACT

GaAs thermophotovoltaic (TPV) devices with a patterned dielectric back contact (PDBC) architecture, featuring a dielectric spacer between the semiconductor and back metal contact over most of the back surface for high reflectance, and metal point contacts over a smaller area for electrical conduction were demonstrated. In the TPV application, high sub-bandgap reflectance is needed to reflect unused sub-bandgap photons to the thermal emitter to minimize energy losses in this portion of the thermal spectrum. Different PDBC fabrication processes with SU-8 and $SiO_2$ dielectric spacer layers to maximize sub-bandgap reflectance while minimizing series resistance to increase TPV conversion efficiency was explored. GaAs SU-8 PDBC TPV devices with 2200°C blackbody-weighted sub-bandgap reflectance of 94.9% and 96.5% with and without a front metal grid, respectively were demonstrated. This was 0.7% and 2.3% (absolute) higher than the mean sub-bandgap reflectance of 94.2% for GaAs baseline TPV devices with 100% Au back contact with a front metal grid. Lower sub-bandgap reflectance in TPV devices with front grids indicated the front grid induced light scattering led to additional parasitic absorption in the TPV device. For higher contact coverage fractions, the PDBC reflectance cannot, in general, be treated by linear interpolation of the mirror and point-contact areas using simple 1D transfer matrix method modeling and should be treated instead as a diffraction grating by solving Maxwell's equations in 3D. GaAs PDBC TPV device with series resistance less than 10 $m\Omega \cdot cm^2$ was demonstrated. Finally, GaAs PDBC TPV device with 22.8% TPV efficiency measured in a thermophotovoltaic test platform with the thermal emitter at 2100°C was demonstrated.

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# CHAPTER 1

# MOTIVATION

## 1.1 High-temperature TPV based thermal battery for grid-level storage

Grid-level energy storage solutions are essential to increase renewable energy penetration in the electricity grid. These energy storage systems act as a buffer and store excess electricity during off-peak load demand and generate electricity during peak load demand. Researchers[1,2,3,4,5] have shown that renewable energy penetration in the electricity grid will be limited to less than 10-15% in the absence of a grid-level energy storage system. One of the primary grid-level storage systems is pumped hydroelectric storage[6]. In this system, excess electricity is stored by pumping water from a low-level to a high-level water reservoir, and energy is generated through hydropower plants by flowing the water from the high-level to low-level reservoir. Though this system has a high round-trip efficiency of 80 - 90%[7], it is plagued by geographical constraints and the need for two reservoirs that are capital intensive and may not be environmentally friendly.

The current champion technology for grid-level energy storage is Li-ion batteries. The Li-ion batteries are also highly efficient but suffer from high capital costs thus a high levelized cost of storage[5] (LCOS). In addition, widespread demand for Li-ion batteries in automobiles and other portable electronics may cause the cost of key materials needed for their construction to rise[8]. The materials used in current Li-ion batteries are rare and concentrated in very few parts of the globe[9] which may lead to supply bottlenecks.

An alternative storage system that can circumvent the disadvantages of both pumped hydroelectric and Li-ion battery-based grid-level energy storage systems is one based on high-temperature thermal energy storage, which can be built using earth-abundant

materials and without geographical constraints. Such a storage system should have a low levelized cost of storage (LCOS) below $0.06 / KWHr, greater than 10 hours of storage, and must be reliable. Generally, thermal energy storage systems are predicted to be 1-2 orders of magnitude cheaper[7] than electrochemical battery storage.

In a high-temperature thermal battery system, excess electricity in the grid can be stored as high-temperature heat energy in the 1800 – 2200°C range resulting in a high energy storage density. The stored heat energy can be converted to electricity on demand by using a suitable heat engine. The heat engine can employ either a typical steam cycle used in a thermal power plant or a thermophotovoltaic (TPV) [10, 11, 12, 13, 14] system. In a thermophotovoltaic system, the thermal blackbody radiation from the hot emitter can directly be converted to electricity by using a suitable thermophotovoltaic module [Fig. 1]. Thus the TPV heat engine is a solid-state system with very few moving parts, allowing a noise-free operation.

This thermal energy storage system can be constructed using earth-abundant materials that are commercially available, like graphite block for the thermal emitter and porous carbon insulation for heat energy retention. The graphite thermal emitter can be heated either by resisitive or inductive heating using the excess electricity from the power grid. Typical graphite has an emissivity spanning 0.77 to 0.9[15] depending on the material quality, surface polish etc and has a melting point of 3500°C. The graphite blocks are commercially available in various shapes and size and can be fabricated according to the needs and is one of the cheapest and effective material available for grid-scale energy storage. The insulation materials of choise should withstand very high temperatures greater than 1800°C and must be able to retain heat for a longer period of time and should not be cost prohibitive

for grid-scale commercial deployment. Materials of interest are powdered carbon insulation based on coke powder or carbon black[16].

But, even with a very high quality insulation, there will still be a significant parasitic heat discharge because of the high thermal emitter temperature. This waste heat can be either used for large-area domestic heating or industrial heating needs and the cost associated with this heat loss can atleast be partially recovered. As the graphite thermal emitter is heated to temperatures >1800°C, the sublimation of graphite and subsequent deposition of carbon on relatively colder surface like TPV modules resulting in shading, poses to be a huge challenge in grid-scale thermal energy storage systems. Carbon sublimation partial pressure is much higher at low system pressures compared to high system pressures. This problem can be partially subverted by either constantly flushing the system with inert gases like Ar at pressures greater than 1 Atm and / or by deploying gas curtains in front of the TPV module to constantly intercept the carbon vapor. Also a mechanical scrubbing unit can be deployed to periodically clean the carbon deposits on the TPV module.

Another important challenge would be in keeping the TPV modules below 40 – 50°C. The TPV module faces really high temperature thermal emitter and the incoming photon flux is very high thus the resulting parasitic photon absorption and resistive loss from high operating current density results in TPV device heating. High TPV device temperatures will negatively affect the device performance[17], therefore the TPV devices or modules must be actively cooled. Thermal convection-conduction coefficients h, ranging from 1 – $10^6$ $W/m^2K$[18] is achievable for passive water cooling to active impinging water jet cooling. Therefore, water cooling of the TPV panels is possible and the technology can be borrowed

from concentrator photovoltaics (CPV). The TPV module will sit in an idle bay during thermal energy storage / stand-by phase and proper engineering design should be employed to minimize the heat spillage during transition of TPV modules in and out of the storage medium, and to depoly a periodical TPV module maintainence.

Efficiency in solar photovoltaics is affected by many uncontrollable components like solar irradiance spectrum, the latitudinal and longitudinal position of the sun, cloud cover, and other environmental factors. However, the efficiency of a TPV system in principle can be controlled by changing the local parameters like thermal emitter temperature, relative position, and aperture of the thermal emitter. Changing the thermal emitter temperature changes the thermal emission blackbody spectrum. Changing the thermal emitter aperture and relative position changes the incident intensity on the TPV device which in turn would change the short circuit current density. Also, the TPV device is close to the thermal emitter and in principle, most of the unused photons can be reflected in the thermal emitter to minimize parasitic heat loss. In solar photovoltaics, the light reflected from the front surface of the device due to Fresnel reflection constitutes a loss but not in TPV. To increase the current density in solar PV, an anti-reflection coating is used on the front surface to reduce the semiconductor reflection but such a coating may not be beneficial in TPC as the reflected light recuperates energy in the thermal emitter. Therefore, the theoretical TPV conversion efficiency can be much higher than the solar photovoltaic conversion efficiency.

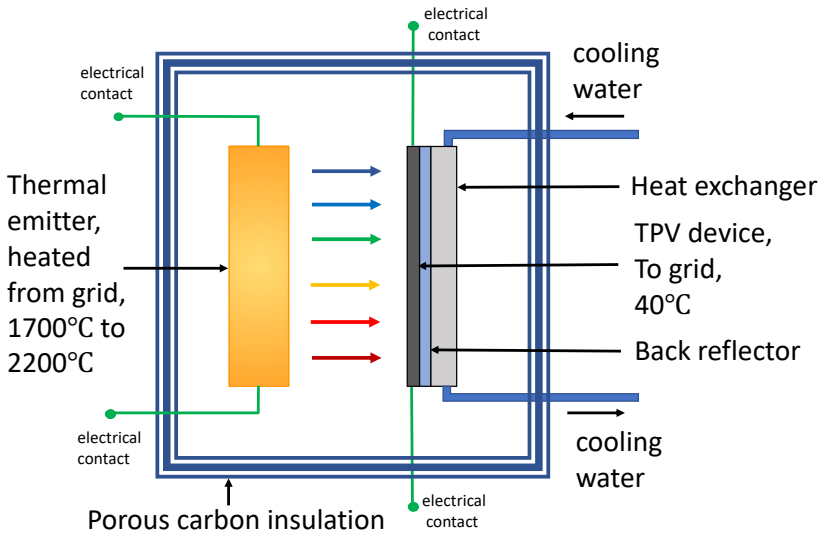



Figure 1. Schematic of grid-level thermal energy storage system with retractable TPV heat engine for thermal to electricity conversion.

Important TPV applications include solar thermal TPV[19,20,21,22,23,24,25,26], industrial waste heat recovery[27] and, solar thermal energy storage[28,29,30], and high-temperature thermal energy storage[7,31] which is the focus of the present work.

The important challenges in building a grid-scale thermal battery are multifold and are as follows,

1. Efficiently heating the thermal emitter to high temperatures (>1800°C).
2. Efficiently storing the thermal energy at such high temperatures for the required hours of storage or operation.
3. Designing cooling systems for the safe operation of the thermal insulation and the TPV devices.
4. Designing technologies to prevent sublimation and deposition of the thermal emitter on the TPV module or to remove depositions from the TPV module at regular intervals.

5. Designing high-efficiency TPV devices and modules for maximizing energy extraction.

So, a significant amount of research is needed in building a high-efficiency thermophotovoltaic heat engine which is essential for realizing a low LCOS grid-level thermal battery system.

Fig. 2 shows the blackbody irradiance as a function of wavelength for two different temperatures namely 1800°C and 2200°C. In a semiconductor TPV device, only a narrow spectrum of the incident blackbody power indicated by the green shaded region represents the photons above the bandgap of the semiconductor that could be absorbed and be converted to useful electricity. The broadband blackbody power indicated by the unshaded region represents the sub-bandgap photons that cannot be converted to useful electricity. But these sub-bandgap photons carry a lot of thermal energy and parasitic absorption of

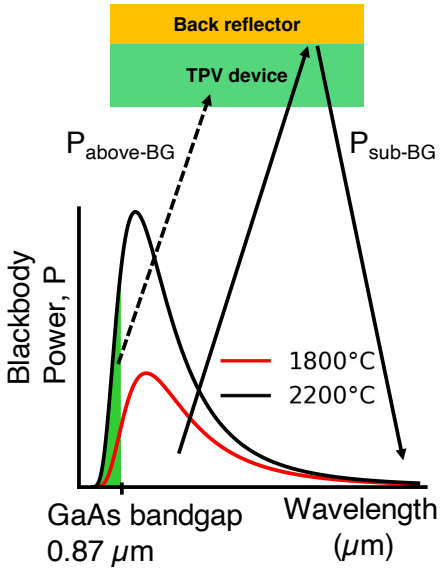



Figure 2. Schematic illustrating a TPV device as a bandgap filter with blackbody power density as a function of wavelength. The green shaded area represents above bandgap photons that can be converted to electricity. The unshaded area represents the sub-bandgap photons that must be reflected to thermal emitter to minimize parasitic loss.

these photons constitutes a loss in thermal energy thus poor energy storage efficiency. So, one of the key aspects of high efficient TPV system is sub-bandgap photon management to minimize parasitic absorption.

Different approaches for the reuse of sub-bandgap light in TPV systems include the use of selective emitters[32,33,34,35], selective band edge filters[36], and use of the TPV device as a band-edge filter[37,38,39,40] as shown in Fig. 3.

In the selective emitter design [Fig. 3a], the thermal emitter is engineered to emit only in a narrow wavelength band near the bandgap of the TPV device thus minimizing the thermalization loss in the TPV device and no need for sub-bandgap photon management. However, the selective emitter needs to be stable at temperatures >1800°C and must be capable of emitting at a very narrow spectrum, at very high emissivities as possible. However, there is no such capable selective emitter material commercially available.

In the selective filter design [Fig. 3b], an optical filter is engineered to selectively reflect most of the sub-bandgap photons to the thermal emitter and be transparent to most of the above-bandgap photons. In this design, the optical filter is plagued by the same problems as that of the selective emitter. Baldasaro et al.[41] states that the filter must be broadband as the thermal emitter emits in a broadband spectrum and must operate at a spectral filter efficiency close to 100% for maximal TPV efficiency. High angular dispersion of TPV emitter proposes an imminent challenge in TPV spectral filter design. Interference-based filters depend on the optical thickness of filter layers which depends also on the angle of incidence. A high angle of incidence may also lead to multiple reflections and total internal reflections within the filter. For a high angle of incidence, the Fresnel reflection from the filter surface may be higher. So, broad angular distribution

compromises the spectral filter efficacy. In close-space configurations, the energy transfer occurs via emitter-sink coupling rather than free-space propagation where the notion of the spectral filter is not the same.

The TPV device itself as a band-edge filter [Fig. 3c], is appealing for its elegance and simplicity of utilizing the absorbing layer in the device which is already present. The TPV device absorbs above-bandgap photons to create electron-hole pairs but is transparent to sub-bandgap photons. For a direct bandgap semiconductor, the filter can be quite sharp. By using a broadband back surface reflector, most of the sub-bandgap photons can be reflected to the blackbody emitter to minimize parasitic heat loss. This study focuses on the TPV device as a filter design.

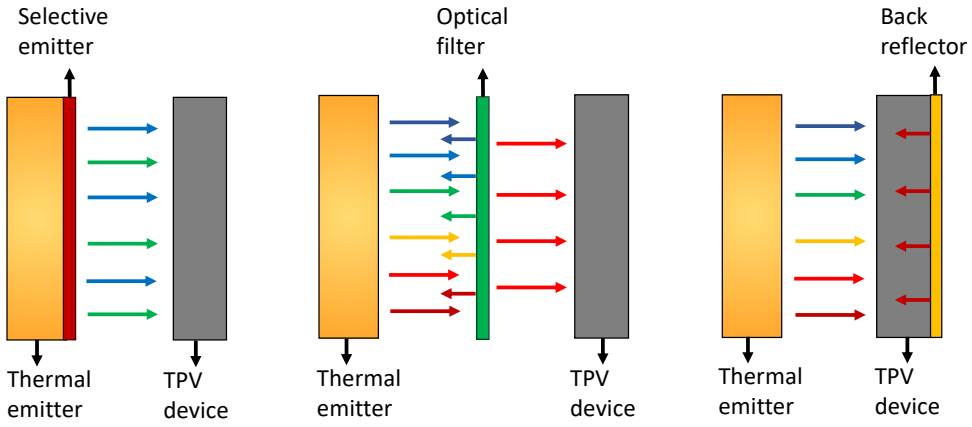



Figure 3. Schematic illustrating different ways in which the TPV system can be implemented (a) a selective thermal emitter, (b) an optical filter, (c) TPV device as optical filter TPV system.

TPV device research has historically focused on absorber bandgaps in the 0.5-0.8 eV range, for lower thermal emitter temperatures, typically in the ≤1100°C range[42]. However, with higher thermal emitter temperatures, the thermodynamic[43,44] efficiency limits are higher, and higher energy storage densities[7,27] are possible. Here the focus is on 1.4-eV GaAs[45] absorber which also serves as a band-edge filter, designed for thermal emitter

temperatures greater than 1800°C. Even at such high emitter temperatures, only a narrow spectrum of the incident electromagnetic radiation falls in the absorption range of GaAs, as shown in Fig. 1, with a broad sub-bandgap spectrum spanning all wavelengths greater than 0.87 μm. These sub-bandgap photons should be reflected to the thermal emitter to minimize parasitic heat loss. GaAs PV technology is well-established, well-understood, and the semiconductor layer material quality is much better than other lower bandgap III-V devices.

For these higher emitter temperatures and correspondingly higher incident intensities, a higher bandgap[14,46] GaAs TPV device is preferred in some ways over a lower bandgap TPV device for several reasons. 1) The voltage that can be achieved for a higher bandgap ($E_g$) cell is a greater fraction of the bandgap voltage $E_g/q$ than for cells with a lower bandgap. For a given above-gap photon flux and photogenerated current density $J_{ph}$, the bandgap-voltage offset $W_{oc} \equiv (E_g/q) - V_{oc}$ can be treated as approximately constant with respect to the bandgap[47], so $V_{oc}$ is a greater fraction of $E_g/q$ for higher $E_g$. 2) For a given $J_{ph}$, for a cell with higher bandgap and higher voltage $V$, the resistive ($I^2R$) losses are a smaller fraction of the power generated ($I \cdot V$) by the cell. The practical limit of $J_{ph}$ in concentrator PV or TPV is typically determined by the resistance $R$ that can be achieved by the metal grid technology used and other factors affecting the cell series resistance, and the $I^2R$ resistive power losses that are acceptable, so evaluating different cell bandgaps at a given $J_{ph}$ is reasonable. 3) Finally, GaAs cells can be grown epitaxially on GaAs substrates, which are much less expensive than InP, GaSb, and InAs substrates traditionally used for the growth of lower bandgap III-V materials.

We use a rear-heterojunction (RHJ) GaAs TPV device than a traditional front-homojunction (FHJ) GaAs TPV device. In a RHJ GaAs TPV, the absorber is a thick n-GaAs and the base is p-GaInP layer, which is present on the rear side of the device, away from the light incident side. Therefore, a part of the junction depletion region is moved away from the absorber into the p-GaInP heterobase, reducing the non-radiative recombination in the junction thus improving the open-circuit voltage[48,49]. This if compared to a FHJ device, the junction depletion region is present both in the n-GaAs and p-GaAs absorber layers and is also much wider in p-GaAs because of lower doping compared to RHJ, therefore an increased junction non-radiative recombination. In addition, the material quality of the bulk n-type GaAs absorber in a RHJ GaAs, is probably better than bulk p-type GaAs absorber in FHJ GaAs therefore a possibility for improved open-circuit voltage in RHJ GaAs.

There are at least three key challenges in designing a GaAs TPV device: First, the sub-bandgap reflectance of the TPV device weighted by the blackbody thermal spectrum from the emitter must be maximized. In solar PV, interference based back reflectors are demonstrated to enhance photon recycling[50,51,52], and boost open-circuit voltage. These reflectors are usually designed to improve the back reflectance at wavelengths near the bandgap of the active layer. In TPV, the back reflector must be designed for broadband sub-bandgap wavelengths spanning from bandgap of the active layer to mid-infrared. Second, the specific series resistance ($R_{series}$) must be minimized. The GaAs TPV device operates at a very high current density of 3-6 A/cm$^2$ depending on emitter temperature and presence of anti-reflection coating. In comparison, typical operating current density in a one-sun GaAs solar PV device is only around 20-30 mA/cm$^2$. Thus, in a GaAs TPV device,

high $R_{series}$ would result in high $I^2R_{series}$ loss, detrimental for TPV efficiency. Third, as with solar PV, the quality of the semiconductor device itself must be at the highest level possible, by minimizing non-radiative recombination, *e.g.*, from trap-assisted and Auger mechanisms, and enhancing photon recycling to increase the device voltage.

As mentioned in the previous section, improving the sub-bandgap reflectance is a key to improved TPV efficiency. So, in this study, some targeted epitaxial device layer changes and the addition of an improved rear reflector referred to as patterned dielectric back contact (PDBC), without compromising the device's electrical performance were explored.

### 1.2 Patterned dielectric back contact GaAs TPV devices for high-temperature TPV thermal battery

One of the main factors affecting the sub-bandgap reflectance is absorption in the metal back contact. By inserting a low-refractive-index, low-loss dielectric spacer between the semiconductor and metal, back contact absorption in the metal is reduced[53]. However, since the dielectric spacer materials are insulating, we adopt a patterned dielectric back contact[54,55,56,57] (PDBC) design [Fig. 4,5]. In a PDBC, a low-loss, low-refractive index dielectric spacer layer with through metal point contacts [Fig. 5a] is fabricated between the semiconductor back contact layer and the metal back contact. Due to refractive index contrast, the dielectric acts as a partial mirror and reflects most of the photons with negligible loss. The remaining photons that get transmitted through the dielectric gets reflected at the lossy, metal rear-mirror. In this design, the dielectric-metal region is an improved rear mirror over just the metal mirror and the metal point contacts in the dielectric help in electrical conduction on the rear side. The first order reflectance from the PDBC

can be approximated as superposition of reflectance from the dielectric-metal region and from the metal point contact region.

However, we show that this approximation is not valid for all the configurations of PDBC, later in the modeling and in the experimental sections. But this simple approximation helps us understand the impact of the change in dielectric and metal point contact area from the lens of contact coverage fraction (CCF). The CCF is defined as the ratio of total metal point contact area to the total semiconductor back contact area. CCF determines the total metal point contact area available for electrical conduction and 1-CCF represents the total dielectric spacer area responsible for improved reflectance. So, 0% CCF [Fig. 5b] implies no through metal point contact in the dielectric and this structure is electrically insulating. Similarly, 100% CCF [Fig. 5c] implies no dielectric spacer layer between the semiconductor back contact layer and the metal back contact and all the back contact area is available for electrical conduction but at the expense of lower reflectance. This 100% CCF is the simple baseline case referred as planar metal back contact.

PDBC like structures in various capacities has been demonstrated in the literature for various applications. One of the foremost applications in solar photovoltaics is for the improvement in open-circuit voltage by suppressing the surface plasmon polaritons (SPP) and is geared towards reflectance improvements for near bandgap electromagnetic wavelengths. Some other studies have also demonstrated the use of dielectric spacer for TPV devices.

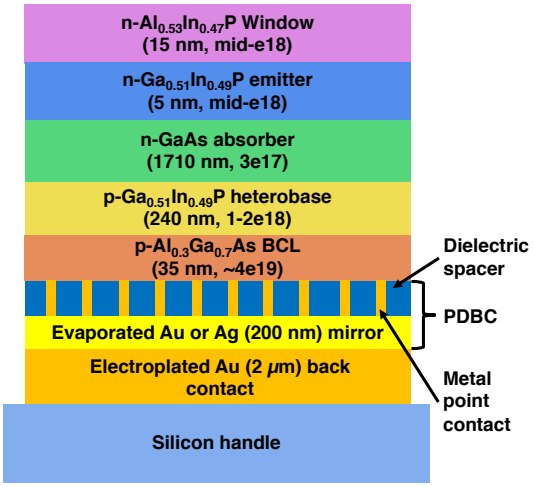



Figure 4. Schematic of GaAs TPV Device with a PDBC on a Si handle. The front contact layer (200 nm GaAs + 100 nm GaInNAs) is not shown and is present only beneath the Ni/Au front grids.

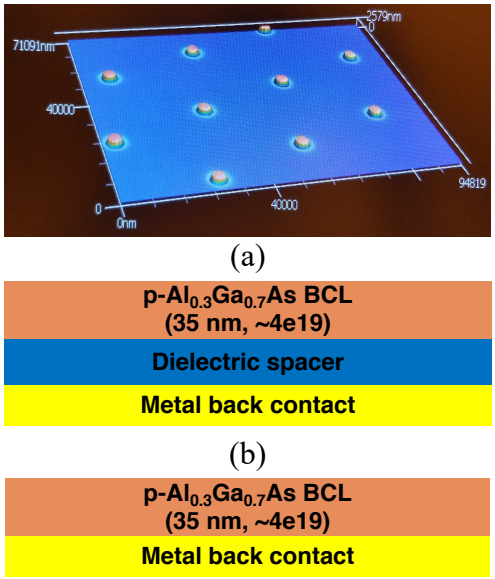



Figure 5. Schematic of (a) a patterned dielectric back contact (PDBC) with metal point contacts and dielectric/metal mirror area in three-dimension (b) 0% contact coverage fraction (CCF) back contact; and (c) 100% CCF back contact.

Swanson et al.[37] demonstrated Si PDBC TPV devices with $SiO_2$ dielectric spacer with an efficiency of 29% at 2027°C. Similarly, Fan et al.[40] demonstrated a 0.7-eV GaInAs TPV device with gridded back contacts and with air as the dielectric spacer layer, with an efficiency of 31.3% at 1200°C.

This study aims to demonstrate a higher bandgap 1.4-eV GaAs TPV device for ultra-high thermal emitter temperatures of >1800°C. It addresses the challenges in designing, fabricating, and integrating a high reflectance PDBC to GaAs TPV devices; explores the PDBC structures with hexagonally distributed metal point contacts in the dielectric spacer; explores PDBC micro-fabrication methods for different types of dielectrics; explores a novel use of SU-8 photoresist as dielectric; studies the interaction of the sub-bandgap wavelengths with the point contacts in three-dimensions as a function of point contact coverage fraction; studies the series resistance implications of the point contact coverage fraction and thick front-metal grids; explores the trade-off between maximizing the sub-bandgap reflectance and minimizing the series resistance in choosing the metal point contact coverage fraction. Finally, experimentally demonstrates reflectance improvements, series resistance improvements, and the actual TPV efficiency measurements from a calorimetry-based TPV measurement platform. The next section will describe the organization of this dissertation.

### 1.3 Dissertation overview

CHAPTER 2 delves into the background details and a brief TPV device history. It discusses some of the important concepts like free-carrier absorption, Plank blackbody radiation, short-circuit current density calculation, and works like TPV device with planar back contact, PDBC like back contacts for enhanced photon recycling, TPV devices with

PDBC like back contacts, TPV based grid-level thermal energy storage systems, and the thermodynamic assessment on the trade-off between efficiency and power density limitations of TPV devices.

CHAPTER 3 discusses the modeling and experimental methods used throughout this study. The modeling methods are about the different modeling techniques used to determine the performance of the TPV devices. The experimental methods are about the tools and techniques used to fabricate and characterize the TPV devices.

CHAPTER 4 investigates the modeling studies done in this work. It explores series resistance contributions due to front grids and PDBC. Then it explores the sub-bandgap reflectance improvements with low refractive index, low loss dielectric spacer, and then the complex 3D diffraction grating effects of PDBC. It also explores the TPV efficiency as a function of sub-bandgap reflectance and series resistance.

CHAPTER 5 discusses the different experiments conducted in this study. It first investigates the trade-offs between different PDBC fabrication methods. Then it experimentally studies the sub-bandgap reflectance and series resistance dependence on PDBC processing methods, dielectric spacer, and contact coverage fraction.

CHAPTER 6 discusses the integrated results of modeling, fabrication, characterization, and analysis of GaAs TPV devices. It explores the sub-bandgap reflectance and series resistance as a function of PDBC contact coverage fraction. It compares the photovoltaic and thermophotovoltaic performance of GaAs TPV devices with planar back contact and PDBC.

CHAPTER 7 presents a summary and addresses some future work.

# CHAPTER 2

# BACKGROUND AND PRIOR WORKS

## 2.1 Background and TPV device history

Foundation for TPV[58] was laid in 1956 by Henry Kolm[59] at MIT Lincoln Laboratory. Numerous experts like Pierre Aigrain, White, and Wedlock[60] worked on fuel-powered portable TPV generators. After the 1970s, the TPV research focused on solar thermal[61] TPV converters to address the energy crisis. But lack of high-quality infrared-sensitive TPV devices impeded high-efficiency TPV systems. The technological advancement in GaSb[62] and GaInAs[63] devices and later the concept of back surface reflectors[38] further kindled the TPV research interests. These developments culminated in a then-reported highest efficiency of 23.6% at 1039°C in 2004 using GaInAs monolithic interconnected module. With further improvement in back surface reflectors, higher TPV efficiencies of 24.1% at 1055°C[34], 29.1% at 1207°C using GaInAs TPV[39], and nearly 30% 1182°C using GaInAs TPV[40] devices were reported.

Around the early 2000s, near-field TPV[64,65,66] [NF-TPV] garnered attention. In NF-TPV, heat transfer occurs through non-propagating waves from the thermal emitter in addition to the radiative heat transfer. The distance of separation between the thermal emitter and the TPV device ranges from a few nm to μm. Recently, interest in cost-effective, long-term, grid-level, high-temperature thermal energy storage[7,28,29,30,31] applications has rekindled the research efforts in TPV heat engines. In this dissertation work, we will majorly focus on the far-filed TPV systems and GaAs TPV devices with improved rear reflector for grid-level energy storage applications.

## 2.2 Free-carrier absorption

The introduction of dopants in semiconductor give rise to excess carrier concentration which can move in the conduction or valence band depending on n-type or p-type dopants respectively with an effective mass $m^*$. When an alternating electromagnetic field is incident on the semiconductor, the bound electrons from the background undoped semiconductor and the free carriers that arise from doping experience electrical polarization[67]. Therefore, the Drude-Lorentz model which explains the free electron behavior in metals can be extended to also include the bound electrons from the background undoped semiconductor with the effective mass $m^*$ for the carriers to explain the free-carrier absorption in the doped semiconductors. The relative permittivity calculated using the extended Drude-Lorentz model is as shown in Eq. 1, where $\omega_p$ is plasma frequency, $\gamma$ is damping coefficient, $\omega$ is angular frequency of light, and $\epsilon_{opt}$ is dielectric function of undoped semiconductor measured in a transparent region below interband absorption edge and greater than $\omega_p$ where the semiconductor should nominally be transparent i.e., $\kappa = 0$. This $\epsilon_{opt}$ takes into account the background polarizability of the undoped semiconductor i.e., mainly the effects of the bound electrons. The plasma frequency $\omega_p$ is calculated through Eq. 2, where N is doping induced carrier concentration of the semiconductor, $m^*$ is carrier effective mass as described earlier, e is the electron charge, and $\epsilon_0$ is free-space permittivity.

$$\epsilon_r(\omega) = \epsilon_{opt}\left(1 - \frac{\omega_p^2}{(\omega^2 + i\gamma\omega)}\right) \tag{1}$$

$$\omega_p^2 = \frac{Ne^2}{\epsilon_{opt}\epsilon_0 m^*} \tag{2}$$

At frequencies above plasma frequency and below interband absorption edge, where the semiconductor should be nominally transparent, the presence of free carriers leads to absorption of electromagnetic waves known as free carrier absorption. Under an assumption that $\gamma$ equals $\tau^{-1}$ where is $\tau$ is scattering time, and ωt >>1 for near infrared frequencies, $\epsilon_1 \approx \epsilon_{opt}$ and $\epsilon_2 << \epsilon_1$, where $\epsilon_1$ and $\epsilon_2$ are real and imaginary parts of $\epsilon_r$. From these approximations, the free-carrier absorption $\alpha_{free\text{-}carrier}$ can be calculated according to the Eq. 3.

$$\alpha_{free-carrier} = \frac{\epsilon_{opt}\omega_p^2}{nc\tau\omega^2} = \frac{Ne^2}{\epsilon_0 m^* nc\tau}\frac{1}{\omega^2} = \frac{Ne^3\lambda^2}{4\pi^2\mu m^{*2} n\varepsilon_0 c^3} \quad (3)$$

Therefore, the free-carrier absorption depends on wavelength λ, doping concentration N, mobility μ, and effective mass $m^*$. But experimental results indicate that $\alpha_{free\text{-}carrier} \propto \omega^{-\beta}$ where β can be from 2-3. This deviation in β is due to failure of the assumption that $\tau$ independent of ω.

Physically, free-carrier absorption is an intra band transition and is considered as parasitic absorption in photovoltaic applications. In an n-type semiconductor, absorption of photons excites the free-carrier from occupied to unoccupied state above Fermi level in the conduction band. But in order for this event to occur, there must be a momentum conservation from a scattering event as the photon momentum is very small compared to an electron. Therefore, the free-carrier absorption is proportional to $\tau^{-1}$. Momentum conservation can be either from a phonon scattering or from ionized impurity scattering. Therefore, simplifying all scattering events with $\tau$ calculated from D.C. conductivity, independent of ω is not always valid.

In a p-type semiconductor, the above model holds but with an extension accounting for intervalence band transitions due to light-hole to heavy-hole, spilt-off to heavy-hole, and split-off to light-hole bands except at momentum k = 0, where these transitions are forbidden, as all hole bands are derived from p-like atomic states. These absorptions are strong as it does not require any scattering events for momentum conservation indicating that the free-carrier absorption in the p-type semiconductor to be higher than n-type semiconductor.

In a TPV device, the semiconductor layers are doped, and the sub-bandgap spectrum falls in the near- and mid-infrared regions. In this spectral region, the semiconductor and metal absorption are dominated by free-carrier absorption. Therefore, the parasitic free-carrier absorption in the device can be minimized either by reducing the doping concentration or by reducing the thickness of the semiconductor layers without affecting the electrical performance of the TPV device.

**2.3 Blackbody emission and short-circuit current density**

The blackbody emission is given by Plank's law[68] [Eq. 4] which describes the spectral density of electromagnetic radiation emitted by a blackbody in a thermal equilibrium at a given temperature T when there's no net flow of matter or energy between the blackbody and environment. The S.I. unit of the blackbody emission is $W/sr/m^3$ and is isotropic and unpolarized. In [Eq. 4], q is charge, h is Planck's constant, c is velocity of light in free space, $\lambda$ is wavelength, $K_B$ is Boltzmann constant, and T is temperature of the blackbody in K. The energy distribution of the blackbody changes with respect to blackbody temperature where both the energy intensity and the peak energy wavelength shifts as a function of temperature.

$$B_\lambda(\lambda, T) = \frac{2hc^2}{\lambda^5} \frac{1}{e^{\frac{hc}{\lambda K_B T}} - 1} \quad (4)$$

In reality, there is no ideal blackbody and thermal emission from a hot object can be approximated as a grey body where the Plank distribution is multiplied with its emissivity ε, where emissivity is the ratio of actual radiance to ideal Plank radiation. Emissivity of an object depends on various factors like its chemical composition, surface texture, temperature, wavelength, angle of passage, and polarization. An infinitesimal power that is radiated at an angle θ from surface normal, from infinitesimal surface area dA into infinitesimal solid angle dΩ in an infinitesimal wavelength dλ is given by $B_\lambda(\lambda,T)\cdot\cos\theta\cdot dA\cdot d\Omega\cdot d\lambda$ where cosθ is from the Lambert cosine law [69] and dΩ is $\sin\theta\cdot d\theta\cdot d\phi$. The total power radiated in W can be calculated by integrating the infinitesimal power over the required geometrical parameters for all the wavelengths in the range 0 - ∞. In the grid-level thermal storage environment, the geometrical parameters are polar angle θ in 0-90°, azimuthal angle ϕ in 0-180°, and area can be arbitrary thermal emitter area. Because of the $\sin\theta\cdot\cos\theta$ dependence, the maximum radiated power will be at a θ value of 45°

For a TPV device, the number of photons with energies above the bandgap of the absorber defines the photon current density ($J_{ph}$) and can be equal to short-circuit current density ($J_{sc}$) if all the incident photons are absorbed in the semiconductor absorber layer (external quantum efficiency, EQE = 1) and converted to electron-hole pairs and are extracted (internal quantum efficiency, IQE = 1) as charge carriers. In this case, the $J_{sc}$ of the device can be calculated according to the Eq. 5, where $A_{cell}$ is the TPV device area, ε is emissivity of the thermal emitter and ranges from 0-1, EQE is the external quantum

efficiency of the TPV device, and all other symbols were discussed earlier. In Eq. 5, the multiplicand λ/hc converts the radiated power density to radiated photon density. And the EQE defines the above-band edge absorption that can be converted to electron-hole pairs in the TPV device as a function of wavelength.

$$J_{sc} = \frac{qA_{cell}\varepsilon}{hc}\int_0^{2\pi}\int_0^{\frac{\pi}{2}}\int_0^{\lambda_{BG}} EQE(\lambda)\, B_\lambda(\lambda,T)\,\lambda\cos\theta\sin\theta\, d\lambda d\theta d\phi \quad (5)$$

**2.4 TPV device bandgap, output power, and efficiency**

In 2001, Baldasaro et al.[41] presented a thermodynamic assessment on the trade-off between efficiency and power density limitations of TPV devices under radiative limited (ideal) and defect limited (practical) cases. Analysis revealed that bandgap selection sets limits on achievable TPV efficiency well-below Carnot level. Spectral filter performance dominates the diode performance for any practical TPV system and determines the optimal bandgap for a given emitter temperature. The entropy sources in a TPV system are 1, temperature drop during transport of heat from a blackbody to thermal emitter 2, electric current flow to generate power 3, illumination induced deviation from diode equilibrium. The basic components of the TPV system are photon emitter, spectral filter, and TPV device. The photon or thermal emitter, assumed to be a Lambertian surface, has a frequency and angular characteristics similar to energy radiated from a small hole in a blackbody cavity. The angular dispersion of the TPV emitter has a sinθcosθ dependence thus the emission intensity peaks at 45°.

The TPV conversion process can be effectively viewed as the selective conversion of above-bandgap photons to electron-hole pairs and selective reflection of the sub-bandgap photons to the thermal emitter to minimize parasitic heat loss using a TPV spectral filter.

This spectral filter can be an independent entity or sometimes be the TPV semiconductor device itself. Though filter reflectivity has no thermodynamic limits, it plays a huge part in deciding the TPV efficiency.

The TPV device conversion efficiency can be written as a product of device quantum efficiency, thermalization efficiency, open-circuit voltage efficiency ($V_{oc}/E_g$), and power usage efficiency (fill-factor) defined by Eq. 1-7. The quantum efficiency depends on carrier diffusion length and surface recombination velocity of the semiconductor materials. Thermalization efficiency is the fraction of photon energy that is not lost to the lattice as heat. For a given thermal emitter temperature, a higher bandgap TPV device will result in lower thermalization loss. The thermodynamic limit on recombination current in a TPV device or diode at temperature $T_c$ is determined by radiative recombination due to equilibrium blackbody emission, assuming negligible other types of recombination. Assuming, a diode has a backside reflector to support photon recycling, the recombination current has the same exponential dependence on bandgap as more traditional drift-diffusion formulations.

The integrated efficiency of diode and filter indicates that even a low parasitic absorption in the sub-bandgap spectrum (like ~1%) can have a strong degradation effect on TPV system efficiency. Therefore, the filter performance dominates the diode performance and plays a dominant role in determining the optimal device bandgap (because of the low no. of above-bandgap photons). Therefore, lower bandgap devices can enable both higher power density and efficiency if the spectral control limitations are included. The non-ideal attributes that can emerge from cavity designs are 1, non-active parasitically absorbing diode areas 2, non-Lambertian emitter (may cause multiple

reflections and alter the cavity angular dispersion) 3, angular and polarization-dependent filter reflectivity 4, the separation between the diode and emitter 5, cavity edge leakage. Even a tiny parasitic absorption fraction from a non-active area can be magnified by multiple reelections in the system leading to significant efficiency degradation.

Therefore, the trade-off between TPV power density and efficiency is due to internal entropy generation introduced by the conversion process which increases with current. The key results are 1, filter performance dominates diode performance 2, under spectral control limitations, low-bandgap diodes enable high TPV efficiency and power density 3, thermodynamic trade-off between efficiency and power which limits efficiency limits to well below Carnot efficiency 4, closed-space emitter/diode configuration offers superior efficiency 5, emitter, filter, diode technology should be developed from a system perspective

Datas[46] discusses the optimal 1J and 2J semiconductor bandgaps leading to maximum efficiency and power densities in TPV systems. The optimum semiconductor bandgaps are calculated as a function of the emitter and cell temperature, and the quality of spectral control. Total heat to electricity efficiency of TPV device is the product of thermal and device efficiency. In constant heat input applications, maximizing the device power output is preferred. In constant emitter temperature applications, maximizing TPV efficiency is preferred. Under detailed balance limit, a system of equations is solved for different values of V resulting in JV curve. The maximum power point is calculated and then the efficiency is calculated for the thermal emitter – TPV device with back surface reflectance (BSR) TPV system. Multi-dimensional Nelder-Mead algorithm was used to find the optimal bandgap.

If the BSR reflectivity is ~1, the TPV cell efficiency can be increased by increasing the bandgap to minimize cell recombination and maximize Voc. But the power density drastically decreases due to poor match between thermal emitter spectrum and device spectral response. To maximize power density, the bandgap is decreased but it will lead to increase in both power density and to a certain extent efficiency as a result of increase in electrical power output. So, maximizing a product of electrical power output and TPV device efficiency results in better evaluation metric and the resultant bandgap is slightly above the power density maximized bandgap. In maximum power density case, the optimal bandgap is almost independent of the BSR. Therefore, multijunction cells provide higher efficiencies, especially multijunction cells even with a BSR = 0 provides higher efficiency than single junction cells with BSR =1.

The TPV cell bandgap plays an important role in deciding the trade-off between power density and efficiency. Higher bandgap devices provide higher efficiency at a cost of lower power density when the BSR is close to unity, and it sharply goes down even for a minute drop in BSR. For two junction cells, the efficiency and power density drastically drop for higher than optimal bandgap. Though efficiency can be gained from improvements in BSR it has minimal impacts on power density. Multijunction cells do not perform better than single junction cells if the lower junction cell bandgap is higher than optimum i.e., 0.5 eV (which lead to lower power density).

In terms of cell temperature, the higher cell temperature results in higher radiative recombination therefore the optimum bandgap increases but will also result in reduced photogeneration. But when BSR is extremely high, increasing photogeneration through

bandgap reduction is optimal. Also, the semiconductor bandgap temperature dependence on cell temperature should also be accounted.

**2.5 Prior works on TPV devices with planar back contacts**

Some of the important works with TPV device as filter and with a metal rear reflector/back contact are discussed in this section.

In 1963, Wedlock[60] has demonstrated a Ge thermophotovoltaic device with p-i-n structure for thermal emitter temperatures around 1600°C. Among the p-n and p-i-n structures evaluated, the p-i-n structure had better output. The p and n regions in p-i-n can be degenerately doped leading to maximum possible open-circuit voltage. A high lifetime can be maintained in i-region resulting in higher collection efficiency. But in a p-n structure, a heavy doped n-region can result in higher output voltage at the expense of lower collection efficiency. At a wide-band infrared radiation, the Ge p-i-n device showed a maximum efficiency of 4.23% and an output power density of 282 $mW/cm^2$. No correction of reflection losses was made. Also, from the trends, with increase in intensity, a steady increase in efficiency is predicted up to a range of 10 – 16% at 3 – 30 $W/cm^2$. The device had a collection efficiency of 67% and increasing it to 100% could improve the predicted efficiency by a factor of 3/2. By adding an anti-reflection coating, and a narrow wavelength region of operation should improve the efficiency significantly. So, in total, a 30% TPV conversion efficiency at 10 $W/cm^2$ is predicted.

In 1996, Charache et al.[38] have demonstrated the use of back surface reflector as spectral control strategy in TPV devices. The back surface reflector should have high reflectivity, low specific contact resistivity, strong adhesion, and thermal stability. In TPV high reflectivity and low specific contact resistivity are very important due to strong

wavelength dependence on free-carrier absorption and high operating current density. Different back surface reflector strategies like semiconductor/metal alloyed back contact, semiconductor/interdigitated, non-reflective ohmic grid – reflective metal back contact, semiconductor/interdigitated non-reflective ohmic grid – dielectric – reflective metal back contact was evaluated while each having its own trade off. The interdigitated contact without dielectric suffers from low temperature metal-semiconductor reaction thus degradation in long term reflectivity. Multiple test structures were fabricated with different process technologies based on the back surface strategies discussed. Then the reflectance up to 10 μm wavelength and specific contact resistivities were measured. Thus, a proof-of-concept high reflectivity, low contact resistance back surface reflector for GaAs, InAs, and InP was demonstrated.

In 2003, Wehrer et al [70] have demonstrated a 0.74 eV $Ga_{0.47}In_{0.53}As$/0.63 eV $Ga_{0.36}In_{0.64}As$ series connected tandem and a 10 cell monolithically interconnected module. The module showed a short-circuit current of 0.292 A/cm$^2$, an open-circuit voltage of 6.14 V, and a fill factor of 67.6% at a cell temperature of 52℃ and at a graybody emitter temperature of 1000℃ with 90% emissivity. The cells were double heterostructures with GaInAs/InAsP for improved passivation and were grown metamorphically on InP substrate. The bandgap 0.74 eV/0.63 eV was specifically selected for 1000℃ graybody emitter with 90% emissivity. The tandem device had a peak reflectance of 86-87% between 3.7 and 4.9 μm.

In 2019, Omair et al.[39] have demonstrated a 0.7 eV GaInAs TPV device, employing band edge spectral filtering. By combining a very high material quality GaInAs device with a good back reflector, a high conversion efficiency of 29.1% ± 0.4% at an emitter

temperature of 1207℃ was reported. The device had an average sub-bandgap reflectance of 94.6%. A trade-off exists between minimizing sub-bandgap parasitic absorption and minimizing thermalization loss by using an optimal bandgap TPV device. A 0.75 eV bandgap is well matched to an emitter temperature at 1207℃, balancing the tradeoff, resulting in high TPV efficiency. This study also suggests improvements in device parameters like lowering device series resistance to less than 0.01 Ω, improving the sub-bandgap reflectance to 98% by addition of dielectric spacer between the semiconductor and metal, improving the material quality to increase the internal luminescence efficiency to 98%, and finally adding an anti-reflection coating can improve the TPV efficiency to >50%.

In 2020, Narayan et al.[45] demonstrated a calorimetric test platform for accurate measurement of TPV efficiency. With a well-calibrated set-up, the team has demonstrated greater than 30% TPV conversion efficiency on GaInAs and GaAs devices with Au rear reflector. A different study from T. Narayan et al.[71] demonstrated GaInAs TPV devices with greater than 30% efficiency for 19 devices and greater than 35% efficiency for two devices. Thus, demonstrating the distribution of cells resulting from high-quality fabrication and characterization process.

In 2020, Schulte et al.[72] have demonstrated an inverted metamorphic 2-junction TPV device for thermal emitter temperatures greater than 2000℃. Traditionally, growing two metamorphic lattice-mismatched junctions needs a graded buffer layer between them and it will remain permanently in the device. In a PV application, the graded buffer will be mostly transparent but in the TPV application, the graded buffer contributes to a high degree of sub-bandgap absorption. So, the graded buffer needs to be removed for improved

TPV efficiency. Therefore, in this device, both the junctions are grown lattice-matched but are lattice-mismatched to the GaAs substrate, with a graded buffer layer between the device and the substrate. Thus, the graded buffer can be etched off after the substrate removal. The device is a 1.2 eV AlGaInAs top junction and 1.0 eV GaInAs bottom junction with a GaAsSb:C/GaInP:Se tunnel junction layer, step-graded $Ga_{1-x}In_xP$ buffer, grown on a GaAs substrate. In addition, a metamorphic GaInAs front contact layer was developed replacing a traditional GaInAsN contact layer as the GaInAsN material system is difficult to grow and is also lattice-mismatched to the top and bottom junction devices. This tandem device was characterized under an adjustable high intensity pulsed simulator simulating the 2150°C TPV blackbody spectrum. The device exhibited an estimated peak TPV efficiency of 39.9% at a 30% fractional effective irradiance, and 36% at full TPV irradiance. This study also shows that through improved sub-bandgap reflectance and reduced series resistance, the TPV efficiency can be increased further.

In 2021, LaPotin et al.[73] have demonstrated one of the highest reported measured TPV efficiencies of greater than 40%, which is one of the most efficient heat-conversion engines in existence other than simple cycle gas turbines. They demonstrate two different 2-junction TPV devices and compares the TPV efficiency and output power density. The first device is a 1.2 eV AlGaInAs top junction and 1.0 eV GaInAs bottom junction, with both junctions lattice-matched to each other and lattice-mismatched to GaAs substrate. The second device is a lattice-matched 1.4 eV GaAs top junction and a lattice-mismatched 1.2 eV GaInAs bottom junction grown on GaAs substrate. The first device 1.2 / 1.0 eV has the potential for higher power density and potential for a less stringent back surface reflector. The second device 1.4 / 1.2 eV has a reduced current density thus a lower series resistance

loss and a potential for higher efficiency at higher temperatures. The weighted sub-bandgap reflectance for the devices 1.4 / 1.2 eV and 1.2 / 1.0 eV are 93.1% and 93% respectively. The 1.4 / 1.2 eV TPV device was 42.0% ± 1% efficient at 2400°C and had an average TPV efficiency of 37.4% in 1900 – 2400°C thermal emitter temperatures. The maximum power density was 2.39 W/cm$^2$ at 2401°C. Reduction in efficiency slope is due to reduction in fill-factor due to increase in series resistance loss. Reduction in $J_{sc}$ for temperatures greater than 2250°C is because of the cell becoming current limited by the bottom junction. As the thermal emitter temperature increases, the peak of the radiated spectrum shifts towards higher energy photons thus increasing the current density in the top cell and decreasing the current density in the bottom cell. As the two junctions are series connected, the current in both the junctions should be same and will be dictated by the junction with lower current density of the two. Therefore, at higher emitter temperatures, the device is bottom junction limited. Similarly, 1.2 / 1.0 eV reached a maximum TPV efficiency of 40.3% ± 1% at 2127°C, close to the predicted temperature of 2150°C where the 1.2 / 1.0 eV is optimal bandgap. The maximum power density was 2.42 W/cm$^2$ at 2297°C. For temperatures greater than 2150°C, the cell becomes bottom junction limited.

**2.6 Prior work on dielectric spacer layer for improved rear reflectors**

Many studies have demonstrated the use of a dielectric spacer layer between the semiconductor and the metal for improved rear reflectance near band edge emission, for improved photon recycling resulting in improved open-circuit voltage ($V_{oc}$). Some of the recent important works demonstrating the use of a dielectric spacer layer in between the semiconductor and rear metal discussed.

In 2018, N. Gruginkie et al.[74] demonstrated GaAs photovoltaic devices with point contacted rear mirror, GaAs contact layer etched everywhere except the point contacts and ZnS spacer. Though $MgF_2$ provided better reflectance improvements, thermally evaporated $MgF_2$ was found to delaminate from the semiconductor surface due to poor adhesion. This study compares front-junction and rear-junction GaAs devices and the influence of the contact layer etch and dielectric spacer on the reflectance and electrical performance of the device. The calculated total reflectance from the active layers of the cell increased from 63.5% at 100% contact coverage to 93.2% at 10% contact coverage. But, for the device with 10% contact coverage, the fill-factor was reduced by 3% due to an increase in series resistance. So, the optimized design should include smaller, evenly distributed point contacts. In the thin film front junction device, the non-radiative saturation current density was higher and no net boost in device electrical performance was noted. But in the rear-junction device, there's a significant decrease in reverse saturation current density. In another extended study from N. Gruginkie et al.[75], the rear contact coverage was further reduced to 6%, 3%, and 1.5% by keeping a constant point contact diameter of 20 μm. This study further explores the effect of front contact coverage on the photon recycling factor in addition to rear contact coverage. With 20 μm, 3% contacts, and 20 μm, 1.5% of contacts the drop in fill factor was only 1% and 3% respectively. Under conditions where the rear reflectance was no longer a limitation, optical and electrical modeling suggested that front grid coverage was the main factor for reduced photon recycling. This can be minimized by using a smaller front contact coverage fraction and a thinner front contact layer. Perimeter and interface recombination were identified as limiting factors for lower internal quantum

efficiency preventing further increase in the open-circuit voltage so lowering it will further boost the open-circuit voltage.

In 2017, Schilling et al.[76] have compared GaAs photovoltaic devices with rear GaAs substrate, rear Ag mirror, and rear $MgF_2$/Ag mirror with less than 1% contact coverage to study the effects of photon recycling under high-intensity illuminations. Their study shows that $MgF_2$/Ag mirror offers the highest boost in photon recycling amongst the compared devices. Enhanced photon recycling was found to reduce the reverse saturation current density component $J_{01}$ thus increasing the open-circuit voltage and this effect increase became stronger with increasing illumination intensity due to stronger radiative recombination. The device with $MgF_2$/Ag mirror exhibited an open-circuit voltage of 1230 mV at 182 suns intensity, a 28-mV increase compared to the device with rear GaAs substrate.

In 2019, Micha et al.[56] have demonstrated three different design strategies to implement optical cavities in a GaAs photovoltaic device to confine internal luminescence to enhance photon recycling. The three strategies are the use of an Ag rear reflector, dielectric-metal rear reflector, and a transparent conducting oxide (TCO)-metal rear reflector to a GaAs photovoltaic device. In strategy one, the Ag mirror yielded an internal reflectance of 95.2%. Strategy two of using aluminum-doped zinc oxide (AZO, a TCO)-Ag had poor contact resistance and an internal reflectivity of only 85% compared to the calculated 97%. Lower reflectance is attributed to increased surface roughness and increased absorption due to surface plasmon polaritons. In strategy three, a layer of sputtered AZO was necessary to improve Ag adhesion to $MgF_2$ and the structure yielded an internal reflectance of 98.6%. This structure used a reduced 1% rear contact coverage, and the point contact metal stack

was evaporated Pd/Zn/Pd/Au. Due to improved internal reflectance, strategies one and three were implemented on GaAs PV devices to yield an external radiative efficiency of 7.29% and 5.67%, $V_{oc}$ of 1075 mV and 1069 mV respectively, where both parameters are an improvement over a baseline GaAs PV device with absorbing GaAs substrate instead of a rear mirror.

In 2021, Helmers et al.[77] have demonstrated a 68.9% efficient photonic power conversion (PPC) device with a dielectric rear mirror through improved photon recycling and optical resonance. A photonic power converter is essentially a photovoltaic device that is designed for incident light source like laser or LED's. This study shows that by tuning the optical cavity and by increasing the rear reflectance through introduction of dielectric spacer between semiconductor and metal back contact, the photon recycling can be increased which leads to increased open-circuit voltage and device conversion efficiency. The study compared two rear-mirror configurations one with planar Au and the other with $MgF_2/AlO_x$/Ag reflector with 1.8% metal point contact areal coverage. By balancing the thickness of the $MgF_2/AlO_x$/Ag reflector, an optical cavity is created in the device for near bandgap emission to boost both the absorption and photon recycling. The study found that the PPC device with $MgF_2/AlO_x$/Ag reflector outperformed the PPC device with Au reflector and no reflector in many parameters. The PPC device with $MgF_2/AlO_x$/Ag reflector exhibited a peak spectral response of 0.653 A/W at 858 nm; the related thermalization loss reduced to 21 meV or 1% relative compared to Au reflector; the corresponding external quantum efficiency was 94.4% and the spectral reflectance was 95.5%; the electroluminescence intensity was 4.8 and 2.9 times higher than no reflector and Au reflector cases. The recombination current density $J_0$ decreased from 2.8 x $10^{-20}$

$A/cm^2$ to 1.3 x $10^{-20}$ $A/cm^2$ and 8.1 x $10^{-21}$ $A/cm^2$ for no reflector, Au reflector, and $MgF_2/AlO_x$/Ag reflector. Thus, the calculated effective lifetime in n-GaAs increased by a factor of 2.2 and 3.4 for Au reflector, and $MgF_2/AlO_x$/Ag reflector respectively. The median experimental ERE was 3.1%, 7.0%, and 10.8% for PPC devices with no reflector, Au reflector, and $MgF_2/AlO_x$/Ag reflector respectively. Due to all the improved device parameters, the PPC device with $MgF_2/AlO_x$/Ag mirror showed a measured 68.9% ± 2.8% at an incident laser intensity of 11.4 $W/cm^2$ at 858 nm.

**2.7 Prior works on TPV devices with PDBC like rear reflectors**

In 1979, R. Swanson[61] has proposed a solar TPV system with use of Si TPV cells. In this system a concentrated solar light heats a thermal absorber to 1727 – 2172℃ and the radiation from thermal absorber is converted to electricity using Si p-i-n photovoltaic device. Waste heat is extracted though a cooling system which maintains the cell at 70℃. The emitted thermal wavelength is red shifted compared to solar spectrum therefore minimizing the thermalization losses in Si device. The sub-bandgap photons can be reflected to the thermal emitter to minimize parasitic heat loss by using a Si device with Ag back mirror. The TPV cell tested with a resistively heated TPV test platform resulted in a TPV conversion efficiency of 26%.

In 1980, Swanson[37] demonstrated a world record Si TPV conversion efficiency of 29% at 2027℃ blackbody spectrum. The Si TPV device had a gridded, ion-implanted, low-doped junction, both on the front and backside for charge carrier separation, and a shallow, ion-implanted, high-doped region between the junction and metal for enhanced electrical contact. A 170 nm $SiO_2$ was used as a spacer layer on Si between the doped contact regions both in the front and back sides. The front side was metalized with screen-printed Ag only

above the junction region. The backside had a fully screen-printed Ag which doubled as electrical contact and rear mirror. On the front side, $SiO_2$ acted as an anti-reflection coating for bandgap radiation, and on the backside $SiO_2$ with Ag acted as an improved mirror. The Si wafer doping, contact coverage fraction of the ion-implanted contacts, Ag metal grids were optimized for improved electrical transport and reduced sub-bandgap parasitic absorptance. 1 nm of Ti was used as an adhesion layer between $SiO_2$ and Ag. Though Ti is absorptive than Ag, the presence of $SiO_2$ spacer reduced the impact on reflectance. To further improve this device, Swanson fabricated an interdigitated point contacted Si TPV device with contacts only at the intersection of the Ag grids, reducing the contact coverage fraction to nearly 1% from 32%. Swanson also proposed an interdigitated rear-contacted Si TPV device to further reduce parasitic sub-bandgap absorptance to further improve the TPV efficiency to 36%.

In 2020, Burger et al.[53] have compared three different spectral management strategies to improve TPV efficiency. The study compares the use of an Au rear reflector, an $MgF_2$ dielectric spacer with Au rear reflector, the use of an anti-reflection coating (ARC), and a combined case with $MgF_2$ + Au rear reflector with ARC on GaInAs device to that of a GaInAs device without any rear reflector. The $MgF_2$ spacer layer offered a significant boost in sub-bandgap reflectance compared to only Au rear reflector. They have also demonstrated that the device with only ARC can only improve the above bandgap absorptance thus the power density but not the TPV efficiency. But the combined case exhibited the highest spectral selectivity where the ARC improved the above bandgap absorptance and the $MgF_2$ + Au rear reflector improved the sub-bandgap reflectance.

In 2021, Fan et al.[40] have demonstrated a GaInAs device with an airgap dielectric spacer layer. Air as dielectric spacer eliminated parasitic absorptance in the dielectric material and maximized the refractive index mismatch at each interface. Au metal gridlines were fabricated on the rear side of the GaInAs device. This device was cold-welded to a clean, Au deposited Si surface for the mechanical handle. Then the substrate was removed, and the front-grid was fabricated. In this design, the airgap spacer between the Au gridlines and the Au on Si handle is the improved rear reflector. The measured device sub-bandgap reflectance was nearly 99% which represents a fourfold reduction in sub-bandgap absorptance. A trade-off exists between photocurrent and bandgap devices with sub-bandgap reflectance <95% but for devices with sub-bandgap reflectance near 100%, the spectral efficiency becomes almost insensitive to bandgap and emitter temperature. This GaInAs device with airgap dielectric spacer had a measured 30% TPV peak efficiency at 1182°C thermal emitter temperature.

**2.8 Prior works on a thermal grid-level energy storage system with TPV**

In 2016, Datas et al.[31] have shown a conceptual latent heat energy storage system using phase change material as a storage medium and thermophotovoltaics for electricity generation. Such systems have high energy storage density and high specific energy. Current phase change mediums (PCM) of choice offer low heat extraction and heat transport mediums limit heat transfer to a conversion. Therefore, PCM like Si and B which have a high melting point and high latent heat are suitable candidates for thermal energy latent heat storage. But Si is the second most available material and is the most economically viable option. Solidification of PCM material near emitter will not be a problem as the solid phase heat conduction of Si will mitigate the impact. This article

models the transient performance of this storage system using the quasi 1D analytical model in which the solid-liquid is a moving cylinder moving at a distance from the axial center assuming an adiabatic container and neglecting natural convection. In addition, TPV device performance was also calculated for an ideal, 0.5 eV bandgap TPV cell. Under an assumption of an ideal TPV device with back surface reflectance ~1, the lower emitter temperature does not affect the efficiency but only the output power. Such a system is theoretically scalable in terms of power from KW – MW, in terms of energy from KWh to MWh, discharge times in hours- days, and enables high thermal energy storage density. According to modeled results, discharge efficiencies can be in 20-45%, depending on device quality and electric storage densities in 200-450 KWh/$m^3$, which is comparable to Li-ion batteries.

In 2019, Caleb et el.[7] have shown that any storage system can be evaluated if its round-trip efficiency (RTE), cost per unit power (CPP), and cost per unit energy (CPE) are known. They also show that a storage system can be economically viable even if has a low RTE if the CPP and CPE are low. Based on this calculation, the authors propose a thermophotovoltaic - molten Si thermal energy storage system. In this system, the molten Si is stored in two tanks namely, the 'cold' Si tank at 1900℃ and the 'hot' tank at 2400℃. Energy storage happens by pumping the molten Si using a seal-less sump pump from the cold Si tank, nominally heated to 2400℃ using the excess electricity in the grid and storing the heated Si in the hot Si tank. Similarly, thermal discharge and electricity generation happen by pumping the molten Si from the hot tank through a graphite heat exchanger and storing the molten Si back in the cold tank. The graphite heat exchanger will be nominally around 2100℃ and will behave like a grey-body radiator. The photons from the heat

exchanger can be collected and converted to electricity using a multi-junction photovoltaic module. As a proof of concept, the authors demonstrated molten Si storage at 2000℃ and Sn pumping at 1400℃. For a thermal emitter temperature of 2100℃, the authors propose to use a 1.2 eV / 1.0 eV series-connected, multi-junction TPV device which could ideally have a ≥50% RTE and a CPP < $0.5 / W.

# CHAPTER 3

# MODELING AND EXPERIMENTAL METHODS

Chapter 3 describes the different tools and techniques that were used in this study. Initially the modeling methods used in this study are discussed followed by the experimental tools and techniques.

## 3.1 Modeling methods

The optical modeling methods used in this study are 1D transfer matrix method and 3D rigorous coupled wave analysis to understand the sub-bandgap reflectance properties of the GaAs device and the PDBC. The optical constants (n,κ) used in the modeling were measured using ellipsometry for the actual MOVPE grown device layers [Fig.6] and for the SU-8 photoresist. A set of samples were prepared in the beginning of this study and the optical constants were measured by J.A. Woollam ellipsometry services for GaAs device layers and for SU-8. The SU-8 optical constant dataset is compared along with $SiO_2$ in the section 4.2.1. For $SiO_2$[78], $MgF_2$[79], ZnS[80], Au[81], Ti[82], and Ag[83] the complex refractive index data were from the literature.

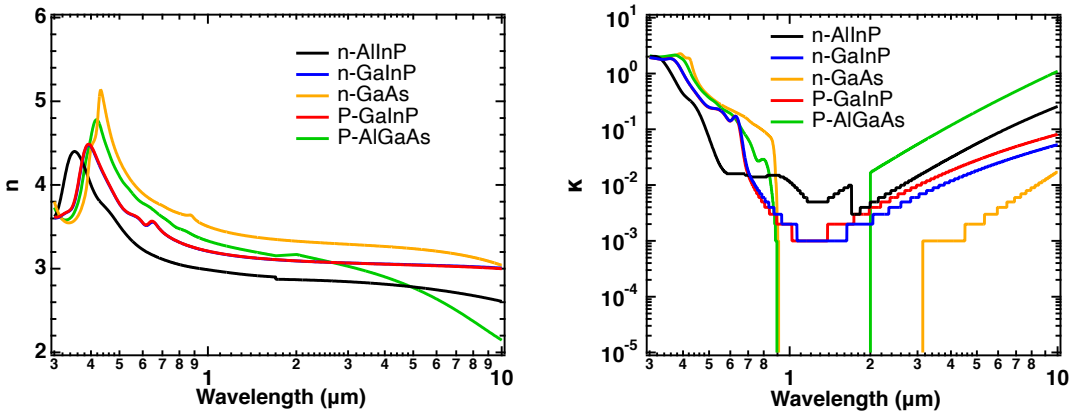



Figure 6. Optical constants (a) n (b) k for the GaAs TPV device semiconductor layers that were used in all the optical modeling works.

### 3.1.1 Transfer matrix method

The one-dimensional transfer matrix method[84] (TMM) is used to model the sub-bandgap reflectance of GaAs PDBC TPV devices for different device layer parameters, dielectric spacers, and metal back contacts. The TMM is implemented using an open-source TMM package[85] in Python. A plane wave excitation in both p- and s- polarization is incident from air. The calculated total reflectance is an average of the p- and s-polarization excitations. As a first order approximation, the PDBC is modeled as a linear interpolation between the 0% CCF and 100% CCF though it is shown later in this study that it is not an accurate representation and a full solution to Maxwell's equations are required.

### 3.1.2 Rigorous coupled wave analysis

The PDBC structure is a three-dimensional structure, requiring a full solution to Maxwell's equations to rigorously model the reflectance. We use an open-source RCWA[86] Python library[87] called $S^4$ developed at Stanford University throughout this study. In RCWA, in each layer, the electromagnetic field is expanded as Eigen modes with Fourier basis in the plane of periodicity with exponential dependence in the normal direction. The Eigen modes are coupled through dielectric distribution within each layer. The modal expansion coefficients are related at each layer interface to satisfy field continuity conditions in Fourier basis. We model each semiconductor material with an experimentally measured wavelength dispersed complex refractive index. The models were run simultaneously in multiple CPU cores in order to minimize the computation time.

## 3.2 Experimental methods

### 3.2.1 MOVPE epitaxial GaAs TPV devices

The inverted GaAs devices were grown in a custom-built, atmospheric pressure, metal-organic vapor phase epitaxy (MOVPE) reactor [Fig. 7]. Single-crystal Si-doped (100) n-GaAs substrates miscut by 2° towards (111)B, were used for all the growths. Standard[88]

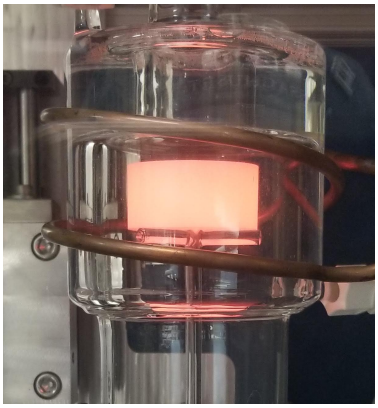


Figure 7. Custom-built quartz MOVPE chamber. The substrate sits on a carbon susceptor which is heated by a high-frequency induction coil.

metal-organic precursors were used in the MOVPE reactor; details can be found elsewhere[51]. As we will describe below, the processing sequence first involves the fabrication of the PDBC back mirror. Then the sample was secured to a mechanical handle using epoxy and the growth substrate was removed by chemical etching. Finally, the front grids were deposited, and the individual devices were isolated by wet-chemical etching.

### 3.2.2 Device fabrication methods

Photolithography and device fabrication was done in a class 100 and 1000 cleanroom. The photolithography step consists of photoresist spin coat, bake, and exposure steps. Spin coater and hot plate were in-built in the dry hood model 200CBX from the vendor Cost Effective Equipment. The hood blowers were always on for maintaining temperature and airflow uniformity. Exposure was done using an i-line (UV - 365 nm) light source, contact

photolithography mask aligner from ABM systems. The lamp illumination controller was from Photomask was designed using L-edit software and was fabricated by vendors Photomask Portal and Photo Sciences Inc. The discs in the photomask were approximated as hexagons for ease of fabrication. The photomasks were 4”x4” quartz with either iron oxide or chrome masking layers depending on the size of features, with chrome masks preferred for finer features. D.I. water was used as an index matching fluid between the photoresist and photomask during contact photo exposure.

Various photoresists were used for PDBC fabrication depending on the required features. AZ5214E inversion photoresist from Merck for photoresist pillar fabrication. Microposit S1818 positive photoresist from Shipley for defining vias on the dielectric. SU-8, a negative tone, permanent photoresist from Kayaku Advanced Materials, Inc. was used as a dielectric spacer. Similarly, various photoresists were used for front-metal grid fabrication depending on the required features. AZ15NXT is a negative photoresist from MicroChemicals. Megaposit SPR 220 7.0, SPR 220 4.5, are positive photoresists from Dow Chemicals AZNLOF2070 a negative photoresist from MicroChemicals.

Similarly, various developer solutions corresponding to each photoresist used were AZ 300 MIF developer from IMM for AZ5214E photoresist, Microposit MF CD 26 developer from Rohm and Hass Electronic Materials LLC for S1818 photoresist, SU-8 developer from Kayaku Advanced Materials, Inc. for SU-8 photoresist. The various photoresist strippers used were Remover PG from MicroChem Corp. for AZ5214E and acetone for S1818.

For electroplating metal point contacts and front-metal grids, sulfite gold – TSG-250 from Transene was used as Au electrolyte and the Watts nickel plating solution from Transene was used as Ni electrolyte. The electroplating was controlled using the Metrohm PGSTAT101 tool with a proprietary software Nova 2.1.2. A Au and Ni electrode were used as counter electrodes for Au and Ni electroplating respectively. Before the electroplating step, the semiconductor samples were surface prepped in 1:10 $NH_4OH:H_2O$ for 10 s.

The plasmaPro 100 COBRA reactive ion etch tool from Oxford instruments was used in the device fabrication process to clean the organic residues and to perform controlled etch of SU-8 photoresist.

Dektak-3 profilometer tool was used to measure the front-grid thickness and device mesa thickness.

A custom-built physical vapor deposition tool from Angstrom Engineering was used for $SiO_2$ and $MgF_2$ deposition runs controlled using proprietary software. Both $SiO_2$ and $MgF_2$ were deposited through e-beam evaporation and the substrate temperature was 100°C and 80°C respectively for reduced film porosity. The $O_2$ flow was set to 10 SCCM for $SiO_2$ depositions to maintain the stoichiometry. The substrate was constantly rotated for film uniformity. The film thickness calibration was done using ellipsometry measurements.

Temescal FC2000 tool was used for Ti, Au, and Ag blanket metal deposition. The metal deposition rates were current controlled through the proprietary software. The metal thickness was measured using quartz crystal monitor readings. For 1 nm Ti, the evaporation was set to 0.25 A/s to give a uniform deposition. The substrate holder rotated a 25 RPM for all depositions.

Optical profilometry was done using a VK-X260K laser microscope from Keyence and the images were analyzed through proprietary software from Keyence. An optical microscope MX6R was used for quick feature verification.

All the scanning electron microscopy (SEM) imaging was done using the Hitachi S4800 tool. Sample preparation involved mounting the sample to a sample holder using carbon tape. The sample was painted on the edges with Ag paint to enable electrical conduction for static discharge.

Ellipsometry for dielectric thickness and optical constants verification was done using the M2000 ellipsometer tool from J.A. Woollam. A proprietary software WVASE from the vendor was used for model fitting and analysis. Ellipsometry measurements were done at an angle of incidence of 60°, 65°, 70°, and 75° after required tool calibrations.

### 3.2.3 Inverted device fabrication

The inverted device fabrication process flow is shown in Fig. 8. After PDBC fabrication, the PDBC side of the GaAs device was bonded to a silicon handle substrate using a low viscosity epoxy[89]. The epoxy was cured at 100°C for 20 minutes on a hot plate. The GaAs substrate was completely etched off in 1:3 $NH_4OH$:$H_2O_2$ at room temperature in 20 minutes, revealing the GaInP etch stop layer. The etch stop layer was etched off in undiluted HCl revealing the GaAs/GaInNAs front contact layer. In the first photolithography step, the front grid was defined on the front contact layer using SPR 220 4.5 photoresists from Dow Chemicals followed by electroplating Ni and Au. After a second photolithography step, the devices were masked in the photoresist and were mesa isolated by alternating etching of unmasked device area of arsenide layers with 3:4:1 $H_3PO_4$:$H_2O_2$:$H_2O$ etchant, and phosphide layers with concentrated HCl etchant. Finally, the front contact layer was etched

off everywhere except beneath the front grids using 2:1:10 $NH_4OH:H_2O_2:H_2O$ to increase the light transmission to the absorber layer.

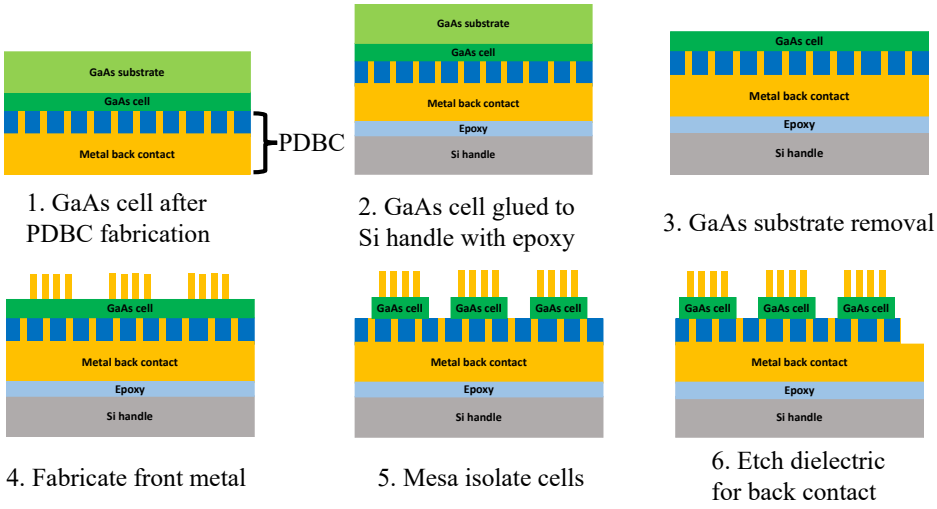



Figure 8. Schematic illustrating the inverted device fabrication process.

### 3.2.4 Fourier transform infrared spectroscopy (FTIR) reflectance measurement

All measurements are conducted by Antora Energy on an integrating sphere (PIKE technologies) coated with diffuse gold using the substitution method. A typical reflectance measurement is constructed from measurements of the following configurations:

1. Light is directed to the sample port with no sample in place.
2. The reflectance standard is placed on the sample port.
3. The sample of interest is placed on the sample port.

These three measurements are used with the tabulated reflectance spectrum of the reference to calculate the sample's reflectance spectrum. We note that the average reflectance of the integrating sphere changes in each case, which we account for with a correction term based on the geometry of the sphere[90] .

We use a NIST standard with a reflectance known to ± 0.3% absolute and have found an uncertainty of 0.4% introduced by sample-to-sample deviations, resulting in a ±0.5% uncertainty on our measurements. Measurements of separate NIST-calibrated samples referenced to our primary NIST standard yield reflectance values within the uncertainty bounds of the tabulated values.

We use an FTIR instrument to measure reflectance at the long wavelengths out to 15 μm that impact the total integrated sub-bandgap reflectance $R_{sub\text{-}BG}$, weighted by the 2200°C blackbody spectrum. For all $R_{sub\text{-}BG}$ values measured by FTIR, the total (diffuse + specular) reflectance is measured at an incident angle of 12° from the normal, which was the closest possible angle to normal incidence, from 0.95 to 10 μm wavelength. The short end of this range at 0.95 μm is used instead of the 0.871 μm GaAs bandgap wavelength to avoid low-intensity interference fringes in the reflectance spectrum close to the bandgap which may be a result of thickness variation in the GaAs device, and which could artificially lower $R_{sub\text{-}BG}$, even if the device is highly reflective. Similarly, the long end of this range at 10 μm is used as the blackbody power density for >10 μm is negligible. All the $R_{sub\text{-}BG}$ values measured by FTIR have a measurement error bar of ± 0.5%, in absolute % reflectance.

### 3.2.5 TLM measurement

The circular TLM[91] test structures [Fig. 9] were electroplated on the front contact, back contact, and PDBC for specific contact resistivity measurements. In this TLM structure there were six concentric TLM pads. The inner TLM pad had a constant radius of 100 μm and the outer TLM pad had a varying radius of 110 μm, 135 μm, 165 μm, 200 μm, 245

μm, and 300 μm. One clear advantage of circular TLM is that there is no need for mesa isolation as the current flow is between the concentric Au pads.

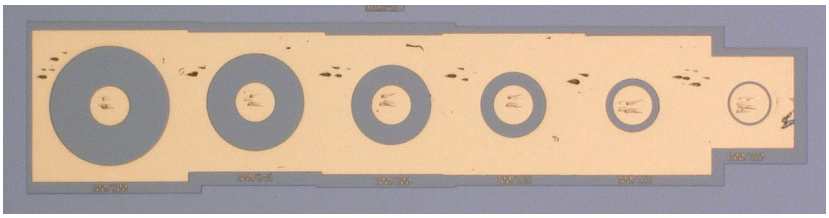


Figure 9. Photograph of circular TLM test structure used for specific contact resistivity measurements. The inner and outer Au TLM pads are shown and grey region between the pads is the semiconductor region where the current flows.

### 3.2.6 Device electrical characterization

The external quantum efficiency (EQE) and internal quantum efficiency (IQE) were measured using a custom-built tool[92]. The incident light was from a Xe light source and was split into different wavelengths using a metal diffraction grating. The light is incident on the sample at an angle in ~15-17° and was the closest possible angle to normal incidence. The reflected light was measured using a semiconductor detector.

One-sun IV, dark IV, and electroluminescence (EL) data were measured using XT-10 solar simulator from Boeing Spectrolab. A tungsten-halogen lamp was the source of illumination. Before one-sun IV measurements, the GaAs photocurrent density was calibrated using a GaAs photovoltaic reference cell, independently calibrated by Photovoltaic device performance calibration services, NREL. The dark IV is measured in the same setup at no illumination. The EL and thus the external radiative efficiency (ERE)[93] was measured using the same XT-10 setup but with a fiber optic cable pointing at the device that goes to the spectrophotometer which measures the luminescence spectrum. The calibrations and procedure are discussed in Ref. 93. The XT-10 measurements are controlled by custom software written in Igor.

The multiple suns IV i.e. IV at concentration measurement was done in high intensity pulsed solar simulator (HIPSS) from Boeing Spectrolab. The photo intensity was adjusted by changing the shutter position and by using a screen on the Xe flash-light source. The flash-light is energized from capacitor banks in turn controlled by custom software written in LabView. The incident light intensity was measured using an independently calibrated GaAs device.

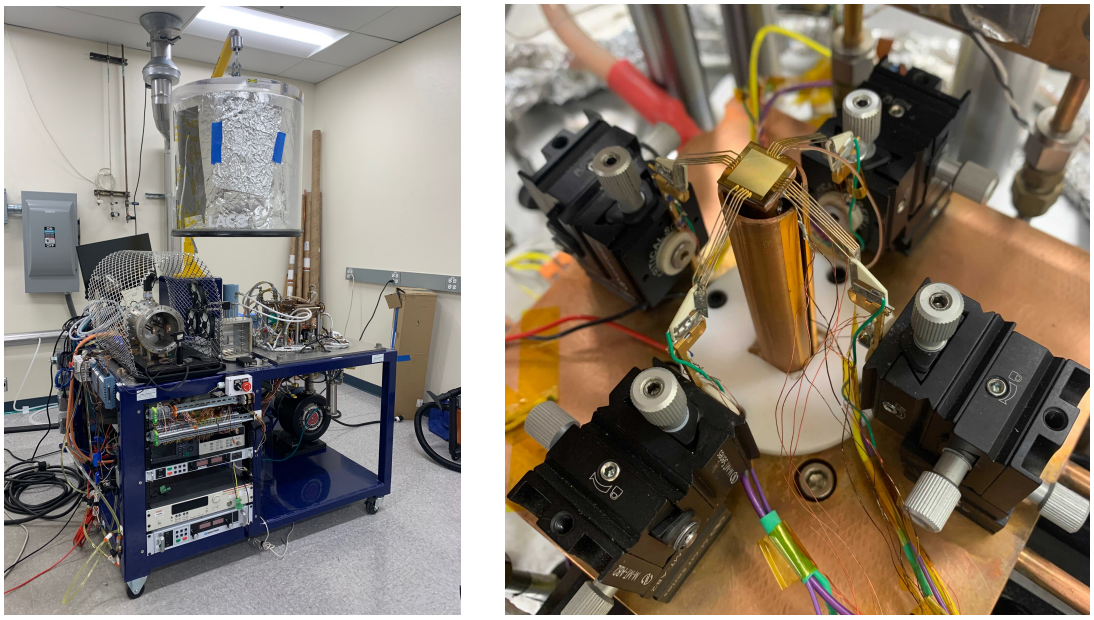
The total device resistance can be extracted by fitting the dark IV, ERE, and multiple-suns IV data together according to a generalized optoelectronic model described in the reference[94].

### 3.2.7 TPV efficiency measurement

TPV efficiency was measured in a custom-built calorimetric test platform[45] [Fig. 10]. The tests were carried out in closed bell jar under vacuum. An electrically heated graphite block represented the thermal emitter. The graphite block was insulated with porous carbon blocks. The device to be tested sat on a pedestal directly below the thermal emitter, separated by a diamond window.

Multiple Kelvin probes were used for electrical contact with separate probes for voltage and current measurement to eliminate contact resistance. For front contact, multiple probes uniformly contacted both the device busbars. For back contact, multiple probes uniformly contacted the back metal contact from the front side, on both sides of the device. The waste heat was accurately measured using thermocouples on the device, the pedestal, and the electrical probes. The temperature of the graphite block was measured using a heat flux sensor. The steady-state IV curves of the device, the incident heat, and the waste heat were measured at different emitter temperatures thus the TPV efficiency was calculated at

different emitter temperatures. The accuracy and reliability of TPV measurement was described in the reference[71].



(a) (b)

Figure 10. Photographs of the custom-built, calorimetry based thermophotovoltaic device measurement platform (a) full setup with removable bell jar vacuum enclosure and other electronics, (b) the TPV device placed on a pedestal contacted with kelvin probes for electrical power output measurement. (Image courtesy: Cecilia Luciano, Antora Energy)

# CHAPTER 4

# TPV DEVICE MODELING

## 4.1 Series resistance modeling

Series resistance ($R_{series}$) of the TPV device is a major factor in determining the TPV system efficiency. At high current density, high device series resistance results in high resistive ($I^2R$) loss. Therefore, the device series resistance should be minimized. The total device series resistance [Eq. 6] is the sum of series resistance contributions from front grids, bulk semiconductor, and PDBC assuming a simplified, lumped parameter, 1D model for all the resistive component calculations in this study. The bulk resistance contribution is given by Eq. 7[95]where $\rho_{bulk\text{-}semi}$ is the resistivity of the semiconductor bulk and $t_{bulk\text{-}semi}$ is the thickness of the semiconductor bulk. The bulk resistance contribution from the n-GaAs absorber is 1.7 x $10^{-3}$ m$\Omega\cdot cm^2$ and from p-GaInP heterobase is 3.5 x $10^{-4}$ m$\Omega\cdot cm^2$ which are almost negligible compared to the front-grid and PDBC resistance contributions as will be shown in the coming sections.

$$R_{series} = R_{front\ grid} + R_{bulk} + R_{PDBC} \tag{6}$$

$$R_{bulk} = \rho_{bulk-semi} t_{bulk-semi} \tag{7}$$

For both the front-grid and PDBC resistive contribution breakdowns, the equations are derived by calculating the fractional power loss from each component, a unit less quantity, and multiplying it with the characteristic resistance, $R_{ch}$ in $\Omega\cdot cm^2$ given by $V_{mp}/J_{mp}$ of the TPV device. This simple approximation holds for fractional power loss less than 20%[96].

The calculated resistive contribution and thus the $R_{series}$ are in the units of $\Omega \cdot cm^2$ as its calculated by multiplying the fractional power loss with $R_{ch}$, in $\Omega \cdot cm^2$. Therefore, the calculated resistive components are independent of the operating current density.

### 4.1.1 Contributions from front grid

The front-grid contribution to series resistance is the sum of contributions from the emitter lateral conduction resistance, semiconductor to metal contact resistance, finger, and busbar as shown in Eq. 8 assuming a simplified lumped parameter model. The busbar contribution can be negligible if the current is collected evenly from multiple points on the busbar. However, it can be higher if the current collection was at one single location on the busbar. The TPV devices used in this study had two rectangular busbars on opposite ends with fingers between them. For the experimental device electrical measurements, multiple Kelvin probes were used on both the busbars thus the busbar losses can be assumed negligible.

Fig. 11 shows total front grid contribution to series resistance, calculated according to Eq. 8-11[97,98,99] as a function of front grid height/thickness for different grid finger spacing and emitter sheet resistance. $P_{em}$ is emitter sheet resistance, $S_f$ is finger spacing, $w_f$ is finger width, $d_f$ is finger height, $l_f$ is finger length, and $L_t$ is transfer length. The front grid parameters used in the calculations for [Fig. 11] are as follows. The contact resistance of Ni/Au to the front contact layer and p-AlInP window layer is $13\times10^{-6}$ $\Omega \cdot cm^2$ and the sheet resistance is 50 Ω/sq as measured using circular TLM pads. $w_f$ was 10 μm, $l_f$ was 4 mm, and device dimension was 0.8 $cm^2$.

The front grid contribution significantly decreases with an increase in grid height. For a 190 μm grid spacing and 50 Ω/sq emitter sheet resistance, the front grid contribution

decreases from 11 mΩ·cm$^2$ to nearly 4 mΩ·cm$^2$ for the grid height increase from 2 µm to 10 µm respectively. Similarly, front grid contribution significantly decreases for an increase in grid spacing. For 10 µm grid height and 50 Ω/sq emitter sheet resistance, the front grid contribution decreases from nearly 4 mΩ·cm$^2$ to nearly 0.8 mΩ·cm$^2$ for grid spacing decrease from 190 µm to 50 µm. The TPV device front grid design should be towards targeting taller grid and tighter grid spacing. Therefore, the recommended parameters were at least 10 µm tall front grids resulting in a 1:1 grid aspect ratio, if increasing the grid aspect ratio further is a fabrication challenge; a 50 µm grid spacing if the lower output power density resulting from higher grid shadowing loss is not a concern. Otherwise, a wider spacing like 190 µm can be used which still results in a very low (<5 mΩ·cm$^2$) series resistance contribution.

$$R_{front\ grid} = R_{front\ lateral} + R_{front\ contact} + R_{finger} + R_{busbar} \tag{8}$$

$$R_{front\ lateral} = \frac{S_f^2 \rho_{em}}{12} \tag{9}$$

$$R_{front\ contact} = \frac{S_f L_t \rho_{em} \coth \frac{w_f}{2L_t}}{2} \tag{10}$$

$$R_{finger} = \frac{l_f^2 S_f \rho_f}{3 w_f d_f} \tag{11}$$

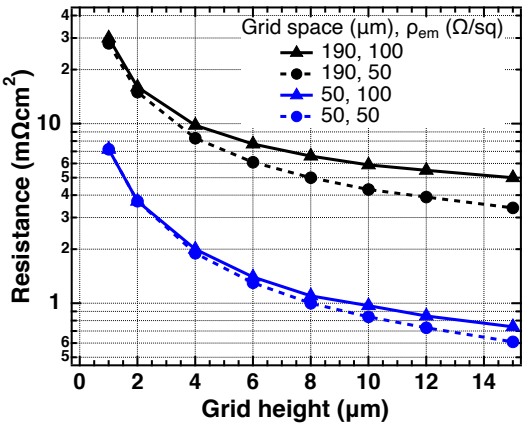



Figure 11. Total front grid loss as a function of front grid height for different grid spacing and emitter sheet resistance.

### 4.1.2 Contributions from PDBC

The series resistance contribution from PDBC is the sum of contributions from the lateral conduction, contact resistance, resistivity of the point contacts, and the back metal conduction [Eq. 12].

$$R_{PDBC} = R_{back\ lateral} + R_{back\ contact} + R_{point\ contact} + R_{back\ metal} \quad (12)$$

Due to the reduced contact coverage fraction in a PDBC TPV device, $R_{series}$ of the cell can easily become dominated by the sheet resistance of the PDBC. Babcock et al.[100] calculated the fractional power loss in a PDBC for metal point contacts in a square/hexagonal lattice arrangement in photovoltaic devices. A similar approach is considered here to analyze resistive loss components for the TPV devices.

Experimental values of specific series resistivity associated with the back contact have been measured on TPV devices and test structures, to quantify the expected resistive loss for two different back contact designs. For the case in which the back contact is intact (intact BCL case) in Fig.14, the lateral conduction layer (LCL) consists of a stack of a 240

nm p-GaInP:Zn ($2 \times 10^{18}$ $cm^{-3}$ Zn-doped) back surface field (BSF) layer, and a 35 nm p-AlGaAs:C ($4 \times 10^{19}$ $cm^{-3}$ C-doped) back contact layer (BCL), giving a total measured sheet resistance of 1030 Ω/sq. The specific contact resistivity ($\rho_{cb}$) between the Au and BCL was measured to be $1 \times 10^{-6}$ Ω·$cm^2$ for 100% contact coverage. Similarly, the average specific contact resistivity between a BCL and dielectric-metal point contacts in PDBC for electroplated Au point contact and e-beam evaporated 150 nm Ag pads was also measured through a test structure to be ~$66 \times 10^{-6}$ Ω·$cm^2$.

Since the p-AlGaAs:C back contact layer was heavily doped, it was a strongly free-carrier[101,102] absorbing material. For the case in which the back contact is etched away (etched BCL case) leaving only the p-GaInP:Zn BSF layer as in Fig. 14, we calculated in the previous section that the $R_{sub\text{-}BG}$ can be increased by ~0.9%. However, the p-GaInP:Zn layer alone in this etched BCL case has a higher resistance to lateral current transport than the combined p-GaInP:Zn/p-AlGaAs:C layers in the intact BCL case, with a measured sheet resistance of 6100 Ω/sq and specific contact resistivity $\rho_{cb}$ at the p-GaInP/p-AlGaAs/Au contact of $20 \times 10^{-6}$ Ω·$cm^2$ for 100% contact coverage. The measured average specific contact resistivity for PDBC was unavailable and was assumed to be ~$66 \times 10^{-6}$ Ω·$cm^2$, same as the BCL intact case. However, based on the 20 times increase in specific contact resistivity between intact BCL and etched BCL cases for 100% contact coverage, the specific contact resistivity for PDBC may also be higher.

The lateral spreading contribution of the PDBC is calculated as a function of point contact diameter and CCF according to Eq. 13[100]. The contact resistance contribution is calculated as a function of point contact diameter and CCF by incorporating the transfer length $L_t$ [Eq. 14]. The metal current has higher conductivity than the semiconductor layer

to which it is contacted. Therefore, the current crowds near the edge of the metal more compared to away from edge and this phenomenon is known as current crowding[91]. Therefore, the entire metal contact area will not participate in contacting and the physical dimensions of the metal contact area cannot be used to calculate the contact resistance. Therefore, we use a concept called transfer length $L_t$ which is the average distance the charge carriers travel beneath the contact in the semiconductor before it contacts the metal contact [Eq. 14.]. In the PDBC, the current flows radially in the semiconductor back contact layer and the contact area is approximated with the help of transfer length $L_t$ [Fig. 12b].

The contact resistance contribution equation is derived using the Eq. [15-22] based on the fractional power loss method described earlier. The total power loss in the back contact is calculated by Eq. 15, where the current is assumed to flow radially inwards from the perimeter of the imaginary circle with radius $r_2$ towards the circular point contact with radius $r_1$ where both the circles are concentric. The perimeter of the imaginary circle defines the maximum distance from which the current flows into a point contact. The sum of area of all the imaginary circles with radius $r_2$ around a point contact within a hexagonal unit cell is assumed to be equal to the area of the hexagonal unit cell itself[100]. The contact resistance R is calculated from Eq. 17, with measured specific contact resistivity value and the area available for electrical contact. The area for electrical contact is determined by the transfer length. If the transfer length is equal to or greater than the radius of point contact $r_1$, the entire area of point contact with radius $r_1$ is defined as the electrical contact area [Eq. 18]. If the transfer length is less than the radius of point contact $r_1$, the area of the annulus [Eq. 19] defined by the transfer length is defined as the electrical contact area and. After calculating the contact areas, the total power in the given region [Eq. 20] is calculated then

the fractional power loss is calculated according to Eq. 21. The fractional power loss is then multiplied with characteristic resistance $R_{ch}$ as described earlier to give the contact resistance contribution [Eq. 22]. Finally, the contact resistance contribution for transfer length equal to or greater than the radius of point contact $r_l$ is given by Eq. 23 and for transfer length less than radius of point contact $r_l$ is given by Eq. 24.

$$R_{back\ lateral} = \frac{\rho_{bulk}}{2t}\left\{r_2^2\left[ln\left(\frac{r_2}{r_1}\right) - \frac{3}{4}\right] + r_1^2\left[1 - \left(\frac{r_1}{2r_2}\right)^2\right]\right\} \tag{13}$$

$$L_t = \sqrt{\frac{\rho_{cb}}{\rho_{sheet}}} \tag{14}$$

$$P_{back\ contact} = I_{mp}^2 R = J_{mp}^2 A_p R \tag{15}$$

$$A_p = \pi r_2^2 \tag{16}$$

$$R = \frac{\rho_{cb}}{A_{con}} \tag{17}$$

$$A_{con\ (L_t \geq r_1)} = \pi r_1^2 \tag{18}$$

$$A_{con\ (L_t < r_1)} = \pi(r_1^2 - (r_1 - L_t)^2) \tag{19}$$

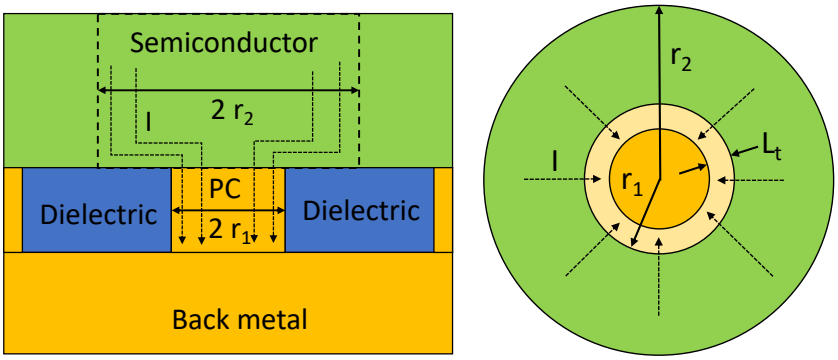
$$P_{back\ contact\ total} = J_{mp} A_p V_{mp} \tag{20}$$

$$F_{contact} = \frac{P_{back\ contact}}{P_{back\ contact\ total}} \tag{21}$$

$$R_{back\ contact} = F_{contact}\, R_{ch} = F_{contact}\, \frac{V_{mp}}{J_{mp}} \tag{22}$$

$$R_{back\ contact\ (L_t \geq r_1)} = \left(\frac{r_2}{r_1}\right)^2 \rho_{cb} \tag{23}$$

$$R_{back\ contact\ (L_t < r_1)} = \frac{{r_2}^2 \rho_{cb}}{r_1^2 - (r_1 - L_t)^2} \tag{24}$$



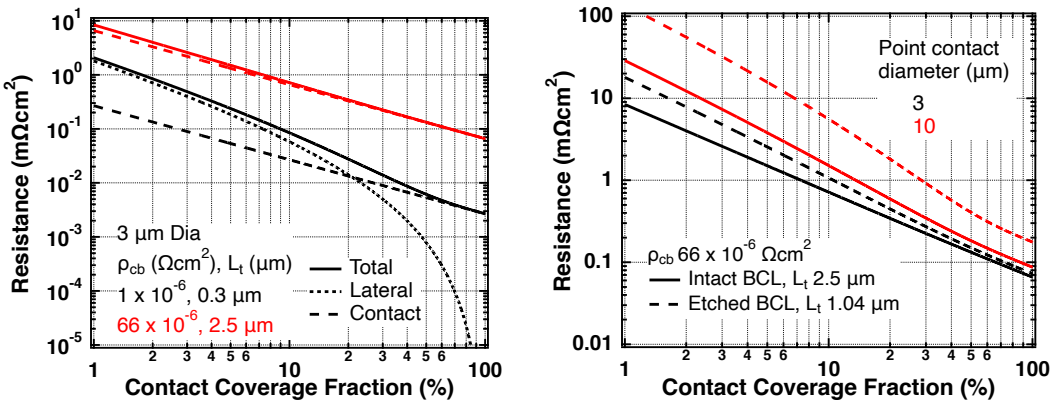

(a) (b)

Figure 12. Schematic of (a) cross-sectional view of PDBC (b) aerial view of point contact in PDBC illustrating the current flow (I) in the PDBC, imaginary circle with radius $r_2$, point contact with radius $r_1$ and transfer length $L_t$.

Fig. 13a shows the resistive contribution to $R_{series}$ in the PDBC of a GaAs TPV device, calculated as a function of CCF for 3 μm point contact and for two different specific contact resistivity at sheet resistance value of 1030 Ω/sq. The calculated transfer length is 0.3 μm and 2.5 μm for specific contact resistivity of $1 \times 10^{-6}$ Ω·cm$^2$ (lower $\rho_{cb}$) and $66 \times 10^{-6}$ Ω·cm$^2$ (higher $\rho_{cb}$) respectively. The total resistance contribution is dominated by lateral resistance for $L_t$ 0.3 μm (lower $\rho_{cb}$), for CCF <20% and by contact resistance for CCF

>20%. The total resistance contribution is dominated by contact resistance for all CCF for $L_t$ 2.5 μm (higher $\rho_{cb}$). The lateral contribution is significantly decreasing at higher CCF's due to increased number on point contacts and thus reduced point contact spacing (pitch). The pitch map [Fig. 15] is the nearest neighbor spacing between the metal point contacts (pitch) as a function of point contact diameter and contact coverage fraction. For a given point contact diameter 3 μm indicated by dash-dot line and 10 μm indicated by dashed line), as the contact coverage fraction increases the pitch decreases. The lateral distance travelled by the current before reaching the point contact is much smaller for a PDBC design with a smaller pitch compared to a wider pitch. Therefore, the lateral resistance contribution is much smaller for a PDBC design with a smaller pitch compared to a wider pitch.

Fig. 13b shows the resistive contribution to $R_{series}$ in the PDBC of a GaAs TPV device, calculated as a function of CCF for 3 μm and 10 μm point contact diameters at a constant




(a) (b)

Figure 13. Resistive contribution to series resistance as a function of contact coverage fraction (CCF) in a PDBC of GaAs TPV device (a) Total, lateral, and contact resistance for metal point contact diameter 3 μm, and two different specific contact resistivities. (b) Total resistance for metal point contact diameter 3 μm and 10 μm, and for p-AlGaAs back contact layer (BCL) intact and selectively etched everywhere except point.

specific contact resistivity of 66 × $10^{-6}$ Ω·$cm^2$ for intact BCL and etched BCL cases. For constant CCF, a smaller contact via diameter results in lower resistive loss. The higher sheet resistance of the etched BCL case, increases resistive losses relative to the intact BCL case, tending to at least partially offset the $R_{sub-BG}$ reflectance advantage for the etched BCL structure. The resistance contribution from etched BCL case may be much higher if the specific contact resistance value is also higher. For CCF greater than 10%, the total PDBC resistance contribution is <8 mΩ·$cm^2$ for all the four cases discussed and any of it can be used to implement the PDBC.

However, the fabrication challenges of forming very small contact vias are ameliorated if larger diameters and larger CCF can be used, at the same contact spacing. Lower CCF is preferred to achieve higher $R_{sub-BG,}$ but higher CCF and closer contact spacing are preferred for lower $R_{series}$. Thus, for a given contact diameter that is achievable for a specific patterning technology, a trade-off exists in the contact spacing and corresponding CCF that is chosen, to maximize $R_{sub-BG}$ and minimize $R_{series}$ in the quest for high GaAs TPV efficiency.

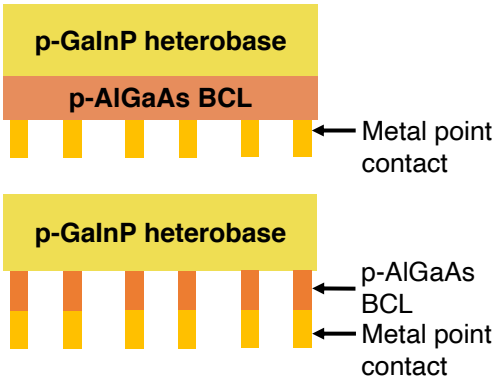



Figure 14. Schematic illustrating p-AlGaAs BCL intact (top) and p-AlGaAs BCL selectively etched with metal point contact as mask (bottom).

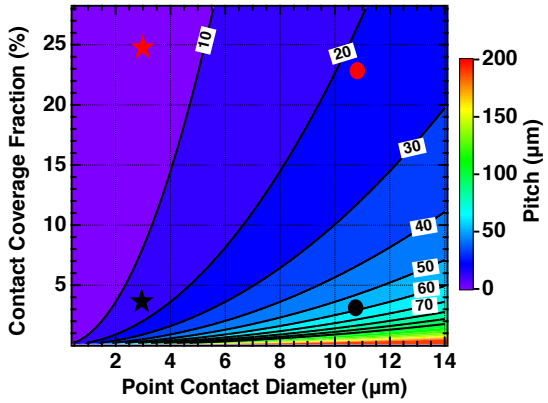



Figure 15. Spacing between point contacts (pitch) in a hexagonal lattice as a function of contact coverage fraction and point contact diameter. The four datapoints indicated are 2 different CCF for 2 different point contact diameter.

The cylindrical point contacts are made of Au and are only ~200 nm in height and a few μm in diameter depending on the design. The resistive contribution from these cylindrical point contacts was calculated to be negligible and was not considered in the analysis. The back metal contact was contacted using multiple Kelvin probes for current collection on either side of the device that did not have the busbars, from the front side. Though the current collection loss was negligible because of multiple probes, the current has to travel from underneath the device to the device perimeter which constitutes a significant loss. For an Au back metal dimension of 8 mm x 8mm, a 0.3 μm and a 2 μm thick metal would yield a resistive contribution of 4.3 mΩ·cm$^2$ and 0.64 mΩ·cm$^2$ respectively [Eq. 25]. Therefore, for reduced back metal contribution, a greater than 2 μm thick back metal is used.

$$R_{back\ metal} = \frac{b_m^2 \rho_m}{12 t_m} \tag{25}$$

## 4.2 Sub-bandgap reflectance modeling

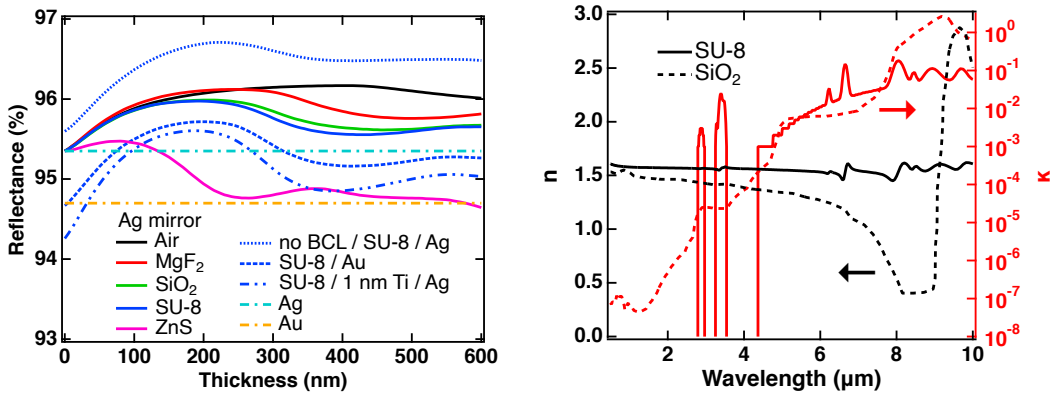
### 4.2.1 $R_{sub\text{-}BG}$ modeling and dielectric material selection using transfer matrix method:

$R_{sub\text{-}BG}$ is defined as the sub-bandgap reflectance of the GaAs TPV device, integrated from 0 to 90° angle of incidence θ, azimuthal angle 0 to 360°, for all wavelengths in 0.87 – 10 μm, weighted by the 2200°C blackbody spectrum, where $r_{sub\text{-}BG}$ is the sub-bandgap spectral reflectance as a function of wavelength as shown in Eq. 26. To achieve high $R_{sub\text{-}BG}$, we evaluate a GaAs TPV device with PDBC as shown in Fig. 4. The one-dimensional transfer matrix method[84] (TMM) is used to model the sub-bandgap reflectance of GaAs PDBC TPV devices for different dielectric spacers and metal back contacts. The PDBC structure is a 3D structure [Fig. 5a] requiring a full solution to Maxwell's equations to rigorously model the reflectance, as discussed in the reference[103] and later in this document. As a zeroth-order approximation, however, we initially calculate the reflectance of the PDBC as an interpolation between a 1D 0% CCF [Fig. 5b] and 1D 100% CCF [Fig. 5c] cases using Eq. 27.

$$R_{sub-BG} = \frac{\int_{\phi 1}^{\phi 2}\int_{\theta 1}^{\theta 2}\int_{\lambda 1}^{\lambda 2} r_{sub-BG} P_{sub-BG} \cos\theta \sin\theta \, d\lambda d\theta d\phi}{\int_{\phi 1}^{\phi 2}\int_{\theta 1}^{\theta 2}\int_{\lambda 1}^{\lambda 2} P_{sub-BG} \cos\theta \sin\theta \, d\lambda d\theta d\phi} \tag{26}$$

$$R_{sub\ BG}(CCF) = R_{sub\ BG\ 0\%}(1 - CCF) + R_{sub\ BG\ 100\%}(CCF) \tag{27}$$

For the TMM modeling shown here, a rear heterojunction GaAs TPV device stack as shown in Fig. 4, but with 0% CCF as shown in Fig. 5b, is evaluated using open-source TMM python library, at 0-90° angle of incidence. A 0° to 90° angle of incidence is used to model the blackbody radiation environment from the thermal emitter in the final grid-level energy storage TPV application where the photon emission has a Lambertian distribution across all angles. In Fig. 16a, we plot $R_{sub\text{-}BG}$ as a function of dielectric thickness for different dielectrics for 0% CCF (meaning the limit of no pillars through the dielectric) along with $R_{sub\text{-}BG}$ of Au and Ag planar mirrors (100% CCF, equivalent to zero dielectric thickness). Ray/geometric optics indicates that the dielectric with the lowest refractive index and extinction coefficient should result in the maximum $R_{sub\text{-}BG}$. Between gold and silver, Ag gives the higher $R_{sub\text{-}BG}$. Amongst the different dielectrics evaluated, the air has




(a) (b)

Figure 16. (a) Sub-bandgap reflectance for GaAs TPV device with a dielectric spacer layer between the semiconductor back contact layer and the metal back contact (0% CCF PDBC) as a function of dielectric thickness for different dielectrics with Ag back mirror, SU-8 / Au mirror, 1 nm Ti / Ag mirror, no BCL layer / SU-8 / Ag mirror, only Au, and only Ag mirror. All reflectance is weighted to 2200°C blackbody spectrum integrated at 0°-90° angle of incidence from 0.874 μm to 10 μm wavelength. (b) Optical constants (n, κ) of SU-8 and $SiO_2$ dielectrics. Real part (n) on the left-axis and imaginary part (κ) on the right-axis.

the lowest refractive index resulting in a maximum $R_{sub\text{-}BG}$ of 96.2% at a thickness of 400 nm with Ag mirror behind the dielectric. Similarly, ZnS has the highest refractive index thus resulting in the lowest maximum $R_{sub\text{-}BG}$ among the cases in Fig. 5a, of 95.5% at a thickness of 80 nm with an Ag mirror behind the dielectric.

SU-8 is a negative photoresist epoxy polymer that can be spin-coated, photolithographically processed, and hard-baked to remain in the TPV device as a dielectric spacer. Both $SiO_2$ and SU-8 have similar refractive indices [Fig. 16b] and yield similar maximum $R_{sub\text{-}BG}$ values of ~96% at a thickness of 205 nm and 195 nm respectively, with an Ag mirror [Fig 16a]. $R_{sub\text{-}BG}$ can be further increased to 96.7% if we can etch away the highly doped and highly absorbing p-AlGaAs back contact layer (BCL) between the contact vias. This p-AlGaAs layer acts as a lateral conduction layer as well as a back contact layer to metal. High doping in the back contact layer leads to lower sheet and specific contact resistance but also results in increased free-carrier absorption in the sub-bandgap spectrum. For certain low current density TPV applications, the p-GaInP heterobase layer can be designed to act as the lateral conduction layer. In this case, the p-AlGaAs back contact layer can be selectively etched everywhere except the metal point contacts. We refer to this structure as the etched back contact layer (etched BCL) case.

As a special case, the maximum $R_{sub\text{-}BG}$ for a GaAs TPV device with SU-8 / 1 nm Ti / Ag mirror is calculated to be 95.6%, just 0.5% lower than the SU-8 / Ag mirror. The 1 nm of Ti is used as an adhesion layer between SU-8 and Au or Ag and has lower reflectance compared to Au or Ag. Even with this 1 nm Ti layer to provide robust metal-to-dielectric adhesion in practical devices, we get an absolute boost in $R_{sub\text{-}BG}$ of 0.9% compared to the baseline case of a 100% CCF Au-only back contact.

Based on the TMM modeling and real-world material processing considerations, SU-8 and $SiO_2$ dielectrics are chosen to demonstrate two different PDBC fabrication methods, which in principle should yield a similar boost in $R_{sub\text{-}BG}$ compared to the planar Au back contact with 100% CCF. The TMM modeling indicated that $R_{sub\text{-}BG}$ is not highly sensitive to the dielectric spacer thickness, thus any thickness in the 150 – 220 nm range is sufficient for SU-8 and $SiO_2$.

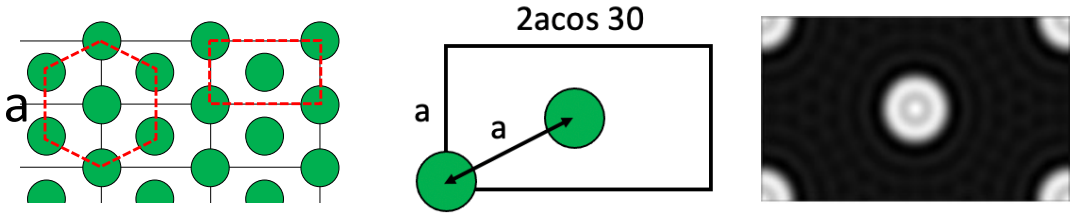
### 4.2.2 Diffraction effects from the PDBC using RCWA method

Reflectance from the device can be calculated with the transfer matrix method (TMM), looking at coherent wave interference between forward- and backward-propagating waves. The reflectance from the dielectric/metal mirror and from the metal point contacts are different, in general, and to first order the total reflectance can be approximated as an area-weighted superposition. That is, the reflectance from the PDBC can be approximated as a linear interpolation between 0% CCF and 100% CCF using 1D TMM analysis. However, 1D analysis is not a completely accurate representation because the PDBC structure is composed of metal point contacts that are periodic in the xy-plane, forming a two-dimensional (2D) grating structure, with constant height in z-direction. The characteristic length scales of the PDBC structure are the contact diameter and spacing as compared to the incident wavelength, and will determine the working optical regime. Features that are much smaller and much larger compared to the incident wavelength do not diffract light and can be modeled as a one-dimensional (1D) problem[104,105]. However, feature sizes closer to the incident wavelength will behave more like a diffraction grating. In this case, the PDBC will excite diffraction orders in the TPV device where each diffraction order may carry a certain fraction of reflected energy. Light that is diffracted to a propagation

angle outside of the escape cone from the semiconductor surface has a higher probability of being trapped in the structure and being parasitically re-absorbed, thus lowering the total reflectance and the TPV efficiency.

We investigate different PDBC design parameters for a GaAs TPV device using rigorous coupled wave analysis (RCWA)[86,87], a semi-analytical form of Maxwell's equations in Fourier space for three dimensional structures, to analyze the effects of diffraction in a GaAs PDBC TPV device and to narrow the parameter space for PDBC designs to increase sub-bandgap reflectance. This analysis plays an important role since there is a trade-off in PDBC designs between increasing the sub-bandgap reflectance and increasing resistive losses.

The PDBC is based on a hexagonal 2D unit cell with side a, and basis points are made of cylinders, as shown in Fig. 17a. However, as the RCWA code we use is based on a rectangular lattice, we reproduce the hexagonal lattice by using a rectangular lattice with two cylinders, one in the center, and another one (divided by each corner) in the corner of the rectangle [Fig. 17b] where a is the pitch (nearest neighbor center to center spacing between the metal point contacts). In Fig. 17c, we plot the relative permittivity of the PDBC unit cell as reconstructed by the Fourier expansion, and it confirms the rectangular lattice. In the reconstructed relative permittivity, the Au point contacts are shown as grey regions and dielectric as dark region. Initial simulations are done for a fixed point contact diameter and spacing for convergence tests. The total reflectance spectrum attained convergence when using 751 plane waves (Fourier expansion orders) which are used throughout this study.




(a) (b) (c)

Figure 17. (a) Hexagonal lattice used to model PDBC; (b) Unit cell of PDBC used in RCWA calculations showing the point contacts (green discs) and dimensions; (c) Calculated real part of relative permittivity of a unit cell used in RCWA PDBC with $SiO_2$ dielectric spacer and Au metal point contacts.

The pitch a, of the hexagonal lattice is calculated as a function of point contact diameter d and contact coverage fraction CCF in Eq. 28, and its dependence on these parameters is shown in Fig. 17b.

$$a = \sqrt{\frac{\pi d^2}{4 \cos 30 \ CCF}} \tag{28}$$

We modeled a GaAs PDBC TPV test structure [Fig. 18] with a 172 nm thick $SiO_2$ spacer layer with no front metal grid and no front semiconductor contact layer, because these two layers only exist at the widely spaced front grid locations. $SiO_2$ PDBC was used instead of SU-8 PDBC, as fabricating via with diameter <5 μm was challenging on 172 nm SU-8 photoresist through contact photolithography, primarily limited by the tool specifications. The 172 nm lies in the 150-200 nm thickness window that was determined in chapter 3, also the 172 nm $SiO_2$ was the deposited thickness for experimental samples. The different structures modeled are GaAs PDBC variations with Au point contact diameters of 1, 3, 5, 7, 10, and 20 μm for varying contact coverage fractions of 3%, 10%, and 20%. We calculate the total, specular and diffuse reflectance, and the absorptance of

each layer in the GaAs PDBC TPV device as a function of wavelength in the 0.3 μm to 10 μm range where the blackbody power density for temperatures >2000°C is significant[45]. A 12° angle of incidence is used for both s and p polarization in the models as the experimental sample reflectance were also measured at 12° angle of incidence using FTIR.

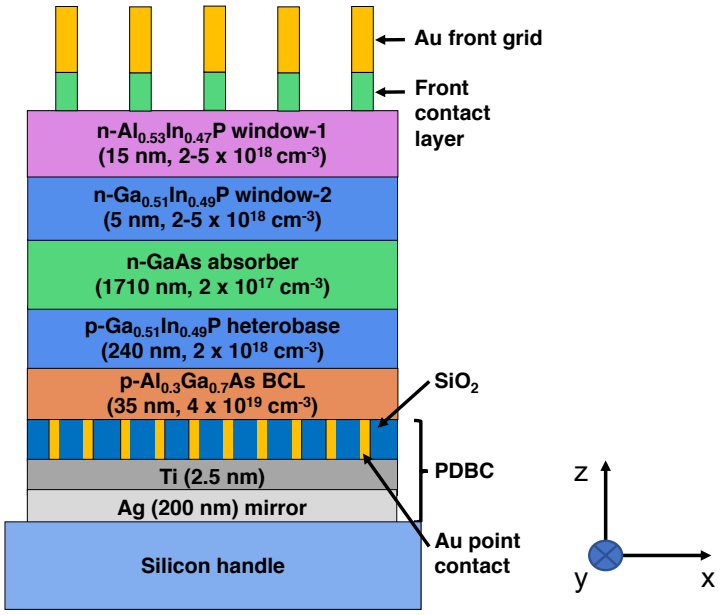



Figure 18. Schematic of a GaAs TPV cell with a PDBC on a Si handle. The Au front-grid and the front contact layer (200 nm n-GaAs + 100 nm GaInNAs) are excluded from the RCWA modeling (schematic not drawn to scale).

In experimental samples, the point contact diameter deviated from the mask parameters due to deviation in photolithographic pattern transfer. Change in point contact diameter also results in change in CCF therefore all the experimental samples will have different CCF (deviated from 3%, 10%, and 20% used in the calculations) and it becomes almost impossible to compare the effects of point contact diameter on sub-bandgap reflectance at different CCF. For instance, the average point contact diameter was measured using an optical profilometer (Keyence) and was found to slightly deviate from the nominal point

contact diameters, which resulted in actual average CCF values of 3.5%, 12%, and 24.3%. Therefore, for the ease of comparison of trends in the modeled and experimental data, the experimental CCF values are compared to the modeled ideal CCF values of 3%, 10%, and 20%. The total (specular + diffuse) and diffuse sub-bandgap reflectance from the fabricated GaAs PDBC TPV test structures were measured using Fourier transform infrared (FTIR) spectroscopy at an incident angle of 12° from 0.87 μm to 10 μm and not at 0 - 90° to mimic the sub-bandgap reflectance in actual TPV environment due to tool limitations.

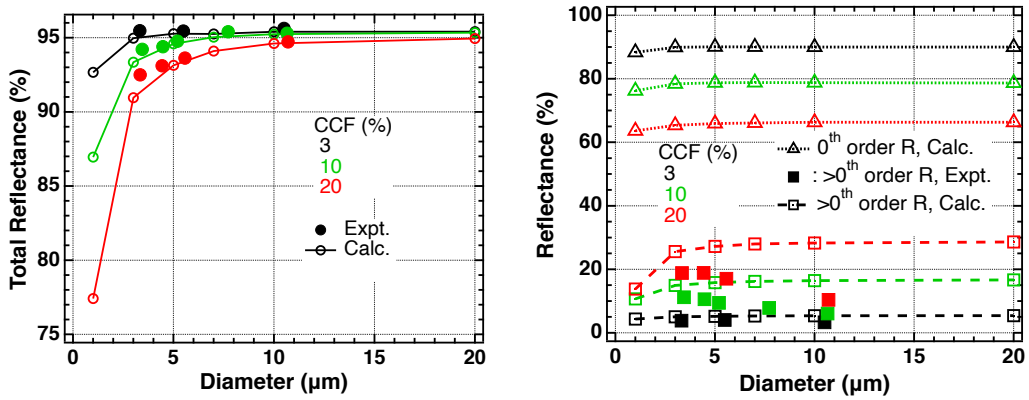
#### 4.2.2.1 Simulation and experimental studies on GaAs PDBC TPV device

Fig. 19a shows experimental and modeled total $R_{sub\text{-}BG}$ for light that escapes the front surface of the cell, as a function of point contact diameter for different CCF values. The total $R_{sub\text{-}BG}$ is the sum of specular and diffuse components. The figure indicates that the modeled total $R_{sub\text{-}BG}$ depends on point contact diameter and CCF. Modeled total $R_{sub\text{-}BG}$ decreases at higher CCF and this effect is stronger for smaller point contacts, such as 1μm diameters, than for 10-μm-diameter contacts. Total $R_{sub\text{-}BG}$ for the PDBC modeled with 1 μm point contact diameter is 92.7% at 3% CCF and is 77.4% at 20% CCF. In contrast, total $R_{sub\text{-}BG}$ the PDBC with 10 μm point contact diameter is ~95.4% for 3% CCF, and 94.6% for 20% CCF. Total $R_{sub\text{-}BG}$ stays at a high value for a wide range of point contact diameters from 3 μm to 10 μm for the smallest CCF shown, 3% CCF. The trends in the experimental total $R_{sub\text{-}BG}$ follow the calculated total $R_{sub\text{-}BG}$ fairly well, indicating the validity of the RCWA model for GaAs PDBC TPV test structures. To understand this further we will take a look at the modeled and experimental diffuse $R_{sub\text{-}BG}$.

Fig. 19b shows the modeled specular ($0^{th}$ order), and the modeled and experimental diffuse ($>0^{th}$ order) components of $R_{sub\text{-}BG}$ for light that escapes the front surface of the cell,

as a function of point contact diameter for different CCF values. The specular component denotes the specular $R_{sub\text{-}BG}$. Data labeled diffuse in the legend is the sum of all the reflectance components other than the $0^{th}$ order, indicating the diffuse component of $R_{sub\text{-}BG}$ due to diffraction.

The modeled specular $R_{sub\text{-}BG}$ stays almost constant as a function of point contact diameter from 5 μm to 20 μm but decreases significantly for increasing CCF. Similarly, the modeled diffuse $R_{sub\text{-}BG}$ stays almost constant as a function of point contact diameter from 5 μm to 20 μm but significantly increases for increasing CCF. The decrease in specular and increase in diffuse $R_{sub\text{-}BG}$ at higher CCF suggests that more light is diffracted to off-normal angles, though it does not strongly depend on the point contact diameter. However, a difference was observed in the trends betxween modeled and experimental diffuse $R_{sub\text{-}BG}$. The experimental diffuse $R_{sub\text{-}BG}$ decreases with greater point contact diameter while the modeled diffuse $R_{sub\text{-}BG}$ almost remains constant for point contact diameters greater than 5 μm.




(a) (b)

Figure 19. (a) Experimental and modeled total sub-bandgap reflectance, and (b) modeled specular reflectance and experimental and modeled diffuse reflectance, weighted by the 2200°C blackbody spectrum as a function of point contact diameter, for different contact coverage fraction values, at 12° angle of incidence.

To understand these trends further, we will look at the total and diffuse reflectance spectra of four extreme PDBC cases those fabricated. These represent a narrow and wide point contact diameters at both low and high values of CCF. As mentioned earlier, the experimental GaAs PDBC TPV test structures had actual point contact diameters different from their nominal values. Thus, the experimentally measured PDBC specifications of point contact diameter and CCF for the four extreme cases are, 3.3 μm and 3.7%; 3.3 μm and 24.8%; 10.5 μm and 3.3%; and 10.7 μm and 22.9%. Therefore, the total and diffuse reflectance spectra are modeled for the experimentally measured PDBC specifications to compare with the FTIR measured reflectances. These 4 cases are highlighted on the pitch map [Fig 15b] as black or red stars or disks, with black representing low CCF and red representing high CCF.

Fig. 20 shows the modeled and FTIR measured total reflectance as functions of wavelength for the GaAs PDBC test structures. The normalized blackbody irradiance spectrum (blue curve) at 2200°C is superimposed on all the reflectance spectra. The reflectance curves show that there is an envelope function defined by the Fabry-Perot resonance for all the structures, that depends on the thickness of semiconductor and $SiO_2$ spacer layers. Constructive interference fringes due to the Fabry-Perot resonance show double peaks, which are more evident at 20% CCF, due to superposition of reflected waves from the $SiO_2$ dielectric spacer and the Au metal point contacts. The shallower of the two peaks is likely the reflection from Au, since it becomes lower with increasing wavelength as would be expected for strong free-carrier absorption compared to $SiO_2$. As the CCF increases, the Au point contact area increases, resulting in greater loss. In addition, there

are also finer peaks superimposed on this envelope, where the 3 μm, 20% PDBC shows multiple sharper peaks.

The sharper absorption peaks indicate that sub-bandgap wavelengths strongly interact with PDBC when the point contact diameter and pitch are comparable to electromagnetic wavelengths. In particular, the pitch is smaller than 10 μm for the 3.3 μm, 24.8% case, as indicated by the red star in Fig. 15 and this case showed multiple sharper peaks in its reflectance spectrum while the other three PDBC cases have a pitch > 10 μm and their total reflectance do not show these sharper peaks. The 10.5 μm, 3.3% (black disk) case has a pitch > 50 μm and its total reflectance is similar to reflectance from a GaAs TPV device with a planar rear mirror. The blackbody irradiance spectrum indicates that the blackbody power quickly drops to less than 20% for wavelengths greater than 3 μm. Therefore, the wavelength region where the reflectance enhancement from PDBC is most strongly needed is from ~0.9 to 3 μm.

Among the four different PDBC designs shown, the higher CCF designs show lower modeled maximum reflectance peaks compared to lower CCF PDBCs in the range of highest blackbody irradiance. However, at lower blackbody temperatures, the irradiance spectrum will red-shift towards higher wavelengths, where the destructive interference fringes are deep, implying strong absorption enhanced by the PDBC.

The experimental total reflectance curves [Fig. 20] do not precisely agree with the modeled total reflectance curves in all four PDBC cases. This is likely due to minor deviations in the actual device layer thickness and complex refractive indices from the modeled values. This may be a result of non-uniform epitaxial growth in terms of thickness and doping or miscalculated device layer thickness. But the constructive interference fringe

position and width agree well in lower wavelength ranges. The destructive interference fringes of the modeled reflectance curves are much deeper than the experimental reflectance curves which indicate that the RCWA model calculates lower than actual reflectance values. The sharpness of the peak appears for an ideal model with a FP. The lower values appear for small inhomogeneities that effectively lower the quality factor of the optical cavity, lowering the absorption and therefore increasing the experimental reflectance. Nevertheless, these RCWA models capture the qualitative behavior and give a very good approximation of relative trends between different PDBC designs.

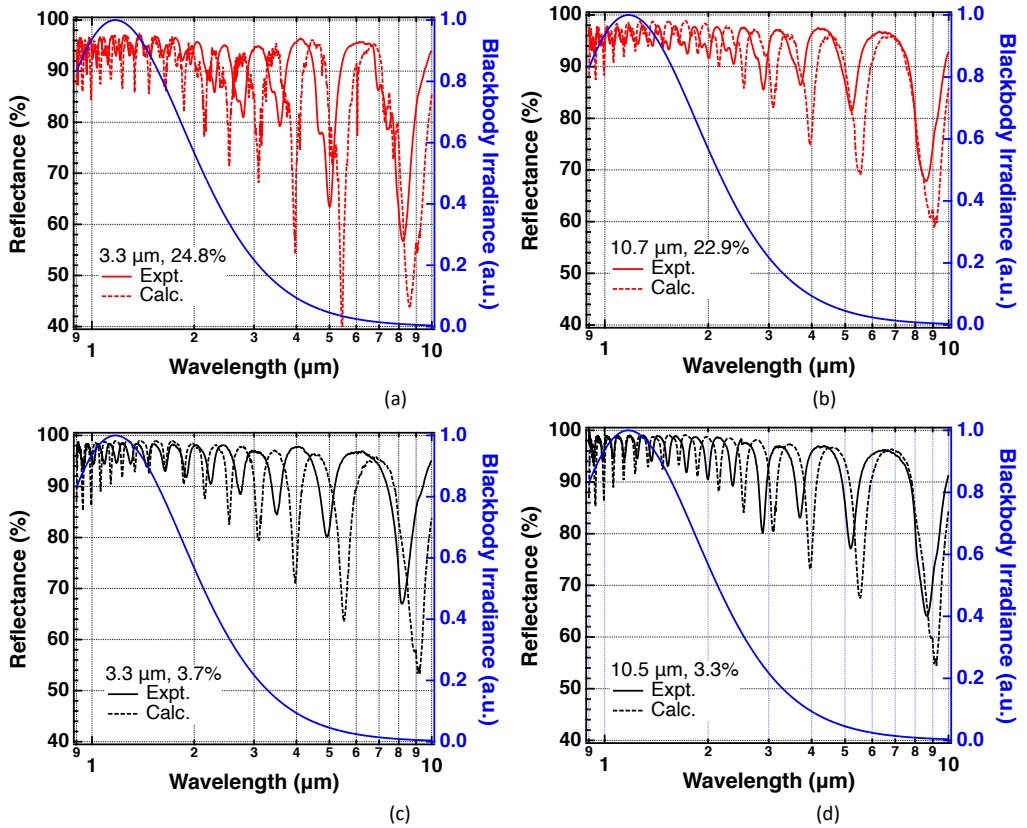



Figure 20. Experimental and modeled total sub-bandgap reflectance as a function of wavelength for different point contact diameters and contact coverage fractions: (a) 3.3 μm and 24.8%; (b) 10.7 μm and 22.9%; (c) 3.3 μm and 3.7%; and (d) 10.5 μm and 3.3%. Wavelength is on a log scale. The right-axis represents the normalized blackbody irradiance at 2200°C (blue curve).

Fig. 21 shows the modeled and measured diffuse reflectance as a function of wavelength for the GaAs PDBC test structures along with the normalized blackbody irradiance spectrum (blue curve) at 2200°C. The diffuse reflectance is greater at higher CCF than at lower CCF. But the modeled and experimental diffuse reflectance do not agree well. Only for 3.3 μm, 24.8% PDBC, the reflectance values at least look similar. For the other three PDBC cases, the reflectance values do not agree well at the lower wavelengths and tend only partially agree at higher wavelengths. To examine this further, we will calculate the diffraction orders and their corresponding diffraction angles for the previously mentioned four extreme PDBC cases.

Fig. 22 shows the diffraction angle of reflected waves that escape the front of the GaAs TPV device surface in air as a function of diffraction orders for different PDBC designs at a shorter wavelength of 1.06 μm and at a longer wavelength of 5.5 μm, along the y-direction in the rectangular unit cell [Fig. 17b]. The diffraction angles were calculated using the general diffraction grating equation [Eq. 29], with the pitch as the grating period in the y-direction and $2a\cos\theta$ as the grating period in the x-direction.

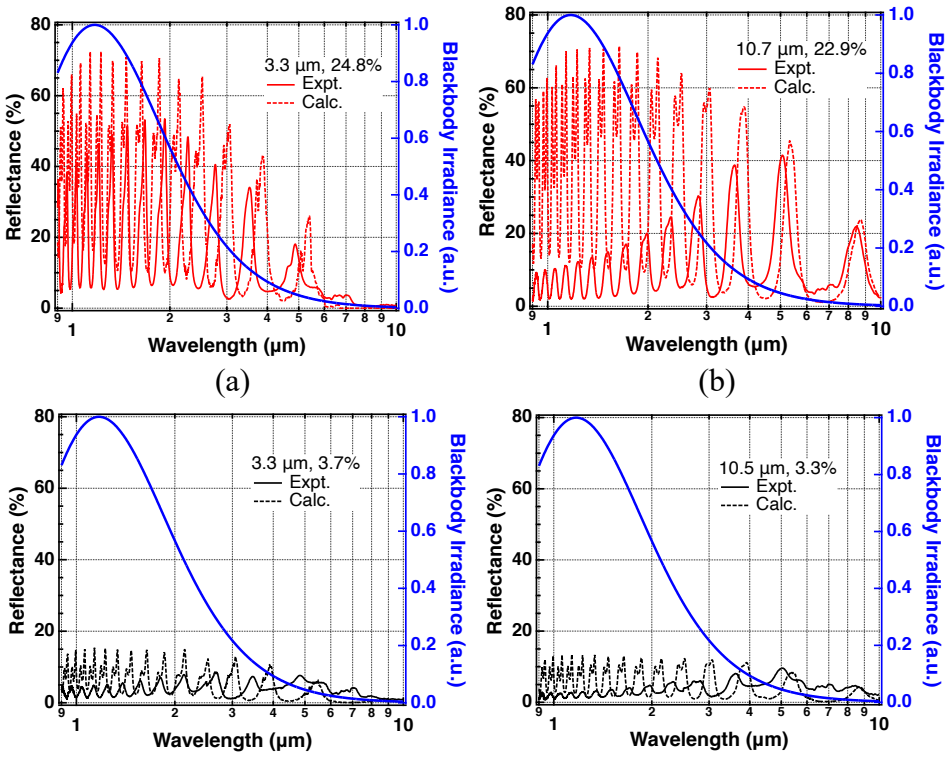



Figure 21. Experimental and modeled sub-bandgap diffuse reflectance as a function of wavelength for different point contact diameter and contact coverage fractions: (a) 3.3 µm and 24.8%; (b) 10.7 µm and 22.9%; (c) 3.3 µm and 3.7%; and (d) 10.5 µm and 3.3%. Wavelength is on a log scale. The right-axis represents the normalized blackbody irradiance at 2200°C (blue curve).

In Eq. 22, $n_{ref}$ is the refractive index of the medium into which the light is reflected (GaAs), $\theta_m$ is the angle of the diffracted order, $n_{inc}$ is the refractive index of the incident medium (GaAs), $\theta_{inc}$ is the incident angle in GaAs, m is the number of the order, $\lambda_0$ is incident wavelength in GaAs, and $\Lambda_y$ is the period of the grating (pitch *a*, in the y-direction). The diffraction angles calculated along the x-direction are not shown as they are similar to diffraction angles along the y-direction for similar diffraction orders. Three PDBC designs with increasing pitch among the extreme four PDBC designs discussed earlier are evaluated.

$$n_{ref} \sin \theta_m = n_{inc} \sin \theta_{inc} - m \frac{\lambda_0}{\Lambda_y} \tag{29}$$

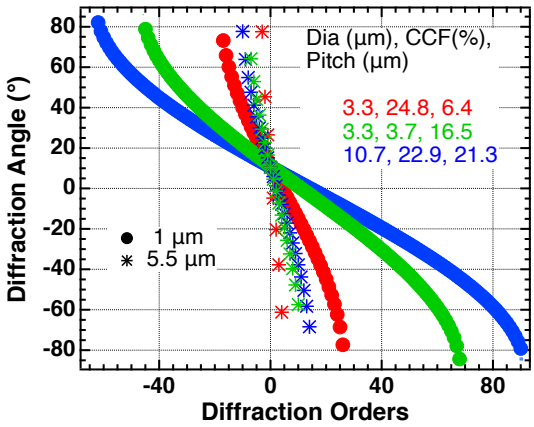



Figure 22. Diffraction angle as a function of diffraction orders for different PDBC designs with an increasing pitch at a lower wavelength (1.06 µm) and a higher wavelength (5.5 µm).

For a given incident wavelength and diffraction order, the diffraction angle increases with a decrease in pitch. At higher wavelength, the trend remains the same, but the angle variability is minimal. Also, for pitches significantly larger than the wavelength, for a significant number of diffracted orders around the $0^{th}$ order, the diffracted angle is close to the $0^{th}$ order angle (specular component). However, when the pitch is small (especially < 10 µm), the angle of diffracted orders deviates widely from the $0^{th}$ order angle both at lower and higher wavelengths. If the angle of diffuse orders is close to the $0^{th}$ order, the chances of it escaping through the specular port are enhanced. If the angle of diffuse orders deviates significantly from the $0^{th}$ order, the chances of it escaping through the specular port is minimal.

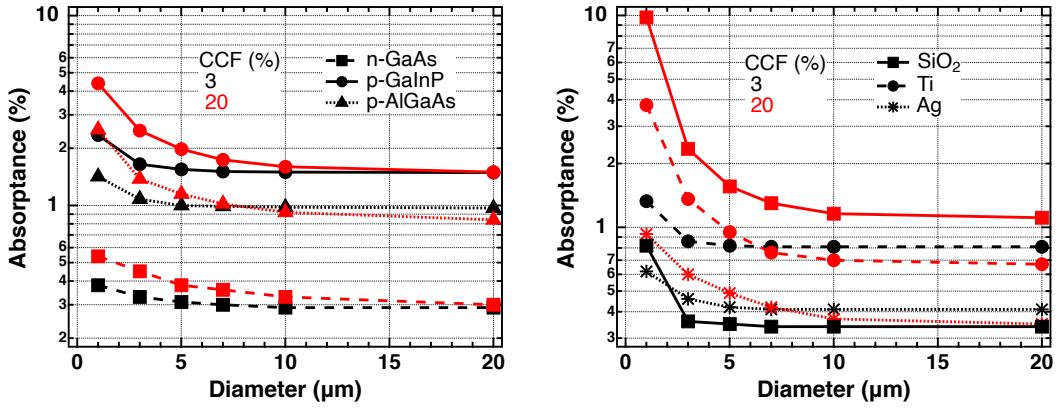
This explains the reason for better agreement between the modeled and experimental diffuse reflectance for the 3.3 µm, 24.8% PDBC case at both lower and higher wavelengths, while the wider pitch designs agree only at higher wavelengths. For PDBC designs with

wider pitch, the diffraction orders span the entire $90° \geq \theta \geq -90°$ in grating y-direction at lower wavelengths but have discreet angles at higher wavelengths. But as the pitch narrows (<10 μm), the orders tend to have discrete angles even at lower wavelengths and discrete and widely separated angles at higher wavelengths. There are diffraction orders that exist within the semiconductor but whose angle exceeds the escape cone. These orders experience total internal reflection in the semiconductor.

In addition, there may be many higher order diffraction modes that may be evanescent in the grating x- and y-direction. These total internal reflection and evanescent orders have a higher chance of getting absorbed within the device and can get parasitically lost in the reflection process. The diffraction equation can only calculate the diffraction angle of the orders and not the power in each order. So, we use the RCWA model to calculate weighted absorptance for a range of PDBC designs.

Fig. 23 shows the modeled weighted absorptance in each layer of the semiconductor [Fig. 23a] and PDBC [Fig. 23b] in a GaAs TPV device as a function of PDBC point contact diameter at different contact coverage fractions. The absorption in the n-AlInP and n-GaInP window layers is very small and is not shown. Among the semiconductor layers, the absorption in the p-GaInP absorber layer is the highest and remains constant with CCF for point contact diameters >10 μm up to 20 μm and increases by ~1.8 times when the point contact diameter is 1 μm. The absorption in p-AlGaAs and n-GaAs absorber also follows a similar trend as that of the p-GaInP. Absorption in the $SiO_2$ spacer layer Fig. 23b is small at lower CCF but significantly increases at higher CCF for all the point contact diameters.

For point contact diameter of 1 μm, the increase in absorption is more than 10 times larger at 20% CCF than at 3% CCF.




(a) (b)

Figure 23. Modeled diffuse sub-bandgap absorptance (a) in the different semiconductor layers of GaAs TPV device (b) in the PDBC weighted to 2200°C blackbody spectrum as a function of point contact diameter for 3% and 20% contact coverage fraction, at 12° angle of incidence.

This implies that at tighter pitch, the diffraction orders from the PDBC strongly increase absorption in the $SiO_2$ spacer layer. The trends in absorption in the Ti and Ag layers [Fig. 23b] as a function of point contact diameter at different CCF values are similar. The absorption stays nearly constant for point contact diameter >5 μm and increases at higher CCF when the point contact diameter is 1 μm. Except $SiO_2$ spacer layer, the trends in weighted absorptance are almost constant with respect to CCF in all the other layers. Therefore, the $SiO_2$ spacer layer or in general the dielectric spacer layer housing the point contact diffraction grating plays the dominant role in the parasitic sub-bandgap absorption at higher CCF.

Fig. 24 shows the absorption as a function of wavelength in the semiconductor layers [Fig. 24 a,b] and in the PDBC layers [Fig. 24 c,d] for GaAs TPV devices at two different CCFs. Fig. 24 a,b shows increasing absorption with wavelength in the semiconductor layers for both lower and higher CCFs, which would be consistent with higher free carrier

absorption as a possible absorption mechanism. As discussed previously, lower blackbody temperatures will shift the irradiance spectrum to longer wavelengths which will increase the weighted absorptance contribution from each layer. A decrease in pitch as a result of an increase in CCF (at constant point contact diameter) leads to higher angle diffraction orders that are absorbed in the semiconductor layers compared to lower CCF PDBCs. In Fig. 24 c,d the absorption in $SiO_2$ shows increasing absorption with wavelength. At lower CCF like 3.7%, the absorption peak in $SiO_2$ is <1% for wavelengths <7 μm however, for higher CCF like 24.8%, the absorption peaks range from 3% to 10% in the same wavelength range. In both the 3.7% and 24.8% CCF, the $SiO_2$ absorption is the strongest near the 9 μm wavelength which is probably from the absorption at resonance frequency.

In Ti, the absorption is stronger at shorter wavelengths (<2 μm) and is almost negligible at longer wavelengths at 3.7% CCF and a slight increase in absorption peaks at 24.8% CCF. The absorption in the Ag layer is the lowest among the PDBC layers and seems to increase with the wavelength as well. Compared to 3.7% CCF, showing smooth absorption spectra probably as a result of Fabry-Perot resonance, the 24.8% CCF absorption spectra shows characteristics of superposition of Fabry-Perot resonance and other finer peaks. As mentioned earlier, the finer peaks indicate the absorption resulting from diffraction orders that are trapped and parasitically absorbed in the device, originating from the $SiO_2$ – Au point contact two-dimensional grating structure.

The light that is diffracted from the periodic array of contacts in the PDBC structure at angles other than the incident angle is much higher than the fraction that escapes the cell and is measured. The diffracted propagation directions are largely totally internally reflected by the semiconductor surfaces and are trapped in the cell for many passes through the semiconductor absorber. Note that such light trapping is beneficial for many

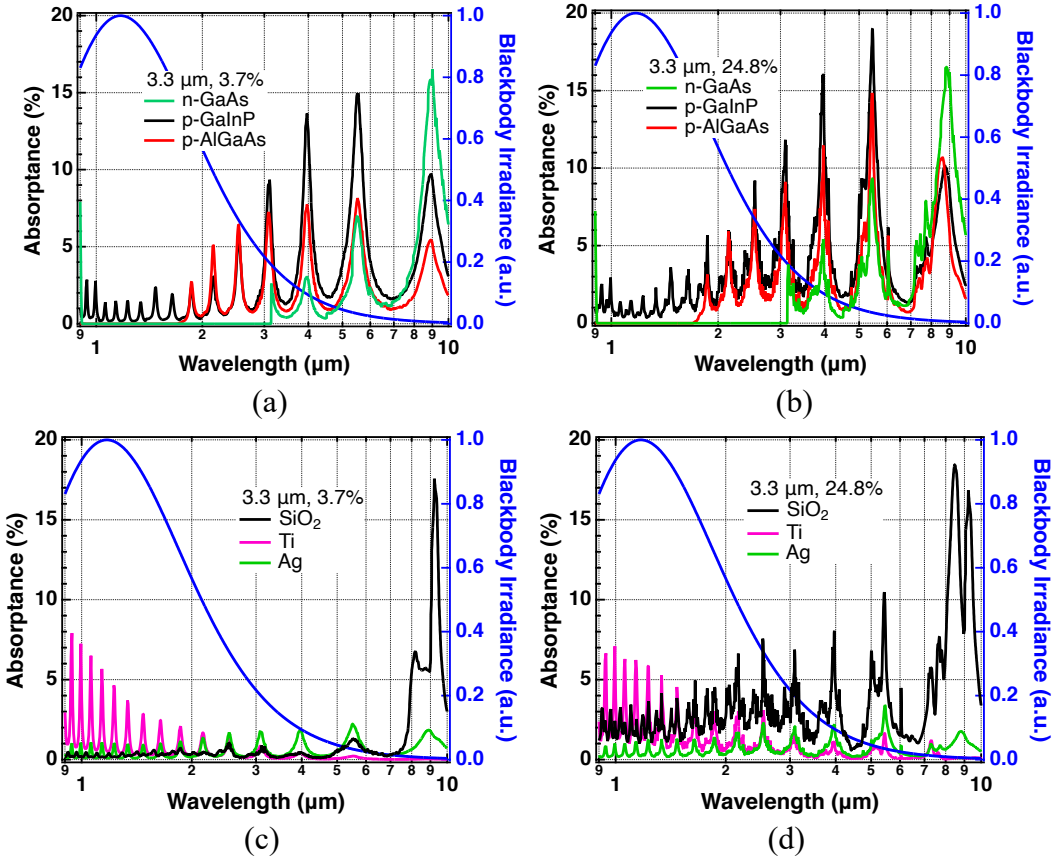



Figure 24. Absorption as a function of wavelength in semiconductor layers in GaAs PDBC TPV point contact diameter 3.3 μm (a) 3.7% (b) 24.8% CCF and in PDBC layers for point contact diameter 3.3 μm (c) 3.7%, and (d) 24.8% CCF.

photovoltaic cells to increase photogenerated current density, such as in cells with low absorption coefficients such as Si or very thin III-V and other direct gap solar cells. But because of the need to recycle sub-bandgap light to the thermal emitter, this light-trapping tends to be detrimental to the efficiency of TPV systems.

These results highlight the importance of modeling the full 3D electromagnetic wave diffracted from a PDBC structure. They indicate that a simple treatment where the reflectance from a PDBC is approximated as a linear combination of reflectance from the dielectric spacer and from the metal point contacts using 1D TMM is insufficient when the size of the point contacts approaches the wavelength of the incident electromagnetic radiation. In addition to light scattering and trapping from diffraction at a non-specular angle, absorption enhanced by different physical mechanisms like surface plasmon polaritons, localized plasmon resonance, etc. may become relevant at such length scales.

### 4.3 Recommended PDBC design parameters from resistance and reflectance modeling studies

PDBC resistance contribution modeling indicated that for low resistance PDBC (< 10 $m\Omega \cdot cm^2$), the design parameters should be smaller point contact diameter like 3 μm for smaller CCF like 3% and a specific range of wider point contact diameters at higher CCF. Similarly, the sub-bandgap reflectance modeling using RCWA method indicated that higher sub-bandgap reflectance is possible for smaller point contact diameter like 3 μm for smaller CCF like 3% and for wider point contact diameter like 20 μm for higher CCF like 20%. These two modeling results confirm that there exists a trade-off, given the contact spacing and corresponding CCF that is chosen, to maximize $R_{sub\text{-}BG}$ and minimize $R_{series}$ in the quest for higher TPV efficiency. Combining the resistance and reflectance modeling results, the recommended PDBC design parameters for GaAs TPV device for higher $R_{sub\text{-}BG}$ and lower $R_{series}$ thus higher TPV efficiency are point contact diameters in the rage of 3-6 μm and CCF in the range of 3-5%.

### 4.4 TPV efficiency modeling

In a TPV system, the thermal emitter is near the TPV device. Ideally, all the unabsorbed above-bandgap and sub-bandgap photons can be reflected in the thermal source to minimize parasitic heat loss. The net power absorbed by the TPV device is the difference between incident power from the thermal emitter and reflected power, and it is this net power absorbed that is used to calculate TPV device efficiency. Accordingly, the simple GaAs TPV efficiency[106] is semi-empirically calculated using Eq. 30-32, where $r_s$ is the characteristic resistance[107], $P_{tot}$ is total blackbody power incident on the TPV device, $P_{sub-BG}$ is blackbody power incident on the TPV device in the sub-bandgap spectrum, $P_{above-BG}$ is blackbody power incident on the TPV device in the above bandgap spectrum, calculated at 2200°C blackbody spectrum, and other symbols carry their usual meaning. TPV device efficiency is calculated [Fig. 25] using experimental TPV device electrical parameters from multi-sun current-voltage (I-V) measurement of a GaAs PDBC TPV device at 3.5 A/cm$^2$, corresponding to the short-circuit current density $J_{sc}$ of a GaAs TPV device for a 2200°C blackbody thermal emitter.

Efficiency modeling [Fig. 25] indicates that $R_{sub-BG}$ has a stronger effect on TPV efficiency than typical values of $R_{series}$ for $R_{sub-BG}$ greater than 90%. For $R_{sub-BG}$ above about 95%, an increase of only 1% (absolute) in $R_{sub-BG}$ is calculated to boost the TPV system efficiency by >3% (absolute). Nevertheless, due to the high operating current density, $I^2R_{series}$ losses can be significant if the series resistance is too high. Thus, both increasing $R_{sub-BG}$ and reducing $R_{series}$ have significant impacts on improving TPV efficiency.

$$\eta_{TPV} = \frac{Total\ output\ electrical\ power}{Total\ blackbody\ power\ - Total\ reflected\ power} \tag{30}$$

$$\eta_{TPV} = \frac{V_{oc}\, J_{sc}\, FF_{ideal}\, (1 - r_s)}{P_{tot} - \left(R_{sub-BG} P_{sub-BG} + R_{above-BG} P_{above-BG}\right)} \tag{31}$$

$$r_s = \frac{R_{series}\, J_{sc}}{V_{oc}} \tag{32}$$

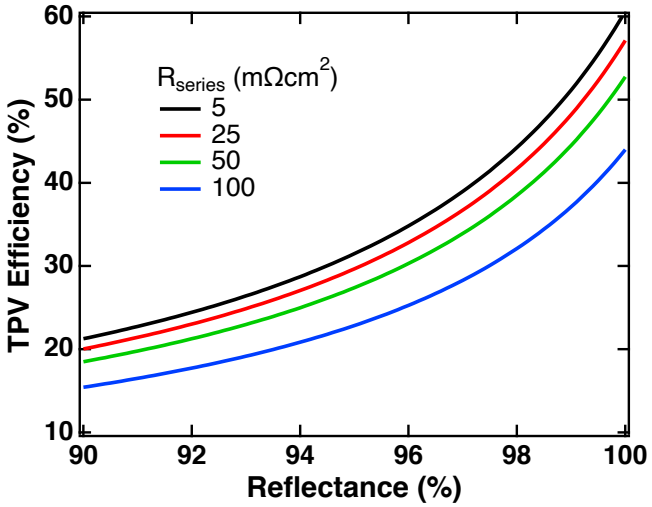



Figure 25. Simple GaAs TPV efficiency as function of $R_{sub\text{-}BG}$ and $R_{series}$ at 2200°C blackbody spectrum.

# CHAPTER 5

# EXPERIMENTS

## 5.1 Trade-off in different PDBC fabrication methods

Multiple articles introduce PDBC[56,75,77,] fabrication methods for various application. In this section, we explore PDBC fabrication methods for different dielectric materials in detail. For instance, two different methods to fabricate PDBCs with SU-8 photoresist – that can be spin-coated, photolithographically processed, and hard-baked to remain in the device permanently as a dielectric spacer – are explored. Similarly, two different methods to fabricate PDBCs with common evaporable dielectrics like $SiO_2$, $MgF_2$, and similar dielectrics as well as stacks of these dielectrics are also explored. These PDBC fabrication methods are developed with an eye for both commercial deployment with simple process flows, and for laboratory-scale use with improved flexibility.

The PDBC fabrication process flows discussed here are generally applicable in full or in part to semiconductor devices requiring a PDBC mirror or a reduced-area contact device architecture. However, these processes were mainly designed with a focus on III-V optoelectronic devices, specifically, thermophotovoltaic cells. Each process flow has its advantages and disadvantages. A sub-group of these process flows are dielectric specific or specific to the back contact layer (BCL) selective etch used [Fig. 14]. The primary purpose of a BCL selective etch is to reduce parasitic light absorption in the epitaxial stack, increasing both sub-bandgap reflectance[39,108] and photon recycling[109,110], both of which can be important in different optoelectronic applications [Fig. 16a]. Based on the selection of dielectric spacer between BCL and back mirror, the processes are broadly classified as

process A (for spin-on dielectrics), and process B (for other common evaporable dielectrics) [Fig. 26].

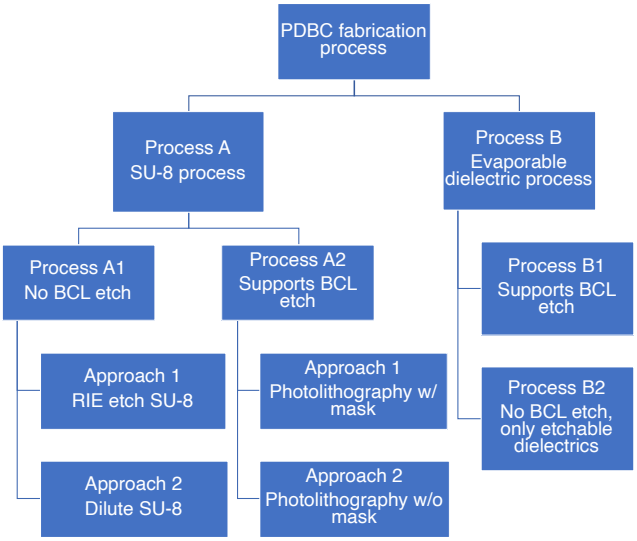



Figure 26. Classification of PDBC fabrication process.

### 5.1.1 Process A for SU-8 photoresist as dielectric

Process A [Fig. 27] is designed for SU-8 photoresist as a dielectric spacer. As pointed out in the previous section, several optoelectronic applications benefit from a selective etch of the highly doped BCL such that the BCL is present only between the semiconductor device and the metal point contacts. Etching highly doped layers can enhance sub-bandgap reflectance by reducing free carrier absorption and can enhance photon recycling by reducing band-edge absorption if the band edge energy of the BCL is similar to or lower than that of the active layer. The main purpose of highly doped BCL in these applications is to provide low specific contact resistivity to the metal point contacts and not necessarily to participate in lateral current transport. Depending on whether or not the BCL is etched, process A is classified into processes A1 and A2. Process A1 does not support a BCL selective etch while process A2 does support a BCL selective etch.

#### 5.1.1.2 Process A1 for SU-8 photoresist first fabrication

In the A1 process [Fig. 27a], SU-8 is spin-coated on the BCL, and vias extending through to the BCL are photolithographically patterned and developed. The vias are electroplated with the metals used to make electrical contact, followed by evaporated or sputtered metal to fabricate the back mirror.

Many optoelectronic applications require adjusting the optical interference condition depending on the need to selectively reflect or transmit at the required wavelengths. Thickness control in the dielectric layer of the PDBC can be used in this way to engineer the optical interference condition as required. In process A1, two different process approaches are considered to control the SU-8 thickness: approach 1 and approach 2.

In process A1, SU-8 6000.5 from MicroChem is used and is hereafter referred to as 100% SU-8. In approach 1, a thick, as-spun, SU-8 film is etched back to the desired thickness using reactive ion etching. In approach 2, the SU-8 6000.5 is diluted using CPG thinner from MicroChem to a concentration that will directly yield the desired thickness after spin coating.

In process A1, approach 1, we spin coat, photolithographically process, and hard-bake the 100% SU-8, as shown in the recipe in Table 1. Since the SU-8 is a negative photoresist, the UV exposed region stays, and the unexposed region clears after development. Thus, a via or a clear region in the SU-8 after development corresponds to a dark region on the photomask. The smallest diameter via we were able to fabricate on 100% SU-8 was 3 μm on a 1-mm-thick Si substrate and 5 μm on a 325-μm-thick GaAs substrate using contact photolithography, and deionized (DI) water as index-matching fluid during exposure.

After the hardbake, the SU-8 is etched to the desired thickness using reactive ion etching (RIE) in inductively coupled plasma (ICP) mode using the recipe listed in Table 1. The etched SU-8 thickness has a linear dependence on the etch time as shown in Fig. 28a for the RIE-ICP recipe listed in Table 1. The advantage of this approach is that any SU-8 residue in the via is also etched away, creating a cleaner semiconductor surface for better electrical contact.

However, etching induces surface roughness on SU-8 which may lead to light scattering at the interface with the subsequently deposited metal mirror and thus higher absorption in the device. The mean and RMS surface roughness on the 100% SU-8 surface measured using atomic force microscopy (AFM) at different etch times are shown in Fig. 28b. The average surface roughness on as-spun 100% SU-8 is 0.36 nm, and it increases by 14.7 times to 5.32 nm after a 66 s RIE-ICP etch in $O_2$ plasma. The surface roughness indicates the height difference between peaks and valleys, but scattering is determined by the periodicity of the peaks and valleys in the lateral direction. So, the higher surface roughness may or may not directly correspond to increased scattering. One advantageous effect of approach 1 is that higher surface roughness promotes adhesion[111] between SU-8 and the back metal contact.

In process A1, approach 2, SU-8 is diluted using CPG thinner to achieve the desired thickness as-spun. Fig. 29 shows SU-8 thickness at different % volume/volume (%v/v) concentrations diluted in CPG thinner and spun-coat at 6000 RPM. The average SU-8 thickness is 223 nm at 60% v/v and this composition is hereafter referred to as 60% SU-8. The recipe to photolithographically fabricate 60% SU-8 film with via regions for point contacts is listed in Table 2. The UV exposure dose depends on the thickness of the SU-8

film and this data is not completely available for SU-8 compositions other than 60% and 100%. The photomask is the same as the one described in process A1, approach 1. The average surface roughness measured using AFM is 0.19 nm on as-spun 60% SU-8, which is approximately two times lower than the average surface roughness of 0.36 nm on as-spun 100% SU-8, and far lower than the surface roughness of 100% SU-8 after RIE etching.

The SU-8 film thickness varies linearly with % v/v composition between 10% and 100%, and at 10% v/v SU-8 composition the average SU-8 film thickness is only 26 nm. Thus, SU-8 can be used as a replacement to $SiO_2$ , due to their similar refractive indices, in cases in which thermal / e-beam evaporation of $SiO_2$ results in detrimental effects on the device.

The disadvantage of approach 2 is that it is difficult to get good contact between a thin SU-8 film and the photomask in contact photolithography if the substrate is thin or has curvature. Poor contact can illuminate nominally dark resist areas through scattering, diffraction, or reflection. Therefore, the development of narrow spaces becomes difficult. This can be ameliorated by using index matching fluid between the SU-8 and photomask, through hard vacuum contact, and/or by using a photolithographic stepper instead of the aligner. With the 60% SU-8 in approach 2, the smallest diameter via we were able to fabricate was 5 μm on a - mm-thick Si substrate and 7 μm on 325-μm-thick GaAs substrate using contact photolithography, and DI water as index matching fluid.

Importantly, we found that 325-μm-GaAs substrates bend away from the photomask due to the force of the substrate vacuum, creating poor contact between SU-8 and the photomask. However, substrate vacuum is necessary to detach the thin GaAs substrate

from the photomask, bound by the capillary action of the index matching fluid, after exposure. A satisfactory process to overcome these issues is to turn off the substrate vacuum right before exposure to create good contact, and then turn on the substrate vacuum to detach the substrate from the photomask.

| Step | Equipment | Details | Comments |
|---|---|---|---|
| **Photolithography to define via on 100% SU-8** | | | |
| Spin coat SU-8 6000.5 | Spin-coater | 1. 500 RPM, 5 s, 500 RPM/s<br>2. 6000 RPM, 36 s, 1000 RPM/s<br>3. 0 RPM, 6 s, 1000 RPM/s | SU-8 thickness 433 nm |
| Soft bake | Hot plate | 100°C, 60 s | Hotplate surface temperature |
| Photolithography | Contact aligner / stepper, photomask | 76 mJ/cm$^2$, 365 nm (i-line) UV (Varies with SU-8 thickness) | Use index matching fluid to improve contact between SU-8 and mask and create hard-contact in the case of contact aligner. |
| Post-exposure bake | Hot plate | 100°C, 120 s | Hotplate surface temperature |
| Develop in SU-8 developer | Wet bench | 30 s | Vigorous swish. Wash developer in IPA, blow dry IPA in $N_2$ |
| Hard bake | Hot plate | 100°C, 30 mins | Hotplate surface temperature |
| **Etch-back of the SU-8 to Desired Thickness** | | | |
| SU-8 thickness control etch | RIE-ICP tool | RF power 50 W, ICP power 300 W, 50 sccm $O_2$, 10 mT, He backed substrate cooling at 10 torr | Refer Figure 28a for SU-8 etch thickness as a function of time |

Table 1. Process details in process A1, approach 1, for 100% SU-8

| Step | Equipment | Details | Comments |
|---|---|---|---|
| **Photolithography to define via on 60% SU-8** | | | |
| Spin coat 60% SU-8 6000.5 | Spin-coater | 1. 500 RPM, 5 s, 500 RPM/s<br>2. 6000 RPM, 36 s, 1000 RPM/s<br>3. 0 RPM, 6s, 1000 RPM/s | SU-8 thickness 223 nm |
| Soft bake | Hot plate | 100°C, 60 s | Hotplate surface temperature |
| Photolithography | Contact aligner / stepper, photomask | 329 mJ/cm$^2$, 365 nm (i-line) UV (Changes with SU-8 composition/thickness) | Use index matching fluid to improve contact between SU-8 and mask and create hard-contact in the case of contact aligner. |
| Post-exposure bake | Hot plate | 100°C, 120 s | Hotplate surface temperature |
| Develop in SU-8 developer | Wet bench | 30 s | Vigorous swish. Wash developer in IPA, blow dry IPA in $N_2$ |
| Hard bake | Hot plate | 100°C, 30 mins | Hotplate surface temperature |

*Table 2.* Process details in process A1, approach 2, for 60% SU-8.

#### 5.1.1.3 Process A2 for metal point contact first fabrication

In the A2 process [Fig. 27b], the metal point contacts are fabricated first on the semiconductor BCL, followed by an optional selective etch of BCL using the metal point contacts as a mask, fabrication of the SU-8 dielectric spacer, and deposition of the back mirror. This process is preferred if the BCL must be selectively etched or if fabricating a

smaller diameter via or residue-free via through the SU-8 is difficult using process A1. As the metal point contacts are fabricated first in process A2, this process is expected to result in better electrical contact. As the SU-8 is spun coat after metal point contact fabrication, the SU-8 may completely or partially engulf the metal point contacts. So, the SU-8 on top of the metal point contacts must be removed to get electrical contact between the metal point contacts and the back mirror. In process A2, two different approaches, approach 1 and approach 2, are considered for selectively removing the SU-8 on top of the metal point contacts for electrical contact. In approach 1, the SU-8 on top of the metal point contacts is cleared through photolithography. In approach 2, the SU-8 on top of the metal point contacts is cleared by reactive ion etching.

In process A2, a removable photoresist is spun coat on the BCL, patterned, and developed with photolithography to fabricate vias extending through to the BCL. Any photoresist compatible with the via feature size that can be stripped off after electroplating can be used. In this study, Shipley S1818 positive photoresist is used. The spin-coat and photolithography recipes to fabricate vias in S1818 are listed in Table 3. In a positive photoresist, the regions that are exposed to UV are cleared, while the unexposed regions stay during development. So, the clear region in the photomask corresponds to the via region in the S1818 photoresist.

After via development, the metals for electrical contact are electroplated in the vias to fabricate the metal point contacts. Then the photoresist is stripped (the S1818 strip recipe is listed in Table 3). With these metal point contacts as masks, the BCL can be etched everywhere except the metal point contacts using a suitable selective etchant[112]. In this study 2:1:50 $NH_4OH$:$H_2O_2$:$H_2O$ for 5 s was used to etch the p-AlGaAs BCL. The BCL

selective etch can also be done through a suitable reactive ion etch (RIE) recipe[113]. After BCL etch, we spin-coated 100% SU-8 on the surface with metal point contacts. Depending on the spin speed and metal point contact height, the SU-8 may or may not completely cover the metal point contacts. Two different process approaches, namely: approach 1 – reactive ion etching with a photoresist mask; and approach 2 – reactive ion etching without a mask are explored to clear out the SU-8 on top of the metal point contacts for electrical contact to the back mirror/back metal contact, as shown in steps 5-7 of Fig. 27b.

In approach 1, reactive ion etching with a photoresist mask, SU-8 in the field area between point contacts is protected with a photoresist etch mask, and the metal point contact areas are revealed using photolithography. For negative photoresist, it involves the somewhat difficult step of aligning a photomask containing dark discs to the metal point contacts on the sample. This photomask is essentially an inverted design of the photomask used for fabricating vias on the S1818 positive photoresist in step 1. After photomask alignment, UV exposure, and development, the SU-8 on top of the metal point contacts is cleared by reactive ion etching, using the same recipe as in process A1, approach 1 listed in Table 1.

In approach 2, reactive ion etching without a mask, we hard-bake the SU-8 and etch it in RIE-ICP $O_2$ plasma [Fig. 27,28] to reveal the metal point contacts. For approach 2 to work, the SU-8 film after spin coating should be thicker than the metal point contacts. Otherwise, the SU-8 will interfere with the metal point contacts during spin coating and result in a non-planar film, possibly resulting in light scattering thus undesirable absorption in the final device.

In both of the approaches for process A2, the RIE-ICP etch in step 6 [Fig. 28a] can be used to control the SU-8 thickness to engineer the optical interference conditions. Finally, the back mirror is fabricated by metal evaporation or sputtering.

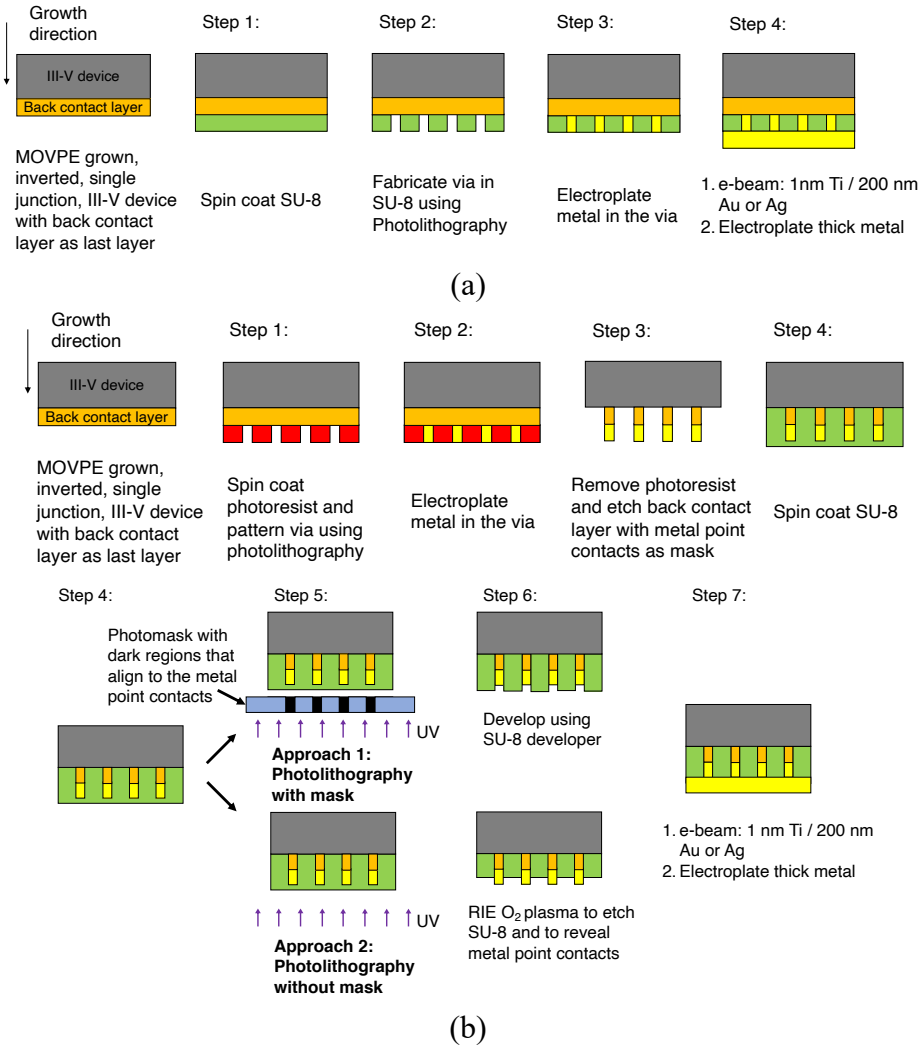
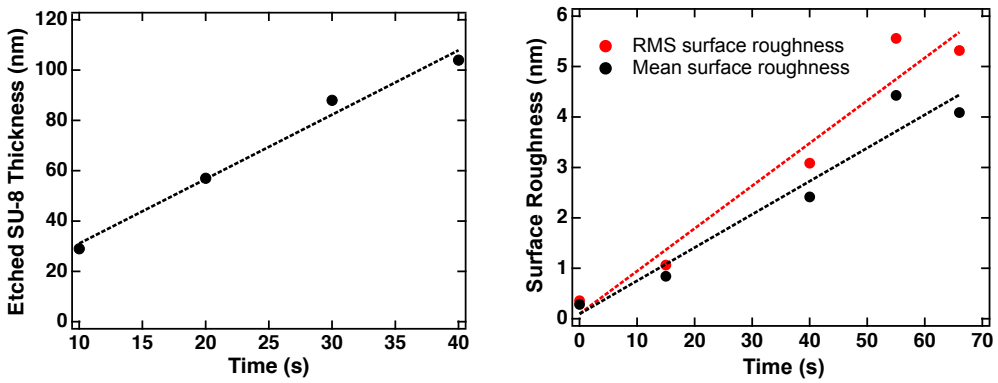



Figure 27. Schematic of PDBC fabrication process flow A, used primarily for SU-8 photoresist as the dielectric layer: (a) process A1 for an intact back contact layer; and (b) process A2 for a structure in which the back contact layer is etched everywhere except at the point contacts.




(a) (b)

Figure 28. (a) Etched SU-8 thickness as a function of RIE-ICP etch time in RF power 50 W, ICP power 300 W, 50 sccm $O_2$ flow, 10 mT chamber pressure in $O_2$ plasma with He backed substrate cooling at 10 torr (b) Mean, and RMS surface roughness measured using AFM.

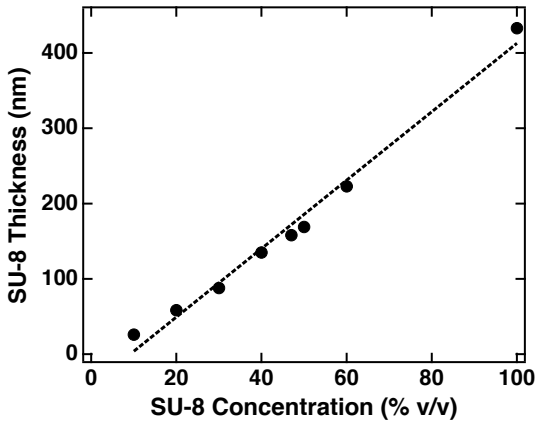



Figure 29. SU-8 thickness as a function of SU-8 concentration diluted in CPG thinner spin coated at 6000 RPM after hardbake at 100°C for 30 mins. Dashed line in the figures indicate linear fit to the data.

### 5.1.2 Process B for evaporable dielectric

Process B is designed for fabricating PDBCs with evaporable dielectrics like $SiO_2$, $MgF_2$, ZnS, etc. Process B is further classified into process B1 and process B2. In process B1 the BCL can be selectively etched, while in process B2 the BCL cannot be selectively etched.

#### 5.1.2.1 Process B1 for any evaporable dielectric

The liftoff process B1 [Fig. 30a] can be used for any evaporable dielectrics. In this process, the BCL can be optionally selectively etched with photoresist pillars as a mask.

An inversion photoresist that is processed negatively, or a negative photoresist, is spin coated on the BCL and is photolithographically processed to reveal an array of photoresist pillars of the required dimensions with an undercut edge profile. The undercut is essential to lift off the dielectric material on top of the photoresist pillars after dielectric deposition.

| Step | Equipment | Details | Comments |
|---|---|---|---|
| **Photolithography to define S1818 photoresist film with vias** | | | |
| Spin coat Shipley S1818 | Spin-coater | 4000 RPM, 30 s, 800 RPM/s | Approximately 1µm thick film |
| Soft bake | Hot plate | 100°C, 5 min | Hotplate surface temperature |
| Photolithography | Contact aligner / stepper, photomask | 75 mJ/cm$^2$, 365 nm (i-line) UV | Use index matching fluid to improve the contact between photoresist and mask and create hard contact in the case of contact aligner. |
| Develop in MF CD-26 developer | Wet bench | 30 s | Wash developer off in D.I. water and blow dry water in $N_2$ |
| **S1818 photoresist wet strip process** | | | |
| Remove S1818 after metal point contact fabrication | Wet bench | Acetone, IPA, $N_2$ blow dry | Acetone removes S1818, IPA removes acetone, $N_2$ evaporates IPA |

Table 3. Process details to fabricate vias in S1818 positive photoresist and to strip S1818 photoresist.

A negative photoresist stays in the region of UV exposure and clears in the region of no UV exposure after development. So, the photoresist pillars with undercut are fabricated at the locations of an array of clear circular areas in the photomask.

In this study, AZ5214-E, an inversion photoresist, is used for defining the photoresist pillars with undercut. The spin coating and photolithography recipes are listed in Table 4. A dielectric layer of the required thickness is deposited using a suitable method (thermal evaporation/ e-beam evaporation/ ALD) of deposition. The dielectric is deposited everywhere on the sample surface, including on top of the photoresist pillars. Following dielectric deposition, the dielectric on top of the photoresist pillars is lifted off using the recipe listed in Table 4. We then fabricate the metal point contacts in the vias, followed by the back mirror fabrication.

#### 5.1.2.2 Process B2 for etchable dielectrics

The etch-through process B2 [Fig. 30b] is suitable only for dielectrics that can be either dry or wet etched, selective to etch the dielectric more rapidly than the photoresist used and the BCL. In this process, the BCL cannot be selectively etched. Process B2 is preferred over process B1 if photoresist dissolution or lift-off of the dielectric in the via areas in process B1 is a problem.

In process B2, the dielectric is deposited on the BCL first. In this study, we deposit ~200 nm $SiO_2$ by e-beam evaporation on the BCL. A photoresist film with vias of the required dimensions is deposited and patterned on the dielectric. In this study, we use Shipley S1818 positive photoresist, and the spin coat and photolithography recipes are listed in Table 3. The dielectric is etched with the photoresist film as an etch mask everywhere except in the via region. In this study, $SiO_2$ is etched with a diluted buffered

oxide etch (BOE - 7:1, HF : $NH_4F$ = 12.5 : 87.5%), using the process as listed in Table 5. The photoresist mask is then stripped off in a suitable dry/wet stripper, leaving the dielectric with its array of patterned vias. In this study, acetone is used to strip the S1818 photoresist as listed in the strip recipe in Table 3. The metal point contacts are electroplated in the vias in the dielectric, and the back mirror is fabricated.

| Step | Equipment | Details | Comments |
|---|---|---|---|
| **Photolithography recipe to define AZ5214-4 photoresist pillars with under cut** | | | |
| Spin coat AZ5214-E | Spin-coater | 2500 RPM, 30 s, 2500 RPM/s | Approximately 1 μm thick photoresist film |
| Soft bake | Hot plate | 95°C, 60 s | Hotplate surface temperature |
| Photolithography | Contact aligner / stepper, photomask | 14.4 mJ/cm$^2$, 365 nm (i-line) UV | Use index matching fluid to improve contact between SU-8 and mask and create hard-contact in the case of contact aligner. |
| Wait time | Wet bench / hood | 5 mins | $N_2$ bubble release |
| Post-exposure bake | Hot plate | 105°C, 60 s | Hotplate surface temperature. |
| Flood-expose | Contact aligner / stepper, no photomask | 860 mJ/cm$^2$, 365 nm (i-line) UV | Image reversal |
| Develop in AZ300 MIF developer | Wet bench | 30 s | Wash developer off in D.I. water and blow dry water in $N_2$ |
| **AZ5214-E photoresist lift-off recipe** | | | |
| Soak in Remover PG stripper | Wet bench | 20 mins on hotplate set at 95ºC | Occasional stirring |
| Ultrasonication in Remover PG stripper | Wet bench | 20 mins | Heated / unheated water bath for ultrasonication |

Table 4. Process to fabricate photoresist pillars using AZ5214-E photoresist and to lift-off AZ5214-E photoresist after dielectric deposition.

| Step | Equipment | Details | Comments |
|---|---|---|---|
| **$SiO_2$ etch with S1818 photoresist as mask** | | | |
| 1:10 Buffered oxide etch (BOE):$H_2O$ etchant | Wet bench | 5 s | Wash 1:10 etchant off in D.I. water and blow dry water in $N_2$ |

*Table 5.* Process details in process B2 for etchable dielectrics.

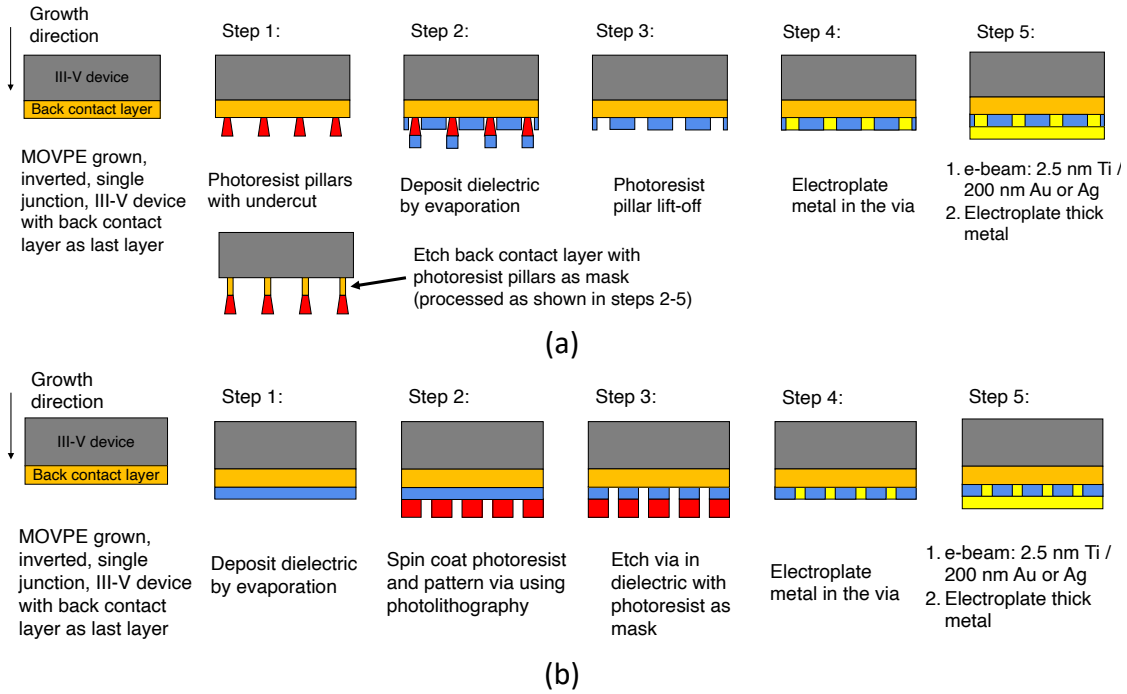



Figure 30. Schematic of PDBC fabrication process flow B primarily for evaporable dielectrics (a) process B1 for any dielectrics (b) process B2 for etchable dielectrics.

### 5.1.3 Point contact and back mirror fabrication

If the stack of metals in the point contact via is different than the metals in the back mirror, electroplating of the contact metal in the vias only is a preferred process, made possible by selective electroplating only on the exposed semiconductor at the bottom of the via, rather than on the insulating dielectric. One key to high reflectance in the vias is a

smooth semiconductor-metal contact interface, which can be achieved with slow electroplating rates of the metal point contacts. In addition, it is desirable to choose a metal for the contact that has high reflectance as well as low specific contact resistivity to the BCL; some metals such as Ti, Cr, and Ni have significantly lower reflectance than other metals. Some of these are metals that give low specific contact resistivity, so a tradeoff can occur between contact reflectivity and contact resistivity, influencing the contact metal selection. The back mirror metal is often either evaporated or sputter coated. If the metal point contact and the back mirror consist of the same metal, evaporating or sputtering the metal would be preferred over electroplating, so that both the metal point contacts and the back mirror are deposited simultaneously

We tried both electroplated Ni/Au and Au metal contacts in the via for electrical conduction. Both Ni/Au and Au point contacts to $3.5 \times 10^{19}$ $cm^{-3}$ Zn-doped p-AlGaAs BCL showed a very low specific contact resistivity of $1 \times 10^{-6}$ $\Omega cm^2$ for 100% CCF, measured with circular TLM pads[91].

For the back mirror fabrication, we initially tried 200 nm e-beam evaporated Au and found that the adhesion between the dielectric and Au was insufficient. In this case, the devices either cracked or detached from the substrate, either during the substrate removal process or the mesa isolation process. Even sputtered Au did not offer satisfactory adhesion to the dielectric. Instead, a layer of 1 nm thick Ti for SU-8 and a layer of 2.5 nm Ti for $SiO_2$ was e-beam evaporated between the dielectric and the mirror metal, which gave satisfactory adhesion. These Ti layers are thin enough and transparent enough to light for the dielectric-metal mirror to be highly reflective. Thus, the blanket metal for the back

mirror consisted in these experiments of a 1 to 2.5 nm Ti adhesion layer, depending on the dielectric used, followed by 200 nm of Au or Ag.

**5.2 Sub-bandgap reflectance as a function of contact coverage fraction**

Fig. 31a shows the reflectance of GaAs TPV device[114] structures with no front grids measured using Fourier transform infrared spectroscopy (FTIR) with SU-8 and $SiO_2$ patterned dielectric back contacts, as well as for a 100% CCF (planar, full metal) Au back contact. The reflectance was measured from 0.6 to 15 μm while Fig. 31a plots the range 0.8 to 2.5 μm to show details more clearly. The contact coverage fraction of the SU-8 PDBC in Fig. 31a was 4.0%, while for the $SiO_2$ PDBC it was 3.6%. The normalized blackbody spectral irradiance is superimposed on this reflectance plot to indicate that most sub-bandgap blackbody power at 2200°C is distributed between 0.9 μm and 2.5 μm.

Fig. 31a shows that the valleys of the reflectance interference fringes for PDBC devices are shallow compared to the device with 100% CCF Au back contact, indicating that absorption observed with a planar Au back contact can be reduced by adding a dielectric spacer. The valleys of reflectance interference fringes for the GaAs $SiO_2$ PDBC device are lower than for the GaAs SU-8 PDBC device, indicating higher absorption across a broad range of wavelengths. The stronger absorption for the 2.5 nm Ti adhesion layer used with the $SiO_2$ PDBC device than for the 1 nm Ti in the SU-8 PDBC device is likely a strong contributor to this effect.

Separate studies of the absorptance of Ti films of varying thickness indicate that the magnitude of absorption in Ti films is consistent with the difference in reflectance between the SU-8 and $SiO_2$ PDBC samples with different Ti adhesion layer thicknesses. We hypothesize that the dominant cause of the reflectance difference between these specific

samples is due to their different Ti layer thicknesses since modeling of these structures using different Ti thicknesses and the optical constants of SU-8 and $SiO_2$ shown in Fig. 16b indicates this to be the case, but this hypothesis is as yet unproven.

Fig. 31b shows that the ideal 0% CCF GaAs SU-8 PDBC gives the highest experimental $R_{sub\text{-}BG}$ of 96.7%. This is a 1.4% absolute improvement compared to the 95.3% measured $R_{sub\text{-}BG}$ of the baseline case of 100% CCF Au, and a 2.4% absolute improvement over 94.3% $R_{sub\text{-}BG}$ for the same 1 nm Ti / Ag metal stack without SU-8 that was used in the 0% CCF case. The highest $R_{sub\text{-}BG}$ measured for the SU-8 patterned back contact is 96.5% at 4.9% CCF, 1.2% higher than the baseline 100% CCF Au, despite the presence of 1 nm Ti in for the PDBC that was not present in the full coverage 100% CCF case.

The highest $R_{sub\text{-}BG}$ measured for the GaAs $SiO_2$ PDBC is 94.7% at 11% CCF which is 0.5% lower than 100% CCF. As discussed above, the thicker 2.5 nm Ti layer is a likely cause of these lower values for these $SiO_2$ PDBCs.

The measured $R_{sub\text{-}BG}$ is higher than the calculated $R_{sub\text{-}BG}$ from ID TMM modeling for both 0% and 100% CCF SU-8 PDBC. For 100% CCF, this deviation between measured and calculated $R_{sub\text{-}BG}$ is within the measurement error of 0.5%, but the deviation at 0% CCF is significant. This deviation is possible if the optical constants or device thickness used in the calculation do not match the actual device parameters because of non-uniform growth. We note that measured and calculated $R_{sub\text{-}BG}$ values agree very well for the 100% CCF 1 nm Ti / Ag device structure indicating good agreement between experimental and modeled device layer thickness and doping in this case.

For both SU-8 and $SiO_2$ PDBC structures, linear fits to experimental $R_{sub\text{-}BG}$ vs. CCF data show a rapid decrease in reflectance with rising CCF, deviating significantly from the calculated 1D TMM model. The linear fits to experimental data in the 4-30% CCF range indicate that at higher CCF, $R_{sub\text{-}BG}$ is projected to be lower than even the 100% CCF case, for both SU-8 and $SiO_2$ PDBCs. The linear fits to $R_{sub\text{-}BG}$ vs. CCF will be linear but with much higher slopes for a wide range of CCF for a given point contact diameter compared to a 1D model calculated linear interpolation between 0% and 100% CCF. At higher CCF, where the pitch is much lesser than the incident wavelength, the incident waves almost does not interact with the point contact array and the sub-bandgap reflectance can be approximated as a linear interpolation between 0% and 100% CCF. At smaller CCF, where the effects of 2D diffraction grating is dominant, the slope of these linear fits will increase with decrease in point contact diameter as the pitch decreases much faster at higher CCF, leading to higher absorption. This indicates that the PDBC is significantly deviating from the approximations made in the 1D linear interpolation approximation.

For via spacing less than ~10 μm, light diffraction in the range of interest for sub-bandgap reflection from the array of metal-filled vias in the dielectric can be significant, scattering light at wider angles than the incoming angular distribution, and thus increasing sub-bandgap absorption in the device[103]. For a constant via diameter, this effect becomes stronger for increasing contact coverage fraction, as the via spacing decreases with rising CCF. So, at higher contact coverage fractions, and particularly for small via diameter and spacing, reflectance from the PDBC structure should be modeled using 3D optical algorithms, such as rigorous coupled-wave analysis (RCWA)[115] and finite-difference time-domain (FDTD)[116] models, rather than simple 1D approximations.

Fig. 31c plots the experimental $R_{sub\text{-}BG}$ values measured by FTIR for GaAs TPV devices with SU-8 patterned dielectric back contacts, with and without a front grid on the devices. The measured $R_{sub\text{-}BG}$ is significantly lower for PDBC devices that have a ~10-μm-thick Au front grid compared to no front grid. This was not expected from first principles, since the gold front grids should in principle also be highly reflective. We note that the trends in $R_{sub\text{-}BG}$ as a function of CCF are similar in PDBC devices both with and without front grids. Among samples with a front grid, the highest measured $R_{sub\text{-}BG}$ is 94.9% at a 4.0% CCF for GaAs TPV devices with a SU-8 PDBC, which is only 0.5% higher than for a 100% CCF Au back contact device, also with a front grid. The present data in Fig. 31c and its experimental variation is consistent with an explanation based on front-grid light scattering, due for instance, to rougher side walls, inverted trapezoidal finger profile, and resulting light trapping due to thick front grids. The present data cannot confirm if there is an interaction between scattering induced by front grids and the patterned dielectric back contact, or if their effects are simply additive, though that is an area for future investigation.

Fig. 31d plots the experimental diffuse reflectance component weighted to 2200°C blackbody spectra, measured by FTIR for GaAs TPV devices with SU-8 patterned dielectric back contacts, with and without front metal grids on the devices. The diffuse reflectance is significantly lower for samples without front grids than for those with front grids. In particular, for 100% CCF planar Au back contact samples for which there is no patterning of the back contact to add to the diffuse reflectance, the measured diffuse reflectance is within noise limits for the sample with no front grids and is taken as 0% (*i.e.*, the planar back reflector is mostly specular). For the corresponding sample with a planar Au back contact but with front grids, the median diffuse reflectance measured is ~11%.

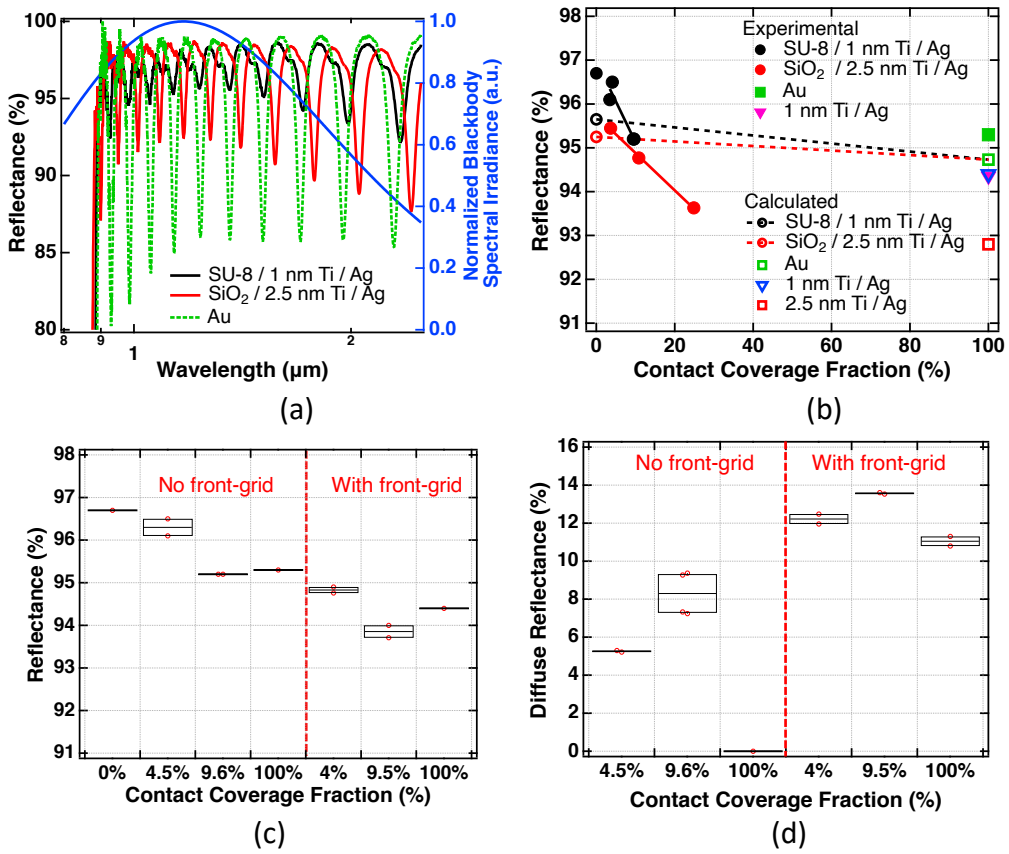



Figure 31. (a) Reflectance of GaAs TPV device with SU-8 and $SiO_2$ PDBC, without front-grid, at similar contact coverage fraction, as a function of wavelength zoomed in from 0.8 to 2.5 μm where the blackbody spectrum at 2200°C has the most power. The right y-axis is normalized blackbody spectral irradiance at 2200°C. (b) FTIR measured and calculated sub-bandgap reflectance weighted to 2200°C blackbody spectrum as a function of contact coverage fraction for different GaAs TPV devices without front grids. Solid line is linear fit to the $R_{sub\text{-}BG}$ data. Dashed line is TMM-calculated weighted reflectance interpolated between 0% CCF and 100% CCF. (c) FTIR measured sub-bandgap reflectance weighted to 2200°C blackbody spectrum as a function of contact coverage fraction (CCF) for GaAs SU-8 PDBC TPV devices with and without front-grids. (d) FTIR measured diffuse component of sub-bandgap reflectance weighted to 2200°C blackbody spectrum as a function of contact coverage fraction (CCF) for GaAs SU-8 PDBC TPV devices with and without front-grids. FTIR $R_{sub\text{-}BG}$ has a measurement error bar of ±0.5% absolute.

This comparison strengthens the argument that the front grids cause a significant increase in diffuse reflectance, separate from that of the back contact. For PDBC devices,

increasing CCF causes an increasing diffuse reflectance component which strengthens the argument that the PDBC should be treated as a three-dimensional diffraction grating.

### 5.3 Series resistance of the GaAs TPV devices

As discussed in chapter 3, the $R_{series}$ contribution to efficiency loss is significant at high operating current densities and it needs to be minimized. In this section, the $R_{series}$ of GaAs TPV devices as a function of CCF in PDBC devices with similar front-grid parameters and as a function of front-grid thickness and spacing in planar back contact devices with similar back contact parameters are investigated. The GaAs TPV device semiconductor epitaxial layers used in both the studies are similar.

In the contact coverage fraction study, the PDBC parameters are as follows. The PDBC is made up of SU-8 dielectric spacer, Ni/Au point contact, 150 nm e-beam evaporated Ag, and 2 μm electroplated Au. The additional 2.2 μm thick electroplated Au is to reduce the backside sheet resistance of the device. The devices differ in the PDBC where the point contact diameter and the CCF are different with a constant point contact pitch of 28.8 μm. The contact resistance of Ni/Au and Au with the p-AlGaAs back contact layer was measured using circular TLM and found to be similar. Also modeling in section 4.1.2 indicates that the resistive loss contribution of the PDBC is dominated by the sheet resistance loss while the contact resistance loss is minimal.

In the contact coverage fraction study, the front-grid parameters are as follows. The front grids are made of electroplated Au with inverted trapezoidal grid fingers with a thickness of ~11 μm, bottom width of ~7.4 μm, and top width of ~15.48 μm, and are spaced 190 μm apart. The grid lines are 8 mm long and current is collected by busbars at both ends, effectively halving the distance current must travel along with the fingers to 4 mm.

The two rectangular busbars are 900 μm wide and 8 mm long. This is a tight grid spacing and a high metal coverage fraction on the front side compared with one-sun solar PV. This corresponds to a calculated $R_{series}$ contribution of about ~3.79 mΩ·cm$^2$ in the front grid metal. In the front-grid thickness and spacing study, the front-grid parameters are similar except the varying front-grid thickness and spacing.

The semiconductor front contact layer in both the study is composed of 100 nm n-GaAs and 200 nm GaInAs and is present only beneath the Au front grid. The contact resistance of Au to the front contact layer and p-AlInP window layer is 7-13×10$^{-6}$ Ω·cm$^2$ and the sheet resistance is 51 Ω/sq as measured using circular TLM pads. The total illuminated/aperture area is 0.64 cm$^2$ and the total dark area is 0.8 cm$^2$. $R_{series}$ was calculated using a generalized optoelectronic model[94] by fitting the dark-IV, external radiative efficiency, and the multiple-suns IV data together.

### 5.3.1 Series resistance as a function of contact coverage fraction

Fig. 32 shows the $R_{series}$ of GaAs PDBC TPV devices as a function of contact coverage fraction. The $R_{series}$ of baseline GaAs TPV device with 100% CCF Au back contact was calculated to be 3.9 mΩ·cm$^2$ indicated by the blue dotted line which is one of the lowest $R_{series}$ measured in this study. The $R_{series}$ of the PDBC devices decreases with increasing CCF which is consistent with the calculations shown in section 4.1.2.

With increasing CCF, the lateral current path length decreases which decrease the effective PDBC sheet resistance leading to lower resistive loss. The maximum measured $R_{series}$ for a GaAs PDBC TPV device was 8.5 mΩ·cm$^2$ for 1% CCF. As $R_{sub\text{-}BG}$ has a stronger impact than $R_{series}$ on TPV efficiency, $R_{series}$ less than 10 mΩ·cm$^2$ should still yield a high TPV efficiency.

As discussed in section 4.3, $R_{sub\text{-}BG}$ improvement of over 1% leads to a predicted TPV efficiency improvement of over 3%. Combining the measured FTIR $R_{sub\text{-}BG}$ and the calculated $R_{series}$, the GaAs TPV device efficiency can be predicted. The maximum measured $R_{sub\text{-}BG}$ of an electrically inactive GaAs TPV test device with no front-grid at 4.9% CCF is 96.5% which may yield a theoretical TPV efficiency of ~36% at 2200°C thermal emitter temperature. Similarly, $R_{sub\text{-}BG}$ of electrically active GaAs TPV device with front-grid at 4% CCF is 94.9% which would be predicted to yield a theoretical TPV efficiency of ~33% at 2200°C thermal emitter temperature. Assuming both the TPV devices with and without front-grid have the same $R_{series}$ of ~8.5 $m\Omega \cdot cm^2$.

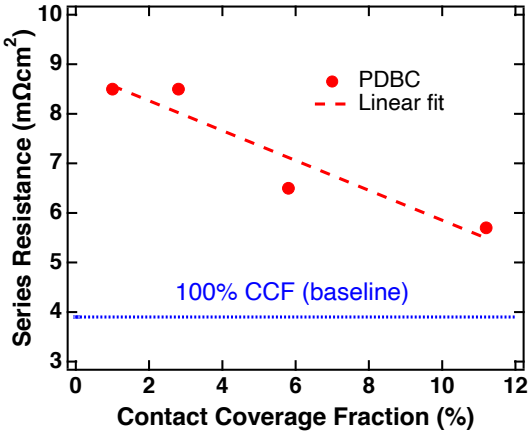



Figure 32. Series resistance of GaAs PDBC TPV devices as a function of contact coverage fraction calculated using optoelectronic model by simultaneously fitting the dark I-V, external radiative efficiency, and multiple-suns IV measurements. The 100% Au planar back contact device series resistance is indicated as dotted blue line.

The recommended optimal parameters for GaAs PDBC TPV devices based on the experimental $R_{sub\text{-}BG}$ and $R_{series}$ are the use of SU-8 over $SiO_2$ dielectric due to the need for a thinner, less absorptive, 1 nm Ti adhesion layer; a CCF in the 1% - 5% range; and a point contact diameter in the 3-10 μm range. This configuration will yield $R_{sub\text{-}BG}$ greater than

96%, provided that lower reflectance with the addition of front metal grids can be addressed, $R_{series}$ less than 10 mΩ·cm$^2$ for front metal grid thickness greater than 10 μm, and in principle, a GaAs TPV efficiency greater than 33%.

### 5.3.2 Series resistance as a function of front-grid thickness

The device front grids may also contribute significantly to the device $R_{series}$ if they are not optimized to handle the current density generated by the TPV radiation. In this study we systematically vary the front-grid thickness and front-grid spacing to study its impact on $R_{series}$ as shown in Fig. 33. The different center-center grid-spacing explored are 190 μm, 140 μm, and 50 μm. Similarly, the different average grid-heights explored are 1.8 μm, 4 μm, 10 μm, and 11 μm. As mentioned earlier, these grid-thicknesses and spacings are much narrower than the corresponding parameters used for one-sun GaAs TPV device.

For 190 μm grid-spacing, the $R_{series}$ decreases as a function of grid thickness. For 1.8 μm and 11 μm grid thickness, the median $R_{series}$ is 17 mΩ·cm$^2$ and 3.9 mΩ·cm$^2$ respectively, which is at least four times decrease in $R_{series}$. Similarly, $R_{series}$ decreases with decrease in grid spacing. Among 190 μm, 140 μm, and 50 μm grid spacing, the 50 μm grid shows the least $R_{series}$. For 2 μm back metal thickness, the calculated back contact resistance contribution is 0.64 mΩ·cm$^2$. For 50 μm grid spacing and 50 Ω/sq emitter sheet resistance, assuming a rectangular grid, the calculated front-grid resistive contribution to $R_{series}$ is 0.8 mΩ·cm$^2$. Therefore, the calculated total $R_{series}$ is 1.44 mΩ·cm$^2$ which is at least 2 times lower than the experimental $R_{series}$. But the experimental devices have an inverted trapezoidal grid whose cross-sectional parameters are not measured. Also, if the probes for current collection on the back contact if placed away from the cell could contribute to

increase resistance contribution. Nevertheless, the median $R_{series}$ of 3 $m\Omega \cdot cm^2$ is one of the lowest values in this study which could positively contribute to TPV efficiency.

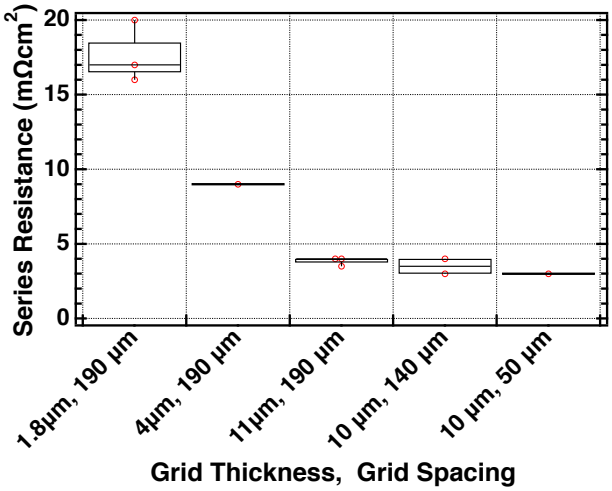



Figure 33. Series resistance of GaAs TPV device with planar back contact as a function of front grid thickness and spacing.

# CHAPTER 6

## ANALYSIS OF GaAs PLANAR AND PDBC TPV DEVICES

In this chapter, we compare the temperature weighted sub-bandgap reflectance, standard photovoltaic electrical performance characteristics, and thermophotovoltaic electrical performance characteristics for GaAs TPV devices with a planar back contact and a PDBC hereafter referred as planar and PDBC devices. The planar and PDBC devices have a different epitaxial architecture as shown in Fig. 34. The planar device selected for this study had the highest weighted sub-bandgap reflectance and the lowest series resistance among all the fabricated planar devices.

The planar device has an electroplated Au back contact with a 100% contact coverage fraction. The PDBC device has a rear mirror structure of ~200 nm SU-8 / 1 nm Ti / 200 nm Ag with Au point contacts. The Au point contacts are 5.6 μm in diameter, spaced 28.8 μm apart, with a contact coverage fraction of 3.42% of the total back contact area. Both the devices have an aperture area of 0.64 $cm^2$ and a mesa area of 0.8 $cm^2$. Both the devices had a 3 μm thick Au back metal contact to aid lateral current transport from the device to the busbar. The measured specific contact resistivity of 67 x $10^{-6}$ $\Omega \cdot cm^2$ for a Au point contact / SU-8 / Ag PDBC as discussed in chapter 4 was used for further calculations in this section.

Both the devices have an inverted trapezoidal, electroplated Au front grid [Fig. 35] with a finger spacing of ~190 μm, with an average measured thickness of 13.2 μm and 11 μm for planar and PDBC respectively as shown in Fig. 34. The fingers are widest near the top and narrow near the bottom [Fig. 35]. The average bottom width was ~7.4 μm and the average top width was calculated based on the grid thickness 13.2 μm and 11 μm to be

19.54 µm and 16.28 µm respectively. Though the PDBC configuration used in this study should result in an improved reflectance over the planar back contact, the front grid scattering resulted in a lower reflectance. However, the front grid is necessary for frontside electrical transport. Therefore, we evaluate both planar and PDBC GaAs TPV devices with front grid.

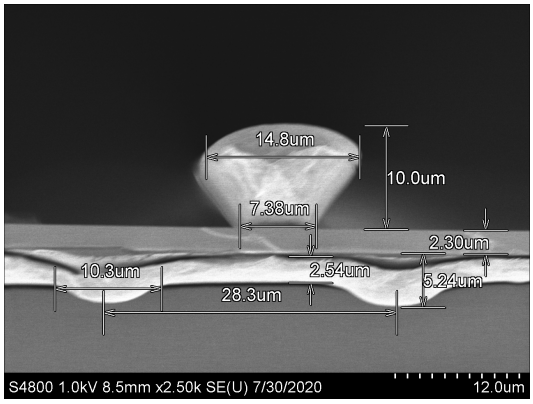



Figure 34. Schematic of cross-sectional SEM image of Au front metal finger on the GaAs PDBC TPV device.

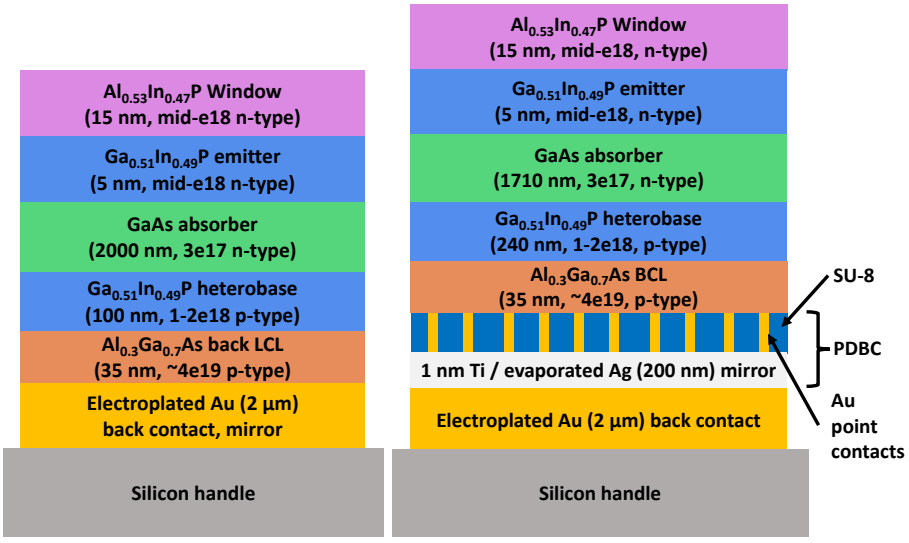



Figure 35. Schematic of GaAs TPV device with (a) planar back contact, (b) PDBC.

### 6.1 Resistance contribution breakdown

The front and back contact resistive contribution of the planar and PDBC device are calculated in this section. The resistance contribution breakdown for the planar and PDBC devices are calculated according to equations discussed in section 4.1.

The fabricated devices have an inverted trapezoidal finger with bottom width of 7.4 μm and a calculated cross-sectional area of 226.6 $\mu m^2$ and 141.7 $\mu m^2$ for planar and PDBC device respectively. For both the planar and PDBC devices, the calculated breakdown resistive contributions from the front and back contacts are shown in Table 6.

For the planar device, the front contact contribution dominates the series resistance. But for the PDBC device, both the front and back contact equally contributes to the series resistance. The busbar contribution was assumed negligible as multiple distributed probes were used for current collection for both the front and back contacts. Therefore, the calculated total series resistance of planar device was 3.3 $m\Omega \cdot cm^2$ which is very close to the experimentally measured total series resistance of 3 $m\Omega \cdot cm^2$. The calculated total series resistance for PDBC device is 7.6 $m\Omega \cdot cm^2$ which is very close to the experimentally measured total series resistance of 7.9 $m\Omega \cdot cm^2$. The small deviations between the calculated and experimental series resistance contributions are probably a result of deviations in the actual device parameters. For instance, the finger cross sectional area is calculated based on the grid height and trapezoidal shape. Similarly, the average specific contact resistance value used for PDBC was measured on BCL / Au point contact / Ag, and not the exact BCL / Au point contact / Ti / Ag which could lead to deviations in the resistive contribution calculations.

| Resistive Contributions | GaAs planar TPV device | GaAs PDBC TPV device |
|---|---|---|
| **Front-grid resistance contribution (mΩ·cm$^2$)** | | |
| Lateral conduction | 1.53 | 1.53 |
| Contact | 0.18 | 0.39 |
| Finger | (13.2 μm) 1.16 | (11 μm) 1.86 |
| Busbar | Negligible | Negligible |
| Front-grid total | **2.88** | **3.79** |
| **Back contact resistance contribution (mΩ·cm$^2$)** | | |
| Bulk conduction | 3.53 x $10^{-3}$ | NA |
| Lateral conduction | NA | 1.15 |
| Contact | 1 x $10^{-3}$ | 1.95 |
| Point contact | NA | Negligible |
| Back metal | 0.43 | 0.43 |
| Back contact total | **0.43** | **3.53** |
| **Total series resistance (mΩ·cm$^2$)** | | |
| Calculated | **3.31** | **7.62** |
| Measured | **3** | **7.9** |

Table 6. Series resistance component breakdown of planar and PDBC GaAs TPV devices.

### 6.2 FTIR reflectance

Fig. 36a shows FTIR measured reflectance as a function of wavelength in a planar and a PDBC GaAs TPV device. In the 0.9 – 2 μm wavelength range, the valleys due to absorption are significantly reduced in the PDBC device compared to the planar device. The lower absorption is due to the SU-8 spacer layer that reduces absorption in the Ti/Ag rear mirror[53,117]. In this wavelength region, the double peaks are due to the superposition of reflectance from the SU-8 spacer layer and the Au point contacts. But for wavelengths greater than 2 μm, the valleys due to absorption are much stronger in the PDBC than the planar device. The stronger absorption is a contribution of the interaction of the incident

waves with the metal point contacts and the interaction becomes stronger as the wavelength increases[103].

Fig. 36b shows sub-bandgap reflectance ($R_{sub-BG}$) of the TPV devices weighted to the blackbody spectrum at different temperatures. The $R_{sub-BG}$ of the PDBC device increases with temperature and that of the planar device decreases with temperature in the 1600 – 2200°C range. The intensity of the blackbody irradiance spectrum shifts towards lower wavelengths or higher energy photons with an increase in temperature as shown in Fig. 36a. At lower blackbody temperatures like 1600°C, there are more photons in the 1.5 – 10 µm wavelength range compared to higher blackbody temperatures like 2200°C. So, stronger absorption valleys in the 3 – 10 µm wavelength range in PDBC results in lower $R_{sub-BG}$ at lower temperatures. But, as the blackbody temperature increases, the lower absorption in PDBC results in a higher $R_{sub-BG}$ compared to the planar back contact device. Therefore, the GaAs PDBC TPV device may yield a higher $R_{sub-BG}$ thus a higher TPV

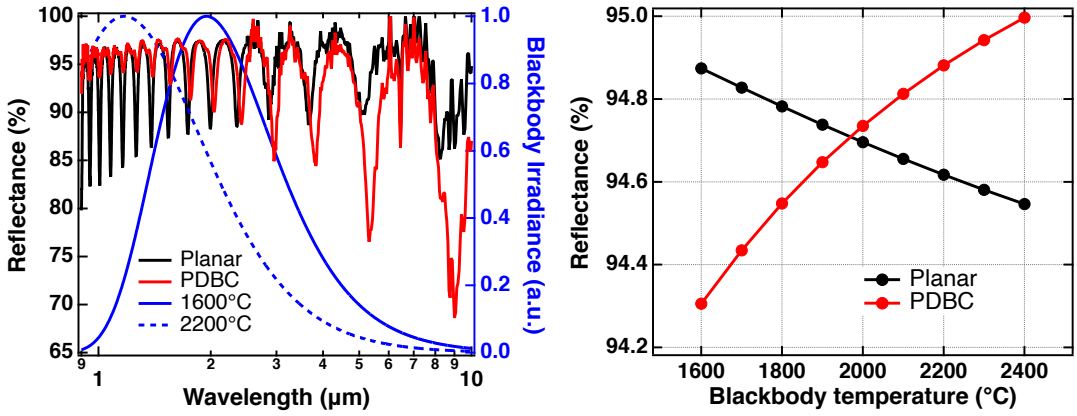



Figure 36. (a) FTIR measured reflectance as a function of wavelength from 0.9 µm to 10 µm wavelength for a GaAs TPV device with a planar back contact and a PDBC. Normalized blackbody irradiance is on the right axis. (b) Weighted sub-bandgap reflectance as a function of blackbody temperature for both planar and PDBC GaAs TPV devices.

efficiency only for thermal emitter temperatures greater than 2000°C. Therefore, at lower emitter temperatures, the planar device may be more efficient than the PDBC device.

### 6.3 Photovoltaic electrical performance

Standard photovoltaic electrical characterization like quantum efficiency, I-V at one- and multiple-suns, dark I-V, and external radiative efficiency (ERE) were measured on both the planar and the PDBC GaAs TPV devices. The multiple-suns I-V, dark I-V, and external radiative efficiency (ERE) are fit using generalized optoelectronic model[94] from which the important device parameters like series resistance, dark saturation current density, and ideality factors [Table 7] for a two-diode model is obtained. $J_{knee}$ is the current density at which the contributions from non-radiative and radiative recombination are equal.

| | **Planar** | **PDBC** |
|---|---|---|
| **$J_{01}$** | 6.45 x $10^{-21}$ A/cm$^2$ | 5.75 x $10^{-21}$ A/cm$^2$ |
| **$J_{0\text{-}NR}$** | 5.35 x $10^{-12}$ A/cm$^2$ | 3.66 x $10^{-11}$ A/cm$^2$ |
| **Ideality factor, $m_{NR}$** | 2 | 2.1 |
| **$J_{knee}$** | 8.9 x $10^{-3}$ A/cm$^2$ | 6 x $10^{-2}$ A/cm$^2$ |

Table 7. Calculated radiative and non-radiative (NR) dark saturation current density, non-radiative ideality factor, and $J_{knee}$.

The external quantum efficiency (EQE) of the planar and PDBC devices with no anti reflection coating are shown in Fig. 37. The EQE measurements were done on different days in the same system but were not calibrated together. EQE was measured in wavelengths between 375 and 1000 nm for every 5 nm interval. The interference fringes near the GaAs band edge of 874 nm occurs from the Fabry Perot resonance due to really good back reflectors in both planar and PDBC devices. The planar device may have a lower

EQE due to increased shading from the thicker and broader front grids as discussed in the beginning of this chapter. For the mid-range wavelengths, the average EQE values are around 0.62 as the devices did not have an anti-reflection coating. The slight shift in the interference fringes may occur from the differences in the device architectures. The improved blue response in both the planar and PDBC device was due to the n-GaInP

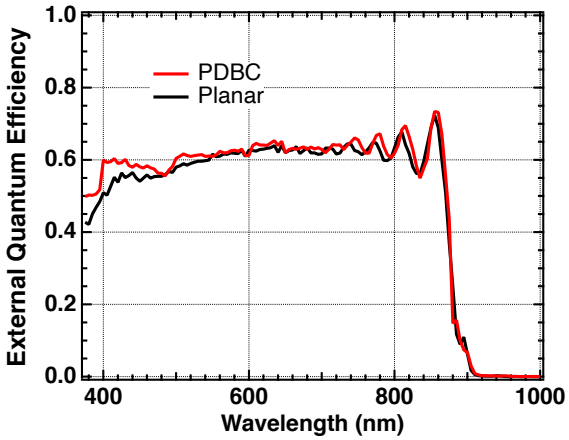



Figure 37. External quantum efficiency (EQE) as a function of wavelength.

window layer in front of the n-GaAs absorber layer compared to a GaAs TPV device with no passivated window layer.

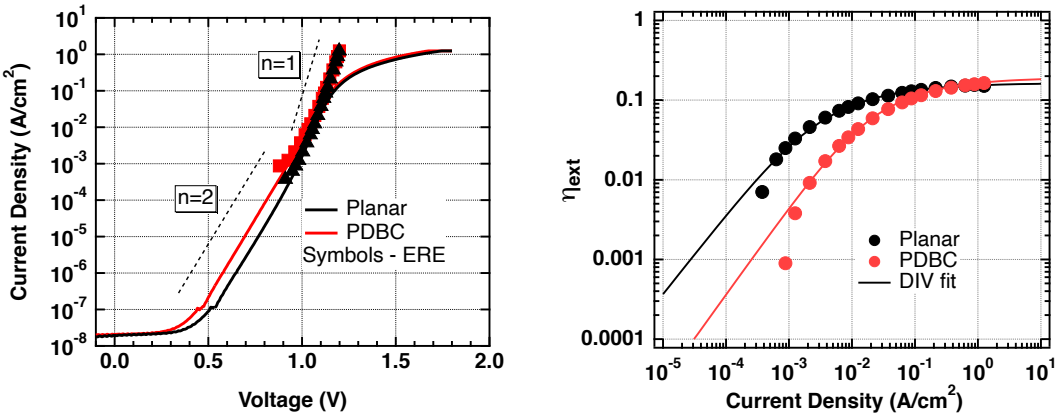
The experimentally measured dark I-V is shown in Fig. 38a. The ERE data is also superimposed on the dark I-V data as a part of the generalized optoelectronic model fit. The dashed lines indicate the slopes corresponding to ideality factors 1 and 2 in the general two-diode model[17]. At low voltages, both the planar and PDBC device show an ideality factor 2 characteristics, i.e. I-V dominated by non-radiative recombination. For increasing voltage, the slope of dark I-V for PDBC device shows a minor deviation from I-V defined by ideality factor 2 near 0.9-1 V, indicating the knee region where the contribution from radiative and non-radiative recombination are equal. The dark I-V rolls over at high voltages as the series resistance contribution dominates.

The experimentally measured ERE as a function of injection current density is shown in Fig. 38b. The calculated dark-IV from the ERE at an I-V region, using Eq. 33,34 is fit to the ERE and is represented by a solid line[94,93]. At current densities higher than 0.5 A/cm$^2$ which corresponds to typical low blackbody temperature (1600°C) GaAs TPV short circuit current densities, both the planar and PDBC devices show similar ERE of greater than 10%. At high current densities, the bulk recombination represented by ideality factor 1 dominates thus the ERE saturates at a constant value. At current densities lower than 0.1 A/cm$^2$, the ERE of the planar device is higher than the PDBC device.

Table 7 shows that the non-radiative dark saturation current density ($J_{0\text{-}NR}$) is lower for the planar device than the PDBC device. At low current densities, the non-radiative recombination dominates therefore a lower $J_{0\text{-}NR}$ in planar device results in a higher ERE. The higher $J_{0\text{-}NR}$ is possible if the perimeter recombination in PDBC device is higher than the planar device which may be a result of any unintentional deviation in the mesa isolation etch process or from the PDBC. As the $J_{0\text{-}NR}$ is higher in the PDBC device, the effects of back reflectance improvement on $V_{oc}$ from the presence of a dielectric spacer (SU-8) between the BCL and metal back contact may be negligible at lower current densities. In addition, the SU-8 thickness in PDBC device is not optimized for maximizing the Fabry-Perot resonance at band edge emission, therefore $V_{oc}$ improvement over the planar device is negligible.

$$V_{oc} = V_{db} + \frac{KT}{q} \ln\left(ERE(J_{sc})\right) \tag{33}$$

$$ERE\left(J_{inj}\right) \approx \frac{J_0^{rad}}{J_{inj}} \exp\left(\frac{qV}{kT}\right) \tag{34}$$




(a) (b)

Figure 38. (a) Measured dark I-V with its corresponding external radiative efficiency superimposed. Dashed lines indicate the slopes for ideality factor n. (b) External radiative efficiency as a function of injection dark current density of planar and PDBC GaAs TPV cells. The DIV fit is the calculated dark I-V from the injection current and external radiative efficiency using Eq. 33,34.

The experimentally measured multiple-suns I-V curves for GaAs TPV device with a planar back contact and a PDBC are shown in Fig. 39. The multiple-suns I-V measurement shows that the planar device has a lower short circuit current density ($J_{sc}$) than the PDBC device. Though both the devices have the same epi architecture, slight differences in the grid shadowing could result in different $J_{sc}$. As the cross-sectional finger profile resembles an inverted trapezoid, a thicker front-grid may mean wider finger width which may lead to increased shadowing which may, in turn, result in a lower $J_{sc}$. Nevertheless, the multiple-suns IV curves show no signs of device breakdown even at 4-5 times the typical 2200°C blackbody GaAs TPV operating current density of 3.5 A/cm$^2$.

The multiple-suns IV summary ($V_{oc}$, fill-factor, and efficiency) for GaAs TPV device with a planar back contact and a PDBC is shown in Fig. 40a. The $V_{oc}$, fill-factor, and efficiency data are fit with a standard optoelectronic model shown by a solid line[94].

The $V_{oc}$ for both planar and PDBC devices at high intensities are similar, consistent with the similar ERE. The typical GaAs TPV short circuit current density at 2200°C black-body spectrum is ~3.5 A/cm$^2$. But the multiple-suns I-V measurement is carried out up to intensities of ~20 A/cm$^2$ to ensure that both the planar and the PDBC devices are electrically stable well beyond the typical TPV operating range. The IV data was not measured for the current ranges between 0.02 and 8 A/cm$^2$ due to tool limitations. However, the  The experimental $V_{oc}$ is deviating from the modeled $V_{oc}$ at high current densities. During multiple-suns I-V measurement, the sample was not placed on a temperature-controlled stage therefore with increase in injection current density, the cell temperature may increase which may lead to the deviation in the measured $V_{oc}$ from the modeled $V_{oc}$[118]. Currently, the cell temperature during multiple suns IV is not measured. Both the planar and the PDBC devices at similar $V_{oc}$ at similar high injection current density indicates similar device heating thus similar rise in device temperature.

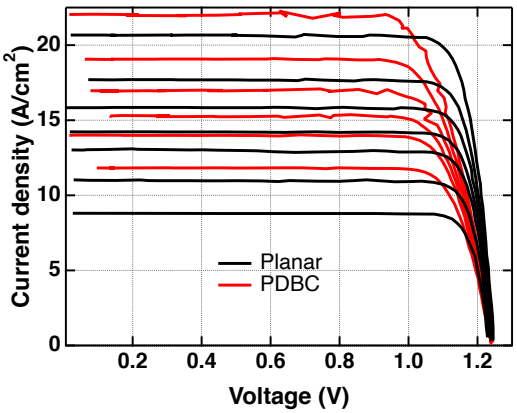



Figure 39. Experimentally measured multiple suns I-V of planar and PDBC GaAs TPV devices.

The fill-factor (FF) of the planar device is higher compared to the PDBC device at any given incident light intensity. The FF roll-over at higher incident intensities is a strong function of the series resistance of the device. Given that the epi stack and the front grids

are comparable in both the planar and the PDBC devices, the FF roll-over is primarily dictated by the back contact of the devices. In the planar device, the electrical back contact coverage fraction is 100%, i.e., the electrical back contact spans the entire semiconductor back contact layer (p-AlGaAs in this study). However, in a PDBC device, the electrical back contact coverage fraction is just 3.42% of the semiconductor back contact layer in the form of hexagonally distributed Au point contacts. So, the current in the back contact must flow laterally in the semiconductor back contact layer before reaching the Au point contacts[100]. This causes increased lateral conduction resistance thus increasing the overall series resistance. The solar conversion efficiency is irrelevant for the TPV application, but it can just be used as a metric to gauge the device efficiencies as a benchmark for comparison.

### 6.4 Thermophotovoltaic electrical performance

The measured TPV efficiency and other related electrical parameters for GaAs TPV device with a planar back contact and a PDBC is shown in Fig. 40b. The measured GaAs TPV efficiency is higher for the planar device than the PDBC device in the 1600 – 2100°C thermal emitter temperature range. Increasing the thermal emitter temperature beyond 2100°C was challenging due to thermal emitter sublimation leading to carbon deposition on the diamond window. In a real grid-scale energy storage system, sublimation and subsequent carbon deposition can be reduced by setting the thermal chamber pressure greater than 1 atm in an inert gas environment or by using a gas curtain on the TPV module. However, the TPV test platform was neither equipped for high pressure testing or with a gas curtain on the window layer. At 2100°C thermal emitter temperature, the measured TPV efficiency is 23.4% and 22.8% for the planar and the PDBC device. The linear fit to

TPV efficiency in the 1600 – 2100℃ is calculated and is interpolated to 2300℃. At 2200℃ thermal emitter temperature, the predicted TPV efficiency is 26.2% and 25.9% for the planar and the PDBC device. The maximum predicted TPV efficiency at 2300℃ for both devices is ~29%. The TPV efficiency and related parameters were also measured during thermal emitter temperature ramp down and there was no significant hysteresis effect was seen, suggesting that the devices did not suffer from any thermal or optical shock. The TPV efficiency is calculated according to the equation [Eq. 28]. Where the denominator electrical power output + heat loss equals the total absorbed power in the TPV device.

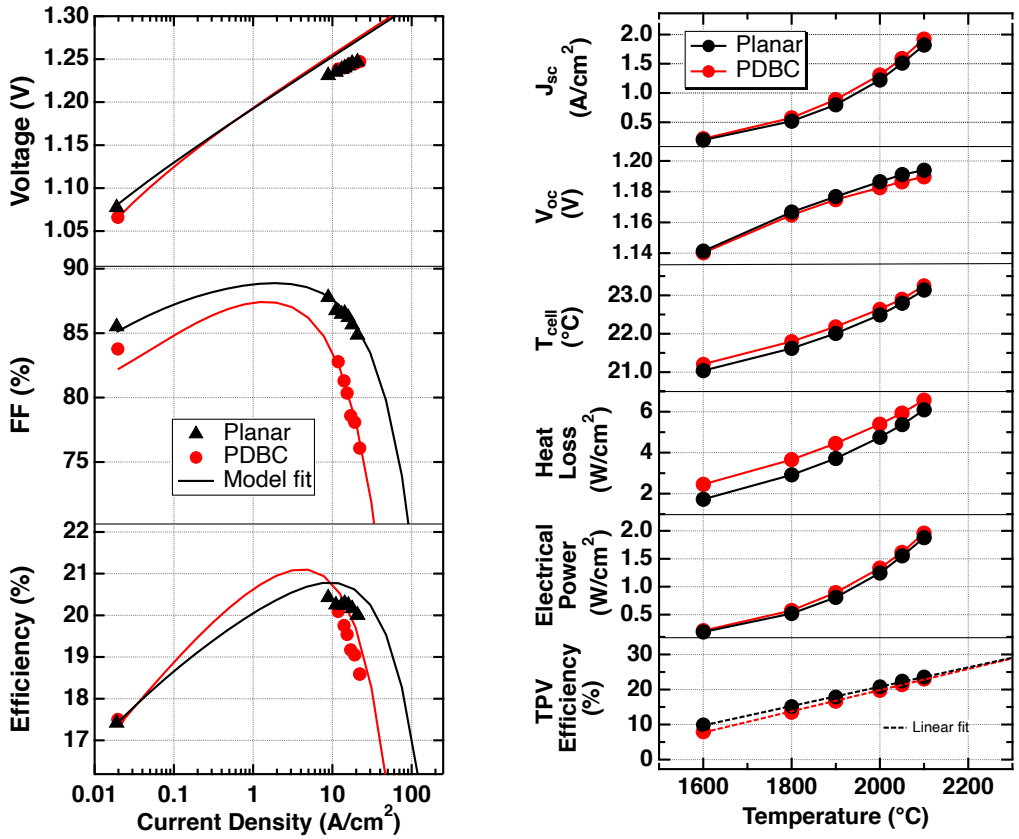
$$\eta_{TPV} = \frac{Electrical\ power\ output}{Electrical\ power\ output + Heat\ loss} \tag{35}$$

The electrical power output from both the planar and PDBC devices were similar in the 1600 – 2100℃ thermal emitter temperature range. However, the heat loss in the PDBC device is a little higher than the planar device in the entire measured emitter temperature range. The difference in heat loss between the devices is also decreasing with the increasing emitter temperature. Similarly, the temperature of the PDBC device is also a little higher than the planar device with the difference in temperature between the cells slightly decreasing with an increase in temperature. The $V_{oc}$ of both the planar and PDBC devices are almost similar in the 1600 – 1900℃ range. However, for emitter temperatures greater than 1900℃ the $V_{oc}$ of the PDBC rolls over and starts to decrease compared to the planar device. The multiple-suns IV measurement did not indicate a similar trend in $V_{oc}$ even at 10 times higher current densities.

The total measured heat loss is a sum of heat loss from device series resistance and parasitic photon absorption. At a given thermal emitter temperature and a corresponding maximum power point current density, the resistive loss is calculated as $I_{mp}^2 \cdot R_{series}$. Subtracting the resistive loss from the total heat loss, the heat loss from the parasitic photon absorption can be determined. For the GaAs PDBC device, at thermal emitter temperatures of 1600℃ and 2100℃, the heat loss contribution from the parasitic absorption is calculated as ~99.9% and 99.6% of the total heat loss (Q) respectively. This shows that the heat loss is almost entirely dominated by parasitic absorption, strengthening the significance of improving the device reflectance. The remaining heat loss is from the resistive loss contribution due to device series resistance and is almost negligible due to the low device series resistance. At a similar heat loss, the calculated resistive contribution would have been ~5.5% of total heat loss at 2100℃ thermal emitter temperature, if the device series resistance were to be 100 $m\Omega \cdot cm^2$ instead of 7.9 $m\Omega \cdot cm^2$.

The lower TPV efficiency is probably due to lower device reflectance in the TPV test platform. At 2200℃, the measured weighted sub-bandgap reflectance of PDBC device is ~94.9% at 12° angle of incidence, which should have yielded a TPV efficiency of >30% [Fig. 25]. But the projected TPV efficiency from the measured TPV efficiency for PDBC device at 2200℃ being ~26% indicates that the weighted sub-bandgap reflectance is only ~93% in the TPV test platform. This could probably be dominated by parasitic absorption due to front-grid[119] scattering as we see similar effects from the planar TPV device which had no diffraction grating to scatter light like a PDBC. Therefore, it could be possible that the sub-bandgap reflectance measurement at a single angle of incidence like 12° is insufficient to capture all the scattering effects and resulting absorption from the TPV

device and reflectance measurement should be done for a range of angle of incidence from 0-90°.




(a) (b)

Figure 40. Experimentally measured summary of (a) multiple-suns I-V at different injection intensity, and (b) TPV efficiency and other related electrical parameters at different thermal emitter temperature.

# CHAPTER 7

# SUMMARY AND FUTURE WORK

## 7.1 Summary

In this work, we have modeled, designed, and fabricated GaAs patterned dielectric back contact (PDBC) thermophotovoltaic (TPV) devices, for high-temperature energy storage, with and without front grids, and measured the long-wavelength reflectance. We have shown that for high TPV conversion efficiency it is essential to maximize the sub-bandgap reflectance and minimize the series resistance. It was found that GaAs TPV devices can be fabricated with patterned dielectric back contacts for improved sub-bandgap reflectance without compromising the electrical back contact.

From rigorous coupled wave analysis (RCWA) modeling and corroborating experiments, we showed that the PDBCs behave as a two-dimensional diffraction grating which is piecewise constant in the z- direction, in which the point-contact pitch should be at least 10 μm if it is desired to minimize the interaction of incident waves. Multiple processing methods to fabricate PDBC structures were explored, which vary according to the dielectric spacer material and the need to etch the back contact layer. We then fabricated GaAs PDBC TPV devices with SU-8 and $SiO_2$ dielectric layers, as well as with and without front grids, to quantify light scattering and reflection from PDBC structures and the front grids. We designed experiments to study the effects of contact coverage fraction on the sub-bandgap reflectance and series resistance, and the effect of front grid thickness and spacing on the series resistance.

We measured the total sub-bandgap reflectance using FTIR and found that on GaAs devices, a SU-8/metal back mirror structure with the limiting case of 0% CCF shows the highest $R_{sub\text{-}BG}$ of (96.7 ± 0.5)%, while PDBC structures with 4.9% CCF still have a very high measured $R_{sub\text{-}BG}$ of (96.5 ± 0.5)% with no front grid. Both values are a >1% absolute improvement over the baseline $R_{sub\text{-}BG}$ of (95.3 ± 0.5)% for GaAs TPV devices with 100% CCF Au back contact, with no front grid. We also show the measured $R_{sub\text{-}BG}$ for GaAs $SiO_2$ PDBC structures to be lower than the baseline 100% CCF, likely due to the thicker Ti adhesion layer used on $SiO_2$. The slopes of linear fits to experimentally measured $R_{sub\text{-}BG}$ for GaAs PDBC TPV devices with respect to CCF are very high compared to the 1D TMM linear interpolation model, indicating that the array of metal-filled vias in the PDBC exhibits substantial diffraction as well as specular reflection; it thus cannot be approximated by a simple 1D linear interpolation model and should be treated as a diffraction grating.

We also show that measured $R_{sub\text{-}BG}$ for GaAs SU-8 PDBC devices with a metal front grid is lower than for test devices without a front grid, likely due to light scattering from the front grid. We experimentally derived $R_{series}$ of the GaAs TPV devices as a function of CCF and the maximum measured $R_{series}$ was ~8.5 $m\Omega \cdot cm^2$ at 1% CCF. Combining the FTIR measured $R_{sub\text{-}BG}$ of 94.9% and experimentally derived $R_{series}$ of ~8.5 $m\Omega \cdot cm^2$, the predicted TPV efficiency for GaAs PDBC device with 4% CCF and with the front grid is ~33% at 2200°C.

Finally, we compare the best of the GaAs planar and PDBC TPV devices and discuss the FTIR reflection measurement, standard photovoltaic electro-optical characterization, and TPV efficiency measurement in a TPV test platform, in which the TPV efficiency is

based on measured heat fluxes for more accurate results. The measured TPV efficiency of the devices were lower than the modeled values, in part due to scattering from the front grids.

### 7.2 Contributions to knowledge

A higher bandgap 1.4-eV GaAs TPV device for high thermal emitter temperature >1800 ℃ was investigated. Historically, TPV research has focused on low temperature thermal emitters and correspondingly low semiconductor bandgap TPV devices. Prior to this research work, GaAs TPV device work is almost non-existent in the literature.

A patterned dielectric back contact to the GaAs TPV device with SU-8 photoresist as the dielectric spacer was investigated and developed. SU-8 has been used as a dielectric spacer layer in certain optoelectronic devices for various functions and applications, but there have been almost no studies looking at its long-wavelength (0.9 – 10 μm) reflectance properties that are relevant for TPV applications.

Looking at point contact array PDBCs in the context of the long wavelength (0.9 – 10 um) reflection properties which are important for TPV applications and modeling their diffractive effects using rigorous coupled wave analysis and resulting increased, undesired parasitic sub-bandgap absorption, is a novel contribution to TPV research.

Series resistance implications of the point contact array PDBC were also investigated. Though there have been many studies looking at the resistive contributions of point contact arrays, systematically studying the resistive implications as a function of point contact diameter, pitch, and contact coverage fraction along with the measured reflectance properties is a contribution to knowledge in TPV research.

A variety of PDBC fabrication methods were investigated and developed, their advantages and disadvantages were identified, and solutions to fabrication barriers were researched and found experimentally, allowing the point contact rear reflector architecture to work. Multiple fabrication processes, such as: patterning first, then depositing an evaporable dielectric ($SiO_2$); depositing dielectric first, then patterning (SU-8, $SiO_2$); and selective removal of the light-absorbing lateral conduction layer on back of the semiconductor, were developed and implemented. The intricate processing details that were developed and documented here could in general be applicable to any III-V optoelectronics device in which the combination of high back reflectance and low resistance is beneficial.

**7.3 Future work**

The reason for lower reflectance from the front-grid scattering and the interaction of PDBC optics with the front grid is key to improving the TPV efficiency and should be investigated. We experimentally identified that the front grid scattering effects play a dominant role in determining the TPV efficiency, but the root cause of the scattering is still unidentified. Thus, a systematic study to quantify the scattering from front grids with experimentally varied parameters such as shape, spacing, material, semiconductor front contact layer beneath the metal grids, shadowing loss, parasitic light trapping, and others, important for future efficiency improvements.

Studying the FTIR measured sub-bandgap reflectance properties of the TPV device in the entire 0-90° angle of incidence is essential to accurate understand its performance in the TPV environment. Currently the device reflectance measured at a single angle of incidence is insufficient to capture and quantify all the parasitic absorption. Additionally,

the effect of TPV test platform on the device reflectance is also not captured in this study, which could be studied using Monte Carlo methods. The details of photon incidence angle, photon reflection angle, luminescence emission angle, and corresponding parasitic absorption that may result from these photon exchange properties in the TPV test platform environment are not fully available and may play an important role in quantifying the effect of photon scattering on TPV efficiency. Also, it is important to note that the importance of these effects may be affected if the front-grid scattering is negligible.

Studying the effects of open-circuit voltage from parasitic near-bandgap luminescence absorption due to surface plasmon polaritons (SPPs) in the PDBC, and interaction with diffraction grating effects, along with the sub-bandgap reflectance may be relevant for improving the electrical power output. At very high incident light intensities as in the TPV environment, these effects may be small but may also constitute a worthwhile contribution.

Increasing the output electrical power density, as contrasted with the total electrical power, is also a key to improving the TPV efficiency. Output power density can be increased either by lowering the absorber bandgap, by designing and developing a multijunction TPV cell with a lower bandgap absorber as second junction, by adding an anti-reflection coating, or through near-field thermophotovoltaics, thus increasing the above-bandgap incident intensity. Each method listed above has its own challenges, but in combination could blaze a path to >50% TPV efficiency.

# REFERENCES


1. Denholm, P., Jorgenson, J., Hummon, M., Jenkin, T., Palchak, D., Kirby, B., ... & O'Malley, M. (2013). *Value of energy storage for grid applications* (No. NREL/TP-6A20-58465). National Renewable Energy Lab.(NREL), Golden, CO (United States).

2. Sioshansi, R., Denholm, P., Jenkin, T., & Weiss, J. (2009). Estimating the value of electricity storage in PJM: Arbitrage and some welfare effects. *Energy economics*, *31*(2), 269-277.

3. Bradbury, K., Pratson, L., & Patiño-Echeverri, D. (2014). Economic viability of energy storage systems based on price arbitrage potential in real-time US electricity markets. *Applied Energy*, *114*, 512-519.

4. Slocum, A. H., Fennell, G. E., Dundar, G., Hodder, B. G., Meredith, J. D., & Sager, M. A. (2013). Ocean renewable energy storage (ORES) system: Analysis of an undersea energy storage concept. *Proceedings of the IEEE*, *101*(4), 906-924.

5. Schmidt, O., Hawkes, A., Gambhir, A., & Staffell, I. (2017). The future cost of electrical energy storage based on experience rates. Nat Energy 2017; 2: 17110.

6. Blakers, A., Stocks, M., Lu, B., & Cheng, C. (2021). A review of pumped hydro energy storage. *Progress in Energy*.

7. Amy, C., Seyf, H. R., Steiner, M. A., Friedman, D. J., & Henry, A. (2019). Thermal energy grid storage using multi-junction photovoltaics. *Energy & Environmental Science*, *12*(1), 334-343.

8. https://www.cnbc.com/2021/03/24/goldman-electric-cars-face-rising-battery-lithium-nickel-cobalt-costs.html

9. Xu, C., Dai, Q., Gaines, L., Hu, M., Tukker, A., & Steubing, B. (2020). Future material demand for automotive lithium-based batteries. *Communications Materials*, *1*(1), 1-10.

10. Werth, J. J. (1967). *U.S. Patent No. 3,331,707*. Washington, DC: U.S. Patent and Trademark Office.

11. Chubb, D. (2007). *Fundamentals of thermophotovoltaic energy conversion*. Elsevier.

12. Bauer, T. (2011). *Thermophotovoltaics: basic principles and critical aspects of system design*. Springer Science & Business Media.

13. Coutts, T. J. (1999). A review of progress in thermophotovoltaic generation of electricity. *Renewable and sustainable energy reviews*, *3*(2-3), 77-184.

14. Burger, T., Sempere, C., Roy-Layinde, B., & Lenert, A. (2020). Present efficiencies and future opportunities in thermophotovoltaics. *Joule*.

15. https://www.entegris.com/content/dam/web/resources/brochures/brochure-properties-and-characteristics-of-graphite-7329.pdf

16. Woodside, W. M. J. H., & Messmer, J. H. (1961). Thermal conductivity of porous media. I. Unconsolidated sands. *Journal of applied physics*, *32*(9), 1688-1699.

17. Shockley, W., & Queisser, H. J. (1961). Detailed balance limit of efficiency of p-n junction solar cells. *Journal of applied physics*, *32*(3), 510-519.

18. Dupré, O. (2015). *Physics of the thermal behavior of photovoltaic devices* (Doctoral dissertation, Lyon, INSA).

19. Lenert, A., Bierman, D. M., Nam, Y., Chan, W. R., Celanović, I., Soljačić, M., & Wang, E. N. (2014). A nanophotonic solar thermophotovoltaic device. *Nature nanotechnology*, *9*(2), 126-130.

20. Harder, N. P., & Würfel, P. (2003). Theoretical limits of thermophotovoltaic solar energy conversion. *Semiconductor science and technology*, *18*(5), S151.

21. Ungaro, C., Gray, S. K., & Gupta, M. C. (2015). Solar thermophotovoltaic system using nanostructures. *Optics express*, *23*(19), A1149-A1156.

22. Rephaeli, E., & Fan, S. (2009). Absorber and emitter for solar thermo-photovoltaic systems to achieve efficiency exceeding the Shockley-Queisser limit. *Optics express*, *17*(17), 15145-15159.

23. Zhou, Z., Sakr, E., Sun, Y., & Bermel, P. (2016). Solar thermophotovoltaics: reshaping the solar spectrum. *Nanophotonics*, *5*(1), 1-21.

24. Wang, Y., Liu, H., & Zhu, J. (2019). Solar thermophotovoltaics: Progress, challenges, and opportunities. *APL Materials*, *7*(8), 080906.

25. Bierman, D. M., Lenert, A., Chan, W. R., Bhatia, B., Celanović, I., Soljačić, M., & Wang, E. N. (2016). Enhanced photovoltaic energy conversion using thermally based spectral shaping. *Nature Energy*, *1*(6), 1-7.

26. Datas, A., & Algora, C. (2013). Development and experimental evaluation of a complete solar thermophotovoltaic system. *Progress in Photovoltaics: Research and Applications*, *21*(5), 1025-1039.

27. Licht, A., Pfiester, N., DeMeo, D., Chivers, J., & Vandervelde, T. E. (2019). A review of advances in thermophotovoltaics for power generation and waste heat harvesting. *MRS Advances*, *4*(41-42), 2271-2282.

28. Chubb, D. L., Good, B. S., & Lowe, R. A. (1996, February). Solar thermophotovoltaic (STPV) system with thermal energy storage. In *AIP Conference Proceedings* (Vol. 358, No. 1, pp. 181-198). American Institute of Physics.

29. Datas, A., Chubb, D. L., & Veeraragavan, A. (2013). Steady state analysis of a storage integrated solar thermophotovoltaic (SISTPV) system. *Solar energy*, *96*, 33-45.

30. Veeraragavan, A., Montgomery, L., & Datas, A. (2014). Night time performance of a storage integrated solar thermophotovoltaic (SISTPV) system. *Solar energy*, *108*, 377-389.

31. Datas, A., Ramos, A., Martí, A., del Cañizo, C., & Luque, A. (2016). Ultra high temperature latent heat energy storage and thermophotovoltaic energy conversion. *Energy*, *107*, 542-549.

32. DeSutter, J., Bernardi, M. P., & Francoeur, M. (2016). Determination of thermal emission spectra maximizing thermophotovoltaic performance using a genetic algorithm. *Energy Conversion and Management*, *108*, 429-438.

33. Bermel, P., Ghebrebrhan, M., Chan, W., Yeng, Y. X., Araghchini, M., Hamam, R., ... & Johnson, S. G. (2010). Design and global optimization of high-efficiency thermophotovoltaic systems. *Optics express*, *18*(103), A314-A334.

34. Woolf, D. N., Kadlec, E. A., Bethke, D., Grine, A. D., Nogan, J. J., Cederberg, J. G., ... & Hensley, J. M. (2018). High-efficiency thermophotovoltaic energy conversion enabled by a metamaterial selective emitter. *Optica*, *5*(2), 213-218.

35. Pfiester, N. A., & Vandervelde, T. E. (2017). Selective emitters for thermophotovoltaic applications. *Physica status solidi (a)*, *214*(1), 1600410.

36. Höfler, H., Paul, H. J., Ruppel, W., & Würfel, P. (1983). Interference filters for thermophotovoltaic solar energy conversion. *Solar Devices*, *10*(3), 273-286.

37. Swanson, R. M. (1980, December). Recent developments in thermophotovoltaic conversion. In *1980 International Electron Devices Meeting* (pp. 186-189). IEEE.

38. Charache, G. W., DePoy, D. M., Baldasaro, P. F., & Campbell, B. C. (1996, February). Thermophotovoltaic devices utilizing a back surface reflector for spectral

control. In *AIP Conference Proceedings* (Vol. 358, No. 1, pp. 339-350). American Institute of Physics.

39. Omair, Z., Scranton, G., Pazos-Outón, L. M., Xiao, T. P., Steiner, M. A., Ganapati, V., ... & Yablonovitch, E. (2019). Ultraefficient thermophotovoltaic power conversion by band-edge spectral filtering. *Proceedings of the National Academy of Sciences*, *116*(31), 15356-15361.

40. Fan, D., Burger, T., McSherry, S., Lee, B., Lenert, A., & Forrest, S. R. (2020). Near-perfect photon utilization in an air-bridge thermophotovoltaic device. *Nature*, 1-5.

41. Baldasaro, P. F., Raynolds, J. E., Charache, G. W., DePoy, D. M., Ballinger, C. T., Donovan, T., & Borrego, J. M. (2001). Thermodynamic analysis of thermophotovoltaic efficiency and power density tradeoffs. *Journal of Applied Physics*, *89*(6), 3319-3327.

42. Wojtczuk, S., Gagnon, E., Geoffroy, L., & Parodos, T. (1995). InxGa1−xAs thermophotovoltaic cell performance vs bandgap. *AIP Conference Proceedings*, *321*, 177–187.

43. Modest, M. F. (2013). *Radiative heat transfer*. Academic press.

44. Howell, J. R., Menguc, M. P., & Siegel, R. (2010). *Thermal radiation heat transfer*. CRC press.

45. T. Narayan, L. Kuritzky, Dustin P. Nizamian, Benjamin A. Johnson, Eric J. Tervo, Alexandra R. Young, Cecilia Luciano, Madhan K. Arulanandam, B. Kayes, E. Perl, M. Limpinsel, P. Santhanam, J. Slack, W. Olavarria, J. Carapella, M. Young, Cheng-Lun Wu, Zhengshan J. Yu, Z. Holman, R. King, M. Steiner, David M. Bierman, Andrew J. Ponec, Justin A. Briggs. (2020, June). World record demonstration of> 30% thermophotovoltaic conversion efficiency. In *2020 47th IEEE Photovoltaic Specialists Conference (PVSC)* (pp. 1792-1795). IEEE.

46. Datas, A. (2015). Optimum semiconductor bandgaps in single junction and multijunction thermophotovoltaic converters. *Solar Energy Materials and Solar Cells*, *134*, 275-290.

47. R. R. King, D. Bhusari, A. Boca, D. Larrabee, X.-Q. Liu, W. Hong, C. M. Fetzer, D. C. Law, and N. H. Karam, "Band Gap-Voltage Offset and Energy Production in Next-Generation Multijunction Solar Cells," *Prog. Photovolt: Res. Appl.* **19**, 797-812 (2011), doi: 10.1002/pip.1044.

48. Sun, Y., Perna, A., & Bermel, P. (2019). Comparing front-and rear-junction GaInP photovoltaic devices through detailed numerical and analytical modeling. *IEEE Journal of Photovoltaics*, *9*(2), 437-445.

49. Geisz, J. F., Steiner, M. A., Garcia, I., Kurtz, S. R., & Friedman, D. J. (2013). Enhanced external radiative efficiency for 20.8% efficient single-junction GaInP solar cells. *Applied Physics Letters*, *103*(4), 041118

50. Miller, O. D., Yablonovitch, E., & Kurtz, S. R. (2012). Strong internal and external luminescence as solar cells approach the Shockley–Queisser limit. *IEEE Journal of Photovoltaics*, *2*(3), 303-311.

51. Steiner, M. A., Geisz, J. F., Garcia, I., Friedman, D. J., Duda, A., & Kurtz, S. R. (2013). Optical enhancement of the open-circuit voltage in high quality GaAs solar cells. *Journal of Applied Physics*, *113*(12), 123109.

52. Ganapati, V., Steiner, M. A., & Yablonovitch, E. (2016). The voltage boost enabled by luminescence extraction in solar cells. *IEEE Journal of Photovoltaics*, *6*(4), 801-809.

53. Burger, T., Fan, D., Lee, K., Forrest, S. R., & Lenert, A. (2018). Thin-film architectures with high spectral selectivity for thermophotovoltaic cells. *ACS Photonics*, *5*(7), 2748-2754.

54. Swanson, R. M., Beckwith, S. K., Crane, R. A., Eades, W. D., Kwark, Y. H., Sinton, R. A., Swirhun, S. E., "Point-Contact Silicon Solar Devices," *Trans. Electron Dev.* **31**, 661 (1984).

55. Swanson, R. M., "Point-Contact Solar Devices: Modeling and Experiment," *Solar Devices* **17**, 85 (1986).

56. Micha, D. N., Höhn, O., Oliva, E., Klinger, V., Bett, A. W., Dimroth, F., "Development of back side technology for light trapping and photon recycling in GaAs solar devices," *Prog. Photovolt: Res. Appl.*, 1-8 (2018).

57. Helmers, H., Lopez, E., Höhn, O., Lackner, D., Schön, J., Schauerte, M., ... & Bett, A. W. (2021). 68.9% Efficient GaAs-Based Photonic Power Conversion Enabled by Photon Recycling and Optical Resonance. *physica status solidi (RRL)–Rapid Research Letters*, 2100113.

58. Datas, A., & Vaillon, R. (2021). Thermophotovoltaic energy conversion. In *Ultra-High Temperature Thermal Energy Storage, Transfer and Conversion* (pp. 285-308). Woodhead Publishing.

59. Nelson, R. E. (2003). A brief history of thermophotovoltaic development. *Semiconductor Science and Technology*, *18*(5), S141.

60. Wedlock, B. D. (1963). Thermo-photo-voltaic energy conversion. *Proceedings of the IEEE*, *51*(5), 694-698.

61. Swanson, R. M. (1979). A proposed thermophotovoltaic solar energy conversion system. *Proceedings of the IEEE*, *67*(3), 446-447.

62. Fraas, L. M., Avery, J. E., Sundaram, V. S., Kinh, V. T., Davenport, T. M., Yerkes, J. W., ... & Emery, K. A. (1990, May). Over 35% efficient GaAs/GaSb stacked concentrator cell assemblies for terrestrial applications. In *Conference Record, 21st IEEE Photovoltaic Specialists Conference, Kissimimee* (pp. 190-195).

63. Wanlass, M. W., Ward, J. S., Emery, K. A., Gessert, T. A., Osterwald, C. R., & Coutts, T. J. (1991). High-performance concentrator tandem solar cells based on IR-sensitive bottom cells. *Solar cells*, *30*(1-4), 363-371.

64. Pan, J. L., Choy, H. K., & Fonstad, C. G. (2000). Very large radiative transfer over small distances from a black body for thermophotovoltaic applications. *IEEE Transactions on Electron Devices*, *47*(1), 241-249.

65. Whale, M. D., & Cravalho, E. G. (2002). Modeling and performance of microscale thermophotovoltaic energy conversion devices. *IEEE Transactions on Energy Conversion*, *17*(1), 130-142.

66. Phillipe-Jean, M., Joulain, K., Carminati, R., & Greffet, J. J. (2002). Microscale Therm. *Eng*, *6*, 209.

67. Fox, M. (2002). Optical properties of solids.

68. Planck, M. (1900). The theory of heat radiation. *Entropie*, *144*(190), 164.

69. Lambert, J. H. (1760). *Photometria sive de mensura et gradibus luminis, colorum et umbrae*. sumptibus vidvae E. Klett, typis CP Detleffsen.

70. Wehrer, R., Wanlass, M., Wilt, D., Wernsman, B., Siergiej, R., & Carapella, J. (2003, May). InGaAs series-connected, tandem, MIM TPV converters. In *3rd World Conference on Photovoltaic Energy Conversion, 2003. Proceedings of* (Vol. 1, pp. 892-895). IEEE.

71. Narayan, T. C., Nizamian, D. P., Luciano, C., Johnson, B. A., Limpinsel, M., Young, A. R., ... & Bierman, D. M. (2021, June). Platform for Accurate Efficiency Quantification

of> 35% Efficient Thermophotovoltaic Cells. In *2021 IEEE 48th Photovoltaic Specialists Conference (PVSC)* (pp. 1352-1354). IEEE.

72. Schulte, K. L., France, R. M., Friedman, D. J., LaPotin, A. D., Henry, A., & Steiner, M. A. (2020). Inverted metamorphic AlGaInAs/GaInAs tandem thermophotovoltaic cell designed for thermal energy grid storage application. *Journal of Applied Physics*, *128*(14), 143103.

73. LaPotin, A., Schulte, K. L., Steiner, M. A., Buznitsky, K., Kelsall, C. C., Friedman, D. J., ... & Henry, A. (2021). Thermophotovoltaic Efficiency of 40%. *arXiv preprint arXiv:2108.09613*.

74. Gruginskie, N., Van Laar, S. C. W., Bauhuis, G., Mulder, P., Van Eerden, M., Vlieg, E., & Schermer, J. J. (2018). Increased performance of thin-film GaAs solar cells by rear contact/mirror patterning. *Thin Solid Films*, *660*, 10-18.

75. Gruginskie, N., Cappelluti, F., Bauhuis, G., Tibaldi, A., Giliberti, G., Mulder, P., ... & Schermer, J. (2021). Limiting mechanisms for photon recycling in thin-film GaAs solar cells. *Progress in Photovoltaics: Research and Applications*, *29*(3), 379-390.

76. Schilling, C. L., Hoehn, O., Micha, D. N., Heckelmann, S., Klinger, V., Oliva, E., ... & Dimroth, F. (2017). Combining photon recycling and concentrated illumination in a GaAs heterojunction solar cell. *IEEE Journal of Photovoltaics*, *8*(1), 348-354.

77. Helmers, H., Lopez, E., Höhn, O., Lackner, D., Schön, J., Schauerte, M., ... & Bett, A. W. (2021). 68.9% Efficient GaAs-Based Photonic Power Conversion Enabled by Photon Recycling and Optical Resonance. *physica status solidi (RRL)–Rapid Research Letters*, 2100113.

78. Kitamura, R., Pilon, L., & Jonasz, M. (2007). Optical constants of silica glass from extreme ultraviolet to far infrared at near room temperature. *Applied optics*, *46*(33), 8118-8133.

79. Rodríguez-de Marcos, L. V., Larruquert, J. I., Méndez, J. A., & Aznárez, J. A. (2017). Self-consistent optical constants of $MgF_2$, $LaF_3$, and $CeF_3$ films. *Optical Materials Express*, *7*(3), 989-1006.

80. Ozaki, S. O. S., & Adachi, S. A. S. (1993). Optical constants of cubic ZnS. *Japanese journal of applied physics*, *32*(11R), 5008.

81. Olmon, R. L., Slovick, B., Johnson, T. W., Shelton, D., Oh, S. H., Boreman, G. D., & Raschke, M. B. (2012). Optical dielectric function of gold. *Physical Review B*, *86*(23), 235147.

82. Mash, I. D., & Motulevich, G. P. (1973). Optical constants and electronic characteristics of titanium. *Sov. Phys. JETP*, *36*, 516-519.

83. Yang, H. U., D'Archangel, J., Sundheimer, M. L., Tucker, E., Boreman, G. D., & Raschke, M. B. (2015). Optical dielectric function of silver. *Physical Review B*, *91*(23), 235137.

84. Born, M., & Wolf, E. (2013). *Principles of optics: electromagnetic theory of propagation, interference and diffraction of light*. Elsevier.

85. Byrnes, S. J. (2016). Multilayer optical calculations. *arXiv preprint arXiv:1603.02720*.

86. M. G. Moharam, D.A. Pommet, E.B. Grann, T.K. Gaylord, Stable implementation of the rigorous coupled-wave analysis for surface-relief gratings: enhanced transmittance matrix approach, J. Opt. Soc. Amer. A 12 (1995) 1077–1086.

87. Liu, V., & Fan, S. (2012). S4: A free electromagnetic solver for layered periodic structures. *Computer Physics Communications*, *183*(10), 2233-2244.

88. Zanella, P., Rossetto, G., Brianese, N., Ossola, F., Porchia, M., & Williams, J. O. (1991). Organometallic precursors in the growth of epitaxial thin films of III-V semiconductors by metal-organic chemical vapor deposition (MOCVD). *Chemistry of Materials*, *3*(2), 225-242.

89. Duda, A., Ward, S., & Young, M. (2012). *Inverted metamorphic multijunction (IMM) cell processing instructions* (No. NREL/TP-5200-54049). National Renewable Energy Lab. (NREL), Golden, CO (United States).

90. Hanssen, L. M., & Snail, K. A. (2002). Integrating spheres for mid-and near-infrared reflection spectroscopy. *Handbook of Vibrational Spectroscopy*, *2*, 1175-1192.

91. Schroder, D. K. (2015). *Semiconductor material and device characterization*. John Wiley & Sons.

92. Steiner, M. A., Kurtz, S. R., Geisz, J. F., McMahon, W. E., & Olson, J. M. (2012). Using phase effects to understand measurements of the quantum efficiency and related luminescent coupling in a multijunction solar cell. *IEEE Journal of Photovoltaics*, *2*(4), 424-433.

93. Geisz, J. F., Steiner, M. A., Garcia, I., Kurtz, S. R., & Friedman, D. J. (2013). Enhanced external radiative efficiency for 20.8% efficient single-junction GaInP solar cells. *Applied Physics Letters*, *103*(4), 041118.

94. Geisz, J. F., Steiner, M. A., García, I., France, R. M., McMahon, W. E., Osterwald, C. R., & Friedman, D. J. (2015). Generalized optoelectronic model of series-connected multijunction solar cells. *IEEE Journal of Photovoltaics*, *5*(6), 1827-1839.

95. https://www.pveducation.org/pvcdrom/design-of-silicon-cells/base-resistance

96. https://www.pveducation.org/pvcdrom/solar-cell-operation/characteristic-resistance

97. https://www.pveducation.org/pvcdrom/design-of-silicon-cells/finger-resistance

98. https://www.pveducation.org/pvcdrom/design-of-silicon-cells/emitter-resistance

99. https://www.pveducation.org/pvcdrom/design-of-silicon-cells/contact-resistance

100. Babcock, S. J., Irvin, N. P., Chen, E. Y., Honsberg, C. B., & King, R. R. (2019, June). Effects of high photon gas density and radiative efficiency on upper bounds of energy conversion efficiency in single-crystal solar cells. In *2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)* (pp. 3195-3199). IEEE.

101. Dumke, W. P., Lorenz, M. R., & Pettit, G. D. (1970). Intra-and interband free-carrier absorption and the fundamental absorption edge in n-type InP. *Physical Review B*, *1*(12), 4668.

102. Walukiewicz, W., Lagowski, J., Jastrzebski, L., Rava, P., Lichtensteiger, M., Gatos, C. H., & Gatos, H. C. (1980). Electron mobility and free-carrier absorption in InP; determination of the compensation ratio. *Journal of Applied Physics*, *51*(5), 2659-2668.

103. Arulanandam, M. K., Buencuerpo, J., Steiner, M. A., Tervo, E. J., Kuritzky, L. Y., Perl, E. E., ... & King, R. R. (2021, June). Rigorous Coupled Wave Analysis of GaAs Thermophotovoltaic Devices with a Patterned Dielectric Back Contact. In *2021 IEEE 48th Photovoltaic Specialists Conference (PVSC)* (pp. 2580-2583). IEEE.

104. Palmer, C., & Loewen, E. G. (2005). Diffraction grating handbook.

105. Hutley, M. C. (1982). Diffraction gratings. *Techniques of Physics*.

106. Swanson, R. M. (1979). *Silicon photovoltaic cells in TPV conversion* (No. EPRI-ER-1272). Stanford Univ., CA (USA). Stanford Electronics Labs.

107. Green, M. A. (1982). Accuracy of analytical expressions for solar cell fill factors. *Solar Cells*, *7*(3), 337-340.

108. Fan, D., Burger, T., McSherry, S., Lee, B., Lenert, A., & Forrest, S. R. (2020). Near-perfect photon utilization in an air-bridge thermophotovoltaic cell. *Nature*, *586*(7828), 237-241.

109. Schilling, C. L., Hoehn, O., Micha, D. N., Heckelmann, S., Klinger, V., Oliva, E., ... & Dimroth, F. (2017). Combining photon recycling and concentrated illumination in a GaAs heterojunction solar cell. *IEEE Journal of Photovoltaics*, *8*(1), 348-354.

110. Hwang, S. T., Hwang, T., Lee, S., Gil, B., & Park, B. (2018). Selective rear contact for Ga0. 5In0. 5P-and GaAs-based solar cells. *Solar Energy Materials and Solar Cells*, *182*, 348-353.

111. Ashraf, Shakeel, et al. "Surface modification of SU-8 for metal/SU-8 adhesion using RF plasma treatment for application in thermopile detectors." *Materials Research Express* 2.8 (2015): 086501.

112. Kim, J. H., Lim, D. H., & Yang, G. M. (1998). Selective etching of AlGaAs/GaAs structures using the solutions of citric acid/H 2 O 2 and de-ionized H 2 O/buffered oxide etch. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, *16*(2), 558-560.

113. Liao, Z., & Aitchison, J. S. (2017). Precision etching for multi-level AlGaAs waveguides. *Optical Materials Express*, *7*(3), 895-903.

114. Arulanandam, M. K., Steiner, M. A., Tervo, E. J., Young, A. R., Kuritzky, L. Y., Perl, E. E., ... & King, R. R. (2022). GaAs thermophotovoltaic patterned dielectric back contact devices with improved sub-bandgap reflectance. *Solar Energy Materials and Solar Cells*, *238*, 111545.

115. Liu, V., & Fan, S. (2012). S4: A free electromagnetic solver for layered periodic structures. *Computer Physics Communications*, *183*(10), 2233-2244.

116. A. Taflove and S.C. Hagness, Computational Electrodynamics: The Finite-Difference Time-Domain Method, Artech: Norwood, MA, 2005.

117. Holman, Z. C., Filipič, M., Lipovšek, B., De Wolf, S., Smole, F., Topič, M., & Ballif, C. (2014). Parasitic absorption in the rear reflector of a silicon solar cell: Simulation and measurement of the sub-bandgap reflectance for common dielectric/metal reflectors. *Solar Energy Materials and Solar Cells*, *120*, 426-430.

118. Singh, P., & Ravindra, N. M. (2012). Temperature dependence of solar cell performance—an analysis. *Solar energy materials and solar cells*, *101*, 36-45.

119. Friedman, D. J., & Steiner, M. A. (2019, June). Design of Thermophotovoltaic Cells for Optimal System Efficiency, Accounting for Photon Reuse from Front and Back Contacts. In *2019 IEEE 46th Photovoltaic Specialists Conference (PVSC)* (pp. 3215-3218). IEEE.