Flash Sharing in a Time-Interleaved Pipeline ADC

by

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ABSTRACT

With the advent of parallel processing, primarily the time-interleaved pipeline ADCs, high speed and high resolution ADCs became a possibility. When these speeds touch giga samples per second and resolutions go beyond 12-bits, the parallelization becomes more extensive leading to repeated presence of several identical blocks in the architecture. This thesis discusses one such block, the sub-ADC (Flash ADC), of the pipeline and sharing it with more than two of the parallel processing channels thereby reducing area and power and input load capacitance to each stage. This work presents a design of 'sub-ADC shared in a time-interleaved pipeline ADC' in the IBM 8HP process. It has been implemented with an offset-compensated, kickback-compensated, fast decision making (large input bandwidth) and low power comparator that forms the core part of the design.

ACKNOWLEDGEMENTS

I would like to express my gratitude to my advisor, Dr. Hugh Barnaby, for this opportunity to work under him on this topic. His continuous guidance, insights and encouragement, especially during the critical phase of this thesis, helped me complete this work. I thank him for his moral and financial support as well. I am indebted Dr. Esko Mikkola for all the valuable discussions and suggestions during the course of this project. I would also like to extend my sincerest thanks to Dr. Jennifer Kitchen for agreeing to serve on the defense committee.

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LIST OF ABBREVIATIONS

ADC	Analog to Digital Converters
ENOB	Effective Number Of Bits
DAC	Digital to Analog Converter
FF	Flip Flop
FFT	Fast Fourier Transform
LSB	Least Significant Bit
MDAC	Multiplying Digital to Analog Converter
MSB	Most Significant Bit
RSD	Redundant Signed Digit
S/H	Sample and Hold
SFDR	Spurious Free Dynamic Range
SNDR	Signal-to-Noise and Distortion Ratio
THD	Total Harmonic Distortion
TIA	Time Interleaved ADC
TIPA	Time Interleaved Pipeline ADC
T/H	Track and Hold

1. Introduction

Low-power, low-area analog-to-digital converters (ADCs) are always a subject of research due to the growing number of critical ADC applications, from satellites to mobile communications to medical instruments. Of these, of special interest are high resolution and high sampling rate ADCs. Figure 1-1 [5] shows where different types of ADCs fit into the specification space defined by part resolution or effective number of bits (ENOB) and sampling rate.

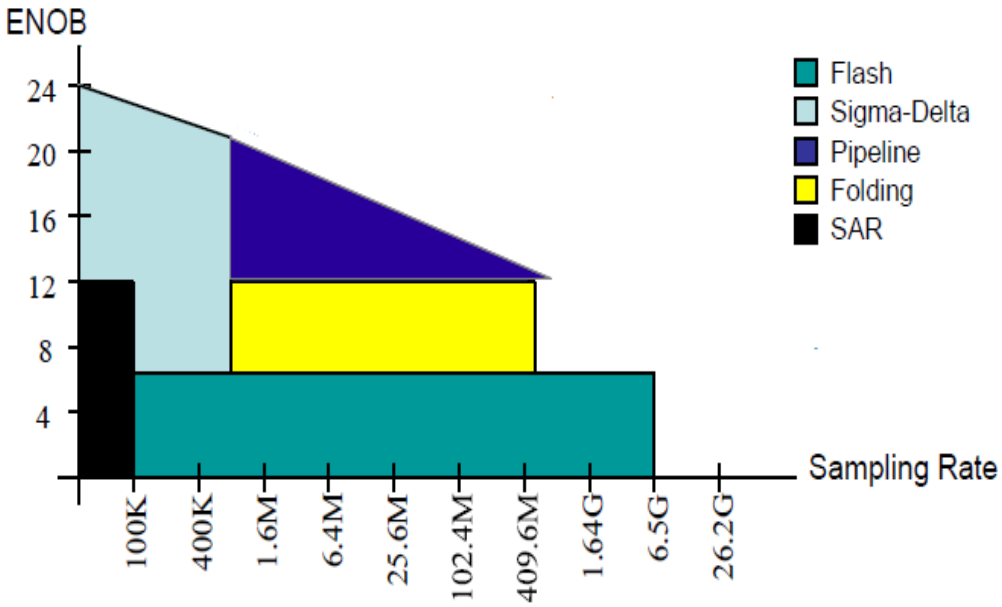

Figure 1-1. Different types of ADCs over resolution and speed [5].

This thesis presents the details of different high-speed, high-resolution ADCs and presents a new resource sharing mechanism which can realized critical reductions in area and switching power.

2. ADC Architectures (High Speed ADCs)

2.1 Flash ADC

Flash ADCs are by far the fastest and simplest architecture types which are designed for resolutions up to seven or eight bits and frequencies ranging from few hundreds of kilo samples per second to beyond giga samples per second. Such high speeds of conversions are achieved due to fully parallel conversions of the input signal and hence the flash architectures are also called parallel ADCs.

Figure 2-1 shows a typical N-bit flash converter. It employs a series of comparators, each comparing the input signal with a unique reference voltage. The difference between two consecutive reference voltages is one LSB and is derived by the stacked resistor ladder as shown. The comparison produces a "1" (logic high) when analog input voltage is greater than the applied reference voltage; otherwise, a "0" (logic low) is produced. This generates a 2N-1 bit thermometer code which is then encoded into an N-bit digital code. N-bits ➔ 2N-1 bit thermometer code ➔ 2N-1 comparators

The main drawbacks to this architecture are

- It requires 2^N-1 comparators for N-bit resolution implying that area, power and input parasitic capacitance become prohibitively large[5] beyond a six or seven bit implementation. Considering seven to eight bits a general necessity for a practical ADC, this architecture shows its weakness [4].
- The linearity and resolution are dependent on resistor matching and the transistor matching in the comparators.

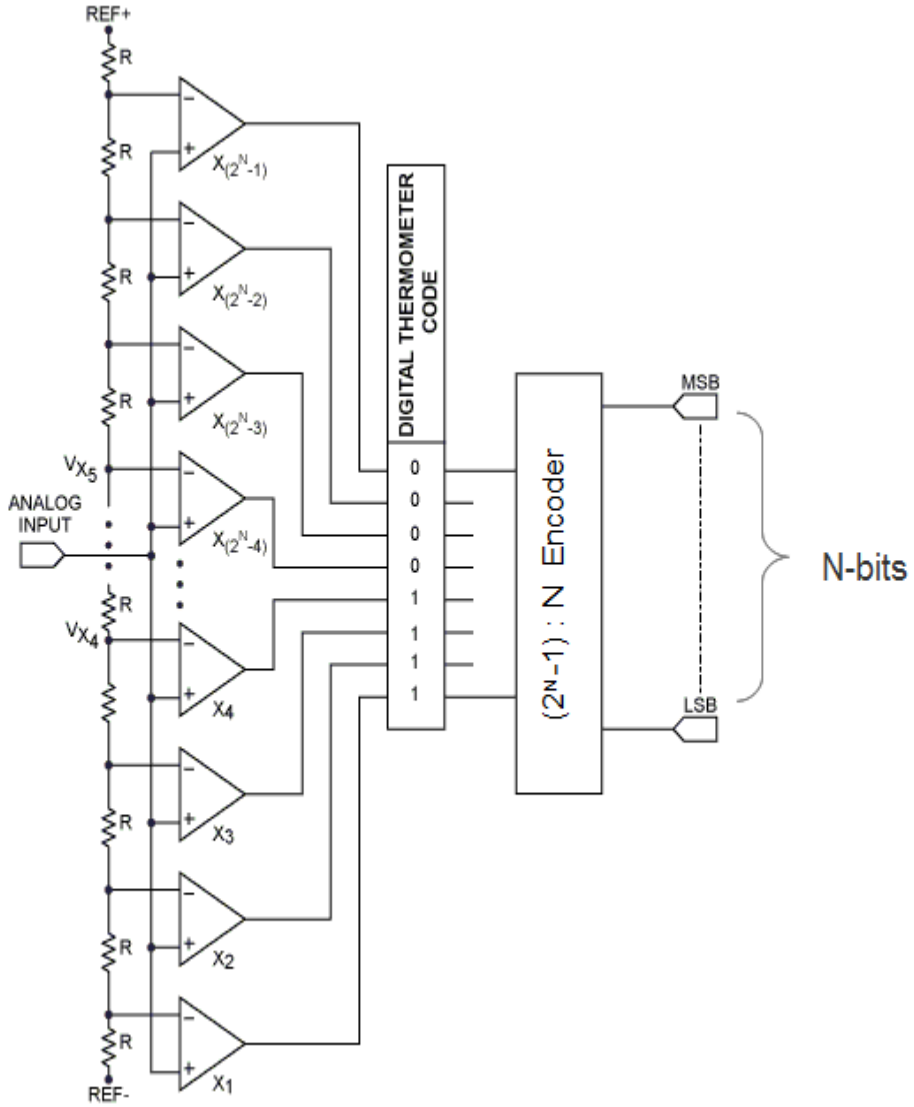

Figure 2-1. Flash ADC with Thermometer to Binary Encoder

2.2 Two-step Flash

A two-step flash is a split flash ADC where the most significant bits (MSBs) and least significant bits (LSBs) are converted using two ADCs. As shown in Figure 2-2, it has an M-bit flash ADC for MSB conversion, an MDAC for analog conversion of these MSBs, an error amplifier (2^M) for residue generation and an N-bit flash ADC for LSB conversion. MDAC must be M-bit linear and the second ADC N-bit linear.

The key features of this conversion process are shown in Figure 2-3. The advantage of this architecture is that the number of comparators is significantly reduced. For example if M and N were equal to K, for resolving 2K bits in flash, one would need 22K - 1 comparators and in this architecture we need just 2(2K - 1) comparators for resolving the same 2K bits.

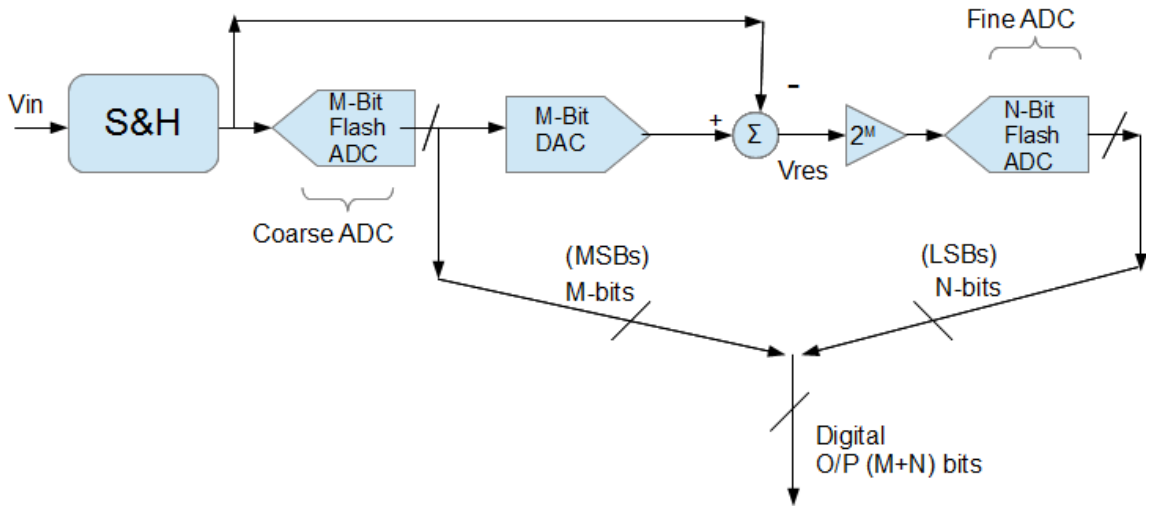

Figure 2-2. Two Step Flash

As the resolution increases, two-step ADCs still suffer from drawbacks similar to flash ADCs since the flash ADCs are the core part of conversion. The area and power are still a power function of the number of bits (as the number of bits increase the number of quantization levels in each ADC increase and hence the number of comparators increase). The linearity again depends on transistor matching in comparators and resistor matching of the reference voltage network. In order to address these linearity, power and area issues the next step is Pipelined ADCs.

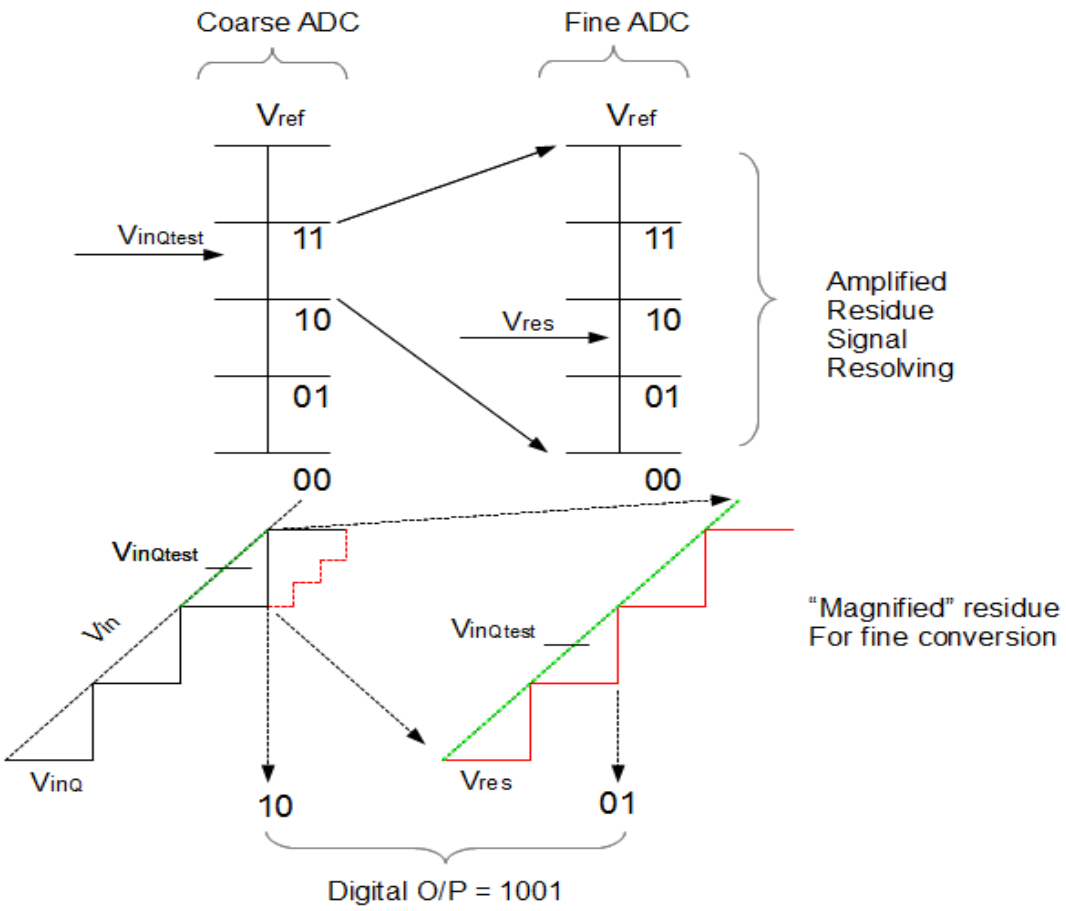

Figure 2-3. Voltage conversion in a 2-Step Flash

As shown in the Figure 2-3, the first ADC, also called the 'coarse ADC', resolves the MSBs of the $V_{inQtest}$ and then a residue signal is generated using the input and the MDAC signals. This residue signal is multiplied by 2M and is resolved to give LSBs of the $V_{inQtest}$ and then the bits are added to give the final resolution of $V_{inQtest}$.

2.3 Pipeline ADC:

The Pipeline architecture is a solution for higher resolution and high speed converters. The key idea is to cascade several low resolution stages to obtain a high overall resolution ADC. They work on the same principle as a 2-step flash, but they have more stages 'pipelined'. A typical pipeline ADC is shown in Figure 2-4.

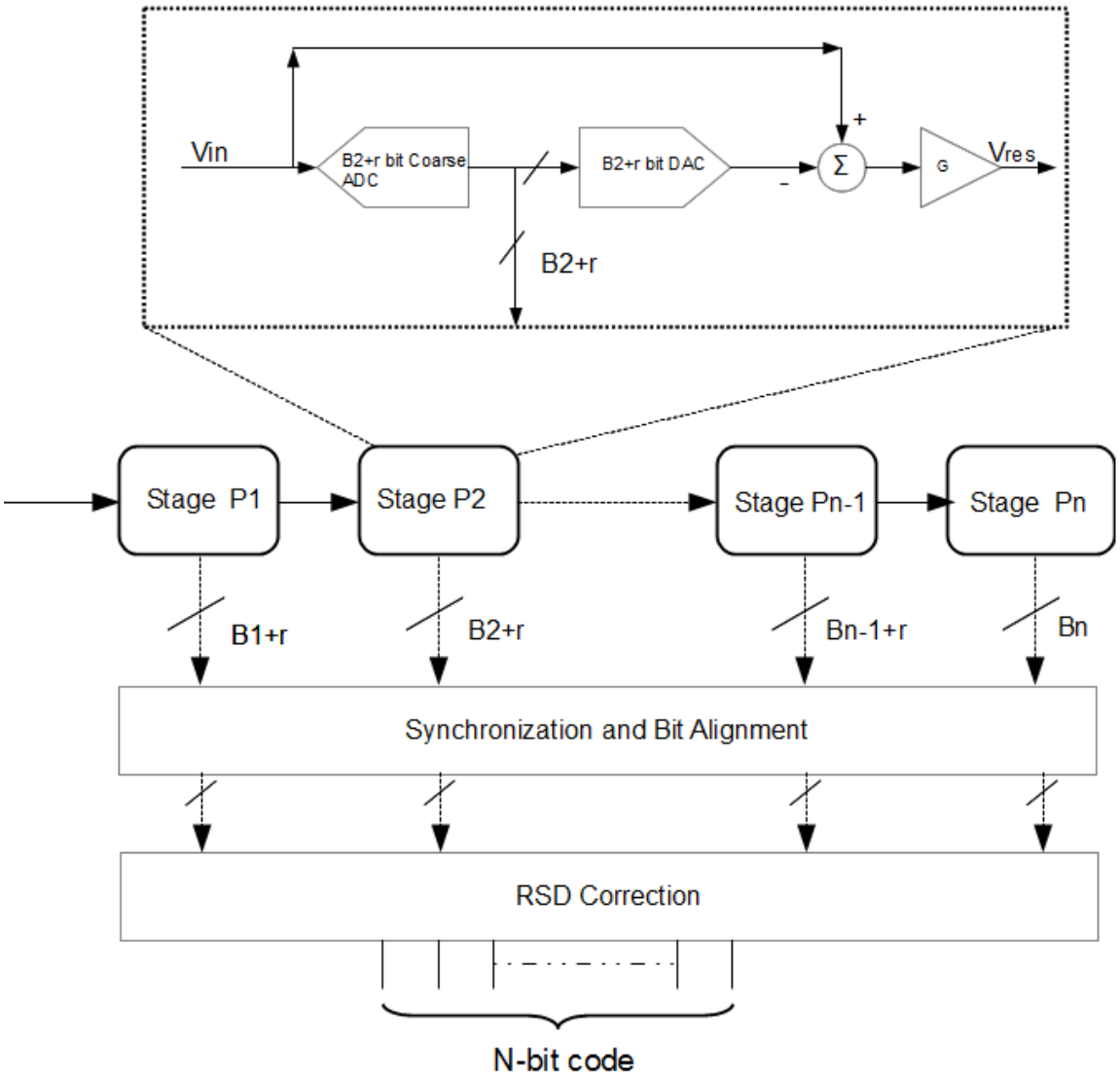

Figure 2-4. Pipelined ADC with RSD correction.

Each stage (similar to first stage of 2-step flash) consists of S/H, Flash ADC, MDAC, feed-forward and a voltage gain amplifier. Each stage makes a 'rough' estimation of its input signal and passes a precise 'remainder' to the next stage for 'fine' estimation. While the next stage is operating on this remainder as its input, the previous stage samples a new input and performs its own operation simultaneously thereby increasing the throughput via this concurrent operation.

Due to the stacking of stages and each stage having its own conversion-dependent residue generation, pipeline ADCs have large latencies compared to other

high speed ADCs. Each stage produces Bk+r bits i.e. where Bk represents the regular output bits and r is the redundant bit. All the redundant bits caused by offsets in the comparators in the coarse ADC are corrected and resolved in Redundant Signed Digit (RSD) correction. The complexity of the design increases linearly with increased resolution. However with the increase of resolution (and eventually sampling rate), higher slew rate gain amplifiers are required which can bring design challenges in gain stages. A Time Interleaving ADC solves this problem.

2.4 Time-Interleaved ADCs (TIA):

Time-Interleaving is a technique to further parallelize the processing of the ADC or to multiply the sampling rates, using multiple channels. As shown in Figure 2-5 [17], it cycles through N channels such that the total sample rate is N times the sample rate of individual channels. Each channel has a clock which is phase shifted by

$$Td = 1/(N*f_{ts}), \qquad (2\text{-}1)$$

where N is the number of channels (or interleaving factor) and f_{ts} is the aggregate sampling rate. Each channel's sampling rate (or digitizing rate) would be f_s/N. As shown in Figure 2-6, each clock that drives a unique channel has a unique sampling point in the time domain. So each channel's output is given by equation

$$yi[n] = x((nN + i)Ts), \qquad (2\text{-}2)$$

where Ts is sampling period of i_{th} channel processing n_{th} sample.

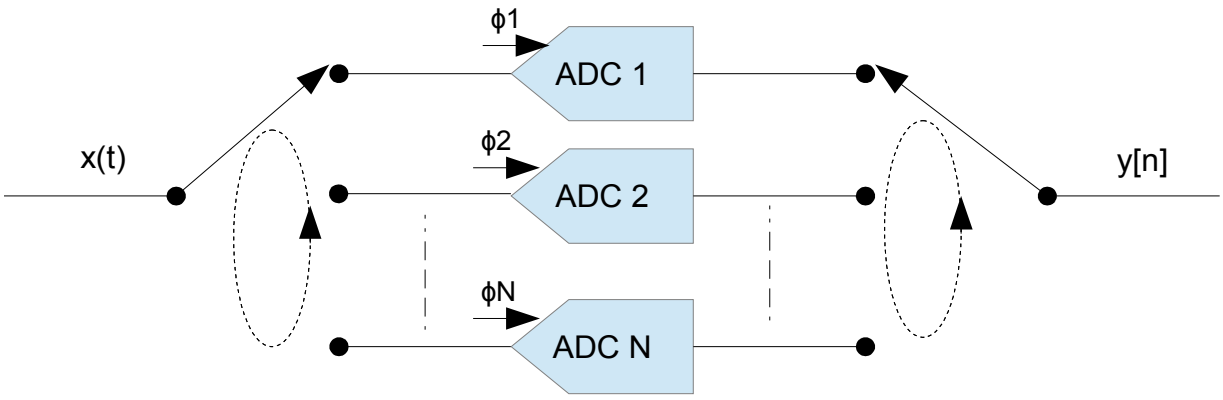

Figure 2-5. Time Interleaving ADC

After output muxing (in the same order as input muxing) we have

$$y[n] = yi((n - i)/N \qquad (2\text{-}3)$$

where i is n mod N.

Two of the main drawbacks [17] of TIAs are:

a) Gain and offset mismatch

b) Timing skew

a) Gain and offset mismatch

These mismatches are caused by mismatch in the channels. The gain Gi in each channel is not precisely the same value. Each channel should be processing ideally, yi[n] = x((nN + i)Ts), but practically it processes,

$$yi[n] = Gi*x((nN + i)Ts) \qquad (2\text{-}4)$$

where *Gi* is the gain mismatch in i_{th} channel and $y_i[n]$ output of the n_{th} sample at the i_{th} channel.

Similarly we have offset mismatch defined as,

$$yi[n] = x((nN + i)Ts) + oi \ , \qquad (2\text{-}5)$$

where *oi* is the offset mismatch caused in i_{th} channel.

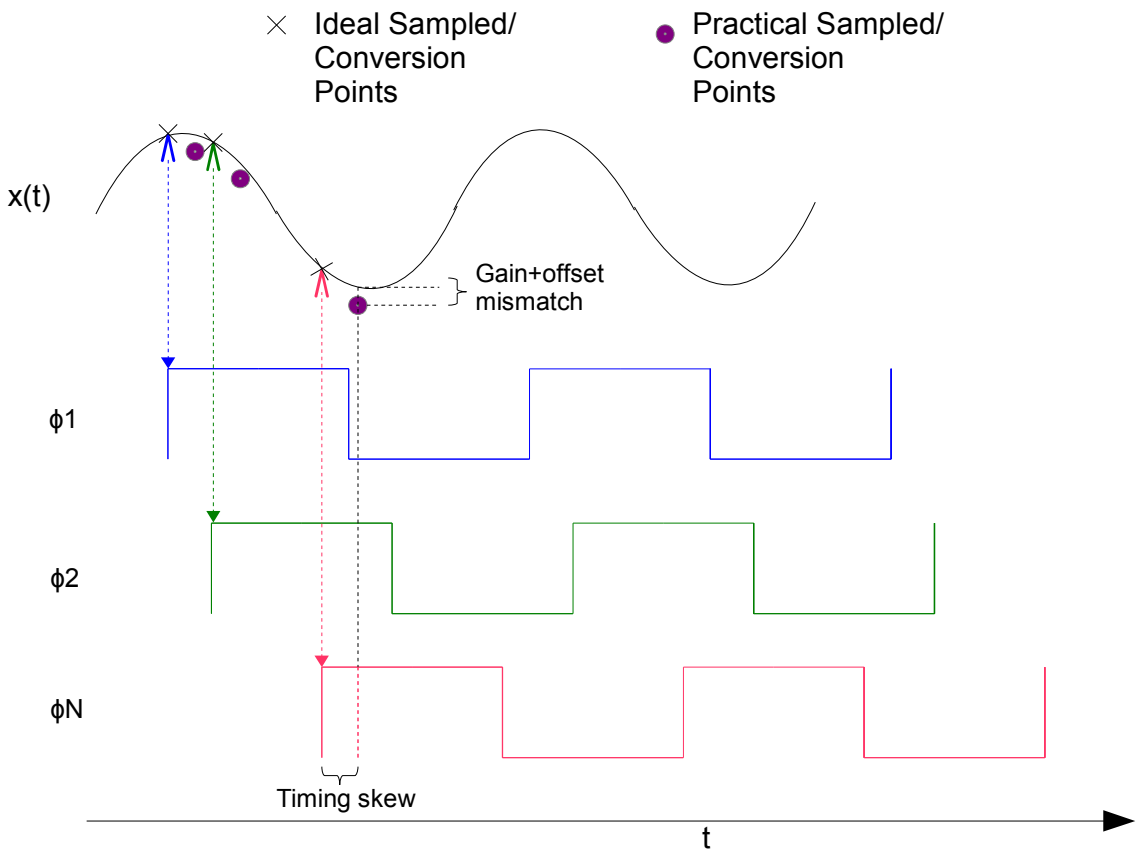

Figure 2-6. Mismatches and skews in TIA

b) Timing Skew

Improper sampling of the input signal because of a skewed sampling edge in the ADC clock causes timing skew. So instead of the expected samples at every nNTs (discrete samples after time period of NTs i.e time between two samples in each channels), we have samples at nNTs ±td, where td is the skew in the clock.

Hence we have samples at

$$yi[n] = x((nN + i)Ts \pm tdi) \qquad (2\text{-}6)$$

where *tdi* is skew in each channel. The combined effects of these offsets and timing skew are shown in Figure 2-6. Gain and offset mismatch are usually corrected by means of digital calibration or by background calibration (by estimation and correction).

For addressing the issue of timing skew, the popular solution is to have a Track and Hold (T/H) at the input stage before the signal is digitized by the channels. The T/H samples at N times the individual channel frequency so that every other channel gets a sample to digitize by the end of its clock cycle.

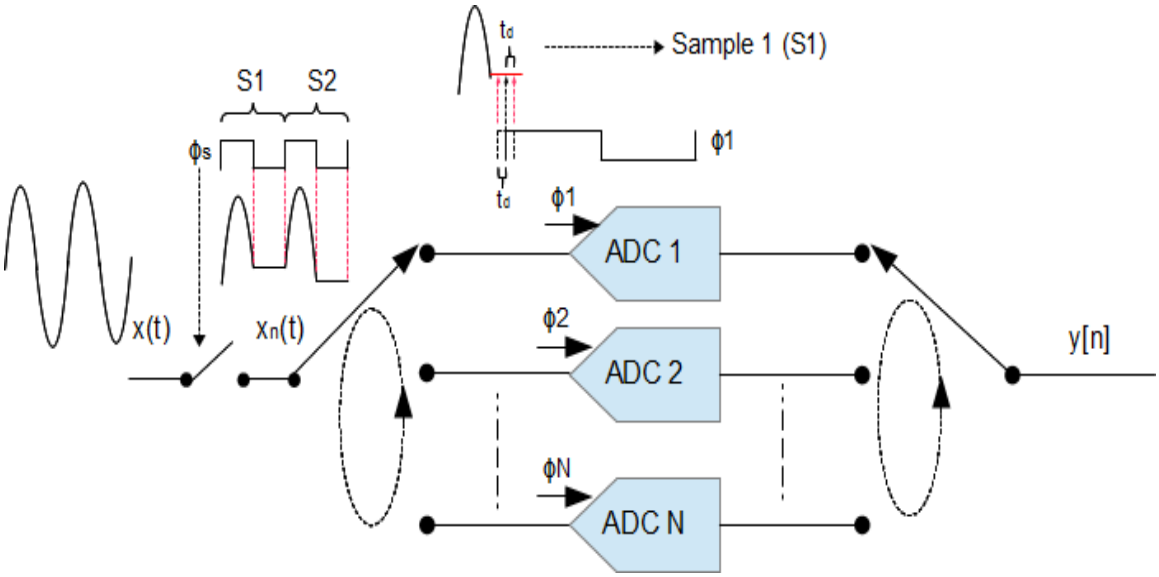

Figure 2-7. Possible alignment of channel clocks according to the sampled input.

This will make sure that the signals to channel ADCs are held (samples) and timing skews in channel clocks will have little effect on digitizing these samples. Figure 2-7 shows a possible alignment of channel clocks with respect to the input sample where a skew of td will not have an effect on digitizing the sample as long as td is not comparable to (1/4Φs).

2.5 Architecture of 3GS/s, 13-bit, Low-Power, 8 way, Time-Interleaved Pipeline ADC (TIPA):

Combining the architectures of Pipeline and Time-Interleaving, we can have an ADC capable of high sampling rates and high resolution as explained before. The

initial proposed architecture of a TIPA has a T/H as front end sampler (as discussed in chapter 2.4) and parallel channels following the sampler is shown in Figure 2-8.

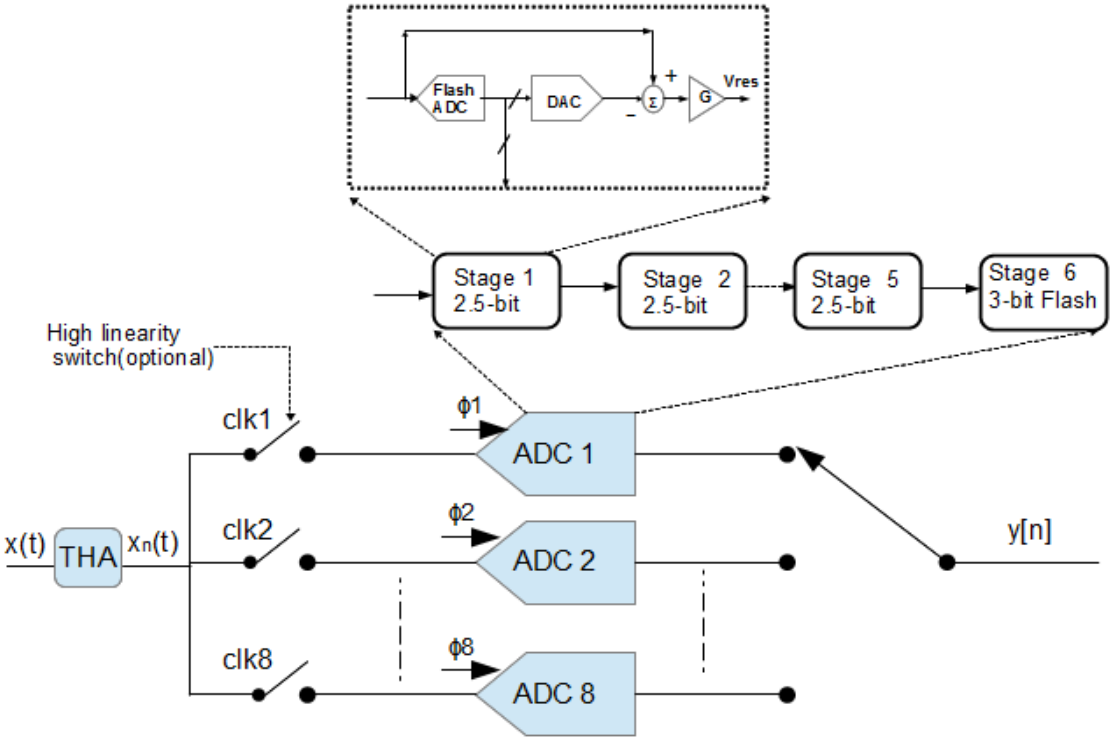

Figure 2-8. Showing TIPA

Each channel has a front-end 2.5-bit stage followed by four 2.5-bit stages and a 3-bit flash at the back-end. This architecture has multiplexer (switches) between T/H and ADC for each channel so that the T/H is not overloaded by all eight channels at the same time. However having these switches will result in high settling errors thereby degrading the Signal-to-Noise and Distortion Ratio (SNDR) of the output. So there is a choice between having these switches based on the design complexity of these high linear switches and/or T/H load driving strength. The design complexity increases as the new switches have to be high linear switches and the timing constraint becomes stringent as the new clocks required to drive these switches have very short duty cycle. So if the T/H is able to drive the channels with the new architecture, then we can avoid these switches. Also each stage of the channel has

its own switching network that works as sample and hold at the summation point. Figure 2-9 gives a more detailed view of first stage in the channel.

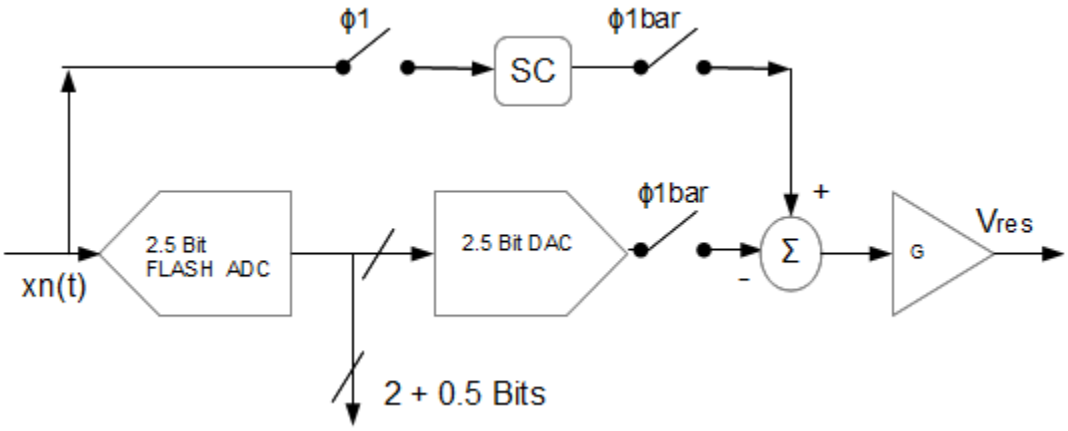

Figure 2-9. Showing first stage of pipeline

Since it operates at 3GS/s, the main T/H runs on a 3GHz clock and each of the channels run on 375 MHz (time-interleaving factor 8) complementary clocks. During the phase Φ1 high & Φ1bar low, the input xn(t)) is sampled by the switch cap (SC) block, the 2.5 Bit Flash ADC makes the conversion and these are read by flip flops clocked by delayed Φ1 so that the data after the flash is stored until the end of the clock cycle. During the phase Φ1 low & Φ1bar high, the sampled data by the SC is held and the MDAC output is subtracted and amplified to produce Vres. The idea extends to the following stages too, except that every other stage works on alternating clocks, i.e, if stage k works with Φ1 as a sampling clock and Φ1bar as the holding clock, then stage k+1 works with Φ1 as the holding clock and Φ1bar as the sampling clock. The architecture remains the same for other stages through Stage 6. All the clocks for the eight channels are shown in Figure 2-10.

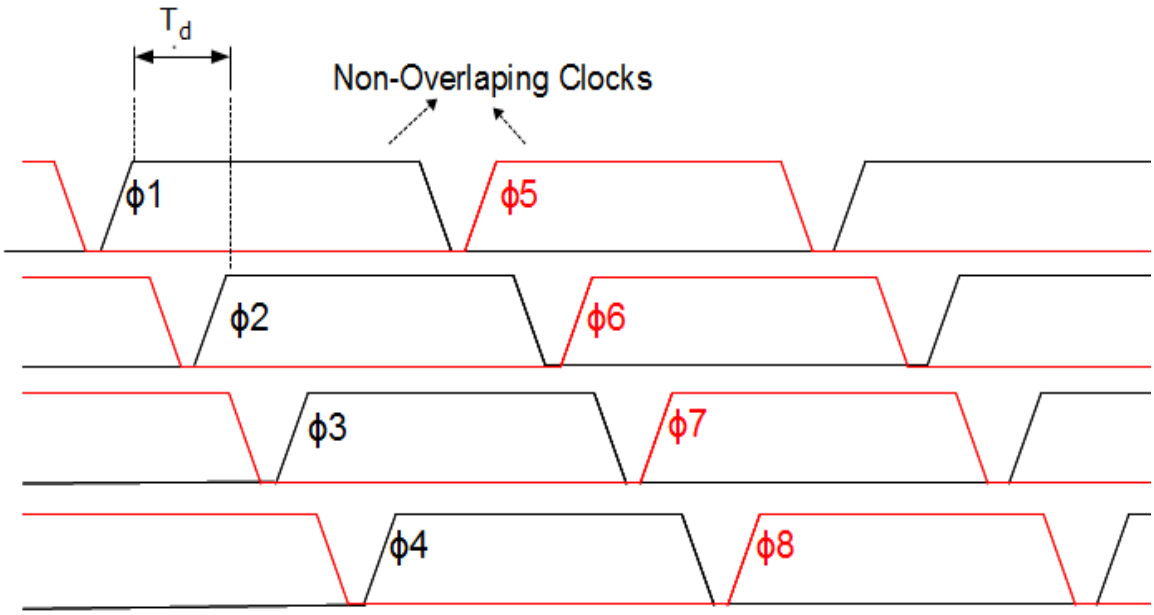

Figure 2-10. Channel clocks each delayed by Td

The clocks are generated as non-overlapped clocks in order to implement a double sampling technique. Φi and Φi+1 are separated by a time delay of Td (from chapter 2.4) of 333pS which is equivalent to a phase shift of 45°.

As shown in Figure 2-9, high resolution low power pipeline ADCs implement a first stage that resolves 2 bits (and a redundant bit) by a 2.5-bit Flash ADC that is connected to the output (xn(t)) of the T/H. Each 2.5-bit Flash ADC has 6 comparators and 8 channels thus requires a total of 48 comparators. Each comparator (design discussed in chapter 3.3) presents a load of 30 fF to 60 fF (depending on the phase of operation) which makes the total load on the T/H due to the front end 2.5-bit stage 1.44pF to 2.88pF, which greatly effects the bandwidth of the T/H. Also the total number of comparators required in one channel (five 2.5-bit stages: 30 comparators, a three bit flash: 7 comparators) is 37. So eight channels need 296 comparators. This consumes significant amount of area. So we propose a

new sub-ADC architecture which exploits the availability of eight different-phased clocks and some good static timing management. This new sub-ADC can be shared between two or more (depending on the inputs) channels thereby becoming area efficient, power efficient and also offer less load to the T/H.

2.6 Proposed Sub-ADC Architecture

The proposed architecture, shown in Figure 2-11, uses specially designed comparators (discussed in chapter 3.4) that share their inputs with more than one channel and use the available clocks for novel switching leading to resource sharing approach. The clock sequences (clock seq1 and clock seq2 discussed in chapter 3.4.2) form effectively a 4:1 demux from comparator outputs to the ROM encoder for the thermometer code for binary conversion. After the binary conversion, each of the bits is again distributed to its respective channel with proper timing analysis of the flip-flop clocks.

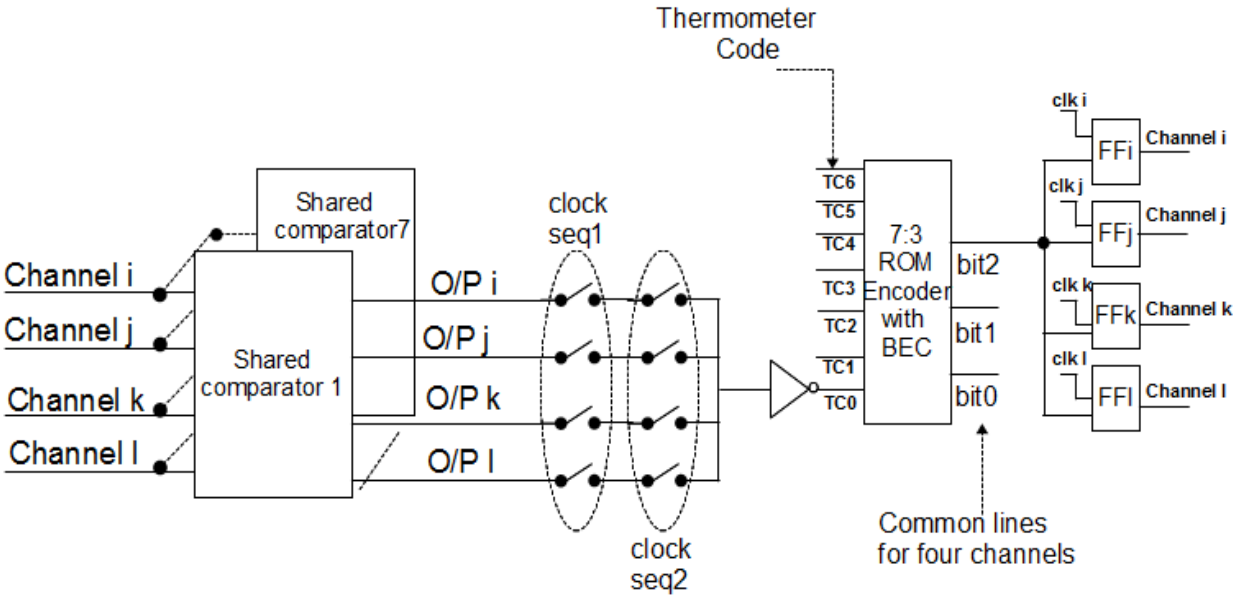

Figure 2-11. Proposed sub-ADC Architecture

The proposed new front-end stage is shown in Figure 2-12 which has a sub-ADC shared between four channels. The selection of channels were done after static timing analysis (discussed in chapter 3.4.2).

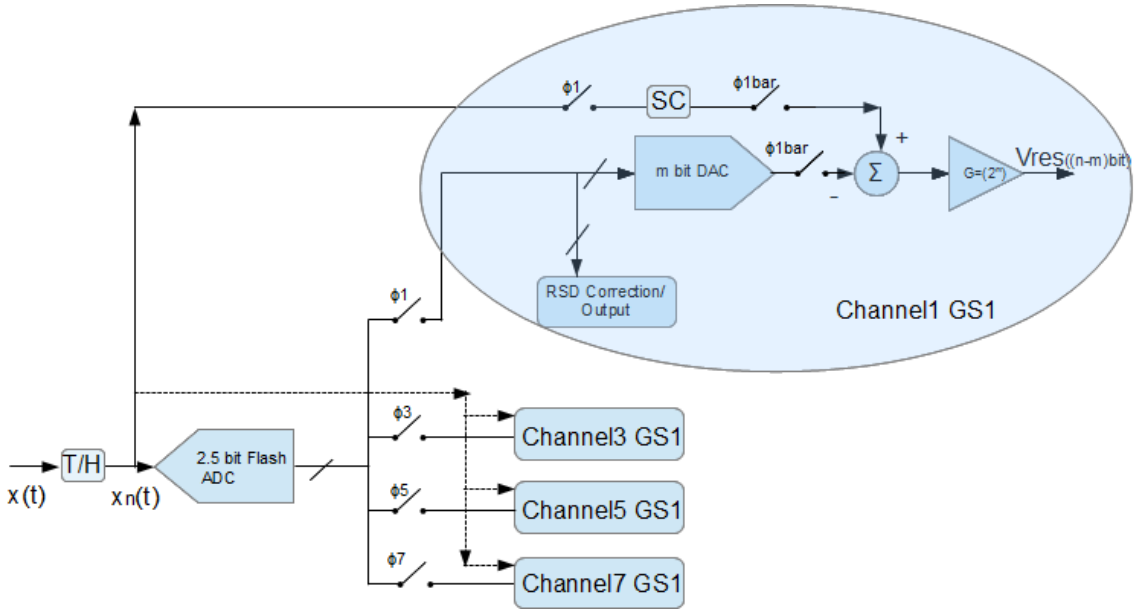

Figure 2-12. Proposed front-end stage

The goal is to design a 3-bit flash ADC that operates at the given channel frequency (375MHz), is able to generate 4-channel outputs and test its linearity for each of the channels.

As discussed in chapter 2.1, an N-bit flash requires a 2N-1 levels (and hence 2N-1 comparators) of thermometer code. Here we need a 2.5-bit flash or higher (3-bit flash in this report) which has two effective bits and a half redundancy bit. Hence a 7-comparator flash with a resolution of 2.5-bits or more is needed. The first step of our design is the comparator, which forms the core of the Flash adc.

3. Choice of Comparator

3.1 Introduction

Comparison is a fundamental operation in any analog to digital converter. Typically a latched comparator that does the comparison on an edge of a clock is used in pipelined ADCs. These comparators can be classified based upon their power dissipation, speed of decision making (smaller input pulse width), kickback noise (discussed in chapter 3.4.2) and offset voltage.

3.2 Pre-Amp based Comparators (Static Latched & Class AB Latched Comparators)

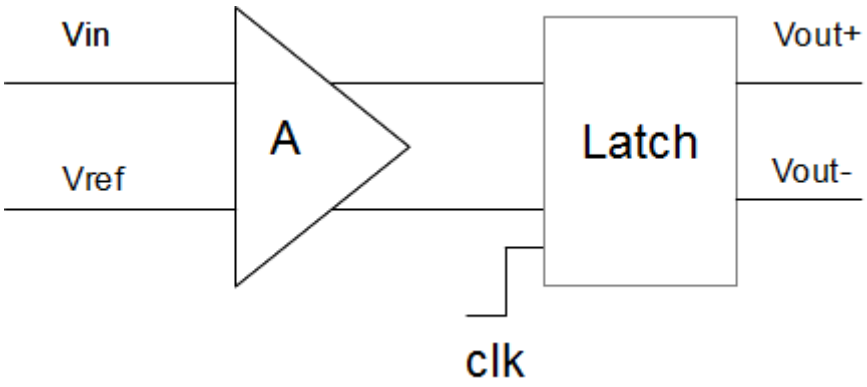

Figure 3-1. Functional diagram of Amplifier based Comparators

In this class of comparators we have an amplifier (or multiple stages of amplifiers cascaded) preceding the latch stage. They have two modes of operation: 1) reset, where both complementary outputs are set at logical high (or low) and 2) evaluation, where outputs are toggled based upon the inputs at pre-amplifier. These kinds of comparators, because of their gain in the pre-amplifier, reduce the input-referred offset voltage. The static latched (SL) comparator has less kickback noise than the standard Class AB latched type because of the lower drain voltages required. The SL comparator also offers high rates of data conversion. However since both topologies have static supply current flowing in the pre-amplifier (SL / class-AB), they consume static power and hence are not good choice for low power data converters. Figure 3-1 shows a simple block diagram of a Pre-Amp based comparator.

3.3 Dynamic Latched Comparators:

For low power comparators, the well-known solutions are dynamic Latched (DL) comparators. Unlike the pre-amp based comparators, current flows in these comparators only during regeneration phase. Three well known topologies of dynamic latched comparators are 1) Resistive Divider Comparator 2) Capacitive Differential Pair Comparator 3) Differential Pair Comparator 3) Modified Differential Pair Comparator.

3.3.1 Resistive Divider Comparator (RDC):

The comparator shown in Figure 3-2 is first introduced in [9] and is widely used in pipeline ADCs. It is based on differential sensing amplifier. Transistors M1-M4 are biased in linear region and act as voltage controlled resistors (hence the name resistive divider). Transistors M5-M12 form a latch.

During the reset phase, when the clock is low ($\Phi = 0$): M7 and M8 are cutoff, M9 and M12 start conducting which forces output nodes Vout+ and Vout- to charge up to Vdd. This means the gates of M5 and M6 are also at Vdd. During the evaluation phase, when the clock is high ($\Phi = Vdd$), M7 and M8 are turned on and act like switches thereby making the pairs M5-M10 and M6-M11 act as cross-coupled latches. Based on the imbalance between the currents flowing in branches B1 and B2, the cross-coupled inverters split to complementary (Vdd, 0) outputs. The imbalance in currents is caused by to the node voltages at B1 and B2. If no mismatch is present, the trip (voltage splitting in the cross-coupled latch) point is set when both the branches have same current. This happens when

$$V_{in+} - V_{in-} = \frac{W_B}{W_A}(V_{ref+} - V_{ref-}) \qquad (3\text{-}1)$$

where $W_A = W2 = W4$ and $W_B = W1 = W3$.

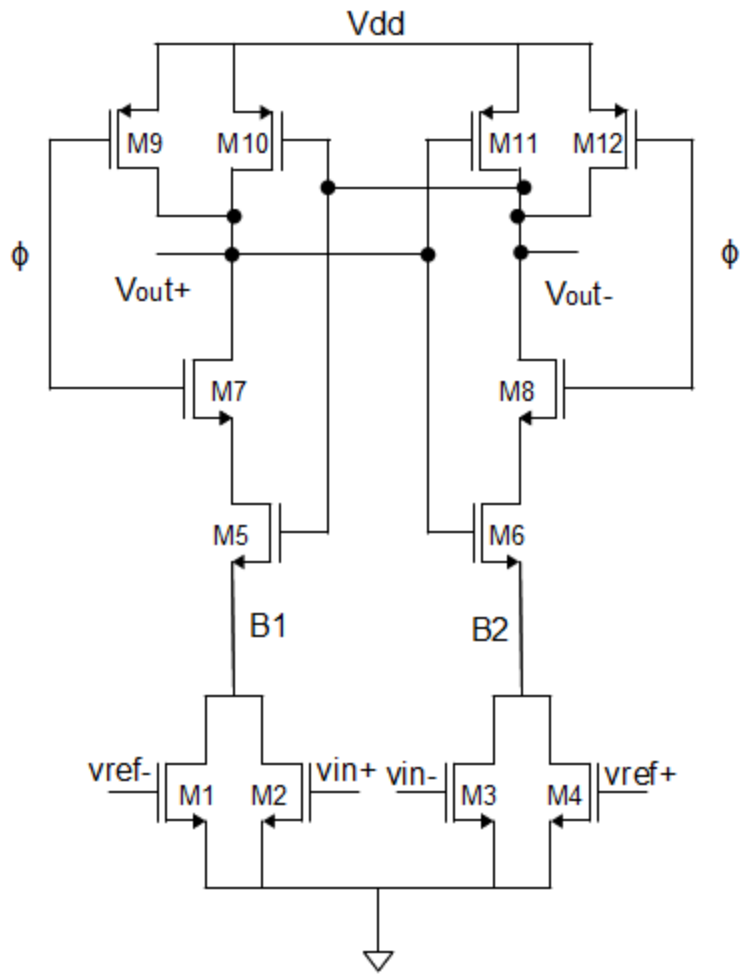

Figure 3-2. RDC or Lewis Gray Comparator

From the above equation it can be said that the trip point of the comparator is largely affected by the width mismatch of M1-M4, resulting in offset. Offsets due to mismatch in M7-M12 are attenuated by gain of M5 and M6. The currents through the branches are dependent on the input voltages of M1-M4. As the common mode voltage of the transistors increases, the gate controlled resistances decrease which results in larger offsets for smaller mismatches in the input pair.

Though this comparator is popular for its low static power, the offset reaches hundreds of millivolts which cannot be corrected by the RSD of the pipeline ADC.

3.3.2 Capacitive Differential Pair Comparator (CDC)

The topology shown in Figure 3-3 employs a charge summation at the input transistor pair M1-M2. This comparator's offset voltage has no dependence on the input common mode voltage, due to the tail transistor M3 which keeps M1 and M2 in saturation region. During the reset phase (Φ = 0, Φb = Vdd), all sampling capacitors (Cin and Cref) are charged to inputs and reference voltages, transistors M1,M2 & M3 are grounded (cutoff) and simultaneously the outputs Vout+ and Vout- are charged to Vdd.

During the evaluation phase (Φ = Vdd, Φb = 0), the sampled voltages are summed at the gates of M1 and M2. M1, M2 and M3 are in saturation, setting voltages at cross-coupled latch. The trip point is set by the current imbalance between branches B1 and B2 which is dependent on the gate voltages and is given by

$$V_{in+} - V_{in-} = \frac{C_{ref}}{C_{in}}\left[V_{ref+} - V_{ref-}\right] \qquad (3\text{-}2)$$

The offset voltage is dependent on three factors. First is the mismatch in sampling capacitors. With the current technology the capacitors can be matched up to 0.02%, which is well within RSD correction. Second, the ratio of sampling capacitors and parasitic capacitors of input pair should be as small as possible to reduce the charge distribution during evaluation phase. This means large sampling capacitors, which leads to more load on the T/H and more power consumption in switched capacitors. The third factor that determines the offset voltage is the input differential pair:

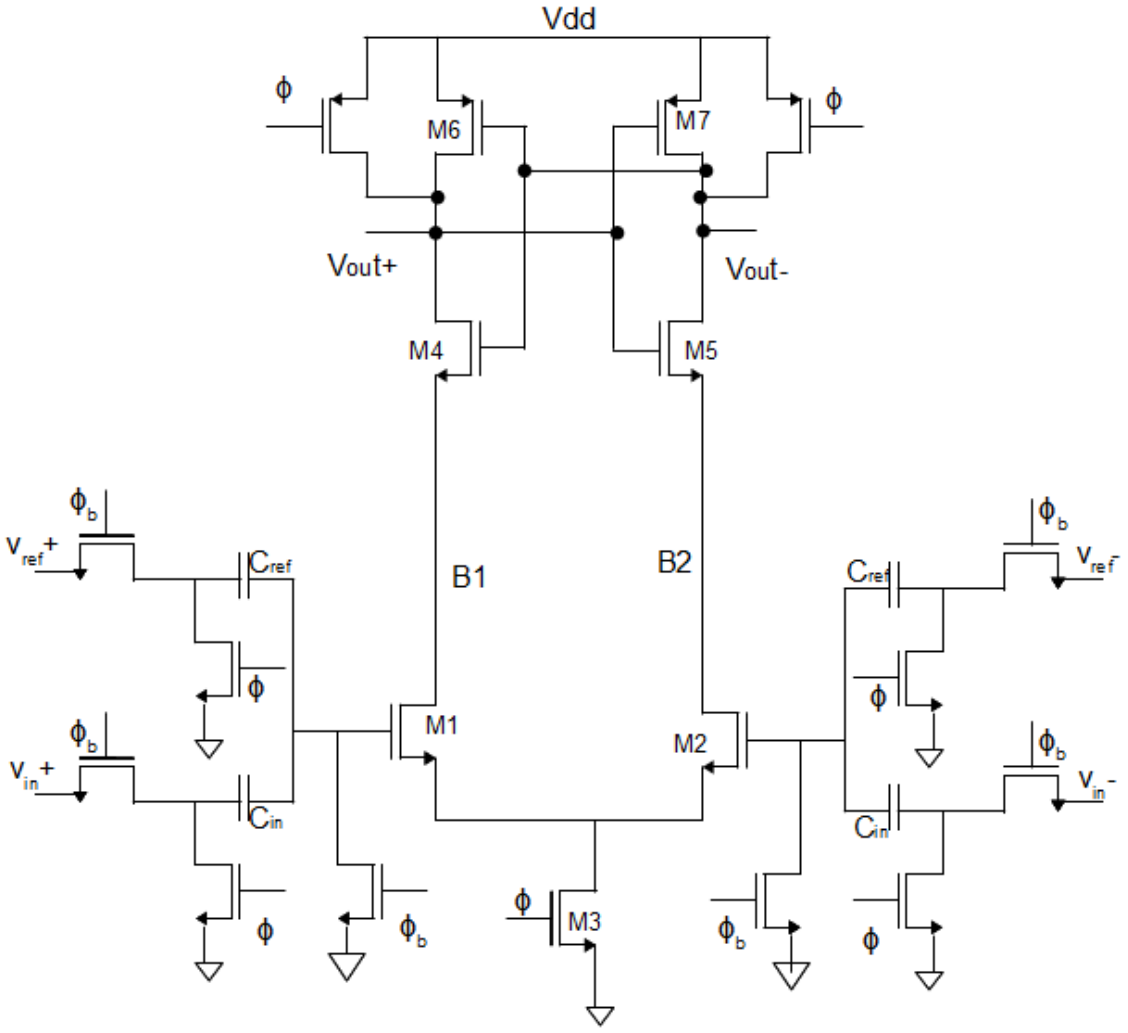

Figure 3-3. Capacitive Differential Pair Comparator

$$V_{os} = \Delta V_t + \frac{V_{gs} - V_t}{2}\left[\frac{\Delta R_L}{R_L} + \frac{\Delta\beta}{\beta}\right], \qquad (3\text{-}3)$$

where $\Delta\beta$ is transistor dimension mismatch, ΔR_L load resistance mismatch and ΔV_t is threshold voltage mismatch between the transistors M1 and M2. Typically, $\Delta\beta$ dominates the mismatch. Due to the large sampling capacitors it requires, the T/H

can exhibit settling time errors. Additionally due to the power consumption of switched capacitor network, this comparator is not chosen for the application discussed in this thesis.

3.3.3 Differential Pair Comparator (DPC)

The comparator shown in Figure 3-4 has a trip point that is set by the imbalance in currents of branches B1 and B2.

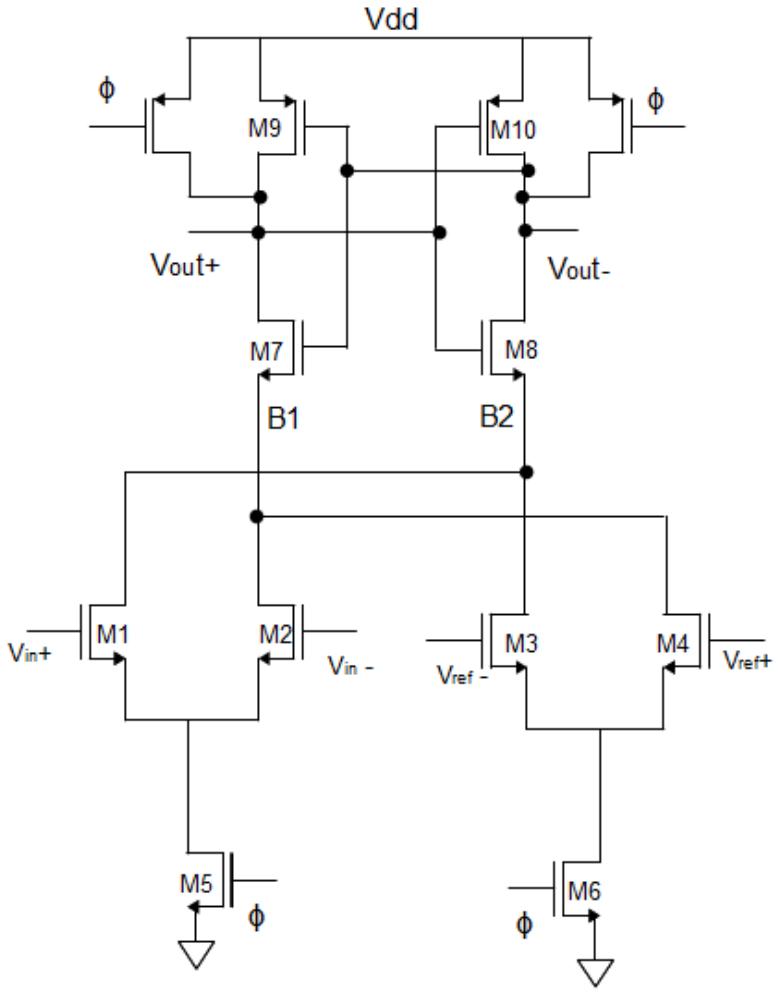

Figure 3-4. Differential Pair Comparator

The currents are controlled by the cross-coupled differential pairs with switched current sources. In the reset phase (Φ = 0), transistors M5-M6 are cutoff to

ensure no DC current flows to ground. Drain nodes Vout+ and Vout- (which are also gates of M7-M8) are pulled up to Vdd by the pull up p-channel MOSFETs (M9 and M10) forcing M7 and M8 to conduct. The drains of M5 and M6 are determined by the gate voltages of the input differential pairs. In evaluation phase (Φ = VDD) the pull up transistors are cutoff and the tail currents are turned on bringing the input differential pair transistors to saturation. M1-M4 compare (Vin+-Vin-) against (Vref+-Vref-). The trip point follows a equation

$$2\alpha k^2 I_{D6}\left(\frac{W_1}{L}\right) - \mu_n C_{ox} k^4 V_{ref}^2 \left(\frac{W_1}{L}\right)^2 = 2I_{D6}\left(\frac{W_3}{L}\right) - \mu_n C_{ox} V_{ref}^2 \left(\frac{W_3}{L}\right)^2, \qquad (3\text{-}4)$$

where $k = (\Delta V_{in})/(\Delta V_{ref})$, $\alpha = I_{D5}/I_{D6}$. $\Delta V_{ref} = (V_{ref+} - V_{ref-})$ and

$\Delta Vin = (V_{in+} - V_{in-})$.

The offset voltage follows the same equation as (3-3)

Since all the differential pair transistors are always in saturation, the offset is insensitive to device mismatch. There are several shortcomings to this design. The non-linear complex relationship between input and reference voltages makes it difficult to calculate the trip point. Another drawback is that when a large input swing is applied, one of the differential pairs will be turned off (as the input voltages are differential in nature) resulting in all the current drawn into the "turned on" pair. Hence comparison of only one set of inputs (the pair that is turned on) is made. It compares either Vin+ with Vref+ or Vin- with Vref-.

3.3.4 Modified Differential Pair Comparator:

To overcome the above shortcomings, a modified differential comparator as shown in Figure 3-5 is chosen.

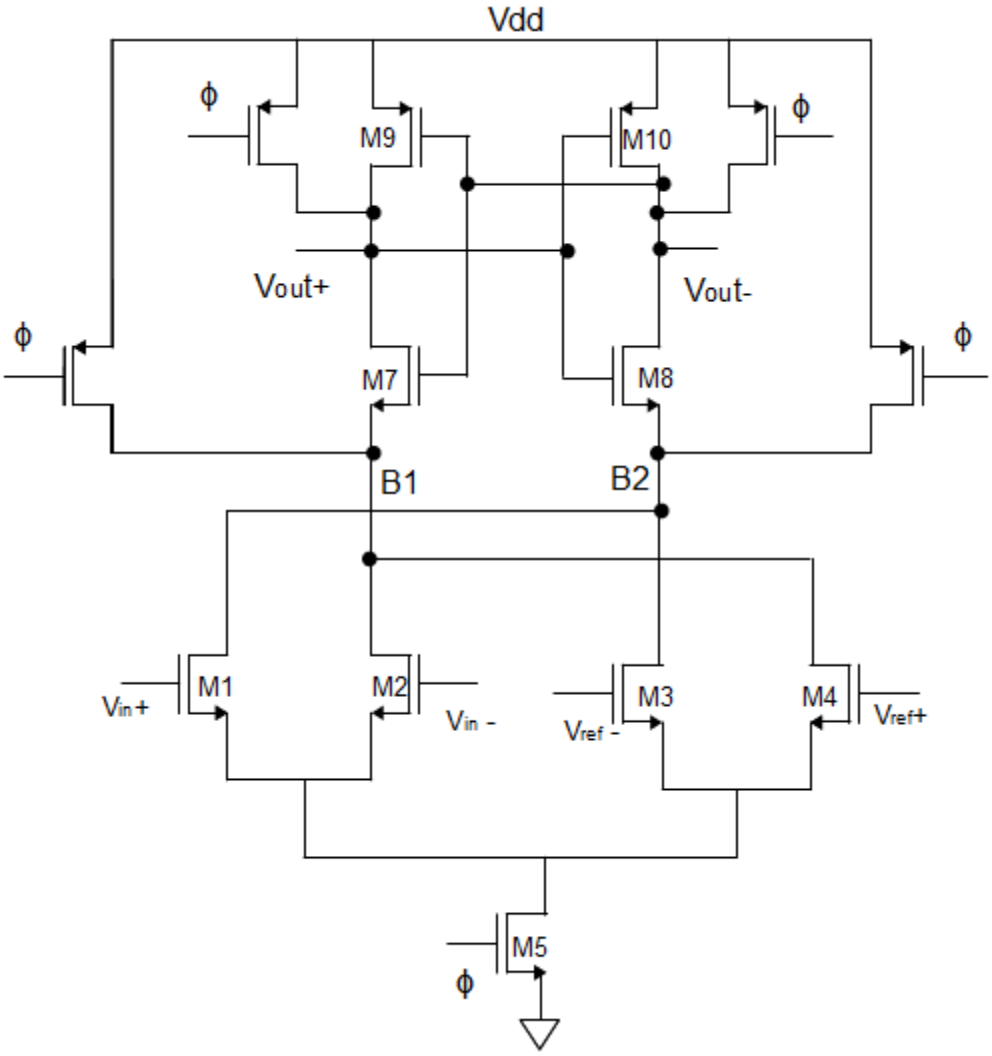

Figure 3-5. Modified Differential Pair Comparator

Combining two differential pairs under one tail current serves two purposes.

a) The new current equations for the branches B1 and B2 are

$$I_{B1}=\mu_n C_{ox}\beta_1\left(V_{in-}- V_{tn}\right)^2 + \mu_n C_{ox}\beta_2\left(V_{ref+}- V_{tn}\right)^2 \quad (3\text{-}5)$$

$$I_{B2}=\mu_n C_{ox}\beta_1\left(V_{in+}- V_{tn}\right)^2 + \mu_n C_{ox}\beta_2\left(V_{ref-}- V_{tn}\right)^2 \quad (3\text{-}6)$$

where β_1 = W2/L2 = W1/L1 and β_2 = W3/L3 = W4/L4

The trip point is caused by an imbalance in the above currents. So from the above equations, the trip point occurs when IB1 = IB2 and can be expressed as

$$V_{in+}-V_{in-}= \frac{\beta_2}{\beta_1}\left(V_{ref+}- V_{ref-}\right) \quad (3\text{-}7)$$

This trip point is similar to that of resistive divider comparator in equation (3-1) and is easy to determine.

b) Since all the transistors have the same tail current, the differential pairs M1-M2 and M3-M4 will all contribute currents for the trip point unlike the previous topology. Pull up p-channel MOSFETs are also added at B1 and B2 to remove the memory effect of the previous trip point. The offset is the lowest in in this comparator compared to all of those analyzed above, however it still follows equation (3-2).

The modified differential pair comparator is the best fit for proposed ADC application because of its low offset, low power consumption and simple trip point. Since all of the input differential pairs are in saturation, the trip point is independent of input common mode voltage, which strengthens its case for use in pipelined ADCs, where a wide range of input common mode voltages are used. However these comparators are still susceptible to offsets and kickback effects (during both reset and evaluation operation modes).

In this thesis, an architecture based on the modified differential pair comparator which overcomes the earlier short comings and also is able to operate for multi-channels without effecting other equations of the comparator is used.

The comparator used in this architecture, as shown in Figure 3-6, operates in the same way as a modified differential comparator. It operates based on two signals:

clock (Φ) and reset. Clock (Φi) and reseti together connect/disconnect latchi to (from) the common input differential pair transistors and current steering DAC.

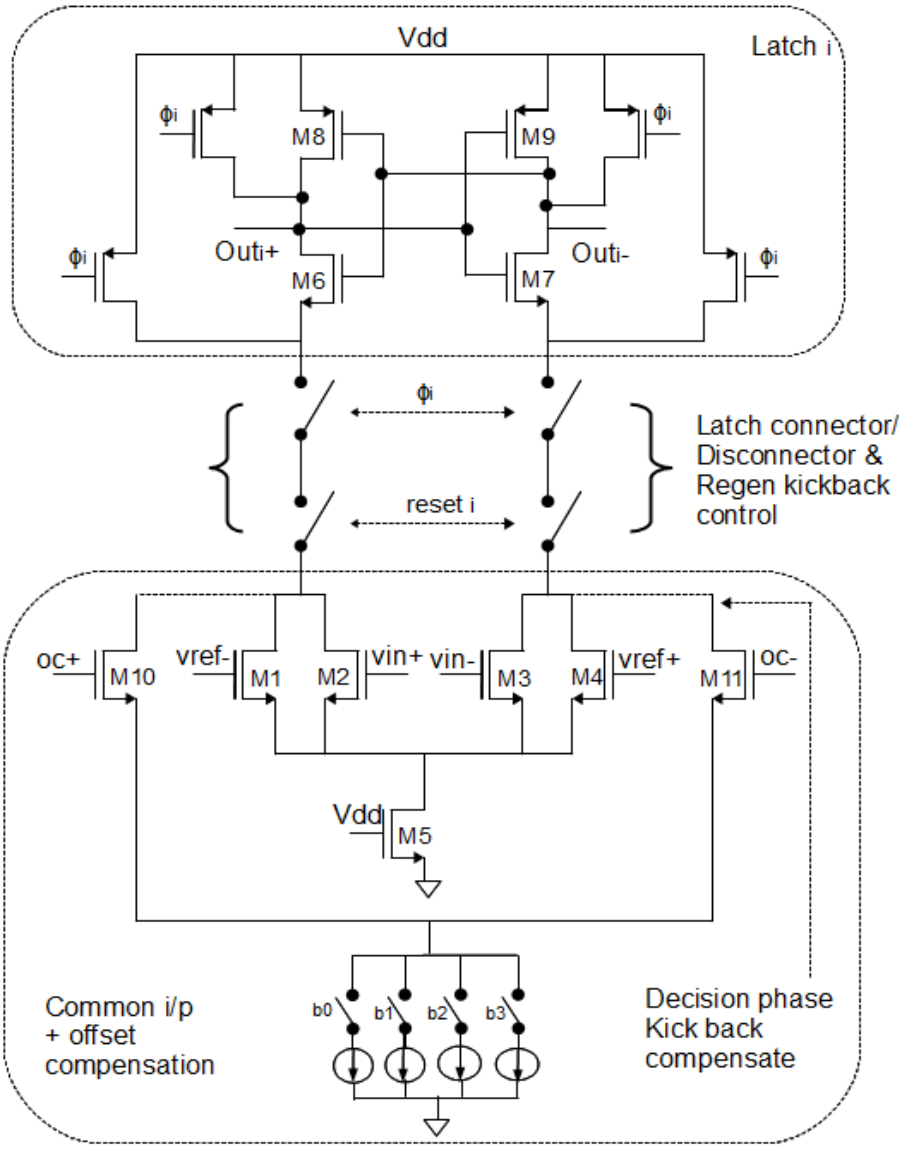

Figure 3-6. 4-Channel Modified Differential Pair Comparator

The signals Φi and reseti are chosen in such a way that during the evaluation of one channel, the other channel latches reset phases (Φ = 0, not to be confused with reset signal reseti) do not cause kickbacks [23]. The kickback effect works as shown in Figure 3-7. The input transistors and latches are designed in such a way that it has very little meta-stable delay so as to make decisions for really small input

pulse widths possible. It should be noted that the inputs to the comparator are the sampled values xn(t) from the T/H. The decisions are made for these held values with proper clock edge placements.

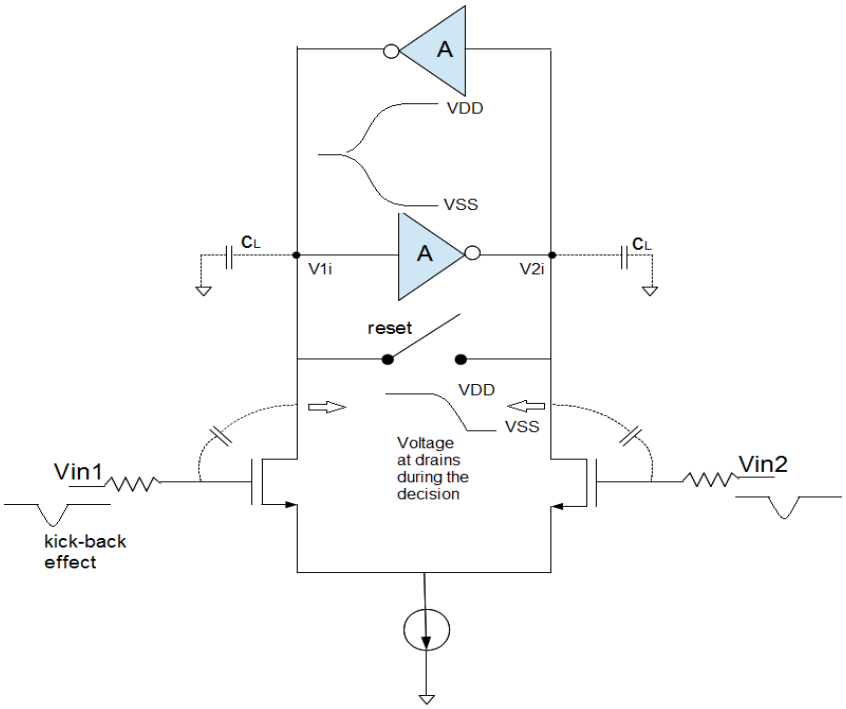

Figure 3-7. Illustration of kickback effects on to the inputs

3.3.5 Meta-Stable Delay and Offset Voltage Compensation

The meta-stable time for the above comparator is given by

$$\tau_d = \left(\frac{C_L}{A}\right)\ln\left(\frac{V_1}{V_2}\right) \qquad (3\text{-}8)$$

where C_L is the parasitic load capacitance (as shown on Figure 3-7), A is the gain of the latch, V_1 is the final voltage to be reached and V_2 is the initial voltage setup at the drains/gates. C_L and A are inversely proportional when we use minimum length transistors. As we try to increase the g_m (i.e., gain A) of the inverter by increasing its width we also increase the parasitic load capacitance. Another factor that can affect

(i.e., reduce) the meta-stable delay time is to decrease V_1/V_2 (initial voltage difference setup). This can be done by sizing up the input differential pair transistors which helps in more branch current difference ($\Delta I_B = I_{B1} - I_{B2}$). This also increases the β and hence reduces the offset voltage. The tail transistor is sized big so that the input differential pairs are brought to as close to ground as possible for large input signal swings. Hence, the bulk of the area of the comparator is in the input differential pair and tail transistors. The offset can also be calibrated post silicon with the programmable current steering DACs [26] which can draw current from either of the two branches thereby removing the current imbalance caused by mismatch and process variation.

A test bench [27] has been implemented as shown in Figure 3-8 to measure voltage offsets due to β mismatch between input pairs, latch outputs, V_T mismatch and capacitive load mismatch.

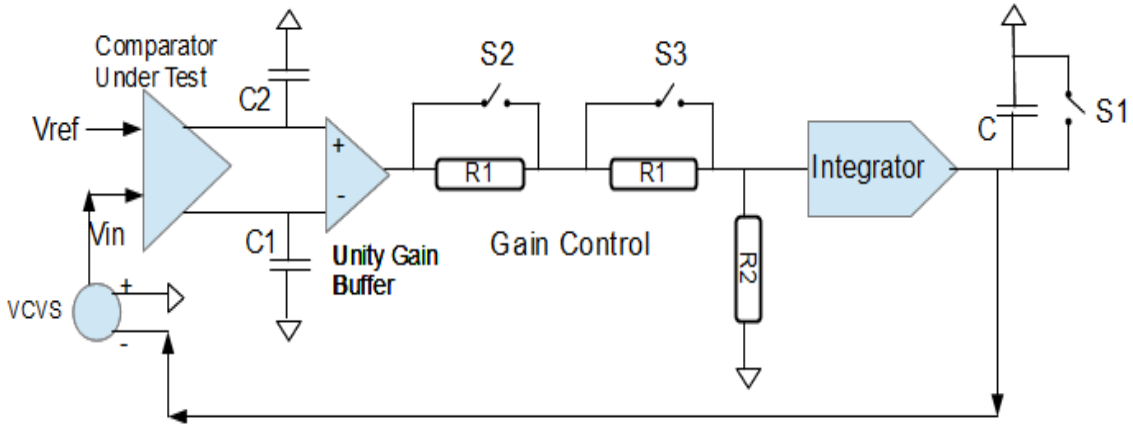

Figure 3-8. Test bench for accurate offset calculation in comparator.

In the system shown in Figure 3-8 the unity gain buffer converts the comparator's (device under test) differential output to single ended output to +V or -V. Depending on the S1 and S2 on/off state, the input voltage can be scaled from +-V to +-V(R2/(2R1 + R2)). The integrator output keeps increasing/decreasing

depending on the sign of voltage at its input. This is fed as a negative feedback to a voltage control voltage source which decreases/increases the input signal. The system comes to an equilibrium after a long time when the input voltage Vin equals the reference voltage Vref (or the number of ones and zeroes to the integrator are equal averaged over time after reaching the equilibrium point). In order to reduce this long steady state time and gain equilibrium quickly, the switch-resistor pairs have been used which provide attenuation and reduce the input swing when they opened. This attenuates the input signal to the integrator and reduces the peak to peak variations of the integrator and helps reach closer to equilibrium.

A possible worst case scenario has been calculated [22][27] for β mismatch of 3%, ΔV_T (Threshold voltage mismatch) of 10mV ΔC_L (parasitic load cap mismatch C2-C1) of 3fF (10%) and has been simulated. The worst corner output waveform as shown in Figure 3-9 showed an offset voltage of ~55mV.

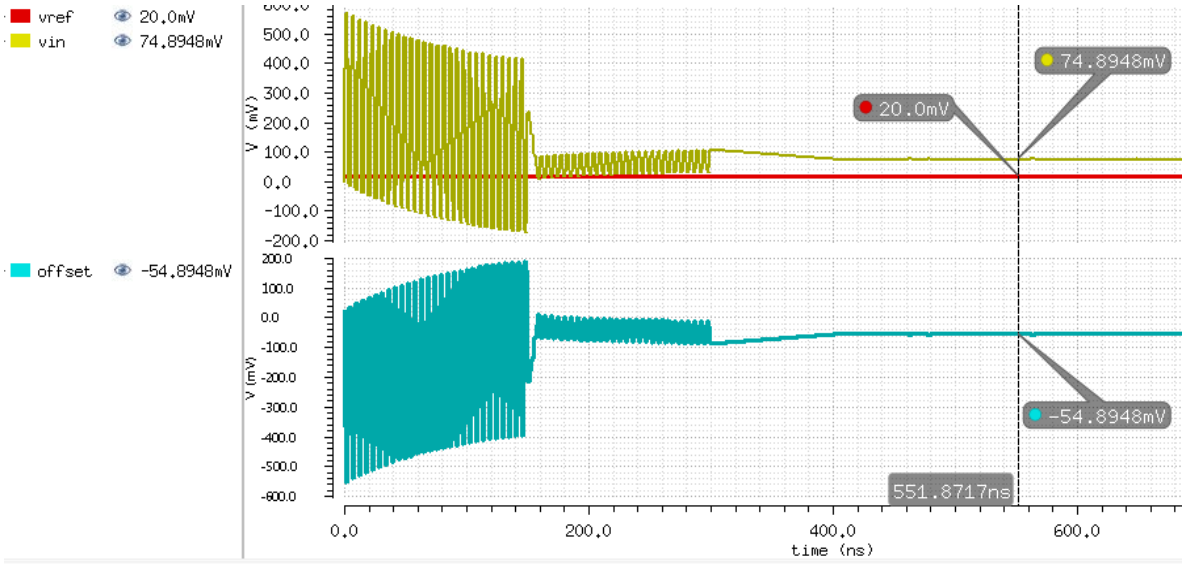

Figure 3-9. Accurate offset simulation

This test case is re-simulated with the current steering DACs turned on to compensate the offset. A simulated offset calibration is shown in Figure 3-10 which calibrates up to 3mV of resolution

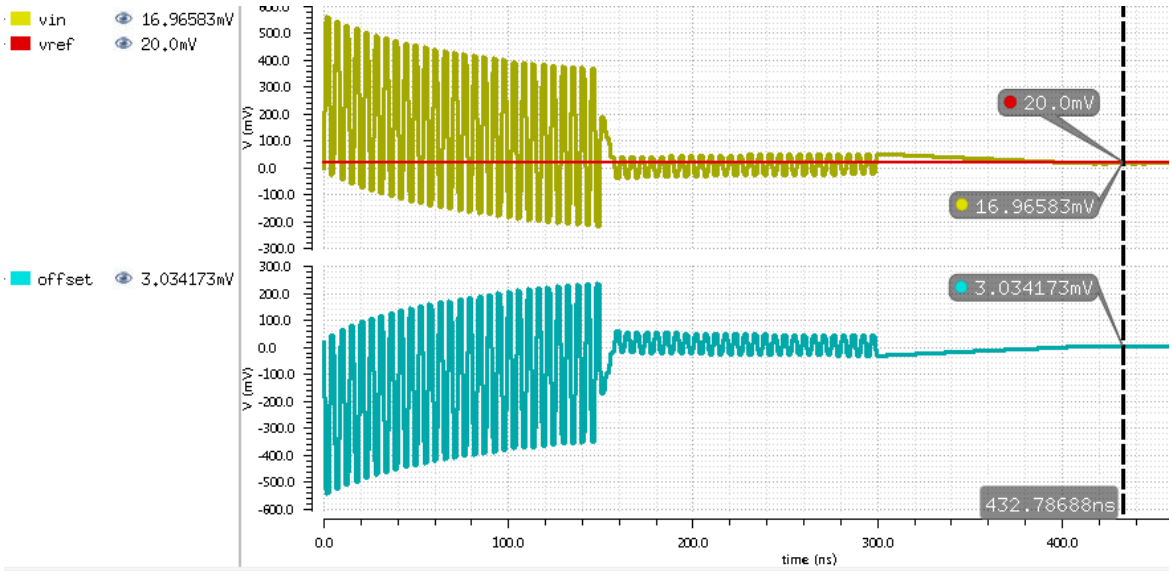

Figure 3-10. Offset Compensation using current steering DACs

3.3.6 Kickback Effects and Charge Injection and Static Timing Analysis for all Channels

The drain node voltages of the input differential pairs in Figure 3-7 come under large variations during the evaluation phase due to positive feedback of the cross-coupled latch [21][23]. These variations couple to inputs (Vin1, Vin2) through the parasitic capacitances of the input differential pair causing a disturbance called kick-back noise. This can be mitigated in two steps [21]: 1) By providing an alternate path to the current during the evaluation and 2) By disconnecting the latch from the inputs during reset phase.

In the Figure 3-6 transistors M10 and M11 provide an alternate path to the current during evaluation phase reducing the kickback effect on to the inputs during evaluation phase. Switches Φi and reseti disconnect the latch from inputs before the

reset phase protecting other channels from charge injection during reset edge (Φ = 1→0). A careful timing analysis must be done in selecting the Φi and reseti signals so that the differential pairs are always attached to the latch when the inputs are ready and detached once the evaluation phase is completed. The clock and reset timing diagrams for the four channels that use the common input differential pair are shown in Figure 3-11. These clocks are already available in the pipelined ADC as mentioned in Figure 2-10. The resets are the other four channel clocks that are not used as evaluation phases in this comparator.

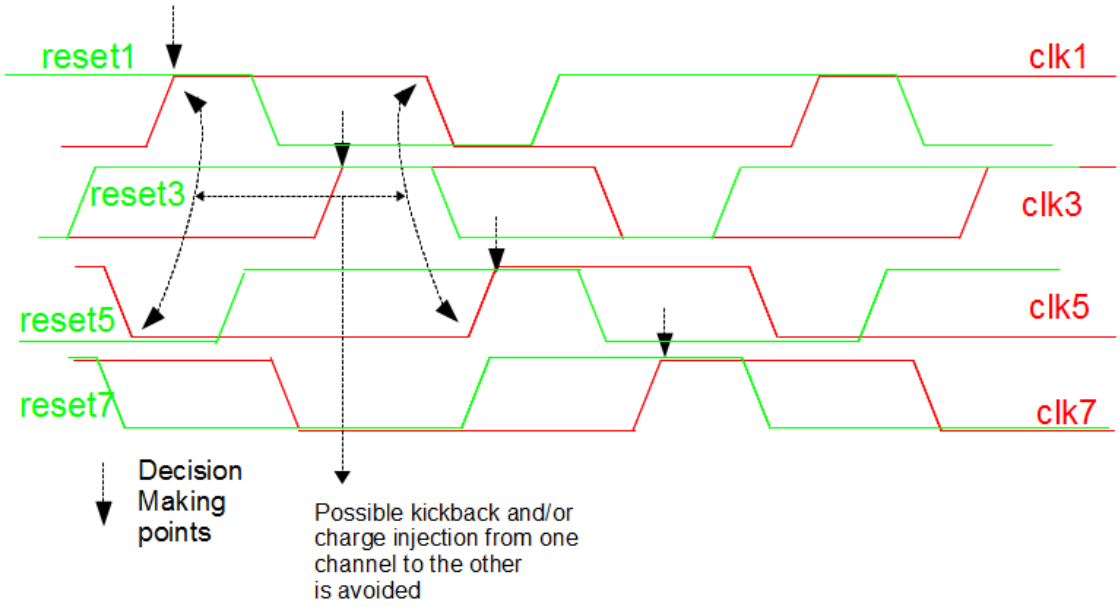

Figure 3-11. Static timing of clocks and resets

It should be noted that these combinations of resets and clocks will also avoid any static current through the tail transistor now that it is connected to Vdd unlike in previous case where it was clocked, during the reset phase of each latch.

4. 4-Channel 3-bit Sub-ADC

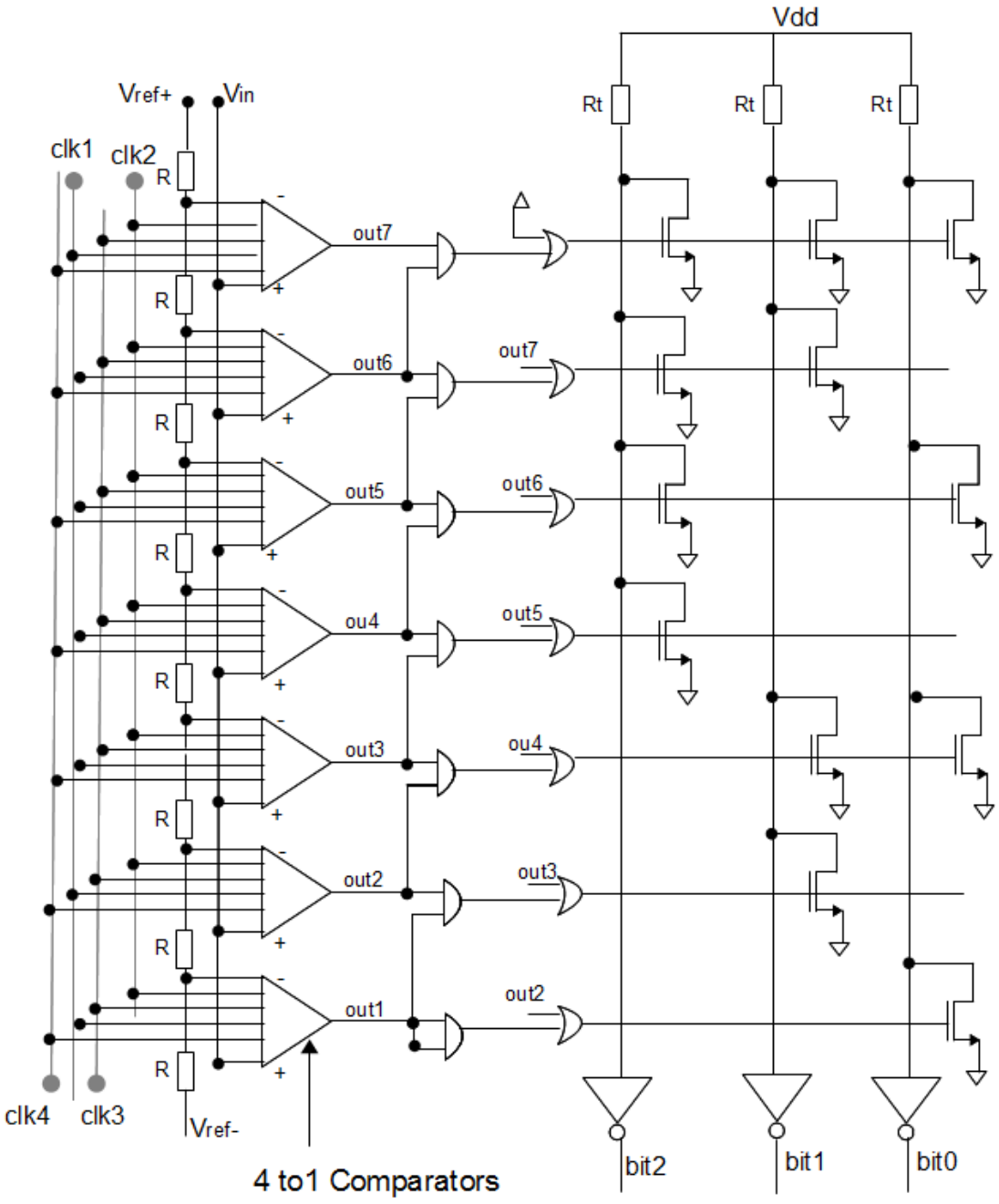

Figure 4-1. 4-Channel 3-Bit Flash ADC

Once the outputs of the comparator are de-multiplexed they are fed to 'bubble' correction combinational logic and a ROM-encoder. Bubble correction is correcting the improper bit in the thermometer code that results from a wrong decision of the comparator. The three bits of the flash ADC are passed to a set of D flip-flops which work on clocks of the respective channels so that these outputs can be fed back to their DACs for further processing down the pipeline.

5. Simulation Results and Schematics

Meta-stable Delay

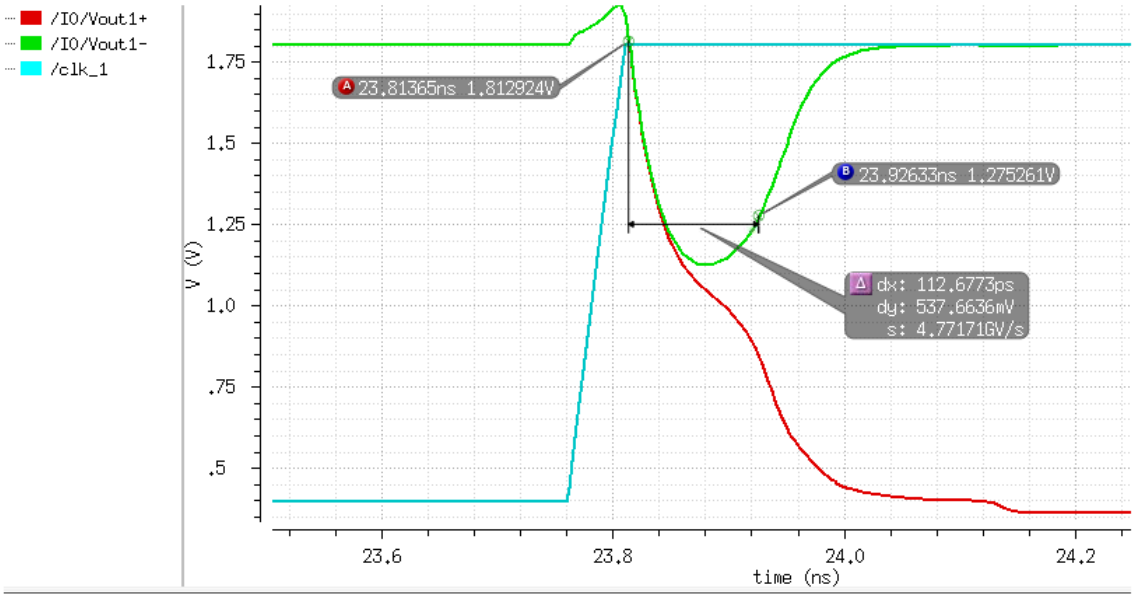

Figure 5-1. Meta-Stable Delay at ΔVo= ΔVin - ΔVref = 2mV

Table 5-1. Meta-stable delay changing over ΔVo

Delay	130.3pS	124pS	116pS	109pS
ΔV_o	2mV	10mV	25mV	50mV

As the difference in levels of comparison increases, the meta-stable delay decreases. The maximum meta-stable time of 130 pS indicates it can read pulse widths around 100pS and can be used as front end sub-ADC.

Transient Analysis of all four channels

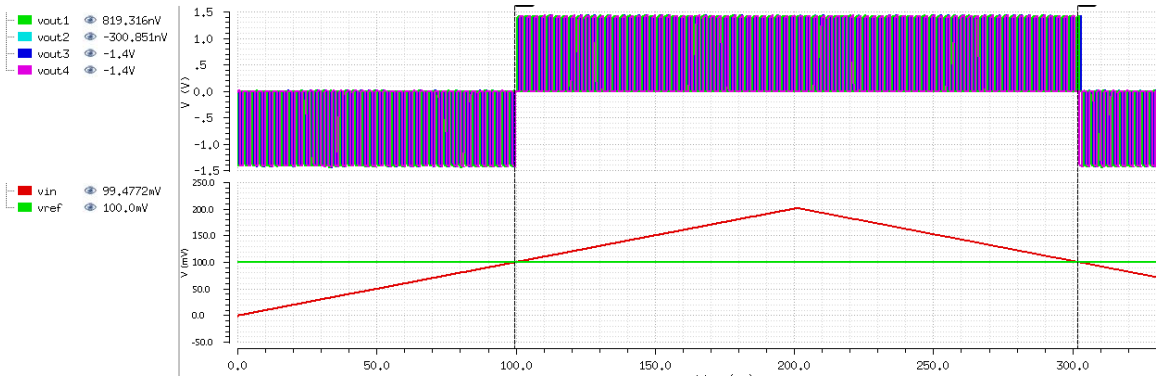

Figure 5-2. All four channels tripping at Vin = Vref for a slow input ramp from 0 to 200mV in 400 nS

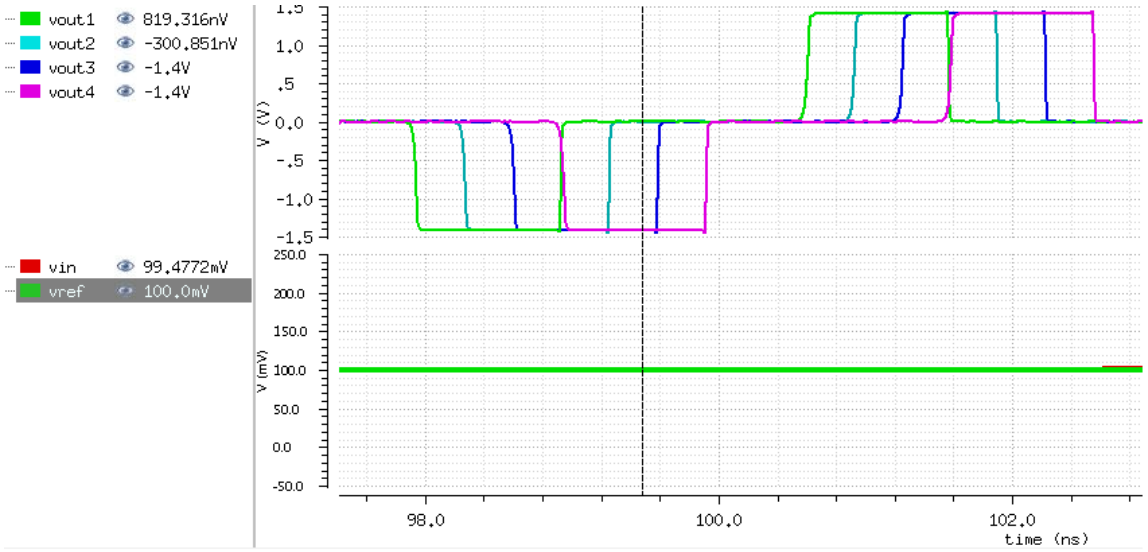

Figure 5-3. Magnified portion of the tripping point for all four channels. Note the vin and vref values at ΔVo = 522μV.

Figure 5-2 and Figure 5-3 show the tripping points (at V_{out+}) of all the comparators as the input voltage crosses the reference voltage.

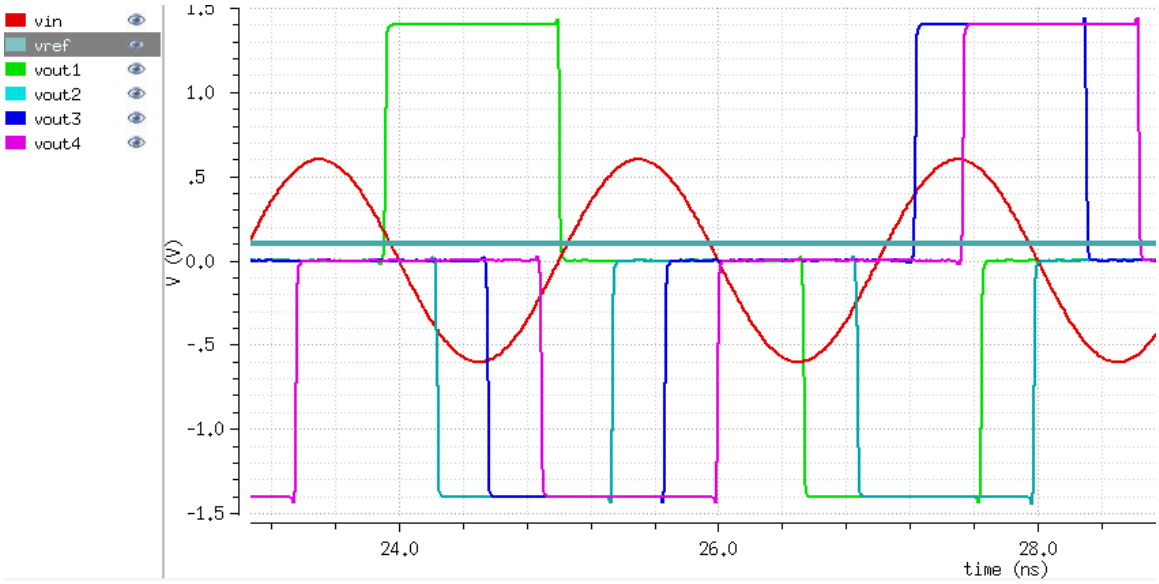

Figure 5-4. Channels Tripping for a fast moving input at 500MHz.

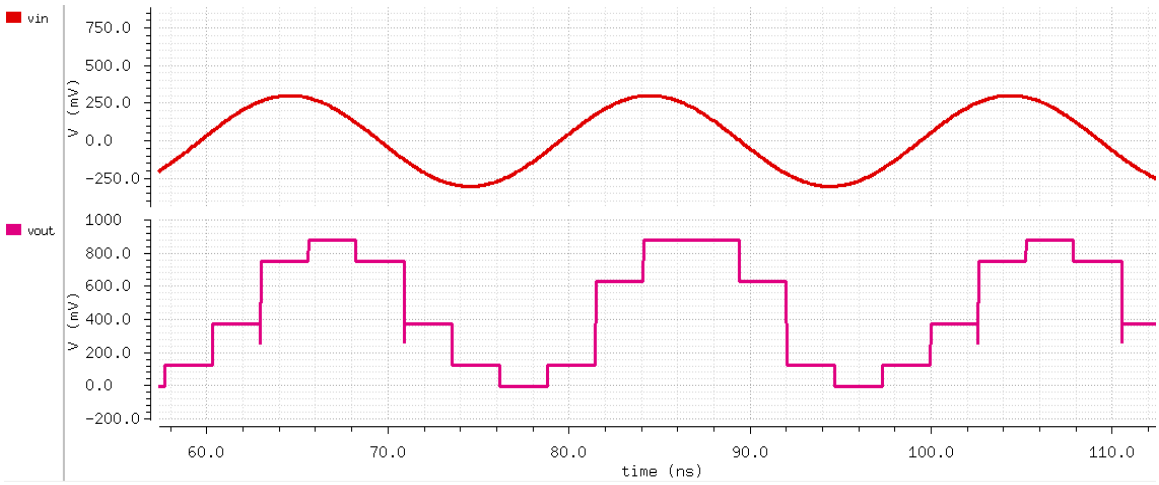

Figure 5-5. Reconstruction of a input sine wave by the 3-bit Flash ADC at F_{in} = 50.307765047364MHz

Figure 5-5 shows the Flash ADC output after reconstruction from 3-bit code. The Flash was operated at 378.78 MHz clock (2.64ns clock period).

The following plots are coherently sampled FFTs at 378.78 MS/s sampling rate and signal reconstruction.

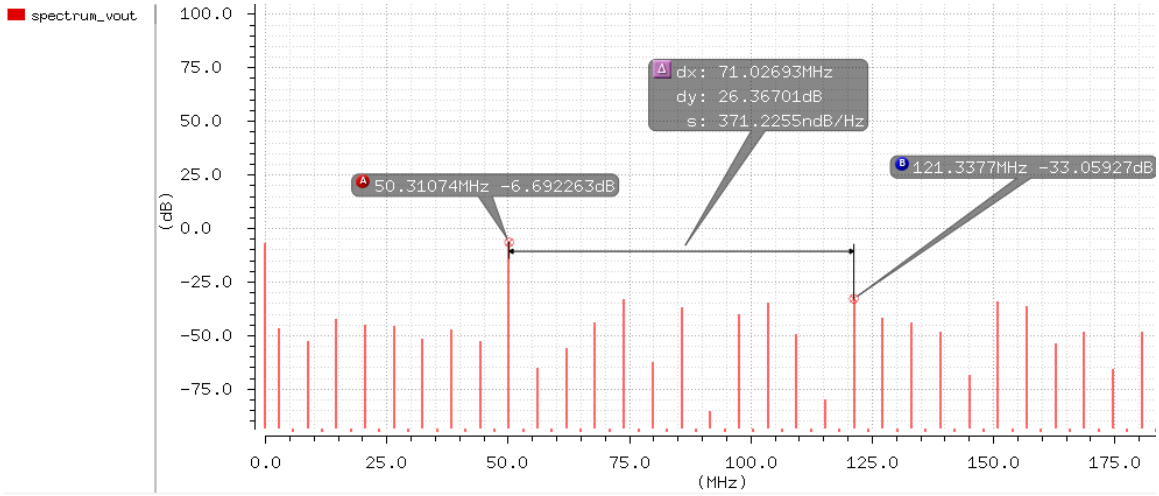

Figure 5-6. FFT of the reconstructed input sine wave by the 3-bit Flash ADC at F_{in} = 50.307765047364MHz

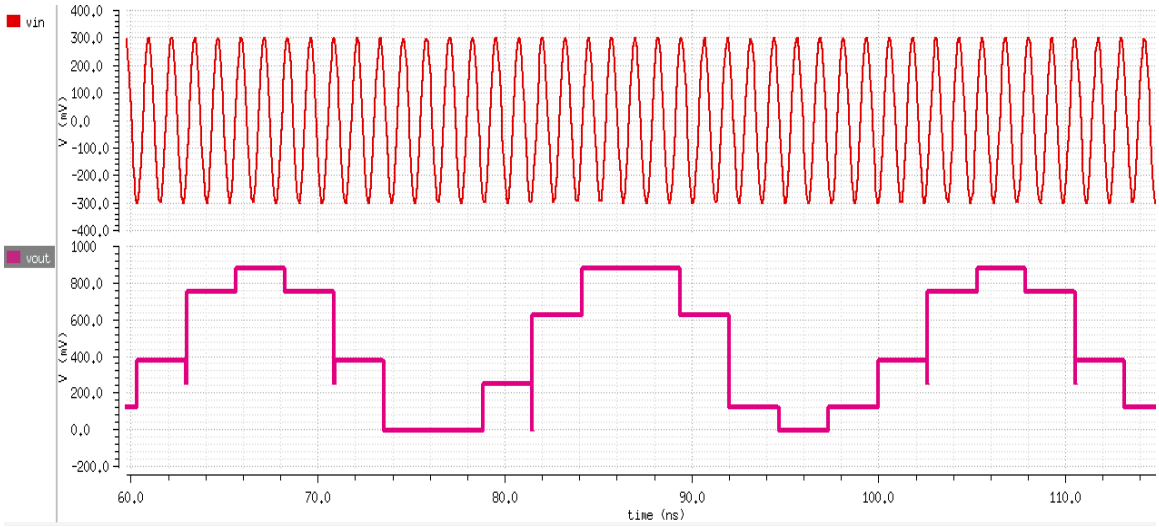

Figure 5-7. Reconstruction of a input sine wave by the 3-bit Flash ADC at F_{in} = 807.88352262312MHz sub-sampled at F_{out}= 50.307765047364MHz

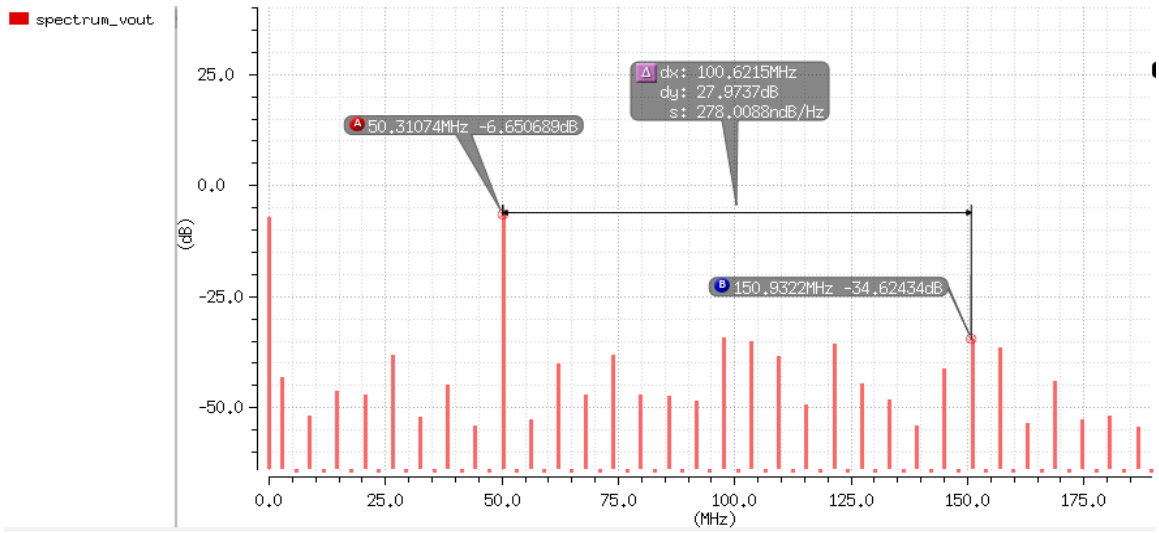

Figure 5-8. FFT of the reconstructed input sine wave by the 3-bit Flash ADC at F_{in} = 807.88352262312MHz sub-sampled at F_{out}= 50.307765047364M

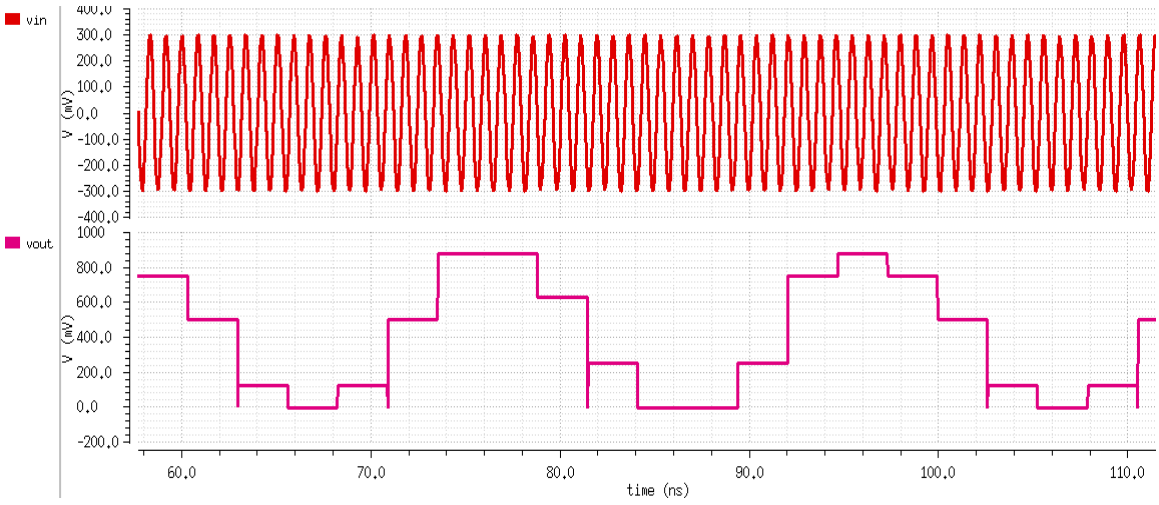

Figure 5-9. Reconstruction of a input sine wave by the 3-bit Flash ADC at F_{in} = 1.186671401411GHz sub-sampled at F_{out}= 50.307765047364MHz

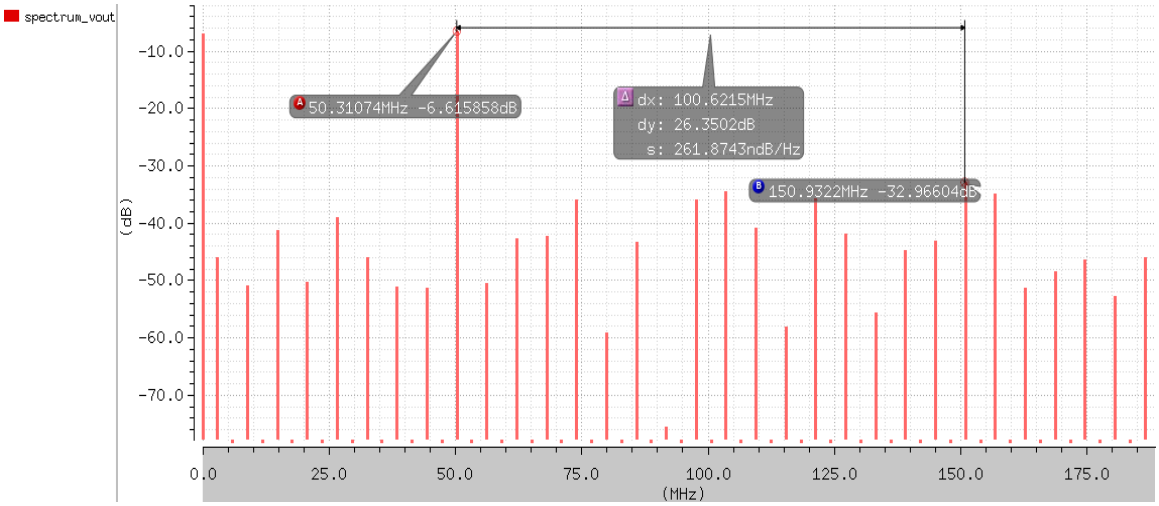

Figure 5-10. FFT of the reconstructed input sine wave by the 3-bit Flash ADC at F_{in} = 1.186671401411GHz sub-sampled at F_{out}= 50.307765047364MHz

Table 5-2. SFDR vs Input frequency for all four channels at sampling rate of f_{clk} = 378.78MHz

f_{in}	50MHz	800MHz	1.18GHz
Channel1	26.37dB	27.97dB	26.35dB
Channel2	26.42dB	28.1dB	26.38dB
Channel3	26.29dB	27.89dB	26.27dB
Channel4	26.44dB	28.11dB	26.40dB

Table 5-3. SNDR vs Input frequency for all four channels at clock sampling rate of f_{clk} = 378.78MHz

f_{in}	50MHz	800MHz	1.18GHz
Channel1	19.27dB	19.52dB	19.24dB
Channel2	19.30dB	19.53dB	19.27dB
Channel3	19.21dB	19.45dB	19.17dB
Channel4	19.33dB	19.57dB	19.31dB

The Estimated Number Of Bits (ENOB) for all the channels ranges from 2.89 bits to 2.96 bits over the range of input frequencies up to 1.2 GHz.

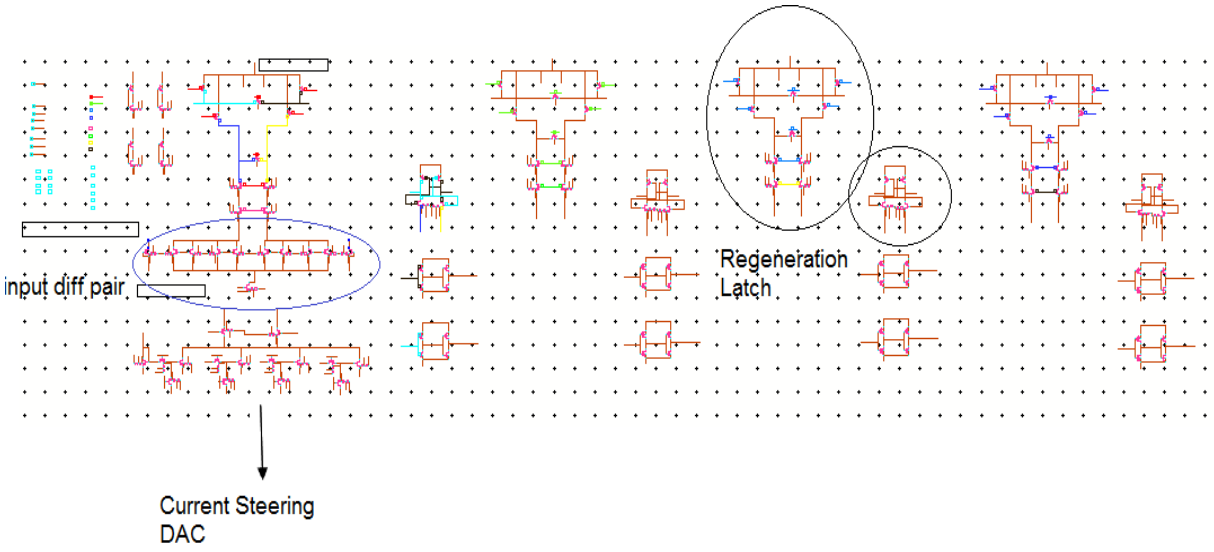

Figure 5-11. Schematic showing the comparator circuit

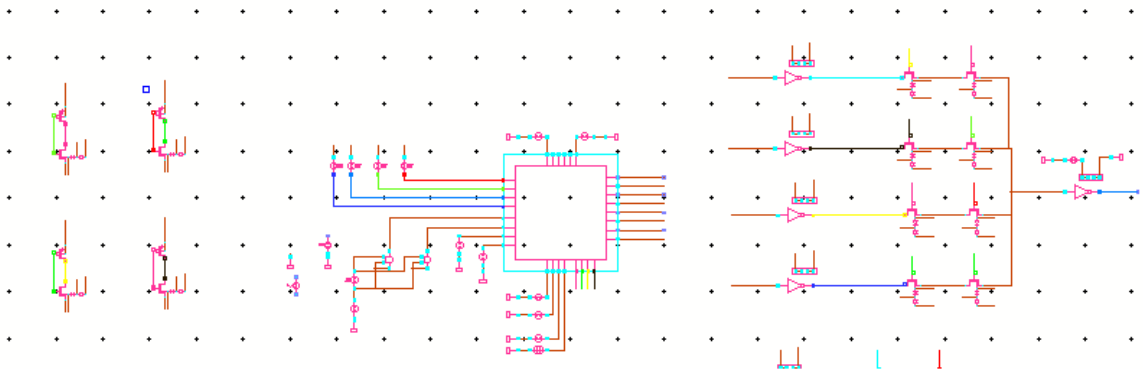

Figure 5-12. Schematics of 4-channels multiplexed onto single line

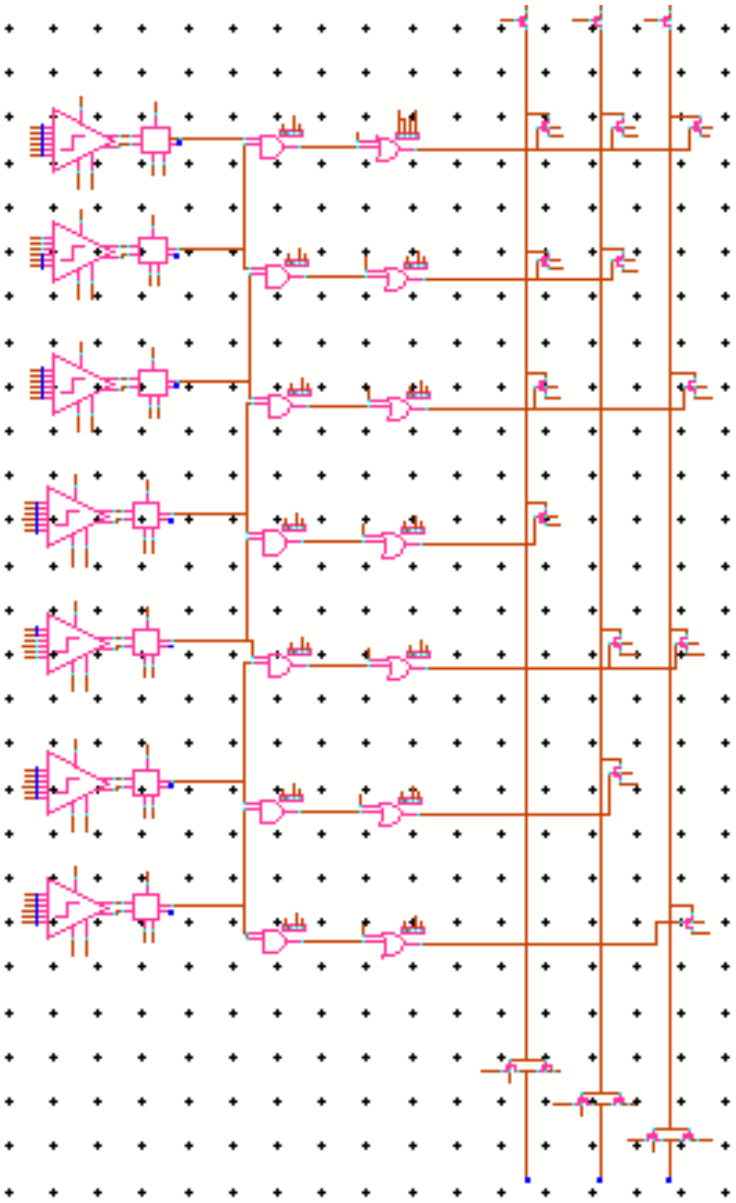

Figure 5-13. Schematic of complete 3-bit Flash with Bubble Correction and ROM encoder

Each of the comparator shown in Figure 5-14 is a 4-channel comparator that has 4:1 multiplexed output.

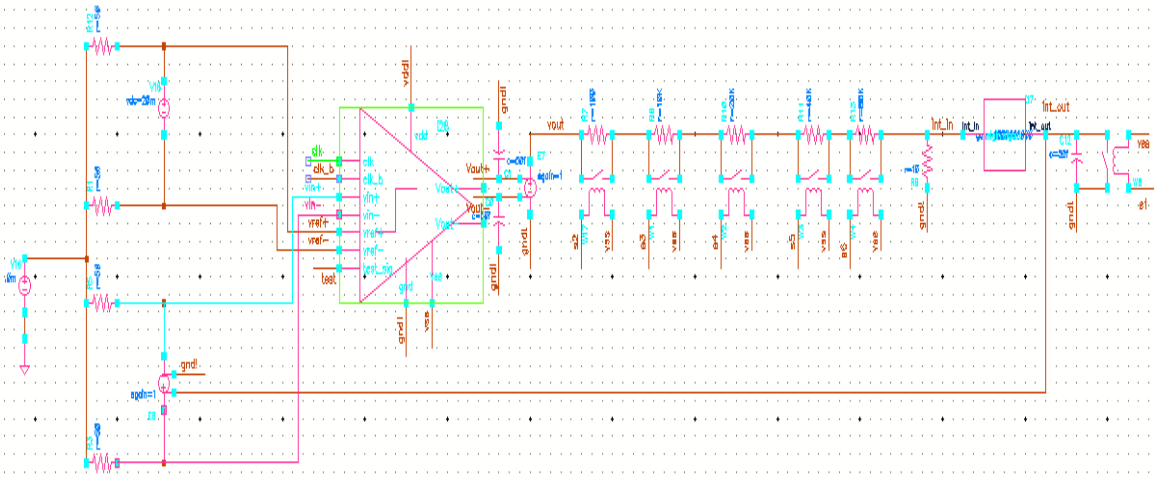

Figure 5-14. Schematic of test bench for offset measurement

Test bench using multiple gain control switch-resistor pair for better attenuation and quicker equilibrium with high accuracy.

6. Conclusion

A 2.5 bit 4-channel Flash ADC was designed and simulated in a 130 nm IBM 8HP process. The total number of comparators used were reduced from 296 to 136 effectively reducing the sub-ADC occupied area by 2.1 times (accounting for independent latches also). The input load for the T/H is reduced by a factor of four from around 2.88 pF to 0.74 pF. The power consumption is similar or less (switching power from ROM encoding saved) compared to individual channel separate sub-ADC. A new comparator that can be shared across more than two channels, without compromising on accuracy and linearity, is presented and characterized across all parameters.

The design for the comparator has been laid out and fabricated in IBM 130nm 8HP process. The chips will be tested and then the complete flash will be integrated in to the main time-interleaving Pipelined ADC. Future scope of work extends to improving the power consumption by reducing the switching activity common to multiple channels and sharing of other sub-ADC parts like DACs and their switching circuits.

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