Post processing Treatment of InGaZnO Thin Film Transistors for Improved Bias-Illumination Stress Reliability

by

Muhammad Ruhul Hasin

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Graduate Supervisory Committee:

Terry Alford, Chair
Stephen Krause
Jennifer Kitchen

ARIZONA STATE UNIVERSITY

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ABSTRACT

This thesis work mainly examined the stability and reliability issues of amorphous Indium Gallium Zinc Oxide (a-IGZO) thin film transistors under bias-illumination stress. Amorphous hydrogenated silicon has been the dominating material used in thin film transistors as a channel layer. However with the advent of modern high performance display technologies, it is required to have devices with better current carrying capability and better reproducibility. This brings the idea of new material for channel layer of these devices. Researchers have tried poly silicon materials, organic materials and amorphous mixed oxide materials as a replacement to conventional amorphous silicon layer. Due to its low price and easy manufacturing process, amorphous mixed oxide thin film transistors have become a viable option to replace the conventional ones in order to achieve high performance display circuits. But with new materials emerging, comes the challenge of reliability and stability issues associated with it. Performance measurement under bias stress and bias-illumination stress have been reported previously. This work proposes novel post processing low temperature long time annealing in optimum ambient in order to annihilate or reduce the defects and vacancies associated with amorphous material which lead to the instability or even the failure of the devices. Thin film transistors of a-IGZO has been tested for standalone illumination stress and bias-illumination stress before and after annealing. HP 4155B semiconductor parameter analyzer has been used to stress the devices and measure the output characteristics and transfer characteristics of the devices. Extra attention has been given about the effect of forming gas annealing on a-IGZO thin film. a-IGZO thin film deposited on silicon substrate has been tested for resistivity, mobility and carrier concentration before and after annealing in various ambient. Elastic Recoil Detection has been performed on

the films to measure the amount of hydrogen atoms present in the film. Moreover, the circuit parameters of the thin film transistors has been extracted to verify the physical phenomenon responsible for the instability and failure of the devices. Parameters like channel resistance, carrier mobility, power factor has been extracted and variation of these parameters has been observed before and after the stress.

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CHAPTER I

INTRODUCTION

1.1 Transparent conducting oxides for Display electronics

Since the inception of first integrated circuits in 1958, engineers and researchers are trying to make smaller devices so that they can install more functionality in a single chip. As predicted by the Moore's law, researchers built transistors which are extraordinarily small. Latest of which is only 14 nm of channel length. However, there has been a completely opposite trend for display technologies to cover larger area with circuit functionality. For different kinds of display circuits, the substrate could be glass or organic materials like Polyethylene Naphthalate (PEN) and Polyethylene Terephthalate (PET). These substrate materials have lower melting point thus requiring low temperature process to fabricate display circuits. That is why the cost of production varies significantly from the conventional integrated circuits where the substrate is crystalline silicon. Recent display technologies are dominated by all kinds of Flat panel displays (FPD) such as liquid crystal displays (LCD), plasma display panels (PDP), field emission displays (FED) and displays with organic light emitting diodes (OLED). One significant element used in these displays is transparent conducting oxide (TCO). Due to its transparency in visible region and good electrical properties, TCO has been studied and used in several optoelectronic devices. TCO can be broadly categorized in two types, which are polycrystalline oxide semiconductors (POS) and amorphous oxide semiconductors (AOS). Although polycrystalline semiconductors have higher field effect mobility, due to its grain boundaries, it lacks reproducibility and uniformity which deteriorates device characteristics. On the contrary,

amorphous oxide semiconductors have better uniformity and competitive field effect mobility compared to polycrystalline oxides when deposited at room temperature. The low temperature process of AOS is an advantage for the manufacturers due to its lower cost of production. However, many different materials and manufacturing process of AOS has been introduced over the years to meet the technological requirements. It is essential to achieve certain level of conductivity along with the desired transparency in the visible region for a particular generation of technology, which eventually dominates the fabrication process. Apart from the application in display technologies, AOSs are used in solar cells and photo-detectors as transparent electrodes. Researchers tried many materials with varying composition to achieve high optical transparency in the visible region with low enough film resistance, which requires the creation of electron degeneracy in wide gap oxides (> 3 eV) by introducing suitable dopants. As stated earlier, the process condition and deposition system dictates the characteristics of the AOS. The type of sputtering used, deposition rate, substrate temperature, reactive oxygen gas flow rates, inert gas flow rates, post deposition annealing are some of the critical process parameters to determine the AOS quality and characteristics.

1.2 Amorphous silicon thin film transistors (TFTs)

Thin film transistors (TFTs) are the most common device used in modern display technologies. Although its functionality is very similar to that of silicon field effect transistors, its structure and materials used are completely different. In TFT, gate voltage controls the conduction in the channel layer, hence creating an electrical path for the carriers to flow between the two electrodes (drain and source) through the channel layer. First large area electronics with

TFTs, used hydrogenated amorphous silicon (a-Si:H) as the channel material in 1970s [1]. Since then, researchers tried to develop a-Si:H as channel material and achieved their goal to some extent. Although latest a-Si:H has large switching ratio ($<10^6$) and low off current which is suitable for active-matrix liquid crystal displays (AMLCDs), yet it is not good enough for modern applications such as OLED or image sensor circuits. To understand the limitations of a-Si:H, it is necessary to know its properties such as electron energy band structure and carrier transportation.

Amorphous structure of a-Si:H produces three types of electron states. First of them is the band tail states. The amorphous nature of a-Si:H brings a degree of disorder in the material which causes a range of bond lengths and bond angles. That is why there is a perturbation in the energy of the bonding and anti-bonding states, causing the formation of localized 'band tail' states in the energy band diagram which extends into the band gap and decreases exponentially. The width of this tail is known as Urbach energy [2]. This band tail actually represents the weak bond states in the energy band diagram. Electrons localized near these weak bonds may tunnel from one localized state to another. This process is called band tail hopping.

Secondly, there are a lot of dangling bonds in the a-Si, typically 10^{20} cm^{-3}. These dangling bond defects introduces states deep inside the band gap. The conduction mechanism of these states depends on temperature and position of the Fermi level. Typically at low temperatures, an electron at a localized dangling bond defect site just below the Fermi level may tunnel into an unoccupied localized defect state just above the Fermi level which is in close

proximity to the first state, upon the application of an electric field. However, the introduction of hydrogen can reduce the dangling bond density to as low as 10^{16} cm^{-3}. Hydrogen occupies the defects by forming an Si-H bond there [3]. Moreover, it reduces the local stress in the network thereby lowering the number of weaker bond in the layer [4]. The deposition temperature is the main parameter that controls the amount of hydrogen in a-Si:H. Typically, the higher the substrate temperature is, the lower is the hydrogen content in the a-Si:H. The third type of electron state is the extended conduction and valence band states produced by the tetrahedral network. Conduction in these states happen at elevated temperature (above 500 K). Here the carriers are not bounded to the local defect states or weak bonds, rather they move through the periodic potential of the tetrahedral silicon network [5].

However, the major drawback of a-Si:H based TFTs is its bias induced instability which affects both the threshold voltage and subthreshold swing. There are two major mechanism that explains this bias induced instability [6-7]. Firstly, the trapping of carriers in the gate insulator upon the application of gate bias for a longer period of time. This deteriorates as the bias stress time increases. Gate dielectric with higher density of defects, facilitates this phenomenon. Electrons are captured at the interfacial states at the a-Si:H/dielectric boundary, later on moves onto the deeper energy states inside the dielectric by variable-range hopping [6] or through a multiple-trapping and emission process [8-10]. Second one is the defect creation in the channel layer of the TFT [11]. Application of positive bias on the gate, causes electrons from the regular silicon network to occupy tail states near the channel/dielectric interface. As these electrons break away from the silicon network, it creates silicon dangling bonds or deep state defects in the

channel layer [12-13]. Later on, these deep state defects hurts the carrier conduction through the channel layer. Both the charge trapping and defect creation mechanism affects the threshold voltage of the TFTs. The charge trapping phenomenon dominates at the high bias voltage and longer stress time but defect creation mechanism dominates at lower bias voltage for smaller stress time. So the quality of a-Si:H film and a-Si:H/dielectric interface has a direct impact on the overall TFT performance. If the fabrication is done at low temperature ($\leq 150^{o}$ C), there is significant amount of charge trapping in the dielectric which causes large threshold voltage shift of the TFTs. As modern technologies require TFTs to be fabricated on flexible substrate like PEN, these TFTs cannot be fabricated at higher temperature than 150°C. This is because the flexible substrates has lower melting point. As a result it is very tough to fabricate TFTs without larger threshold voltage shift using a-Si:H as the channel material. For classical applications such as AMLCD, threshold voltage shift can be tolerated but it is not the same for applications like active matrix organic light emitting diode (AMOLED). Apart from the instability, modern technologies require higher carrier mobility which is also a deterrent towards the usage of a-Si:H as a channel material for TFTs [14]. Because of all these issues, researchers came up with solutions to these problems in the form of amorphous mixed oxide based TFTs. Next section discusses the advantages of amorphous mixed oxides over amorphous hydrogenated silicon as a channel material.

1.3 Conduction mechanism in Amorphous oxide semiconductors

The conduction mechanism in Amorphous oxide semiconductors is different from the usual semiconductors. Researchers tried to find a material which would be amorphous in nature

and also exhibit higher carrier mobility to realize many complex applications [15-17]. In 1996 Hosono *et al.* proposed a hypothesis for finding amorphous wide band gap oxide semiconductor which would have higher carrier mobility compared to the conventional covalent semiconductors like silicon [18]. In silicon the bottom of the conduction band is formed by the highly directional sp^3 hybrid orbital. Mobility of these types of semiconductors directly depends upon the amount of overlap exists between the sp^3 hybrid orbital of neighboring atoms. However, in oxide semiconductors the valence shell of the metal cation forms the conduction band of the semiconductor. If suitable metal cation is chosen, then it have larger spherical s orbital for faster conduction mechanism. It is evident from figure 1.1, for covalent semiconductors like silicon, the mobility suffers significantly for amorphous state compared to that of crystalline.

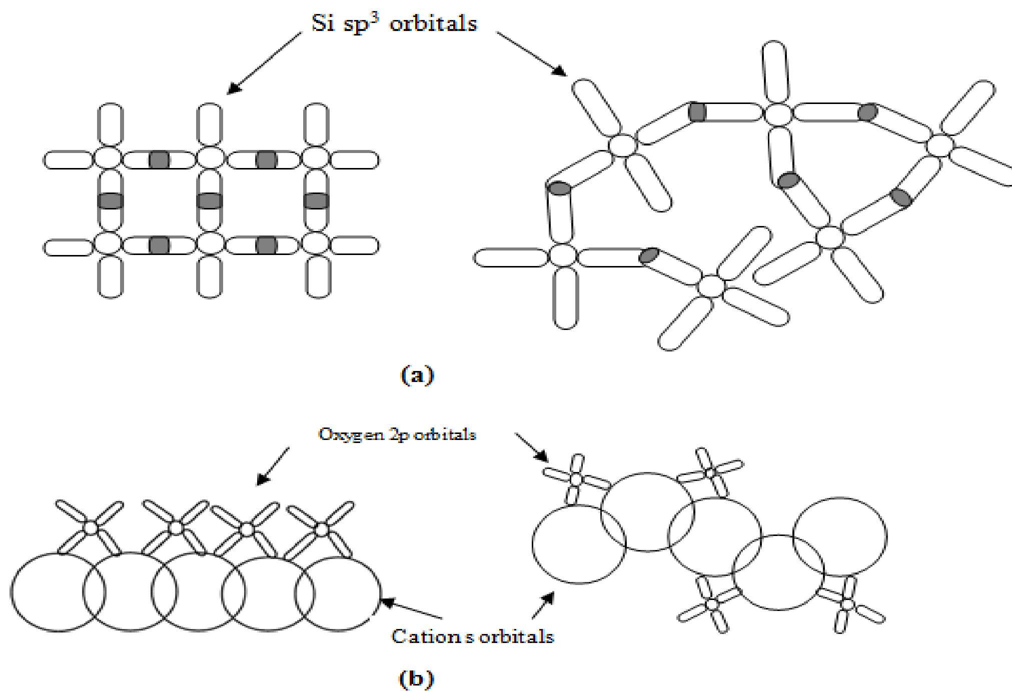


Figure 1.1 Orbital schematic of conduction band minimum (CBM) in (a) Si (b) oxide semiconductors in crystalline phase and amorphous phase

This is so because, there is little overlap between the sp^3 orbitals which causes the electrons to transport through hopping, affecting the overall mobility. Contrary to that, the large isotrophic spherical orbitals in oxide based semiconductors provide enough overlap between neighboring atoms irrespective of the bonding angles which gives similar mobility for both amorphous and crystalline states. Regarding the choice of material, Hosono *et al.* proposed to use heavy metal cations (HMCs) that have an electronic configuration of $(n-1)d^{10}\ ns^0$ where $4 \leq n \leq 6$ [19-20]. It was also suggested to use double oxides instead of single oxides, to confirm the formation of an amorphous film.

1.4 Amorphous Indium Gallium Zinc Oxide (a-IGZO)

As mentioned in the earlier section, amorphous mixed oxide based TFTs can provide high mobility as the larger spherical s orbit of the cation is conducive to higher mobility irrespective of the bonding angles. But this new material should have few qualities in it, which are (1) it must be able to form a stable and uniform amorphous phase (2) it must have a high carrier mobility (3) it must be able to form uniform films at low temperatures (4) carrier concentration must be controllable at low levels ($< 10^{15}$ cm^{-3}), with good stability and reproducibility to control device characteristics such as threshold voltage and off current [21] (5) it must not have uncontrollable higher carrier concentration ($> 10^{17}$ cm^{-3}) as some oxide semiconductors has easy formation of oxygen vacancy which leads to excess carrier concentration. To meet these requirements, researchers tried many different materials. To have a material with high carrier mobility, it is necessary to form a dispersed conduction band minimum (CBM) which could be achieved by incorporating unoccupied metal ns orbital with large

principal quantum number (n > 4) [19-21]. That is why Zinc Oxide (ZnO) is used in these types of compound materials. Moreover, to suppress the formation of excess oxygen vacancies, stronger metal-oxygen bonds are used [22]. So metals like Gallium and Aluminum are introduced to create Ga-O and Al-O bonds. These requirements and findings actually lead researchers to try Indium Gallium Zinc Oxide (IGZO) as a channel material for TFTs.

Table 1.1 Comparison between a-Si:H, LTPS and a-IGZO

TFT channel material	a-Si:H	Low temperature poly silicon (LTPS)	a-IGZO
Field effect mobility ($cm^2V^{-1}s^{-1}$)	~1	~100	> 10
TFT uniformity	Good	Poor	Good
Fabrication cost	Low	High	Low
Yield	High	Low	High
Processing temperature	~250° C	> 250° C	Room temperature (RT) ~ 360° C
Electrical stability	Poor	Good	Good in dark
Optical stability	Poor	Poor	Good
On-off current ratio	< 10^{-7} A	< 10^{-7} A	10^{-8} A
Visible transparency	Poor	Poor	~ 80 %
Number of mask	4-5	5-12	5-6
Pixel circuit	1T + 1C	5T + 2C	2T + 1C
Pixel TFT	nMOS	CMOS	nMOS
Generation	8G	4G	8G

In 2004 Nomura *et al.* [22], first introduced amorphous IGZO as a channel material for TFTs. Theses TFTs showed better performance than a-Si:H TFTs, its mobility was more than 10 $cm^2V^{-1}s^{-1}$, which provides an opportunity to use these TFTs in big size high resolution active matrix display. Later on Mativenga *et al.* [23] introduced higher operating frequency (94.8 kHz) of a-IGZO TFT based ring oscillator on polymide substrate. a-IGZO naturally generates n-type

carrier concentration, that is why it is not require to have any extra doping process to generate free carriers. This is an added advantage of a-IGZO over other possible options. The reason behind this n type carrier concentration, has been found to be due to the native point defects. Researchers tried to find out the origin of this defects to better understand the material and control its conductivity for different types of application. Chris G. Van de Wall [24] explained that the Hydrogen molecule acts as a donor origin because of its lower formation energy, but Stephan Lany and Alex Zunger [25] argued that Oxygen is the main donor in metal oxide semiconductors. Since then many research has been done to study many properties of a-IGZO. It has been tested with bias stress, illumination stress, kinetic stress and mechanical stress to understand the stability issues which is the key factor in many applications. Table 1.1 shows a comparative study of a-IGZO with other materials.

1.5 Thesis Outline

This thesis starts with a little background of different types of TFTs and advantages of a-IGZO TFTs over others. Chapter I basically discusses the advent of amorphous mixed oxide semiconductor in TFTs. Then Chapter II deals with stability issues of a-IGZO as a channel material for inverted staggered TFTs. This chapter shows the TFT stability issues when subjected to bias, illumination and combined stress condition. Then it also shows a way to solve these issues using post fabrication processing steps. Later on Chapter III discusses the role of hydrogen atom in a-IGZO film as a compensating donor. Forming gas annealing showed improved stability and reliability of a-IGZO TFTs. This makes it interesting to study the effect of hydrogen atoms in a-IGZO thin film. This chapter analyzes the impact of hydrogen atom on parameters

like film resistivity, mobility and carrier concentration. Then Chapter IV discusses the effect of standalone illumination and bias-illumination stress on the circuit parameters of the TFTs. It shows the variation of extracted parameters such as channel resistance, threshold voltage and power factor. Finally this thesis ends with a comprehensive summary of the complete work in Chapter V.

CHAPTER II

CONTROLLED POST FABRICATION PROCESSING OF a-IGZO THIN FILM TRANSISTORS FOR IMPROVED BIAS-ILLUMINATION STRESS RELIABILITY

2.1 Introduction

Thin film transistors (TFTs) are essential building block for liquid crystal display (LCD), organic light emitting diode (OLED) or X-ray image sensors. All these applications require high mobility, fast switching operation and high I_{on}/I_{off} ratio [21]. Amorphous hydrogenated silicon (a-Si:H) TFTs has been the leading device for these types of applications, but new generations of these technologies require higher mobility, low temperature fabrication process with improved stability. Moreover, these a-Si:H TFTs had stability issues for slightly longer bias or illumination stress. These stability issues would lead to threshold voltage shift or varied subthreshold swing, which is not suitable for many modern applications. All of these issues actually led to the introduction of Metal Oxide TFTs (MOTFTs) [26-30]. MOTFTs has been extensively investigated to meet requirements of modern applications. However, the instability of the MOTFTs under prolonged stressed condition is a genuine concern. A lot of work has been done to improve the stability when MOTFTs are subjected to prolonged bias stress [31-32] and MOTFTs showed improved performance at prolonged bias stress condition. But it is required to put the MOTFTs under practical stress condition which is the combined effect of bias and illumination stress, to understand the reliability issues completely. Effect of illumination from ultra violet light sources has been studied but it is critical to study the effect of photonic energies within the visible spectrum. Because the TFTs would experience prolonged stress under

backlight illumination in practical conditions. This study investigates the reason behind instability in a-IGZO TFTs under combined stress condition and performs post fabrication steps to improve the device reliability.

2.2 Fabrication And Experimental Technique

TFTs used in the experiments are bottom gate staggered n-type IGZO based enhancement mode devices. Its cross section is shown in figure 2.1. It is fabricated on 300 mm silicon wafer with a very thin layer of SiN on the wafer. Molybdenum (Mo) of 150 nm is DC sputtered as a gate electrode followed by SiOx of 200 nm to form the gate dielectric after pattering gate electrode. Following that 50 nm thick IGZO channel is deposited using a RF sputter system. Target for sputter system is, 99.99% pure $InGaZnO_4$ which is sputtered at RF power of 100 W with a chamber pressure of 10 mTorr at 80° C. After patterning the channel region, SiOx is deposited as inter metal dielectric (IMD) at 180° C.

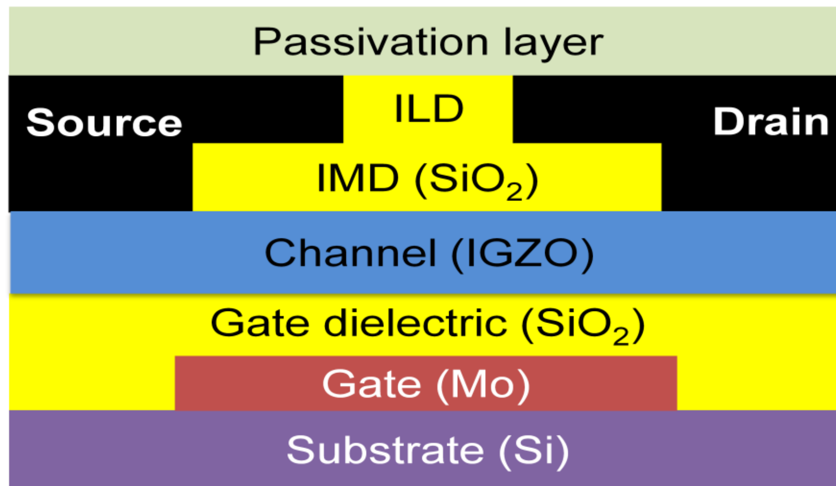


Figure 2.1 a-IGZO TFT cross section

Then Mo is sputtered to form drain and source electrodes followed by a layer of SiOx to form a transistor of W/L ratio. Finally, SiN is deposited as a passivation layer. This passivation layer have a great positive impact on the reliability of the TFTs which will be discussed soon. TFTs fabricated from low temperature processes, have high density of defects and trap states in the dielectric and channel region which eventually causes performance degradation or device failure under different kinds of stresses. An HP 4155B semiconductor parameter analyzer has been used to measure output characteristics and transfer characteristics of the TFTs to determine performance under different stress conditions. TFTs used for this investigation has W/L ratio of 9 µm/9µm. Gate voltage was swept from -20 V to +20 V with 10 V of drain bias while source was grounded to measure transfer characteristics. The output characteristics were also extracted by sweeping the drain from 0 to 20 V, for gate voltages of -5 V to 20 V in steps of 5 V and the threshold voltages for each of the stress conditions were verified from the *turn on* voltages observed from the transfer characteristics. For practical stress condition, both bias and illumination stressing has been done simultaneously. Gate voltage of ± 20V has been applied for extended period of time with 0 V drain voltage along with illumination stressing using a Dolan Jenner Fiber Lite Illuminator with a dual gooseneck optical cable attachment, which has been used to generate white light. The illuminator consisted of an EKE quartz halogen lamp which could generate white light of different intensities with a rheostat control to tune the intensity of the light source. Optical Filters were used to generate lights having wavelength of 410, 467, 532 and 632 nm from the white light to stress the TFTs. Transistors were stressed up to 25k seconds to determine the reasons behind instabilities. Since red light from the lamp source had the highest intensity in the visible region as seen in figure 2.2, tests conducted during illumination using

other wavelength filters, were done with concurrent normalization of the intensity using the rheostat. Finally post processing annealing in various ambient has been done to reduce defects and trap states and improve the performance of the TFTs.

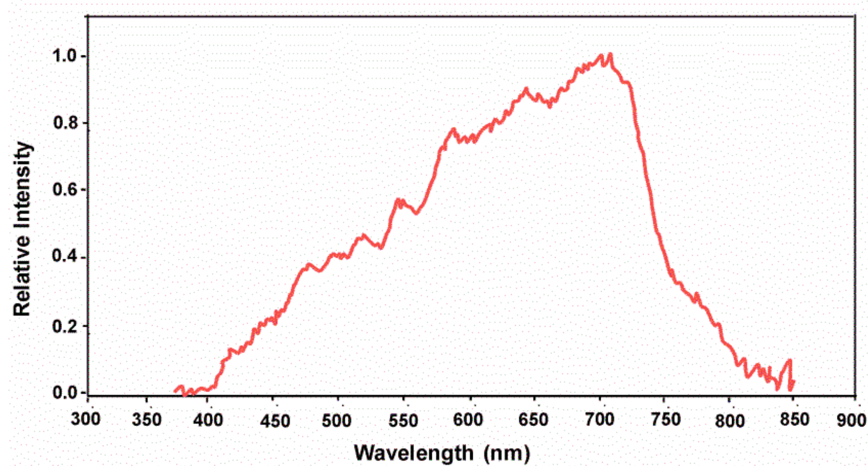


Figure 2.2 Spectrum of a standard EKE 3200 lamp source used for illumination

2.3 Standalone Bias Stress

It is critical to analyze the effect of standalone bias stress on TFTs, to fully understand the effect and reason behind instability while subjected to both bias and illumination stress simultaneously. Rajitha *et al*. reported that the results vary from the earlier results found in the literature for bias stress on Indium Zinc Oxide (IZO) based TFTs [33-35]. When subjected to -20 V gate stress, for both +20 V and 0 V drain voltage, a minor positive shift in the threshold voltage is found instead of a negative shift. This phenomenon is observed because electrons repelled from the channel, get trapped in IMD SiO_x. Earlier studies observed negative shift in the threshold voltage because, holes used to get trapped in the gate dielectric which has limited possibility in this particular case. However, the larger shift is observed when TFTs are put under

positive gate bias stress. For +20 V of gate voltage with 0 V and 10 V drain voltage, TFTs experience significant positive shift in threshold voltage. This suggest that there are trapped electrons in the gate dielectric as electrons are attracted by +20 V at the gate. But this is not the main reason for this phenomenon, rather the continuous creation of trap states in the channel region is [32, 33, 36]. No device failure has been observed even after 10^5 seconds of bias stress. Figure 2.3 shows the transfer characteristics of the TFTs for ± 20 V bias stress after 10^5 seconds.

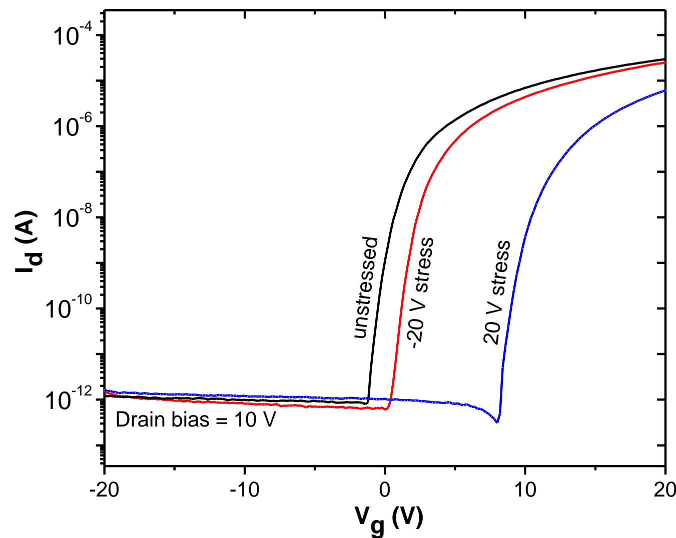


Figure 2.3 a-IGZO TFT under Vg= ± 20 V, Vd=0 V bias stress for 100,000 seconds

2.4 Standalone Illumination Stress

Standalone illumination stress testing has been done with the light wavelengths of 410 nm, 467 nm, 532 nm and 632 nm for 25,000 seconds with an intensity of 0.5 W/cm^2. The reported results demonstrate a greater negative shift in threshold voltage, for light of shorter wavelength [37]. Illumination with light of 632 nm wavelength, resulted in little to no shift in transfer characteristics which could be attributed to phenomena such as state creation or charge

trapping. As the wavelength of light used is reduced, a considerable threshold voltage shift is noticed, making the *turn on* voltage smaller, as shown in figure 2.4. Earlier studies showed that Ultra-violet (UV) light is capable of producing band-to-band transitions [38] and the negative V_t shift observed in this study can also be attributed to a similar effect. The photonic energies of 3.02, 2.66, 2.33, and 1.96 eV correspond to the shortest to longest wavelengths in this study. With the exception of the longest wavelength, all of the other cases have displayed a similar phenomenon as that of UV light.

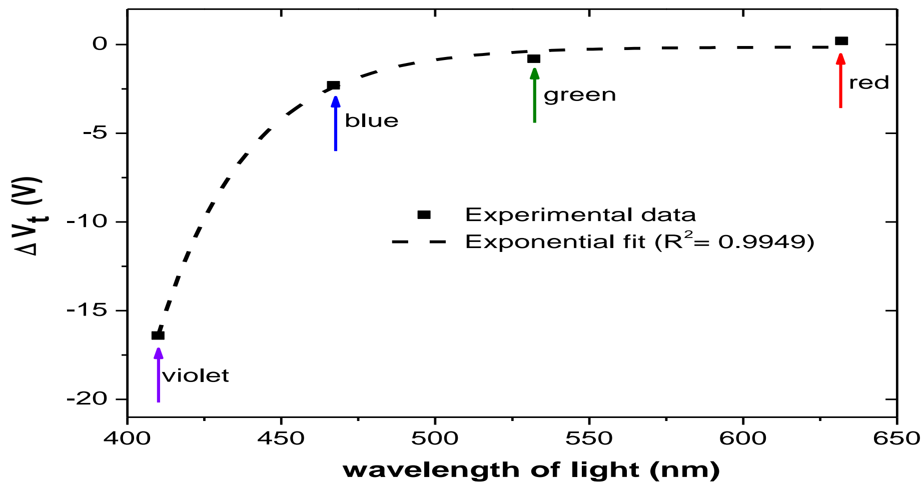


Figure 2.4 Threshold voltage shift after 25 k seconds of illumination stress for the shortest to longest wavelengths

The threshold shift observed for violet light (wavelength of 410 nm) is -17 V after stressing for 25,000 seconds. For bias stress, there was a continuous change in the threshold voltage during the period of stressing, but for illumination stressing it is different. Initially the threshold voltage shift towards the negative direction is higher, but eventually this effect begins to saturate. This is shown in figure 2.5. To understand the reason behind this large shift of

threshold voltage in negative direction, it is important to study the energy band diagram of a-IGZO films. The bandgap of a-IGZO is approximately 3.1 eV which depends on the composition of In, Ga and Zn. As a-IGZO TFTs are exposed to different photonic energies, it could lead to band to band transition of carriers from valence band to the conduction band. This could cause the earlier *turn on* of the TFTs, hence a negative threshold voltage shift.

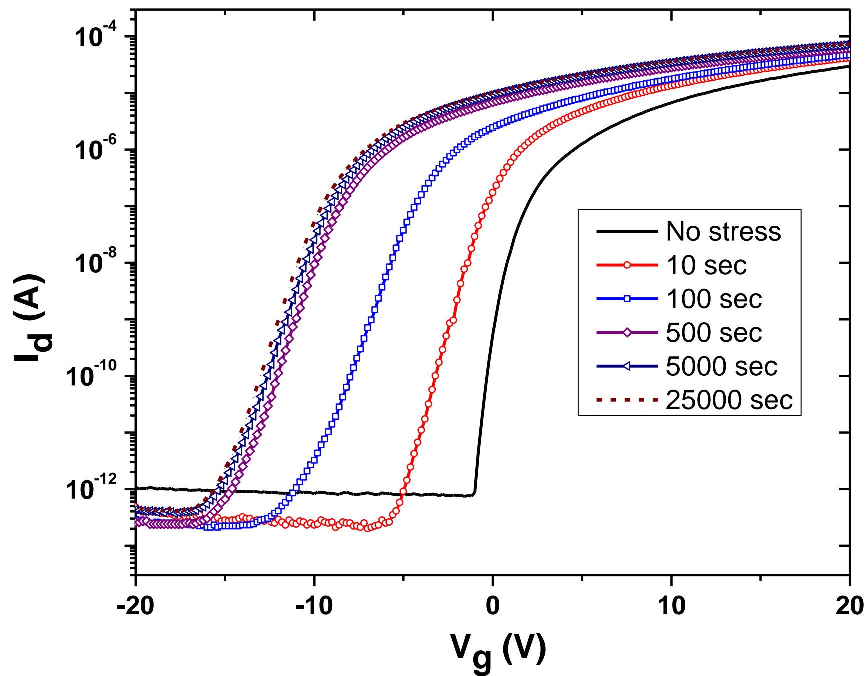


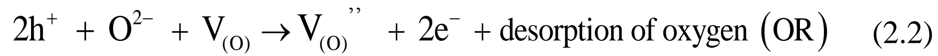
Figure 2.5 IGZO TFT under 410 nm light illumination stress for 25,000 seconds.

However, the early *turn on* of the TFTs upon illumination stress depends mainly on two mechanisms. First of them is, the excitation of the carriers from deep level trap states of the semiconductor and the dielectric material due to the effect of photonic energies. This increases the net carrier concentration causing an early *turn on* of the TFTs. Earlier studies have reported an increase in I_{off} due to the photo excitation of the carriers from the tail states of the valence

band to the conduction band [39]. But this effect was absent in the particular type of TFTs. Moreover, there was a reduction in *off current* under illumination stress under all the wavelengths. This reduction in *off current* is due to the presence of oxygen vacancies who act as hole traps in the source/channel and drain/channel interface during the reverse bias condition when subjected to illumination stress [33, 37]. But the positive effect of reduction in off current is usually nullified by a drop in mobility and on current [40]. However, in this case higher *on current* during illumination stress has been observed.

Second mechanism that causes negative threshold shift of the TFTs, is the influence of oxygen vacancies. The neutral oxygen vacancies present in the IGZO layer and SiO_x can act as dopants [40] by becoming singly or doubly ionized vacancies with the help of an energy of 2.2 eV [41-44]. This energy can be available because of illumination stress, hence increasing the carrier concentration and causing an early *turn on* of the TFTs. This whole mechanism is initiated by the generation of new electron hole pairs in the TFTs. Then these holes and incident light energy help the neutral oxygen vacancies to be ionized, shown in the following equations [41].

$$\text{IGZO} + h\upsilon \rightarrow e^- + h^+ \tag{2.1}$$



$$2h^+ + O^{2-} + V_{(O)} \rightarrow V_{(O)}^{''} + 2e^- + \text{desorption of oxygen (OR)} \tag{2.2}$$

$$h^+ + O^- + V_{(O)} \rightarrow V_{(O)}^{'} + e^- + \text{desorption of oxygen} \tag{2.3}$$

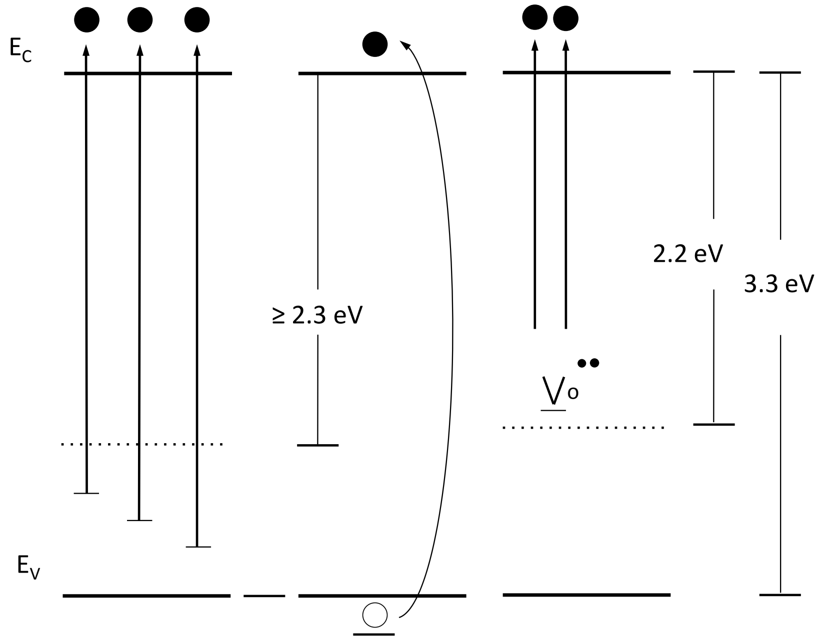
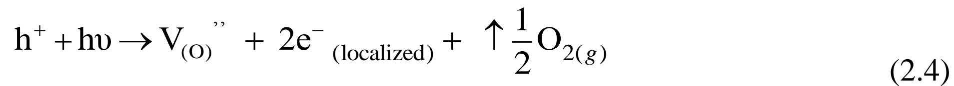
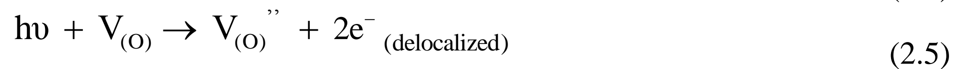


Figure 2.6 Creation of excess carriers under illumination stress

Figure 2.6 shows these two mechanism which causes early *turn on* of the TFTs under illumination stress. Equation (2.2) represents the case for doubly ionized oxygen vacancies while equation (2.3) is for the singly ionized oxygen vacancies. However, the term neutral vacancy means, when an oxygen escapes from its position into an interstitial position, it localizes the ions of the oxygen, and appears to be neutral in charge [37], as explained in the relation below:



$$h^{+} + h\upsilon \rightarrow V_{(O)}^{''} + 2e^{-}{}_{(\text{localized})} + \uparrow \frac{1}{2} O_{2(g)} \quad (2.4)$$



$$h\upsilon + V_{(O)} \rightarrow V_{(O)}^{''} + 2e^{-}{}_{(\text{delocalized})} \quad (2.5)$$

Earlier studies [45] showed that, when illumination stress is removed, excess electron hole pairs recombine and excess electrons fall back into the deep level states. However, the recovery process for this case has been slow and incomplete, which suggests that the recombination of the electron hole pairs is immediate but the excess carriers falling back into the deep level states

depend on the diffusion length. Moreover, the passivation layer upon the TFTs, prevented the absorption of the oxygen to reverse the equation (2.2) and (2.3), which eventually resulted in the incomplete recovery of the TFTs.

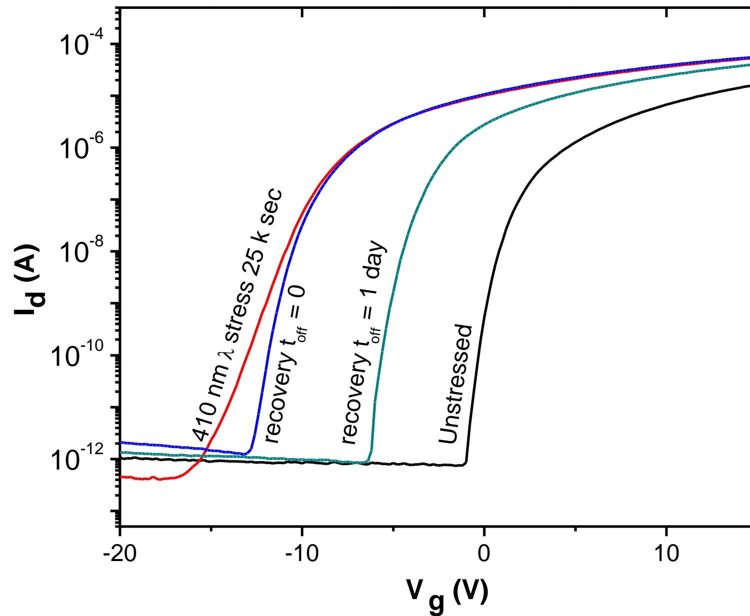


Figure 2.7 Incomplete recovery of the TFTs after stressing with light of 410 nm

2.5 Combined Stressing and Post processing annealing

After analyzing the TFTs for bias stress and illumination stress separately, both stress has been combined to analyze its effect. It has been found that light of 632 nm has little effect on the TFTs. So it is not expected to have any significant effect when applied simultaneously with the bias stress. Illumination stress for all other wavelengths with positive bias stress have little effect on the TFTs as these two different stressing seem to compensate each other. However, for negative bias stress along with the illumination stress, the TFTs showed significant change in its I-V characteristics. As the wavelength of the illuminated light decreased, the threshold shift

increased. At one point the device failed when stressed with the light of 410 nm along with -20 V bias stress for more than 5000 seconds. However, as the light is turned off, the device recovered from the failed state but there was still significant threshold shift present in its characteristics. Figure 2.8 shows the transfer characteristics of the TFT when subjected to ±20 V bias stress along with 410 nm light illumination stress for 10,000 seconds.

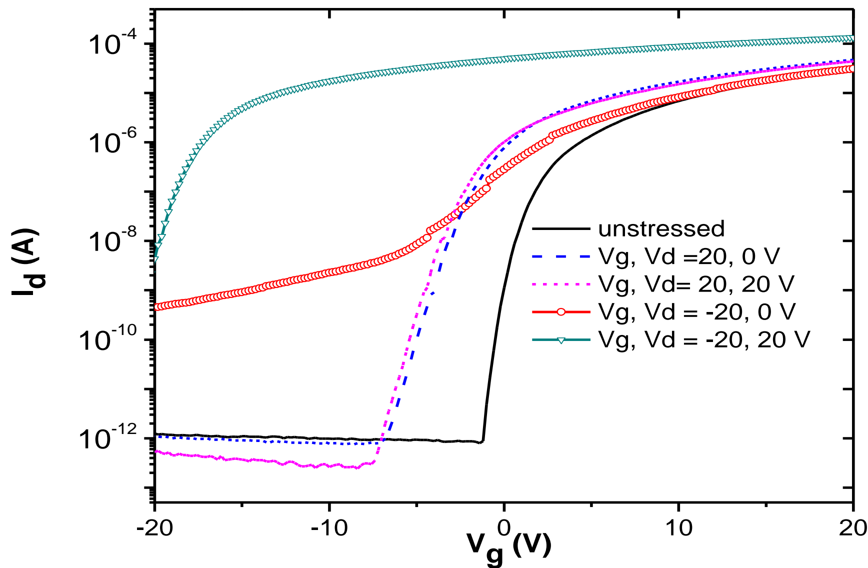


Figure 2.8 Transfer characteristics under 410 nm illumination stress along with ± 20 V gate bias

The mechanism or combination of mechanisms contributing to the failure modes of the TFTs under illumination and bias stress are explained as follows. The extensive negative gate bias causes accumulation of holes near the channel/gate dielectric interface, leading to charge trapping within the dielectric, but also creates an excess of electrons within the channel near the source interface, hence lowering the barrier for charge transport at the source-channel. When combined with excess concentration of charges due to photonic excitation, over a period of time,

this reduced barrier leads to free transport of charges in the negative bias region (*off* region) and hence failure of TFTs. These phenomena can be observed for negative gate bias stresses (-20 V) under illumination of 410 nm, for drain bias voltages of both 0 and 20 V. But, for positive gate bias stress combined with 410 nm illumination, the effects compensate each other as discussed earlier.

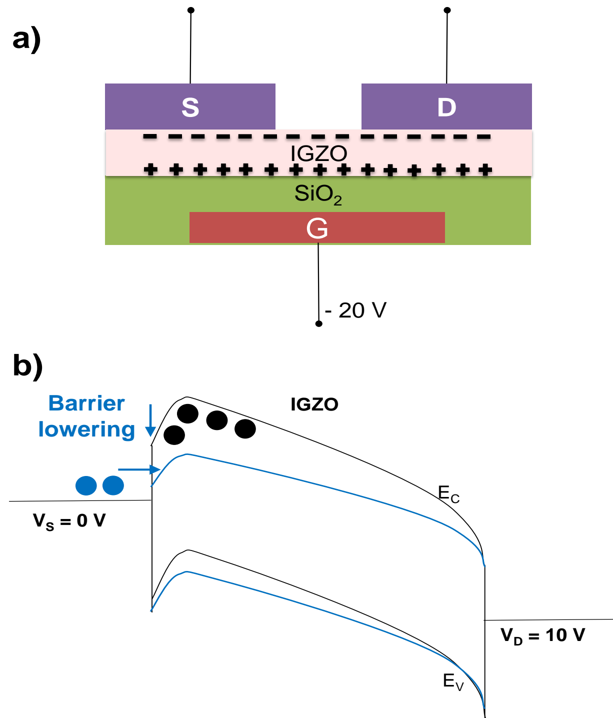


Figure 2.9 (a) Charge distribution in TFT under -20 V bias stress (b) Barrier lowering at the source channel interface

However, this failure under extended stresses can be regulated by efficient post process techniques such as annealing the fabricated TFTs in suitable ambient. To facilitate processing compatibility with low temperature fabrication methods and polymer substrates, low temperature anneals have been suggested in this study. Post deposition treatment has been performed in

vacuum, oxygen, and forming gas, at temperatures as low as 150° C for 12 hours, instead of high temperature anneals where channel crystallization is targeted. Reliability tests have been performed post annealing, at conditions previously known to cause failure (410 nm wavelength, -20 V gate bias). Although the TFTs experience a shift in threshold voltage due to carrier induced lowering of barrier (excess electrons from photonic excitation) for earlier *turn on* of the TFTs, no failure of the devices has been observed.

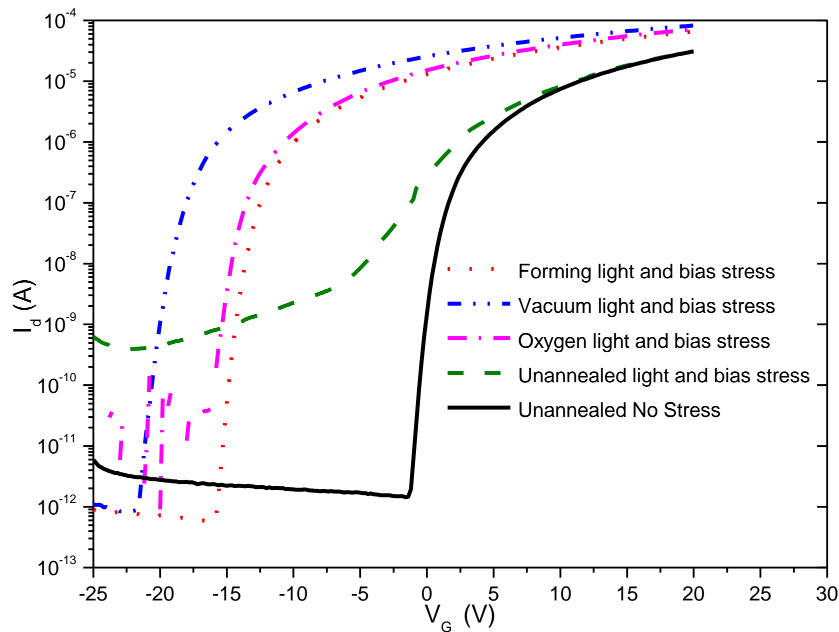


Figure 2.10 Transfer characteristics under combined stress (410 nm wavelength, -20 V gate bias) after post processing annealing in different ambient

A standalone illumination stress study of the post fabrication annealed TFTs with photonic energies from the 410 nm wavelength light demonstrates the annihilation of defects within the bandgap. The unannealed TFTs experience a threshold voltage shift of -17 V under

photonic stresses, whereas the oxygen annealed TFT displays the least threshold voltage shift of -1.3 V after the illumination stresses for 25,000 seconds. The vacuum anneal has the least capability of annihilation of defects, although the threshold voltage shift is as low as -4.5 V. The effectiveness of oxygen anneal confirms that deep level oxygen vacancies are annihilated (filled by oxygen), which reduces the concentration of electrons that are supplied from ionization of these deep level oxygen vacancies. The trap states created within the channel and the dielectric as a result of the low temperature fabrication are also annihilated due to the anneal process. Figure 2.11 shows the transfer characteristics for only illumination stress after post processing annealing.

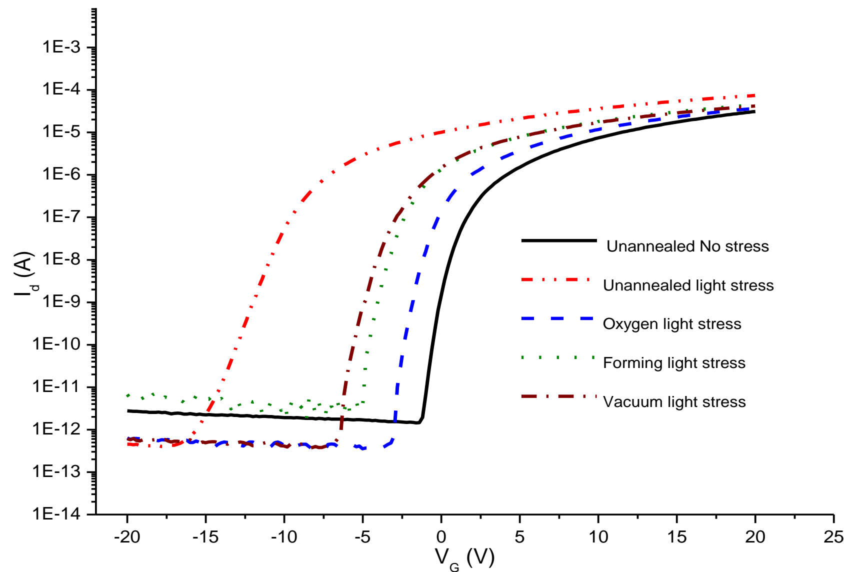


Figure 2.11 Transfer characteristics under illumination stress (410 nm wavelength) after post processing annealing in different ambient

Gadre *et al.* have performed oxygen, vacuum, and forming gas anneals of IGZO thin films and have confirmed that oxygen anneal annihilates oxygen vacancies, which can be correlated to the carrier concentrations [46]. However, vacuum anneal creates more vacancies,

and hence greater concentration of carriers from ionization of these vacancies, which can be correlated once again with the increased carrier concentration post vacuum anneal. Similar to the study on IGZO thin films, the TFTs are annealed in oxygen, and then in vacuum ambient, and the threshold voltage shift under illumination as seen in Table 1 suggests annihilation of oxygen vacancies, followed by creation of vacancies due to vacuum anneal, which creates greater shift in threshold voltage than for oxygen only anneals. The forming gas anneal also contributes towards annihilating defects, and improving transistor reliability under photonic stresses, but the TFTs annealed in forming gas demonstrate altered *off* current characteristics.

Table 2.1 Summary of threshold voltage shifts in unannealed and low temperature annealed TFTs under various stress conditions

Stress Condition	**Threshold Voltage Shift (V)**				
	Unannealed	**Vacuum**	**Forming**	**Oxygen**	**Oxygen and Vacuum**
Illumination Only (410 nm)	-17	-4.5	-3.3	-1.3	-2.4
Illumination and Bias (410 nm and -20 V)	Device failure	-20.8	-16	-18.2	-19

The nature of annihilation of defects and vacancies using forming gas is different from the effect of oxygen gas. Hydrogen from forming gas not only fills into vacancies within in the channel, but also bonds with the dangling bonds at the interface of the dielectric (IMD and gate dielectric) to channel layer. The vacancies within the dielectric material that trap the excess

carriers for *off* currents under photo-excitation are also filled with hydrogen, hence the excess carriers can contribute towards increased *off* currents without being trapped. The improved subthreshold swing of the TFT annealed under forming gas further confirms the annihilation of defects at the dielectric interface. Low temperature annealing in ambient such as oxygen or forming gas facilitate annihilation of defects by driving in oxygen or hydrogen atoms into locations and by filling in vacancies and the dangling bonds. This is an important finding which improves reliability and lifetime of low temperature/room temperature deposited TFTs, while maintaining compatibility with fabrication onto flexible or large area substrates as well the conductivity and transparence properties. Furthermore, improvements in properties of TFTs post forming gas anneal, on par with oxygen anneal lead to speculation of hydrogen as a donor within the mixed oxide channel material, which could be used to an advantage where post fabrication anneal can annihilate the vacancies, without hindering the carrier concentration in the material.

2.6 Conclusion

The failure mechanisms arising from the instability in operation of indium gallium zinc oxide based thin film transistors have been extensively studied and reported. The effect of prolonged real scenario stresses such as simultaneous bias and illumination has been investigated. Positive and negative gate bias conditions, along with several wavelengths in the visible spectra (between 410 nm and 632 nm) are used as stress conditions. Defects within band gap and ionized vacancies are generated with photonic excitation from wavelengths lower than that of green light. The reduction in off currents under illumination is contributed to the trapping of carriers in the intermetal dielectric. Device failure condition was determined as 410 nm light

based stress along with -20 V gate bias. The defect identification assisted in proposing suitable low temperature post processing steps in specific ambient. Reliability tests with post designed anneals confirmed the correlation of the defect type with anneal ambient. Annealed TFTs demonstrated high stabilities under illumination stresses and did not fail when subjected to combined stresses that cause failure in as-fabricated TFTs. The phenomena guiding metal oxide based transistors into failure while under practical stress scenario for a prolonged duration of time have been understood. However, degradation due to few expected defect centers has been reduced by a large extent due to the appropriate post anneal steps. TFTs with lower off currents under negative bias illumination stress were achieved. The post fabrication anneal was also efficient in regulating the density of oxygen vacancies (also reducing the carrier concentration from the ionization of vacancies) and reduced the density of traps at the semiconductor/dielectric interface. The post-fabrication process step improved the subthreshold swing of the device which is crucial for fast switching speeds of devices. The Ion/Ioff ratio in most stressed TFTs increased instead of showing a drop, due to which the active electronics based on these TFTs can have faster performance even under extreme practical stress conditions.

CHAPTER III

ROLE OF HYDROGEN AS A COMPENSATING DONOR IN MIXED OXIDE THIN FILMS

3.1 Introduction

Amorphous mixed oxide based thin film transistors (MOTFTs) are a lucrative alternative for amorphous Si based TFTs in display based electronics due to their transparency as well as inexpensive deposition methods onto large area substrates. Previous chapters elaborated the advantages of a-IGZO as the channel layer in place of extensively used a-Si:H. Chapter II discussed stability issues associated with this new material as a channel layer for the TFTs. TFTs has been studied under bias stress, illumination stress, combined stress (bias and illumination simultaneously) and kinetic stress by the researchers for various period time. Post processing low temperature annealing has been done to improve the performance and stability of the TFTs. Components like deep level trap states and ionized oxygen vacancies in the channel layer, play vital role in determining the stability of the TFTs under stressed condition. Especially under illumination stress, neutral oxygen vacancies ionize to give rise to the increased carrier concentration and also act as a scattering site for the carriers. Researchers have studied the nature and effect of oxygen vacancies in a-IGZO extensively [43, 47-49]. Oxygen annealing proved to be a solution to remove these vacancies and provide a more stable device. However, in this study, it has been shown that forming gas annealing could be helpful. Forming gas annealing has the best result in terms of threshold voltage shift, when exposed to light and bias stress simultaneously. This gives us the opportunity to study the effect of hydrogen atom in a-IGZO

thin films and its interaction with oxygen vacancy and other defect sites in the thin film. This chapter studies the nature of oxygen vacancies in crystalline and amorphous IGZO thin film and the role of hydrogen in vacancy annihilation and its impact on the carrier concentration, mobility and resistivity of the thin film.

3.2 Experimental Setup

3.2.1 Sample Preparation

The a-IGZO films were deposited on silicon at room temperature using an RF sputter deposition system. The composition of the sputtering target was 99.99% InGaZnO4.The deposition was done at 100 W RF power and 10 mTorr of pressure using argon gas.

3.2.2 Sheet Resistance Measurement

After depositing a-IGZO on silicon, a four point probe setup has been used to measure its sheet resistance. This four point probe used two probes to supply the current and other two to sense the voltage drop. The outer two probes supply the current to the sheet of a-IGZO and inner two probes use a voltmeter to measure the voltage drop in the a-IGZO film between those two points where the probes are placed. This is unlike the two probe system where same two probes are used to provide the current and measure the voltage drop. The additional two probes help to avoid the contact resistance and provide only the sheet resistance of the film. Each probe in the setup has probe resistance R_p, a probe contact resistance R_{cp} and spreading resistance R_{sp}. As current is supplied by the outer two probes, voltage drop is not measured across them, since parasitic resistances (R_p, R_{cp}, R_{sp}) are taken into account in the process. Hence, the inner two

probes are used to measure the voltage drop using a high impedance voltmeter. As the voltmeter draws very little current, the voltage drop across the parasitic resistances is negligible, hence this setup negates other resistances and provides the correct sheet resistance of the film. The sheet resistance is calculated by dividing the voltage measured by the current supplied and multiplying this with the correction factor which depends on the probe spacing, film thickness and the probe distance from the edge of the sample.

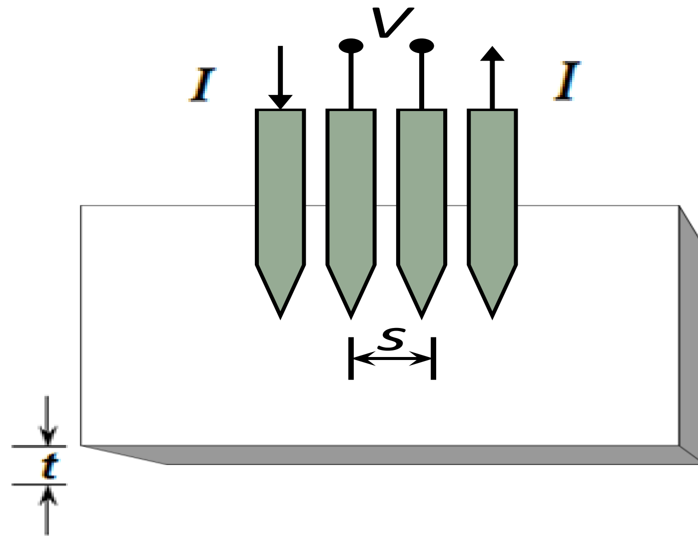


Figure 3.1 Schematic of a typical four-point probe setup. Measurements taken at ASU have a probe spacing of 1 mm. Where S = spacing between the probes, and t = thickness of the sample.

The sheet resistance expressions can be expressed as follows:

$$R_s = (V/ I) \times CF \qquad (3.1)$$

Where CF = Correction factor and V/ I is the reading from the monitor, V is the voltage drop and I is the current driven through the sample. The resistivity of the material is calculated by using the following expression:

$$\rho = R_s \times t \qquad (3.2)$$

Where t = thickness of the material.

3.2.3 Hall Measurements

Hall measurements were performed on the sample using Van der Pauw method. The main purpose of this experiment, is to find out the carrier mobility and concentration in a-IGZO thin film which has been sputtered on to the silicon wafer. Initially, the samples were mounted onto a printed circuit board using copper wires and silver paste to establish contacts. The Van der Pauw method is the most common one to be used to measure the electrical properties of the film such as resistivity, doping type of the film (p-type or n-type), mobility of the majority carriers and carrier densities. However, it is necessary to have the sample thickness much less than the length and width of the sample to use this method. In other words, the sample needs to be two dimensional. Moreover, the sample needs to be symmetrical in order to avoid measurement errors and there should not be any isolated holes within the sample. The contacts for the sample need to be ohmic.

From the top right corner of the sample as schematic seen in Fig. 3.2, if the contacts are numbered 1 to 4 in a clockwise direction, current is made to flow along one edge of the sample (along the 1-2 side), and voltage is noted on the other edge (along the 3-4 side). The ratio of the voltage V_{34} and I_{12} gives the resistance in the material

$$R = \frac{V_{34}}{I_{12}} \qquad (3.3)$$

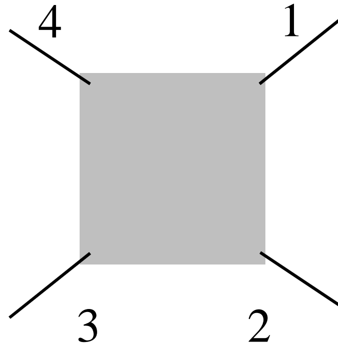


Figure 3.2 Sample labeling for the contacts made to perform Van der Pauw Hall measurements

Hall effect is the main principle used here for electrical characterization of the material. When electrons flow through a magnetic field, a force called Lorentz force is exerted on them which depends on the velocity of their motion in the field. The force is maximum when the field is perpendicular to the motion of the electrons, and is given by

$$F_L = q.\upsilon.B \qquad (3.4)$$

where q = the charge on the particle in coulombs

υ = velocity

B = the strength of the magnetic field (Wb/cm^2)

Applying current on a semiconductor material results in a steady state flow of electrons within the material, with a velocity given by

$$\upsilon = \frac{1}{n_m \mu_m q} \qquad (3.5)$$

where n = electron density, A = cross-sectional area of the material and $q = 1.6 \times 10^{-19}$ coulombs.

This force accumulates charges at the edge which creates an electric field and the hall voltage can be directly extracted from this field, given by

$$V_H = \omega \epsilon \qquad (3.6)$$

$$= \frac{IB}{nqd}$$ (d=depth of the material; I = current across the film)

$$= \frac{IB}{n_s q}$$

Hence, we can obtain the sheet density n_s from the hall voltage. From previously obtained resistivity measurements, sheet resistance of the material is known from which the mobility of the material is given by

$$\mu = \frac{1}{n_s q R_s} \qquad (3.7)$$

Finally the resistivity of the material is given by

$$\rho = \frac{1}{n_m \mu_m q} \qquad (3.8)$$

where n_m = doping level of majority carrier, μ_m = mobility of the majority carrier.

Figure 3.3 shows the setup for the Ecopia HMS 3000 Hall measurement system used in this characterization methods, for which a magnet of 0.98 Tesla was used. To recover the measurements, the magnet was aligned in N-S, S-N directions.

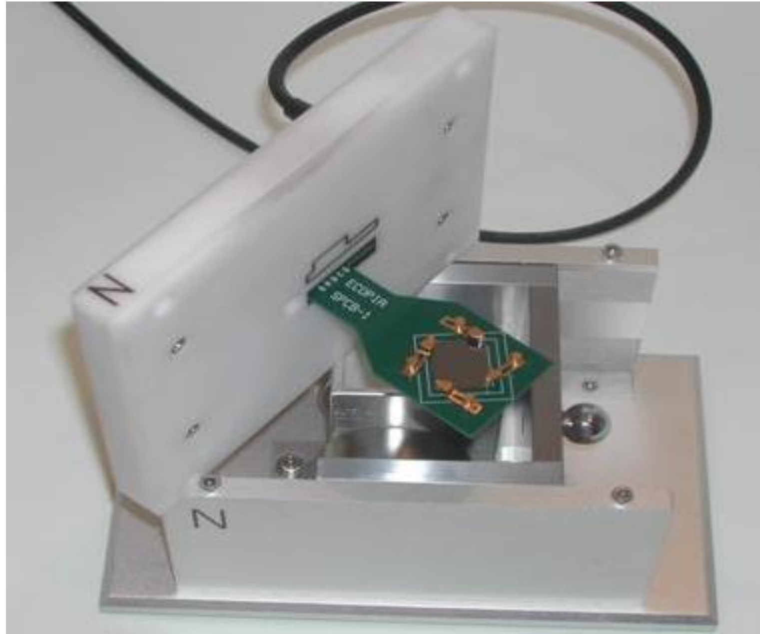


Figure 3.3 Ecopia HMS-3000 Hall Effect Measurement System used at ASU (Courtesy: *CSSS,* ASU)

3.2.4 Elastic Recoil Detection (ERD)

Elastic Recoil Detection (ERD) has been used in this study, to measure the hydrogen content in the a-IGZO thin film after annealing in forming gas ambient. ERD is a characterization technique which is typically used to detect light elements ($1 \leq z \leq 9$) near the surface region of materials. It is mainly used to detect hydrogen content in thin film materials. The basic principle of ERD is similar to Rutherford Backscattering Spectrometry (RBS), however the detection mechanism is not. In ERD, the incident beam is heavier than the element to be profiled which is directed at a grazing angle into the sample surface. As the light element is targeted, after the collision, it will recoil to the forward direction and some of them will be detected. A mylar foil is placed before the detector to filter out the heavier element which might have come from the incident beam or other elements of the thin film.

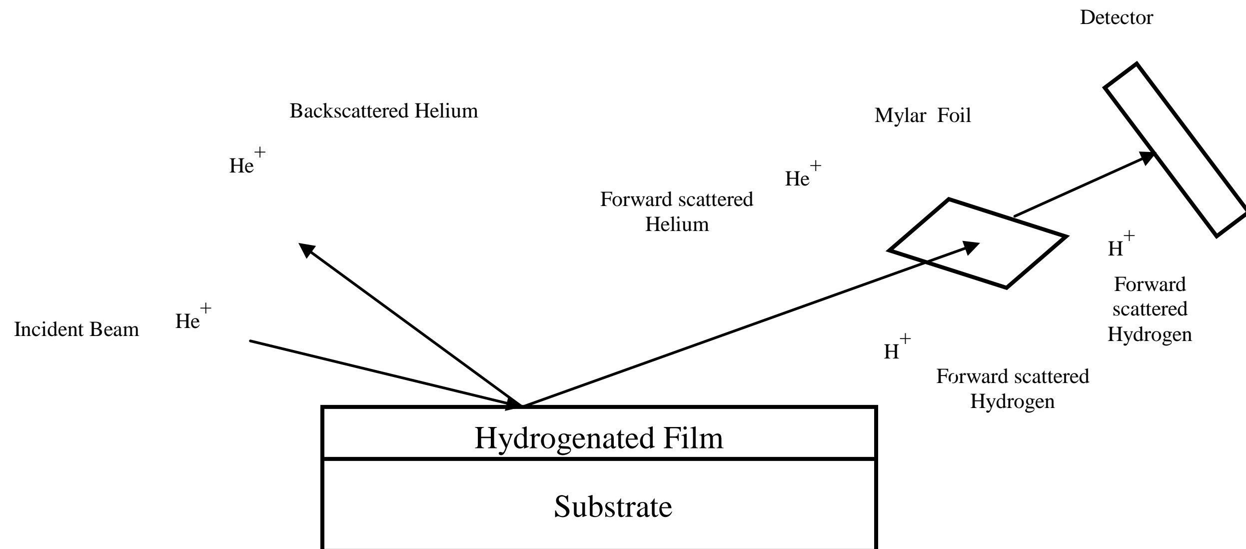


Figure 3.4 ERD working principle

In this particular experiment, Helium has been used as the incident beam as it is slightly heavier than Hydrogen. Incident energy of Helium beam was 2.8Mev and detector was placed at angle of 70° from the normal.

3.3 Discussions and Results

The presence of oxygen vacancies in a-IGZO has been an influential element towards the stability of TFTs using this material. Extensive studies have been done to understand its nature and effect, mostly under illumination stress. To understand the effect of oxygen vacancies, it is important to study the structure of IGZO. In past few years, many researchers have reported the electronic structure of crystalline and amorphous IGZOs [48]. Several density function theory (DFT) based calculations have been done to study IGZO structure. However, Nomura *et al.* reported that the nearest neighbor distances are similar both in crystalline and amorphous IGZO but a-IGZO has lower coordination number compared to crystalline structure, resulting in lower

density. Crystalline IGZO has a layered structure with alternating laminated layers of InO_2^- and $GaO(ZnO)^+$ [48]. It has two layers of $GaO(ZnO)^+$ followed by single layer of InO_2^-.

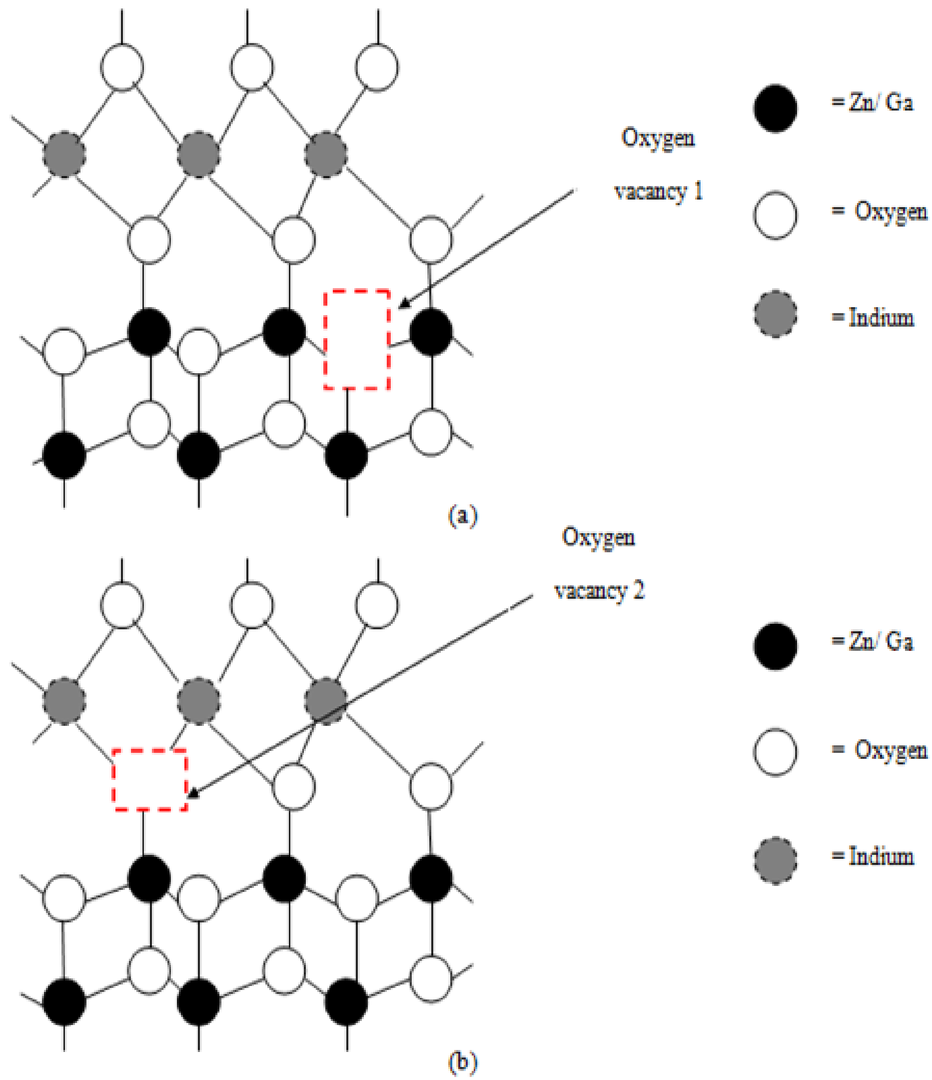


Figure 3.5 Structure of oxygen vacancy in c-IGZO (a) Type 1 (b) Type 2

The conduction band minimum (CBM) of crystalline IGZO (c-IGZO) is formed by the overlapping 5s orbital of Indium [48]. However, there are two types of oxygen vacancies found

in c-IGZO as shown in figure 3.5. First type of oxygen vacancy is between four Zn/Ga mixture atoms and second type is between three Indium and one Zn/Ga mixture atom. It is well established that the IGZO behaves as a n-type material due to its innate defects which gives rise to the free electron carriers. Initially researchers thought, these oxygen vacancies are the source of the free electron carriers. However, later on it was found that these oxygen vacancies are placed deep in the band diagram, hence it cannot be the source of free electron carriers. But these vacancies can still give up the electrons under stressed condition, mostly under illumination stress.

Although, the c-IGZO and a-IGZO has similarities in many aspects, it is necessary to study the oxygen vacancies for a-IGZO as it is more popular for TFTs because of its lower manufacturing cost. Unlike c-IGZO, a-IGZO does not have a layered structure but the In, Ga, Zn atoms are well distributed in the supercell models that is found in the literature [48]. Moreover, in a-IGZO few oxygen vacancies also exhibit shallow defect levels along with the deep level ones due to the weak interaction between the metal atoms . The nature and location of the oxygen vacancies depend on the ratio of In, Ga and Zn in the material [47]. The deep level oxygen vacancies do not give up the electrons without any stressing. However, when subjected to illumination stressing, these electrons tied to the neutral vacancies, become free carriers transforming the neutral vacancies to ionized vacancies. This phenomenon is described in equation 2.2 and equation 2.3 in chapter II. Figure 3.6 (a) shows the electronic structure of a typical neutral vacancy for a-IGZO. This structure is very similar to that of c-IGZO oxygen vacancy shown in figure 3.5 (b).

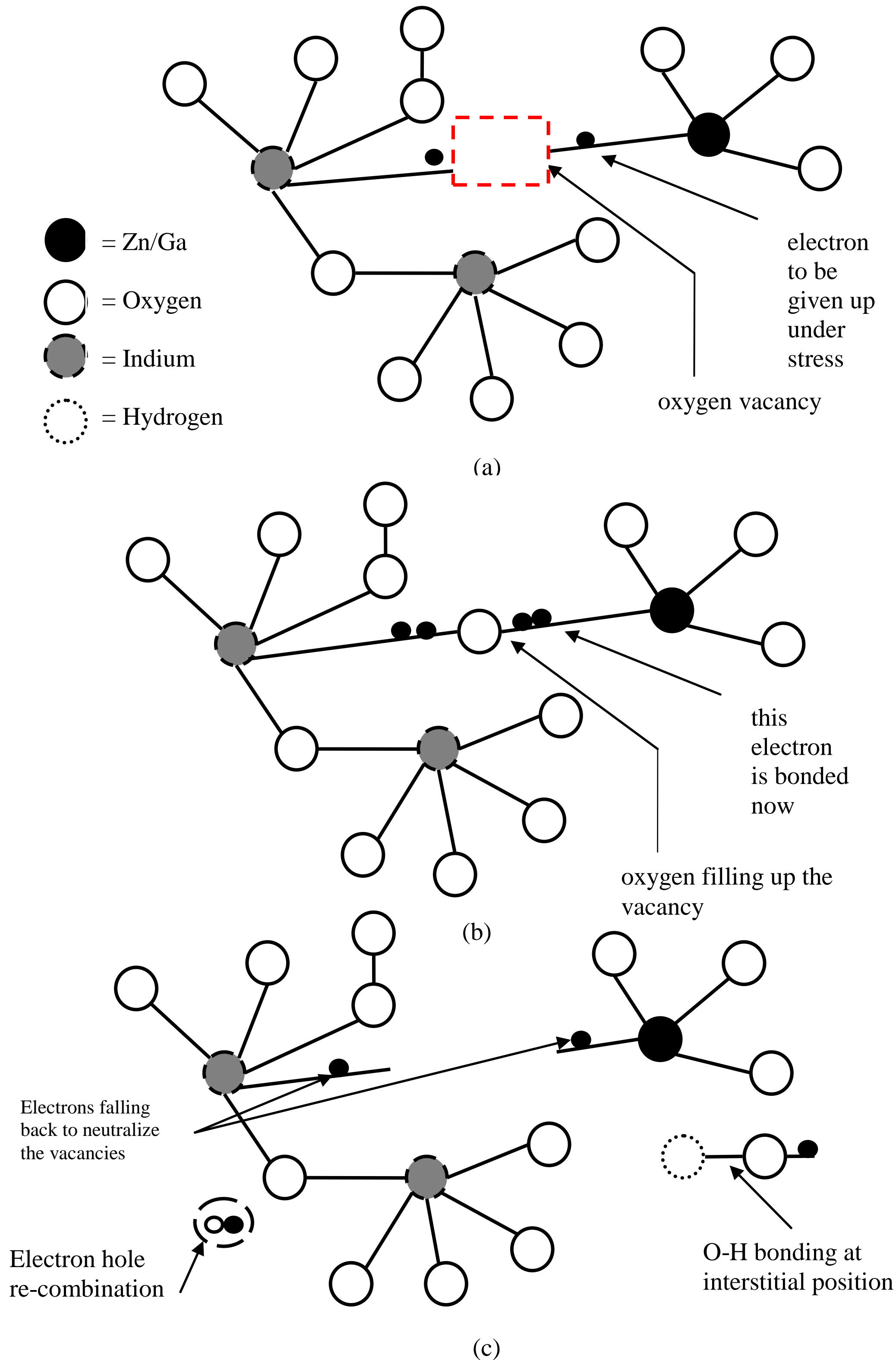
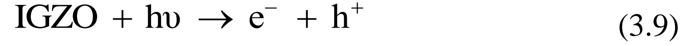
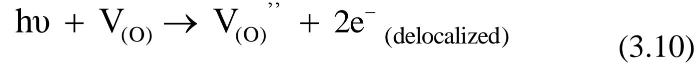


Figure 3.6 (a) a-IGZO oxygen vacancy (b) Vacancy after oxygen annealing (c) After forming gas annealing

These extra carriers from the oxygen vacancies, cause early *turn on* of the TFTs under illumination stress. Moreover, TFTs under bias and illumination stress simultaneously, experience failure condition due these extra free carriers. Results from chapter II shows that these problems can be solved by annealing the TFTs in oxygen ambient. This is because, annealing the TFTs causes the oxygen vacancies to fill with oxygen atoms from the ambient. Oxygen sitting in the vacancy forms O=O bond which makes sure that there is no electron to be freed up under stressing condition. However, superior result has been found for forming gas annealing when subjected to bias and illumination stress simultaneously. Moreover, threshold voltage shift also reduced significantly under illumination only stressing when annealed in forming gas (5% H_2, 95% N_2) ambient. The reason for these results is, hydrogen creates O-H bonding with the oxygen at interstitial position. As shown in equation 2.1, illumination on IGZO layer creates electron and hole pairs and it also ionizes the neutral oxygen vacancies. For clarity, this is again repeated in equation 3.9 and 3.10. Now without any annealing the holes generated would combine with O^- ion to create O_2 which will cause desorption of oxygen and extra electron generated from oxygen vacancy will add into the number of free carriers. But with forming gas annealing, hydrogen atoms will diffuse into the a-IGZO layer, give up an electron to ionize and create -OH ion with O^{2-} ions at interstitial position. This will help the extra electrons generated from oxygen vacancy to recombine with the generated holes. Moreover, the electrons given up by hydrogen will be captured by the ionized oxygen vacancies to return to the neutral state. This way total number of carriers remains lower than the unannealed case and some of the oxygen vacancies also recovers to the neutral state. All of these phenomenon are shown in equation 3.9 to 3.12.

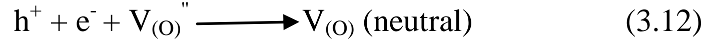


$$IGZO + h\upsilon \rightarrow e^{-} + h^{+} \quad (3.9)$$



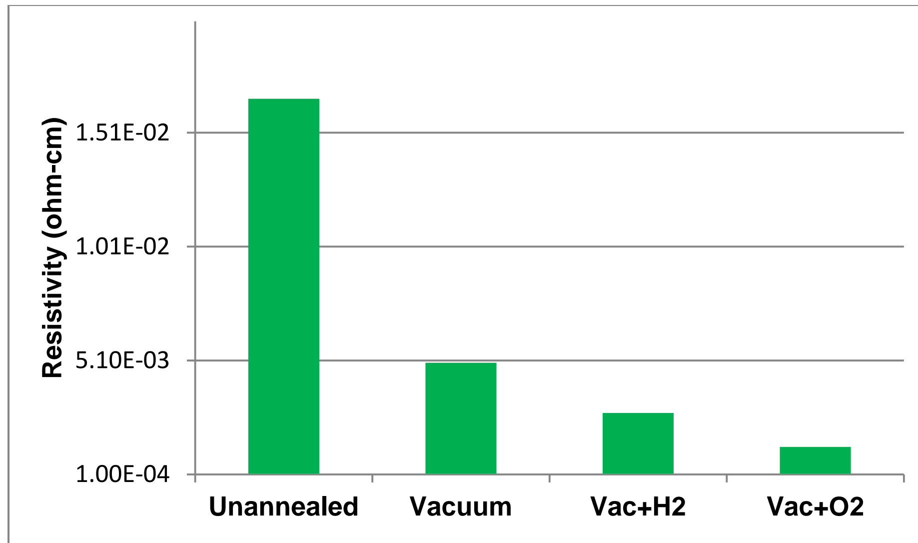
$$h\upsilon + V_{(O)} \rightarrow V_{(O)}^{''} + 2e^{-}_{(delocalized)} \quad (3.10)$$

$$H^{+} + O^{2-} \longrightarrow OH^{-} \quad (3.11)$$

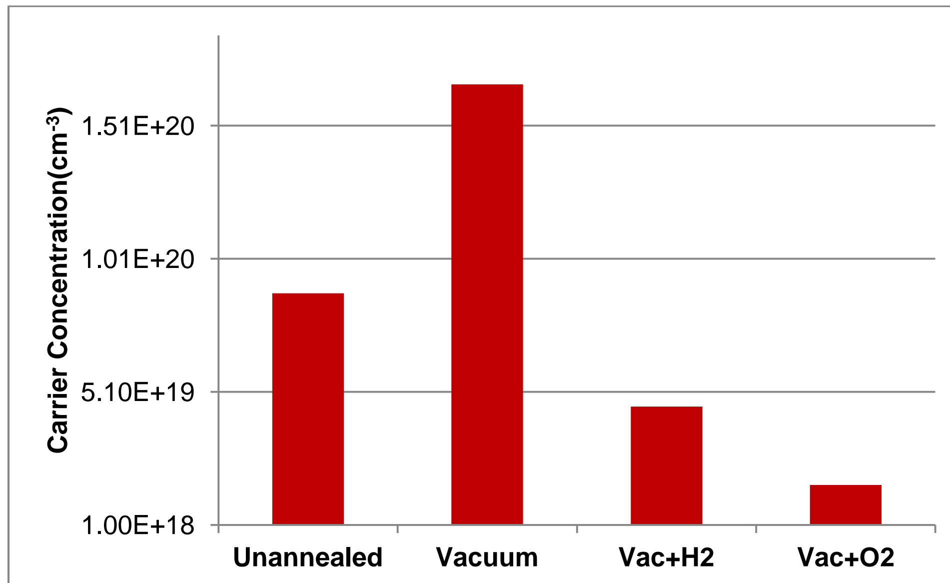


$$h^{+} + e^{-} + V_{(O)}^{''} \longrightarrow V_{(O)} \text{ (neutral)} \quad (3.12)$$

So it is expected to have less free carriers in the a-IGZO film after annealing in the forming gas ambient. Moreover, as the carrier concentration decreases, the mobility should increase due to less interaction or scattering between the carriers. The reduction of ionized oxygen vacancies would also facilitate the carrier mobility because ionized vacancies behave as a scattering site for the free electrons. To verify these claims, a-IGZO film on silicon substrate has been annealed in three different circumstances. First sample was annealed in vacuum ambient for 9 hours at 150° C. Second and third sample was also annealed in vacuum ambient followed by annealing in oxygen and forming gas ambient respectively for 9 hours at 150° C. All of these samples along with the unannealed sample have been characterized for resistivity, mobility and carrier concentration using four point probe system and Hall measurement technique. These results are shown in Fig. 3.7.



(a)



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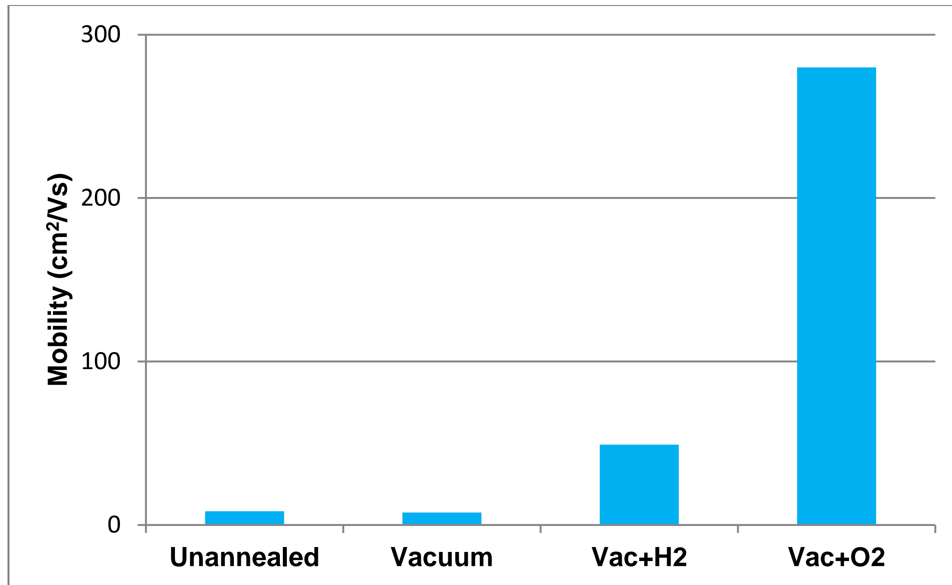


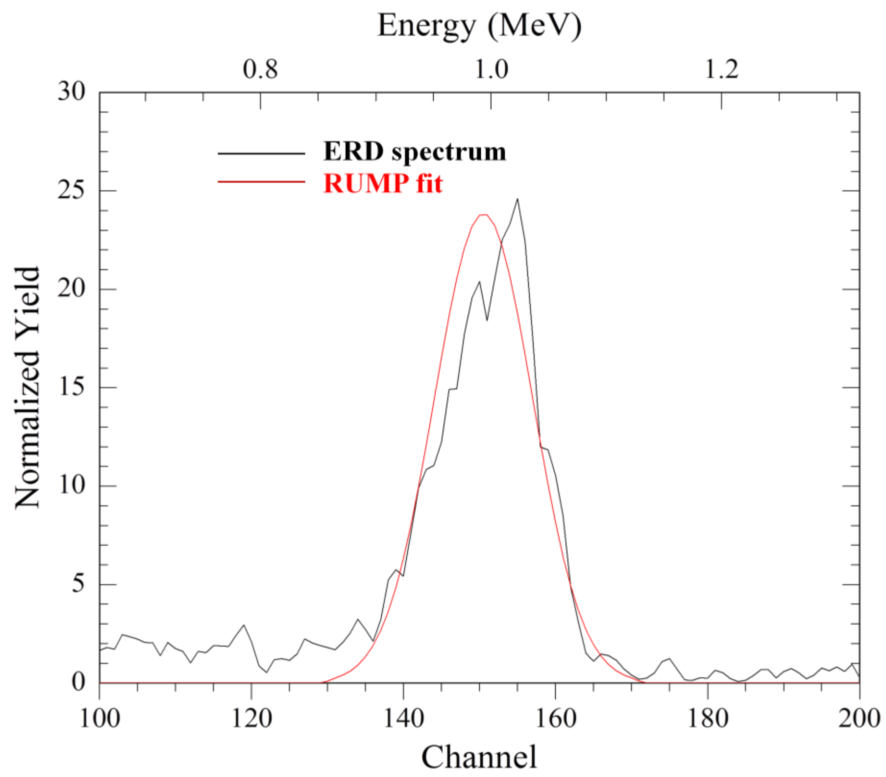
(c)

Figure 3.7 Comparison between four samples in terms of (a) Resistivity (b) Carrier concentration (c) Mobility

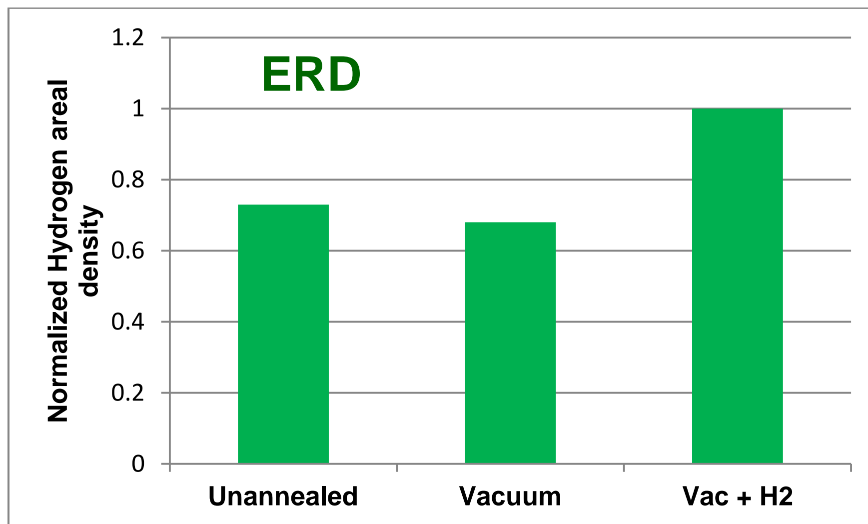
As expected, it is found that the vacuum annealed sample has highest carrier concentration as vacuum annealing increases defects in the form of oxygen vacancies (amongst other vacancies) in the thin film thus increasing carrier concentration. Oxygen annealed sample has lowest carrier concentration because most of the oxygen vacancies are filled up by oxygen atoms. As both unannealed and vacuum annealed sample has relatively higher carrier concentration, their mobilities are lowest because of increased scattering effect between the carriers or at the vacancy sites. Oxygen annealed sample has better mobility than forming gas annealed sample, because it has lower carrier concentration and lower oxygen vacancies which act as scattering sites in the film. The relationship between resistivity, mobility and carrier concentration is given by the following equation, where ρ is resistivity, N_C is carrier concentration and μ is mobility.

$$\rho = \frac{1}{N_C \, q \, \mu} \quad (3.13)$$

Result from figure 3.7 agrees with this equation, as it is seen that the sample with oxygen annealing exhibit highest mobility and lowest resistivity. Forming gas annealed sample shows moderate performance in terms of all three parameters which is because of the role of hydrogen atoms as discussed earlier. To verify the role of hydrogen atoms, ERD has been performed on the samples to measure the hydrogen content in the samples. Figure 3.8 (a) shows the ERD data for forming gas annealed sample and Fig. 3.8 (b) shows the hydrogen content in the unannealed, vacuum annealed and vacuum followed by forming gas annealed samples. The ERD results clearly show the reduced H concentration post vacuum anneal, and increased H concentration post forming gas anneal, and corroborate well with the Hall measurement parameters discussed earlier.. Moreover, it is mentioned previously that the vacuum annealing increases defects in the sample. In other word, it decreases oxygen content in the sample hence creating more oxygen vacancies, along with creating more hydrogen vacancies as seen from the reduced H content in the ERD spectra. To measure oxygen content in the film, oxygen resonance analysis has been performed on the unannealed and vacuum annealed sample.



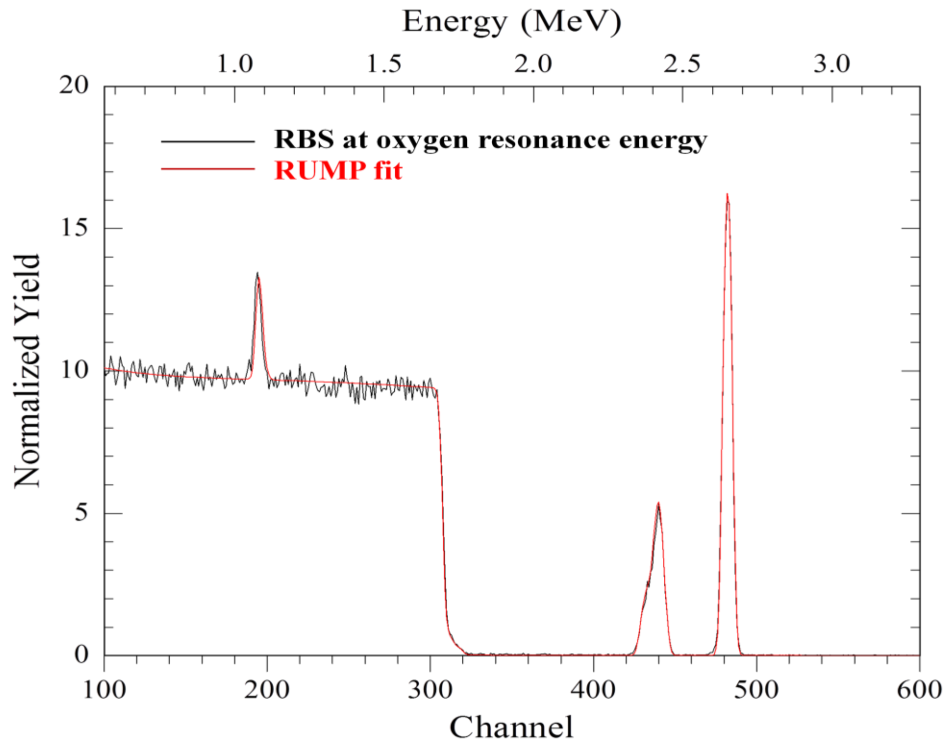
(a)



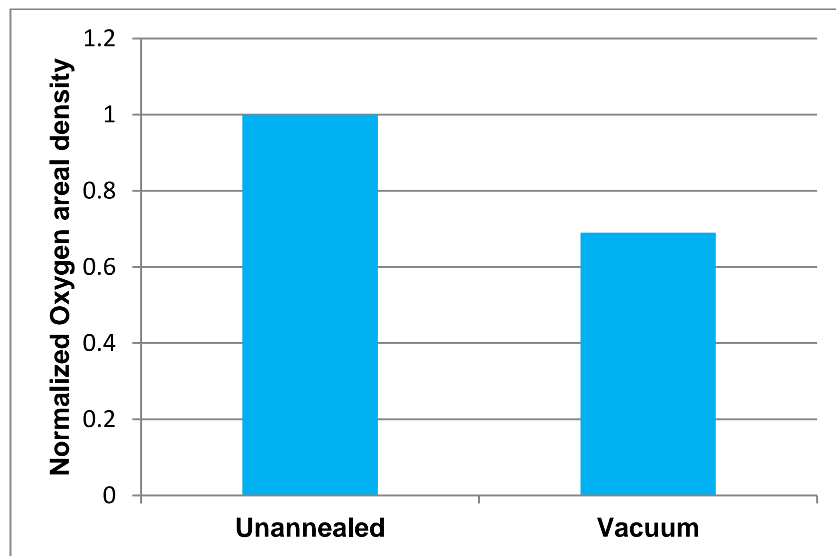
(b)

Figure 3.8 (a) ERD analysis data on vacuum followed by forming gas annealed sample

(b) comparison of hydrogen content in different samples



(a)



(b)

Figure 3.9 (a) Oxygen resonance analysis data on vacuum annealed sample

(b) comparison of oxygen content in different samples

Figure 3.9 (a) shows the oxygen resonance analysis on the sample with vacuum annealing through the RBS spectra, while Fig. 3.9 (b) compares the oxygen content with the unannealed film. The oxygen concentration from the oxygen resonance spectra corroborates well with the Hall mobilities and concentrations confirming the increased carrier concentrations and reduced mobilities in case of vacuum annealed are indeed due to increased ionized oxygen vacancies and vacancy scattering, respectively.

3.4 Conclusion

As a channel layer in TFTs a-IGZO showed great potential and researchers worked extensively to understand the structure, composition and limitation of this new material. The fundamental advantage of a-IGZO is its high mobility and higher carrier concentration than that of a-Si:H. However, under different types of stressing these advantages tend to deteriorate. This particular study tried to find out the right balance between stability and performance. Oxygen annealing provides the best result in terms of threshold voltage shift and helps the device to achieve better stability. However it, affects the carrier concentration in the film which is related to the current conduction through the film. Introducing forming gas annealing, helps to achieve a better carrier concentration with reasonable resistivity and mobility of the film. All of these comes without compromising the stability of the TFTs under stressed condition, especially practical stressing (bias and illumination) condition.

CHAPTER IV

INFLUENCE OF BIAS-ILLUMINATION STRESS ON THE ELECTRICAL PARAMETERS OF a-IGZO TFTs

4.1 Introduction

The benefits and limitations of a-IGZO TFTs have been discussed already in the previous chapters. The effect of extended illumination stress with and without bias stress have been studied thoroughly and post processing techniques have been proposed to achieve better stability and performance from the TFTs. However, it is important to analyze the effect of stressing from circuit point of view. These TFTs are going to be a part of critical circuits in many display technologies. Parameters like threshold voltage, mobility, sub threshold swing, power factor, k' factor etc add another dimension to this analysis. The variation of these parameters under stressed condition, explains the underlying phenomenon that causes the device to degrade. Extraction of circuit parameters for bias stressed TFTs has been done previously [50]. It has been mentioned that, illumination stress could de-trap carriers from the deep states in the band gap region and also could excite the carriers from the neutral oxygen vacancies. These phenomenon should have an impact on the carrier mobility, channel resistance and TFT threshold voltage. So, analyzing these circuit parameters, would confirm the physical phenomenon mentioned in the previous chapters. Moreover, this chapter deals with power factor n, which is subject to change under stressed condition. This power factor n confirms the distribution of states in the conduction band [51]. The variation of threshold voltage and power factor under stressed condition would confirm the effect of illumination stress on the TFTs with and without bias stress.

4.2 Fabrication Technique

Bottom gate staggered n-type a-IGZO based TFTs are used towards the analysis of bias and illumination stresses, with a structural cross-section as previously seen in Fig. 2.1. Fabricated on 300 mm silicon wafer, it has used Molybdenum (Mo) of 150 nm thickness as the gate electrode. SiO_x of 200 nm has been used as the gate dielectric after patterning the gate metal. a-IGZO has been used as the channel layer with the thickness of 50 nm which is sputtered at RF power of 100 W, using $InGaZnO_4$ as the target for sputtering. The metal and mixed oxide layers were sputtered at temperatures between 71°C and 91 °C. After the channel layer, SiO_x is deposited as the inter metal dielectric at 180° C. Then Mo is again used to form the source and drain electrodes of the TFT. Finally, a passivation layer of SiN is deposited on the TFT and the entire wafer is annealed at 200° C for 1 hour.

4.3 Experimental Setup

TFTs under stress have, an aspect ratio of 9 µm/9µm. HP 4155B semiconductor parameter analyzer has been used to measure the transfer characteristics and output characteristics of the TFTs. The devices were stressed with a Dolan Jenner Fiber Lite Illuminator with a dual gooseneck optical cable attachment, which has been used to generate white light. Certain filters were used to generate lights having 410 nm, 467 nm, 532 nm and 632 nm wavelength. For Bias stress, only -20 V has been applied to the gate of the TFTs as negative bias stress along with illumination stress, demonstrated worst stability scenario. For transfer characteristics, gate voltage has been swept from -20 V to + 20 V with V_{DS} of 10 V. The output

characteristics were also extracted by sweeping the drain from 0 to 20 V, for gate voltages of -5 V to 20 V in steps of 5 V.

4.4 Results and Discussions

TFTs under test were subjected to standalone illumination stress under lights having wavelengths of 410 nm, 467 nm, 532 nm and 632 nm for 25000 seconds. As mentioned in chapter II, illumination stressing can excite carriers from the deep trap states in the band gap region. It could also excite free electrons from the neutral oxygen vacancies. All of these these factors contribute towards increased free carrier concentration in the channel layer, causing an early *turn on* of the TFTs. Figure 4.1 shows the transfer characteristics of the TFTs when subjected to illumination stress with lights of different wavelengths.

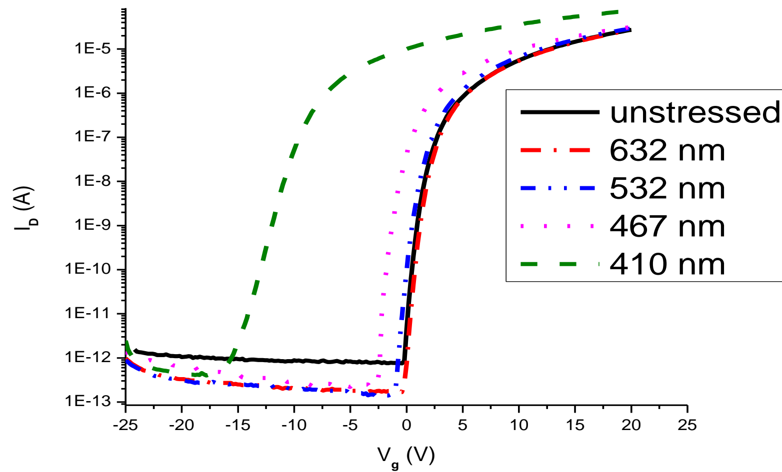


Figure 4.1 a-IGZO TFT under illumination stress for 25,000 seconds for light of various wavelengths

Figure 4.1 clearly shows that the light of 410 nm has the worst effect on the TFT. It causes a significant shift in the threshold voltage. The red light (632 nm) has very limited effect on the TFTs, which is why it is ignored for rest of the analysis. Light of 410 nm has the lowest wavelength or it has highest energy amongst the available lights of different wavelengths. Thus it can excite more electrons from the very deep level trap states in the channel layer, giving the maximum threshold voltage shift. However, it is noticeable that, the drain current of the TFTs exhibit similar subthreshold swing when subjected to illumination stress for different periods of time. This means that the illumination stressing does not have a pronounced impact on the interfacial (dielectric and channel layer interface) charge densities.

However, none of the standalone illumination stressing, have driven the device into failure condition. This changes, when the TFTs are stressed with bias and illumination stressing simultaneously. As discussed in chapter II, +20 V bias stress with 410 nm illumination stress have little effect on the TFTs, as these two separate types of stressing have compensating effect on the device characteristics. But a -20 V bias stress along with violet light (410 nm) stressing, drives the device into failure condition. The reason for this type of behavior is well explained in chapter II. This chapter will analyze the threshold voltage shift, channel resistance, power factor *n* and carrier mobility to verify the physical phenomenon mentioned in the earlier chapters. In TFTs the effective channel mobility increases with the gate voltage, $V_{g.}$ Moreover the drain current has *n*th power dependence on the overdrive voltage. These factors made it difficult to extract the threshold voltage using the conventional methods such as extrapolating the $I^{1/2}_{dsat}$ vs V_g curve [52] or taking the derivative of the drain current with respect to the gate voltage [53].

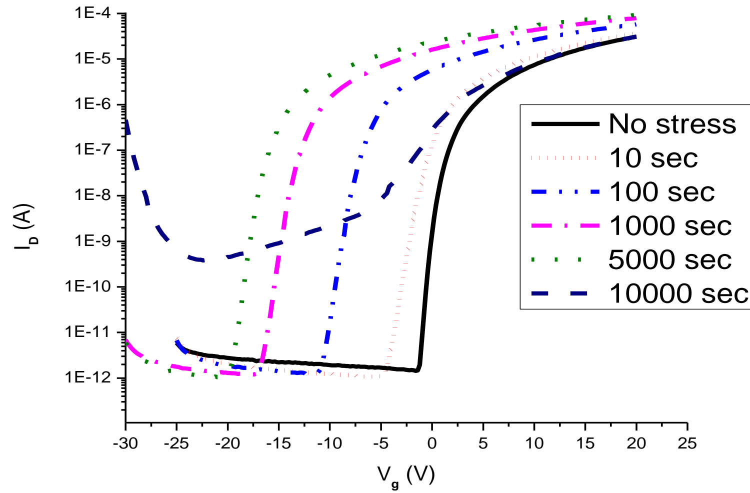


Figure 4.2 a-IGZO TFT when exposed to bias-illumination (410 nm and -20 V) stress

That is why an integral method is applied to extract the threshold voltage of the TFTs [54]. In this method the drain current is integrated over the gate voltage and this integrated drain current is plotted against the gate voltage. Then linear curve fitting is performed to find out the x-axis intercept which is the extracted threshold voltage and the slope of the fitted curve could be used to extract the power factor *n* of the device. If the integrated curve is defined by $H(V_g)$, then

$$H(V_g) = \frac{\int_0^{V_g} I_{DSAT}(V_g)dV_g}{I_{DSAT}} \qquad (4.1)$$

after solving which could be written as, $$H(V_g) = \frac{(V_g - V_{th})}{n+1} \qquad (4.2)$$

Here n is the power factor and V_{th} is the threshold voltage of the TFT. This is how the threshold voltage is extracted. If threshold voltage and power factor *n* is known then k' factor could be easily calculated. Table 4.1 shows the threshold voltage, power factor *n* and k' factor when TFTs were exposed to light of 410 nm wavelength, both with and without bias stress of -20 V. In conventional MOSFETs, drain current has a quadratic relation with the overdrive voltage

but it is not the case for a-IGZO TFTs. a-IGZO TFTs drain current is proportional to the *n*th power of overdrive voltage which is shown in equation 4.3.

$$I_{DSAT} = k'. (V_{gs} - V_{th})^n \qquad (4.3)$$

Power factor *n* gives the idea about the distribution of tail states near the conduction band. The deep states in the band gap follow Gaussian distribution whereas the tail states near the conduction band exhibit exponential distribution.

Table 4.1 Effect of Bias-Illumination stress on various parameters of the TFTs

Standalone illumination stress with violet (410 nm) light				
Stress time (s)	Vth (V)	slope	n	k' ($A.V^{-n}$)
NS	-1.7	0.364	1.75	1.94E-07
10	-3.1	0.362	1.76	1.86E-07
100	-4.7	0.375	1.67	2.56E-07
1k	-5.5	0.383	1.61	3.19E-07
5k	-6.2	0.380	1.63	3.02E-07
10k	-6.5	0.3967	1.52	4.44E-07
15k	-7	0.3960	1.52	4.30E-07
20k	-7.3	0.403	1.48	5.09E-07
25k	-7.5	0.405	1.47	5.30E-07
-20 V bias stress along with illumination stress of violet light				
Stress time (s)	Vth (V)	slope	n	k' ($A.V^{-n}$)
NS	-1.5	0.343	1.91	8.86E-08
10	-2.5	0.353	1.84	1.20E-07
100	-8.3	0.367	1.73	1.78E-07
1k	-14.3	0.365	1.74	1.68E-07
5k	-17.5	0.371	1.69	2.03E-07
10k	**Device Failed**			

TFT *turn on* voltage depends on the deep states in the band gap and ON current depends on the tail states near the conduction band [55]. As the TFTs were exposed to the light of 410 nm with and without -20 V gate bias, it has been found that, the power factor *n* decreases in both the occasions. This suggests that the density of the tail states from the conduction band to the deep of band gap, increases as the stressing period increases. This increment of density of states actually facilitates the conduction of excess carriers, which eventually resulted in the early *turn on* and higher ON current of the TFTs. After extracting threshold voltage, power factor and k', attention has been given to the channel resistance (R_{DS}) and carrier mobility in the channel layer. The drain to source resistance, R_{DS} of TFTs is the combination of channel resistance and contact resistance at the channel and source/drain interface. The channel resistance degrades with the degradation of effective channel mobility. The contact resistance depends on the injection of carrier through the metal/semiconductor interface and bulk resistance of the semiconductor. It is found that the channel resistance decreases significantly for violet light stressing with and without -20 V bias stress. This phenomenon is confirmed by the increment of carrier mobility as the stressing time increases. However, for light of 467 nm, little changes have been observed in R_{DS} and channel mobility. This confirms the fact that, the lights of other wavelengths (467 nm, 532 nm) could not excite enough extra carriers which would significantly impact the channel resistance and mobility, compared to that of violet (410 nm) light. Figure 4.3 shows that the mobility increases very sharply for combined stress condition. Coherent information has been found from the extraction of R_{DS}. For MOS like devices the drain to source resistance,

$$R_{DS} = R_{channel} + R_{contact} \qquad (4.4)$$

$$R_{channel} \approx \frac{L}{W.k'.(V_{gs} - V_{th})^{n-1}} \qquad (4.5)$$

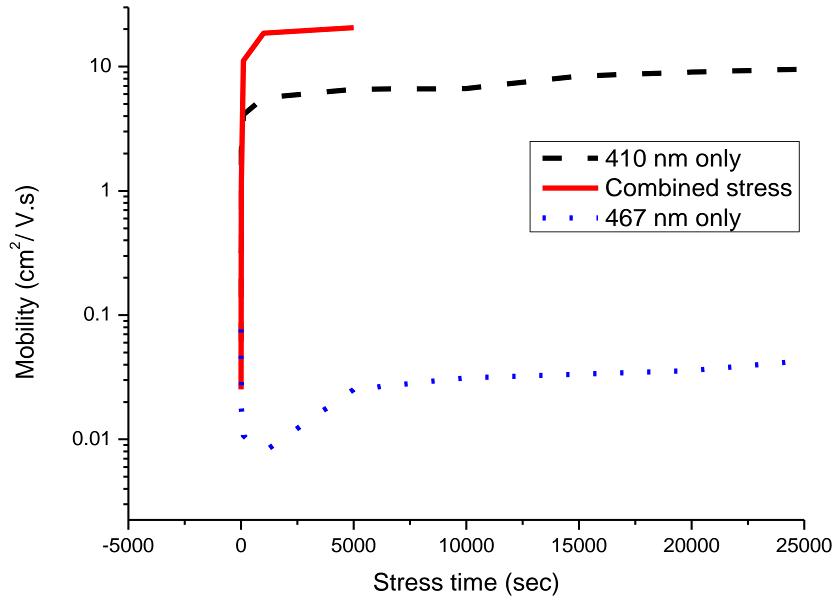


Figure 4.3 Channel mobility against stress time for various stressing condition

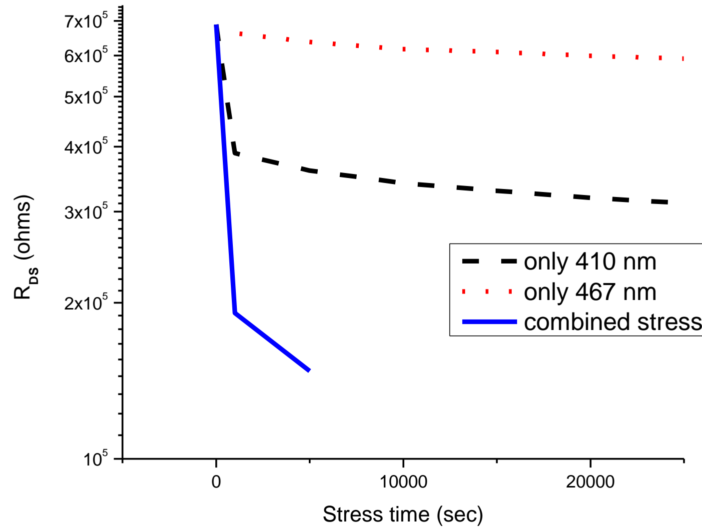


Figure 4.4 R_{DS} against stress time for various stressing condition

Figure 4.4 clearly shows that the R_{DS} drops severely due to combined stressing, which verifies the drain induced barrier lowering (DIBL) phenomenon at the source/channel interface, explained in chapter II. Results demonstrate that, as effective channel mobility increases, R_{DS} decreases. This could also be seen from table 4.1, where the k' factor increases with the stressing time which is directly proportional to the channel mobility. Moreover, the channel mobility is also related to the power factor *n,* which is shown in equation 4.6.

$$\mu_{eff} = \mu_{band} \cdot \frac{N_c}{N_o} \cdot \left(\frac{N_o}{N_{tc}}\right)^{n/2} \text{ where } N_{tc} > N_o \qquad (4.6)$$

Here N_o is a reference concentration, N_c is the free electron concentration and N_{tc} is the concentration of the trapped electrons. From this equation, it is also evident that, as power factor *n* increases with stressing period, channel mobility also increases. This agrees with the results extracted from the TFTs.

It has been mentioned previously that the drain current of TFTs depends on the *n*th power of the overdrive voltage. That is why the transconductance, g_m of these transistors are different from the conventional MOSFETs. The transconductance of these TFTs is given in equation 4.7.

$$g_m = n.\ k'.\ (V_{gs} - V_{th})^{n-1} \qquad (4.7)$$

That means, with longer stressing period, the transconductance of the TFTs increases however the trend reverses when bias stress is applied [50].

4.5 Conclusion

This chapter illustrated the effect of longer illumination stress on the TFT circuit parameters. Extraction of threshold voltage, power factor *n,* k' factor, R_{DS} and channel mobility provided a better understanding about the effect of illumination stressing with or without

negative bias stress. Extracted parameters showed results which is congruent with the physical phenomenon responsible for the variation of these parameters under stressed condition. The mechanisms elaborated in chapter II, have been verified by the results of this chapter. It showed that the power factor n increases as the stressing period increases, which means the density of the tail states near the conduction band increases. This facilitates the conduction of excess carriers that has been excited from the trapped states or neutral oxygen vacancies. Moreover, combined stressing showed abrupt increase in carrier mobility and decrease in R_{DS} which eventually drove the TFT into failure condition.

CHAPTER V

SUMMARY AND FUTURE WORKS

5.1 Summary

This thesis work mainly focused on the behavior of a-IGZO TFTs under Bias-Illumination stressed condition. Testing of the TFTs under practical stress (Bias and Illumination simultaneously) condition is extremely important, because the TFTs will be exposed to both of these stresses when it will be incorporated in an integrated circuit. As a relatively new material, there is not enough information about its behavior under extreme conditions. After its advent as a potential material for the channel layer of TFTs, researchers studied its behavior under bias stressed condition, extensively. A lot of literature could also be found for a-IGZO film and TFTs when it is exposed to light stress. However, there were very little on the performance of TFTs when they are subjected to practical stress condition, until Rajitha *et al*. reported it in June 2012.

Chapter I of this work discussed the background of TFTs with different materials as the channel layer. Initially it discussed the conventional TFTs and its application in different display technologies. Later on it brought up the issue of enhanced performance from the TFTs due to the advent of high performance display technologies. Then it discussed the opportunity of amorphous mixed oxide TFTs to meet those demands which opened the door for a-IGZO as a channel material for the TFTs. It followed on to explain the advantages and disadvantages of a-IGZO as a material for the channel layer of the TFTs and compared its performance with earlier TFTs made of a-Si:H and poly silicon materials. Table 1.1 provided a comprehensive

understanding of these three types of materials and their related advantages and disadvantages as a channel material for the high performance TFTs.

After brief introduction to TFT history and potential of a-IGZO as a channel material for the high performance TFTs, Chapter II starts discussing the TFT behavior under varied stressed condition, thoroughly. The main focus of this chapter, is to find a way to improve TFT performance and stability which degraded due to bias-illumination stressing for a longer period of time. At first this chapter reported the results of bias stress on TFTs, both positive and negative. It discussed the physical phenomenon that is responsible for such changes or degradation of TFT performances. Then it discussed the effect of standalone illumination stress for lights of various wavelengths. It illustrated the role of deep level trap states and oxygen vacancies when the TFTs are subjected to illumination stress. After discussing the effect of both bias and illumination stress separately, TFT performance has been tested when both types of stresses were applied simultaneously. As stated previously, -20 V gate bias and 410 nm light driven the TFTs into failure condition when stressed for more than 5000 seconds. This chapter discussed the reason for this type of behavior and provided related I-V characteristics to elaborate the fact. After discussing all these observations under bias and illumination stresses, a solution to these problems have been sought. This thesis work, proposed low temperature post processing annealing in optimum ambient to improve the TFT performances. Initially the TFTs were annealed at 150° C in different ambient such as air, vacuum, oxygen and forming gas. Then the TFTs were exposed to standalone illumination stress and practical stress condition. It is found that the annealing in oxygen ambient improves the TFT stability significantly. For

standalone illumination stressing, the threshold voltage shift for unannealed TFTs were -17 V. However, after annealing in oxygen ambient, the threshold voltage shift reduced significantly, a mere -1.3 V shift. Forming gas annealing also showed competitive performance with threshold voltage shift of -3.3 V only. Reasons behind these improvements are also discussed in that particular chapter. Finally, the TFTs were exposed to bias-illumination stressing after performing the annealing. Under extreme stressing condition (light of 410 nm wavelength and -20 bias stress), TFTs do not fail, however they still experience significant threshold voltage shift. For combined stress condition, forming gas annealing showed better performance than oxygen annealing, with a threshold voltage shift of -16 V compared to -18.2 V of oxygen annealing.

As mentioned earlier, forming gas annealing showed improved performance of the TFTs compared to oxygen annealing for combined stressing of the devices. This prompted to investigate more about the effect of forming gas annealing on a-IGZO material, which has been presented in chapter III. In this chapter, a-IGZO films has been tested for resistivity, mobility and carrier concentration after annealing it in different ambient. Previous chapters provided that, oxygen annealing fills up the oxygen vacancies in the channel layer to provide better stability and performance of the TFTs. However, annihilating the oxygen vacancies actually reduces the carrier concentration in the channel layer which is negative for a device. For the experiments, a-IGZO film has been annealed under three different circumstances, they are vacuum only annealing, vacuum annealing followed by oxygen annealing and vacuum annealing followed by forming gas annealing. Then these three types of samples along with the unannealed sample have been tested for resistivity, carrier concentration and mobility. It is found that vacuum annealing

creates more vacancies in the film, which is confirmed by the oxygen resonance analysis of the films. This increment of vacancies give rise to carrier concentration in vacuum annealed sample, causing a great damage to the film mobility and resistivity. However, the sample with oxygen annealing showed far less carrier concentration and enhanced mobility and film resistivity. It is noticeable that, less carrier concentration means less current flow through the film which is not desirable from a high performance TFT, integrated in advanced display technology circuits. On the other hand, sample with forming gas annealing showed reasonable performance, in terms of carrier concentration, mobility and resistivity. Forming gas helps to reduce the extra carrier concentration which drives the TFTs into failure or unstable condition. However, it also maintains a better carrier concentration than oxygen annealed sample and a better carrier mobility than the vacuum annealed sample. Further studies can be done to understand the effect of forming gas annealing on the performance of a-IGZO TFTs.

Finally, chapter IV discusses the effect of illumination and bias-illumination stressing on the electrical parameters of the TFTs. It has been observed that the bias and illumination stress have little effect on the subthreshold swing of the TFTs, which suggest that these stressing have no impact on the channel and dielectric interfacial states. However, this chapter investigates the parameters like threshold voltage, channel mobility, channel resistance, power factor n and k' factor. TFTs were subjected to illumination stressing under lights of different wavelengths. However, light of 410 nm showed highest threshold voltage shift, that is why only this case has been studied more extensively than the other cases. Results showed that power factor n decreases as the stressing time increases which suggests that the distribution of states in the conduction

band changes. Moreover, the channel mobility increased and channel resistance decreased significantly which is in line with the findings of chapter II. Finally, this chapter shows the analysis for the combined stressing on the TFTs. It shows the variation in channel mobility, resistance and power factor n, to better understand the physical phenomenon responsible for this type of behavior. Results found in this chapter are complementary to those found or explained in chapter II. So this chapter acts as a verifying tool to confirm the impact of illumination and bias-illumination stress on a-IGZO TFTs.

5.2 Future Work

As stated earlier, most of the stability issues of the amorphous mixed oxide TFTs are associated with the deep level defects or vacancies present within the matrix. To have better understanding of these defects sites, Deep level transient spectroscopy (DLTS) could be used on the amorphous mixed oxide thin films. Moreover, more information could be gathered on the interface states between dielectric and semiconductor materials. As many of the modern technologies will have flexible display system, it is very important to test the stability issues of a-IGZO TFTs under mechanical stress. Comprehensive studies on the kinetic stress of amorphous indium zinc oxide TFT has been done previously. Similar studies could be done on a-IGZO TFTs to better understand the devices.

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