Evaluation and Characterization of Silicon MESFETs in Low Dropout Regulators

by

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ABSTRACT

The partially-depleted (PD) silicon Metal Semiconductor Field Effect Transistor (MESFET) is becoming more and more attractive for analog and RF applications due to its high breakdown voltage. Compared to conventional CMOS high voltage transistors, the silicon MESFET can be fabricated in commercial standard Silicon-on-Insulator (SOI) CMOS foundries without any change to the process. The transition frequency of the device is demonstrated to be 45GHz, which makes the MESFET suitable for applications in high power RF power amplifier designs. Also, high breakdown voltage and low turn-on resistance make it the ideal choice for switches in the switching regulator designs.

One of the anticipated applications of the MESFET is for the pass device for a low dropout linear regulator. Conventional NMOS and PMOS linear regulators suffer from high dropout voltage, low bandwidth and poor stability issues. In contrast, the N-MESFET pass transistor can provide an ultra-low dropout voltage and high bandwidth without the need for an external compensation capacitor to ensure stability. In this thesis, the design theory and problems of the conventional linear regulators are discussed. N-MESFET low dropout regulators are evaluated and characterized. The error amplifier used a folded cascode architecture with gain boosting. The source follower topology is utilized as the buffer to sink the gate leakage current from the MESFET. A shunt-feedback transistor is added to reduce the output impedance and provide the current adaptively. Measurement results show that the dropout voltage is less than 150 mV for a

1A load current at 1.8V output. Radiation measurements were done for discrete MESFET and fully integrated LDO regulators, which demonstrate their radiation tolerance ability for aerospace applications.

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CHAPTER 1

INTRODUCTION

Metal Semiconductor Field Effect Transistors (MESFETs) utilize a Schottky gate (metal-semiconductor) to control the device. It was first developed in 1966 [1]. Conventional MESFETs are fabricated using compound semiconductors such as GaAs and are usually used for RF and microwave applications. The research group at ASU has demonstrated that the MESFET can be fabricated on commercial partially depleted (PD) SOI CMOS processes without any changes to the process flow [2][3]. Devices on a SOI substrate have lower parasitic capacitance and leakage current compared to those on a bulk silicon substrate. It has been demonstrated that the Si-MESFETs from ASU have high breakdown voltage and over 35GHz cut-off frequency [4]. Although these Si-MESFETs cannot compete with their GaAs counterparts for high frequency performance, they can be integrated with CMOS, which will reduce the cost of certain analog circuits. In this chapter, an introduction of the PD-MESFETs will be given, including their structure, fabrication, operation and the applications.

1.1 MESFET DEVICE STRUCTURE AND FABRICATION

Figure 1 shows the cross-section view of the n-type PD-MESFET. Compared to a conventional GaAs three-terminal device, it has four terminals including the substrate. The n-MESFET is fabricated on an n-well since it is a majority carrier device. A Schottky gate is formed with the silicide and the lightly doped n-well. The source and drain area

are heavily doped and are also processed with silicide to reduce the contact resistance. Two spacers are inserted between the gate and source and gate and drain to prevent shorting between them. The access length is defined as the length of spacer on the source side (L_{aS}) and drain side (L_{aD}). The gate length (L_g) is defined as the distance between the two spacers [6].

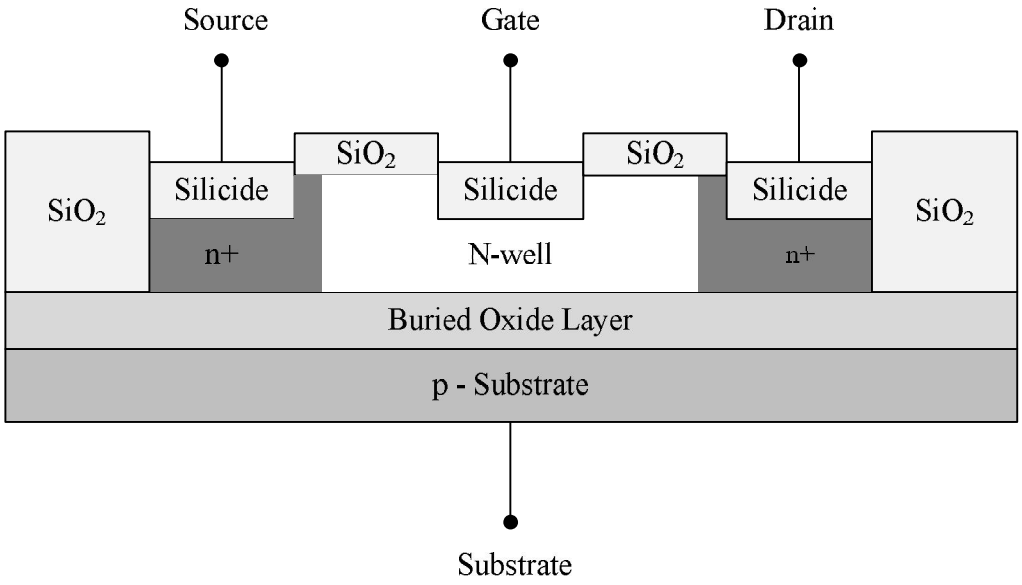


Figure 1. Cross sectional view of the n-type SOI MESFET.

The MESFETs can be fabricated in a standard SOI process. The steps to fabricate a MESFET are the same as MOSFET until the LOCal Oxidation of Silicon (LOCOS) step, which is used to form the active region of the substrate. After the well is patterned, the gate for the MOSFET will be formed while nothing is done during this step for the MESFET except the wafer cleaning, which will make the channel slightly thinner. After that, the silicide block layer will result in silicon dioxide (SiO_2) being patterned. This forms the Schottky gate and also the spacer regions between the gate and the source/drain.

The oxides that are not required for the sidewall spacer and the silicide block region will be removed. Ion implantation will be used to form the source and drain area for the MOSFET and the MESFET. During this step, a layer is necessary to cover the channel of the MESFET to make it lightly doped which is necessary in order to make a Schottky gate. As discussed later, modern CMOS technology has some additional process steps, specifically implants, which can affect the performance of the device. After the implant of the source/drain area, the exposed silicon will react with the cobalt, which will create a low-resistance contact after the annealing. The rest of the fabrication process steps are the same as for the CMOS.

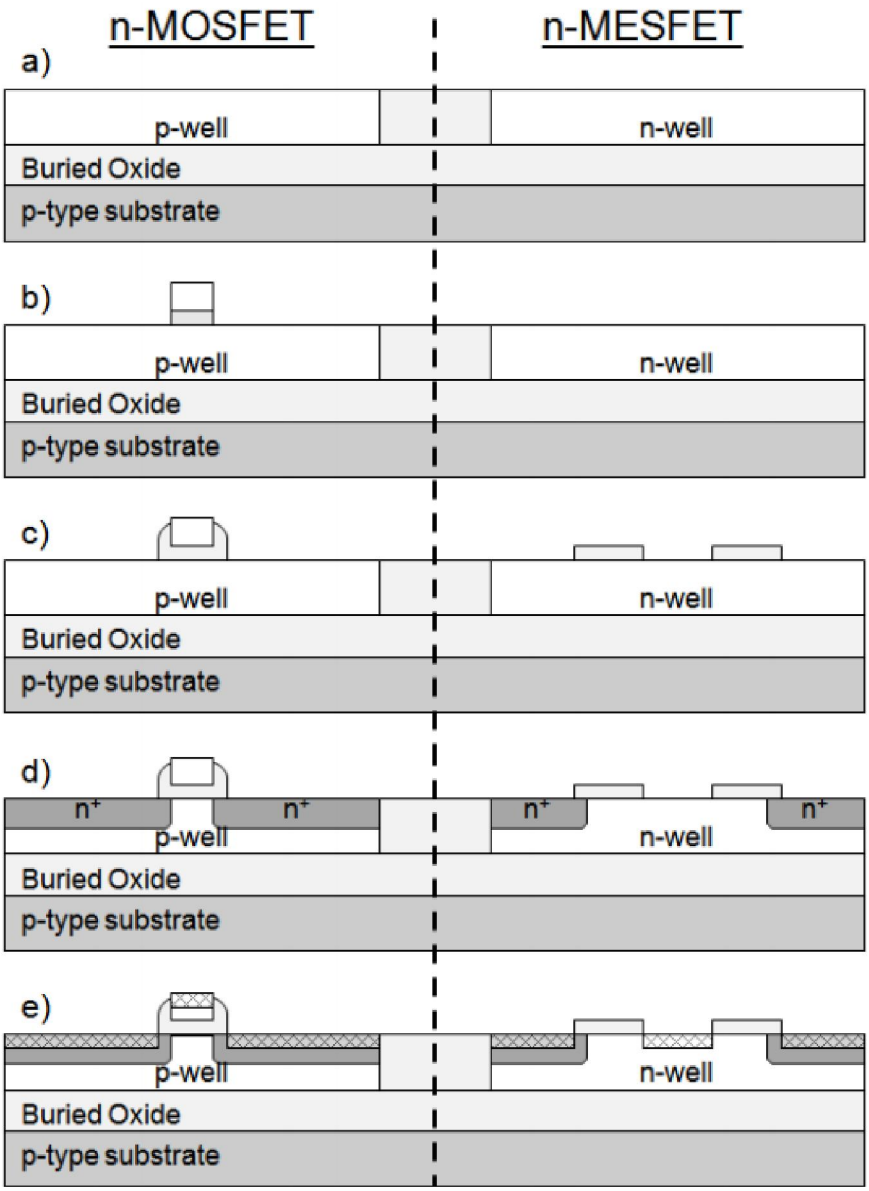


Figure 2. Fabrication step for SOI MESFET [5].

In deep submicron processes, short channel and threshold voltage effects limit the performance of the devices [7]. Modern CMOS technologies use many additional implants and doping for the well and the substrate to overcome these effects [8]. However, this is typically unwanted for the MESFET fabrication. As discussed early in this chapter,

the nearly ideal Schottky gate is formed between the silicide and a lightly doped well. Any changes to the well-doping will affect the leakage of the device. What is typically done for these processes is colleagues in the research group will go through the design kit and the manual and will identify certain drawing layers, to the best of their ability, which block some of these unwanted implants. However, modern CMOS processes are very complex and many layers are derived from various Boolean expressions. Thus, it is very difficult to block all the necessary implants while only working with the design manual. Moreover, some of the layers are restricted for internal use at the foundry.

Figure 3 shows how the leakage current changes when the drain voltage increases for an SOI MESFET on a 32nm process. As it can be seen, the leakage current goes down about 10 times. The reason why this happened has not been pointed yet been identified. It may be the trapped charge in the channel that moves forward due to the high voltage of the drain side changing the MESFET threshold voltage but it is hard to see how this can reduce the reverse bias gate leakage current. More work is required to identify the mechanisms responsible for the shift in the gate and drain currents after a high voltage is applied to the drain.

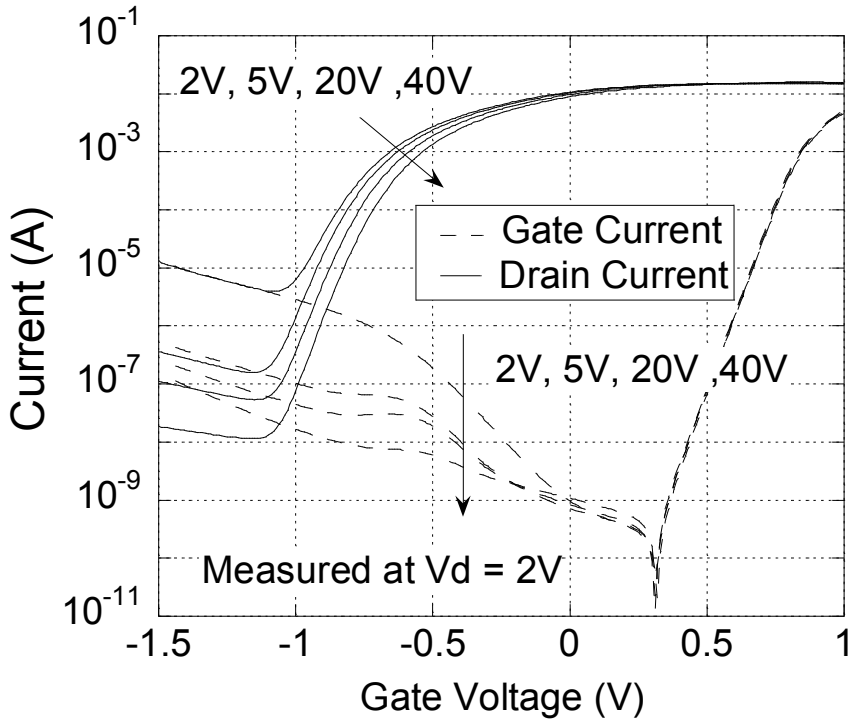


Figure 3. 32nm SOI MESFET device Gummel plots after progressive exposure to high drain voltages.

1.2 MESFET OPERATION AND CHARACTERIZATION

The MESFET is an n-channel depletion mode device which means its threshold voltage is negative. The current from the drain to the source is controlled by the width of the depletion region. Figure 4 shows the device operated in different bias regions. Figure 5 shows the Gummel plot and family of curves (FOC) results from a MESFET fabricated using the IBM 45nm SOI process. Several characteristics can be acquired from these figures, which will be discussed in the next sections.

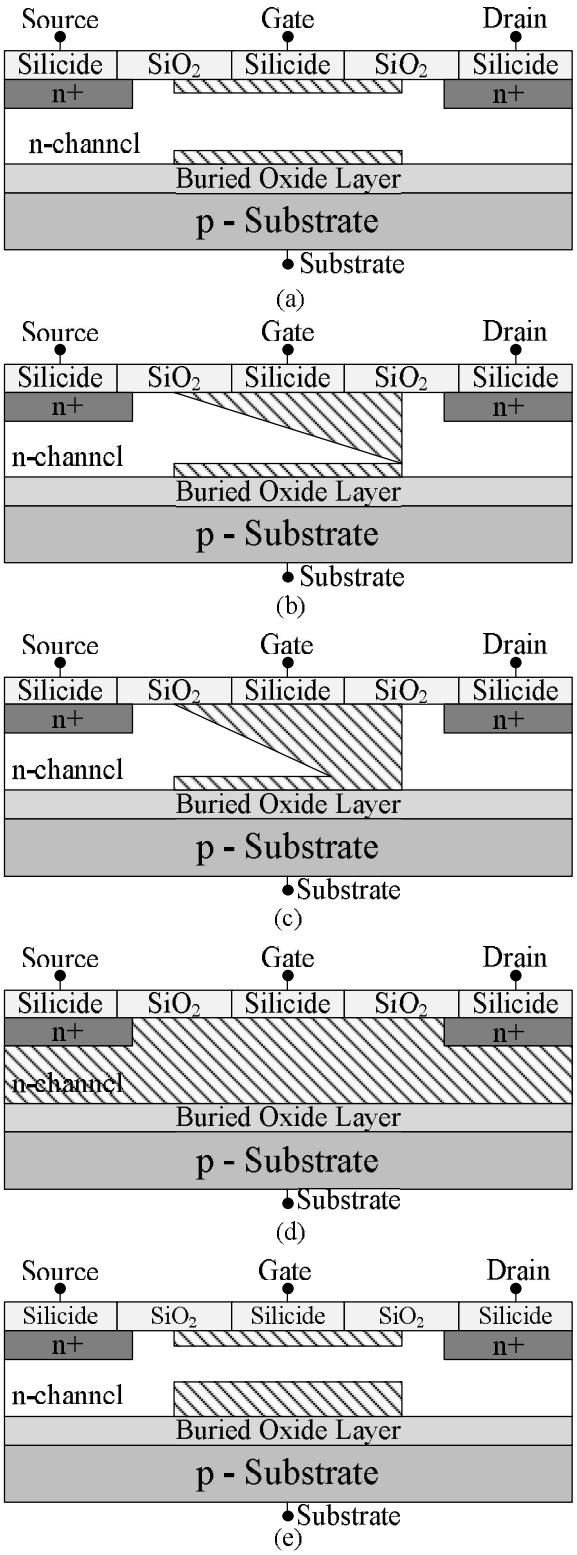


Figure 4. SOI MESFET Device Operation: (a) linear region ($V_{GS}>V_{TH}$, $V_{DS}«V_{DSAT}$), (b) the boundary between the saturation and the linear region ($V_{DS}=V_{DSAT}$), (c) saturation region ($V_{DS} > V_{DSAT}$), (d)cut-off region ($V_{GS}<V_{TH}$), (e) body effect.

1.2.1 THRESHOLD VOLTAGE

Since Si MESFETs are depletion mode devices, a channel is already present at a V_{GS} of 0V. As V_{GS} becomes more negative, the width of the depletion region under the gate will increase. When V_{GS} reaches a certain value, the depletion region will fill all the silicon region under the gate and the device will be pinched-off. Typically the threshold voltage of a SOI-MESFET is -0.5V – 1V [5]. For the SOI MESFETs, different ways can be used to change the threshold voltage. The simplest way is to modulate the back-gate of the device. Decreasing V_{BS} will increase the depletion width from the bottom of the device. This will make the threshold voltage more positive. Another way is to change the thickness of the silicide or the thickness of the channel. However, both of these may be difficult since it requires changing the process steps. One feasible method is to change the doping level of the region under the gate. Increasing the doping level of the well will make the threshold more negative since it is more difficult to pinch-off the device with the same V_{GS}. This is possible on many modern CMOS processes since there are typically more than one threshold voltage options for MOSFET devices that can be used to change the doping of the n-well.

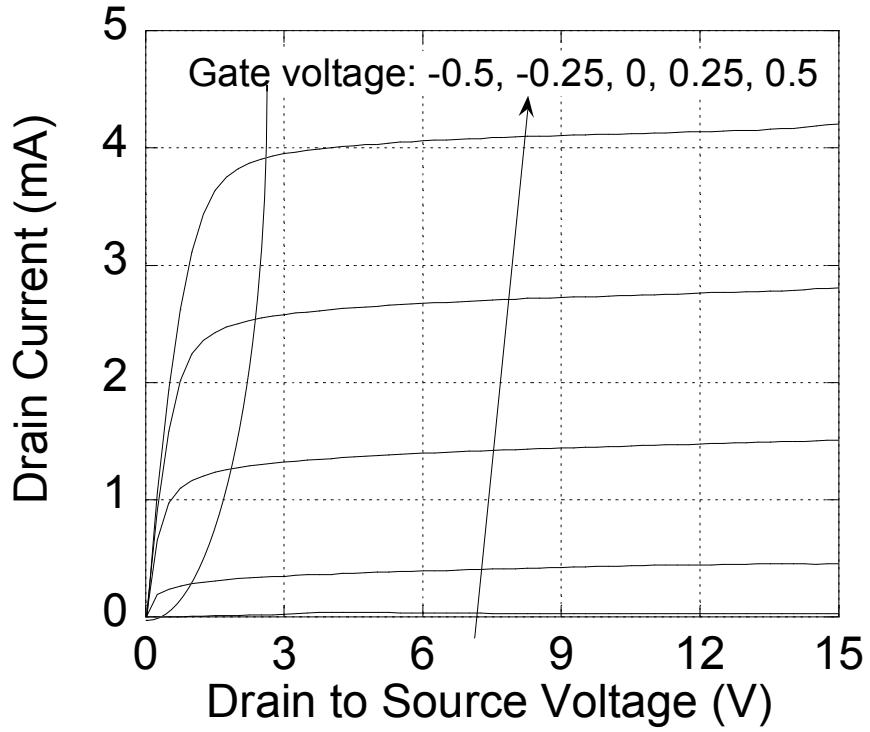


Figure 5. Family of Curves (FOC) plot of a 45nm SOI MESFET with L_{aD} = 2000nm, L_g = 200nm, and L_{aS} = 200nm.

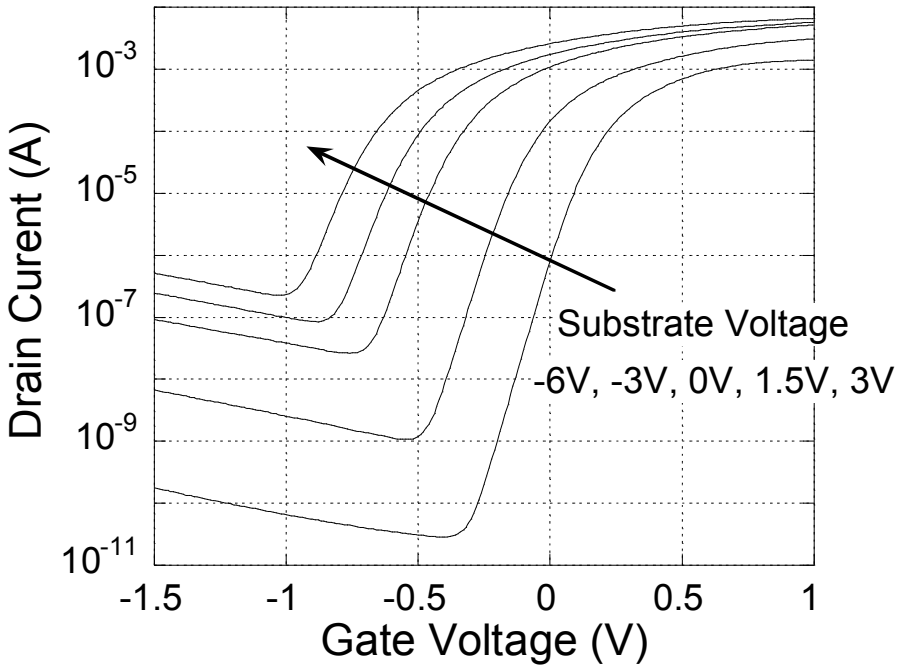


Figure 6. Threshold voltage change due to the body effect of the device. The substrate voltage is change from -6V to 3V with V_D=2V. The MESFET has an L_{aD} = 1000nm, L_{aS} = 1000nm, and L_g = 200nm.

1.2.2 DEVICE OPERATION

When V_{GS} exceeds the threshold voltage, a channel forms in the n-well. If a voltage source is applied between the drain and the source, current will flow through the channel. At this condition, the device is working in the linear region and the current will increase proportional to the source drain voltage (V_{DS}). In this region, the device will work like a resistor, whose value is controlled by the gate to source voltage. By applying a larger V_{GS}, the resistance of the device will reduce.

As V_{DS} keeps increasing, the width of the depletion region at the drain side will further increase. With enough V_{DS} voltage, the depletion region from the top will contact with the bottom one. At this time, the channel will pinch-off and the device will go into the saturation region. Further increasing V_{DS} will not increase the drain current as much as in the linear region. As a result of channel length modulation the MESFET drain current will increase slightly with increasing V_{DS}. The equations for the drain current of the device operated in the linear (1) and saturation (2) regions are shown as follows.

$$I_D = \beta(V_{GS} - V_t)^2 \tanh(\alpha V_{DS}) \quad (1)$$

$$I_D = \beta(V_{GS} - V_t)^2 (1 - \lambda V_{DS}) \quad (2)$$

where

β is the transconductance gain,

α is the saturation factor,

λ is the channel length modulation factor,

V_t is the threshold voltage of the device. [5]

1.2.3 Leakage Current and Temperature Dependence

One of the major differences between MOSFETs and MESFETs is that the latter have a leakage current due to the Schottky gate. The leakage current from the Schottky gate can be written as shown in (3) [5].

$$I_G \approx AA^*T^2 e^{\frac{-\phi_B}{U_T}} e^{\frac{V_{GS}}{nU_T}} \quad (3)$$

where

A is the conducting area,

A* is the Richardson constant,

T is absolute temperature,

Φ_B is the Schottky barrier.

Since there is a temperature dependent parameter in the drain current and gate current, the performance of the device will change with temperature. The leakage current will increase with increasing temperature, which can be described by (3). The drain current change with temperature has a corner point of V_{GS} since there are two factors changing. When V_{GS} is low, the threshold changing with temperature will dominant and the current will increase with temperature since the threshold voltage is decreasing. As V_{GS} becomes higher, the effect of the mobility will be dominant since the over-drive voltage of the device is becoming larger. Thus the current will decrease with the increasing of the temperature. This behavior is illustrated in Figure 7.

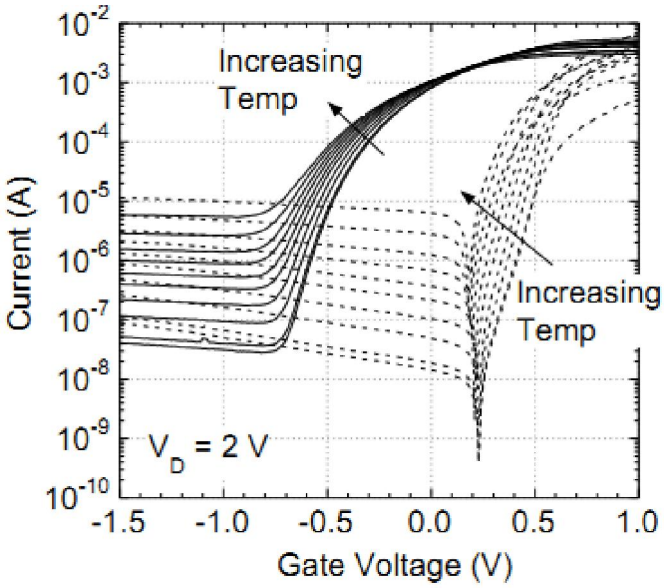
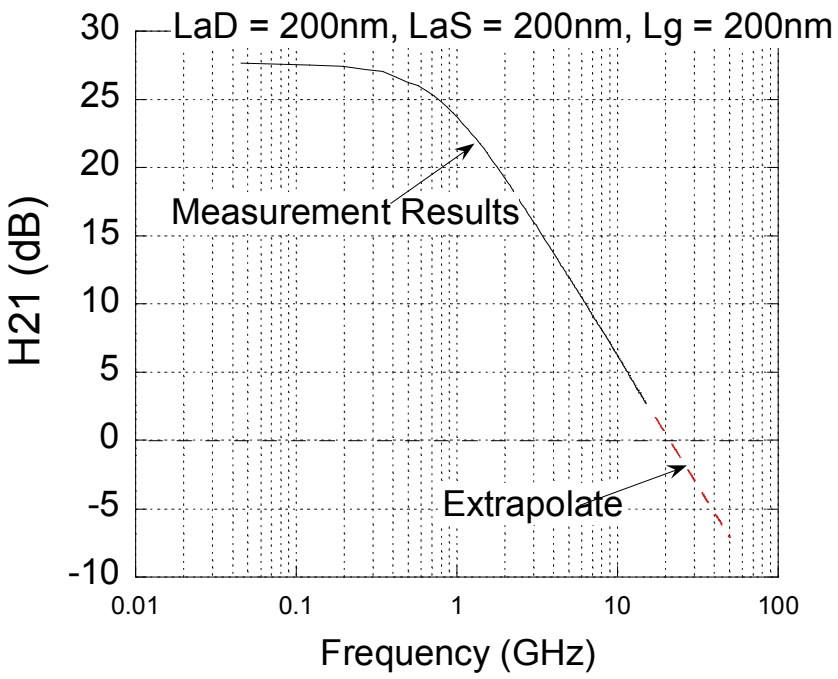


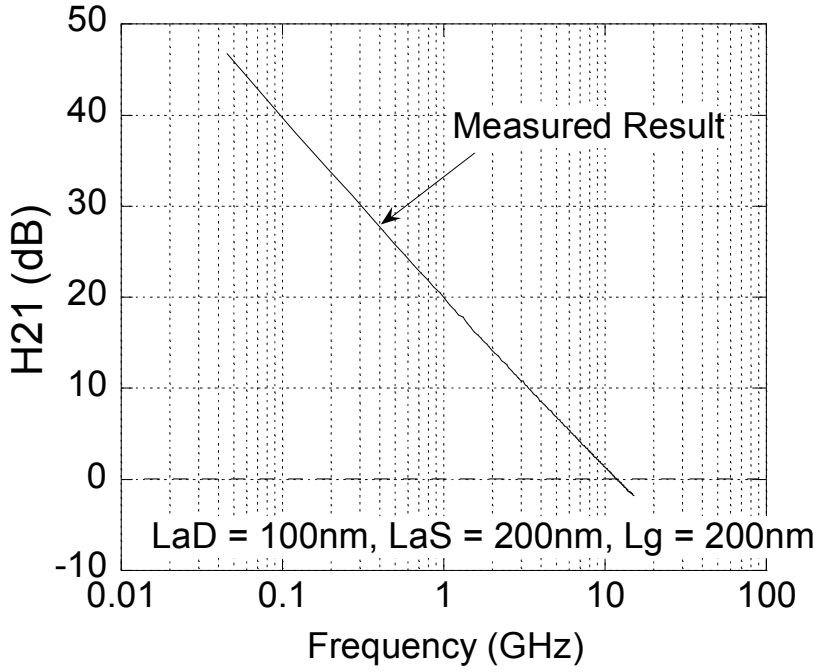
Figure 7. The device operation change with temperature from -60° to 150°. The solid lines are the drain current while the dash ones are the gate current. The device is from 350nm SOI process, $L_g = L_{aD} = L_{aS} = 0.6\mu m$ [5].

1.2.4 RF PERFORMANCE

The S-parameters of the MESFET under different biasing conditions have been measured using a vector network analyzer. In order to remove the effects of the parasitic capacitance and resistance of the pads used to probe the device, the s-parameters of the pads alone were measured first, and then removed (i.e. de-embedded) from the device results. The results are converted to h-parameters to extract the cut-off frequency. Figure 8 shows the h-parameters of the MESFET under the biasing condition that gives the peak cut-off frequency, f_T. Figure 9 shows the cut-off frequency under different biasing conditions.

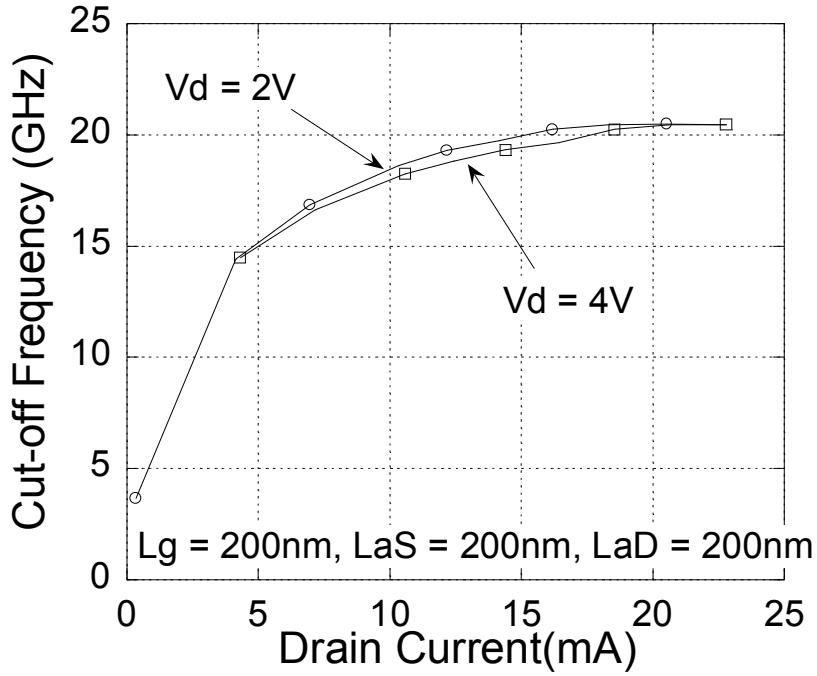


(a)

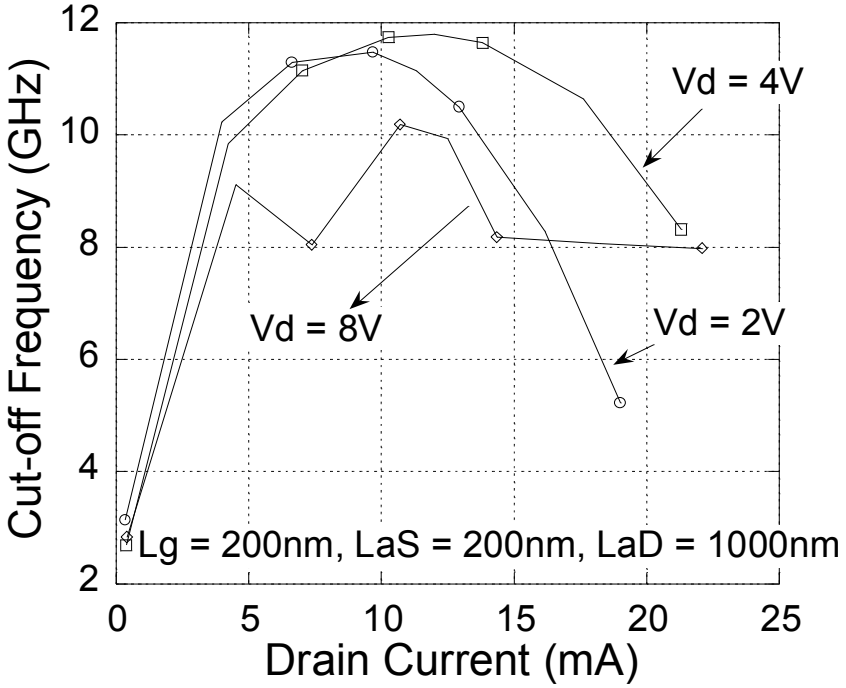


(b)

Figure 8. The measured h_{21} parameters of the MESFETs from the IBM 45nm process: (a) L_g = 200nm, L_{aS} = 200nm, L_{aD} = 200nm, V_{GS} = 0.45V, V_{DS} = 2V; (b) Lg = 200nm, L_{aS} = 200nm, L_{aD} = 1000nm, V_{GS} = 0.25V, V_{DS} = 4V.



(a)



(b)

Figure 9. The cut-off frequency of the MESFET from the 45nm IBM process: (a) L_g = 200nm, L_{aS} = 200nm, L_{aD} = 200nm; (b) Lg = 200nm, L_{aS} = 200nm, L_{aD} = 1000nm.

The cut-off frequency has a peak value with the increasing drain current. This is because of the change of the transconductance of the device with V_{GS}. The cut-off frequency of a device is given by (4)

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \quad (4)$$

where

g_m is the transconductance of the device,

C_{gs} is the gate to source parasitic capacitance,

C_{gd} is the gate to drain parasitic capacitance.

Usually, C_{gd} is much smaller than C_{gs} and can be neglected. As the change in the parasitic capacitance with respect to the biasing point is relatively small, the transconductance will dominate the change of cut-off frequency. The transconductance of the device can be extracted from the Gummel plot, as shown in Figure 10.

The cut-off frequency is also smaller for the device with larger L_{aD}, as shown in Figure 9. This is because large L_{aD} will result more parasitic capacitance (especially for Cgs). Also it will increase the parasitic resistance for the drain side and reduce the voltage that applied on it. The cut-off frequency of the device also decreases with increasing of L_{aS}. Large LaS will add more parasitic resistance to the source, which acts as the source degeneration to the device and reduce the transconductance [5].

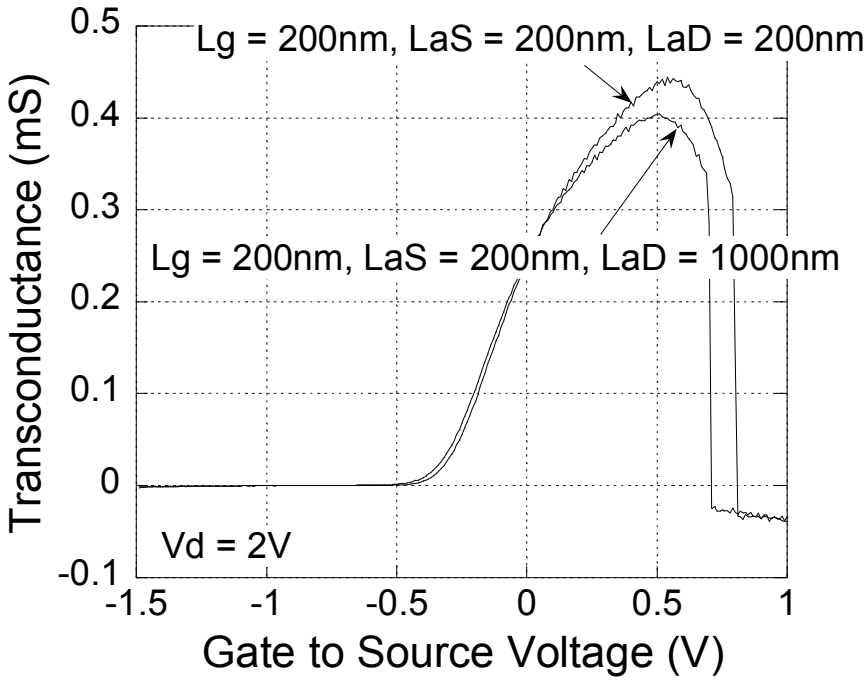


Figure 10. Transconductance of the MESFET from the 45nm IBM process, extracted from the Gummel plots, V_D = 2V.

1.3 Brief Summary of the MESFET Applications

One of the most promising applications of the SOI MESFET is that it can be used for high power RF power amplifiers (PAs) [9]. The power output is dependent on the voltage or current level. Modern CMOS devices in deep submicron technology give a high cut-off frequency as the channel length becomes shorter. However, as the process is scaled, the voltage also scales. Modern CMOS processes usually have a voltage limitation not larger than 1V. Some processes provide thick oxide transistor, which can have the ability to handle 2V. Such a low voltage limitation will have problems for designing RF PAs. For example, in order to deliver 1W (+30dBm) power to a 50 Ohm antenna, the peak current in a Class A amplifier needs to be 2A. Thus, the output

impedance of the power amplifier is 0.5Ω. To match such a small resistance to the 50Ω antenna, an impedance matching network with a large transformation ratio needs to be added. As discussed in [26], a large impedance transformation network will decrease the efficiency of the PA – see Figure 11. Moreover, the voltage drop across the parasitic resistance and inductance of the bonding wires will affect the performance of the circuit. SOI MESFETs provide a solution for these applications. With the large access length L_{aD}, the device can have a high breakdown voltage. High voltage gives a small current, which will help the impedance matching and improve the overall performance of the PA. The cut-off frequency of the 45 nm SOI MESFET is about 20 GHz, which limits the working frequency to ~2 GHz. Although it is a little lower compared to GaAs MESFET, it can be integrated on chip with the high performance CMOS for a system-on-a-chip (SoC) applications, which reduces the cost of the product.

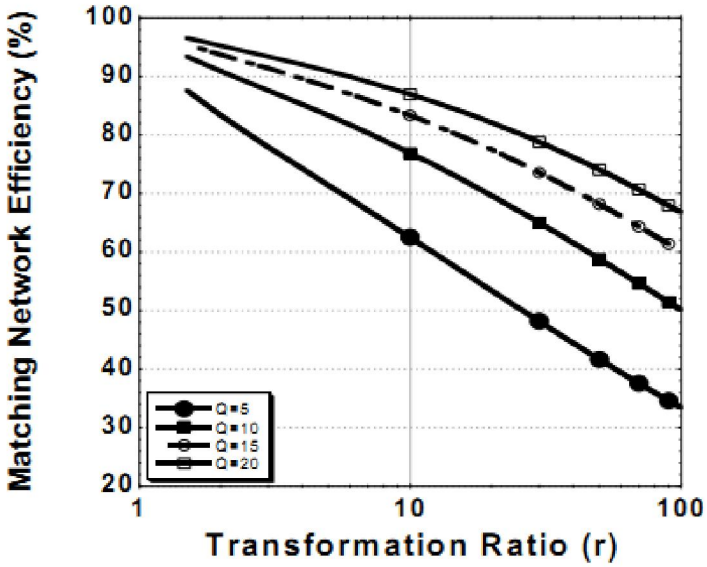


Figure 11. Matching network efficiency versus transformation ratio [26].

Another very important application for the MESFET is as the pass device of the linear regulator [10]. It enables the source follower configuration for the output stage, which gives good stability, low dropout voltage and the low noise output at the same time.

1.4 Conclusion

Silicon MESFETs have been demonstrated to be a promising device for analog and RF applications. By using the silicide to form the Schottky gate, the MESFETs can be fabricated using standard SOI CMOS processes without any further changes to the process flow. N-channel SOI MESFETs are depletion mode devices and have a negative threshold. Besides these characteristics, they have almost the same operation as the MOSFETs. Due to their high breakdown voltage and good cut-off frequency, they have potential applications for high power RF power amplifiers.

Another important application is the MESFET based linear regulator. Since the MESFET based linear regulators have been designed by another colleague in the research group [5], and this thesis will focus on their evaluation and characterization. The thesis is organized as follows. Chapter 2 will give a basic review of the design of the linear regulator, including the general parameters for evaluating the regulator and the trade-offs between n-type and p-type pass devices. MESFET based linear regulator designs will be reviewed in Chapter 3. Chapter 4 will focus on the characterization of the MESFET based linear regulator. Measurement results will be shown and analyzed. Finally, conclusion and future work will be discussed in Chapter 5.

CHAPTER 2

DESIGN THEORY OF LINEAR REGULATORS

2.1 INTRODUCTION TO LINEAR REGULATOR

Power management integrated circuits (PMIC) are one of the most fundamental and important parts in modern electronics systems. Good power management systems lead to longer stand-by time for portable devices such as cell phones and laptops. In general, power management circuits can be classified into two categories: linear regulators and switching regulators. The most popular type of linear regulars is low-dropout (LDO) regulators since they can operate with input voltages much closer to the regulated output which allows them to be more efficient. This chapter will give an introduction to the design theory of linear regulators [11].

2.1.1 LINEAR REGULATOR

Figure 7 shows the basic topology of a linear regulator, which consists of three parts: a pass device which drives the load current, a feedback network which senses the output voltage and an error amplifier, which generates the control signal. The circuit includes negative feedback and the loop is designed with high enough gain so that V_A will equal to V_B. Thus the output voltage will be V_B divided by the feedback factor. V_A often comes from a bandgap reference and is typically about 1.2V. The feedback network often is realized using a resistor divider, as illustrated in Figure 12(b). Thus the output voltage can be written as,

$$V_{out} = V_{ref} \times (1 + \frac{R_1}{R_2}) \quad (5)$$

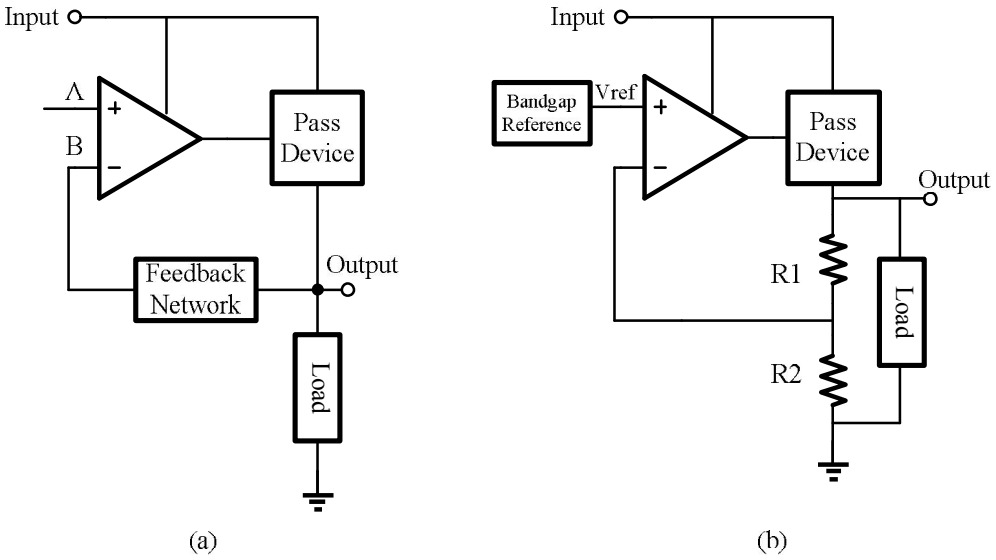


Figure 12. Linear Regulator topology: (a) General topology. (b) One with a bandgap and feedback resistors included [11].

The efficiency of the LDO regulator is shown in Equation (6) and is limited by the difference between the input and output voltage.

$$\eta = \frac{P_o}{P_i} = \frac{V_{out} \times I_{load}}{V_{in} \times I_{in}} < \frac{V_{out}}{V_{in}} \quad (6)$$

2.1.2 SWITCHING REGULATOR

Another kind of power management circuit is the switching regulator. Figure 13 shows the typical architecture for a voltage mode buck switching regulator [12]. Switches are turned on or off based on the pulsed width modulated signal generated from the controller to provide a constant output voltage. Compared to linear regulators, switching regulators can provide high efficiency. From (2), the efficiency of the linear regulators

cannot be higher than output over input voltage. On the other hand, most switching regulators offer a high efficiency. However, compared to switching regulators, linear regulators can provide a much cleaner output voltage. Due to the digital nature of the switching regulator, most of them will have a large ripple at the output voltage, while the noise of the linear regulator can be as low as the thermal noise floor of the circuit. This is why switching regulators are more suitable for digital circuits while linear regulators are more ideal for certain analog applications. [11]

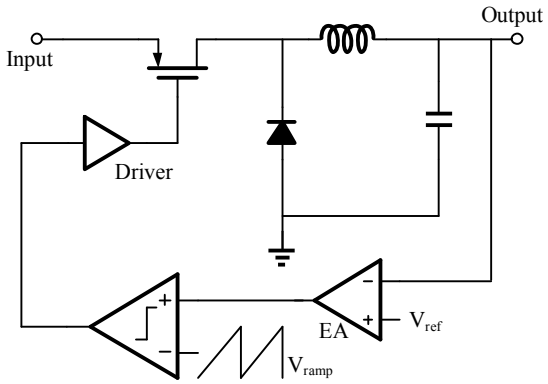


Figure 13. A typical architecture for a voltage mode buck DC-DC converter.

Another advantage of the linear regulator is its high bandwidth. Compared to the bandwidth of the linear regulator, which is limited by the poles and zeroes in the loop, the speed of the switching regulator is much lower and always limited by the switching speed. Fast switching speed will give rise to higher bandwidth; however, the efficiency decreases due to switching losses.

Since switching regulators provide high efficiency while linear regulators provide a clean signal, these two are usually designed in series to provide a better power supply. The trade-offs between linear and switching regulator are summarized in Table 1 [11]

Table 1. Comparison between switching and linear regulators

	Switching Regulator	Linear Regulator
Speed	Limited by the switches	High bandwidth
Noise	Large ripple at output	Limited by thermal noise
Efficiency	High efficiency	Poor, unless V_{IN} is close to V_{OUT}

2.2 Linear Regulator Specifications

Before going to the detail design and trade-offs, it is better to review the definition of different parameters to evaluate linear regulators. These parameters include line regulation, load regulation, dropout voltage, efficiency, transient response and power supply rejection (PSR) [13].

2.2.1 Load Regulation

Load regulation is the ability of the regulator to maintain the output voltage under different load currents. It is defined as,

$$LDR = \frac{\Delta V_{out}}{\Delta I_{out}} \quad (7)$$

The unit of the load regulation is usually mV/A. For an ideal regulator, the output voltage remains the same with different load currents. However, due to the finite gain of the op-amp, the regulated output voltage will change with the load current. Load regulation is approximately the output impedance of the regulator, which can be written as [11]

$$LDR = \frac{\Delta V_{out}}{\Delta I_{out}} = \frac{R_o}{1 + A_V \beta} \quad (8)$$

where

A_V is the gain of the error amplifier,

β is the feedback factor determined by the resistor divider,

R_O is the output resistance of the pass device.

2.2.2 LINE REGULATION

Line regulation (LNR) of the LDO is the ability of the circuit to maintain the output voltage for different input voltages. It is defined as follows [11]:

$$LDR = \frac{\Delta V_{out}}{\Delta V_{in}} \quad (9)$$

The unit for line regulation is mV/V, since the change at the output small relative to the change in the input. If a perfect reference voltage is used (i.e. it does not change with the supply voltage), the line regulation is proportional to the PSR of the regulator. Load regulation and line regulation can be improved by putting a high gain error amplifier in the loop.

2.2.3 DROPOUT VOLTAGE

Dropout voltage is defined as the difference between the input and output voltage at the point when the regulator loses regulation. Figure 14 shows a typical V_{IN}-V_{OUT} characteristic for the linear regulator. As the input voltage decreases, the transistor needs more over-drive voltage to provide the load current. When the transistor cannot provide enough current, it will enter the triode region, which will decrease the loop gain and the output cannot maintain regulation. For a LDO regulator, the dropout voltage is usually approximately proportional to the on-resistance of the pass transistor when it is in the edge of the triode region

The dropout voltage defines the lowest input voltage to maintain the constant output voltage. For a specific circuit, the highest efficiency can be obtained with the input voltage slightly higher than the output voltage plus dropout voltage. Low dropout voltage will give rise to higher efficiency, which can be acquired by rewriting the efficiency equation [11].

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} < \frac{(V_{IN} - V_{DROP}) \times (I_{IN} - I_Q)}{V_{IN} \times I_{IN}} < 1 - \frac{V_{DROP}}{V_{IN}} \quad (10)$$

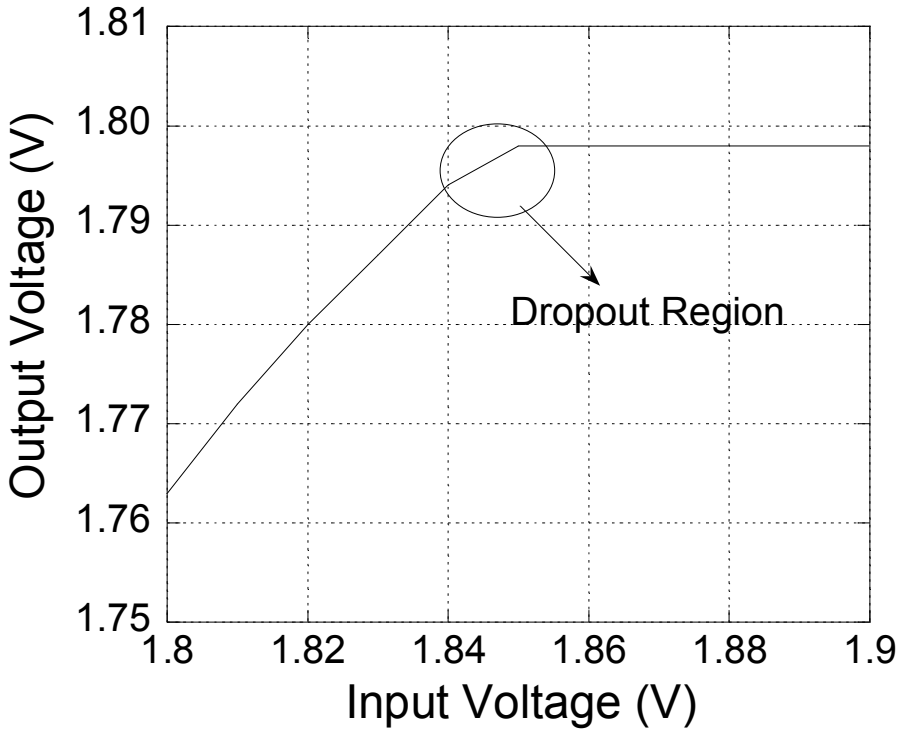


Figure 14. The typical input-output characteristic of a linear regulator.

2.2.4 POWER SUPPLY REJECTION

Power supply rejection (PSR) is defined as the ability of a linear regulator to resist high frequency noise at the input. Figure 15 shows the typical PSR response. At low frequency, the linear regulator can reject the noise due to the high loop gain. As the frequency is increasing, the gain of the error amplifier and the pass device decrease, increasing the noise at the output. The corner frequency of the PSR is usually determined by the dominant pole of the loop. Decoupling capacitors with different values will be put at the input to filter out the high frequency noise [14].

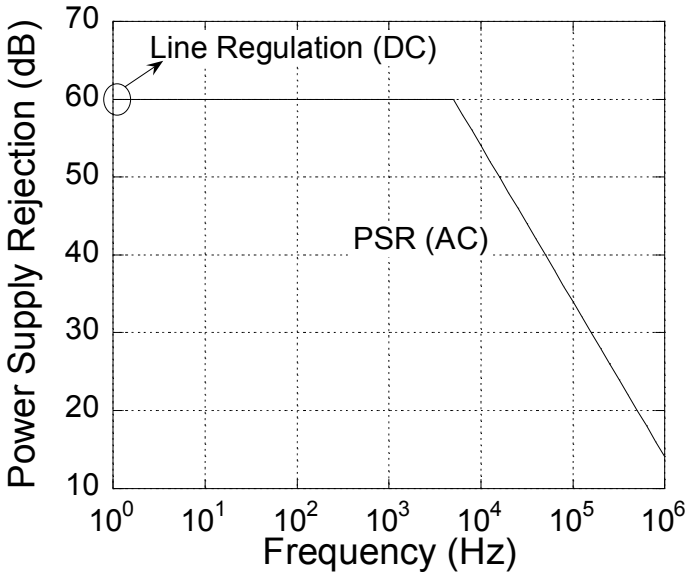


Figure 15.Typical PSR of the linear regulator versus frequency.

2.2.5 TRANSIENT RESPONSE

Transient variation is used to evaluate how the regulators response with a sudden change in the load current or the line voltage. Load transient response usually reflects the loop gain, bandwidth and stability of the regulator. For the same bandwidth, a good phase margin results a fast recover time (typical 60° for fastest) while poor stability performance will lead to ringing. Line transient response usually reflects the PSR of the regulator.

As we can see from the previous analysis, the pass device plays an important role in the performance of a linear regulator, since it has influences loop gain, bandwidth, stability and dropout voltage. In standard CMOS technology, two kinds of transistors are usually used as the pass device: PMOS and NMOS. In the following section, the design and trade-off between these two type regulators will be analyzed in details.

2.3 PMOS LINEAR REGULATOR

A typical PMOS linear regulator is shown in Figure 11. The main advantage of this topology is its low dropout voltage. For a PMOS transistor, the gate voltage is lower than the source for turning on the device. To ensure the pass device is in the saturation region to maintain regulation, the source to drain voltage of the device should be larger than the over-drive voltage. The dropout region happens at the edge of the saturation region, which is

$$V_{DROP} = R_{ON} \times I_{OUT} \quad (11)$$

where, R_{ON} is the on resistance of the pass device, I_{OUT} is the load current. This is why PMOS linear regulators are also called low dropout (LDO) regulators. In reality, the dropout voltage also includes the voltage dropped across the bonding wires and the metal lines on the chip and circuit board.

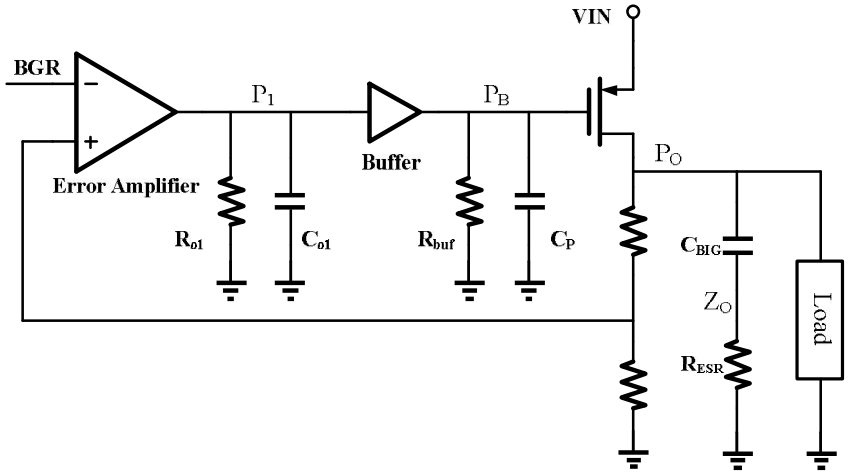
One disadvantage of this topology is the mobility of the p-type transistor, which is typically 2-3 times lower than n-type devices. In order to have a specific current driving ability, the p-type device also has to be 2-3 times larger than an n-type device. As a result, it will have much more parasitic capacitance and need more silicon area.

Another critical issue for the PMOS linear regulator is its inherent instability due to the common-source topology of the output stage. This is illustrated in Figure 16, where the error amplifier (EA) is assumed to be a single pole system. Due to the parasitic capacitance in the circuit, there are two dominant poles inside the loop, which are,

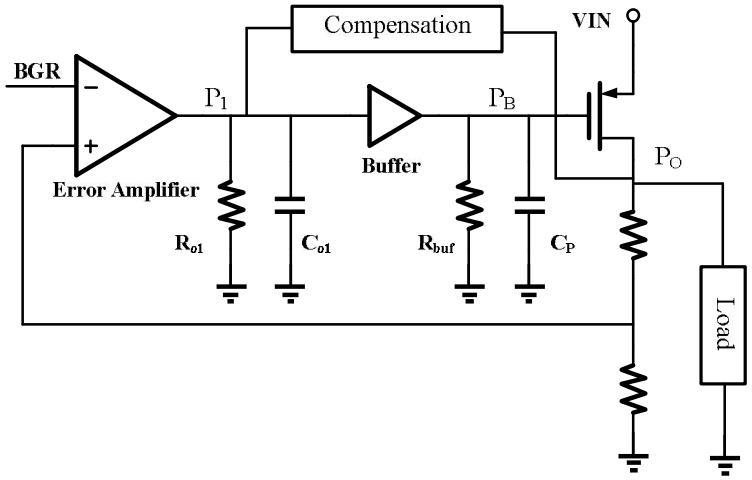
$$P_1 = \frac{1}{2\pi R_{o1} C_{o1}} \quad (8)$$

$$P_o = \frac{1}{2\pi R_{o(PMOS)} C_L} \quad (9)$$

where, R_{O1} and C_{O1} is the output resistance and capacitance of the EA respectively. $R_{O(PMOS)}$ is the output resistance of the pass device and C_L is the load capacitor.



(a)



(b)

Figure 16. PMOS linear regulator topology: (a) External compensation using big capacitor and the Equivalent Series Resistor (ESR) (2) Internal compensation.

Due to the high output impedance of the common source configuration and the high load capacitor, the location for P_o and P_1 may become very close to each other, which will result in low phase margin or even unstable operation. In order to solve the stability problem as discussed above, two types of compensation are generally used: external compensation and internal compensation [11].

External compensation is usually utilized for the conventional LDO regulator design, which means that the bandwidth is determined by the output of the regulator [11]. A big capacitor (about several micro fara) is added at the output to make P_o the dominant pole. On one hand, it can help splitting the two low frequency pole by pushing the output one further close to the origin. On the other, adding a capacitor can be used as a bypass filter to reduce the over-shoot and under-shoot due to the wire resistance and inductance when the load current changes. A buffer is usually added between the error amplifier and the pass device to further push P_1 into high frequency. Due to the load current variation and the high output impedance of the EA, the stability is still difficult to ensure. The most popular way is to take advantage of the Equivalent Series Resistance (ESR) of the output capacitor to create a left hand plane zero (LHP) to compensate for the stability, which is

$$Z_O = \frac{1}{2\pi C_O R_{ERS}} \quad (10)$$

For a conventional LDO regulator, the output capacitor must be carefully chosen to ensure the stability. Most of the conventional LDO regulators provide the specifications for the output capacitor [15]. The typical bode plot of the loop gain is shown in Figure 17.

System on Chip (SoC) is becoming more popular due to its low cost and chip size. In order to integrate the conventional LDO regulator onto a SoC design, either a large capacitor is required on-chip, or an external pin is required. The first option is hard on a CMOS process since a large area is needed to achieve the required capacitance while the second option requires additional board space. Thus, a capacitor-free LDO regulator is ideal for this particular application.

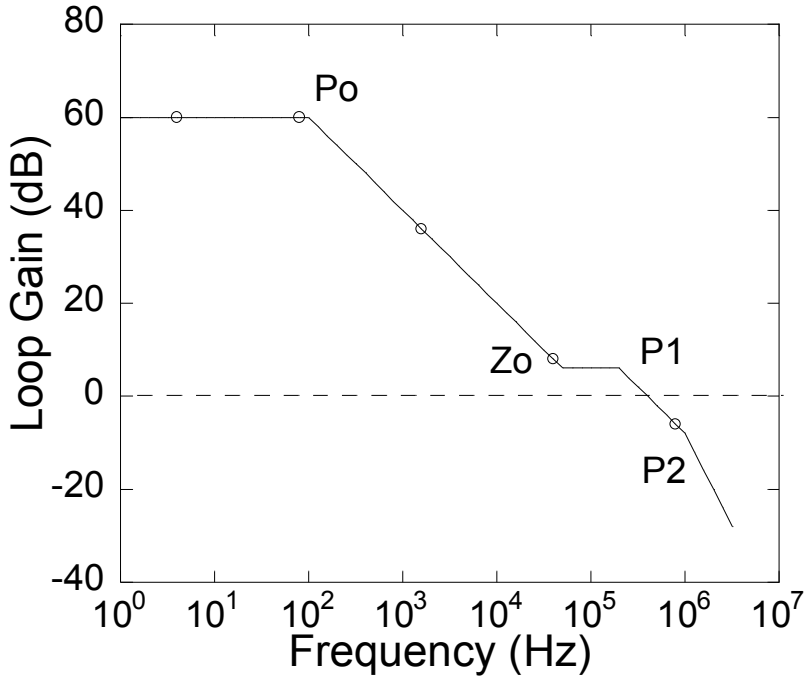


Figure 17. Bode plot of the closed-loop gain of the externally compensated linear regulator.

Compared to a conventional regulator, internal compensation is usually used for a capacitor-free regulator, which means that the dominant pole is determined inside the loop. Usually, P_1 will be designed as the dominant pole of the loop, while some techniques will be used for further splitting of P_1 and the non-dominant pole such as P_O and P_2. Unlike the conventional LDO regulator, adding capacitors at the output will decrease the phase

margin; thus giving poor load transient response. However, for SoC applications, the load capacitor and the bypass capacitor are not as large as traditional designs. Since the output resistance of the PMOS device (R_o of the transistor) is very high, the bandwidth of the capacitor-free LDO regulator is usually around a few hundred kHz. Figure 18 shows a typical Bode plot for the internally compensated linear regulator.

The PSR of PMOS linear regulators are not very good. The noise at the power supply are presented directly at the source of the PMOS, which will modulate the over-drive voltage of the pass device and change the output.

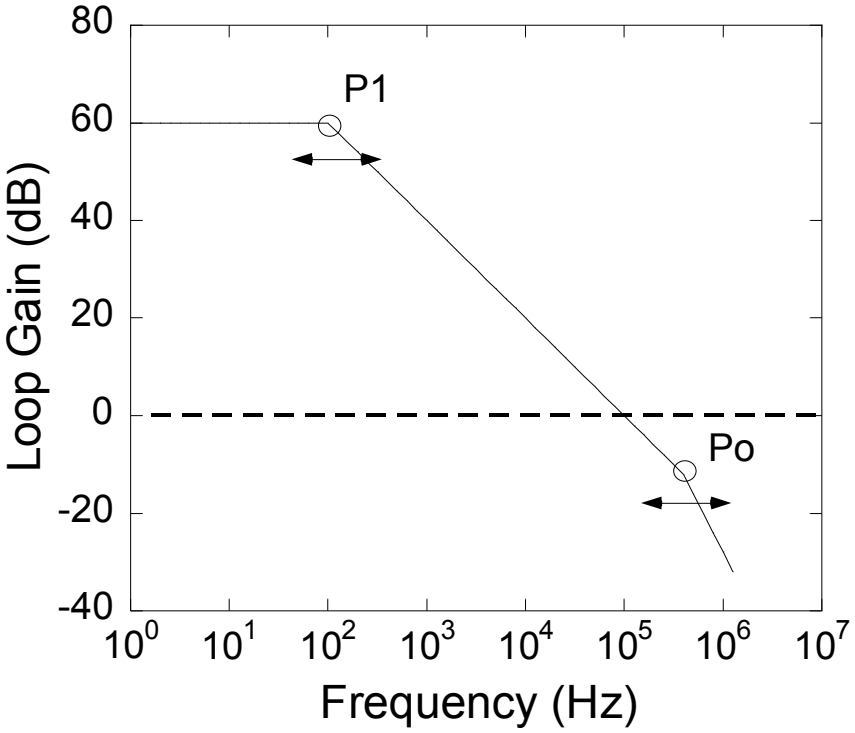


Figure 18. Bode plot of the loop gain of the internal compensated PMOS linear regulator.

2.4 NMOS LINEAR REGULATOR

An n-channel MOSFET can also be used as the pass device of the linear regulator. A typical NMOS regulator is shown in Figure 14. Compared to p-type devices, the mobility of electron is usually faster, thus requiring smaller silicon area to provide for the same current driving ability. The main drawback of this topology is its high dropout voltage. In order to make the NMOS work properly, the gate voltage (V_G) must be higher than the output plus the threshold voltage, which is typically about 600mV-1V due to the body effect. For a normal circuit, V_G cannot exceed the supply voltage. Thus

$$V_{DROP} = V_{IN} - V_{OUT} > V_G - V_{OUT} = R_{on} \times I + V_{TH} \quad (11)$$

where V_{TH} is the threshold voltage of the pass device. Equation (11) shows that the dropout voltage of the NMOS linear regulator includes the threshold voltage and will be higher than PMOS linear regulator. In order to remove V_{TH} from dropout voltage, a charge pump can be added to boost the gate voltage higher than the supply [16]. However, such a circuit will introduce switching noise to the circuit, losing the natural advantage of the linear regulator.

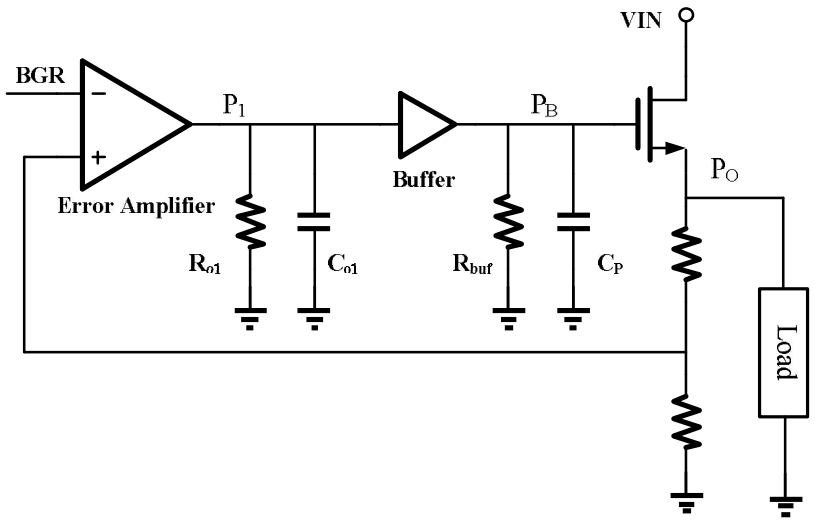


Figure 19. NMOS linear regulator topology with internal compensation being used [5].

An advantage of the NMOS linear regulator is its good PSRR performance. Since the supply voltage is added to the drain of the pass device, the NMOS device works as a cascode device to shield the output [17]. Another important advantage of the NMOS linear regulator is the better stability performance compared to PMOS regulators.

As illustrated in Figure 19, there are still three poles in the loop. However, the output impedance of the NMOS in common-drain configuration is $1/g_m$ since the output is looking into the source compared to R_O of the PMOS linear regulator. Thus the output pole is at a relative high frequency. The equation for each pole is given below.

$$P_1 = \frac{1}{2\pi R_{o1} C_{o1}} \quad (12)$$

$$P_1 = \frac{1}{2\pi R_{o1} C_{o1}} \quad (13)$$

$$P_O = \frac{gm_{NMOS}}{2\pi C_o} \quad (14)$$

Internal compensation is usually utilized for NMOS linear regulator. A simple way is adding a capacitor at the output of the error amplifier to push P_1 closer to the origin [5]. Other compensation techniques can also be utilized to further split the poles. Although internal compensation can still be used for a PMOS regulator, in order to have the same stability performance, the bandwidth is much smaller than that of a NMOS regulator. Higher bandwidth will provide a fast transient response.

2.5 CONCLUSION

Linear regulators are one of the most popular power converters for power management circuits. Compared to switching regulators, linear regulators have higher bandwidth and lower noise. Line regulation, load regulation, dropout voltage, transient response, and power supply rejection are important parameters to evaluate the performance of the linear regulator. Generally, two types of transistors, PMOS and NMOS can be utilized as the pass device for the linear regulator. The PMOS regulator provides low dropout voltage, but it has inherent stability issues, lower bandwidth and needs a larger device. The NMOS regulator has better stability and is much faster, however, it requires additional circuits like a charge pump in order to provide low dropout operation. The comparison between these two types linear regulator are summarized in Table 2.

Table 2. Comparison between NMOS and PMOS linear regulators

	NMOS	PMOS
Dropout Voltage	Low	High
Bandwidth	High	Low
Stability	Good	Poor
Area	Smaller	Larger
PSRR	High	Low

CHAPTER 3

DESIGN OF N-MESFET LDO REGULATOR

In the last chapter, the design trade-offs between NMOS and PMOS linear regulators were compared. From the loop stability perspective, the n-type pass device is a better choice. However, it suffers from either a high dropout voltage or it requires a charge pump which increases switching noise and die area. The silicon MESFET discussed in Chapter 1 solves this problem by operating in depletion mode. The threshold of the device is negative thus a charge pump is naturally removed. An N-MESFET LDO regulator is designed by one of the colleague in the research group [18]. The design principle of the MESFET LDO regulator will be reviewed in this chapter. Characterization and evaluation results are discussed in Chapter 4. Based on the measurement results, a new version LDO regulator was fabricated. Since the chips have not come back from the foundry yet, the results from the new version will not be included in this thesis.

3.1 N-MESFET REGULATOR AND DESIGN ISSUES

The size of the pass device plays an important role in the performance of the LDO regulator. The L_g of the device should remain the minimum achievable length for the process. Since the input voltage, which is at the drain of the MESFET, is limited to 2V by the constraints of the CMOS process, minimum L_{aD} and L_{aS} will be sufficient for the breakdown voltage. The size of the pass device used in the linear regulator is as follows: L_{aD} = 200nm, L_{aS} = 200nm, L_g = 200nm and W = 150mm. Figure 20 shows the drain and

the gate current versus V_{GS}. [18]

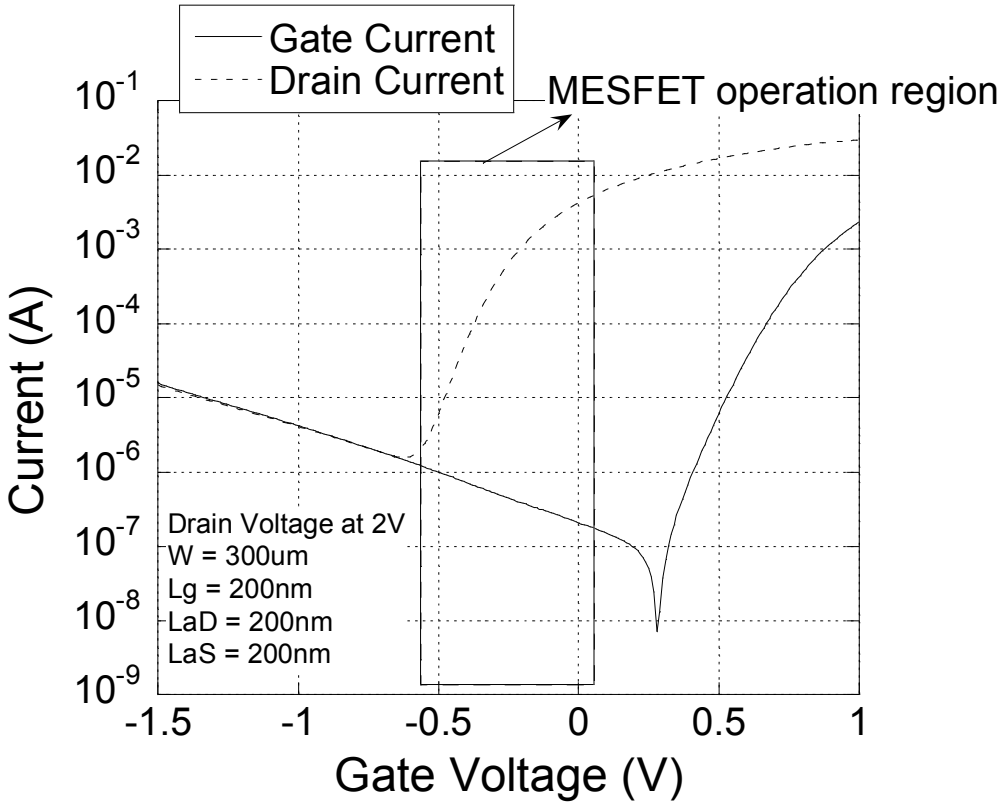


Figure 20. Scaled down pass device performance and the operating region.

When the regulator is in the dropout region, the gate voltage of the MESFET will be at its highest value in order to provide enough load current with smaller V_{DS}. In this particular case, V_{GS} will be approximately 0V since it is limited by the supply voltage. The lowest V_{GS} happens at light load currents, where the gate voltage is approaching the pinch-off point.

Compared to a conventional CMOS linear regulator, several issues need to be considered in the design of the MESFET LDO regulator. One of the major problems is the leakage current from the gate of the MESFET. From Figure 20 and the analysis in Chapter 1, it can be concluded that the leakage current flows away from the gate. Thus, the buffer needs to have the ability to sink the leakage current.

Another important issue comes from the negative threshold voltage of the MESFET. In order to operate at light load conditions (i.e. when the load current is ultra-low or the load is open), the gate voltage of the MESFET should be low enough to pinch-off the device. That requires the output of the buffer to be able to swing low enough to produce a sufficiently negative V_{GS}.

A drawback of the MESFET LDO regulator is that it cannot provide a shutdown operation. For the conventional enhancement mode device, one can push the gate to the rails to fully turn-off the regulator. To overcome this issue, an enhancement mode device can be put in series with the MESFET, which acts as a switch. The trade-off is such a device needs to be large enough to provide enough current, which will consume more silicon area. Also the voltage drop across the enhancement mode device, which is R_{ON} of the device times I_{LOAD}, will be added to the dropout voltage. Since this design required a very low dropout voltage, the series enhancement mode device was not added here.

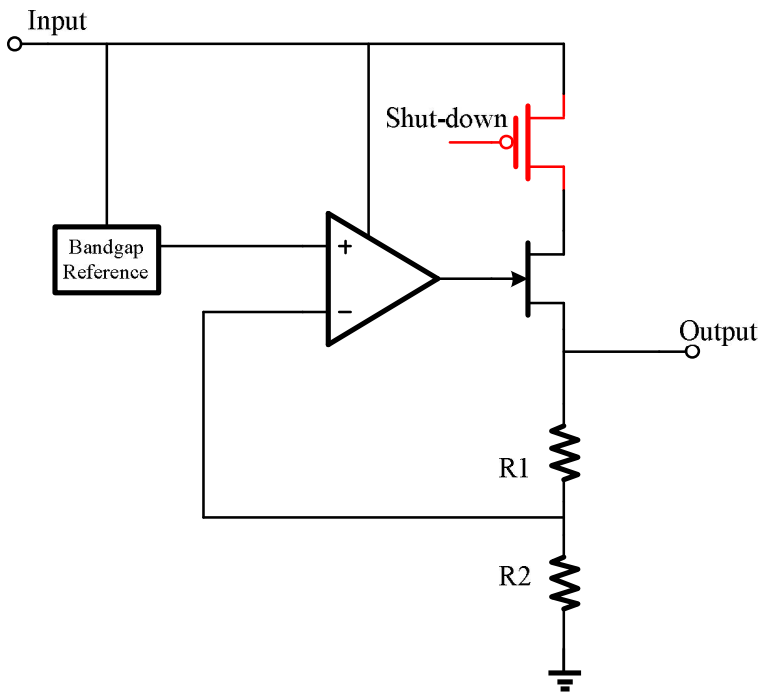


Figure 21. MESFET based LDO regulator with shut-down operation.

3.2 Error Amplifier and Buffer Design

3.2.1. Error Amplifier (EA) Design

The topology of the error amplifier used in this design is a single stage folded-cascode amplifier for its high output gain. The architecture of the error amplifier with the size of each transistor is shown in Figure 22.

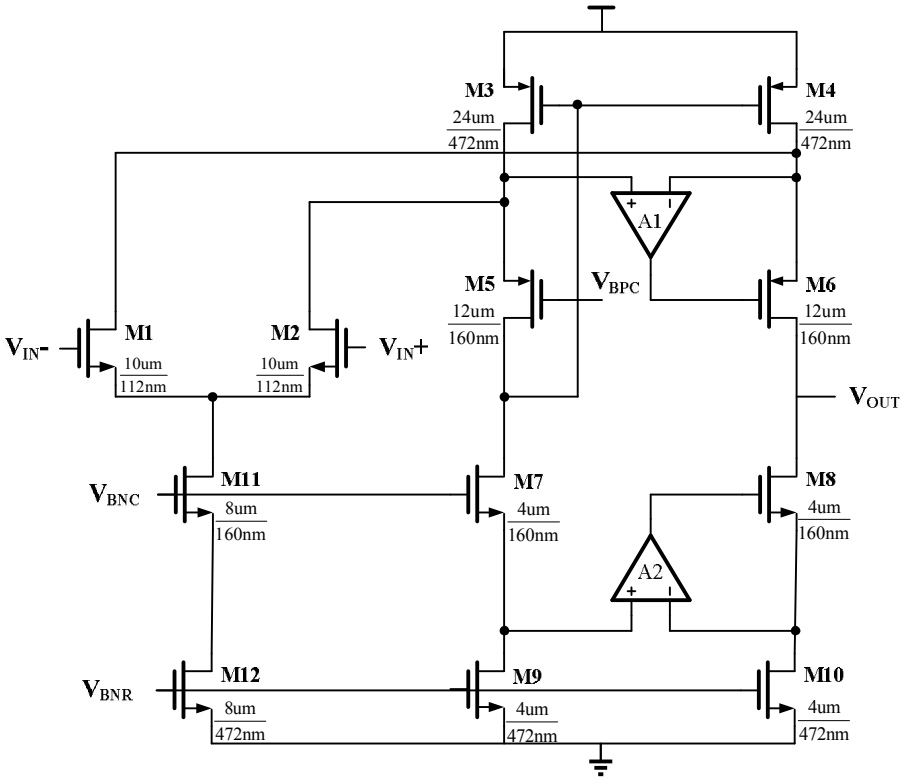


Figure 22. Folded cascode error amplifier with the device sizing.

NMOS input pairs are used for since they have high g_m. The input pair is sized to be large enough to provide sufficient g_m for high gain and bandwidth. The size of the rail current source devices are designed to have a small W/L_g ratio to limit the noise and offset contribution [19]. Cascode devices are designed with the same width as the rail device but smaller length to provide higher g_m while giving good layout matching.

Since the intrinsic gain of the transistor in 45nm CMOS process is quite low, gain boosting amplifiers are added to regulate the gates of the cascode devices to further improve the output impedance. The amplifiers are only added at the output side, since the other side does not impact the output impedance. Figure 23 shows the auxiliary amplifier schematic [20]. N-type input pairs are used for A1 while p-type ones are used for A2 for

headroom reasons. The source followers are added as the input stage to further reduce the headroom issue. Simulation results show that the transconductance of the input pair of the main amplifier is 17.23 μS and the DC gain of the entire error amplifier is 71.49dB at 1.2V common mode input voltage.

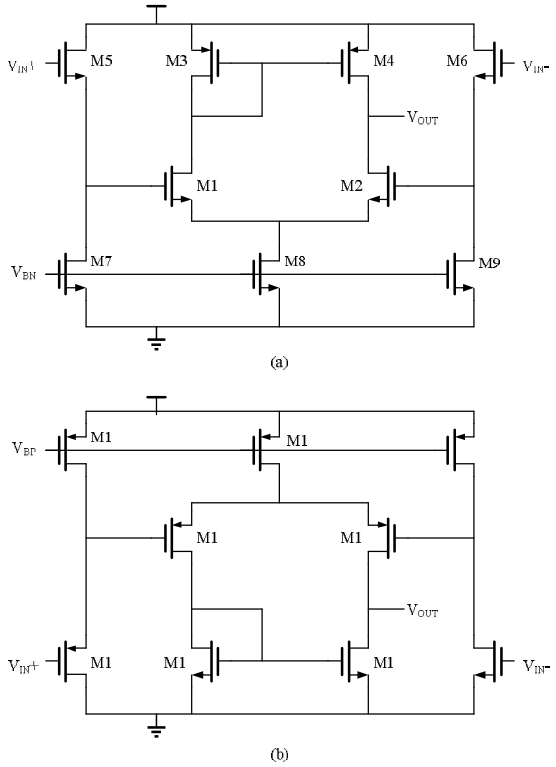


Figure 23. Auxiliary amplifiers used for gain boosting: (a) A1 have a NMOS input pair, (b) A2 has a PMOS input pair [20].

3.2.2 BUFFER DESIGN

As discussed earlier, a buffer is necessary to sink the gate current from the n-MESFET pass transistor. In this design, a PMOS source follower acts as a buffer to drive the MESFET. A shunt-feedback transistor is added between the output and the drain, as shown in Figure 24.

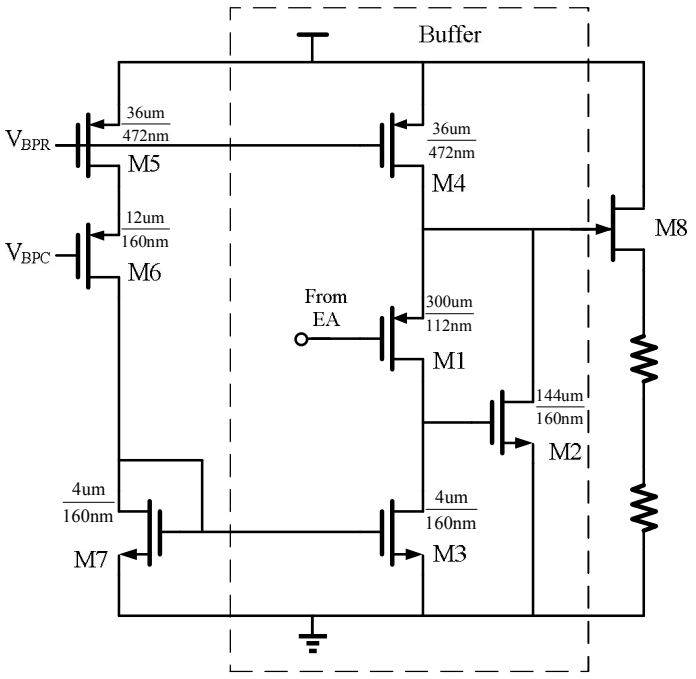


Figure 24. PMOS source follower and shunt feedback to improve the output impedance.

The output impedance of the source follower is $1/g_m$, which will contribute a non-dominant pole in the loop. Since the input capacitance of the pass transistor is quite large due to its large area, one should design the g_m of the buffer to be large enough to make a good phase margin, which will result in a large buffer transistor. Here, M2 is added as shunt feedback to reduce the output impedance [21]. It can be shown that the output impedance after adding the feedback transistor is [22]:

$$R_o = \frac{1}{(g_{m1} + g_{mb1})}\left(\frac{1}{g_{m2} r_{o2}}\right)$$

where g_{m1} and g_{mb1} is the transconductance of M1, g_{m2} is transconductance of M2 and r_{o2} is the output resistance of M2.

Besides lowering the output impedance, M2 also sinks most of the gate current from the MESFET. Whereas, using the source follower to sink the current would require the current source of M4 to be large enough. An advantage of M2 is it will adaptively change its gate voltage based on the leakage current. Such an operation will reduce the quiescent current and also save silicon area. The only limitation is that M2 needs to be large enough to sink the largest leakage current, which occurs at light load condition and at high temperature.

3.3 Stability Issues

From the stability and settling perspective, it is necessary to design the loop as a single pole system. In this design, the pole from the output of the error amplifier acts as the dominant pole, as discussed in Chapter 2. Although the output impedance of the MESFET source follower is $1/g_m$, large variations can occur based on the capacitance presented by the load which will push the second pole close to the origin and result in lower phase margin. In this design, a 2.5 pF capacitor is added at the output of the error amplifier to further push the dominant pole towards the origin [18], which will give a larger range for the variation in load capacitance. Simulation results show the phase margin is 43° with a 100nF load capacitor at 10mA load condition. The unity gain frequency of the LDO regulator is 294kHz.

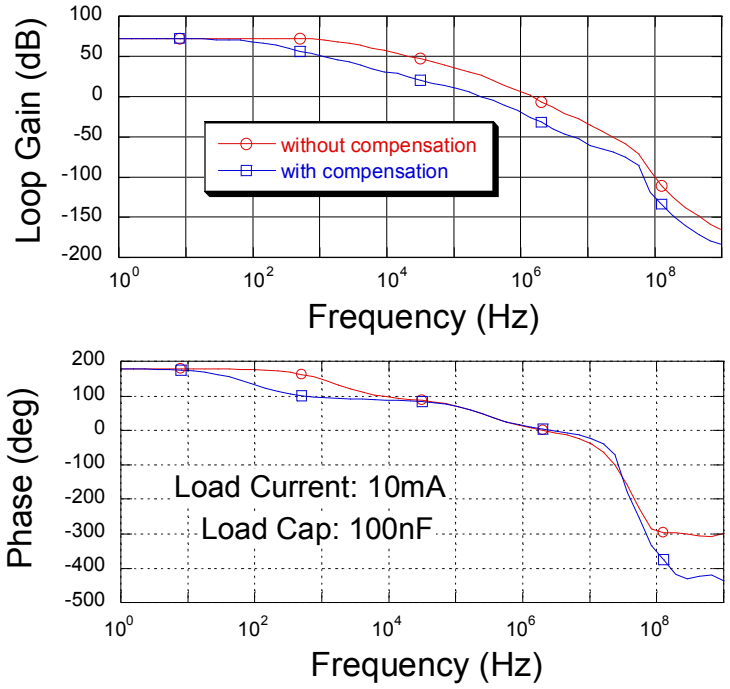


Figure 25. Simulation result of the bode plot of the MESFET LDO regulator with 100nF output capacitor and 10mA load current.

3.4 CONCLUSION

Silicon MESFETs provide a promising solution for the high power linear regulator. Compared to a conventional CMOS LDO regulator, it provides high bandwidth and good stability while still providing a low dropout voltage. The only problem is that it cannot provide a shutdown operation, which is necessary for some applications. When designing the MESFET based LDO, one should be careful about the output voltage and the output swing of the error amplifier since it needs to encompass a large enough negative V_{GS} to pinch-off the device. A buffer is required to sink the leakage current from the gate of the MESFET. In this design, the bandgap reference is integrated on-chip. The next step is to add some compensation techniques to further improve the capacitor driving ability.

CHAPTER 4

MEASUREMENT OF THE N-MESFET LDO

4.1 General Board Setup

In this chapter, the measurement results of the IBM 45nm LDO regulator will be shown, which includes DC performance, dropout voltage, load transient response, power supply rejection (PSR) and the radiation measurements. Figure 26 shows the PCB board used for the measurements. The LDO was bonded in a 16 pin DIP package and attaches to the PCB via a socket. A separated input and output pin was designed for the 4-wire measurement as discussed below. Three banana connections are used for input, ground and output respectively. An SMA connector was also included at the output for its low parasitic capacitance for the transient measurements. Four jumper connections enable different load configurations and lastly a switching NMOS transistor followed by a resistor is connected at the output node for the load transient measurement.

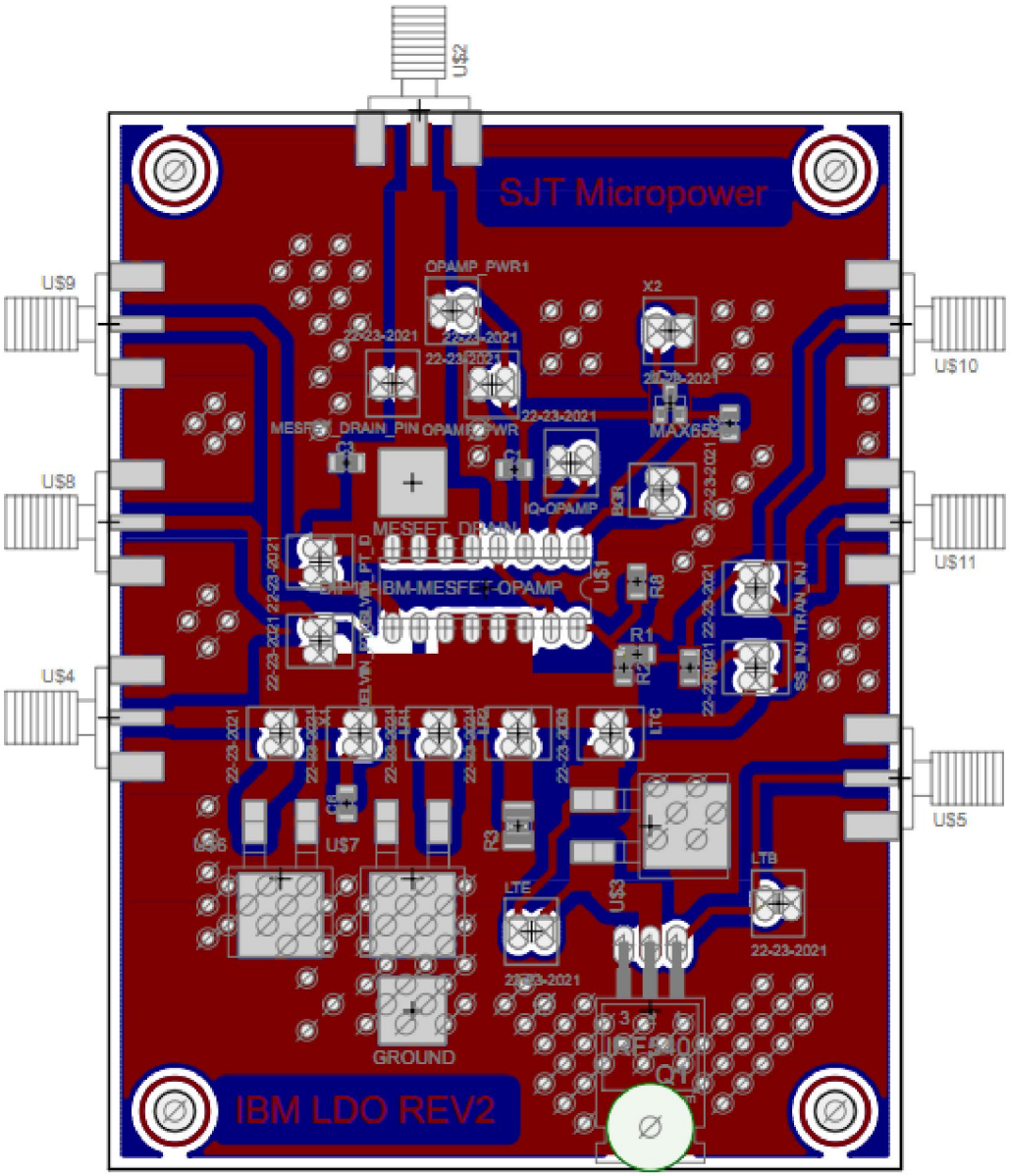


Figure 26. Board layout for the IBM N-MESFET linear regulator.

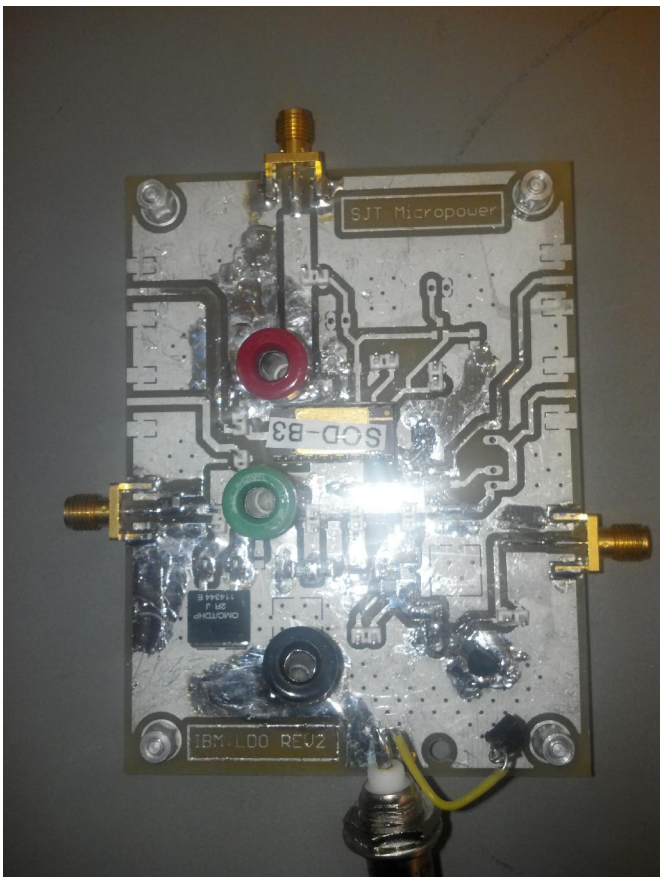


Figure 27. The pictures for the board setup.

4.2 DC PERFORMANCE

The DC performance of the linear regulator can be obtained by measuring the V_{IN}-V_{OUT} characteristic of the linear regulator. The measurement setup is illustrated in Figure 28.

A DC voltage source-meter (Keithley 2400) is connected at the input to provide the supply voltage and a current source-meter is connected at the output to provide the load current. Multi-meters were connected at the output and to monitor their voltage. In order to measure the ground current of the op-amp, a source-meter with 0V is connected in series between the error amplifier ground and the regulator's ground.

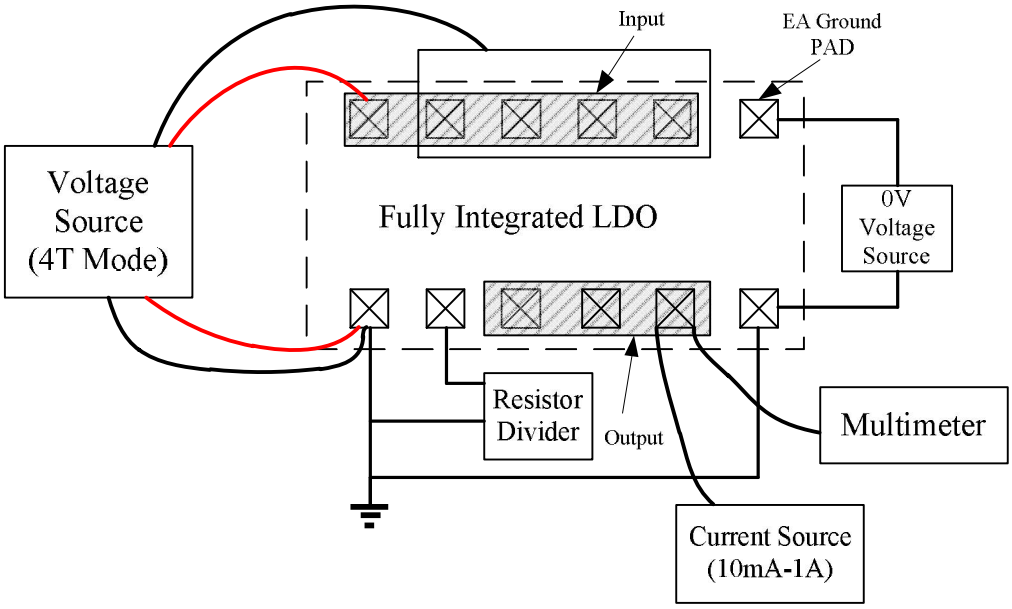
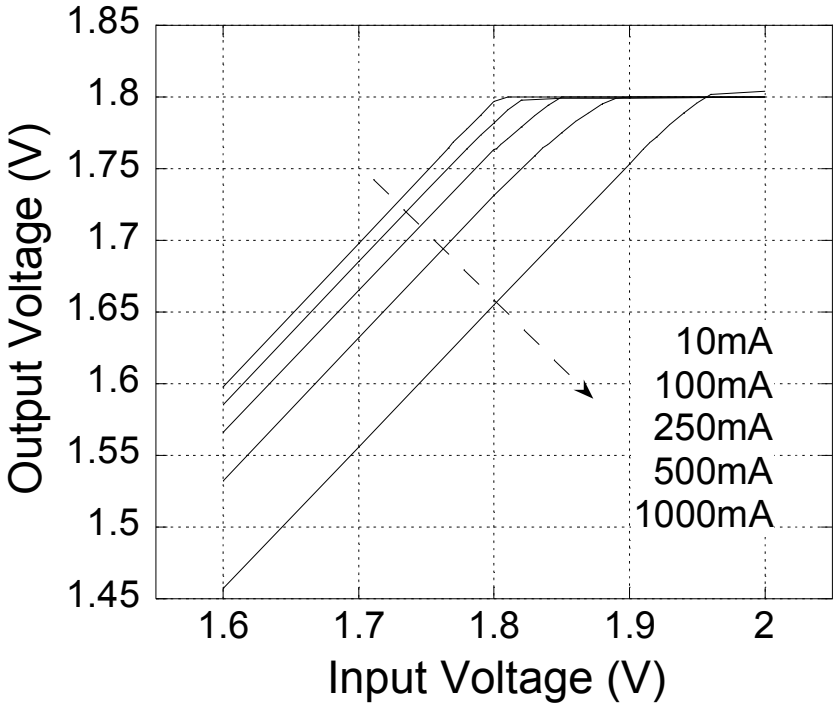
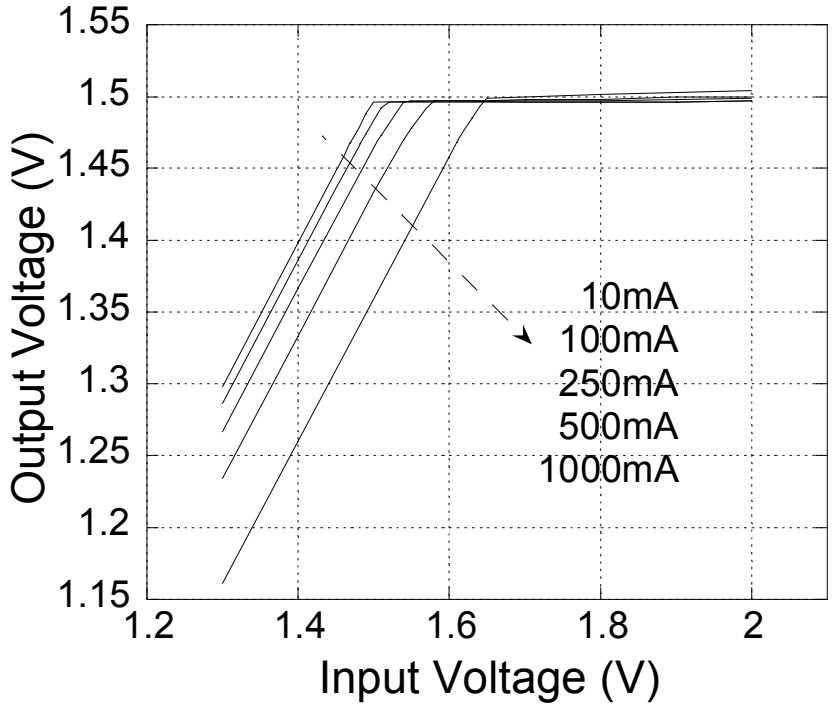


Figure 28. V_{IN}-V_{OUT} characteristic measurement setup.

Measurement results have shown that the parasitic resistance of a 2 feet BNC cable is about 0.2Ω. The parasitic resistance of the bonding wire is proportional to the length and many are put in parallel to reduce that. Even though by doing that, the voltage drop across the parasitic resistance becomes significantly large when the load current goes high. The voltage drop will contribute to the dropout voltage. In order to remove that, 4-wire sensing [23] can be used instead of 2-wire, as shown by the red lines illustrated in Figure 28. Two additional wires are added at the supply voltage to sense the input voltage while the other two are used to supply the voltage and current. Since the sensing wires do not supply any current, they can measure the voltage at the input precisely. By knowing the exact input voltage, the source meter can increase its output voltage to compensate for the voltage drop across the cable.



(a)



(b)

Figure 29. IBM LDO regulator input-output characteristic: (a) for 1.8V, (b) for 1.5V output.

Figure 29 shows the V_{IN}-V_{OUT} characteristic of the proposed LDO regulator at different output voltages and load currents. When the input is high enough, the output will regulate to the desired voltage. As the input voltage decreases close to the dropout region, the output will start to decrease. The dropout voltage was extracted as the voltage difference between the input and the output when the output voltage dropped to 98% of its nominal value. The dropout voltage with load current is shown in Figure 30.

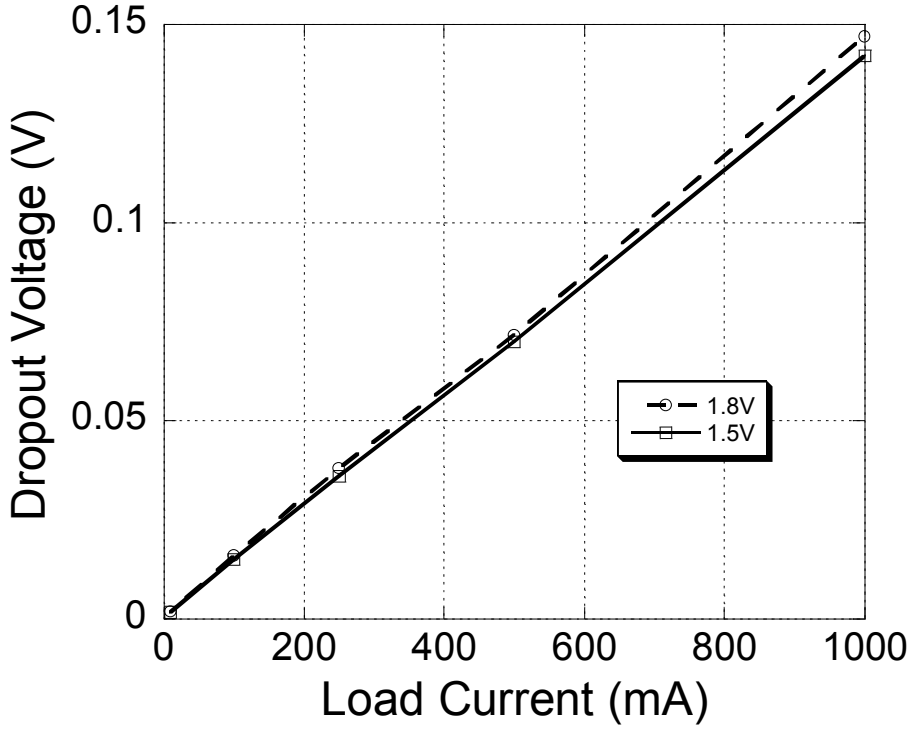


Figure 30. Dropout voltage with load current for IBM N-MESFET LDO regulator.

Based on the V_{IN}-V_{OUT} characteristic under different load currents, line regulation and load regulation can be obtained. The input voltage range for 1.8V output regulation is limited, because of the voltage constraints of the IBM 45nm CMOS process, where the input voltage is limited to 2V. The performances are summarized in Table 3.

Table 3. Line and Load Regulation of the MESFET LDO Regulators

Line regulation	ΔV_{IN}=1.5V-2V, I_{LOAD}=100mA	2mV/V
@ V_{OUT}=1.5V	ΔV_{IN}=1.65V-2V, I_{LOAD}=1A	14.2mV/V
Load reg @ V_{OUT}=1.5V	V_{IN}=2V, I_{LOAD}=10mA-1A	7mV/V
Load reg @ V_{OUT}=1.8V	V_{IN}=2V, I_{LOAD}=10mA-1A	4mV/V

4.3 POWER SUPPLY REJECTION

Power supply rejection (PSR) is the ability of the regulator to resist high frequency noise at the input. To measure the PSR, a small signal is usually injected into the input of the regulator. The amplitude of the small signal at the output is measured and the ratio is PSR. Figure 31 (a) shows the setup for the measurement.

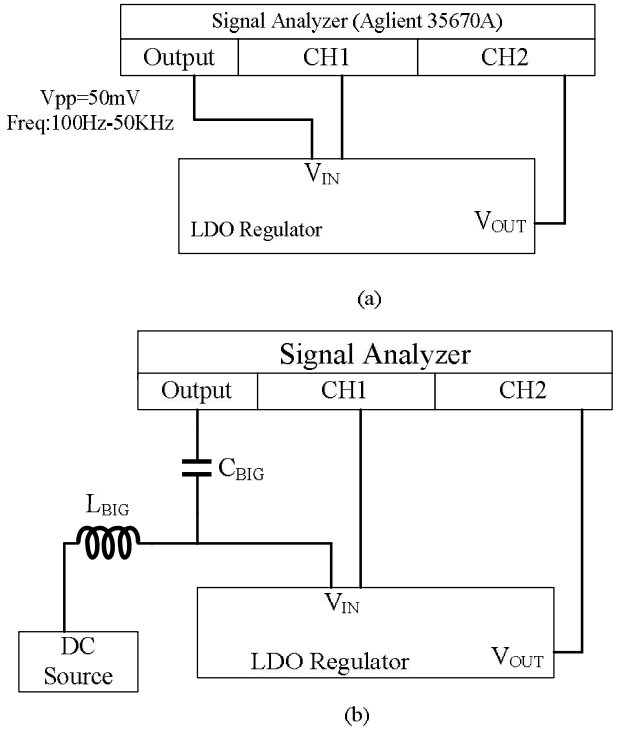


Figure 31. PSR Measurement setup: (a) typical setup, (b) using a large value choke and capacitor.

The amplitude of the small signal input must be set carefully. Too large of an amplitude will give rise to distortion in the circuit, while too small amplitude will be buried into the thermal noise floor, which cannot be detected. Here, the input amplitude of the signal is $50mV_{PP}$. The frequency range was 100Hz to 50kHz.

The limitation of this measurement is the driving ability of the signal analyzer, since the current is also provided by the analyzer. To overcome this issue, a source meter can be used to provide the DC bias voltage and current. In order to inject DC and AC signal together, it is necessary to put some bias circuit between these two. Figure 31(b) shows the measurement setup of this method [24]. A large value capacitor can be added between the AC signal and the input of regulator to block the DC signal from the AC signal source. The low-side of the frequency range is determined by the value of the capacitor. A large value choke is added between the DC source and the input voltage, V_{IN}, to block the AC signal going into the DC source meter. Besides using the biasing circuit, some vendors also provide the signal injectors to inject these two signal together [27]. Figure 32 shows the PSR measurement result with a100mA load current.

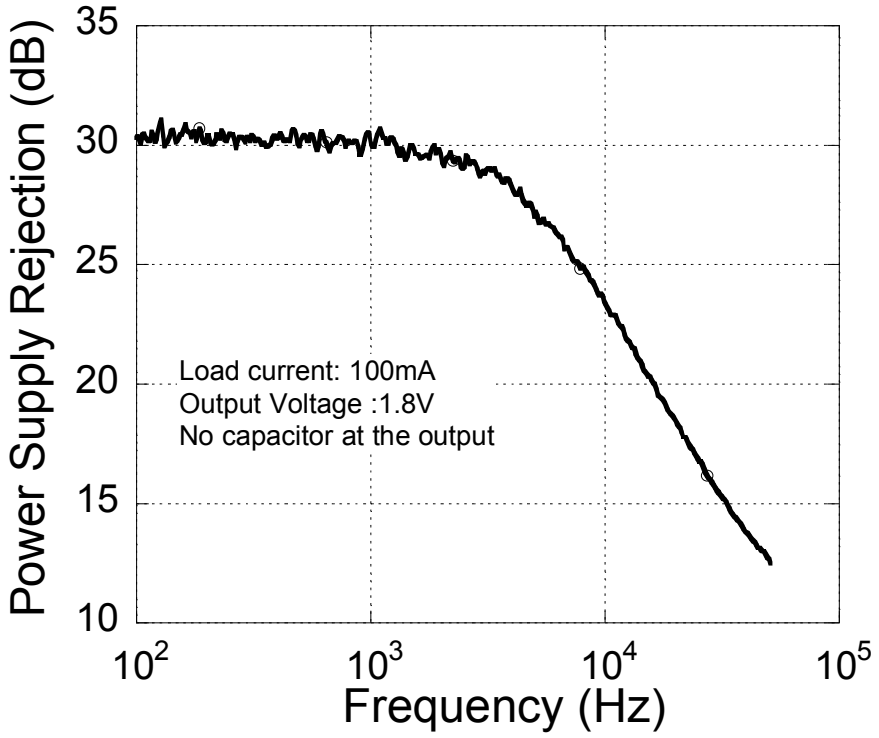


Figure 32. Power supply rejection as a function of frequency frequency for 1.8V output and 100mA load current.

4.4 RADIATION MEASUREMENT

Radiation measurements were conducted on a discrete MESFET and the fully integrated LDO regulator to demonstrate the potential of the device and circuit for aerospace applications. The discrete MESFET and the LDO regulator were irradiated in a MDS Nordion Gammacell 220 Co^{60} source. Each device was in a DIP-16 package with the protected lid removed so as not to block the radiation dose. When irradiating the discrete device, each pin of the MESFET was grounded, while the LDO regulators were biased with 100mA load current. The exposure lasted about two days at a rate of ~0.9krad (Si)/min. DC measurements, including a Gummel plot and the V_{IN}-V_{OUT} characteristics

were done after cumulative doses of 10, 20, 50, 100, 250 and 1000krad (Si). The measurement setup was the same as the V_{IN}-V_{OUT} characteristic measurement of the LDO regulator. [25]

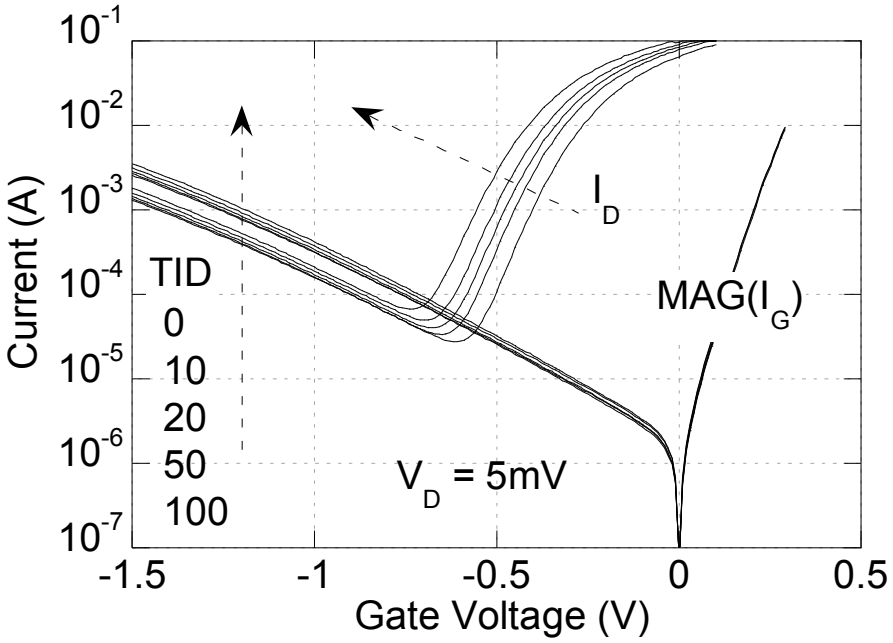


Figure 33. Drain and gate current versus gate voltage for different TID [25].

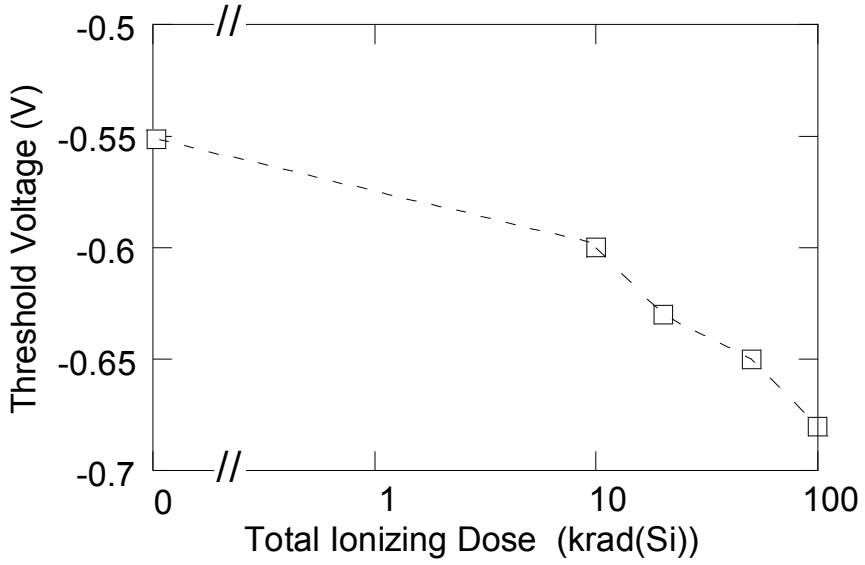


Figure 34. Threshold voltage of a discrete MESFET versus TID [25].

Figure 33 shows the drain and gate current versus the total ionizing dose (TID). Threshold voltage can be extracted from the data, which as shown in Figure 34**,** becomes more negative with increasing TID. This is because the ionizing radiation provides positive trapped charge at the interface between the silicon channel and the buried oxide layer [25]. In order to pinch off the channel, a smaller gate voltage is needed, thus V_t becomes more negative.

The LDO regulator performance after exposure to radiation was shown in Figure 35, which demonstrates the radiation tolerance of the CMOS and MESFET fabricated on a deep submicron commercial SOI process. The output voltage decreases with TID increasing. Since the MESFET is put in the feedback loop, its threshold and leakage current change will not disturb the output. Dropout voltage may be affected due to the change of the on-resistance, but also will not change the nominal output voltage. Two reasons contribute for the change of the output regulated voltage, the bandgap reference and the offset from the EA.

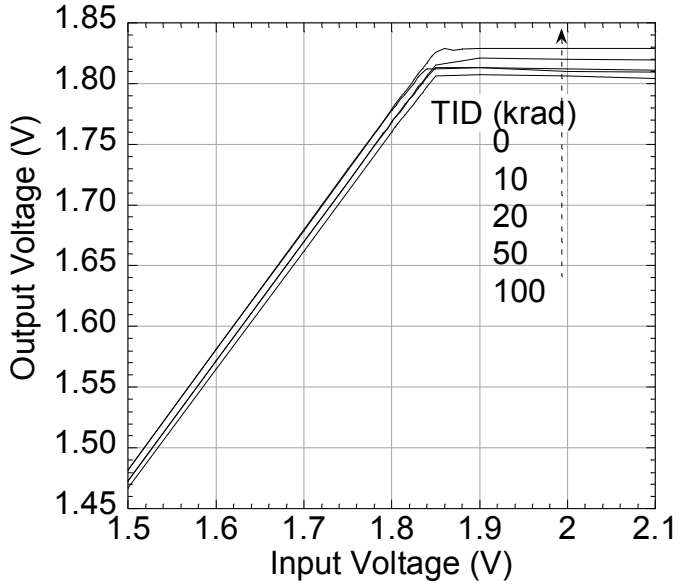


Figure 35. Line regulation for 100mA load current versus TID [25].

Figure 36 shows the variation of the bandgap reference voltage with TID, and shows a 10mV change for the total range, which results in a 15mV change at the output due to the feedback resistor ratio. The change in the bandgap reference probably comes from the diode turn-on voltage due to radiation.

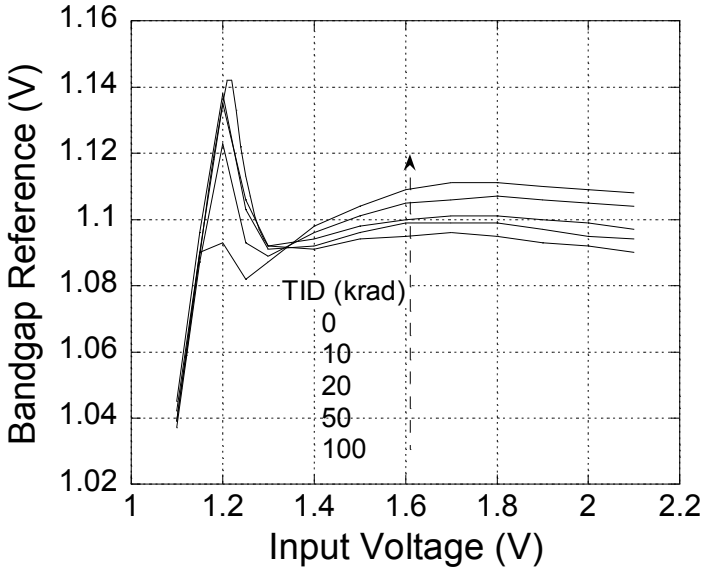


Figure 36. The bandgap reference voltage variation due to the radiation [25].

If the voltage reference variation is substrate from the output voltage, the offset variation still makes about 1/3 contribution for the total output change. Such a variation may come from the change of the input pair transconductance of the amplifier. In order to work as a radiation-tolerant application, a low offset op-amp is needed. Since the offset source of the op-amp is mainly from the input pair, larger devices can be used as part of a future design. Reducing the g_m of the rail load device can further reduce the input-referred offset.

4.5 Load Transient Response

The load transient response shows how the regulator responds to a step in the load current. Usually it is very difficult to break the loop when measuring the close-loop frequency response due to the integration of the feedback resistors. Thus, the load transient response plays an important role in predicting the loop bandwidth and phase margin of the linear regulator. Higher bandwidth will lead to faster recovery time and good phase margin which gives a smooth transition without large over-shoot. Figure 37 shows the measurement setup. An HP-8110A pulse generator was used to generate the pulse signal to control the transistor switch. A battery was utilized instead of a source-meter since it provides faster line response after a large current step. All the wires that connected to the pulse generator are SMA cables in an effort to lower the parasitic inductance and capacitance. As discussed in [7], poor terminations will result in reflection and lead to ringing for the signal. Thus it is better to use 50 Ohm termination at the gate

(base) of the switching device for better signal integrality.

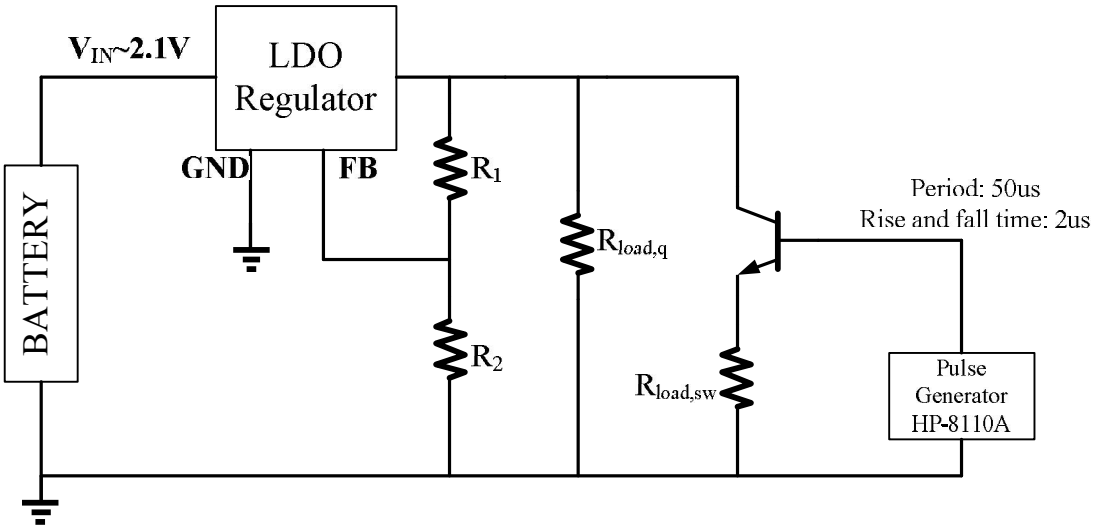


Figure 37. Measurement setup for the load transient response.

The battery is connected to the input of the circuit using thick copper wires with a gauge of 8 and banana connectors. When switching large load currents the parasitic resistance of the connecting wires will lead to significant voltage drops. In order to reduce these effects, the length of the wires was designed to be as short as possible to reduce the area they enclosed. In this measurement, the length of the wires is about 4.5 inches. Decoupling capacitors can be used to further improve the performance. A 47µF electrolytic capacitor was added at the battery terminals before the copper wire and a 10µF ceramic capacitor was added at the input to the LDO regulator on the board. The output of the regulator is connected to an oscilloscope directly using an SMA-to-BNC connector without any cables (see Figure 38). That further reduced parasitic capacitance and inductance.

Figure 38. The connector that used to connect the output to the oscilloscope directly.

The rise time and fall time of the signal generator needed to be set very carefully. Fast rise and fall time will have high frequency components in the signal, which will result in a large overshoot at the output, possibly causing damage to the device. It is well known that the voltage drop across the inductance is L×dI/dt. As the switching is large (up to 500mA for the load tests performed as part of this work), fast rise and fall times will cause significant drop across the parasitic inductance, which will degrade the performance of the regulator. However, the rise and fall time need to be faster than the recovery-time of the LDO regulator so that the transient response can be measured accurately. In this design, the rise time and fall time was set to be 2μs.

The switching transistor used here was a 2N2222 NPN BJT transistor. $R_{load,q}$ provided the quiescent load current while $R_{load,sw}$ provided the switching current. The current was switching from 0-100mA first by setting $R_{load,sw}$ to 10Ω and controlling the voltage swing at the emitter of the BJT to 1V. $R_{load,sw}$ was then changed to 5Ω and 2Ω to provide a 0-200mA and 0-500mA switching pulse. The 2Ω resistor used here was a large

power resistor and was needed to achieve the high load current. The measurement results are shown in Figure 39, 40 and 41.

Figure 39. Load transient response with 0-100mA load current. The orange line shows the output voltage and the purple line shows the voltage at the emitter of the BJT.

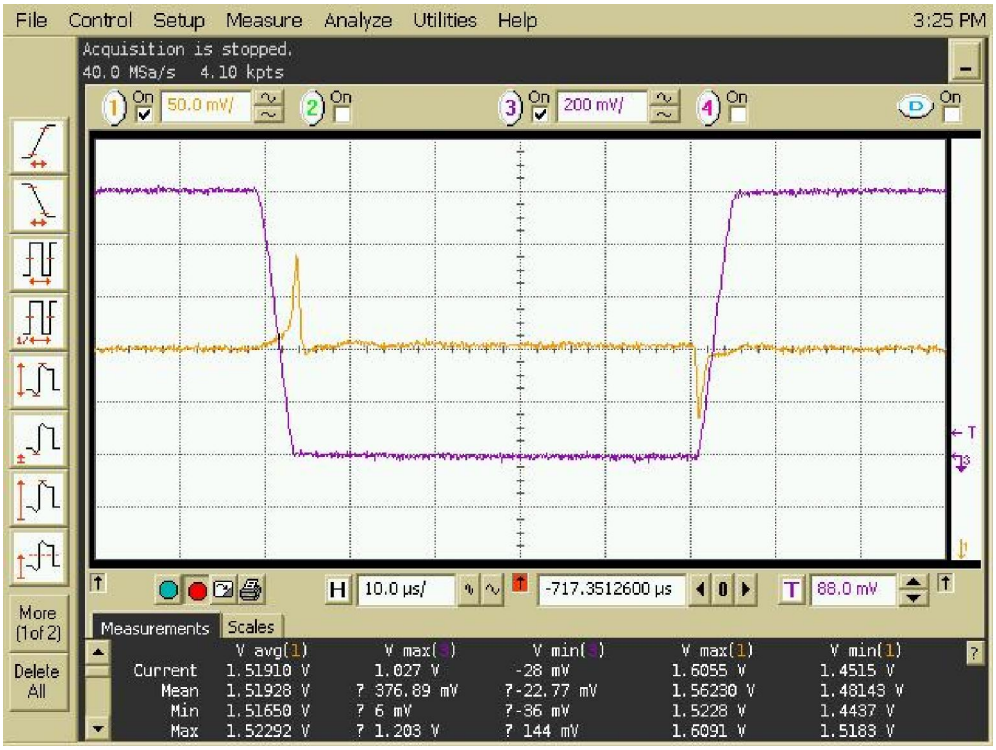


Figure 40. Load transient response with 0-200mA load current. The orange line shows the output voltage and the purple line shows the voltage at the emitter of the BJT.

Figure 41. Load transient response with 0-500mA load current. The orange line shows the output voltage and the purple line shows the voltage at the emitter of the BJT.

The voltage scale for the output in Figure 39 is 20mV/div and for Figure 40 and Figure 41 is 50mV/div. The voltage scale for the emitter of the BJT is 200mV/div. The time scale for the three figures is all 10.0μs/div. As shown, the LDO regulator is stable with no load capacitor and shows good load transient response from 0-500mA. From the results, it can be seen that the over-shoot for the output voltage was approximately 80mV, 90mV and 120mV for 100mA, 200mA and 500mA step respectively. For the 100mA and 200mA load step, the LDO regulator also shows good recovery. For 500mA step, there is about 10mV ringing that can be seen at the output voltage.

The load transient response was also measured with the presence of the load capacitor to demonstrate its capacitor loading ability. In this measurement, the load current is switching from 0mA to 500mA. A 6.8nF ceramic capacitor is connected at the output as the load cap. The measurement result is shown in Figure 42.

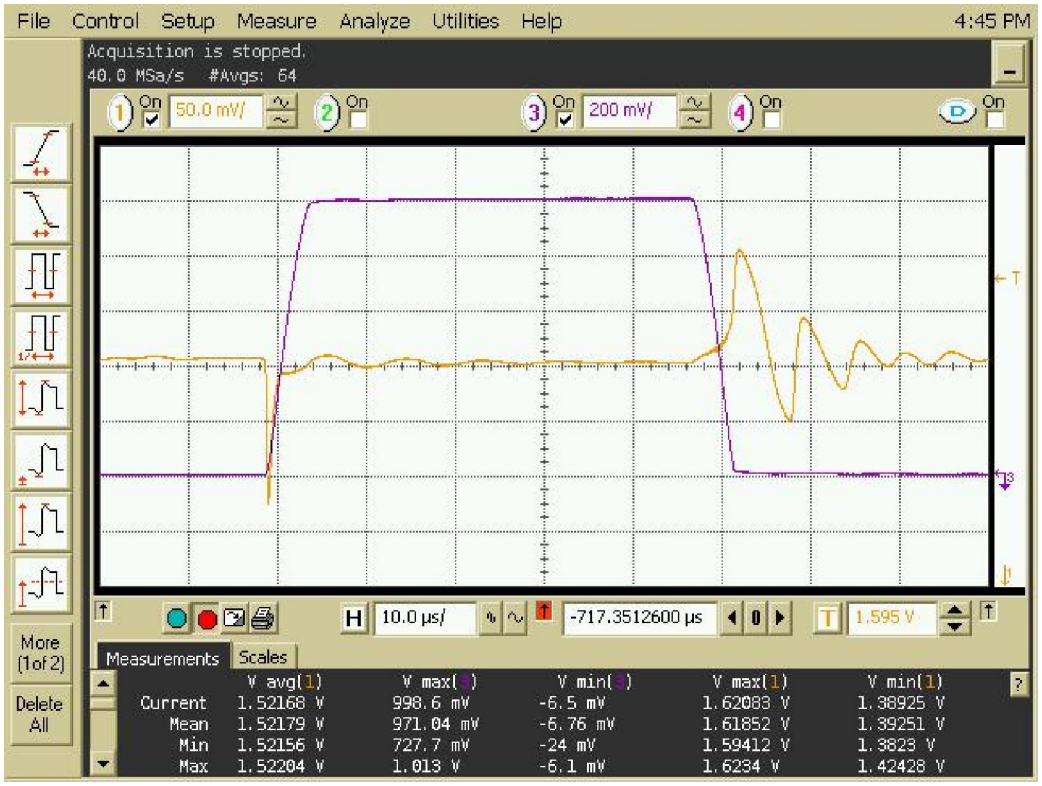


Figure 42. Load transient response with 0-500mA load current. A 6.8 nF capacitor is connected to the output. The orange line shows the output voltage and the purple line shows the voltage at the emitter of the BJT.

The voltage scale in **Figure 1** is 50mV/div and the time scale is 10.0us/div. From the measurement result, we can see a very small ringing for the current rising edge while there is a significant overshoot of approximately 100mV for the current falling edge. Two main reasons can potentially cause this to happen, the parasitic inductance from the measurement setup and/or the stability issues from the feedback loop.

Let us first consider the parasitic inductance. While the load current changes from high to low, the load capacitor will discharge through the parasitic inductance. However, after carefully considering the frequency of the ringing shown in **Figure 1** it is clear that parasitic inductance cannot be the origin. From the measurement result the oscillation

frequency is approximately 100 kHz. To ring at such a low frequency, the parasitic inductance needs to be approximately 0.3mH. Usually the parasitic inductance for wires or cables is about 1-2μH/m [29] and it is nearly impossible to have such a huge parasitic inductance on the test board.

Another potential reason is due to the low phase margin of the feedback loop. As discussed in Chapter 2, the loop of the n-type linear regulator is usually designed as a single pole system. The dominant pole is at the output of the error amplifier and other poles are designed to be at high frequency. For our regulator, the location for the dominant pole and the first non-dominant pole is

$$P_1 = \frac{1}{r_o C_{comp}} \quad (15)$$

$$P_2 = \frac{g_{m(n-MESFET)}}{C_L} \quad (16)$$

where r_o is the output impedance of the error amplifier, C_{comp} is the compensation capacitor, $g_{m(n\text{-}MESFET)}$ is the transconductance of the pass device and C_L is the load capacitor. As discussed in Chapter 2, a large load capacitor will push P_2 towards the origin. Furthermore, the transconductance of the MESFET is also small for light loads, pushing P_2 to much lower frequency. Thus it is very likely that our linear regulator will experience a relatively low phase margin with large load capacitor and light load currents, which will cause this ringing.

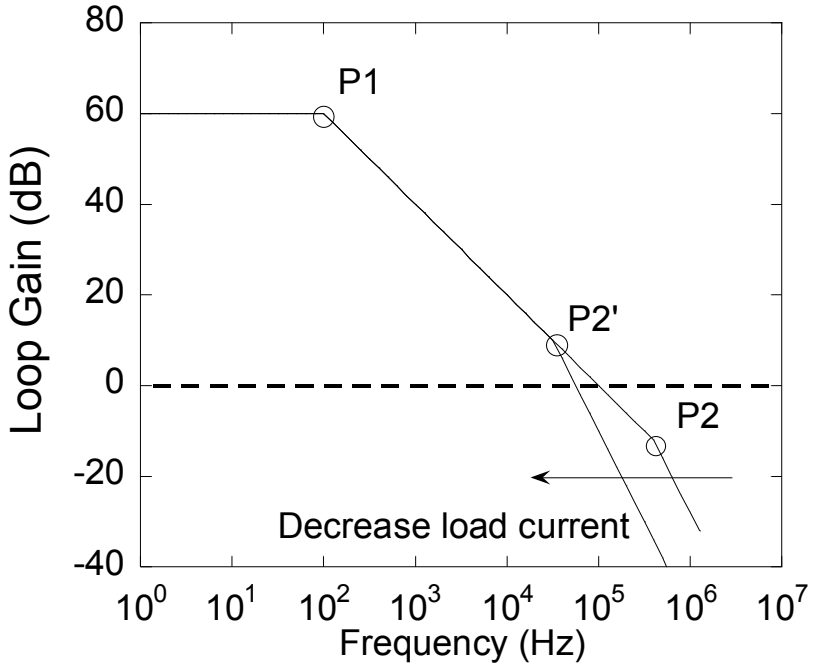


Figure 43. Closed loop frequency response with respect to the load current change..

In order to have a clean transient response for a specific load capacitor, one way is to increase the internal compensation capacitor, moving P_1 to a lower frequency and giving more room for $g_{m(n\text{-}MESFET)}$. However, such a design will decrease the loop bandwidth, thus resulting in a long transient recovery time. Another method is to limit the lowest value of $g_{m(n\text{-}MESFET)}$ by limiting the lowest current flowing through the pass device. This can be achieved by reducing the value of the feedback resistors. Although, this will increase the quiescent current, if it is used for a heavy load application (few amps) it usually can be neglected.

4.5 CONCLUSION

In this chapter, the characterization results of the IBM 45nm MESFET based LDO regulator are discussed. The methods to measure the DC performance, power supply rejection, radiation response and load transient response were introduced. In order to remove the voltage drop across the bonding wire and cables for the DC measurement, 4-wire sensing was used. Two additional wires that do not carry any current are only used to "sense" the voltage. Measurement results show good DC line and load regulation. The dropout voltage was less than 150mV with 1A load current. The power supply rejection was measured for a 100mA load current and showed a 30dB result. The performance under large load current can be measured with the help of a biasing circuit or signal injector. The regulator was measured up to a TID of 1000krad, showing the potential for aerospace applications. Load transient response was the last measurement taken and the environment was set up very carefully. The results show low overshoot and faster recovery time for low load currents. Ringing occurs with the presence of high current and a large capacitor load.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 CONCLUSIONS

As we have discussed in Chapter 2, linear regulators can be used to provide a wide bandwidth, low noise power supply for analog and digital circuits. Compared to switching regulators, linear regulators have low efficiency but much cleaner output voltage. In order to improve the efficiency, a low-dropout voltage is required. Conventional PMOS linear regulators can provide a low dropout voltage. However, that requires an external capacitor for stability purposes. Recent research work has demonstrated how to design capacitor-free LDO regulators [28]. However, they are difficult to compensate and the bandwidth is low. Enhancement-mode NMOS linear regulators provide easy compensation and good stability but require a charge pump for low-dropout operation.

SOI MESFET devices solve this issue naturally by operating in depletion mode. Chapter 3 has discussed the design of the MESFET linear regulator. Minimum achievable gate length and access length is used for the pass device for its low parasitic resistance and capacitance. The error amplifier utilizes the folded cascode architecture. A source follower with shunt-feedback is followed as a buffer to sink the leakage current from the gate of the MESFET. The shunt-feedback transistor needs to be large enough to sink the leakage under any conditions for different load current, temperatures and radiation. A 2.5pF capacitor is added at the output of the error amplifier to compensate for the

stability.

Characterization results are discussed in Chapter 4. Methods for measuring DC performance, power supply rejection, load transient response and radiation response are discussed. DC performance shows good load and line regulation. The dropout voltage for a 1A load current is less than 150mV. The power supply rejection of the linear regulator is approximately 30dB. The regulator was exposed to gamma radiation from an MDS Nordion Gammacell 220 Co^{60} source for radiation measurements. The results show that it can maintain regulation up to a total ionizing dose of 1000krad, demonstrating the potential for aerospace applications.

5.2 Future Work

From the characterization results, several issues have been found for the design. One problem is that the size of the shunt feedback transistor for the source follower buffer my not be large enough to sink the leakage current at high temperature, making the output of the buffer not high enough and the circuit lose regulation. In the next design, the size of the shunt-feedback transistor has been increased to sink more current.

Another issue is that the regulator shows poor load transient response when presented with a large load capacitor. This is because that the internal compensation capacitor is not large enough and the bonding-wires have parasitic inductance. The compensation on-chip capacitor will make the gain margin of the loop become low. Simulation results have shown that with the large parasitic inductance from the bonding

wires and the cables, there will be a peaking in the bode plot. With a low gain margin, such a peaking will result in a poor load transient response and even have the potential to make the regulator oscillate. The reason for this is due to the aggressive design of the error amplifier in the initial design to get a high bandwidth and fast recovery time. In the revised version of the design, a large compensation capacitor is used to provide even large phase margin and gain margin. A low-bandwidth error amplifier is used to further ensure the stability

Also from the results of the radiation measurements of the LDO regulator, several suggestions about the design can be concluded. Firstly, a radiation tolerant voltage reference needs to be designed. As discussed in [5], MESFETs have the potential to provide a PTAT voltage with relatively low temperature drift. Such a PTAT voltage can be used as the reference voltage for the linear regulator.

The input-offset variation of the CMOS op-amp also contributes to the performance of the regulators under radiation, which is probably because of the change of the threshold voltage of the MOSFET after TID exposure. To further reduce the change, a low-offset error amplifier is necessary. Reference [19] gives a basic guide to the design of low-offset operational amplifiers. The sizes of the input pairs need to be large enough, while to ensure that the output swing is large enough, the size of the current source device needs to be small. These changes are applied to the next version of the linear regulator design.

In conclusion, this thesis shows the evaluation and characterization results of a MESFET-based low dropout regulator, demonstrating its low-dropout voltage, good stability and radiation tolerant performance. Further developing the CMOS process will allow the SOI MESFET from ASU to find more applications.

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