Carrier Lifetime Measurement

for Characterization of Ultraclean Thin p/p^+ Silicon Epitaxial Layers

by

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ABSTRACT

Carrier lifetime is one of the few parameters which can give information about the low defect densities in today's semiconductors. In principle there is no lower limit to the defect density determined by lifetime measurements. No other technique can easily detect defect densities as low as 10^9-10^{10}cm^{-3} in a simple, contactless room temperature measurement. However in practice, recombination lifetime τ_r measurements such as photoconductance decay (PCD) and surface photovoltage (SPV) that are widely used for characterization of bulk wafers face serious limitations when applied to thin epitaxial layers, where the layer thickness is smaller than the minority carrier diffusion length L_n. Other methods such as microwave photoconductance decay (μ-PCD), photoluminescence (PL), and frequency-dependent SPV, where the generated excess carriers are confined to the epitaxial layer width by using short excitation wavelengths, require complicated configuration and extensive surface passivation processes that make them time-consuming and not suitable for process screening purposes. Generation lifetime τ_g, typically measured with pulsed MOS capacitors (MOS-C) as test structures, has been shown to be an eminently suitable technique for characterization of thin epitaxial layers. It is for these reasons that the IC community, largely concerned with unipolar MOS devices, uses lifetime measurements as a "process cleanliness monitor." However when dealing with ultraclean epitaxial wafers, the classic MOS-C technique measures an effective generation lifetime τ_{geff}which is dominated by the surface generation and hence cannot be used for screening impurity densities.

I have developed a modified pulsed MOS technique for measuring generation lifetime in ultraclean thin p/p^+ epitaxial layers which can be used to detect metallic impurities with densities as low as $10^{10}\mathrm{cm}^{-3}$. The widely used classic version has been shown to be unable to effectively detect such low impurity densities due to the domination of surface generation; whereas, the modified version can be used suitably as a metallic impurity density monitoring tool for such cases.

For my parents

M. R. Elhami Khorasani, and M. Zarei

and

In memory of

Dieter K. Schroder

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I would like to express my greatest gratitude for Professor Dieter K. Schorder, who is not among us today, for being my advisor through most of my M.S. education at ASU. He supervised my research with his profound knowledge and support. The greatest honor of my academic studies is being his student and the greatest sorrow would be that I could not benefit from his guidance any more. He was the greatest adviser, teacher and mentor who gave me a chance to broaden my knowledge in his research group. He will be respected in my memory forever.

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TABLE OF CONTENTS

Page

CHAPTER Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

Figure Page

Figure Page

Figure Page

Figure Page

Figure Page

CHAPTER 1:

INTRODUCTION

All semiconductor materials and devices contain defects. Some of these are metallic impurities others are structural defects such as dislocations, stacking faults, *etc*. Fortunately, the defect density in virgin silicon is extremely low [1]. Although the impurity density sometimes increases during device fabrication, gettering reduces its density to sufficiently low levels. Nevertheless, these defects have, at times, a significant influence on device operation. For example, interface traps at the SiO_2/Si interface and oxide traps in the oxide of MOS devices lead to noise, random telegraph signals, leakage current, stress-induced leakage current, non-volatile memory retention degradation, dynamic random access memory storage time degradation and other deleterious effects [2]. Impurities in the silicon lead to reduced recombination/generation lifetimes and increased leakage or dark current. In general, device performance after fabrication is generally very good to excellent, but operation-induced stress during device operation can lead to degradation.

Defects come in point, line, area, and volume configurations. Examples of these are: point defects: metals, oxygen, dopants; line defects: edge dislocations; area defects: stacking faults; volume defects: oxide and metal precipitates. The bulk defect density in Si has decreased over the years and Si today contains on the order of 10^9-10^{10} cm^{-3} metallic impurities after crystal growth. The SiO_2/Si interface defect density, on the other hand, has hardly changed with interface trap densities of ~10^{10} cm^{-2} being about the same

as 20-30 years ago [3]. As a result, device parameters such as junction leakage current, are usually dominated by interface, rather than bulk, effects.

1.1 Deep Level Metallic Impurities

Deep level metallic impurities, also called as deep level defects or traps, categorize a variety of foreign atoms that when introduced to silicon perfect crystal breaks its periodicity and create a discrete energy level E_T within Si band gap. Such energy level, referred to as the trap level, for metallic impurities lies deep and far from band edges of Si band diagram and acts as a generation/recombination site that, from a device point of view, alters the electrical behavior of material. Although impurities are sometimes introduced to silicon intentionally for enhancing properties such as resistivity or switching time [4], unintentional contamination of metallic impurities has always been a concern in silicon fabrication during crystal growth, wafer preparation and devices fabrication. Introduction of foreign impurities to silicon, in general, can take place from gas, liquid or solid phases. Carbon, for instance, can be introduced to the wafers during contact with photoresist and from its residue, while metallic impurities can come from a variety of sources ranging from pipelines, furnaces, and instruments to the unpurified deionized water [5]. Metallic impurities, based on how often one may come across them in silicon, can be categorized to: main metallic impurities such as Iron, Nickel, Copper, Molybdenum, Palladium, Platinum, Gold, and rare metallic impurities such as Scandium, Titanium, Tungsten, Silver, *etc*. However, in recent years, the amount of unintentionally introduced main metallic impurities has been minimized and the industry is now virtually dealing with detection and reduction of rare impurities that can be unintentionally

introduced to the silicon by cross contamination. Tungsten, as a good example of this, is an impurity which is mostly introduced to clean silicon wafers through cross contamination in industrial fabrication plants.

From an electrical point of view, each metallic impurity within silicon is characterized by the energy level E_T it introduces to the silicon band gap, and its capture cross section for electrons and holes: σ_n and σ_p, respectively [6]. Since according to equations 1-1 and 1-2, the electron (hole) emission rate and capture coefficient from a deep level impurity is directly related to these two parameters, they mainly define how an individual impurity will affect the electrical properties of the Si and hence the devices that are fabricated on it. Figure 1.1 shows the process of electron emission from a generation/recombination center which lies deep in the band gap of Si in absence of an external electric field [7].

$$e_n = \frac{\sigma_n \vartheta_{th} n_i}{\exp(E_i - E_T/kT)} \tag{1-1}$$

$$c_n = \sigma_n \vartheta_{th} \tag{1-2}$$

Moreover, depending on its physical properties, a deep level trap can act either as an acceptor or donor. In general, a trap is either occupied by an electron or hole and depending on being an acceptor or a donor it can have three distinct electrical states: neutral, positively charged or negatively charged. Whether a state has any of these 3 conditions depends on its kind and its location in respect to Fermi energy level. For instance, a donor site, whose energy level is below E_F is occupied by an electron and hence neutral [2].

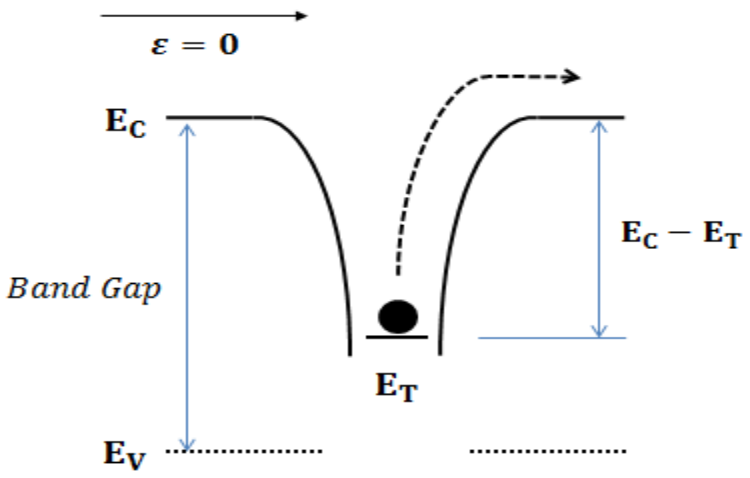


Figure 1.1: Electron emission from a deep level impurity energy level - recombination/generation site.

Sometimes it has been observed that an individual impurity can introduce more than one energy level depending on its atomic structure and how it is residing inside the silicon crystallographic structure –interstitial or substitutional. Tungsten, for instance, has been reported [8] first by Fujisaki to have an energy level of $E_V + 0.41$, while later Boughaba suggested three more energy levels of $E_V + 0.22$, $E_V + 0.33$ and $E_C - 0.59$, respectively [9]. Table 1 shows several impurities [5] with their energy level as well as their source of contamination, respectively, that are so far identified. There is a still ongoing research on more precisely identifying the metallic impurities within silicon. Most of this work consists of deliberately introducing impurities to the silicon and then by performing characterization techniques such as Deep Level Transient Spectroscopy (DLTS) identifying the energy level they introduce to the semiconductor's band diagram.

Table 1.1: Several foreign impurities in silicon with their energy level and source of contamination [5].

Foreign Impurity	Activation Energy (eV)	Source of Contamination
Iron (FeB)	$E_T = E_V + 0.10$ $= E_C - 0.23$	Ultrasonic cleaning, stainless steel pipelines, wet processing
Tungsten	$E_T = E_V + 0.41$ $= E_C - 0.22$	Cross contamination from VLSI interconnects
Carbon	$E_T = E_c - 0.25$	Photoresist residue
Gold	$E_T = E_c - 0.54$ $= E_V - 0.34$	Contaminated tweezers, heat treatment furnaces
Copper	$E_T = E_c - 0.16$ $= E_V + 0.45$ $= E_V + 0.23$	Wet processing, furnace tubes, crucibles in electron-beam evaporators
Nickel	$E_T = E_c - 0.35 \sim 0.38$	Stainless steel pipes, mechanical contact, sputtering chambers
Chromium	$E_T = E_c - 0.22$	Cross contamination with etching solutions

1.2 Interface trapped charge

Interface trapped charge, also known as interface states, interface traps, and fast surface states, exist at the SiO_2/Si interface. They are the result of a structural imperfection. In the wafer bulk each silicon atom is tetrahedrally bonded to four other Si

atoms. When the Si is oxidized, the bonding configuration at the surface is as shown in Figure 1.2 (a) and (b) with most Si atoms bonded to oxygen at the surface. Some Si atoms bond to hydrogen, but some remain unbonded. An interface trap, is an interface trivalent Si atom with an unsaturated (unpaired) valence electron usually denoted by $Si_3 \equiv Si\bullet$, where the "≡" represents three complete bonds to other Si atoms (the Si_3) and the "•" represents the fourth, unpaired electron in a dangling orbital (dangling bond). Interface traps, also known as P_b centers [10], are designated as D_{it} ($cm^{-2}eV^{-1}$), Q_{it} (C/cm^2), and N_{it} (cm^{-2}).

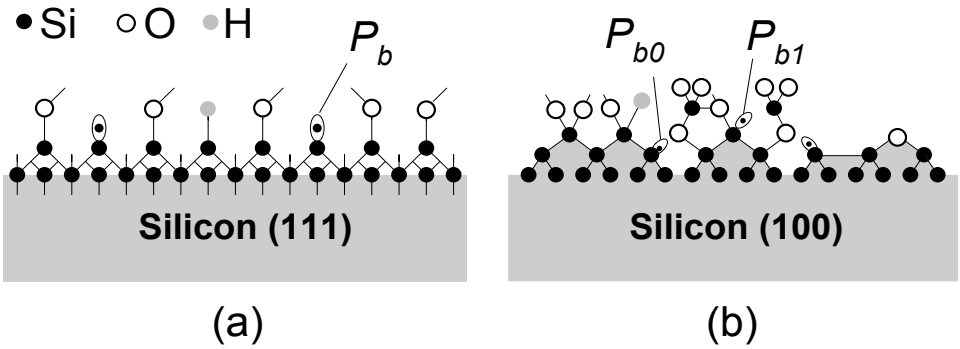


Figure 1.2: Structural model of the (a): (111) Si surface and (b): (100) Si surface.

On (111)-oriented wafers, the P_b center is situated at the Si/SiO_2 interface with its unbonded central-atom orbital perpendicular to the interface and aimed into a vacancy in the oxide immediately above it, as shown in Figure 1.2(a). On (100)-oriented Si, the four tetrahedral Si-Si directions intersect the interface plane at the same angle. Two defects, named P_{b1} and P_{b0}, that are shown in Figure 1.2(b), have been detected by electron spin resonance. Interface traps are electrically active defects with an energy distribution throughout the Si energy gap. They act as generation/recombination centers and contribute to leakage current, low-frequency noise, and reduced mobility. Interface traps

become charged and contribute to threshold voltage shifts. The surface potential dependence of the occupancy of interface traps is illustrated in Figure 1.3.

Interface traps at the SiO_2/Si interface are acceptor-like in the upper half and donor-like in the lower half of the band gap [11, 12]. Hence, as shown in Figure 1.3(a), at flatband voltage, with electrons occupying states below the Fermi energy, the states in the lower half of the band gap are neutral (occupied donors designated by "0"). Those between mid-gap and the Fermi energy level are negatively charged (occupied acceptors designated by "-"), and those above E_F are neutral (unoccupied acceptors). For an inverted p-MOS in Figure 1.3(b), the fraction of interface traps between mid-gap and the Fermi level is now unoccupied donors, leading to positively charged interface traps (designated by "+").

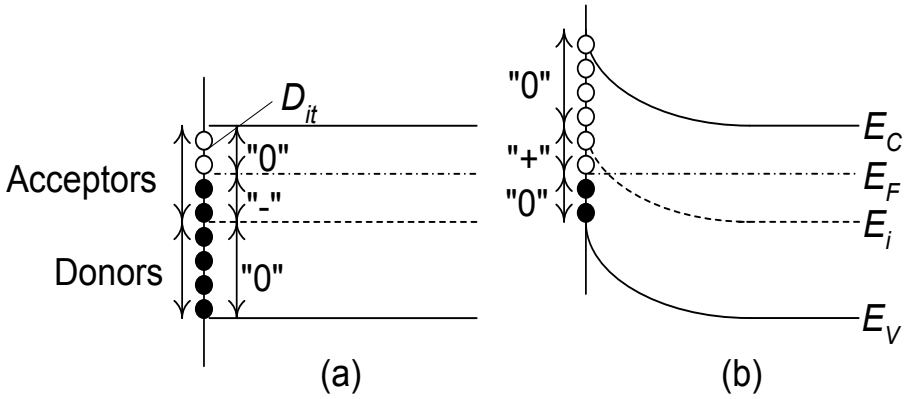


Figure 1.3: Band diagrams of the Si substrate of a p-channel MOS device showing the occupancy of interface traps and the various charge polarities with (a) negative interface trap charge at flatband and (b) positive interface trap charge at inversion. Interface traps are either occupied by electrons (solid circle) or holes, shown by the open circles.

Unlike deep level traps, the interface traps are characterized by continuous energy levels that are spreaded through the Si band-gap at the oxide/Si interface. The density of interface traps are most suitably reduced by forming gas anneal [13].

1.3 Border Traps

In 1980, a committee headed by Deal established the nomenclature for charges associated with the SiO_2/Si system, *i.e.*, interface trapped, fixed oxide, mobile ionic and oxide trapped charge [14]. In 1992, Fleetwood *et al.* suggested that this list be augmented by including border traps also designated as slow states, near-interfacial oxide traps, E' centers, and switching oxide traps [15, 16, 17]. He proposed border traps to be those near-interfacial oxide traps located within approximately 3 nm of the oxide/semiconductor interface. There is no distinct depth limit, however, and border traps are considered to be those traps that can communicate with the semiconductor through capture and emission of electrons and/or holes.

Oxide, border, and interface traps are schematically illustrated in Figure 1.4(a). Defects at or near the SiO_2/Si interface are distributed in space and energy and communicate with the Si over a wide range of time scales. While for interface traps, the communication of substrate electrons/holes with interface traps is predominantly by capture/emission, for border traps it is mainly by tunneling from the semiconductor to the traps and back. Figure 1.4(b) shows the flatband energy band diagram with interface and border traps occupied by electrons to the Fermi level E_F. The energy band diagram in Figure 1.4(c) applies immediately after V_{G1} is applied, before unoccupied border and interface traps have captured electrons. Interface traps now capture electrons from the

conduction band, indicated by (ii) and inversion electrons tunnel to border traps, indicated by (i). Tunneling (i) is followed by electron capture of lower energy border traps. In Figure 1.4(d) interface and border traps up to E_F are occupied by electrons through (ii) electron capture and (iii) tunneling. For $-V_{G2}$ in Figure 1.4(e), electrons tunnel from border traps to the conduction band (iv), interface traps (v) and the valence band (vi).

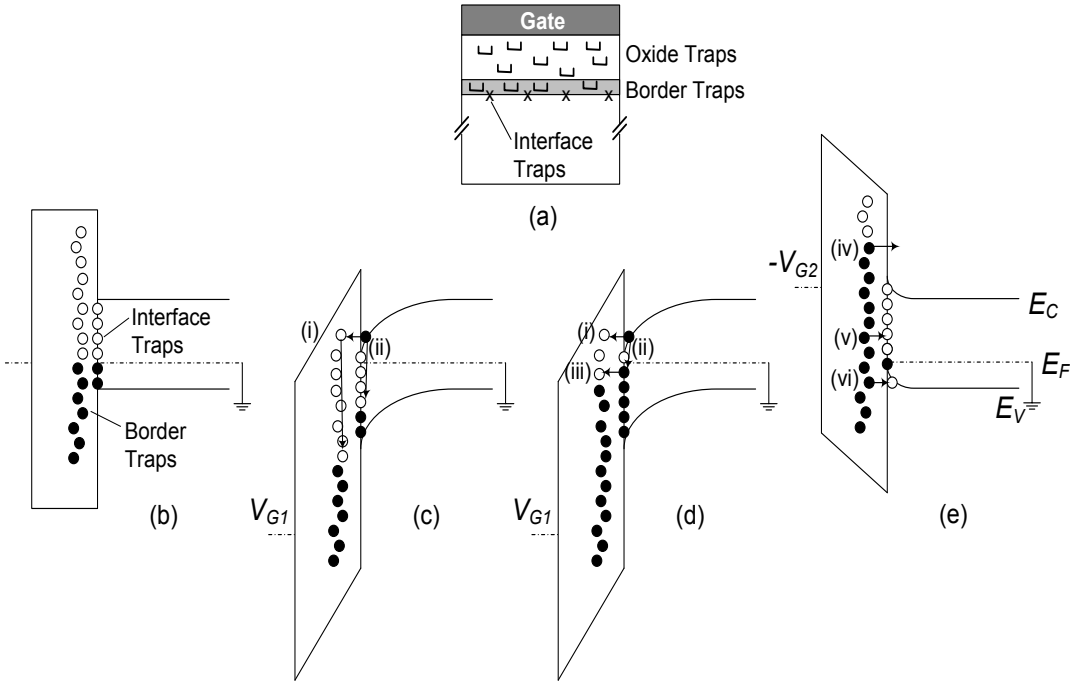


Figure 1.4: (a) Schematic of oxide, border, and interface traps, (b) flatband, (c) capture of electrons by interface traps and tunneling of electrons to border traps from conduction band, (d) border and interface trap occupied by electrons (e) electron tunneling from border traps. The solid circles represent occupied and the open circles unoccupied traps.

Electron tunneling is a direct tunnel process with time constant [18]

$$\tau_t \approx \tau_0 \exp(x/\lambda),\ \lambda = \frac{\hbar}{\sqrt{8m_t^*\phi_B}} \qquad (1\text{-}3)$$

where τ_0 is a characteristic time ($\approx 10^{-10}$ s), λ the attenuation length ($\approx 10^{-8}$ cm), m_t* the tunneling effective mass, and ϕ_B the barrier height at the semiconductor/insulator interface. τ_t varies from 0.01 to 1 s (100 to 1 Hz) for x varying from 1.8 to 2.3 nm. Hence border traps can be determined to a depth of approximately 2.5 nm from the SiO_2/Si interface by measurements for frequencies as low as 1 Hz. Such measurements include low-frequency noise, conductance, frequency-dependent charge pumping, and others. The valence band hole tunnel times are longer than for electrons due to the higher effective mass and barrier height.

1.4 Carrier Lifetimes

Carrier (electrons and holes) lifetimes are routinely measured for some bipolar semiconductor devices (solar cells, imagers), but usually not for unipolar devices like MOSFETs. Except for the reverse-biased drain leakage current, which is governed by electron-hole thermal generation or tunneling, lifetimes play no role in MOSFETs as the channel electrons never mix with substrate holes. Lifetime is very useful, however, because it is one of few parameters giving information about the low defect densities in today's semiconductors [19]. No other technique can detect defect densities as low as 10^9-10^{11} cm^{-3} in a simple, contactless room temperature measurement. In principle there is no lower limit to the defect density determined by lifetime measurements. It is for these reasons that the IC community, largely concerned with unipolar MOS devices, uses

lifetime measurements as a "process cleanliness monitor."

Different measurement methods can give widely differing lifetimes for the same material or device [20]. In many cases, the reasons for these discrepancies are fundamental and are not due to a deficiency of the measurement. The difficulty with defining a lifetime is that we are describing a property of a carrier within the semiconductor rather than the property of the semiconductor itself. Although we usually quote a single numerical value, we are measuring some weighted average of the behavior of carriers influenced by surfaces, interfaces, energy barriers, and the density of carriers besides the properties of the semiconductor material and its temperature. Lifetime measurements yield effective values influenced by the bulk and surfaces/interfaces.

Lifetimes fall into two primary categories: recombination lifetimes and generation lifetimes [21]. The concept of recombination lifetime τ_r holds when excess carriers decay as a result of recombination. Generation lifetime τ_g applies when there is a paucity of carriers, as in the space-charge region (scr) of a reverse-biased device and the device tries to attain equilibrium. During recombination an electron-hole pair ceases to exist on average after a time τ_r, illustrated in Figure 1.5(a). The generation lifetime, by analogy, is the time that it takes on average to generate an ehp, illustrated in Figure 1.5(b). Thus, generation lifetime is a misnomer, since the creation of an ehp is measured and generation time would be more appropriate. Nevertheless, the term "generation lifetime" is commonly accepted.

When these recombination and generation events occur in the bulk, they are characterized by τ_r and τ_g. When they occur at the surface, they are characterized by the surface recombination velocity s_r and the surface generation velocity s_g, also illustrated

in Figure 1.5. Both bulk and surface recombination or generation occurs simultaneously and their separation is sometimes quite difficult. The measured lifetimes are always effective lifetimes consisting of bulk and surface components [22].

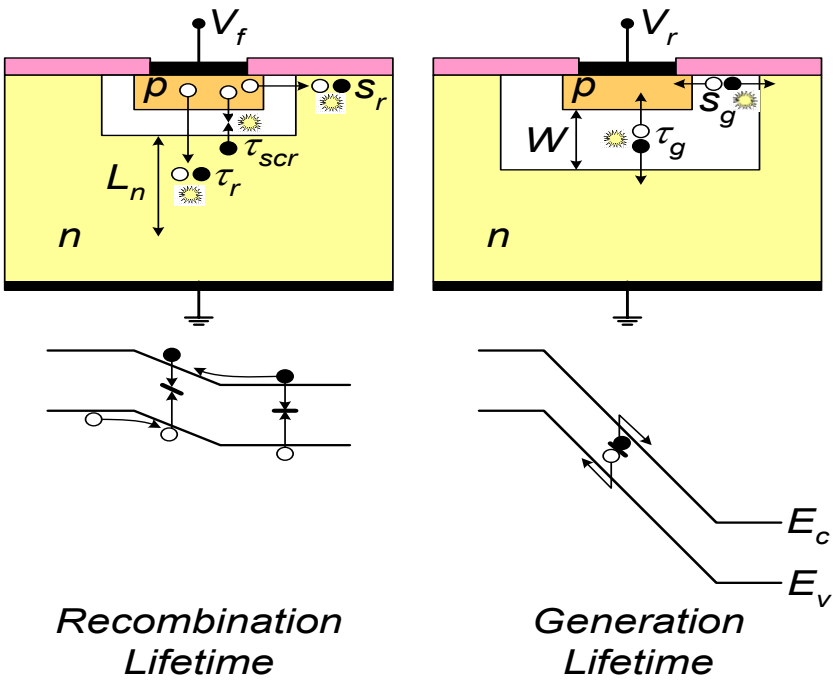


Figure 1.5: Cross section and energy band diagrams for forward- and reverse-biased junctions illustrating recombination and generation.

1.4.1 Recombination Lifetime/Surface Recombination Velocity

Three main recombination mechanisms determine the recombination lifetime: Shockley-Read-Hall (SRH) or multiphonon recombination characterized by τ_{SRH}, radiative recombination characterized by τ_{rad} and Auger recombination characterized by τ_{Auger}. The three recombination mechanisms are illustrated in Fig 1.6. The recombination lifetime τ_r is determined according to the relationship

$$\tau_r = \frac{1}{\tau_{SRH}^{-1} + \tau_{rad}^{-1} + \tau_{Auger}^{-1}} \tag{1-4}$$

During SRH recombination, electron-hole pairs recombine through deep-level impurities or traps, characterized by the density N_T, energy level E_T, and capture cross-sections σ_n and σ_p for electrons and holes, respectively. The energy liberated during the recombination event is dissipated by lattice vibrations or phonons, illustrated in Figure 1.6(a). The SRH lifetime is given by

$$\tau_{SRH} = \frac{\tau_p(n_o + n_1 + \Delta n) + \tau_n(p_o + p_1 + \Delta p)}{p_o + n_o + \Delta n} \tag{1-5}$$

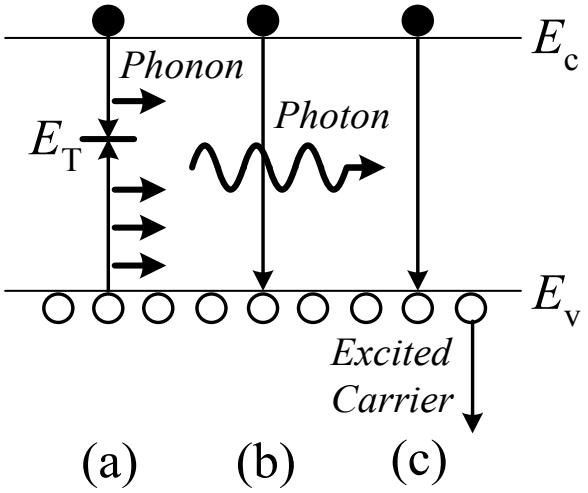


Figure 1.6: Three main recombination mechanisms: (a) SRH, (b) Radiative, and (c) Auger recombination.

where n_1, p_1, τ_n, and τ_p are defined as

$$n_1 = n_i \exp\left(\frac{E_T - E_i}{kT}\right);\ p_1 = n_i \exp\left(-\frac{E_T - E_i}{kT}\right);\ \tau_p = \frac{1}{\sigma_p v_{th} N_T};\ \tau_n = \frac{1}{\sigma_n v_{th} N_T} \tag{1-6}$$

The radiative lifetime is

$$\tau_{rad} = \frac{1}{B(p_o + n_o + \Delta n)} \tag{1-7}$$

where B is the radiative recombination coefficient. The radiative lifetime is inversely proportional to the carrier density because in band-to-band recombination both electrons and holes must be present simultaneously.

During Auger recombination, showed in Figure 1.6(c), the recombination energy is absorbed by a third carrier. The Auger lifetime is inversely proportional to the carrier density squared. The Auger lifetime is given by

$$\tau_{Auger} = \frac{1}{C_p(p_o^2 + 2p_o\Delta n + \Delta n^2) + C_n(n_o^2 + 2n_o\Delta n + \Delta n^2)} \approx \frac{1}{C_p(p_o^2 + 2p_o\Delta n + \Delta n^2)} \tag{1-8}$$

where C_p is the Auger recombination coefficient for a holes and C_n for electrons.

For low-level injection when the excess minority carrier density is low compared to the equilibrium majority carrier density, $\Delta n << p_o$; for high-level injection $\Delta n >> p_o$. The injection level is important during lifetime measurements. The appropriate expressions for low-level (ll) and for high-level (hl) injection become

$$\tau_{SRH}(ll) \approx \frac{n_1}{p_o}\tau_p + \left(1 + \frac{p_1}{p_o}\right)\tau_n \approx \tau_n;\ \tau_{SRH}(hl) \approx \tau_p + \tau_n \tag{1-9}$$

$$\tau_{rad}(ll) = \frac{1}{Bp_o};\ \tau_{rad}(hl) = \frac{1}{B\Delta n}\ ;\ \ \tau_{Auger}(ll) = \frac{1}{C_p p_o^2};\ \tau_{Auger}(hl) = \frac{1}{(C_p + C_n)\Delta n^2} \qquad (1\text{-}10)$$

The Si recombination lifetimes are plotted in Figure 1.7. At high carrier densities, the lifetime is controlled by Auger recombination and at low densities by SRH recombination. Auger recombination has the characteristic $1/n^2$ dependence. The high carrier densities may be due to high doping densities or high excess carrier densities. Whereas SRH recombination is controlled by the cleanliness of the material, Auger recombination is an intrinsic property of the semiconductor. Radiative recombination plays almost no role in Si because τ_{rad} is so high

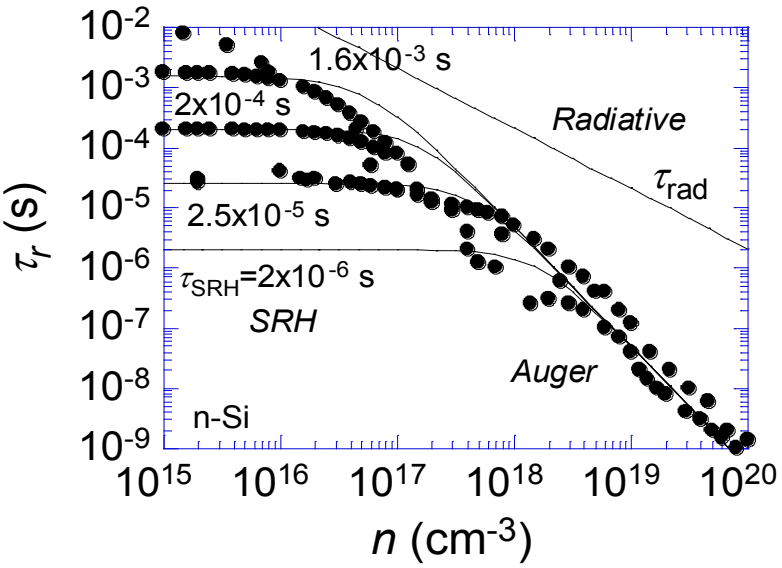


Figure 1.7: Recombination lifetimes due to three different recombination mechanisms in n-type silicon. SRH dominates at low doping density, while auger takes over at higher doping concentrations. Radiative recombination lifetime is usually higher than the other two for silicon and plays no role [2]. Courtesy of D. K. Schroder.

The surface recombination velocity s_r is:

$$s_r = \frac{s_n s_p (p_{os} + n_{os} + \Delta n_s)}{s_n (n_{os} + n_{1s} + \Delta n_s) + s_p (p_{os} + p_{1s} + \Delta p_s)} \tag{1-11}$$

hence the surface recombination velocity for low-level and high-level injection becomes:

$$s_r(ll) = \frac{s_n s_p}{s_n (n_{1s} / p_{os}) + s_p (1 + p_{1s} / p_{os})} \approx s_n; \; s_r(hl) = \frac{s_n s_p}{s_n + s_p} \tag{1-12}$$

where

$$s_n = \sigma_{ns} v_{th} N_{it}; \; s_n = \sigma_{ns} v_{th} N_{it} \tag{1-13}$$

and σ_{ns} and σ_{ps} are the capture cross sections of interface traps with density N_{it}.

1.4.2 Generation Lifetime/Surface Generation Velocity

Each of the recombination processes of Figure 1.6 has a generation counterpart, that is shown in Figure 1.8. The inverse of multiphonon recombination is thermal ehp generation. The inverse of radiative and Auger recombination are optical and impact ionization generation. Optical generation is negligible for a device in the dark and with negligible blackbody radiation from its surroundings. Impact ionization is usually considered to be negligible for devices biased sufficiently below their breakdown voltage. However, impact ionization at low ionization rates can occur at low voltages, and care must be taken to eliminate this generation mechanism during τ_g measurements.

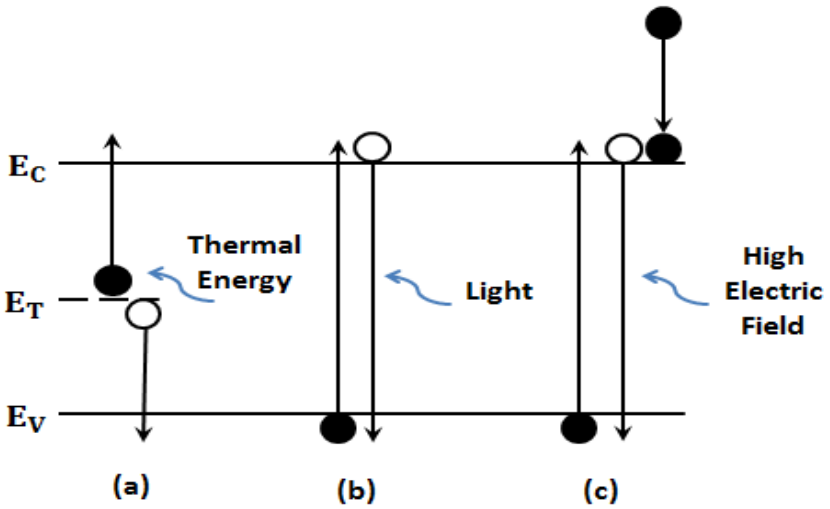


Figure 1.8: (a) thermal generation, (b) optical generation and (c) carrier multiplication.

The generation lifetime is

$$\tau_g = \tau_p \exp\left(\frac{E_T - E_i}{kT}\right) + \tau_n \exp\left(-\frac{E_T - E_i}{kT}\right) \approx \tau_r \exp\left(\frac{|E_T - E_i|}{kT}\right) \qquad (1\text{-}14)$$

τ_g depends inversely on the impurity density and on the capture cross-section for electrons and holes, just as recombination does. It also depends exponentially on the energy level E_T. The generation lifetime can be quite high if E_T does not coincide with E_i. Typically $\tau_g \approx (50\text{-}100)\,\tau_r$. The surface generation velocity is given by

$$s_g = \frac{s_n s_p}{s_n \exp((E_{it} - E_i)/kT) + s_p \exp(-(E_{it} - E_i)/kT)} \qquad (1\text{-}15)$$

as can be seen in equation 1-15 for $E_{it} \neq E_i$, s_r is larger than s_g.

1.4.3 Epitaxial Layer Recombination Lifetime/Minority Carrier Diffusion Length

Thin epitaxial layers on heavily-doped substrates can be characterized with generation

lifetime measurements, but present some recombination lifetime measurement difficulties. Let us consider the device in Figure 1.9(a) with different doping densities and different recombination lifetimes in the two regions. The same considerations apply to wafers with a low-defect density denuded zone on an oxygen-precipitated substrate in Figure 1.9(b). In this case the doping densities in the two regions are the same, but the recombination lifetimes are different. For zero recombination at the upper surface, the effective minority carrier diffusion length in the layer of thickness t is [22]

$$L_{n,eff} = L_n \frac{1+(s_{\text{int}}L_n/D_n)\tanh(k)}{\tanh(k)+s_{\text{int}}L_n/D_n};\ k=\frac{t}{L_n} \tag{1-16}$$

where t is the layer thickness, s_{int} the interface recombination velocity, L_n the true layer minority carrier diffusion length and D_n the electron diffusion coefficient. In this equation the substrate recombination is represented by the interface recombination velocity and minority carriers can recombine in the layer and at the interface.

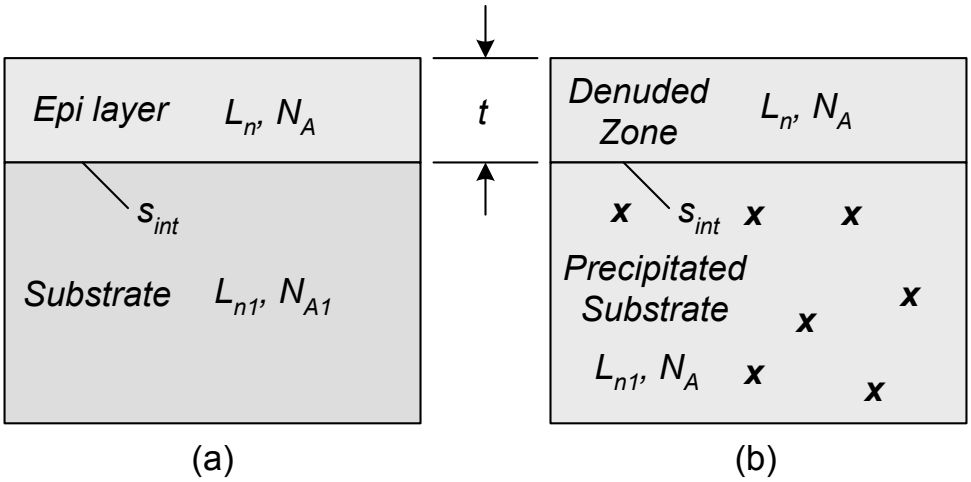


Figure 1.9: (a) Epi/substrate and (b) denuded zone/precipitated substrate.

The interfacial recombination velocity depends on the epi-layer and substrate doping

densities, N_{epi} and N_{sub}, on the substrate diffusion length and diffusion coefficient, L_{sub} and D_{sub}, the substrate thickness t_{sub} and the surface recombination velocity at the substrate bottom contact s_b

$$s_{\text{int}} = \frac{N_{epi}}{N_{sub}} \frac{D_{sub}}{L_{sub}} \exp[(\Delta E_{G,sub} - \Delta E_{G,epi})/kT] \frac{(s_b L_{sub}/D_{sub}) + \tanh(t_{sub}/L_{sub})}{1 + (s_b L_{sub}/D_{sub}) \tanh(t_{sub}/L_{sub})} \qquad (1\text{-}17)$$

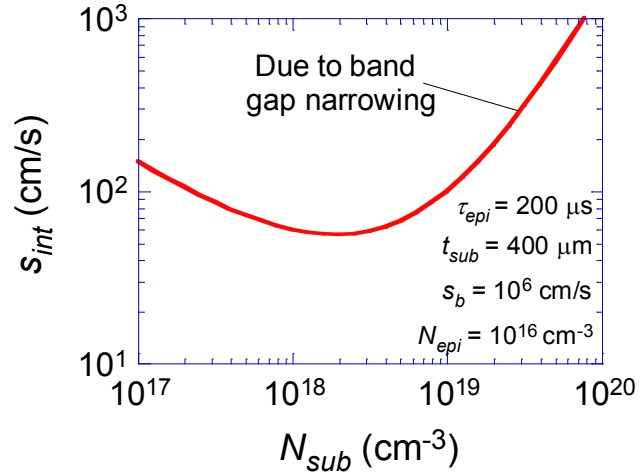
where s_b is the surface recombination velocity at the back substrate surface. The energy gap depends on doping density. As the doping density of a semiconductor increases, the energy gap decreases according to

$$\Delta E_G = 0.231 \left[\left(\frac{10^{20}}{N_A} \right)^{0.75} + 1 \right]^{-2/3} \qquad (1\text{-}18)$$

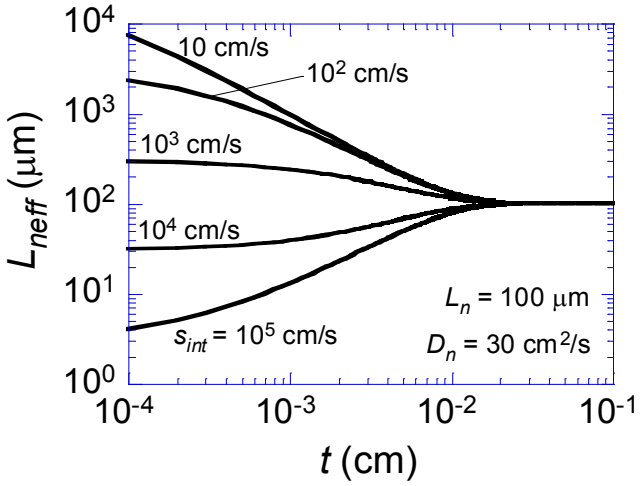
This makes it easier for minority carriers to diffuse to the substrate to recombine there which is reflected in a change of s_{int}. The dependence of s_{int} on N_{sub} is shown in Figure 1.10(a) and the dependence of L_{neff} on thickness and s_{int} in Figure 1.10(b).

The effective diffusion lengths in Figure 1.10(b), calculated with the above equation, show that it is very difficult to determine the true diffusion length, which is 100 μm in this example. In fact, L_{neff} can be higher or lower than L_n and depends very sensitively on the interfacial recombination velocity. For $s_{int} \Rightarrow 0$, L_{neff} becomes L_n^2/t and for $s_{int} \Rightarrow \infty$, L_{neff} becomes t. To determine the true diffusion length, the epi layer thickness $t \approx 3L_n$, because the characteristic length for recombination lifetime measurements is the diffusion length. This is rarely possible, however, since the layer diffusion length is hundreds of microns and the thickness is a few microns. This shows that the recombination lifetimes

or diffusion lengths of epi layers are difficult to determine. Generation lifetime measurements, on the other hand, confine the generation length to the space-charge region width which is typically contained within the epi layer and is under the control of the operator.



(a)



(b)

Figure 1.10: (a) Dependence of s_{int} on N_{sub} and (b) dependence of L_{neff} on s_{int} and t.

As a good example of this case let's consider a p/p$^+$ epitaxial layer that is contaminated with 10^{10}cm^{-3} metallic impurities. According to the equation 1-19 one should expect to have recombination lifetime in order of 1 ms.

$$\tau_r = \frac{1}{\sigma_n \vartheta_{th} N_T} \tag{1-19}$$

where σ_n is the minority carrier capture cross section, v_{th} the thermal velocity and N_T the deep-level impurity concentration. For τ_r =1 ms, it has been assumed that σ_n=10^{-14} cm^2, v_{th}=10^7 cm/s and N_T =10^{10} cm^{-3}. The recombination lifetime is measured over a distance of approximately a minority carrier diffusion length L_n=$(D_n \tau_r)^{1/2}$. τ_r =1 ms and D_n=36 cm^2/s $\Rightarrow$ L_n=1900 μm, which is much longer than typical epi layer thicknesses of several μm and recombination lifetime measurements by, for example, photoconductance decay, are unsuitable because they measure a combination of epi-layer and substrate lifetime. The substrate lifetime, owing to its much higher doping concentration than the epi-layer, is much lower than the epi-layer lifetime. The generation lifetime, on the other hand, is measured in a reverse-biased space-charge region, whose width is determined by the gate voltage of the MOS capacitor, which is under the experimenter's control. Furthermore, the generation lifetime is an important parameter for the dark current of CMOS imagers. The space-charge region generated dark current density is given by

$$J_{dk} = \frac{q n_i W}{\tau_g} \tag{1-20}$$

where n_i is the intrinsic carrier concentration and W the space-charge region width. Room temperature, W=3 μm and τ_g=10 ms $\Rightarrow$ ~5x10^{-11} A/cm^2.

The generation lifetime τ_g is related to the recombination lifetime by

$$\tau_g = \tau_r \exp\left(\frac{|E_T - E_i|}{kT}\right) \tag{1-21}$$

where E_T is the impurity energy level, E_i the intrinsic energy level and T the temperature. Just as surface recombination influences recombination lifetimes, the electron-hole pair interface generation at the SiO_2/Si interface influences generation lifetimes and an effective generation lifetime is measured. For $|E_T$-$E_i|$≈0.05-0.1 eV, it is expected that τ_g≈10-50 τ_r, but this value will be somewhat reduced by interface generation.

1.5 Effect of Lifetime and Defects on Device Parameters

Aside from being a direct measure of metallic impurity density in Si, the lifetime itself is a critical parameter that controls many of today's devices performance. Therefore lifetime measurement is more than just a process cleanliness monitoring tool and gives viable information on how to expect a device to work.

In Charge Coupled Devices (CCD) [23], which is of particular interest in this context, the presence of impurities and reduced lifetime will cause the quantum efficiency to degrade following the equation 1-22. Quantum efficiency (η) is an important parameter in CCDs which is a measure of how well the device converts the incident optical photons to CCD charge.

$$\eta = \left(\frac{(1-R)\alpha L_n}{(\alpha L_n)^2 - 1}\right)\left(\frac{\mathrm{K} + \alpha L_n}{Den} - (\alpha L_n + A)e^{-\alpha T_{bulk}}\right) + (1-R)e^{-\alpha T_{bulk}}(1 - e^{-\alpha W}) \qquad (1\text{-}22)$$

where R is the reflectivity, T_{bulk} bulk thickness, L_n the minority carrier diffusion length that is related to lifetime through L_n=$\sqrt{D_n \tau_r}$ where D_n is minority carrier diffusion coefficient and τ_r recombination lifetime, α optical absorption coefficient, K= $s_r L_n / D_n$ where s_r is the surface recombination velocity, and A= $(\mathrm{K}\cosh(\xi) + \sinh(\xi))/Den$ where Den is $\cosh(\xi) + \sinh(\xi)$. As equation 1-22 suggests, many lifetime parameters influence the quantum efficiency of CCDs: τ_r, s_r, and L_n. A high η would be obtained with small ξ and short s_r. The latter is usually controlled through p/p$^+$ structures [24]. ξ, however, can be made small by reducing L_n or decreasing the thickness. L_n is directly related to recombination lifetime τ_r.

Another important parameter in CCDs is the dark signal, also referred to as dark current or dark charge. It describes the output in the absence of any external radiation. For silicon devices operating at room temperature, this current originates from scr rather than qnr and hence it is due to the thermal generation of ehp in the scr through equation 1-23.

$$J_{dark\ current} = J_{scr} = q n_i \left(\frac{W}{\tau_g} + s\right) \qquad (1\text{-}23)$$

where W is the scr width, τ_g generation lifetime in the scr and s is the surface generation velocity. The dark current itself is not a serious problem in CCDs, but its variation

throughout an imaging array is detrimental. Such problem occurs when there are defects in parts of the system giving rise to localized reduced generation lifetime.

Total signal delay in a *N*-stage CCD is defined as:

$$t_d = N/f_c \tag{1-24}$$

where f_c is the clock frequency. According to equation 1-24, the delay time can be varied by changing the clock frequency. In practice, however, the upper bound is limited by thermally generated electron hole pairs which add charge to the potential well and hence distort the signal. Signal to noise ratio is influenced directly by the defects in the material. This happens by the interaction of charge packets with the traps in form of electron capture and emission. In Surface-CCDs interface states act as traps, while in Bulk-CCDs impurities act as traps.

And finally, the modulation transfer function (MTF) which is a measure of resolution is CCDs is under influence of lifetime. Total MTF in CCDs is comprised of three components:

$$\mathrm{MTF_{CCD}} = \mathrm{MTF_d} \times \mathrm{MTF_s} \times \mathrm{MTF_t} \tag{1-25}$$

where $\mathrm{MTF_t}$ is due to charge-transfer inefficiency, $\mathrm{MTF_s}$ is due to spacing between charge-collection wells and $\mathrm{MTF_d}$ is due to minority carrier diffusion in the device. $\mathrm{MTF_d}$ [25] is proportional to the minority carrier diffusion length and so the recombination lifetime.

In p-n junctions the leakage current in reverse bias is related to lifetime and hence the metallic impurity density through [26]:

$$J_R = q\sqrt{\frac{D_p}{\tau_p}}\left(\frac{{n_i}^2}{N_D}\right) + \frac{qn_iW}{\tau_g} \quad (1\text{-}26)$$

where N_D is doping concentration, D_p hole diffusion constant, τ_p hole recombination lifetime, $\tau_g$the generation lifetime, and W is the scr width. According to equation 1-26, increasing the impurity density which will lead to reduced recombination/generation lifetime will result in an increase in junction leakage current in reverse bias.

Defects in DRAMs would cause degraded refresh time and storage time [27]. In bipolar devices defects will lead to leakage currents and reduced gain as dislocation pipes forms through the device structure [1].

MOSFETs are not directly influenced by lifetime. The reason behind this is the separation of minority layer (channel) from majority carriers through scr. However, defects in these devices will lead to leakage current from drain and source to body which is not favorable. Moreover, the presence of defects will cause degradation of gate oxide integrity. Figures 1.11 and 1.12 show that the oxide breaks down at lower electric fields when the defect density increase [2].

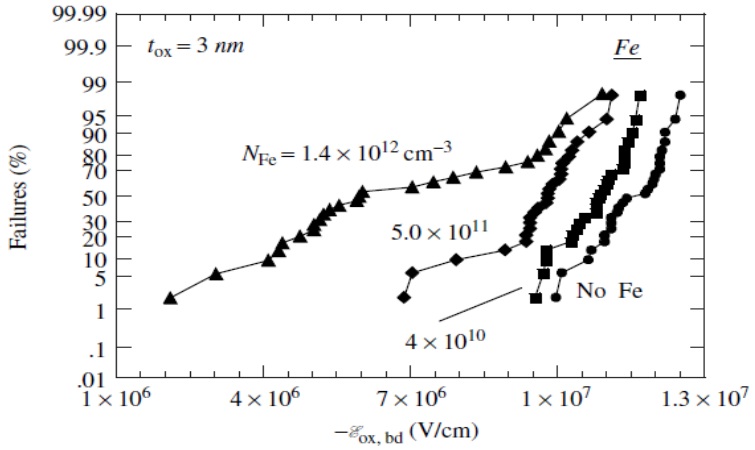


Figure 1.11: Oxide failure percentage versus oxide breakdown electric field as a function of metal contamination for Fe-contaminated Si. Courtesy of D. K. Schroder.

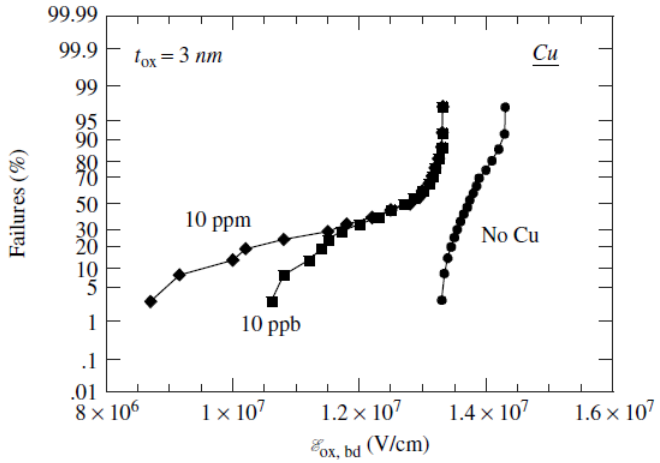


Figure 1.12: Oxide failure percentage versus oxide breakdown electric field as a function of metal contamination for Cu-contaminated Si; the wafers were dipped in a 10 ppb or 10 ppm CuSO4 solution and annealed at 400 ºC. Courtesy of D. K. Schroder.

1.6 Pulsed MOS Capacitor for Lifetime Measurement

Previously, the importance of carrier lifetime in silicon was mentioned. It was also noted that for epitaxial layers measuring generation lifetime is more applicable than recombination lifetime. Generation lifetime measurement techniques are categorized based on the type of perturbation introduced, what is measured, and how one evaluates the experimental data. One of the most widely-used techniques for measuring generation lifetime is pulsed MOS-C where the generation current – which is similar to operational conditions of DRAMs and CCDs – is measured in a non-equilibrium MOS-C that is pulsed into deep-depletion. MOS-C devices, in contrast to other semiconductor devices that are characterized by their current-voltage behavior, are characterized by their charge-voltage and charge-time behaviors. This key feature makes them interesting test structures for investigation of lifetime in semiconductors. Considering a p-type MOS-C the capacitance in the device is described as:

$$C = dQ_G/dV_G \tag{1-27}$$

where Q_G represents the gate charge and V_G is the gate voltage. This capacitance is change of charge in respect to change of gate voltage and has units of farad/unit area. Since the total charge in the device sums to zero then:

$$Q_G = -(Q_s + Q_{it}) \tag{1-28}$$

$$Q_s = Q_p + Q_b + Q_n \tag{1-29}$$

where Q_s is the semiconductor charge and Q_{it} is the interface trapped charge – assuming there is not oxide charge. Q_s itself is comprised of hole charge density Q_p, electron charge in inversion layer Q_n, and scr charge density Q_b.

The gate voltage partially drops across the oxide and partially across the semiconductor and hence:

$$V_G = V_{FB} + V_{ox} + \varphi_s. \tag{1-30}$$

where $V_{FB}$is the flatband voltage, V_{ox} the oxide voltage and φ_s is the surface potential, as illustrated in Figure 1.13.

Therefore, taking into account equations 1-28 through 1-30, the equation 1-27 can now be rewritten as:

$$C = \frac{1}{\frac{dV_{ox}}{dQ_s + dQ_{it}} + \frac{d\varphi_s}{dQ_p + dQ_b + dQ_n + dQ_{it}}} \tag{1-31}$$

Equation 1-31, based on basic definition of capacitance, contains five different capacitances, namely: C_{ox}, C_p, C_b, C_n and C_{it}. It can be written as:

$$C = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_p + C_b + C_n + C_{it}}} \tag{1-32}$$

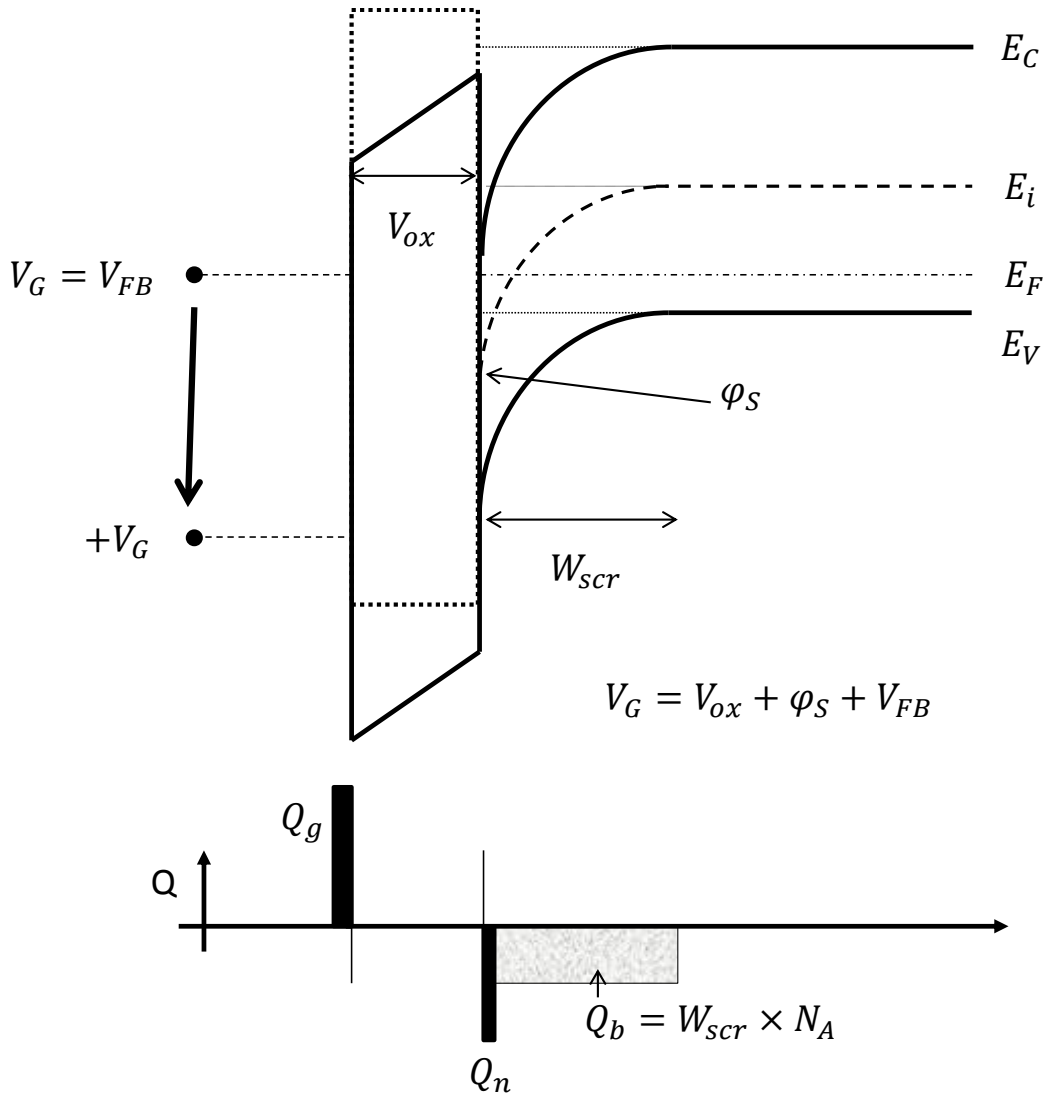


Figure 1.13: Energy band diagram of a heavily inverted MOS-C device. Below is the charge distribution diagram which shows the gate charge, inversion layer charge and scr charge. Interface trap charges are not illustrated in this Figure.

Each of these capacitances dominates at a specific gate voltage due to their series and parallel combination and their charge component. Figure 1.14, shows the equivalent

circuit of a MOS-C in different gate voltages. When the gate voltage is positive, the accumulation charge (hole charge density) $Q_p$becomes very large and $C_p$dominates over other four capacitances. However, since C_p and C_{ox} are in series, C_{ox} will dominate over C_p and the capacitance that is measured at positive gate voltages is the oxide capacitance. At small positive gate voltages, where device is slightly depleted, the scr capacitance and interface charge capacitance will dominate. At negative gate voltages where the inversion layer has formed beneath the gate, $Q_n$will dominate. The measured capacitance for this case depends on the probing ac signal frequency. If the frequency is low enough so that the inversion layer charge can follow it, the C_n will dominate over four other capacitances and since it is in series with C_{ox} the measured capacitance would be C_{ox}. On the other hand, if the frequency is high so that the minority carriers cannot follow it, then scr capacitance will dominate and the measured capacitance would be a combination of C_{ox} and C_b. Figure 1.15 shows a typical *C-V* curve that exhibits all four capacitances.

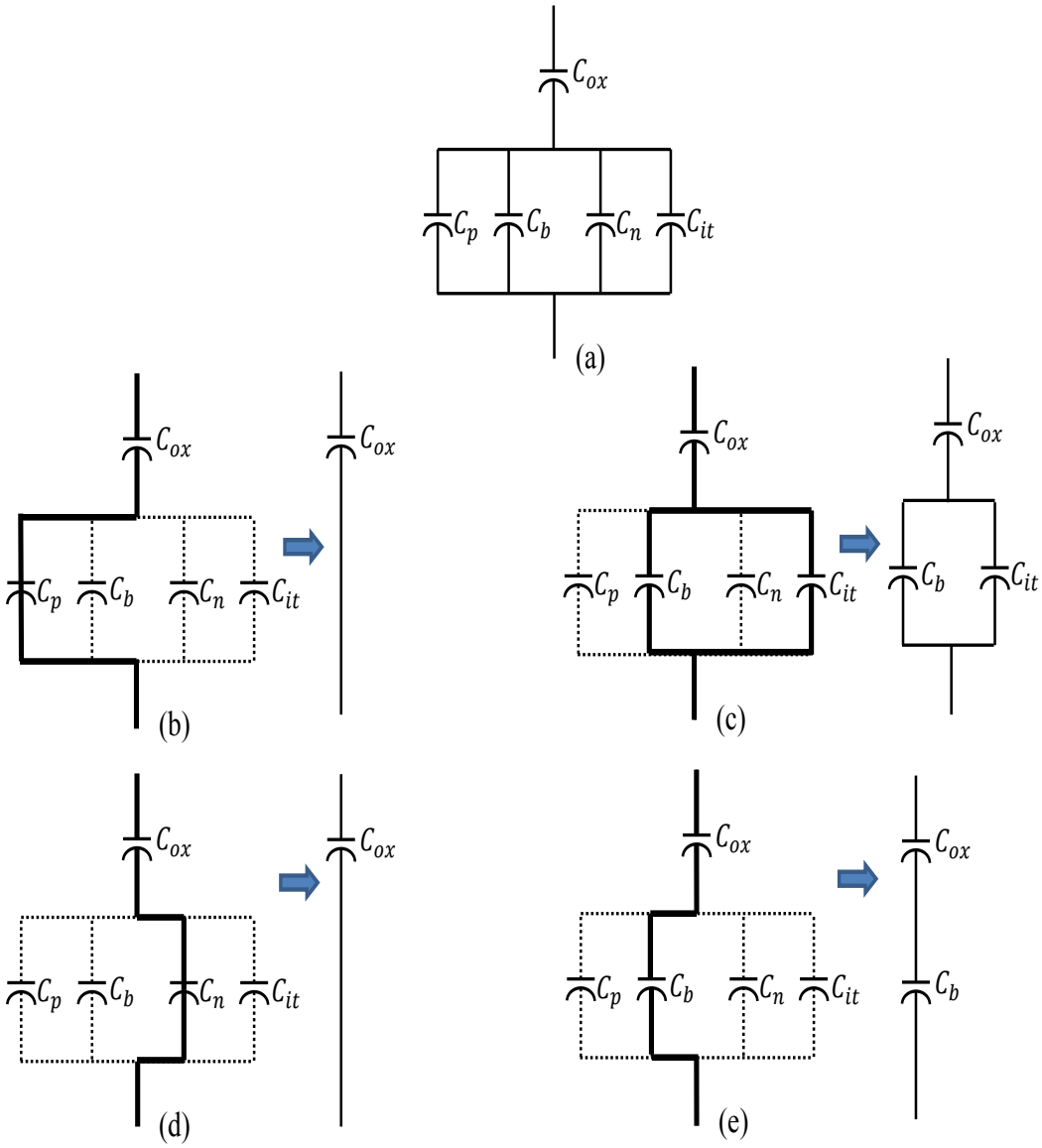


Figure 1.14: (a) MOS-C equivalent circuit for different gate voltages: (b) accumulation, (c) depletion, (d) low frequency inversion, and (e) high frequency inversion.

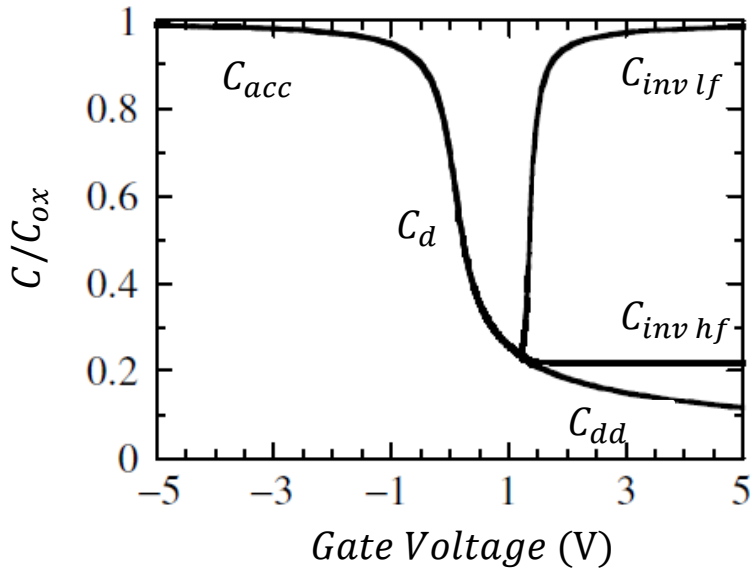


Figure 1.15: Normalized *C-V* curve of a p-type MOS-C showing C_{acc} which is equal to C_{ox}, the capacitance in depletion region C_d, inversion capacitance in low-frequency region $C_{inv\ lf}$, inversion capacitance in high-frequency region $C_{inv\ hf}$, and deep-depletion capacitance C_{dd}.

All of four above mentioned states are equilibrium conditions. In practice, however, the formation of the inversion layer – unlike the scr width that can instantly change – requires generation of electron hole pairs (ehp) which does not happen instantly. When a MOS-C device is pulsed quickly from accumulation to inversion a fifth non-equilibrium state would occur called the deep-depletion. The scr width in this case would be extended beyond its equilibrium value and the surface will remain depleted until minority carriers are generated to from the inversion layer and the device moves back to equilibrium state with scr width returning to its equilibrium value. The inversion layer's electrons will be

supplied mainly through generation of electron hole pairs. This concept was first introduced and used for study of generation properties by Rupprecht [28].

When a fabricated MOS-C device on an epitaxial layer is pulsed from accumulation to deep depletion, in the absence of any external excitation such as light, seven thermal generation mechanisms become active to supply minority carriers and drive it back to equilibrium, as shown in Figure 1.16.

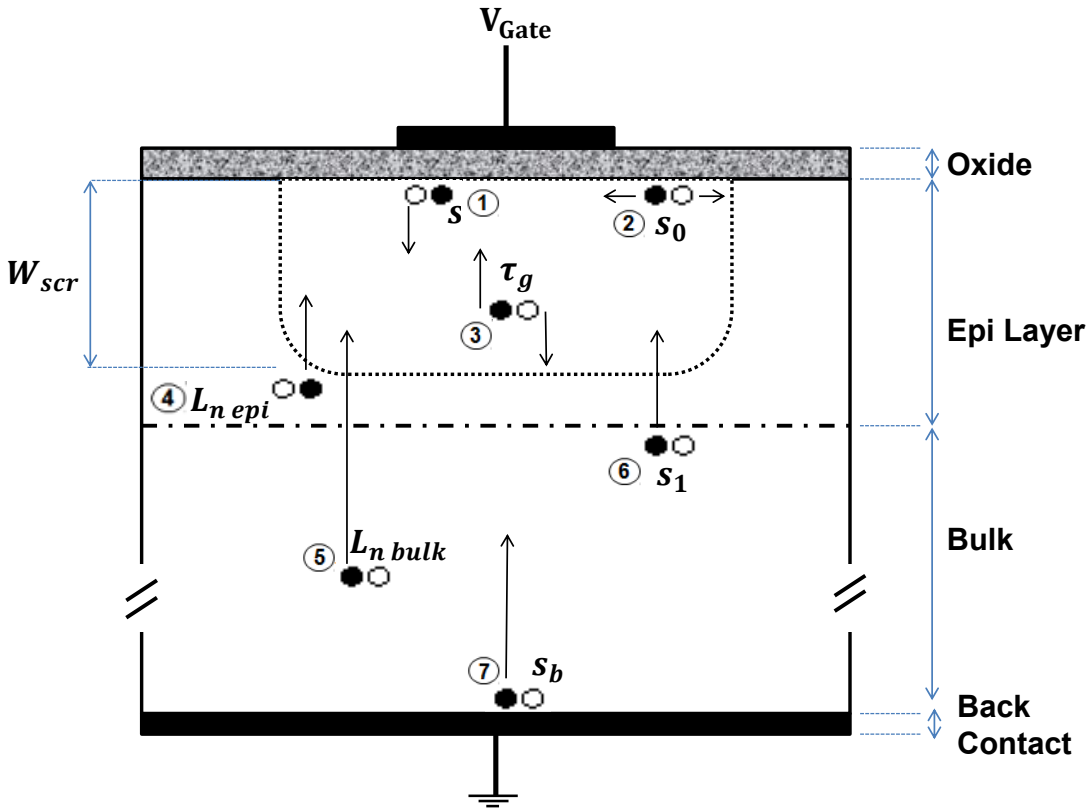


Figure 1.16: Seven generation mechanisms that drive the deep depleted MOS-C device back to equilibrium.

number 1 and 2. In this case, s_0 is the surface generation velocity in the lateral portion of the space charged region (scr) beyond the inversion layer which is always depleted of

minority carriers and so its value remains constant during the transition. The term *s*, on the other hand, is the surface generation velocity in the lateral portion of the scr under the gate which is initially depleted and equal to s_0 but as time passes and the inversion layer forms decreases to a final theoretical value of 0. There is also carrier generation in both the quasi neutral region (qnr) of the epitaxial layer and the substrate. These generations are characterized by their respective diffusion length – mechanisms number 5 and 4 – since that is how they contribute in supplying minority carriers to scr and forming the inversion layer. The epi/bulk interface and the back ohmic contact can also be considered for their surface generation and are respectively characterized by s_1 and s_b – mechanisms numbers 6 and 7. And finally, τ_g – mechanism number 3 – which is the generation in the scr where electron hole pairs are generated on deep level impurity energy levels. This latter mechanism is of interest since it is directly related to deep level impurity density in epitaxial layer following:

$$\tau_g \approx \tau_r \times \exp\left(\frac{|E_T - E_i|}{kT}\right);\ \tau_r = \frac{1}{\sigma_n \vartheta_{th} N_T}$$
$$\rightarrow \tau_g = {N_T}^{-1} \times A \qquad (1\text{-}33)$$

where E_T is the deep level impurity energy level, E_i intrinsic energy level, σ_n is minority carrier capture cross section, ϑ_{th} the thermal velocity, N_T the deep-level impurity concentration, and *A* is a constant.

Each of these mechanisms can be considered as a current that discharge a charged capacitor, as illustrated in Figure 1.17. The scr current can then be written as:

$$J_{scr} = qn_i \frac{A(W - W_F)}{\tau_g} + qn_i A_s s_0 + qn_i As \tag{1-34}$$

where W is the non-equilibrium scr width, W_F the equilibrium scr width when the inversion layer has formed and A is the gate area. The qnr current can be written as:

$$I_{qnr} = \frac{qn_i{}^2 D_n}{N_A L_{n\,eff}} \tag{1-35}$$

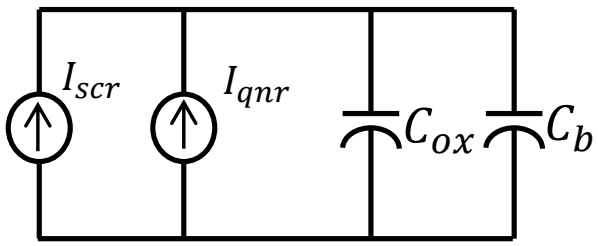


Figure 1.17: Equivalent circuit for a deep-depleted MOS-C. Two I_{scr} and I_{qnr} currents discharge the charged capacitor.

The $L_{n\,eff}$, as previously mentioned, characterizes the diffusion of minority carriers that have been generated both in qnr of epitaxial layer and the substrate as well as the epi/ bulk interface and probably the back contact surface. It is an effective value that is determined by minority carriers' diffusion length in qnr of epitaxial layer $L_{n\,epi}$, substrate $L_{n\,sub}$, s_1 and s_b through equations 1-16 and 1-17.

Assuming that the lateral area of the scr is dependent on the scr width through:

$$A_s = 2\pi r(W - W_F) \tag{1-36}$$

then the first two terms in equation 1-34 can form a width-dependent current as:

$$I_1 = qn_i \frac{A(W - W_F)}{\tau_{g\,eff}} = qG_1A \tag{1-37}$$

where $\tau_{g\,eff}$ is an effective generation lifetime whose value is determined by:

$$\tau_{g\,eff} = \frac{\tau_g}{1 + 2s_0\tau_g\,/r} \tag{1-38}$$

where r is the gate radius. The third term in equation plus the qnr current will form a width independent current as:

$$I_2 = qn_iAs' = qG_2A \tag{1-39}$$

where s' is an effective value whose value is determined by:

$$s' = s + {n_iD_n}\Big/{N_AL_{n\,eff}} \tag{1-40}$$

When the MOS-C device is pulsed into deep depletion – *i.e,* a positive gate voltage pulse is applied – in the absence of any external excitation such as light, thermal generation of electron hole pairs starts at t=0 both in scr and qnr. Electrons will reach to the oxide/Si interface by means of diffusion and drift to form the inversion layer, while holes will partly neutralize the ionized acceptor at the edge of scr and partly form a current through loop. As a result, the non-equilibrium scr width at *t*=0 will start to decrease with time. Since the C_b is inversely proportional to scr width, its value will increase from a minimum value at $t = 0$ to its maximum value which is the hf inversion capacitance at $t = t_f$, as shown in Figure 1.18.

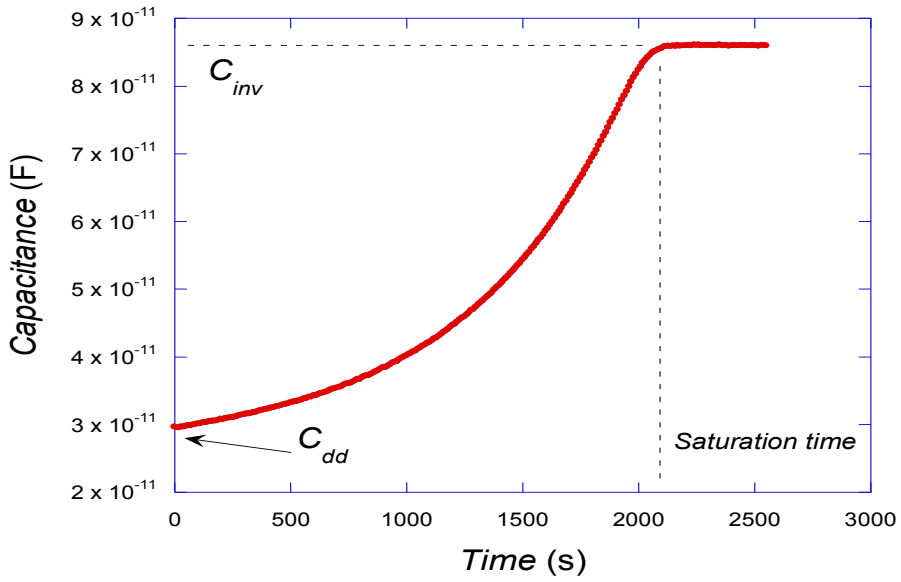


Figure 1.18: *C-t* curve for a pulsed MOS-C device from accumulation to deep-depletion.

According to equation 1-29 and the definition of oxide capacitance the oxide voltage can be defined as

$$V_{ox} = \frac{Q_{ox}}{C_{ox}} = \frac{Q_b + Q_n}{C_{ox}} = \frac{qN_A W_{scr} + Q_n}{C_{ox}} \tag{1-41}$$

Using the equation 1-30, substituting for φ_s by:

$$\varphi_s = qN_A W^2 / 2K_s \varepsilon_0 \tag{1-42}$$

, and assuming that the flatband voltage does not change with time, since the gate voltage throughout the capacitance transition is kept constant we can write:

$$\frac{dV_G}{dt} = \left(\frac{qN_A dW}{dt} + \frac{dQ_n}{dt}\right)\frac{1}{C_{ox}} + \frac{qN_A W}{K_s \varepsilon_0}\frac{dW}{dt} = 0 \tag{1-43}$$

Replacing dQ_n/dt with generation components of equation 1-37 and 1-39 and solving the resulting differential equation for *C* in respect to time by appropriate boundary conditions will result in equation 1-44 which describes the *C-t* curve of Figure 1.16 where the MOS-C device is transitioning from deep-depletion to inversion (for detailed solution see reference [29]):

$$(1-\gamma)ln\frac{(C_F/C_i-1+\gamma)}{(C_F/C-1+\gamma)}+\frac{C_F}{C_i}-\frac{C_F}{C}=\frac{C_F n_i t}{C_{ox}N_A\tau_{g-eff}} \quad (1\text{-}44)$$

$$\gamma = C_F s'\tau_{g\,eff}/K_s\varepsilon_0 \quad (1\text{-}45)$$

in equation 1-44 C_F is the inversion capacitance, and C_i is the initial deep-depletion capacitance. This equation can be used to extract the generation lifetime value from experimental *C-t* curves, as it will be mentioned in the subsequent chapters.

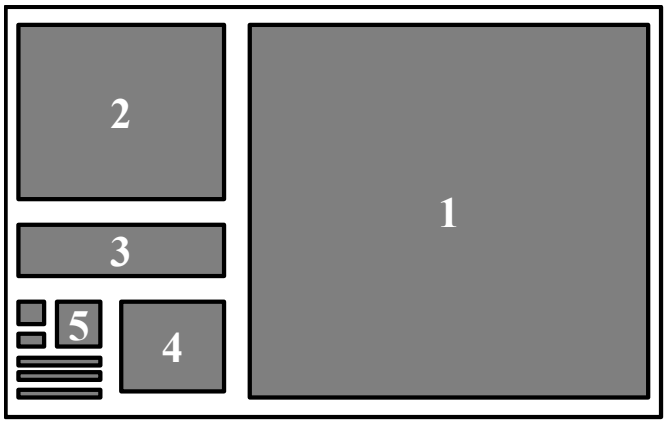
CHAPTER 2:

EXPERIMENT

2.1 Sample Preparation

I received two packages of wafers from Samsung Electronics. First package, which was received initially, included two sets of samples with four different types of wafers in each. One set called "GOI" (Gate Oxide Integrity) has MOS capacitors of different areas with poly-silicon gates, as shown in Figure 2.1, and the second set was bare silicon wafers of the corresponding wafer types. Each wafer has a p-epi on a p^+ substrate type structure. The wafer cross section is shown in Figure 2.2. The thickness of the epi layer is 4 μm with resistivity ρ_{epi} = 30 ohm-cm and the substrate is 725 μm thick with $\rho_{susbtrate}$ = 0.001 ohm-cm. The back of all wafers (GOI and bare silicon) have a 300 μm oxide layer, a remnant of the epi growth process. The physical wafer structure is the same for all the wafers except they differed by the purge time of the epi layer. The different purge times are 300, 600, 1200, and 1800 s; the wafers are labeled as Purge 300 (P300), Purge 600 (P600), Purge 1200 (P1200), and Purge 1800 (P1800), respectively, according to their purge times. This nomenclature will be used to address the different wafers in the rest of the document. I also fabricated MOS capacitor with aluminum gates on the bare silicon wafers for lifetime measurements as the results from the poly-silicon-gate samples were inconclusive and showed unexpected behavior, it is discussed in the subsequent section. First, the 300 nm bottom oxide was removed by dipping the wafers in 10:1 diluted HF in DI water for 10 minutes and rinsing thoroughly in DI water followed by drying. Then the

wafers were cleaned using RCA1 (5:1:1 ratio of water, ammonium hydroxide (NH_4OH), and hydrogen peroxide (H_2O_2)) and RCA2 (6:1:1 ratio of water, hydrochloric acid (HCL), and hydrogen peroxide (H_2O_2)) cleaning method to remove organics and metal contaminants.



Size: #1- 4x4 mm, #2 - 2x2 mm, #3 - 2x1 mm, #4 - 1x1 mm, #5 - 0.5x0.5 mm

Figure 2.1: Top view of poly-silicon gate devices fabricated on p/p+ wafers.

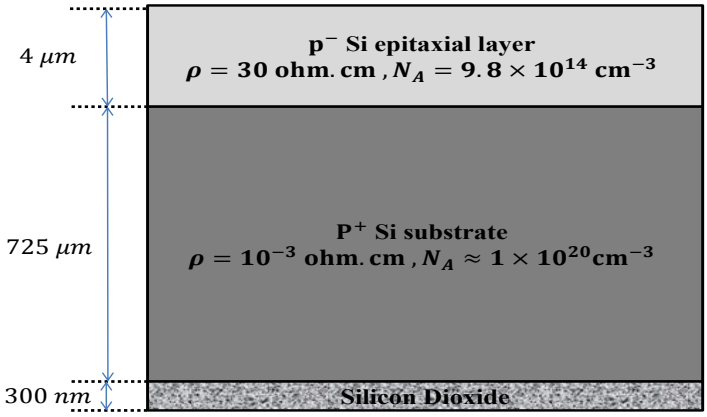


Figure 2.2: p- on p+ epitaxial silicon wafer cross section.

A 47 nm thick thermal oxide was grown on the epi-side of the wafer and circular metal gates of 1 mm diameter and 300 nm thickness were formed on top of the gate oxide

by evaporating aluminum in an e-beam evaporator through a shadow mask. Al contact was also formed on the wafer back after removing the back oxide using concentrated HF swab (backside oxide was formed during gate oxide growth).

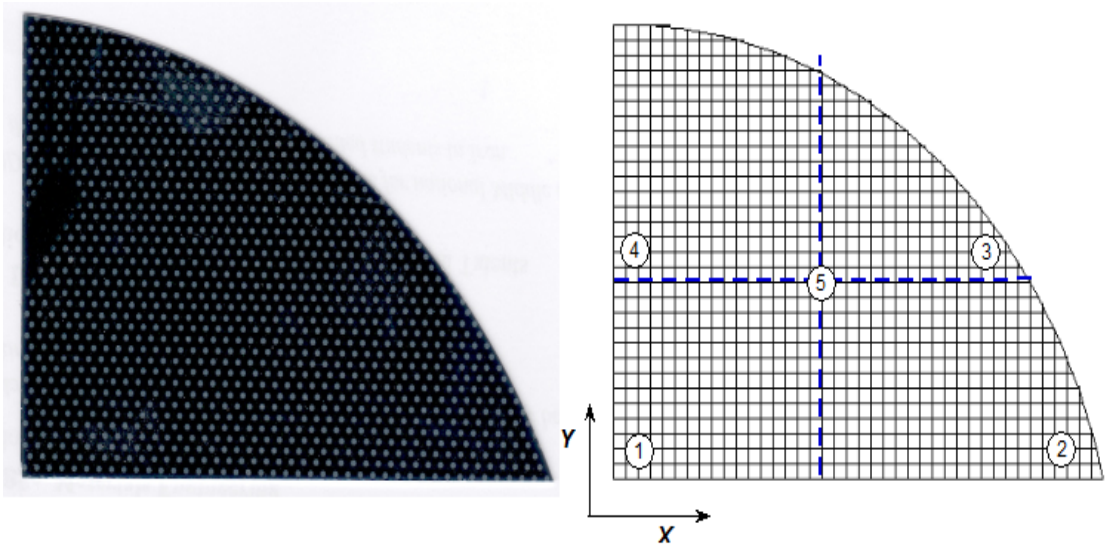
The second packaged, which I received in the second half of project, included two sets of wafers with already grown 20 nm thermal oxide on top and had the same structural properties as fist package. At the moment, our cleanroom's furnace was not capable of growing such thin oxide. Moreover, since the oxide was deposited in an industrial fab I expected that the oxide/Si interface for new package me be better in quality than the first package whose oxide was deposited at our local facility, ASU. Previous characterization measurements were performed on these wafers by the vendor (LG Electronics). DLTS measurements are suggesting that one set is having $3 \times 10^{10}\text{cm}^{-3}$, while the other set has less that 10^{10}cm^{-3} Tungsten contamination densities. Dark current measurement and Arrhenius plots measured by the vendor were suggesting that the Tungsten is having an energy level of $E_T = E_V + 0.41$ eV though Si band-gap. I will refer to these samples as more- and less-contaminated wafers.

To characterize these samples under different experimental conditions, I broke the wafers into segments by scratching a small spot near the edge of the wafer and since the orientation of the surface is (001), the cleavage mechanism did the rest automatically by applying a moderate torque to the wafer. Special care was taken during fabrication process to reduce contamination as much as possible. The oxide thickness was measured by ellipsometry and it was in good agreement with the reference thickness of 20 nm. The size of the samples is ~10x10 cm^2 in the form of quarters from a 200 mm wafer.

The aluminum gates were evaporated through a shadow mask with circular holes of 1 mm in diameter. The shadow mask was cleaned with isopropyl alcohol (IPA) to reduce its contamination. The deposition was done in an E-Beam Lesker-75 PVD evaporator. The 300 nm back oxide was removed with concentrated HF, like previous samples. The thickness of gates and back contact are 200 nm, deposited at a rate of 2 Å/s with the sample rotating during the deposition. Forming gas annealing, to reduce interface traps, was done at 450 °C with 95% nitrogen and 5% hydrogen for 30 minutes.

For a valid statistical experiment, a randomized-selection approach was used with a Cartesian coordinate system assigned to the wafer's surface. The surface of each wafer was separated into five parts and one gate was chosen randomly in each part. By using the random number function in an excel sheet, random coordinates were chosen, each of which represents a specific gate, Figure 2.2.

Capacitance vs. voltage (*C-V*) and capacitance vs. time (*C-T*) measurements were taken using an Agilent 4294a precision impedance analyzer and a temperature controlled probe station. The *C-V* measurements were taken by applying the bias to the substrate contact to avoid noise and achieve high precision measurements. Series *C-V* method (C_s-*V*) was used as it gave better results than parallel *C-V* (C_p-*V*). A KEITHLEY Model 82 C-V system instrument was also used for quasi-static measurement of interface trap density D_{it}.



(a) (b)

Figure 2.3: (a) Wafer with deposited Al gates. (b) Defined Cartesian coordinate system and four partitions plus a central region.

CHAPTER 3:

RESULTS AND DISCUSSION

3.1 X-Ray Diffraction Study to Check Sample Purity

X-Ray diffraction measurements were made with a PANalytical X'Pert PRO Materials Research Diffractometer and $CuK_{\alpha 1}$ radiation on two samples P300 and P1800 to evaluate the crystal uniformity and defect density. The reciprocal space maps in the vicinity of Si (004) reflection indicated no extended defects in the volume of the epitaxial layers for both samples in Figure 3.1. The omega rocking curves (RC) are shown in Figures 3.2 and 3.3. The main epilayer RCs (Figure 3.2) show FWHM = 5.4 arc.sec for P1800 and 6.4 arc.sec for P300 sample respectively (FWHM – Full Width at Half Maximum). Density of clusters of point defects are more or less homogeneously distributed in the volume of the main epi-layer and it increases from P1800 to P300 as expected, because longer purge time results in better quality epi-layer. Figure 3.3 shows the second (P1800 – 5.4 arc.sec) and third (P300 – 6.8 arc.sec) epilayer peaks, indicating no extended crystal defects. The XRD studies indicated very low level of defect density and uniform crystalline epi-layer indicating longer lifetime

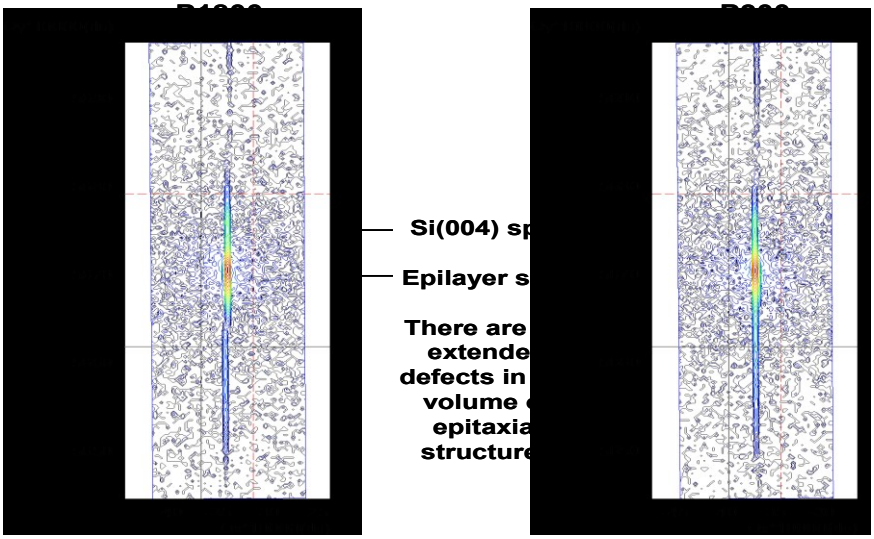


Figure 3.1: XRD - Reciprocal space maps in the vicinity of Si (004) reflection for P1800 and P300 samples.

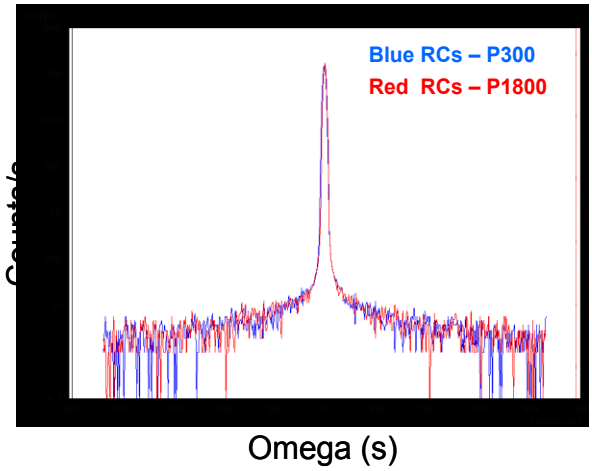


Figure 3.2: XRD – Omega Rocking Curves (RCs), reflection in the vicinity of Si (004) using $CuK_{\alpha 1}$ radiation for main epi-layer RCs $\Rightarrow$ homogeneous point defect density in epi, increases from P1800 to P300.

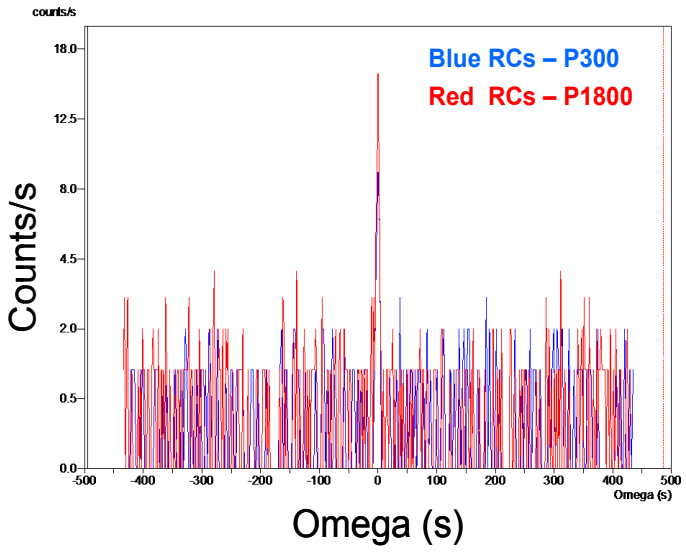


Figure 3.3: Omega Rocking Curves (RCs), reflection in the vicinity of Si(004) using $CuK_{\alpha 1}$ radiation. 2nd and 3rd epi-layer peaks $\Rightarrow$ No extended crystal defects.

3.2 Time-Resolved Photo Luminescence (TRPL)

Photoluminescence (PL) is an important contactless non-destructive optical method to measure purity, crystalline quality and identify certain impurities in semiconductors [2, 30]. It is easier to identify the type of impurity than its density using PL [31]. Radiative recombination is needed for PL measurement and it is more difficult for an indirect energy gap material like silicon than for direct energy gap semiconductors like GaAs, InP, *etc*. Time resolved photoluminescence is based on PL technique where an optical laser pulse is applied to the semiconductor and the decay in photoluminescence with time is measured to determine the minority carrier lifetime.

In the time-resolved PL measurement the sample is excited by a pulsed laser (667 nm, 100 Hz, 350 mW). The PL signal is detected by a Hamamatsu near infrared photo multiplier tube (PMT) and then analyzed by a photon counting multichannel scaler (SRS

430). Once the pulse is applied a large number of electron-hole pairs are generated in the semiconductor which would then decay with time due to recombination. The purer the material, the longer the carrier lifetime and PL decay time would be. The decay is governed by an effective lifetime, determined by bulk, surface and interface recombination [32]. The challenge in measuring the carrier lifetime in epi-layers is to confine the optically generated carriers within the epi-layer thickness; otherwise the carriers generated in the substrate will also impact the measurement and may mask the epi-lifetime and result in incorrect lifetime measurement.

Since the epi-layers are 4 μm thick, one needs a short wavelength light source, either a blue or a green laser (532 nm) for excitation. In our laboratories, such a blue or green laser is not available at this moment and instead a red laser (667 nm) was used. The absorbance of a 667 nm light source (vertically excited) in a 4 μm epi layer is 61.5% using the formula absorbance = $1\text{-}e^{\alpha t}$, where α is the absorption coefficient (= 2389 cm^{-1}) and t = epi layer thickness (4 μm). Hence, the substrate lifetime will affect the overall measurement as some of the carriers are generated in the substrate and recombine there. I carried out TRPL measurements for all four bare silicon samples (P300, P600, P1200, and P1800) as shown in Figure 3.4. The PL decay for all samples agree very well with each other and are similar whether the incident light pulse is on the front or the back of the samples. The 1/e point is taken as the lifetime which is around 100 ns. Since the epi-layer lifetime is expected to be much higher than this, the substrate carrier generation and recombination dominates the measurement. This lifetime is close to the Auger recombination lifetime for a 10^{20} cm^{-3} doped silicon substrate, which is the case for our

sample. As expected, PL measurements are not suitable for thin epi layers that are much thinner than the minority carrier diffusion length.

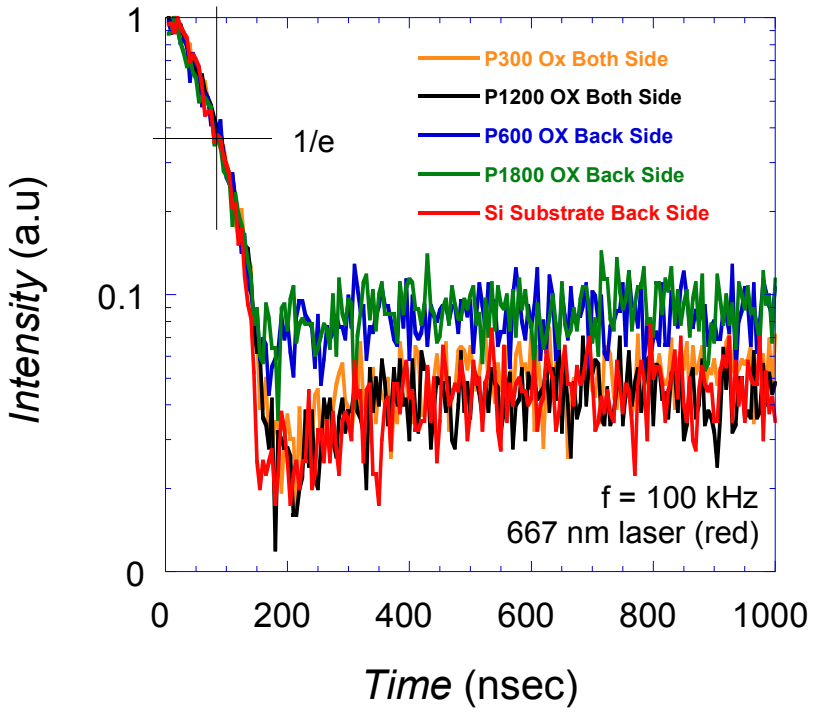


Figure 3.4: TRPL measurement of epitaxial silicon samples using a 667 nm (red) pulsed laser.

3.3 Quasi-Steady-State Photoconductance Decay Method

I have attempted to make recombination lifetime measurements using the quasi-steady-state photoconductance decay method [2]. In this technique the sample conductance is measured as a function of time following a long light pulse. During the light pulse decay the sample's conductance is continuously monitored giving the recombination lifetime as a function of excess carrier density. Since the epi-layer conductance is shunted by the heavily-doped, high-conductivity substrate, the conductivity change due to the optical

excitation is so low that it cannot be measured. This is similar to conventional photoconductance decay measurements, which also do not work for the same reason.

3.4 Classic Pulsed MOS Technique

The fundamentals of this technique were previously reviewed in section 1.6. For the p-type samples a voltage pulse from -5 V to +5 V was applied to the gate that drives the device from strong accumulation to deep depletion and then +5 V gate voltage was kept constant for a time period long enough for the device to enter strong inversion by thermal ehp generation. External excitation was avoided by doing the measurement in dark. As the device goes from deep-depletion to strong inversion with time, a gradual rise in the capacitance will be observed from its initial value (deep-depletion capacitance) to a saturation value at inversion, this time is called t_f (transition time).

In order to extract the generation lifetime from *C-t* curves in a fast way one can simplify equation 1-45 to equation 3-1 by assuming $\gamma \sim 3$ [23]. Such assumption is sound for clean wafers and when high precision in extracting lifetime is not required. I will initially use equation 3-1 for lifetime extraction and then extend the extraction method in subsequent sections.

$$\tau_{g\,eff} = \frac{n_i}{N_A} \times \frac{1}{1 + C_{ox}/C_i} t_f \qquad (3\text{-}1)$$

where N_A is the doping concentration, t_f the saturation time and C_{ox} and C_i are oxide and deep-depletion capacitances, respectively, whose values should be obtained from *C-t* curve. The theoretical values of C_{ox} and C_i , however, are [2]:

$$C_i = \frac{K_s \varepsilon_0 A}{W_{dd}} \tag{3-2}$$

where $K_s = 11.9$ is the silicon dielectric constant, ε_0 vacuum permittivity, A gate area, and W_{dd} is the scr width at t=0 whose theoretical value is:

$$W_{dd} = \frac{K_s t_{ox}}{K_{ox}} \left(\left(\sqrt{1 + \frac{2V_G}{V_0}} \right) - 1 \right) ; \; V_0 = \frac{q K_s \varepsilon_0 N_A}{(C_{ox}/A)^2} \tag{3-3}$$

where $K_{ox} = 3.9$ is oxide dielectric constant, t_{ox} is oxide thickness and V_G is the gate voltage.

3.4.1 Doping Concentration

As can be seen in both equations 1-45 and 3-1, precise knowledge of epitaxial layer doping concentration N_A is crucial for extracting generation lifetime. Consequently, the doping concentration profile was determined from the deep-depletion *C-V* curves using the relationships [2]

$$N_A = \frac{2}{q K_s \varepsilon_o A^2 d(1/C^2)/dV}; W = K_s \varepsilon_o A \left(\frac{1}{C} - \frac{1}{C_{ox}} \right) \tag{3-4}$$

where W is the scr width.

The *C-V* curves are shown in Figure 3.5. Since these MOS capacitors have extremely long recovery times when pulsed into deep depletion (times approaching 10,000 seconds), the deep-depletion *C-V* curves are little influenced by minority carrier generation during the *C-V* sweep time of approximately 60 s. For MOS capacitors with shorter recovery times, minority carrier generation during the *C-V* sweep distorts the

deep-depletion *C*-*V* curve and yields incorrect doping profiles. But, that is no of concern for these devices. The $1/C^2$-*V* curve in Figure 3.6 is quite linear over most of the voltage range, indicating very uniform doping concentration. At $W \approx 3.8$ μm, the epi layer approaches the heavily-doped substrate and the doping concentration starts to increase, as expected. Figure 3.7 shows the doping profile throughout the epitaxial layer. The doping concentration is uniform throughout the epitaxial layer which makes further interpretations easier than the case of non-uniform doping profile. The doping concentration is equal to $9.8 \times 10^{14} \mathrm{cm}^{-3}$. Since the samples are p-type boron doped, the measure doping concentration well follow the Hall measurements done by the vendor and the resistivity data I was provided with (30 ohm.cm).

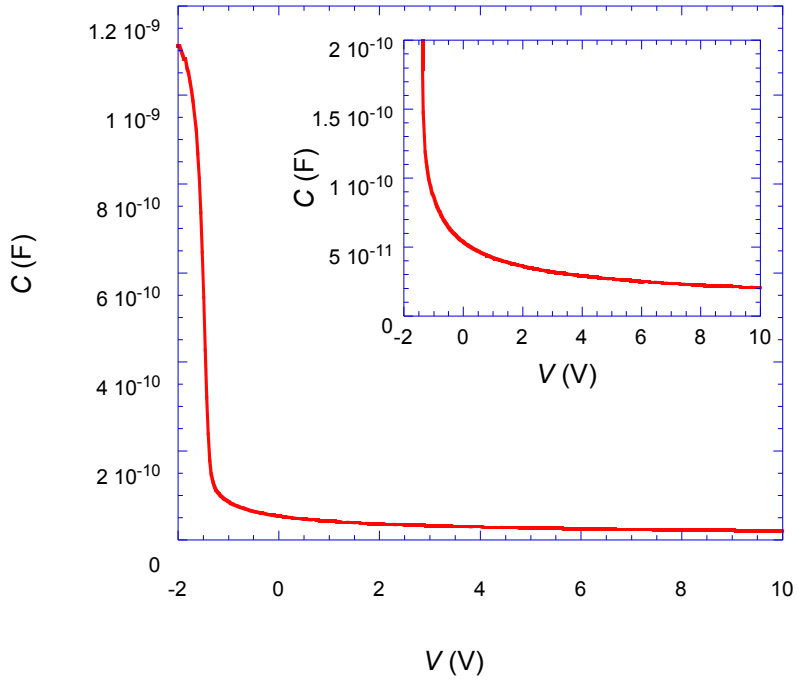


Figure 3.5: Deep-depletion *C*-*V* curves; the curve at the corner is an enlarged part of the depletion part of the main *C*-*V* curve.

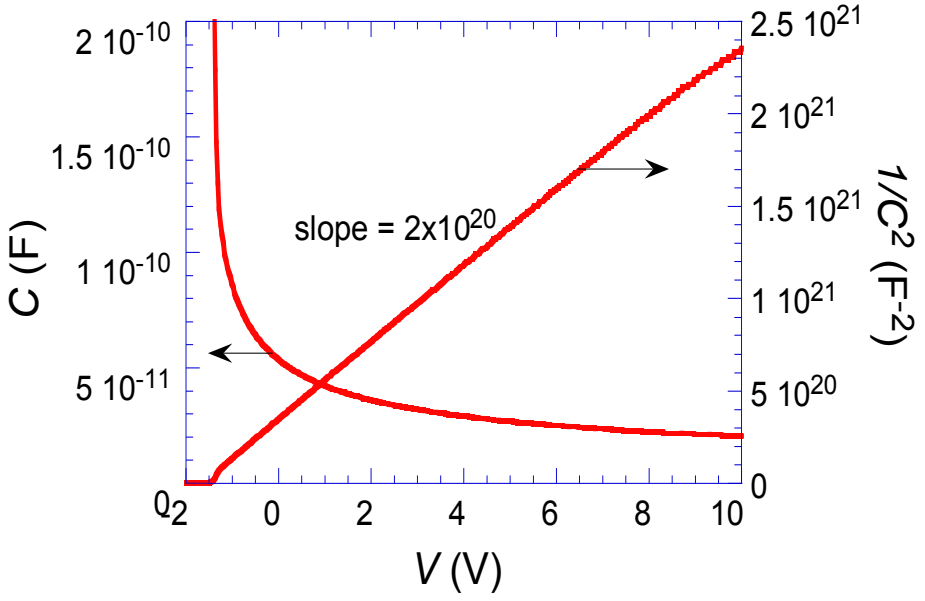


Figure 3.6: Deep-depletion *C*-*V* and $1/C^2$ –*V* curves.

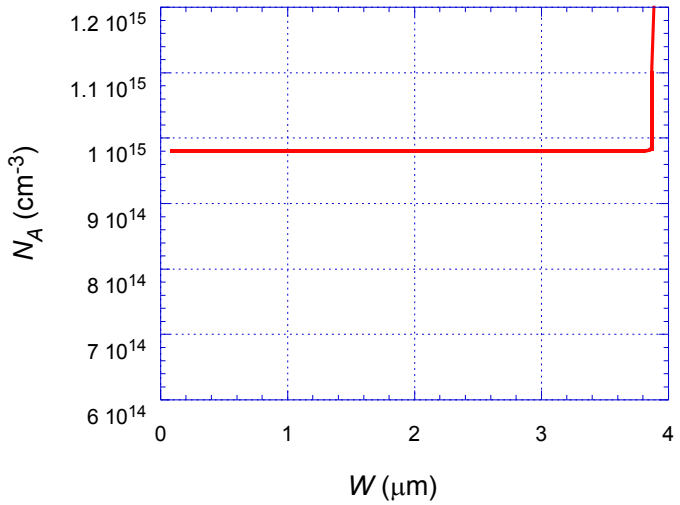


Figure 3.7: Doping profile calculated for the epitaxial layer. The doping concentration is uniform throughout the epitaxial layer and equal to 9.8×10^{14} cm^{-3}.

3.4.2 Measurements for Poly-Silicon Gate Samples

When measuring the generation lifetime of the poly-silicon gate samples using the pulsed MOS capacitor method I encountered unusual behavior with significant voltage shifts and low-frequency (LF) behavior in the inversion region using high-frequency (HF) probing frequencies, as shown in Figure 3.8. The *C-t* measurements showed unusual fast rise from deep-depletion to inversion, which is unexpected for these high-purity samples. One expects the transient time to be hundreds to thousands of seconds, not the short times in Figure 3.9. Capacitance vs. frequency measurements in accumulation showed a variation of capacitance with frequency in the HF region (1 kHz to 1 MHz), which is not expected. This is an indicative that poly-silicon gates have cause series resistance problem which distort [2] the measured capacitance data. Figures 3.8 through

3.10 show some of *C-V*, *C-t* and *C-f* measurements for the poly-silicon gate samples and their anomalies. These are a representative of a large number of measurements I did. Hence I could not use the poly-silicon gate samples for lifetime measurements through pulsed MOS capacitor technique.

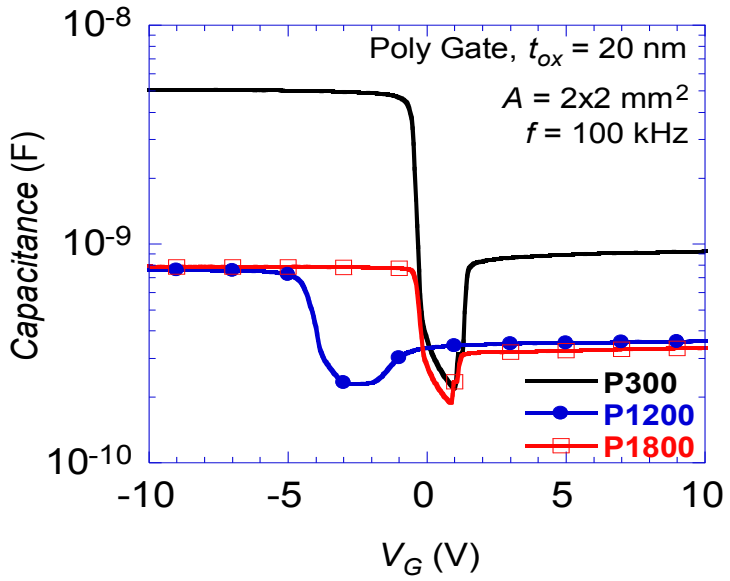


Figure 3.8: Poly-silicon gate samples' *C-V* curves show shifts and low frequency behavior at high probing frequency which is unexpected.

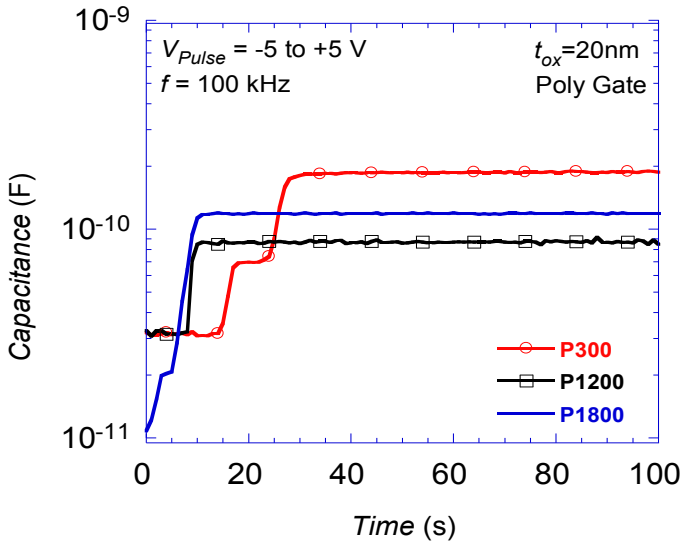


Figure 3.9: *C-t* curves for poly-silicon gate devices show very short saturation times and inconsistent inversion capacitances.

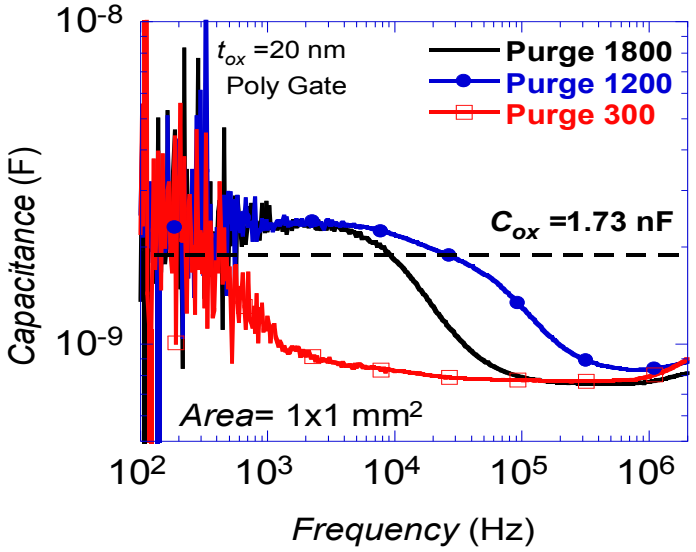


Figure 3.10: Capacitance vs. frequency curves for poly-silicon gate devices. C_{acc} changes with frequency which is indicative of series resistance problem.

3.4.3 Measurements for the Aluminum Gates for 1st Package Samples

The MOS capacitor measurements using the poly-silicon gate samples were inconclusive so I fabricated MOS capacitors with metal (aluminum) gates; the fabrication steps are described in chapter 2, respectively. The *C-V* and *C-f* shown in Figures 3.11 and 3.12 show no rise in the inversion capacitance at any positive gate bias, and the accumulation capacitance changes little with frequency. So these devices can be used for pulsed MOS-C measurements. For the *C-V* measurements the bias was applied to the substrate and for *C-t* the bias was applied to the top gate. During negative to positive voltage sweep direction the capacitance goes into deep depletion region due to the low minority carrier generation. For the positive to negative voltage sweep direction, on the other hand, the device starts at deep depletion but gradually goes into inversion with time as shown in Figure 3.11. The accumulation capacitance did not change much with frequency unlike the poly-silicon gate samples in the HF zone (1 kHz to 1 MHz) in Figure 3.12. The *C-V* plots of P600 and P1800 are almost identical indicating no impact of lifetime due to better quality of epi-layer for higher purge time (P1800). Figure 3.13 shows the comparative *C-t* behavior of two devices on P600 and P1800 wafers. These two devices have the longest lifetime in the respective wafer types for the current fabrication, P1800 sample shows slightly longer lifetime compared to P600 at 27.5ºC indicating better epi-layer with lower defect density as confirmed by XRD.

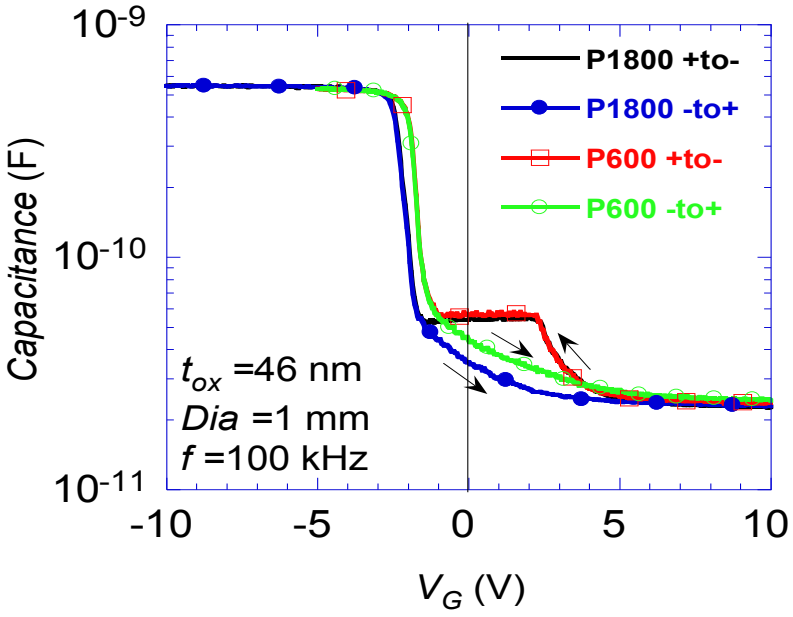


Figure 3.11: MOS Capacitor with Al gates' *C-V* curves: no rise in capacitance in inversion region and no other major abnormality.

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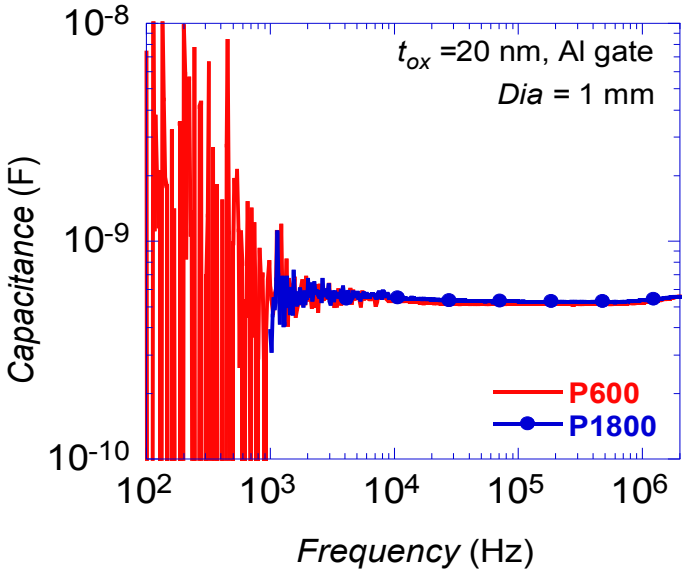

Figure 3.12: MOS Capacitor with Al gates Capacitance vs. Frequency curves: constant accumulation capacitance through most of the HF zone.

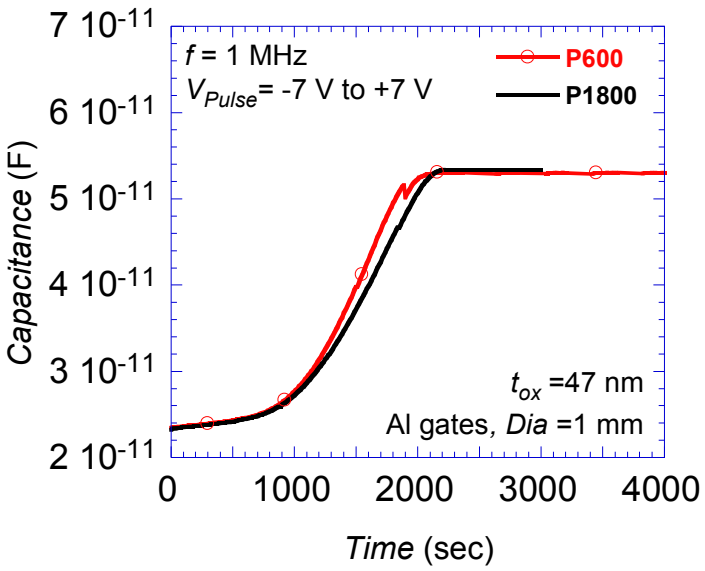

Figure 3.13: MOS Capacitors with Al gates *C-t* curves. Comparison between P1800 and P600 shows that P1800 has longer lifetime than P600 at 27.5 ºC.

I extracted the generation lifetime form the transient time through the equation 3-1. The generation lifetime ($\tau_{g\ eff}$) is calculated from the saturation time with C_{ox} = 536 pF and C_i = 23.1 pF for P600 and C_{ox} = 524 pF and C_i = 23.1 pF for P1800. The measured generation lifetime is an effective lifetime given by equation 1-40. Assuming s_0 = 10 cm/s, a reasonable value for the SiO_2/Si interface and r = 0.05 cm, I get

$$\tau_{geff} = \frac{\tau_g}{1 + 400\tau_g} \Rightarrow \tau_g = 10 \text{ ms for } \tau_{geff} = 2 \text{ ms} \qquad (3\text{-}5)$$

10 ms is a very respectable value for high quality Si wafers/epi layers. However, for industrial application making such assumption on the surface generation velocity value may not be precise and more accurate study of lifetime parameters is required. Moreover,

it is necessary to find a correlation between the lifetime to impurity concentration in the epitaxial layer – as desired by industry.

3.4.4 Measurement for 2nd package wafers

Up to this point the mentioned measurements had the sole purpose of extracting generation lifetime. It is showed that optical measurements such as time-resolved photoluminescence and quasi-static photoconductance decay are not suitable for measuring lifetime in epitaxial layers. Moreover, It is showed that poly-silicon gate MOS-C devices are not suitable for generation lifetime measurements due to series resistance introduced by poly-silicon gates. However, metal gates MOS-C devices has been shown to be suitable test structures for extraction of lifetime parameters through *C-t* measurements.

The second package of wafers, as previously mentioned in chapter 2, has already deposited 20 nm thermal oxide on top. Since the oxide is deposited with industrial quality it should have better interface quality than the deposited oxide at our facilities. Furthermore, since the oxide for second samples is thinner that the first samples, the saturation time in *C-t* curves should be longer due to larger C_{ox} and in accordance with equation 3-1. This makes lifetime extractions easier. We have been also provided with DLTS measurement data about the metallic impurity density in these wafers. Now it can be investigated if it is possible to correlate the lifetime measurement data with impurity concentration in samples. One set of samples has Tungsten impurity concentration of less

that 10^{10} cm^{-3} – referred to as less-contaminated wafers – while the other set has 3×10^{10} cm^{-3} – referred to as more-contaminated wafers.

I fabricated Al gates MOS-C devices on these wafers, as mentioned in chapter 2, and performed classic pulsed MOS-C measurements on them. Before starting the *C-t* measurements, we made *C-V* measurements to determine the oxide capacitance C_{ox} and the flatband voltage V_{FB}. A typical *C-V* curve is shown in Figure 3.14. The oxide capacitance was in good agreement with theoretical calculated C_{ox} =1.35x10^{-9} F for a gate area of 7.85×10^{-3}cm^2 and the oxide thickness of 20 nm. The flatband voltage is ~ 0.1 V. The *C-t* measurements were made by applying a gate voltage pulse from accumulation (-5 V) to inversion (+5 V) at probing frequency of f =100 kHz and measuring the capacitance as a function of time. Many of the *C-t* measurements were made at elevated temperatures to reduce the recovery time. The MOS capacitor time of 10,000 s is the limit of the HP4294a unit we use for these measurements. At temperatures of 60-80 °C quasi-neutral region generation mechanism starts to dominate. Hence, we kept the temperature in 40-50°C range [23], but some measurements were made at temperatures as high as 100°C. One key element in the extraction of generation lifetime is the value of intrinsic carrier density n_i which is very sensitive to temperature. For calculation n_i in respect to time we use [33]

$$n_i = 9.38 \times 10^{19} (T/300)^2 \exp(-6884/T) \qquad (3\text{-}6)$$

with T in Kelvin.

C-t curves for different temperatures are shown in Figure 3.15. The room-temperature curve exhibits classical deep-depletion MOS capacitance-time behavior with recovery time of about 6500 s. Other devices showed recovery times as high as 10,000 s. As the

temperature is raised, the recovery time decreases substantially to about 50 s at 100 °C. The recovery time decrease, according to equation 3-1, is due to the increase in n_i with temperature. The qnr bulk generation starts to dominate over scr generation at temperatures of around 70-80 °C. Space-charge region generation is governed by generation lifetime in the scr width and quasi-neutral region generation by recombination lifetime or diffusion length.

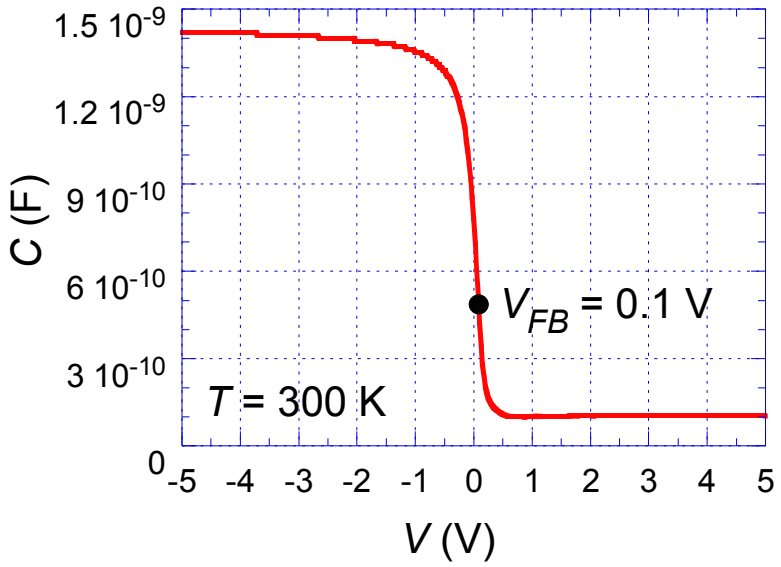

Figure 3.14: A typical measured *C-V* curve for second package wafers. The sweep direction in from positive to negative and hence no deep depletion is present.

Tables 3.1 and 3.2 include measurements data on two wafers. Equation 3-1 was utilized for extraction of generation lifetime. It is obvious that there is a fairly large spread in the generation lifetime values. This may be due to local variations in defect density, interface trap generation parameters, *etc*.

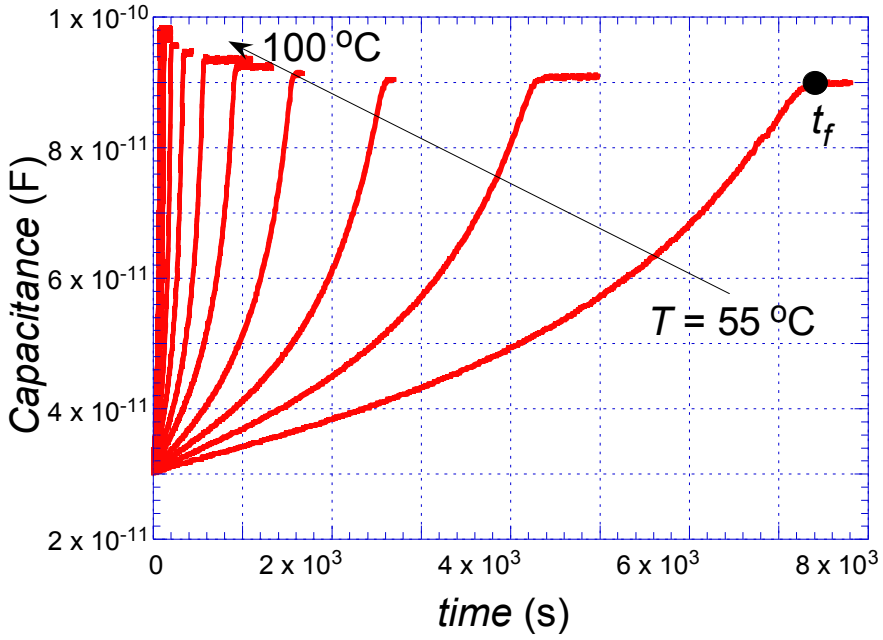

Figure 3.15: Deep depletion *C-t* curves for T =55-100 ºC. Device is pulsed from -5 V to +5 V. C_{ox} =1.35×10^{-9} pF, N_A =9.8×10^{14} cm^{-3}, t =20 nm. t_f denotes the saturation time when device reaches equilibrium.

Table 3.1: Less-contaminated wafer's extracted generation lifetime

Device #	t_f (s)	T (°C)	τ_g (ms)
1	1935	27	0.44
2	1625	27	0.37
3	593	27	0.136
4	1268	27	0.29
5	4224	27	0.96
6	2090	27	0.48
7	987.5	47.5	1
8	6125	46.2	5.6
9	9237.5	50	12.6
10	6450	27	1.47
11	8050	44	7.59

Table 3.2: More-contaminated wafer's extracted generation lifetime.

Device #	t_f (s)	T (°C)	τ_g (ms)
1	3800	27	0.8
2	5500	57	11.6
3	3150	55	5.3
4	275	50	0.31
5	5250	56	9.2
6	6025	56	10.7
7	635	50	0.83
8	2850	50	3.37
9	2200	50	2.6
10	8450	50	10.2
11	5900	50	7.4

One of the approaches to compare these data sets is to use the pooled two sample *t*-test [34]. In this pooled *t*-test we are statistically investigating the hypothesis of equal mean lifetime as the response variable for the "wafer type" as factor in two levels of "less-contaminated" and "more-contaminated". What we have measured is a sample of all the population of devices fabricated on each wafer. Based on the measured data from this sample we can draw statistical conclusion about the entire population of devices leading to a valid comparison of both wafer's mean lifetime. In this regard, the JMP statistical software package [35] was used to analyze the data.

Below is the JMP software output for current *t*-test experiment. Figure 3.16 shows the dot diagram of response variable vs. factor level which is the wafer type. This diagram gives a quick insight of the dispersion and central tendency of the measured lifetime for two wafers and can be used for subjective checking of some statistical assumptions such as equal variances. It also includes a schematic presentation of box plots in form of triangles where green lines specify 25, 50 and 75 percentile points for each factor level's data. Referring to such diagrams will only provide a subjective review of the data while for an objective discussion we refer to Figure 3.17 which is the pooled t-test output from JMP software. It reports 2.85 as the difference in average measured lifetime on both wafers and 1.789 as the standard error of the difference in calculated averages for each factor level. Utilizing those values, JMP has calculated the value of t_0 statistic (*t*-ratio) for this test which is 1.59. The general way to calculate the t_0 statistic is:

$$t_0 = \frac{factor\ level\ 1\ data\ average - factor\ level\ 2\ data\ average}{Standard\ error\ of\ differences\ in\ averages} \qquad (3\text{-}7)$$

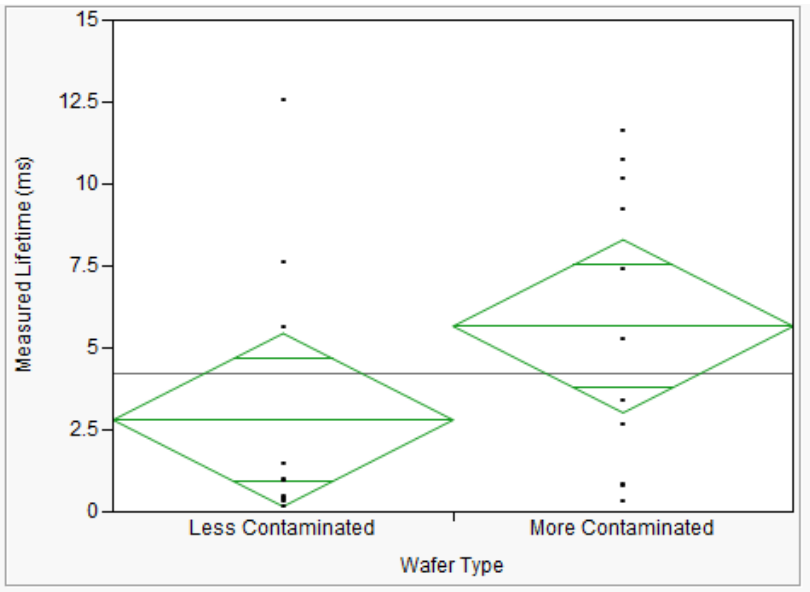

Figure 3.16: JMP - dot diagram of response variable (lifetime) vs. factor level (wafer type).

Since there are 11 replicates, the Degree of Freedom for this experiment is 20. JMP has also drawn the reference t_{20} distribution diagram and has compared the value of calculated t_0 from sample data to the upper and lower $\alpha/2$ percentile points of this distribution. In a pooled *t*-test, if the absolute value of t_0 is higher than $\alpha/2$ percentile point of the reference distribution then the hypothesis of equal means would be rejected or in other words the data are significant. The minimum value of α at which the data are significant is called the *P*-value which is indicated in JMP output as Prob > |*t*| with the value of 0.1257. Since the reported *P*-value for this experiment is large, it indicates that the hypothesis of equal mean lifetime on both wafer types is true for any significance level lower than reported *P*-value such as 0.05 – a reasonable value for most industrial

conclusions. Such significance level indicates that the probability of being wrong while rejecting this hypothesis is only 5%.

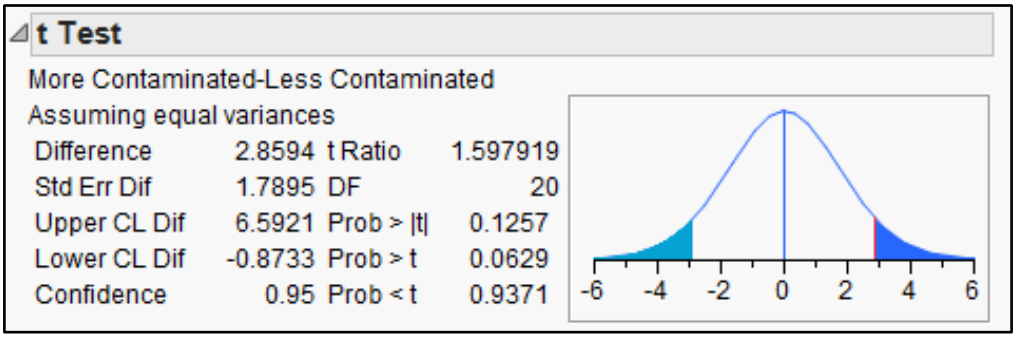

Figure 3.17: JMP software output for the t-test on lifetime comparison on two more- and less-contaminated wafers.

Figure 3.17 also includes the JMP reported 95% confidence interval of the difference between mean lifetime of more contaminated and less contaminated wafers which is (-0.8733, 6.5921). This range can be interpreted as if any two random gates are chosen on more-contaminated and less-contaminated wafers, the difference between the measured lifetime, with 95% of confidence, would be between -0.8733 and 6.5921 ms. It is interesting to notice that since the hypothesis of equal mean lifetime has been approved, the value "0" can be seen in this difference interval.

According the above discussion, we cannot declare these two samples having different generation lifetime by using the classic pulsed MOS-approach and using equation 3-1 for extraction of lifetime.

3.5 Modified Pulsed MOS-C Techniqu

3.5.1 More Accurate Lifetime Extraction Method from *C-t* Curves

Up to this point we used the simplified equation 3-1 to extract generation lifetime. Although this equation is a fast approach, it does not give any information about the surface generation velocity and ignores critical properties of the *C-t* diagram such as its curvature. A more comprehensive way to extract lifetime parameters from *C-t* diagrams is to use the method of least squares to fit equation 1-44 to the experimental data and extracting $\tau_{g\,eff}$ and s' , respectively. We observed that a good fit of this equation to experimental data can be obtained at temperatures slightly higher than room temperature, as showed in Figure 3.16.

However at room temperature, due to erratic variations of s and s' – that is characterized by an abrupt change in curvature of the *C-t* curve – a good fit of equation 2 could not be obtained. This change of curvature in C-t curves has been shown in Figure 3.17.

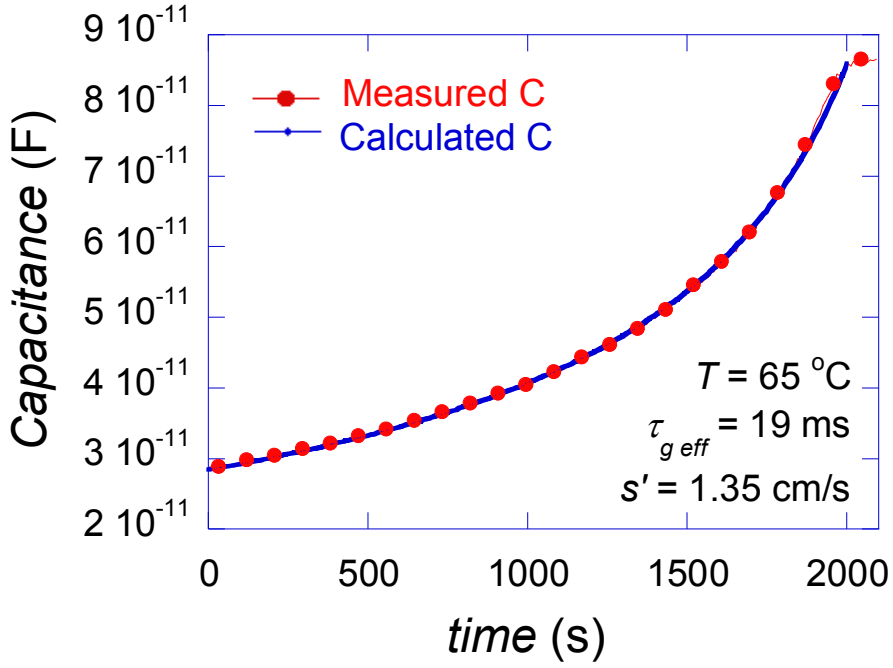

Figure 3.18: Experimental and calculated *C-t* curve for T =65 ºC where the Device is pulsed from -5 V to +5 V. C_{ox} =1.35×10^{-9} pF, N_A =9.8×10^{14} cm^{-3}, t =20 nm.

One way to deal with this problem is to use the famous Zerbst method for extracting $\tau_{g\,eff}$ and *s'* from *C-t* curves [36]. Zerbst has proposed the following equation which is known as Zerbs equation:

$$-\frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2 = \frac{2n_i}{\tau_{g\,eff}N_A}\frac{C_{ox}}{C_f}\left(\frac{C_f}{C}-1\right)+\frac{2n_i C_{ox}s'}{K_s\varepsilon_0 N_A} \qquad (3\text{-}8)$$

Using the data from C-t measurements, the Zerbst plot which is a plot of $-(d/dt)(C_{ox}/C)^2$ vs. $(C_f/C-1)$ can be obtained. The linear portion of this graph has a slope which is inversely proportional to $\tau_{g\,eff}$ and has an intercept of *s'*, as shown in figure 3.18. The inherent problem of Zerbst method is the data differentiation, which

becomes a severe problem in C-t curves which has long saturation time. Differentiation will magnify the mico-noises that are present in the measure data and hence makes finding the linear portion rather subjective and cumbersome. This problem becomes out of control when we increase the temperature. Small variations of temperature in range of ±0.05 ºC will introduce considerable amount of noise in the measured capacitance and hence the resulted Zerbst plot would not be usable at all. This problem has been shown in Figure 3.19. Other limitations of the Zerbst technique have been noticed in literature [37] such as the linear portion becoming small at low gate voltages. Since we are specifically interested in extracting lifetime parameters at elevated temperatures, we prefer to fit equation 1-45 to experimental data rather than using Zerbst method.

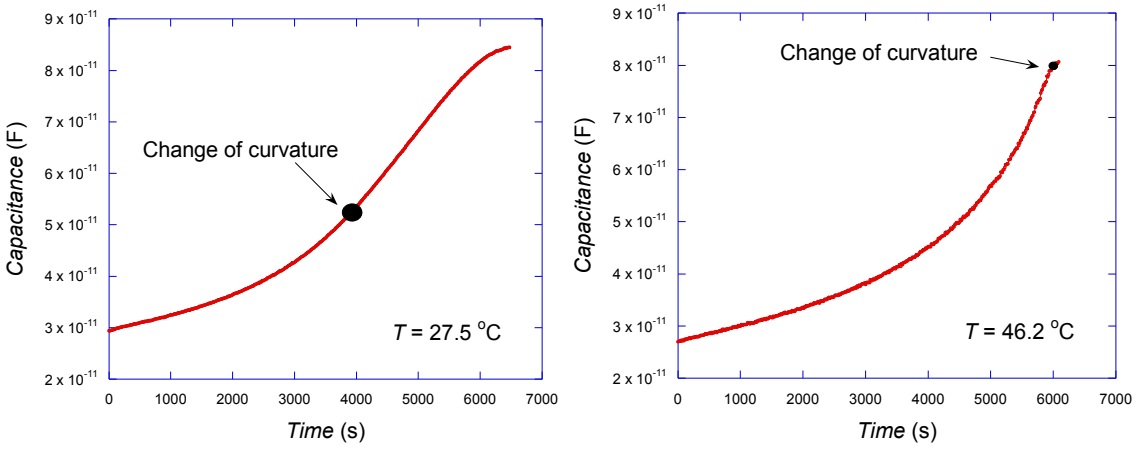

Figure 3.19: Left: *C-t* curve at room temperature shows a change of curvature in middle part. Right: *C-t* curve at slightly above room temperature has no sign of change of curvature in middle parts. Change of curvature happens in a non-sensitive region.

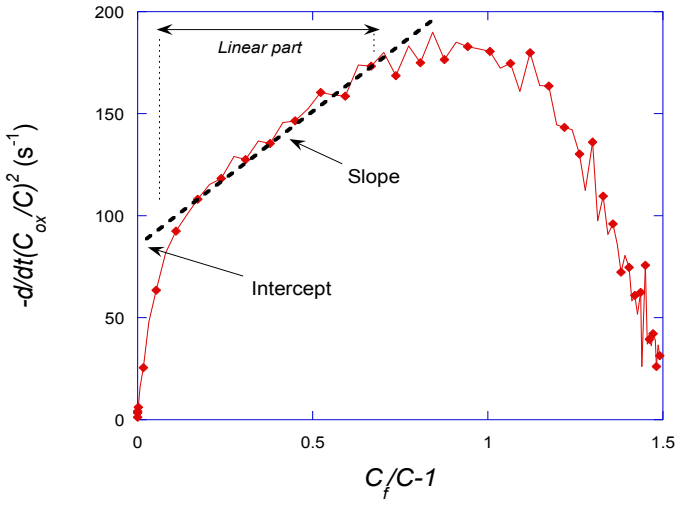

Figure 3.20: A typical Zerbst plot for 1st package wafers where the saturation time and so the amount of noise is low.

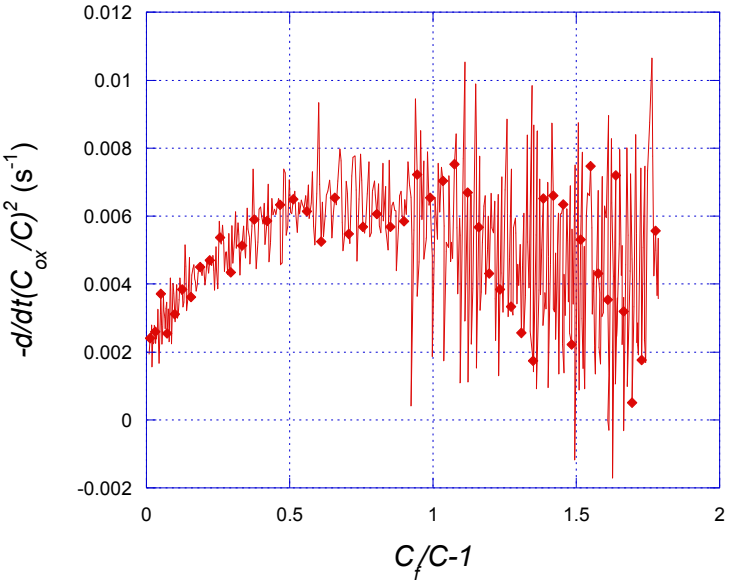

Figure 3.21: Zerbst plot showing considerable amount of noise. The plot is for 2nd package wafers where saturation time is thousands of seconds and the noise on data is considerable. The noise becomes even worst when temperature is increased.

3.5.2 Domination of Surface Generation

As discussed previously in section 1.6, according to equation 3-9, $\tau_{g\,eff}$ is an effective parameter whose measured value is always lower than τ_g due to the term s_0. The critical point here is that the amount of the reduction in $\tau_{g\,eff}$ under the influence of s_0 depends on the magnitude of τ_g. Figure 3.20 shows four different plots of $\tau_{g\,eff}$ for τ_g = 0.1, 1, 3 and 10 ms as s_0 increases over a plausible range.

$$\tau_{g\,eff} = \frac{\tau_g}{1 + 2s_0\tau_g\,/r} \tag{3-9}$$

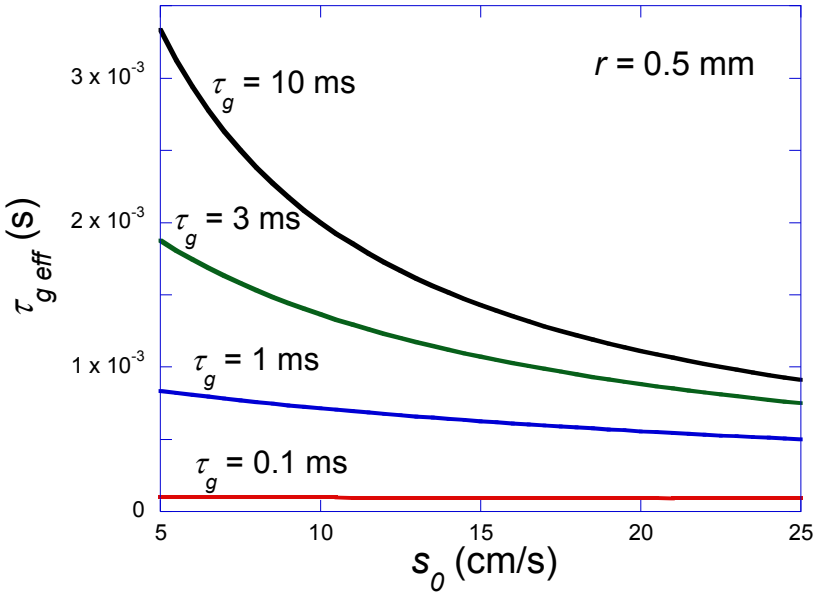

Figure 3.22: Variation of $\tau_{g\,eff}$ with s_0 for constant values of τ_g. At higher values of τ_g there is more decrease in $\tau_{g\,eff}$ while s_0 increases.

It can be easily seen that for high values of τ_g the decrease in $\tau_{g\,eff}$ due to s_0 is far greater than for low values of τ_g. This concept plays an important role in the interpretation of effective generation lifetime $\tau_{g\,eff}$ extracted from *C-t* diagrams for ultraclean wafers where the τ_g value is considerably large and in order of 10-50 ms. The classic study of transient *C-t* response of pulsed MOS-C ignores to separate the components of $\tau_{g\,eff}$ and assumes that it is reflecting the generation lifetime in the epitaxial layer τ_g. Such assumption is only sound for traditional wafers where the generation lifetime is low enough for the $\tau_{g\,eff}$ not to be affected in the presence of s_0. However, while dealing with ultra clean wafers, due to the high value of τ_g, the $\tau_{g\,eff}$ term is most likely dominated by the surface generation and it should not be referred to unless its components are suitably separated. Figure 3.21 is another presentation of how effective lifetime becomes dominated by s_0 as τ_g increases.

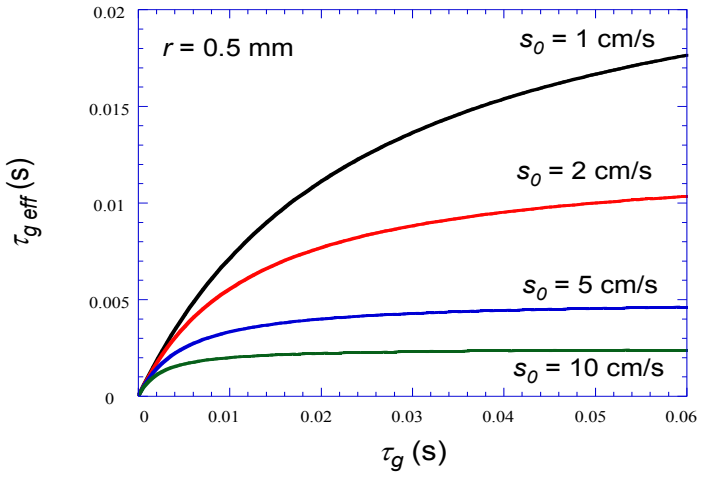

Figure 3.23: Variation of $\tau_{g\,eff}$ with τ_g for constant values of s_0. At higher values of s_0 the $\tau_{g\,eff}$ shortly ceases to reflect τ_g.

3.5.3 Separating Surface and Bulk Components of $\tau_{g\,eff}$

According to the above discussion on the role of the surface generation in masking scr generation in the measured effective lifetime data, it is necessary to modify the pulsed MOS-C technique in order to separate the surface and bulk generation components of the $\tau_{g\,eff}$ parameter when extracted from *C-t* diagrams. As mentioned in section 1.6 and according to equation 3-10, s' is a linear combination of a temperature-dependent "$n_i D_n / N_A L_{n\,eff}$" term and a temperature-independent "s" term.

$$s' = s + (n_i D_n / N_A L_{n\,eff}) \tag{3-10}$$

At low temperatures, since the term $n_i D_n / N_A L_{n\,eff}$ is negligible compared to *s*, to the first approximation we can assume that $s' = s$. As we increase the temperature, the diffusion term $n_i D_n / N_A L_{n\,eff}$ starts to increase due to the n_i^2 term until it dominates *s,* and s' reaches a saturation value from which $n_i D_n / N_A L_{n\,eff}$ and the effective diffusion length $L_{n\,eff}$ can be extracted, respectively. Hence, *s*'(*T*) - *s*'(low *T*) values that are extracted from *C-t* curves measured at different temperatures (Figure 3.15), can be used to determine $L_{n\,eff}$. Figures 3.22 and 3.23 showsthe effective diffusion length versus temperature using D_n = 30 cm^2/s [38]. The saturation values of 60 µm and 120 µm are the true effective diffusion length which take into account diffusion length in the epitaxial quasi neutral region and the heavily-doped substrate as well as s_1 and s_b. Using the measured $L_{n\,eff}$, the value of $n_i D_n / N_A L_{n\,eff}$ can be now calculated at any temperature for that individual device. By measuring the *s'* from a low temperature *C-t* diagram,

according to equation 3-10, and subtracting calculated $n_i D_n / N_A L_{n\,eff}$ value for that temperature from it, the value of *s* can be then extracted.

Although so far *s* has been obtained, care should be taken that the surface component of $\tau_{g\,eff}$ is s_0 which is always larger than *s*. The calculated *s* is an empirical average value between 0 and s_0 which provides the best fit to the experimental data. One way to deal with this problem and to relate *s* to s_0 with good accuracy is to focus on the initial portion of the *C-t* diagram where the surface is still partially depleted and so that value of *s* is fairly close to that of s_0 – *i.e.* at first 30% of measured data. The method of least squares can be utilized to fit equation 1-45 to this portion of the *C-t* curve and extract the respective s' value – which we will refer to as s_i in this context. By having the previously calculated $n_i D_n / N_A L_{n\,eff}$, the approximate value of s_0 can be obtain from the measured s_i. Now with s_0 and $\tau_{g\,eff}$ in hand, using equation 3-9, we can easily calculate τ_g.

It worth noting that when dealing with sufficiently clean enough wafers (of which we can heat to temperatures where the temperature-dependent term becomes dominant), it is unnecessary to do the intermediate temperature *C-t* measurements. The minimum number of two *C-t* curves at lower and higher bound temperatures would suffice for the purpose of the $L_{n\,eff}$ calculation.

Figures 3.22 and 3.23 show the data measured for two devices on less and more contaminated wafers. Respectively the effective diffusion length has been shown to be 60 microns for less-contaminated and 120 microns for more-contaminated wafer. Following

the modified *C-t* measurement calculations mentioned above we obtained lifetime parameters are shown in table 3.3.

Table 3.3: Extracted lifetime parameters for two devices on more- and less-contaminated samples.

Wafer:	$\tau_{g-eff}\,(s)$	$S'(cm/s)$	$L_{n-eff}\,(cm)$	$S_i\,(cm/s)$	$S_0(cm/s)$	$\tau_g\,(s)$
More-contaminated	0.0141	0.501	0.012	1.094	0.755	**0.024**
Less-contaminated	0.0160	1.066	0.006	1.630	1.009	**0.045**

In this typical example, the new calculated τ_g is now following the expectations about these two devices, while the measured values of $\tau_{g\,eff}$ are fairly similar to each other. Taking into consideration equation 1-33 the τ_g value must be inversely proportional to N_T *i.e.* an increase of N_T by a factor of three would lead to a decrease in τ_g to 30%. According to the DLTS data we have been provided with, we should then expect for the two wafers to differ in their τ_g by approximately a factor of 3 which is roughly confirmed by the new measurement technique whereas the classic method revealed no difference.

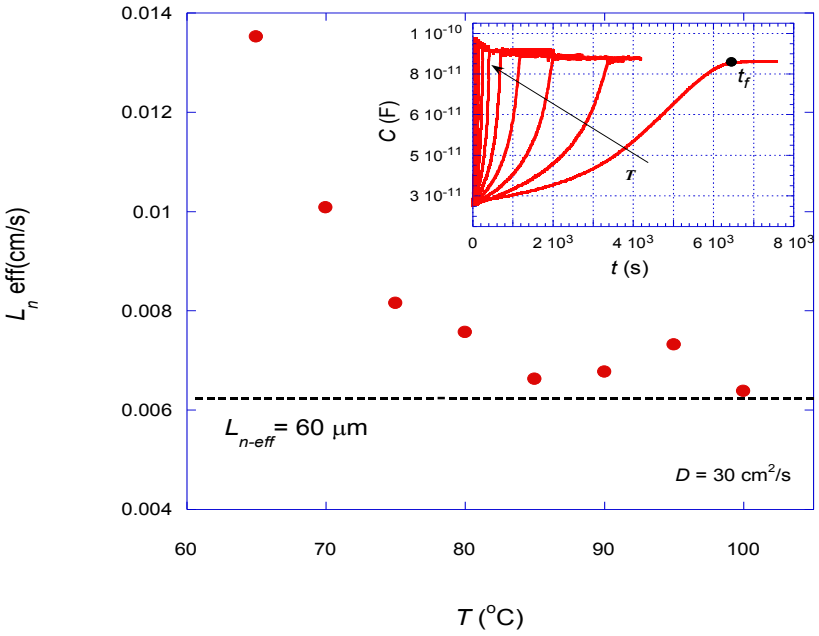

Figure 3.24: Plot of $L_{n\,eff}$ vs T from $S'(T) - S'(low\ T)$ showing a saturation value of $L_{n\,eff}$ which is the true $L_{n\,eff}$. Corner: Measured C-t for different temperatures – Less contaminated wafer.

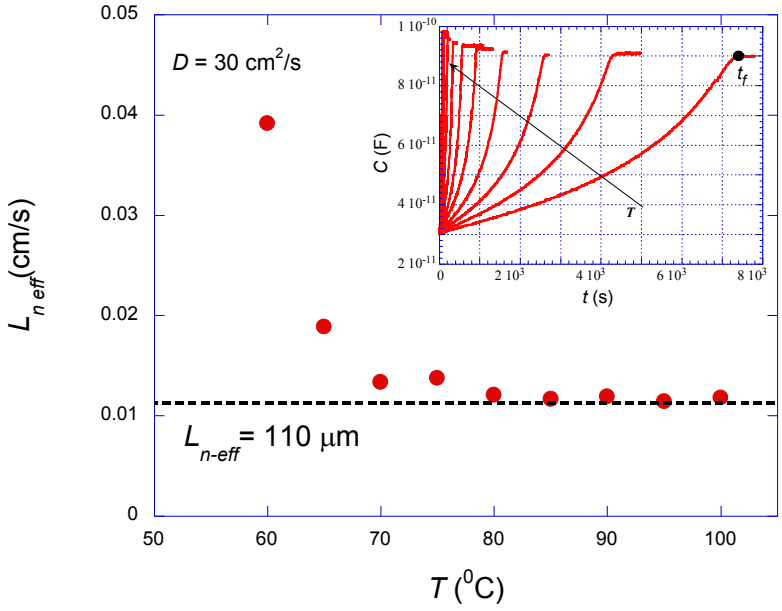

Figure 3.25: Plot of $L_{n\,eff}$ vs T from $S'(T) - S'(low\ T)$ showing a saturation value of $L_{n\,eff}$ which is the true $L_{n\,eff}$. Corner: Measured C-t for different temperatures – More-contaminated wafer.

3.5.4 A Statistically Designed Experiment with Modified Pulsed MOS-C Technique

In order to see if the proposed method can fully distinguish the difference in impurity concentration of the two more- and less- contaminated wafers a two-sample t-test comparison experiment was performed on these two wafers using the following test statistic [34]:

$$t_0 = \overline{\tau}_{g\,1} - \overline{\tau}_{g\,2} \Big/ \sqrt{S_1{}^2/n_1 + S_2{}^2/n_2} \tag{3-11}$$

$$\vartheta = \frac{(S_1{}^2/n_1 + S_2{}^2/n_2)^2}{\frac{(S_1{}^2/n_1)^2}{n_1 - 1} + \frac{(S_2{}^2/n_2)^2}{n_2 - 1}} \tag{3-12}$$

where *S* represents the standard deviation of measured data, *n* number of measurements on each wafer, and ϑ the degree of freedom for the experiment assuming unequal variances. The JMP software package [35] was used for exact analysis of data. Each run of the experiment was comprised of doing two *C-t* measurements on one individual device at temperatures of 58 °C and 90 °C respectively and the experiment was replicated 5 times in randomized order. The choice of these temperatures was based on several factors: first, the lower bound temperature was chosen slightly higher than the room temperature so that equation 1-45 can be effectively used for extraction of lifetime parameters. Moreover, this temperature was chosen low enough to be in the region where the surface term *s* is dominant over $n_i D_n / N_A L_{n-eff}$ in equation 3-10. The higher bound temperature on the other hand, was chosen high enough to be completely in the region where diffusion term $n_i D_n / N_A L_{n-eff}$ is dominated over the surface term. Table 3.4 contains lifetime parameters for two wafers.

Analyzing these data with classic pulsed MOS-C approach and taking into account $\tau_{g\,eff}$ which is obtained from measurements done at 58 ºC as response variable would lead to an ambiguous conclusion. The test statistic t_0 is 1.18 which has a *P*-value of 0.28. Hence, the null hypothesis of mean $\tau_{g\,eff}$ of these two wafers being different is insignificant. In other words, this t-test cannot declare the mean effective lifetime to be different at 10% significance level (α) for these two wafers. Moreover, as illustrated in Figure 3.25, the standard deviations of measured $\tau_{g\,eff}$ for two wafers are unequal which leaves doubt about the results being under influence of generation lifetime τ_g . Since the experiment was ran in a complete randomized order we expect the signal-to-noise ratio in

results to be due to nuisance factors in the experiment and hence the variance to be equal for both samples.

Table 3.4: Measured lifetime parameters on more- and less-contaminated wafers.

Wafer	run	$\tau_{g\,eff}(ms)$	$S'(cm/s)$	$L_{n\,eff}(cm)$	$S_i(cm/s)$	$S_0(cm/s)$	$\tau_g\,(s)$
Less-contaminated	1	12.3	1.78	0.003	2.6	1.56	53.8
Less-contaminated	2	9.4	3.54	0.002	3.57	2.01	38.6
Less-contaminated	3	18.1	0.63	0.008	1.24	0.83	45.1
Less-contaminated	4	11.2	1.08	0.005	2.06	1.43	31.5
Less-contaminated	5	22.5	0.55	0.01	1.05	0.72	64.5
More-contaminated	6	11.7	0.58	0.009	1.58	1.21	27
More-contaminated	7	15.7	0.67	0.016	1.14	0.93	38
More-contaminated	8	10.9	0.79	0.013	2.03	1.78	49
More-contaminated	9	10.1	0.46	0.01	1.56	1.22	19.9
More-contaminated	10	9.3	0.82	0.006	2.1	1.58	22.6

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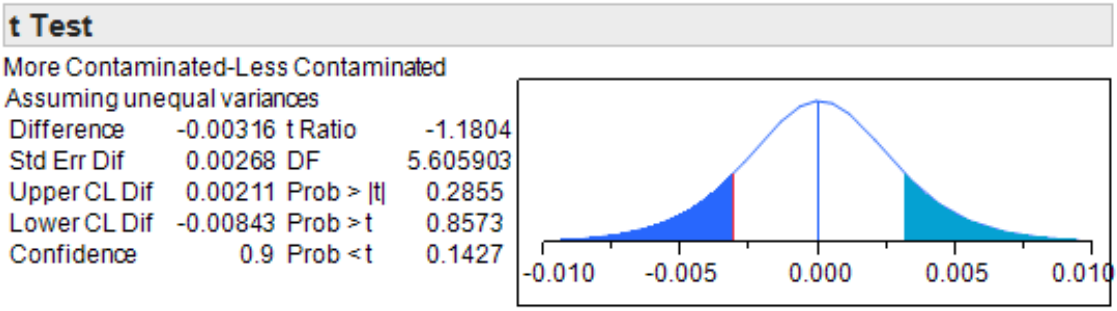

Figure 3.26: JMP software output for the t-test comparison of the mean effective generation lifetime for both less and more contaminated wafers

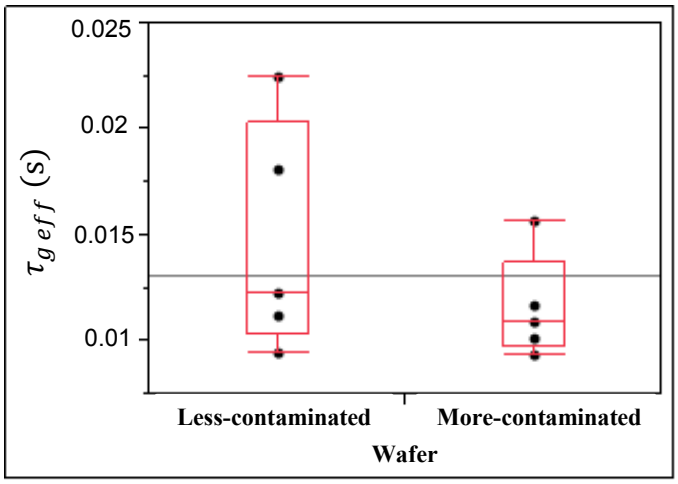

Figure 3.27: Box plots and dot diagrams of measured $\tau_{g\,eff}$ for two more- and less-contaminated wafers, plotted by JMP software. Unequal standard deviation of measured $\tau_{g\,eff}$ for two samples is obvious.

However, if we take into account the *C-t* curves measured at 90 °C and follow the modified pulsed MOS-C theory, we can extract additional lifetime parameters for two

samples: $L_{n\,eff}$, s_0, and τ_g. Now, constructing a new t-test by taking τ_g as the response variable would result in a promising conclusion. The t-test on the hypothesis of equal mean τ_g on two wafers has a test statistic t_0 of 1.97, with a *P*-value of 0.087. Based on this test we can declare that the mean generation lifetime of less-contaminated wafer is longer than more-contaminated wafer with a risk level of only 5%. Since, according to equation 1-45, τ_g is a direct measure of deep-level impurity density in the epitaxial layer, this is a valuable conclusion which shows that the proposed method can successfully distinguish the difference in impurity densities as low as 10^{10} cm^{-3}. Furthermore, as showed in Figure 3.27, the inequality of standard deviation in measured data is no longer visible when τ_g is used instead of $\tau_{g\,eff}$ as response variable.

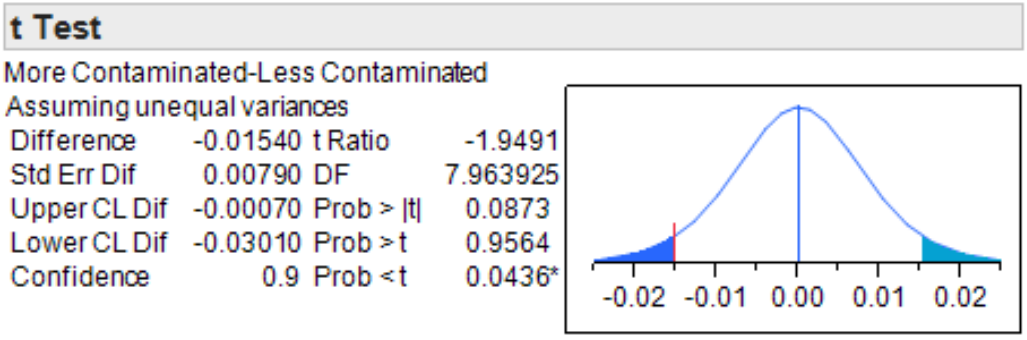

Figure 3.28: JMP software output for the t-test comparison of the generation lifetime calculated through modified *C-t* method for both less and more contaminated wafers.

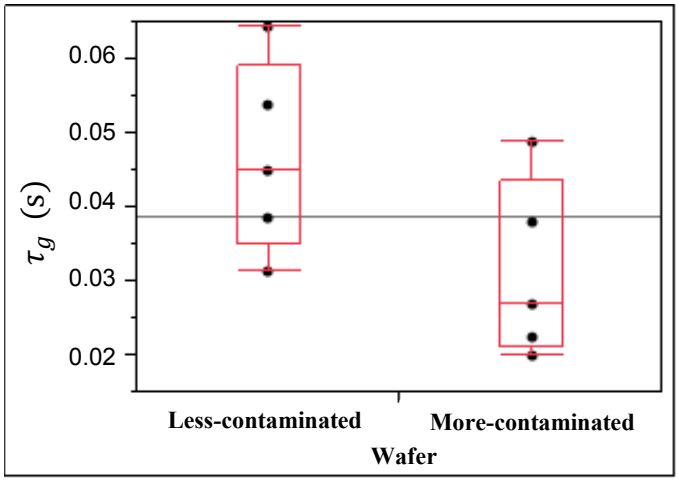

Figure 3.29: Box plots and dot diagrams of measured τ_g for two more- and less-contaminated wafers, plotted by JMP software. Two samples show equal standard deviations in measured τ_g.

3.6. Oxide/Si interface study

Although it is difficult to independently measure s_0, there are various techniques which can measure interface trap density D_{it} which is related to surface generation velocity through equation 3-13 [23].

$$s_0 = {}^{\pi}/_{2} \times (c_{ns}c_{ps})^{\frac{1}{2}} kTD_{it} \qquad (3\text{-}13)$$

where c_{ns} *and* c_{ps} denotes electron and hole capture coefficients for interface states. Since the exact values of these parameters are unknown, calculating the exact numerical value of s_0 is not possible. However, equation 3-13 shows that S_0 is directly proportional to D_{it}. This point can be used to compare the measured effective generation lifetime $\tau_{g\,eff}$ in first and second sets of wafers received by Samsung –referred to as old and new

samples. The first set has 45nm thermal oxide, fabricated at ASU facilities while the second set has 20 nm oxide processed at Samsung so we suspect the quality of oxide/Si interface to be better leading to lower s_0 for new sets of wafers.

Quasi-static measurement is one of the techniques by which D_{it} can be measured over the entire range of bang gap with good accuracy and with lower detection level of $10^{10}\mathrm{cm}^{-2}\mathrm{eV}^{-1}$ [2]. The drawbacks for this measurement technique are that it is very sensitive to leakage current and it also doesn't provide the capture cross section of the states. The concept of this measurement technique is based on the assumption that at very high frequencies the interface traps will not respond to probing ac signal and contribute no capacitance while at quasi-static condition they and the inversion minority carriers are able to respond the ac probe frequency. Therefore a high frequency *C-V* curve measured at frequencies of 100 KHz - 1 MHz can be suitably assumed to resemble a device which is free of interface traps and then. By comparing such curve with a quasi-static measurement where interface states disturb the theoretical *C-V* behavior, interface states density can be measured – Figure 3.28. Although this method provides D_{it} over band gap, for process screening purposes it is enough to focus on values close to mid-gap where surface potential is in the light inversion region and the technique is most sensitive. D_{it} can be extracted with following equation from quasi static and high frequency *C-V* curves [39]:

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{C_{qs}/C_{ox}}{1 - C_{qs}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}}\right) \tag{3-14}$$

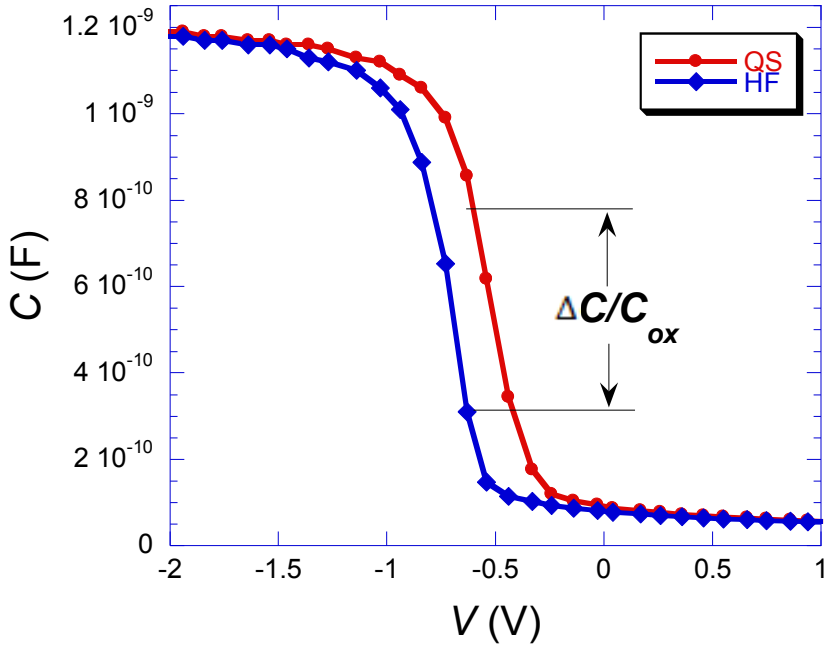

Figure 3.30: High frequency and quasi-static $C-V$ curves showing the offset $\Delta C/C_{ox}$ due to interface states measured on new set of samples.

We did the quasi-static measurement using a KEITHLEY Model 82 C-V system unit with high frequency range of 100 kHz. As showed in Figure 3.30, the D_{it} is larger for old set of wafers by approximately a factor of 10. In accordance to equation 3-13, it is expected respectively for s_0 to be larger for these wafers by a factor of 10.

Now taking into consideration equation 3-9, this can greatly impact the measured effective generation lifetime. The measured $\tau_{g\,eff}$ for old set of wafers is in range of 1-2 ms while for new set of wafers it is in the range of 10 ms. We have also calculated the τ_g – which should be essentially the same for both wafers – to be 30-60 ms.

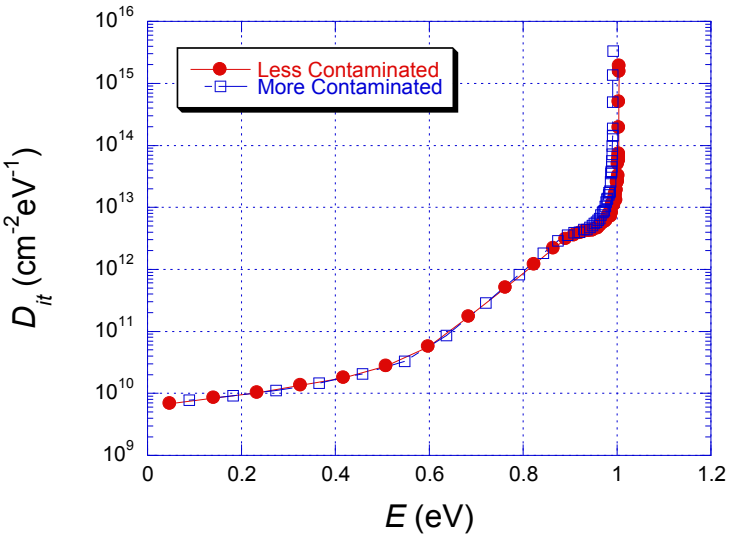

Figure 3.31: Interface states density versus energy from quasi-static method: more and less contaminated samples of new wafers.

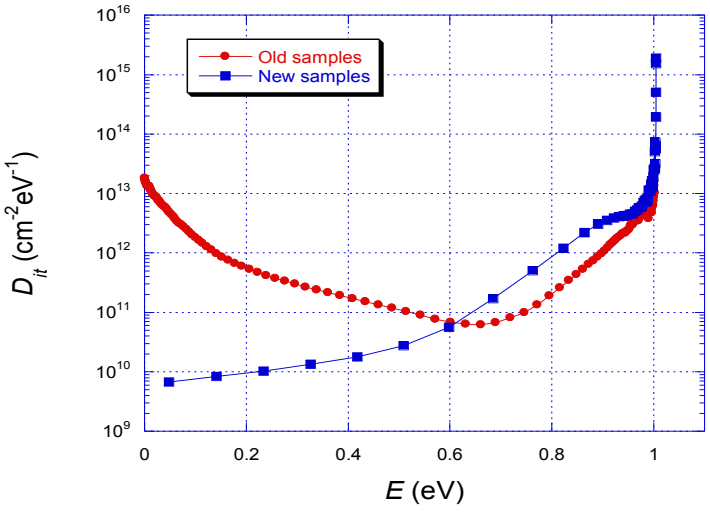

Figure 3.32: Interface states density versus energy from quasi-static method: old and new wafers.

Therefore, the observed difference in the values of S_0 between these sets of wafers justifies the different measured effective lifetime $\tau_{g\,eff}$ for these samples following equation 3-9. Figure 3.31 shows the contour plots of constant $\tau_{g\,eff}$ lines and can be used to visualize this problem. For any given τ_g in the above mentioned range, a ten-times increase of any low S_0 value would shift the measured $\tau_{g\,eff}$ from 10 ms range to 1 ms range. Care should be taken that no difference is detectable between more and less contaminated wafers in new set of samples, as illustrated in Figure 3.30. Therefore the independent study of interface states density is not a suitable choice for directly measuring the value of S_0 and using it for separating the bulk and surface components of $\tau_{g\,eff}$ and therefore this method cannot substitute the modified *C-t* method we proposed as a fast and reliable technique.

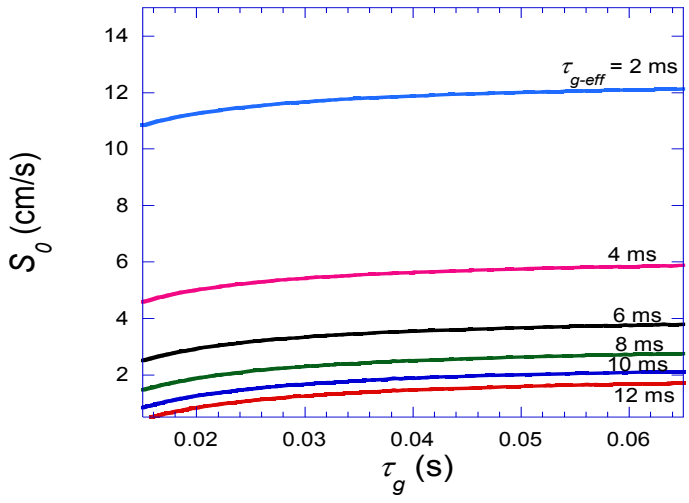

Figure 3.33: Contour plot of constant $\tau_{g\,eff}$ lines following equation 3-9 for gate radius of 0.5 mm.

CHAPTER 4:

CONCLUSION

We have made various measurements on the p/p^+ silicon epitaxial layers. X-ray diffraction results show excellent structural properties as one would expect from high-quality epi-layers. Photoluminescence measurements, which do not depend on the sample conductivity, yield recombination lifetimes entirely dominated by the heavily-doped substrate in which recombination is controlled by Auger recombination. Pulsed MOS capacitor measurements are suitable for characterization of epi layers, as they measure electron-hole pair generation lifetime in the reverse-biased space-charge region whose width is controlled by the operator and is typically a few microns wide and confide to the epitaxial layer.

We show results of pulsed MOS-C generation lifetime measurements on two different wafers, referred to as "less-contaminated" and "more-contaminated". The contamination level was provided to us as $<10^{10}$ cm^{-3} and 3×10^{10} cm^{-3} – both are very low. We find no significant lifetime difference between the two samples using the classic pulsed MOS Capacitor technique. This is not surprising as the measured lifetime is a combination of bulk and surface lifetimes. The effective generation lifetimes reported here, in the 10-20 ms range, are among the longest reported anywhere and are indicative of very pure silicon. Such silicon is suitable for image dark currents in 10^{-11} A/cm^2 range.

In addition, we showed that the classic pulsed MOS measurement technique is unable to distinguish low levels of impurity densities in epitaxial wafers due to domination of

surface over the generation lifetime. This fact doesn't change even with increasing the accuracy with which generation lifetime is extracted from *C-t* diagrams. Consequently, we presented a modified version of pulsed MOS measurement technique which can successfully reveal the difference between generation lifetime and therefore impurity densities in very clean epitaxial wafers. The modified pulsed MOS technique separates the generation lifetime from surface component by utilizing the measured effective diffusion length. The new technique is showed to be valid by a statistically designed experiment done on two wafers provided by Samsung with reported impurity levels of 3×10^{10} and less than $10^{10}\ cm^{-3}$.

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