Programmable ANalog Device Array (PANDA): A Methodology for

Transistor-Level Analog Emulation

by

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A Thesis Presented in Partial Fulfillment
of the Requirements for the Degree
Master of Science

Approved November 2012 by the
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ARIZONA STATE UNIVERSITY

December 2012

ABSTRACT

The design and development of analog/mixed-signal (AMS) integrated circuits (ICs) is becoming increasingly expensive, complex, and lengthy. Rapid prototyping and emulation of analog ICs will be significant in the design and testing of complex analog systems. A new approach, Programmable ANalog Device Array (PANDA) that maps any AMS design problem to a transistor-level programmable hardware, is proposed. This approach enables fast system level validation and a reduction in post-Silicon bugs, minimizing design risk and cost. The unique features of the approach include 1) transistor-level programmability that emulates each transistor behavior in an analog design, achieving very fine granularity of reconfiguration; 2) programmable switches that are treated as a design component during analog transistor emulating, and optimized with the reconfiguration matrix; 3) compensation of AC performance degradation through boosting the bias current. Based on these principles, a digitally controlled PANDA platform is designed at 45nm node that can map AMS modules across 22nm to 90nm technology nodes. A systematic emulation approach to map any analog transistor to PANDA cell is proposed, which achieves transistor level matching accuracy of less than 5% for I_D and less than 10% for R_{out} and G_m. Circuit level analog metrics of a voltage-controlled oscillator (VCO) emulated by PANDA, match to those of the original designs in 90nm nodes with less than a 5% error.

Voltage-controlled delay lines at 65nm and 90nm are emulated by 32nm PANDA, which successfully match important analog metrics. And at-speed emulation is achieved as well. Several other 90nm analog blocks are successfully emulated by the 45nm PANDA platform, including a folded-cascode operational amplifier and a sample-and-hold module (S/H)

ACKNOWLEDGEMENT

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

viii

1. INTRODUCTION

(1) Motivation

a. Fast Prototyping

The scaling of CMOS technology has provided enormous opportunities to integrate billions of transistors in circuit designs. Meanwhile, the development of analog/mixed-signal (AMS) chips becomes increasingly expensive, complex, and lengthy. [1] Fasting prototyping of analog circuits is important to lower design risks and enhance the confidence of designs. Not like digital signals, analog signals are more sensitive to the noise, since discrete representation of logic high and low in digital domain can accept more noise. Analog signals are represented as continuous values, whose precision can be easily affected by even minor noise. [2] There are a lot which have to be considered, such as variations of PVT (process, power supply, and temperature), mismatch, and etc, in order to increase Signal-to-Noise Ratio (SNR) and reduce design-to-market time. So it requires solid knowledge and sufficient design experiences for analog designers. Moreover, as shown in Figure 1, the traditional design flow takes a huge amount of time from concept building to products. The iteration of layout, fabrication, and testing can easily continue over a year for a typical IC product. The whole process is time-consuming and costs much money if multiple iterations need to be fabricated. [3] Without a reconfigurable analog platform, a counterpart of field

1

programmable gate arrays (FPGA), analog engineers are prevented from the benefits of fast prototyping and hardware emulation. Field Programmable Analog Arrays (FPAA) is highly demanded due to such benefits. With the tremendous help of rapid reconfiguration and hardware emulation, it enables instant testing phase before VLSI layout and fabrications. The total period of a typical analog IC design is reduced to a few days, instead of a year. [3]

Traditional Analog Design Cycle:

Concept → Simulation → VLSI Layout → Fabrication → Testing

(3 months)

x 3
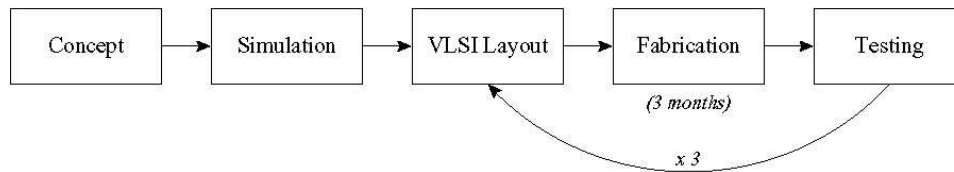
FPAA−based Rapid Prototyping Design Cycle:

Concept → Simulation → Testing → VLSI Layout → Fabrication

x 20
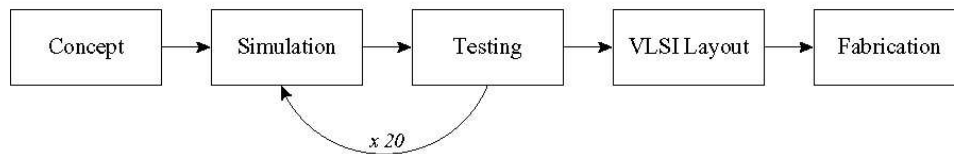
Figure 1 The comparison between Traditional Analog Design Cycle and FPAA design Cycle. [3]

b. The Analog Advantage

Regarding to the increasing popularity of portable devices, such as smart phones and pad computers, power efficient signal processing plays a more significant role in current academic and industrial areas. It is still difficult to implement digital friendly analog systems, considering limitation of the size and total power consumption. However, using and integrating analog systems into a larger digital system becomes a relatively easy option. FPAA fills into this

category, which is capable of transitioning systems from digital to analog. [2]
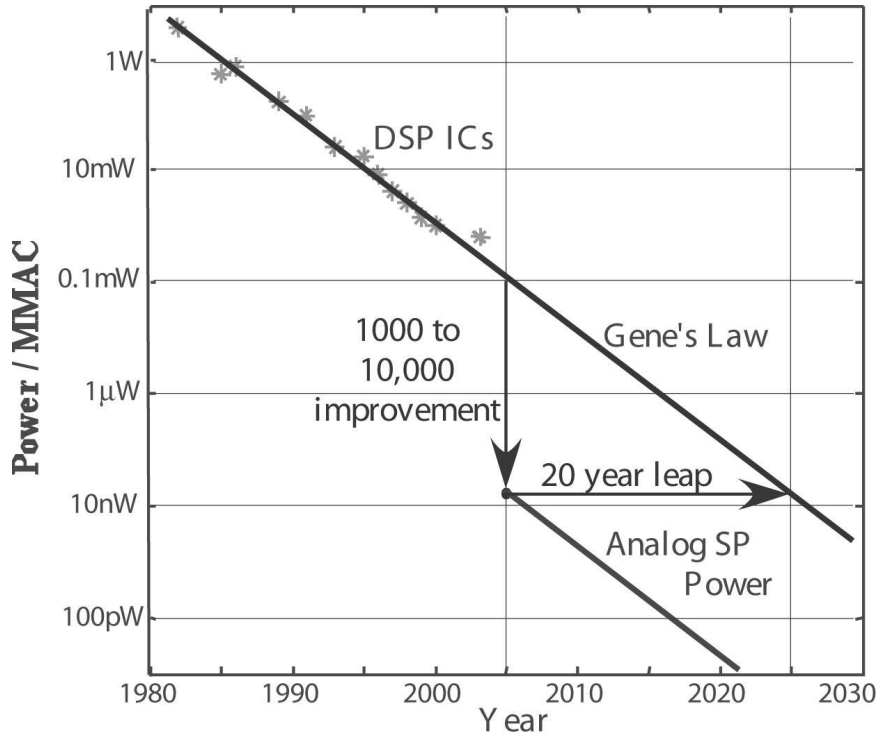
Figure 2 Power consumption trends in DSP microprocessors along with floating-gate based chip [Data Source: G. Franz, IEEE Micro, 2000; R. Ellis et al. (2002); P. Hasler et al. (2002); P. D. Smith et al. (2002b)].

One of main benefits of FPAA is the ability of power saving by implementing signal process in analog. According to Gene's law, the power consumption of DSP microprocessors decreases to one half every 18 months, which is consistent with Moore's law. Such advancement results from size scaling of advanced technology and some speed-up methodology. However, the power consumption of Analog to Digital Convertor (ADC) does not follow Gene's law, which is one serious problem needed to be solved for power efficient signal processing. And that part of power consumption will soon dominate the total power spending of digital systems. As the resolution of ADC moving forward by

3

1.5 bits every 5 years, a tradeoff that ADC consumes more power, or at least remains the same has been observed. [3]

In terms of the availability of computational flexibility, ADC is usually placed as close as possible to the analog input in most current signal processing systems. If some of the computations in reconfigurable analog platform could be completed prior to ADC, computational load on the digital processor would be largely reduced, and it would only require a simpler ADC. And therefore, the total power consumption would be saved during signal processing. The development of large-scale FPAAs and related CAD tools embraces such need and offer designers this option. As shown in Figure 2, floating-gate technology based FPAA and Reconfigurable Analog Signal Processor (RASP) perform an incredible power efficiency, up to 5 orders of magnitude, compared to custom DSP for the same application. [2][3]

(2) Overview of Past FPAA

Almost any types of digital circuits and systems can be simplified as some simple NAND gates, latches and D flip-flops. It enables the basic structure of Field Programmable Gate Arrays (FPGA). Any combinational logic can be derived by implementing NAND gates under the rule of Boolean logic. For sequential logic, a set of simple flip-flops and latches is able to store the data.

Regarding to them, NAND gates, basic flip-flops and latches provide the FPGA structure with repeated elements. Since there are a great amount of repeated cells in the platform, complicated routing is avoided. Due to simple topology of a single cell, the total area is saved largely. It benefits the area-efficient placement and easy routing for FPGA. For modern FPGA, copying such two basic primitives can create a digital friendly FPGA, and a large number of digital circuits and systems are able to be synthesized. [2]

Since the implementation of a FPGA is easy and generic, similar configurations are attempted for fast synthesis in the analog domain. In the analog signal processing, Computational Analog Blocks (CABs) are implemented to achieve computational logic in FPAA. The granularity of CAB characterizes different FPAA. So far, there are three types of FPAA in total in terms of the computational granularity and functionalities. However, the bottleneck of designing a versatile FPAA platform is lack of sufficiently generic basic cell, which is equivalent to NAND gates, flip-flops and latches of a FPGA. The large granularity of a FPAA demonstrates a good prototyping performance, but not enough functionality. For the fine-grain FPAA, it can provide a wide variety of functionality, but its performance degrades a lot because of its great parasitic from its switches. The next three small chapters describe such three types of FPAA briefly with respect to their advantages and disadvantages. [3]

5

a. Coarse Grain

Coarse grain CAB is made of Fourier processor or 'expert cell', which is able to deal with some direct signal conditioning application. Since the 'expert cell' is well designed with sufficient functionalities, low pass filter, D/A converter, and analog comparator are all configured with those cells by an easy interconnect matrix. IMP's EPAC[TM] devices are based on this coarse grain reconfigurable analog cell blocks. (Klein, 1996) But the main drawback of coarse-grain FPAA is limited flexibility and functionality. [3]

b. Fine Grain
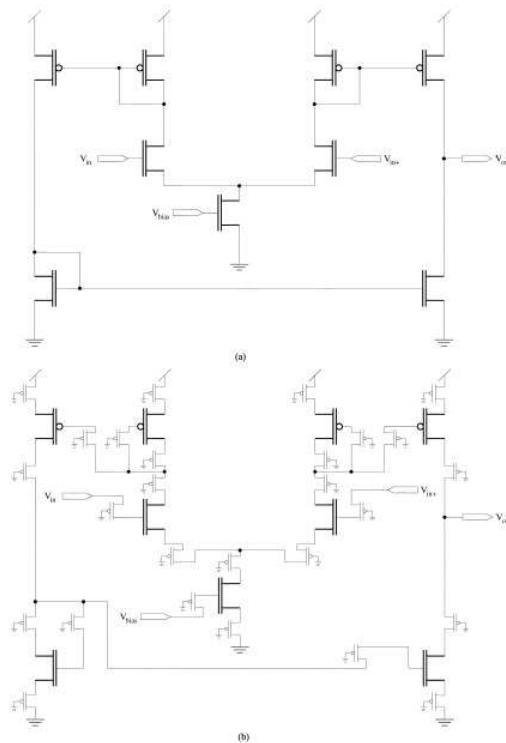
Figure 3 Comparison between a basic OTA and the same OTA implemented on a fine-grain FPAA. [2]

Fine-grain CAB is considered as programmable transistor-level block, which is usually used by only a transistor and its switches. It demonstrates a great benefit of synthesizing generic building blocks, whose primary application is an evolvable hardware. Nevertheless, the transistor-level analog block requires a large number of interconnect switches. Due to their non-ideal resistance linearity and large parasitic, the performance has to be degraded. [2]

Figure 3 gives us a good example of the impact of the switches of fine-grain CABs. Graph (a) shows a circuit schematic of a 9-transistor Operational Trans-conductance Amplifier (OTA). On a fine-grain FPAA, each transistor of the OTA needs to be replaced by a same-sized transistor and three reconfigured switches. It is how reconfiguration functions on the fine-grain FPAA. The synthesis requires at least 27 switches, which turn out to degrade OTA's performance dramatically. [2]

c.   Medium Grain

In order to balance the function versatility and signal processing performance on FPAA platform, medium-grain CABs become the mainstream of modern FPAAs. The fundamental structure of medium-grain CAB can be accomplished by a couple of options. One option is OTA, which can be synthesized as several linear and non-linear circuits and achieve amplification, integration, and filtering. (Ray et al., 2000; Pankiewicz et al., 2001, 2002) The

filter can be de-moduled to integrators and lossy integrators. OTA is the key component of all kinds of integrators and lossy integrators. And therefore, such OTA-based basic reconfigured blocks lead the advantage of rapid synthesizing analog circuits. The other option for medium-grain CAB is current conveyor, which saves a compensation circuit and offers a constant bandwidth, independent of its gain. By implementing current conveyor based CABs, the FPAA has more stability. With respect to its application, the current conveyor based FPAA exhibits amplification and filtering as well as log and antilog functions. (Gaudet and Gulak, 1997) [3]

(3) Programmable ANalog Device Array (PANDA)

The scaling of CMOS technology has provided tremendous opportunities in integrated circuit design, enabling integration capacity of billions of transistors [1]. The motivation for significant research in the design of power efficient signal processing systems has stemmed from the growing demand for complex information processing on portable devices. One method to achieve such low power designs has been to utilize analog signal processing, analog-to-digital converter (ADC) and the digital signal processing (DSP) core in the same system-on-chip (SOC). However, the performance of the analog device will continue to degrade with ongoing device scaling, especially with the intrinsic gain of a single transistor. [2][3][4]

8

Reduced headroom (around 1V), makes several gain and impedance enhancement techniques such as cascoding impractical. Overall, development of analog and mixed-signal (AMS) integrated circuits in deep sub-micron processes has become increasingly expensive, complex, and lengthy [1]. By leveraging a programmable analog platform, similar to a digital Field Programmable Gate Array (FPGA), it becomes possible for analog designers to attain the benefits of rapid prototyping, hardware emulation, and smooth migration to advanced technology nodes [4]–[6]. To retain such rapid prototyping capability and flexibility of FPGAs, previous commercial and academic efforts focused on an analog counterpart of the FPGA, namely Field Programmable Analog Arrays (FPAAs) [7].

Typical building blocks in an FPAA range from analog macros, such as switched capacitor circuits [8][9], operational amplifiers and transconductance amplifiers [10][11], to megamodules like ADCs, DACs, track and hold circuits [2]. In certain applications, floating-gate transistors were used as reconfiguration switches for the FPAA [12]–[14]. However, limited by the type and number of these primitives, FPAAs still do not have sufficient functionality and versatility for large-scale analog applications. Their performance is further degraded by low implementation density and high interconnect parasitics [10][11][14][15].

9

In this paper, a technique for transistor-level programmable analog design, named Programmable ANalog Device Array (PANDA) is proposed [16]. It enables device and circuit level optimization for various design choices through benchmarking representative AMS modules and aims to demonstrate the potential of the new analog platform. It also achieves transistor-level fine-granularity emulating and tuning flexibility in hardware, which is limited in a conventional field programmable-analog-array (FPAA) or other analog reconfigurable approaches [17].

(4) Unique Features of PANDA platform
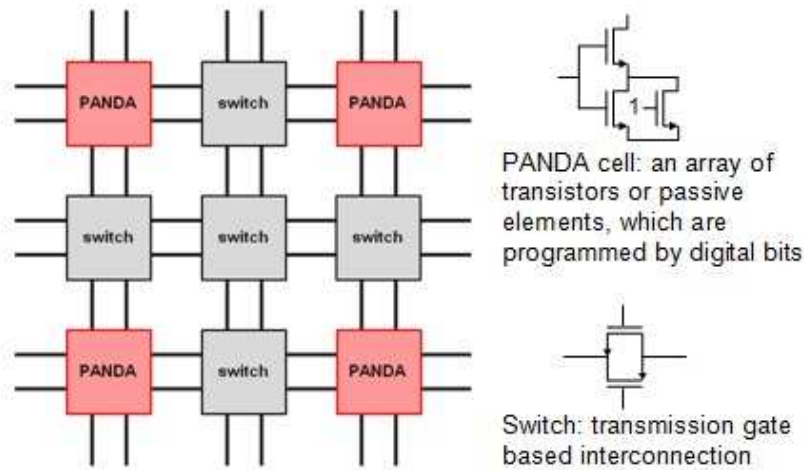
Figure 4 The Architecture and Components of A Digital-controlled Reconfigurable Analog Platform has it.

This paper describes techniques for transistor-level reconfigurable analog design, enabling optimization to various design choices through benchmarking representative AMS modules. It aims to demonstrate the potential of the new analog platform. Figure 4 illustrates the basic structure of the proposed platform.

Similar to a digital FPGA, it consists of programmable blocks of the device array, which emulates the behavior of an analog device, and switches.

Key features in this platform include:

- *Programmable PANDA Cell*: Distinguished from a digital logic design, the transistor is the fundamental building block in an analog design, requiring precise adjustment of its operating conditions. Therefore, the successful emulation of each transistor behavior in an analog design is the key to reproduce the system performance. In this paper, an array of scaled digital transistors is introduced to achieve this goal. Such an array is able to emulate the important metrics of a single analog transistor at the same bias condition, such as trans-conductance (g_m) and output resistance (r_0).

- *Programmable Switches*: Similar to digital FPGAs, transmission gate based switches are required to reconnect PANDA cells, depending on the topology of the analog circuit. To avoid their impact on analog performance, the synthesis of switches will be integrated into the cell reconfiguration, and their impact will be compensated during the sizing of PANDA cells.

- *Parasitics Reduction*: One of the limitations of traditional FPAAs is high parasitics from switches in the signal path. The additional resistance and capacitance dramatically lower the small signal bandwidth of the system. The proposed solution leverages the aggressive scaling of CMOS transistors, which

11

significantly reduces the parasitics, and reproduces the AC behavior across technology nodes.

- *New mapping technique* to recover the AC performance: It involves the boosting of bias current during cell mapping with the original design in order to achieve at-speed emulation.

These merits are demonstrated through the emulating of multiple high speed benchmarks circuits, including the operational amplifier, VCO, VCDL, and S/H modules.

The rest of the paper is organized as follows. Section 2 focuses on the architecture of the transistor-level PANDA platform, the principles of reconfigurability, and it also explains the details of a transistor-level PANDA cell design. Moreover, it explains managing routing and switching parasitics and automatic cell sizing methodology. At-speed emulation technique is discussed in detail as well. In Section 3, several benchmarks circuits, including the operational amplifier, sample and hold (S/H) modules, and voltage-controlled oscillator (VCO) are used to demonstrate 45nm PANDA for 90nm technology node. 65nm and 90nm Voltage-Controlled Delay Lines (VCDL) are emulated by 32nm PANDA, whose AC performance is recovered by speed-up methodology. Initial benchmark results illustrate the promises and opportunities of the proposed PANDA platform.

2. PRINCIPLES OF TRANSISTOR-LEVEL RECONFIGURABILITY

Transistor-level optimization, such as biasing and sizing is the fundamental step of an analog design procedure. To successfully map any analog circuit to a target platform, it is essential to emulate the desired behavior of each analog transistor and to achieve very fine granularity of reconfiguration. This section discusses the principles and design of a PANDA cell in order to find a simple, physical, and generic solution.

(1) Analog Properties in Scaling

Achieving a good balance among various performance metrics is one of the fundamental challenges in analog design. While such trade-offs are complex, they can be linked to fundamental attributes of transistors [18]. Some important analog attributes include the bias current (I_D), trans-conductance (g_m), and output impedance (r_0). A detailed understanding of these device-level effects, as well as their scaling trend, provides a useful insight into analog circuit construction. Based on first-order short-channel MOSFET models [19], these analog properties can be described using the following equations for a short-channel device in the saturation region:

$$
\begin{aligned}
I_D &\approx W \cdot v_{sat} \cdot C_{ox} \cdot (V_{GS} - V_{TH} - V_{DSsat}) \\
&\approx W \cdot v_{sat} \cdot C_{ox} \cdot (V_{GS} - V_{TH0} + \alpha \cdot V_{DS} - V_{DSsat})
\end{aligned}
\tag{1}
$$

where v_{sat} is the saturation velocity, C_{ox} is the gate capacitance, V_{TH0} is the long-channel threshold voltage V_{TH}, and α is the Drain-Induced Barrier

13

Lowering (DIBL) coefficient, which significantly influences the output impedance. The small signal parameters g_m and r_0 can be represented by:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx W \cdot v_{sat} \cdot C_{ox} \tag{2}$$

$$r_0 = \frac{\partial V_{DS}}{\partial I_D} \approx (W \cdot v_{sat} \cdot C_{ox} \cdot \alpha)^{-1} \tag{3}$$
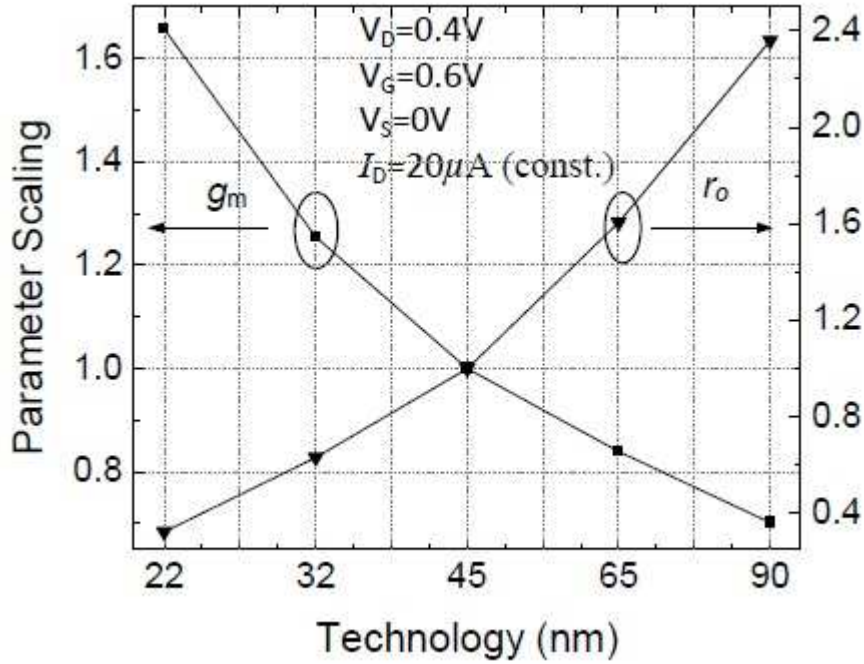
Figure 5 The scaling trend of transistor properties at same bias conditions. g_m and r_0 are normalized by those of 45nm node transistor to compare their trend between each technology node. Because of the thinner gate dielectric and faster carrier transport, g_m increase at smaller technology nodes and r_0 degrades mainly due to stronger DIBL effect.

Figure 5 illustrates the trends of these properties, using the Predictive Technology Model [20]. Under constant bias voltages and transistor width, I_D and g_m increase at smaller technology nodes, because of thinner gate dielectric and faster carrier transport. On the other side, r_0 degrades with device scaling mainly

14

due to stronger drain-induced barrier lowering (DIBL) effect. These observations

match the model prediction in Eqts. (1-3), helping to guide the construction of a

PANDA cell, as presented in the next section.

(2) PANDA Cell Topology And Sizing Strategy

(a)

(b)

(c)
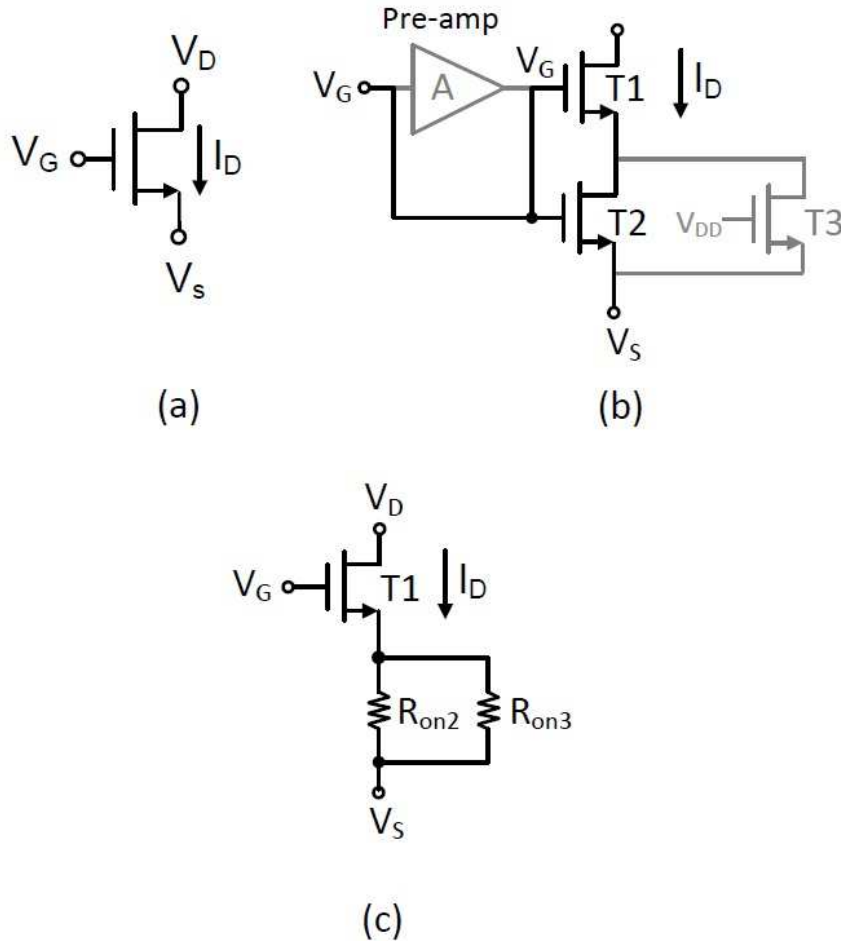
Figure 6 The transistor-level mapping with a PANDA cell; (a) the original analog transistor (b) A 3-transistor PANDA cell. The pre-amplifier and T3 can be connected to the cell or bypassed. (c) The equivalent circuit of the 3-transistor PANDA cell. R_{on2} and R_{on3} are the on resistance of T2 and T3.

The foundation of the PANDA platform is a programmable cell, which

consists of transistor stacks, parallel branches and if needed, a pre-amplifier

(pre-amp) as shown in Figure 6 (b). The platform maps the analog properties of both backward emulation (BE) and forward-emulation (FE). As shown in Figure 6, the focus is to boost the transconductance for FE and decrease it for BE. In this paper, BE is more focused. Such a cell should be generic to handle various analog conditions and it should also be area-efficient to minimize the parasitics. The cell construction is based on device physics so that the accuracy and scalability will be guaranteed. Figure 6 (b) presents such a transistor-level solution for analog mapping.

Three digital transistors are employed in this structure, based on the consideration of MOSFET scaling properties:

- T1: T1 is the primary transistor in the cell to match the analog properties of the original transistor.

- T2: T2 is added in series to T1. It has the same gate bias as that of T1 and operates in the linear region.

- T3: T3, which is gate biased at V_{DD}, is added in parallel to T2 in order to better control the source end of T1. Based on the requirement of g_m and r_o, T3 can be connected to the cell or bypassed (Figure 6 (b)).

Several critical analog transistor properties, such as I_D, G_m, and R_{out}, can be matched by tuning the transistor size in this parallel-series network. To achieve uniformity within each cell, all devices have the same gate length and V_{TH}. An

NMOS transistor is mapped to an NMOS only cell, and a PMOS only cell is used to map a PMOS transistor. Since analog design usually involves multiple gate lengths and V_{TH} values in practice, PANDA offers a couple of gate lengths and two V_{TH} values, which are applied to all transistors in a cell. This improves the flexibility and accuracy in the matching procedure. In order to match the analog properties of the original transistor, the sizes of T1, T2, and T3, which are defined W1, W2, and W3 respectively, act as the tuning knobs during the matching process. Figure 6 (c) shows the equivalent circuit of the 3-transistor PANDA cell. As T2 and T3 operate in linear region, they can be considered as variable resistors whose resistance can be controlled by their widths W2 and W3. The equivalent transconductance (G_m) and output resistance (R_{out}) of the PANDA Cell can be expressed in terms of the device parameters as follows.

$$
\begin{aligned}
G_m &= \frac{\partial I_D}{\partial V_G} \\
&\approx \frac{g_{m1} r_{o1}}{R_{on2} \parallel R_{on3} + [1 + g_{m1} \cdot (R_{on2} \parallel R_{on3})] r_{o1}} \\
&\approx \frac{g_{m1}}{1 + g_{m1} \cdot (R_{on2} \parallel R_{on3})}
\end{aligned}
\tag{4}
$$

Where g_{m1} is the transconductance of T1 and R_{on2}, R_{on3} are output resistance of T2 and T3, respectively. The combined device output impedance is defined by

$$
\begin{aligned}
R_{out} &= [1 + g_{m1}(R_{on2} \parallel R_{on3})] \cdot r_{o1} + (R_{on2} \parallel R_{on3}) \\
&= [1 + g_{m1} r_{o1}] \cdot (R_{on2} \parallel R_{on3}) + r_{o1}
\end{aligned}
\tag{5}
$$

Since $g_{m1}r_{o1} \quad 1$, the output impedance can be approximated by

$$R_{out} \approx g_{m1}r_{o1}(R_{on2} \quad R_{on3}) + r_{o1}$$
$$= [1 + g_{m1} \cdot (R_{on2} \quad R_{on3})] \cdot r_{o1} \qquad (6)$$

The parallel combination of T2 and T3 serves as source degeneration that reduces G_m, but boosts R_{out} by the degeneration factor, $1 + g_{m1}(R_{on2} \quad R_{on3})$. Since R_{on2} and R_{on3} can be approximated as

$$R_{on2} \approx [W_2 \cdot (V_{GS} - V_{TH})]^{-1}$$
$$R_{on3} \approx [W_3 \cdot (V_{DD} - V_{TH})]^{-1} \qquad (7)$$

The degeneration factor can be maximized when W2 and W3 are minimum, achieving the lowest G_m and the strongest R_{out}. The matching is an iterative process: initially, W1, as the size of the primary cell transistor, is adjusted to match I_D; then W2 and W3 are tuned for G_m and R_{out} matching. The iteration continues until the errors in all three metrics are small enough.

Figure 7 shows the matching ranges of G_m and R_{out} of a 45nm PANDA cell compared against that of transistors across different technology nodes at the same bias current and voltages. The region of G_m that can be achieved by a 45nm PANDA cell for different W2, W3 and fixed bias current is shown in Figure 7 (a). For small W3, G_m increases with increase in W2, but at sufficiently large W3, G_m is independent of W2 which is evident from Eqt. (4). It shows that a 45nm PANDA cell can achieve G_m of transistors across 32nm to 90nm nodes; however, to match G_m of advanced technology node transistors like 22nm special

18

G_m boosting circuit is required. The region of achievable R_{out} of a 45nm PANDA cell for varying W2, W3 sizes at fixed bias current is shown in Figure 7 (b). It can be observed that for small W3, R_{out} decreases with increase in W2 but the dependence of R_{out} on W2 decreases as W3 increases which is evident from Eqt. (6). It illustrates that 45nm PANDA cell can successfully emulate R_{out} of transistors across 22nm to 90nm technology nodes.
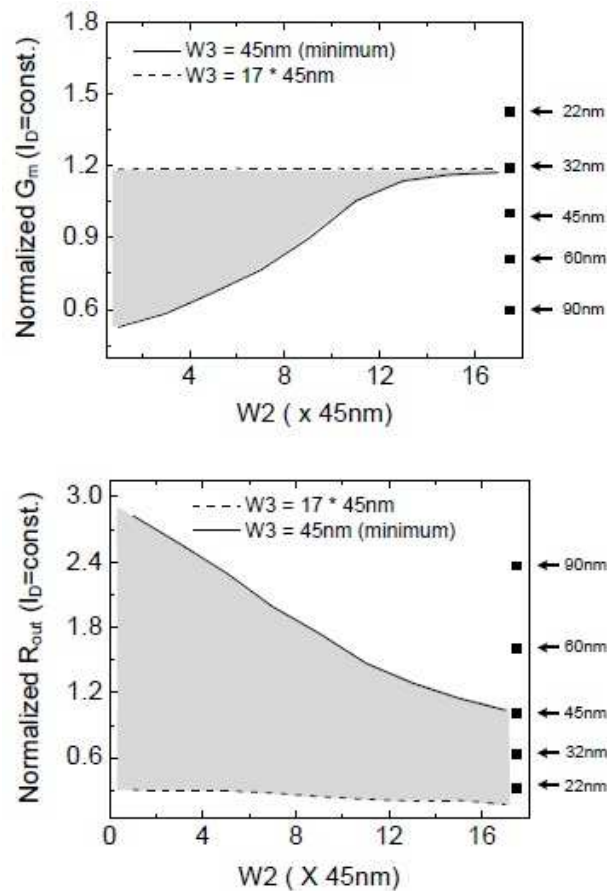
Figure 7 The G_m and R_{out} trend of the PANDA cell according to sizing transistors in the cell. The bias voltages and current are constant (V_D=0.4 V, V_G=0.5 V, V_S=0 and I_D=20 uA). The right side points are the values of g_m and r_o of the single transistors in different technologies. All points are normalized with respect to the 45nm single transistor performance for comparison. The shaded areas are the possible G_m and R_{out} matching ranges using 45nm PANDA. ((a): Top Graph; (b): Bottom Graph)

(3) Automatic Sizing of a PANDA Cell

The digital FPGA platforms gained popularity in the design community since they

facilitate rapid prototyping and design validation of digital circuits. Computer

Aided Design (CAD) tools play a major role in the development of FPGAs as

they efficiently map the design to the logic cells in FPGAs. Automation is

possible, only if there is a systematic way of mapping any design to its

digital/analog programmable cell. Exhaustive search on transistors sizes for

mapping the AMS design to PANDA cells is time-consuming, and hence it is not
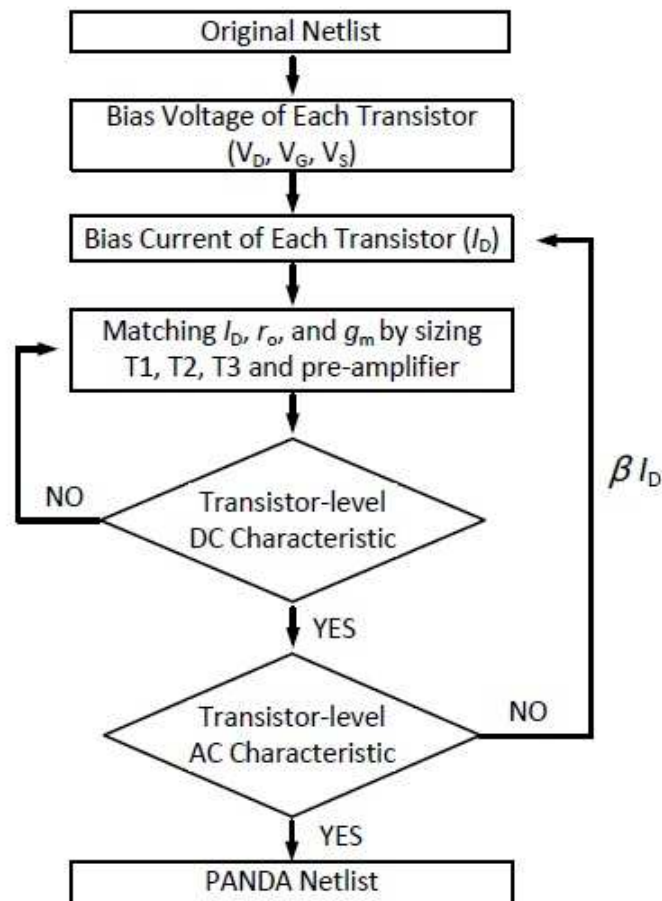
Figure 8 Automatic PANDA mapping methodology

20

feasible for large-scale analog emulation. In this section, a systematic way

mapping the PANDA cells enabling automation is proposed. To avoid the impact

of non-idealities in reconfiguration switches, they are incorporated into the cell

design during the mapping stage so that their impact is compensated by the

transistor sizing.

Emulating of an analog transistor to a PANDA cell in order to match the

transistor-level analog properties is an iterative process. The methodology
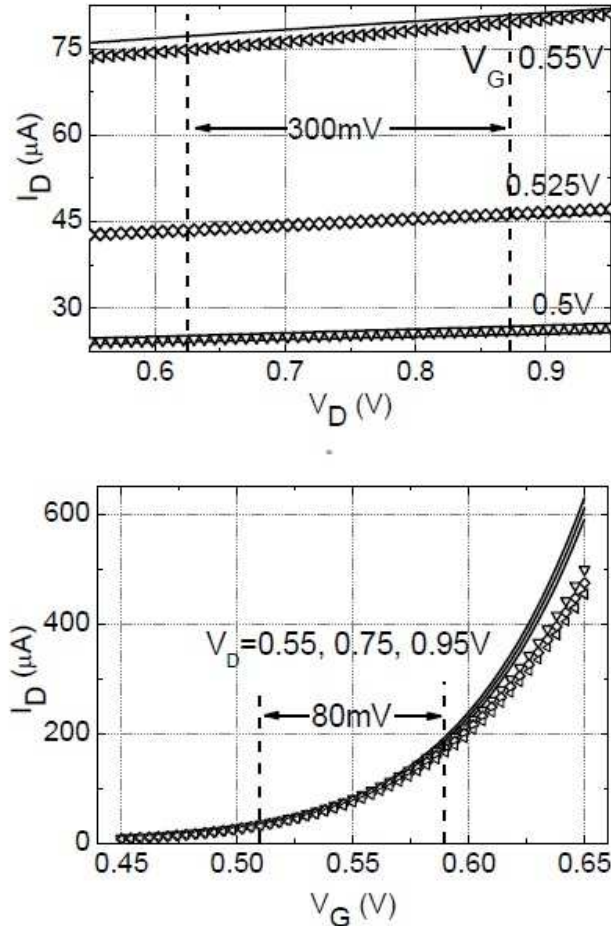
Figure 9 An example of transistor mapping. Nominal bias: V_G=0.55V, V_D=0.81V, V_S=0.23V. Within the matching range, the maximum error in I_{bias}<5%, in G_m and R_{out}< 10%.

to map a given AMS module into PANDA platform is shown in Figure 8. For each transistor in the netlist of original AMS circuit, bias voltages (V_S, V_G and V_D) are extracted. Transistors T1 and T2 in Figure 6 are sized iteratively to match the I_D and r_o respectively under the same bias voltages as that of the original transistor. For BE, T3 is sized to match the g_m. The sizing step of the transistors is adaptively changed in each iteration loop, based on error percentage, which aids for faster convergence to the final solution.

Figure 9 shows the examples of the automatic size matching between a 45nm PANDA cell (L=100nm) and a 90nm analog transistor (L=200nm). The matching range for V_G and V_D is 80mV and 300mV respectively in BE. The maximum mapping errors are optimally controlled (<3% in I_D, <10% in r_o and g_m). Such matching accuracy is sufficient to reproduce DC performance for BE application.

(4) Integration of a Switch

In addition to programmable PANDA cells, programmable switches are needed to configure the cell connection, based on the original analog design topology. By utilizing a programmable metal-fuse, which enables a one-time programmable post-silicon tuning, can help minimize the challenges of programmable switches [21], [22]. In this study, the transmission gate is employed as the switch (Fig 4), for the sake of simplicity. However, different

22

from a switch in a digital FPGA system where it is always linked to a high impedance node (i.e., gate input), the switch in an analog design may be required to connect two low impedance nodes, such as the source and drain of two transistors. In this condition, it may induce some voltage drop across the switch which significantly affects the DC bias conditions, small signal gain and bandwidth [2]. The solution is to size the cell transistors in the presence of the switch, as shown in Figure 4. With the existence of the switch, the additional voltage drop is absorbed by cell transistor sizing during the emulation procedure. Following the cell configuration, there will be no additional voltage drop or performance degradation when the cells are connected. The metal wires used for routing the signals also have some resistance, however this resistance is negligible compared to the resistance of the transmission gate switch. For instance, the resistance of metal interconnects in the 45nm node with the minimum width ranges from $5\Omega/um$ in metal layer-1 to $3\Omega/um$ in metal layer-5 [23], which is too less compared to the ON resistance of transmission gate switch. The mapping error of I_D, R_{out} and G_m depends on the size of the transmission gate switch as illustrated in Figure 10, which shows the total size of the mapped transistors T1, T2 and T3 for different switch resistances at 3 bias currents of 20uA, 50uA and 100uA. As the resistance of the switch increases, the voltage drop across the switch increases and hence the sizes of T1, T2 and T3 required for

23

matching the I_D, R_{out} and G_m of the target transistor increases. Also the mapping

error in R_{out} and G_m increases as the resistance of the switch increases as shown in

Figure 10.
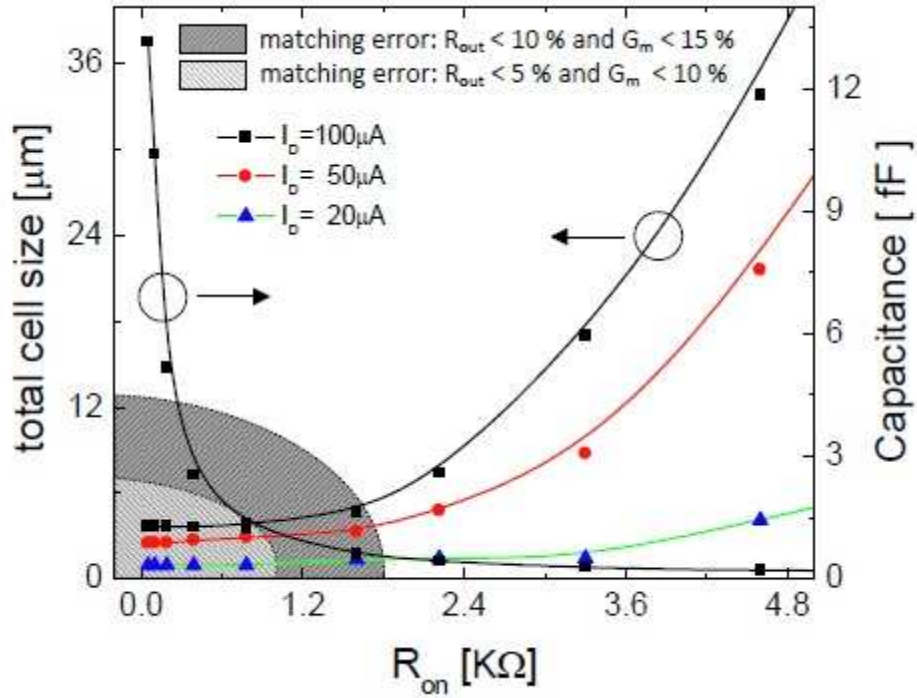
Figure 10 The mapping error of I_D, R_{out} and G_m versus the switch resistance and capacitance.

3. PARASITICS AND AC PERFORMANCE

(1) Parasitics

While the procedure detailed in previous section matches the I-V curves to

the first derivatives, the impact of such a matching on parasitic capacitance needs

to be evaluated for AC circuit behaviors (e.g., unity-gain frequency, slew rate,

etc.). Figure 11 illustrates the total cell parasitic capacitance during the tuning, as

a variable of bias voltages and the matching error. The error in I_D is controlled to be smaller than 1% in order to ensure the matching of DC bias conditions after all cells are connected, and the errors in G_m and R_{out} are monitored; the total cell
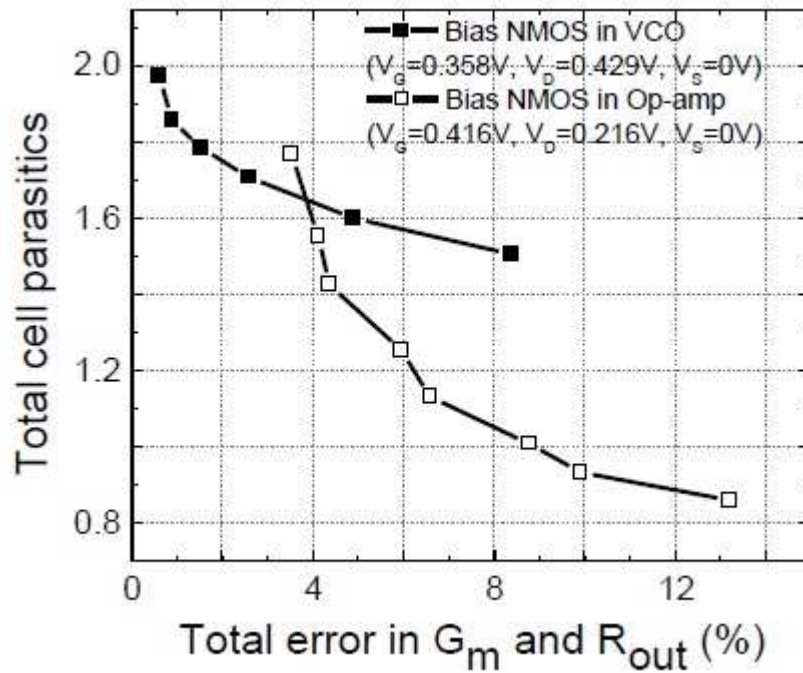
Figure 11 The cell parasitics depend on the bias condition and the accuracy requirement. The cell parasitics are normalized to that of the original 90nm transistor.

parasitics is normalized with respect to the original transistor, i.e., the parasitic capacitance stays the same if the normalized value is one. Two matching cases are shown, one from the VCO (Sec. 3. (3)) and the other from the folded cascode operational amplifier (Sec. 3. (1)). There are mainly two factors influencing the cell parasitics:

25

- *Gate bias voltage*: since I_D is proportional to the product of W and $(V_{GS}-V_{TH})$ (Eqt. (1)), a lower V_{GS} leads to smaller voltage headroom and thus, requires larger W1 to match I_D, which increases the parasitic capacitance.

- *The matching error in G_m and R_{out}*: with a larger W1 to match I_D, G_m is usually over-estimated (Eqts. (2) and (4)). In this case, W2 needs to be further increased to reduce G_m, as indicated by Eqt. (4). Therefore, a higher matching accuracy requires a larger cell size and larger parasitics.

These tradeoffs can be observed in Figure 11. For instance, due to larger V_G than that of the NMOS and a better tolerance of G_m and R_{out} error, the PANDA cell to match the Op-amp NMOS may have a lower parasitics than the original 90nm one, implying the feasibility to match the AC response of the Op-amp. On the other side, the parasitics in the VCO case will increase after the matching, because of lower V_G and tighter error control.

(2) AC Performance Recovery

Matching the bias current (I_D), transconductance (G_m) and output resistance (R_{out}) for each transistor to those of the PANDA cell ensures that DC performance metrics, such as DC gain, common-mode rejection ratio (CMRR), power supply rejection ratio (PSRR) and slew rate of the AMS units, are matched. However, AC performance of such circuits may be degraded in some cases, as parasitic capacitance at each node is hard to be evaluated and matched. AC

26

performance limitation can be observed especially in forward-emulation where a scaled technology transistor is emulated using a network of mature node transistors which are intrinsically slower. In order to achieve at-speed emulation (e.g. high speed input and output circuits), increasing the bias current (I_D) facilitates the recovery of AC response.

$$I'_D = \beta \cdot I_D \tag{8}$$

$$G'_m = \beta \cdot G_m \tag{9}$$

$$R'_{out} = R_{out} / \beta \tag{10}$$

By increasing the bias current and transistor size by β, Gm increases β, R_{out} decreases by β, and thereby DC gain (G_mR_{out}) is maintained. The bias voltages for each PANDA cell are also maintained. However, the decreased r_o results in the improvement of AC performance.

4. CIRCUIT BENCHMARKS OF PANDA

Several representative AMS circuits have been chosen and mapped onto the proposed platform to demonstrate PANDA approach. Specific examples include a high-gain operational amplifier (op-amp), the most fundamental block in the analog design, a sample-and-hold module (S/H), a wide tuning range VCO, and a wide tuning range VCDL. The benchmark study starts from the custom design at the 90nm for BE emulation. The entire design, including the bias circuit, is then decomposed into transistors, each of which is automatically mapped to a

45nm PANDA cell as detailed in Section 3. Finally these 45nm PANDA cells are connected by the switches for performance evaluation. In order to demonstrate the BE emulation durable, the 65nm and 90nm VCDLs are implemented by 32nm PANDA cells.

(1) Folded-cascode Op-amp

The op-amp is a fundamental building block in analog integrated circuit design, ranging from DC bias circuits to high-speed amplification or filtering circuits [24]. The opamp design continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. Design of the op-amp consists of determining specifications, selecting device sizes and biasing conditions, compensating the op-amp for stability, simulating and characterizing the op-amp A_o (open loop gain), CMRR (common-mode rejection ratio), PSRR (power supply rejection ratio), output voltage range, current sourcing/sinking capability, and power dissipation. Popular op-amp architectures include the current-mirror, folded-cascode, and the telescopic structure. Among them, the folded-cascode structure (Figure 12) is commonly used because of its high DC gain and large unity-gain frequency. For this 90nm circuit, as well as the S/H module, gate length (L) of 200nm is used for high gain and circuit robustness. The 45nm PANDA cell has L=90nm and V_{TH} is 100mV lower than the nominal value.
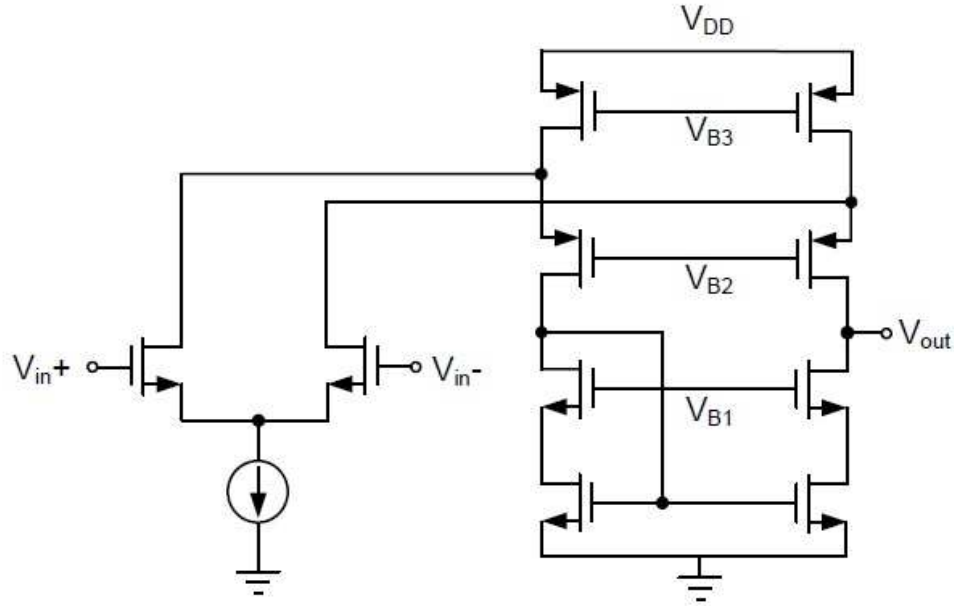
Figure 12 The circuit topology of the 90nm folded-cascode op-amp (L=200nm for all transistors).

Table I PERFORMANCE COMPARISON OF BE 45NM PANDA BASED OP-AMPS

Topology	90nm	45nm PANDA (BE)
DC Gain	71.11 dB	66.45 dB
Gain Bandwidth	121.9 MHz	107.8 MHz
Phase Margin	68.1 deg	61.9 deg
Slew Rate	58.08 V/us	51.53 V/us
PSRR+ at 10 kHz	92.73 dB	84.02 dB
PSRR- at 10 kHz	71.02 dB	66.12 dB
CMRR at 10 kHz	92.29 dB	82.94 dB

Table I compares the analog properties of each op-amp transistor after the mapping. The mapping of I_D and r_o achieves higher accuracy than that of g_m. The tolerance of g_m error provides better area efficiency, as indicated in Fig 10, and thus, improves the matching of AC performance. Most DC and AC specifications are very well matched.

(2) Sample and Hold

The sample-and-hold module plays a crucial role in the design of data acquisition interfaces, particularly ADCs. S/H design is fundamentally difficult because of the tradeoff among multiple metrics, such as linearity, unity-gain frequency, large voltage swing, high drive capability, and low power dissipation [25].

Figure 13 illustrates the structure of a fully differential S/H stage. The operation is based on the switched-capacity, with an operational trans-conductance amplifier (OTA) in the center to support high-speed, high-resolution ADCs [26]. Table II presents the OTA performance after mapping to a 45nm PANDA. The AC metrics, such as the slew rate and the settling time, match or slightly out-perform those in the original design. Figure 14 presents the input and output of the S/H circuits between target and 45nm PANDA. Good matching of the analog metrics of the OTA in S/H circuit between the target and PANDA circuit ensures proper matching of output transients. This guarantees the validation of the S/H operation.
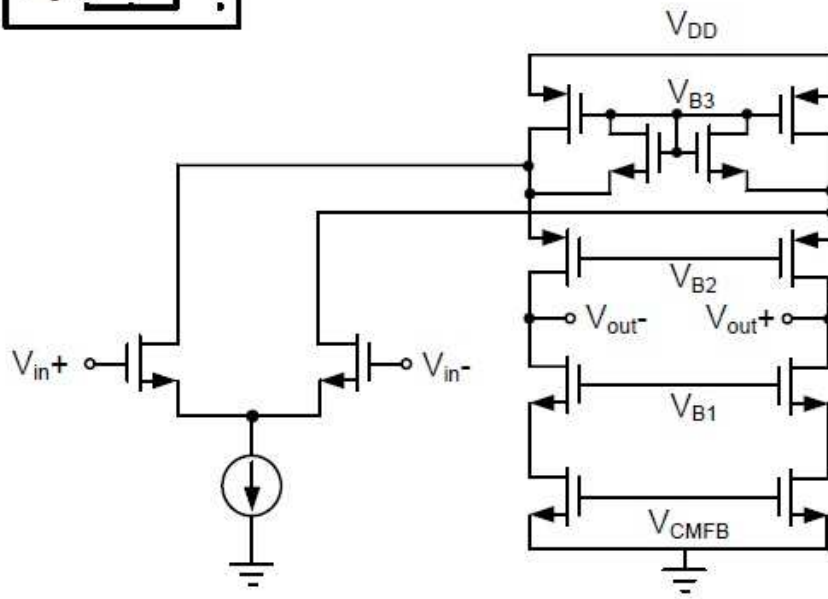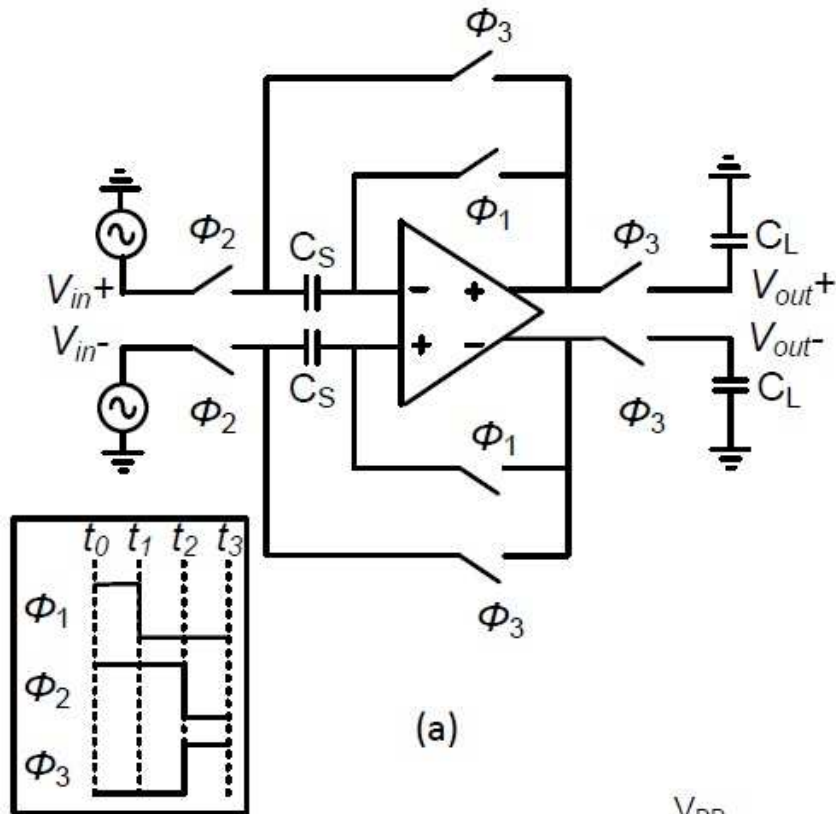
Figure 13 The 90nm design of the sample-and-hold module (L=200nm; the bias circuit is not shown).

31

Table II PERFORMANCE COMPARISON OF 45NM PANDA BASED FULLY DIFFERENTIAL OTAS

Technology	90nm	45nm PANDA (BE)
DC Gain	65.54 dB	61.54 dB
Gain Bandwidth	704.2 MHz	690.56 MHz
Phase Margin	62.26 deg	65.91 deg
Slew Rate	121.5 V/us	124.6 V/us
Settling Time	2.79 ns	2.56 ns
THD	54 dB	51 dB

Figure 14 Comparison of S/H module transient response. Backward-emulation settling time difference < 5%.

(3) Voltage Controlled Oscillator (VCO)

Different from the op-amp and S/H, which mainly process analog signals, a VCO usually operates in a much wider range of operating points, and its output is autonomous. This mixed-signal unit is essential to today's microprocessor design, especially in PLL and DLL circuits [27], [28].
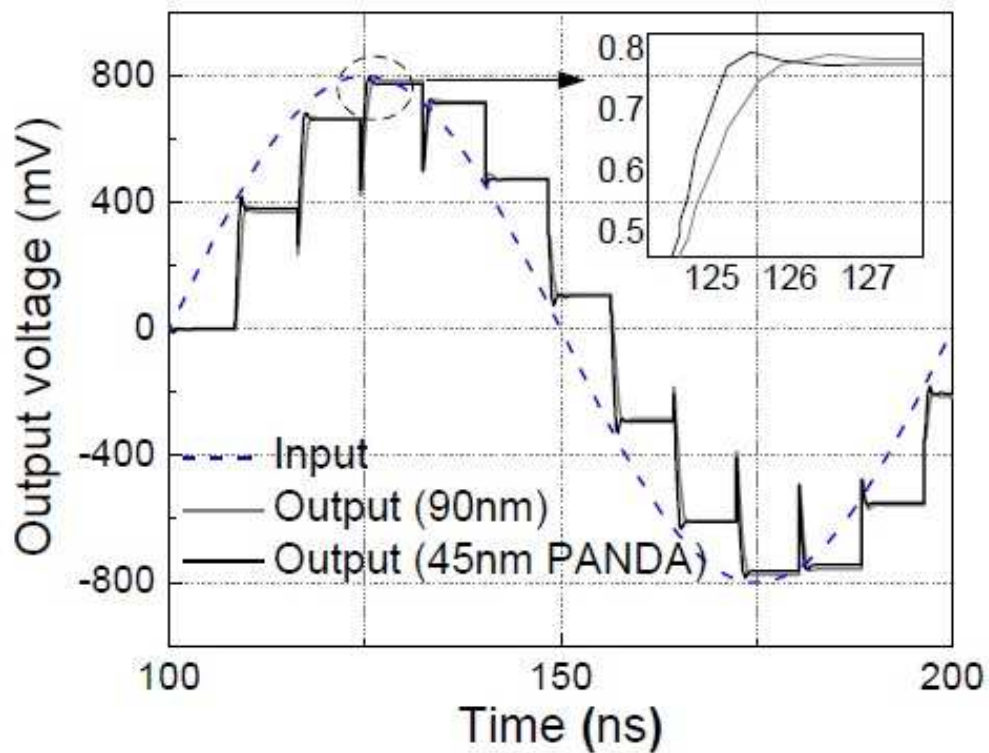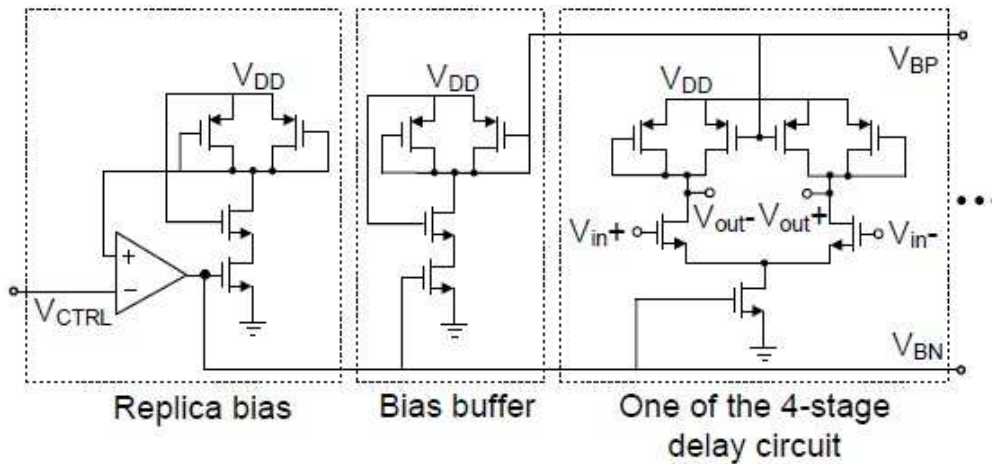

Figure 15 The circuit topology of the 90nm VCO (L=90nm for all transistors).

Figure 15 shows the basic structure of the VCO design, including a 4-stage differential ring oscillator and the replica feedback biasing [27]. The minimum gate length (L=90nm for the original 90nm design and L=60nm for 45nm PANDA) is used in this example to achieve high oscillation frequency. Each delay stage contains a source coupled pair with symmetric loads. The PMOS bias voltage limits the lower bound of the output voltage swing. An external control voltage, V_{CTRL}, changes the effective load resistance, tuning the delay of the

33

differential ring oscillator and frequency. This design achieves better delay control

and high rejection to dynamic supply noise [28].
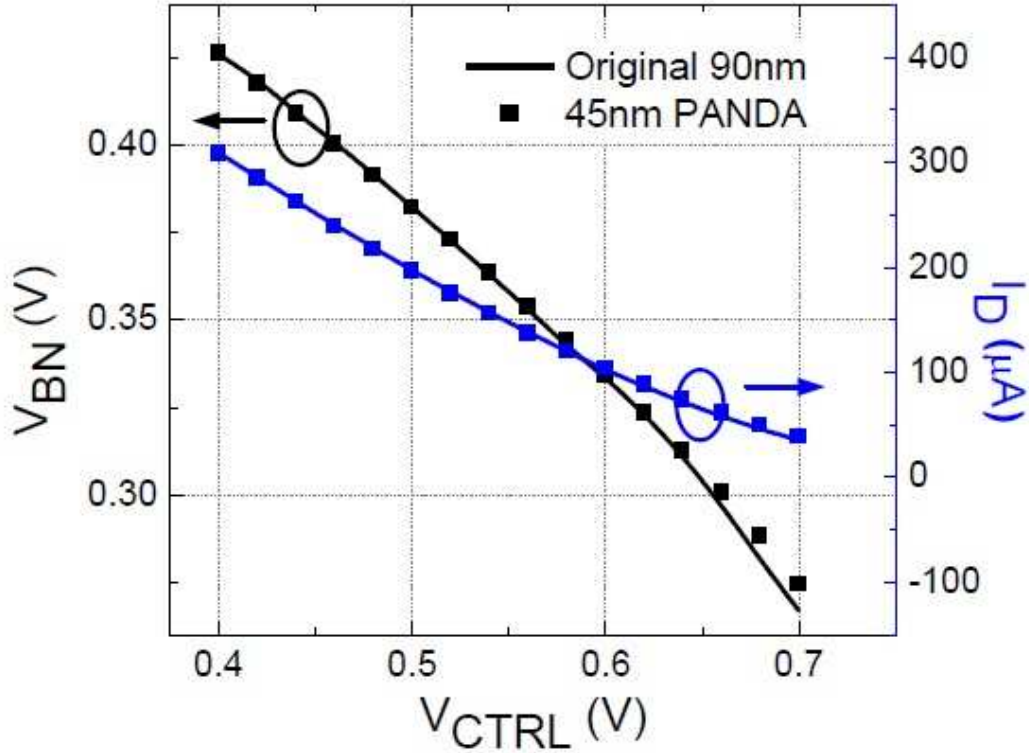
Figure 16 The bias control in VCO design. The response of bias current (I_D) and voltage (V_{BN}) under V_{CTRL} tuning.

Since the VCO operates across a wide range of V_{CTRL}, high accuracy in

transistor-level matching is required to ensure correct voltage to frequency gain.

The proposed PANDA approach is capable of supporting such a need, as

demonstrated in Figure 16. Figure 16 presents the response of bias current (I_D)

and voltage (V_{BN}) under V_{CTRL} tuning. The result from PANDA closely matches

that of the original design and thus, promises the correct sensitivity of VCO

performance to voltage tuning. On the other side, such fine matching inevitably

leads to larger parasitics after the matching, as indicated in Sec. IV. Therefore, the oscillation frequency degrades in the PANDA circuit.

Figure 17 examines the tuning characteristic of the VCO frequency. As expected, the center frequency drops significantly after the mapping, due to the increase in parasitic capacitance, while the sensitivity to V_{CTRL} is well maintained by 45nm PANDA. The linearity also matches that of the original 90nm design. The tuning range of this VCO is defined as the range of V_{CTRL} beyond which the frequency has >10% deviation from the linear control [29]. Under this definition, a similar tuning range is realized by PANDA.
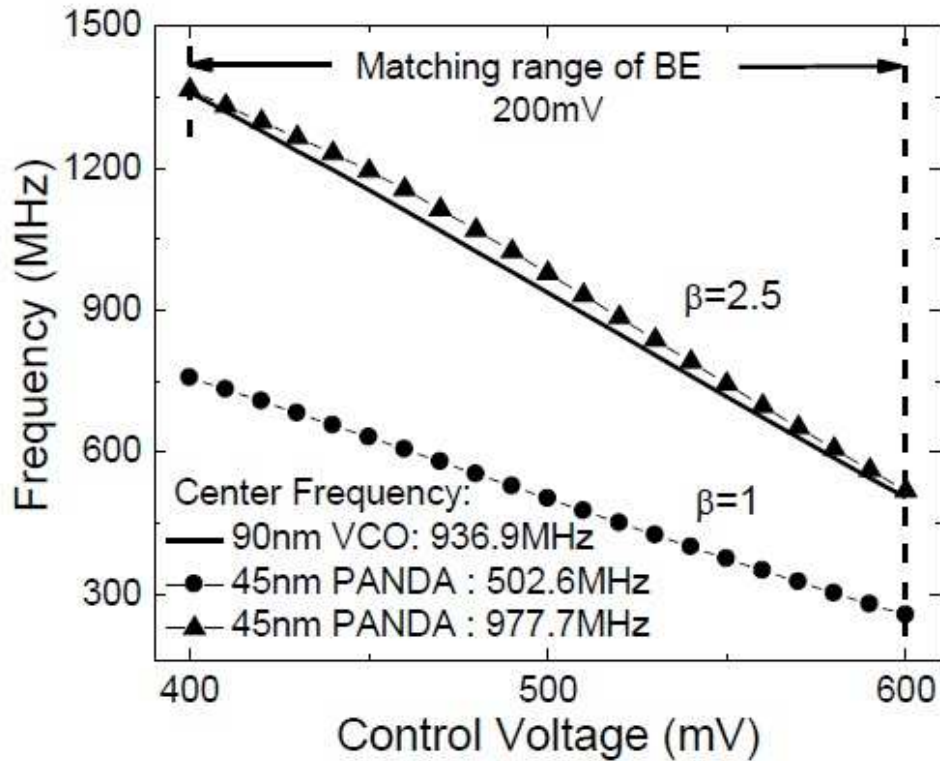

Figure 17 The variation of VCO frequency with control voltage for backward emulation.

VCO is an important component in high speed I/O circuits. The validation of high speed I/O circuit functionality requires that VCO be emulated at the speed of its peripheral circuits. Especially, at-speed emulation of an advanced technology transistor using a mature technology is very challenging as the intrinsic speed of a single transistor in an advanced technology node is much higher than that in a mature technology node. However, Figure 17 successfully demonstrates that increasing the current βI_D can recover the VCO back to its original speed while maintaining its sensitivity to control voltage. The matching ranges of the actual frequency sensitivity to control voltage are 200mV for backward-emulation.

Table III PERFORMANCE COMPARISON OF 45NM PANDA BASED VCOS

Technology	90nm	45nm PANDA (BE)
Center Frequency	936.9 MHz	977.7 MHz
Frequency Gain (K_{VCO})	543 MHz/mV	521 MHz/mV
Frequency Range	284.2-1343 MHz	297.8-1363 MHz
Tuning Range	200 mV	200 mV
Phase Noise	-121 dBc/Hz	-123 dBc/Hz

Table III summarizes the comprehensive evaluation of VCO performance in 45nm PANDA. Most important metrics, especially the sensitivity to the control voltage, the tuning range and the phase noise, are well matched. This confirms PANDA as a vehicle for functionality validation.

36

The speed recovery of 90nm PANDA VCO is successfully demonstrated by properly increasing the bias current through the cell (β factor). To overcome the difficulties of large parasitic and insufficient drive ability, the speed recovery technique is essentially oriented by how to choose the optimal sizes of T1, T2, and T3 such that the delay through the PANDA cell is minimized. To maintain the voltage bias condition of each cell element, the transistors relative ratio in T1, T2, and T3 are supposed to be kept constant.
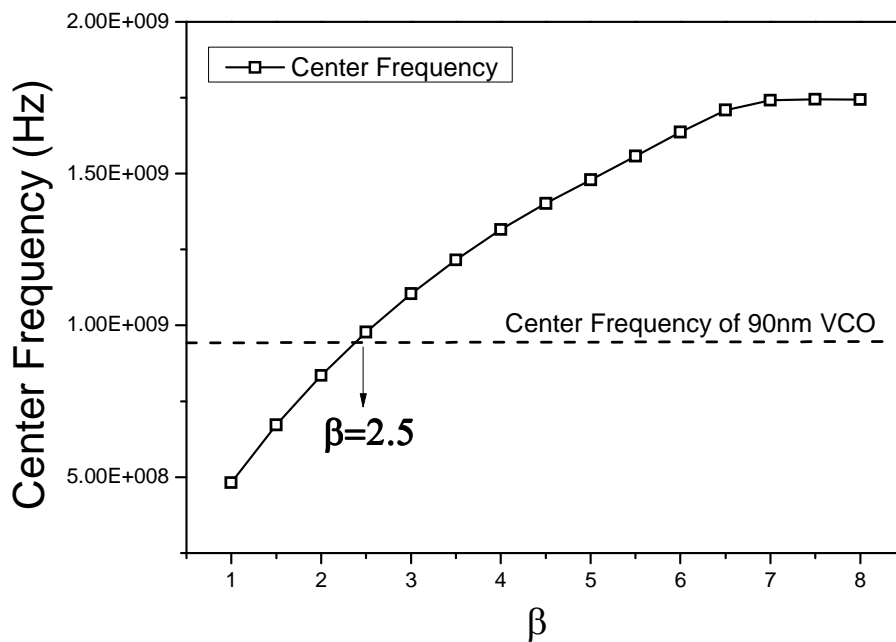

Figure 18 The center frequency variation with β.

However, there is a limitation of β factor in term of at-speed emulation. Figure 18 shows the variation of center frequency with β values. We can see that center frequency increases with increase in β. Increase in I_{bias} helps decrease

the charge/discharge period and hence center frequency is boosted. After a particular β, center frequency does not increase as expected, because increased size of T1, T2, and T3 loads itself. The huge parasitic capacitance due to β factor would slow down the complete speed. Center frequency eventually saturates for higher β values and even decrease if the PANDA cell is too large. Hence by optimizing β factors, the center frequency of the 45nm PANDA VCO can achieve that of the target 90nm VCO.

(4) Voltage Controlled Delay Line (VCDL)
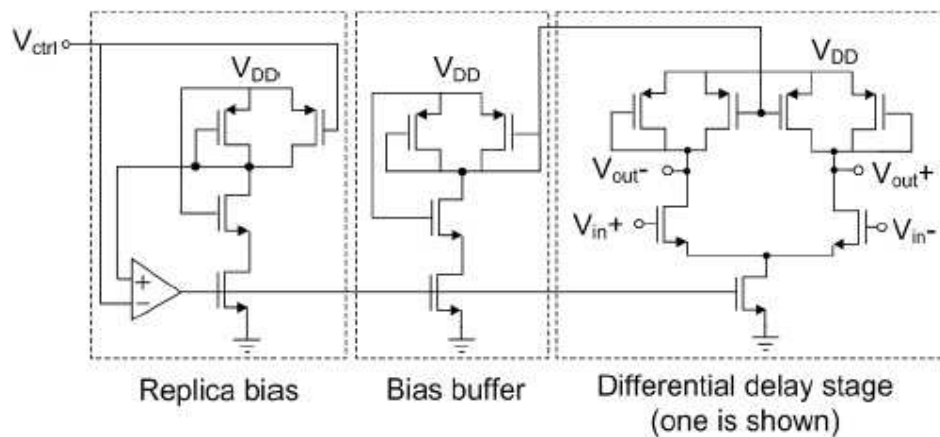
Figure 19 A self-bias VCDL schematic.

The first generation of DDR SDRAMs showcased clock frequencies of approximately 66-133 MHz, a speed slow enough to use a simple digital delay-locked loop (DLL) to synchronize the clock with output data. High-performance GDDR4 SDRAMs have progressed from these previous generations by pushing speeds up to multi-giga-hertz range, while scaling cycle

times down to less than 1ns. To accommodate the improved performance of high-speed SDRAMs, a mixed-mode DLL which combines both digital and analog implementations is vastly emerging.
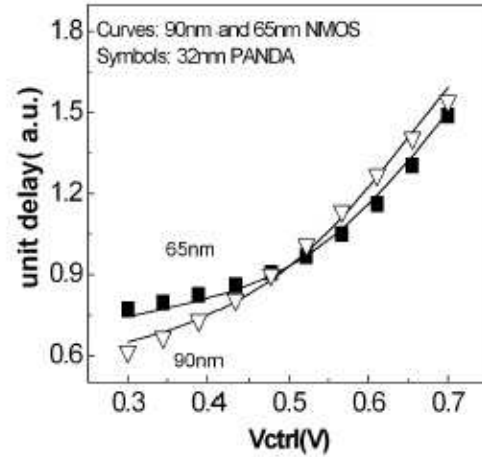
(a)
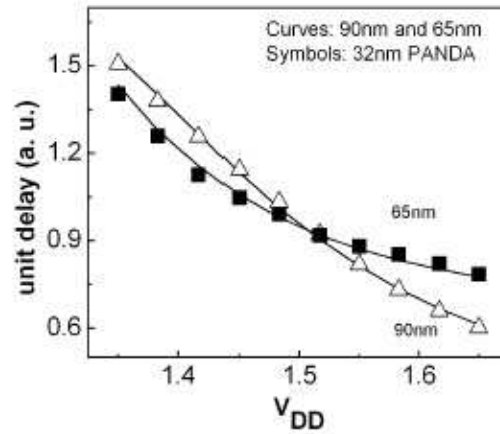
(b)

Figure 20 The sensitivity of VCDL performance to external voltages; (a) the unit delay versus the control voltage. (b) the sensitivity of VCDL delay to external voltages.

A voltage-controlled delay line (VCDL), shown in Figure 19, is suitable for the analog. [30][31] The tuning characteristic and supply sensitivity of the VCDL delay is illustrated in Fig 20. The mapping strategy succeeds to the

emulation of the sensitivity of the VCDL performance for both mapping cases. At

the matching stage, each transistor is replaced by one PANDA cell, which under

the same bias conditions, has the identical G_m and R_{out}, so that the VCDL behaves

identically after matching. As shown in Figure 20, the sensitivity to V_{ctrl} is well

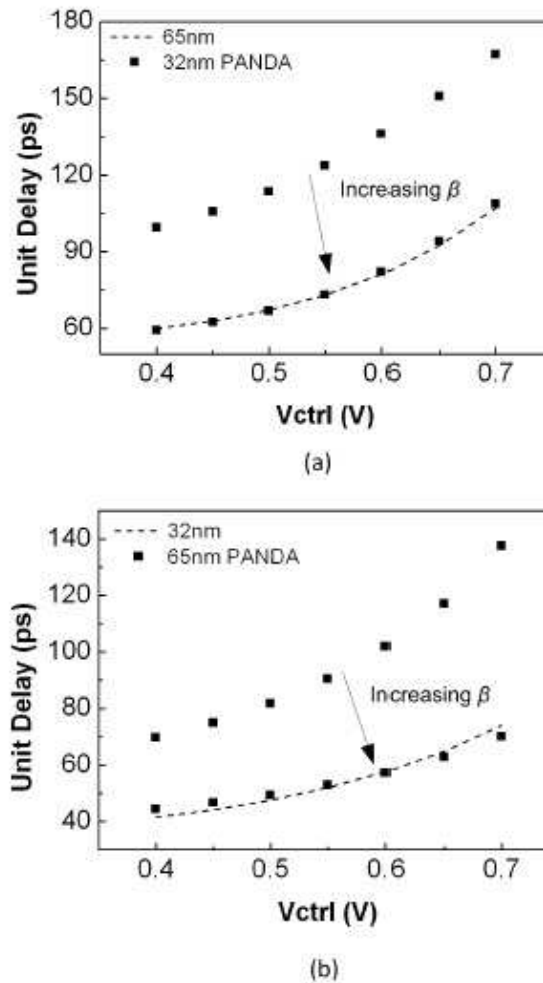maintained by the 32nm PANDA.

(a)

(b)

Figure 21 The speed and sensitivity of VCDL performance to external control voltage; (a) 32nm tech maps 65nm (b) 32nm maps 90nm.

The expected DC behavior matching process comes with large parasitics.

In the PANDA cell, for instance, as the V_{gs} decreases, the W_1 size is required to

40

increase to maintain an equal I_{bias}, which contributes to greater parasitics. Moreover, the number of parasitics again inflates as the W_1 size increases. And G_m reaches an increasingly greater value, and in an effect to reduce this value.

Meanwhile, the sizes of W_2 and W_3 proportionately grow. This condition is seen in Figure 21, where within the entire voltage control region, the delays of VCDL after an original PANDA mapping are much greater than those with a stricter G_m and R_{out} error regulation.

The speed matching method aims to control such variance in VCDL speeds through two different approaches: the increase of I_{bias}, and the reduction of parasitics and resistance.

• The most important element of VCDL is the fully differential delay stage. The charge or discharge time of the delay stage highly depends on I_{bias}. Thus, boosting I_{bias} reduces the delay time, which eventually contributes to an increase of speed.

• The charging or discharging process is through the internal capacitance and resistance in VCDL. The boosting I_{bias} associates with the reduction of the R_{out}, because of the same bias voltage condition. The reduced R_{out} promises decreasing the time constant of VCDL, and therefore the speed can be improved.

Figure 21 shows the speed match method in effect, as over a wide control

41

voltage area, the I_{bias} is tuned and the PANDA cell resized, which allows for the most accurate G_m level to be reached, reducing the delays and eventually matching the original values of the VCDL. The boosting factor β was 1.14 and 1.31, respectively, for the 90nm (DDR3) and 65nm (GDDR4) mapping. However, β is not supposed to keep going up without the limitations of the sensitivity match and power consumption. Other metrics of the speed matching strategy, such as minor errors of G_m and R_{out}, constrain the increase of β.

5. LIMITATION OF THE PANDA PLATFORM

Since a network of scaled transistors in the PANDA platform are applied to emulate both mature and advanced technology nodes, there is a upper bound for this type of platform due to technology capability. It cannot ignore the impacts of power supply limitation and process variation after fabrication. This chapter mainly discusses about the technology mapping range and the recovery technique after fabrication.
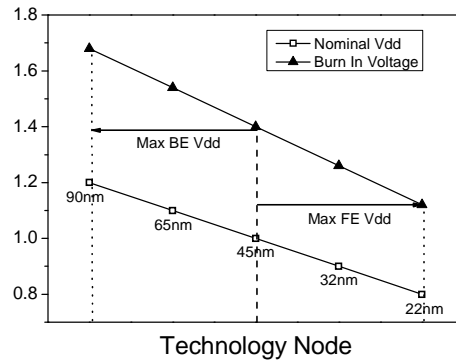
(1) Limitation of Power Supply

Figure 22 Technology emulation range due to power supply limitation.

The nominal power supply of 45nm node is lower than that of 90nm node, and higher than that of 32nm. In order to emulate 90nm circuits and systems, the 45nm PANDA platform may function at a power supply voltage above its nominal value. The burn-in voltage should be taken into account, which is the maximum power supply, maintaining a stable reliability. Usually, the burn-in voltage is 1.4 times larger than its nominal value.

In Figure 22, the burn-in voltage line is upper bound for each technology node. For the advance technology node, like 22nm, its nominal power supply is a lot smaller than nominal 45nm power supply. Figure 22 shows that even the burn-in voltage of 22nm just reach 1.1X 45nm nominal supply value. Figure 22 also tells us that the burn-in voltage of 45nm is 1.17X 90nm nominal supply value. It means that there is a limitation of BE in the PANDA platform. It should be aware of 1.4V is the upper bound of 45nm PANDA platform if BE is used.

(2) Process Variation

The length, width, and oxide thickness may vary after fabrication. It is called "Process Variation". The threshold voltage change is one of leading effects, because of process variation. It eventually has an impact on the speed and bias point of analog/digital circuits. Process variation is particularly important at an advanced technology node (<65nm). Since our PANDA platform is made at 45nm node, how the threshold voltage variation changes the mapping of a single

43

transistor's attributes is our first consideration, as shown in Table IV. Table IV

indicates the huge mapping error regarding to the threshold voltage change after

fabrication.

Table IV THE COMPARISON OF A SINGLE TRANSISTOR'S MAPPING ERROR DUE
TO PROCESS VARIATION

Error (90nm/45nm PANDA)	I_{bias}	R_{out}	G_m
V_{th} decreases 10%	-64.46%	42.72%	-17.04%
V_{th} decreases 5%	-29.27%	25.77%	-0.12%
Nonimal V_{th}	-2.9%	6.1%	14.45%
V_{th} increases 5%	20.65%	-20.90%	28.83%
V_{th} increases 10%	40.55%	-58.63%	42.49%

Programmable capability benefits the performance recovery tuning after

fabrication. Since T1, T2, and T3 consist of many parallel transistors, the number

of the parallel transistors is proportional to the equivalent width. The degraded

analog attributes could be recovered

Table V THE COMPARISON OF A SINGLE TRANSISTOR'S MAPPING ERROR AFTER
WIDTH TUNING FOR RECOVERY

Error (90nm/45nm PANDA)	I_{bias}	R_{out}	G_m
V_{th} decreases 10%	-1.86%	7.46%	26.86%
V_{th} decreases 5%	-2.88%	7.96%	19.54%
Nonimal V_{th}	-2.9%	6.1%	14.45%
V_{th} increases 5%	1.99%	-1.01%	13.61%
V_{th} increases 10%	2.18%	-1.5%	7.72%

6. CONCLUSION

This paper presents a design methodology achieving a transistor-level programmable analog design. The proposed programmable PANDA cell consists of three scaled transistors to emulate an individual analog transistor DC and AC performance under various bias conditions. PANDA fundamentally overcomes the shortcomings of previous FPAAs, achieving transistor level granularity, convenient reconfiguration, and generic mapping of any analog design between process nodes. A systematic mapping algorithm that maps any analog transistor to the PANDA platform within 10% error is also proposed. The effectiveness in analog emulation and prototyping is demonstrated through the mapping of several representative AMS modules, including the op-amp, sample and hold stage, and VCO. Recovery of AC performance metrics such as opamp bandwidth, VCO which are degraded because of reconfigurability, is demonstrated. Overall, this technique promises a new approach toward programmable analog design, which is vitally important for design productivity.

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