Efficient Circuit Analysis under Multiple Input Switching (MIS)

by

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of the Requirements for the Degree
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ABSTRACT

Characterization of standard cells is one of the crucial steps in the IC design. Scaling of CMOS technology has lead to timing un-certainties such as that of cross coupling noise due to interconnect parasitic, skew variation due to voltage jitter and proximity effect of multiple inputs switching (MIS). Due to increased operating frequency and process variation, the probability of MIS occurrence and setup / hold failure within a clock cycle is high. The delay variation due to temporal proximity of MIS is significant for multiple input gates in the standard cell library. The shortest paths are affected by MIS due to the lack of averaging effect. Thus, sensitive designs such as that of SRAM row and column decoder circuits have high probability for MIS impact. The traditional static timing analysis (STA) assumes single input switching (SIS) scenario which is not adequate enough to capture gate delay accurately, as the delay variation due to temporal proximity of the MIS is ~15%-45%. Whereas, considering all possible scenarios of MIS for characterization is computationally intensive with huge data volume. Various modeling techniques are developed for the characterization of MIS effect. Some techniques require coefficient extraction through multiple spice simulation, and do not discuss speed up approach or apply models with complicated algorithms to account for MIS effect. The STA flow accounts for process variation through uncertainty parameter to improve product yield. Some of the MIS delay variability models account for MIS variation through table look up approach, resulting in huge data volume or do not consider propagation of RAT in the design flow. Thus, there is a need for a methodology to

model MIS effect with less computational resource, and integration of such effect into design flow without trading off the accuracy. A finite-point based analytical model for MIS effect is proposed for multiple input logic gates and similar approach is extended for setup/hold characterization of sequential elements. Integration of MIS variation into design flow is explored. The proposed methodology is validated using benchmark circuits at 45nm technology node under process variation. Experimental results show significant reduction in runtime and data volume with ~10% error compared to that of SPICE simulation.

DEDICATION

This thesis is dedicated to my parents, my husband Desikan and my three children

Akila, Nive & Math.

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First of all I would like to express my sincere thanks to committee chairman and advisor Dr. Kevin Cao for all his valuable guidance throughout the challenging course of this research work. Also I am very grateful to Dr Kevin for providing me flexible time schedule without which my part-time Ph.D program would not be a success.

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CHAPTER 1

INTRODUCTION

1.1 Static Timing Analysis

1.1.1 Synchronous design:

VLSI designs widely apply pipelined synchronous design approach for performance improvement. The sequential elements such as latches and flip flops are clocked by the synchronous clock with a set of logic function performed by logic gates in between them in a given clock period. As shown in Figure 1.1, the number of standard cells in between the sequential elements can be longer of shorter as required by the definition of the sub system.

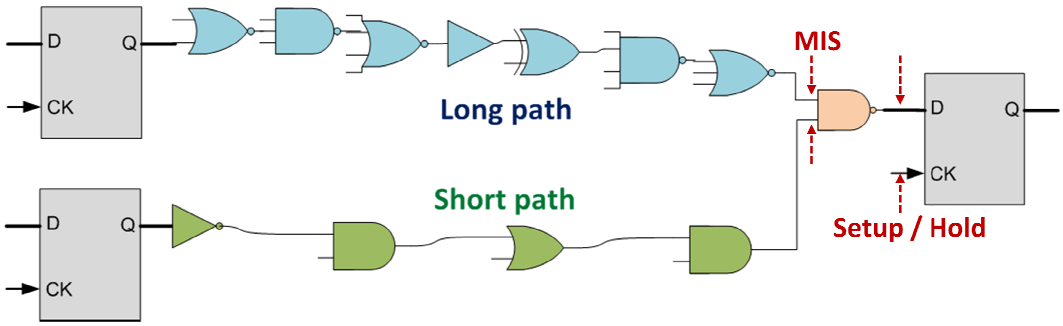

Figure 1. 1: Critical path in Synchronous design

As shown in Figure 1.2, the setup time is the time interval before active clock edge when the data must be stable to meet the performance requirement of the design. The hold time is the time interval after the active clock edge where the data must be held stable to meet the desired functionality of the design. The longest paths impact the setup time of the design for a given clock frequency and the shortest path impact the hold time of the design for required functionality.

Meanwhile, the Scaling of CMOS technology has led to timing un-certainties in VLSI designs, due to increasingly high variability in device and circuit performance caused by static and dynamic variations. Also the proximity effect of the input signals in multiple input gate is becoming prominent, which is referred as multiple input switching effect (MIS) in Figure 1.1. Thus the timing analysis of the longest and shortest critical paths in the design is one of the crucial steps for design closure.

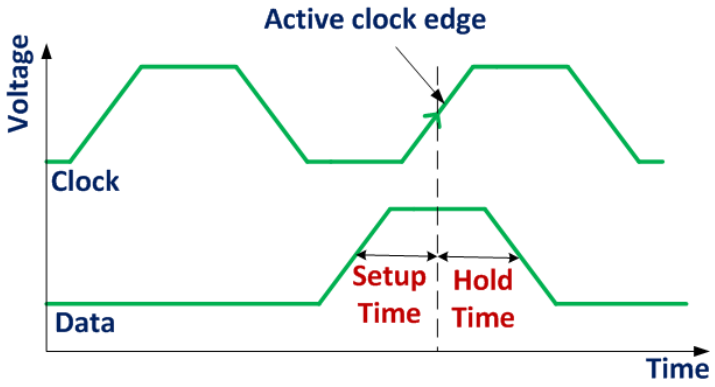

Figure 1. 2: Definition of Setup time and Hold time

Dynamic simulation for timing analysis is computationally expensive, as it uses device-level models and requires state vectors to capture all possible scenarios of boundary conditions. Static timing analysis [1-3] on the other hand is comparatively faster due to the usage of gate level timing models by analyzing all possible longest and shortest paths between the sequential elements in the design. The delay model used in traditional STA assumes single input switching (SIS) condition for the characterization of multiple input logic gates. Thus the delay variation due to temporal proximity effect of MIS is not accounted during timing analysis.

To speed up the performance verification of the VLSI design flow, circuit parameters such as physical size, timing behavior, power consumption and RC parasitic information of the standard cells are defined in the standard cell library for usage in the design flow. Thus it is critical to model the information in the standard cell library accurately without increasing the data volume.

1.1.2 Standard cell library characterization:

Standard cell characterization is the process of extracting the standard cell information and developing the standard cell library model for design analysis. The library models are developed for fundamental building blocks such as INVERTER, BUFFER, NAND, NOR, XOR, AOI, OAI, adder bit cells, sequential elements such as latch, registers and SRAM bit cells. The method by which the standard cell information are extracted, defines the accuracy of the fundamental building blocks in the standard cell library.

The timing information of the standards cells is stored in a non-linear table look up (TLU) format as shown in Figure 1.3. The timing details of the standard cells are characterized with the assumption of single input switching (SIS) criteria, where only the primary input switches at a time in arriving the cell delay for output rise or fall conditions, while the secondary inputs are settles to its final state. Figure 3 demonstrates a the non-linear TLU of 2-input NAND gate for a set of four input transition time values and three output load values for output fall case with respect to input in1 low to high condition, where in2=V_{dd}. The same

approach is extended for output rise case and for cell delay with respect to in2 as well.

Also the traditional static timing analysis (STA) flow used for critical path analysis, models the essential design parameters such as setup and hold constraints of the sequential elements in a table lookup format. Such table lookup models are characterized for extreme PVT (process, voltage, temperature) corners [47-48] under worst case state vectors using dynamic SPICE level simulations. Similarly the entire model parameters such power look up table, capacitance and transition time limits that are required by the design flow, is captured in the library model.

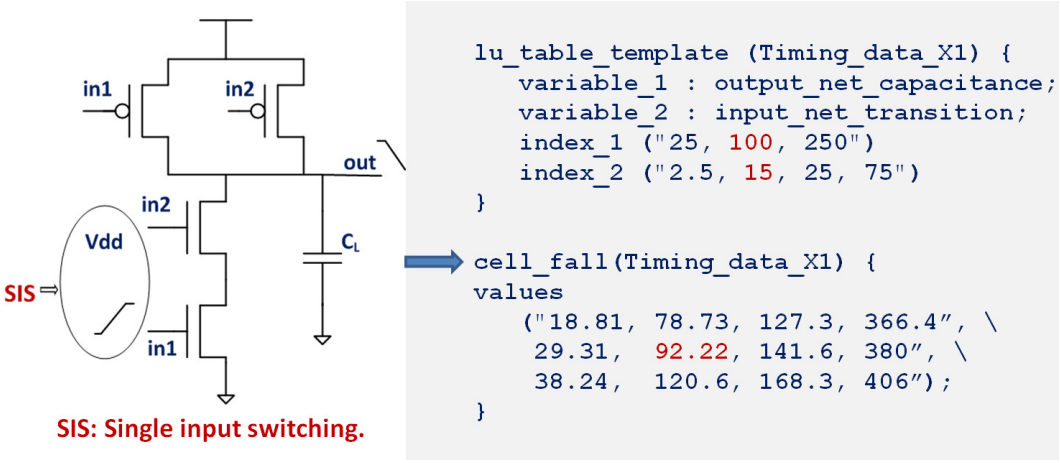

Figure 1. 3: Library characterization of NAND2 output fall delay

1.2 Impact of Static Variation

1.2.1 Modeling of process variation:

With the aggressive scaling of the minimum feature size in CMOS technology, semiconductor manufacturing is more and more constrained by the lithography process, especially when the Critical Dimensions (CD) are getting

much smaller than the optical wave length. Due to the sub-wavelength lithography process, the gate shape of a device is distorted at the gate edge and the end of the gate, which is referred to as non-rectangular gate (NRG) effect, as illustrated in Figure 1.4.

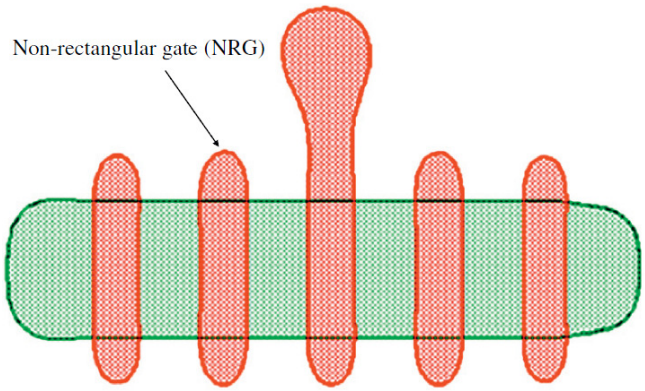

Figure 1. 4: Impact of lithography on layout [4-5]:
Post-lithography aerial image of the gate and diffusion showing NRG.

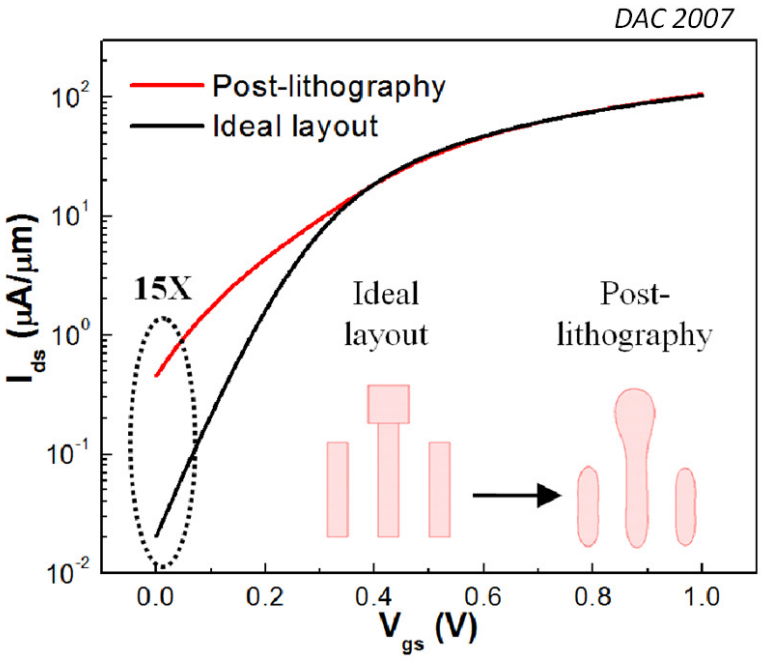

Figure 1. 5: Impact of lithography device performance [6-7]:
Dramatic leakage increase due to the lithography effect.

Such an effect inevitably induces a significant impact on CD variations in scaled CMOS, contributing to ever-increased leakage and performance margining. As illustrated in Figure 1.5, the NRG effect may increase sub- threshold leakage by more than 15X from that of an ideal physical layout at 65 nm technology node. In the worst case, the shortening of gate end may even cause device failure (Figure 1.4). The product yield also suffers from this effect as the lithography process causes pattern bridging for features with tight space, pinching effects for the isolated features and edge placement errors.

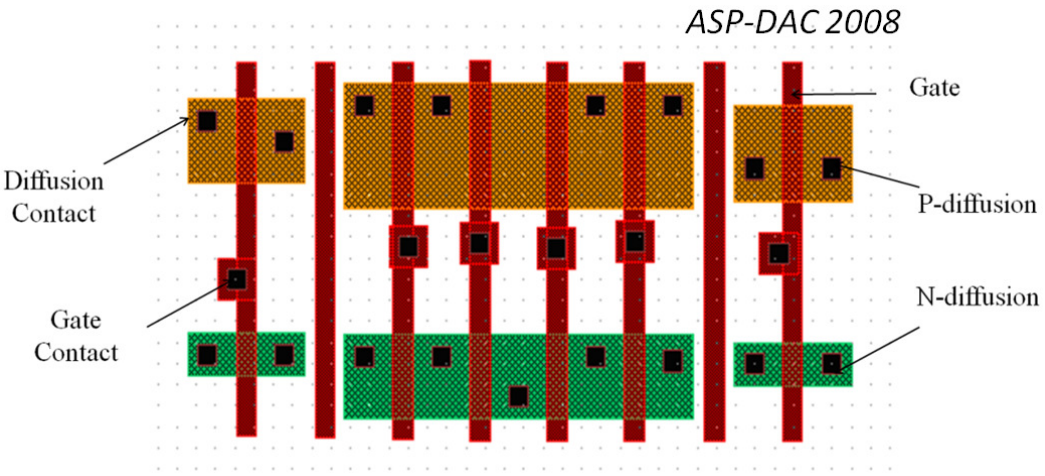

Figure 1.6 (a): Regular Layout of XOR gate [4-5].

Thus regular layout that follow restrictive design rule (RDR) as shown in Figure 1.6 (a) are essential to robust CMOS design in order to alleviate manufacturing induced effect, such as the effect of NRG due to sub-wave length lithograph. To mitigate such a penalty, optimizing the regular layout through RDR parameters helps benchmark the post-lithography circuit performance. More

than 70% reduction in leakage can achieved with area penalty of ~10% and 9–12% overhead on circuit speed and active energy [4-5] using the layout optimization flow for standard cells as described in Figure 1.6 (b).

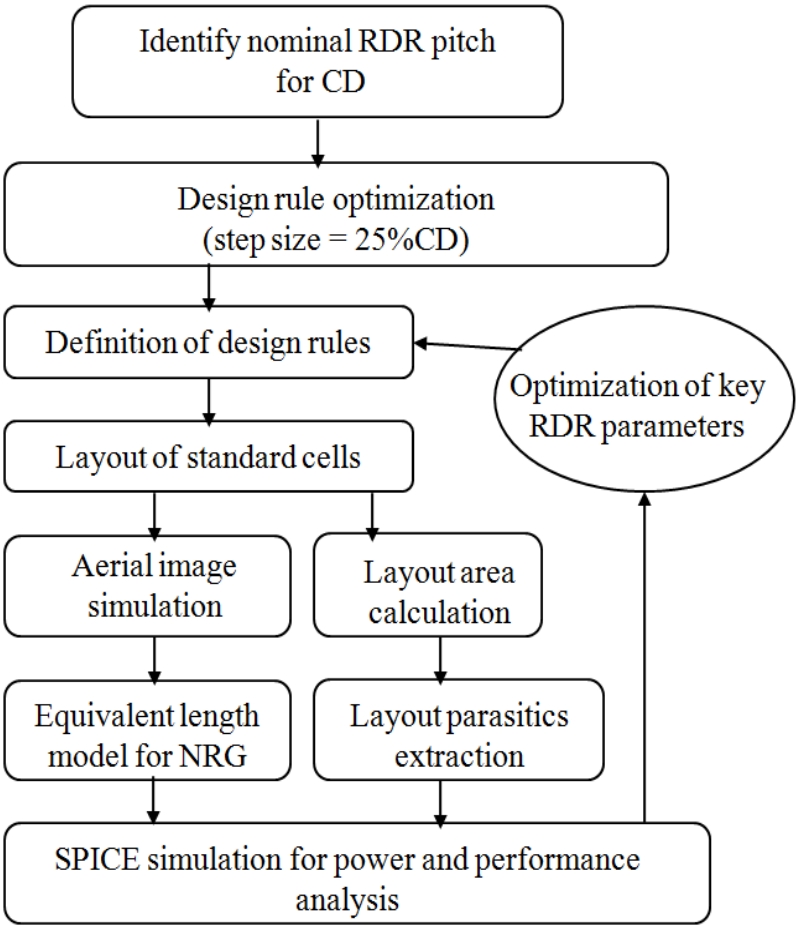

Figure 1.6 (b) : Flow diagram for regular layout optimization [4-5].

1.2.2 Gate timing under static variation:

CMOS scaling has led to increasingly high variability in device and circuit performance due to variation in device width, length threshold voltage and variation in oxide thickness etc as shown in Figure 1.7.

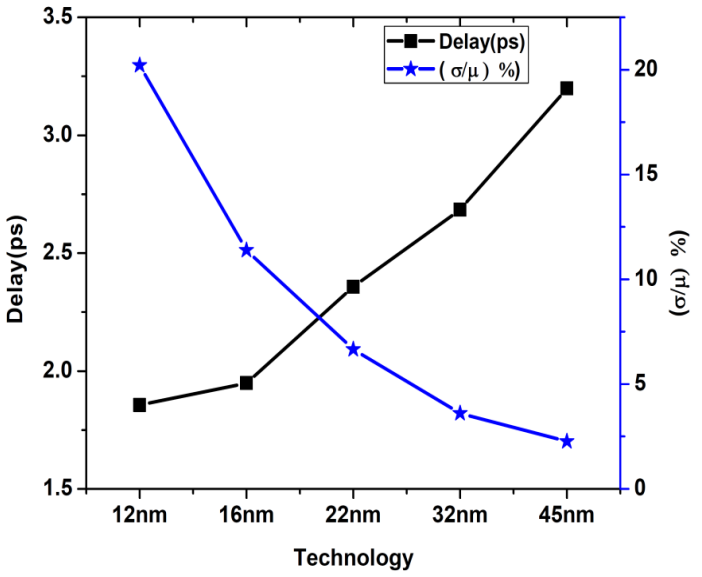

Figure 1. 7: Gate delay variation under technology scaling.

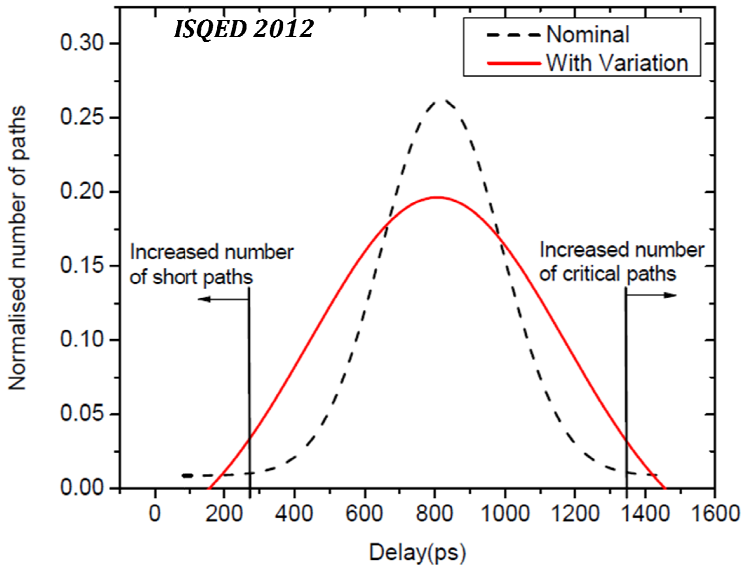

Figure 1. 8: Path delay under gate delay variation [8]

To improve design robustness, it is important to consider variation in the design flow as the number of setup and hold timing violations are more compared to nominal condition while accounting for variation in the standard cells as shown

in Figure 1.8. Static variation account for variation upto ~15% of the nominal performance.

1.3 Variation under Dynamic Operation

In addition to static variations described in Section 1.2, dynamic variations such as cross talk noise due to interconnect parasitic, skew variation due to voltage jitter and multiple input switching (MIS) effect due to the temporal proximity of relative arrival time (RAT) of the input signals in multiple input gates impact the circuit performance as well. The effect due to cross talk noise is usually handled by miller factor and skew variations are accounted through uncertainty parameter in the design flow. The components of variations due to dynamic operations are demonstrated in Figure 1.9.

The traditional standard cell library used by STA design flow assumes single input switching (SIS) scenario and do not account for the effect of MIS. Integration of existing MIS delay models into design flow is still a question.

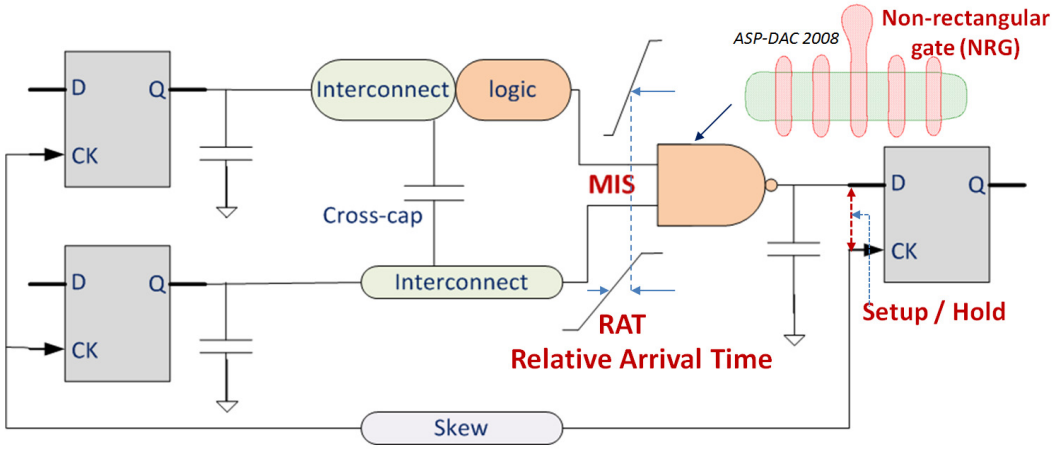

Figure 1. 9: Source of variations in circuit performance

1.4 Previous Work

Process variation has been handled using restrictive design rules (RDR) and regular layout structures for physical design [4-5]. Non-rectangular gate effect due to process variation is included in the design flow using equivalent gate length model [6-7]. Static variations caused by the fabrication process in device width, device length, threshold voltage and oxide thickness, etc are analytically modeled for combinational gates in standard cell library [8]. Variation due to interconnect coupling [9] is effectively handled by the use of miller factor. The un-certainty due to voltage jitter [10] is well accounted through programmable delay buffers in the clock network. Various modeling techniques have been developed to account for process variation through manufacturing aware physical layout design and resolution enhancement technique [11-20] without accounting for MIS effect. Compact variation aware standard cell model is developed in [24] to account for process variation including MIS effect, which applies complex waveform generation method and lacks integration of MIS effect into STA flow. Statistical timing models including, spatial correlation is studied by [25] which applies heuristic method to select the arrival time of propagated signals to consider MIS. Method to improve the accuracy of STA is proposed in [26] at the expense of computation cost.

Modeling techniques for analyzing the effect of MIS include: statistical timing analysis using MIS is studied in [27-28], which involves coefficient extraction through multiple SPICE simulations to analyze the sensitivity of RAT on the delay; MIS effect with and without signal transition time is explored in [29] that

requires extensive SPICE simulation for standard cell library characterization; a theoretical frame work has been developed in [30] for statistical STA considering coupling noise and MIS, but does not discuss any solution to speedup the simulation; delay variation due to transistor stack is analyzed by [31] from charge and path-resistance point of view, which does not integrate MIS effect into design flow. Depending on the granularity of RAT between the signals, these SPICE simulation based approaches are computationally intensive.

Complicated algorithm based MIS model has been developed in [32] without accounting for the variability of signal slope. Analytical model is proposed in [33] based on SIS delay in standard cell library and fitting constants derived from minimum amount of MIS characterization. Polynomial approximation based MIS analysis is presented in [34], which requires large combination of SPICE simulation for coefficient extraction. Equivalent inverter model with complicated input mapping algorithm is studied in [35]. Multi-port current source model is developed by [36] which is computationally expensive with high data volume due to the use of the current source model. Thus, there is a need for fast characterization methodology for multiple input logic gates in the standard cell library with efficient computational resources. And the integration of MIS variation into design flow is required for faster design closure without trading off the accuracy.

Due to high speed design and process variation [37] caused by scaling of technology node, the probability of MIS occurrence within a clock cycle is high. MIS variation is observed to be significant for signal paths with lower number of

stages [28] and is prominent at fast operating condition (i.e.) fast process, voltage and temperature (PVT) corner, suggesting that MIS potentially impacts hold violations in the synchronous design resulting in chip failure. On the other hand, for the traditional STA flow, the design performance is pessimistically analyzed under variation using multiple STA at crucial PVT conditions [38-39]. Where as, the computation cost of SPICE level simulation, for the characterization of setup and hold time constraint of the sequential cells is extremely high [40], due to the application of binary search mechanism for identifying the failure criteria. Due to process shrink, more PVT corners are required for design verification, resulting in high computation cost. On the other hand, the statistical timing analysis such as Monte Carlo method and statistical STA are time consuming due to the application of various trial simulations and usage of complicated algorithms [38-39] for analyzing the 3σ variation in the design.

Various techniques have been developed to reduce the pessimism of setup and hold time characterization in STA [2] by exploiting the failure criteria and using the interdependent behavior of setup and hold times [41]. Very few studies have been performed to improve computation cost for the characterization of setup and hold time such as, the algorithm based technique studied in [40] for independent and inter dependant setup and hold time characterization for latches and registers. Thus there is a need for simplified method of characterization of the setup and hold time for sequential element with less computation cost and without trading off accuracy.

1.5 Proposal

A finite-point based analytical model is proposed for efficient characterization of MIS effect for multiple input gates in the standard cell library with less computational resources. Similar approach is extended for the characterization of setup and hold time of sequential elements in the standard cell library. The characterization method is demonstration using 2-input NAND gate and extended for 2-input NOR gates and 3-input NAND gate respectively. Similar approach can be extended for other multiple input gates in the standard cell library as well.

The proposed characterization methodology is validated using benchmark circuits in 45nm technology. Post-layout SPICE netlist from NANGATE library [NANGATE], device model and interconnect information from predictive technology model [PTM] as well as realistic waveform from active driver with 20-80% V_{dd} for the input transition time and active load with multiples of FO4 devices are used for validation. The characterization methodology is further validated using fast and slow operating conditions for wide range of input transition time and output load respectively. The proposed models of MIS effect is integrated into STA flow and validated for selective benchmark circuits including ISCAS family.

Experimental results show significant reduction in runtime with less than ~10% error compared to that of SPICE simulation data.

CHAPTER 2

ANALYSIS OF MIS EFFECT

2.1 Multiple Input Switching

2.1.1 Gate delay under MIS

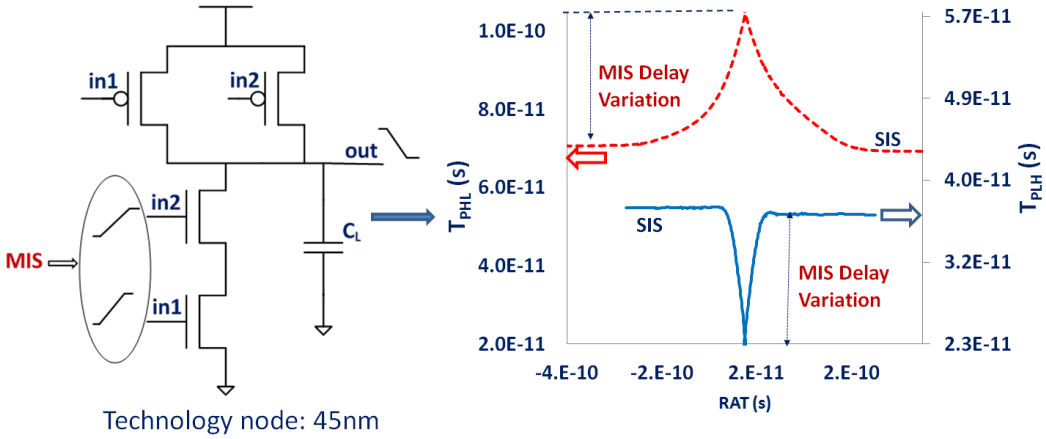

Figure 2. 1 : MIS variation of 2-input NAND gate

Due to high speed design and process variation, the probability of MIS occurrence within a clock cycle is high. As the RAT gets shorter, the gate delay due to temporal proximity of MIS can vary from 15%-50% compared to that of SIS scenarios used in the characterization of standard cell library. Figure 2.1 shows the MIS induced delay variation for a 2-input NAND gate in 45nm technology node for output rise and fall conditions. When RAT=0, the variation due to MIS is the worst case for that particular input condition. Thus it is important to account for the proximity effect of MIS into design flow for delay calculation.

2.1.2 Scaling trend of MIS

The MIS induced variation is similar or more due to technology scaling. For the same input condition for a 2-input NAND gate, the delay variation due to MIS with scaled CMOS technology is shown in the Figure 2.2. The delay variation due to MIS gets worst for high to low transition compared to SIS delay and the delay variation due to MIS gets better for low to high transition compared to SIS delay respectively. This suggests that the MIS variation can potentially impact the setup and hold time of the critical paths.

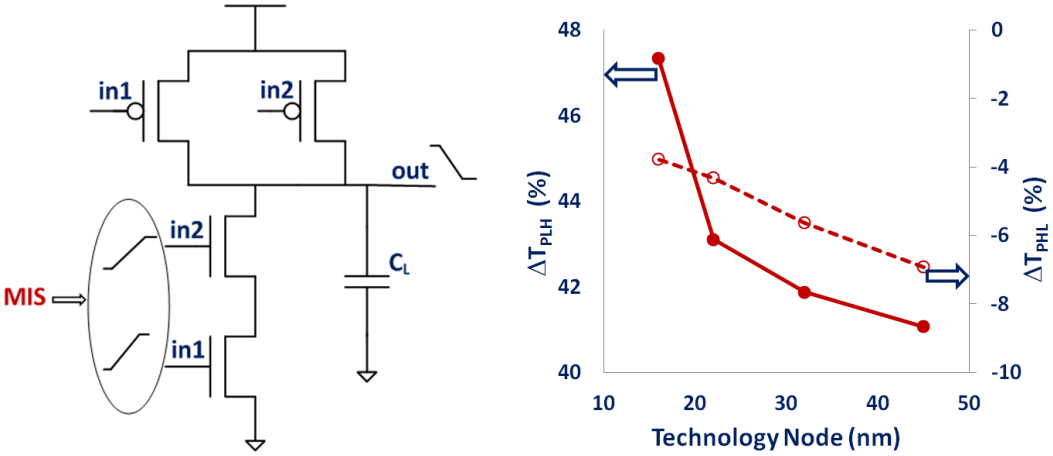

Figure 2. 2 : MIS variation with technology scaling

2.1.3 Problem of MIS characteristic

Figure 2.3 shows the impact of MIS variation on critical paths. It is observed that the ISCAS C432 with 17 logic gates in critical path has only 2% variation due to MIS induced in the middle stage of the critical path. Where as ISCAS C17 circuit with three logic gates in critical path has MIS variation of about 10%-20% for output rise and fall conditions respectively. This suggests that

short paths such as that in SRAM decoders have high probability of such MIS variation.

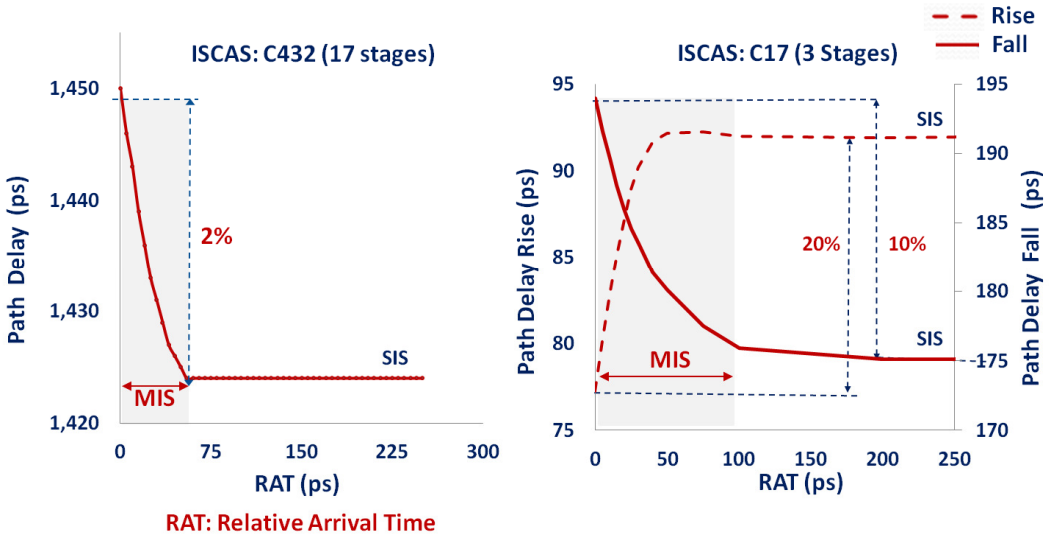

Figure 2. 3: Impact of MIS variation on critical path

2.1.4 MIS under process variation

The effect of MIS under process variation is shown in Figure 2.4. The switching window of a stage is calculated from the difference between SIS delay and MIS delay due to proximity effect of the input signals in a particular gate. The early and late arrival time of the switching window is defined by the best case and worst case delay of the SIS and MIS condition of the stage. The switching window is propagated to the next stage by accounting for all the proximity effect of the multiple input gates. As the number of stages increase the difference between the early and late arrival time of the signal gets widen until another close proximity effect occurs in the critical path.

Figure 2.4 shows effect of process variation on in addition to MIS effect. The FAST PVT (process, voltage and temperature) corner has the narrow window across all stages suggesting that MIS is prominent in the FAST corner and will result in more hold violations during critical path analysis. Thus it is necessary to account for MIS variation during design flow.

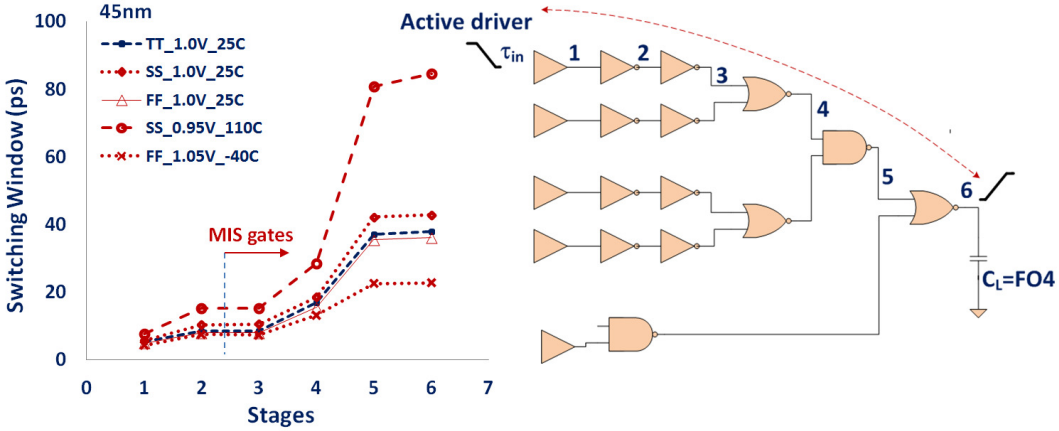

Figure 2. 4: MIS effect under process variation

CHAPTER 3

MODEL DEVELOPMENT

3.1 MIS Modeling Strategy

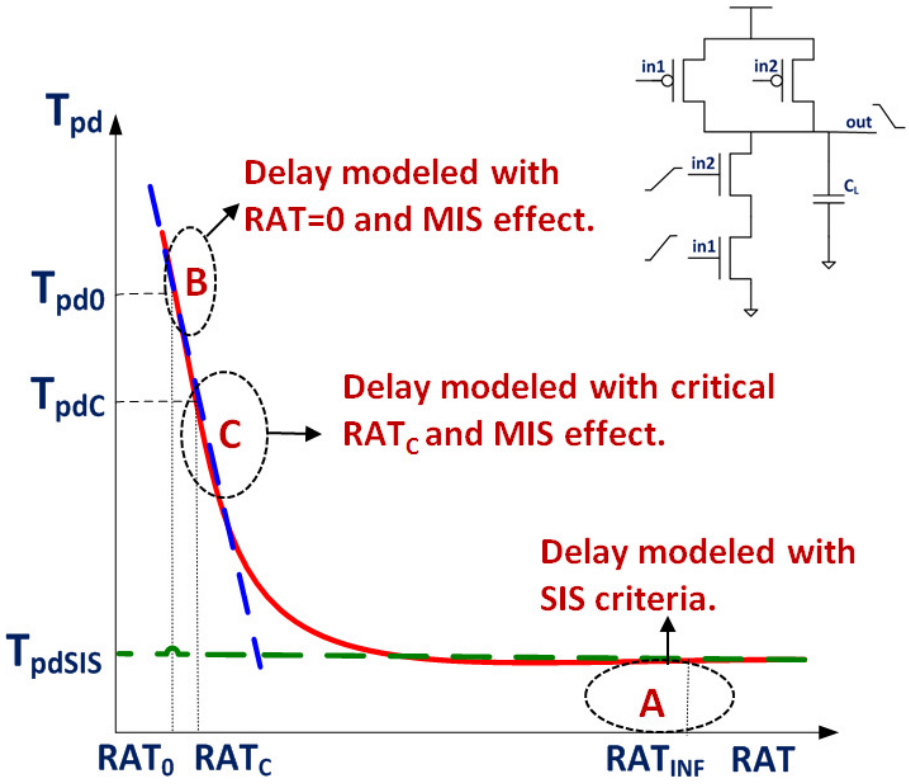

Figure 3. 1: MIS modeling principles

The modeling strategy is explained using 2-input NAND gate with both input switching from low to high as shown in Figure 3.1. The assumption here is that the bottom input in1 of the 2-input NAND gate is the lagging input meaning, it arrives later than the top input in2, which is considered as leading input. Similar approach is extended for input high to low transition of 2-input NAND gate and 2-input NOR gate with appropriate changes to device parameters. To first order

approximation, under different amount of RAT between two inputs, the propagation delay (T_{pd}) vs RAT curve can be constructed using three finite points A, B and C, as shown in Figure 3.1.

Point A: The delay at point A (T_{pdSIS}) is defined using SIS criteria with RAT=infinity (RAT_{INF}). Point A models traditional SIS delay.

Point B: The delay at point B (T_{pd0}) is defined using RAT=0 (RAT_0) condition and including MIS effect.

Point C: This is the critical boundary condition for MIS. The delay at point C (T_{pdC}) is defined using critical RAT=RAT_C and MIS effect. The detailed procedure to find RAT_C is discussed in the later section.

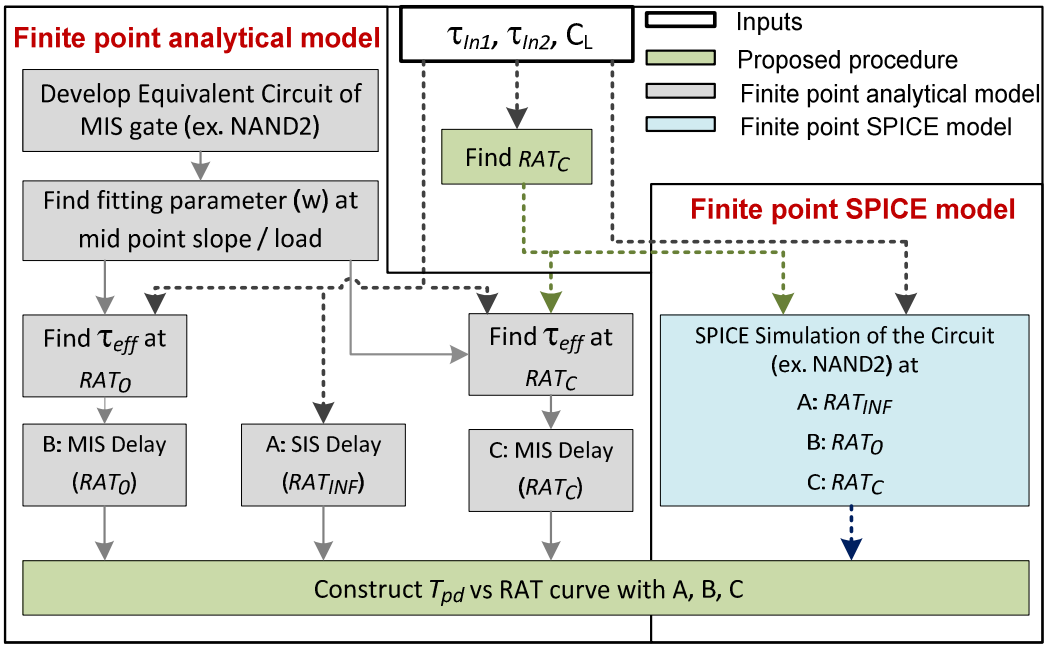

Figure 3. 2: Finite point MIS characterization flow.

Based on these three finite points, a piece-wise linear model can be generated to capture the transition of T_{pd} from Point A (SIS) toward the rapid increasing portion when MIS happens. In the case of input switching from high to low, Point A, B and C are found similar to the input switching from low to high case with the exception of PMOS device parameters are used in the model. And based on these three points, a piece-wise linear model can be generated to capture the transition of T_{pd} from Point A (SIS) toward the rapid decreasing portion when MIS happens. The flow diagram for finite point based characterization of MIS for a 2-input NAND gate is shown in Figure 3.2. Here τ_{in1} and τ_{in2} are the input transition time and C_L is the output load used for MIS characterization. Each steps involved in this flow diagram are discussed in detail as follows.

In general, the accuracy of the finite point model for characterization can be improved through usage of SPICE-based simulation or through other source of analytical delay models for finite points A, B, C, combined with the proposed procedure for finding critical boundary condition for RAT=RAT_C. Further, the accuracy of the finite point model can be improved by additional finite points. The procedure to identify optimal number of finite point is discussed in APPENDIX F. The same approach is extended for output rise condition of the 2-input NAND gate and for the delay characterization of 2-input NOR gate with changes to appropriate device parameters.

3.1.1 Definition of point A

The SIS delay at point A (T_{pdSIS}) is modeled using RAT_{INF}. The output voltage-current equation used for delay calculation is given by,

$$\frac{C_L . dV_{out}}{dt} = -I_D \tag{3.1}$$

where C_L is the load capacitance, I_D is the drain current, V_{out} is the output voltage and dt is the time step. The current equation used in equation (3.1) for the derivation of delay model is given as,

$$I_D = \begin{cases} 0 & (V_{in} \le V_t : cutoff), \\ K_l (V_{in} - V_t) V_{out} & (V_{out} < V_{dsat} : linear), \\ K_s (V_{in} - V_t) & (V_{out} \ge V_{dsat} : saturation) \end{cases} \tag{3.2}$$

where V_{in} is the input voltage, V_t is the threshold voltage, V_{dsat} is the drain saturation voltage at $V_{in} = V_{dd}$, K_s and K_l are the device parameter for saturation and linear mode respectively. In general, the propagation delay T_{pd} of a 2-input NAND gate can be expressed as,

$$T_{pd} = t_{vout} + t_{vx} - \frac{\tau_{in}}{2} \tag{3.3}$$

where t_{vout} is the time to discharge C_L to $0.5V_{dd}$, t_{vx} is the time to discharge the capacitance C_x of internal node x to its final value V_f and τ_{in} is the transition time for the switching input.

3.1.1.1 Boundary condition for fast and slow input

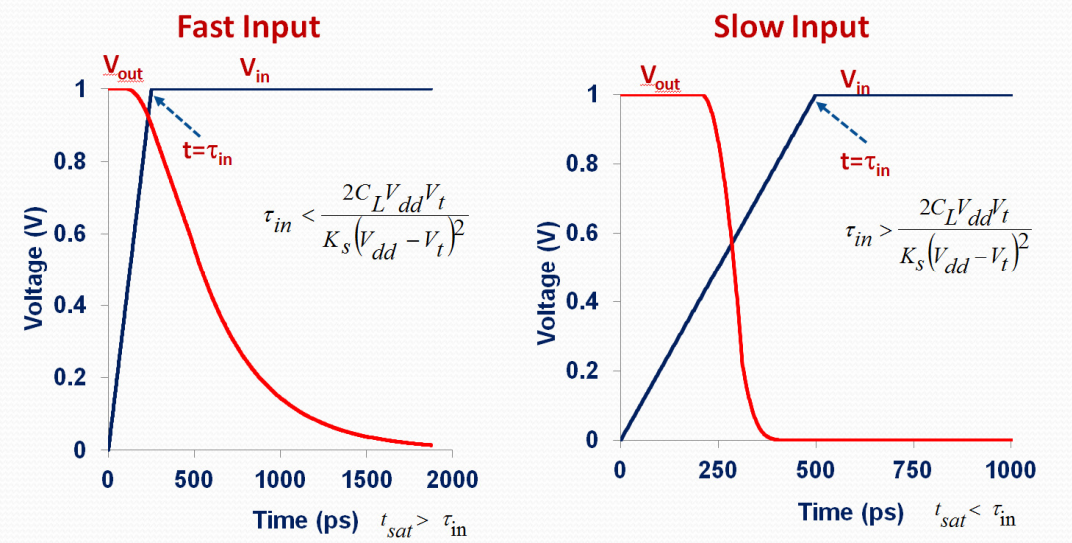

Figure 3. 3: Boundary condition between fast and slow input

In order to improve the accuracy of the delay model, t_{vout} is derived separately for fast and slow inputs respectively. The boundary condition between fast and slow input is shown in Figure 3.3. The detailed derivation is described in APPENDIX A. Consider the fast input where the time for saturation t_{sat} when $V_{out} = V_{in} - V_t$, is greater than the transition time τ_{in} of the input (i.e.) $t_{sat} > \tau_{in}$. For $0 < V_{in}-V_t < V_{out}$, the top transistor is saturated and the input is still a ramp. In such case, the following differential equation can be constructed using saturation current equation in (3.2).

$$C_L \frac{.dV_{out}}{dt} = -K_s.(V_{in} - V_t) \tag{3.4}$$

Solving equation (3.4) for fast input and setting the output $V_{out} > V_{dd} - V_t$, the boundary condition for fast input is expressed as:

$$\tau_{in} = \frac{2C_L V_{dd} V_t}{K_s (V_{dd} - V_t)^2} \tag{3.5}$$

Using the same approach, the t_{vout} for fast input and slow input are derived with the following response. The detailed derivation of t_{vout} is shown in the APPENDIX B and APPENDIX C respectively.

3.1.1.2 Delay model for fast input

Fast input: t_{vout}

$$\begin{aligned}
&t < \tau_{in} && t_{vout} = \left[V_{dd} \sqrt{\frac{C_L}{K_s \tau_{in}}} + V_t \right] \frac{\tau_{in}}{V_{dd}} \\
&\tau_{in} < t < t_{sat} && t_{vout} = \tau_{in} + \frac{C_L}{K_s (V_{dd} - V_t)} \left[0.5 V_{dd} - \frac{K_s \tau_{in}}{2 C_L V_{dd}} . (V_{dd} - V_t)^2 \right] \\
&t > t_{sat} && t_{vout} = \tau_{in} \left(1 - \frac{1}{2} \left(1 - \frac{V_t}{V_{dd}} \right) \right) + \frac{C_L V_t}{K_s (V_{dd} - V_t)} + \frac{C_L}{K_l (V_{dd} - V_t)} \left[0.6931 + \ln \left(1 - \frac{V_t}{V_{dd}} \right) \right]
\end{aligned} \tag{3.6}$$

3.1.1.3 Delay model for slow input

Slow input: t_{vout}

$$\begin{aligned}
&t < t_{sat} && t_{vout} = \left[V_{dd} \sqrt{\frac{C_L}{K_s \tau_{in}}} + V_t \right] \frac{\tau_{in}}{V_{dd}} \\
&t > t_{sat} && t_{vout} = \frac{\tau_{in}}{V_{dd}} (V_1 + V_t) + \frac{C_L}{K_l (V_{in} - V_t)} \left[\ln \left(\frac{0.5 V_{dd}}{V_1} \right) \right] \quad Where\ V_1 = \frac{C_L V_{dd}}{K_s \tau_{in}} \left(1 \pm \sqrt{1 + \frac{2 K_s \tau_{in}}{C_L}} \right)
\end{aligned} \tag{3.7}$$

3.1.1.4 Calculation of t_{vx}

The time taken to discharge the internal node x from its initial value $V_{dd} - V_t$ to final value V_f is given by simple CMOS delay equation as shown below.

$$t_{vx} = \frac{C_x}{K_l (V_{dd} - V_t)} \ln \left(\frac{V_{dd} - V_t}{V_f} \right) \tag{3.8}$$

When the bottom transistor reaches V_t before the top one, t_{vx}=0. Also for slow inputs given to top transistor and when the top transistor reaches V_t before the bottom one, t_{vx} =0. For fast inputs, V_f is achieved at the end of the input ramp (V_{in} = V_{dd}) when the current ceases to increase. V_f is found by equating the saturation current for top device to the linear current of bottom device [35].

$$V_f = \frac{K_s\left(V_{dd} - V_t\right)}{K_l\left(V_{dd} - V_t\right) + K_s} \tag{3.9}$$

Where C_x is the internal node cap at node x.

3.1.2 Definition of point B

The MIS delay at point B is modeled using RAT_0 with equivalent gate modeling approach [34] as shown in Figure 3.4 (a) and Figure 3.4 (b) for a 2-input NAND gate and 2-input NOR gate respectively. The stacking effect and transition time effect are converted to equivalent single gate form. The definition of effective width, W_{eff} and the definition of effective transition time, τ_{eff} are defined as follows.

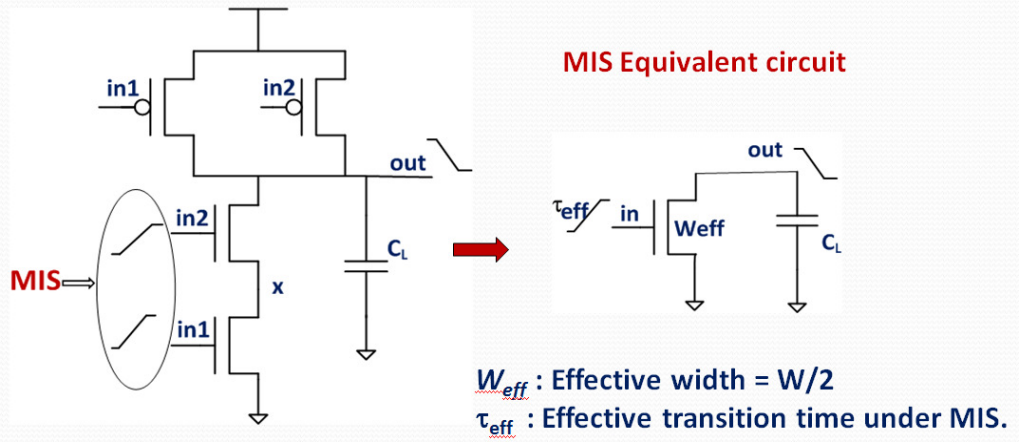

Figure 3.4 (a) : MIS equivalent circuit for 2-input NAND gate

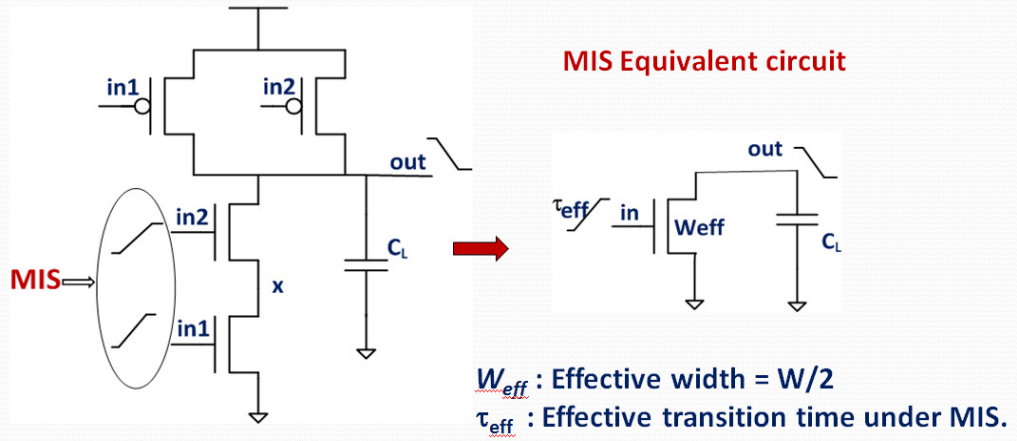

Figure 3.4 (b) : MIS equivalent circuit for 2-input NOR gate

3.1.2.1 Definition of effective width W_{eff}

For a 2-input NAND gate, considering the output fall scenario, when both input are switching from low to high, the W_{eff} is calculated as $W_N/2$, where W_N is the width of the NMOS transistor in the stack. Similarly for output rise scenario, when both input are switching from high to low, $W_{eff} = 2W_P$, where W_P is the width of the PMOS. When one of the input transitions from high to low, $W_{eff} = W_P$ assuming both the PMOS have same width.

3.1.2.2 Definition of effective transition time: τ_{eff} at RAT_0

The τ_{eff} is derived from the transition time values of in1 and in2 respectively with RAT_0 condition as shown in Figure 3.5.

The NMOS stack starts to conduct when the lagging input reaches V_t. The RAT between in1 and in2 defines the delay of the 2-input NAND gate. At RAT_0 the fastest input always lags. In Figure 3.5, V_C is the voltage level of the leading input (in2) when the lagging input (in1) is at V_t. [35]. This voltage level is used to

account for the MIS effect into τ_{eff} as shown below. Referring to Figure 3.5, the final τ_{eff} is defined as:

$$\tau_{eff} = w(t_e - t_s) \tag{3.10}$$

where t_s and t_e are the start time and end time of equivalent input respectively. The detailed derivation of t_s and t_e are discussed in APPENDIX D. w is the fitting parameter extracted from SPICE simulation at mid point slope and load values of characterization range at the nominal condition. The polynomial equation used in the fitting parameter is discussed in APPENDIX E. The MIS delay at point B is found using $\tau_{in} = \tau_{eff}$ in the delay model described for point A in Section 3.1.1.

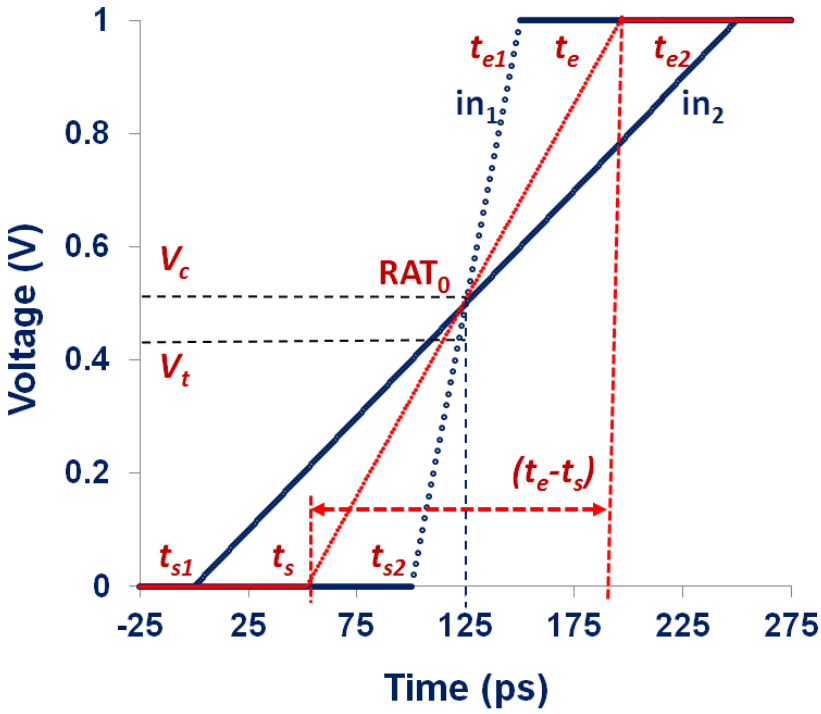

Figure 3. 5: Effective transition time of 2-input NAND gate at RAT_0

3.1.3 Definition of point C

The MIS delay at point C is modeled using RAT_C with equivalent gate modeling approach described for point B. Thus the equivalent circuit used for MIS delay at point C is same as in point B (Figure 3.4 (a) and Figure 3.3(b)). The procedure to find RAT_C is as follows.

3.1.3.1 Equivalent gate modeling for point C

The equivalent circuit used for MIS delay modeling is same as point B as shown in Figure 3.4. The definition of effective transition time τ_{eff} is discussed in the next section.

3.1.3.2 Definition of RAT_C

RAT_C is the boundary condition between the effect of MIS and SIS scenarios. Figure 3.6 describes the methodology for finding RAT_C. In Figure 3.6, RAT_{Crit} is the relative arrival time between two signals at which the leading input (that arrives earlier) is at V_t when the the lagging input starts to ramp. This condition is used because the proximity effect of the leading input is not significant beyond this point. Also the gate delay due to MIS occurs when RAT < 20% of the input transition time [28]. The delay sensitivity to input transition is non-negative and less than one [43]. Thus a sensitivity parameter is used to account for the slope effect of lagging and leading input in the definition of RAT_C as shown in denominator of equation (11). The final expression for the critical RAT_C is defined as.

$$RAT_C = \frac{V_t \frac{\tau_{lead}}{V_{dd}} + 0.5\tau_{lag} - 0.5\tau_{lead}}{1 + \frac{\tau_{lag}}{\tau_{lead}}} \tag{3.11}$$

where τ_{lag} and τ_{lead} are the transition time for lagging input and leading input respectively.

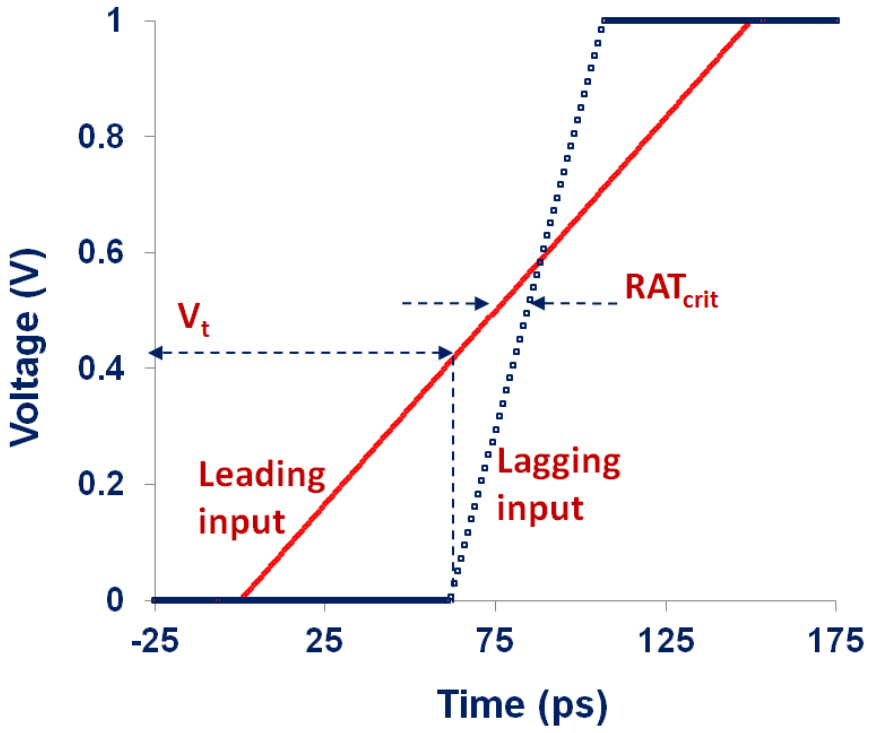

Figure 3. 6: Boundary condition between SIS and MIS effect

The procedure for finding critical RAT point at C using equation 3.11 is applicable for any source of delay model using MIS. Since the timing model for STA captures the slope from 20%-80% V_{dd} which is the linear portion of signal transition, the proposed procedure for RAT_C is valid for various operating

conditions. Additional modeling errors due to the linear approximation of input signal is absorbed by the fitting procedure of model parameters.

3.1.3.3 Definition of effective transition time: τ_{eff} at RAT_C

The definition of τ_{eff} at point C is similar to point B except RAT_C is used instead of RAT_0 as shown in Figure 3.7. The MIS delay at point C is found using $\tau_{in} = \tau_{eff}$ in the delay model described for point A.

The MIS delay at point C is found using τ_{eff} and the delay model described for point A.

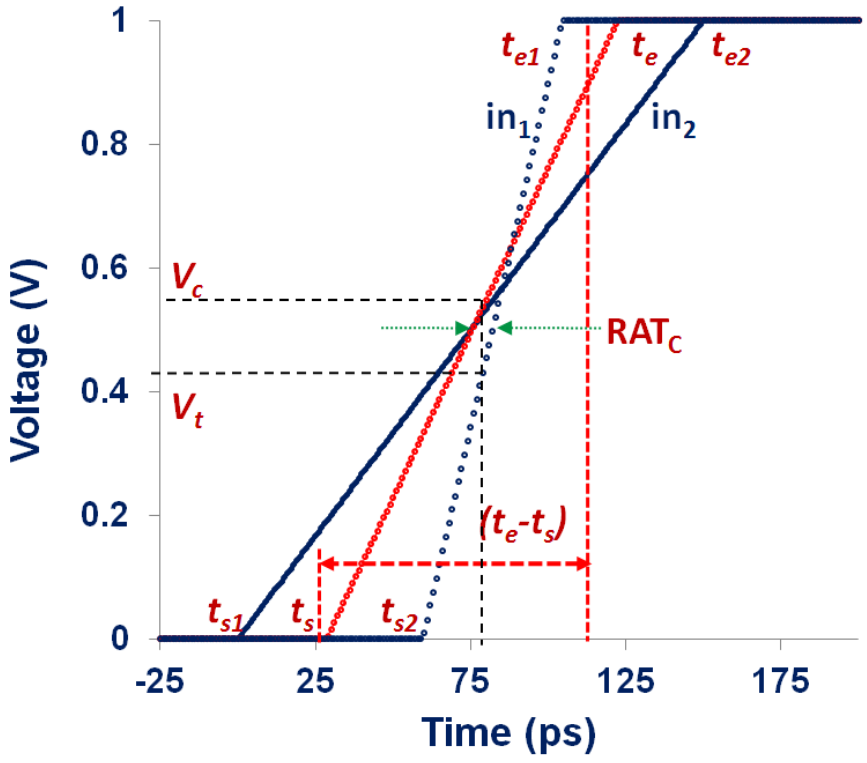

Figure 3. 7: Effective transition time τ_{eff} at RAT_C

3.1.4 Optimal finite point analysis for MIS model

The accuracy of the finite point MIS model can be further improved with additional finite points. The procedure for finding optimal number of finite point is discussed in APPENDIX F.

3.2 MIS Model for gates with more than 2 inputs

For inputs greater than 2, the probability of MIS occurrence is comparatively less, yet the effect is significant when it occurs. The same approach used in the case of 2-input NAND gate is extended for other multiple input logic gates in the library. The MIS modeling procedure for inputs > 2 is demonstrated using the 3-input NAND gate. For a 3-input NAND gate, the MIS variation is ~18% to ~55% for output TPHL and TPLH conditions respectively. The MIS effect is ~4% higher, when 2 of the 3 inputs are tied together and MIS occurs with the remaining input. The circuit diagram and the equivalent circuit used in the characterization of a 3-input NAND gate is shown in Figure 3.8.

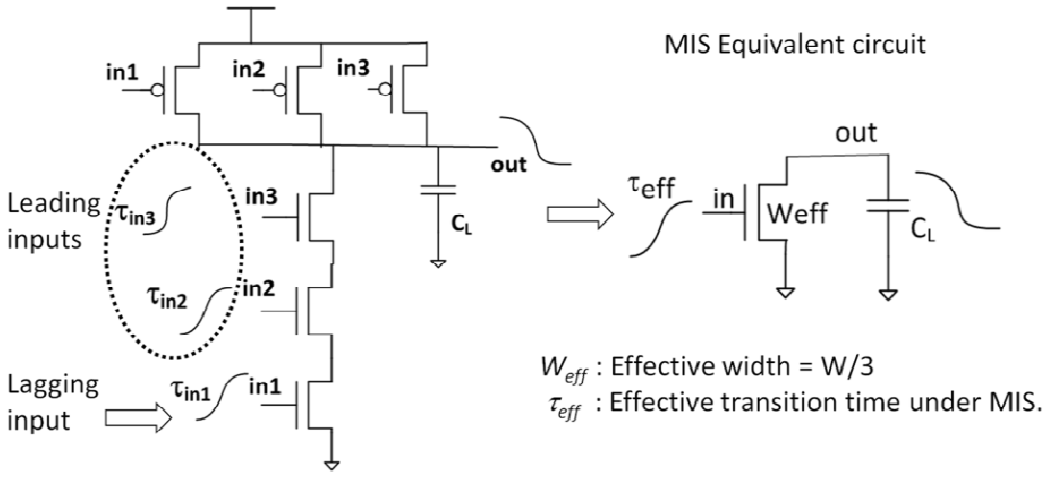

Figure 3. 8: Equivalent circuit of 3-input NAND gate

Consider the case when all three inputs are switching in the proximity as shown in Figure 3.8. The assumption here is that, in1 is the lagging input and in2 and in3 are leading inputs which arrives earlier than in1. The finite-points A, B and C are found as described in the following section and the delay versus RAT curve can be constructed similar to 2-input NAND gate.

3.2.1 Definition of point A

The SIS delay at point A (T_{pdSIS}) is similar to 2-input NAND gate except W_{eff} with appropriate stacking effect is accounted for the delay calculation.

3.2.2 Definition of point B

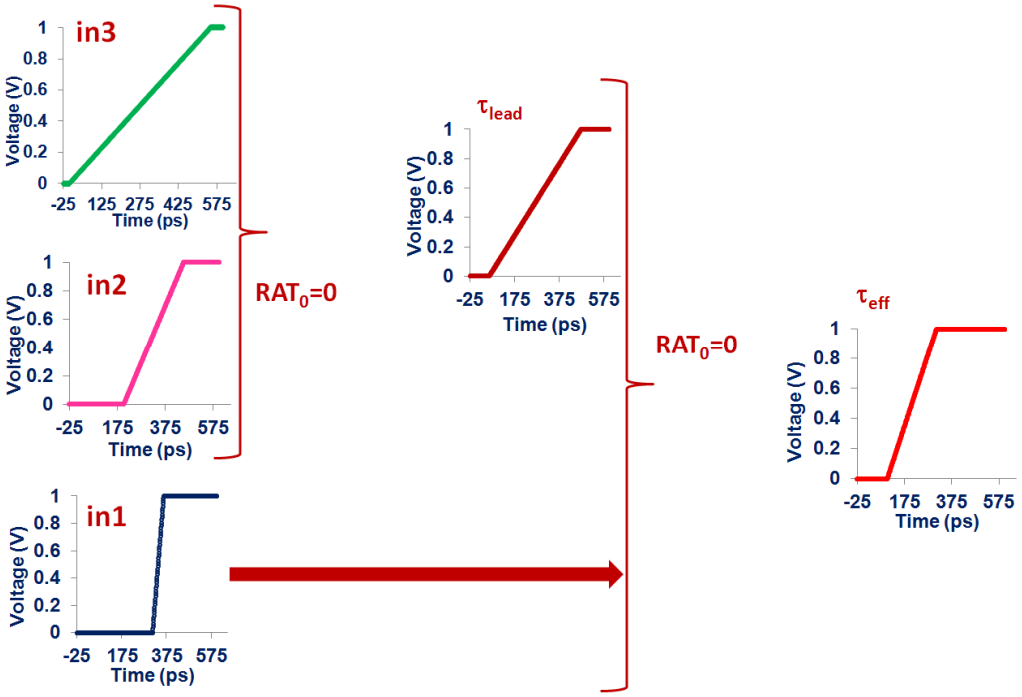

Figure 3. 9 : τ_{eff} of NAND3 at point B (RAT_0)

Delay at point B is found in two steps. First the effective transition time τ_{lead} for two leading signals in2 and in3 are calculated using RAT_0 condition. The final τ_{eff} is then calculated using τ_{lead} and the transition time of the lagging input in1 under RAT_0 condition for delay calculation. This approach is demonstrated for NAND3 in Figure 3.9.

3.2.3 Definition of point C

Delay at point C is found in two steps as well. First $RAT_{C(lead)}$ is calculated for two leading signals in2 and in3. The effective transition time of the leading inputs τ_{lead} is calculated using the $RAT_{C(lead)}$. Then the final RAT_C is found using τ_{lead} and the transition time of lagging input in1 and the final τ_{eff} is calculated for the delay model. This approach is demonstrated for NAND3 in Figure 3.10.

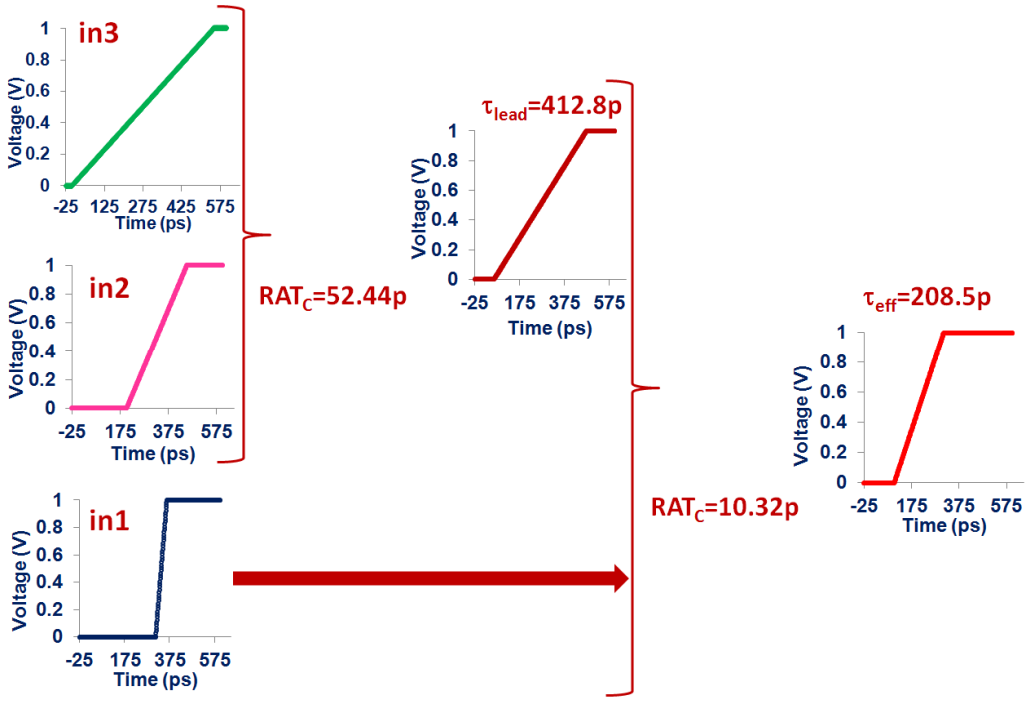

Figure 3. 10: RAT_C and τ_{eff} of NAND3 at point C

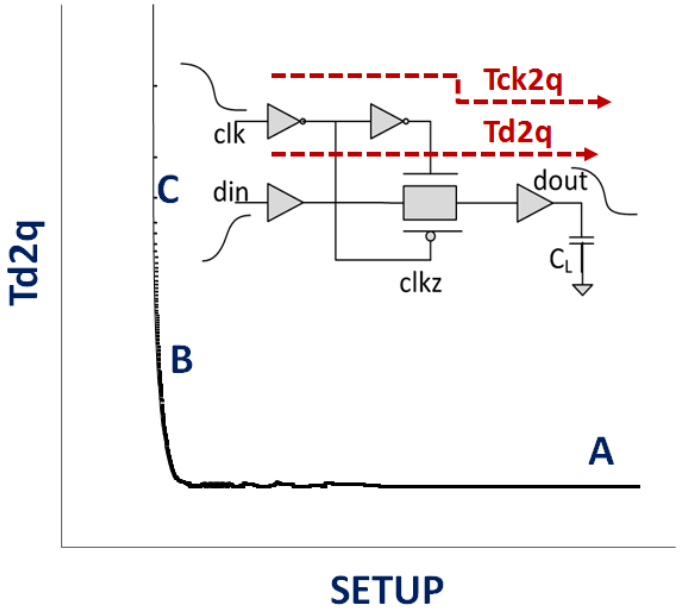

Figure 3. 11 : Setup time characteristic of dynamic latch

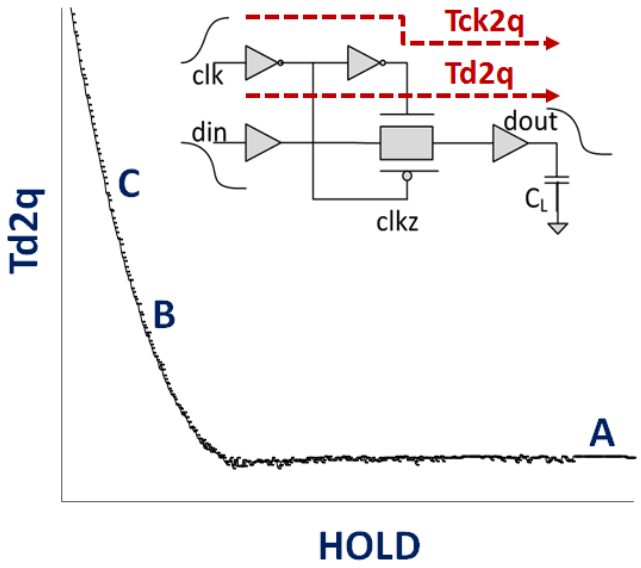

Figure 3. 42 : Hold time characteristic of dynamic latch

The finite point model is derived from the fundamental behavior of the dynamic latch. The setup time is defined as the time interval before the active

clock, when the data must be stable to meet the performance requirement of the design. Where as the hold time is the time interval after the active clock edge where the data must be held stable to meet the desired functionality of the design. In general, the setup and hold time behavior of a dynamic latch are as shown in Figure 3.11 and Figure 3.12 respectively.

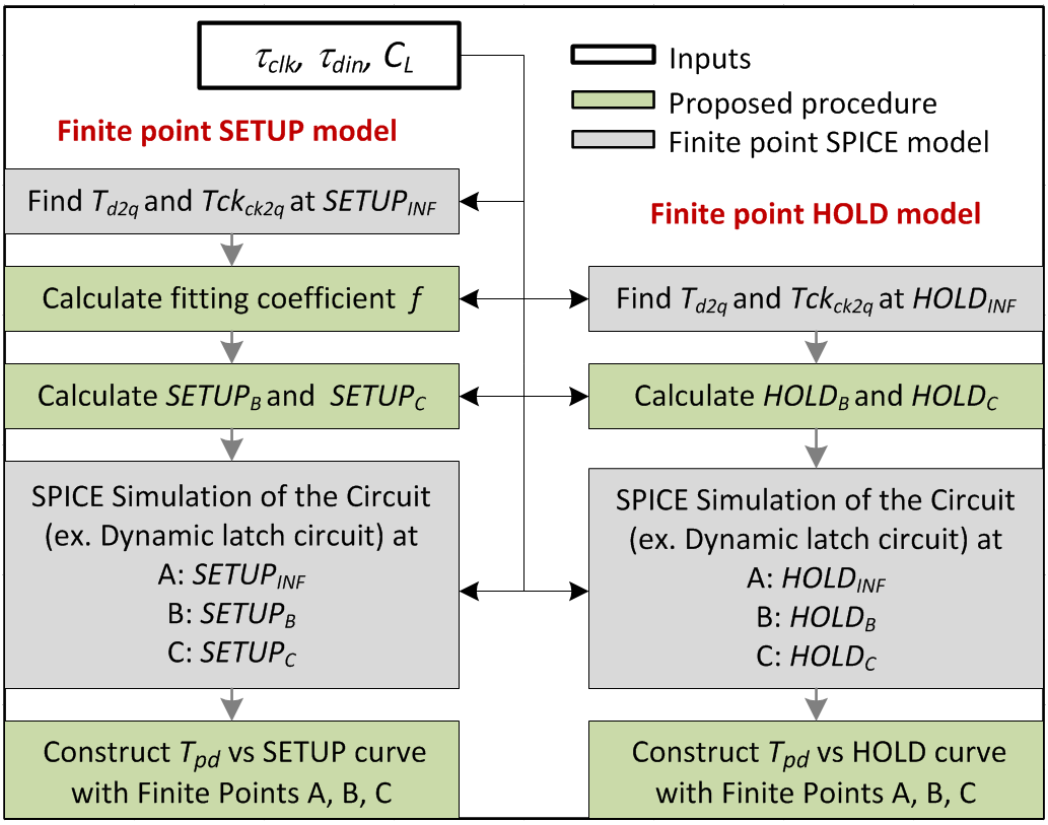

Figure 3. 13 : Finite point characterization flow for setup/ hold time.

To first order approximation the propagation delay (*Td2q*) from data input (din) to data output (dout) versus the setup / hold time curve can be constructed using three finite points A, B, C as marked in Figure 3.11 and Figure 3.12 respectively. The details of the finite point method based characterization for setup and hold time is discussed in the following section.

The accuracy of the finite point model can be further improved with additional finite points between A, B, C. All the finite points used in the construction of the characterization curve are found using the procedure for finding critical setup / hold time discussed in the later section. The flow used in the characterization of setup and hold time, using finite point method is shown in Figure 3.13. The details of each steps involved in the definition of the finite point method for the characterization of setup time and hold time are discussed in detail as follows.

3.3.1 Setup Time

From the behavior of the setup time characteristic as shown in Figure 3.10, the three finite points A, B, C are defined as follows.

3.3.1.1 Definition of Point A

The delay at point A ($Td2q_A$) is defined using infinite setup time ($SETUP_A$).

3.3.1.2 Definition of Point B

This is the boundary condition for the setup time, towards the rapid increasing portion of the delay from $SETUP_A$ in Figure 3.11. The delay at point B ($Td2q_B$) is defined using setup time ($SETUP_B$). The expression for $SETUP_B$ is given by,

$$SETUP_B = \left(T_{d2q} - T_{ck2q} \right)_A + \frac{f}{1 + \frac{\tau_{din}}{\tau_{clk}}} SETUP_{crit} \qquad (3.12)$$

where *Tck2q* is the propagation delay from clock (clk) to dout at point A and *Td2q* is the propagation delay from din to dout at point A, τ_{clk} is the transition time of clk and τ_{din} is the transition time of din respectively. The first term in equation (3.12) is used to account for the delay difference between the clock path and data path during setup time calculation. Figure 3.14 describes the procedure for finding $SETUP_{crit}$ used for the calculation of $SETUP_B$. In Figure 3.14, $SETUP_{crit}$ is the critical setup time during which din is at critical voltage $V_C = 0.75\ V_{dd}$, when the clk starts to close. This condition is used because the proximity effect of clock and data is not significant beyond this point and setup failure quickly occurs below this voltage level.

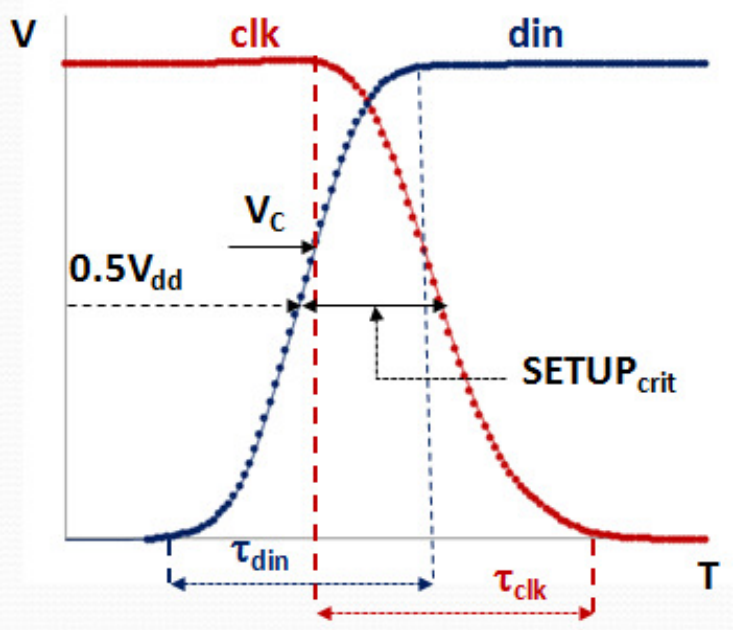

Figure 3. 14 : Procedure for finding critical setup time.

The final expression for $SETUP_{crit}$ is defined as,

$$SETUP_{crit} = V_C \frac{\tau_{din}}{V_{dd}} + 0.5\tau_{clk} - 0.5\tau_{din} \quad (3.13)$$

The delay sensitivity to input transition is non-negative and less than one [43]. Also the gate delay due to the proximity of multiple input switching occurs when the relative arrival time between two signals are less than < 20% of the input transition time [28]. Thus a sensitivity parameter is used to account for the slope effect of clk and din in the definition of $SETUP_{crit}$ as shown in denominator of second term in equation (3.12). The fitting factor f is to account for the device and circuit characteristics and is extracted from mid point slope and load condition for the characterization range. The detailed procedure for finding f is discussed in APPENDIX G.

3.3.1.3 Definition of Point C

This is the boundary condition for minimum setup time before setup failure. The delay at point C ($Td2q_C$) is defined using critical setup time ($SETUP_C$). The procedure for finding critical setup time $SETUP_C$ is similar to point B except $V_C = 0.5V_{dd}$ is used in equation (3.12). This condition is used as the setup failure most likely occurs beyond this point.

3.3.2 Hold Time

Similar to the setup time, the hold time characteristic can be constructed using the three finite points A, B, C as shown in Figure 3.12.

3.3.2.1 Definition of Point A

The delay at point A ($Td2q_A$) is defined using infinite hold time ($HOLD_A$).

3.3.2.2 Definition of Point B

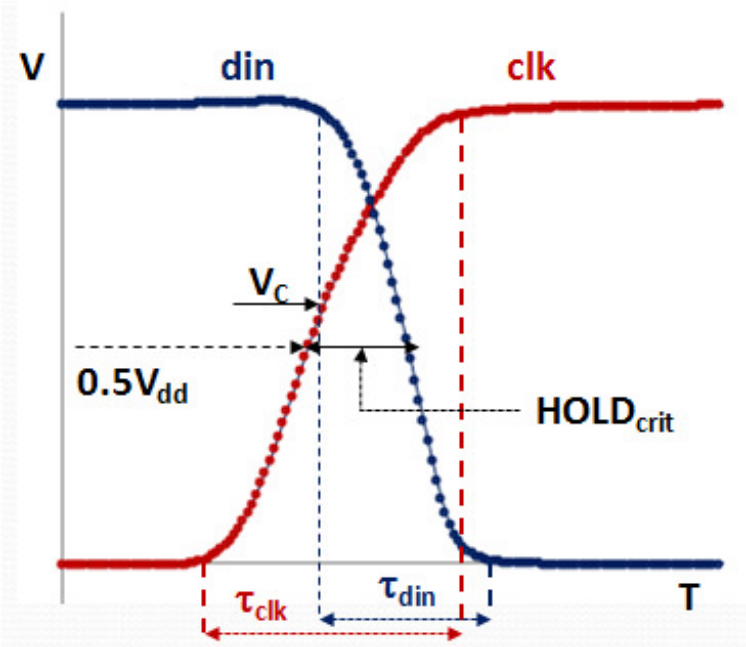

Figure 3. 15 : Procedure for finding critical hold time.

The definition of finite points B is similar to the setup time scenarios except the position of clk and din are as shown in Figure 3.15. The expression for $HOLD_B$ is given by,

$$HOLD_B = \frac{f}{1+\frac{\tau_{din}}{\tau_{clk}}} HOLD_{crit} \tag{3.14}$$

Figure 3.15 describes the procedure for finding $HOLD_{crit}$ used in equation (3.14). In Figure 3.15, $HOLD_{crit}$ is the critical hold time during which clk is at critical voltage $V_C = 0.75\ V_{dd}$, when the din starts to change its state. This condition is

used because the proximity effect of clock and data is not significant beyond this point. The final expression for $HOLD_{crit}$ is defined as,

$$HOLD_{crit} = V_C \frac{\tau_{clk}}{V_{dd}} + 0.5\tau_{din} - 0.5\tau_{clk} \quad (3.15)$$

Similar to the setup time model, a sensitivity parameter is used to account for the slope effect of clk and din in the definition of $HOLD_{crit}$ as shown in denominator of equation (3.14). The fitting factor f is defined to account for the delay difference between the clock path and data path during hold time calculation. Due to the behavior of the hold time characteristic shown in Figure 3.12, the fitting factor f can be simplified as f=1 when $Td2q < Tck2q$, f = -1 when $Td2q > Tck2q$ and f=0 when $Td2q = Tck2q$.

3.3.2.3 Definition of Point C

This is the boundary condition for minimum hold time before failure. The procedure for finding $HOLD_C$ is similar to point B except $V_C = 0.5V_{dd}$ is used in equation (3.15). This condition is used as the hold time is close to failure beyond this point.

3.3.3 Optimal Finite Point Analysis for Setup and Hole Time

The accuracy of the finite point model can be improved using few additional finite points. Irrespective of the number of finite points used in the model, the method for finding points A, B, C are similar for all cases as discussed in previous section. For additional finite points, V_C is varied from $0.5V_{dd}$ to V_{dd}

with the number of critical finite points of interest, excluding the values used for finite points A, B, C. Table 3.1 summarizes the V_C levels used in the definition of additional finite points. Using the similar approach, any number of finite points can be defined and the optimal number of finite points can be analyzed per design requirement.

Table 3. 1: Critical voltage levels V_C for additional finite point

Finite points	V_C for additional finite points in Eqn. (3.13) and Eqn. (3.15)
3	N/A
4	$0.85V_{dd}$
5	$0.65V_{dd}$; $0.85V_{dd}$
6	$0.6V_{dd}$, ; $0.7V_{dd}$; $0.85V_{dd}$; $0.95V_{dd}$
7	$0.6V_{dd}$, ; $0.7V_{dd}$; $0.85V_{dd}$; $0.9V_{dd}$; $0.95V_{dd}$

CHAPTER 4

MODEL VALIDATION

4.1 Model Parameters from Device

The extraction of the device parameters used in equation (2) is described in this section. The threshold voltage of the device V_t is extracted based on the I_d vs V_{gs} characteristic of the MOS device. The device parameter in saturated region K_s and linear region K_l are extracted based on the I_d vs V_{ds} characteristic of the MOS.

4.2 Circuit Simulation Setup

High performance predictive technology model [PTM] for 45nm CMOS devices and interconnects are used for circuit simulation using HSPICE. Post-layout standard cell library models (SPICE netlist) using 45nm technology from NANGATE library [NANGATE] is used for validation. ISCAS circuit with short path such as C17 is used for design flow validation. Realistic waveform from active CMOS gate driver with transition time of 20%-80% V_{dd} ranging from ~25ps to 500ps is used for the characterization. The load range used for the characterization is active CMOS gate load with fanout of FO4 to 50xFO4. Three sets of operating conditions were used for standard cell characterization to analyze MIS effect with PVT variations. The typical corner (nominal condition) is characterized using TT, 1.0, 25^{o}C. Fast corner is characterized at FF, 1.1V, 25^{o}C and slow corner is characterized at SS, 0.9V, 25^{o}C respectively. The fitting parameter w is found from nominal SPICE delay for mid point slope and load

condition, to account for the modeling approximation error due to device characteristics . The circuit parameters used in the circuit are: channel length L=45nm, NMOS width W_n=2L and W_p /W_n =2.25.

4.3 Benchmark Circuits

The bench mark standard cell circuits from NANGATE library [NANGATE] were used for the validation of finite point method for the characterization of MIS effect in multiple input switching gates include 2-input NAND gate, 2-input NOR gate and 3-input NAND gate respectively.

The proposed method for the characterization of setup and hold time is validated using various benchmark circuits in the standard cell library. The benchmark circuits used for the validation of finite point method used for the characterization of setup and hold time include: dynamic latch, static latch, pseudo static latch, TSPC latch, flip flop and SRAM bit cell.

Similar approach can be extended for any type of multiple input switching gate and sequential element in the standard cell library.

4.4 2-input MIS gates

4.4.1 MIS delay at RAT_0 (point B)

The nominal delay using finite point MIS delay model is compared against SPICE result for 2-input NAND gate for various input and output conditions of the characterization range as shown in Figure 4.1. Here $\tau_{in1,}$ output $\tau_{in2,}$ are the transition time for in1 and in2 respectively and C_L is the load capacitance at the

output. AT RAT_0, the model results are within 10% compared to that of SPICE simulation data. Similar approach is extended for 2-input NOR gates as well.

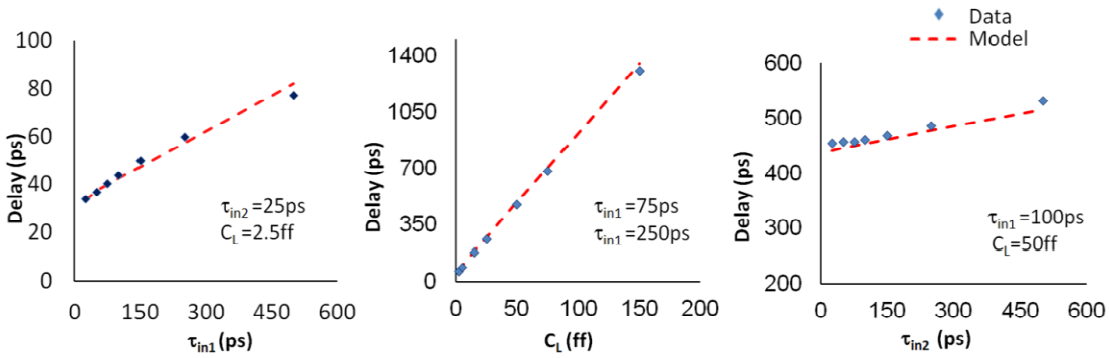

Figure 4. 1: Delay of 2-input NAND gate at RAT_0

4.4.2 Validation of RAT_C (point C)

For a 2-input NAND gate, the model predicted RAT_C is compared with nominal SPICE results as shown in Figure 4.2 for different values of τ_{in1}, τ_{in2}, and C_L conditions.

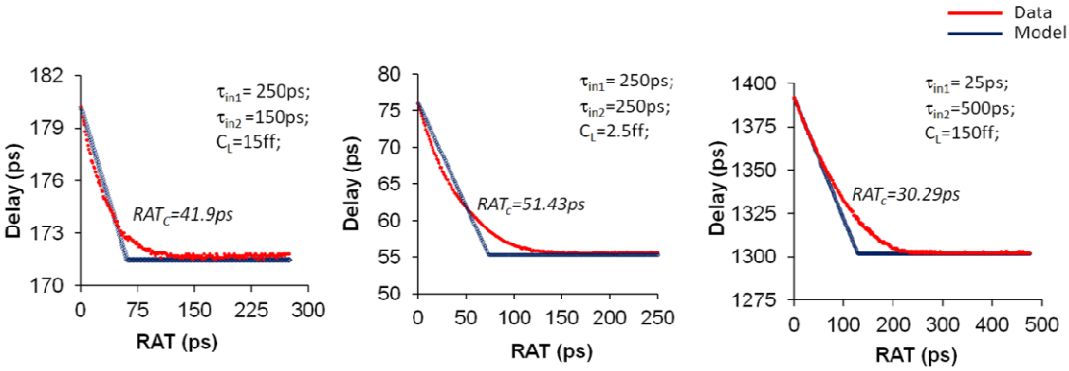

Figure 4. 2: Model vs. SPICE for RAT_C under nominal condition

Also the model predicted RAT_C for typical, slow and fast PVT corners are compared with SPICE result for output TPHL and TPLH conditions as specified in Figure 4.3. With the proposed RAT_C, model, the delay vs. RAT curve results are

in agreement with SPICE data as shown in Figure 4.2 and Figure 4.3 respectively. The same approach is extended for 2-input NOR gates as well.

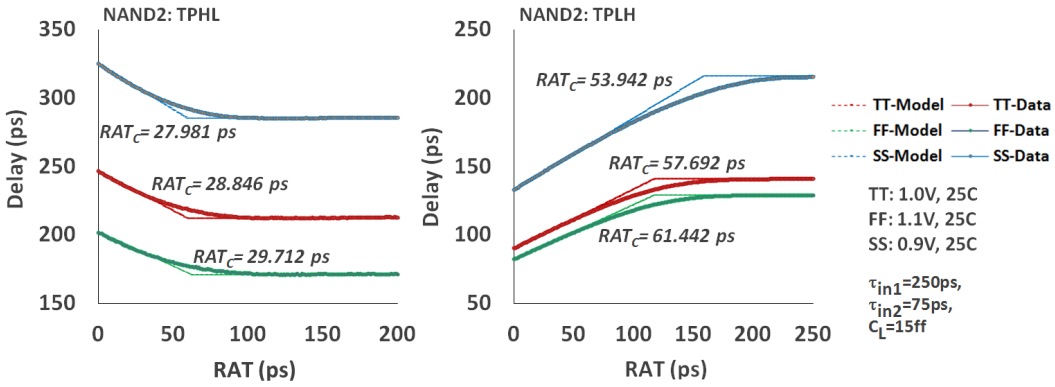

Figure 4. 3 : RAT_C Model vs SPICE for NAND2 at various PVT

4.4.3 Library characterization

The finite-point analytical model based characterization results, over the characterization range for Point A, B, C are shown in Figure 4.4 for 2-input NAND gate and Figure 4.5 for 2-input NOR gate respectively. At typical corner, approximately 343 test cases for various values of τ_{in1} x τ_{in2} x C_L were analyzed. The model results are within 10% compared to that of the SPICE simulation data.

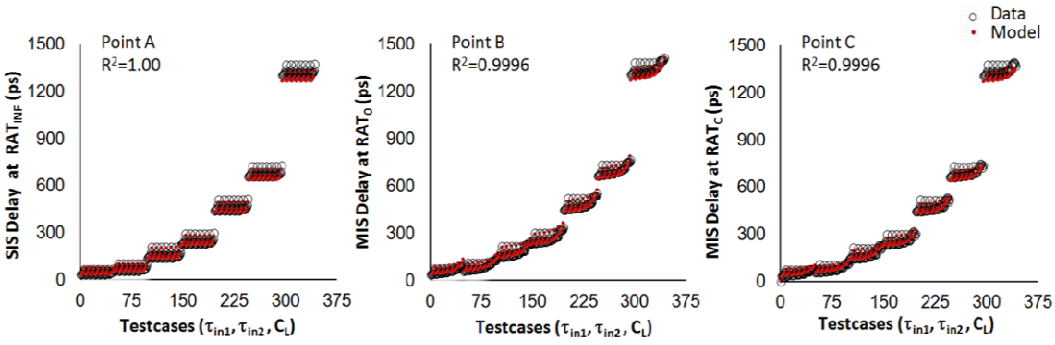

Figure 4. 4 : Library characterization for NAND2

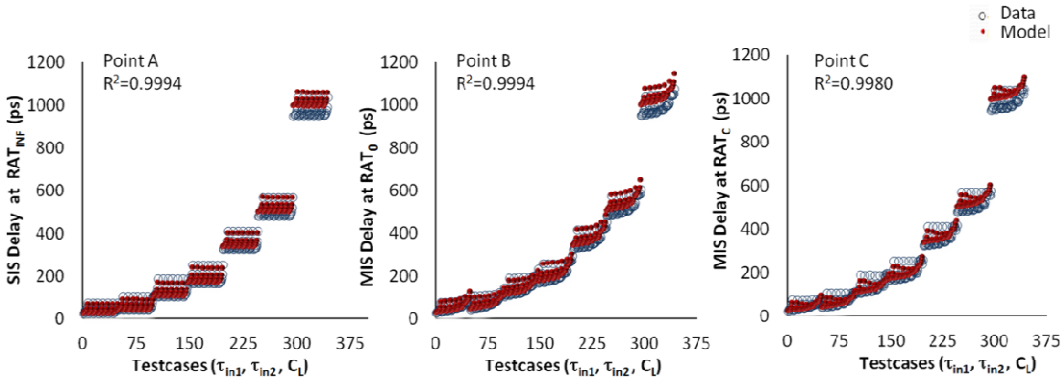

Figure 4. 5 : Library characterization for NOR2

4.4.4 Correlation to SPICE results

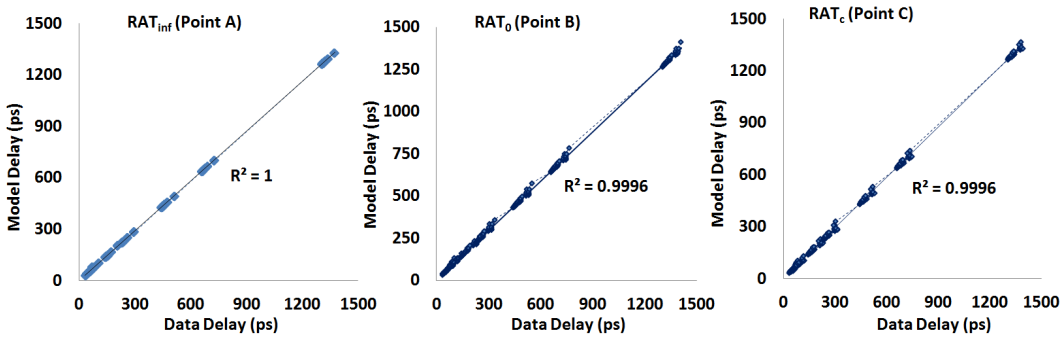

Figure 4. 6 : Correlation to SPICE results for NAND2

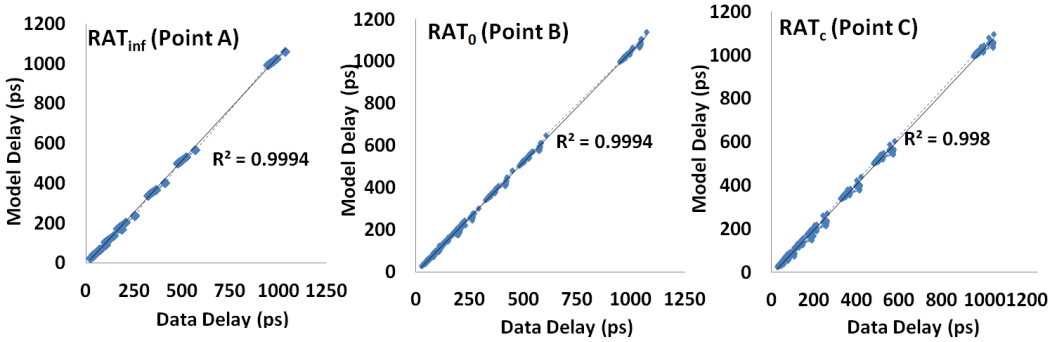

Figure 4. 7 : Correlation to SPICE results for NOR2

The root mean square error R^2 for finite-point approach based delay vs. SPICE simulation data is shown in Figure 4.6 for 2-input NAND gate and Figure 4.7 for a 2-input NOR gate respectively. For various combinations of τ_{in1}, τ_{in2}, C_L, over the entire range of characterization using 343 test cases, the R^2 error for point A, B and C are ~0.99.

4.4.5 Comparison of setup region

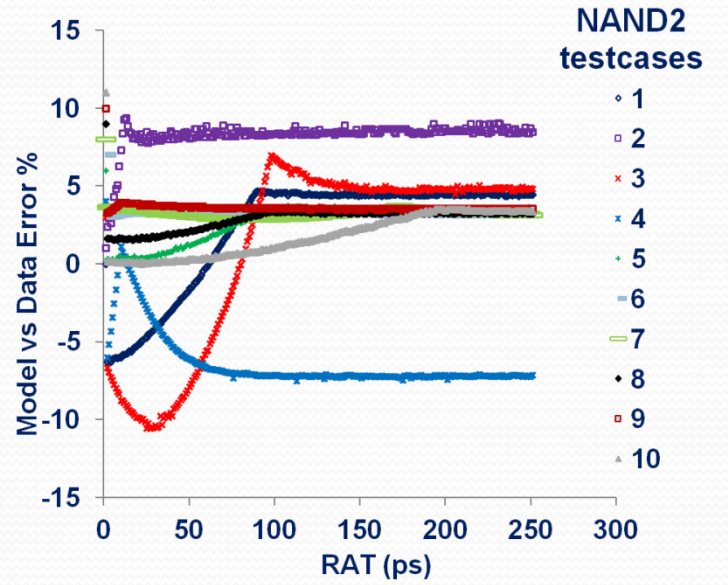

Figure 4. 8: Model vs SPICE for different RAT points

This analysis is performed in order to help analyze the setup region in case of sequential cell characterization method using finite point modeling approach. Model vs. SPICE error for ~11 test cases are shown in Figure 4.8 for various range of RAT. The model based delay is within ~10% of SPICE simulated data. The largest error occurs for biggest slope and smallest load condition.

Further the Model vs. SPICE comparison for SIS delay +1% to +11% delay values are also compared. Approximately 11 test cases in the extreme corners of

characterization range and center of TLU model in the synopsys library were taken for analysis. The model based delay is within 10% of SPICE data as shown in Figure 4.9.

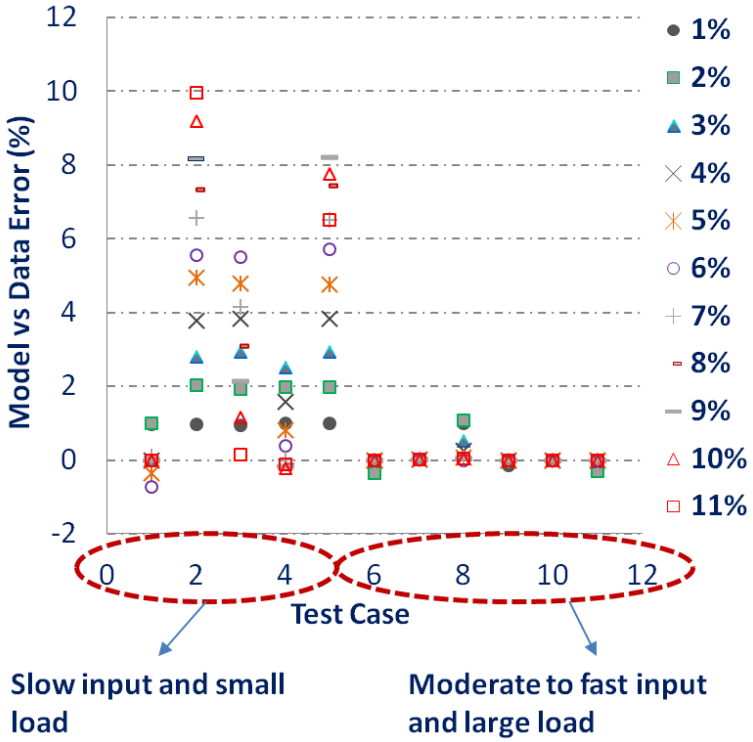

Figure 4. 9 : Comparison of setup region

4.4.6 Computation cost

The computation cost of a 2-input NAND gate is analyzed under four scenarios as shown in Table 4.1 for the delay corresponding to output high to low transition measured from bottom input of the NMOS stack. Scenario 1: The traditional SIS model is the single input switching delay of the gate for a set of input slope and output load combination. Scenario 2: The dynamic MIS simulation is the SPICE simulation of the 2-NAND gate for input RAT=0 to

RAT=250ps with the RAT step of 1ps. Scenario 3: The finite point SPICE model is the finite point model with delay for point A, B, C extracted from SPICE simulation for a given slope and load combination. Scenario 4: The finite point Analytical model is the finite point model with delay for Point A, B, C extracted from proposed Analytical model for a given slope and load combination.

The computation cost of proposed finite point MIS characterization approach is compared with dynamic MIS simulation as well as the traditional SIS model as shown in Table 4.1. MIS characterization using finite-point analytical model is a fraction of second compared to that of dynamic MIS simulation and finite-point SPICE simulation based model. Finite-point SPICE simulation based MIS characterization is 3X compared to that of traditional SIS runtime. Thus the proposed finite-point based MIS characterization methodology helps characterize the MIS effect with less computation cost.

Table 4. 1 : Computation cost of finite-point characterization

Slope X Load (TLU)	Traditional SIS Model (s)	Dynamic MIS Simulation (s)	Finite-point SPICE Model (s)	Finite-point Analytical Model (s)
1x1	3	750	9	0.001
5x5	75	18750	225	0.025
7x7	147	36750	441	0.049
10x10	300	75000	900	0.100

TLU: Table look up.

4.5 MIS gates with more than 2 inputs

4.5.1 RAT_C and delay correlation with SPICE

For a 3-input NAND gate, the final RAT_C calculated using proposed methodology is compared with SPICE results for mid point transition time and load condition of the characterization range as shown in Figure 4.10 (a.). Here the RAT_C for leading input is 11.808ps. τ_{in1} τ_{in2} and τ_{in3} are the transition time of inputs in1, in2 and in3 and C_L is the output load respectively.

The MIS delay using proposed methodology is further compared against SPICE for various transition times of all three inputs and output loading condition. For each combination of input and output conditions used for characterization, the RAT value is considered from RAT_0 to $RAT_{INF.}$ The root mean square error for the entire characterization range is R^2 = 0.93 as shown in Figure 4.10 (b.).

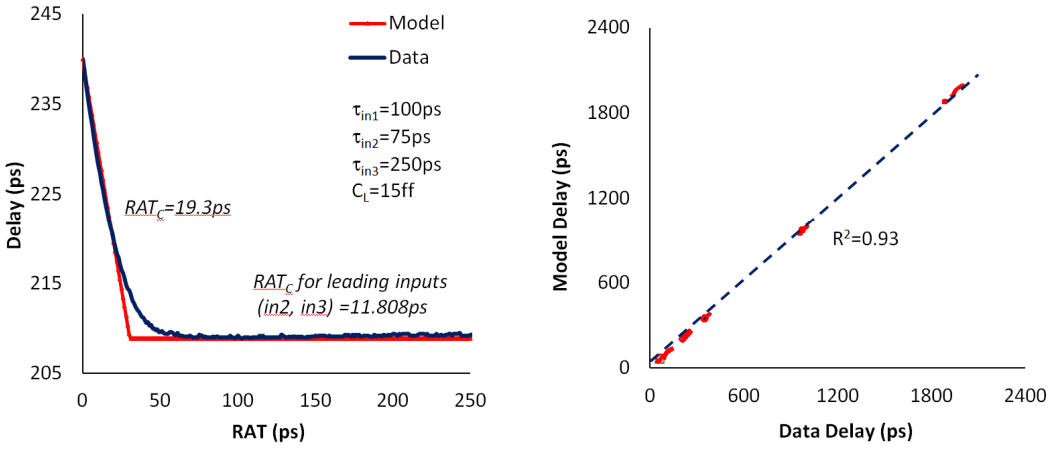

Figure 4. 10 : NAND3: RAT_C and delay correlation with SPICE

For a 3-input NAND gate, Figure 4.11 and Figure 4.12 presents the the delay vs RAT curve from proposed Model and SPICE simulation data for typical, slow and fast corners and for output TPHL and TPLH conditions respectively. Here, WC represents worst case where two of the leading inputs in2 and in3 are tied together when MIS occurs with the lagging input in1 and BC represents best case where non of the three inputs are tied together. Here note that for WC scenario $RAT_{C(lead)}$ =0, as the two leading inputs are tied together. The same approach can be extended to other multiple input gates in the standard cell library with appropriate device parameters.

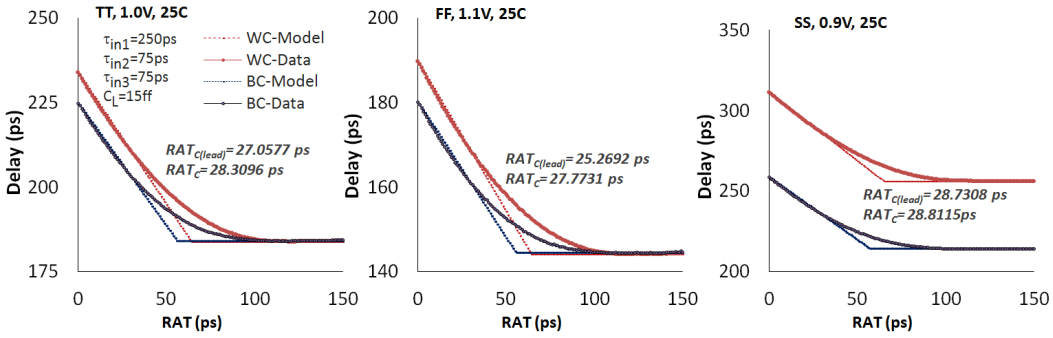

Figure 4. 11 : RAT_C for NAND3 with PVT variation – TPHL

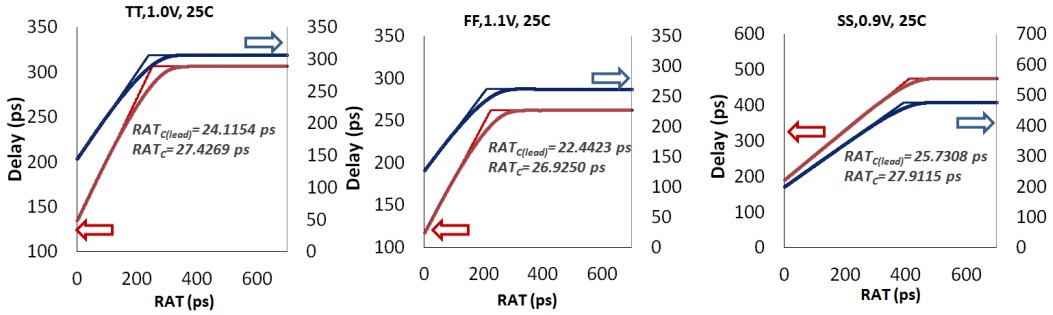

Figure 4. 12 : RAT_C for NAND3 with PVT variation – TPLH

4.6 Sequential elements

The finite point method used for setup and hold model is applicable for any type of sequential element. This is valid, since the model accounts for the delay difference between the clock path and data path in the circuit. The model is extensively validated using finite-point model with 3 finite points. The validation results are demonstrated using dynamic latch circuit shown in Figure 4.13. Similar approach is extended for all the benchmark sequential circuits in the standard cell library.

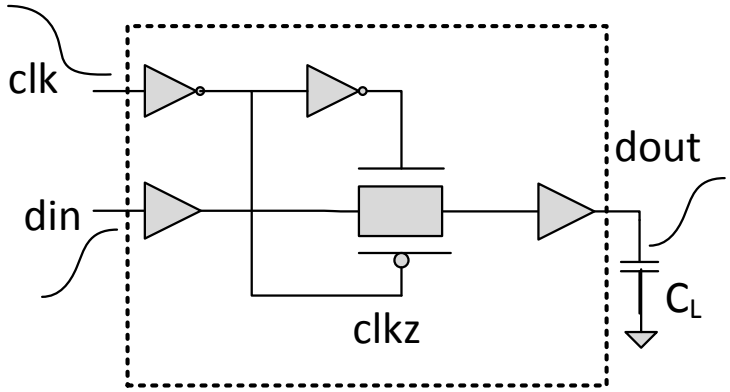

Figure 4. 13 : Benchmark circuit : dynamic latch

4.6.1 Minimum setup time correlation to SPICE

The accuracy of the model is highly dependent on the accurate prediction of minimum setup time. With the minimum setup time, the model accuracy can be further improved with additional finite points. The model predicted minimum setup time is compared to SPICE simulation as shown in Figure 4.14 for an active high dynamic latch for date input rise and fall conditions respectively. The root mean square error (R^2) is approximately 0.92 to 0.986 considering all cases.

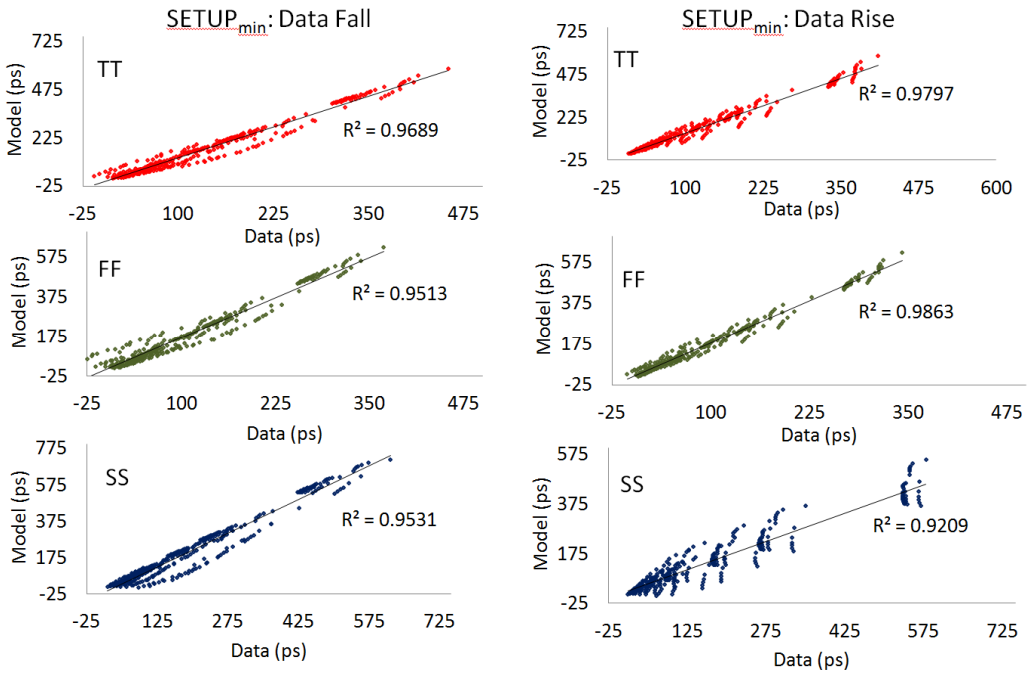

Figure 4. 14 : Minimum setup time: correlation to SPICE simulation.

4.6.2 Model validation for setup time

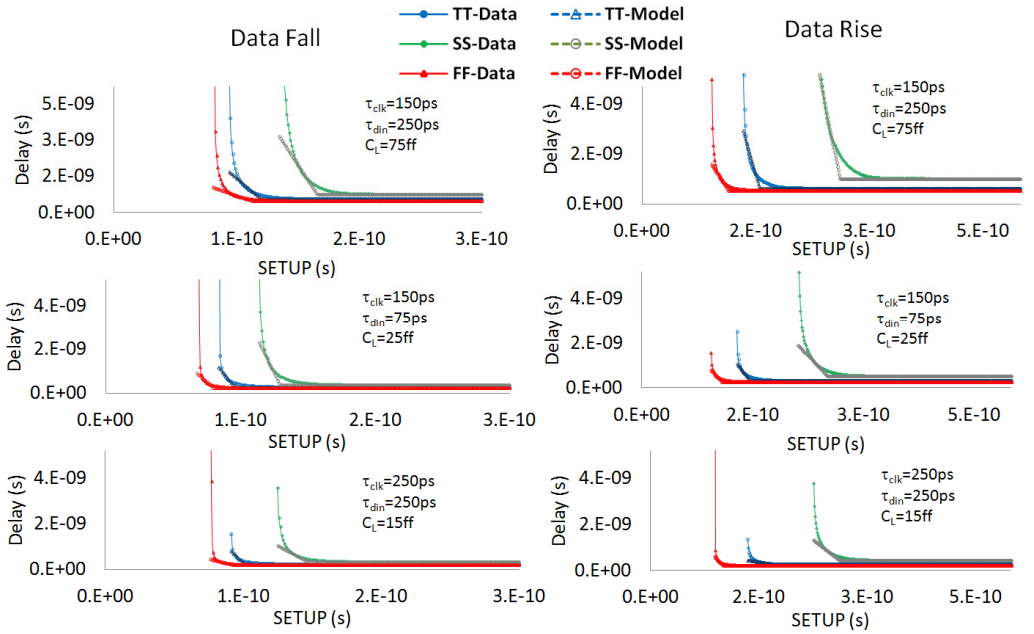

Figure 4. 15 : Finite-point model for setup time compared to SPICE.

The model generated delay versus setup time characteristics, are compared to SPICE results for various operating conditions in Figure 4.15. The finite-point setup characteristic curve is compared to SPICE simulation results for various clock / data transition time and output load conditions using typical, fast and slow corners. The model error is within 10% compared to that of SPICE simulation results.

4.6.3 Finite point analysis for setup time

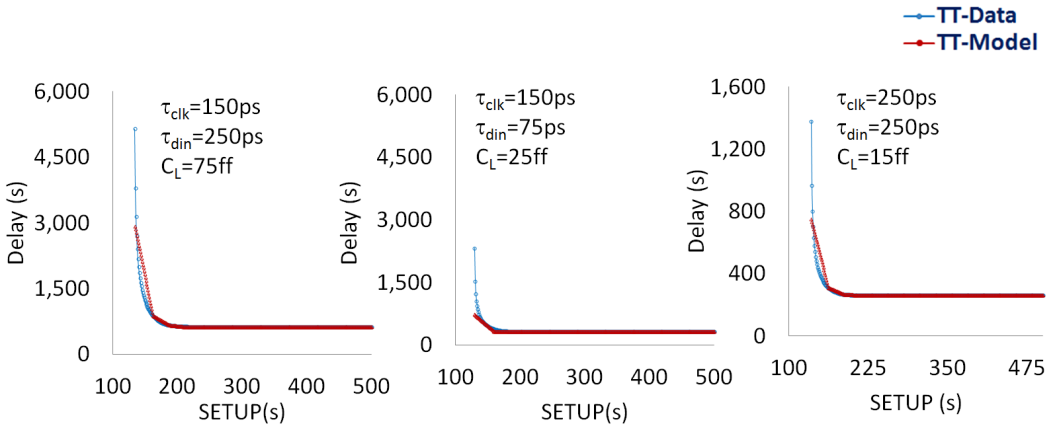

Figure 4. 16 : Finite-point analysis of setup time.

Once the minimum setup time is obtained, the accuracy of the model can be further improved with additional finite points in the delay vs setup curve. Delay vs setup time using 7 finite points is shown in Figure 4.16 for various input slope and output load condition. Here the critical voltage level for the clk is set to V_C : 0.5 V_{dd} , 0.65 $V_{dd,}$ 0.75 $V_{dd,}$ 0.85 $V_{dd,}$ 0.95 $V_{dd,}$ 1.0 $V_{dd,}$ respectively. Due to the nature of the setup characteristic curve, not all finite

points are very useful. Yet the model accuracy can be improved by additional finite points.

4.6.4 Finite point analysis for hold time

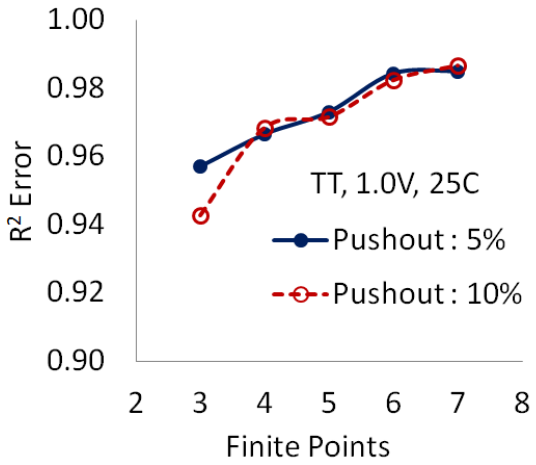

Figure 4. 17 : Finite-point analysis of hold time.

In general, the minimum hold time for a sequential cell can be of negative value. The accuracy of hold time is one of the critical parameter for circuit operation. Thus the number of finite points versus the accuracy of finite point model is further analyzed. Using the procedure for finite point analysis discussed in Section 3.3.3 and the finite points specified in Table 3.1, under nominal condition, the hold time is characterized for 5% delay pushout and 10% delay pushout respectively. The characterization is performed over the entire characterization range, consisting of 7x7x7 matrix of τ_{clk} x τ_{din} x C_L.

Figure 4.17 shows the model error for different number of finite points over the entire characterization range at typical corner. The error almost saturates beyond 5 finite points. Since the computation cost for 3 finite point modeling

approach is comparatively less, and the accuracy is comparable to SPICE simulation results, we have used 3 point approach for all our analysis.

Also at typical corner, the model predicted hold time is compared to SPICE results for finite point model using 3-points and 7-points as shown in Figure 4.18. In all cases the error is greater than R^2=0.9 with model accuracy close to 0.99 for finite point model using 7 finite points. Thus the accuracy of the finite point model can be improved by use of increased number of finite points as shown in Figure 4.18.

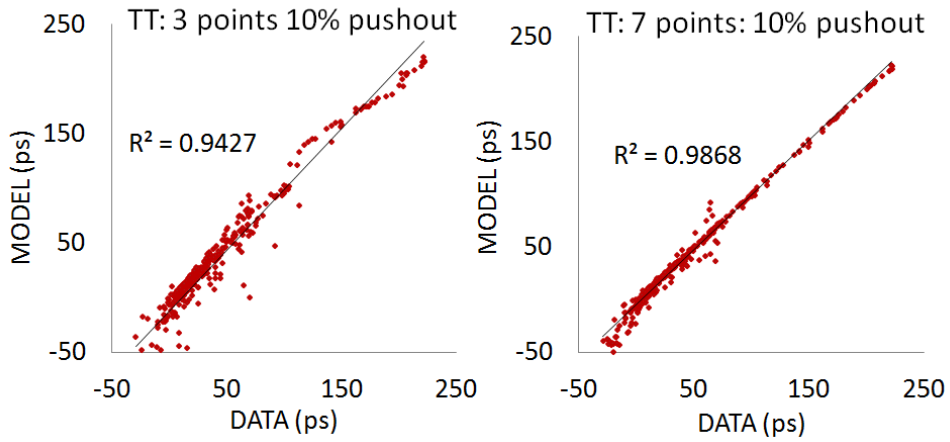

Figure 4. 18 : Finite-point correlation to SPICE for hold time .

The R^2 in the model is further analyzed for fast and slow corners for input rise and fall conditions using delay pushout of 5% and 10% respectively. The R^2 error is summarized in Table 4.2 for finite point model constructed using 3 and 5 finite points. The R^2 error is observed to be greater than 0.8 for all PVT corners.

Table 4. 2 : Finite-point analysis for hold time

Dynamic latch R^2 Error		Data fall delay puhout		Data rise delay puhout	
Finite points	PVT corner	5%	10%	5%	10%
3	TT: 1.0V, 25C	0.9572	0.9650	0.9000	0.9658
	FF: 1.1V, 25C	0.9400	0.9552	0.8700	0.9639
	SS: 0.9V, 25C	0.9682	0.8870	0.9650	0.9843
5	TT: 1.0V, 25C	0.9696	0.8500	0.8430	0.8944
	FF: 1.1V, 25C	0.9500	0.9690	0.8600	0.9463
	SS: 0.9V, 25C	0.9662	0.8313	0.9544	0.8755

4.6.5 Hold time correlation to SPICE

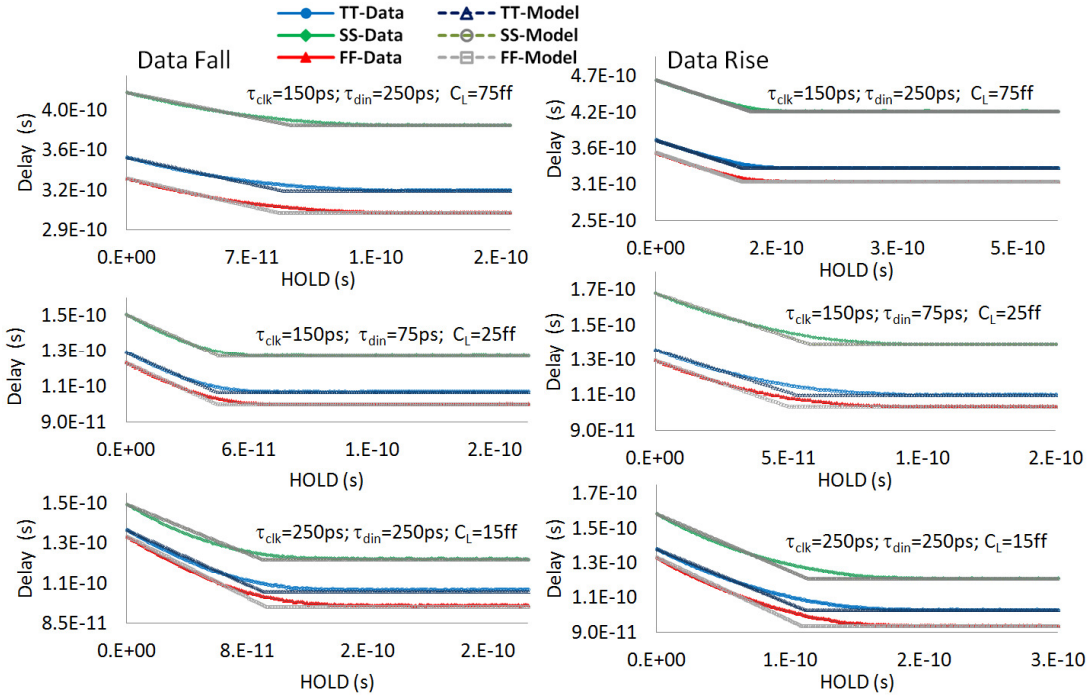

Figure 4. 19 : Finite-point model for hold time compared to SPICE.

For the dynamic latch, the finite-point based hold time is compared with SPICE in Figure 4.19 for data input rise and fall conditions. Here three finite points were used for the construction of the characterization curve. For various

operating conditions such as τ_{clk} x τ_{din} x C_L using typical, slow and fast PVT corners, the model error is ~10% compared to that of SPICE simulation results.

4.6.6 Setup and hold time analysis for benchmark Circuits

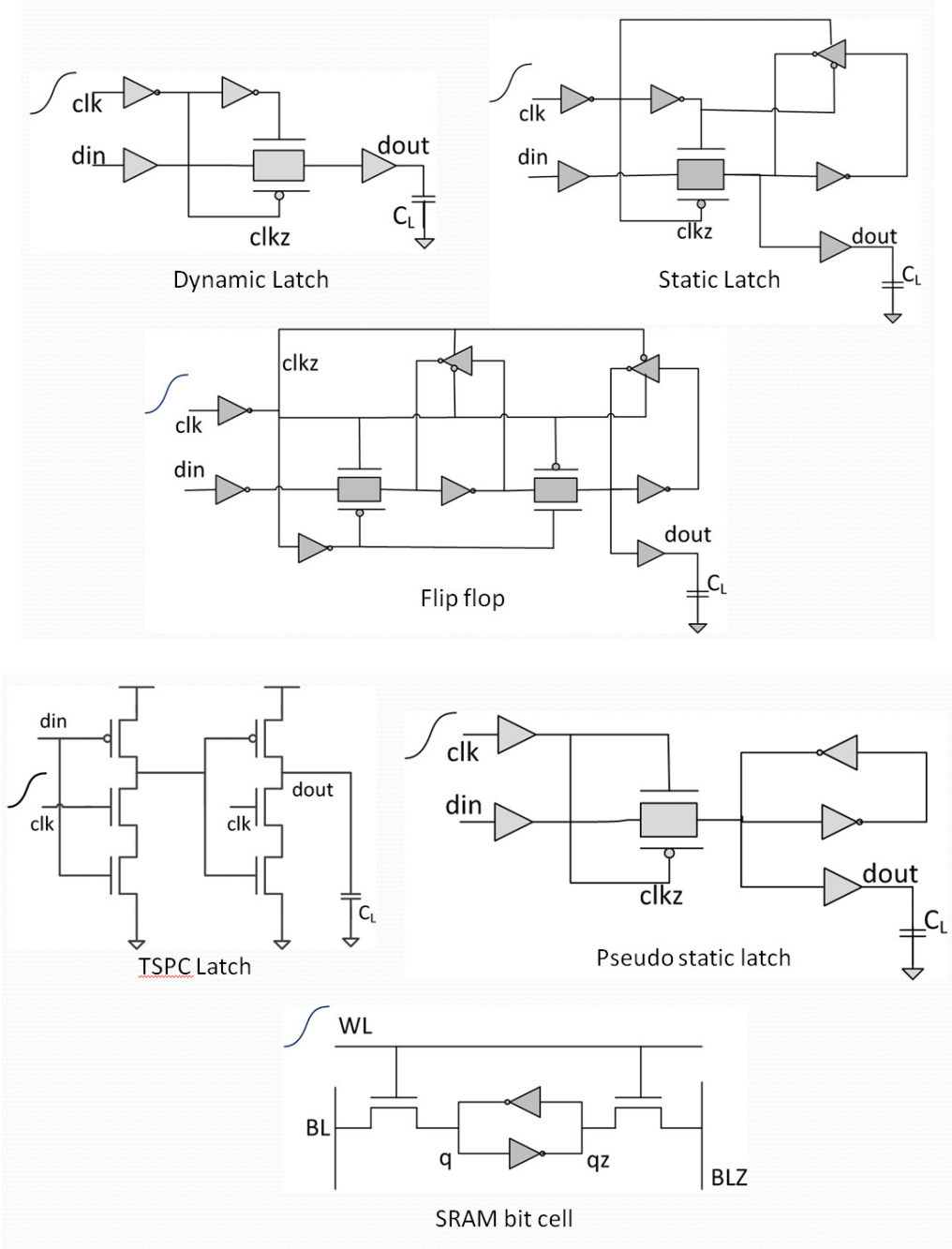

Figure 4. 20 : Benchmark circuits for Setup / Hold characterization.

The benchmark circuits used for the validation of setup and hold time are shown in Figure 4.20. For the benchmark circuits, the setup time correlation to SPICE results are compared in Table 4.3 and hold time correlation to SPICE results are compared in Table 4.4 respectively.

Table 4. 3 : Setup time correlation to spice for benchmark circuits

Delay pushout (%)	PVT	τ_{clk} (ps)	τ_{din} (ps)	C_L (ff)	SETUP TIME : Model Error (ps)					
					dynamic latch	static latch	pseudo static latch	TSPC latch	flip flop	sram bit cell
5	TT, 1.0V, 25C	150	250	75	-7.60	13.41	-17.00	-3.00	-3.00	-9.38
		150	75	25	10.50	1.23	-9.00	4.00	-1.00	-11.12
		250	250	15	5.82	0.24	-2.52	4.80	1.80	-1.66
	SS, 0.9V, 25C	150	250	75	13.30	-5.00	3.00	12.00	-1.00	-6.97
		150	75	25	1.00	2.00	1.00	10.00	-1.00	7.51
		250	250	15	3.99	-10.24	-4.00	14.00	-16.00	-13.16
	FF, 1.1V, 25C	150	250	75	8.52	-18.00	-15.50	-9.00	-16.00	-7.43
		150	75	25	4.25	-7.00	-10.00	-6.00	-2.00	-3.24
		250	250	15	6.49	1.69	9.48	-13.00	-8.00	-5.45
10	TT, 1.0V, 25C	150	250	75	10.30	-2.44	17.00	-4.00	-3.00	-5.50
		150	75	25	15.03	5.85	-10.00	3.00	5.68	-9.17
		250	250	15	1.15	-3.76	6.12	2.90	10.27	11.73
	SS, 0.9V, 25C	150	250	75	4.20	-7.00	1.00	11.00	0.00	18.30
		150	75	25	-4.85	-5.00	-1.00	3.99	-2.00	-2.76
		250	250	15	12.31	0.28	-6.00	12.00	-18.00	-15.23
	FF, 1.1V, 25C	150	250	75	-2.26	-18.00	-15.50	-10.00	-16.00	-4.17
		150	75	25	-2.99	-9.00	-1.00	-7.00	-3.00	5.26
		250	250	15	0.01	-5.00	-16.25	-14.00	-10.00	2.37

For the benchmark circuit, delay pushout of 5% and 10% are used for the validation of setup time and hold time. The setup and hold time error for the finite point method is within ±20ps compared to that of SPICE simulated results. Thus the finite point characterization method can help reduce the computation cost for setup and hold time characterization within SPICE margin.

Table 4. 4 : Hold time correlation to spice for benchmark circuits

Delay pushout (%)	PVT	τ_{clk} (ps)	τ_{din} (ps)	C_L (ff)	HOLD TIME : Model Error (ps)					
					dynamic latch	static latch	pseudo static latch	TSPC latch	flip flop	sram bit cell
5	TT, 1.0V, 25C	150	250	75	-0.17	-0.43	-0.20	-0.13	-1.96	0.10
		150	75	25	-0.01	0.50	-0.68	-0.29	5.14	1.00
		250	250	15	2.99	0.13	-0.86	0.25	13.00	-0.10
	SS, 0.9V, 25C	150	250	75	2.09	-0.28	4.69	-0.06	-13.00	-0.20
		150	75	25	0.08	-0.43	0.05	-0.13	-8.96	5.80
		250	250	15	1.61	2.64	0.80	-0.43	-15.00	1.60
	FF, 1.1V, 25C	150	250	75	-0.03	-0.31	-0.20	-0.11	8.00	-1.10
		150	75	25	0.47	0.50	-0.13	-0.16	11.00	-1.22
		250	250	15	3.47	2.00	0.65	0.46	-4.20	0.12
10	TT, 1.0V, 25C	150	250	75	-0.47	-0.45	0.53	-0.10	-6.29	-3.80
		150	75	25	0.99	0.28	-0.97	0.08	-1.82	-1.00
		250	250	15	0.70	-0.83	-0.81	0.10	7.00	-0.43
	SS, 0.9V, 25C	150	250	75	9.88	-0.16	-0.34	0.46	-19.70	-0.20
		150	75	25	8.01	-0.63	1.66	-0.13	13.19	5.80
		250	250	15	-0.23	0.28	0.76	-1.16	-18.40	1.60
	FF, 1.1V, 25C	150	250	75	-0.49	0.42	1.51	-0.50	-0.80	-1.70
		150	75	25	0.63	-0.22	0.50	-0.14	11.00	-0.76
		250	250	15	0.80	-0.80	-0.39	-0.44	6.80	-2.00

4.6.7 Computation cost for setup and hold time

The computation cost for setup and hold time is compared in Table 4.5 for a dynamic latch using traditional SPICE simulation and for the finite point model with different number of finite points. Using finite-point method for characterization, the runtime is significantly reduced by an order of magnitude compared to that of SPICE simulation. The finite point model with 3 finite-points has minimal computation cost as expected. Using 5 or 7 finite-points for the characterization of setup and hold still yields significant reduction in runtime of approximately 25x compared to that of tradition SPICE simulation. The runtime for finite point method with 3 finite points is ~0.5x compared to that of model

with 7 finite points. Similar trend is observed for other sequential elements in the standard cell library.

Table 4. 5 : Computation cost for Setup and Hold time

Slope X Load (TLU)	SPICE Model (s) Setup/Hold Step=3ps	Finite Point Model (s)		
		3 points	5 points	7 points
1x1x1	1360	12	20	28
5x5x5	170000	1500	2500	3500
7x7x7	466480	4116	6860	9604
10x10x10	1360000	12000	20000	28000

TLU: Table look up in synopsys library model file; Slope: signal trasition time.; Load : output fanout.

CHAPTER 5

INTEGRATION WITH DESIGN FLOW

5.1 Design Flow Integration

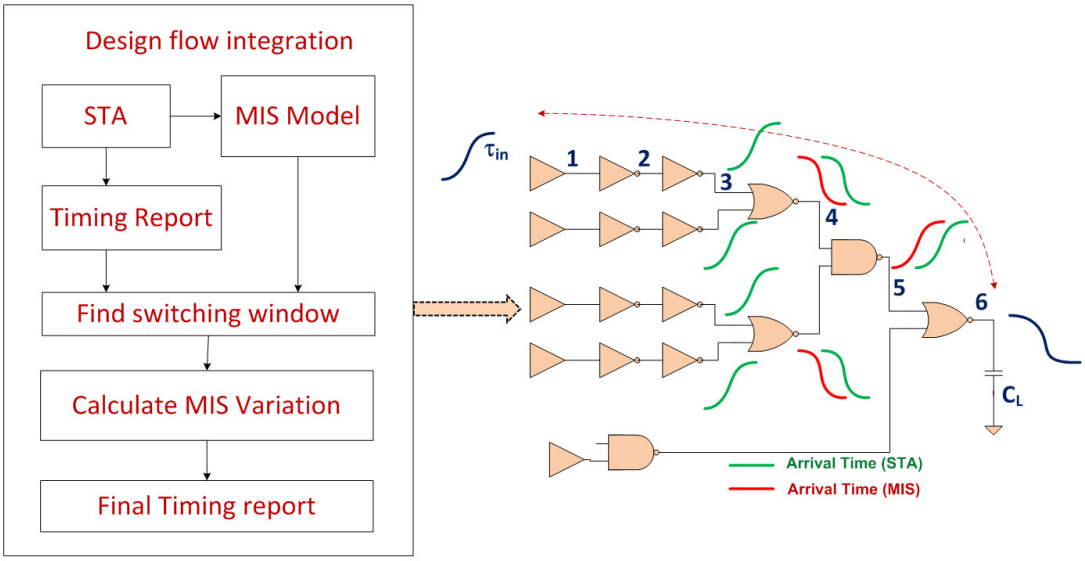

Figure 5. 1 : Flow diagram for MIS model integration in design flow

The flow diagram for MIS model integration with STA flow is shown in Figure 5.1. The input to MIS model such as input transition time and output load of the gate is taken from STA and finite point MIS characterization is performed. Since the output load of the gate, mainly defines the input transition time for the next stage, the impact of output slew of the gate is not considered in our analysis. The switching window of a stage is calculated from the difference between SIS delay and MIS delay due to proximity effect of the input signals in a particular gate. The early and late arrival time of the switching window is defined by the best case and worst case delay of the SIS and MIS condition of the stage. The switching window is propagated to the next stage by accounting for all the

proximity effect of the multiple input gates. As the number of stages increase the difference between the early and late arrival time of the signal gets widen until another close proximity effect occurs in the critical path. The variation due to MIS effect is adjusted to STA timing report and final report is generated for timing analysis.

ISCAS C17 circuit is used to validate the MIS integration with design flow due to the shortest paths in the design along with column decoder and row decoder circuit of the SRAM which are some of the most critical circuits in the VLSI design.

5.2 Validation of design flow

5.2.1 ISCAS C17 benchmark circuit

The ISCAS C17 benchmark circuit is shown in Figure 5.2. The propagation delay from input node G4 to output node G16 is recorded in Table 5.1 for output rise and fall conditions.

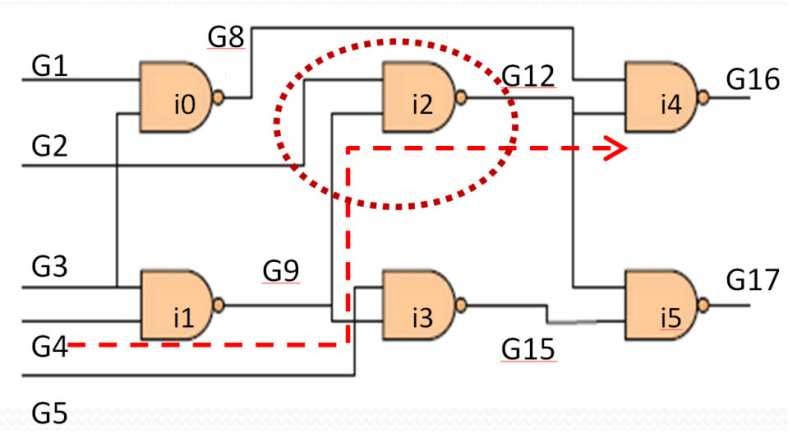

Figure 5. 2 : ISCAS C17 benchmark circuit

The finite points A, B, C were derived from finite point analytical model. Same finite point analytical model is used for rise and fall condition with changes to appropriate circuit and device parameters. Active driven waveform is applied to G4 and G3 with transition time of 100ps and 150ps respectively. Active load is applied to G16 with 15ff load. For various range of RAT between inputs G3 and G4 for low to high transition, the path delay using finite-point model is within 7% of SPICE data as shown in Table 5.1.

Table 5. 1: Path delay comparison of ISCAS C17

ISCAS C17 (TT)	RAT (G3,G4) (ps)	Fall delay			Rise delay		
		SPICE (ps)	Model (ps)	SPICE vs Model (%) Error	SPICE (ps)	Model (ps)	SPICE vs Model (%) Error
MIS	0	184.6	192.66	-4.39	315.10	330.00	-4.73
	5	182.2	190.67	-4.62	318.30	331.90	-4.27
	10	180.1	189.14	-5.00	321.20	333.84	-3.93
	15	178.5	187.61	-5.12	324.30	335.82	-3.55
	20	177.0	186.11	-5.16	326.90	337.88	-3.36
	25	175.7	184.62	-5.05	329.30	339.98	-3.24
	30	174.9	183.21	-4.78	331.60	342.21	-3.20
	35	174.1	181.81	-4.43	333.60	344.42	-3.24
	50	172.2	177.54	-3.13	338.10	351.34	-3.92
	175	171.2	174.51	-1.96	340.20	364.19	-7.05
SIS	1600	171.2	174.51	1.56	340.20	363.63	-6.89

Furthermore the propagation of switching window due to MIS is summarized in Table 5.2 for the second stage 2-input NAND gate as highlighted in Figure 5.2. The switching window in Table 5.2 is the RAT between inputs G2 and G9 nodes in Figure 5.2. Here G2 transitions from low to high at 0ps and transitions high to low at 32.5 ps for switching window analysis. The delay variation due to switching window changes can be observed from Table 5.2. Though the delay

variation in single stage 2-input NAND gate in the case of ISCAS C17 is not much significant in Table 5.2, the propagation of switching window helps capture significant proximity effect during timing analysis in the design flow.

Table 5. 2 : MIS switching window for 2nd stage NAND2 of ISCAS C17

ISCAS C17 (TT)	RAT (ps) (G3, G4)	Node G12 rise condition		Node G12 fall condition	
		Switching window (ps) (G2, G9)	Delay (ps) (G12)	Switching window (ps) (G2, G9)	Delay (ps) (G12)
MIS	0	2.51	12.21	39.83	51.19
	5	4.58	11.95	43.11	51.19
	10	6.21	11.67	46.09	51.13
	15	7.49	11.40	48.99	51.17
	20	8.49	11.17	51.56	51.26
	25	9.29	10.95	53.85	51.43
	30	9.94	10.76	55.86	51.65
	35	10.49	10.62	57.61	52.00
	50	11.78	10.38	60.49	53.59
	175	12.97	10.46	60.62	55.19
SIS	1600	12.85	10.39	60.61	55.22

5.2.2 Column decoder

A circuit in the column decoder is used to analyze the path delay impact due to MIS effect on 3 input NAND gate, as highlighted in Figure 5.3.

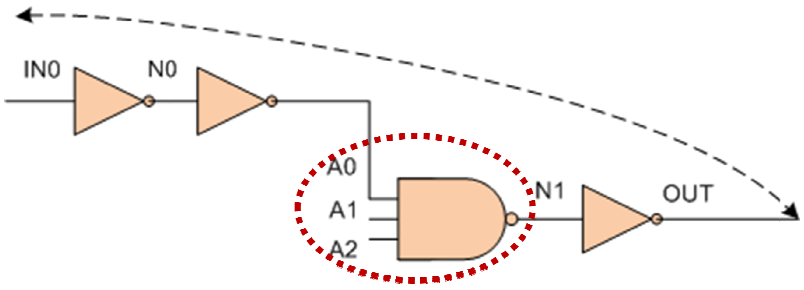

Figure 5. 3 : Critical path of the column decoder

Based on the input transition time and output load from STA, the 3-input NAND gate is characterized using the proposed finite-point method. For the path delay shown in Table IV, the active driven input transition time are used for nodes A0, A1 and A2 are 175ps, 50ps and 75ps respectively and active load of 7.5ff used for node N1. The finite points A, B, C are extracted from SPICE simulation for this analysis. The path analysis with finite point method is within 2% compared to that of SPICE for various RAT conditions as shown in Table 5.3.

Table 5. 3 : Path delay comparison of column decoder

RAT (ps)	SPICE		Model		Error	
	Stage delay (ps)	Path delay (ps)	Stage delay (ps)	Path delay (ps)	Stage delay (%)	Path delay (%)
0	240.00	463.31	240.00	463.31	0.00	0.00
5	233.70	457.13	235.07	458.50	-0.59	-0.30
10	228.20	451.56	230.14	453.50	-0.85	-0.43
15	223.60	446.92	225.21	448.53	-0.72	-0.36
20	219.70	443.12	220.27	443.69	-0.26	-0.13
25	216.50	439.92	215.34	438.76	0.54	0.26
30	214.20	437.54	210.41	433.75	1.77	0.87
35	212.10	435.51	208.90	432.31	1.51	0.73
40	210.90	434.35	208.90	432.35	0.95	0.46
50	209.60	432.87	208.90	432.17	0.33	0.16
75	209.30	432.68	208.90	432.28	0.19	0.09
175	209.10	432.45	208.90	432.25	0.10	0.05
520	209.50	432.74	208.90	432.14	0.29	0.14

5.2.3 Row decoder

The critical path of the row decoder circuit is shown in Figure 5.4. The propagation delay for SIS, RAT_0 and dynamic simulation conditions are compared in Table 5.4.

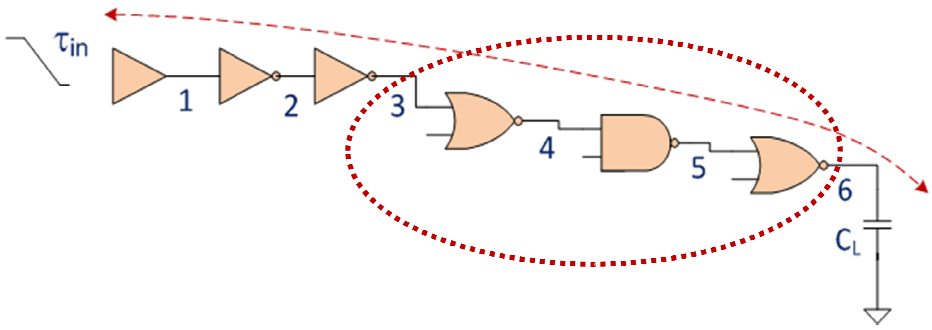

Figure 5. 4 : Row decoder critical path

Table 5. 4: Critical path delay comparison of row decoder under MIS

Path delay	Output fall condition	Output rise condition
SIS : STA (ps)	474.43	340.90
MIS : RAT_0 (ps)	526.11	221.26
MIS : Dynamic (ps)	501.46	221.06
SIS vs RAT_0 (% error)	-10.89	35.10
SIS vs Dynamic (% error)	-5.70	35.15

Finite points A, B, C for this analysis is extracted from SPICE simulation. The active driven input transition time of approximately 250ps and active load of 25ff is used for this analysis. It is observed that the path delay for input high to low transition for RAT_0 condition and dynamic simulation case are very close and vary by ~35% compared to that of SIS condition using STA. For input low to high transition, for RAT_0 condition, the path delay vary by ~11% compared to that of SIS and for dynamic condition it vary by ~6% compared to that of SIS.

The switching window is analyzed for output fall and rise and conditions. The critical path used for this analysis is shown in Figure 5.5. Table 5.5 summarizes the switching window for all 6 stages of row decoder critical path for output rise and fall conditions. The variation in switching window is summarized for RAT_0 and dynamic simulation are compared to that of SIS case.

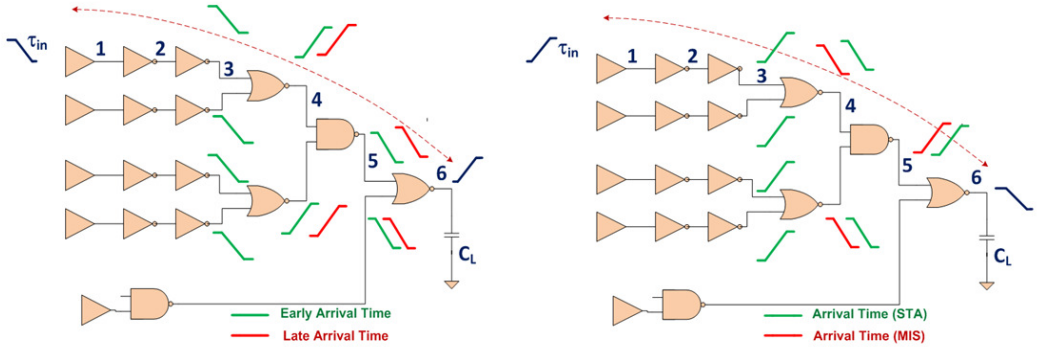

Figure 5. 5 : Row decoder switching window propagation

It is observed that depending on the input low to high or high to low transition, the switching window for RAT_0 condition and dynamic simulations comes close together or diverts apart suggesting the need for propagation of switching window through all the stages of MIS gates. The switching window is calculated for the multiple input gates from the STA report. The switching window is propagated through each MIS stage and the variation between the SIS delay and the MIS delay is adjusted in the final timing report for design analysis.

Table 5. 5 : Switching window analysis for row decoder

Stage	Switching window			
	Output rise condition		Output fall condition	
	RAT_0	Dynamic SPICE simulation	RAT_0	Dynamic SPICE simulation
1	4.52	4.55	3.46	3.44
2	7.01	7.05	5.25	5.20
3	7.65	7.61	5.59	5.51
4	14.72	14.74	9.57	9.58
5	24.97	24.83	29.05	29.06
6	51.69	27.03	119.64	119.38

CHAPTER 6

FUTURE WORK

This section describes the research work being done for setup and hold characterization of pass gate.

6.1 Limitations

Finite-point approach has ~10% error for extreme cases such as large signal transition time and small load condition due to linear approximation in the non-linear portion of the delay versus RAT curve or Setup/Hold time vs delay curve respectively.

6.2 Statistical Method for Coefficient Extraction

For the sequential cells with steep transition for the output delay from minimum setup/hold time to infinite setup/hold time, the accuracy of the finite-point method can be further improved by any means of fast and accurate coefficient extraction method using modern statistical engines.

CHAPTER 7

SUMMARY AND CONCLUSION

Due to the effect of technology scaling, characterization of standard cell using SIS is not sufficient for the measurement of circuit performance during timing analysis in the design flow. The delay of the multiple input gates in the critical path can vary up to 50% while considering the temporal proximity effect of the MIS scenarios. Such effect can cause variation during setup and hold timing analysis. Further, due to the technology shrink, there is a need for multiple library models for various operating conditions during STA. The characterization of setup and hold time constraint of the sequential elements is a time consuming process due to the binary search method used for identifying the failure criteria of the circuit. Thus there is a demanding need to integrate MIS effect into design flow for timing analysis and improved the computation cost for the characterization of setup and hold time of sequential elements

With the help of the proposed finite-point method for MIS characterization of multiple input gates, and integration of such effect into design flow through propagation of switching window, the gate delay variation due to MIS can be tracked in the STA flow. Hence the proposed finite-point characterization approach and design flow integration can complement the design phase for setup and hold analysis. The proposed finite-point method for the characterization of setup and hold time, can significantly reduced the runtime for all sequential elements in the standard cell library. It is also critical to define the optimal finite-point for a given set of input condition. The proposed method to find RAT_C,

efficiently defines the critical point C for multiple input gates without trading off accuracy. And the proposed method to find critical setup and hold time, efficiently defines the critical points without trading off accuracy

At 45nm technology node, under various operating conditions such as typical, slow and fast PVT conditions, the experimental results show significant reduction in runtime with less than 10% error for MIS gates and ±20ps error for setup and hold time compared to that of SPICE simulation data.

Thus the proposed approach for the characterization of multiple input gates and setup / hold time of sequential elements can be efficiently applied during early design phase of the product cycle to analyze the dynamic variation induced by MIS in the VLSI design.

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APPENDIX A

BOUNDARY CONDITION FOR FAST AND SLOW INPUT

Consider the fast input $V_{in} = V_{dd}\, t/\tau_{in}$. where $t_{sat} > \tau_{in}$. In such case, the following differential equation can be constructed using saturation current equation $I_D=K_s(V_{in}-V_t)$.

$$C_L \frac{dV_{out}}{dt} = -K_s.\left(V_{in} - V_t\right) \tag{A.1}$$

Integration of equation (A.1) with initial condition $V_{out} = V_{dd}$ and $V_{in} = V_t$, yields,

$$V_{out} = V_{dd} - \frac{K_s \tau_{in}}{2C_L V_{dd}}.\left(\frac{V_{dd}}{\tau_{in}} t - V_t\right)^2 \tag{A.2}$$

For boundary condition $V_{in} = V_{dd}$ at $t = \tau_{in}$ (A.2) can be expressed as,

$$V_{out} = V_{dd} - \frac{K_s \tau_{in}}{2C_L V_{dd}}.\left(V_{dd} - V_t\right)^2 \tag{A.3}$$

For $V_{out} > V_{dd} - V_t$, the NMOS is saturated when V_{in} reaches $V_{dd,}$ Thus (A.3) can be defined as,

$$V_{dd} - \frac{K_s \tau_{in}}{2C_L V_{dd}}.\left(V_{dd} - V_t\right)^2 > V_{dd} - V_t \tag{A.4}$$

To meet the criteria in (A.4), the following condition needs to be satisfied.

$$\frac{K_s \tau_{in}}{2C_L V_{dd}}.\left(V_{dd} - V_t\right)^2 < V_t \tag{A.5}$$

Thus the boundary condition between fast and slow input can be expressed as

$$\tau_{in} > \frac{2C_L V_{dd} V_t}{K_s \left(V_{dd} - V_t\right)^2} \tag{A.6}$$

APPENDIX B

CALCULATION OF t_{vout} FOR FAST INPUT

The fast input is defined by the condition $t_{sat} > \tau_{in}$. Where t_{sat} is the time for saturation and τ_{in} is the input transition time of the switching input in case of SIS scenario and effective transition time in case of MIS scenario. Here when t=t_{sat}, $V_{in} = V_{dd,}$ thus $V_{out}=V_{dd} - V_t$. And when t=τ_{in}, $V_{in} = V_{dd,}$ thus using the saturation current equation equation in (2) and solving equation (1) with initial condition $V_{out} = V_{dd}$, the following solution is arrived.

$$V_{out} = V_{dd} - \frac{K_s \tau_{in}}{2C_L V_{dd}} . (V_{dd} - V_t)^2 \tag{B.1}$$

Also at t_{sat} the following condition is true.

$$V_{dd} - V_t = V_{dd} - \frac{K_s \tau_{in}}{2C_L V_{dd}} . (V_{dd} - V_t)^2 - \frac{I(V_{out})}{C_L} \Delta t \tag{B.2}$$

where $I(V_{out})$ is the saturation current equation and $\Delta t = t_{sat} - \tau_{in}$. By solving (B.2), t_{sat} is given as,

$$t_{sat} = \tau_{in} \left(1 - \frac{1}{2} \left(1 - \frac{V_t}{V_{dd}} \right) \right) + \frac{C_L V_t}{K_s (V_{dd} - V_t)} \tag{B.3}$$

When $V_{in} > V_t$ and $t < \tau_{in}$, using the saturation current equation in (2) the solution for V_{out} is ,

$$V_{out} = V_{dd} - \frac{K_s \tau_{in}}{2C_L V_{dd}} . \left(\frac{V_{dd}}{\tau_{in}} t - V_t \right)^2 \tag{B.4}$$

Using $V_{out} = 0.5 V_{dd}$ and $t = t_{vout}$ in equation (B.4), t_{vout} is expressed as,

$$t_{vout} = \left[V_{dd} \sqrt{\frac{C_L}{K_s \tau_{in}}} + V_t \right] \frac{\tau_{in}}{V_{dd}} \tag{B.5}$$

When $\tau_{in} < t < t_{sat}$, using equation (B.1) and saturation current equation in (2), V_{out} can be expressed as,

$$V_{out} = V_{dd} - \frac{K_s \tau_{in}}{2C_L V_{dd}} . (V_{dd} - V_t)^2 - \frac{K_s}{C_L} . (V_{dd} - V_t) . (t - \tau_{in}) \qquad \text{(B.6)}$$

Using $V_{out} = 0.5V_{dd}$ and $t = t_{vout}$ in equation (B.6), t_{vout} is expressed as,

$$t_{vout} = \tau_{in} + \frac{C_L}{K_s (V_{dd} - V_t)} \left[0.5V_{dd} - \frac{K_s \tau_{in}}{2C_L V_{dd}} . (V_{dd} - V_t)^2 \right] \qquad \text{(B.7)}$$

When $t > t_{sat}$, using the linear current equation in (2), the following differential equation can be formulated.

$$\frac{dV_{out}}{dt} = -\frac{K_l}{C_L} . [(V_{dd} - V_t) V_{out}] \qquad \text{(B.8)}$$

Solving equation (B.8) for $V_{out} = 0.5V_{dd}$ and $t = t_{vout}$ yields,

$$t_{vout} = t_{sat} + \frac{C_L}{K_l (V_{dd} - V_t)} \left[0.6931 + \ln \left(1 - \frac{V_t}{V_{dd}} \right) \right] \qquad \text{(B.9)}$$

APPENDIX C

CALCULATION OF t_{vout} FOR SLOW INPUT

The slow input is defined by the condition $t_{sat} < \tau_{in}$. When $t<t_{sat}$ and $V_{in} > V_t$, V_{out} is defined using equation (B.4) and t_{vout} is defined using equation (B.5). When $t > t_{sat}$, the differential equation (B.8) is integrated with the following limits shown in equation (C.1).

$$\int_{t_{sat}}^{t_{vout}} dt = \int_{V_1}^{0.5V_{dd}} -\frac{C_L}{K_l}\frac{dV_{out}}{\left[\left(V_{in}-V_t\right)V_{out}\right]} \tag{C.1}$$

Where $V_1 = V_{out} = V_{in} - V_t$. From equation (B.4), V_1 can also be expressed as,

$$V_1 = V_{dd} - \frac{K_s \tau_{in}}{2C_L V_{dd}} . V_1^{\,2} \tag{C.2}$$

Solving equation (C.2) yields,

$$V_1 = \frac{-C_L V_{dd}}{K_s \tau_{eff}} \left(1 \pm \sqrt{1 + \frac{2K_s \tau_{eff}}{C_L}} \right) \tag{C.3}$$

Also V_1 can be expressed as,

$$V_1 = \frac{V_{dd}}{\tau_{in}} t_{sat} - V_t \tag{C.4}$$

From equation (C.4) t_{sat} can be derived as,

$$t_{sat} = \frac{\tau_{in}}{V_{dd}} \left(V_1 + V_t \right) \tag{C.5}$$

Solution to equation (C.1) is,

$$t_{vout} = t_{sat} + \frac{C_L}{K_l \left(V_{in} - V_t \right)} \left[\ln \left(\frac{0.5V_{dd}}{V_1} \right) \right] \tag{C.6}$$

APPENDIX D

CALCULATION OF t_s AND t_e FOR τ_{eff}

In general the transition time (τ) can be defined as the rate of change of voltage (V) per time step (t) and can be expressed as shown in equation (14).

$$\tau = \frac{dV}{dt} \tag{D.1}$$

The transition time of the two inputs can be expressed as:

$$\frac{dV_1}{dt_1} = \beta \frac{dV_2}{dt_2} \tag{D.2}$$

Where $\beta = W/2L$, W and L are the width and length of the NMOS transistor in the stack. Using equation (3.11) and referring to Figure 3.6, the following equations are formed.

$$\left(\frac{W}{2L}\right)\frac{t_{s2} - t_{s1}}{t_s - t_{s1}} = \frac{V_{dd}}{V_{dd} - V_C} \tag{D.3}$$

$$\left(\frac{W}{2L}\right)\frac{t_{e2} - t_{e1}}{t_e - t_{e1}} = \frac{V_{dd}}{V_{dd} - V_C} \tag{D.4}$$

V_C can be found as shown in Figure 3.5 for RAT_0 condition and Figure 3.6 for RAT_C condition respectively. The start time t_s and the end time t_e of τ_{eff} is defined as,

$$t_s = t_{s1} + \left(1 - \frac{V_c}{V_{dd}}\right).(t_{s2} - t_{s1}).\frac{W}{2L} \tag{D.5}$$

$$t_e = t_{e1} + \left(1 - \frac{V_c}{V_{dd}}\right).(t_{e2} - t_{e1}).\frac{W}{2L} \tag{D.6}$$

APPENDIX E

CALCULATION OF WEIGHT FUNCTION *w*

To account for transition time sensitivity to top and bottom transistor the weight function is given by polynomial equation shown below.

$$w = F\frac{\tau_{n2}(\tau_{n1}-1)}{2\tau_{n2}(\tau_{n1}-1)-\tau_{n1}(\tau_{n2}-1)} \quad \text{(E.1)}$$

where, τ_{n1} is the normalized transition time for bottom input in1, τ_{n2} is the normalized transition time for top input in2 and F is the fitting parameter.

The fitting parameter F is found from SPICE nominal delay for mid point slope and load condition. For $\tau_{in1} = \tau_{in2}$, w =1. And for $\tau_{in1} < \tau_{in2}$ or $\tau_{in1} > \tau_{in2}$, [0.5< w <1.5]. The behavior of the weight function is shown below in Figure E.1.

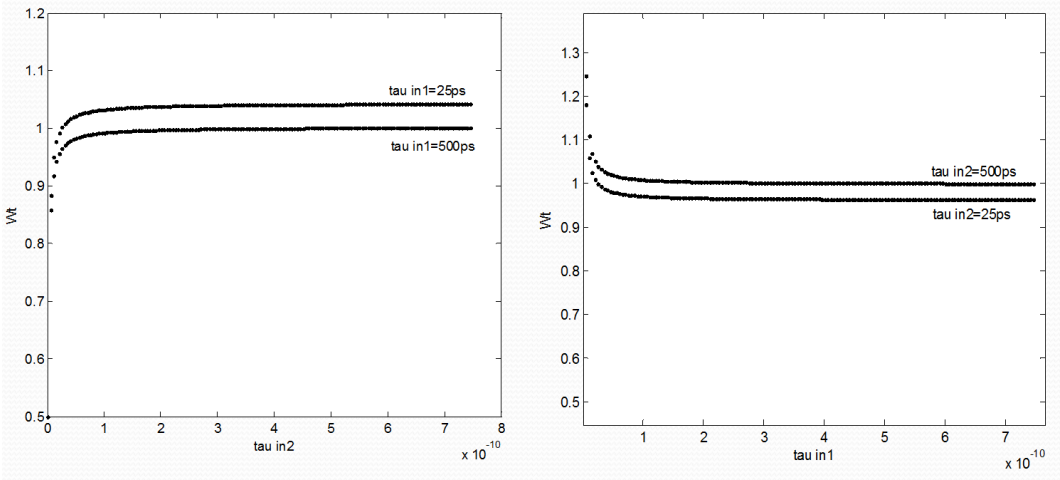

Figure E- 1: Behavior of the weight function for MIS model

The fitting paraters F for point A, B, C for NAND2 is given below in Table E-1.

Table E- 1: Fitting factor for NAND2 MIS model

	F
Point A	0.45
Point B	1
Point C	0.75

APPENDIX F

FINITE POINTE ANALYSIS

The optimal number of finite point is analyzed for a 2-input NAND gate with the use of equation 11 and Figure 5 for TPHL and TPLH. The method for finding finite points A and B are similar for all cases except, the V_t of the circuit is varied from $0.5V_{dd}$ to V_{dd} with the number of critical finite points of interest. For example in the case of four finite point model, two critical RAT_C points are identified using equation 11 and Figure 5. Here the lagging inputs start to ramp when the leading input is at $0.5V_{dd}$ and $0.75V_{dd}$ respectively. Similarly the three critical RAT_C points in the case of 5 finite point approach can be identified as shown in Table F.1.

Table F- 1: Critical V_t for RAT_c in MIS finite point analysis

Finite points	Point A	Point B	Point C: Circuit V_t	Additional Finite Points: Circuit V_t
3	RAT=∞	RAT=0	0.5 V_{dd}	
4	RAT=∞	RAT=0	0.5 V_{dd}	0.75 V_{dd}
5	RAT=∞	RAT=0	0.5 V_{dd}	0.7 V_{dd}, 0.9 V_{dd}
7	RAT=∞	RAT=0	0.5 V_{dd}	0.6 V_{dd}, 0.7 V_{dd}, 0.8 V_{dd}, 0.9 V_{dd}
10	RAT=∞	RAT=0	0.5 V_{dd}	0.6 V_{dd}, 0.7 V_{dd}, 0.75 V_{dd}, 0.8 V_{dd}, 0.85V_{dd}, 0.9 V_{dd}, 0.95 V_{dd}

For the finite points specified in Table E.1, the delay is captured using SPICE simulation and the RAT vs delay is characterized. The error in the model delay is analyzed using ~2500 sampling points for typical (TT, 1.0V, 25C), slow (SS, 0.9V, 25C) and fast (FF, 1.1V, 25C) corners respectively. The sampling points do not include the finite points that are used in the construction of finite point model. The R^2 error for finite point model versus the SPICE simulation delay is shown in Figure F.1. In all cases the R^2 is greater than 0.95. In all cases the R^2 is greater

than 0.95 with more than 3 finite points giving more accurate results as expected. Since the computation cost for 3 finite point approach is comparatively less, and the accuracy is comparable to SPICE, we have used 3 point approach for all our analysis. The user can adopt more than 3 finite points to improve the accuracy of of finite point method for characterization.

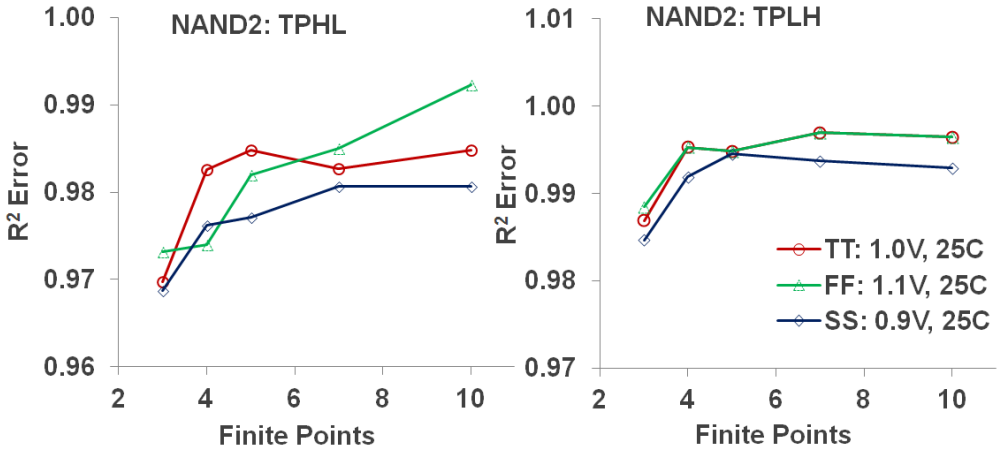

Figure F- 1: Finite point analysis for identifying optimal finite points.

APPENDIX G

CALCULATION OF f FOR SETUP TIME

The procedure for the calculation of fitting factor f in the finite point model for setup time is defined as follows

Due to the behavior of setup time, in order to improve the accuracy of the finite point based setup model, the fitting factor f is extracted using analytical model with polynomial approximation [34] for physical behaviors as shown is equation G.1.

$$f = a_0 + a_1 + a_2 a_3 \tag{G.1}$$

where,

a_0 : is the minimum start point for the clock to change its state. a_0 is found using simple inverter model with the condition, $V_{dout}=V_{clk}-V_{din}-V_t$. When $V_{clk}=V_{dd.}$ a_0 is given by equation G.2.

$$a_0 = \frac{2C_L V_{dd} V_t}{k\left(V_{dd} - V_t\right)^2} \tag{G.2}$$

where, the threshold voltage of the device V_t is extracted based on the I_d vs V_{gs} characteristic of the CMOS device for rise and fall conditions seperately. The device parameter k is extracted based on the I_d vs V_{ds} characteristic of the CMOS device.

a_1 : is the time taken to discharge the output load using saturation current equation of the CMOS device and is given by equation G.3.

$$a_1 = \frac{C_L V_{dd}}{k\left(V_{dd} - V_t\right)} \tag{G.3}$$

a_2 : is the sensitivity of the slope and load effect derived using simple inverter model with the condition, $\tau_{clk=}=\tau_{din}$ and $V_{out}= V_{clk}-V_{din}-V_t$ and is given by equation G.4.

$$a_2 = \left[\frac{C_L \tau_{clk}}{k\tau_{din} + C_L} + V_t \right] \frac{\tau_{clk}}{V_{dd}} \tag{G.4}$$

a_3 : is the sensitivity of slew rate difference between clock and data and is given by equation given by equation G.4. The fitting coefficient η is found by matching the simulation result for mid point slope and load condition.

$$a_3 = \frac{(1+\eta)}{\left(1 + \frac{\tau_{clk}}{\tau_{din}}\right)} \tag{G.5}$$

Thus the accuracy of the setup time characterization is improved based on the physical behavior of the circuit. In the case of hold time, the fitting factor f is simplified to f=±1 or 0 depending on the datapath delay *Td2q* and clock path delay *Tck2q* respectively.