High Efficiency Design Techniques

for Linear Power Amplifiers

by

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ABSTRACT

This thesis describes the design process used in the creation of a two stage cellular power amplifier. A background for understanding amplifier linearity, device properties, and ACLR estimation is provided. An outline of the design goals is given with a focus on linearity with high efficiency. The full design is broken into smaller elements which are discussed in detail.

The main contribution of this thesis is the description of a novel interstage matching network topology for increasing efficiency. Ultimately the full amplifier design is simulated and compared to the measured results and design goals. It was concluded that the design was successful, and used in a commercially available product.

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Chapter 1

INTRODUCTION

Cellular power amplifiers are all around us. Most people never take notice of them, but they make possible many modern conveniences we now take for granted. Whenever we want to surf the internet in a coffee shop, call a friend, send a text message, or update our Facebook status on a smartphone we rely on power amplifiers to make it happen. In 2011 the total number of mobile phones sold worldwide was more than 1.5 billion[1] with multiple power amplifiers in each phone. The mobile market is growing and the trend is toward more complex phones with more power amplifiers (often abbreviated PA singular and PAs plural). A recent teardown of the Apple iPhone 4S[2] reveals eight PAs inside with the number expected to increase in the iPhone 5 when LTE capability is added. Similar smart phones have high numbers of PAs as well.

Even though they enable our wireless world and enrich our lives power amplifiers waste a tremendous amount of electricity. At its best, a cellular PA will waste a little more than one watt for each watt of power it delivers. At its worst less than 1% of the energy it consumes is converted into useful power. The motivation for this research is to investigate the design decisions related to optimizing efficiency in cellular handset PAs and explore new methods for improving it. Cellular power amplifiers present unique challenges due to the harsh environment they operate

within. They see wide ranges of temperature, antenna mismatch, input voltage and mechanical shock.

Efficiency is one of the most important factors in mobile amplifier design. Battery capacity in a handset is limited and must be shared with other parts of the phone that consume power such as the processor and display. The market is highly competitive and phone vendors make purchasing decisions on peak efficiency differences as small as a few percent. A high efficiency amplifier will increase the talk time and reduce the need to charge the phone frequently. Phone customers are sensitive to these issues and continue to demand longer talk time and battery life. The blue trace in Figure1-1 shows the efficiency of a 3rd generation (3G) amplifier as a function of drive. The efficiency is very low at low power levels and increases to 40% at the peak linear power of 28dBm.

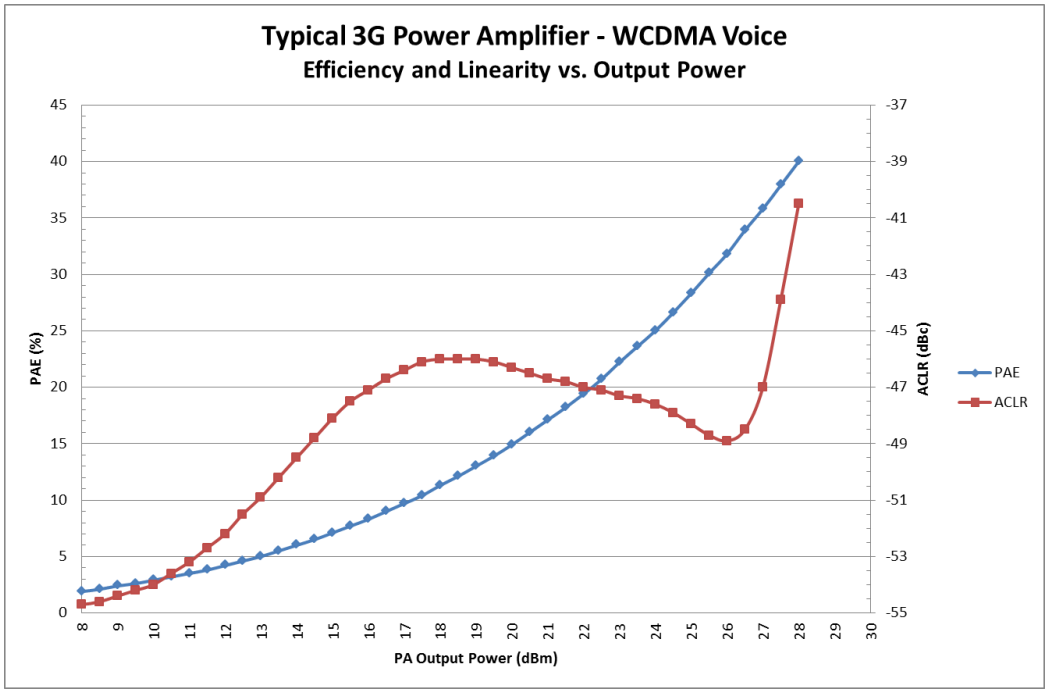


Figure 1-1 - 3G Amplifier Efficiency and Linearity

The behavior of increasing efficiency with increased power continues beyond 28dBm, but the linearity will degrade beyond a usable level. The linearity of the device is decreasing rapidly as power increases as is shown by the red trace in Figure 1-1. It is the linearity limitation that prevents power from being increased. The traces in Figure 1-2 show the efficiency and linear output power for seventeen 3G power amplifiers from four different vendors. The figure contains two groupings. The grouping captured in the blue circle use a balanced amplifier topology.

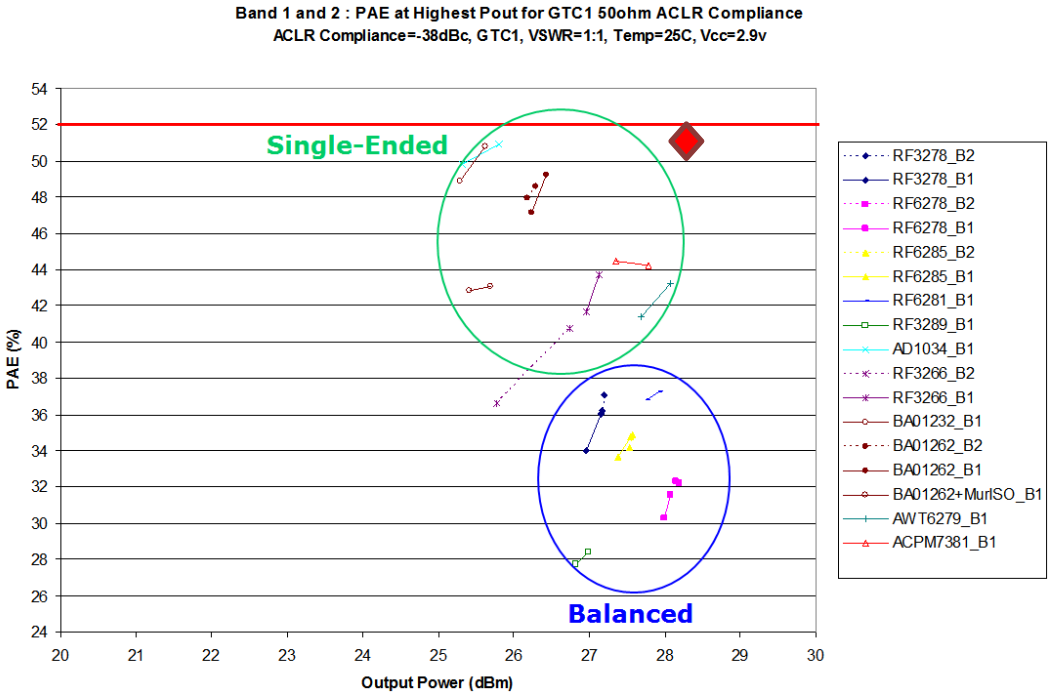


Figure 1-2 – Peak Efficiencies of Various 3G Amplifiers

Balanced amplifiers are valued for the ability to maintain performance into a wide range of load impedances, but the load insensitivity comes at the expense of peak efficiency. Because the balanced topology has compromised peak efficiency and is a shrinking part of the market it will

not be focused on for this research. The groups of traces circled in green are from amplifiers with a single ended topology. This means the amplifier stages are in a common emitter configuration with one signal path. It is clear to see the relationship between output power and peak efficiency. The amplifiers with the highest peak efficiency have the lowest linear output power capability. For example the trace labeled BA01262_B1 exhibits the highest overall peak efficiency (49% - 51%), but the lowest overall linear output power (25.3dBm - 25.6dBm). This relationship is in part due to impedance matching losses. Design changes to improve the power capability will reduce the efficiency. The 3GPP specification for handsets[3] allows for a maximum of 24dBm of antenna transmit power. Switch and filter losses after the PA but before the antenna are in the range of 2.5dB to 3.5dB. The low output power high efficiency amplifiers are only usable in niche applications where power class rating is reduced. Phone vendors would like amplifier performance at a level denoted by the red diamond on Figure 2. The diamond marks a performance level of Pout=28dBm, PAE ≥ 50%, and ACLR ≤ -38dBc.

Up to this point the focus has been on linearity of a PA excited by a WCDMA voice signal. Mobile handsets are increasingly used as data devices. The modulation required to transmit high speed data puts more linearity demand on the power amplifier. Figure 1-3 shows the relationship between several different 3G/4G waveforms in terms of the peak signal strength relative to the average signal strength. The colored

bars for each waveform show the percentage of the time a waveform spends above the average power level. As a specific test case let's look at the HSDPA signal which is the second group from the left. Assume an amplifier with an average output power of 27dbm. The chart indicates that 10% of the time the signal level would be at or above 29.6dBm, 1% of the time the signal would be at or above 30.3dBm, 0.1% of the time at or above 30.5dBm, and 0.01% of the time at or above 30.8dBm.

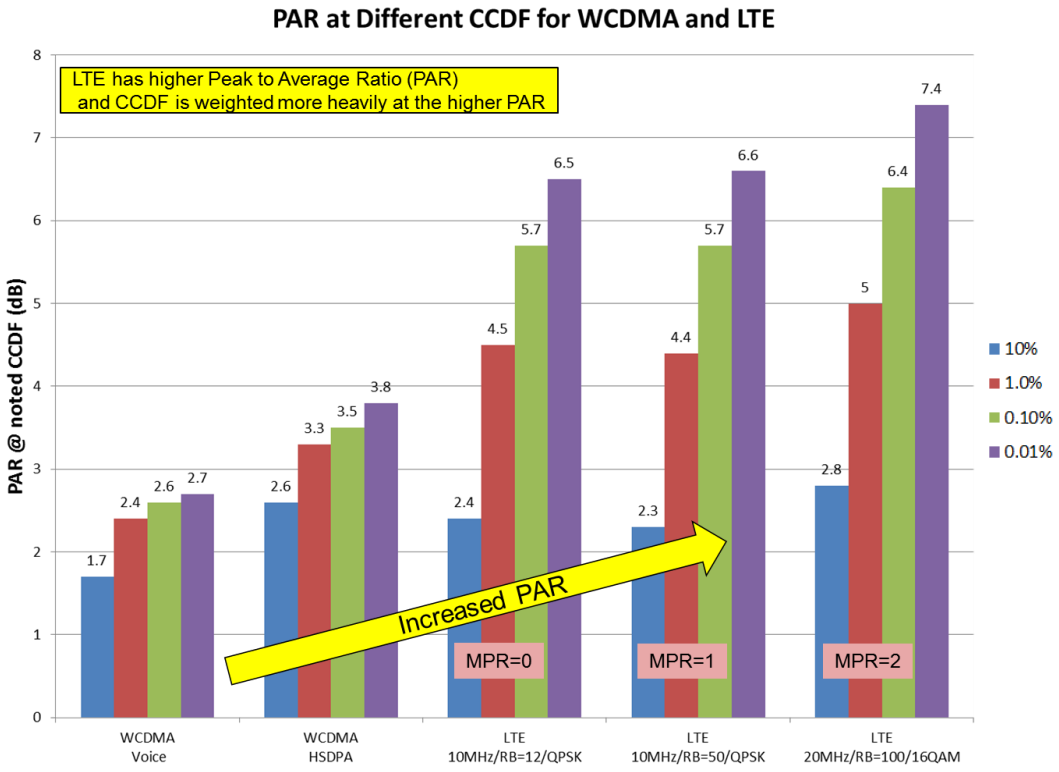


Figure 1-3 – Peak to Average Signal Ratio for 3G/4G Waveforms

A linear amplifier that is used with a high PAR signal must be operated at a lower power than with a low PAR signal to maintain the same linearity. Figure 1-4 is a chart of a 3G amplifier operated with

several different modulation formats. This amplifier was designed for WCDMA voice signals and has linearity better than -39dBc at an output power of 28dBm. To meet the same -39dBc linearity target with a 5MHz, 25 resource block LTE signal the output power must be reduced by 2dB. Referencing Figure 1-1, we can see the peak efficiency is reduced by 7.5% if the output power is lowered by 2dB. Similar behavior is observed for any power amplifier. The further away from the peak power the amplifier is operated, the lower the efficiency will be. The future evolution of the

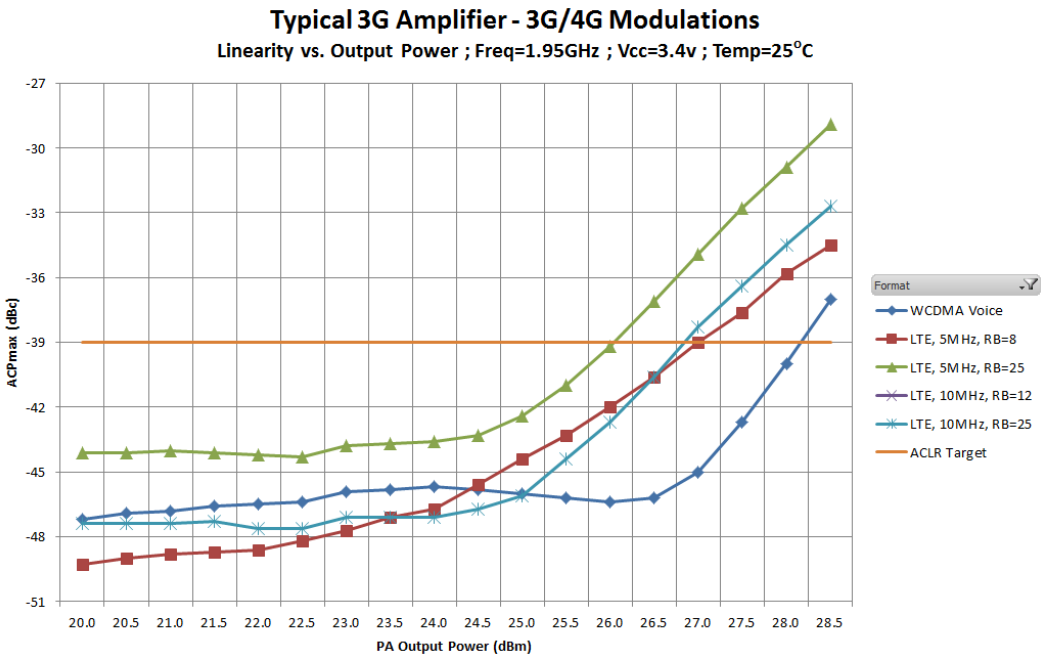


Figure 1-4 – 3G Linearity with 3G/4G Waveforms

cellular infrastructure ensures reduced peak efficiencies in handsets if no other changes are made. Even with high upfront cost of upgrading existing 3G networks to 4G networks and the known penalties to efficiency

network providers like Verizon, AT&T, and T-Mobile are quickly making the transition. There are several motivating factors. The first is spectral efficiency. It is estimated LTE will increase spectral efficiency by a factor of 2-4 (bps/Hz) over 3GPP Release 6[4]. With the cost of frequency spectrum in the billions of dollars it is a tremendous financial advantage to increase the number of users and data that can be fit into a unit of bandwidth. Other motivating advantages for 4G LTE networks are improved latency, scalable bandwidth (1.4, 3, 5, 10, 15, 20 MHz), and peak data rate.

	Downlink (20 MHz)		Uplink (20 MHz)		
Unit	Mbps	bps/Hz	**Unit**	Mbps	bps/Hz
Requirement	100	5.0	**Requirement**	50	2.5
2x2 MIMO	172.8	8.6	**16QAM**	57.6	2.9
4x4 MIMO	326.4	16.3	**64QAM**	86.4	4.3

Table 1-1 – LTE Uplink/Downlink Requirements

The design of a market competitive power amplifier is a mix of analytical and empirical design techniques. Each method has its own inherent set of strengths and weaknesses, and they work in a complementary fashion. Amplifiers exhibit many nonlinear effects making high level high accuracy models difficult to produce. Additionally many sub elements that make up the design are incompletely modeled from an electrical standpoint (for example SMT components, switches, bond wires, and filters). Aspects of the modeling process can be improved by careful

measurement of the individual sub elements and use of the best simulation tools available such as 3D EM solvers, harmonic balance, envelope, and transient circuit simulators, and multi-port linear / nonlinear vector network analyzers.

However, even if it was possible to perfectly measure each element or sub-element that was used in a design, an important aspect of the model is missed when the pieces are put together. The electrical interaction between parts due to their close proximity is not possible even in principle without detailed information of the interior structures of the parts. Figure 1-5 shows an example layout of a power amplifier matching network. To simulate the coupling effect between the two capacitors located in the center of the picture or the coupling between one of the capacitors and the nearby bond wires the designer would need to use a full 3D solver, and know the location, size, thickness, and metal composition of all of the plates inside the capacitor as well as the electrical properties of the dielectric material.

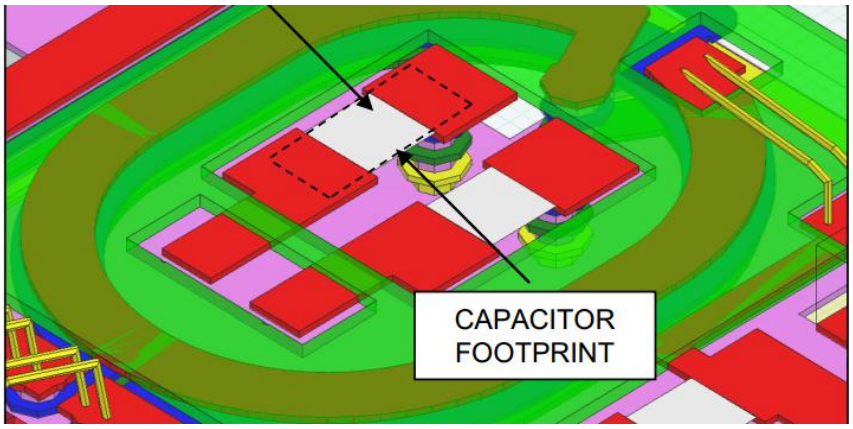


Figure 1-5 – Physical Circuit Feature Proximity

Details like these are not obtainable in practice. Even if the details were obtainable, the computational time and cost becomes prohibitive as the model complexity increases to include these interactive effects. It can take days to setup a complicated simulation and days to run the simulation. Making small changes in the model can take hours of additional simulation time to update the results. In contrast it can take only minutes or seconds to achieve an answer by performing a lab experiment. Thus, the empirical aspect of amplifier design is not going away in the foreseeable future, but simulation still has a strong role to play. The secondary goal for this research is to clearly demonstrate how simulation can be used in a productive way to identify sensitivities in a design and understand the important aspects of large signal behaviors that arise during the development process along with the impact of thermal effects on the design.

The thesis is organized as follows. Chapter 2 covers the background required to understand amplifier performance. Chapter 3 discusses the details of the amplifier design with a special emphasis on the interstage matching network . The interstage match is performed in a novel way to enhance the amplifier efficiency. Chapter 4 presents full simulation results and compares measured and modeled results. Chapter 5 outlines potential future work as a follow up to the research from this thesis.

Chapter 2

SETION 1: LINEARITY

At its output, an ideal amplifier produces a linearly scaled version of the signal applied to its input. Mathematically we can express the time domain relationship of the voltage gain as the function:

$$\mathrm{Vout}(V_{in}) = a_1 \cdot V_{in}$$

Real world amplifiers add distortion products in addition to scaling the input signal. These added signals are related to the input signal and can be expressed in general as the function:

$$\mathrm{Vout}(V_{in}) = a_0 + a_1 \cdot V_{in} + a_2 \cdot V_{in}^{2} + a_3 \cdot V_{in}^{3} + \ldots + a_n \cdot V_{in}^{n}$$

This is commonly referred to as the polynomial model or the Volterra series model. Observe that in both of these functions the term V_{in} is a sinusoidal signal with amplitude, frequency, and phase components. For example:

$$V_{in} = V \cdot \sin(2 \cdot \pi \cdot f \cdot t + \phi)$$

Where V is the voltage amplitude of the input signal in volts, f is the frequency of the signal in Hertz, t is the time in seconds, and ϕ is the phase of the signal in radians. In an example like this with a single sinusoid, the distortion is seen in the frequency domain as multiples of the

input frequency and are referred to as harmonics. All frequency content will be at f, 2f, 3f, 4f, and so on. Harmonic distortion of this type is easy to deal with by using filtering to reject the unwanted parts of the signal. Because of the wide separation in the frequency domain it is possible to have an amplifier with large values of a_2, a_3, …, a_n. and still produce an output very much like the ideal amplifier by including a high rejection low pass filter after the amplifier before the load.

In communication systems the input signal is not as simple as single sinusoid and typically has frequency content at more than one frequency. Consider a simple case with two sinusoids where ϕ=0.

$$V_{in} = V_1 \cdot \sin(2 \cdot \pi \cdot f_1 \cdot t) + V_2 \cdot \sin(2 \cdot \pi \cdot f_2 \cdot t)$$

When this definition of V_{in} is substituted back into the polynomial and then expanded the model predicts spectral content at frequencies related to the harmonics of f_1 and f_2 added and subtracted from each other. This process is called intermodulation distortion and is abbreviated IMD. In general intermodulation products will be at frequencies $m \bullet f_1 + n \bullet f_2$, where m and n are integer numbers and will depend on the exponent considered in the polynomial model. If the third order term is considered in the case $V_1=V_2=1$ the following terms are part of the expansion.

$$\frac{3}{4}\cos\left[2 \cdot \pi \cdot (2 \cdot f_1) \cdot t - 2 \cdot \pi \cdot (f_2) \cdot t\right] \qquad \frac{3}{4}\cos\left[2 \cdot \pi \cdot (2 \cdot f_2) \cdot t - 2 \cdot \pi \cdot (f_1) \cdot t\right]$$

If f_1 and f_2 are very close in frequency the $2f_1 – f_2$ and $2f_2 – f_1$ terms will fall very close to the two fundamental terms f_1 and f_2. These types of distortion products are often within the pass band of the amplifier, and hence are difficult or impossible to eliminate by using filtering. Figure 2-1 shows all of the 3rd order IMD products for the two signal test case $\omega_1=2\pi f_1$ and $\omega_2 = 2\pi f_2$.

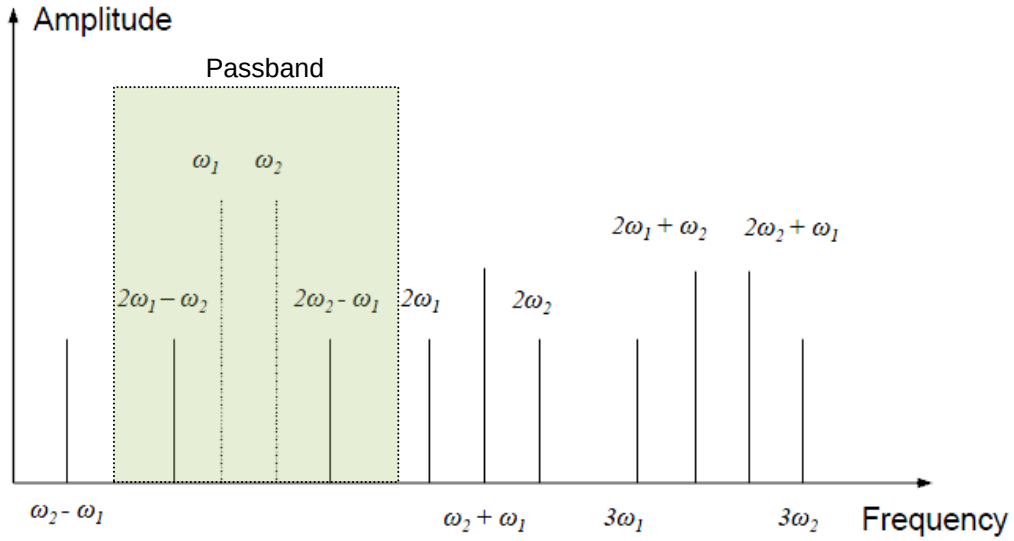


Figure 2-1 – Amplifier 3rd Order IMD Products

Higher order terms from the polynomial model will continue to add frequency content at intervals of f1 – f2. These terms require the mixing of products at higher frequencies where the active device gain is lower and the polynomial coefficients generally become smaller as n becomes larger. Because of this the 3rd order IMD products are almost always the strongest with each subsequent product getting smaller. A common way to quantify the linearity of a power amplifier is to compare level of the

intermodulation product to the level of fundamental signal. An examination of the polynomial model shows that as Vin increases the higher order V_{out} terms will increase faster than the fundamental V_{out} term because they are proportional to V_{out}^2, V_{out}^3, …, V_{out}^n. Figure 2-2 is a graph of output power as a function of input power for the fundamental tone the 2nd order products, and 3rd order products. At low power levels the output of the fundamental tone increases with the input power level by a ratio of 1:1 in dB. The 2nd order increases at a 2:1 ratio in dB and the 3rd order increases at a 3:1 ratio in dB.

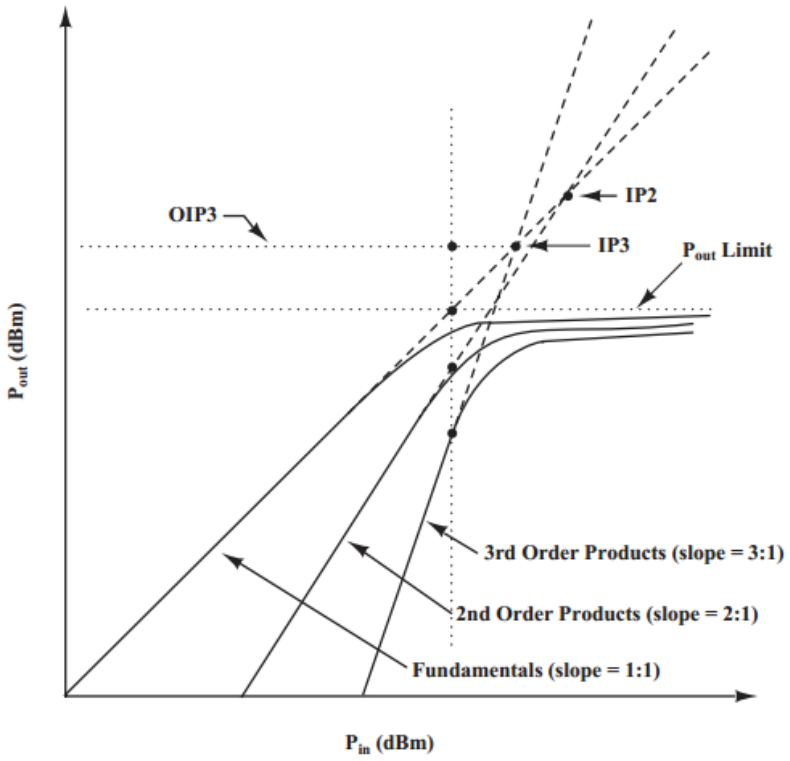


Figure 2-2 – 3rd order intercept (IP3)

Given these fixed relationships we can extrapolate to a theoretical point where the 3rd order products would be equal in power to the fundamental

tone. This is shown in Figure 2-2 as IP3, and the dotted lines illustrate where the lines would intersect if there were no other nonlinear mechanisms to restrict the growth of the fundamental and IMD products. In practice the P_{out} Limit in Figure 2-2 is reached long before the IP3/OP3 intersection occurs. The output power limit is caused by output voltage clipping and/or maximum current capacity of the active device. The OP3 can be calculated by using the following formula which is based on the slope relationships between the IMD and fundamental.

$$OP3(dBm) = Pout(dBm) + \frac{IMD(dBc)}{2}$$

OP3 is often used as a figure of merit because the higher the OP3 the higher the linear output power of the amplifier. OP3 is especially easy to calculate because it only requires a single 3rd order dBc measurement in addition to knowing the output power. Care must be taken to ensure the amplifier is in a power range where the fixed slope relationships exist. At very low and high power levels nonlinearity effects can change the relative IMD power levels, so extrapolating to the OP3 can lead to erroneous conclusions. Although IP3/OP3 is sometimes used in cellular PA design a variation of this concept is more common. An amplifier is generally designed with a goal for the output power. The designer works to achieve a targeted linearity at the rated output power. A 3rd order IMD level of -30dBc is considered acceptable for many applications. The OP3 in dBm would then be P_{out}(dBm) + 15dB.

All of the proceeding analysis assumes the output of the amplifier at any instant in time is ONLY dependent on the present input of the amplifier at that time and the transfer function that describes the relationship between the two. In reality the output of an amplifier is also somewhat dependent on previous states and cannot fully be captured (even in principle) by the polynomial model. This phenomenon of dependency on the previous states of the amplifier is known as “memory effects”. The dominate causes of memory effects are energy storage in the device and surrounding circuit, thermal effects, and device speed limitations. The impact of memory effects in an amplifier is to cause the intermodulation products to be asymmetric and generally reduce the agreement between measured and modeled performance. The study of memory effects in amplifiers is an area of active research and a detailed analysis of them is beyond the scope of this research. In many instances they can be ignored and will only cause subtle errors in the predictions of the model. In the simulation test cases with a mathematically derived device (behavioral model) no memory effects will be present that are not captured by the simulation. When using RFMD device models some of the thermal memory effects are captured within the model and will be noted.

In modern communication systems the signals are periodic waveforms with complex amplitude and phase modulation. The waveform to be amplified is distributed over a range of frequencies and the

intermodulation distortion is also spread out over a range of frequencies. Figure 2-3 is a measurement of the output of a power amplifier that is excited by a WCDMA signal. The signal bandwidth of a WCDMA waveform is defined by the 3GPP standard as 3.84MHz and each channel is separated by a space of 5MHz. Linearity measurements for WCMDA waveforms are done by integrating the power in the main channel and comparing that to the integrated power in the adjacent channel (the next one over) above and below in frequency.

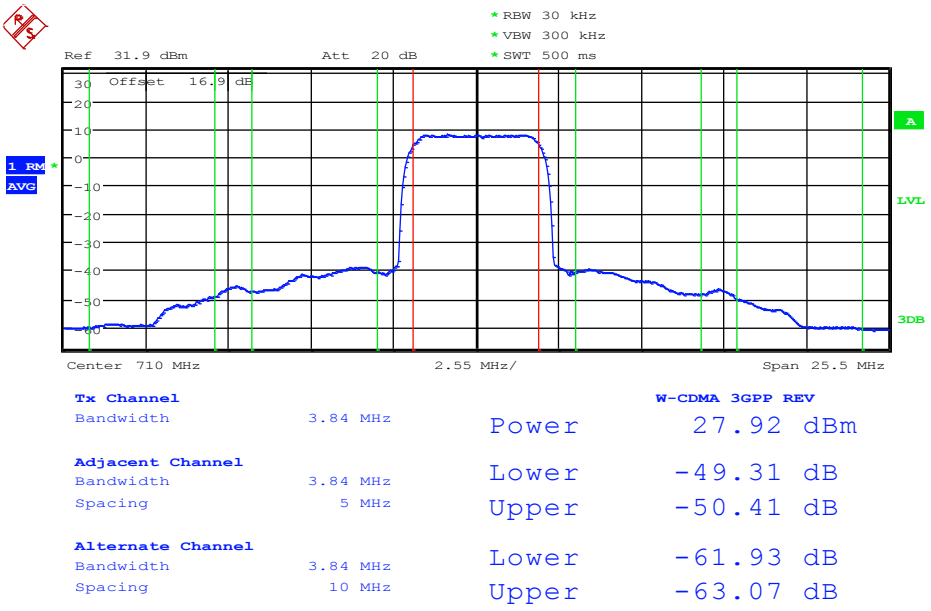


Figure 2-3 – Low Distortion WCDMA Signal

In Figure 2-3 the red lines mark the main channel power. The result is 27.93dBm and is displayed below the graph. The adjacent power can be seen in the sets of green lines on each side of the red lines. The adjacent channel power is reported as a ratio of the main channel power and is abbreviated ACLR. The signal displayed in Figure 2-3 has an ACLR

of -49.31dBc on the high frequency side and -50.41dBc on the low frequency side. ACLR system compliance for handsets in the 3GPP standard is required to be -33dBc or better. The next set of green traces are centered 10MHz from the main channel and represent channels that are two positions away. These channels are referred to as the alternate channels and are abbreviated ALT1. All channels beyond ALT1 are considered alternate channels and are distinguished from each other by incrementing the suffix. So the channels 15MHz away would be ALT2, the channels 20MHz away would be ALT3. The 3GPP system spec for leakage in the alternate channels is -43dBc. The ALT1 on the high frequency side in Figure 2-3 is -63.07dBc and -61.93dBc on the low frequency side. Notice the blue trace becomes flat about half way through the ALT1 channel. This is due to the measurement floor of the spectrum analyzer, so the signal is actually below this line which means the ALT1 level is lower than measured. This is a common metrology issue, especially when measuring modulated signals with high linearity at low power levels.

The signal plotted in Figure 2-4 represents a WCDMA waveform with very poor linearity compared to Figure 2-3. While the signal power in both graphs is the same at 27.9dBm in Figure 2-4 the power in ACLR channels is about 20dB higher and the power in ALT1 is about 10dB higher. It is easy to see the difference between the waveforms in the two figures just by looking at them. An interesting observation is the PA in

Figure 2-4 fails the 3GPP ACLR system spec by 3.5dB, but it passes the ALT1 spec with margin. The specifications are written in a way that usually ensures an amplifier that passes the ACLR specification will also pass the ALT specification.

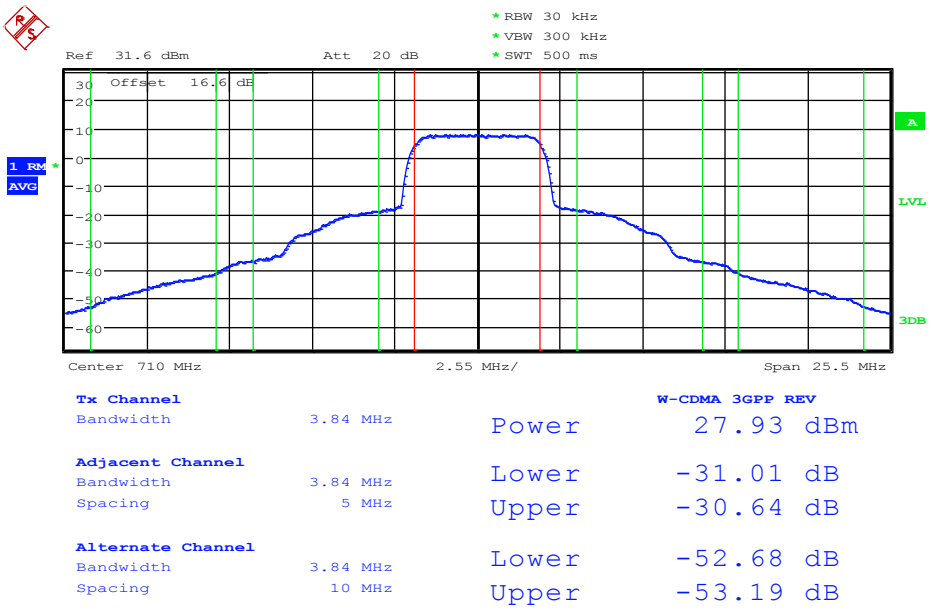


Figure 2-4 – High Distortion WCDMA Signal

ACLR and ALT performance are a concern in a mobile communications system for two primary reasons. The first reason is ALCR power can interfere with another mobile subscriber if that subscriber happens to be transmitting on the adjacent channel frequency. However, the large power difference of ≥ 33dB ensures any interference is small. The second reason is ACLR performance is a good indicator of how well a PA can amplify the signal without corrupting the digital data modulated onto the carrier. The direct way to measure the data corruption is to demodulate the data from the carrier and perform a direct assessment of

detected symbol quality such as an error vector magnitude (abbreviated EVM) measurement. EVM is a measurement that quantifies how much the actual constellation points in the signal deviate from ideal constellation points in an IQ diagram as shown in Figure 2-5[5]. Mathematically EVM is defined as:

$$EVM(\%) = \sqrt{\frac{P_{error}}{P_{ref}}} \cdot 100$$

P_{error} = RMS power of the error vector
P_{ref} = RMS power of the highest power
In the signal constellation

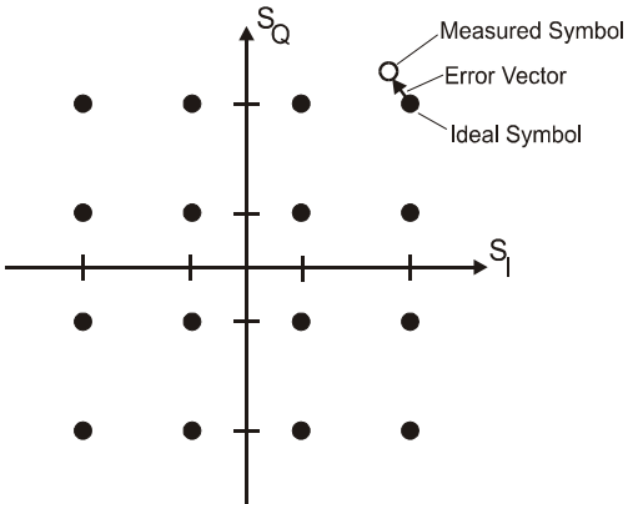


Figure 2-5 – Normalized Constellation Diagram for 16QAM

Although EVM is a more direct way to measure the data corruption there are some drawbacks that make it used less in practice for characterizing an amplifier during development. To demodulate the symbols encoded on the carrier it requires the demodulator in the receiver (usually built into the spectrum analyzer) to have knowledge of the symbols being used which adds setup complexity to coordinate between the signal source and the

demodulator. Imperfections in the demodulator itself can add uncertainty to the measurement. Measuring EVM takes more time than measuring ACLR. Although the time difference is only a few seconds for a single measurement the time can be substantial when testing hundreds of points over a wide range of conditions. The cost of adding a demodulator to a spectrum analyzer can exceed $10,000 and extra costs are incurred to demodulate different kinds of signals like IS-95, GSM, WCDMA, and LTE. These drawbacks and make EVM less useful during development and instead ACLR measurements are used more frequently to determine linearity improvements. Good ACLR performance is highly correlated with good EVM performance so once one is achieved the other can be confidently assumed to be achieved as well.

One final method for evaluating linearity will be discussed. This method is known as AM-AM and AM-PM distortion. AM is an abbreviation for amplitude modulation and PM is an abbreviation for phase modulation. AM-AM describes how the ratio of input and output power changes vs. drive level and is identical to a gain compression measurement. AM-PM describes how the phase changes in an amplifier as a function of drive level.

Figure 2-6 shows both AM-AM and AM-PM responses for a very linear amplifier that is driven into compression. Both the AM and PM traces are constant until the PA starts to go into compression. The AM-PM characteristic also begins to change around 23dBm where increases

in output power will cause the phase shift through the amplifier to change. In real amplifiers this change can be much larger due to bias level shift and nonlinear capacitance at the output of the device. AM-AM and AM-PM behavior is very useful in designing and understanding amplifiers that are used with signals that have amplitude and phase components. The two characteristics are very easy to measure and simulate which makes them straightforward to compare. ACLR levels can also be quickly and accurately estimated based on AM-AM and AM-PM profiles[6].

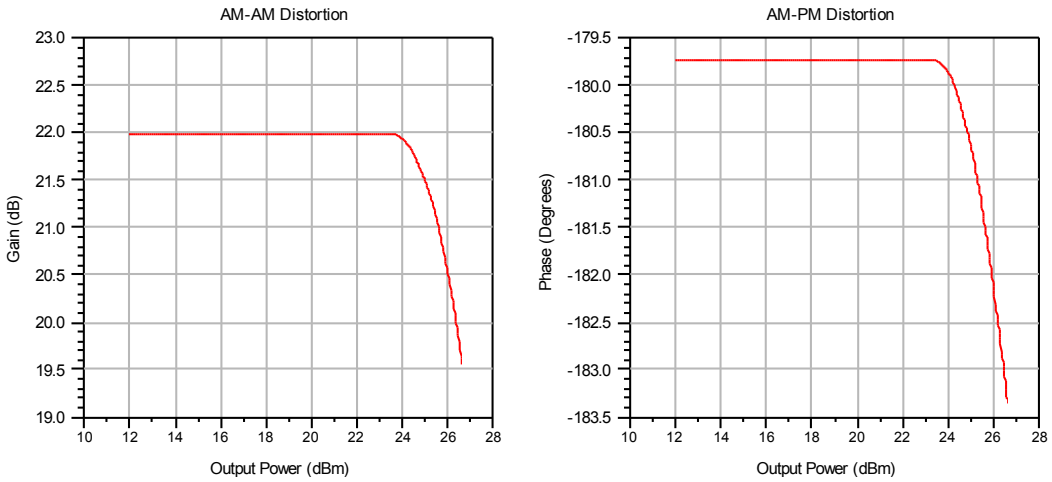


Figure 2-6 – AM-AM and AM-PM Distortion Plots

We have seen there are numerous ways to quantify the linearity of an amplifier. Polynomial/Volterra models, IP3/OP3, ACLR/ALT, EVM, and AM-AM / AM-PM have all been discussed. To quantify the linearity of a simulated and measured amplifier in this thesis we will use a combination of approaches. The polynomial model is useful for pedagogic reasons in simple examples, but very quickly can become intractable to solve more

complex waveforms and circuits. It is also difficult to compare two different Volterra models because the coefficients are in general complex and there is no consensus on how to systematically do so. Volterra models also numerically explode if used to predict performance outside their characterization range. EVM has issues that have been discussed earlier in this chapter and will not be used to characterize performance. IP3 and OP3 also will not be used because they don't offer more information than measuring IMD or ACLR at a fixed power level. In the simulation environment the preferred method will be to perform power sweeps to establish AM-AM and AM-PM profiles. From these profiles ACLR/ALT profiles vs. output power can be calculated. This makes it simple to compare different devices and amplifier circuits by looking at the power level of interest on the power drive up curve. This method will be explored in more detail later in this chapter. This method also provides a convenient way to compare simulation to measured results since ACLR/ALT power drive up measurements can be taken quickly and easily.

SETION 2: DEVICE MODELS

Two different approaches will be taken to model active devices for this research. The first method will be to develop idealized mathematical representations of active devices. These mathematical models are often referred to as behavioral models because they mimic the behavior of

active devices without considering any of the underlying physical processes that are present in a real device. The behavioral approach allows for complete insight into any simulation results since the relationships between the ports of the device are defined with a closed form mathematical expression developed during this research, so no aspect of the behavior is hidden. It is also possible to experiment by adding non ideal behavior of different types to the model and observing the changes at the circuit level. These models will be used to look at underlying principles and ideas

The second method will be to use models created by RFMD which characterize the behavior of GaAs HBT devices used in RFMD products. These RFMD models do not have complete transparency which is a drawback, but have the advantage of being developed and tested against actual devices which will be necessary to enable the comparison of a simulated amplifier to a physical amplifier. The RFMD models are a customized modification of a Gummel-Poon device model[7]. They are written in Verilog A and can be used in a variety of simulators[8]. RFMD models also include both electrical and thermal aspects. These device models will be used in the actual circuit designs.

For creating the behavioral models we will use an ideal circuit element that is called a symbolically defined device which is abbreviated SDD. This circuit component allows for explicit definitions for the current and voltage relationships between the ports. A variety of mathematical

operators are permitted including, addition, multiplication, exponentiation, logic, conditional definitions, and function references. It is a very useful element for experimenting with device models. A transistor is a three terminal device. We will use a two port SDD model with the two reference pins connected together to create the third terminal. Figure 2-7 shows the SDD mathematical model along with the pin definitions.

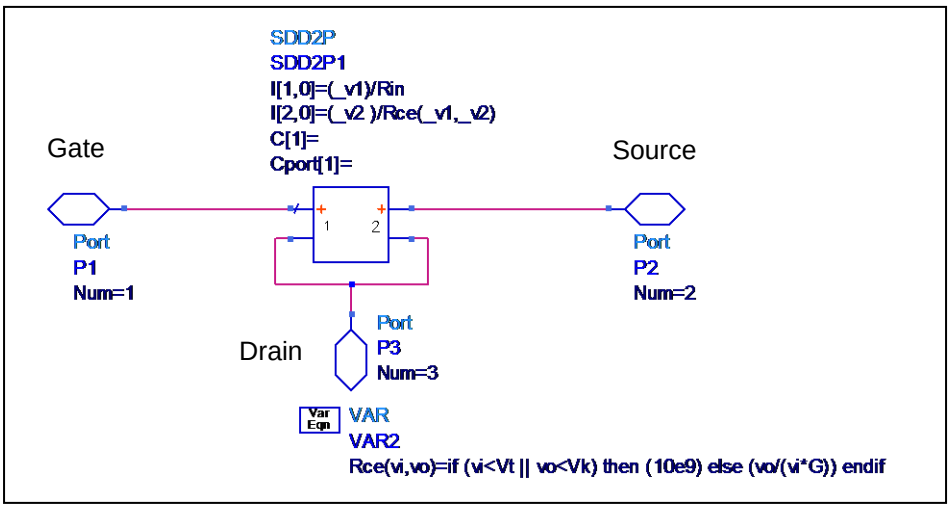


Figure 2-7 – Initial Behavioral FET Model

The Figure 2-7 device approximates an ideal FET. The model parameters are V_t (V_{gs} threshold), V_k (drain-source knee voltage), R_{in} (gate-source resistance), and G (transistor voltage to current gain in Siemens). The conditional statement that defines the resistance between the drain creates a constant current as long as V_{ds} exceeds the knee voltage and V_{gs} exceeds the threshold voltage. When the Vds is below V_k or Vgs is below V_t the drain to source resistance becomes 10 GOhms and is effectively an open circuit. In Figure 2-8 the ideal FET is attached to a curve tracer and the IV curves are shown.

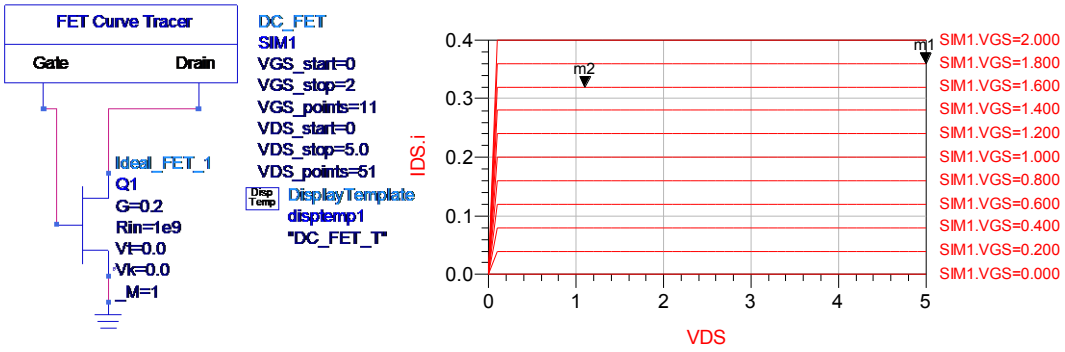


Figure 2-8 – IV Curves of Ideal FET

As expected the IV curves are perfectly flat and Ids is a function of G and V_{gs}. This ideal FET model was then used in a Class A amplifier schematic as shown in Figure 2-9. This simulation sets the FET bias point and sweeps the RF input over a range of power levels.

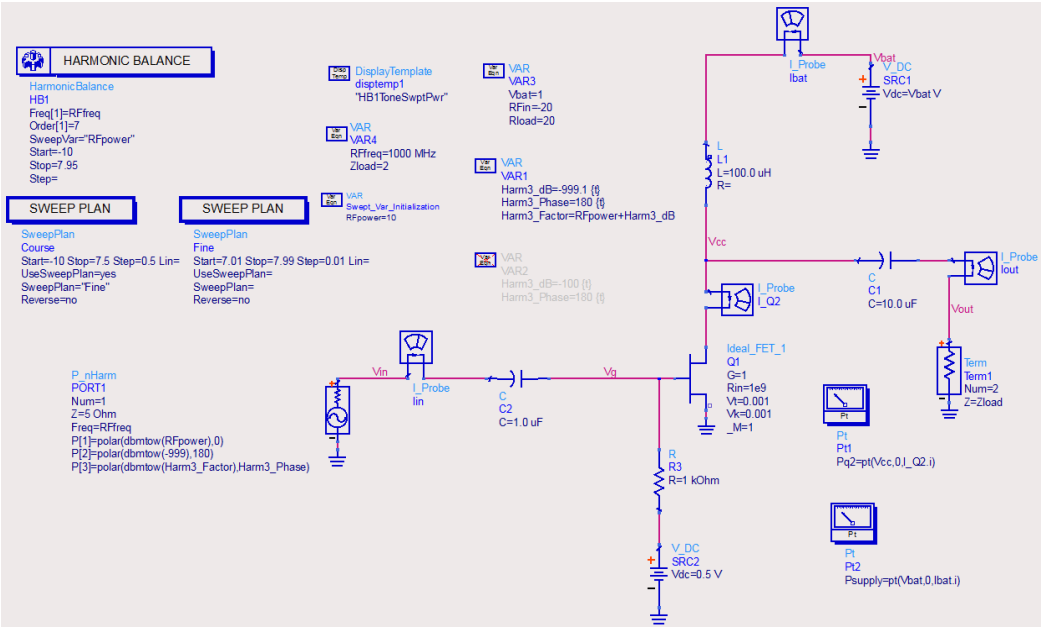


Figure 2-9 –Simulation Schematic – Class A Initial FET Model

The device gain, bias point, and the battery voltage were chosen so the device output would swing exactly between 0 V and 2 V when the RF

input was at the maximum value. The results of the simulation are shown in Figure 2-10. As expected when the voltage swing is between twice the supply voltage and ground the power delivered to the load which is 2 ohms is 24dBm (0.25W).

$$P_{load} = \frac{V^2}{R} = \frac{\left(\frac{1}{\sqrt{2}}\right)^2}{2} = 0.25W$$

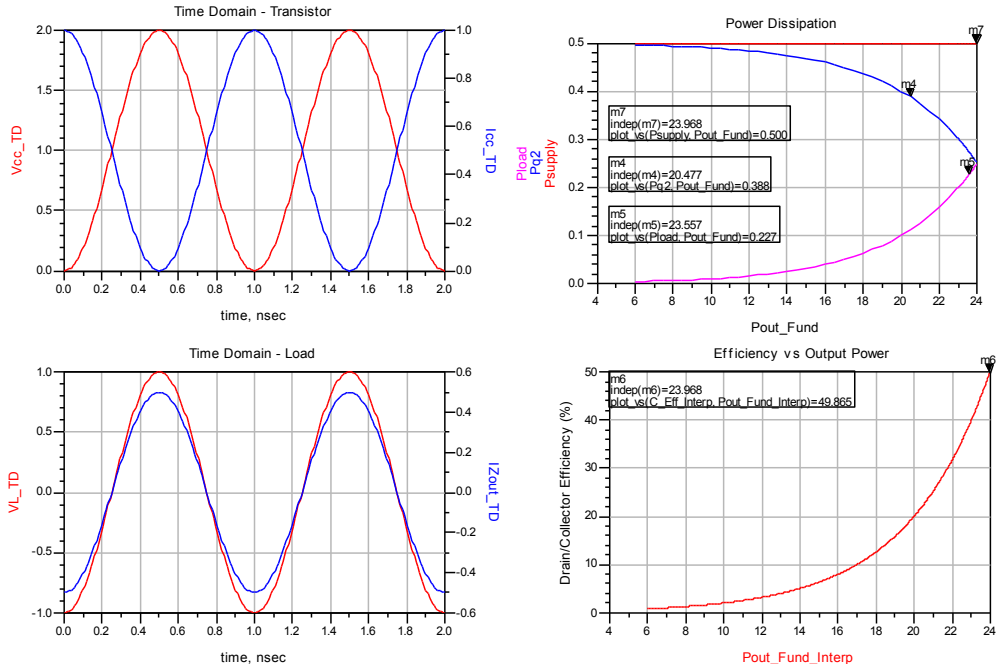


Figure 2-10 – Simulation Results – Class A Initial Model

The simulation confirms the result as shown in the upper right graph of Figure 2-10 and the efficiency as shown in the lower left graph is 50% as expected from an ideal Class A amplifier[9]. Further experimentation with the ideal FET model reveals a serious limitation to its use in PA circuits. If the input power is increased to the point the output voltage attempts to go beyond the limits of 0v ≤ Vgs ≤ 2Vbat the simulator is unable to obtain

numeric convergence for the circuit. After spending considerable time troubleshooting the issue and working with the Agilent ADS support personnel it was determined the issue was related to the discontinuities in the model at the threshold and knee voltages. The piecewise linear model works well when operating in the forward active region, but breaks down when the voltage waveform tries to clip in the areas shown by the green circles in Figure 2-11. Because the function is not differentiable between the two regions the harmonic balance engine is not able to solve the circuit.

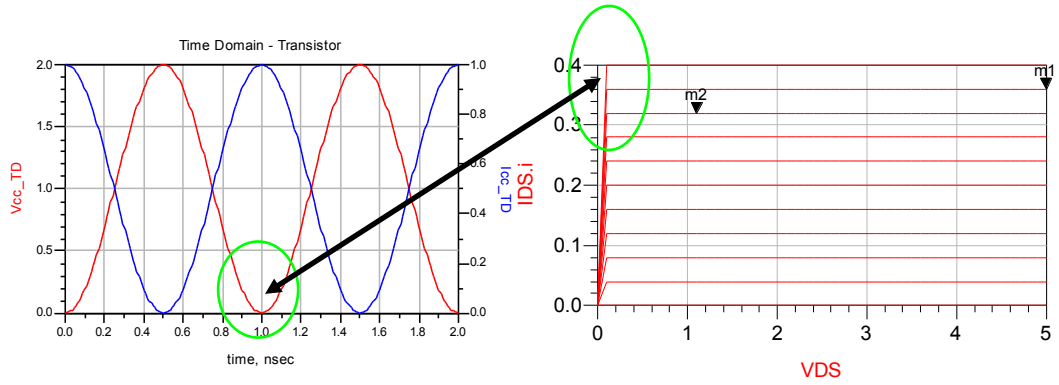


Figure 2-11 – Model Clipping and Convergence

To address the convergence issue a modification needed to be made to the model. The piecewise linear model is replaced with a piecewise exponential model. The new model uses an e^{x} function below the knee voltage and a $1-e^{-x}$ function above the knee voltage. At the knee voltage the two functions are equal so a smooth transition is created across the piecewise boundary. The new SDD model is shown in Figure 2-12. The structure of the model is unchanged to the gate, drain, and

source pins are the same as the ideal model, only the mathematical relationships between the ports are affected. A new parameter that defines the “sharpness” of the transition between conductance and cutoff is introduced. The parameter will be referred to as V_s.

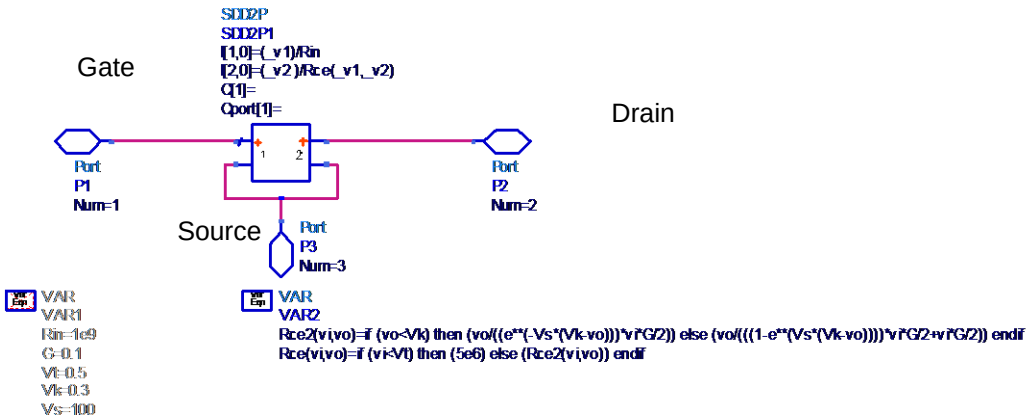


Figure 2-12 – Modified FET

Figure 2-13 is a Maple plot of the new model’s drain to source current vs. voltage with a chosen set of parameters. The sharpness factor $V_s = 2$ and enables good visibility of the transition region highlighted by the green circle.

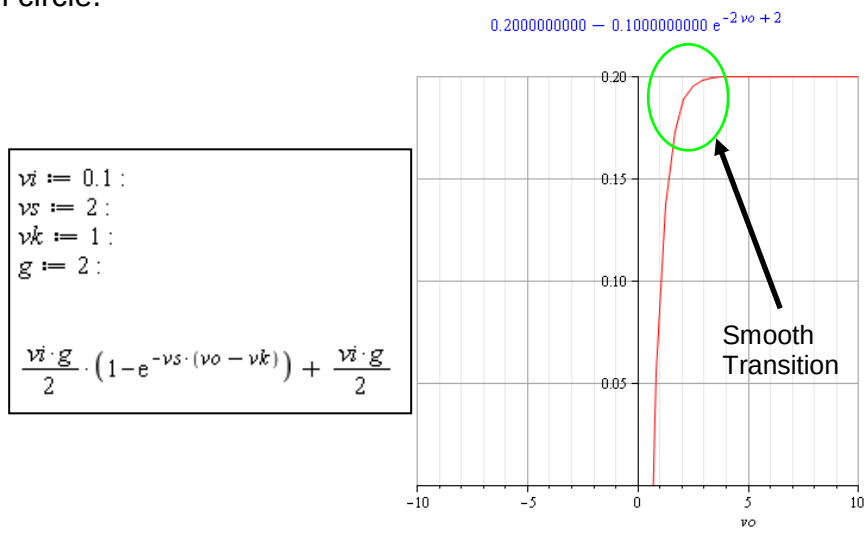


Figure 2-13 – Shape of IV Function for Modified Model

The sharpness factor was experiment with over various ranges and no convergence issues were observed. The higher the value chosen for V_s the more the new model approaches the old model. Figure 2-14 shows IV curves generated with a curve tracer for different values of V_s when V_k is set to 0.5 volts and V_{in} and V_{out} are both swept.

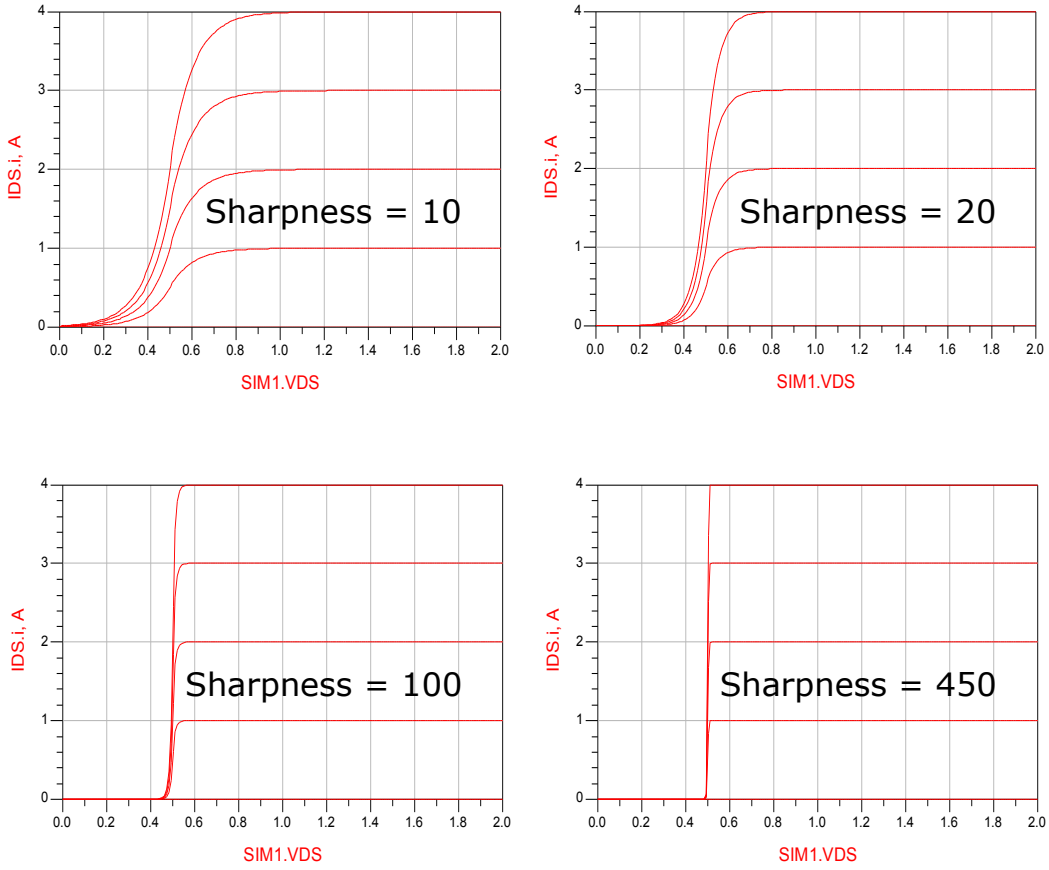


Figure 2-14 – Modified FET Model Sharpness

To determine a value of V_k to use in simulations we will insert the device into an ideal Class B amplifier circuit which is show in Figure 2-15. The gate voltage is biased to 0v so the circuit only conducts during the positive 180° of the input signal. The harmonics are then filtered at the output by a

high Q tank circuit that removes all the frequency content except the fundamental signal. The circuit was simulated over a range of powers different settings for the sharpness factor. If the device and circuit elements are ideal we should expect the peak efficiency to be of a Class B amplifier to be π/4% which is approximately 78.5%.

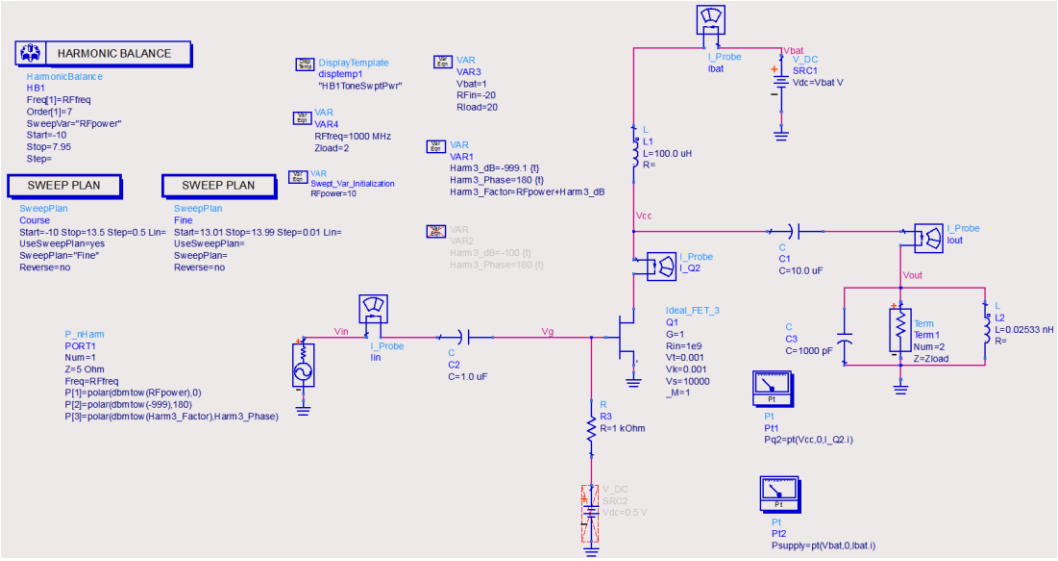


Figure 2-15 – Class B Amplifier

The peak efficiencies predicted by the simulator is summarized in Table 2-1. When the sharpness factor is 5 the simulated efficiency is 12.4% below the theoretical value but when V_k = 200 the efficiency is only 1% below the theoretical limit. Increasing V_k to 10,000 gives a result that

V_k	5	10	50	100	200	500	1000	10K	100K
Class B Efficiency	66.10%	69.80%	75.80%	76.89	77.50%	77.90%	78.10%	78.30%	78.35%

Table 2-1 – Class B PAE vs. Sharpness Factor V_k

is only 0.2% less than π/4%. The simulation time starts to increase noticeably as the sharpness goes above 10,000 but the efficiency

increases very slowly. Based on the results from the family of simulations a sharpness factor of 10,000 will be used in subsequent simulations.

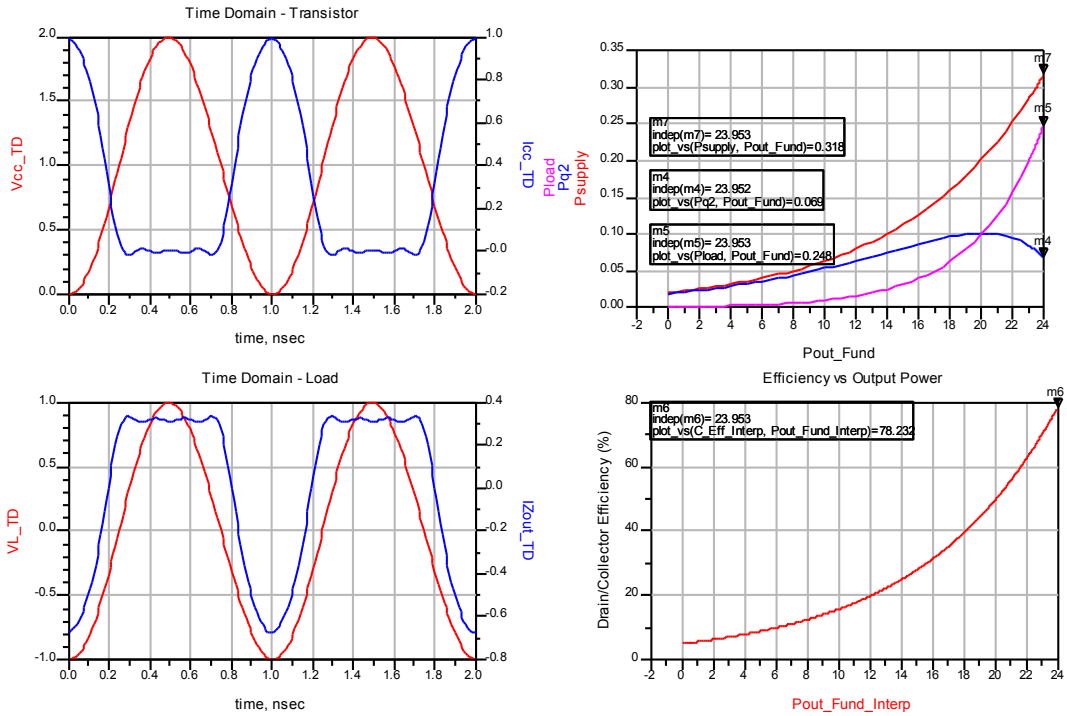


Figure 2-16 – Simulation Results – Class B Improved FET Model

Figure 2-16 is the simulation result from schematic depicted in Figure 2-15 with the improved FET model and the sharpness set to 10,000. The efficiency, supply current, and delivered power are shown on the right two graphs and the time domain waveforms of the voltage and current are shown in the left two graphs at the collector and load reference planes. As expected the device only conducts current for the positive 180° portion of the voltage waveform giving excellent agreement between the circuit model and theoretical target.

SETION 3: ACLR ESTIMATION

Linearity is an important aspect of the overall performance of a handset amplifier. As mentioned previously in this chapter we will be using ACLR measurements for comparisons between amplifiers and as a metric when optimizing performance. Agilent ADS has an envelope simulator which can be used to determine the ACLR level of an amplifier. Unfortunately envelope simulations require extreme amounts of time and computer power to solve anything more than a simple circuit. We need to calculate the ACLR on a full two stage amplifier module which will include electromagnetic characterization of the substrate. On a real world problem like this, the envelope simulation can only be used for verification of a design, not synthesis.

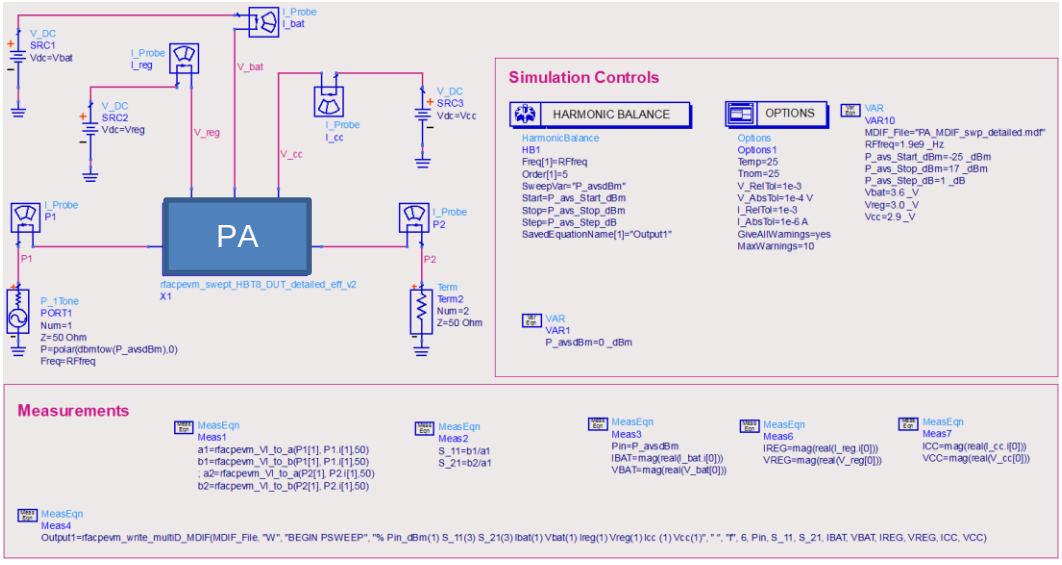


Figure 2-17 – Power Amplifier AM/AM- AM/PM Characterization

The technique to be used for ACLR simulation will be an approach that combines the harmonic balance simulator and the envelope simulator[10].

The first step in this alternate approach is to perform a harmonic balance analysis on the amplifier over a range of power levels. Figure 2-17 shows the ADS schematic used for the power sweep. The details of the power amplifier circuit are in the blue block labeled “PA”. It is important to sweep the harmonic balance simulation over a range of powers wide enough to establish WCDMA results. This means the peak to average ratio of the waveform must be considered. In the case of a WCDMA voice signal this requires a harmonic balance result 4dB higher than the highest average WCDMA power and 26dB below the lowest average WCDMA power. At each power level large signal S Parameters are calculated around the large signal operating point[11], and written to a file along with the supply voltages and currents. This file is referred to as an MDIF and is created with the measurement equations in the red box at the bottom of Figure 2-17.

The text from the characterization of a single stage amplifier is shown in Figure 2-18. After the MDIF file is created a second schematic is used to simulate the ACLR performance which is shown in Figure 2-19. This schematic reads the data from the MDIF file created by the first schematic. The S Parameters are converted to Y Parameters and then used in an ADS FDD block.

PA_MDIF_swp_detailed.mdf

```
BEGIN PSWEEP
% Pin_dBm(1) S_11(3) S_21(3) Ibat(1) Vbat(1) Ireg(1) Vreg(1) Icc (1) Vcc(1)
-23.000000 -0.118836 0.253473 1.046754 5.181013 0.002978 3.600000 0.002478 3.000000 0.060042 2.900000
-22.500000 -0.118840 0.253466 1.046823 5.181041 0.002978 3.600000 0.002478 3.000000 0.060064 2.900000
-22.000000 -0.118844 0.253457 1.046900 5.181071 0.002978 3.600000 0.002478 3.000000 0.060090 2.900000
-21.500000 -0.118849 0.253448 1.046987 5.181106 0.002978 3.600000 0.002478 3.000000 0.060118 2.900000
-21.000000 -0.118854 0.253437 1.047085 5.181145 0.002979 3.600000 0.002478 3.000000 0.060150 2.900000
-20.500000 -0.118860 0.253425 1.047194 5.181188 0.002979 3.600000 0.002478 3.000000 0.060186 2.900000
-20.000000 -0.118867 0.253411 1.047316 5.181237 0.002979 3.600000 0.002478 3.000000 0.060227 2.900000
-19.500000 -0.118874 0.253396 1.047454 5.181292 0.002980 3.600000 0.002478 3.000000 0.060272 2.900000
-19.000000 -0.118883 0.253379 1.047607 5.181354 0.002980 3.600000 0.002478 3.000000 0.060322 2.900000
-18.500000 -0.118892 0.253360 1.047780 5.181423 0.002980 3.600000 0.002478 3.000000 0.060379 2.900000
-18.000000 -0.118903 0.253339 1.047973 5.181501 0.002981 3.600000 0.002478 3.000000 0.060443 2.900000
-17.500000 -0.118915 0.253315 1.048189 5.181589 0.002981 3.600000 0.002478 3.000000 0.060515 2.900000
-17.000000 -0.118928 0.253288 1.048432 5.181688 0.002982 3.600000 0.002478 3.000000 0.060595 2.900000
-16.500000 -0.118943 0.253258 1.048703 5.181799 0.002983 3.600000 0.002478 3.000000 0.060685 2.900000
-16.000000 -0.118960 0.253225 1.049007 5.181925 0.002983 3.600000 0.002478 3.000000 0.060786 2.900000
-15.500000 -0.118978 0.253187 1.049347 5.182064 0.002984 3.600000 0.002478 3.000000 0.060900 2.900000
-15.000000 -0.118999 0.253145 1.049728 5.182223 0.002985 3.600000 0.002478 3.000000 0.061027 2.900000
-14.500000 -0.119022 0.253098 1.050154 5.182402 0.002986 3.600000 0.002478 3.000000 0.061170 2.900000
-14.000000 -0.119048 0.253045 1.050630 5.182604 0.002987 3.600000 0.002478 3.000000 0.061330 2.900000
```

Figure 2-18 – Large Signal Characterization Data

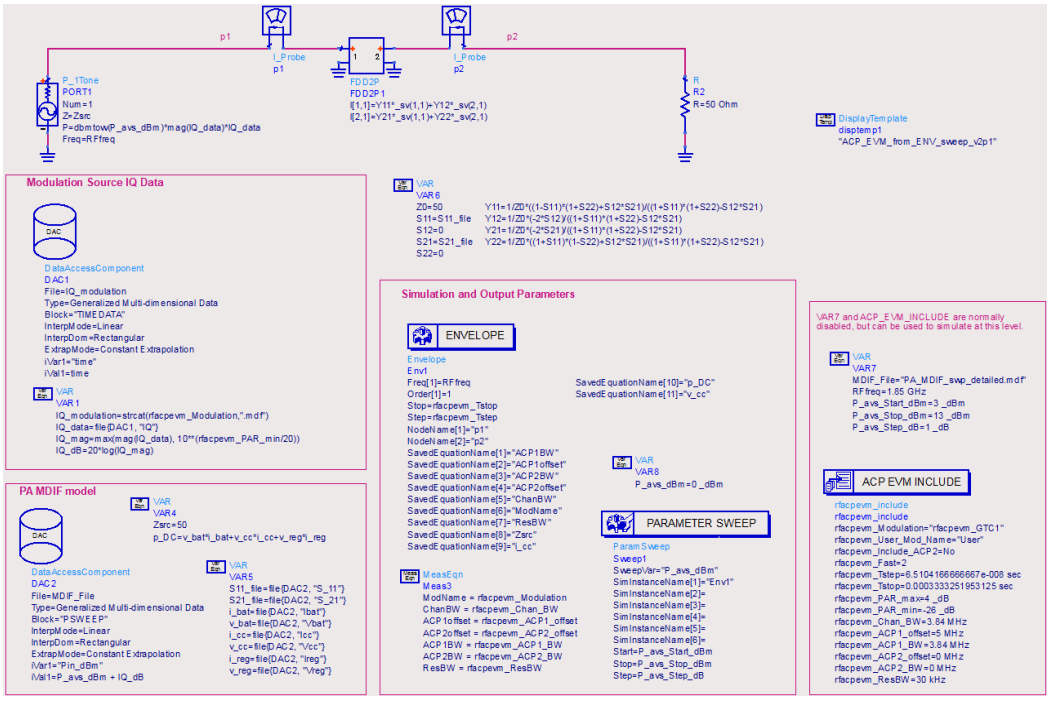


Figure 2-19 – WCDMA Simulation Schematic

The FDD is a multi-port device that describes current and voltage spectral values in terms of algebraic relationships of other voltage and current spectral values. It is for developing nonlinear, behavioral models that are more easily defined in the frequency domain. The envelope simulation uses the FDD which is a much simpler behavioral representation of the amplifier. The simulation results of a swept single stage amplifier using this technique are shown in Figure 2-20. AM/AM, AM/PM, gain, efficiency, ACLR, and EVM are plotted. The EVM was estimated using measurement equations based on the complementary cumulative distribution function of the modulated waveform[12]. The complementary cumulative distribution function is abbreviated CCDF and is calculated by integrating a probability density function from negative infinity to a chosen stopping point and subtracting it from one.

Using this two-step process may initially seem to be an unnecessary complication, but it has the compelling advantage of short simulation time. Figure 2-21 shows a side by side comparison of two envelope simulations. The result on the left was from a simulation done on a full two stage amplifier and the result on the right was done on an FDD representation of the same amplifier. The results are very close to each other, but the FDD version took a little over a minute to simulate and the direct envelope simulation took almost 24 hours. The envelope simulation of the full circuit can take especially long if there are any convergence problems during the simulation.

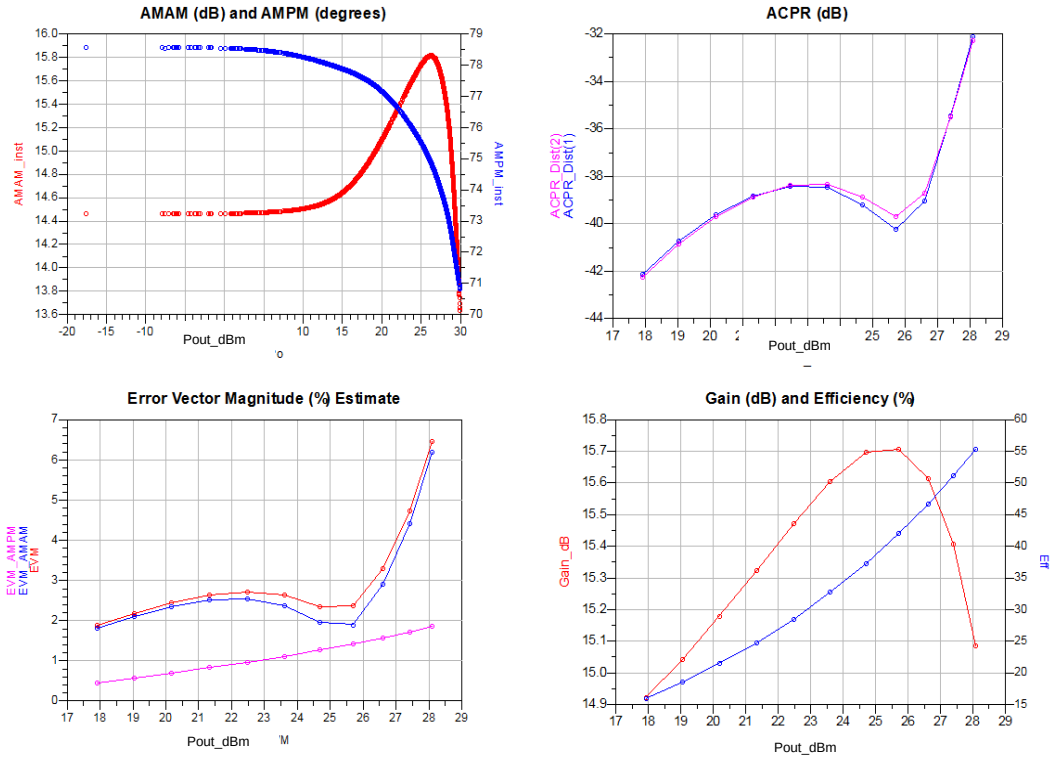


Figure 2-20 – WCDMA Voice – Simulation Results

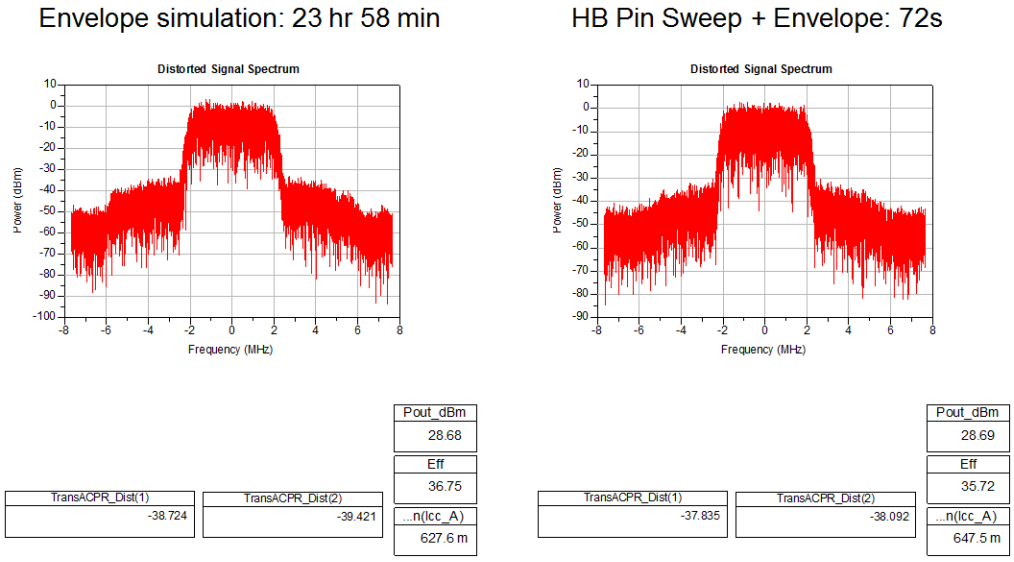


Figure 2-21 – Envelope Simulation Comparison

The tradeoffs for this faster simulation time are fairly modest. The FDD model is static and cannot capture any type of electrical or thermal memory effects. It is also not possible to cascade two models together and the user must ensure the load terminations are the identical between the harmonic balance and envelope schematics.

Chapter 3

DESIGN DETAILS

SECTION 1: OVERVIEW AND MATERIALS

Building on the concepts introduced in the first two chapters we go through the process of designing a cellular handset amplifier in detail. As mentioned in the first chapter handset amplifiers have numerous constraints related to size, cost, ruggedness, and efficiency. Many of the decisions for material and network design are related to these real world constraints and are discussed in the appropriate sections.

To begin the design process the goals for the design must be considered. A functional block diagram of the power amplifier module (also abbreviated PAM) is shown in Figure 3-1. This figure shows the main elements of the amplifier module and the connections to the pins

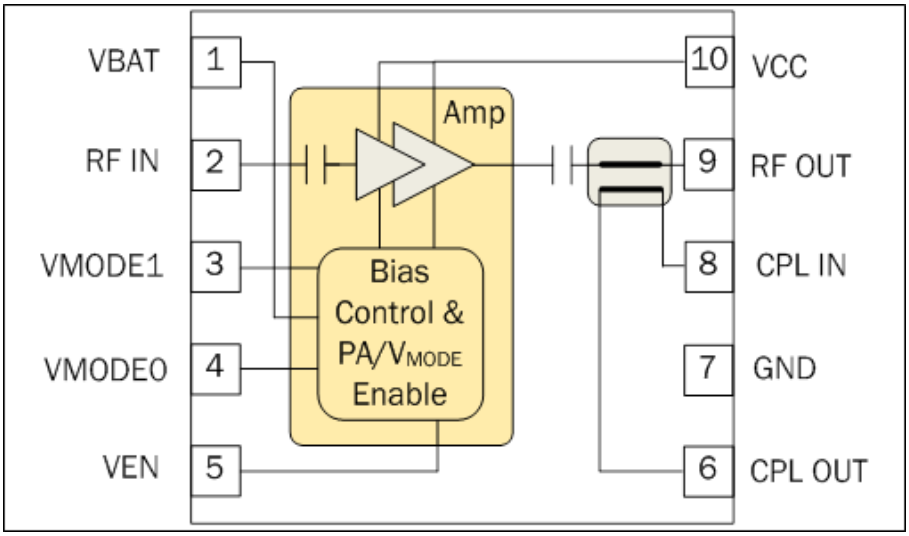


Figure 3-1 – Functional Block diagram of PAM

that are exposed to the outside world. The PAM contains a two stage amplifier, a directional coupler, and bias/control circuitry. A brief functional description of the operation for each pin is shown in Table 3-1. The bottom of the package has a large ground region which must be connected to a large ground plane for both RF performance and thermal

Pin	Function	Description
1	VBAT	Supply voltage for bias circuitry.
2	RF IN	RF input internally matched to 50Ω and DC blocked.
3	VMODE1	Digital control input for power mode selection (see Operating Modes truth table)
4	VMODE0	Digital control input for power mode selection (see Operating Modes truth table)
5	VEN	Digital control input for PA enable and disable (see Operating Modes truth table)
6	CPL_OUT	Coupler output
7	GND	This pin must be grounded
8	CPL_IN	Coupler input used for cascading couplers in series. Terminate this pin with a 50Ω resistor if not connected to another coupler
9	RF OUT	RF output internally DC blocked and matched for operation in 50Ω system
10	VCC	Supply voltage for the first and second stage amplifier which can be connected to battery supply or output of DC-DC converter
PKG Base	GND	Ground connection. The package backside should be soldered to a topside ground pad connecting to the PCB to the ground plane.

Table 3-1 – Power Amplifier Module Pin Description

dissipation. Table 3-2 is a truth table that maps the digital pins and supply voltage to the operating modes of the PAM. The Vbat pin must be tied directly to the battery of the handset and requires ≥ 3.0 V for proper operation. The Vcc pin is connected to the stage 1 and stage 2 collectors. The Vcc range is valid from 0.5 V to 4.2 V with a nominal design voltage of 3.4 V. The Vcc and Vbat pins are sometimes tied together, but are typically separated so the customer has the ability to supply voltage to Vcc with a DC-DC converter. The use of a DC-DC converter allows the handset to conserve battery current when the amplifier output is below the maximum rated power level or when the battery voltage is above the PAM

design voltage of 3.4 V. This can significantly reduce the power consumed by the amplifier at lower transmit powers especially when combined with the medium or low power mode condition.

VEN	VMODE0	VMODE1	VBAT	VCC	Operating mode
Low	Low	Low	3.0V to 4.2V	0.5V to 4.2V	Power Down Mode
Low	X	X	3.0V to 4.2V	0.5V to 4.2V	Standby Mode
High	Low	Low	3.0V to 4.2V	0.5V to 4.2V	High Power Mode
High	High	Low	3.0V to 4.2V	0.5V to 4.2V	Medium Power Mode
High	High	High	3.0V to 4.2V	0.5V to 4.2V	Low Power Mode

Table 3-2 – Power Amplifier Module Truth Table

The PAM is designed to operate in three distinct power modes referred to as high power mode, medium power mode, and low power mode (abbreviated HPM, MPM, and LPM respectively). The difference between the three modes is the quiescent bias point setting for two stages of the amplifier. In HPM the bias current is the highest and supports the highest linear power levels. In LPM the bias current is the lowest and only supports linear power levels up to 10dBm but allows the quiescent current from the battery to be as low as 5mA. The medium power mode is between these two extremes. Details for how the power modes are implemented are discussed in the section discussing the bias network design.

Before a design can be started a set of specifications that outline the performance requirements must be generated. The PAM described in this thesis is now a product in the RFMD portfolio and has a lengthy set of specifications associated with it[13]. I was the design engineer assigned to

this product. The design engineer is responsible for circuit design, simulation, die layout, laminate layout, and initial compliance testing. Exploring the complete set of compliance requirements is beyond the scope of this thesis. An abridged set of specification is given in Table 3-3.

Parameter	Specification			Unit	Condition
	Min	Typical	Max		
Frequency Range	880		915	MHz	
Vbat	+3.0		+4.2	V	
Vcc	+0.5	+3.4	+4.2	V	
Ambient Temperature	-30	+25	+85	°C	
Max Linear Pout in HPM	28.5			dBm	Vcc ≥ 3.4v
Max Linear Pout in MPM	19.0			dBm	Vcc ≥ 1.48v
Max Linear Pout in LPM	10.0			dBm	Vcc ≥ 0.84v
Gain	26	27.5	31	dBm	HPM, Pout = 28.5dBm, Vcc=3.4v
	23	24	28	dBm	MPM, Pout ≤ 19dBm, Vcc=1.31v
	18	20.5	24	dBm	LPM, Pout ≤ 10dBm, Vcc=0.76v
ACLR - 5MHz Offset		-40	-38	dBc	HPM, Pout = 28.5dBm, Vcc=3.4v
		-40	-38	dBc	MPM, Pout ≤ 19dBm, Vcc=1.31v
		-40	-38	dBc	LPM, Pout ≤ 10dBm, Vcc=0.76v
ACLR - 10MHz Offset		-52	-48	dBc	HPM, Pout = 28.5dBm, Vcc=3.4v
		-60	-48	dBc	MPM, Pout ≤ 19dBm, Vcc=1.31v
		-60	-48	dBc	LPM, Pout ≤ 10dBm, Vcc=0.76v
PAE	45	47		%	HPM, Pout = 28.5dBm, Vcc=3.4v
	35	41		%	MPM, Pout ≤ 19dBm, Vcc=1.31v
	20	22.5		%	LPM, Pout ≤ 10dBm, Vcc=0.76v
Current Drain		440	463	mA	HPM, Pout = 28.5dBm, Vcc=3.4v
		145	170	mA	MPM, Pout ≤ 19dBm, Vcc=1.31v
		58	65	mA	LPM, Pout ≤ 10dBm, Vcc=0.76v
Quiescent Current		50	70	mA	HPM, DC only
		31	50	mA	MPM, DC only
		20	33	mA	LPM, DC only
Input Return Loss			-14	dB	Pout ≤ 28.5dBm, all modes
Harmonic, 2fo		-22	-12	dBm	Pout ≤ 28.5dBm, all modes
Harmonic, 3fo		-31		dBm	Pout ≤ 28.5dBm, all modes
Coupling Factor	-18.3	-20	-22.3	dB	Pout ≤ 28.5dBm, all modes
Coupler Directivity		20		dB	Pout ≤ 28.5dBm, all modes
Temperature=+25°C, VBAT=+3.4V, VEN=+1.8V, 50Ω system, WCDMA Rel 99 Modulation unless otherwise specified					

Table 3-3 – Abridged Power Amplifier Module Specifications

The power amplifier size requirement is 3.0mm x 3.0mm x 1.0mm. The simulated PA performance and the measured performance is compared to this specification table and to each other. Table 3-3 is referenced throughout the design process when necessary.

PARAMETER	CX-50
DIELECTRIC	
Dielectric	Hitachi GEA-679FG(S) 1080 Glass, 1080+1037 Glass for 4L inner layer
Dielectric Thickness	50 ± 12.5µm
	80 ± 12.5µm for 4L (D2), 6L (D3) layer
Overall finished thickness (does not include bottom-side soldermask in total) (For higher layer count thickness estimate, add 140 µm for each 2L added)	3L – 175µm ± 30µm 4L – 275µm ± 30µm 5L – 315µm ± 30µm 6L – 415µm ± 30µm 7L -- 455µm ± 30µm
SURFACE FINISH (TOP METAL, BOTTOM METAL)	
Ni/Pd/Au Plate	Electroless Ni Electroless Pd electroless (hybrid) Au
Nickel	2-5 µm
Palladium	0.11– 0.18µm
Gold	0.07 – 0.11µm
SOLDERMASK	
Soldermask Type	Taiyo AUS-308
Soldermask Thickness	15 ± 7µm

PARAMETER	CX-50
METAL LAYER	
Copper (Trace) Thickness (measured under soldermask when layer has soldermask)	20 ± 5µm
Trace Width/Space (measured bottom of trace)	50/50 ± 8µm
Pad Width, (measured at top of pad)	± 10µm
VIA	
Size, (measured at top)	125 ± 10µm
Capture/Landing pad	200µm 225µm (in common metal)
Via copper plate	Plated solid w/copper Dimple <3µm
THERMAL VIA BARS	
Size Tolerance in either x or y	± 10µm
Capture pad Landing pad	Via Bar size + 100µm
Via surface	Dimple <3µm

Table 3-4 – CX-50 Laminate Specifications (Table from RFMD Document[14])

The specific version of the laminate material used is four layer CX-50 which is available from a variety of PCB fabrication vendors. The CX-50 laminate has dielectric properties similar to FR4 with a relative permittivity

of 4.7 in the 1 GHz and above frequency range. The loss tangent is 0.018 at 1 GHz. The outer metallization is gold which allows both soldering and bond wire attachment. Table 3-4 shows many of the process parameters in the CX-50 technology along with the minimum metal widths and spacing. Vias in this material can be thru blind or buried which allows connection from any layer to any other layer with no metal clear out required above or below the vias. This allows for an extremely dense PCB layout. In addition to normal round vias the CX-50 material offers a solid thermal via bar which is shown in Figure 3-2. The via bars are used under the active devices to lower the thermal resistance under the amplifier which allows the devices to operate at a lower temperature with the same dissipated power.

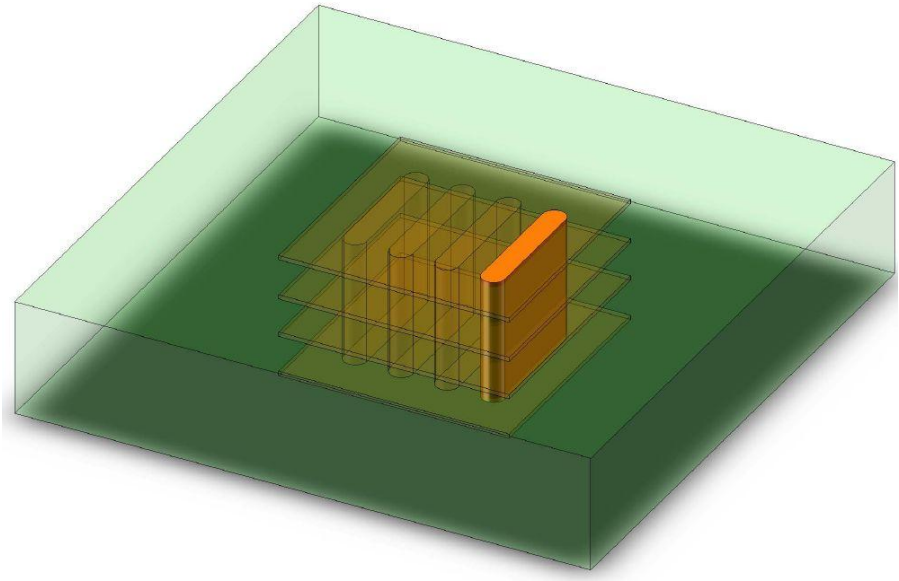


Figure 3-2 – CX-50 Thermal Via Bar Example

The active device technology used for this design is RFMD's BiFET InGaP/GaAs process[15]. This process allows for the design of rugged high efficiency amplifiers. The process also includes a depletion mode N-FET that can be used in the creation of bias networks, logic, and switches. The GaAs die can be attached to the CX-50 laminate via conductive epoxy and allows for gold bond wire connectivity between the top bond pads and the gold metalized traces on the laminate.

The design will also require the use of numerous surface mount components. Due to the size of the amplifier module the only sizes of components that can be reasonably used are 0201 (X-Y dimensions of 0.02" x 0.01") and 01005 (X-Y dimensions of 0.010" x 0.005"). Because of the cost and quality factor 0201 sizes will be used whenever possible. Even larger components such as 0402 (X-Y dimensions of 0.04" x 0.02") would be preferred if space permitted because they can have a wider range of values, higher quality factor, lower cost, and tighter tolerance. In particular the high quality factor or Q is very desirable in portions of the design such as the output matching network where insertion loss should be kept to a minimum.

Figure 3-3 shows a diagram of the different design sections of the two stage power amplifier. In the remainder of this chapter we will go through each of the blocks in Figure 3-3 and show the design process of that section. The blocks are mostly independent and can generally be designed without regard to each other. There are some exceptions to this

general behavior and when interactions occur they will be noted. Table 3-5 gives a more detailed description of each block in Figure 3-3 and the section of this chapter in which the design will be done.

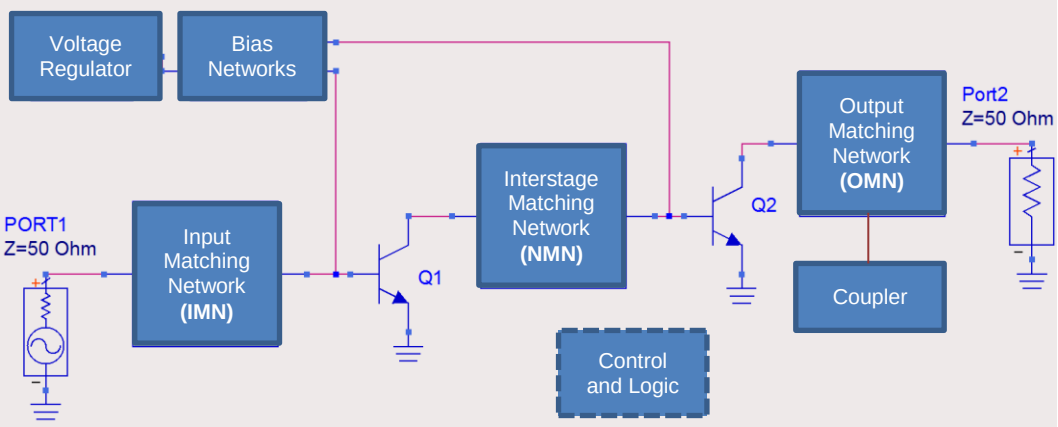


Figure 3-3 – Two Stage Amplifier Block Diagram

Block Name	Section	Description
Output Matching Network	3-2	Provides the power match between the collector of Q2 and the external load the PAM will be delivering power to. The output matching network includes a choke which feeds Vcc to Q2. This circuit will be abbreviated OMN.
Coupler	3-3	High directivity coupler used to detect the output power of the power amplifier.
Q1/Q2	3-4	The active devices used to amplifiy the input signal. Device sizes and layout considerations will be covered.
Bias Networks	3-5	Circuits used to set the bias points for Q1 and Q2. Bias networks need to work with the voltage regulator to be consistent over process and exhibit the proper temperature slope over temperature.
Interstage Matching Network	3-6	Matches the impedances between the output of Q1 and the input of Q2. Important for gain, harmonics, and linearity. Includes a choke which feeds Vcc to Q1. This circuit will be abbreviated NMN.
Input Matching Network	3-7	Matches the base of Q1 to the source impedance of 50Ω. Important for stability, gain, return loss, and linearity. This circuit will be abbreviated IMN.

Table 3-5 – Descriptions of Amplifier Blocks

The general design procedure is to start with a simplified model of the section (either mathematical or a basic circuit) and then increase the complexity using more advanced simulation tools like S Parameters, harmonic balance, and an electromagnetic simulator like Agilent Momentum. To model the surface mount components in the design we use the Modelithics library[16]. Modelithics is a company that specializes in creating simulation models for RF/microwave components. These models account for substrate effects and are more reliable than S Parameters provided by the component vendor and result in better agreement when comparing simulation to measurement.

In the spirit of having models that are easy to use and understand we characterize the laminate material so basic information on metal traces is easy to look up. The laminate material used in this PAM has four layers of metal. The bottom metal layer is attached to the customer's application board and is only used as a ground plane and for pin connections so it cannot be used for other purposes. Figure 3-4 shows the calculations from Agilent LineCalc™ for a section of 50Ω transmission line with an electrical length of 90° at a frequency of 1GHz for the three usable metal layers in the PCB material. The line impedance is more or less independent of frequency and the line length scales linearly with frequency so it is easy to calculate the length of a line for a different frequency. Often in the design of a PAM a transmission line width or

length is chosen not for electrical reasons, but for physical reasons such as connecting two locations together in a limited space. Table 3-6 can be used to lookup the electrical characteristics of a transmission line based

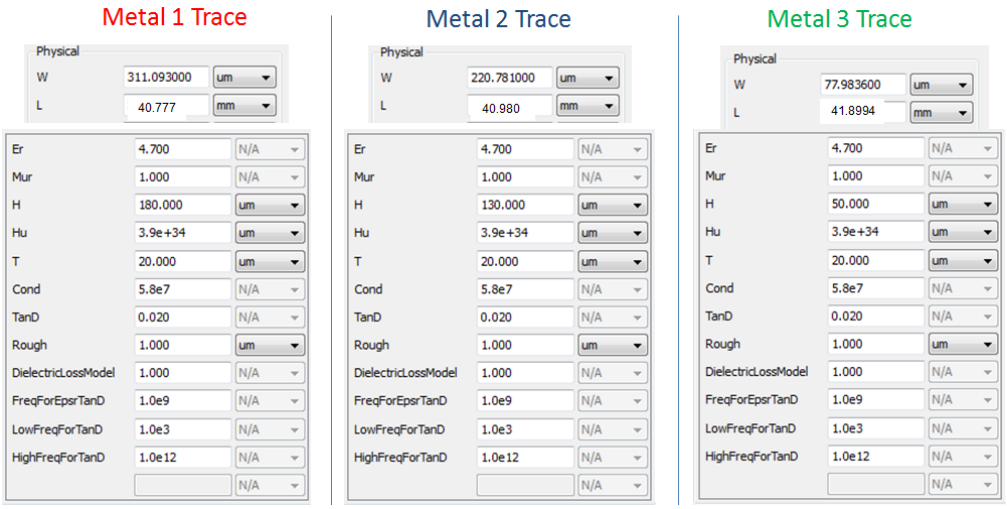


Figure 3-4 – 90° Transmission Lines on CX-50 with 4 Layers

on the physical with and length. A wide range of widths are shown and all the lengths are given for a 1° section of line at a frequency of 1 GHz. In all subsequent layout pictures the top metal will be referenced as M1 and be colored red, second layer will be M2 and colored blue, third layer will be M3 and colored green, and bottom metal will be M4 and colored yellow.

Trace Width (um)	M1 Impedance (ohms)	M1 Length 1 Degree (um)	M2 Impedance (ohms)	M2 Length 1 Degree (um)	M3 Impedance (ohms)	M3 Length 1 Degree (um)
50	103.1	122.5	92.1	122	61.3	119.5
75	91.9	120.5	81.0	120	51.0	116.5
100	83.5	119.5	72.7	118.5	43.8	114.5
125	76.9	118.5	66.2	117	38.5	113
150	71.4	117.5	60.2	116	34.4	111.5
175	66.8	116.5	56.5	115	31.1	110.5
200	62.8	116	52.7	114	28.4	109.5
250	56.2	114.5	46.6	113	24.2	108
300	51.0	113.5	41.8	112	21.1	107

Table 3-6 – Impedances and Transmission Line Lengths

SECTION 2: OUTPUT MATCHING NETWORK

The output matching network is one of the most misunderstood aspects of high power amplifier design. The idea that a conjugate relationship between the transistor output and the matching network is necessary can be found in numerous technical papers and books[17]. In fact when optimizing efficiency and linearity the device impedance is almost irrelevant to the design. The device must have the capacity to deliver the current required by the application and be able to withstand the voltage swings without breaking down. The device selection will impact the gain and the reactive portion of the output impedance which must be absorbed into the OMN.

The design parameters that decide the OMN are the available Vcc level and the desired output power of the amplifier. The choice of OMN impedance based on the power requirements of the amplifier is referred to as a power match[18]. The starting design equation for the output matching network is shown below

$$R_{load} = \frac{(V_{cc} - V_{knee})^2}{2 \cdot Pout}$$

This equation is the classic Class A relationship between the available voltage, the output power, and the load. Note the only device dependent portion of the equation is the V_{knee} term which is similar among devices of

different sizes. The equation assumes the voltage at the output of the device is a single sinusoidal and swings between $2 \bullet V_{cc}$ and V_{knee} without any clipping. One may question the R_{load} calculation in this application because the amplifier is Class AB not Class A, the output voltage waveform will experience clipping, and the waveform is a mix of multiple sinusoids with harmonics. Experience has shown for this type of design the R_{load} where a single sinusoidal voltage waveform would start to clip at Pout is approximately where the resistive part of the load should be set for a WCMDA voice waveform. Looking back at Figure 1-3 it can be seen the WCDMA voice signal spends 90% of the time below the average Pout+1.7dB. Because of this relationship it is typical to use average Pout+2dB as a starting point assumption for calculating R_{load}. This assumption is based on a mix of the load equation and empirical experience with these types of waveforms and amplifiers. The V_{knee} parameter in this process is 0.3 V, the targeted maximum output power from Table 3-3 is 28.5dBm. We must also consider the amount of power that will be lost in the OMN. The type of matching network we will use with the component Q we have available will have about 0.5dB of loss. Putting all of those parameters into the Rload equation we estimate the R_{load} value should be approximately 6.04Ω. For reasons that will be explained in the interstage matching section of this chapter we will use a slightly higher value of 6.5Ω. The reactive portion of the target output impedance will be –j1Ω. The reactive portion of the target is not well

understood. One would expect the device to need an inductive load instead of a capacitive one because the active device has a capacitive parasitic element associated with it. One author has postulated a modified Class AB mode of operation called Class J[19]. The Class J mode of operation requires a capacitive OMN and can yield small efficiency enhancements. In this thesis, the reasons for the capacitive load will be accepted without attempting to understand them. This result is an avenue for future work.

It is necessary to consider the number of matching sections that will be used in the matching network. A single L section has the advantage of being very compact and has very low insertion loss. A two section match has more tuning flexibility, better harmonic rejection, and broader bandwidth[20]. For this type of design an OMN with more than two sections is not considered because of the space required to implement it. The fractional bandwidth for this band is low and can be calculated from the information in Table 3-3.

$$BW = \frac{f_{max} - f_{min}}{f_{mid}} = \frac{915MHz - 880MHz}{897.5MHz} = 3.90\%$$

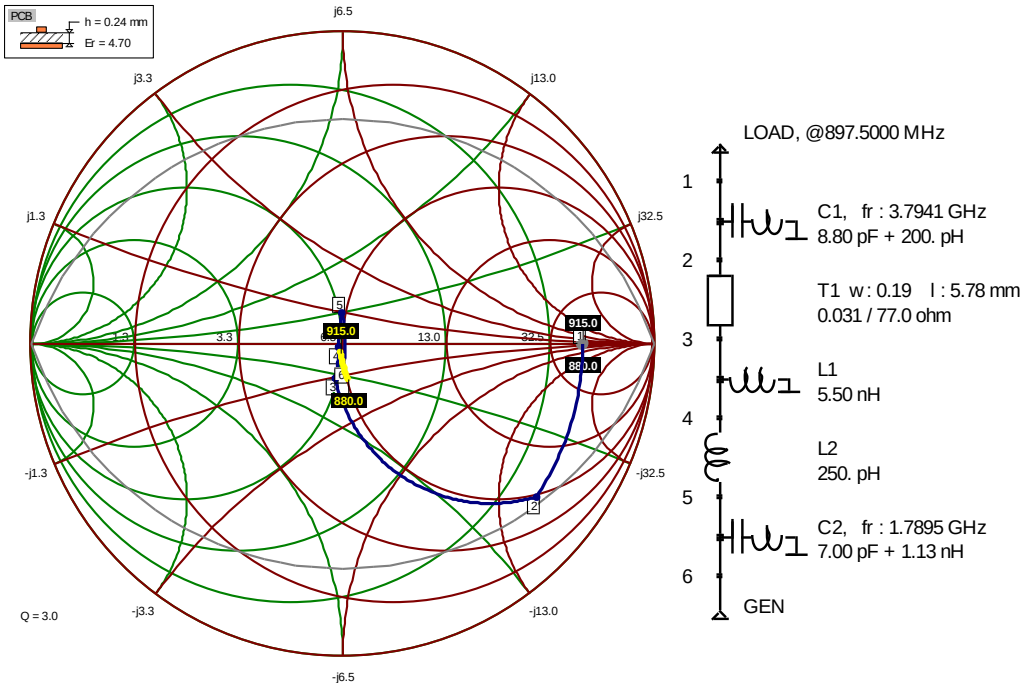
Broadband performance is not required and the harmonic requirements from Table 3-3 can be achieved with a single section match. A single section match is chosen because of the low loss and small size. The output match will also include a 2nd harmonic trap for harmonic and efficiency performance. A harmonic trap will also be included at the

interstage between the Q1 collector and the Q2 base to improve the harmonic performance. The interstage harmonic trap is discussed in detail in the interstage matching section of this chapter.

Since the impedance at the output of the OMN is known (50Ω) and the target impedance at the input of the OMN is known (6.5-j1Ω) closed form equations[21] can be used to determine the L and C values needed to design the OMN. The details of how the match works are lost when using a "plug and chug" approach. Higher levels of understanding occur when using a more graphical method to design the network. In the days before personal computers were ubiquitous this was done with a Smith Chart[22] and a pencil to map out the impedance trajectories vs. component values and frequencies. It was difficult to make changes once the match was set in place and was difficult to see the network behavior over a large bandwidth. The preferred approach today is to use the graphical technique in a virtual environment. A quick internet search for "Smith Chart Matching Program" will reveal several free or nearly free programs. The graphical matching program used in this thesis is Smith32. Smith32 is written by Ib F. Pedersen and can be downloaded from the internet or requested from Ib Pedersen. It is preferred by this author for its rich feature set and intuitive user interface.

An estimate of the OMN is shown in Figure 3-5. The blue trace is the trajectory of impedance change as the components in the match are swept in value. Node 1 is labeled in both the circuit and the Smith Chart

and represents the output of the OMN. The match continues to transform the impedance down to the target impedance of 6.5-j1Ω. The nodes in the circuit are numbered and have corresponding impedance locations on the Smith Chart. Table 3-7 identifies each element in the matching network. The yellow trace shows the change in impedance vs. frequency across the band at the Q2 collector reference plane.



Label	Description
Load	Ouput of power amplifier module
C1	Capacitor in L network
T1	Transmission line in L network (acts like inductor)
L1	Q2 Choke
L2	Bond wire inductance
C2	Series resonant 2fo trap
Gen	Q2 Reference plane

Figure 3-5 – Simple Output Matching Network

With the basic circuit topology established for the OMN the individual elements in the network must be designed. The first element is the choke which is shown in Figure 3-6. The trace widths are 100um and the length is approximately 7.16mm. The inductance and Q of the choke are calculated by measuring network parameters. Once the parameters are known they are used to determine L and R. The input and thru calculations yield different results depending on how much parasitic capacitance to ground exits in the structure. This structure produces almost identical answers with both methods. The simulation results are shown in Figure 3-7. The simulated inductance is 5.5nH and the Q is 37.

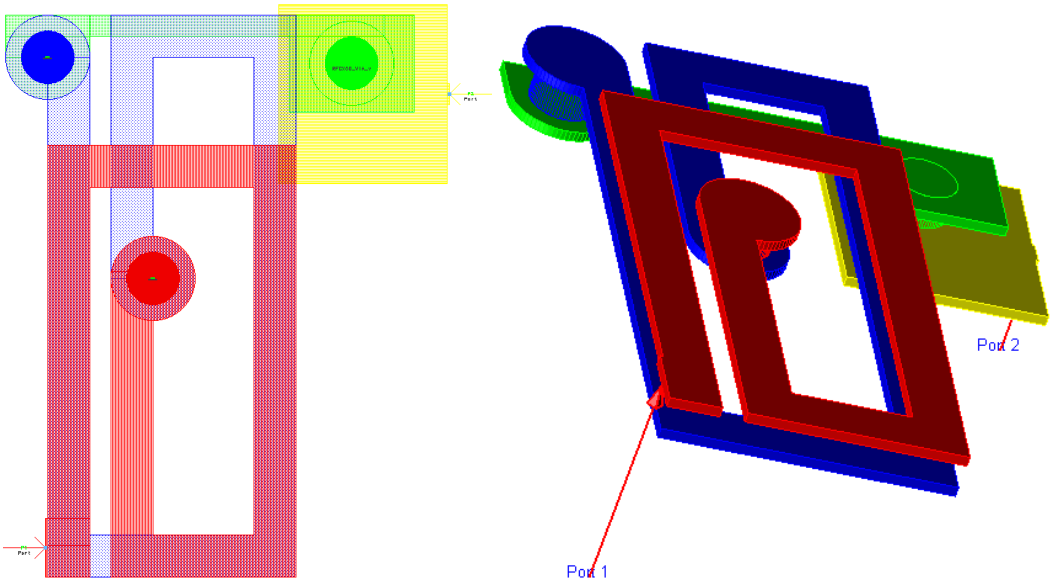


Figure 3-6 – OMN Choke Layout in 2D and 3D

The next step is to simulate an approximate structure for the OMN spiral. The exact spiral width and length will not be known until the entire OMN is complete. Nearby metal structures cause parasitic coupling and affect the

impedance. An iterative approach is taken to reach the OMN design impedance. The process involves putting all of the pieces together and then adjusting the individual parts of the OMN to meet the goal.

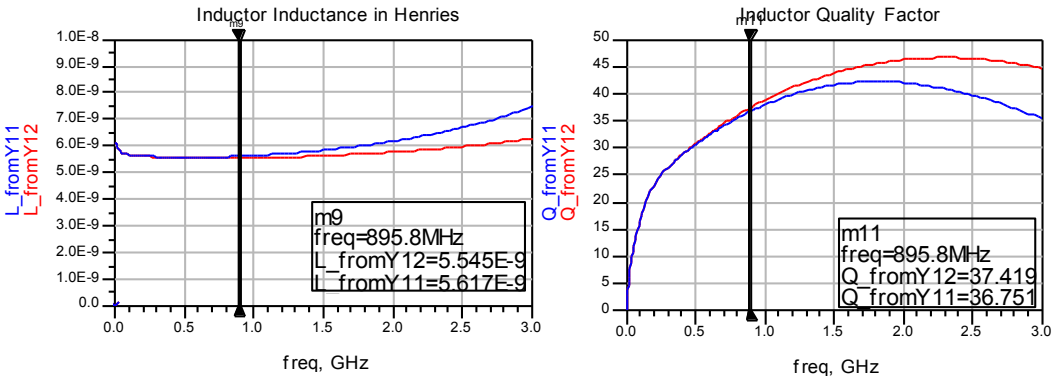


Figure 3-7 – OMN Choke Simulation Results

There are a few details that need to be mentioned regarding the completion of the OMN. The circuit element used to model bond wires is the Phillips Bond Wire Model. This model is capable of capturing the self-inductance, mutual inductance between bond wires, and coupling to the ground plane. If the bond wire shapes, heights and relative positions are captured within the PAM model the Phillip's model can give very accurate results. The capacitor in the output network (C1 in Figure 3-5) was split into two parallel capacitors. Splitting the capacitor allows for increased component Q and gives better resolution for fine tuning the circuit. The increased resolution is needed because the design value of 8.8pF is not a standard value and the step sizes of component values are very coarse near this value. With two capacitors the OMN capacitor can be adjusted in increments as small as 0.1pF. The harmonic trap is implemented with a

capacitor on the die with a bond wire to the laminate. The effect of the coupler and DC blocking capacitor is also needed to be included because they cause a small shift to the impedance. The coupler will be discussed in detail in the next section. Figure 3-8 shows the full output match with the important features labeled.

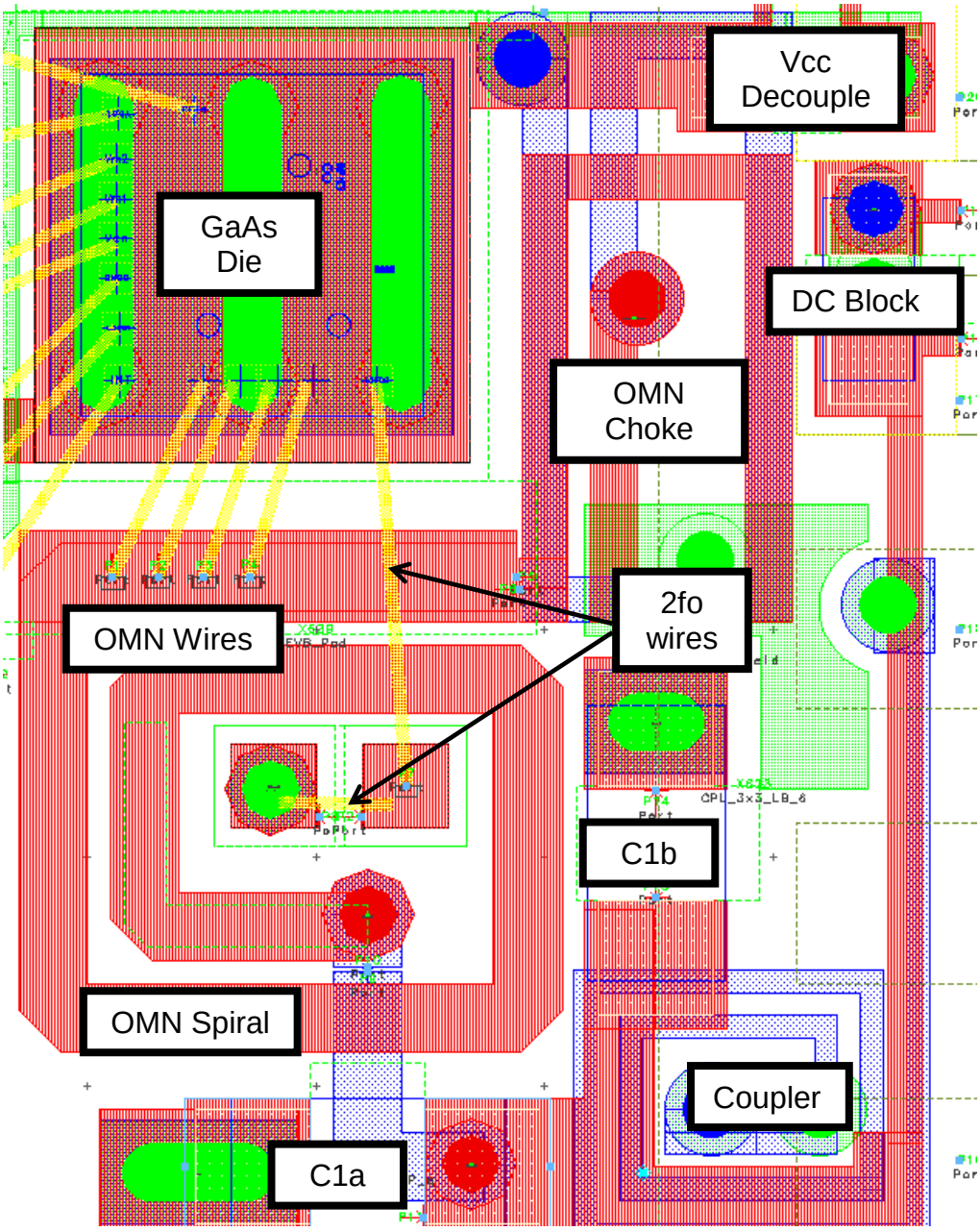


Figure 3-8 – Output Match Layout

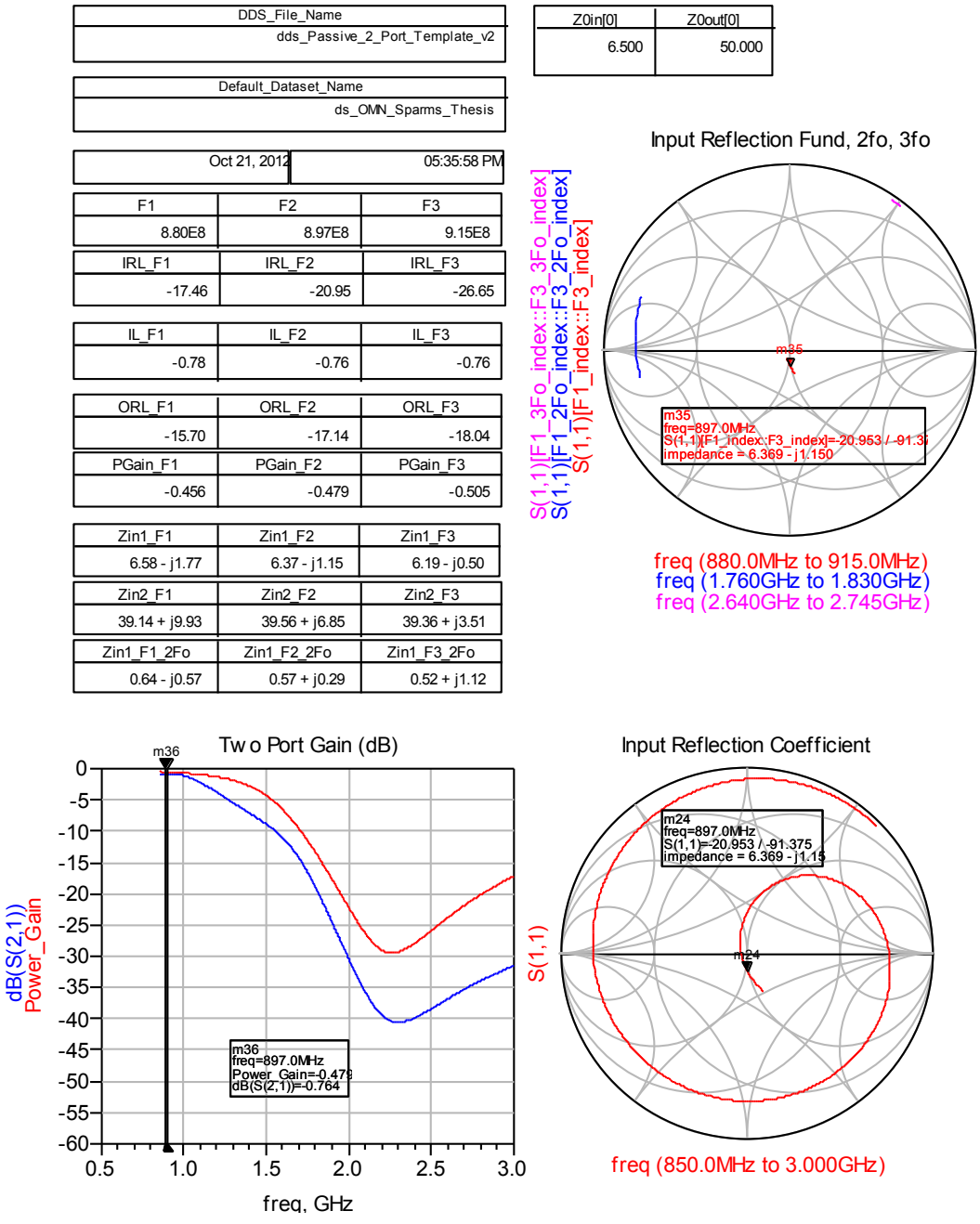


Figure 3-9 – Output Match Simulation Results

The S Parameter simulation results are shown in Figure 3-9. The tabular data in the upper left gives various numeric results at the lower band edge, middle of the band, and the upper band edge. The circuit was simulated with a port 1 impedance of 6.5Ω and a port 2 impedance of 50Ω. Power gain (called PGain in the data) is calculated to measure the actual insertion loss of the network without including any of the reflected power loss[23].

$$PGain = \frac{(|S_{21}|)^2 \cdot [1 - (|\Gamma_L|)^2]}{[1 - (|\Gamma_{in}|)^2 \cdot (|1 - S_{22} \cdot \Gamma_L|)^2}$$

PGain was simulated to be about -0.5dB which is in agreement with our expectations from the R_{load} calculation. The Smith Chart in the upper right of Figure 3-9 shows the impedances at the fundamental, 2fo, and 3fo frequencies. The graph in the lower left displays S21 and the power gain. The lower right graph has S11 swept over a range of frequencies from 850MHz – 3.0GHz.

SECTION 3: COUPLER

The PAM requires a directional coupler as part of the design. The coupler is necessary so the system has a way to monitor the power output from the amplifier. The load presented to the PAM is a function of the phone's antenna impedance. The antenna impedance can vary considerably depending on the location of the user's hand. To maintain accurate power measurement the directivity of the coupler must be high.

Table 3-1 gives the nominal target specs as 20dBc for the coupling factor and 20dB for directivity. The coupler in this module is intended to be used in a series configuration which means the coupled out port of one coupler feeds into the isolated port of the next module. If the impedance is not near 50Ω the couplers interact with each other which degrades coupling and directivity. Figure 3-10 shows 3D view of the coupler layout in the module.

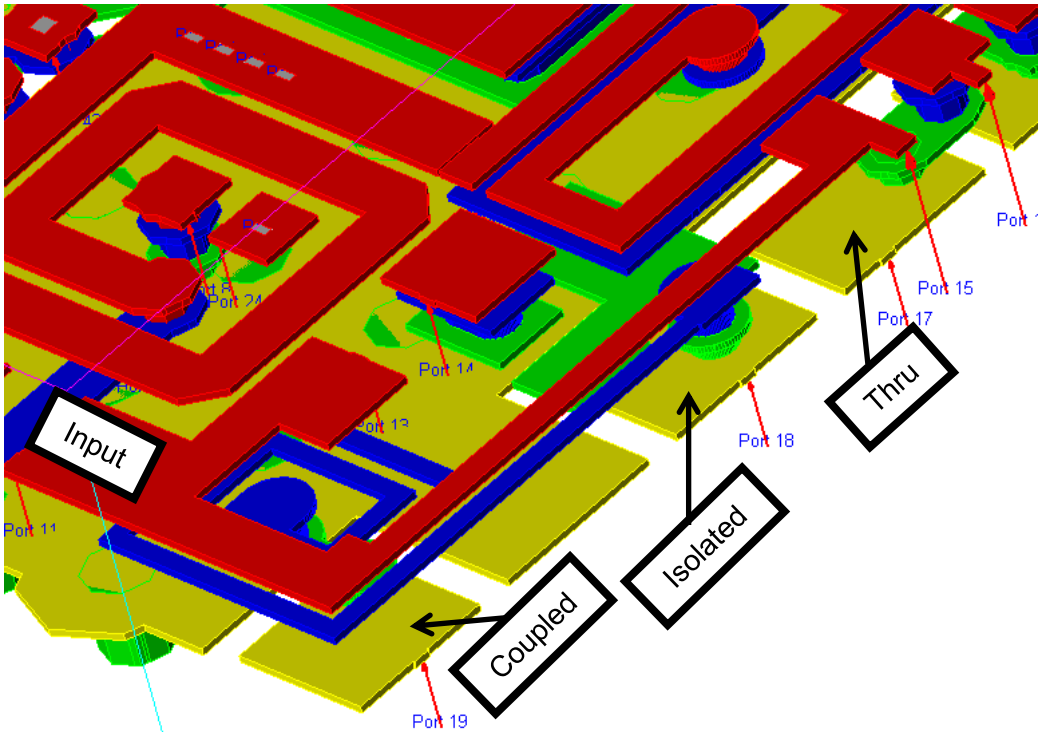


Figure 3-10 – Directional Coupler Layout

Because the coupler arm travels over the pins on the right side of the module the ground plane has been interupted and the assumption of an ideal ground is no longer valid. To accurately model this situation it is necessary to add an additional layer in the substrate stackup and ground

the module to the extra layer with vias (seen in the bottom left corner). This style of coupler is used frequently in cellular amplifer modules. The basic idea is to run a metal trace near a trace that is carrying the full output power. If the trace widths, spacings, and lengths are chosen carefully it is possible to create a high directivity coupler. Cook book design procedures exist for coupler configurations where the thru line and coupled line are on the same layer (edge coupled). Unfortunately no such procedures exist for broadside coupled microstrip lines.

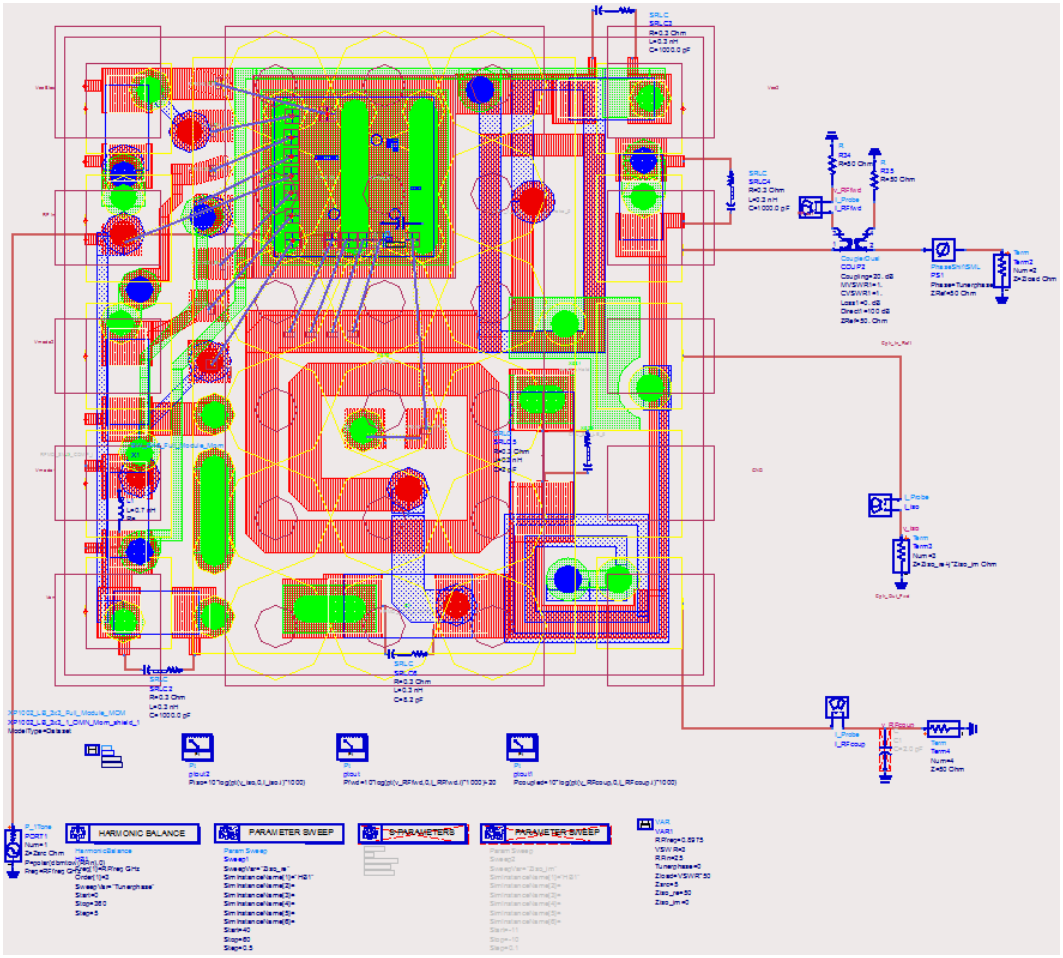


Figure 3-11 – Directional Coupler Simulation Schematic

Several papers discuss specific cases[24,25,26,27], but all use variations of trial and error to optimize the design. The broadside coupling configuration is preferred because the coupling between lines is much stronger and a coupler can be created in a smaller space. The coupler was designed by fitting it into the available space in the bottom right corner of the module and adjusting the overlap between the coupled arm and thru arm and the widths of both arms.

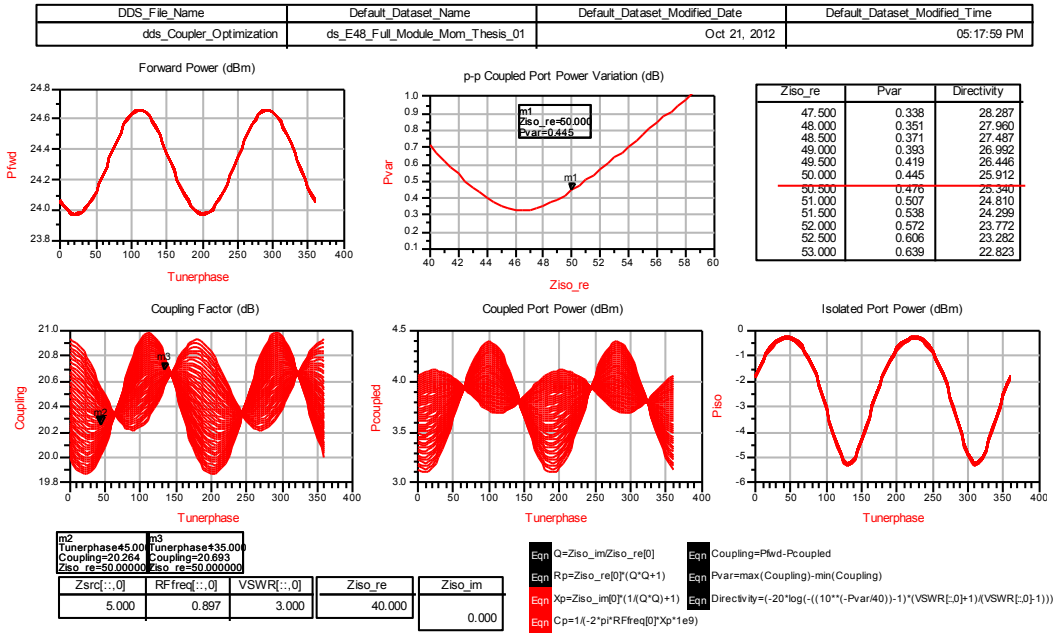


Figure 3-12 – Simulated Coupler Performance

The simulation schematic used to design the coupler is given in Figure 3-11. The simulation uses a Momentum model with the extra evaluation board layer included. A harmonic balance engine is used with a sliding 3:1 load at the output port. The variation of coupled power as a

function of the phase of the output load is used to calculate directivity[27]. In addition to the phase of the output impedance being swept, the isolation port resistance was also varied. By making changes to the coupler structure and then repeating the simulation the optimum configuration was found. The thru arm on M1 was chosen to be 75um wide and 1930um long. The coupled arm on M2 was chosen to be 50um wide and 5286um long. To achieve a 20dB coupling factor the M2 trace had to be spiraled multiple times to increase the coupling. The simulation results are given in Figure 3-12. The simulated coupling factor is 20.5dB which can be determined by averaging the two markers in the bottom left graph. The top middle graph shows the power variation of the coupler when sweeping the isolation resistance. The table in the upper right shows the directivity to be 25.9dB when the isolation port is loaded with 50Ω. Even higher directivity could be achieved by reducing the width of M2 further, but 50um is the minimum allowed metal width in the CX-50 process. Return loss is better than 20dB across the band on both sides of the coupler port as shown in Figure 3-13.

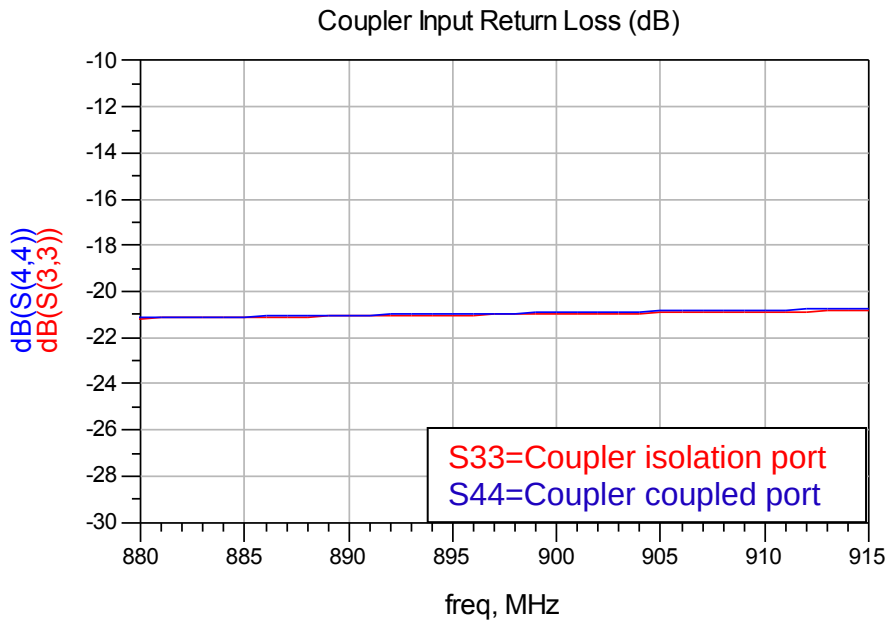


Figure 3-13 – Coupler Input and Output Return Loss

SECTION 4: Q1/Q2

Choosing the correct transistor size and layout for each amplifier stage is necessary for successful implementation of the power amplifier module. The output device (Q2) must be large enough to supply the current required by the power amplifier specification. We also want to keep the device as small as possible to reduce the amount of bias current required for operation and minimize the heat imbalance that can occur in large devices. For a short period of time, an HBT device can sink collector to emitter currents which far exceed the amount of current that would be safe a reliable for a long period of time. Because of this, the long term reliability is the factor that determines the minimum device size. The RFMD HBT process requires HBT devices stay below a current density of 20kA/cm^2 for reliable operation over a period of 7 years[28]. Table 3-3

specifies at the maximum power of 28.5dBm that the maximum current for the PAM is 463mA. After performing the necessary unit conversion, we calculate the minimum emitter device size capable of meeting the specification is 2315 um^2.

The RFMD HBT process does not allow the designer to make devices of arbitrary sizes. The approach used is to have a device that acts as a unit cell which can be put into array configurations. The size of the array is chosen to accommodate the power requirement of the amplifier. The unit HBT for this process is a “2x20 Quad” which is also referred to as a “T4”. The “2” in the name references the width of an emitter finger in the device is 2 um. The “20” identifies the length of an emitter finger is 20 um. The “Quad” means the device has four of the 2x20 emitter fingers in parallel. A simple multiplication of the emitter dimensions works out to be 160 um^2 of emitter area for each T4 device. Based on the minimum size calculation of 2315 um^2 we require a minimum of 15 cells. We add an additional constraint that the number of cells must be divisible by 4 because the output array will be arranged into a four column configuration. This results in an output transistor size of 16 T4 devices.

A similar line of reasoning is used as a starting point to determine the size of the first stage device (Q1). In the presence of mismatch, the output stage can have gain as low as 10dB, which then requires the input stage to supply up to 18.5dBm of power to the second stage. A minimum

would then be 10% of the second stage which would be two cells after increasing to an integer number of cells. However the first stage must have significantly higher linearity so that it does not contribute strongly to the overall amplifier linearity. Achieving the higher linearity requires the first stage be less efficient than the second stage. Typical first stage efficiency for this type of product is around 30% which at 18.5dBm would be a current of 68mA. This current is slightly higher than the limit for two devices so we use three T4 cells for the first stage. The sizes and currents for both stages are summarized in Table 3-7

Stage 1 Device (Q1)		
Emitter Width	2	
Emitter Length	20	
# of Emitters	4	
# of Devices	3	
Total Area	480	um^2
Max Current	96	mA

Stage 2 Device (Q2)		
Emitter Width	2	
Emitter Length	20	
# of Emitters	4	
# of Devices	16	
Total Area	2560	um^2
Max Current	512	mA

Table 3-7 – Q1/Q2 Sizes and Current Densities

Although not considered in this thesis a designer may choose to adjust the size of either device in order to make the conjugate match between the device and matching network closer to the power match target impedance. If the two impedances are brought closer to each other, the overall gain will be higher and the behavior over power drive will be different. In some designs it is more important to have high gain than to minimize the bias current.

The arrangement of the cells in the transistor arrays is also very important. In HBTs like most bipolar devices, the turn on voltage has a negative temperature coefficient. This means that as a device heats up its resistance will go down, so the same base to collector voltage will produce more collector/emitter current. More collector /emitter current will cause more power dissipation in the device which will raise the temperature further which will to increase the current more. This positive feedback mechanism is called thermal runaway and can result in the current increasing without bound until the device fails. Thermal runaway is controlled by adding a resistor between the bias voltage and the HBT base of each unit cell. This technique is called resistor ballasting and is used almost universally in HBT power amplifiers. Choosing the size of the ballast resistor to use is a combination of theoretical and empirical analysis[29]. If the ballast resistor is too small, thermal runaway can still occur under extreme conditions. If the ballast resistor is too large, the linearity and gain can be impacted at high drive conditions because the part can be de-biased due to the large voltage drop across the resistor as more current is required. A long history of experimentation at RFMD has shown a wide range of ballast resistor sizes protect the devices without impacting performance. The ballast resistor value in various RFMD products goes between 250Ω to 600Ω for each T4 device. For the amplifier in this thesis we used a value of 400Ω per T4. This specific value was chosen due to the physical size of the resistor and how it fit into the

overall layout of the die. The ballast resistor layout was done with the minimum width allowed by the process, so making the value smaller would cause the resistor to be wider and making the value larger would cause the resistor to be longer. A change in either dimension of the resistor would cause the layout area to increase.

After the device and ballasting resistor sizes have been determined, the devices must be arranged in a layout and connected to each other. The output of stage 1 is supplied with Vcc and the input of stage 2 is supplied with a different voltage to bias the HBT. At a minimum the interstage match will require a DC block between the two stages. Although possible to use one large capacitor between the two stages there are advantages to breaking up this capacitor to many small capacitors which go with each T4 cell.

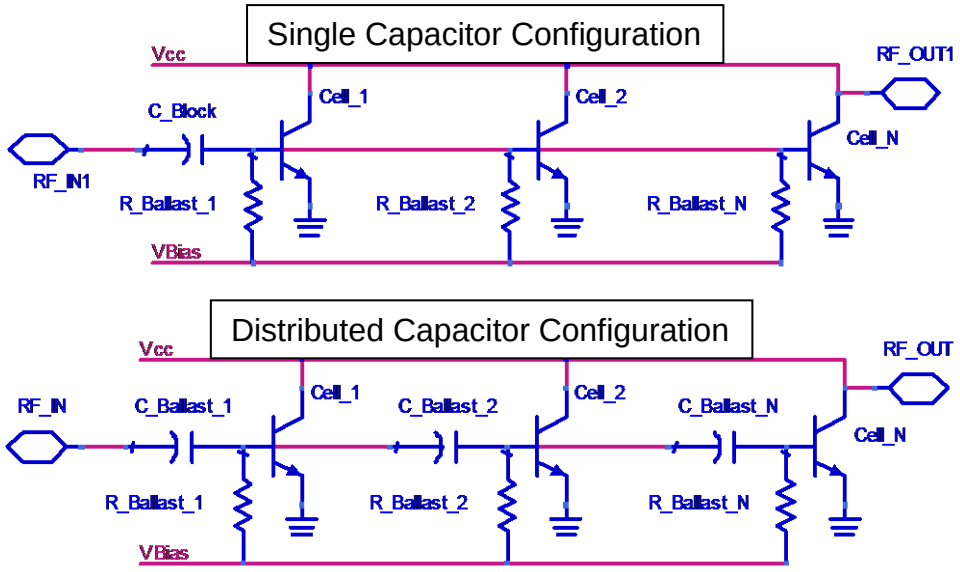


Figure 3-14 – DC blocking Options for HBT Devices

Figure 3-14 shows a schematic of the two different DC blocking configurations considered. Both methods satisfy the condition of a DC block between the two stages. The schematic at the top of Figure 3-14 tends to yield a more compact layout and is easier to make adjustments to the size of the blocking capacitor. However, a careful inspection of this schematic reveals that after the ballast resistors each transistor base is shorted together. With this configuration a form of thermal runaway can still occur. During operation thermal differences exist between the cells in the array. If one cell becomes significantly hotter than the others, it will

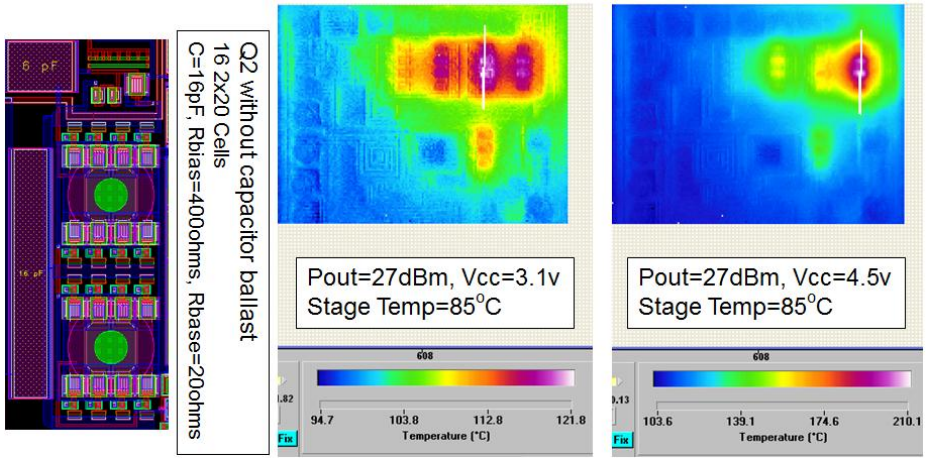


Figure 3-15 – Image of Thermal Runaway with Single DC Block

consume more current at the expense of the other cells. Although the ballast resistor prevents catastrophic destruction, this condition will adversely affect the amplifier performance. Figure 3-15 shows an example of this type of thermal runaway. The leftmost image of Figure 3-15 is the device layout with a single capacitor. Under lower battery conditions the power is reasonably well distributed between the 16 T4

devices as shown in the center image of Figure 3-15. However, when the power dissipation is increased by increasing Vcc from 3.1 V to 4.5 V, the center cells in the rightmost column experience thermal runaway as shown in the right image of Figure 3-15. The maximum device temperature increases from 122°C to 210°C and the devices that did not run away become cooler.

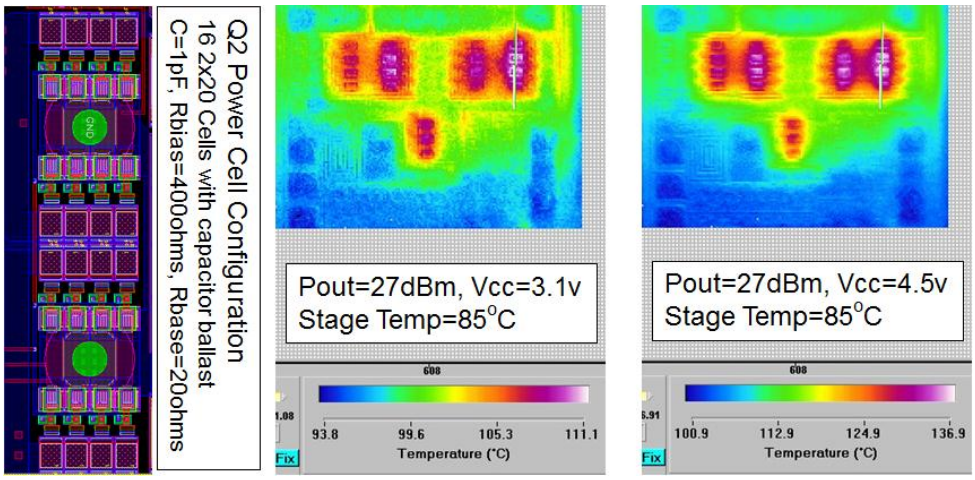


Figure 3-16 – Image of Thermal Dissipation with Capacitive Ballast

In contrast to the single capacitor layout, the distributed capacitor layout results in much better thermal performance. The distributed capacitor approach which is also called capacitor ballasting shows more balanced temperature under both nominal and extreme power dissipation. Experimentation showed the capacitor ballasted output stage did not exhibit any type of thermal runaway up to 12 V which was the test limit.

For the first stage layout capacitive ballasting is not used. As mentioned earlier, the layout and sizing of a single capacitor is easier than using distributed capacitors which is an advantage. Because Q1 only has

three cells that are close to each other they are thermally linked more tightly than the unit cells in Q2. The Q1 unit cells each have 20Ω resistors in the RF path which provides some isolation between the cells. Experimentation shows the Q1 device does not go into thermal runaway until the Vcc is raised above 9 V. Although not as good as the Q2 performance, 9 V is well in excess of the maximum Vcc voltage of 4.2 V and adequate for this power amplifier module.

SECTION 5: BIAS NETWORKS

Bias networks can have an effect on the overall performance of a power amplifier. For this PAM we use a variation of a bias network that is very commonly used in mobile PA designs. This bias network is referred to as a cascode bias network[30, 31]. Figure 3-17 shows the basic circuit schematic. The circuit creates a regulated current by taking a regulated voltage and applying it to a series resistor/diode network. This PAM supports three power modes of operation; the resistor used to set the regulated current is selected by the control circuitry.

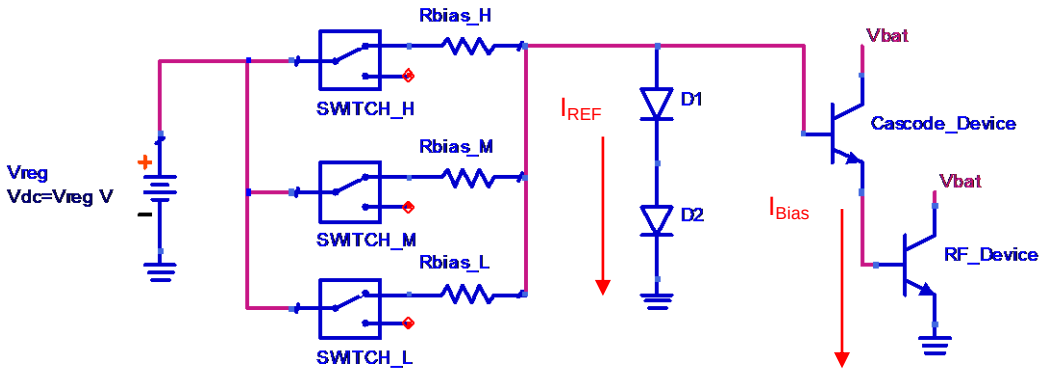


Figure 3-17 – PAM Bias Network Topology

The regulator and control circuitry used for inputs to the bias circuits are part of the overall PAM design; however their detailed operation is not within the scope of this thesis. They are considered “black box” circuits so consequentially only their inputs and outputs will be described. In Figure 3-17 the reference I_{REF} is created by current flowing from Vreg through Rbias_H, Rbias_M, or Rbias_L and D1/D2. Once the reference current is setup in the circuit, a scaled version of that reference current is supplied to the device to be biased. The scaling is inversely proportional to the sizes of D1/D2 and proportional to the size of the cascode device, and the RF device. To maintain linearity over a range of temperature, a GaAs HBT amplifier requires increased bias current as temperature increases. This bias network has a naturally increasing temperature slope due to IREF increasing as D1/D2 forward voltage decreases. The circuit was simulated to determine the proper sizing of the resistors for the Q1 and Q2 bias networks. The results at a temperature of 30°C are displayed in Table 3-8.

Mode	Iref resistor Q1 (Ohms)	Size D1/D2 (um^2)	Size Q1 (um^2)	Q1 Bias (mA)	Iref resistor Q2 (Ohms)	Size D1/D2 (um^2)	Size Q2 (um^2)	Q2 Bias (mA)
HPM	850	20	480	11.7	1050	20	2560	36.4
MPM	1500	20	480	9.6	1900	20	2560	29.2
LPM	2800	20	480	4.9	3600	20	2560	14.7

Table 3-8 – Bias Network Values and Results

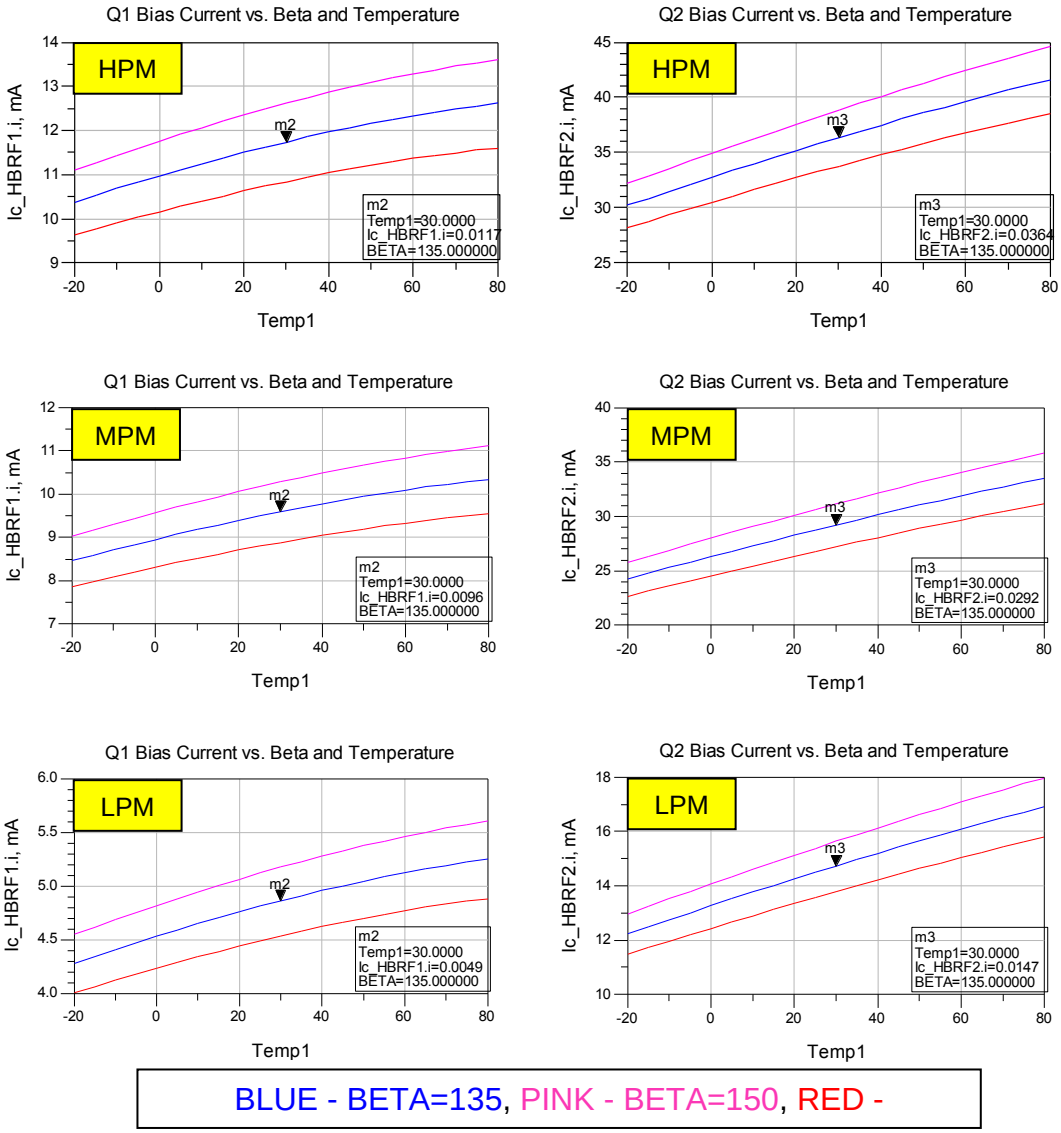


Figure 3-18 – Bias Network Current vs. Temperature and Beta

SECTION 6: INTERSTAGE MATCHING NETWORK

In a two stage amplifier, the interstage network is the connection between the first amplifier stage and the second amplifier stage. It simultaneously sets the load for the first stage and matches the input of the second stage device. A poorly designed interstage match can cause a two stage amplifier to have low gain, poor linearity, poor frequency response, early saturation, and high gain expansion.

To start the interstage network design, we use the load line equation from section 3-2 to provide the design target for the Q1 load line. In section 3-4 it is determined that the maximum power delivered by the interstage is 18.5dBm. To ensure stage 1 operates in a very linear manner, we choose a load based on a 3dB higher power which would be 21.5dBm. Picking a higher power for the load line target ensures the first stage is always operated at a power backed off from its peak capability. With that higher power the real portion of the load line target is calculated to be 34.1Ω.

$$R_{load} = \frac{(V_{cc} - V_{knee})^2}{2 \cdot Pout} = \frac{(3.4 - 0.3)^2}{2 \cdot (0.141)} = 34.1\Omega$$

With the target load line known we use the simulator model to determine the impedances at the base of Q2 and the collector of Q1. The two impedances can be seen in Figure 3-19. The matching network transforms the Q2 base impedance of 4.99-j6.31Ω to the targeted load of

34Ω. In addition to the real portion of the load line it is important to make the imaginary portion of the load equal to the conjugate of the Q1 collector portion. The complete target impedance is therefore 34.1 + j21.1Ω.

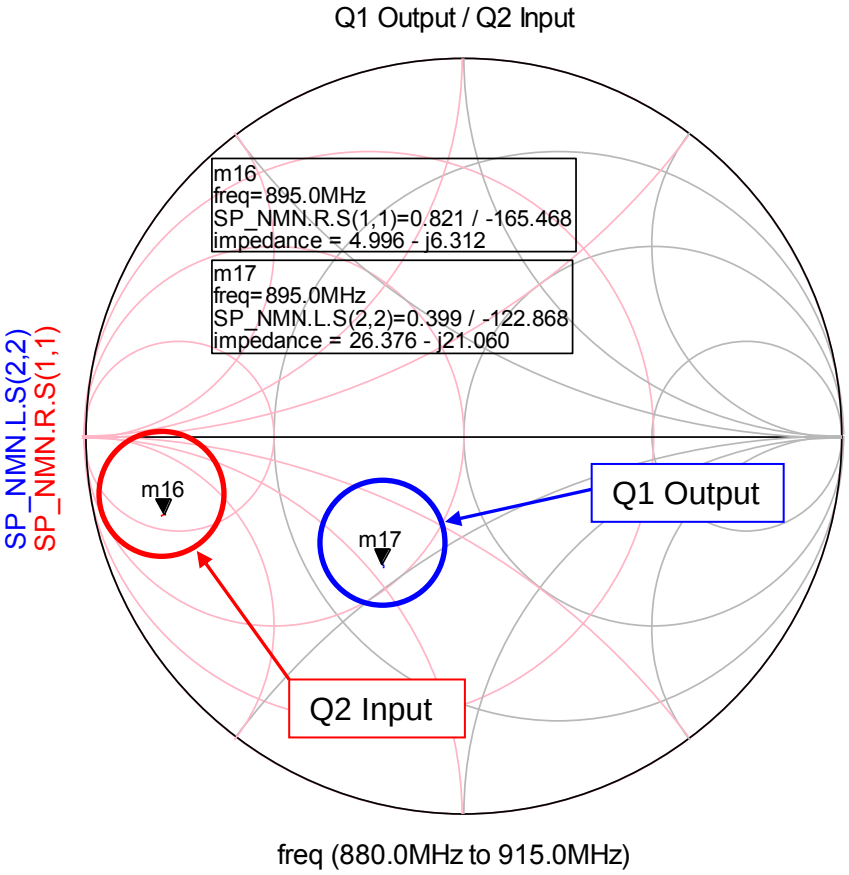


Figure 3-19 – Interstage Terminating Impedances

Because of limited space available for the interstage matching network, we consider only a single section match in the design. If impedance transformation were the only consideration, we could use a series capacitor followed by a shunt inductor or a series inductor followed by a shunt capacitor. However, as demonstrated in section 3-4 the importance of using a distributed capacitor in the Q2 device to prevent thermal

runaway from occurring. To satisfy this condition the matching element closest to the Q2 base is a capacitor. The matching network was designed in Smith32 and response is shown in Figure 3-20. The load impedance presented to Q1 with the match in place is 34.2+j22.8Ω.

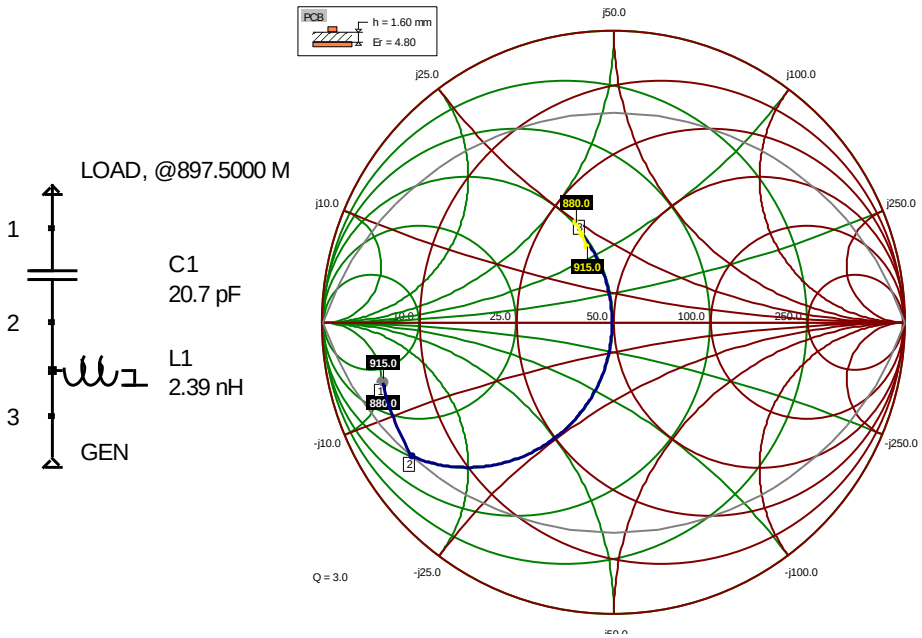


Figure 3-20 – Single Section Interstage Matching Network

The series capacitor / shunt inductor network has another benefit in addition to enabling capacitor ballasting in the second stage. The shunt matching inductor is used as a path to feed DC to the Q1 collector, so it functions as a DC feed in addition to functioning as a matching element. It is necessary to provide an AC short at the inductor for proper operation. Figure 3-21 shows the schematic of the interstage network.

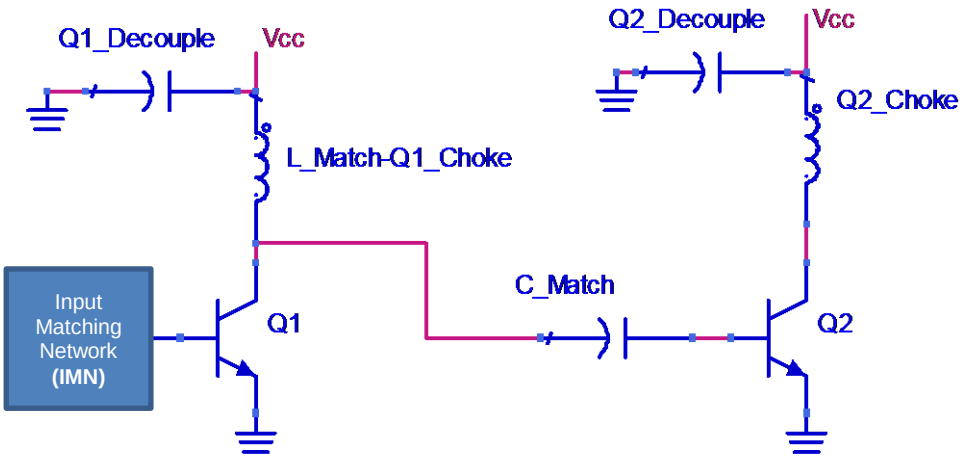


Figure 3-21 – Schematic of Single Section Interstage Network

The interstage network design shown is a common architecture in mobile handset power amplifiers. The design would be complete if no performance enhancements were explored. However, we present a novel efficiency enhancement technique by making a small change to the interstage matching network.

Over the last several years the Class F amplifier topology has been an area of active research. A Class F design offers a theoretical amplifier efficiency of 100%, an increase of 21.5% over an ideal Class B amplifier. To achieve this efficiency increase it is necessary to have ideal devices and to modify the shape of the amplifier's output voltage waveform from a sinusoid to a square wave[32]. Though neither condition can be achieved in practice an approximation yields an improvement. To convert a sinusoid to a square wave, it is necessary to add the odd harmonics of the sinusoid

at the correct phases and amplitudes. The result is well known in signal processing and is expressed with the following mathematical relationship.

$$v(t) = \frac{4}{\pi} \cdot \sum_{k=1}^{\infty} \frac{\sin[2\pi(2k-1)\cdot f \cdot t]}{(2\cdot k-1)}$$

Unfortunately it is difficult to produce the harmonic content needed at the correct amplitude and phase to create a voltage square wave in a power amplifier, especially an amplifier as small as a handset PA. Publications that discuss the implementation of Class F amplifiers generally focus on the harmonic output terminations. Output terminations should look like a short circuit at the even harmonics and an open circuit at the odd harmonics[32]. These open and short circuits prevent any power at the harmonic frequencies from being delivered to the load, but the terminations alone are not enough-the harmonic voltages must be generated too. There are two possible approaches to generating the harmonics. The first is to artificially inject the harmonics into the amplifier from the source. This technique is not practical for handset amplifiers due to size, complexity, and system control constraints. The second approach is to use the harmonics that are naturally generated by the nonlinear behavior of the amplifier in a way to create a Class F benefit. The circuit modification used in the interstage matching is an example of the second approach. It is necessary to understand how much improvement can be realized if only a limited number of the odd harmonics are at the optimum

level and phase. Figure 3-22 presents the ideal odd harmonic voltage levels to add to a waveform[33].

$$V(t) = 1 - \sum_{q=1}^{m} \left[\left(V_{2q-1} \cdot \sin(2 \cdot q - 1) \cdot \theta \right] \right], \quad \theta_r = \frac{r\pi}{m+1}, \text{ r=1 to m}$$

m	V_1	V_3	V_5	V_7	P (dB)	Efficiency
1	1	-	-	-	0	78.5
2	1.155	0.1925	-	-	0.625	90.7
3	1.207	0.2807	0.073	-	0.82	94.8
4	1.231	0.3265	0.123	0.0359	0.90	96.7

Figure 3-22 – Class F Ideal Harmonic Voltages

The voltages $V_1 – V_7$ are normalized to the maximum Class B voltage swing where the subscripts of V denote the harmonic frequency. For example V_3 is the 3rd harmonic. The P(dB) column denotes how much additional output power is delivered by "squaring up" the voltage waveform. The efficiency column is the calculation which gives the realized efficiency when m number of odd harmonics are added. The m=1 condition is when no harmonics are added which reduces to a Class B amplifier. From Figure 3-22 we see the efficiency can be increased by 12.2% by adding the 3rd harmonic alone. If the 5th harmonic is also added the efficiency only increases by 4.1%. Because the efficiency improvements diminish quickly above the 3rd harmonic, only the 3rd harmonic is focused on.

Figure 3-23 shows graphs of 3rd harmonic voltage added to a fundamental voltage at various magnitudes and phases. The voltage level

at the 3rd harmonic that results in the maximum fundamental voltage without clipping is $V_3/V_1 = 1/6$.

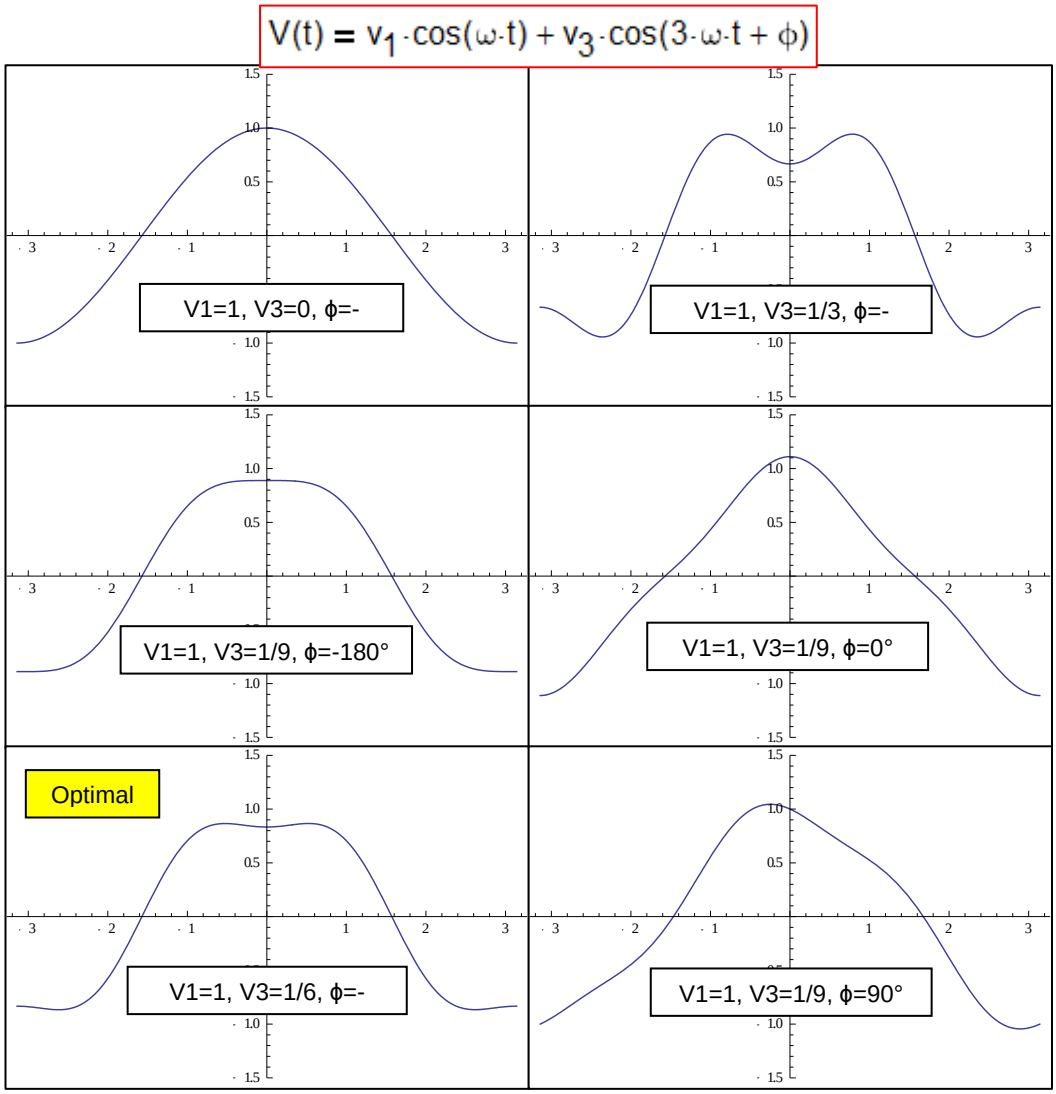


Figure 3-23 – Voltage waveforms with 3rd Harmonic Content

It can be seen in Figure 3-23 that the maximally flat voltage occurs when $V_3/V_1 = 1/9$. Increasing V_3/V_1 beyond 1/9 creates a "double hump" waveform, but the overall maximum voltage continues to be reduced.

When V_3/V_1 = 1/6 the maximum voltage is at the global minimum, and if V_3/V_1 becomes greater than 1/6 the peaks of the “double hump” begin to increase. It can also be seen from Figure 3-23 that the phase of the 3rd harmonic relative to the fundamental is important. The optimal phase to add the two waveforms together is 180°. Knowing the desired relationship between the fundamental and 3rd harmonic, we now examine a method to modify the 3rd harmonic phase and amplitude.

Figure 3-24 shows the previously designed interstage network setup in an S Parameter simulation schematic. The results of the simulation are shown in Figure 3-25. Notice the phase shift through the network is about 90° at the fundamental and 20° at the 3rd harmonic.

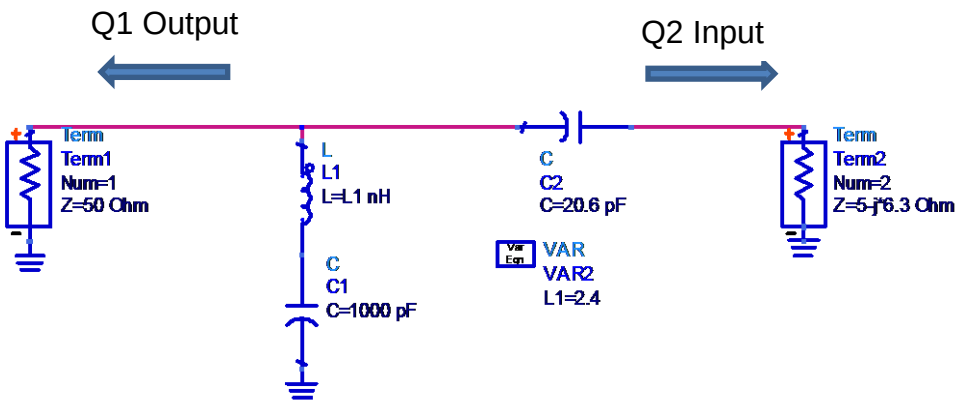


Figure 3-24 – Interstage Network Input and Output

Because Q1 is a nonlinear device it will generate harmonic content in addition to amplifying the input signal. The fundamental signal and 3rd harmonic are created with and unknown phase relationship and their relative phase are shifted by the phase delay of the interstage network

before being delivered to the second stage. In the present form the interstage network has a phase delay that will be relatively fixed at any frequency. The two components in the network are used for impedance matching and there are no additional degrees of freedom to modify the 3rd harmonic.

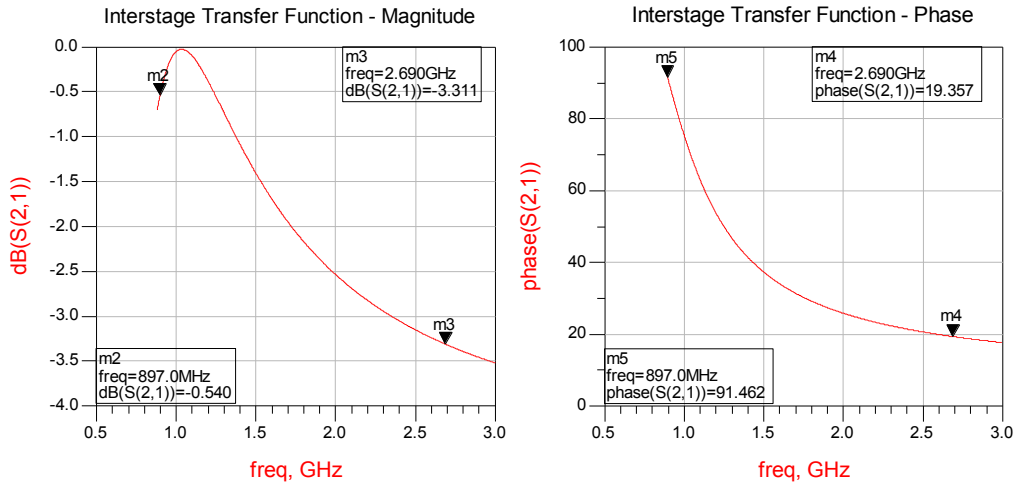


Figure 3-25 – Interstage Network Transfer Function

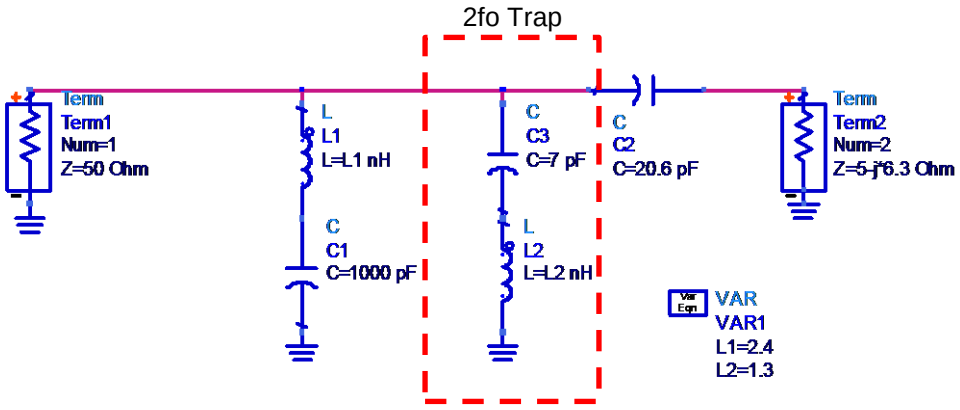


Figure 3-26 – Interstage Network with Harmonic Trap

Figure 3-26 is an S Parameter schematic of the interstage network with a series resonant harmonic trap added. The design values of the harmonic trap are chosen to create a short circuit near the 2nd harmonic frequency. The addition of the harmonic trap results in three important changes in the interstage transfer function. The first and obvious result is that a pass band zero is created near the second harmonic, which can improve the overall harmonic performance as it reduces the second harmonic power delivered to the second stage. The second result can be seen by looking at the simulation results from the modified interstage circuit in Figure 3-27. Figure 3-27 shows a family of sweeps of the interstage S21 response as the harmonic trap inductor values is changed from 0.7nH to 3.0nH. The transfer zero occurs near the 2nd harmonic frequency when the inductor is 1.1nH. In the original interstage circuit, phase change through the network was 90° at the fundamental and 20° at the 3rd harmonic. With the new interstate the phase change is 28°

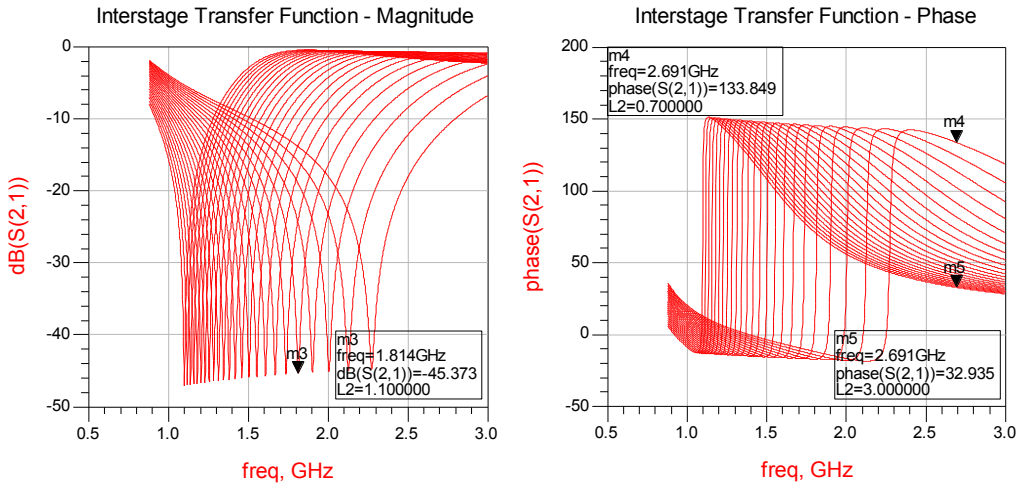


Figure 3-27 – Interstage Transfer Function with Harmonic Trap

at the fundamental and 92° at the 3rd harmonic, which means the phase relationship between the two has changed by 134° by modifying the interstage network. The third important change to the interstage response is the amplitude and phase adjustability at the 3rd harmonic frequency. In Figure 3-27, it can be seen the amplitude and phase at the 3rd harmonic change significantly with the value of the inductor. The 3rd harmonic phase can be adjusted by from 33° to 92°, and the amplitude can be adjusted from -0.8dB to -12.2dB. With the harmonic trap we have a method to adjust the 3rd harmonic in a way that provides improvement to the overall amplifier performance.

From the analysis performed earlier in this section, we know the maximum performance increase occurs when 3rd harmonic level at the output of Q2 is 1/6 the voltage of the fundamental and180° out of phase. Creating this condition is somewhat difficult because there are several unknowns. The 3rd harmonic content generated by Q1 has unknown phase and amplitude, the interstage network changes the phase and amplitude response, and Q2 generates its own 3rd harmonic content while amplifying and phase shifting the two frequencies differently.

To understand how much improvement is achievable in a practical circuit and what the 3rd harmonic should be at the base of Q2, we examine a circuit that is a slightly idealized version of the PAM second stage in Figure 3-28. The schematic is setup for harmonic balance simulation and considers only the second stage without the interstage match. The signal

source is capable of supplying power at both the fundamental frequency and harmonic frequencies. The power and the phase of the 3rd harmonic are setup as simulation variables.

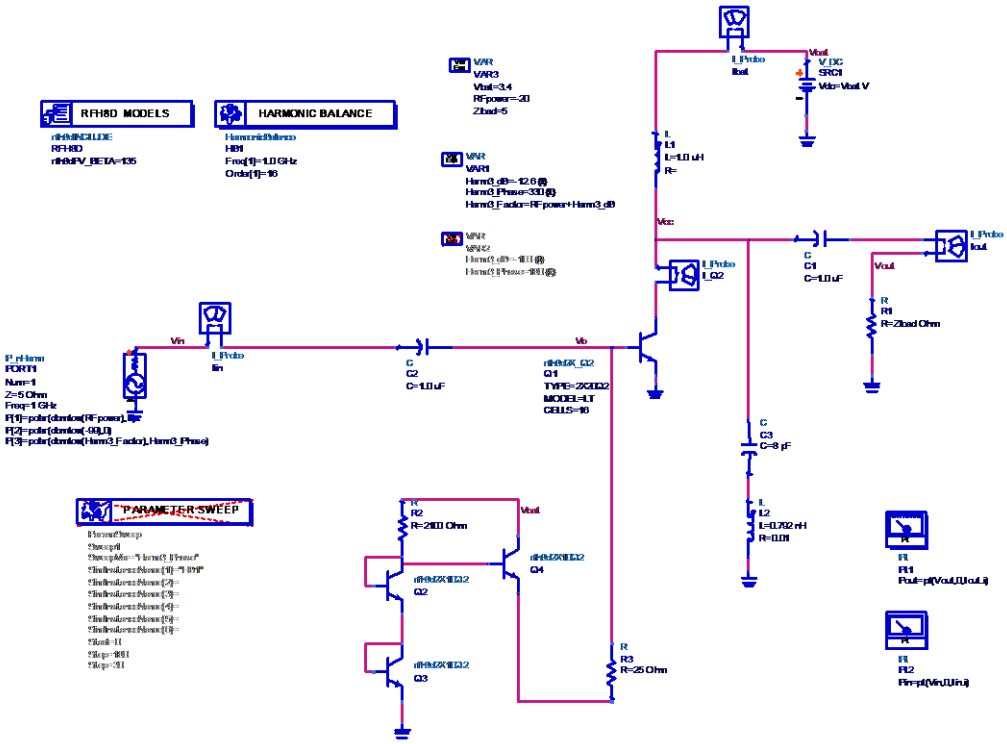


Figure 3-28 – Modified PAM Stage 2 with Harmonic Injection

Figure 3-29 shows efficiency vs. fundamental output power. The harmonic was injected at a low power level and various phases were tested to find the 3rd harmonic phase that gives the best and worst efficiency. A phase of 330° improved the efficiency by 5% and a phase of 180° reduced the efficiency by 5%. The ideal Class F analysis predicts

the two points should be 180° apart and the simulation shows 150° which is very close.

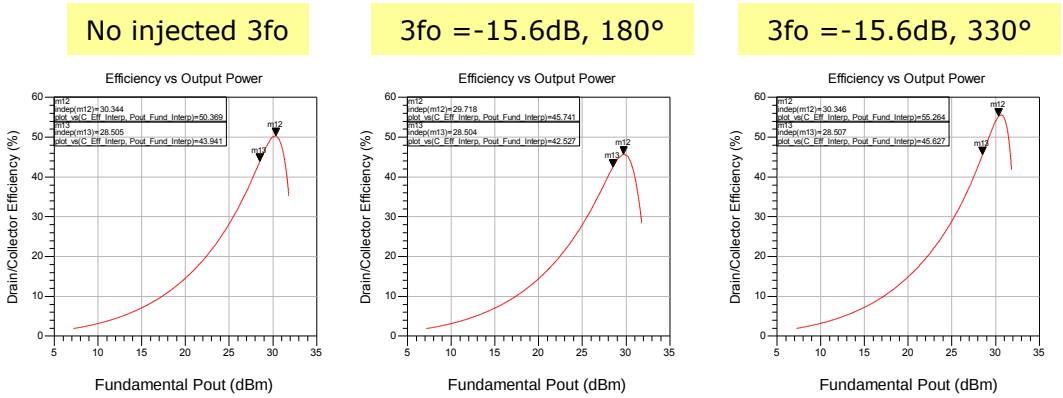


Figure 3-29 – Injected 3rd Harmonic at Different Phases

Using the empirically determined optimum phase we now sweep a range of 3rd harmonic power levels to find the optimum power level for efficiency improvement. The results are displayed in Figure 3-30. The peak efficiency continues to increase as the 3rd harmonic power is increased relative to the fundamental. The maximum efficiency improvement was found when the 3rd harmonic is -6.6dB relative to the fundamental.

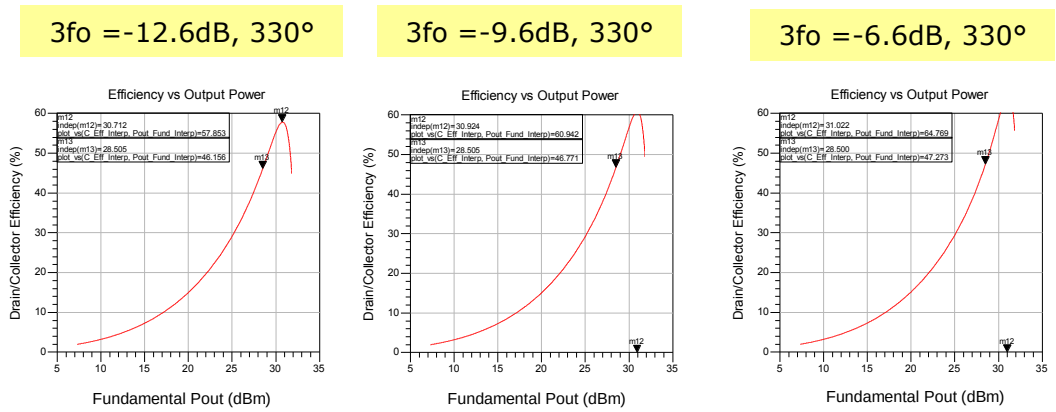


Figure 3-30 – Injected 3rd Harmonic at Different Power Levels

In the circuit shown in Figure 3-28, the transistor output is connected to a load through a DC blocking component. The load has no real dependency other than the second harmonic short created by C3 and L2. In this situation all the 3rd harmonic power is delivered to the load which reduces the overall efficiency. A practical amplifier is usually very reflective at the 3rd harmonic which prevents power being delivered. Figure 3-9 shows the impedance of an output match over a wide range of frequencies. To prevent 3rd harmonic power from being delivered to the load we add a parallel resonant impedance in series with the load. With the 3rd harmonic block in place we re-simulate two conditions. The first is with no harmonic added at the input and the second is with the optimum 3rd harmonic power and phase added.

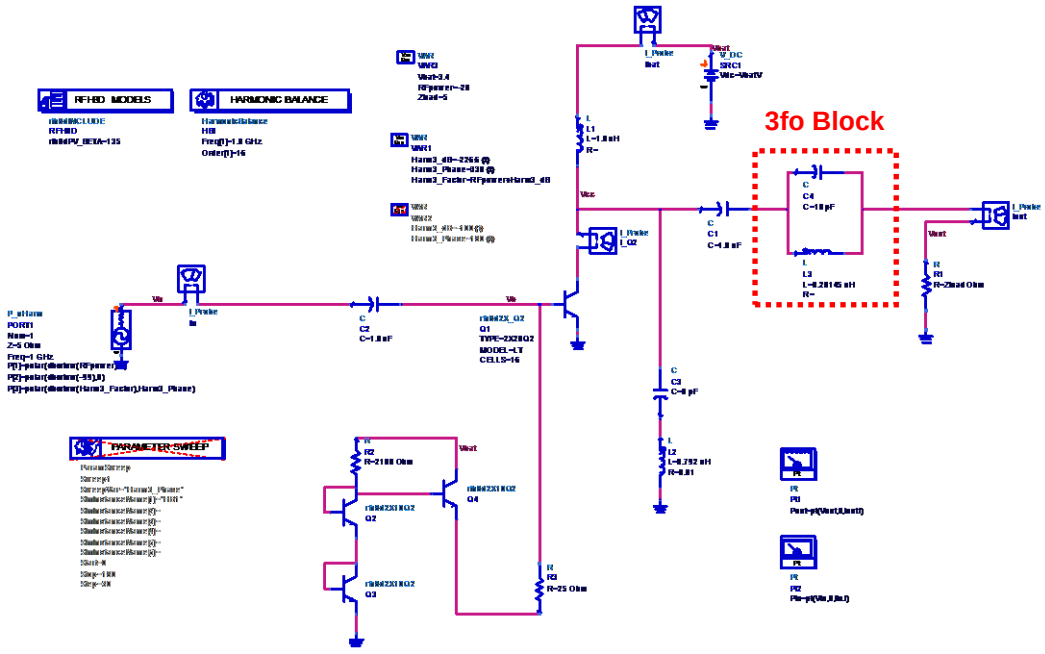


Figure 3-31 – Modified PAM Stage 2 with 3fo Block

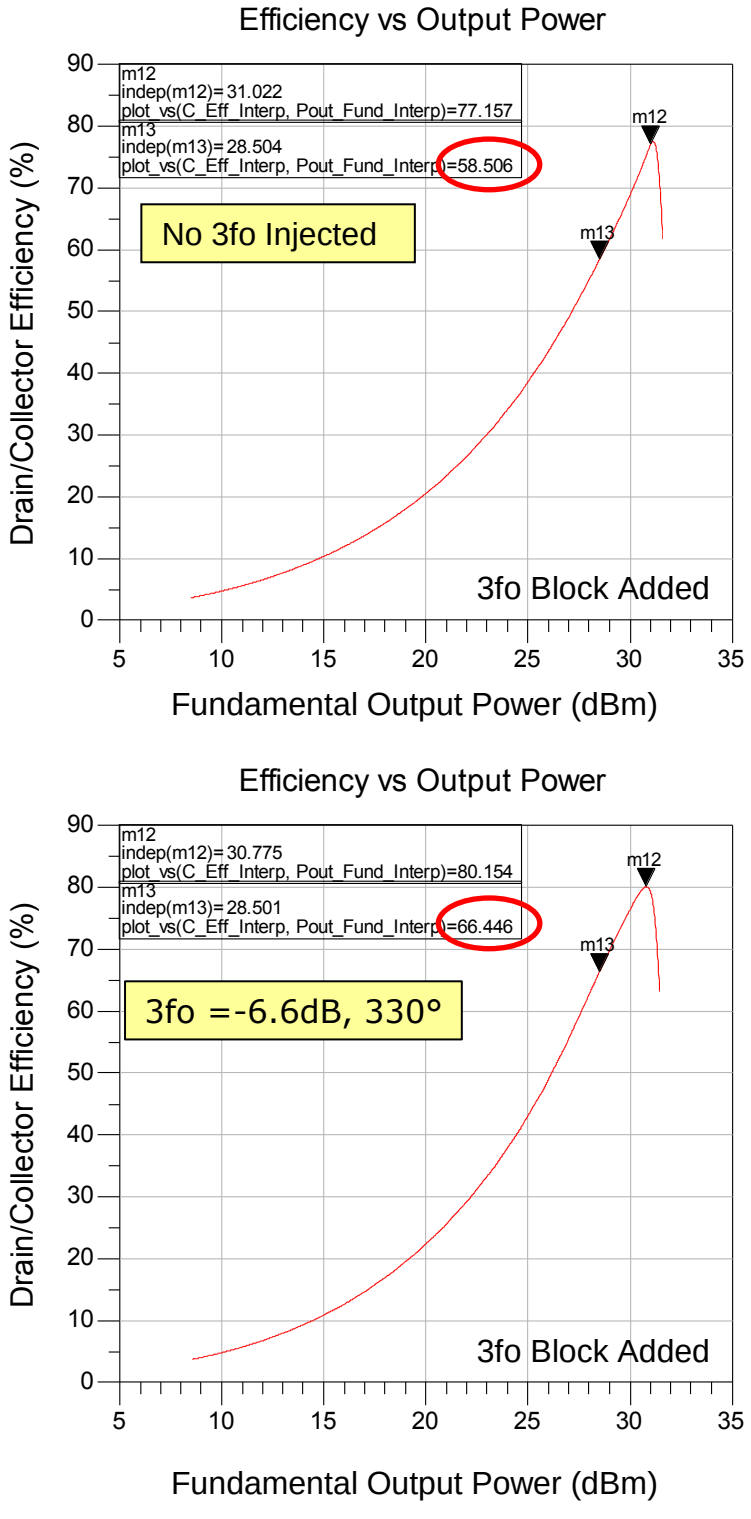


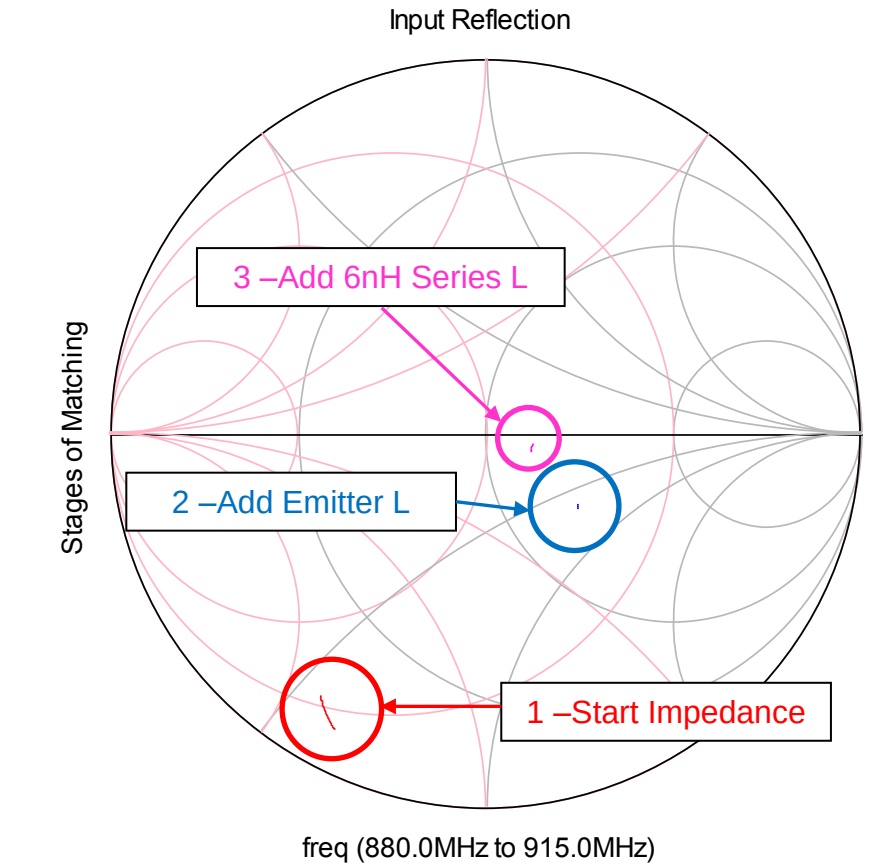
Figure 3-32 – Efficiency Improvement with 3rd Optimum Harmonic

The results of the simulations with the 3rd harmonic trap are shown in Figure 3-32. The output power level at 28.5dBm increases by 8% when the 3rd harmonic excitation is added. In the full amplifier circuit the interstage harmonic trap is used to manipulate the 3rd harmonic power generated in the first stage. If the 3rd harmonic at the input of Q2 is -6.6dBc at a phase of 330° relative to the fundamental we see an 8% increase in efficiency. Because the interstage harmonic trap is unable to change the amplitude and phase independently, we end up with a compromise that is less than the ideal target of 8%. The results of using the interstage match to improve the efficiency are discussed in chapter 4.

SECTION 6: INPUT MATCHING NETWORK

The final part of the amplifier design is to match the input of stage 1 to 50Ω. As mentioned in section 3-4, the first stage does not use capacitive ballasting in the layout. This is done to make the layout easier, and since the first stage transistor comprises only three T4 devices the temperature remains very similar because they are close together. To improve stability and help guard against thermal runaway each cell has a 20Ω resistor in series with it. The resistor also reduces gain and puts some resistance between the base of each cell. We measure the S Parameters of the Q1 cell with the resistors and a 16pF capacitor in series with the base. This is the starting point of the match and is shown in

Figure 3-33 in the red circle. Before adding any matching on the input side of Q1 a 0.5nH inductor is added between the emitter and ground. The inductor is added to improve the noise performance of the amplifier and to raise the input impedance. Once the inductor is added the input impedance shifts to the trace in the blue circle in Figure 3-33. The impedance can now be matched with a 6nH series inductor. The resulting input return loss is shown in the magenta circle in the top graph of Figure 3-33 as well as in the bottom graph. The simulated input return loss is -18dB across the band.



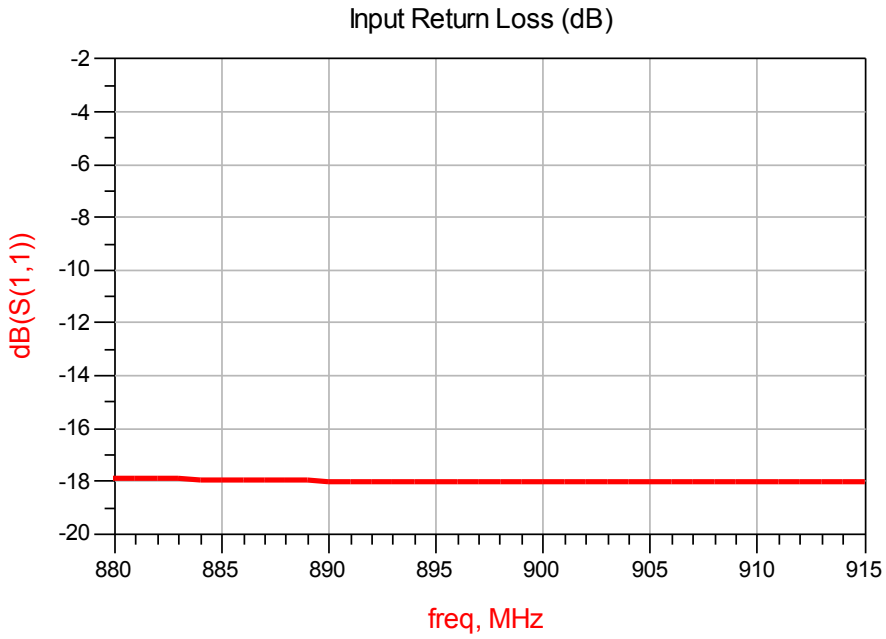


Figure 3-33 – PAM Input Match

Chapter 4

MODULE SIMULATIONS AND MEASURED RESULTS

The material in chapter 3 outlines the design goals and provides detailed information on the different parts of the PA design. With the schematic values determined the module layout is performed. The layout is split into two primarily sections, the GaAs die and the laminate. The die

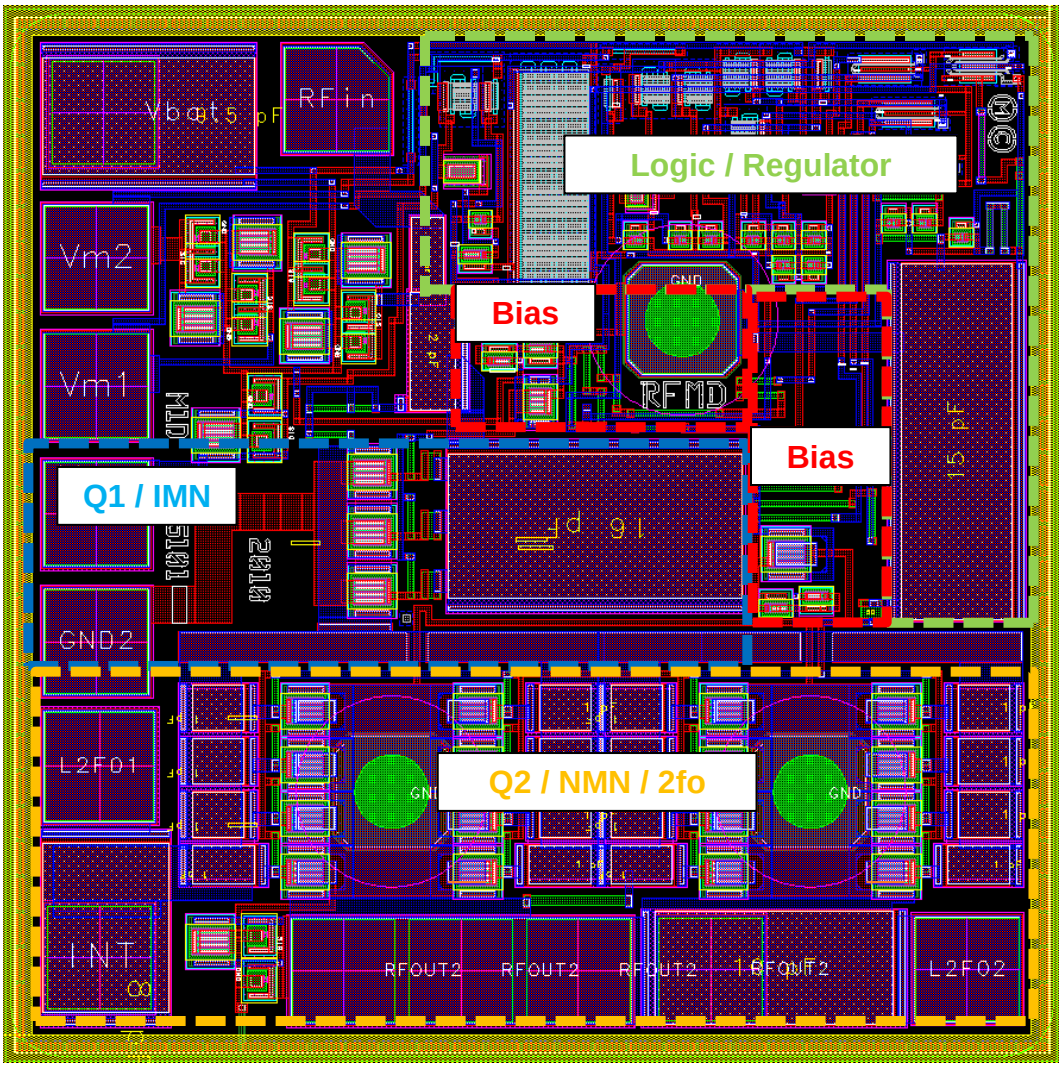


Figure 4-1 – GaAs Die Layout

contains the active devices and as much of the matching network as can be accommodated. In portions of the design where large capacitors (greater than 50pF) or large inductors (greater than 0.5nH) are needed we fabricate the elements using bond wires, laminate traces, or surface mount components. The final die design is shown in Figure 4-1 with the individual sections outlined with colored dashed lines. The physical die size is 750 um x 750 um x 100 um.

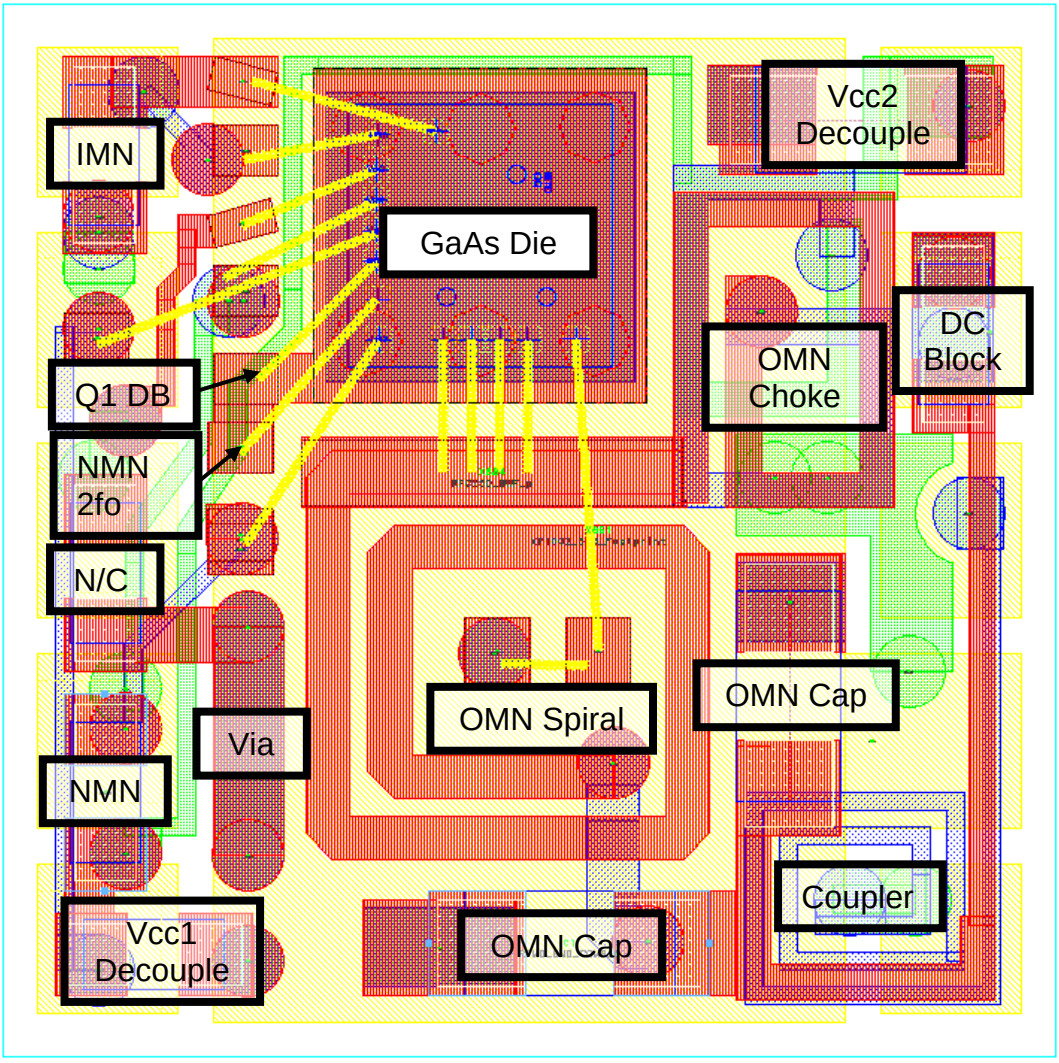


Figure 4-2 – Laminate Layout

The laminate layout is shown in Figure 4-2. The die is mounted at the top center of the laminate. The colors of the metals in Figure 4-2 are defined in section 3-1. Metal 4 (yellow) is used for connecting the module to an application board with pins that go along the right and left edges. The inner portion of metal 4 acts as a ground plane for the PAM.

On metal 3 in the center of the right edge of the module right is a grounded shield structure. When the amplifier is operating the OMN and choke couple power into the coupler. It is necessary to add the shield to prevent degradation of the coupler directivity. Although using the shield reduces this stray coupling effect the directivity is still affected by the coupler's proximity to the choke and OMN.

In the lower left portion of the module a via bar structure (labeled "Via" in Figure 4-2) was added between the OMN and NMN portions of the circuit. The via bar was added to reduce the coupling between the OMN and NMN. The coupling reduced the overall gain and caused stability problems with the module at lower frequencies. Connected to the via bar is an unused component location labeled "N/C". This component location was used during development to experiment with the interstage configuration and isolation between NMN and OMN. In the final circuit it is a vestigial structure.

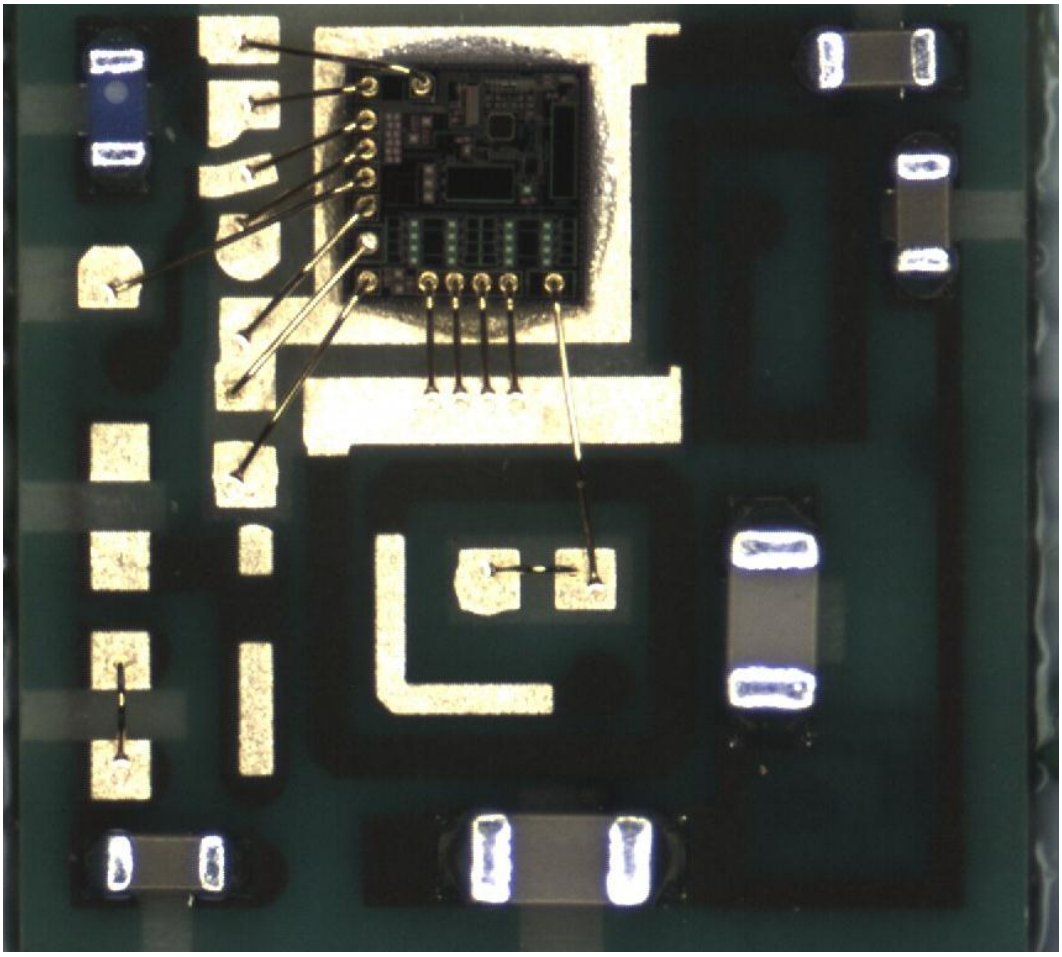


Figure 4-3 – Picture of Completed PA Module

A fully assembled power amplifier module is shown in Figure 4-3. The only notable change from Figure 4-2 is that the NMN SMT inductor from the layout is changed to a bond wire jumper. The inductance derived from the die to laminate bond wire, the laminate trace, and the small jumper bond wire was sufficient to optimize the NMN performance. The jumper bond wire is preferred because it is lower cost and has less variation.

The final die layout, laminate layout, SMT values, and bond wire locations were determined empirically based on the specifications. The portions of the design outlined in chapter 3 were used as a starting point. The design was incrementally modified to improve the performance and meet the specifications. Many intermediate module simulations were performed and material sets were created. The amount of documentation necessary to describe the many changes and iterations of the design is beyond the scope of this thesis. From a pedagogical standpoint including the numerous experiments and attempts to improve the performance make it difficult to see the forest for the trees. However, it is very instructive to understand the difference between the simulated and measured performance. To highlight the differences, we take the final design and create a model based on it. The model is created with the features outlined in section 3-1 and simulated with the technique described in section 2-3. The results of the simulation are shown in Figure 4-4. The simulated data is compared to the actual measured data. Plots of the measured performance are shown in Figures 4-5, 4-6, and 4-7. The differences between the measured performance, simulated performance, and the design targets at 897.5 MHz are summarized in Table 4-1.

The first thing to note is the overall measured efficiency and linearity of the PAM. In Figure 1-2 we examined the linear efficiency of numerous cellular power amplifiers in the market. The goal was to

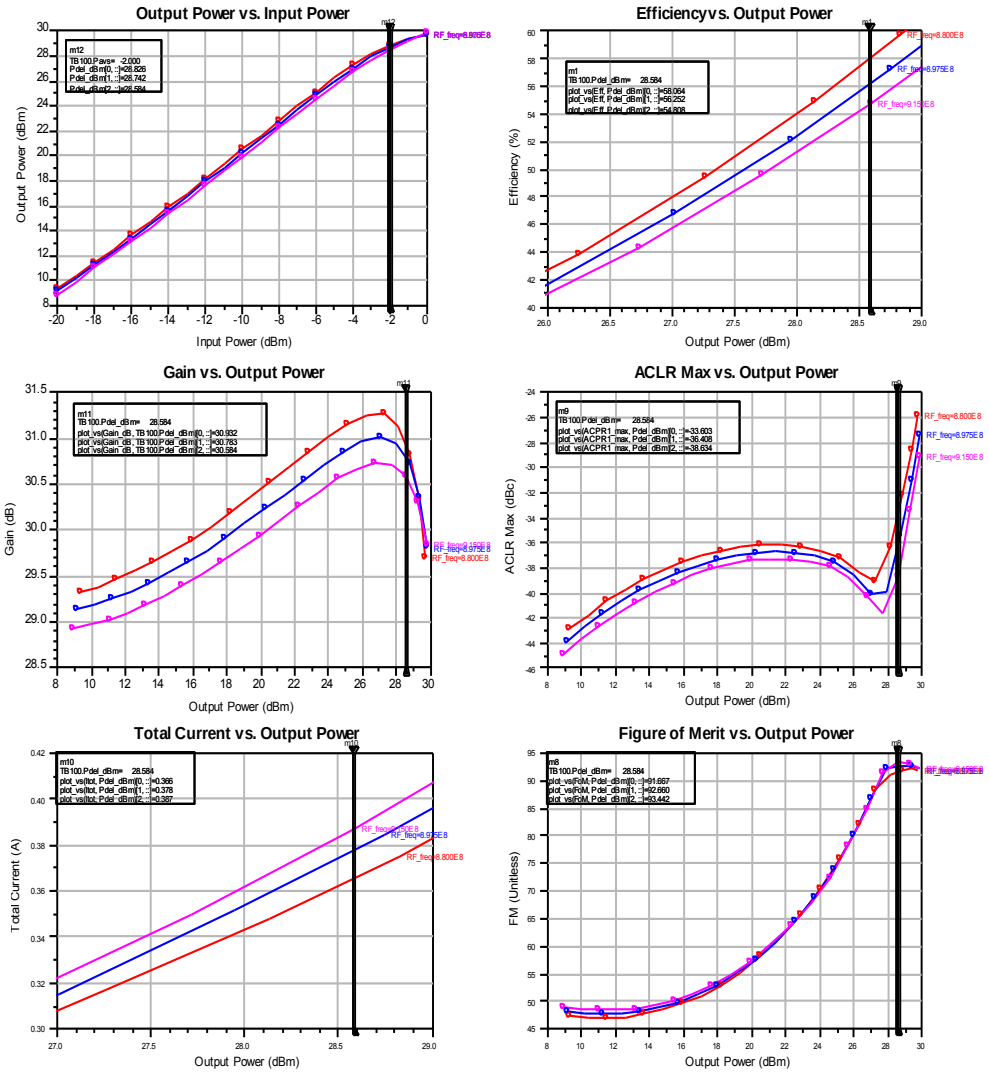
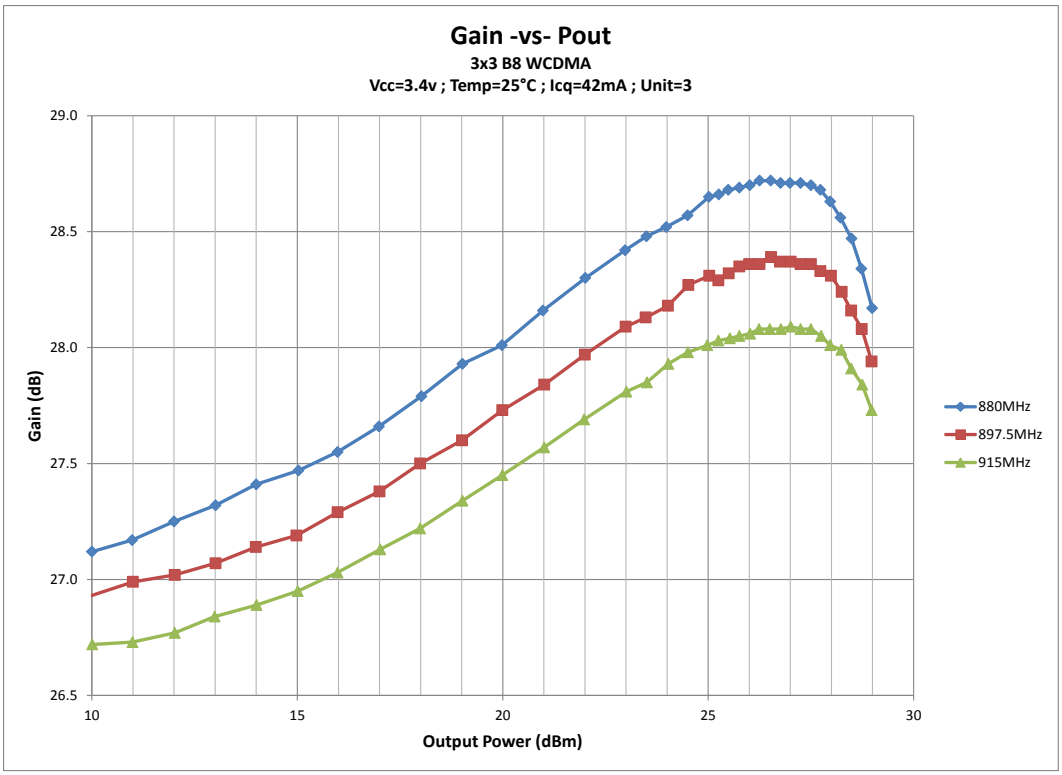


Figure 4-4 – Simulated Performance with WCDMA Voice Modulation



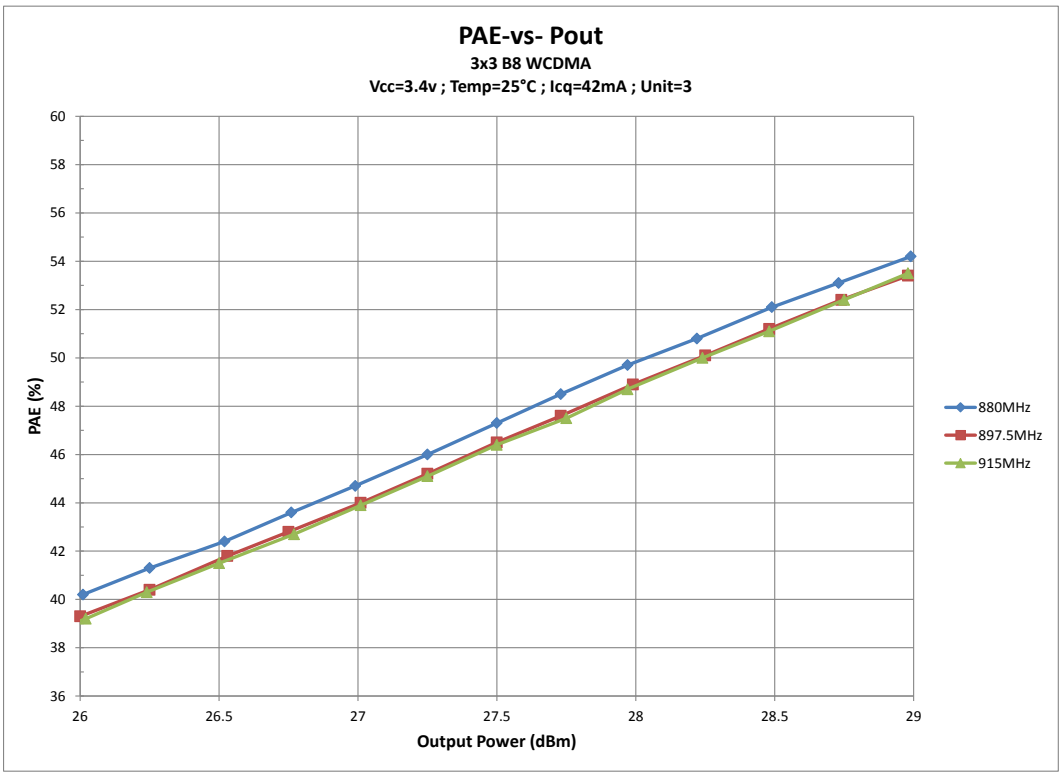
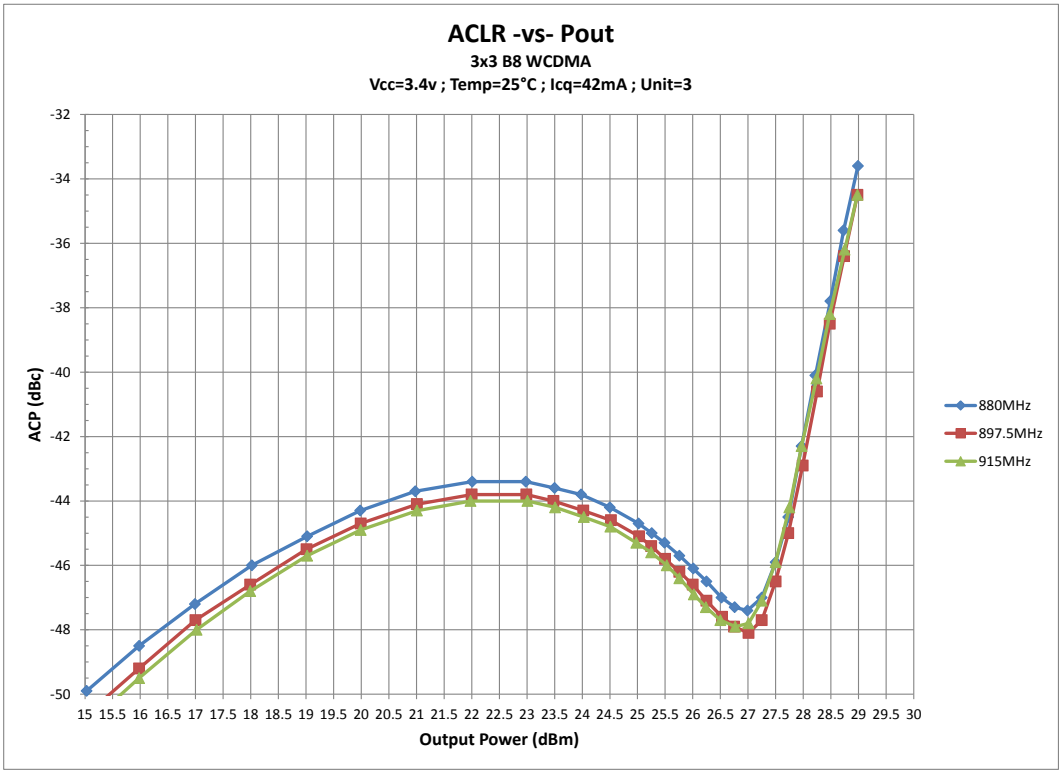


Figure 4-5 – Measured Gain and PAE vs. Output Power



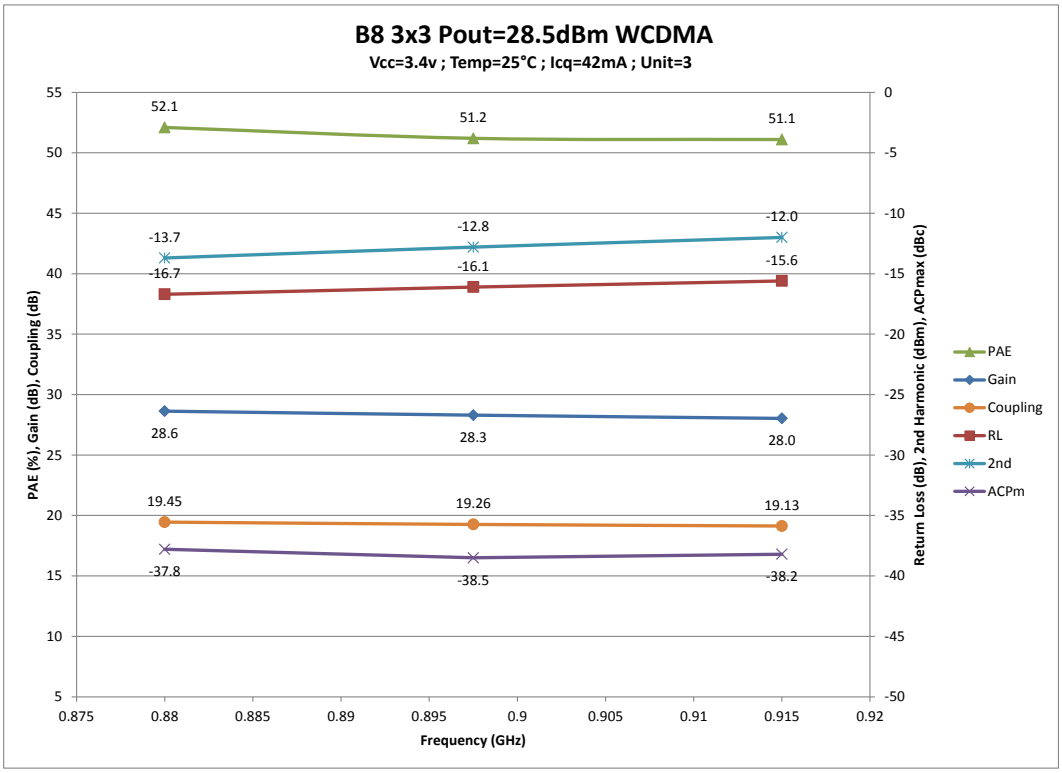


Figure 4-6 – Measured ACLR and Peak Power Performance

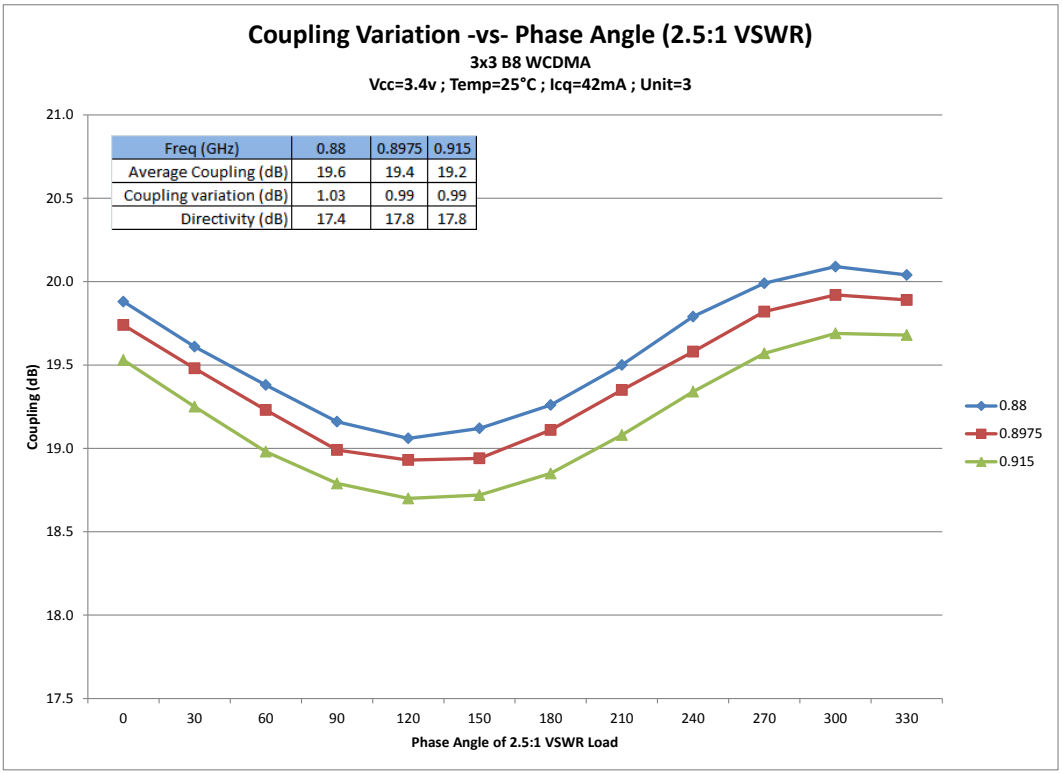


Figure 4-7 – Measured Coupler Variation into 2.5:1 Mismatch

design an amplifier with high output power and high efficiency which corresponds to the red diamond in the upper right portion of Figure 1-2. Table 4-2 shows the measured efficiency is 51.2% at an output power of 28.5dBm with a linearity of -38dBc. The improvement in performance over existing amplifiers is due to the novel interstage implementation, careful selection of the Q1/Q2 device sizes, and the use of a single section output match which favors low loss over high bandwidth.

The agreement between measured and simulated result overall is very good. A cursory comparison of the power drive up profiles in Figures 4-3 through 4-7 shows similar behavior between measured/simulated results versus output power and frequency. A notable exception is the

gain response which is simulated to be 30.8dB and measured to be 28.3dB. The gain difference is partly attributed to coupling between the OMN and NMN. The simulation appears to systematically under represent the coupling between the two matching networks. The Q1 emitter bond wire and the NMN 2nd harmonic bond wire share a common bond pad to ground. Experimentation showed the common inductance between the two networks reduced the overall gain. This effect is also not captured well in the simulation.

Parameter	Specification			Measured	Simulate	Unit	Condition
	Min	Typical	Max	Data	Data		
Frequency Range	880		915	897.5	897.5	MHz	
Vbat	+3.0		+4.2	+3.4	+3.4	V	
Vcc	+0.5	+3.4	+4.2	+3.4	+3.4	V	
Ambient Temperature	-30	+25	+85	+25	+25	°C	
Max Linear Pout in HPM	28.5			28.5	28.6	dBm	Vcc ≥ 3.4v
Max Linear Pout in MPM	19.0			19.0	19.0	dBm	Vcc ≥ 1.48v
Max Linear Pout in LPM	10.0			10.0	9.7	dBm	Vcc ≥ 0.84v
Gain	26	27.5	31	28.3	30.8	dBm	HPM, Pout = 28.5dBm, Vcc=3.4v
	23	24	28	25.8	27.9	dBm	MPM, Pout ≤ 19dBm, Vcc=1.31v
	18	20.5	24	21.2	23.7	dBm	LPM, Pout ≤ 10dBm, Vcc=0.76v
ACLR - 5MHz Offset		-40	-38	-38.5	-36.4	dBc	HPM, Pout = 28.5dBm, Vcc=3.4v
		-40	-38	-40.3	-41.6	dBc	MPM, Pout ≤ 19dBm, Vcc=1.31v
		-40	-38	-40.2	-42.3	dBc	LPM, Pout ≤ 10dBm, Vcc=0.76v
ACLR - 10MHz Offset		-52	-48	-54.1	-	dBc	HPM, Pout = 28.5dBm, Vcc=3.4v
		-60	-48	-62.5	-	dBc	MPM, Pout ≤ 19dBm, Vcc=1.31v
		-60	-48	-63.5	-	dBc	LPM, Pout ≤ 10dBm, Vcc=0.76v
PAE	45	47		51.2	56.2	%	HPM, Pout = 28.5dBm, Vcc=3.4v
	35	41		39.4	42.7	%	MPM, Pout ≤ 19dBm, Vcc=1.31v
	20	22.5		23.1	24.2	%	LPM, Pout ≤ 10dBm, Vcc=0.76v
Current Drain		440	463	406	378	mA	HPM, Pout = 28.5dBm, Vcc=3.4v
		145	170	154	123	mA	MPM, Pout ≤ 19dBm, Vcc=1.31v
		58	65	57	42	mA	LPM, Pout ≤ 10dBm, Vcc=0.76v
Quiescent Current		50	70	42	48	mA	HPM, DC only
		31	50	34	36	mA	MPM, DC only
		20	33	21	21	mA	LPM, DC only
Input Return Loss			-14	-16.1	-18	dB	Pout ≤ 28.5dBm, all modes
Harmonic, 2fo		-22	-12	-12.8	-	dBm	Pout ≤ 28.5dBm, all modes
Harmonic, 3fo		-31		-46.8	-	dBm	Pout ≤ 28.5dBm, all modes
Coupling Factor	-18.3	-20	-22.3	-19.3	-20.5	dB	Pout ≤ 28.5dBm, all modes
Coupler Directivity		20		17.8	25.9	dB	Pout ≤ 28.5dBm, all modes
Temperature=+25°C, VBAT=+3.4V, VEN=+1.8V, 50Ω system, WCDMA Rel 99 Modulation unless otherwise specified							

Table 4-1 – Final Target, Simulated, and Measured Results

Another important difference is the linearity/efficiency tradeoff between the measured and simulated results. The simulation shows higher efficiency but worse linearity with a figure of merit that is higher by two. The linearity/efficiency difference suggests a difference in the load impedance between what is simulated and measured. The figure of merit difference may be due to inaccuracies in the transistor models or loss mechanisms not captured in the model. The difference is not completely understood and the reasons can only be speculated at without further research.

The final difference is with the coupling factor and directivity. The coupler variation into mismatch with the calculated directivity[27] is shown in Figure 4-7. The coupling factor measures about 1dB higher and the directivity measures about 18dB instead of 26dB. A cross sectional analysis was performed and the dielectric thickness between metal 1 and metal 2 was found to be at the minimum allowable limit (37.5 um vs. 50 um nominal). This variation is within the normal manufacturing variation and is considered acceptable. Simulations show when the dielectric thickness is changed to 37.5 um the coupling factor increases by 0.8dB and the directivity is reduced by 5.5dB. The remainder of the directivity discrepancy is explained by stray coupling from other metal structures in the module.

Chapter 5

This thesis naturally suggests several avenues for future research. The most interesting area would be exploring alternate interstage matching networks to enhance the efficiency of the output stage. The approach used in this thesis did not allow for independent control of the amplitude and phase of the 3rd harmonic injected into the final stage. More complex matching networks would allow for independent control. It would also be useful to find alternate ways of creating 3rd harmonic energy at the first stage. If more 3rd harmonic power is available it increases the options for interstage network that can deliver the optimum power and phase to improve efficiency.

It was also noted in section 3-3 that no closed form design equations exist for creating the microstrip coupler that was used in the power amplifier module. It would be useful research to determine closed form expressions to give designers a solid starting point for new designs instead of the current approach of using an EM simulator to design by trial and error.

Further work could also be done to improve the agreement between measurement and simulation. The simulations performed in this thesis did not include EM characterization of the metal structures on the die. Including more design details may improve the agreement. Using a full 3D simulator may also improve the agreement by capturing the

interaction between bond wires and the substrate. A full 3D simulator may also capture coupling between structures that are simulated as separate entities.

REFERENCES

[1] “Key Global Telecom Indicators for the World Telecommunication Service Sector.” Internet: www.itu.int/ITUD/ict/statistics/at_glance/KeyTelecom.html, May. 5, 2012, [Sep. 29, 2012]

[2] “iPhone 4S Teardown.”www.ifixit.com/Teardown/iPhone-4S-Teardown/6610/1, [Sep. 29, 2012]

[3] “3GPP TS 36.101 V9.1.0” Internet: www.etsi.org/deliver/etsi_ts/136100_136199/136101/09.01.00_60/, Oct. 2009 [Sep. 29, 2012]

[4] Mogensen, P.; Wei Na; Kovacs, I.Z.; Frederiksen, F.; Pokhariyal, A.; Pedersen, K.I.; Kolding, T.; Hugl, K.; Kuusela, M.; , "LTE Capacity Compared to the Shannon Bound," Vehicular Technology Conference, 2007. VTC2007-Spring. IEEE 65th , pp.1234-1238, 22-25 Apr. 2007

[5] M. McKinley, K. Remley, M. Myslinski, J. S. Kenney, D. Schreurs, B. Nauwelaers, "EVM Calculation for Broadband Modulated Signals", presented at 64th ARFTG Conf. Dig., Orlando, FL Dec. 2004

[6] Sundstrom, L.; , "Fast and accurate ACLR estimation method," Radio and Wireless Conference, 2004 IEEE , vol., no., pp. 183- 186, 19-22 Sept. 2004

[7] S. Nedeljkovic, J. Mcmacken, P. Partyka, "A Custom III-V Heterojunction Bipolar Transistor Model," *Microwave Journal*, pp. 60-84, Apr. 2009

[8] T. Nielsen, S. Nedeljkovic, D. Halchin, " Large-Signal Hybrid Compact/Behavioral HBT Model for III-V Technology Power Amplifiers," *Microwave Symposium Digest, 2008 IEEE MTT-S International*, pp. 483 - 486, Jun. 2008.

[9] S. Cripps, *Advanced Techniques in RF Power Amplifier Design*. Norwood, MA: Artech House, 2002, pp. 2-9

[10] J. Retz, “Fast ACLR Simulation”, presented at the RFMD Power Amplifier Summit, Greensboro, North Carolina, 2008

[11] M. Medley, *Microwave and RF Circuits: Analysis, Synthesis and Design*. Norwood, MA: Artech House, 1993, pp. 21-34

[12] Yamanouchi, S.; Kunihiro, K.; Hida, H.; , "An efficient algorithm for simulating error vector magnitude in nonlinear OFDM amplifiers," Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004 , vol., no., pp. 129- 132, 3-6 Oct. 2004

[13] “RF7248 3V WCDMA Band 8 Linear PA Module Datasheet.” Internet: https://estore.rfmd.com/RFMD_Onlinestore/Products/RFMD+Parts/PID-P_RF7248.aspx?DC=25, [Oct. 20, 2012]

[14] RFMD Internal Document # PKG-21-1094

[15] Clausen, W.; Moser, B.; , "Modeling of an InGaP/GaAs BiFET VVR Device," Compound Semiconductor Integrated Circuit Symposium, 2009. CISC 2009. Annual IEEE , vol., no., pp.1-4, 11-14 Oct. 2009

[16] “The Modelithics Complete Library.” Internet: www.modelithics.com/products.asp, [Oct. 20, 2012]

[17] C. Bowick, *RF Circuit Design*. Carmel, IN: SAMS, 1995, pp. 157-158

[18] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*. Upper Saddle River, NJ: Prentice-Hall, Inc., 1997, pp. 352-374

[19] S. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 2006, pp. 122-124

[20] T. Bichler, “An Introduction to Broadband Impedance Transformation for RF Power Amplifiers”, *High Frequency Design*, Jan. 2009

[21] D. Pozar, *Microwave Engineering*. Hoboken, NJ: John Wiley & Sons, Inc., 2005, pp 224-227

[22] P. Smith, Electronic Applications of the Smith Chart. Pine Brook, NJ: Kay Electronic Company, 1969, pp. 21-23

[23] D. Pozar, *Microwave Engineering*. Hoboken, NJ: John Wiley & Sons, Inc., 2005, pp 537-538

[24] Yang Li; Prikhodko, D.; Zhu, R.; Abdallah, H.; Nabokin, S.; Batrin, M.; Tkachenko, Y.; , "A compact high directivity coupler with ±0.15dB error under VSWR 2.5:1 for 3×3mm2 UMTS power amplifier modules," Radio and Wireless Symposium (RWS), 2010 IEEE , vol., no., pp.336-339, 10-14 Jan. 2010

[25]Toyoda, I.; Hirota, T.; Hiraoka, T.; Tokumitsu, T.; , "Multilayer MMIC branch-line coupler and broad-side coupler," Microwave and Millimeter-Wave Monolithic Circuits Symposium, 1992. Digest of Papers, IEEE 1992 , vol., no., pp.79-82, 1-3 Jun 1992

[26] Prouty, M.D.; Schwarz, S.E.; , "Hybrid couplers in bilevel microstrip," Microwave Theory and Techniques, IEEE Transactions on , vol.41, no.11, pp.1939-1944, Nov 1993

[27]Abdallah, E.A.F.; El-Said, M.; Ahmed, A.A.N.; El-Kinawy, E.E.K.; , "Analysis and design of broadside and overlap microstrip line couplers by finite element method," Circuits and Systems, 1992., Proceedings of the 35th Midwest Symposium on , vol., no., pp.647-650 vol.1, 9-12 Aug 1992

[27] D. Pozar, *Microwave Engineering*. Hoboken, NJ: John Wiley & Sons, Inc., 2005, pp 314-315

[28] RFMD Internal Document # FAB-09-2089

[29] Liou, L.L.; Bayraktaroglu, B.; Huang, C.I.; , "Thermal runaway analysis of high power AlGaAs/GaAs heterojunction bipolar transistors," High Speed Semiconductor Devices and Circuits, 1993. Proceedings., IEEE/Cornell Conference on Advanced Concepts in , vol., no., pp.468-477, 2-4 Aug 1993

[30] Noh, Y.S.; Park, J.H.; Park, C.S.; , "A novel bias circuit and MMIC power amplifier implementation for W-CDMA mobile handsets," Radio and Wireless Conference, 2004 IEEE , vol., no., pp. 359- 362, 19-22 Sept. 2004

[31] Youn Sub Noh; Chul Soon Park; , "PCS/W-CDMA dual-band MMIC power amplifier with a newly proposed linearizing bias circuit," Solid-State Circuits, IEEE Journal of , vol.37, no.9, pp. 1096- 1099, Sep 2002

[32] Raab, F.H.; "Class-F power amplifiers with maximally flat waveforms," Microwave Theory and Techniques, IEEE Transactions on , vol.45, no.11, pp.2007-2012, Nov 1997

[33] S. Cripps, *RF Power Amplifiers for Wireless Communications*. Norwood, MA: Artech House, 2006, pp. 143-148