Compact Modeling of Multi-Gate Transistors

by

Gajanan Dessai

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved November 2012 by the
Graduate Supervisory Committee:

Gennady Gildenblat, Chair
Colin McAndrew
Yu Cao
Hugh Barnaby

ARIZONA STATE UNIVERSITY

December 2012

ABSTRACT

Scaling of the classical planar MOSFET below 20 nm gate length is facing not only technological difficulties but also limitations imposed by short channel effects, gate and junction leakage current due to quantum tunneling, high body doping induced threshold voltage variation, and carrier mobility degradation. Non-classical multiple-gate structures such as double-gate (DG) FinFETs and surrounding gate field-effect-transistors (SGFETs) have good electrostatic integrity and are an alternative to planar MOSFETs for below 20 nm technology nodes. Circuit design with these devices need compact models for SPICE simulation.

In this work physics based compact models for the common-gate symmetric DG-FinFET, independent-gate asymmetric DG-FinFET, and SGFET are developed. Despite the complex device structure and boundary conditions for the Poisson-Boltzmann equation, the core structure of the DG-FinFET and SGFET models, are maintained similar to the surface potential based compact models for planar MOSFETs such as SP and PSP.

TCAD simulations show differences between the transient behavior and the capacitance-voltage characteristics of bulk and SOI FinFETs if the gate-voltage swing includes the accumulation region. This effect can be captured by a compact model of FinFETs only if it includes the contribution of both types of carriers in the Poisson-Boltzmann equation. An accurate implicit input voltage equation valid in all regions of operation is proposed for common-gate symmetric DG-FinFETs with intrinsic or lightly doped bodies. A closed-form algorithm is developed for solving the new input voltage equation including ambipolar effects. The algorithm is verified for both the surface potential and its derivatives and includes a previously published analytical approximation for surface potential as a special case when ambipolar effects can be neglected. The symmetric linearization method for common-gate symmetric DG-FinFETs is developed in a form free of the charge-sheet approximation present in

its original formulation for bulk MOSFETs. The accuracy of the proposed technique is verified by comparison with exact results.

An alternative and computationally efficient description of the boundary between the trigonometric and hyperbolic solutions of the Poisson-Boltzmann equation for the independent-gate asymmetric DG-FinFET is developed in terms of the Lambert W function. Efficient numerical algorithm is proposed for solving the input voltage equation. Analytical expressions for terminal charges of an independent-gate asymmetric DG-FinFET are derived. The new charge model is C^{∞} continuous, valid for weak as well as for strong inversion condition of both the channels and does not involve the charge-sheet approximation. This is accomplished by developing the symmetric linearization method in a form that does not require identical boundary conditions at the two Si-SiO_2 interfaces and allows for volume inversion in the DG-FinFET. Verification of the model is performed with both numerical computations and 2D TCAD simulations under a wide range of biasing conditions. The model is implemented in a standard circuit simulator through Verilog-A code. Simulation examples for both digital and analog circuits verify good model convergence and demonstrate the capabilities of new circuit topologies that can be implemented using independent-gate asymmetric DG-FinFETs.

Dedicated to my parents and teachers

ACKNOWLEDGEMENTS

This dissertation would not have been possible without the assistance and support of many people. First of all I would like to express my sincere gratitude to my advisor Prof. Gennady Gildenblat for his guidance, encouragement, and support throughout my graduate years at Arizona State University (ASU). His attitude and professionalism towards work has been a source of inspiration for me. He always encouraged me to explore new ideas.

I would also like to thank members of my Ph.D. supervisory committee, Dr. Colin McAndrew, Prof. Yu Cao, and Prof. Hugh Barnaby for taking their time to review my dissertation and for their valuable comments. I am highly indebted to Dr. Colin McAndrew. His insightful comments and questions during our technical discussion and review of the manuscripts helped improve my dissertation research. I would also like to thank Prof. Bertan Bakkaloglu for discussing circuit aspects of compact modeling.

I would like to thank Prof. A. B. Bhattacharyya for introducing me to the exciting field of semiconductor devices and compact modeling. I came across various compact MOSFET models and modeling approaches during my association with his work on the book titled "Compact MOSFET Models for VLSI Design".

As a part of PSP Compact Modeling Group I was fortunate to work with fellow group mates Dr. Wei Yao (now with Xilinx), Dr. Zeqin Zu (now with Freescale), Dr. Xin Li (now with GLOBALFOUNDRIES), and Dr. Weimin Wu (now with Texas Instruments). I thank them for their friendship and having many illuminating discussions on topic related to device physics and compact modeling. The support of the staff from Electrical Engineering Department at ASU is also greatly appreciated. My most rewarding experience was the summer I spent at GLOBALFOUNDRIES where I had an opportunity to work on practical aspects of CMOS technology and modeling.

My graduate life at ASU would not have been wonderful and fulfilling without many of my friends whom I met during my time at ASU. I thank them all.

Most importantly, I would like to thank my family for their immense support and encouragement, without whom none of this would have been possible. Especially, I heartily thank my dear wife Prajakta for her lasting love, understanding, and encouragement.

TABLE OF CONTENTS

Page

LIST OF FIGURES viii

CHAPTER

1 INTRODUCTION 1

1.1 Scaling Limits of Conventional Planar MOSFETs 1

1.2 Multi-Gate MOSFET Structures and their Advantages 3

1.3 Compact Modeling 7

1.4 Organization of the Dissertation 8

1.5 Summary of the Original Results Obtained in this Work 9

1.6 List of Publications Related to this Work 10

2 ELECTROSTATICS of the COMMON-GATE SYMMETRIC DG-FinFET 12

2.1 Introduction 12

2.2 TCAD simulations of bulk and SOI FinFETs 13

2.3 Poisson-Boltzmann Equation for DG-FinFET 16

2.4 Common-Gate Symmetric DG-FinFET 18

2.5 Exact IVE for Common-Gate Symmetric DG-FinFET 20

2.6 Approximate Input Voltage Equation 23

2.7 Unipolar IVE 27

2.8 Closed Form Solution of the Ambipolar IVE 29

3 ELECTROSTATICS of the INDEPENDENT-GATE ASYMMETRIC DG-FinFET 35

3.1 Introduction 35

3.2 Trigonometric Solution 37

3.3 Hyperbolic Solution 39

3.4 Solution Space 41

3.5 Analytical Expression for the Partition Lines 46

3.6 A New Solution Technique for the IVEs 47

Chapter Page

4 CURRENT and CHARGE MODELS for the COMMON-GATE SYMMETRIC DG-FinFET . . . 50

4.1 Introduction . . . 50

4.2 Exact Drain Current . . . 51

4.3 Charge-Sheet Approximation . . . 52

4.4 Symmetric Linearization Method . . . 57

4.5 Terminal Charges . . . 59

4.6 Symmetric Linearization Method for SGFET . . . 66

5 CURRENT and CHARGE MODELS for the INDEPENDENT-GATE ASYMMETRIC DG-FinFET . . . 71

5.1 Drain Current Model . . . 71

5.2 Reformulation of Drain Current in PSP Form . . . 74

5.3 Effective Gate Charge Density Concept . . . 77

5.4 Terminal Charge Model . . . 82

5.5 Results and Discussion . . . 85

5.6 Model Implementation and Simulation . . . 93

6 CONCLUSIONS . . . 96

REFERENCES . . . 98

APPENDIX

A Derivation of (2.26) . . . 108

B Equivalent form of Equation (2.26) . . . 110

C Asymptotes of φ_0 for the Common-Gate Symmetric DG-FinFET . . . 112

D Derivation of $\tilde{q}_\mathrm{n}$ and α_l . . . 115

E Comparison of Symmetric Linearization Method for bulk MOSFETs and DG-FinFETs . . . 118

F Derivation of (5.74)-(5.77) . . . 122

G Common-Gate Symmetric DG-FinFET as a Special Case of Independent-Gate Asymmetric DG-FinFET . . . 124

LIST OF FIGURES

Figure Page

1.1 Structure of (a) bulk FinFET and (b) SOI FinFET. 4

1.2 Independent double-gate (a) FinFET on SOI and (b) ETSOI. 6

1.3 Cross-section of various flavors of multi-gate MOSFETs (a) π-gate , (b) Ω-gate, (c) quad-gate and (d) surrounding-gate. 7

2.1 Simulated device structures (a) bulk FinFET and (b) SOI FinFET. . . . 14

2.2 TCAD simulated normalized transcapacitances (a) C_{gg}, C_{bg} and (b) C_{dg} for bulk and SOI FinFETs with source, drain, and bulk connected. . . . 15

2.3 Cross-section of the common-gate symmetric DG-FinFET. ϕ is the work-function of gate material. 16

2.4 Energy band diagram (a) across the channel ($V_{\mathrm{d}} = V_{\mathrm{s}} = 0$) and (b) along the channel indicating the reference energy level for measuring electrostatic potential ψ. Solid lines corresponds to $\psi = 0$ whereas dashed lines corresponds $\psi > 0$. E_{fm} is the gate Fermi level. 17

2.5 $a(\varphi_0)$ dependence; $t_{\mathrm{si}} = 20$ nm, $T = 300$ K. 24

2.6 Surface and center potential versus gate voltage. Circles represent exact calculations based on (2.27) and the lines corresponds to the new approximation (2.38); $V_{\mathrm{c}} = 0$ V, $t_{\mathrm{si}} = 20$ nm, $t_{\mathrm{ox}} = 2$ nm, $\Delta\phi = 0$ V, $T = 300$ K. 25

2.7 (a) $d\psi_{\mathrm{s}}/dV_{\mathrm{gs}}$ and (b) $d^2\psi_{\mathrm{s}}/dV_{\mathrm{gs}}^2$ versus gate voltage. Circles represent exact calculation and the lines corresponds to the new approximation; $V_{\mathrm{c}} = 0$ V, $t_{\mathrm{si}} = 20$ nm, $t_{\mathrm{ox}} = 2$ nm, $\Delta\phi = 0$ V, $T = 300$ K. 26

2.8 Surface and center potential obtained by solving IVE using closed form algorithm is compared with that obtained by bisection method. Lines and symbols corresponds to the results obtained from closed form algorithm and numerical solution, respectively; $t_{\mathrm{ox}} = 2$ nm, $t_{\mathrm{si}} = 20$ nm, $\Delta\phi = 0$. . 31

Figure Page

2.9 Error in the surface potential obtained by new algorithm when compared to that obtained by numerical solution of (2.50) for $V_c = 0$V. Device parameters are the same as in Fig. 2.8. 32

2.10 (a) First and (b) second derivative of the surface potential with respect to the gate voltage obtained by solving IVE using closed form algorithm is compared with that obtained by numerical solution. Lines and symbols corresponds to the results obtained from closed form algorithm and numerical solution, respectively. Device parameters are same as in Fig. 2.8. 33

2.11 (a) Surface potential obtained by solving IVEs (2.50), (2.57), and (2.61) for $V_c = 0$ V, (b) Surface potential near flatband condition. Device parameters are same as in Fig. 2.8. 34

3.1 Cross-section of the independent-gate asymmetric DG-FinFET. ϕ_1 and ϕ_2 are the workfunctions of gate-1 and gate-2, respectively. 37

3.2 Regions of operation on the V_1-V_2 plane for $V_c = 0.5$ V, $t_{si} = 20$ nm, $t_{ox1} = 2$ nm and $t_{ox2} = 40$ nm. 42

3.3 Partition lines on the V_1-V_2 plane with V_c as parameter obtained from numerical solution (circles) and analytical solution (lines); $t_{si} = 20$ nm, $t_{ox1} = t_{ox2} = 2$ nm. 44

3.4 Partition lines on V_1-V_2 plane with V_c as parameter obtained from numerical solution (circles) and analytical solution (lines); $t_{si} = 20$ nm, $t_{ox1} = 2$ nm , $t_{ox2} = 40$ nm. 44

3.5 Partition lines on V_1-V_2 plane with V_c as parameter obtained from numerical solution (circles) and analytical solution (lines); $t_{si} = 10$ nm, $t_{ox1} = 2$ nm , $t_{ox2} = 40$ nm. 45

3.6 Regions of operation on the $V_1 - V_2$ plane for $V_c = 0.5$ V, $t_{si} = 10$ nm, $t_{ox1} = 2$ nm and $t_{ox2} = 20$ nm. 48

4.1 Relative error for drain current I_d using expression (4.11); $t_{ox} = 1.5$ nm, $T = 300$ K, $V_{ds} = 1$ V. 53

Figure Page

4.2 $g(\theta)$ versus θ. 55

4.3 Position dependence of surface potential in DG-FinFET; $t_{\rm ox} = 1.5$ nm, $t_{\rm si} = 20$ nm, and $V_{\rm ds} = 2$ V. 60

4.4 Normalized transcapacitances of (a) bulk FinFET and (b) SOI FinFET versus gate voltage for $V_{\rm ds} = 1$V. Symbols represents TCAD simulations results and the lines corresponds to a compact model. 63

4.5 Relative error for the terminal charges, using symmetric linearization method for DG-FinFET; $t_{\rm si} = 20$ nm, $t_{\rm ox} = 1.5$ nm, $T = 300$ K, $V_{\rm ds} = 1$ V. 64

4.7 Cross-section of the SGFET. 66

4.8 Relative error for the terminal charges, using symmetric linearization method for SGFET; $R = 8$ nm, $t_{\rm ox} = 1.5$ nm, $T = 300$ K, $V_{\rm ds} = 1$ V. . 69

5.1 Comparison of terminal charges (a) and transcapacitances (b) obtained from the new model and numerical computations; $t_{\rm ox1} = t_{\rm ox2} = 2$ nm , $V_{\rm g2} = 0.4$ V and $V_{\rm d} = 1.5$ V. 87

5.2 Comparison of terminal charges (a) and transcapacitances (b) obtained from the new model and numerical computations; $t_{\rm ox1} = t_{\rm ox2} = 2$ nm, $V_{\rm g2} = 1.0$ V and $V_{\rm d} = 0.5$ V. 88

5.3 Comparison of terminal charges (a) and transcapacitances (b) obtained from the new model and numerical computation; $t_{\rm ox1} = t_{\rm ox2} = 2$ nm, $V_{\rm g1} = 2.0$ V and $V_{\rm g2} = 0.6$ V. 89

5.4 Comparison of transcapacitances obtained from the new model and numerical computations; $t_{\rm ox1} = 2$ nm, $t_{\rm ox2} = 10$ nm, $V_{\rm g2} = 0.6$ V and $V_{\rm d} = 0.5$ V. 90

5.5 Comparison of transcapacitances obtained from the new model and numerical computations; $t_{\rm ox1} = 2$ nm, $t_{\rm ox2} = 10$ nm, $V_{\rm g2} = 1.5$ V and $V_{\rm d} = 2.0$ V. 90

Figure Page

5.6 Comparison of transcapacitances obtained from the new model and numerical computations; $t_{\mathrm{ox1}} = 2$ nm, $t_{\mathrm{ox2}} = 10$ nm, $V_{\mathrm{g1}} = 2.0$ V and $V_{\mathrm{g2}} = 0.6$ V. 91

5.7 Comparison of terminal charges (a) and transcapacitances (b) obtained from the new model and numerical computation at $V_{\mathrm{ds}} = 0.0$ V; $t_{\mathrm{ox1}} = 2$ nm, $t_{\mathrm{ox2}} = 10$ nm, and $V_{\mathrm{g2}} = 0.7$ V. 92

5.8 Double balanced mixer. 94

5.9 Schmitt trigger. 94

5.10 Harmonic balance simulation of double balance mixer shown in Fig. 5.8. 95

5.11 Transfer characteristics of independent-gate FinFET Schmitt trigger shown in Fig. 5.9. 95

Chapter 1

INTRODUCTION

1.1 Scaling Limits of Conventional Planar MOSFETs

Planar MOSFETs have been the basis of CMOS technologies since their inception in 1960 [1]. Continuous improvement as predicted by Moore's law [2] has been achieved by scaling and material innovations keeping the classical planar structure unchanged. Scaling the channel length results in higher currents and hence faster switching speed. Scaling is accomplished by following certain rules called "scaling rules" to attain optimum device performance [3]. The aim is to have a transistor with high on-state current, zero off-state current, a sharp transition from off-state to on-state and the terminal currents apart from the drain to the source terminal must be zero i.e., zero parasitic effects. Classical scaling rules reduce device dimensions (such as channel length, gate oxide thickness, junction depth) and increase doping concentration which helps in boosting on-current and keeps off-current under control. Reducing device dimensions by scaling not only resulted in higher packing density (i.e. more circuits functionality on given die area) but also higher speed, lower power, reduced manufacturing cost, and other performance improvements.

As the feature size approached the sub-100 nm range, the scaling of planar MOSFETs was confronted with many technological limitations as well as problems related with the device characteristics. The problems with scaling of planar MOSFETs are severe short channel effects (SCEs) including threshold voltage ($V_{\rm th}$) roll-off, drain induced barrier lowering (DIBL), and subthreshold-slope (SS) degradation [4]. This is because as the channel length is reduced the field lines originating from the drain/source regions strongly influence the channel potential and reduce the barrier seen by the injecting electrons at the source which enhances the drain current [5]. Ideally, the barrier is controlled by the applied gate field. To increase the gate control of the channel the gate oxide must be made thinner and the channel doping must be increased as suggested by the classical scaling rules. Although this approach

has been followed over the decades, in recent years this has given rise to a series of undesirable effects such as parasitic tunneling current, mobility degradation, and random dopant fluctuation (RDF).

As the gate oxide thickness is reduced the gate current, due to the quantum tunneling, increases exponentially and therefore increases the standby power dissipation. In the current sub-100 nm planar CMOS technologies the gate oxide thickness has been reduced to the point where the power drain from gate leakage is comparable to the power used for circuit switching [6]. In highly doped MOSFETs the presence of a large number of dopant ions hinders carrier motion due to Coulomb scattering and reduces mobility [7]. Additionally, higher channel doping increases the surface electric field for a given inversion level which results in reduced carrier mobility due to surface scattering [8]. The high surface electric field confines the carriers in a narrow potential well resulting in quantum confinement effects [9]. Also a high gate oxide field depletes the poly-silicon gate with appreciable amount of potential drop thus reducing the effective gate bias [10]. Quantum confinement [4, 11] and poly-silicon depletion [12] leads to a threshold voltage shift and gate capacitance decreases. On the other hand, the RDF effect originate due to the discrete nature of dopant ions in the channel region which become prominent at small geometry because the total number of dopant ions is small; hence, their statistical fluctuation is large, which alters the transistor properties especially threshold voltage and drive current [13]. High body doping increases the electric field in the reverse biased source/drain to body junction which significantly enhances the junction band-to-band tunneling (BTBT) current [14].

Even with the above mentioned detrimental side effects of scaling, the classical planar MOSFET has been scaled to 28 nm technology node with ultra-shallow junction, pocket implants [15], and super-steep retrograde channel doping [16]. Material innovations such as high-k dielectric, metal-gate, mechanically inducing strain in the channel and employing alternative channel materials such as SiGe, Ge semi-

conductors helped to push the planar CMOS technology under 100 nm node. With the high-k dielectric as gate insulator material the effective insulator thickness is decreased without decreasing the physical insulator thickness enabling the higher gate control on the channel and the metal-gate eliminates the poly-silicon depletion effect [17, 18]. Suppression of source/drain lateral electric field can be achieved by locally raising the channel doping near source and drain junctions via pocket implants [19]. Process induced strain is used to achieve significant mobility enhancement [20]. With such ingenious technological developments the planar MOSFET has been pushed to the limit. A paradigm shift in device structure was necessary for further scaling and performance improvement.

Multi-gate MOSFETs where the gates are present on more than one side of the channel are seen as an alternative for pushing the CMOS scaling forward under sub-20 nm gate length [21]. The primary advantage of the Multi-gate MOSFETs is the excellent control of SCEs [22, 23] without relying on channel doping, which makes it potentially scalable to the end of the SIA ITRS roadmap [24].

1.2 Multi-Gate MOSFET Structures and their Advantages

Having more than one gate around the channel improves the electrostatic integrity which is the measure of electric field lines from the source/drain influencing the channel region. Higher electrostatic control by the gate results in reduced short channel effects. Various flavors of alternative device structures having multiple gates have been proposed to replace the classical planar MOSFET and extend the channel length scalability into the sub-20 nm regime. Multi-gate MOSFETs shown in Fig. 1.1 have been proven to be strong candidates for the future CMOS technology [25] and been in production in Intel at 22 nm technology node [26]. Such MOSFETs are known as FinFETs [27, 28]. FinFETs offer increased immunity to small-geometry effects, a near-ideal subthreshold slope, and certain other advantages like the increased mobility associated with low or no doping. Lower doping results in less effective electric field which reduces surface carrier scattering and gate tunneling.

The use of an undoped or lightly doped body provides immunity to threshold voltage and drive current variation due to statistical dopant fluctuations in FinFETs. Because of strong coupling between gates the whole potential across the silicon film moves along with the gate voltage and the carriers are not just induced at the interface but throughout the body which is called “volume inversion” [29]. This leads to a near-ideal subthreshold slope (60mV/decade) which improves device turn-off behavior and reduces off-state current. For planar MOSFETs the substrate doping not only served to control the SCEs but also enabled threshold voltage adjustment. In FinFETs the freedom for threshold voltage adjustment is lost with the absence of doping. However, in FinFETs the required threshold voltage is usually set by gate work-function adjustment [30]. Moreover, the absence of doping increases the carrier mobility due to lack of Coulomb scattering and reduces the effects of random dopant fluctuation. Thus FinFETs devices offer the potential for maintaining the scalability of the CMOS technology as it approaches the “end of the road-map” phase of its development [25].

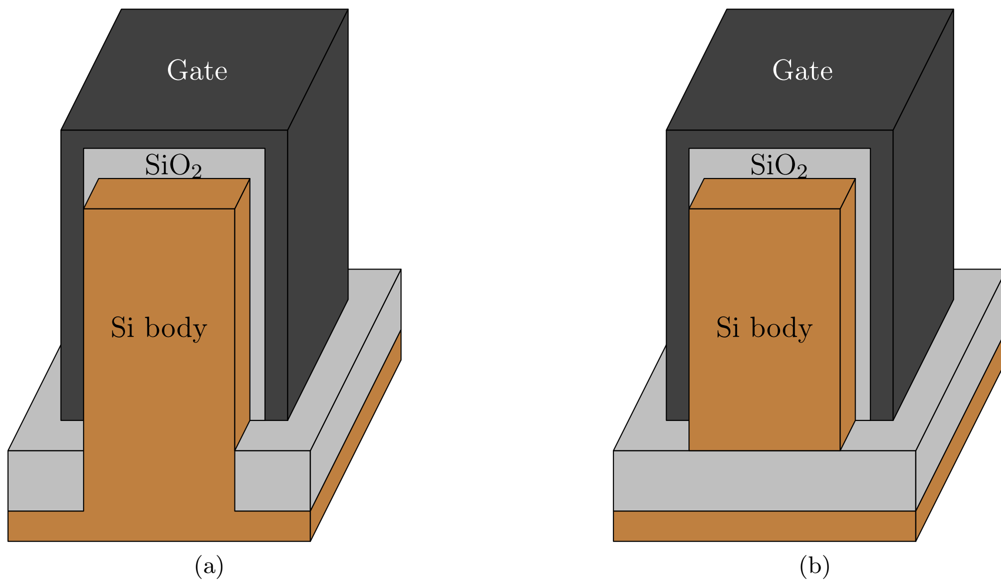


Figure 1.1: Structure of (a) bulk FinFET and (b) SOI FinFET.

Depending upon the substrate type, FinFETs can be classified broadly as a bulk (cf. Fig. 1.1a) or SOI type (cf. Fig. 1.1b). Both types of FinFETs have merits associated with their structure. Some of the advantages of bulk FinFETs are process compatibility with planar CMOS and reduced self-heating, whereas the SOI FinFETs benefit from lower junction capacitances. Apart from these merits the choice of particular structure is decided by the fabrication cost and ease of integrating in the present technology setup. Typically, the body thickness is small compared to its height thus the two side gates have a prominent effect in controlling the channel inversion level as compared to the top gate. Also the top gate influence on the channel reduces when its gate oxide is thicker than the side gate oxide. Since the FinFET is controlled by two side gates it is generally called a double-gate (DG) FinFET. Nevertheless, when the body thickness and top gate oxide are comparable to its height and side gate oxide, respectively, the presence of the top gate cannot be neglected. Such a device is called a tri-gate (TG) FinFET [31].

It can be noted that when the top gate is removed the result is a FinFET with two independent-gate as shown in Fig. 1.2a. Both gates can be tied together to form a common-gate DG-FinFET or can be separated to form an independent-gate DG-FinFET. Structurally, DG-FinFETs can be symmetric or asymmetric. DG-FinFETs with identical parameters (e.g., oxide thickness and gate work-function) for both gates are symmetric otherwise they are called asymmetric. A planar independent-gate asymmetric DG-FinFET is shown in Fig. 1.2b where a thin Si channel is locally isolated from the bulk-Si substrate by a thin buried dielectric layer. The structure resembles an SOI MOSFET with a extremely thin body [32] and relatively thin gate oxide and is called an extremely thin SOI (ETSOI) or ultra-thin body SOI (UTB-SOI). This structure combines the best features of the classical MOSFET (low parasitic source/drain contact resistance) with the best features of SOI technology (improved electrostatic integrity); however, it poses technological difficulty in aligning the bottom gate with the top gate.

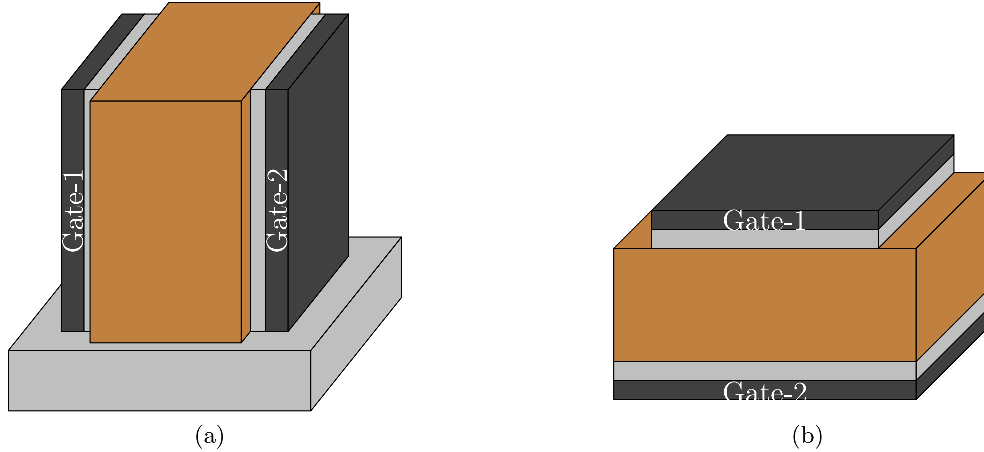


Figure 1.2: Independent double-gate (a) FinFET on SOI and (b) ETSOI.

The control of threshold voltage in the planar MOSFETs was achieved by adjusting the doping concentration in the channel which was useful to build devices with multiple threshold voltages on the same die. The multiple V_{th} capability is important to have low power (high V_{th}) and high performance (low V_{th}) devices on the same die. As FinFETs are typically low-doped devices alternate V_{th} control techniques that have been proposed are the use of asymmetric gate work-function where two gates have different work-function, and use of symmetric mid-gap work-function gate-electrodes. Since the two gate electrodes in the independent-gate DG-FinFET are electrically isolated they provide independent biasing of the two gates and enable dynamic control of threshold voltage V_{th} where one gate is used as a drive gate and other gate as a V_{th} control gate [33, 34]. The performance of an optimally designed asymmetric DG-FinFET is found to be superior to that of its symmetric counterpart [35]. Furthermore, novel circuit applications involving independent-gate asymmetric DG-FinFET for analog [36, 37] and digital [38, 39] applications have been demonstrated.

Apart from the double-gate FinFET various other flavors of the multi-gate MOSFET have been proposed. Fig. 1.3 shows the cross-section of π-gate, Ω-gate, quad-gate and surrounding gate MOSFET.

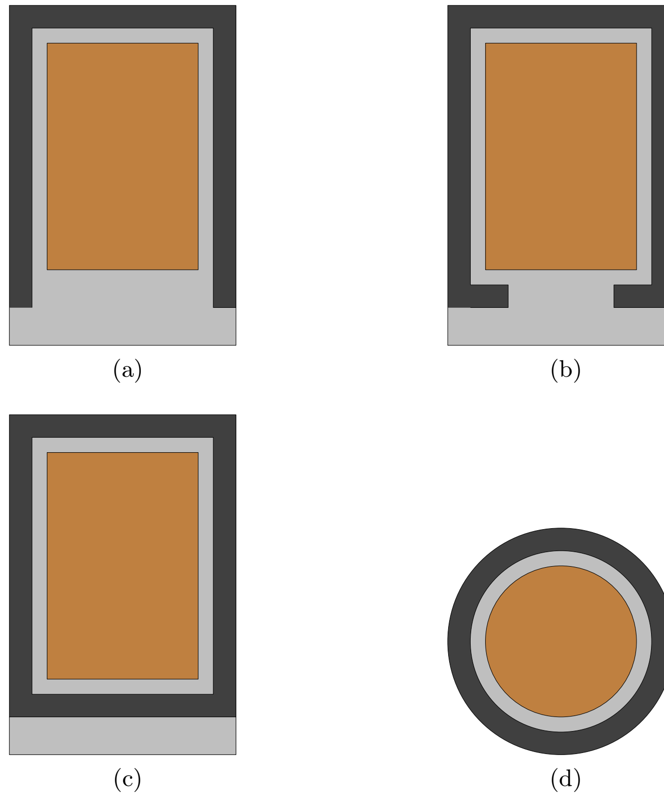


Figure 1.3: Cross-section of various flavors of multi-gate MOSFETs (a) π-gate , (b) Ω-gate, (c) quad-gate and (d) surrounding-gate.

1.3 Compact Modeling

Circuit design with new devices requires the development of compact models. Compact models are a concise mathematical description of the transistor terminal characteristics in closed form. A compact model maintains a balance between the amount of physics captured for model accuracy and amount of approximation made for model simplicity [40, 41, 42]. Compact models provide a bridge between circuit designers and chip manufacturers. Traditionally, compact models of MOSFETs were threshold voltage based where carrier transport via "drift" and "diffusion" were modeled separately and then stitched together by smoothing functions to maintain continuity. Example of such models are BSIM3v3, BSIM4, and MM9. Although inversion charge-based models are powerful alternatives of threshold-based models they have

their own limitations such as modeling in the accumulation region where there is no inversion charge.

Recently, surface-potential-based compact models like PSP have attracted significant attention because of their better physical description of the device characteristics. Apart from accuracy, complexity, and physical framework (threshold voltage, inversion charge, or surface potential based) the typical compact model may differ by inclusion of second order effects and parasitics, physical (charge conservation, symmetry, reciprocity) and mathematical (continuity) consistency, simulation speed and memory usage, availability in EDA design tools, and documentation [40, 43].

Due to the advantages offered by multi-gate transistors there is presently considerable interest in developing compact models in order to assess the impact of multi-gate transistors on circuit performance. Guided by the development of compact models of the bulk [44, 45, 46, 47, 48, 49, 50, 51, 52] and SOI [53, 54, 55] MOSFET one may expect that a compact model of multi-gate transistors will consist of an essentially physical core model of an ideal long-channel transistor to which small-geometry effects [56, 57] and quantum corrections [58, 59] are added using suitably chosen approximations.

Various inversion charge- and surface-potential-based compact models of double-gate FinFETs have been developed. The compact model of FinFETs developed in this work is based on the same principles as the PSP models of conventional planar bulk and SOI MOSFETs. The structural similarity to PSP means that various small-geometry effects can be introduced in a similar manner.

1.4 Organization of the Dissertation

This dissertation is organized as follows. In Chapter 2 we present TCAD simulations illustrating the differences in C-V characteristics between bulk and SOI FinFETs. The rigorous input voltage equation (IVE) in terms of the elliptic integrals is for-

mulated for the common-gate symmetric DG-FinFET and replaced by an accurate approximation suitable for compact modeling applications which takes into account both electron and hole contributions to the charge density. An accurate approximate solution for solving the IVE that does not require an iterative loop is developed.

The IVE for independent-gate asymmetric DG-FinFETs is developed in Chapter 3 with an explicit expression for the boundary between trigonometric and hyperbolic forms of the IVE. However, the IVE for this case is unipolar and valid from weak to strong inversion. An efficient numerical technique for solving the unipolar IVE is proposed.

In Chapter 4 a drain current expression for common-gate symmetric DG-FinFETs in [60] is reformulated in the PSP form. A symmetric linearization method free from the charge-sheet approximation is developed for common-gate DG-FinFETs and SGFETs and is used to derive an accurate terminal charge model.

In Chapter 5 the symmetric linearization method is extended to independent-gate asymmetric DG-FinFETs by defining the concept of effective charge density. The new model is implemented in Verilog-A following the style of the PSP model [45] and circuit simulations are performed to verify its convergence robustness and demonstrate its capabilities to model novel FinFET circuits.

The summary and conclusions of this dissertation are presented in the last chapter.

1.5 Summary of the Original Results Obtained in this Work

In this work compact models for the common-gate symmetric DG-FinFET, SGFET, and independent-gate asymmetric DG-FinFET are developed. Original results obtained in this work are:

- Development of an ambipolar IVE for common-gate symmetric DG-FinFETs which includes the contribution of both types of carriers (electrons and holes)

to charge density and is valid for all regions of operation (from accumulation to inversion).

- An accurate closed-form algorithm for solving the ambipolar IVE of common-gate symmetric DG-FinFETs and proof that the previously known unipolar approximation of the IVE can be derived as a special case of the more general ambipolar IVE.

- The symmetric linearization method is developed for common-gate symmetric DG-FinFETs and SGFETs in a form free of the charge-sheet approximation present in its original formulation for bulk MOSFETs.

- An alternative and computationally efficient description of the boundary between the trigonometric and the hyperbolic solutions of the Poisson-Boltzmann equation for the independent-gate asymmetric DG-FinFET is developed.

- Efficient numerical solution of the independent-gate asymmetric DG-FinFET IVE suitable for circuit simulator implementation is proposed.

- The symmetric linearization method is generalized and extended to the independent gate asymmetric DG-FinFET and an accurate terminal charge model for that device is derived.

- The core model structure for FinFETs is maintained similar to that of PSP for planar MOSFETs.

- The compact models are implemented in commercial circuit simulators through Verilog-A and simulations were performed to verify good model convergence.

1.6 List of Publications Related to this Work

The publications that resulted from this work are given below. The text of this dissertation, in part, is a reprint of the material as it appears in following list of publications. The dissertation author was the primary investigator and author of these publications.

(i) G. Dessai, and G. Gildenblat, “Approximate Closed-Form Solution of Ambipolar Input Voltage Equation for the Common-Gate Symmetric FinFET,” Solid-State Electron., vol. 75, no. 9, pp. 77–80, 2012.

(ii) G. Dessai, and G. Gildenblat, “Inclusion of Accumulation Region in the Compact Models of Bulk and SOI FinFETs,” IEEE Trans. Electron Dev., vol. 58, no. 8, pp. 2644–2651, 2011.

(iii) G. Dessai, W. Wu, B. Bakkaloglu, C. C. McAndrew and G. Gildenblat, “Compact Model and Circuit Simulations for Asymmetric Independent Gate FinFETs,” J. Comput. Electron., vol. 9, pp. 103–107, 2010.

(iv) G. Dessai, W. Wu, and G. Gildenblat, “Compact Charge Model for Independent-Gate Asymmetric DGFET,” IEEE Trans. Electron Dev., vol. 57, no. 9, pp. 2106–2115, 2010.

(v) G. Dessai and G. Gildenblat, “Solution Space for the Independent-Gate Asymmetric DGFET,” Solid-State Electron., vol. 54, no. 3, pp. 382–384, 2010.

(vi) G. Dessai, A. Dey, G. Gildenblat, and G. D. J. Smit, “Symmetric Linearization Method for Double-Gate and Surrounding-Gate MOSFET models,” Solid-State Electron., vol. 53, no. 5, pp. 548–556, 2009.

Chapter 2

ELECTROSTATICS of the COMMON-GATE SYMMETRIC DG-FinFET

2.1 Introduction

In surface potential based compact models such as PSP the drain current and the terminal charges are expressed as explicit functions of the surface potentials at the source and drain ends of the channel. The surface potential is obtained by solving an IVE which is an implicit relation between the surface potential, the gate voltage and the imref splitting. Thus the IVE forms an essential part of any surface potential based compact MOSFET model. The IVE is derived from the integration of the one dimensional Poisson-Boltzmann equation. Generally, the resulting IVE is an implicit function of the surface potential and has to be solved iteratively. In PSP an efficient explicit algorithm is proposed for solving the IVE [61]. Sometimes the IVE is reformulated in terms of a variable on which the surface potential has explicit dependence [62].

In this chapter the Poisson-Boltzmann equation is formulated for the DG-FinFET and the IVE is derived for the common-gate symmetric structure subject to appropriate boundary conditions. An explicit algorithm for solving the IVE of the common-gate symmetric DG-FinFET is formulated.

Most often compact models of FinFETs are developed by including the contribution of only one type of charge carrier to the charge density while integrating the Poisson-Boltzmann equation. This is the unipolar approximation. The inclusion of both type of carriers results in an IVE involving special functions which are undesirable for compact modeling as they are not available in Verilog-A and their implementation is computationally complex. Although the unipolar approximation is sufficient in many cases it is not universal and, for example, does not allow one to reproduce the difference in C-V curves between bulk and SOI FinFETs [63]. It also does not lead to a FinFET model valid in all regions of operation. Hence it is desirable to develop a compact FinFET model that includes ambipolar effects

(contribution of both holes and electrons to the charge density) based on a suitably modified IVE which does not involve special functions.

For the common-gate symmetric FinFET the IVE accounting for ambipolar effects can be formulated in terms of elliptic integrals [64]. This formulation is physical and complete but is difficult to use for compact modeling. Hence in [63] we have presented an approximate IVE which is well conditioned and numerically equivalent to that in [64] but does not include elliptic integrals or other quadratures. The transcendental IVE in [63] was solved iteratively and implemented in a circuit simulator to demonstrate the validity of the approach for compact modeling.

Additionally, we developed and verified an accurate approximate solution that does not require an iterative loop [65]. Our approach is influenced by that in [62] which in turn includes some ideas from the earlier work dealing with the surface potential equation for a traditional bulk MOSFET [61]. In particular, we will show that the results in [62] can be recovered as a special case of this work corresponding to the unipolar approximation.

2.2 TCAD simulations of bulk and SOI FinFETs

In this section we present TCAD simulations illustrating the differences in C-V characteristics between bulk and SOI FinFETs. The simplified structures of bulk and SOI FinFETs are shown in Figs. 2.1a and 2.1b, respectively. The gate contact is metal with a mid-gap work function and the substrate of the bulk FinFET is p-type with doping concentration of 5×10^{15} cm^{-3}. The source and drain are heavily doped n-type and the body is intrinsic. The bulk contact is placed at the bottom of the device.

Small signal a.c. simulations were performed around the d.c. bias point with 100 Hz signal frequency in order to investigate the low-frequency behavior. The source, drain, and the bulk terminals are connected together as shown in the inset of Fig. 2.2a. The gate voltage V_{gs} is swept from -1.5 to 1.5 V. The simulated ca-

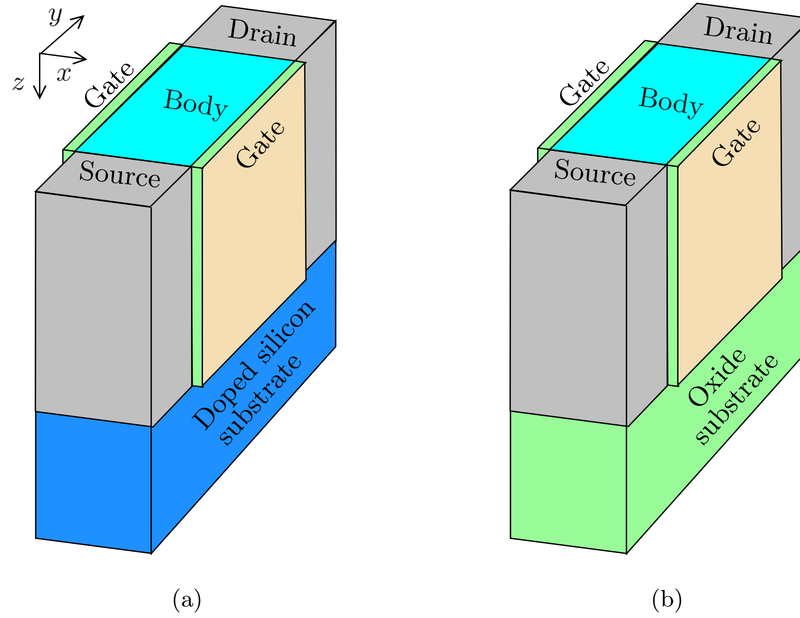
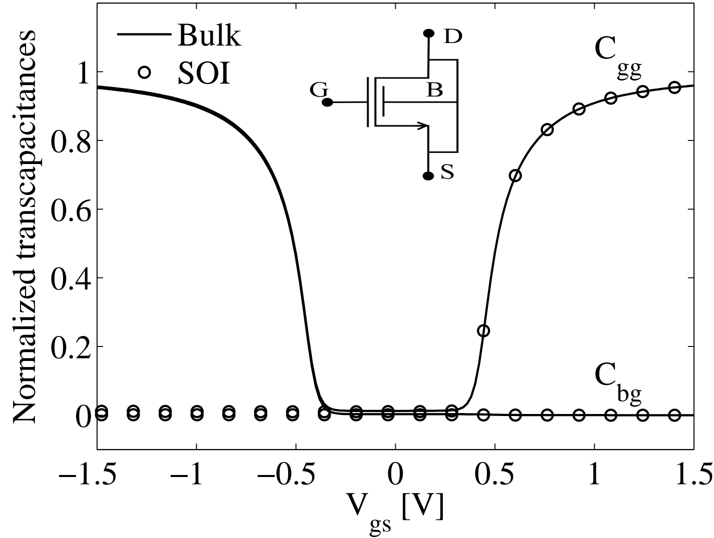


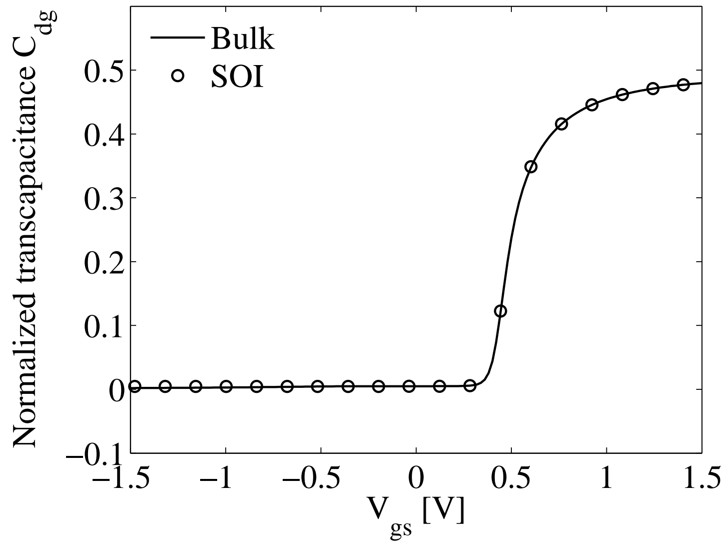
Figure 2.1: Simulated device structures (a) bulk FinFET and (b) SOI FinFET.

pacitances C_{gg}, C_{bg} and C_{dg} for bulk and SOI FinFETs are shown in Fig. 2.2. In the inversion region, electrons are provided by the source and the drain contacts for bulk and SOI FinFETs and similar capacitance characteristics are obtained for both FinFET structures. However, in the accumulation region of the bulk FinFET, holes are supplied by the substrate through the bulk contact, whereas such a supply of holes is absent in the SOI FinFET. These holes need to be supplied from the thermal generation process and through the source/drain contacts where their concentration is extremely low. Even at a frequency as low as 100 Hz such processes fall short of establishing the quasi-equilibrium concentration of holes resulting in negligible capacitance C_{gg} and C_{bg}. Thus in agreement with TCAD simulations the accumulation capacitance for the SOI FinFET can be assumed to be negligible for all practical purposes.

SPICE-like circuit simulators evaluate capacitances as derivatives of the terminal charges with respect to the terminal biases. In surface-potential-based compact models for bulk and SOI MOSFETs, the terminal charges are expressed as functions



(a)



(b)

Figure 2.2: TCAD simulated normalized transcapacitances (a) C_{gg}, C_{bg} and (b) C_{dg} for bulk and SOI FinFETs with source, drain, and bulk connected.

of surface potentials at the source and the drain ends of the channel [45, 66]. The surface potential is obtained by solving the IVE derived from the Poisson-Boltzmann equation. A similar approach is followed in surface-potential-based compact models of the DG-FinFET [67, 68] which is valid from weak to strong inversion regions of

operation. To extend the validity of these models to the accumulation region, an accurate IVE derived by considering both electron and hole contributions to the charge density is needed. The TCAD result shown in Fig. 2.2 clearly illustrate the difference in C-V characteristics of the two FinFET structures and need to be reproduced by a compact model.

2.3 Poisson-Boltzmann Equation for DG-FinFET

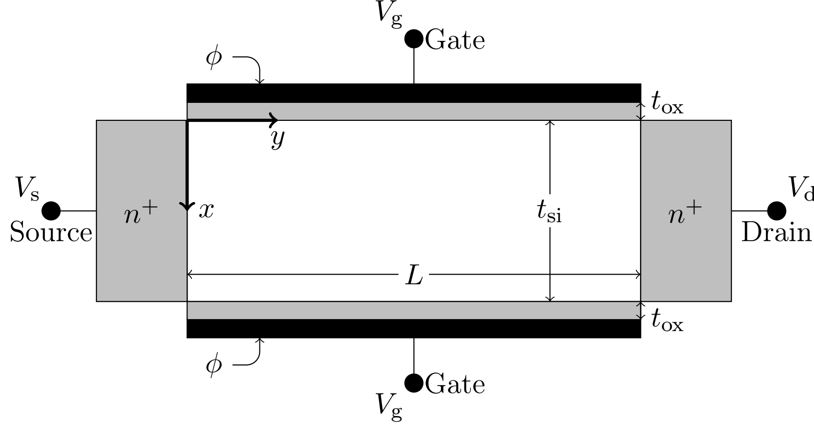


Figure 2.3: Cross-section of the common-gate symmetric DG-FinFET. ϕ is the work-function of gate material.

To understand the electrostatics of DG-FinFETs one needs to solve the Poisson-Boltzmann equation within the device subject to the boundary conditions. Fig. 2.3 shows the cross-section of a common-gate symmetric DG-FinFET. The gradual channel approximation (used universally for the development of compact models for MOSFETs) helps to write the Poisson-Boltzmann equation in one-dimension as

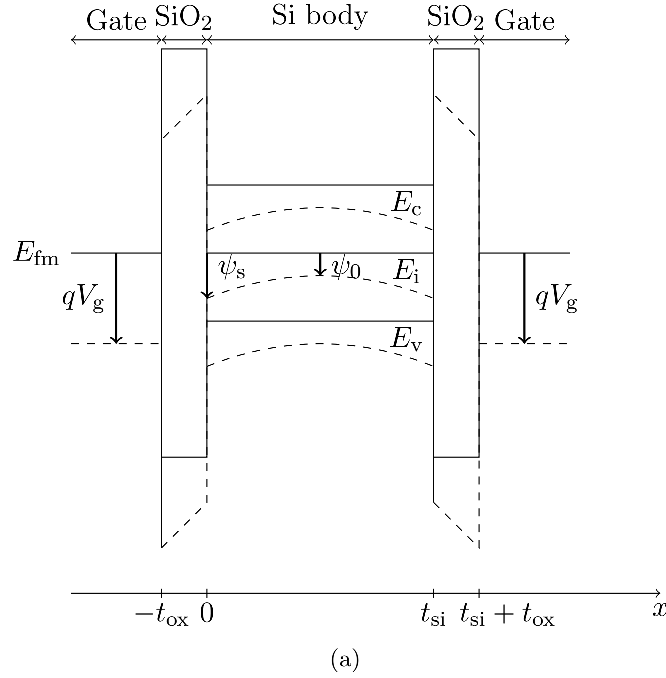
$$\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} = -\frac{\rho}{\epsilon_{\mathrm{si}}} \tag{2.1}$$

where

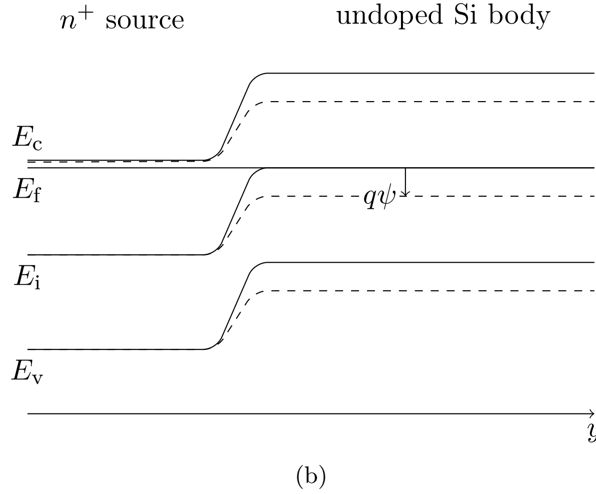
$$\rho = q(p - n) \tag{2.2}$$

is the total charge density for an undoped body,

$$n = n_{\mathrm{i}} \exp\left(\frac{\psi - V_{\mathrm{c}}}{\phi_{\mathrm{t}}}\right) \tag{2.3}$$



(a)



(b)

Figure 2.4: Energy band diagram (a) across the channel ($V_\mathrm{d} = V_\mathrm{s} = 0$) and (b) along the channel indicating the reference energy level for measuring electrostatic potential ψ. Solid lines corresponds to $\psi = 0$ whereas dashed lines corresponds $\psi > 0$. E_fm is the gate Fermi level.

is the electron concentration,

$$p = p_\mathrm{i} \exp\left(-\frac{\psi}{\phi_\mathrm{t}}\right) \tag{2.4}$$

is the hole concentration, x is the direction across the channel, ψ is the electrostatic potential (cf. Fig. 2.4), $V_\mathrm{c} \equiv (F_\mathrm{n} - F_\mathrm{p})/q$ is the electron and hole imref splitting with value V_s at the source and value V_d at the drain, ϵ_si is the permittivity of the silicon, ϕ_t is the thermal voltage, n_i is the intrinsic electron concentration and p_i is the intrinsic hole concentration. Note that $p_\mathrm{i} = n_\mathrm{i}$ and the body is assumed to be undoped. The reference level for ψ is selected as in [69] to facilitate the recovery of the theory in [69] as special case of the present work. In writing (2.4) which is the hole contribution to the charge density, the holes are assumed to be in quasi-equilibrium. This assumption is valid for FinFETs with n^+ source/drain contacts which act as sources and sinks only for electrons [64]. Substituting (2.2)-(2.4) in (2.1) and using fact that $n_\mathrm{i} = p_\mathrm{i}$ yields

$$\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} = \frac{q}{\epsilon_\mathrm{si}}\left[n_\mathrm{i}\exp\left(\frac{\psi - V_\mathrm{c}}{\phi_\mathrm{t}}\right) - n_\mathrm{i}\exp\left(-\frac{\psi}{\phi_\mathrm{t}}\right)\right] \tag{2.5}$$

or equivalently,

$$\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} = \frac{\phi_\mathrm{t} \cdot e^{\frac{-V_\mathrm{c}}{2\phi_\mathrm{t}}}}{L_\mathrm{di}^2} \cdot \sinh\left(\frac{\psi - V_\mathrm{c}/2}{\phi_\mathrm{t}}\right) \tag{2.6}$$

where the intrinsic Debye length [70] is

$$L_\mathrm{di} = \sqrt{\frac{\epsilon_\mathrm{si}\phi_\mathrm{t}}{2qn_\mathrm{i}}}. \tag{2.7}$$

Normalizing ψ and x we have

$$\frac{\mathrm{d}^2\varphi}{\mathrm{d}\xi^2} = \sinh(\varphi) \tag{2.8}$$

where

$$\varphi = \frac{\psi - V_\mathrm{c}/2}{\phi_\mathrm{t}}, \tag{2.9}$$

and

$$\xi = \frac{xe^{-\frac{V_\mathrm{c}}{4\phi_\mathrm{t}}}}{L_\mathrm{di}}. \tag{2.10}$$

2.4 Common-Gate Symmetric DG-FinFET

From the mathematical point of view the essential difference between a common-gate symmetric DG-FinFET and a bulk MOSFET is that in the latter case the boundary

conditions

$$\lim_{x\to\infty} \psi(x) = 0 \tag{2.11}$$

and

$$\lim_{x\to\infty} \frac{\partial\psi}{\partial x} = 0 \tag{2.12}$$

allow one to obtain an IVE directly from the first integral of the Poisson-Boltzmann equation. For common-gate symmetric DG-FinFETs (2.11) does not apply and even though (2.12) takes an equally simple form of (cf. 2.3)

$$\left.\frac{\partial\psi}{\partial x}\right|_{x=t_{\mathrm{si}}/2} = 0 \tag{2.13}$$

it is impossible to arrive at the IVE from the first integral. In other words, in the DG-FinFET there is no point where the values of ψ and $\partial\psi/\partial x$ are known a priori. This necessitates the derivation of the IVE based on the second integral of the Poisson-Boltzmann equation which, even in the case of undoped symmetric DG-FinFETs, is formulated in terms of incomplete elliptic integrals and is not directly suitable for the purpose of the compact modeling. Only if the unipolar approximation is made can the IVE be rigorously reduced to the familiar form [69] almost universally used in compact models of undoped DG-FinFETs. Our approach is to develop an accurate simplified form for the IVE which does not involve elliptic integrals and can be solved numerically within a compact model. This is accomplished in two steps. In section 2.5 we reformulate the rigorous IVE using an approach developed earlier in electrochemistry [71, 72] which is more suitable for our purpose than the equivalent form recently rediscovered in [64] and which has also appeared earlier in the work on electrocapillary slits [73]. The normalized form of the Poisson-Boltzmann equation is the same in [71, 72, 64, 73]. Thus the developed rigorous IVE (including the contributions of both electrons and holes) is simplified in the next section.

For further references we note that flatband condition at a point y along the channel corresponds to $\psi = \psi_{\mathrm{s}} = V_{\mathrm{c}}/2$ where ψ_{s} is the surface potential. This implies that for $V_{\mathrm{d}} > V_{\mathrm{s}}$ we may have flat bands only for one but not for all planes

$y = const.$ We note in passing that the flatband condition can be included in the model formulation only if both kinds of carriers are considered. For a fixed y we have a potential minimum at the center of the channel if $\psi > V_c/2$ and a potential maximum if $\psi < V_c/2$. In terms of the gate bias the flatband condition corresponds to $V_{gs} = \Delta\phi + V_c/2$ since the oxide field $(V_{gs} - \Delta\phi - \psi_s)/t_{ox} = 0$ where at flatband $\psi_s = V_c/2$. Here V_{gs} is gate to source bias and $\Delta\phi$ is the workfunction difference between gate material and body. At a given plane $y = const.$ we have a potential minimum for $V_{gs} > \Delta\phi + V_c/2$ and a maximum $V_{gs} < \Delta\phi + V_c/2$.

2.5 Exact IVE for Common-Gate Symmetric DG-FinFET

By integrating (2.8) and using the boundary condition $\varphi|_{x=t_{si}/2} = \varphi_0$ we have

$$\left(\frac{\mathrm{d}\varphi}{\mathrm{d}\xi}\right)^2 = 2 \cdot (\cosh\varphi - \cosh\varphi_0) \tag{2.14}$$

where

$$\varphi_0 = \frac{\psi_0 - V_c/2}{\phi_t} \tag{2.15}$$

and ψ_0 is the electrostatic potential for $x = t_{si}/2$ (in the middle of the body). In terms of φ_0, the flatband condition for a plane $y = const.$ corresponds to $\varphi_0 = 0$, a potential minimum to $\varphi_0 > 0$ and maximum to $\varphi_0 < 0$. Thus denoting

$$\eta = \mathrm{sgn}(\varphi_0) = \mathrm{sgn}\left(V_{gs} - \Delta\phi - \frac{V_c}{2}\right) \tag{2.16}$$

we have

$$\mathrm{sgn}\left(\frac{\mathrm{d}\varphi}{\mathrm{d}\xi}\right) = \eta \cdot \mathrm{sgn}(\xi - \xi_0), \tag{2.17}$$

where sgn() is the sign function and

$$\xi_0 = \left(\frac{t_{si}}{2 \cdot L_{di}}\right) \cdot \exp\left(-\frac{V_c}{4\phi_t}\right) \tag{2.18}$$

corresponds to ξ at $x = t_{si}/2$. From (2.14) and (2.17)

$$\frac{\mathrm{d}\varphi}{\mathrm{d}\xi} = \eta \cdot \mathrm{sgn}(\xi - \xi_0)\sqrt{2 \cdot \cosh\varphi - 2 \cdot \cosh\varphi_0}. \tag{2.19}$$

From the continuity of the x-component of the displacement vector at $x = 0$

$$\left.\frac{\mathrm{d}\varphi}{\mathrm{d}\xi}\right|_{\xi=0} = -\frac{L_{\mathrm{di}} e^{\frac{V_{\mathrm{c}}}{4\phi_{\mathrm{t}}}}}{r_{\mathrm{c}} t_{\mathrm{si}} \phi_{\mathrm{t}}} \left(V_{\mathrm{gs}} - \Delta\phi - \frac{V_{\mathrm{c}}}{2} - \phi_{\mathrm{t}} \varphi_{s} \right) \tag{2.20}$$

where $r_{\mathrm{c}} = C_{\mathrm{si}}/C_{\mathrm{ox}}$, $C_{\mathrm{si}} = \epsilon_{\mathrm{si}}/t_{\mathrm{si}}$, $C_{\mathrm{ox}} = \epsilon_{\mathrm{ox}}/t_{\mathrm{ox}}$ and

$$\varphi_{\mathrm{s}} = \frac{\psi_{\mathrm{s}} - V_{\mathrm{c}}/2}{\phi_{\mathrm{t}}}. \tag{2.21}$$

From (2.19) and (2.20)

$$\frac{\eta L_{\mathrm{di}} e^{\frac{V_{\mathrm{c}}}{4 \cdot \phi_{\mathrm{t}}}}}{\sqrt{2} \cdot r_{\mathrm{c}} t_{\mathrm{si}} \phi_{\mathrm{t}}} \left(V_{\mathrm{gs}} - \Delta\phi - \frac{V_{\mathrm{c}}}{2} - \phi_{\mathrm{t}} \varphi_{\mathrm{s}} \right) - \sqrt{\cosh \varphi_{\mathrm{s}} - \cosh \varphi_{0}} = 0. \tag{2.22}$$

To obtain an IVE we need another equation relating φ_0 and φ_{s}. Integrating (2.19),

$$\int_{\varphi_0}^{\varphi} \frac{\mathrm{d}\varphi'}{\sqrt{2 \cdot \cosh \varphi' - 2 \cdot \cosh \varphi_0}} = \eta \cdot |\xi - \xi_0|. \tag{2.23}$$

The integral in (2.23) is an elliptic integral of the first kind and can be written in several equivalent forms [71, 73, 72, 64]. In what follows we use the complete

$$K(k) = \int_0^{\pi/2} \frac{\mathrm{d}\theta}{\sqrt{1 - k^2 \sin^2 \theta}}; \quad 0 \le k \le 1 \tag{2.24}$$

and incomplete

$$F(t,k) = \int_0^{t} \frac{\mathrm{d}\theta}{\sqrt{1 - k^2 \sin^2 \theta}}; \quad 0 \le k \le 1 \text{ and } 0 \le t < \pi/2 \tag{2.25}$$

elliptic integrals of the first kind in Legendre's form [74]. Then as shown in Appendix A (2.23) is equivalent to

$$F\left[\sin^{-1} \left(e^{\frac{\eta(\varphi_0 - \varphi)}{2}} \right), e^{-\eta\varphi_0} \right] - K\left(e^{-\eta\varphi_0} \right) = \frac{-e^{\frac{\eta\varphi_0}{2}} |\xi - \xi_0|}{2}. \tag{2.26}$$

Setting $\xi = 0$ and $\varphi = \varphi_{\mathrm{s}}$ yields the desired form of the IVE including the contributions of both electrons and holes:

$$F\left\{ \sin^{-1} \left[e^{\frac{\eta(\varphi_0 - \varphi_{\mathrm{s}})}{2}} \right], e^{-\eta\varphi_0} \right\} - K\left(e^{-\eta\varphi_0} \right) = -\frac{t_{\mathrm{si}} e^{\left(\frac{\eta\varphi_0}{2} - \frac{V_{\mathrm{c}}}{4 \cdot \phi_{\mathrm{t}}} \right)}}{4 \cdot L_{\mathrm{di}}}, \tag{2.27}$$

where φ_0 as a function of φ_s is given by (2.22). In the Appendix B we show that this form of the IVE is mathematically equivalent to the formulation in [64]. The reason for choosing (2.27) as a starting point in this work is that from (2.27) Taur's unipolar approximation [69] appears naturally. To see this set $\eta = 1$ and $e^{-\eta\varphi_0} \approx 0$ for $\varphi_0 \gtrsim 5$ and note that by (2.24), (2.25) $K(0) = \pi/2$ and $F(t, 0) = t$. Then (2.27) becomes

$$\sin^{-1}\left(e^{\frac{\varphi_0 - \varphi_\mathrm{s}}{2}}\right) - \frac{\pi}{2} = -\frac{t_\mathrm{si} e^{\left(\frac{\varphi_0}{2} - \frac{V_\mathrm{c}}{4 \cdot \phi_\mathrm{t}}\right)}}{4 \cdot L_\mathrm{di}} \tag{2.28}$$

Rearranging (2.28),

$$\varphi_\mathrm{s} = \varphi_0 + 2 \cdot \ln\left\{\sec\left[\frac{t_\mathrm{si}}{4 \cdot L_\mathrm{di}} \exp\left(\frac{\varphi_0}{2} - \frac{V_\mathrm{c}}{4 \cdot \phi_\mathrm{t}}\right)\right]\right\} \tag{2.29}$$

or, equivalently,

$$\psi_\mathrm{s} = \psi_0 + 2 \cdot \phi_\mathrm{t} \ln\left\{\sec\left[\frac{t_\mathrm{si}}{4 \cdot L_\mathrm{di}} \exp\left(\frac{\psi_0 - V_\mathrm{c}}{2 \cdot \phi_\mathrm{t}}\right)\right]\right\}, \tag{2.30}$$

which is precisely the IVE in the form obtained in [69] by retaining the contribution of electrons and neglecting the contribution of holes to the space charge density. Similarly, for $\varphi_0 \lesssim -5$ (2.27) can be reduced to

$$\varphi_\mathrm{s} = \varphi_0 - 2 \cdot \ln\left\{\sec\left[\frac{t_\mathrm{si}}{4 \cdot L_\mathrm{di}} \exp\left(-\frac{\varphi_0}{2} - \frac{V_\mathrm{c}}{4 \cdot \phi_\mathrm{t}}\right)\right]\right\} \tag{2.31}$$

or, equivalently,

$$\psi_\mathrm{s} = \psi_0 - 2 \cdot \phi_\mathrm{t} \ln\left\{\sec\left[\frac{t_\mathrm{si}}{4 \cdot L_\mathrm{di}} \exp\left(-\frac{\psi_0}{2 \cdot \phi_\mathrm{t}}\right)\right]\right\}, \tag{2.32}$$

which is an approximation that can be also obtained directly from (2.5) by retaining the contribution of holes and neglecting the contribution of electrons to the space charge density. Note that in the presence of n^+ source/drain contacts the hole imref is approximately constant throughout the device so the imref splitting V_c does not enter (2.32). In weak inversion or weak accumulation the difference between ψ_s or ψ_0 [i.e. the last term in (2.30) and (2.32)] is much less than ϕ_t which means that in the condition of validity of the unipolar approximation ψ_0 can be replaced by ψ_s.

2.6 Approximate Input Voltage Equation

For φ close to φ_0 (near the flat-band) it is possible to obtain φ_{s} as a function of φ_0 in a closed form including contribution to the space charge of both electrons and holes. Using a second order Taylor expansion

$$\cosh\varphi = \cosh\varphi_0 + (\varphi-\varphi_0)\sinh\varphi_0 + \frac{1}{2}(\varphi-\varphi_0)^2\cosh\varphi_0 + \cdots \tag{2.33}$$

in (2.23) yields

$$\int\limits_{\varphi_0}^{\varphi} \frac{\mathrm{d}\varphi'}{\sqrt{2\cdot\tanh\varphi_0\cdot(\varphi'-\varphi_0)+(\varphi'-\varphi_0)^2}} = \eta|\xi-\xi_0|\cosh^{\frac{1}{2}}\varphi_0. \tag{2.34}$$

Integrating and using the boundary condition $\varphi = \varphi_{\mathrm{s}}$ at $\xi = 0$ we find

$$\varphi_{\mathrm{s}} = \varphi_0 + 2\cdot\tanh\varphi_0\cdot\sinh^2 a \tag{2.35}$$

where

$$a = \frac{t_{\mathrm{si}} e^{\frac{-V_{\mathrm{c}}}{4\cdot\phi_{\mathrm{t}}}}\sqrt{\cosh\varphi_0}}{4\cdot L_{\mathrm{di}}}. \tag{2.36}$$

At this point we have the unipolar approximation (2.29) for $\varphi_0 \gtrsim 5$, the unipolar approximation (2.31) for $\varphi_0 \lesssim 5$ and bipolar approximation (2.35) near flatband. The next step is to develop a C^{∞} class approximation to the rigorous IVE (2.27) which has (2.29), (2.31) and (2.35) as proper limiting cases. This is done as follows. First we note that

$$\sinh^2 a = \ln\left[\sec\left(\sqrt{2}\cdot a\right)\right] - \frac{2\cdot a^6}{15} + \cdots \tag{2.37}$$

The $a(\varphi_0)$ dependence near flatband, for $|\varphi_0| \lesssim 5$, is shown in Fig. 2.5 for two values of V_{c}. While a can be of the order of 10^{-3}, the sixth order term in (2.37) is of the order 10^{-18} and is totally inconsequential. Hence for $|\varphi_0| \lesssim 5$ the relation between φ_{s} and φ_0 (2.35) is numerically indistinguishable from

$$\varphi_{\mathrm{s}} = \varphi_0 + 2\cdot\tanh\varphi_0\cdot\ln\left[\sec\left(\sqrt{2}\cdot a\right)\right] \tag{2.38}$$

in which we have approximated $\sinh^2 a$ by the first term in (2.37). From Fig. 2.5 it can also be seen that for higher $V_{\rm c}$ the value of a is further reduced which increases the accuracy of approximation made in (2.38). The advantage of switching from (2.35) to (2.38) is that (2.38) contains not only (2.35) but also (2.29) and (2.31) as its proper limits. For example if $\varphi_0 > 5$ and from (2.36)

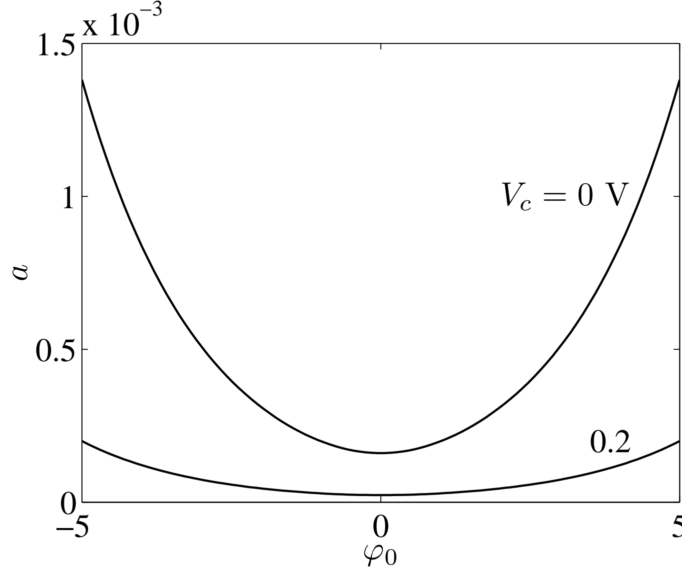


Figure 2.5: $a(\varphi_0)$ dependence; $t_{\rm si} = 20$ nm, $T = 300$ K.

$$\sqrt{2} \cdot a \approx \frac{t_{\rm si}}{4 \cdot L_{\rm di}} \exp\left(\frac{\varphi_0}{2} - \frac{V_{\rm c}}{4 \cdot \phi_t}\right), \tag{2.39}$$

then (2.29) is recovered from (2.38) once we note that in this range $\tanh \varphi_0 \approx 1$. Similarly, for $\varphi_0 < -5$ and from (2.36)

$$\sqrt{2} \cdot a \approx \frac{t_{\rm si}}{4 \cdot L_{\rm di}} \exp\left(-\frac{\varphi_0}{2} - \frac{V_{\rm c}}{4 \cdot \phi_t}\right). \tag{2.40}$$

Since this time $\tanh \varphi_0 \approx -1$ we obtain (2.31). We stress that while (2.35) is a step towards a unified bipolar approximation to the exact IVE (2.27), neither (2.35) nor (2.29) or (2.31) are used in the model formulation. In what follows we work directly with (2.38) which covers all regions of operation and obviates the need for regional approximations.

It remains to check the accuracy of (2.38) in terms of the surface potential and its derivatives. The new IVE is solved numerically using the Newton-Raphson method. The results presented in Figs. 2.6, 2.7 (and several other extensive computations) show that (2.38) is an extremely accurate approximate form of (2.27) and contains the same information about the device physics. Hence there is no trade-off of any kind in switching from (2.27) to (2.38). Note also that in Figs. 2.6, 2.7 we show only the curves for $V_{\mathrm{c}} = 0$ since this is the worst case for the accuracy of (2.38) as discussed above (cf. Fig. 2.5). Substituting for a from (2.36) in (2.38) yields

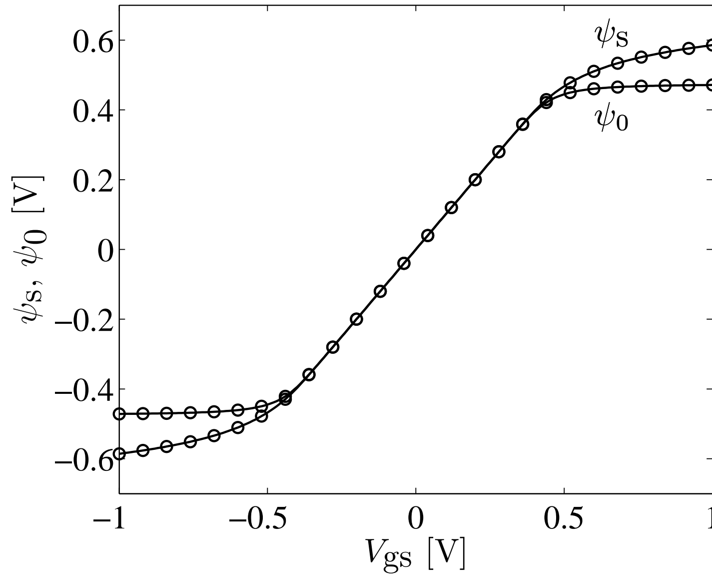


Figure 2.6: Surface and center potential versus gate voltage. Circles represent exact calculations based on (2.27) and the lines corresponds to the new approximation (2.38); $V_{\mathrm{c}} = 0$ V, $t_{\mathrm{si}} = 20$ nm, $t_{\mathrm{ox}} = 2$ nm, $\Delta\phi = 0$ V, $T = 300$ K.

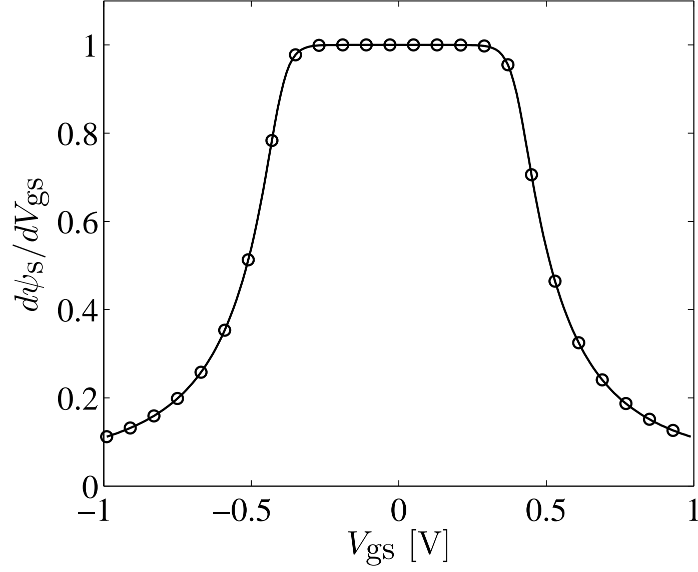
$$\varphi_{\mathrm{s}}(\varphi_0) = \varphi_0 + 2 \cdot \tanh(\varphi_0) \cdot \ln\left[\sec\left(b_1\sqrt{2 \cdot \cosh\varphi_0}\right)\right], \tag{2.41}$$

where

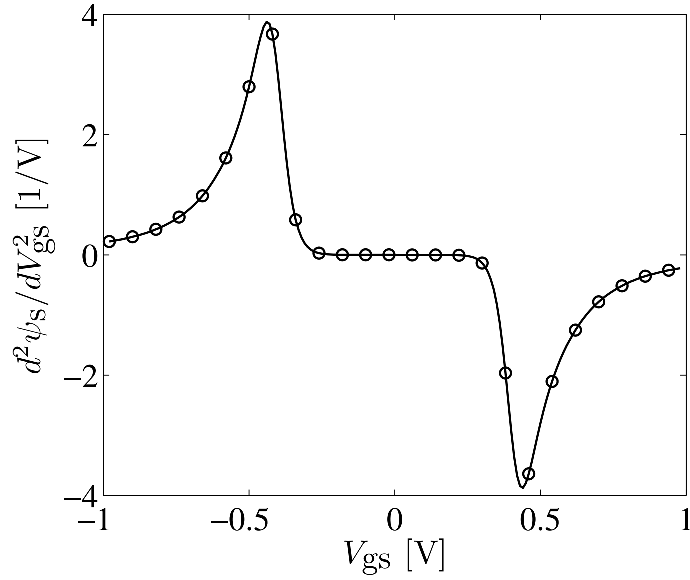
$$b_1 = \frac{t_{\mathrm{si}} \exp(-x_{\mathrm{n}}/4)}{4 \cdot L_{\mathrm{di}}}, \tag{2.42}$$

and

$$x_{\mathrm{n}} = \frac{V_{\mathrm{c}}}{\phi_{\mathrm{t}}}. \tag{2.43}$$



(a)



(b)

Figure 2.7: (a) $d\psi_s/dV_{gs}$ and (b) $d^2\psi_s/dV_{gs}^2$ versus gate voltage. Circles represent exact calculation and the lines corresponds to the new approximation; $V_c = 0$ V, $t_{si} = 20$ nm, $t_{ox} = 2$ nm, $\Delta\phi = 0$ V, $T = 300$ K.

With this notation the IVE (2.22) [63] becomes

$$f(\varphi_0) = 0 \tag{2.44}$$

where

$$f(\varphi_0) = \varphi_\mathrm{s}(\varphi_0) - x_\mathrm{gn} + b_2\sqrt{2 \cdot \cosh[\varphi_\mathrm{s}(\varphi_0)] - 2 \cdot \cosh \varphi_0}, \tag{2.45}$$

$$b_2 = 4 \cdot \eta r_\mathrm{c} b_1, \tag{2.46}$$

$$\eta = \mathrm{sgn}(x_\mathrm{gn}), \tag{2.47}$$

$$x_\mathrm{gn} = x_\mathrm{g} - \frac{x_\mathrm{n}}{2}, \tag{2.48}$$

and

$$x_\mathrm{g} = \frac{V_\mathrm{gs} - \Delta\phi}{\phi_\mathrm{t}}. \tag{2.49}$$

An equivalent form of (2.45) used in this work to develop a closed form solution algorithm in Section 2.8 is

$$f(\varphi_0) = \varphi_\mathrm{s} - x_\mathrm{gn} + b_2 \left\{2 \sinh(\varphi_0) \sinh[p(\varphi_0)] + 2 \cdot \cosh(\varphi_0)[\cosh p(\varphi_0) - 1]\right\}^{1/2} \tag{2.50}$$

where

$$p(\varphi_0) = 2 \cdot \tanh(\varphi_0) \cdot \ln\left[\sec\left(b_1\sqrt{2 \cdot \cosh \varphi_0}\right)\right]. \tag{2.51}$$

The IVE (2.50) is better conditioned than (2.45) near flatband where $\varphi_0 \approx \varphi_\mathrm{s} \approx x_\mathrm{gn}$. For example, for $|x_\mathrm{gn}| \lesssim 10^{-8}$ the square root term in (2.45) becomes zero if double precision calculations are used. This creates difficulties for computing and coding the derivative $df/d\varphi_0$ near the flatband while solving the IVE . The IVE (2.50) does not suffer from this problem except at a single flatband point where we have $\varphi_0 = 0$ and there is no need to solve the IVE. Once the IVE is solved the surface potential can be obtained from (2.41) and the gate charge density can be written as

$$q_\mathrm{g} = 2 \cdot C_\mathrm{ox}\left(V_\mathrm{g} - \Delta\phi - \psi_\mathrm{s}\right) \tag{2.52}$$

where the factor of 2 is from the presence of two gates.

2.7 Unipolar IVE

We now investigate the special case of (2.45) corresponding to $|x_\mathrm{gn}| \gtrsim 5$. This is useful not only for comparison with earlier work on the unipolar closed form

approximation [62] but as a first step in the development of an explicit algorithm to compute $\varphi_0(V_{\mathrm{gs}}, V_{\mathrm{c}})$ from new ambipolar IVE.

Physically, the condition $|x_{\mathrm{gn}}| \gtrsim 5$ means that only one type of carrier contributes appreciably to the charge density within the active region of the device. To simplify (2.45) in this case we introduce

$$\vartheta = b_1 \exp(\eta\varphi_0/2). \tag{2.53}$$

and reformulate (2.41) as

$$\varphi_{\mathrm{s}} = \eta \ln\left(\frac{\vartheta^2}{b_1^2}\right) + 2 \cdot \eta \ln\left[\sec\left(\vartheta\right)\right], \tag{2.54}$$

where we have used the approximations

$$2 \cdot \cosh(\varphi_0) \approx \exp(\eta\varphi_0) \tag{2.55}$$

and

$$\tanh(\varphi_0) \approx \eta \tag{2.56}$$

for $|\varphi_0| \gtrsim 5$. Substituting (2.54) in (2.45) and using the approximation $2 \cdot \cosh(\varphi_{\mathrm{s}}) \approx \exp(\eta\varphi_{\mathrm{s}})$ we obtain the IVE in terms of ϑ

$$\ln(\vartheta \sec\vartheta) + 2 \cdot r_{\mathrm{c}}\vartheta \tan\vartheta - F_{\mathrm{b}} = 0 \tag{2.57}$$

where

$$F_{\mathrm{b}} = \frac{\eta\, x_{\mathrm{gn}} - x_{\mathrm{n}}/2}{2} + \ln\left(\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}}}\right). \tag{2.58}$$

The unipolar IVE (2.57) corresponds to that in [62] when $\eta = 1$ and only the electron contribution is included. In this case

$$\vartheta \approx \theta \equiv b_1 \exp(\varphi_0/2), \tag{2.59}$$

$$F_{\mathrm{b}} \approx F \equiv \frac{x_{\mathrm{g}} - x_{\mathrm{n}}}{2} + \ln\left(\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}}}\right), \tag{2.60}$$

and (2.57) becomes

$$\ln(\theta) + \ln\left(\sec\theta\right) + 2 \cdot r_{\mathrm{c}}\theta \tan\theta - F = 0 \tag{2.61}$$

which is the precisely the IVE given in [62][1].

When (2.57) is used the surface potential is related to ϑ by (2.54) and (2.21). Physically, ϑ is proportional to $\sqrt{n_0}$ where n_0 is the electron ($\eta = 1$) or hole ($\eta = -1$) concentration in the middle of the body.

The inversion charge (electron) density is an important parameter in compact modeling of MOSFETs and its absolute value per channel can be approximated in the inversion region:

$$q_{\rm n} = C_{\rm ox}\left(V_{\rm g} - \Delta\phi - \psi_{\rm s}\right). \tag{2.62}$$

Note that unlike for planar bulk MOSFETs the inversion charge density for DG-FinFETs is a linear function of surface potential due to the absence of doping. In the accumulation region the inversion charge density can be neglected, however, (2.62) can be used to estimate hole charge density per channel in the accumulation region. To write $q_{\rm n}$ in terms of θ we substitute the unipolar approximation (2.54) with $\eta = 1$ in (2.62) and using (2.61) yields

$$q_{\rm n} = 4 \cdot C_{\rm si}\ \phi_{\rm t}\ q_{\rm i} \tag{2.63}$$

where

$$q_{\rm i} = \theta \tan\theta \tag{2.64}$$

is the normalized inversion charge density.

2.8 Closed Form Solution of the Ambipolar IVE

The range of ϑ in (2.57) is between 0 and $\pi/2$ [62]. The asymptotic solutions for ϑ corresponding to $\vartheta \to 0$ and $\vartheta \to \pi/2$ are developed in Appendix C and are used to obtain asymptotic solutions for φ_0 using (2.53). These are denoted as $\varphi_0^{(0)}$ and $\varphi_0^{(\pi/2)}$. The three step algorithm similar to that in [62] is developed in [65] to solve the IVE (2.50):

$$\varphi_0 = \varphi_{00} + \Delta\varphi_{01} + \Delta\varphi_{02} \tag{2.65}$$

[1] In [62] the θ is denoted as β.

where

$$\varphi_{00} = \frac{1}{2}\left[\varphi_0^{(0)} + \varphi_0^{(\pi/2)} + \eta\sqrt{\left(\varphi_0^{(0)} - \varphi_0^{(\pi/2)}\right)^2 + 0.001}\right]. \tag{2.66}$$

The correction term $\Delta\varphi_{01}$ is given by [62]

$$\Delta\varphi_{01} = -\frac{f}{f'}\left\{1 + \frac{f}{2\cdot f'^2}\left[f'' + \frac{f}{f'^2}\left(f''^2 - \frac{f'f'''}{3}\right)\right]\right\} \tag{2.67}$$

where f and its derivatives $f' = \mathrm{d}f/\mathrm{d}\varphi_0$, $f'' = \mathrm{d}^2f/\mathrm{d}\varphi_0^2$, and $f''' = \mathrm{d}^3f/\mathrm{d}\varphi_0^3$ are calculated at $\varphi_0 = \varphi_{00}$. The correction term $\Delta\varphi_{02}$ is also given by (2.67) but with f, f', f'', and f''' evaluated at $\varphi_0 = \varphi_{00} + \Delta\varphi_{01}$.

Once φ_0 is found the surface and the center potentials can be obtained from (2.15), (2.21), and (2.41). In Fig. 2.8 the surface and the center potentials obtained by closed form algorithm are compared with that obtained using numerical solution for three different values of V_c. It is seen that the new closed form algorithm accurately reproduces the exact results. The absolute error is found to be less than 0.01pV as shown in Fig. 2.9. Similar results are obtained for various device dimensions and bias combinations. Fig. 2.10 shows the first and second derivatives of φ_s with respect to V_gs which (as is essential for compact modeling work) vary smoothly as functions of V_gs. Fig. 2.11a shows the surface potential obtained by solving IVEs (2.50), (2.57), and (2.61). In the hole enhancement region (i.e. $-x_\mathrm{gn} \ll -5$) (2.61) does not apply and (2.57) must be used instead. Fig. 2.11b shows the surface potential near the flat band condition. As far as the accuracy is concerned the use of the unipolar approximation (2.57) results in the error of less than 1nV which is acceptable for compact modeling applications. However it results in a discontinuity “cusp" (non existing derivative $d\varphi_\mathrm{s}/dV_\mathrm{g}$) at flatband condition $x_\mathrm{gn} = 0$ (which corresponds to $V_\mathrm{gs} = 0$ in Fig. 2.11 where $V_\mathrm{c} = 0$). This is the motivation for using (2.50) rather than (2.57).

The new algorithm for solving the IVE has been implemented in Verilog-A as part of the compact FinFET model [67, 63] and further tested for accuracy and

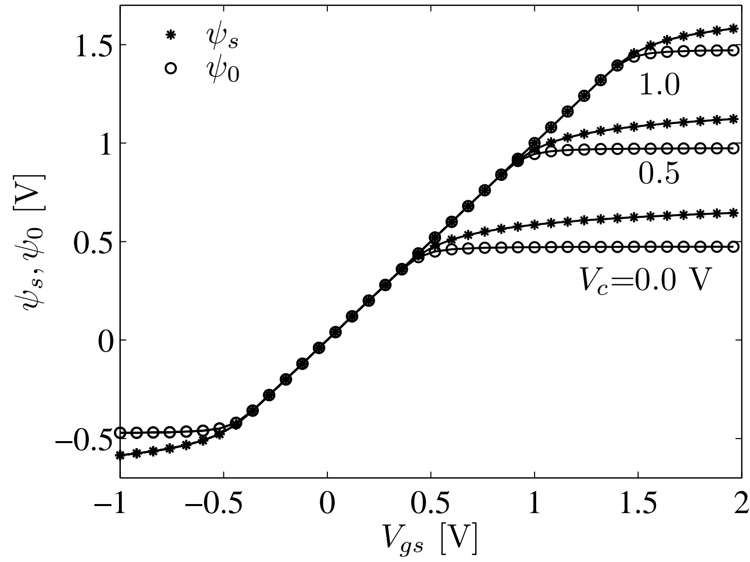


Figure 2.8: Surface and center potential obtained by solving IVE using closed form algorithm is compared with that obtained by bisection method. Lines and symbols corresponds to the results obtained from closed form algorithm and numerical solution, respectively; $t_{\rm ox} = 2$ nm, $t_{\rm si} = 20$ nm, $\Delta\phi = 0$.

convergence. In agreement with Fig. 2.8 the results are indistinguishable from those obtained from iterative solution of the IVE.

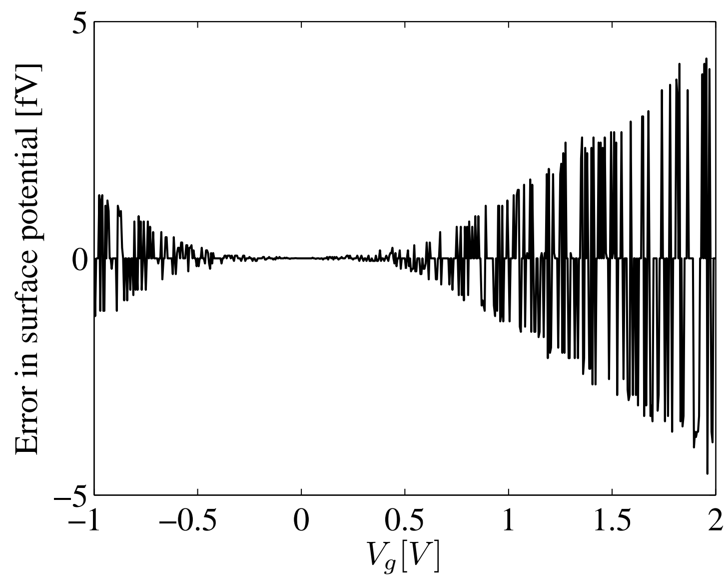
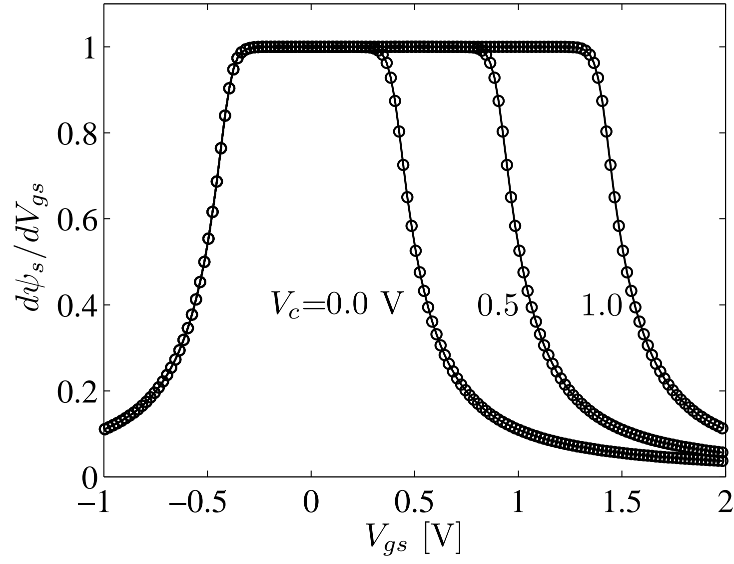
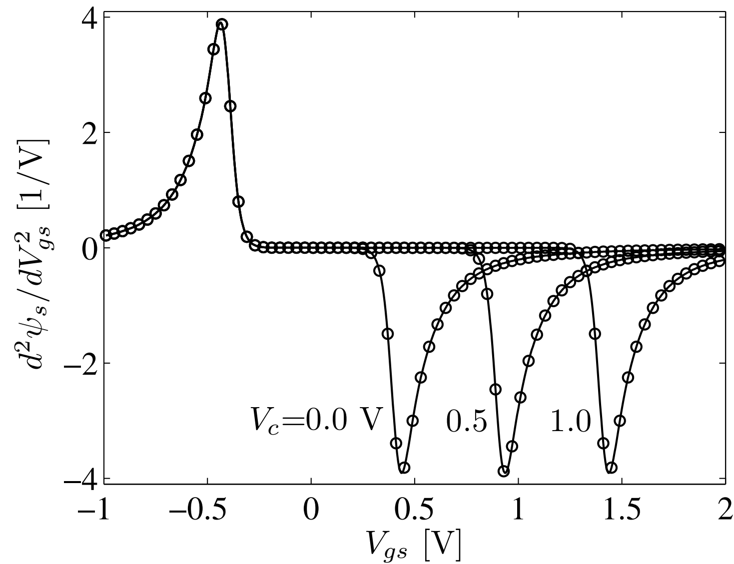


Figure 2.9: Error in the surface potential obtained by new algorithm when compared to that obtained by numerical solution of (2.50) for $V_c = 0$V. Device parameters are the same as in Fig. 2.8.

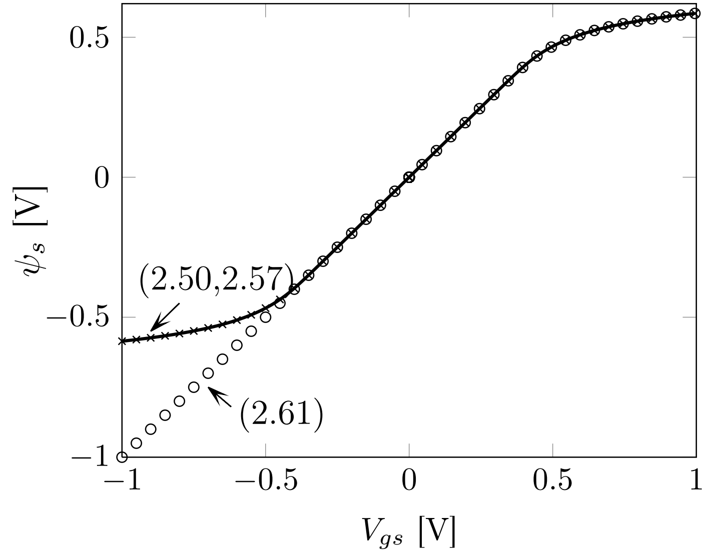


(a)

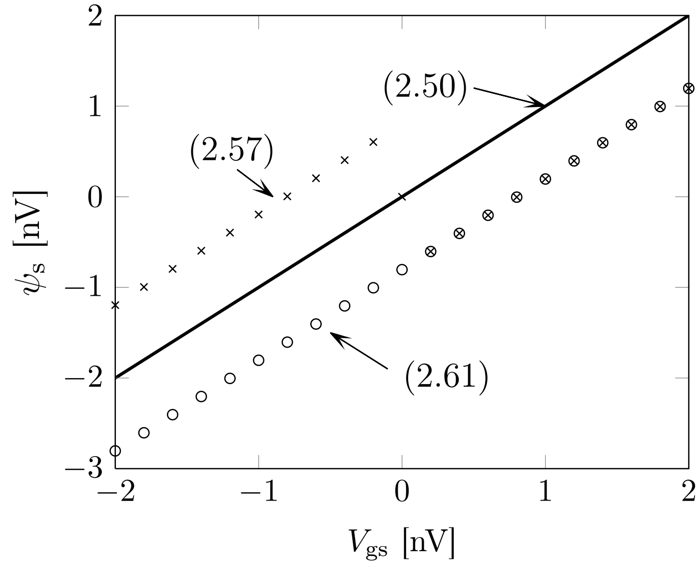


(b)

Figure 2.10: (a) First and (b) second derivative of the surface potential with respect to the gate voltage obtained by solving IVE using closed form algorithm is compared with that obtained by numerical solution. Lines and symbols corresponds to the results obtained from closed form algorithm and numerical solution, respectively. Device parameters are same as in Fig. 2.8.



(a)



(b)

Figure 2.11: (a) Surface potential obtained by solving IVEs (2.50), (2.57), and (2.61) for $V_c = 0$ V, (b) Surface potential near flatband condition. Device parameters are same as in Fig. 2.8.

Chapter 3

ELECTROSTATICS of the INDEPENDENT-GATE ASYMMETRIC DG-FinFET

3.1 Introduction

In this chapter the Poisson-Boltzman equation for an independent-gate asymmetric DG-FinFET is solved and the IVEs are derived. The presence of independent gates with different bias conditions and gate oxide thicknesses destroys the symmetry of the device and results in different boundary conditions at gate-1 and gate-2. Consequently, the boundary condition (2.13) does not apply for the independent gate asymmetric DG-FinFET. The solution of the Poisson-Boltzmann equation (2.5) with both electron and holes contribution to the charge density involves special functions [71]. However, neglecting holes for an n-channel device simplifies the integration and the solution of the Poisson-Boltzmann equation has a trigonometric or hyperbolic form depending upon the bias conditions and device parameters. As the IVEs take different functional forms (trigonometric and hyperbolic), the appropriate form to solve needs to be determined before solving the IVEs. This situation has no analog in compact modeling of other field effect transistors. We derive an explicit expression for the boundary between the trigonometric and the hyperbolic potential solutions. An efficient numerical algorithm is proposed for solving the IVEs to obtain surface potentials at gate-1 and gate-2.

Fig. 3.1 shows the cross-section of the independent-gate asymmetric DG-FinFET where the origin of x-coordinate is placed at the center of the body to be consistent with earlier work on the independent-gate asymmetric DG-FinFET [75, 76, 77]. To simplify integration of the Poisson-Boltzmann equation we start with (2.5) considering only electrons and neglect the hole contribution to the charge density (i.e. we assume $\psi(x) > 3 \cdot \phi_{\mathrm{t}}$):

$$\frac{\mathrm{d}^2\psi}{\mathrm{d}x^2} = \frac{qn_{\mathrm{i}}}{\epsilon_{\mathrm{si}}} \exp\left(\frac{\psi - V_{\mathrm{c}}}{\phi_{\mathrm{t}}}\right) \tag{3.1}$$

Multiplying both sides by $2 \cdot \frac{\mathrm{d}\psi}{\mathrm{d}x}$ and integrating yields

$$\frac{\mathrm{d}\psi}{\mathrm{d}x} = -\sigma \left[\left(\frac{\phi_\mathrm{t}}{L_\mathrm{di}} \right)^2 \exp \left(\frac{\psi - V_\mathrm{c}}{\phi_\mathrm{t}} \right) + c \right]^{1/2} \tag{3.2}$$

where

$$c = E_\mathrm{x0}^2 - \left(\frac{\phi_\mathrm{t}}{L_\mathrm{di}} \right)^2 \exp \left(\frac{\psi_\mathrm{x0} - V_\mathrm{c}}{\phi_\mathrm{t}} \right), \tag{3.3}$$

ψ_{x0} and E_x0 are the electrostatic potential and electric field, respectively, at some point x_0 along the path of integration, and σ is the sign of $-\frac{\mathrm{d}\psi}{\mathrm{d}x}$ in the neighborhood of x_0. Integrating (3.2) we obtain

$$\psi(x) = V_\mathrm{c} - 2 \cdot \phi_\mathrm{t} \ln \left\{ \frac{\phi_\mathrm{t}}{\sqrt{c} L_\mathrm{di}} \sinh \left[\tanh^{-1} \left(\frac{\sqrt{c}}{\sigma E_\mathrm{x0}} \right) - \frac{\sigma \sqrt{c} x_0}{2 \cdot \phi_\mathrm{t}} + \frac{\sigma \sqrt{c} x}{2 \cdot \phi_\mathrm{t}} \right] \right\} \tag{3.4}$$

When $c < 0$ we can use identity $\tanh^{-1}(ix) = i \tan^{-1}(x)$ and $\sinh(ix) = i \sin(x)$ to avoid encountering complex numbers which yields

$$\psi(x) = V_\mathrm{c} - 2 \cdot \phi_\mathrm{t} \ln \left\{ \frac{\phi_\mathrm{t}}{\sqrt{-c} L_\mathrm{di}} \sin \left[\tan^{-1} \left(\frac{\sqrt{-c}}{\sigma E_\mathrm{x0}} \right) - \frac{\sigma \sqrt{-c} x_0}{2 \cdot \phi_\mathrm{t}} + \frac{\sigma \sqrt{-c} x}{2 \cdot \phi_\mathrm{t}} \right] \right\} \tag{3.5}$$

Thus depending on the sign of c the potential $\psi(x)$ can have trigonometric or hyperbolic form. To select the sign of σ it can be noted that for hyperbolic case $\psi(x)$ is monotonic within the device as $\psi(x)$ has sinh function. Physically, for this case $\psi(x)$ should be monotonically decreasing function of x for $V_1 > V_2$ and monotonically increasing function of x for $V_1 < V_2$ where $V_\mathrm{j} = V_\mathrm{gj} - \Delta\phi_\mathrm{j}$, $\Delta\phi_\mathrm{j}$ is the work-function difference between the body and the gate-j, and $j = 1, 2$. Thus σ can be selected as $\sigma = \mathrm{sgn}(V_1 - V_2)$ and x_0 can be any point within the device. However, for trigonometric case as $\psi(x)$ has sin function there exist a potential minimum (within or outside the device) and the sign of E_x0 depends on location of x_0. As suggested in [77] if we set $x_0 = -t_\mathrm{si}/2$ for $V_1 \geq V_2$ and $x_0 = t_\mathrm{si}/2$ for $V_1 < V_2$ then one can write $\sigma = \mathrm{sgn}(V_1 - V_2)$. It may be mentioned that in the original work [75] only the case $V_1 > V_2$ (i.e. $\sigma = 1$) was considered. In [78] we introduced σ to include the case where $V_1 < V_2$.

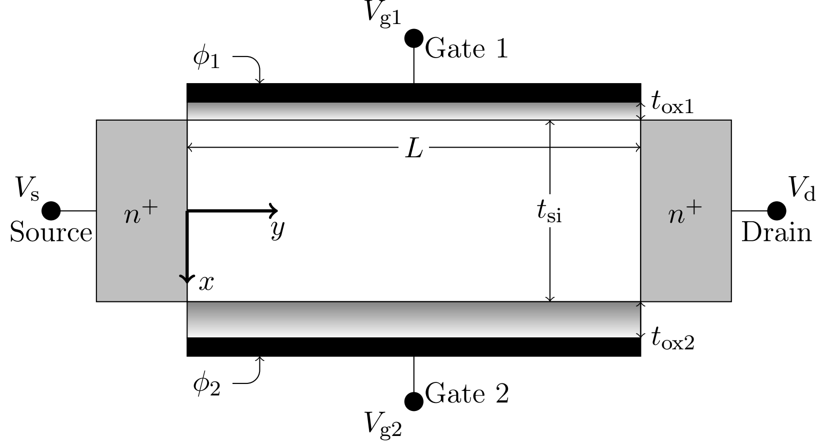


Figure 3.1: Cross-section of the independent-gate asymmetric DG-FinFET. ϕ_1 and ϕ_2 are the workfunctions of gate-1 and gate-2, respectively.

3.2 Trigonometric Solution

To write the solution in a form given by Lu and Taur [75] in term of α and θ, we define

$$\theta = \frac{t_{\mathrm{si}}\sqrt{c}}{4 \cdot \phi_{\mathrm{t}}} \tag{3.6}$$

and

$$\alpha = \begin{cases} \tan^{-1}\left(\frac{\sqrt{-c}}{E_{\mathrm{x0}}}\right) - \frac{\sqrt{-c}x_0}{2 \cdot \phi_{\mathrm{t}}} & \text{for } \sigma = 1 \\ \pi + \tan^{-1}\left(\frac{\sqrt{-c}}{E_{\mathrm{x0}}}\right) - \frac{\sqrt{-c}x_0}{2 \cdot \phi_{\mathrm{t}}} & \text{for } \sigma = -1 \end{cases} \tag{3.7}$$

then (3.5) becomes

$$\psi(x) = V_{\mathrm{c}} - 2 \cdot \phi_{\mathrm{t}} \ln\left[\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}}\theta} \sin\left(\alpha + \frac{2 \cdot \theta x}{t_{\mathrm{si}}}\right)\right]. \tag{3.8}$$

From (3.8) the surface potential at both the interfaces can be expressed in terms of α and θ by setting $x = -t_{\mathrm{si}}/2$ for ψ_{s1} and $x = t_{\mathrm{si}}/2$ for ψ_{s2} which yields

$$\psi_{\mathrm{s1}} = V_{\mathrm{c}} - 2 \cdot \phi_{\mathrm{t}} \ln\left[\frac{t_{\mathrm{si}} \sin(\alpha - \theta)}{4 \cdot L_{\mathrm{di}}\theta}\right] \tag{3.9}$$

and

$$\psi_{\mathrm{s2}} = V_{\mathrm{c}} - 2 \cdot \phi_{\mathrm{t}} \ln\left[\frac{t_{\mathrm{si}} \sin(\alpha + \theta)}{4 \cdot L_{\mathrm{di}}\theta}\right]. \tag{3.10}$$

Differentiating (3.8) w.r.t x the electric field distribution within the body is

$$E(x) = -\frac{\mathrm{d}\psi}{\mathrm{d}x} = \frac{4 \cdot \phi_{\mathrm{t}}\theta}{t_{\mathrm{si}}} \cot\left(\alpha + \frac{2 \cdot \theta x}{t_{\mathrm{si}}}\right). \tag{3.11}$$

The electric field inside the body at $x = -t_{\mathrm{si}}/2$ is

$$E_1 = \frac{4 \cdot \phi_{\mathrm{t}}\theta}{t_{\mathrm{si}}} \cot\left(\alpha - \theta\right) \tag{3.12}$$

and at $x = t_{\mathrm{si}}/2$ is

$$E_2 = \frac{4 \cdot \phi_{\mathrm{t}}\theta}{t_{\mathrm{si}}} \cot\left(\alpha + \theta\right). \tag{3.13}$$

The boundary condition that the normal component of the electric displacement vector is continuous at the gate-1 Si-SiO_2 interfaces gives

$$C_{\mathrm{ox1}}(V_1 - \psi_{\mathrm{s1}}) = \epsilon_{\mathrm{si}} E_1. \tag{3.14}$$

From (3.12) and (3.14) the surface potential there is then

$$\psi_{\mathrm{s1}} = V_1 - 4 \cdot \phi_{\mathrm{t}} r_{\mathrm{c1}} \theta \cot(\alpha - \theta). \tag{3.15}$$

Similarly, the boundary condition that the normal component of the electric displacement vector is continuous at gate-2 Si-SiO_2 interfaces results in

$$C_{\mathrm{ox2}}(V_2 - \psi_{\mathrm{s2}}) = -\epsilon_{\mathrm{si}} E_2. \tag{3.16}$$

From (3.13) and (3.16) the surface potential there is then

$$\psi_{\mathrm{s2}} = V_2 + 4 \cdot \phi_{\mathrm{t}} r_{\mathrm{c2}} \theta \cot(\alpha + \theta) \tag{3.17}$$

Equating (3.9) and (3.15) we have

$$V_1 - V_{\mathrm{c}} = -2 \cdot \phi_{\mathrm{t}} \ln\left[\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}}\theta} \sin\left(\alpha - \theta\right)\right] + 4 \cdot \phi_{\mathrm{t}} r_{\mathrm{c1}} \theta \cot\left(\alpha - \theta\right). \tag{3.18}$$

Similarly, equating (3.10) and (3.17) we obtain

$$V_2 - V_{\mathrm{c}} = -2 \cdot \phi_{\mathrm{t}} \ln\left[\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}}\theta} \sin\left(\alpha + \theta\right)\right] - 4 \cdot \phi_{\mathrm{t}} r_{\mathrm{c2}} \theta \cot\left(\alpha + \theta\right) \tag{3.19}$$

where $r_{c1} = C_{si}/C_{ox1}$ and $r_{c2} = C_{si}/C_{ox2}$. Subtracting (3.18) from (3.19) yields

$$V_2 - V_1 + 2 \cdot \phi_t \ln \left[\frac{\sin(\alpha + \theta)}{\sin(\alpha - \theta)} \right] + 4 \cdot \phi_t \theta [r_{c1} \cot(\alpha - \theta) + r_{c2} \cot(\alpha + \theta)] = 0. \quad (3.20)$$

Any two of the above three equations form a set of coupled input voltage equations which needs to be solved for the unknown variables α and θ and hence the surface potentials ψ_{s1} and ψ_{s2}. It may be noted that instead to two coupled IVEs it is possible to derive a single IVE in terms of ψ_{s1} for $V_1 > V_2$ and ψ_{s2} for $V_1 < V_2$ [77] (cf. Section 3.6). Nevertheless, the coupled IVEs derived in this section are used to derive the drain current and terminal charge model.

Applying Gauss's law, the inversion (electron) charge density can be expressed as

$$Q_n = -\epsilon_{si} (E_1 - E_2) = -4 \cdot \phi_t C_{si} \theta [\cot(\alpha - \theta) - \cot(\alpha + \theta)] \quad (3.21)$$

Note that the Q_n is the total inversion charge density within the body. The variation of the electron concentration with x can be found from (2.3) and (3.8) as

$$n(x) = n_i \left(\frac{4 \cdot C_{si}}{C_f} \right)^2 \theta^2 \csc^2 \left(\alpha + \frac{2 \cdot \theta x}{t_{si}} \right) \quad (3.22)$$

which gives surface electron concentrations

$$n_1 = n(-t_{si}/2) = n_i \left(\frac{4 \cdot C_{si}}{C_f} \right)^2 \theta^2 \csc^2 (\alpha - \theta) \quad (3.23)$$

and

$$n_2 = n(t_{si}/2) = n_i \left(\frac{4 \cdot C_{si}}{C_f} \right)^2 \theta^2 \csc^2 (\alpha + \theta) . \quad (3.24)$$

3.3 Hyperbolic Solution

For this case defining

$$\theta_* = \frac{t_{si} \sqrt{c}}{4 \cdot \phi_t} \quad (3.25)$$

and

$$\alpha_* = \tanh^{-1} \left(\frac{\sqrt{c}}{\sigma E_{x0}} \right) - \frac{\sigma \sqrt{c} x_0}{2 \cdot \phi_t} \quad (3.26)$$

(3.4) becomes

$$\psi(x) = V_{\mathrm{c}} - 2 \cdot \phi_{\mathrm{t}} \ln \left[\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}} \theta_*} \sinh \left(\alpha_* + \sigma \frac{2 \cdot \theta_* x}{t_{\mathrm{si}}} \right) \right]. \tag{3.27}$$

Setting $x = t_{\mathrm{si}}/2$ yields the surface potential at gate 1

$$\psi_{\mathrm{s1}} = V_{\mathrm{c}} - 2 \cdot \phi_{\mathrm{t}} \ln \left[\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}} \theta_*} \sinh \left(\alpha_* - \sigma \theta_* \right) \right] \tag{3.28}$$

and setting $x = -t_{\mathrm{si}}/2$ yields the surface potential at gate 2

$$\psi_{\mathrm{s2}} = V_{\mathrm{c}} - 2 \cdot \phi_{\mathrm{t}} \ln \left[\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}} \theta_*} \sinh \left(\alpha_* + \sigma \theta_* \right) \right]. \tag{3.29}$$

Differentiating (3.27) w.r.t. x we get the electric field distribution

$$E(x) = -\frac{\mathrm{d}\psi}{\mathrm{d}x} = \sigma \frac{4 \cdot \phi_{\mathrm{t}} \theta_*}{t_{\mathrm{si}}} \coth \left(\alpha_* + \sigma \frac{2\theta_* x}{t_{\mathrm{si}}} \right). \tag{3.30}$$

The electric field inside the semiconductor at $x = -t_{\mathrm{si}}/2$ is

$$E_1 = \sigma \frac{4 \cdot \phi_{\mathrm{t}} \theta_*}{t_{\mathrm{si}}} \coth \left(\alpha_* - \sigma \theta_* \right) \tag{3.31}$$

and at $x = t_{\mathrm{si}}/2$ is

$$E_2 = \sigma \frac{4 \cdot \phi_{\mathrm{t}} \theta_*}{t_{\mathrm{si}}} \coth \left(\alpha_* + \sigma \theta_* \right). \tag{3.32}$$

From (3.31) and the boundary condition (3.14) the surface potential at the gate-1 is

$$\psi_{\mathrm{s1}} = V_1 - 4 \cdot \sigma \phi_{\mathrm{t}} r_{\mathrm{c1}} \theta_* \coth(\alpha_* - \sigma \theta_*). \tag{3.33}$$

Similarly, from (3.32) and the boundary condition (3.16) the surface potential at gate-2 is

$$\psi_{\mathrm{s2}} = V_2 + 4 \cdot \sigma \phi_{\mathrm{t}} r_{\mathrm{c2}} \theta_* \coth(\alpha_* + \sigma \theta_*). \tag{3.34}$$

Equating (3.28) and (3.33) we have

$$V_1 - V_{\mathrm{c}} = -2 \cdot \phi_{\mathrm{t}} \ln \left[\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}} \theta_*} \sinh \left(\alpha_* - \sigma \theta_* \right) \right] + 4 \cdot \sigma \phi_{\mathrm{t}} \theta_* r_{\mathrm{c1}} \coth \left(\alpha_* - \sigma \theta_* \right) \tag{3.35}$$

Similarly, equating (3.29) and (3.34) yields

$$V_2 - V_{\mathrm{c}} = -2 \cdot \phi_{\mathrm{t}} \ln \left[\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}} \theta_*} \sinh \left(\alpha_* + \sigma \theta_* \right) \right] - 4 \cdot \sigma \phi_{\mathrm{t}} \theta_* r_{\mathrm{c2}} \coth \left(\alpha_* + \sigma \theta_* \right) \tag{3.36}$$

Subtracting (3.35) from (3.36) we have

$$V_2 - V_1 + 2 \cdot \phi_{\mathrm{t}} \ln \left[\frac{\sinh(\alpha_* + \sigma\theta_*)}{\sinh(\alpha_* - \sigma\theta_*)} \right] + 4 \cdot \sigma\phi_{\mathrm{t}}\theta_* [r_{\mathrm{c1}} \coth(\alpha_* - \sigma\theta_*) + r_{\mathrm{c2}} \coth(\alpha_* + \sigma\theta_*)] = 0 \quad (3.37)$$

Any two of (3.35), (3.36), and (3.37) together form a set of IVEs which needs to be solved for unknown variables α_* and θ_* and hence surface potentials for the hyperbolic case. In this case the inversion charge density becomes

$$Q_{\mathrm{n}} = -\epsilon_{\mathrm{si}} (E_1 - E_2) = -4 \cdot \sigma\phi_{\mathrm{t}} C_{\mathrm{si}} \theta_* [\coth(\alpha_* - \sigma\theta_*) - \coth(\alpha_* + \sigma\theta_*)] \quad (3.38)$$

and the variation of the electron concentration with x can be found from (2.3) and (3.27) as

$$n(x) = n_{\mathrm{i}} \left(\frac{4 \cdot C_{\mathrm{si}}}{C_{\mathrm{f}}} \right)^2 \theta^2 \csc^2 \left(\alpha + \frac{2 \cdot \sigma\theta x}{t_{\mathrm{si}}} \right) \quad (3.39)$$

which gives surface electron concentrations

$$n_1 = n(-t_{\mathrm{si}}/2) = n_{\mathrm{i}} \left(\frac{4 \cdot C_{\mathrm{si}}}{C_{\mathrm{f}}} \right)^2 \theta^2 \mathrm{csch}^2 (\alpha - \sigma\theta) \quad (3.40)$$

and

$$n_2 = n(t_{\mathrm{si}}/2) = n_{\mathrm{i}} \left(\frac{4 \cdot C_{\mathrm{si}}}{C_{\mathrm{f}}} \right)^2 \theta^2 \mathrm{csch}^2 (\alpha + \sigma\theta) . \quad (3.41)$$

3.4 Solution Space

The boundary between the hyperbolic and trigonometric solution is determined by a transcendental equation derived in [75] which defines the critical value V_{cr} for given gate bias and device parameters where the two different solutions merge. To obtain an expression for the critical value V_{cr} one can introduce the variable s representing the limiting value [75]

$$\frac{\alpha}{\theta} = \frac{\alpha_*}{\theta_*} \quad (3.42)$$

on the line Γ_1 separating the trigonometric region from the hyperbolic region with $\sigma = 1$ shown in Fig. 3.2. This line corresponds to $\alpha, \theta, \alpha_*, \theta_* \to 0$. This leads to

$$V_{\mathrm{cr}} = V_1 - 2 \cdot \phi_{\mathrm{t}} \ln \left[\frac{4 \cdot L_{\mathrm{di}}}{t_{\mathrm{si}}(s-1)} \right] - \frac{4 \cdot \phi_{\mathrm{t}} r_{\mathrm{c1}}}{s-1} \quad (3.43)$$

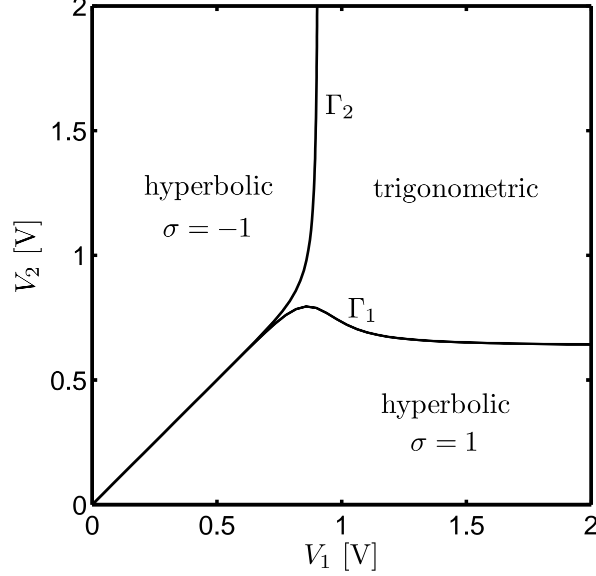


Figure 3.2: Regions of operation on the V_1-V_2 plane for $V_c = 0.5$ V, $t_{si} = 20$ nm, $t_{ox1} = 2$ nm and $t_{ox2} = 40$ nm.

where s is determined numerically from the transcendental equation [75]

$$\frac{V_2 - V_1}{2 \cdot \phi_t} + \ln\left(\frac{s+1}{s-1}\right) + 2 \cdot \left(\frac{r_{c1}}{s-1} + \frac{r_{c2}}{s+1}\right) = 0. \tag{3.44}$$

These equations determine the lower partition line Γ_1 in Fig. 3.2 on which $V_1 > V_2$. The equation of the upper partition line Γ_2 on which $V_1 < V_2$ can be obtained by interchanging $V_1 \leftrightarrow V_2$ and $r_{c1} \leftrightarrow r_{c2}$.

$$V_{cr} = V_2 - 2 \cdot \phi_t \ln\left[\frac{4 \cdot L_{di}}{t_{si}(s-1)}\right] - \frac{4 \cdot \phi_t r_{c2}}{s-1} \tag{3.45}$$

where s can be found from the solution of equation

$$\frac{V_1 - V_2}{2 \cdot \phi_t} + \ln\left(\frac{s+1}{s-1}\right) + 2 \cdot \left(\frac{r_{c1}}{s+1} + \frac{r_{c2}}{s-1}\right) = 0. \tag{3.46}$$

For $t_{ox1} \neq t_{ox2}$ the line Γ_2 has a different shape than the lower partition line Γ_1. Alternatively, equations (3.45) and (3.46) can be also obtained from (3.8), (3.27) and the usual boundary conditions at $x = \pm t_{si}/2$ [75] by redefining

$$s = \frac{\pi - \alpha}{\theta} = \frac{\alpha_*}{\theta_*} \tag{3.47}$$

where the ratio is evaluated on the second partition line Γ_2. As illustrated in Fig. 3.3 and Fig. 3.4, the boundary between the three regions shifts with the increase of the imref splitting. Since the line $V_1 = V_2$ (i.e. $V_{g1} - \Delta\phi_1 = V_{g2} - \Delta\phi_2$) always falls within trigonometric region (cf. Fig. 3.2) the trigonometric solution always applies in this case even if $t_{ox1} \neq t_{ox2}$. This includes the case of the common-gate symmetric DG-FinFET [75]. Mathematically, this property of the partition line is represented by the condition $V_{cr} = \infty$ for $V_1 = V_2$.

For a device with $t_{ox1} = t_{ox2}$ and with independent gates the partition lines are also symmetric (cf. Fig. 3.3). This is required by the intrinsic symmetry of the device and without any computations confirms that there are three (trigonometric, hyperbolic with $\sigma = 1$, and hyperbolic with $\sigma = -1$) rather than two regions on the V_1-V_2 plane.

In [75] the regions of operation are found by first solving (3.44) numerically for s and then substituting s in (3.43) to get V_{cr}. For $V_1 \approx V_2$ equation (3.44) and (3.46) are poorly conditioned and are difficult to solve numerically. Since it is desirable that compact models of independent-gate asymmetric DG-FinFETs should include the common-gate symmetric DG-FinFET as a special case, this represents a potential problem for model development and convergence of circuit simulations.

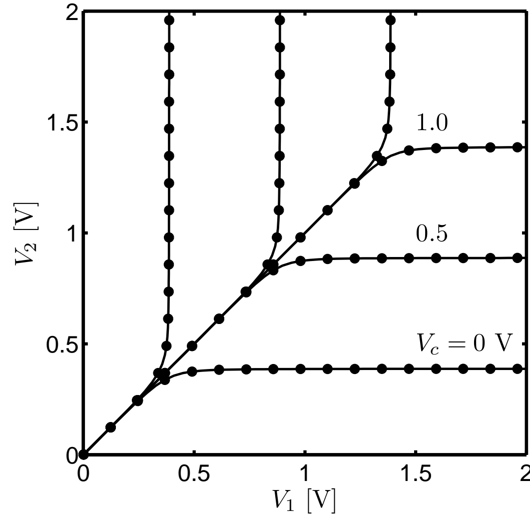


Figure 3.3: Partition lines on the V_1-V_2 plane with V_c as parameter obtained from numerical solution (circles) and analytical solution (lines); $t_{si} = 20$ nm, $t_{ox1} = t_{ox2} = 2$ nm.

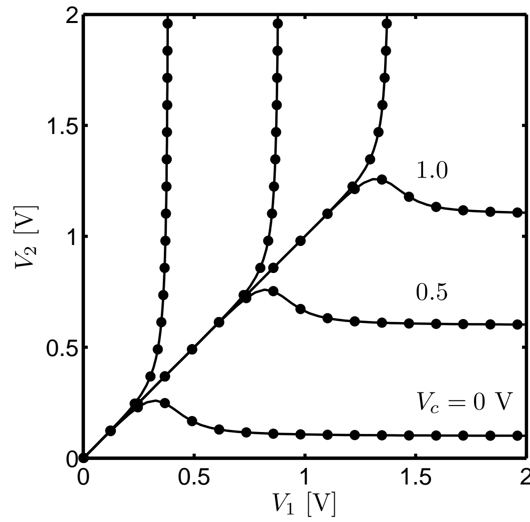


Figure 3.4: Partition lines on V_1-V_2 plane with V_c as parameter obtained from numerical solution (circles) and analytical solution (lines); $t_{si} = 20$ nm, $t_{ox1} = 2$ nm , $t_{ox2} = 40$ nm.

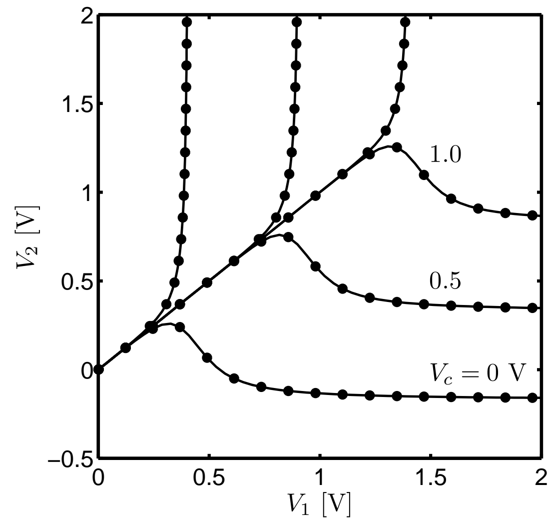


Figure 3.5: Partition lines on V_1-V_2 plane with V_c as parameter obtained from numerical solution (circles) and analytical solution (lines); $t_\mathrm{si} = 10$ nm, $t_\mathrm{ox1} = 2$ nm , $t_\mathrm{ox2} = 40$ nm.

3.5 Analytical Expression for the Partition Lines

With the physical picture and the complete partition diagrams in place it remains to simplify the computational procedure. In this study we switch from computing the critical value V_{cr} of the imref splitting to computing the critical values $V_{1\text{cr}}$ and $V_{2\text{cr}}$ of V_1 and V_2, respectively [78]. This leads to the expressions for $V_{1\text{cr}}$ and $V_{2\text{cr}}$ in terms of the Lambert W function [79] which are mathematically equivalent to (3.43), (3.44) and (3.45), (3.46) but are much better conditioned and exhibit no singular behavior. When $V_1 > V_2$ we find the critical voltage $V_{2\text{cr}}$ at gate 2 for a given value of V_c and V_1. Comparison of V_2 with $V_{2\text{cr}}$ establishes the region of operation. Similarly, for $V_1 < V_2$ we find the critical voltage $V_{1\text{cr}}$ at gate 1 for a given value of V_c and V_2. Now the region of operation is established by comparing V_1 with $V_{1\text{cr}}$. From (3.43)

$$ue^u = v_1; \qquad V_1 > V_2 \tag{3.48}$$

where

$$u = \frac{2 \cdot r_{\text{c1}}}{s-1}; \qquad V_1 > V_2 \tag{3.49}$$

and

$$v_1 = \frac{r_{\text{c1}} t_{\text{si}}}{2 \cdot L_{\text{di}}} \exp\left(\frac{V_1 - V_\text{c}}{2 \cdot \phi_\text{t}}\right); \qquad V_1 > V_2 \tag{3.50}$$

Then $u = W(v_1)$,

$$s = 1 + \frac{2 \cdot r_{\text{c1}}}{W(v_1)}; \qquad V_1 > V_2 \tag{3.51}$$

and from (3.44)

$$V_{2\text{cr}} = V_1 - 2 \cdot \phi_\text{t} \ln\left(\frac{s+1}{s-1}\right) - 4 \cdot \phi_\text{t} \left(\frac{r_{\text{c1}}}{s-1} + \frac{r_{\text{c2}}}{s+1}\right); \qquad V_1 > V_2 \tag{3.52}$$

Similarly, from (3.46)

$$V_{1\text{cr}} = V_2 - 2 \cdot \phi_\text{t} \ln\left(\frac{s+1}{s-1}\right) - 4 \cdot \phi_\text{t} \left(\frac{r_{\text{c1}}}{s+1} + \frac{r_{\text{c2}}}{s-1}\right); \qquad V_1 < V_2 \tag{3.53}$$

where

$$s = 1 + \frac{2 \cdot r_{\text{c2}}}{W(v_2)}; \qquad V_1 < V_2 \tag{3.54}$$

and

$$v_2 = \frac{r_{c2} t_{si}}{2 \cdot L_{di}} \exp\left(\frac{V_2 - V_c}{2 \cdot \phi_t}\right); \qquad V_1 < V_2 \tag{3.55}$$

The advantage of using the Lambert W function is that its defining transcendental equation (3.48) is well-conditioned and efficient procedures for numerical as well as analytical evaluation are readily available [79, 80]. For example, the condition $\lim_{V_1 \to V_2} V_{cr} = \infty$ established above from the physical consideration corresponds to $\lim_{V_1 \to V_2} s = \infty$. Since $W(v)$ is analytic at $v = 0$ numerical evaluation of the case $V_1 \approx V_2$ represents no particular difficulty. Comparison of the two methods of evaluating the partition lines on the V_1-V_2 plane is shown in Fig. 3.3 for $t_{ox1} = t_{ox2}$ and in Fig. 3.4 for $t_{ox1} \neq t_{ox2}$ respectively. As expected a perfect agreement is obtained between the numerical solution of (3.43)-(3.46) and the explicit solution given by (3.52) and (3.53). To show the dependence of the boundary lines on the silicon film thickness, we plot them in Fig. 3.5 for $t_{si} = 10$ nm with the same gate oxide thickness as in Fig. 3.4.

3.6 A New Solution Technique for the IVEs

Originally, for both the trigonometric and hyperbolic cases, the IVEs were formulated as two coupled equations with two unknown variables as shown earlier [75]. A single IVE that is solved with respect to only one of the surface potentials was derived in [77]. Depending on the device parameters and gate voltages V_{g1} and V_{g2} this IVE can take four different forms: (i) $V_1 > V_2$, hyperbolic, (ii) $V_1 \geq V_2$, trigonometric, (iii) $V_1 < V_2$, trigonometric, and (iv) $V_1 < V_2$, hyperbolic. The appropriate functional form of the IVE can be selected analytically as shown in Fig. 3.6, where explicit equations for the boundaries Γ_1 and Γ_2 are described in the previous section [78] and Γ_3 corresponds to $V_1 = V_2$. However, the resulting IVE in [77] was solved using computationally expensive numerical optimization techniques. A better conditioned single IVE is obtained here by changing the variable in the IVE of [77] from ψ_{s1} to

$$\xi_1 = \left[\frac{C_{ox1}\left(V_1 - \psi_{s1}\right)}{C_f \phi_t}\right]^2 \exp\left(\frac{V_c - \psi_{s1}}{\phi_t}\right), \tag{3.56}$$

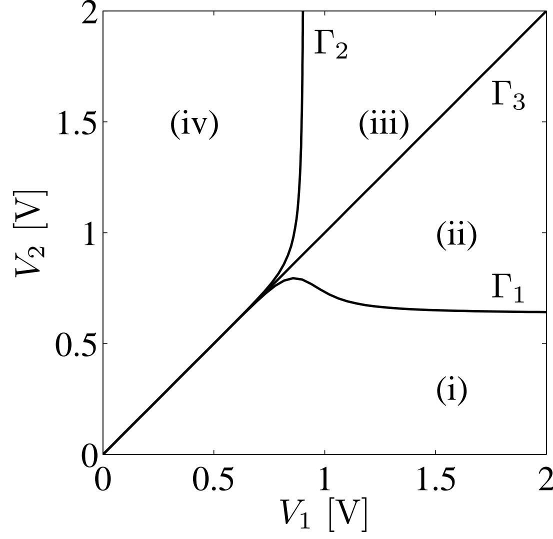


Figure 3.6: Regions of operation on the $V_1 - V_2$ plane for $V_c = 0.5$ V, $t_{si} = 10$ nm, $t_{ox1} = 2$ nm and $t_{ox2} = 20$ nm.

where $C_f = \epsilon_{si}/L_{di}$. For region (i) in Fig. 3.6 this gives an implicit $\xi_1(V_1, V_2, V_c)$ dependence [81]

$$W\left(b_1\sqrt{\xi_1}\right)\left[1 + r\coth(\varphi_1)\sqrt{\frac{\xi_1 - 1}{\xi_1}}\right] + \ln\left[\frac{\sinh(\varphi_1)}{\sqrt{\xi_1 - 1}}\right] + \frac{(V_2 - V_1)}{2\cdot\phi_t} = 0 \qquad (3.57)$$

where

$$\varphi_1 = \sqrt{\frac{\xi_1 - 1}{\xi_1}}\cdot\frac{W\left(b_1\sqrt{\xi_1}\right)}{r_{c1}} + \sinh^{-1}\sqrt{\xi_1 - 1}, \qquad (3.58)$$

$$b_1 = \frac{C_f}{2\cdot C_{ox1}}\exp\left(\frac{V_1 - V_c}{2\cdot\phi_t}\right), \qquad (3.59)$$

$r = C_{ox1}/C_{ox2}$, $r_{cj} = C_{si}/C_{oxj}$, and W is the Lambert-W function. The IVE for the trigonometric case of region (ii) in Fig. 3.6 becomes

$$W\left(b_1\sqrt{\xi_1}\right)\left[1 + r\cot(\varphi_1)\sqrt{\frac{1 - \xi_1}{\xi_1}}\right] + \ln\left[\frac{\sin(\varphi_1)}{\sqrt{1 - \xi_1}}\right] + \frac{V_2 - V_1}{2\cdot\phi_t} = 0, \qquad (3.60)$$

where now

$$\varphi_1 = \sqrt{\frac{1 - \xi_1}{\xi_1}}\cdot\frac{W\left(b_1\sqrt{\xi_1}\right)}{r_{c1}} + \sin^{-1}\sqrt{1 - \xi_1}. \qquad (3.61)$$

IVEs for regions (iii) and (iv) have a similar form. For the hyperbolic case it can be seen that $\xi_1 \geq 1$ and for the trigonometric case $0 < \xi_1 \leq 1$. While the IVEs

(3.57) and (3.60) are mathematically equivalent to those in [77], the well-defined range of ξ_1 allows the Newton-Raphson method to be used directly for solution, without any need for preliminary numerical optimization.

However, during numerical iteration of the trigonometric IVE for some bias conditions ξ_1 can cause $\varphi_1 = \pi$ which creates a problem when evaluating $\cot\varphi_1$ in (3.60). We overcome this problem by selecting the initial range of ξ_1 to be between ξ_π and 1 where ξ_π is found from (3.61) by setting $\varphi_1(\xi_\pi) = \pi$. This also avoids encountering closely located unphysical multiple roots of the IVE between 0 and ξ_π produced by oscillations of $\cot\varphi_1$ in (3.60). Note that (3.57) is equivalent to (3.60) for $\xi_1 \to 1$ i.e. at the boundary between the trigonometric and the hyperbolic IVE forms [78].

The surface potential ψ_{s1} for region (i) is obtained from (3.56) as

$$\psi_{\mathrm{s1}} = V_1 - 2 \cdot \phi_{\mathrm{t}} W\left(b_1\sqrt{\xi_1}\right) \tag{3.62}$$

and the surface potential ψ_{s2} is given by [77]

$$\psi_{\mathrm{s2}} = \psi_{\mathrm{s1}} - 2 \cdot \phi_t \ln\left[\frac{\sinh(\varphi_1)}{\sqrt{\xi_1 - 1}}\right]. \tag{3.63}$$

Traditionally, independent-gate asymmetric DG-FinFET models are formulated in terms of the integration constants α and θ [75, 78] which are also used in expressions for the drain current and terminal charges. They are related to ξ_1 for region (i) as follows

$$\theta = \frac{1}{2 \cdot r_{\mathrm{c1}}}\sqrt{\frac{\xi_1 - 1}{\xi_1}} \cdot W\left(b_1\sqrt{\xi_1}\right) \tag{3.64}$$

and

$$\alpha = \theta + \sinh^{-1}\sqrt{\xi_1 - 1}. \tag{3.65}$$

For region (ii) we replace $\xi_1 - 1$ by $1 - \xi_1$ and $\sinh^{-1}\sqrt{\xi_1 - 1}$ by $\sin^{-1}\sqrt{1 - \xi_1}$ in (3.63)-(3.65).

Chapter 4

CURRENT and CHARGE MODELS for the COMMON-GATE SYMMETRIC DG-FinFET

4.1 Introduction

An exact core model of undoped multi-gate MOSFETs has been developed in [60, 62, 75, 82] for the common-gate symmetric DG-FinFET and in [83, 84] for the SGFET. In both cases one obtains closed-form equations for the drain current I_{d}, but the situation with the terminal charges is different. For the common-gate symmetric DG-FinFET, the charges are obtained as quadratures that require numerical evaluation [75] while exact closed-form expressions for the charges in the SGFET case [84] are somewhat more complex than is customary in compact models. The second problem is that exact core SGFET and common-gate symmetric DG-FinFET models are significantly different, which is disadvantageous for the purpose of realistic compact model development that may require simultaneous inclusion of both models to describe complex geometries and corner effects [85]. The final problem is that the complexity of the exact multi-gate MOSFET core models is not conducive to the inclusion of small-geometry effects (e.g. velocity saturation) and does not allow one to directly use the experience (and code) gained in the development of advanced bulk and SOI MOSFET models.

Significant progress towards the resolution of the three problems outlined above has been made in [56, 57] and [82]. In [56, 57] the current equation of the exact core model of [60, 75] has been reformulated and then simplified so that the resulting expressions for the drain current and charges take a form identical to that used in PSP [45]. This allowed incorporation of small-geometry effects leading to a relatively complete model of symmetric undoped DG-FinFETs that was found to be in good agreement with both TCAD simulations and experimental data. The price for the simplicity and the convenience of this approach is a significant difference (about 20% for current and 4% for transcapacitances) between the simplified [56, 57]

and the exact core models [60, 75]. This difference was absorbed by the parameters included in the model. A different approach to simplifying the exact core model has been introduced in [82]. Starting with the simplified input voltage equation simple analytical expressions were obtained for the drain current and terminal charges. One important accomplishment of the approximate theory developed in [82] is that with a proper mapping, the same equations describe symmetric undoped common-gate symmetric DG-FinFETs and SGFETs. The accuracy of the approximations made in [82] is exactly the same as in [56, 57].

Another approximate core model of symmetric DG-FinFETs has been developed in [86]. Similarly to [82] this was accomplished by simplifying the input voltage equation and as in [57] the result was brought in a form compatible with one of the advanced bulk MOSFET models (EKV) simplifying the inclusion of small-geometry effects [87].

In this work we continue the effort to make the DG-FinFET model as similar as possible to the PSP bulk MOSFET model [45]. For this purpose we first show that despite the different starting points and seemingly different formulation in [57] and [82] both approximations are identical. The origin of error in the charge-sheet approximation is discussed. We then significantly improve the accuracy of this approach while still keeping the equations of the approximate core model in a form nearly identical to that of the PSP model as suggested in [57]. This is accomplished by extending the symmetric linearization technique to not assume the charge-sheet approximation that is used in the bulk MOSFET case [88, 89].

4.2 Exact Drain Current

We start with the drift and diffusion formulation of the drain current:

$$I_{\mathrm{d}} = q\mu h_{\mathrm{f}} \int_0^{t_{\mathrm{si}}} \left(n\frac{\partial\psi}{\partial y} - \phi_{\mathrm{t}}\frac{\partial n}{\partial y} \right) \mathrm{d}x. \tag{4.1}$$

where μ is the electron mobility and h_f is the fin height. Using identity

$$n\frac{\partial \psi}{\partial y} - \phi_\mathrm{t}\frac{\partial n}{\partial y} = n\frac{\partial V_\mathrm{c}}{\partial y} \tag{4.2}$$

and the fact that in a device with the geometry shown in Fig. 2.3a, $V_\mathrm{c} = V_\mathrm{c}(y)$ (4.1) becomes

$$I_\mathrm{d} = 2 \cdot \mu h_\mathrm{f} q_\mathrm{n} \frac{\mathrm{d}V_\mathrm{c}}{\mathrm{d}y} \tag{4.3}$$

where

$$q_\mathrm{n} = q \int_0^{t_\mathrm{si}/2} n(x, y)\ \mathrm{d}x \tag{4.4}$$

is the absolute value of electron charge density per unit area per channel expressed in terms of ψ_s and θ in (2.62) and (2.63), respectively. Integrating (4.4) from source to drain yields

$$I_\mathrm{d} = 2 \cdot \mu \frac{h_\mathrm{f}}{L} \int_0^L q_\mathrm{n} \mathrm{d}V_\mathrm{c}. \tag{4.5}$$

Changing the variable of integration in (4.5) from V_c to θ gives [60]

$$I_\mathrm{d} = 2 \cdot \mu \frac{h_\mathrm{f}}{L} \int_{\theta_\mathrm{s}}^{\theta_\mathrm{d}} q_\mathrm{n} \frac{\mathrm{d}V_\mathrm{c}}{\mathrm{d}\theta}\ \mathrm{d}\theta \tag{4.6}$$

where θ_s and θ_d are the values of θ at source and drain end, respectively. From (2.61)

$$\frac{\mathrm{d}V_\mathrm{c}}{\mathrm{d}\theta} = -2 \cdot \phi_\mathrm{t} \left[\frac{1}{\theta} + (1 + 2 \cdot r_\mathrm{c}) \tan\theta + \frac{2 \cdot r_\mathrm{c}\theta}{\cos^2\theta}\right]. \tag{4.7}$$

Substituting (2.63) and (4.7) in (4.6) the drain current becomes [60]

$$I_\mathrm{d} = 16 \cdot \mu \frac{h_\mathrm{f}}{L} C_\mathrm{si} \phi_\mathrm{t}^2 \left(r q_\mathrm{i}^2 + q_\mathrm{i} - \frac{\theta^2}{2}\right)\Bigg|_{\theta_\mathrm{d}}^{\theta_\mathrm{s}} \tag{4.8}$$

where $q_\mathrm{i} = \theta \tan\theta$ is the normalized inversion charge density. The values of θ_s and θ_d are determined from (2.65) and (2.59) by setting $V_\mathrm{c} = V_\mathrm{s}$ and $V_\mathrm{c} = V_\mathrm{d}$, respectively.

4.3 Charge-Sheet Approximation

Applying Brews charge-sheet approximation [90] to the DG-FinFET [67, 57] we get

$$I_\mathrm{d} = 2 \cdot \mu h_\mathrm{f} \left(q_\mathrm{n} \frac{\mathrm{d}\psi_\mathrm{s}}{\mathrm{d}y} - \phi_\mathrm{t} \frac{\mathrm{d}q_\mathrm{n}}{\mathrm{d}y}\right). \tag{4.9}$$

Substituting for q_n from (2.62) in (4.9) yields

$$I_d = 2 \cdot \mu h_f C_{ox} \left[(V_{gs} - \Delta\phi - \psi_s) + \phi_t \right] \frac{d\psi_s}{dy}. \tag{4.10}$$

Integrating (4.10) from the source end to drain end of the channel the drain current becomes

$$I_d = 2 \cdot \mu \frac{h_f}{L} C_{ox} \left[(V_{gs} - \Delta\phi - \psi_{sm}) + \phi_t \right] \Delta\psi \tag{4.11}$$

where

$$\Delta\psi = \psi_{sd} - \psi_{ss} \tag{4.12}$$

is the total variation of surface potential along the channel,

$$\psi_{sm} = \frac{1}{2}(\psi_{ss} + \psi_{sd}) \tag{4.13}$$

is the surface potential midpoint and ψ_{ss} and ψ_{sd} are the surface potential at the source end and the drain end of the channel, respectively. Fig. 4.1 shows the percentage error introduced by the charge sheet charge sheet approximation (4.11) when compared to the exact equation (4.8). In [82] an equivalent form of (4.11) is derived

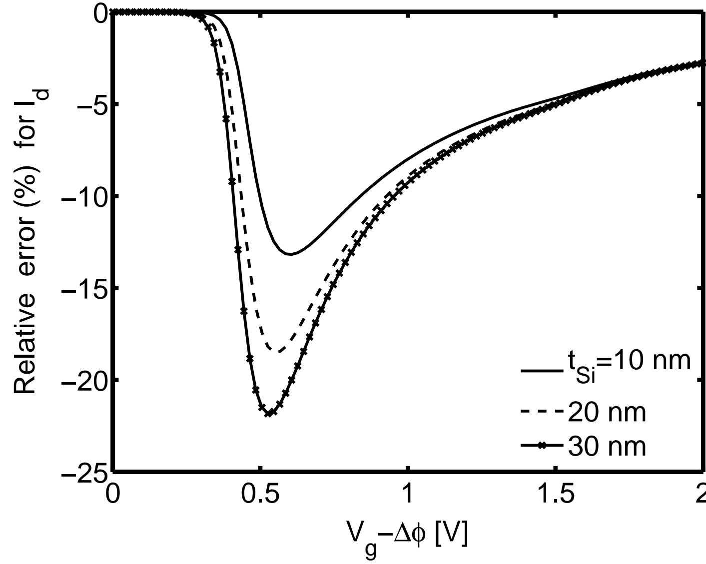


Figure 4.1: Relative error for drain current I_d using expression (4.11); $t_{ox} = 1.5$ nm, $T = 300$ K, $V_{ds} = 1$ V.

by approximating the IVE as

$$\frac{\ln q_{\mathrm{i}}}{2} + 2 \cdot r_{\mathrm{c}} q_{\mathrm{i}} \approx \frac{V_{\mathrm{g}} - \Delta\phi - V_{\mathrm{c}}}{2 \cdot \phi_{\mathrm{t}}} - \ln\left(\frac{4 \cdot L_{\mathrm{di}}}{t_{\mathrm{si}}}\right) \tag{4.14}$$

to give

$$I_{\mathrm{d}} = 16 \cdot \mu \frac{h_{\mathrm{f}}}{L} C_{\mathrm{si}} \phi_{\mathrm{t}}^2 \left(\frac{q_{\mathrm{i}}}{2} + r_{\mathrm{c}} q_{\mathrm{i}}^2\right)\Bigg|_{q_{\mathrm{id}}}^{q_{\mathrm{is}}} \tag{4.15}$$

Using (2.62) and (2.63) in (4.15) it can be shown that although (4.11) and (4.15) originate from seemingly different approximations, they are equal [67]. These approximation were used in [82] and [57] to derive closed form expression for terminal charges which had error of 4% compared to exact results. In Section 4.5 we propose a more accurate terminal charge model based on the symmetric linearization method.

To gain further insight into the origin of the significant error for I_{d} associated with expressions (4.11) or (4.15) we reformulate the exact expression for the drain current [60]. This reformulation is later used in extending the symmetric linearization method. Following [57] (4.1) can be written as

$$I_{\mathrm{d}} = 2 \cdot \mu h_{\mathrm{f}} \left(\tilde{q}_{\mathrm{n}} \frac{\mathrm{d}\psi_{\mathrm{s}}}{\mathrm{d}y} - \phi_{\mathrm{t}} \frac{\mathrm{d}q_{\mathrm{n}}}{\mathrm{d}y}\right) \tag{4.16}$$

where

$$\tilde{q}_{\mathrm{n}} = \frac{q \int_0^{t_{\mathrm{si}}/2} n \frac{\partial \psi}{\partial y} \mathrm{d}x}{\frac{\mathrm{d}\psi_{\mathrm{s}}}{\mathrm{d}y}} \tag{4.17}$$

As shown in Appendix D $\tilde{q}_{\mathrm{n}}$ can be written as [57, 67]

$$\tilde{q}_{\mathrm{n}} = \left(1 + \frac{g}{4 \cdot r_{\mathrm{c}}}\right) q_{\mathrm{n}} \tag{4.18}$$

where

$$g = \frac{\sin(2 \cdot \theta) - 2 \cdot \theta \cos(2 \cdot \theta)}{\theta \tan\theta [2 \cdot \theta + \sin(2 \cdot \theta)]} \tag{4.19}$$

Physically, the difference between q_{n} and $\tilde{q}_{\mathrm{n}}$ accounts for the fact that, generally speaking, current flow in DG-FinFETs is not confined to a narrow surface channel and approximation (4.9) is not always accurate. In Fig 4.2 we plot g as a function of θ where θ varies from 0 (weak inversion) to $\pi/2$ (strong inversion). It can be seen that

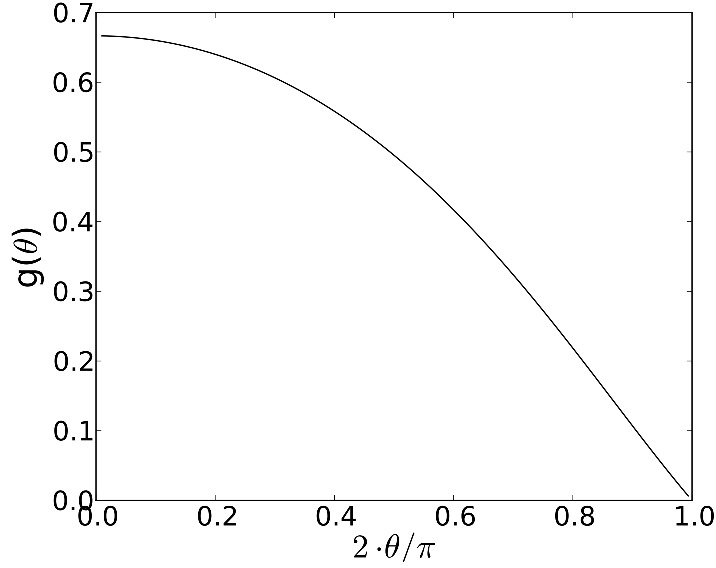


Figure 4.2: $g(\theta)$ versus θ.

in strong inversion g approaches zero and the second term in parentheses in (4.18) can be neglected which results in high accuracy of the charge sheet approximation. In the weak inversion even with the highest value of g neglecting it does not result in significant error in drain current as the diffusion term in (4.9) is dominant. However, in the moderate inversion g has a significant value and since both drift and diffusion terms in (4.9) contribute to current, neglecting g introduces significant error in drain current [57]. Integrating (4.16) from the source end to the drain end of the channel yields

$$I_{\mathrm{d}} = 2 \cdot \mu \, \frac{h_{\mathrm{f}}}{L} \left[\int_{\psi_{\mathrm{ss}}}^{\psi_{\mathrm{sd}}} \tilde{q}_{\mathrm{n}} \mathrm{d}\psi_{\mathrm{s}} + \phi_{\mathrm{t}}(q_{\mathrm{ns}} - q_{\mathrm{nd}}) \right]. \tag{4.20}$$

Reformulating (4.20)

$$I_{\mathrm{d}} = 2 \cdot \mu \, \frac{h_{\mathrm{f}}}{L} \left[k \int_{\psi_{\mathrm{ss}}}^{\psi_{\mathrm{sd}}} q_{\mathrm{n}} \mathrm{d}\psi_{\mathrm{s}} + \phi_{\mathrm{t}}(q_{\mathrm{ns}} - q_{\mathrm{nd}}) \right] \tag{4.21}$$

where

$$k = \frac{\int\limits_{\psi_{\mathrm{ss}}}^{\psi_{\mathrm{sd}}} \tilde{q}_{\mathrm{n}} \mathrm{d}\psi_{\mathrm{s}}}{\int\limits_{\psi_{ss}}^{\psi_{sd}} q_{\mathrm{n}} \mathrm{d}\psi_{\mathrm{s}}} \tag{4.22}$$

or

$$k = 1 + \frac{g_0}{4 \cdot r_{\mathrm{c}}} \tag{4.23}$$

and

$$g_0 = \frac{\int\limits_{\psi_{\mathrm{ss}}}^{\psi_{\mathrm{sd}}} g q_{\mathrm{n}} \mathrm{d}\psi_{\mathrm{s}}}{\int\limits_{\psi_{\mathrm{ss}}}^{\psi_{\mathrm{sd}}} q_{\mathrm{n}} \mathrm{d}\psi_{\mathrm{s}}} \tag{4.24}$$

is a bias-dependent but position-independent variable. From (2.62) we have $dq_{\mathrm{n}}/d\psi_{\mathrm{s}} = -C_{\mathrm{ox}}$ and (4.21) becomes

$$I_{\mathrm{d}} = 16 \cdot \mu \; \frac{h_{\mathrm{f}}}{L} C_{\mathrm{si}} \; \phi_{\mathrm{t}}^2 \left(k r_{\mathrm{c}} q_{\mathrm{i}}^2 + \frac{q_{\mathrm{i}}}{2} \right) \Bigg|_{q_{\mathrm{id}}}^{q_{\mathrm{is}}} \tag{4.25}$$

The value of k can be obtained by direct integration in (4.22) or more conveniently by comparison with the exact result (4.8). Comparison of (4.8) with (4.25) yields

$$k r_{\mathrm{c}} q_{\mathrm{i}}^2 + \frac{q_{\mathrm{i}}}{2} \Bigg|_{q_{\mathrm{id}}}^{q_{\mathrm{is}}} = r_{\mathrm{c}} q_{\mathrm{i}}^2 + q_{\mathrm{i}} - \frac{\theta^2}{2} \Bigg|_{\theta_{\mathrm{d}}}^{\theta_{\mathrm{s}}} \tag{4.26}$$

or

$$g_0 = \frac{2}{q_{\mathrm{is}} + q_{\mathrm{id}}} \left(1 - \frac{\theta_{\mathrm{s}}^2 - \theta_{\mathrm{d}}^2}{q_{\mathrm{is}} - q_{\mathrm{id}}} \right) \tag{4.27}$$

With g_0 given by (4.27) and k by (4.23) expression (4.25) is exact and is just one of many possible reformulations of (4.8). Clearly the approximations made in [57] and [82] are equivalent to setting $k = 1$ i.e. $g_0 = 0$ instead of using the exact expression (4.23). For further reference we note that (4.25) can be also written as

$$I_{\mathrm{d}} = 2 \cdot \mu \; \frac{h_{\mathrm{f}}}{L} \; C_{\mathrm{ox}} \left(k q_{\mathrm{nm}} + \phi_{\mathrm{t}} \right) \Delta\psi \tag{4.28}$$

or in PSP form

$$I_{\mathrm{d}} = 2 \cdot \mu C_{\mathrm{ox}} \frac{h_{\mathrm{f}}}{L} [q_{\mathrm{nm}} + \phi_{\mathrm{t}} + \phi_{\mathrm{t}} \left(1 - g_1 \right)] \Delta\psi, \tag{4.29}$$

where

$$g_1 = \frac{\theta_{\rm s}^2 - \theta_{\rm d}^2}{q_{\rm is} - q_{\rm id}}, \tag{4.30}$$

and

$$q_{\rm nm} = q_{\rm n}|_{\psi_{\rm s}=\psi_{\rm sm}} \tag{4.31}$$

denotes the voltage drop across gate oxide (in the inversion condition) at the surface potential midpoint. The term $\phi_{\rm t}(1 - g_1)$ in (4.29) may be called a non-charge-sheet term and if neglected it results in the drain current under the charge-sheet approximation.

4.4 Symmetric Linearization Method

Introduction of a position-independent k is sufficient to compute $I_{\rm d}$ but not the position dependence of the surface potential required to compute the terminal charges. The latter involves evaluation of the derivative ${\rm d}y/{\rm d}\psi_{\rm s}$ using (4.16) which can be written as [57]

$$I_{\rm d} = 2 \cdot \mu\ h_{\rm f}\ (\tilde{q}_{\rm n} + C_{\rm ox}\ \phi_{\rm t})\frac{{\rm d}\psi_{\rm s}}{{\rm d}y} \tag{4.32}$$

where we used (2.62). In order to obtain compact closed form expressions for $\psi_{\rm s}(y)$ and terminal charges some approximation is required. The simplest possible approximation is $\tilde{q}_{\rm n} = q_{\rm n}$ [57] which leads to the approximate expressions for $Q_{\rm G}$, $Q_{\rm S}$, and $Q_{\rm D}$ developed in [57, 82]. A more accurate approximation is

$$\tilde{q}_{\rm n} = C_{\rm ox}(\nu - \alpha_{\rm l}\ u) \tag{4.33}$$

where

$$u = \psi_{\rm s} - \psi_{\rm sm} \tag{4.34}$$

and variables ν and $\alpha_{\rm l}$ are position independent (they, of course, are functions of the terminal voltages). This approximation represents linearization of $\tilde{q}_{\rm n}$ as a function of surface potential. The value of the coefficients ν and $\alpha_{\rm l}$ can be selected in more than one way. A natural choice is

$$\nu = \frac{\tilde{q}_{\rm nm}}{C_{\rm ox}} \tag{4.35}$$

and

$$\alpha_{\mathrm{l}} = -\frac{1}{C_{\mathrm{ox}}} \left(\frac{\mathrm{d}\tilde{q}_{\mathrm{n}}}{\mathrm{d}\psi_{\mathrm{s}}} \right) \bigg|_{\psi_{\mathrm{s}}=\psi_{\mathrm{sm}}} \tag{4.36}$$

where $\tilde{q}_{\mathrm{nm}}$ denotes the value of $\tilde{q}_{\mathrm{n}}$ at the point where $\psi_{\mathrm{s}} = \psi_{\mathrm{sm}}$. Since, however, a simple expression for $\tilde{q}_{\mathrm{nm}}$ is unavailable, we consider a different choice. From (4.32) and (4.33) we find

$$I_{\mathrm{d}} = 2 \cdot \mu \ h_{\mathrm{f}} \ C_{\mathrm{ox}} \left(\nu + \phi_{\mathrm{t}} - \alpha_{\mathrm{l}} \ u \right) \frac{\mathrm{d}u}{\mathrm{d}y} \tag{4.37}$$

and after integration along the channel

$$I_{\mathrm{d}} = 2 \cdot \mu \ \frac{h_{\mathrm{f}}}{L} \ C_{\mathrm{ox}}(\nu + \phi_{\mathrm{t}})\Delta\psi. \tag{4.38}$$

By comparison with (4.28) it follows that by selecting

$$\nu = k \ q_{\mathrm{nm}} \tag{4.39}$$

we assure that expression (4.38) is exact. The difference between two choices of ν is further discussed in Appendix E where we compare the commonality and differences for the symmetric linearization method as applied to bulk MOSFETs and DG-FinFETs.

From (4.36) the expression for linearization coefficient α_{l} becomes

$$\alpha_{\mathrm{l}} = -\frac{1}{C_{\mathrm{ox}}} \frac{\mathrm{d}}{\mathrm{d}\psi_{\mathrm{s}}} \left[q_{\mathrm{n}} \left(1 + \frac{g}{4r_{\mathrm{c}}} \right) \right] \bigg|_{\psi_{\mathrm{s}}=\psi_{\mathrm{sm}}} \tag{4.40}$$

which is approximated as [67, 63]

$$\alpha_{\mathrm{l}} \approx 1 + \frac{3 \cdot (3 + 2q_{\mathrm{im}})}{8 \cdot r_{\mathrm{c}}(2 + q_{\mathrm{im}})^3} \tag{4.41}$$

where

$$q_{\mathrm{im}} = q_{\mathrm{i}}|_{\psi_{\mathrm{s}}=\psi_{\mathrm{sm}}} = \frac{1}{2}(q_{\mathrm{is}} + q_{\mathrm{id}}) \tag{4.42}$$

The derivation of (4.41) is presented in Appendix D.

With ν and α_{l} established, the terminal charges are obtained as follows. From (4.37) and (4.38)

$$\frac{\mathrm{d}y}{\mathrm{d}u} = \frac{L(H-u)}{H\Delta\psi} \tag{4.43}$$

where

$$H = \frac{\nu + \phi_{\mathrm{t}}}{\alpha_{\mathrm{l}}} = \frac{kq_{\mathrm{nm}} + \phi_{\mathrm{t}}}{\alpha_{\mathrm{l}}} \tag{4.44}$$

After integration of (4.43)

$$y = y_{\mathrm{m}} + \frac{Lu}{\Delta\psi}\left(1 - \frac{u}{2\cdot H}\right) \tag{4.45}$$

where

$$y_{\mathrm{m}} = \frac{L}{2}\left(1 + \frac{\Delta\psi}{4\cdot H}\right) \tag{4.46}$$

gives the position of the "surface potential midpoint", i.e. the point where $\psi_{\mathrm{s}} = \psi_{\mathrm{sm}}$. An explicit form of the $\psi_{\mathrm{s}}(y)$ dependence follows (4.45):

$$\psi_{\mathrm{s}}(y) = \psi_{\mathrm{sm}} + H\left[1 - \sqrt{1 - \left(\frac{2\cdot\Delta\psi}{HL}\right)(y - y_{\mathrm{m}})}\right] \tag{4.47}$$

Expressions (4.43)-(4.46) are exactly the same as for bulk MOSFETs [44, 45, 88, 89] except for the different value of H. The high accuracy of the explicit expression (4.47) for the position dependence of the surface potential is illustrated in Fig. 4.3 where it is compared with the exact result for $\psi_{\mathrm{s}}(y)$ that can be presented in parametric form [60]

$$\psi_{\mathrm{s}}(\theta) = V_{\mathrm{g}} - \Delta\phi - 4\cdot r_{\mathrm{c}}\phi_{\mathrm{t}}\theta\tan\theta \tag{4.48}$$

and

$$\frac{y(\theta)}{L} = \frac{F(\theta_{\mathrm{s}}) - F(\theta)}{F(\theta_{\mathrm{s}}) - F(\theta_{\mathrm{d}})} \tag{4.49}$$

where

$$F(\theta) = \theta\tan\theta - \frac{\theta^2}{2} + r_{\mathrm{c}}\theta^2\tan^2\theta. \tag{4.50}$$

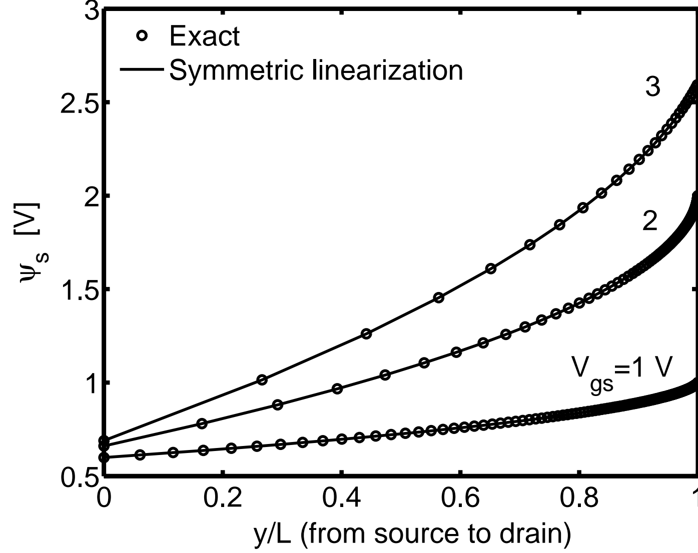


Figure 4.3: Position dependence of surface potential in DG-FinFET; $t_{\mathrm{ox}} = 1.5$ nm, $t_{\mathrm{si}} = 20$ nm, and $V_{\mathrm{ds}} = 2$ V.

Now the gate charge for bulk DG-FinFETs becomes

$$Q_{\mathrm{G}} = h_{\mathrm{f}} \int_{0}^{L} q_{\mathrm{g}} \mathrm{d}y = 2 \cdot h_{\mathrm{f}} C_{\mathrm{ox}} \int_{-\Delta\psi/2}^{\Delta\psi/2} (V_{\mathrm{oxm}} - u) \frac{\mathrm{d}y}{\mathrm{d}u} \mathrm{d}u \tag{4.51}$$

which with reference to (4.43) leads to a closed form expression

$$Q_{\mathrm{G}} = 2 \cdot C_{\mathrm{ox}} h_{\mathrm{f}} L \left(V_{\mathrm{oxm}} + \frac{\Delta\psi^2}{12 \cdot H} \right) \tag{4.52}$$

where

$$V_{\mathrm{oxm}} = (V_{\mathrm{g}} - \Delta\phi - \psi_{\mathrm{sm}}) \tag{4.53}$$

is the potential across gate oxide at surface potential midpoint. The total drain charge using the Ward-Dutton partition scheme [91] is given by

$$Q_{\mathrm{D}} = -2 \cdot h_{\mathrm{f}} \int_{0}^{\mathrm{L}} q_{\mathrm{n}} \frac{y}{L} \mathrm{d}y = -2 \cdot C_{\mathrm{ox}} h_{\mathrm{f}} \int_{-\Delta\psi/2}^{\Delta\psi/2} (q_{\mathrm{nm}} - u) \frac{y}{L} \frac{\mathrm{d}y}{\mathrm{d}u} \mathrm{d}u. \tag{4.54}$$

Substituting (4.43), (4.45) in (4.54) and integrating yields

$$Q_{\mathrm{D}} = -2 \cdot C_{\mathrm{ox}} h_{\mathrm{f}} L \left[\frac{q_{\mathrm{nm}}}{2} - \frac{\Delta\psi}{12} \left(1 - \frac{\Delta\psi}{2 \cdot H} - \frac{\Delta\psi^2}{20 \cdot H^2} \right) \right]. \tag{4.55}$$

Similarly, the total source charge is

$$Q_{\mathrm{S}} = -2 \cdot C_{\mathrm{ox}} h_{\mathrm{f}} L \left[\frac{q_{\mathrm{nm}}}{2} + \frac{\Delta\psi}{12} \left(1 + \frac{\Delta\psi}{2 \cdot H} - \frac{\Delta\psi^2}{20 \cdot H^2} \right) \right]. \tag{4.56}$$

The bulk FinFET body charge follows from the neutrality condition $Q_{\mathrm{B}} = -(Q_{\mathrm{G}} + Q_{\mathrm{D}} + Q_{\mathrm{S}})$. For SOI FinFETs expressions for Q_{S} and Q_{D} remain the same but in (4.52) we change V_{oxm} to q_{nm} to assure the Q_{G} (and hence C_{gg}, C_{bg}) becomes negligible in accumulation ($\psi_{\mathrm{ss}} < 5\phi_{\mathrm{t}}$). A subtle point here which is not needed to be included in the compact model formulation of SOI FinFETs is that in the steady state, Q_{G} can become appreciable due to the leakage of minority carriers from the n^+ contacts provided that the device is not switched for prolonged periods of time. But this build-up of Q_{G} is extremely slow and hence has no consequences for small-signal behavior even at low frequency [cf. TCAD simulations in Fig. 2.2a].

Three dimensional (3D) TCAD simulations are performed for both bulk and SOI DG-FinFETs. Both the electron and hole continuity equations are included in the simulations. The device channel length is kept sufficiently large to reduce small geometry and fringe capacitances effects. The simulated device structure parameters are $L = 1$ μm, $h_{\mathrm{f}} = 0.2$ μm, $t_{\mathrm{ox}} = 2$ nm, $t_{\mathrm{si}} = 10$ nm and $\Delta\phi = 0$ V. The carrier mobility is kept constant and equal to the mobility in intrinsic silicon.

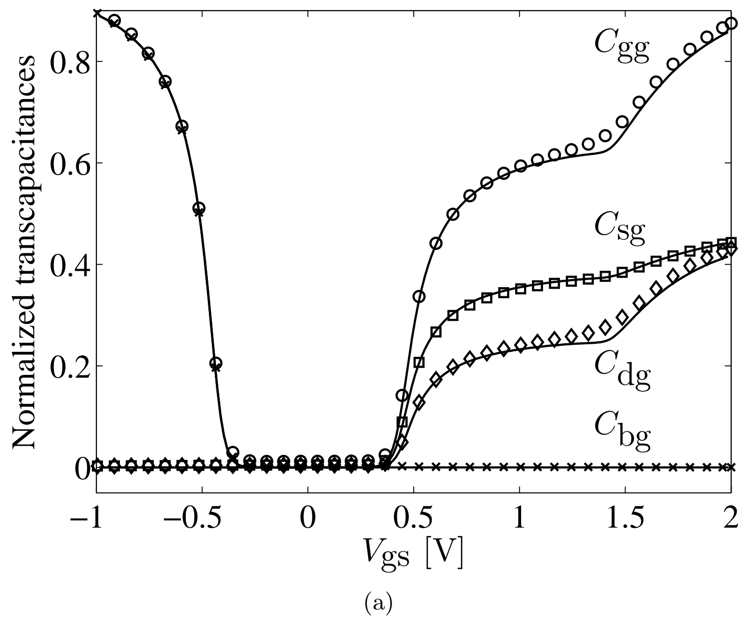
While the implementation of modern compact transistor models in SPICE-like circuit simulators is charge-based, in order to preserve the charge conservation [92], it is often convenient to perform model verification in terms of capacitances.

$$C_{nm} = (2 \cdot \delta_{nm} - 1) \frac{\partial Q_m}{\partial V_n} \tag{4.57}$$

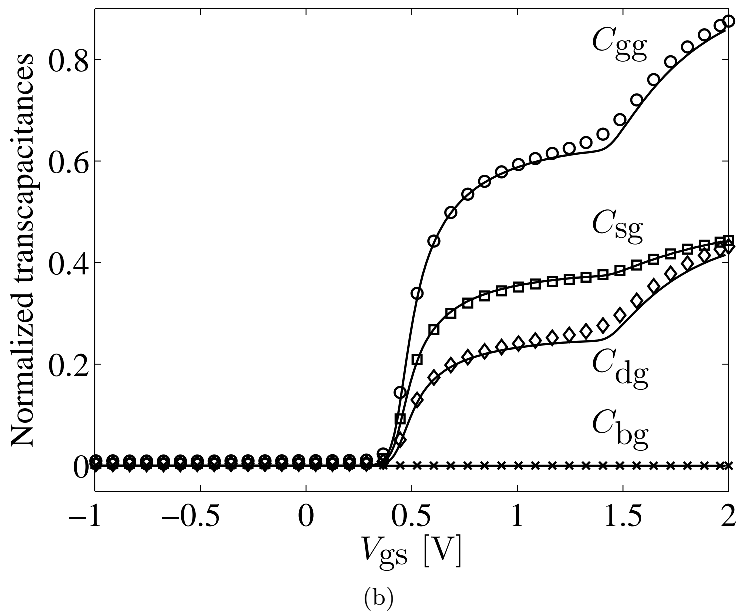
where m, n label the terminals of the device and δ_{nm} is Kronecker's delta. Indeed, any error in the expressions for the terminal charges Q_m is amplified while evaluating the derivatives $\partial Q_m / \partial V_n$. For this reason we present a comparison of the charge model with numerically computed results both in terms of charges and transcapacitances.

Figs. 4.4a and 4.4b compare the capacitances obtained from the 3D TCAD simulations and the compact model for bulk and SOI FinFETs, respectively. The model accurately reproduces the transcapacitance behavior in all regions of operation including accumulation.

Expressions (4.38), (4.52), (4.55) and (4.56) represent a form of the symmetric linearization method applied to common-gate symmetric DG-FinFETs. Unlike the simpler formulation in [57], the result is exact for the drain current and as shown in Fig. 4.5 significantly reduces the error for the terminal charges. Similarly, it provides a better accuracy for the transcapacitances (cf. Fig. 4.6a and 4.6b). An important feature of the new approximations for Q_{G} and Q_{D} is that they are extremely simple, have the same form as in SP [44] and PSP [45] and differ only by using different expression for H. This means that incorporation of small geometry effects can proceed in the same manner as in [56, 57] which already had been shown sufficiently accurate in terms of both TCAD simulations and experimental data. The expressions for Q_{G} and Q_{D} given in [57, 82] can be obtained from (4.52) and (4.55) by setting $\tilde{q}_{\mathrm{n}} = q_{\mathrm{n}}$. Indeed, this implies $k = 1$, $\nu = V_{\mathrm{oxm}}$ and $\alpha_{\mathrm{l}} = 1$. Then by (4.44) $H = V_{\mathrm{oxm}} + \phi_{\mathrm{t}}$ and (4.52) and (4.55) revert to the charge sheet version of terminal charge expressions found in [57, 82].



(a)



(b)

Figure 4.4: Normalized transcapacitances of (a) bulk FinFET and (b) SOI FinFET versus gate voltage for $V_{ds} = 1$V. Symbols represents TCAD simulations results and the lines corresponds to a compact model.

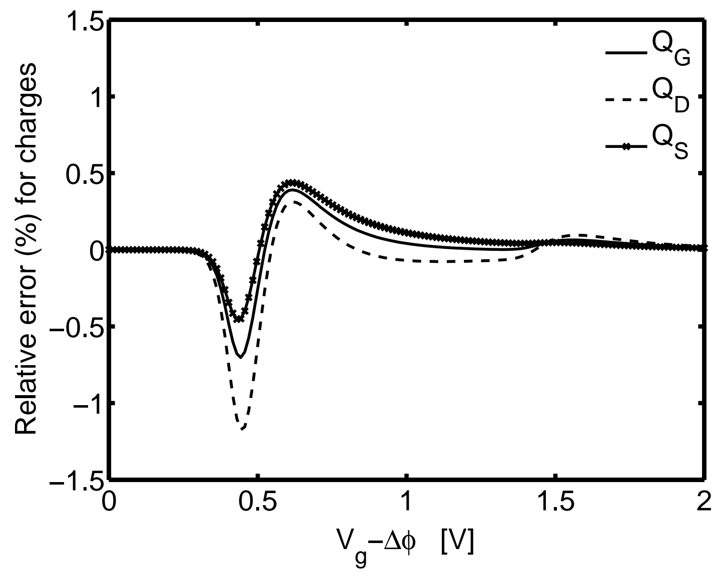
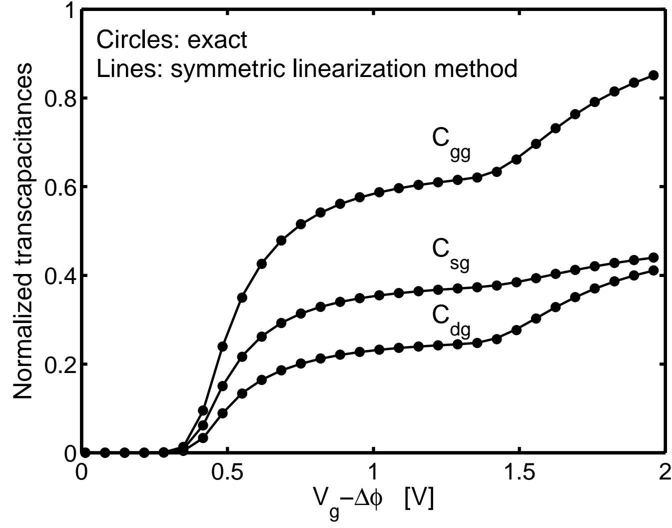
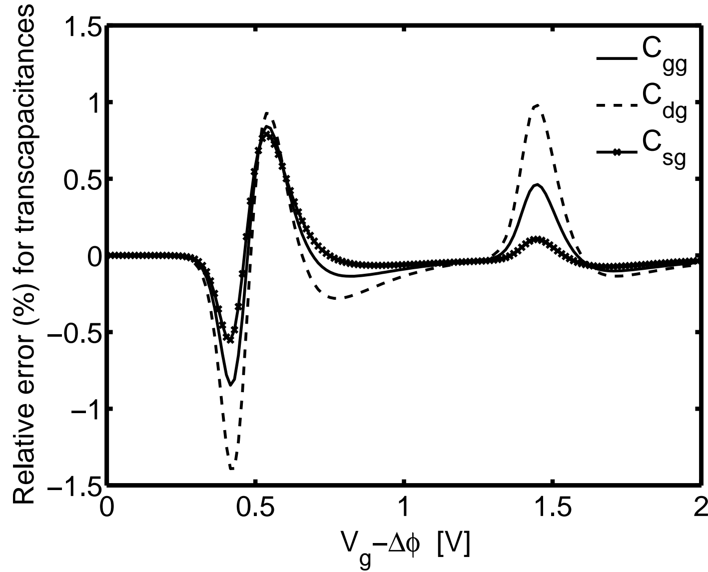


Figure 4.5: Relative error for the terminal charges, using symmetric linearization method for DG-FinFET; $t_{\mathrm{si}} = 20$ nm, $t_{\mathrm{ox}} = 1.5$ nm, $T = 300$ K, $V_{\mathrm{ds}} = 1$ V.



(a)



(b)

Figure 4.6: Plots of (a) transcapacitance and (b) relative error for the transcapacitances, using symmetric linearization method for DG-FinFET; $t_{\mathrm{si}} = 20$ nm, $t_{\mathrm{ox}} = 1.5$ nm, $T = 300$ K, $V_{\mathrm{ds}} = 1$ V.

With reference to Fig. 4.7 the drain current for SGFET

$$I_{\mathrm{d}} = \int J \mathrm{d}A \tag{4.58}$$

where the integral is taken across the area in the direction perpendicular to the current flow (i.e. $\mathrm{d}A = 2 \cdot \pi\rho \mathrm{d}\rho$). The current density

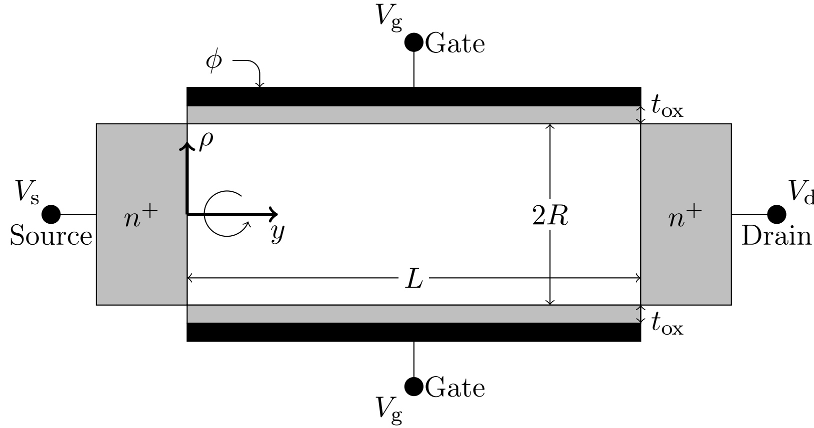


Figure 4.7: Cross-section of the SGFET.

$$J = q\mu \left(n \frac{\partial \psi}{\partial y} - \phi_{\mathrm{t}} \frac{\partial n}{\partial y} \right) \tag{4.59}$$

Hence

$$I_{\mathrm{d}} = \mu \left(\tilde{q}_{\mathrm{n}} \frac{\mathrm{d}\psi_{\mathrm{s}}}{\mathrm{d}y} - \phi_{\mathrm{t}} \frac{\mathrm{d}q_{\mathrm{n}}}{\mathrm{d}y} \right) \tag{4.60}$$

where

$$q_{\mathrm{n}} = q \int n \mathrm{d}A \tag{4.61}$$

is the absolute value of the inversion charge per unit channel length and

$$\tilde{q}_{\mathrm{n}} = \frac{q}{\frac{\mathrm{d}\psi_{\mathrm{s}}}{\mathrm{d}y}} \int n \frac{\partial \psi}{\partial y} \mathrm{d}A. \tag{4.62}$$

Just as for the DG-FinFET the difference between $\tilde{q}_{\mathrm{n}}$ and q_{n} accounts for the fact that, generally speaking, current density is not concentrated near the Si-SiO$_2$ interface.

Integrating along the y direction yields

$$I_{\mathrm{d}} = \frac{\mu}{L}\left[k\int\limits_{\psi_{\mathrm{ss}}}^{\psi_{\mathrm{sd}}} q_{\mathrm{n}}\mathrm{d}\psi_{\mathrm{s}} + \phi_{\mathrm{t}}(q_{\mathrm{gs}} - q_{\mathrm{gd}})\right] \tag{4.63}$$

where formally k is given by the same expression (4.23) as for DG-FinFET.

For SGFETs (cf. Fig. 4.7)

$$\frac{\mathrm{d}q_{\mathrm{n}}}{\mathrm{d}\psi_{\mathrm{s}}} = -2\cdot\pi RC_{\mathrm{ox}} \tag{4.64}$$

where

$$C_{\mathrm{ox}} = \frac{\epsilon_{\mathrm{ox}}}{R\ln\left(1+\frac{t_{\mathrm{ox}}}{R}\right)}. \tag{4.65}$$

It follows that

$$I_{\mathrm{d}} = \frac{\mu}{L}\left(\frac{kq_{\mathrm{n}}^2}{4\cdot\pi RC_{\mathrm{ox}}} + \phi_{\mathrm{t}}q_{\mathrm{n}}\right)\Bigg|_{q_{\mathrm{nd}}}^{q_{\mathrm{ns}}}. \tag{4.66}$$

For SGFETs it is convenient to define the variable θ as [84]

$$\theta = 1 - \left(\frac{R}{4\cdot L_{\mathrm{di}}}\right)^2 \exp\left(\frac{\psi_0 - V_{\mathrm{c}}}{\phi_{\mathrm{t}}}\right) \tag{4.67}$$

where ψ_0 denotes the potential at the center of the device. Then

$$q_{\mathrm{n}} = 8\cdot\pi\phi_{\mathrm{t}}\epsilon_{\mathrm{si}}q_{\mathrm{i}} \tag{4.68}$$

where the normalized gate charge per unit length is

$$q_{\mathrm{i}} = \frac{1-\theta}{\theta}. \tag{4.69}$$

From (4.66)

$$I_{\mathrm{d}} = \frac{8\cdot\pi\mu\epsilon_{\mathrm{si}}\phi_{\mathrm{t}}^2}{L}\left(ksq_{\mathrm{i}}^2 + q_{\mathrm{i}}\right)\Big|_{q_{\mathrm{id}}}^{q_{\mathrm{is}}} \tag{4.70}$$

where

$$s = \frac{2\epsilon_{\mathrm{si}}}{\epsilon_{\mathrm{ox}}}\ln\left(1+\frac{t_{\mathrm{ox}}}{R}\right). \tag{4.71}$$

Comparing this with exact result [83, 84]

$$I_{\mathrm{d}} = \frac{8\cdot\pi\mu\epsilon_{\mathrm{si}}\phi_t^2}{L}\left[\frac{s}{\theta^2} + \frac{2\cdot(1-s)}{\theta} + \ln\theta\right]\Bigg|_{\theta_{\mathrm{d}}}^{\theta_{\mathrm{s}}} \tag{4.72}$$

we find

$$k = 1 + \frac{\frac{1}{\theta_{\mathrm{s}}} - \frac{1}{\theta_{\mathrm{d}}} + \ln\left(\frac{\theta_{\mathrm{s}}}{\theta_{\mathrm{d}}}\right)}{s\left(\frac{1}{\theta_{\mathrm{s}}^2} - \frac{1}{\theta_{\mathrm{d}}^2} + \frac{2}{\theta_{\mathrm{d}}} - \frac{2}{\theta_{\mathrm{s}}}\right)}. \tag{4.73}$$

With this selection of k, (4.70) represents a reformulation of (4.72) conducive to the development of the symmetric linearization method. The approximate expression in [82] follows from (4.70) by setting $k = 1$, i.e. $\tilde{q}_{\mathrm{n}} = q_{\mathrm{n}}$ just as in the case of DG-FinFET considered in Section 4.3.

To introduce symmetric linearization and account for $\tilde{q}_{\mathrm{n}} \neq q_{\mathrm{n}}$we note that

$$\frac{\mathrm{d}q_{\mathrm{n}}}{\mathrm{d}y} = -2 \cdot \pi R C_{\mathrm{ox}} \frac{\mathrm{d}\psi_{\mathrm{s}}}{\mathrm{d}y} \tag{4.74}$$

and set

$$I_{\mathrm{d}} = \mu \left(\tilde{q}_{\mathrm{n}} + 2 \cdot \pi R C_{\mathrm{ox}} \phi_{\mathrm{t}}\right) \frac{\mathrm{d}\psi_{\mathrm{s}}}{\mathrm{d}y}. \tag{4.75}$$

Linearization of $\tilde{q}_{\mathrm{n}}$ as a function of ψ_{s} yields

$$\tilde{q}_{\mathrm{n}} = 2 \cdot \pi R C_{\mathrm{ox}} (\nu - \alpha_{\mathrm{l}} u). \tag{4.76}$$

where u is defined as in (4.34) and the variables ν, α_{l} are yet to be determined. From (4.75) and (4.76)

$$I_{\mathrm{d}} = 2 \cdot \pi \mu R C_{\mathrm{ox}} (\nu + \phi_{\mathrm{t}} - \alpha_{\mathrm{l}} u) \frac{\mathrm{d}u}{\mathrm{d}y}. \tag{4.77}$$

In particular,

$$I_{\mathrm{d}} = \mu \frac{2 \cdot \pi R}{L} C_{\mathrm{ox}} (\nu + \phi_{\mathrm{t}}) \Delta\psi. \tag{4.78}$$

According to (4.72) in order for this expression to be exact

$$2 \cdot (\nu + \phi_{\mathrm{t}}) \Delta\psi = 4 \cdot s \phi_{\mathrm{t}}^2 \left[\frac{s}{\theta^2} + \frac{2 \cdot (1 - s)}{\theta} + \ln\theta\right]\Bigg|_{\theta_{\mathrm{d}}}^{\theta_{\mathrm{s}}}. \tag{4.79}$$

This yields ν. The coefficient α_{l} is selected as

$$\alpha_{\mathrm{l}} = \frac{\tilde{q}_{\mathrm{is}} - \tilde{q}_{\mathrm{id}}}{C_{\mathrm{ox}} \Delta\psi} \approx k \tag{4.80}$$

where the approximation is based on $\tilde{q}_{\mathrm{is}} \approx k q_{\mathrm{is}}$ and $\tilde{q}_{\mathrm{id}} \approx k q_{\mathrm{id}}$. The final justification of the selected approximations for ν and α_{l} for both DG-FinFET and SGFET is by comparison with the exact expressions for terminal charges and transcapacitances.

From (4.77), (4.78)

$$\frac{\mathrm{d}y}{\mathrm{d}u} = \frac{2 \cdot \pi R C_{\mathrm{ox}} \alpha_{\mathrm{l}} (H - u)}{I_{\mathrm{d}}} \tag{4.81}$$

and

$$I_{\mathrm{d}} = \frac{2 \cdot \pi R}{L} \mu C_{\mathrm{ox}} \alpha_{\mathrm{l}} H \Delta\psi \tag{4.82}$$

where

$$H = \frac{\nu + \phi_{\mathrm{t}}}{\alpha_{\mathrm{l}}}. \tag{4.83}$$

This yields (4.45) and after integration one concludes that (4.52), (4.54), and (4.55) apply also to SGFET, after changing h_{f} into πR. The only difference with DG-FinFET or bulk MOSFET is in the expressions for ν and H. Comparison with the exact results for SGFETs is shown in Fig. 4.8 for charges and in Fig. 4.9 for transcapacitances. In all cases the accuracy is better than 2% while expression (4.78) for the drain current is exact.

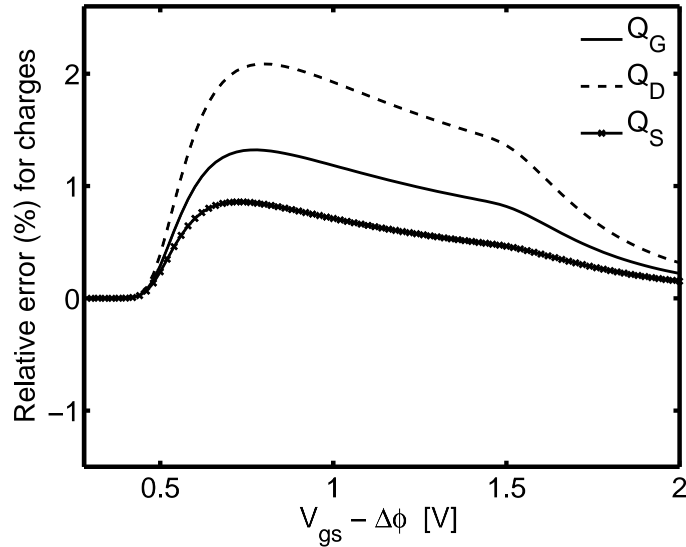
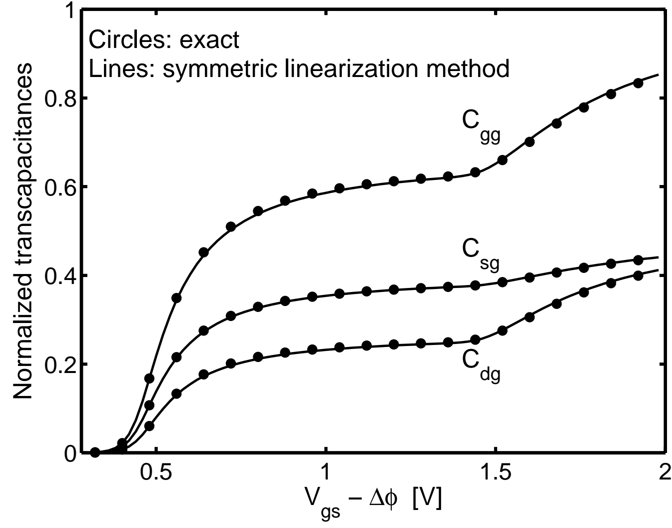
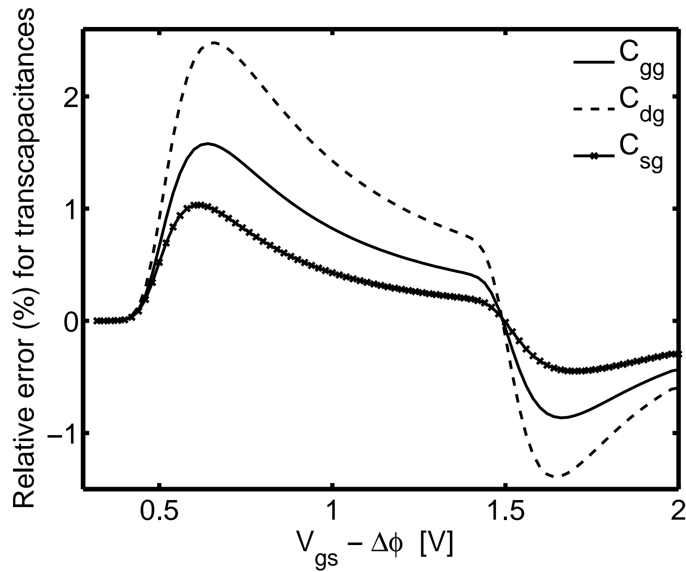


Figure 4.8: Relative error for the terminal charges, using symmetric linearization method for SGFET; $R = 8$ nm, $t_{\mathrm{ox}} = 1.5$ nm, $T = 300$ K, $V_{\mathrm{ds}} = 1$ V.



(a)



(b)

Figure 4.9: Plots of (a) transcapacitances and (b) relative error for the transcapacitances, using symmetric linearization method for SGFET; $R = 8$ nm, $t_{\mathrm{ox}} = 1.5$ nm, $T = 300$ K, $V_{\mathrm{ds}} = 1$ V.

Chapter 5

CURRENT and CHARGE MODELS for the INDEPENDENT-GATE ASYMMETRIC DG-FinFET

5.1 Drain Current Model

In this section the drain current expression for the independent-gate asymmetric DG-FinFET is derived following the approach of [76] and extended to include biasing for which $V_1 < V_2$. The drain current expression (4.5) for common-gate symmetric DG-FinFETs can be used for independent-gate asymmetric DG-FinFETs:

$$I_\mathrm{d} = -\mu \frac{h_\mathrm{f}}{L} \int_{V_\mathrm{s}}^{V_\mathrm{d}} Q_\mathrm{n} \mathrm{d}V_\mathrm{c}. \tag{5.1}$$

Note that in (4.5) q_n is the absolute value of inversion charge density per channel whereas in (5.1) Q_n is the total inversion charge density. The IVE and Q_n for the independent-gate asymmetric DG-FinFET can have trigonometric or hyperbolic form depending on the device parameters and applied bias as discussed in Section 3.1. As V_c varies along the channel from V_s at the source to V_d at the drain the form of IVE and Q_n may or may not change along the channel. Depending on the form of IVE at the source end and the drain end of the channel there are three different cases:

Case I: In this case we have trigonometric form of IVE throughout the channel (i.e. $V_\mathrm{s} \leq V_\mathrm{d} \leq V_\mathrm{cr}$).

Case II: In this case we have hyperbolic form of IVE throughout the channel (i.e. $V_\mathrm{cr} \leq V_\mathrm{s} \leq V_\mathrm{d}$).

Case III: In this case we have trigonometric form of IVE at the source end and the hyperbolic form of IVE at the drain end of the channel (i.e. $V_\mathrm{s} \leq V_\mathrm{cr} \leq V_\mathrm{d}$).

Case I ($V_\mathrm{s} \leq V_\mathrm{d} \leq V_\mathrm{cr}$): For this case we have the trigonometric solution for $\psi(x)$ throughout the channel. Substituting for the inversion charge density from (3.21) in

(5.1) we have

$$I_{\rm d} = 8 \cdot \mu \frac{h_{\rm f}}{L} C_{\rm si} \phi_{\rm t}^2 \left. (J_+ - J_-) \right|_{\rm s}^{\rm d} \tag{5.2}$$

where

$$J_\pm = -\frac{1}{2 \cdot \phi_{\rm t}} \int \theta \cot(\alpha \pm \theta) {\rm d}V_{\rm c}. \tag{5.3}$$

and the limits of integration s and d correspond to values of $(J_+ - J_-)$ at the source and the drain end of the channel, respectively. From (3.18)

$$\frac{{\rm d}V_{\rm c}}{2 \cdot \phi_{\rm t}} = -{\rm d} \ln \left[\frac{\theta}{\sin(\alpha - \theta)} \right] - 2 \cdot r_{\rm c1} {\rm d}[\theta \cot(\alpha - \theta)]. \tag{5.4}$$

Substituting (5.4) in (5.3) and integrating we have

$$J_- = \theta \cot(\alpha - \theta) + r_{\rm c1} \theta^2 \cot^2(\alpha - \theta) - \frac{\theta^2}{2} + \int \theta {\rm d}\alpha. \tag{5.5}$$

To evaluate J_+ we use (3.19) which gives

$$\frac{{\rm d}V_{\rm c}}{2 \cdot \phi_{\rm t}} = -{\rm d} \ln \left[\frac{\theta}{\sin(\alpha + \theta)} \right] + 2 \cdot r_{\rm c2} {\rm d}[\theta \cot(\alpha + \theta)]. \tag{5.6}$$

Substituting (5.6) in (5.3) and integrating yields

$$J_+ = \theta \cot(\alpha + \theta) - r_{\rm c2} \theta^2 \cot^2(\alpha + \theta) + \frac{\theta^2}{2} + \int \theta {\rm d}\alpha. \tag{5.7}$$

From (5.2), (5.5), and (5.7) we have the expression for the drain current

$$I_{\rm d} = 8 \cdot \mu \frac{h_{\rm f}}{L} C_{\rm si} \phi_{\rm t}^2 (f_{\rm d} - f_{\rm s}) \tag{5.8}$$

where $f_{\rm d}$ and $f_{\rm s}$ are values of

$$f = \theta^2 \left[1 - r_{\rm c1} \cot^2(\alpha - \theta) - r_{\rm c2} \cot^2(\alpha + \theta) \right] + \theta \left[\cot(\alpha + \theta) - \cot(\alpha - \theta) \right] \tag{5.9}$$

at the source and the drain end of the channel, respectively. It may be mentioned that since $\psi(x)$ for a common-gate symmetric DG-FinFET has trigonometric form irrespective of $V_{\rm c}$ its drain current can be shown to be a special case of (5.8) (cf. Appendix G).

Case II ($V_{\mathrm{cr}} \leq V_{\mathrm{s}} \leq V_{\mathrm{d}}$): For this case we have a hyperbolic solution for $\psi(x)$ throughout the channel. Substituting for the inversion charge density from (3.38) in (5.1) yields

$$I_{\mathrm{d}} = 8 \cdot \mu \frac{h_{\mathrm{f}}}{L} C_{\mathrm{si}} \phi_{\mathrm{t}}^2 \left. (J_+^* - J_-^*) \right|_{\mathrm{s}}^{\mathrm{d}} \tag{5.10}$$

where

$$J_{\pm}^* = -\frac{\sigma}{2 \cdot \phi_{\mathrm{t}}} \int \theta_* \coth(\alpha_* \pm \theta_*) \mathrm{d}V_{\mathrm{c}}. \tag{5.11}$$

and the limits of integration s and d correspond to values of $(J_+^* - J_-^*)$ at the source and the drain end of the channel, respectively. From the IVE (3.35) we have

$$\frac{\mathrm{d}V_{\mathrm{c}}}{2 \cdot \phi_{\mathrm{t}}} = -\mathrm{d} \ln \left[\frac{\theta_*}{\sinh{(\alpha_* - \sigma\theta_*)}} \right] - 2 \cdot \sigma r_{\mathrm{c1}} \mathrm{d}[\theta_* \coth{(\alpha_* - \sigma\theta_*)}]. \tag{5.12}$$

Substituting (5.12) in (5.11) and integrating yields

$$J_-^* = \sigma\theta_* \coth(\alpha_* - \sigma\theta_*) + r_{\mathrm{c1}} \theta_*^2 \coth^2(\alpha_* - \sigma\theta_*) + \frac{\theta_*^2}{2} - \sigma \int \theta_* \mathrm{d}\alpha_*. \tag{5.13}$$

To evaluate J_+^* we use the IVE (3.36) which gives

$$\frac{\mathrm{d}V_c}{2 \cdot \phi_{\mathrm{t}}} = -\mathrm{d} \ln \left[\frac{\theta_*}{\sinh{(\alpha_* + \sigma\theta_*)}} \right] + 2 \cdot \sigma r_{\mathrm{c2}} \mathrm{d}[\theta_* \coth{(\alpha_* + \sigma\theta_*)}]. \tag{5.14}$$

Substituting (5.14) in (5.11) and integrating yields

$$J_+^* = \sigma\theta_* \cosh(\alpha_* + \sigma\theta_*) - r_{\mathrm{c2}} \theta_*^2 \coth^2(\alpha_* + \sigma\theta_*) - \frac{\theta_*^2}{2} - \sigma \int \theta_* \mathrm{d}\alpha_*. \tag{5.15}$$

From (5.10), (5.13), and (5.15) we get drain current

$$I_{\mathrm{d}} = 8 \cdot \mu \frac{h_{\mathrm{f}}}{L} C_{\mathrm{si}} \phi_{\mathrm{t}}^2 (f_{\mathrm{d}}^* - f_{\mathrm{s}}^*) \tag{5.16}$$

where f_{d}^* and f_{s}^* are values of

$$f^* = -\theta_*^2 \left[1 + r_{\mathrm{c1}} \coth^2(\alpha_* - \sigma\theta_*) + r_{\mathrm{c2}} \coth^2(\alpha_* + \sigma\theta_*) \right] - \sigma\theta_* [\coth(\alpha_* - \sigma\theta_*) - \coth(\alpha_* + \sigma\theta_*)] \tag{5.17}$$

at the source and the drain end of the channel, respectively.

Case III ($V_{\mathrm{s}} \leq V_{\mathrm{cr}} \leq V_{\mathrm{d}}$): The drain current for this case becomes

$$I_{\mathrm{d}} = 8 \cdot \mu \frac{h_{\mathrm{f}}}{L} C_{\mathrm{si}} \phi_{\mathrm{t}}^2 \left[f_{\mathrm{d}}^* - f_{\mathrm{cr}}^* + f_{\mathrm{cr}} - f_{\mathrm{s}} \right] \tag{5.18}$$

where f^*_{cr} and f_{cr} are the respective values of f^* and f at the critical channel potential $V_{\mathrm{c}} = V_{\mathrm{cr}}$ within the channel. Since at $V_{\mathrm{c}} = V_{\mathrm{cr}}$, $\alpha = \alpha_* = \theta = \theta_* = 0$ when $V_1 > V_2$ and $\pi - \alpha = \alpha_* = \theta = \theta_* = 0$ when $V_1 < V_2$ it can be seen that $-f^*_{\mathrm{cr}} + f_{\mathrm{cr}} = 0$ and (5.18) becomes

$$I_{\mathrm{d}} = 8 \cdot \mu \frac{h_{\mathrm{f}}}{L} C_{\mathrm{si}} \phi_{\mathrm{t}}^2 \left[f^*_{\mathrm{d}} - f_{\mathrm{s}} \right] \tag{5.19}$$

5.2 Reformulation of Drain Current in PSP Form

In this section we reformulate the drain current expressions given in Section 5.1 in PSP form to facilitate the inclusion of small geometry effects in a form similar to that of the PSP compact model [44, 45]. This reformulation also helps to independently model gate-1 and gate-2 field dependent mobilities.

Case I ($V_{\mathrm{s}} \leq V_{\mathrm{d}} \leq V_{\mathrm{cr}}$):

Denoting

$$f_1 = -\theta \cot(\alpha - \theta) - r_{\mathrm{c1}} \theta^2 \cot^2(\alpha - \theta) + \frac{\theta^2}{2} \tag{5.20}$$

and

$$f_2 = \theta \cot(\alpha + \theta) - r_{\mathrm{c2}} \theta^2 \cot^2(\alpha + \theta) + \frac{\theta^2}{2} \tag{5.21}$$

the drain current expression (5.8) becomes

$$I_{\mathrm{d}} = I_{\mathrm{d1}} + I_{\mathrm{d2}} \tag{5.22}$$

where

$$I_{\mathrm{d1}} = 8 \cdot \mu \frac{h_{\mathrm{f}}}{L} C_{\mathrm{si}} \phi_{\mathrm{t}}^2 (f_{\mathrm{1d}} - f_{\mathrm{1s}}) \tag{5.23}$$

and

$$I_{\mathrm{d2}} = 8 \cdot \mu \frac{h_{\mathrm{f}}}{L} C_{\mathrm{si}} \phi_{\mathrm{t}}^2 (f_{\mathrm{2d}} - f_{\mathrm{2s}}). \tag{5.24}$$

The s and d in the subscript of f_1 and f_2 indicates their value at the source and the drain ends of the channel, respectively. Substituting for f_{1d} and f_{1s} and noting from (3.15)

$$4 \cdot \phi_{\mathrm{t}} r_{\mathrm{c1}} \theta \cot(\alpha - \theta) = V_1 - \psi_{\mathrm{s1}} \tag{5.25}$$

(5.23) becomes

$$I_{\rm d1} = \mu \frac{h_{\rm f}}{L} C_{\rm ox1} \left[V_{\rm ox1m} + \phi_{\rm t} + \phi_{\rm t} \left(1 - g_1\right)\right] \Delta\psi_1 \tag{5.26}$$

where

$$g_1 = \frac{\theta_{\rm s}^2 - \theta_{\rm d}^2}{q_{\rm gn1s} - q_{\rm gn1d}}, \tag{5.27}$$

$$q_{\rm gn1s} = \theta_{\rm s} \cot(\alpha_{\rm s} - \theta_{\rm s}), \tag{5.28}$$

and

$$q_{\rm gn1d} = \theta_{\rm d} \cot(\alpha_{\rm d} - \theta_{\rm d}). \tag{5.29}$$

Physically $q_{\rm gn1s}$ and $q_{\rm gn1d}$ are the normalized gate-1 charge density at the source and the drain end of the channel, respectively. Similarly, substituting for $f_{\rm 2d}$ and $f_{\rm 2s}$ and noting that from (3.17)

$$4 \cdot \phi_{\rm t} r_{\rm c2} \theta \cot(\alpha + \theta) = -(V_2 - \psi_2) \tag{5.30}$$

(5.24) becomes

$$I_{\rm d2} = \mu \frac{h_{\rm f}}{L} C_{\rm ox2} \left[V_{\rm ox2m} + \phi_{\rm t} + \phi_{\rm t} \left(1 - g_2\right)\right] \Delta\psi_2 \tag{5.31}$$

where

$$g_2 = \frac{\theta_{\rm s}^2 - \theta_{\rm d}^2}{q_{\rm gn2s} - q_{\rm gn2d}}, \tag{5.32}$$

$$q_{\rm gn2s} = -\theta_{\rm s} \cot(\alpha_{\rm s} + \theta_{\rm s}), \tag{5.33}$$

and

$$q_{\rm gn2d} = -\theta_{\rm d} \cot(\alpha_{\rm d} + \theta_{\rm d}). \tag{5.34}$$

The $q_{\rm gn2s}$ and $q_{\rm gn2d}$ are the normalized gate-2 charge density at the source and the drain end of the channel, respectively.

Case II ($V_{\rm cr} \leq V_{\rm s} \leq V_{\rm d}$):

For this case we denote

$$f_1^* = -\sigma\theta_* \coth(\alpha_* - \sigma\theta_*) - r_{\rm c1}\theta_*^2 \coth^2(\alpha_* - \sigma\theta_*) - \frac{\theta_*^2}{2} \tag{5.35}$$

and

$$f_2^* = \sigma\theta_* \coth(\alpha_* + \sigma\theta_*) - r_{c2}\theta_*^2 \coth^2(\alpha_* + \sigma\theta_*) - \frac{\theta_*^2}{2} \tag{5.36}$$

then the drain current expression (5.16) becomes

$$I_\mathrm{d} = I_\mathrm{d1}^* + I_\mathrm{d2}^* \tag{5.37}$$

where

$$I_\mathrm{d1}^* = 8 \cdot \mu \frac{h_\mathrm{f}}{L} C_\mathrm{si} \phi_\mathrm{t}^2 (f_\mathrm{1d}^* - f_\mathrm{1s}^*) \tag{5.38}$$

and

$$I_\mathrm{d2}^* = 8 \cdot \mu \frac{h_\mathrm{f}}{L} C_\mathrm{si} \phi_\mathrm{t}^2 (f_\mathrm{2d}^* - f_\mathrm{2s}^*). \tag{5.39}$$

The s and d in the subscript of f_1^* and f_2^* indicates their value at the source and the drain ends of the channel, respectively. Substituting for f_1d and f_1s and noting that

$$4 \cdot \sigma\phi_\mathrm{t} r_\mathrm{c1} \theta \coth(\alpha - \sigma\theta) = V_1 - \psi_\mathrm{s1} \tag{5.40}$$

and $\sigma^2 = 1$ (5.38) takes a form similar to (5.26) where now

$$g_1 = \frac{-\theta_\mathrm{*s}^2 + \theta_\mathrm{*d}^2}{q_\mathrm{gn1s} - q_\mathrm{gn1d}} \tag{5.41}$$

$$q_\mathrm{gn1s} = \sigma\theta_\mathrm{*s} \cot(\alpha_\mathrm{*s} - \sigma\theta_\mathrm{*s}) \tag{5.42}$$

and

$$q_\mathrm{gn1d} = \sigma\theta_\mathrm{*d} \cot(\alpha_\mathrm{*d} - \sigma\theta_\mathrm{*d}). \tag{5.43}$$

Similarly, I_d2^* for this case is given by (5.31) with

$$g_2 = \frac{-\theta_\mathrm{*s}^2 + \theta_\mathrm{*d}^2}{q_\mathrm{gn2s} - q_\mathrm{gn2d}}, \tag{5.44}$$

$$q_\mathrm{gn2s} = -\sigma\theta_\mathrm{*s} \coth(\alpha_\mathrm{*s} + \sigma\theta_\mathrm{*s}), \tag{5.45}$$

and

$$q_\mathrm{gn2d} = -\sigma\theta_\mathrm{*d} \coth(\alpha_\mathrm{*d} + \sigma\theta_\mathrm{*d}). \tag{5.46}$$

For Case III where we have trigonometric solution at source end of the channel and hyperbolic solution at drain end of the channel (5.26) and (5.31) still apply provided now g_1 and g_2 are given as

$$g_1 = \frac{\theta_{\mathrm{s}}^2 + \theta_{*\mathrm{d}}^2}{q_{\mathrm{gn1s}} - q_{\mathrm{gn1d}}} \tag{5.47}$$

and

$$g_2 = \frac{\theta_{\mathrm{s}}^2 + \theta_{*\mathrm{d}}^2}{q_{\mathrm{gn2s}} - q_{\mathrm{gn2d}}}. \tag{5.48}$$

where q_{gn1s}, q_{gn1d}, q_{gn2s} and q_{gn2d} are given by (5.28), (5.43), (5.33), and (5.46) respectively.

Separation of the drain current into I_{d1} and I_{d2} components facilitates independent modeling of gate-1 and gate-2 field dependent mobility by replacing μ in I_{d1} and I_{d2} with μ_1 and μ_2, respectively, where μ_1 is gate-1 field dependent mobility and μ_2 is gate-2 field dependent mobility.

5.3 Effective Gate Charge Density Concept

The objective in this section is to present the drain current equation in a form that looks as simple as the charge-sheet approximation but does not really use it. This can be accomplished rigorously by introducing the concept of effective charge density. While the true charge density is a linear function of the surface potential, the effective charge density is not. However, this reformulation of the drift-diffusion equation allows one to use the powerful symmetric linearization method developed in [88, 89] that forms the theoretical foundation of the popular PSP model [45]. In particular, symmetric linearization of the effective charge density leads to closed-form expressions for the terminal charges which are almost identical to those used in PSP. This approach has been already successfully implemented for the special case of common-gate symmetric DG-FinFETs [67].

An alternative view of what is done in this and the next section is that we develop symmetric linearization of the difference between the actual channel

current and its charge sheet approximation. By doing so we are able to obtain simple analytical expressions for the terminal charges without relying on the charge-sheet approximation.

We start with the drain current expression including drift and diffusion components

$$I_{\mathrm{d}} = q\mu h_{\mathrm{f}} \int\limits_{-t_{\mathrm{si}}/2}^{t_{\mathrm{si}}/2} \left(n\frac{\partial \psi}{\partial y} - \phi_{\mathrm{t}} \frac{\partial n}{\partial y} \right) \mathrm{d}x \tag{5.49}$$

For any choice of x_{d} we have

$$I_{\mathrm{d}} = I_1 + I_2 \tag{5.50}$$

where

$$I_1 = \mu h_{\mathrm{f}} \left\{ q \int\limits_{-t_{\mathrm{si}}/2}^{x_{\mathrm{d}}} \left(n\frac{\partial \psi}{\partial y} - \phi_{\mathrm{t}} \frac{\partial n}{\partial y} \right) \mathrm{d}x + \epsilon_{\mathrm{si}} E_{\mathrm{x}}(x_{\mathrm{d}}) \frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}y} \right\} \tag{5.51}$$

and

$$I_2 = \mu h_{\mathrm{f}} \left\{ q \int\limits_{x_{\mathrm{d}}}^{t_{\mathrm{si}}/2} \left(n\frac{\partial \psi}{\partial y} - \phi_{\mathrm{t}} \frac{\partial n}{\partial y} \right) \mathrm{d}x - \epsilon_{\mathrm{si}} E_{\mathrm{x}}(x_{\mathrm{d}}) \frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}y} \right\}. \tag{5.52}$$

For the trigonometric case, it is convenient to select x_{d} at the point where the x-component of electric field, E_{x}, goes to zero (in this case the last term in (5.51) and (5.52) is zero). This requires that $x_{\mathrm{d}} = x_{\mathrm{d}}(y)$ be position-dependent. However, an explicit expression for x_{d} does not enter the final expressions of the model developed below due to the fact that last term in the curly braces of (5.51) and (5.52) cancels with the values of integrals in (5.51) and (5.52) at the limit $x = x_{\mathrm{d}}$, respectively. For the hyperbolic case we set $x_{\mathrm{d}} = \sigma \cdot \infty$ [1]. This requires that the expressions for n and ψ as functions of x be extended from the physical range $(-t_{\mathrm{si}}/2, t_{\mathrm{si}}/2)$ to the interval $(-t_{\mathrm{si}}/2, \infty)$ for $\sigma = 1$ and to the interval $(-\infty, t_{\mathrm{si}}/2)$ for $\sigma = -1$, using (3.27). The last terms in (5.51) and (5.52) are included to facilitate subsequent derivation of the charge model. The currents I_1 and I_2 thus defined are position-dependent. However, they add up to produce constant current I_{d} along the channel.

[1] If one approaches the boundary between the trigonometric and the hyperbolic region on the V_1-V_2 plane [78] from inside the trigonometric region (cf. lines Γ_1, Γ_2 in Fig. 3.2) then x_{d} approaches $\sigma \cdot \infty$. This explains the selection of x_{d} for the hyperbolic region. Naturally, this selection of x_{d} is a matter of convenience and does not enter into the final model equation.

In both the trigonometric and the hyperbolic cases we define

$$q_{\mathrm{g1}} = q \int_{-t_{\mathrm{si}}/2}^{x_{\mathrm{d}}} n \mathrm{d}x + \epsilon_{\mathrm{si}} E_{\mathrm{x}}(x_{\mathrm{d}}) \tag{5.53}$$

$$q_{\mathrm{g2}} = q \int_{x_{\mathrm{d}}}^{t_{\mathrm{si}}/2} n \mathrm{d}x - \epsilon_{\mathrm{si}} E_{\mathrm{x}}(x_{\mathrm{d}}) \tag{5.54}$$

$$\tilde{q}_{\mathrm{g1}} = \frac{q}{\frac{\mathrm{d}\psi_{\mathrm{s1}}}{\mathrm{d}y}} \int_{-t_{\mathrm{si}}/2}^{x_{\mathrm{d}}} n \frac{\partial \psi}{\partial y} \mathrm{d}x + \epsilon_{\mathrm{si}} E_{\mathrm{x}}(x_{\mathrm{d}}) \frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}\psi_{\mathrm{s1}}} + \phi_{\mathrm{t}} \epsilon_{\mathrm{si}} \frac{\mathrm{d}E_{\mathrm{x}}(x_{\mathrm{d}})}{\mathrm{d}\psi_{\mathrm{s1}}} \tag{5.55}$$

and

$$\tilde{q}_{\mathrm{g2}} = \frac{q}{\frac{\mathrm{d}\psi_{\mathrm{s2}}}{\mathrm{d}y}} \int_{x_{\mathrm{d}}}^{t_{\mathrm{si}}/2} n \frac{\partial \psi}{\partial y} \mathrm{d}x - \epsilon_{\mathrm{si}} E_{\mathrm{x}}(x_{\mathrm{d}}) \frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}\psi_{\mathrm{s2}}} - \phi_{\mathrm{t}} \epsilon_{\mathrm{si}} \frac{\mathrm{d}E_{\mathrm{x}}(x_{\mathrm{d}})}{\mathrm{d}\psi_{\mathrm{s2}}}. \tag{5.56}$$

Physically, $q_{\mathrm{g1}}(y)$ and $q_{\mathrm{g2}}(y)$ represent the charge densities at two gates at a distance y from the source. In particular, the total mobile charge density is $-q_{\mathrm{g}}$ where

$$q_{\mathrm{g}} = q_{\mathrm{g1}} + q_{\mathrm{g2}}. \tag{5.57}$$

With the above definitions

$$I_{\mathrm{j}} = \mu h_{\mathrm{f}} \left(\tilde{q}_{\mathrm{gj}} \frac{\mathrm{d}\psi_{\mathrm{sj}}}{\mathrm{d}y} - \phi_{\mathrm{t}} \frac{\mathrm{d}q_{\mathrm{gj}}}{\mathrm{d}y} \right). \tag{5.58}$$

Substituting

$$q_{\mathrm{gj}} = C_{\mathrm{oxj}}(V_j - \psi_{\mathrm{sj}}) \tag{5.59}$$

in (5.58) we have

$$I_{\mathrm{j}} = \mu W \left(\tilde{q}_{\mathrm{gj}} + \phi_{\mathrm{t}} C_{\mathrm{oxj}} \right) \frac{\mathrm{d}\psi_{\mathrm{sj}}}{\mathrm{d}y}. \tag{5.60}$$

Using the identity

$$n \frac{\partial \psi}{\partial y} - \phi_{\mathrm{t}} \frac{\partial n}{\partial y} = n \frac{\partial V_{\mathrm{c}}}{\partial y} \tag{5.61}$$

and the fact that in a device with the geometry shown in Fig. 3.1, $V_{\mathrm{c}} = V_{\mathrm{c}}(y)$, expressions (5.51) and (5.52) can be reformulated as

$$I_{\mathrm{j}} = \mu h_{\mathrm{f}} q_{\mathrm{gj}} \frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}y}. \tag{5.62}$$

In particular, from (5.50) and (5.57)

$$I_{\mathrm{d}} = \mu h_{\mathrm{f}} q_{\mathrm{g}} \frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}y}. \tag{5.63}$$

Equating (5.60) and (5.62) we have

$$(\tilde{q}_{\mathrm{gj}} + \phi_{\mathrm{t}} C_{\mathrm{oxj}}) \frac{\mathrm{d}\psi_{\mathrm{sj}}}{\mathrm{d}y} = q_{\mathrm{gj}} \frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}y}. \tag{5.64}$$

Substituting $\mathrm{d}V_{\mathrm{c}}/\mathrm{d}y$ from (5.63) yields

$$I_{\mathrm{d}} = \mu h_{\mathrm{f}} \hat{q}_{\mathrm{gj}} \frac{\mathrm{d}\psi_{\mathrm{sj}}}{\mathrm{d}y} \tag{5.65}$$

where

$$\hat{q}_{\mathrm{gj}} = (\tilde{q}_{\mathrm{gj}} + \phi_{\mathrm{t}} C_{\mathrm{oxj}}) \frac{q_{\mathrm{g}}}{q_{\mathrm{gj}}}. \tag{5.66}$$

To interpret (5.65), consider the corresponding equation for a bulk MOSFET with a single gate. Under the charge-sheet approximation

$$I_{\mathrm{d}} = \mu h_{\mathrm{f}} \hat{q} \frac{\mathrm{d}\psi_{\mathrm{s}}}{\mathrm{d}y} \tag{5.67}$$

where ψ_{s} denotes the surface potential and

$$\hat{q} = q_{\mathrm{i}} + \phi_{\mathrm{t}} C_{\mathrm{ox}} \tag{5.68}$$

where q_{i} is the absolute value of the inversion charge density and the second term accounts for the diffusion current. Thus, the drain current in the double-gate device considered here rigorously without the charge-sheet approximation is given by the same expression as the current in a single gate device provided that instead of the charge density $\hat{q}$ and the surface potential ψ_{s} we use the effective charge density $\hat{q}_{\mathrm{gj}}$ and the surface potential ψ_{sj}. In (5.66), the difference between $\tilde{q}_{\mathrm{gj}}$ and q_{gj} accounts for the fact that the charge-sheet approximation is not used in (5.65) and the factor $q_{\mathrm{g}}/q_{\mathrm{gj}}$ reflects the presence of the second gate. This interpretation is not necessary for the subsequent analysis but provides the motivation for symmetric linearization of $\hat{q}_{\mathrm{gj}}$ in the next section. Indeed, such linearization of the charge $\hat{q}$ for the single

gate bulk MOSFET leads to a remarkably simple and accurate terminal charge model [88, 89, 45].

To complete the discussion, we present the following analytical expressions for $q_{\rm gj}$ and $\tilde{q}_{\rm gj}$ for $j = 1, 2$ derived in Appendix F.

In the trigonometric case

$$q_{\rm g1} = 4 \cdot \phi_{\rm t} C_{\rm si} \theta \cot(\alpha - \theta), \tag{5.69}$$

$$q_{\rm g2} = -4 \cdot \phi_{\rm t} C_{\rm si} \theta \cot(\alpha + \theta), \tag{5.70}$$

$$\tilde{q}_{\rm g1} = q_{\rm g1} - \phi_{\rm t} C_{\rm ox1} \left[1 - \frac{2 - 2 \cdot q_{\rm gn1}(\alpha' - 1)}{1 - (n_{\rm n1}/q_{\rm gn1})(\alpha' - 1)} \right], \tag{5.71}$$

and

$$\tilde{q}_{\rm g2} = q_{\rm g2} - \phi_{\rm t} C_{\rm ox2} \left[1 - \frac{2 + 2 \cdot q_{\rm gn2}(\alpha' + 1)}{1 + (n_{\rm n2}/q_{\rm gn2})(\alpha' + 1)} \right] \tag{5.72}$$

where

$$\alpha' = \frac{\mathrm{d}\alpha}{\mathrm{d}\theta} = \frac{2 \cdot (r_{\rm c1} n_{\rm n1} - r_{\rm c2} n_{\rm n2}) + 2 \cdot (r_{\rm c1} q_{\rm gn1} - r_{\rm c2} q_{\rm gn2}) + (q_{\rm gn1} - q_{\rm gn2})}{q_{\rm gn} + 2 \cdot (r_{\rm c1} n_{\rm n1} + r_{\rm c2} n_{\rm n2})}, \tag{5.73}$$

$q_{\rm gn1}$ and $q_{\rm gn2}$ is the respective gate charge density $q_{\rm g1}$ and $q_{\rm g2}$ normalized to $4 \cdot \phi_{\rm t} C_{\rm si}$, $q_{\rm gn} = q_{\rm gn1} + q_{\rm gn2}$, and $n_{\rm n1}$ and $n_{\rm n2}$ is the surface electron concentration normalized to $n_{\rm i}(4 \cdot C_{\rm si}/C_{\rm f})^2$.

In the hyperbolic case

$$q_{\rm g1} = 4 \cdot \sigma \phi_{\rm t} C_{\rm si} \theta_* \coth(\alpha_* - \sigma \theta_*), \tag{5.74}$$

$$q_{\rm g2} = -4 \cdot \sigma \phi_{\rm t} C_{\rm si} \theta_* \coth(\alpha_* + \sigma \theta_*), \tag{5.75}$$

$$\tilde{q}_{\rm g1} = q_{\rm g1} - \phi_{\rm t} C_{\rm ox1} \left[1 - \frac{2 - 2 \cdot q_{\rm gn1}(\sigma \alpha' - 1)}{1 - (n_{\rm n1}/q_{\rm gn1})(\sigma \alpha' - 1)} \right]. \tag{5.76}$$

and

$$\tilde{q}_{\rm g2} = q_{\rm g2} - \phi_{\rm t} C_{\rm ox2} \left[1 - \frac{2 + 2 \cdot q_{\rm gn2}(\sigma \alpha' + 1)}{1 + (n_{\rm n2}/q_{\rm gn2})(\sigma \alpha' + 1)} \right] \tag{5.77}$$

where α' is same as in (5.73).

5.4 Terminal Charge Model

The physical charge density q_{gj} on gate j is a linear function of the surface potential ψ_{sj} [cf. (5.59)] but the effective charge density $\hat{q}_{\mathrm{gj}}$ is not [cf. (5.66)]. This is the price paid for the apparent simplicity of (5.65) for the drain current in terms of $\hat{q}_{\mathrm{gj}}$. The approximation made in the proposed charge model consists of symmetric linearization of $\hat{q}_{\mathrm{gj}}$. For this purpose we introduce the value $\hat{q}_{\mathrm{gjm}}$ of $\hat{q}_{\mathrm{gj}}$ at the point $y = y_{\mathrm{jm}}$ where the surface potential ψ_{sj} reaches its average value

$$\psi_{\mathrm{sjm}} = \frac{\psi_{\mathrm{sjs}} + \psi_{\mathrm{sjd}}}{2} \tag{5.78}$$

where ψ_{sjs} and ψ_{sjd} are the values of ψ_{sj} at the source and drain ends of the channel, respectively. The simplest form of symmetric linearization consists of setting

$$\hat{q}_{\mathrm{gj}} = \hat{q}_{\mathrm{gjm}} + \left(\frac{\mathrm{d}\hat{q}_{\mathrm{gj}}}{\mathrm{d}\psi_{\mathrm{sj}}}\right)_{\psi_{\mathrm{sj}}=\psi_{\mathrm{sjm}}} \cdot u_{\mathrm{j}} \tag{5.79}$$

where $u_j = \psi_{\mathrm{sj}} - \psi_{\mathrm{sjm}}$. This is a valid approximation closely resembling the one used in the case of bulk MOSFETs [88, 89, 45]. However, in the context of a double-gate device it is somewhat difficult to use, since evaluation of $\hat{q}_{\mathrm{gjm}}$ and $(\mathrm{d}\hat{q}_{\mathrm{gj}}/\mathrm{d}\psi_{\mathrm{sj}})_{\psi_{\mathrm{sj}}=\psi_{\mathrm{sjm}}}$ requires knowledge of $V_{\mathrm{c}}(y_{\mathrm{jm}})$. Instead, we generalize (5.79) as

$$\hat{q}_{\mathrm{gj}} = C_{\mathrm{oxj}}(\nu_{\mathrm{j}} - \alpha_{\mathrm{j}} u_{\mathrm{j}}) \tag{5.80}$$

where bias-dependent (but position-independent) coefficients ν_j and α_j are selected so as to assure model accuracy and simplicity.

Substituting (5.80) in (5.65)

$$I_{\mathrm{d}} = \mu h_{\mathrm{f}} C_{\mathrm{oxj}}(\nu_{\mathrm{j}} - \alpha_{\mathrm{j}} u_{\mathrm{j}}) \frac{\mathrm{d}\psi_{\mathrm{sj}}}{\mathrm{d}y}. \tag{5.81}$$

After integration

$$I_{\mathrm{d}} = \mu \frac{h_{\mathrm{f}}}{L} C_{\mathrm{oxj}} \nu_{\mathrm{j}} \Delta\psi_{\mathrm{sj}} \tag{5.82}$$

where

$$\Delta\psi_{\mathrm{sj}} = \psi_{\mathrm{sjd}} - \psi_{\mathrm{sjs}}. \tag{5.83}$$

We now select ν_j so that the expression for I_d (available, for example, in [93, 94, 95, 76, 96]) remain unaffected by the symmetric linearization approximation (5.80):

$$\nu_\mathrm{j} = \frac{LI_\mathrm{d}}{\mu h_\mathrm{f} C_\mathrm{oxj} \Delta\psi_\mathrm{sj}} \tag{5.84}$$

In this way the new charge model can be used with any of the published drain current models and the channel potential V_c at the point $y = y_\mathrm{jm}$ is not needed. In this work we use the exact analytical current model of [76]. For the linearization coefficient α_j we use the quotient approximation [66]

$$\alpha_\mathrm{j} = -\frac{\hat{q}_\mathrm{gjd} - \hat{q}_\mathrm{gjs}}{C_\mathrm{oxj} \Delta\psi_\mathrm{sj}}. \tag{5.85}$$

In the final analysis, this selection of ν_j and α_j is justified by comparing the charge model with the results of numerical computations performed in Section 5.5. Nevertheless, it is instructive to point out the difference between (5.79) and (5.80). Using (5.79) provides an exact value for $\hat{q}_\mathrm{gj}$ at $y = y_\mathrm{jm}$ but approximate expression for I_d. On the other hand, (5.80) provides approximate expression for $\hat{q}_\mathrm{gjm}$ but does not introduce any error for the drain current.

The advantage of the symmetrically linearized form (5.80) of the effective charge densities is that it leads to simple expressions for the position dependence of the surface potential for the terminal charges. Equating (5.81) and (5.82) yields

$$\frac{\mathrm{d}y}{\mathrm{d}u_j} = \frac{L(H_\mathrm{j} - u_\mathrm{j})}{H_\mathrm{j} \Delta\psi_\mathrm{sj}} \tag{5.86}$$

where

$$H_\mathrm{j} = \frac{\nu_\mathrm{j}}{\alpha_\mathrm{j}}. \tag{5.87}$$

The total charge on gate j is

$$Q_\mathrm{Gj} = h_\mathrm{f} \int_0^L q_\mathrm{gj} \mathrm{d}y = h_\mathrm{f} \int_{u_\mathrm{js}}^{u_\mathrm{jd}} q_\mathrm{gj} \frac{\mathrm{d}y}{\mathrm{d}u_\mathrm{j}} \mathrm{d}u_\mathrm{j} \tag{5.88}$$

where $u_{\rm js}$ and $u_{\rm jd}$ are the values of $u_{\rm j}$ at the source and drain ends of the channel, respectively. Substituting (5.86) in (5.88) we have

$$Q_{\rm Gj} = h_{\rm f} \int_{-\Delta\psi_{\rm sj}/2}^{\Delta\psi_{\rm sj}/2} q_{\rm gj} \frac{L(H_{\rm j} - u_{\rm j})}{H_{\rm j}\Delta\psi_{\rm sj}} {\rm d}u_{\rm j} \tag{5.89}$$

where

$$q_{\rm gj} = C_{\rm oxj}(V_{\rm oxjm} - u_{\rm j}) \tag{5.90}$$

and $V_{\rm oxjm} = V_{\rm j} - \psi_{\rm sjm}$ is the voltage across oxide $t_{\rm oxj}$ at point $y = y_{\rm jm}$. Hence

$$Q_{\rm Gj} = h_{\rm f} L C_{\rm oxj} \left(V_{\rm oxjm} + \frac{\Delta\psi_{\rm sj}^2}{12 \cdot H_{\rm j}} \right) \tag{5.91}$$

The drain charge is found from Ward-Dutton partitioning [97]

$$Q_{\rm D} = -h_{\rm f} \sum_{j=1}^{2} \int_{0}^{L} q_{\rm gj} \frac{y}{L} {\rm d}y \tag{5.92}$$

or

$$Q_{\rm D} = -\frac{h_{\rm f}}{L} \sum_{j=1}^{2} \int_{-\Delta\psi_{\rm sj}/2}^{\Delta\psi_{\rm sj}/2} q_{\rm gj} y \frac{{\rm d}y}{{\rm d}u_{\rm j}} {\rm d}u_{\rm j}. \tag{5.93}$$

To evaluate the integral we use the relations between the position y and the surface potentials which are obtained by integrating (5.86):

$$y = y_{\rm jm} + \frac{L}{\Delta\psi_{\rm sj}} \left(u_j - \frac{u_j^2}{2 \cdot H_{\rm j}} \right) \tag{5.94}$$

where

$$y_{\rm jm} = \frac{L}{2} \left(1 + \frac{\Delta\psi_{sj}}{4 \cdot H_{\rm j}} \right). \tag{5.95}$$

Then

$$Q_{\rm D} = -h_{\rm f} L \sum_{j=1}^{2} C_{\rm oxj} \left[\frac{V_{\rm oxjm}}{2} - \frac{\Delta\psi_{\rm sj}}{12} \left(1 - \frac{\Delta\psi_{\rm sj}}{2 \cdot H_{\rm j}} - \frac{\Delta\psi_{\rm sj}^2}{20 \cdot H_{\rm j}^2} \right) \right]. \tag{5.96}$$

Finally, the integrated source charge is evaluated from the neutrality condition $Q_{\rm S} = -(Q_{\rm G1} + Q_{\rm G2} + Q_{\rm D})$.

The concept of symmetric linearization of the effective charge has been investigated for a common-gate symmetric DG-FinFET in the previous chapter [67].

The present model includes [67] as a special case (cf. Appendix G), thus eliminating the need for two separate models of symmetric and asymmetric DG-FinFETs which until now represented the state of the art in compact modeling of these devices.

5.5 Results and Discussion

To verify the accuracy of the proposed model we compare it with the results of numerical integration of (5.88) and (5.92) and also with two-dimensional TCAD simulations [98]. All transcapacitances are normalized to $C_{\mathrm{ox1}} h_{\mathrm{f}} L$. These capacitances are automatically evaluated in SPICE-like circuit simulators by differentiating terminal charges w.r.t. terminal voltages.

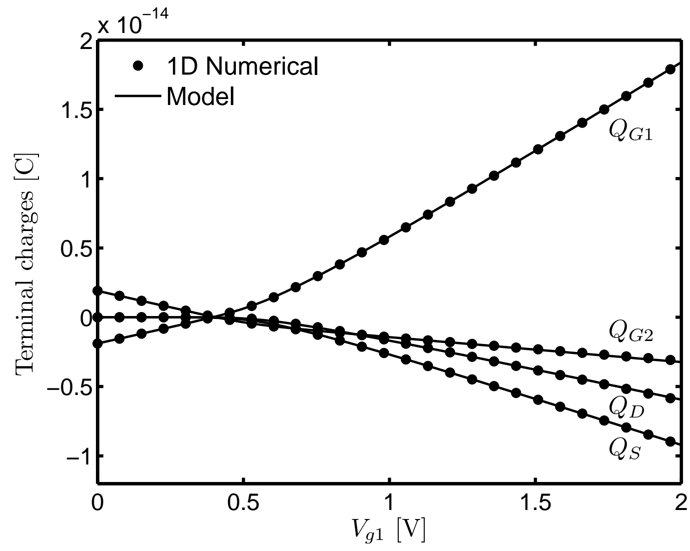
The terminal charges and transcapacitances are plotted for different biases assuming $T = 300$ K, $t_{\mathrm{si}} = 10$ nm and $\Delta\phi_1 = \Delta\phi_2 = 0$. The asymmetry is introduced with different gate oxide thicknesses. To concentrate on the core model the length and height of the channel are kept sufficiently long ($L = h_{\mathrm{f}} = 1$ μm) to suppress small geometry effects. These effects can be introduced as a correction to the core model as done for symmetric DG-FinFET [56].

Figs. 5.1a and 5.1b show the terminal charges and the transcapacitances as a functions of V_{g1} for independent-gate symmetric DG-FinFET with V_{g2} and V_{d} as parameters. In these plots the channel under gate 2 is in weak inversion. Figs. 5.2a and 5.2b show similar plots for the same device with channel under gate 2 strongly inverted. The terminal charges and the transcapacitances plots versus drain voltage are shown in Figs. 5.3a and 5.3b, respectively, for fixed values of V_{g1} and V_{g2}.

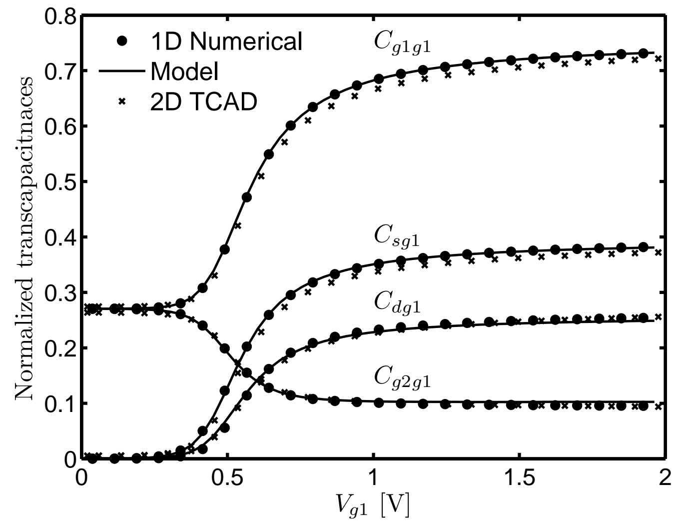
The capacitances versus V_{g1} plots for asymmetric DG-FinFET with V_{g2} and V_{d} as parameters are shown in Fig. 5.4 with the channel under the gate 2 weakly inverted, and in Fig. 5.5 with the channel under the gate 2 strongly inverted. Fig. 5.6 shows a plot of transcapacitances as functions of V_{d}. Finally, at $V_{\mathrm{ds}} = 0$ the removable singularity in the expression for H_{j} does not appear since an expression

equivalent to, but more elaborate than (5.87) is used. The plots for charges and transcapacitances at $V_{\mathrm{ds}} = 0$ V are shown in Figs. 5.7a and 5.7b, respectively.

Good accuracy of the proposed model is observed in all cases. The small differences between the TCAD results and the new model present in Fig. 5.5 are inconsequential for practical compact modeling purposes and do not affect the physical behavior of the device transcapacitances.

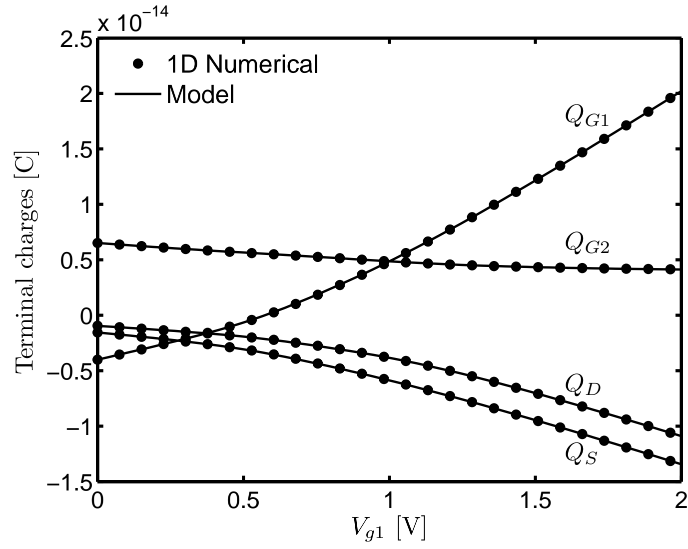


(a)

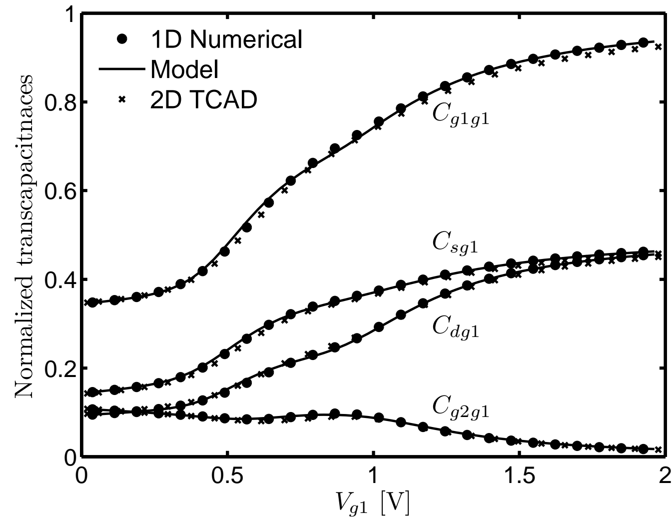


(b)

Figure 5.1: Comparison of terminal charges (a) and transcapacitances (b) obtained from the new model and numerical computations; $t_{\mathrm{ox1}} = t_{\mathrm{ox2}} = 2$ nm , $V_{\mathrm{g2}} = 0.4$ V and $V_{\mathrm{d}} = 1.5$ V.

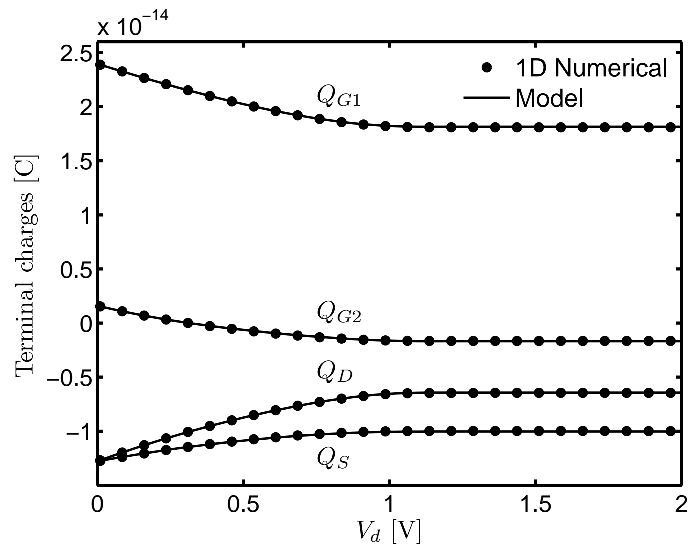


(a)

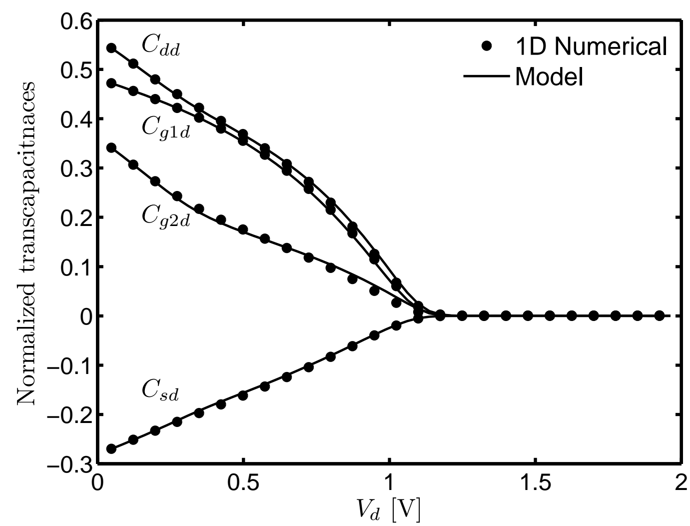


(b)

Figure 5.2: Comparison of terminal charges (a) and transcapacitances (b) obtained from the new model and numerical computations; $t_{\mathrm{ox1}} = t_{\mathrm{ox2}} = 2$ nm, $V_{\mathrm{g2}} = 1.0$ V and $V_{\mathrm{d}} = 0.5$ V.



(a)



(b)

Figure 5.3: Comparison of terminal charges (a) and transcapacitances (b) obtained from the new model and numerical computation; $t_{\text{ox1}} = t_{\text{ox2}} = 2$ nm, $V_{\text{g1}} = 2.0$ V and $V_{\text{g2}} = 0.6$ V.

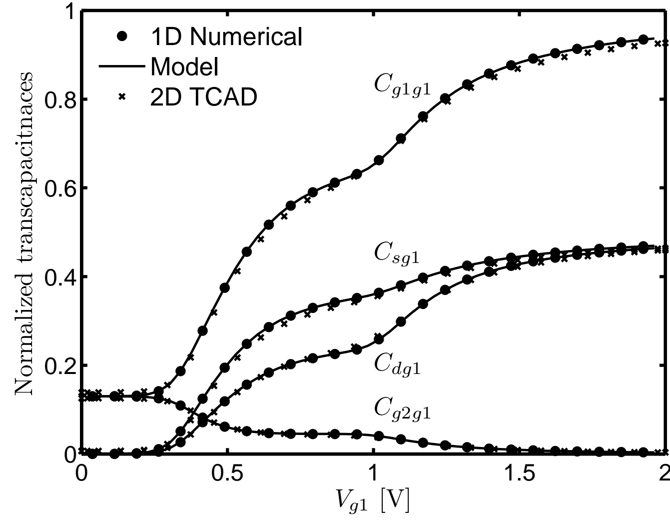


Figure 5.4: Comparison of transcapacitances obtained from the new model and numerical computations; $t_{\mathrm{ox1}} = 2$ nm, $t_{\mathrm{ox2}} = 10$ nm, $V_{\mathrm{g2}} = 0.6$ V and $V_{\mathrm{d}} = 0.5$ V.

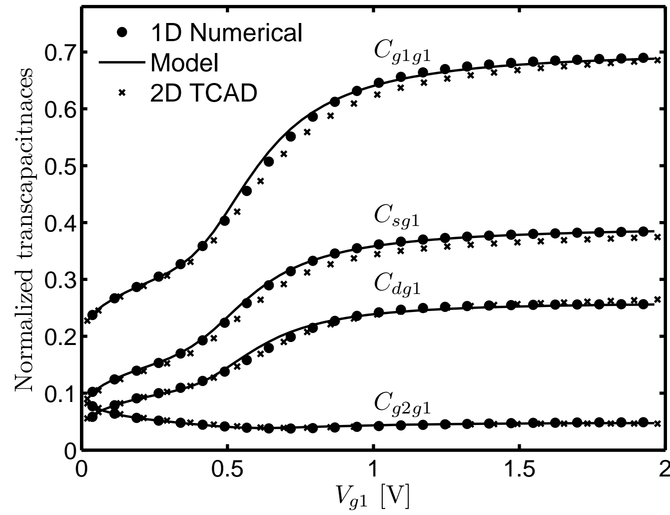


Figure 5.5: Comparison of transcapacitances obtained from the new model and numerical computations; $t_{\mathrm{ox1}} = 2$ nm, $t_{\mathrm{ox2}} = 10$ nm, $V_{\mathrm{g2}} = 1.5$ V and $V_{\mathrm{d}} = 2.0$ V.

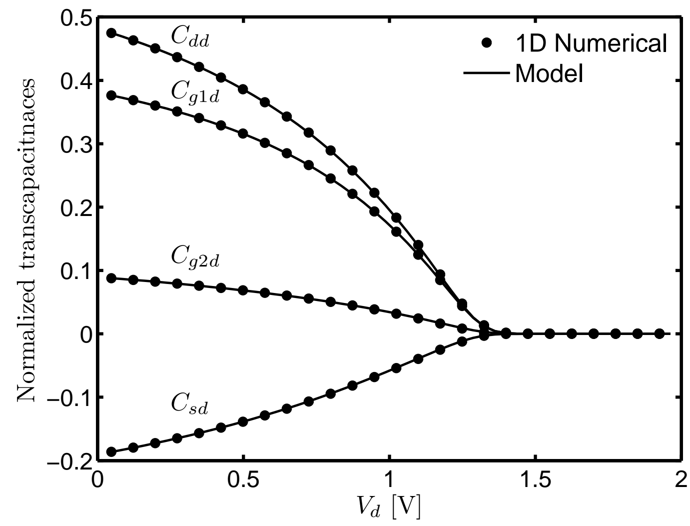
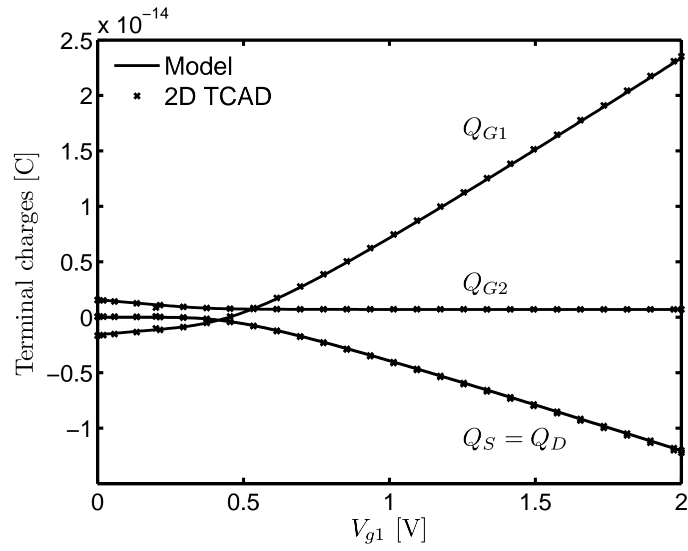
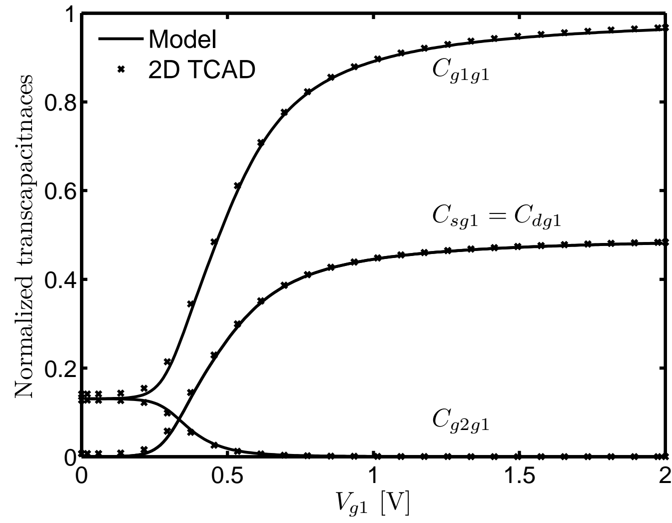


Figure 5.6: Comparison of transcapacitances obtained from the new model and numerical computations; $t_{\mathrm{ox1}} = 2$ nm, $t_{\mathrm{ox2}} = 10$ nm, $V_{\mathrm{g1}} = 2.0$ V and $V_{\mathrm{g2}} = 0.6$ V.



(a)



(b)

Figure 5.7: Comparison of terminal charges (a) and transcapacitances (b) obtained from the new model and numerical computation at $V_{\mathrm{ds}} = 0.0$ V; $t_{\mathrm{ox1}} = 2$ nm, $t_{\mathrm{ox2}} = 10$ nm, and $V_{\mathrm{g2}} = 0.7$ V.

5.6 Model Implementation and Simulation

As Verilog-A has emerged as the de facto standard language for defining compact models [99] we have implemented our model in Verilog-A and used this, in a commercial circuit simulator, to investigate circuit behavior. Two examples illustrate the advantages of the gate-to-gate coupling feature of independent gate DG-FinFETs for both analog and digital applications. A double balanced mixer [100, 34] and Schmitt trigger [101] are shown in Figs. 5.8 and 5.9, respectively. In the mixer circuit RF+ and RF- are the RF signal ports, with input frequency f_{RF}, and LO+/LO- is the local oscillator signal of frequency f_{LO}. The '+' signal is antiphase with respect to the '−' signal. A three tone (f_{RF1}, f_{RF2}, and f_{LO}) harmonic balance simulation of the mixer was done and Fig. 5.10 shows the output power of the first, second, and third order inter-modulation products (at frequencies $|f_{\mathrm{RF1}} - f_{\mathrm{LO}}|$, $|f_{\mathrm{RF1}} - f_{\mathrm{RF2}}|$, and $|2f_{\mathrm{RF1}} - f_{\mathrm{RF2}} - f_{\mathrm{LO}}|$, respectively) as a function of the input power of the RF signals. The slopes of the inter-modulation product power in Fig. 5.10 are very close to their theoretical values. Two situations are shown, with symmetric gate oxides and with an asymmetry in the thickness of the two gate oxides of each DG-FinFET. For the symmetric case the second order product of the mixer cancels out, as expected. However, the asymmetric case destroys the balance of the mixer, which results in the non-zero second order product seen in Fig. 5.10.

In the Schmitt trigger circuit of Fig. 5.9 the threshold voltages of M_1 and M_2 are altered dynamically by positive feedback from output to gate 2 of both M_1 and M_2. This causes hysteresis in the transfer characteristic as shown in Fig. 5.11. The four transistor independent-gate FinFET Schmitt trigger has advantages of reduced area and reduced power consumption compared to a conventional six transistor common-gate FinFET Schmitt trigger [101].

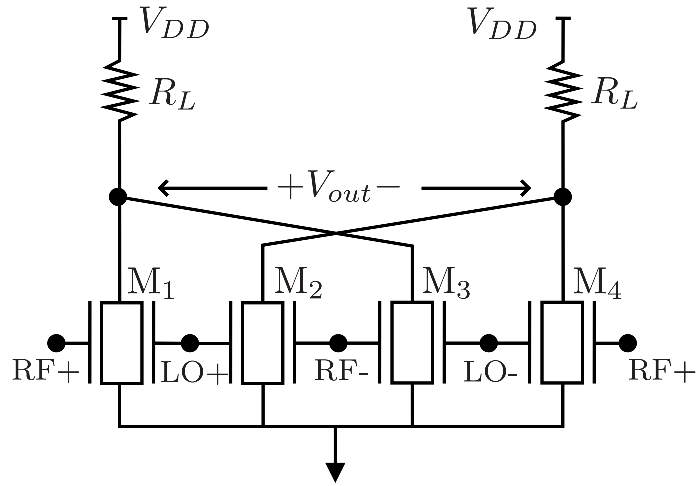


Figure 5.8: Double balanced mixer.

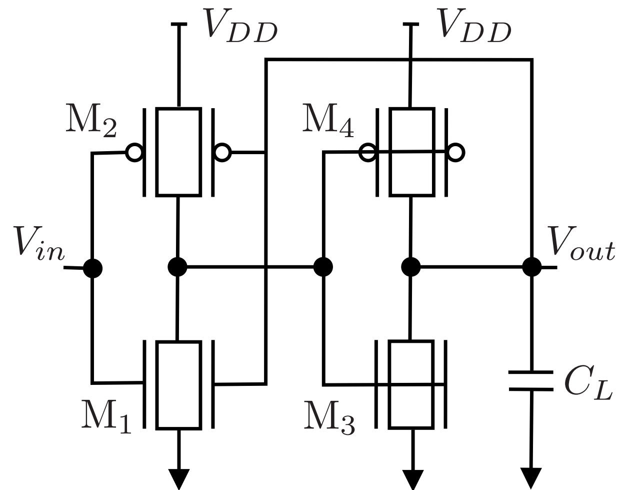


Figure 5.9: Schmitt trigger.

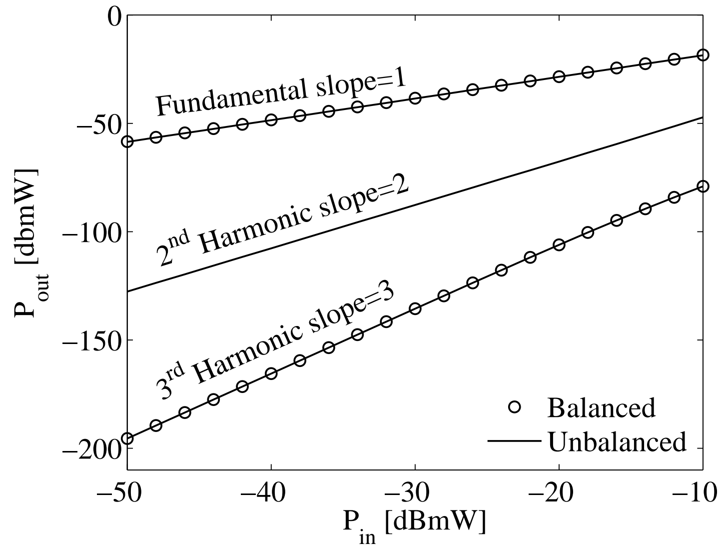


Figure 5.10: Harmonic balance simulation of double balance mixer shown in Fig. 5.8.

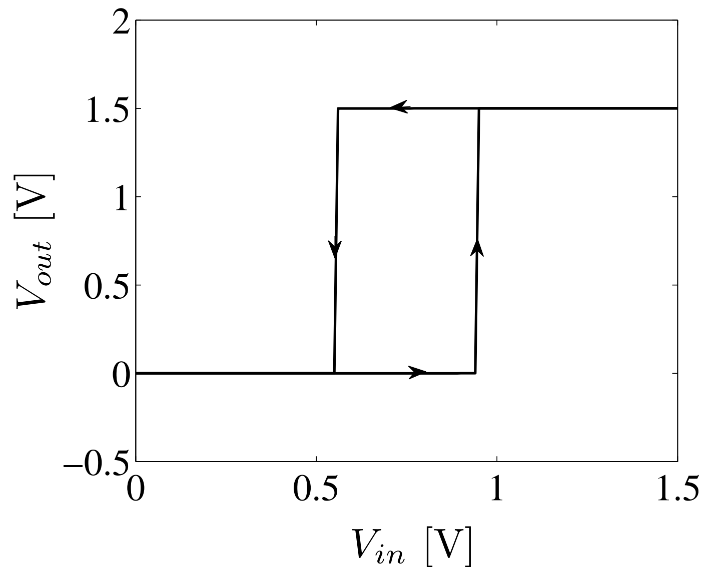


Figure 5.11: Transfer characteristics of independent-gate FinFET Schmitt trigger shown in Fig. 5.9.

Chapter 6

CONCLUSIONS

The transcapacitance characteristics of bulk and SOI DG-FinFETs are studied in all regions of operation and it is found that the unipolar approximation is inaccurate in describing the observed transcapacitances of bulk DG-FinFETs in the accumulation region. An accurate approximate ambipolar IVE for common-gate symmetric DG-FinFETs considering both electron and hole contributions to space charge is proposed. The new IVE developed in this work is general and can be adopted in any surface-potential-based compact model of DG-FinFETs with intrinsic or lightly-doped bodies.

We have presented an accurate closed form algorithm for solving the ambipolar IVE of common-gate symmetric DG-FinFETs. The new algorithm can be used with any surface-potential-based compact model of common-gate symmetric DG-FinFETs. We also show that the earlier unipolar approximation of the IVE in [62] emerges as an important special case of the more general ambipolar IVE.

Based on the new IVE a compact core model for drain current and terminal charges valid in all regions of operation is developed for common-gate symmetric DG-FinFET. Distinct C-V characteristics of bulk and SOI FinFETs can be reproduced by the new model with good accuracy. The approximations developed in [56, 57] and [82] from different assumptions are shown to be equivalent and can be significantly improved by developing symmetric linearization forms that do not involve the charge-sheet approximation. The new closed-form expressions for the drain current and terminal charges are similar to those used in the bulk PSP model. The expression for I_{d} is exact while those for Q_{G}, Q_{S}, Q_{B} and Q_{D} are accurate within 1% for common-gate symmetric DG-FinFETs and 2% for SGFET.

The solution space for the Poisson-Boltzmann equation in independent-gate asymmetric DG-FinFETs has been partitioned including all possible cases. The

analytical expressions for the partition lines are given in terms of the Lambert W function. The results simplify the development of a core compact model of asymmetric DG-FinFETs. A surface-potential-based compact model of the independent-gate asymmetric DG-FinFET, valid for all inversion conditions (from weak to strong inversion) of both channels, is developed, verified, and implemented in a circuit simulator. Efficient numerical IVE solution suitable for circuit simulator implementation is proposed.

We have developed analytical C_∞ continuous models for terminal charges of independent-gate asymmetric DG-FinFETs valid for all bias conditions. Terminal charges are obtained through the linearization of the effective gate charge densities as functions of the surface potentials.

The equations of the new models are brought in a form similar to that used in the PSP model but with separate contributions from each of the two gates. The structural similarity to the PSP [45] and PSP-based symmetric DGFET models [57] means that various small-geometry effects can be introduced in a similar manner. For the common-gate symmetric DGFET this approach has been already experimentally verified in [56].

Sample circuit simulations demonstrate the convergence properties and practicality of the new compact model. This work provides a promising core model for the development of a practical compact DG-FinFET and SGFET model.

REFERENCES

[1] D. Kahng and M. Atalla, Patent US patents 3 206 670 and 3 102 230, 1960.

[2] G. E. Moore, "Cramming more components onto integrated circuits," Electronics, vol. 38, no. 8, 1965.

[3] R. Dennard, F. Gaensslen, V. Rideout, E. Bassous, and A. LeBlanc, "Design of ion-implanted MOSFETs with very small physical dimensions," IEEE Jour. of Solid-State Circuits, vol. 9, no. 5, pp. 256–268, 1974.

[4] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, 2nd ed. Cambridge University Press, 2009.

[5] T. Nguyen and J. Plummer, "Physical mechanisms responsible for short channel effects in MOS devices," in IEDM Tech. Dig., vol. 27, 1981, pp. 596–599.

[6] N. Kim, T. Austin, D. Baauw, T. Mudge, K. Flautner, J. Hu, M. Irwin, M. Kandemir, and V. Narayanan, "Leakage current: Moore's law meets static power," Computer, vol. 36, no. 12, pp. 68–75, 2003.

[7] C. Kittle, Introduction to Solid State Physics. Wiley, New York, 1976.

[8] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part I-effects of substrate impurity concentration," IEEE Trans. on Electron Devices, vol. 41, no. 12, pp. 2357 –2362, 1994.

[9] F. Stern and W. E. Howard, "Properties of semiconductor surface inversion layers in the electric quantum limit," Phys. Rev., vol. 163, pp. 816–835, 1967.

[10] C.-Y. Lu, J. Sung, H. Kirsch, S. Hillenius, T. Smith, and L. Manchanda, "Anomalous $C-V$ characteristics of implanted poly MOS structure in n^+/p^+ dual-gate CMOS technology," IEEE Electron Device Letters, vol. 10, no. 5, pp. 192–194, 1989.

[11] D. Vasileska, D. K. Schroder, and D. K. Ferry, "Scaled silicon MOSFETs: degradation of the total gate capacitance," IEEE Trans. on Electron Devices, vol. 44, no. 4, pp. 584 –587, 1997.

[12] N. Arora, E. Rios, and C.-L. Huang, "Modeling the polysilicon depletion effect and its impact on submicrometer CMOS circuit performance," IEEE Trans. on Electron Devices, vol. 42, no. 5, pp. 935–943, 1995.

[13] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFET's: A 3-D "atomistic" simulation study," IEEE Trans. Electron Devices, vol. 45, no. 12, pp. 2505–2513, 1998.

[14] Y. Taur, D. Buchanan, W. Chen, D. Frank, K. Ismail, S.-H. Lo, G. Sai-Halasz, R. Viswanathan, H.-J. Wann, S. Wind, and H.-S. Wong, "CMOS scaling into the nanometer regime," Proceedings of the IEEE, vol. 85, no. 4, pp. 486 –504, 1997.

[15] T. Tomimatsu, Y. Goto, H. Kato, M. Amma, M. Igarashi, Y. Kusakabe, M. Takeuchi, S. Ohbayashi, S. Sakashita, T. Kawahara, M. Mizutani, M. Inoue, M. Sawada, Y. Kawasaki, S. Yamanari, Y. Miyagawa, Y. Takeshima, Y. Yamamoto, S. Endo, T. Hayashi, Y. Nishida, K. Horita, T. Yamashita, H. Oda, K. Tsukamoto, Y. Inoue, H. Fujimoto, Y. Sato, K. Yamashita, R. Mitsuhashi, S. Matsuyama, Y. Moriyama, K. Nakanishi, T. Noda, Y. Sahara, N. Koike, J. Hirase, T. Yamada, H. Ogawa, and M. Ogura, "Cost-effective 28-nm LSTP CMOS using gate-first metal gate/high-k technology," in VLSI Symp. Tech. Dig., 2009, pp. 36 –37.

[16] J. Jacobs and D. Antoniadis, "Channel profile engineering for MOSFET's with 100 nm channel lengths," IEEE Trans. on Electron Devices, vol. 42, no. 5, pp. 870–875, 1995.

[17] S. Mayuzumi, J. Wang, S. Yamakawa, Y. Tateshita, T. Hirano, M. Nakata, S. Yamaguchi, Y. Yamamoto, Y. Miyanami, I. Oshiyama, K. Tanaka, K. Tai, K. Ogawa, K. Kugimiya, Y. Nagahama, Y. Hagimoto, R. Yamamoto, S. Kanda, K. Nagano, H. Wakabayashi, Y. Tagawa, M. Tsukamoto, H. Iwamoto, M. Saito, S. Kadomura, and N. Nagashima, "Extreme high-performance n- and p-MOSFETs boosted by dual-metal/high-k gate damascene process using top-cut dual stress liners on (100) substrates," in IEDM Tech. Dig., 2007, pp. 293 –296.

[18] M. Chudzik, B. Doris, R. Mo, J. Sleight, E. Cartier, C. Dewan, D. Park, H. Bu, W. Natzle, W. Yan, C. Ouyang, K. Henson, D. Boyd, S. Callegari, R. Carter, D. Casarotto, M. Gribelyuk, M. Hargrove, W. He, Y. Kim, B. Linder, N. Moumen, V. Paruchuri, J. Stathis, M. Steen, A. Vayshenker, X. Wang, S. Zafar, T. Ando, R. Iijima, M. Takayanagi, V. Narayanan, R. Wise, Y. Zhang, R. Divakaruni, M. Khare, and T. Chen, "High-performance high-κ/metal gates for 45nm cmos and beyond with gate-first processing," in VLSI Symp. Tech. Dig., 2007, pp. 194 –195.

[19] B. Yu, C. Wann, E. Nowak, K. Noda, and C. Hu, "Short-channel effect improved by lateral channel-engineering in deep-submicronmeter MOSFET's," IEEE Trans. on Electron Devices, vol. 44, no. 4, pp. 627–634, 1997.

[20] S. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced strained-Si: extending the CMOS roadmap," IEEE Trans. on Electron Devices, vol. 53, no. 5, pp. 1010–1020, 2006.

[21] D. Frank, R. Dennard, E. Nowak, P. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," Proceedings of the IEEE, vol. 89, no. 3, pp. 259–288, 2001.

[22] J.-P. Colinge, "The SOI MOSFET: from single gate to multigate," in FinFETs and Other Multi-Gate Transistors, J.-P. Colinge, Ed. Springer, 2008, ch. 1.

[23] W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Dokumaci, A. Kumar, X. Wang, J. B. Johnson, and M. V. Fischetti, "Silicon CMOS devices beyond scaling," IBM Journal of Research and Development, vol. 50, no. 4.5, pp. 339–361, 2006.

[24] http://www.itrs.net/Links/2011ITRS/Home2011.htm.

[25] K. Kuhn, "CMOS scaling for the 22nm node and beyond: Device physics and technology," in VLSI Symp. Tech. Dig., 2011, pp. 1–2.

[26] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," in VLSI Symp. Tech. Dig., 2012, pp. 131 –132.

[27] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub 50-nm FinFET: PMOS," in IEDM Tech. Dig., 1999, pp. 67–70.

[28] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," IEEE Trans. on Electron Devices, vol. 47, no. 12, pp. 2320–2325, 2000.

[29] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume inversion: A new device with

greatly enhanced performance," IEEE Electron Device Lett., vol. 8, no. 9, pp. 410– 412, 1987.

[30] Y. Liu, S. Kijima, E. Sugimata, M. Masahara, K. Endo, T. Matsukawa, K. Ishii, K. Sakamoto, T. Sekigawa, H. Yamauchi, Y. Takanashi, and E. Suzuki, "Investigation of the TiN gate electrode with tunable work function and its application for FinFET fabrication," IEEE Trans. on Nanotechnology, vol. 5, no. 6, pp. 723–730, 2006.

[31] J. Kavalieros, B. Doyle, S. Datta, G. Dewey, M. Doczy, B. Jin, D. Lionberger, M. Metz, W. Rachmady, M. Radosavljevic, U. Shah, N. Zelick, and R. Chau, "Tri-gate transistor architecture with high-k gate dielectrics, metal gates and strain engineering," in VLSI Symp. Tech. Dig., 2006, pp. 50 –51.

[32] A. Majumdar, R. Zhibin, S. J. Koester, and W. Haensch, "Undoped-body extremely thin SOI MOSFETs with back gates," IEEE Trans. Electron Devices, vol. 56, no. 10, pp. 2270 –2276, 2009.

[33] M. Masahara, Y. Liu, K. Sakamoto, K. Endo, T. Matsukawa, K. Ishii, T. Sekigawa, H. Yamauchi, H. Tanoue, S. Kanemaru, H. Koike, and E. Suzuki, "Demonstration, analysis, and device design considerations for independent DG MOSFETs," IEEE Trans. Electron Devices, vol. 52, no. 9, pp. 2046– 2053, 2005.

[34] W. Zhang, J. G. Fossum, L. Mathew, and Y. Du, "Physical insights regarding design and performance of independent-gate FinFETs," IEEE Trans. Electron Devices, vol. 52, no. 10, pp. 2198–2206, 2005.

[35] K. Kim and J. G. Fossum, "Double-gate CMOS: Symmetrical- versus asymmetrical-gate devices," IEEE Trans. Electron Devices, vol. 48, no. 2, pp. 294–299, 2001.

[36] M. Shrivastava, M. S. Baghini, A. B. Sachid, D. K. Sharma, and V. R. Rao, "A novel and robust approach for common mode feedback using IDDG FinFET," IEEE Trans. Electron Devices, vol. 55, no. 11, pp. 3274–3282, 2008.

[37] A. Amara and O. Rozeau, Planar Double-Gate Transistor: From Technology to Circuit. Springer, 2009.

[38] M.-H. Chiang, K. Kim, C.-T. Chuang, and C. Tretz, "High-density reduced-stack logic circuit techniques using independent-gate controlled double-gate devices," IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 2370–2377, 2006.

[39] S. A. Tawfik and V. Kursun, "Low-power and compact sequential circuits with independent-gate FinFETs," IEEE Trans. Electron Devices, vol. 55, no. 1, pp. 60–70, 2008.

[40] A. B. Bhattacharyya, Compact MOSFET Models for VLSI Design. John Wiley and Sons, 2009.

[41] Y. Tsividis and C. McAndrew, Operation and Modeling of the MOS Transistor. Oxford University Press, 2010.

[42] "Compact modeling: Principles, techniques and applications," G. Gildenblat, Ed. Springer, 2010.

[43] R. Woltjer, L. Tiemeijer, and D. Klaassen, "An industrial view on compact modeling," Solid-State Electron., vol. 51, pp. 1572–1580, 2007.

[44] G. Gildenblat, H. Wang, T.-L. Chen, X. Gu, and X. Cai, "SP: An advanced surface-potential-based compact MOSFET model," IEEE J. Solid State Circuits, vol. 39, no. 9, pp. 1394–1406, 2004.

[45] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. van Langevelde, G. D. J. Smit, A. J. Scholten, and D. B. M. Klaassen, "PSP: An advanced surface-potential-based MOSFET model for circuit simulation," IEEE Trans. Electron Devices, vol. 53, no. 9, pp. 1979–1993, 2006.

[46] Y. Cheng, M.-C. Jeng, Z. Liu, J. Huang, M. Chan, K. Chen, P. K. Ko, and C. Hu, "A physical and scalable I-V model in BSIM3v3 for analog/digital circuit simulation," IEEE Trans. Electron Devices, vol. 44, no. 2, pp. 277–287, 1997.

[47] Y. Cheng, C. Hu, and C. Y. Cheng, MOSFET Modeling and BSIM3 User's Guide. Springer-Verlag, 1999.

[48] W. Liu, MOSFET Models for SPICE Simulation Including BSIM3v3 and BSIM4. WileyBlackwell, 2001.

[49] http://www.nxp.com/models/mos_models/model11/.

[50] C. C. Enz and E. A. Vittoz, Charge-Based MOS Transistor Modeling: The EKV Model for Low-Power and RF IC Design. Wiley InterScience, 2006.

[51] C. Galup-Montoro and M. C. Schneider, MOSFET Modeling for Circuit Analysis and Design. World Scientific, 2007.

[52] J. Watts, C. McAndrew, C. Enz, C. Galup-Montoro, G. Gildenblat, C. Hu, R. van Langevelde, M. Miura-Mattausch, R. Rios, and C.-T. Sah, "Advanced compact models for MOSFETs," in NSTI Nanotech, 2005, pp. 3–12.

[53] http://www-device.eecs.berkeley.edu/ bsimsoi/.

[54] W. Wu, X. Li, H. Wang, G. Gildenblat, G. Workman, S. Veeraraghavan, C. McAndrew, M. Sureddin, and C. Weintraub, "SP-SOI: A third generation surface potential based compact SOI MOSFET model," in Proc. IEEE CICC, 2005, pp. 819–822.

[55] W. Wu, X. Li, G. Gildenblat, G. Workman, S. Veeraraghavan, C. C. McAndrew, R. van Langevelde, G. D. J. Smit, A. J. Scholten, D. B. M. Klaassen, and J. Watts, "PSP-SOI: A surface potential based compact model of partially depleted SOI MOSFETs," in Proc. IEEE CICC, 2007, pp. 41–48.

[56] G. D. J. Smit, A. J. Scholten, N. Serra, R. M. T. Pijper, R. van Langevelde, A. Mercha, G. Gildenblat, and D. B. M. Klaassen, "PSP-based compact FinFET model describing dc and RF measurements," in IEDM Tech. Dig., 2006, pp. 175–178.

[57] G. D. J. Smit, A. J. Scholten, G. Curatola, R. van Langevelde, G. Gildenblat, and D. B. M. Klaassen, "PSP-based scalable compact FinFET model," in NSTI-Nanotech, vol. 3, 2007, pp. 520–525.

[58] G. Baccarani and S. Reggiani, "A compact double-gate MOSFET model comprising quantum-mechanical and nonstatic effects," IEEE Trans. Electron Devices, vol. 46, no. 8, pp. 1656–1666, 1999.

[59] L. Ge and J. G. Fossum, "Analytical modeling of quantization and volume inversion in thin Si-film DG MOSFETs," IEEE Trans. Electron Devices, vol. 49, no. 2, pp. 287–294, 2002.

[60] Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain-current model for DG MOSFETs," IEEE Electron Device Lett., vol. 25, no. 2, pp. 107–109, 2004.

[61] T.-L. Chen and G. Gildenblat, "Analytical approximation for the MOSFET surface potential," Solid-State Electron., vol. 45, no. 2, pp. 335–339, 2001.

[62] B. Yu, H. Lu, M. Liu, and Y. Taur, “Explicit continuous models for double-gate and surrounding-gate MOSFETs,” IEEE Trans. Electron Devices, vol. 54, no. 10, pp. 2715–2722, 2007.

[63] G. Dessai and G. Gildenblat, “Inclusion of the accumulation region in the compact models of bulk and SOI FinFETs,” IEEE Trans. Electron Devices, vol. 58, no. 8, pp. 2644–2651, 2011.

[64] X. Zhou, Z. Zhu, S. C. Rustagi, G. H. See, G. Zhu, S. Lin, C. Wei, and G. H. Lim, “Rigorous surface-potential solution for undoped symmetric double-gate MOSFETs considering both electrons and holes at quasi nonequilibrium,” IEEE Trans. Electron Devices, vol. 55, no. 2, pp. 616–623, 2008.

[65] G. Dessai and G. Gildenblat, “Approximate closed-form solution of ambipolar input voltage equation for the common-gate symmetric FinFET,” Solid-State Electronics, vol. 75, no. 9, pp. 77–80, 2012.

[66] W. Wu, W. Yao, and G. Gildenblat, “Surface-potential-based compact modeling of dynamically depleted SOI MOSFETs,” Solid-State Electron., vol. 54, no. 5, pp. 595–604, 2010.

[67] G. Dessai, A. Dey, G. Gildenblat, and G. D. J. Smit, “Symmetric linearization method for double-gate and surrounding-gate MOSFET models,” Solid-State Electron., vol. 53, no. 5, pp. 548–556, 2009.

[68] D. Lu, C.-H. Lin, A. Niknejad, and C. Hu, “Multi-gate MOSFET compact model BSIM-MG,” in Compact Modeling: Principles, Techniques and Applications, G. Gildenblat, Ed. Springer, 2010, ch. 13.

[69] Y. Taur, “An analytical solution to a double-gate MOSFET with undoped body,” IEEE Electron Device Lett., vol. 21, no. 5, pp. 245–247, 2000.

[70] C.-T. Sah, Fundamentals of Solid-State Electronics. World Scientific, 1991.

[71] O. F. Devereux and P. L. D. Bruyn, Interaction of plane-parallel double layers. M. I. T. Press, 1963.

[72] M. N. Tamashiro and H. Schiessel, “Where the linearized Poisson-Boltzmann cell model fails: The planar case as a prototype study,” Phys. Rev. E, vol. 68, no. 6, p. 066106, 2003.

[73] D. Burgreen and F. R. Nakache, "Electrokinetic flow in ultrafine capillary slits," J. Phys. Chem., vol. 68, no. 5, pp. 1084–1091, 1964.

[74] D. F. Lawden, Elliptic functions and applications. Springer-Verlag, 1989.

[75] H. Lu and Y. Taur, "An analytic potential model for symmetric and asymmetric DG MOSFETs," IEEE Trans. Electron Devices, vol. 53, no. 5, pp. 1161–1168, 2006.

[76] F. Liu, J. He, Y. Fu, J. Hu, W. Bian, Y. Song, X. Zhang, and M. Chan, "Generic carrier-based core model for undoped four-terminal double-gate MOSFETs valid for symmetric, asymmetric, and independent-gate-operation modes," IEEE Trans. Electron Devices, vol. 55, no. 3, pp. 816–826, 2008.

[77] A. Sahoo, P. K. Thakur, and S. Mahapatra, "A computationally efficient generalized Poisson solution for independent double-gate transistors," IEEE Trans. Electron Devices, vol. 57, no. 3, pp. 632–636, 2010.

[78] G. Dessai and G. Gildenblat, "Solution space for the independent-gate asymmetric DGFET," Solid-State Electron., vol. 54, no. 4, pp. 382–384, 2010.

[79] R. M. Corless, G. H. Gonnet, D. E. G. Hare, D. J. Jeffrey, and D. E. Knuth, "On the Lambert W function," Adv. Comput. Math., vol. 5, no. 1, pp. 329–359, 1996.

[80] D. Barry, J.-Y. Parlange, L. Li, H. Prommer, C. Cunningham, and F. Stagnitti, "Analytical approximations for real values of the Lambert W-function," Math. Comput. Simul., vol. 53, no. 1-2, pp. 95–103, 2000.

[81] G. Dessai, W. Wu, B. Bakkaloglu, C. C. McAndrew, and G. Gildenblat, "Compact model and circuit simulations for asymmetric, independent gate FinFETs," J. Comput. Electron., vol. 9, no. 3-4, pp. 103–107, 2010.

[82] H. Lu, B. Yu, and Y. Taur, "A unified charge model for symmetric double-gate and surrounding-gate MOSFETs," Solid-State Electron., vol. 52, no. 1, pp. 67–72, 2008.

[83] D. Jiménez, B. Iníguez, J. Suné, L. F. Marsal, J. Pallarès, J. Roig, and D. Flores, "Continuous analytic I-V model for surrounding-gate MOSFETs," IEEE Electron Device Lett., vol. 25, no. 8, pp. 571–573, 2004.

[84] B. Yu, W.-Y. Lu, H. Lu, and Y. Taur, "Analytic charge model for surrounding-gate MOSFETs," IEEE Trans. Electron Devices, vol. 54, no. 3, pp. 492–496, 2007.

[85] B. Yu, J. Song, Y. Yuan, W.-Y. Lu, and Y. Taur, "A unified analytic drain-current model for multiple-gate MOSFETs," IEEE Trans. Electron Devices, vol. 55, no. 8, pp. 2157–2163, 2008.

[86] J.-M. Sallese, F. Krummenacher, F. Prégaldiny, C. Lallement, A. Roy, and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism," Solid-State Electron., vol. 49, no. 3, pp. 485–489, 2005.

[87] B. Diagne, F. Prégaldiny, C. Lallement, J.-M. Sallese, and F. Krummenacher, "Explicit compact model for symmetric double-gate MOSFETs including solutions for small-geometry effects," Solid-State Electron., vol. 52, no. 1, pp. 99–106, 2008.

[88] T.-L. Chen and G. Gildenblat, "Symmetric bulk charge linearisation in charge-sheet MOSFET model," Electronics Lett., vol. 37, no. 12, pp. 791–793, 2001.

[89] H. Wang, T.-L. Chen, and G. Gildenblat, "Quasi-static and nonquasi-static compact MOSFET models based on symmetric linearization of the bulk and inversion charges," IEEE Trans. Electron Devices, vol. 50, no. 11, pp. 2262–2272, 2003.

[90] J. R. Brews, "A charge-sheet model of the MOSFET," Solid-State Electron., vol. 21, no. 2, pp. 345–355, 1978.

[91] D. E. Ward and R. W. Dutton, "A charge-oriented model for MOS transistor capacitances," IEEE J. Solid-State Circuits, vol. 13, no. 5, pp. 703–708, 1978.

[92] P. Yang, B. D. Epler, and P. K. Chatterjee, "An investigation of the charge conservation problem for MOSFET circuit simulation," IEEE J. Solid-State Circuits, vol. 18, no. 1, pp. 128–138, 1983.

[93] A. S. Roy, J. M. Sallese, and C. C. Enz, "A closed-form charge-based expression for drain current in symmetric and asymmetric double gate MOSFET," Solid-State Electron., vol. 50, no. 4, pp. 687–693, 2006.

[94] M. Reyboz, O. Rozeau, T. Poiroux, P. Martin, and J. Jomaah, "An explicit analytical charge-based model of undoped independent double gate MOSFET," Solid-State Electron., vol. 50, no. 7-8, pp. 1276–1282, 2006.

[95] A. Ortiz-Conde, F. J. García-Sánchez, J. Muci, S. Malobabic, and J. J. Liou, "A review of core compact models for undoped double-gate SOI MOSFETs," IEEE Trans. Electron Devices, vol. 54, no. 1, pp. 131–140, 2007.

[96] M. Reyboz, P. Martin, T. Poiroux, and O. Rozeau, "Continuous model for independent double gate MOSFET," Solid-State Electron., vol. 53, no. 5, pp. 504–513, 2009.

[97] S.-Y. Oh, D. E. Ward, and R. W. Dutton, "Transient analysis of MOS transistors," IEEE Trans. Electron Devices, vol. 27, no. 8, pp. 1571–1578, 1980.

[98] DESSIS User Manual, Integrated Systems Engineering, Zurich, Switzerland, 2004.

[99] L. Lemaitre, G. Coram, C. McAndrew, and K. Kundert, "Extensions to Verilog-A to support compact device modeling," in Proc. BMAS, 2003, pp. 134–138.

[100] G. Pei and E.-C. Kan, "Independently driven DG MOSFETs for mixed-signal circuits: part II-applications on cross-coupled feedback and harmonics generation," IEEE Trans. Electron Devices, vol. 51, no. 12, pp. 2094–2101, 2004.

[101] T. Cakici, A. Bansal, and K. Roy, "A low power four transistor Schmitt trigger for asymmetric double gate fully depleted SOI devices," in Proc. IEEE Int. SOI Conf., 2003, pp. 21–22.

[102] "Mathematica edition: Version 6.0," Wolfram Research, Inc., 2007.

[103] S. Winitzki, "Uniform approximations for transcendental functions," in Proc. ICCSA, 2003, pp. 780–789.

[104] C. C. McAndrew and J. J. Victory, "Accuracy of approximations in MOSFET charge models," IEEE Trans. Electron Devices, vol. 49, no. 1, pp. 72–81, 2002.

APPENDIX A

Derivation of (2.26)

The integral in (2.23) can be written as

$$I = \int_{h_0}^{h} \frac{\mathrm{d}h'}{\sqrt{h'(h'-k)\,(h'-1/k)}}, \tag{A.1}$$

where $h = e^{\varphi}$ and $k = e^{-\varphi_0}$. For $\eta = 1$ we have $h > 1/k > k$. Setting

$$h = \frac{1}{k\sin^2 t}; \qquad 0 \le t \le \pi/2, \tag{A.2}$$

we find

$$I = -2\cdot\sqrt{k}\left(\int_0^{t} \frac{\mathrm{d}t'}{\sqrt{1-k^2\sin^2 t'}} - \int_0^{\pi/2} \frac{\mathrm{d}t'}{\sqrt{1-k^2\sin^2 t'}}\right), \tag{A.3}$$

where

$$t = \sin^{-1}\left(e^{\frac{\varphi_0-\varphi}{2}}\right) \tag{A.4}$$

The first and second integrals are incomplete and complete elliptic integral of first kind in Legendre's form as defined in (2.24) and (2.25). Thus,

$$I = -2\cdot e^{-\varphi_0/2}\left[F\left(t, e^{-\varphi_0}\right) - K\left(e^{-\varphi_0}\right)\right]. \tag{A.5}$$

Similarly, for $\eta = -1$ where $h < 1/k < k$ setting

$$h = \frac{\sin^2(u)}{k}; \qquad 0 \le u \le \pi/2 \tag{A.6}$$

yields

$$I = 2\cdot e^{\frac{\varphi_0}{2}}\left[F\left(u, e^{\varphi_0}\right) - K\left(e^{\varphi_0}\right)\right], \tag{A.7}$$

where

$$u = \sin^{-1}\left(e^{-\frac{\varphi_0-\varphi}{2}}\right) \tag{A.8}$$

Equation (A.5) and (A.7) can be combined together as

$$I = -2\cdot\eta e^{\frac{-\eta\varphi_0}{2}}\left\{F\left[\sin^{-1}\left(e^{\frac{\eta(\varphi_0-\varphi)}{2}}\right), e^{-\eta\varphi_0}\right] - K\left(e^{-\eta\varphi_0}\right)\right\}. \tag{A.9}$$

Substituting (A.9) in (2.23) yields (2.26).

APPENDIX B

Equivalent form of Equation (2.26)

We show that (2.26) is equivalent to equation (7) of [64]. The integral in (2.23) can be written as

$$I = \frac{1}{2}\int_{\varphi_0}^{\varphi} \frac{\mathrm{d}\varphi'}{\sqrt{\cosh^2(\varphi'/2) - \cosh^2(\varphi_0/2)}}. \tag{B.1}$$

Setting $r = \cosh\frac{\varphi}{2}/\cosh\frac{\varphi_0}{2}$ yields

$$I = \eta\int_{1}^{r} \frac{\mathrm{d}r'}{\sqrt{(1-r'^2)\left[1-\cosh^2(\varphi_0/2)\cdot r'^2\right]}} \tag{B.2}$$

or

$$I = \eta\left\{\int_{0}^{r} \frac{\mathrm{d}r'}{\sqrt{(1-r'^2)\left[1-\cosh^2(\varphi_0/2)\cdot r'^2\right]}} - \int_{0}^{1} \frac{\mathrm{d}r'}{\sqrt{(1-r'^2)\left[1-\cosh^2(\varphi_0/2)\cdot r'^2\right]}}\right\}. \tag{B.3}$$

The integrals in (B.3) are elliptic integrals in a form given in equation (5) of [64]. They can be easily transformed into Legendre's form given in (2.24) and (2.25). As in [64] denote

$$F_{\text{elliptic}}\{z,k\} = \int_{0}^{z} \frac{\mathrm{d}x}{\sqrt{1-x^2}\sqrt{1-k^2x^2}}, \tag{B.4}$$

then (B.3) becomes

$$I = \eta\left[F_{\text{elliptic}}\{r,\cosh(\varphi_0/2)\} - F_{\text{elliptic}}\{1,\cosh(\varphi_0/2)\}\right]. \tag{B.5}$$

Substituting (B.5) in (2.23) and setting $\xi = 0$, $\varphi = \varphi_{\mathrm{s}}$ yields equation (7) of [64]. We note that while I is real, each of the two terms in (B.3) contains imaginary parts.

APPENDIX C

Asymptotes of φ_0 for the Common-Gate Symmetric DG-FinFET

We start with the unipolar IVE (2.57). In the region where ϑ is small we retain the first two terms in the Taylor series expansion

$$\ln(\vartheta \sec \vartheta) + 2 \cdot r_{\mathrm{c}} \vartheta \tan \vartheta = \ln(\vartheta) + \frac{(1 + 4 \cdot r_{\mathrm{c}})\vartheta^2}{2} + \frac{(1 + 8 \cdot r_{\mathrm{c}})\,\vartheta^4}{12} + \cdots \tag{C.1}$$

in (2.57) to yield

$$\ln(\vartheta) + \frac{(1 + 4 \cdot r_{\mathrm{c}})\vartheta^2}{2} - F_{\mathrm{b}} = 0. \tag{C.2}$$

Equation (C.2) can be solved for ϑ using the principal branch of the Lambert-W function [79]

$$\vartheta = \sqrt{\frac{W\left[(1 + 4 \cdot r_{\mathrm{c}})e^{2 \cdot F_{\mathrm{b}}}\right]}{1 + 4 \cdot r_{\mathrm{c}}}}. \tag{C.3}$$

From (2.53) and (C.3)

$$\varphi_0^{(0)} = \frac{\eta x_{\mathrm{n}}}{2} - 2 \cdot \eta \ln\left(\frac{t_{\mathrm{si}}}{4 \cdot L_{\mathrm{di}}}\right) + \eta \ln\left\{\frac{W[(1 + 4 \cdot r_{\mathrm{c}})e^{2 \cdot F_{\mathrm{b}}}]}{1 + 4 \cdot r_{\mathrm{c}}}\right\}. \tag{C.4}$$

The following approximation is valid in this region where the argument $(1+4 \cdot r_{\mathrm{c}})e^{2 \cdot F_b}$ of W is small

$$W(z) \approx \ln(1 + z) \cdot \frac{1 + \frac{123}{40}z + \frac{21}{10}z^2}{1 + \frac{143}{40}z + \frac{713}{240}z^2}. \tag{C.5}$$

Here the rational portion is the Pade approximation of $W(z)/\ln(1+z)$ was obtained by using Mathematica [102].

In the region where ϑ is close to $\pi/2$ the Taylor series expansion of

$$\ln(\vartheta \sec \vartheta) + 2 \cdot r_{\mathrm{c}} \vartheta \tan \vartheta = \frac{\pi r_{\mathrm{c}}}{\pi/2 - \vartheta} - 2 \cdot r_{\mathrm{c}} + \ln\left(\frac{\pi}{2}\right) - \ln\left(\frac{\pi}{2} - \vartheta\right) + \left(\frac{2}{\pi} - \frac{\pi r_{\mathrm{c}}}{3}\right)\left(\frac{\pi}{2} - \vartheta\right). \tag{C.6}$$

Retaining the first four terms of the series expansion in (C.6) and substituting in (2.57) yields

$$\frac{\pi r_{\mathrm{c}}}{\frac{\pi}{2} - \vartheta} - \ln\left(\frac{\pi}{2} - \vartheta\right) - 2 \cdot r_{\mathrm{c}} + \ln\left(\frac{\pi}{2}\right) - F_{\mathrm{b}} = 0. \tag{C.7}$$

Solving (C.7) for ϑ using the principal branch of the Lambert W function we obtain

$$\vartheta = \frac{\pi}{2} - \frac{\pi r_{\mathrm{c}}}{W\left[2 \cdot r_{\mathrm{c}} \exp\left(2 \cdot r_{\mathrm{c}} + F_{\mathrm{b}}\right)\right]}. \tag{C.8}$$

From (2.53) and (C.8)

$$\varphi_0^{(\pi/2)} = \frac{\eta x_{\rm n}}{2} - 2 \cdot \eta \ln\left(\frac{t_{\rm si}}{4 \cdot L_{\rm di}}\right) + 2 \cdot \eta \ln\left[\frac{\pi}{2} - \frac{\pi r_{\rm c}}{W\left(2 \cdot r_{\rm c} e^{2 r_{\rm c}} e^{F_{\rm b}}\right)}\right] \tag{C.9}$$

In this region the argument $2 \cdot r_{\rm c} e^{2 \cdot r_{\rm c}} e^{F_{\rm b}}$ of the Lambert W function in (C.9) is large and we can use the approximation suggested in [103] for $z \gg e$

$$W(z) \approx \frac{\{\ln(z) - \ln[\ln(z)]\}^2 + \ln(z)}{1 + \ln(z) - \ln[\ln(z)]}. \tag{C.10}$$

Then from (C.9) and (C.10)

$$\varphi_0^{(\pi/2)} = \frac{\eta x_{\rm n}}{2} - 2\eta \ln\left(\frac{t_{\rm si}}{4 \cdot L_{\rm di}}\right) + 2 \cdot \eta \ln\left\{\frac{\pi}{2} - \frac{\pi r_{\rm c}\left[1 + G - \ln(G)\right]}{[G - \ln(G)]^2 + G}\right\} \tag{C.11}$$

where

$$G = F_{\rm b} + 2 \cdot r_{\rm c} + \ln(2 \cdot r_{\rm c}). \tag{C.12}$$

For computational purpose we change G to $G_{\rm m}$ where

$$G_{\rm m} = \frac{1}{2}\left[G + 6 \cdot r_{\rm c} - \sqrt{(G - 6 \cdot r_{\rm c})^2 + 1}\right]. \tag{C.13}$$

APPENDIX D

Derivation of $\tilde{q}_{\mathrm{n}}$ and α_{l}

The potential $\psi(x)$ in inversion condition ($\varphi > 5$) can be obtained from (2.26) as

$$\psi(x) = \psi_0 + 2 \cdot \phi_{\rm t} \ln \left\{ \sec \left[\frac{x}{2 \cdot L_{\rm di}} \exp \left(\frac{\psi_0 - V_{\rm c}}{2\phi_{\rm t}} \right) \right] \right\}. \tag{D.1}$$

Rearranging (D.1) using (2.59) yields

$$\psi(x) = V_{\rm c} - 2 \cdot \phi_{\rm t} \ln \left[\frac{t_{\rm si}}{4 \cdot L_{\rm di}\theta} \cos \left(\frac{2 \cdot \theta x}{t_{\rm si}} \right) \right]. \tag{D.2}$$

Hence,

$$\frac{\partial \psi}{\partial y} = \left\{ \frac{\partial V_{\rm c}}{\partial y} + 2 \cdot \phi_{\rm t} \left[\frac{1}{\theta} + \frac{2 \cdot x}{t_{\rm si}} \tan \left(\frac{2 \cdot \theta x}{t_{\rm si}} \right) \right] \right\} \frac{\partial \theta}{\partial y}. \tag{D.3}$$

From (D.3)

$$\frac{\partial \psi / \partial y}{\partial \psi_{\rm s} / \partial y} = \frac{\frac{{\rm d}V_{\rm c}}{{\rm d}\theta} + 2 \cdot \phi_{\rm t} \left[\frac{1}{\theta} + \frac{2 \cdot x}{t_{\rm si}} \tan \left(\frac{2 \cdot \theta x}{t_{\rm si}} \right) \right]}{\frac{{\rm d}V_{\rm c}}{{\rm d}\theta} + 2 \cdot \phi_{\rm t} \left(\frac{1}{\theta} + \tan \theta \right)} \tag{D.4}$$

thus

$$\frac{\partial \psi / \partial y}{\partial \psi_{\rm s} / \partial y} = 1 + \frac{\tan \theta + \frac{2 \cdot x}{t_{\rm si}} \tan \left(\frac{2 \cdot \theta x}{t_{\rm si}} \right)}{2 \cdot r \left(\tan \theta + \frac{\theta}{\cos^2 \theta} \right)}. \tag{D.5}$$

where we have used (4.7). The electron concentration n can be obtained by substituting (D.2) in (2.3) to yield

$$n = n_0 \sec^2 \left(\frac{2 \cdot \theta x}{t_{\rm si}} \right) \tag{D.6}$$

where n_0 denotes the electron concentration at $x = 0$. From (D.5), (D.6), and (4.17) we obtain

$$\tilde{q}_{\rm n} = q_{\rm n} + \frac{q n_0 t_{\rm si}}{4 \cdot r_{\rm c} \theta \left(\tan \theta + \frac{\theta}{\cos^2 \theta} \right)} \int_0^\theta \frac{\tan u - \frac{u}{\theta} \tan u}{\cos^2 u} {\rm d}u \tag{D.7}$$

where it is convenient to set $q n_0 t_{\rm si} / \theta = q_{\rm n} \cot \theta$. Using standard trigonometric identities (D.7) can be reduced to (4.18).

To evaluate $\alpha_{\rm l}$ note that by (4.36)

$$\alpha_{\rm l} = 1 - \phi_{\rm t} \left(\frac{{\rm d}g_1}{{\rm d}\psi_{\rm s}} \right) \bigg|_{\psi_{\rm s} = \psi_{\rm sm}} \tag{D.8}$$

where

$$g_1 = q_{\rm i} \cdot g = \frac{\sin(2 \cdot \theta) - 2 \cdot \theta \cos(2 \cdot \theta)}{2 \cdot \theta + \sin(2 \cdot \theta)} \tag{D.9}$$

then

$$\frac{\mathrm{d}g_1}{\mathrm{d}\psi_\mathrm{s}} = \frac{\frac{\mathrm{d}g_1}{\mathrm{d}\theta}}{\frac{\mathrm{d}\psi_\mathrm{s}}{\mathrm{d}\theta}} \tag{D.10}$$

where

$$\frac{\mathrm{d}g_1}{\mathrm{d}\theta} = \frac{8\cdot\theta^2\sin(2\cdot\theta) - 4\cdot\sin(2\cdot\theta)\cos^2\theta + 8\cdot\theta\cos^2\theta}{(2\cdot\theta+\sin(2\cdot\theta))^2} \tag{D.11}$$

and $\mathrm{d}\psi_\mathrm{s}/\mathrm{d}\theta$ is found from (D.2) as

$$\frac{\mathrm{d}\psi_\mathrm{s}}{\mathrm{d}\theta} = \frac{\mathrm{d}V_\mathrm{c}}{\mathrm{d}\theta} + 2\cdot\phi_\mathrm{t}\left(\tan\theta + \frac{1}{\theta}\right). \tag{D.12}$$

Substituting $\mathrm{d}V_\mathrm{c}/\mathrm{d}\theta$ from (4.7) yields

$$\frac{\mathrm{d}\psi_\mathrm{s}}{\mathrm{d}\theta} = -4\cdot\phi_\mathrm{t} r_\mathrm{c}(\tan\theta + \theta\sec^2\theta) \tag{D.13}$$

and from (D.8), (D.9) and (D.11)

$$\alpha_\mathrm{l} = 1 + \frac{1}{r_\mathrm{c}}\cdot\frac{[2\cdot\theta_m^2\sin^2(2\cdot\theta_\mathrm{m}) - \sin(\theta_\mathrm{m})\cos^2\theta_\mathrm{m} + \theta_\mathrm{m}\cos^2\theta_\mathrm{m}]}{(2\cdot\theta_\mathrm{m}+\sin(2\cdot\theta_\mathrm{m}))^2(\tan\theta_\mathrm{m} + \theta_\mathrm{m}\sec^2\theta_\mathrm{m})} \tag{D.14}$$

where

$$\theta_\mathrm{m} = \theta|_{\psi_\mathrm{s}=\psi_\mathrm{sm}}. \tag{D.15}$$

An equivalent form is

$$\alpha_\mathrm{l} = 1 + \frac{\theta_m^2}{2\cdot r_\mathrm{c}}\cdot\frac{q_\mathrm{im}(2\cdot q_\mathrm{im}^2 + 2\cdot\theta_\mathrm{m}^2 - 1) + q_\mathrm{im}^2 + \theta_\mathrm{m}^2}{(q_\mathrm{im}^2 + q_\mathrm{im} + \theta_\mathrm{m}^2)^3}. \tag{D.16}$$

While for common-gate symmetric DG-FinFETs q_im is given by (4.42), the corresponding approximation $\theta_\mathrm{m}^2 = \theta_0^2 \equiv (\theta_\mathrm{s}^2 + \theta_\mathrm{d}^2)/2$ for θ_m^2 is valid only in weak inversion where $q_\mathrm{i} = \theta\tan\theta \approx \theta^2$. Since in strong inversion, $q_\mathrm{im} \gg \theta_\mathrm{m}^2$ an approximation [67]

$$\alpha_\mathrm{l} = 1 + \frac{\theta_\mathrm{m}^2}{2\cdot r_\mathrm{c}}\cdot\frac{q_\mathrm{im}(2\cdot q_\mathrm{im}^2 + 2\cdot\theta_0^2 - 1) + q_\mathrm{im}^2 + \theta_0^2}{(q_\mathrm{im}^2 + q_\mathrm{im} + \theta_0^2)^3} \tag{D.17}$$

is quite accurate in all regions of DG-FinFET operation. However, approximating θ_m^2 by θ_0^2 in (D.17) does not result in accurate expressions for Q_G and Q_D. Better accuracy is achieved by setting $\theta_\mathrm{m}^2 = 3\cdot q_\mathrm{im}/4$ i.e. by using α_l in the form given by

$$\alpha_\mathrm{l} \approx 1 + \frac{3\cdot q_\mathrm{im}}{8\cdot r_\mathrm{c}}\cdot\frac{q_\mathrm{im}(2\cdot q_\mathrm{im}^2 + 2\cdot\theta_0^2 - 1) + q_\mathrm{im}^2 + \theta_0^2}{(q_\mathrm{im}^2 + q_\mathrm{im} + \theta_0^2)^3}. \tag{D.18}$$

This conclusion is invariant of device parameters such as t_ox and t_si. Without adding much error further simplification is made to (D.18) in [63] by setting θ_0^2 in (D.18) to q_im which gives (4.41).

APPENDIX E

Comparison of Symmetric Linearization Method for bulk MOSFETs and DG-FinFETs

For both DG-FinFETs and bulk MOSFETs symmetric linearization is introduced to obtain compact expressions for the terminal charges. The difference is that in the case of the bulk device symmetric linearization is required for the inversion charge while for undoped DG-FinFETs the inversion charge

$$Q_{\mathrm{i}} = -q_{\mathrm{n}} = -2 \cdot C_{\mathrm{ox}}(V_{\mathrm{g}} - \Delta\phi - \psi_{\mathrm{s}}) \tag{E.1}$$

is already a linear function of ψ_{s}. However, the surface potential dependence of the "effective charge" $\tilde{q}_{\mathrm{n}}$ is nonlinear necessitating the approximation given by (4.33). In other words, for DG-FinFETs the complexity of the model comes from the fact that, generally speaking, $\partial\psi/\partial y \neq d\psi_{\mathrm{s}}/dy$ and symmetric linearization approximation is introduced in order to account for this complication in a computationally efficient way.

The second difference is that the value of ν in this work selected so as to make the expression (4.25) for I_{d} not just accurate but exact. This approach is also applicable to bulk MOSFETs. Indeed, the equations for the drain current in [90, 41] can be written in the form

$$I_{\mathrm{d}} = \mu \frac{W}{L} C_{\mathrm{ox}} \left[V_{\mathrm{gb}} - V_{\mathrm{fb}} - \psi_{\mathrm{sm}} + \phi_{\mathrm{t}} \left(1 + \frac{\gamma}{\sqrt{a} + \sqrt{b}} \right) - \frac{(2 \cdot \gamma/3)(2 \cdot \psi_{\mathrm{m}} - 2 \cdot \phi_{\mathrm{t}} + \sqrt{ab})}{\sqrt{a} + \sqrt{b}} \right] \Delta\psi \tag{E.2}$$

where W is the width of the channel, V_{fb} denotes flat-band voltage, γ is the body effect factor, $a = \psi_{\mathrm{sd}} - \phi_{\mathrm{t}}$ and $b = \psi_{\mathrm{ss}} - \phi_{\mathrm{t}}$.

Using the version of the symmetric linearization method in the form

$$Q_{\mathrm{i}} = -C_{\mathrm{ox}}(\nu - \alpha_{\mathrm{l}} u) \tag{E.3}$$

and proceeding as in [88] yields

$$I_{\mathrm{d}} = \mu \frac{W}{L} C_{\mathrm{ox}}(\nu + \alpha_{\mathrm{l}} \phi_{\mathrm{t}}) \Delta\psi. \tag{E.4}$$

It is now possible to select ν so that (E.4) coincides with the exact result (E.2):

$$\nu = V_{\mathrm{gb}} - V_{\mathrm{fb}} - \psi_{\mathrm{m}} - \frac{(2\cdot\gamma/3)(2\cdot\psi_{\mathrm{m}} + 2\cdot\phi_{\mathrm{t}} + \sqrt{ab})}{\sqrt{a}+\sqrt{b}} + \phi_{\mathrm{t}}\left(1 + \frac{\gamma}{\sqrt{a}+\sqrt{b}} - \alpha_{\mathrm{l}}\right) \quad \text{(E.5)}$$

The linearization coefficient α_{l} can be selected as in [88, 89]

$$\alpha_{\mathrm{l}} = 1 + \frac{\gamma}{2\cdot\sqrt{\psi_{\mathrm{sm}} - \phi_{\mathrm{t}}}} \quad \text{(E.6)}$$

or as

$$\alpha_{\mathrm{l}} = 1 + \frac{\gamma}{\sqrt{a}+\sqrt{b}}. \quad \text{(E.7)}$$

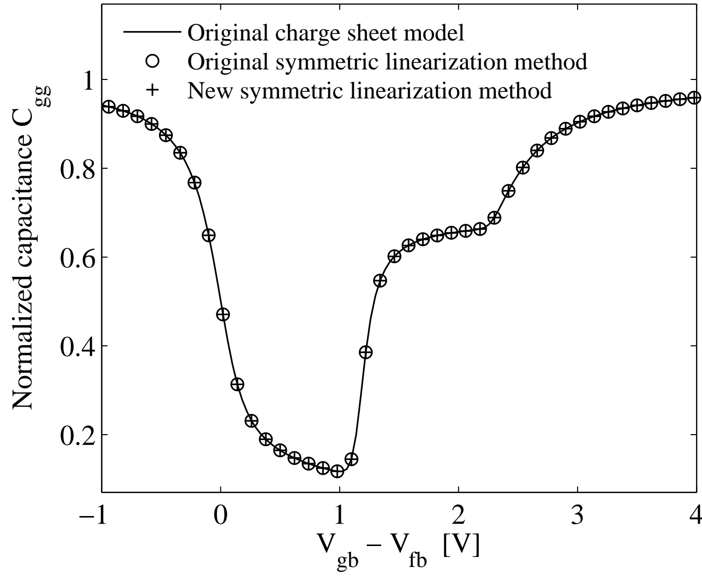
The essence of symmetric linearization, however, is to obtain simple but accurate approximations for the terminal charges. Following [88] or Section 4.4 we obtain (4.43)-(4.47) with

$$H = \frac{\nu}{\alpha_{\mathrm{l}}} + \phi_{\mathrm{t}} \quad \text{(E.8)}$$

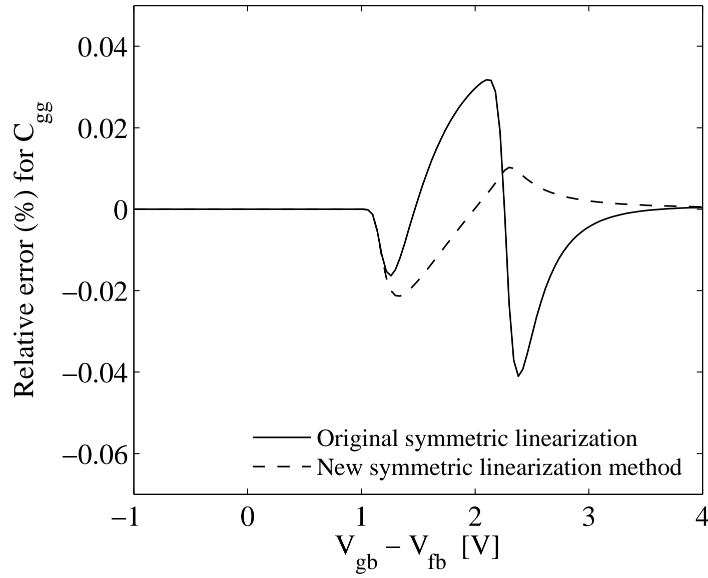
the only difference being that ν and α_{l} are now given by (E.5) and (E.6). The total gate charge, Q_{G}, is still given by (4.52) (without the coefficient 2), while

$$Q_{\mathrm{D}} = -WLC_{\mathrm{ox}}\left[\frac{\nu}{2} - \frac{\alpha_{\mathrm{l}}\Delta\psi}{12}\left(1 - \frac{\Delta\psi}{2\cdot H} - \frac{\Delta\psi^2}{20\cdot H^2}\right)\right] \quad \text{(E.9)}$$

As shown in Fig. E.1, for charges this approach produces results that are even more accurate than the symmetric linearization version developed in [88]. However, this requires using expression (E.5) which is more complex than the approximation $\nu = -(Q_{\mathrm{i}}|_{\psi=\psi_{\mathrm{sm}}})/C_{\mathrm{ox}}$ used in [88]. In contrast, for undoped DG-FinFETs (4.39) results in a model that is both simpler and more accurate than that based on (4.35). This explains the difference in our implementation of the symmetric linearization method in this work relative to [88, 89].



(a)



(b)

Figure E.1: (a) Normalized transcapacitance C_{gg} using original charge sheet model [89, 104], and two versions of symmetric linearization; (b) Relative error (%) for C_{gg} for present technique and symmetric linearization of [88]; $N_{\mathrm{A}} = 3 \times 10^{17}$ cm^{-3}, $t_{\mathrm{ox}} = 2.5$ nm and $V_{\mathrm{ds}} = 1$ V, $V_{\mathrm{bs}} = 0$ V.

APPENDIX F

Derivation of (5.74)-(5.77)

We present a derivation of expressions (5.74)-(5.77) for the hyperbolic case. Expressions (5.69)-(5.73) for the trigonometric case are derived similarly. Substitution of (3.39) in (5.53) and integration yields (5.74) once it is noted that from (3.30) $E(\sigma \cdot \infty) = 4 \cdot \sigma \phi_{\mathrm{t}} \theta_* / t_{\mathrm{si}}$. Similarly, (5.75) follows from (5.54) and (3.39).

The derivation of (5.76) requires evaluation of the integral in (5.55). For this purpose, we differentiate (3.27) with respect to y to obtain

$$\frac{\partial \psi}{\partial y} = \frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}y} + \frac{2 \cdot \phi_{\mathrm{t}}}{\left[\theta_* \mathrm{csch}\left(\alpha_* + \sigma \frac{2 \cdot \theta_* x}{t_{\mathrm{si}}}\right)\right]} \times \frac{\partial}{\partial y}\left[\theta_* \mathrm{csch}\left(\alpha_* + \sigma \frac{2 \cdot \theta_* x}{t_{\mathrm{si}}}\right)\right] \tag{F.1}$$

where from (3.35)

$$\frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}y} = -\frac{2 \cdot \phi_{\mathrm{t}}}{\theta_* \mathrm{csch}(\alpha_* - \sigma\theta_*)} \frac{\mathrm{d}}{\mathrm{d}y}\left[\theta \mathrm{csch}(\alpha_* - \sigma\theta_*)\right] - 4 \cdot \sigma \phi_{\mathrm{t}} r_{\mathrm{c}1} \frac{\mathrm{d}}{\mathrm{d}y}[\theta_* \coth(\alpha_* - \sigma\theta_*)] \tag{F.2}$$

Setting $x = -t_{\mathrm{si}}/2$ in (F.1) yields

$$\frac{\mathrm{d}\psi_{\mathrm{s}1}}{\mathrm{d}y} = -4 \cdot \sigma \phi_{\mathrm{t}} r_{\mathrm{c}1} \frac{\mathrm{d}}{\mathrm{d}y}[\theta_* \coth(\alpha_* - \sigma\theta_*)] \tag{F.3}$$

Substitution of $n(x)$, $\partial\psi/\partial y$, and, $\mathrm{d}\psi_{\mathrm{s}1}/\mathrm{d}y$ from (3.39), (F.2) and (F.3), respectively, in (5.55) and integration yields (5.76). The derivation of (5.77) follows the same lines, except that now it is convenient to obtain $\mathrm{d}V_{\mathrm{c}}/\mathrm{d}y$ from (3.36) rather than (3.35):

$$\frac{\mathrm{d}V_{\mathrm{c}}}{\mathrm{d}y} = -\frac{2 \cdot \phi_{\mathrm{t}}}{\theta_* \mathrm{csch}(\alpha_* + \sigma\theta_*)} \frac{\mathrm{d}}{\mathrm{d}y}\left[\theta_* \mathrm{csch}(\alpha_* + \sigma\theta_*)\right] + 4 \cdot \sigma \phi_{\mathrm{t}} r_{\mathrm{c}2} \frac{\mathrm{d}}{\mathrm{d}y}[\theta_* \coth(\alpha_* + \sigma\theta_*)] \tag{F.4}$$

Finally, (5.73) is obtained by differentiating (3.37).

APPENDIX G

Common-Gate Symmetric DG-FinFET as a Special Case of Independent-Gate Asymmetric DG-FinFET

It is worth noting that we can get the drain current and $\tilde{q}_\mathrm{g}$ for a common-gate symmetric DG-FinFET defined in [67] as a special case of (5.8) and (5.71), respectively. In common-gate symmetric DG-FinFETs we have $V_1 = V_2$, $r_\mathrm{c1} = r_\mathrm{c2} = r_\mathrm{c}$, $\alpha = \pi/2$ and the $\psi(x)$ has a trigonometric form [69]. Thus, considering the drain current expression for case I we have

$$I_\mathrm{d} = 8 \cdot \mu \frac{h_\mathrm{f}}{L} C_\mathrm{si} \phi_\mathrm{t}^2 (f_\mathrm{d} - f_\mathrm{s}) \tag{G.1}$$

where

$$f = -\left[r_\mathrm{c1} u_-^2 + r_\mathrm{c2} u_+^2 - \theta^2\right] - [u_- u_+] \tag{G.2}$$

and

$$u_\pm = \theta \cot(\alpha \pm \theta) = \theta \cot\left(\frac{\pi}{2} \pm \theta\right) = \mp \theta \tan \theta. \tag{G.3}$$

Hence (G.2) becomes

$$f = -\left[2 \cdot r_\mathrm{c} \theta^2 \tan^2 \theta - \theta^2\right] - 2 \cdot \theta \tan \theta. \tag{G.4}$$

Substituting (G.4) in (G.1) the expression for drain current becomes

$$I_d = 16 \cdot \mu \frac{W}{L} C_\mathrm{si} \phi_\mathrm{t}^2 \left(r_\mathrm{c} \theta^2 \tan^2 \theta - \frac{\theta^2}{2} + \theta \tan \theta \right) \Bigg|_{\theta_\mathrm{d}}^{\theta_\mathrm{s}}. \tag{G.5}$$

The equation (G.5) is the equation for the drain current of common symmetric DG-FinFET [60].

Symmetry allows us to write

$$q_\mathrm{g1} = q_\mathrm{g2} = \frac{q_\mathrm{g}}{2} \tag{G.6}$$

and

$$\tilde{q}_\mathrm{g1} = \tilde{q}_\mathrm{g2} = \frac{\tilde{q}_\mathrm{g}}{2}. \tag{G.7}$$

The constant α results in $\mathrm{d}\alpha/\mathrm{d}\theta = 0$ which is consistent with (5.73) for $\alpha = \pi/2$. Substituting $\alpha = \pi/2$ and $\mathrm{d}\alpha/\mathrm{d}\theta = 0$ in (5.71)

$$\tilde{q}_\mathrm{g1} = q_\mathrm{g1} + C_\mathrm{ox} \phi_\mathrm{t} \frac{\sin(2 \cdot \theta) - 2 \cdot \theta \cos(2 \cdot \theta)}{2\theta + \sin(2\theta)}. \tag{G.8}$$

From (G.6)-(G.8),

$$\tilde{q}_{\mathrm{g}} = q_{\mathrm{g}} + 2 \cdot C_{\mathrm{ox}} \phi_{\mathrm{t}} \frac{\sin(2 \cdot \theta) - 2 \cdot \theta \cos(2 \cdot \theta)}{2 \cdot \theta + \sin(2 \cdot \theta)} \tag{G.9}$$

which is precisely the result given in [67] for common-gate symmetric DG-FinFETs.