Triple Sampling an Application to a 14b 10MS/s Cyclic ADC

by

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ABSTRACT

Semiconductor device scaling has kept up with Moore's law for the past decades and they have been scaling by a factor of half every one and half years. Every new generation of device technology opens up new opportunities and challenges and especially so for analog design. High speed and low gain is characteristic of these processes and hence a tradeoff that can enable to get back gain by trading speed is crucial. This thesis proposes a solution that increases the speed of sampling of a circuit by a factor of three while reducing the specifications on analog blocks and keeping the power nearly constant. The techniques are based on the switched capacitor technique called Correlated Level Shifting. A triple channel Cyclic ADC has been implemented, with each channel working at a sampling frequency of 3.33MS/s and a resolution of 14 bits. The specifications are compared with that based on a traditional architecture to show the superiority of the proposed technique.

DEDICATION

I dedicate this work to my beloved family, my wonderful friends and the excellent professors at ASU

ACKNOWLEDGMENTS

First and foremost I would like to thank my advisor Dr.Bahar Jalali Farahani who provided me with this opportunity to work under her on this topic and for supporting this research; it has been a great pleasure working under her. I would also like to thank Dr.Bertan Bakkaloglu, who offered some spectacular classes in analog design, which I just had to attend more than one time, just to enjoy them during which period, I also had a wonderful chance to get to know him – he has shown me to smile at every situation and face it and never to be "too busy" for anyone. I am also deeply indebted to Dr.Douglas Garrity for a lot of things; his encouragement on my work, his wonderful classes on data converters and his recommendations for teaching assistantships and for letting me attend his classes. I should say I learned more from his classes than I did from my research, I have also learnt to be dedicated to work and to enjoy helping others from him. I wish to thank Dr.James Aberle for his amazing courses which I thoroughly enjoyed and also for teaching how important it is to be so polite and kind. I wish to thank Dr.Joseph Palais for providing my with teaching assistantships for my last year at ASU so I could continue to work on my thesis, it was a really good experience for me to have been a teaching assistant, the students were all very interactive and I have made some very lasting friendships during the time and I learnt a lot by being a teaching assistant and I wish to thank Dr.Garrity once again for that opportunity and his interactions with me, I hope I did not fail his expectations.

I wish to thank my parents for offering me great support and inspiration during my tough times, I hope I make them proud someday. I should specially thank Sami for his unwavering support through some of the toughest times I faced during my PhD,

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Finally, I genuinely, whole-heartedly, sincerely wish to thank the companies that interviewed me and turned me down. They lit the raging fires inside me to learn more and to make myself worthy. If not for the smaller failures they had given me, I would have never achieved the great success of becoming a Senior Engineer in one of the best teams at one of the biggest companies after clearing the toughest set of interviews I ever faced.

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Chapter 1

INTRODUCTION

CMOS technology has so far kept up with the Moore's law by scaling a factor of two each one and half years. However, the improvement of the resolution of ADCs for a given power consumption has been about 1.5b in eight years. Data converters are ubiquitous in our world. They are used in many areas, ranging from remote sensing in satellites to simple weighing scales to cars for tire pressure sensing, radar sensing etc. They also play a very important role in radio communication systems, so important in fact that they set the performance limitations on the entire signal chain.

As CMOS technology scales down it imposes serious challenges for the design of high performance analog circuits and specifically on data converters. The difficulties arise due to the low intrinsic gain of transistors, degraded matching properties due to smaller device sizes and limited voltage swings [6]. Low intrinsic gain from the transistors requires that there be multi stage designs to attain the same gain. Lower voltage swings automatically enforce constraints on selecting architectures like the cascodes due to their high voltage headroom issues. As device sizes shrink, matching initially improves because of the tighter control of Cox [22], however the device width and length decrease faster due to a constant aspect ratio, which reduces area and hence matching degrades [22].

The domains of the data converters can be classified based on the speed and the resolution of the converter. Some important domains are high speed low resolution and

low speed high resolution and moderate speed, moderate resolution. The work on this thesis is more inclined towards high resolution moderate speed ADCs. Such ADCs are required for example in the radar systems used in cars. Other implementations of the technique described have also been performed; namely, a moderate speed and moderate resolution ADC was designed using this technique for the Large Hadron Collider system [28], this ADC had 12b resolution and worked at 25Msps and was a pipeline ADC. Similarly, a high speed moderate resolution ADC was designed for the ice penetrating radar in the NASA's flagship mission to Europa, one of Jupiter's moons, this ADC had 12b of resolution and worked at 125 MS/s and again was a pipeline ADC [27].

The following section discusses the various ADC architectures that are most commonly seen in the moderate to high resolution converters regime.

1.2 SAR ADC

The SAR is an acronym that stands for Successive Approximation Register. The SAR ADC uses the binary search algorithm to deduce the binary equivalent of an analog input. The logic of this operation is shown in Fig 1-1.

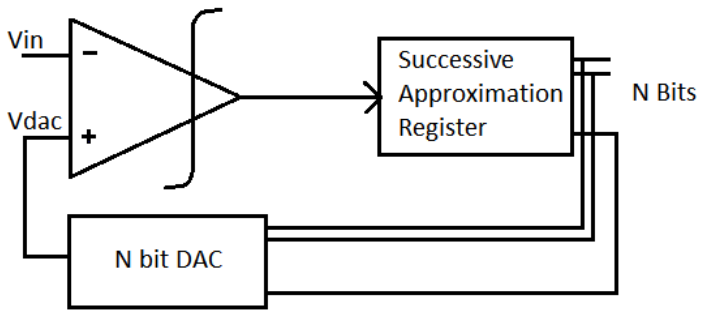

Figure 1- 1: SAR Logic

Traditional SAR architecture used binary weighted capacitors to implement this algorithm. The circuit for this is shown in Fig 1-2. However, for even moderate resolutions, the capacitor spread (ratio of biggest capacitor to smallest capacitor) can be prohibitively high, given by 2^N where N is the resolution. Hence a scale down capacitor or multiple scale down capacitors can be used to reduce the capacitor spread.

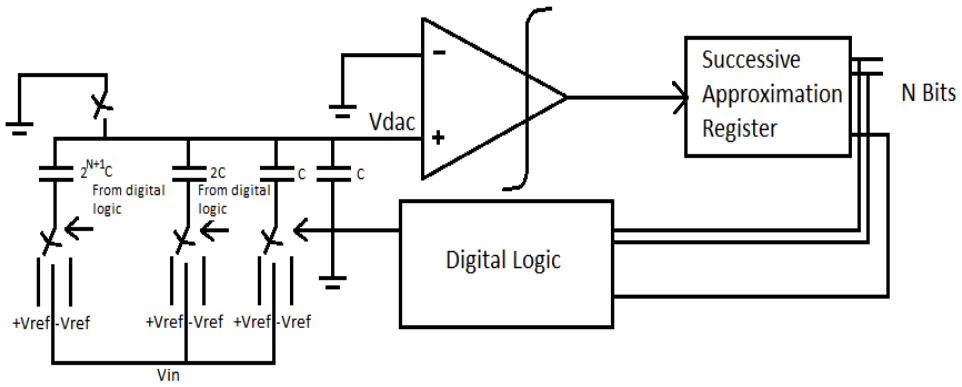

Figure 1- 2: Traditional SAR ADC

1.3 Sigma Delta ADCs

The Sigma-Delta or the Delta-Sigma ADC is a very good choice for high dynamic range or high resolution conversion needs. The ADC relies on the negative feedback concept on a system level and high gain at selected frequencies so that the digital output equals the analog input in a transient sense with very high resolution. The quantization noise from the conversion is pushed inside the loop and is pushed out into the regions where the loop gain is designed to be low. This is called noise shaping and

since it requires frequency space to be pushed into, typically higher OSR than other converters are required.

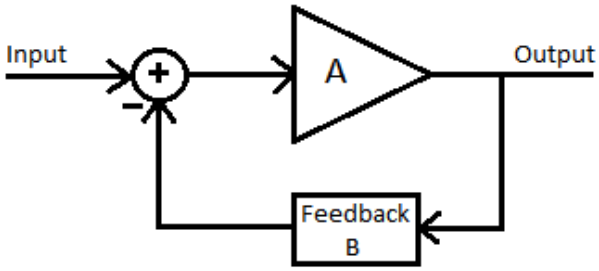

Figure 1- 3: Negative Feedback System

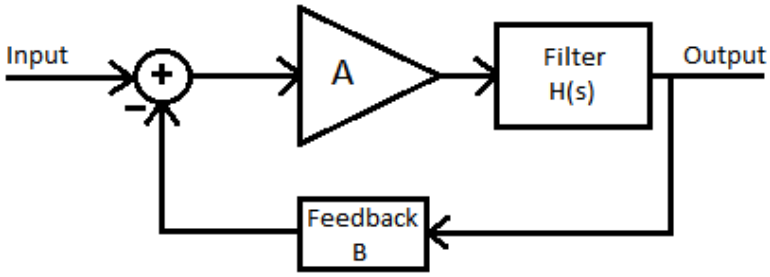

Figure 1- 4: Frequency Selective Negative Feedback System

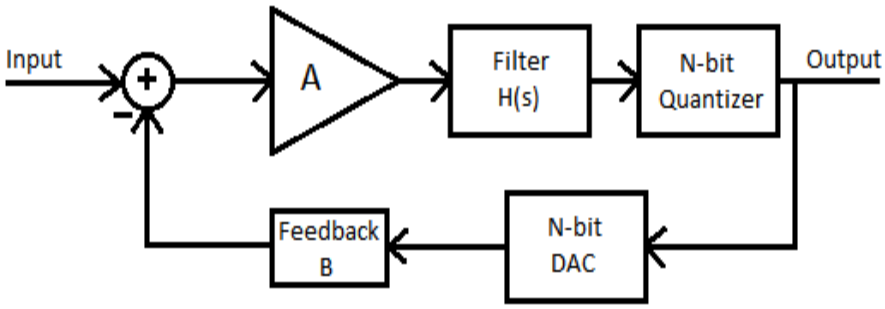

Figure 1- 5: Frequency Selective Negative Feedback System with ADCs and DACs – A Sigma Delta

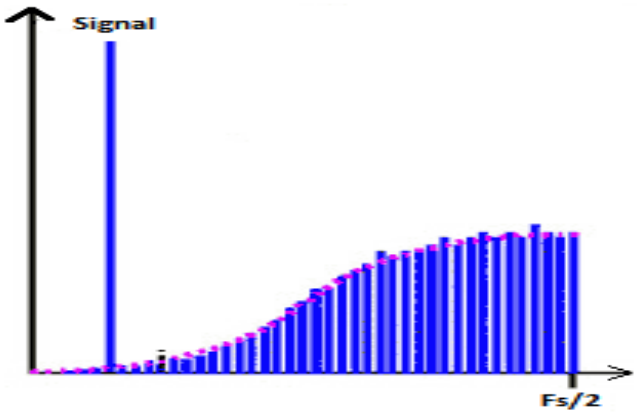

Figure 1- 6: Noise Shaping Response of the System

Fig 1-3 shows a negative feedback system most commonly encountered in analog circuit design. Provided that negative feedback exists and there is high gain in the loop, the amplifier's two input terminals have a virtual short circuit, forcing the output to follow the input. These two conditions can be manipulated to get a sigma delta ADC. Now suppose as in Fig 1-4, a filter is added in the loop, the gain is now high only in certain frequencies (low frequency for low pass and high frequency for high pass etc.), thus the output would have to track the input only at these frequencies and at the other

frequencies where the attenuation of the filter is high, there is no virtual short, thus, any disturbance inside the forward path of the loop is not suppressed by the loop gain and shows up at the output at these frequencies.

As shown in Fig 1-5, to convert the analog signal to digital, we can add a simple ADC to the end of the forward path, thus we get digital output from the loop, but we cannot feedback a digital signal, hence, we can use a simple DAC to the feedback to provide the analog equivalent to the input. The ADC and DAC can be as simple as a quantizer and a pair of switches connecting to either Vdd or ground. Now the system remains the same, analog input and analog feedback, but the output is digital.

This system is still recognizably the standard negative feedback system with gain at selected frequencies. Typically, the filter, quantizer or the ADC inside the loop can be designed with high enough gain such that a separate gain element is not needed. The resulting structure is shown in Fig 1-5. The system's output will match the input with high precision where ever the gain is high. The quantization noise of the coarse ADC inside the loop is suppressed by the high loop gain at the frequencies of interest and pushed out to other frequencies as shown in Fig 1-6, which is called noise-shaping.

The system can be made to work with arbitrarily high resolution, provided there is enough oversampling and enough time for the system to settle down to match the input. There are multiple constraints and cautions that need to be addressed while using or designing a sigma delta ADC, like the maximum input the system can take, the OSR, order of the loop filter, number of bits to use inside the coarse ADC etc. These can be found in good references like [25] and are beyond the scope of this thesis.

Even when all these considerations are addressed, the inherent nature of the sigma delta to need a slow varying signal and its inability to process multiple signals in a short span and its latency together make is unusable for certain applications, like for instance in high speed conversions, polling systems or control systems. However, with technology progress helping make digital systems faster, the loop works at higher frequency and the ADC works at higher frequency and more sigma deltas will be seen in future designs.

1.4 Pipeline and Cyclic Data Converters

Pipeline ADC converters have a high throughput or a conversion rate between 10Msps to even 500 MS/s with moderate to moderately high resolution of about 8-15 bits, but with latency. Certain applications like control systems cannot tolerate latency, but most other applications like video, radar etc need high speed, high resolution conversion but can tolerate latency. In such cases, pipelines are a great fit.

The pipeline architecture is very intuitive in its native form, a coarse ADC is used to make a conversion, then the quantization error or more appropriately, the residue is passed on to another ADC, this ADC resolves some more of the signal, adding more bits to the conversion and produces another quantization error. This logic is shown in Fig 1-7. A basic pipeline architecture is shown in Fig 1-8.

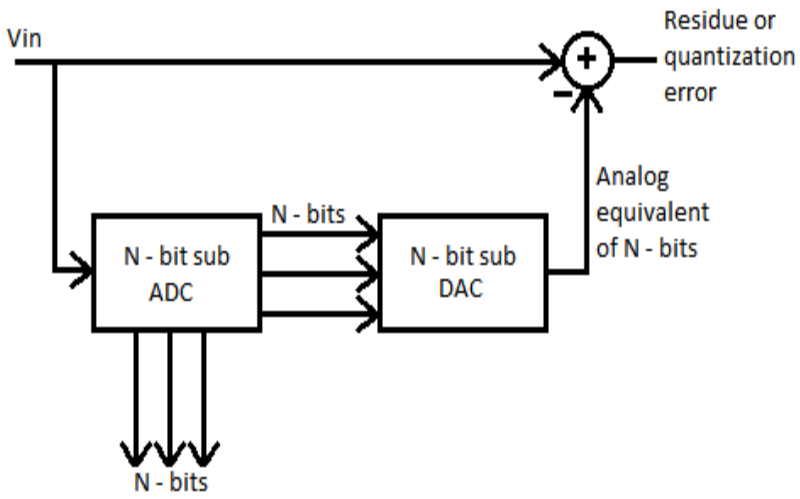

Figure 1- 7: Passing of Quantization Error

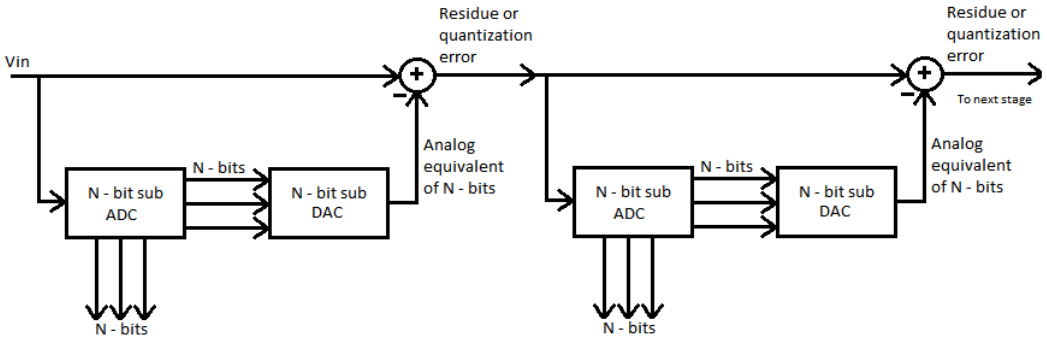

Figure 1- 8: Pipeline Architecture Intuitive Logic

The ADCs have to get better in resolution along the chain for this architecture. To remove this disadvantage, a gain stage can be added to each stage to keep the signal range the same and to make easier ADCs towards the end of the chain as shown in Fig 1-9. This scaling of the residue with each stage also has the advantage of reducing the noise when referred back to the input according to the Frii's equation. Further, since scaling is done such that the quantization error is full scale to the next stage, each time

the comparison inside the ADC is performed with the same reference values, which removes the need to have a new reference value each time.

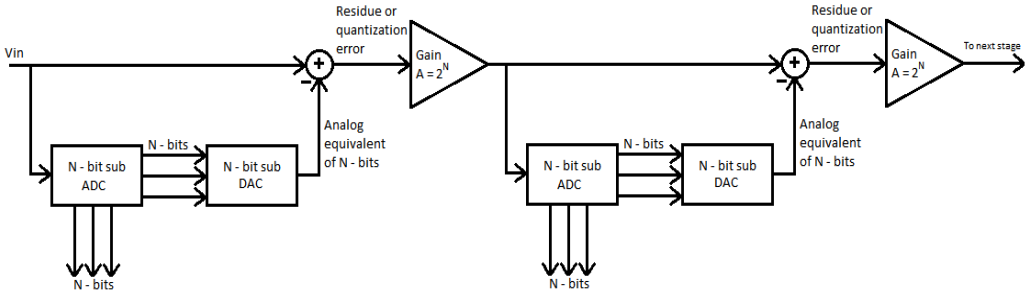

Figure 1- 9: Better Implementation of pipeline with interstage gain elements

As can be seen, each clock cycle, a bit is added to the conversion and also, a new stage operates on the residue, making the previous stage available to process a new value. The pipelining of the operations to increase the throughput and hence the sampling speed gives this ADC its name.

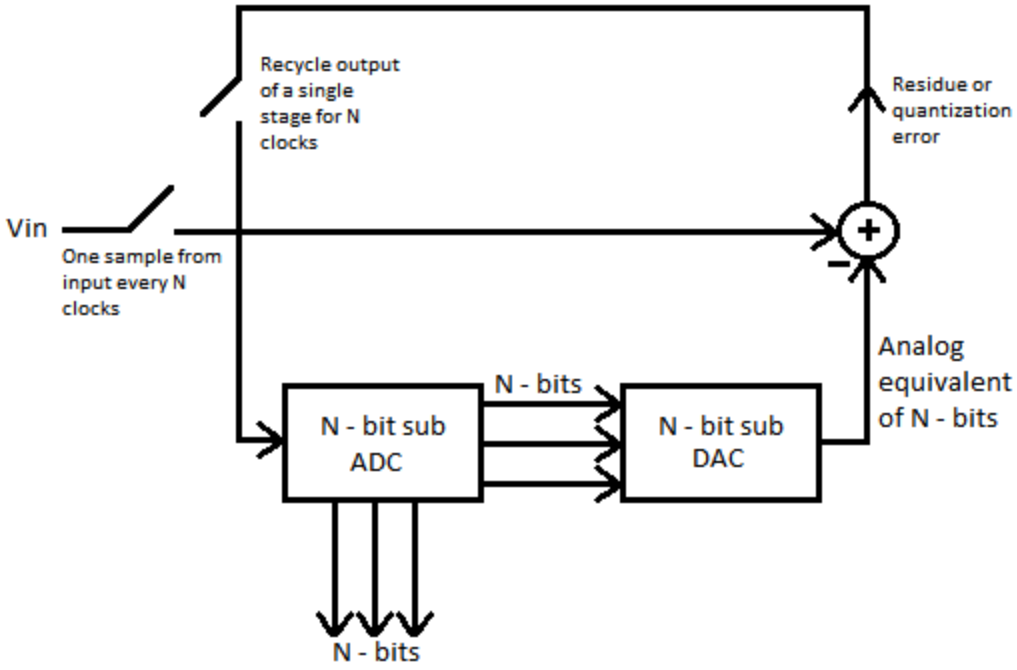

Figure 1- 10: Cyclic ADC Core Logic

A cyclic ADC is a sub class of pipeline ADCs where only a single stage of the pipeline exists and the residue it generates is passed on to itself for the next clock cycle. The core logic is shown in Fig 1-10. Since only one stage is used, the area it consumes is minimal compared to the pipeline ADC, however the sampling rate has reduced compared to the pipeline ADC. This type of architecture can be very useful when high resolution, moderate speed conversion is needed with low area, like in automotive systems.

This intuitive architecture is easy to understand, however has issues that need to be addressed, this has been explained in the following chapter and it also explains the Redundant Signed Digit (RSD) concept that is almost universally implemented to overcome these issues.

1.5 Conclusion

This thesis is organized as follows: Chapter 1 provides an introduction to the background of the work and data converters and the regimes. Chapter 2 provides a detailed description of conventional switch capacitor circuits and the implementation of the pipeline ADCs using switch capacitor techniques. Chapter 3 presents the Correlated Double Sampling technique and the more recently developed Correlated Level Shifting technique and Split CLS techniques. Chapter 4 presents a previously developed technique called Double sampling and the new technique called Triple Sampling technique in detail and its advantages. Chapter 5 presents the implementation of triple sampling with various architectures of Opamps to serve as a guide line in selecting amplifiers. Chapter 6 presents the implementation of a Cyclic ADC with the triple sampling technique and presents the amplifiers, CMFB circuits and other analog components. Chapter 7 presents the digital part of the ADC such as the digital error correction and recombination block of the ADC. Chapter 8 presents the layout of the ADC with the floor plan, matching components. Chapter 9 presents additional simulation results of the ADC and triple sampling scheme.

Chapter 2

PIPELINE ARCHITECTURE

2.1 Introduction

Chapter 1 introduced a multitude of data converters that are dominant in the field currently. It also introduced the concept of pipeline data conversion that has a high throughput of data with moderately low to moderately high resolution of conversion. This chapter describes the pipeline converter in greater detail and its implementation details in traditional CMOS techniques.

2.2 Intuitive Method of the Pipeline Converter

When quantizing an input signal y, the output digital bits represent an approximation of the input signal y', the error between y and y' is the quantization error e. Ideally, y and y' must be the same, which means the ADC has infinite resolution, but for practical ADCs with finite resolution, the error e is set by the accuracy limitation of the ADC and is within LSB/2. The input signal can be expressed as a sum of the digital value y' and the error e:

$$y = y' + e$$

As can be seen from the equation, if e can be minimized or if e can be measured and added to the digital equivalent y', then the representation y' becomes more accurate and e is minimized further, in other words, the resolution of the ADC increases. Using a

low resolution ADC, a conversion is first performed, the error between the actual input and the resolved signal can be minimized by passing on this error, resolving it further and adding it to the previously resolved input. As this cycle continues, the resolved signal gets closer to the actual input.

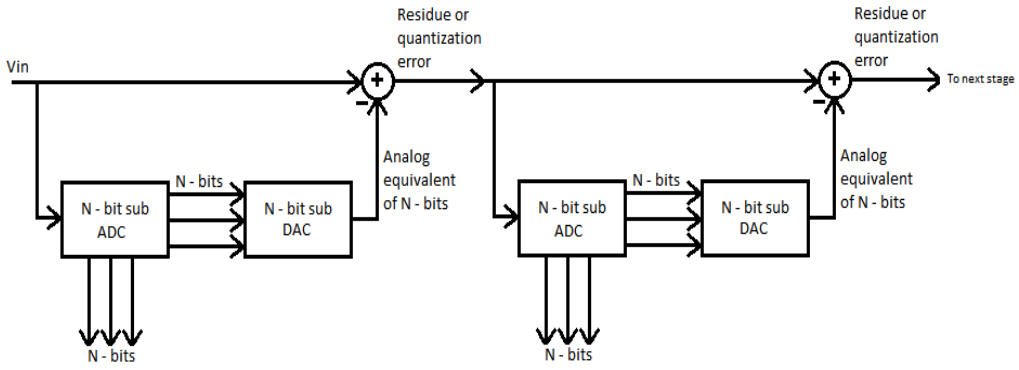

Figure 2 -1: Pipeline of ADCs

2.3 The Use of a Gain Stage in between Conversions:

A gain stage is included in between the stages such that the residue signals at the output of each sub ADC are full scale. This helps the ADC such that each stage along the chain has to resolve a bit with a lower accuracy and noise limitation, since the signal has already undergone amplification by all the previous stages. Thus, typically the gain stages and the ADC along the chain are easy to design. This is the traditional architecture, however the architecture is almost universally implemented using the redundant signed digit architecture to overcome certain issues in this methodology, namely, the comparator offsets, the opamp offset. The issues and the solution will be explained in the following discussion.

The general architecture was shown in Fig 1-8 and has been reproduced here with the gain stage included in between for a more complete picture in Fig 2-1, a more detailed version is shown in Fig 2-2. Each stage has a sub-ADC which makes a comparison with references and decides M bits. The analog equivalence of the M bits are obtained from the M bit DAC, this is then subtracted from the input signal to obtain the residue or the quantization error from the stage. This is then gained up to match the full scale of the next stage.

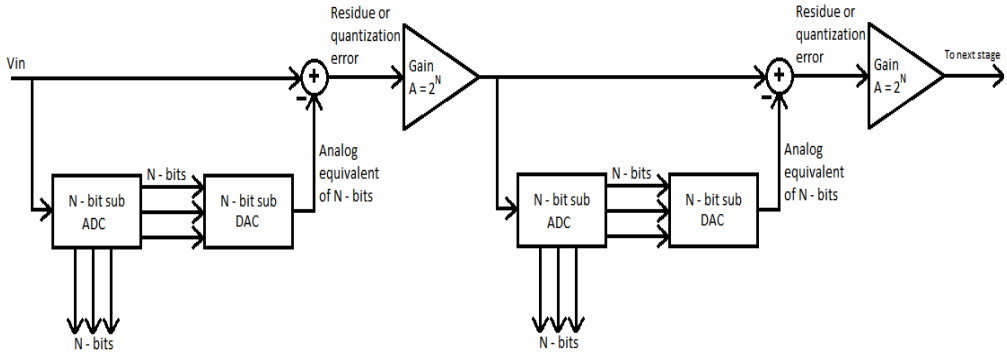

Figure 2 – 2: Pipeline Architecture with Inter-stage gain element

The residue plot for the diagram is as shown in Fig 2-3. The input can range from –Vref to +Vref, inherently the input is compared with one reference levels at 0 and the following output is calculated as the residue:

$$Vin < 0, \qquad Vres = 2Vin + Vref$$

$$Vin > 0, \qquad Vres = 2Vin - Vref$$

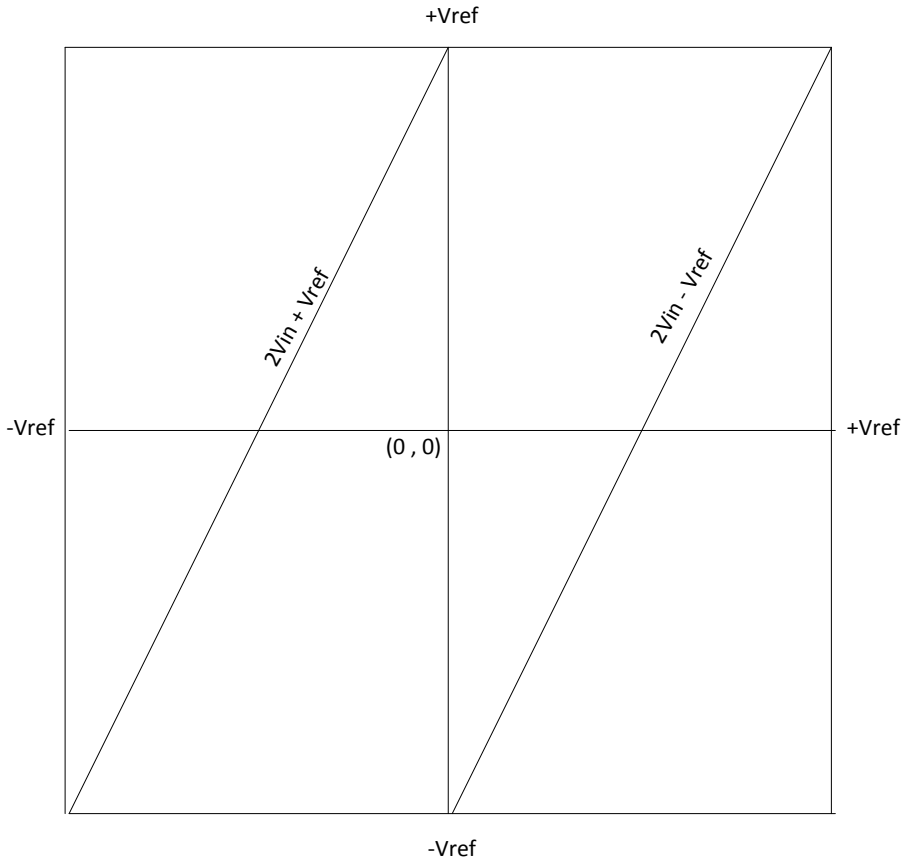

Figure 2 – 3: Conventional Pipeline Residue Plot

The equations for Vres are straight lines and can be plotted versus Vin. This gives the graph in Fig 2-3. The graph has also incorporated a box around the residue plot enclosing a range from –Vref to +Vref for the residue voltages, which are the acceptable regions for the residue voltage. If for example, the residue voltage goes outside the box,

the input to the next stage is larger than Vref and that stage would also generate a residue greater than Vref and hence this process will continue until the entire ADC is saturated. During normal operation of the pipeline, if the input to the first stage of the ADC is within the reference Vref, then the ADC does not saturate.

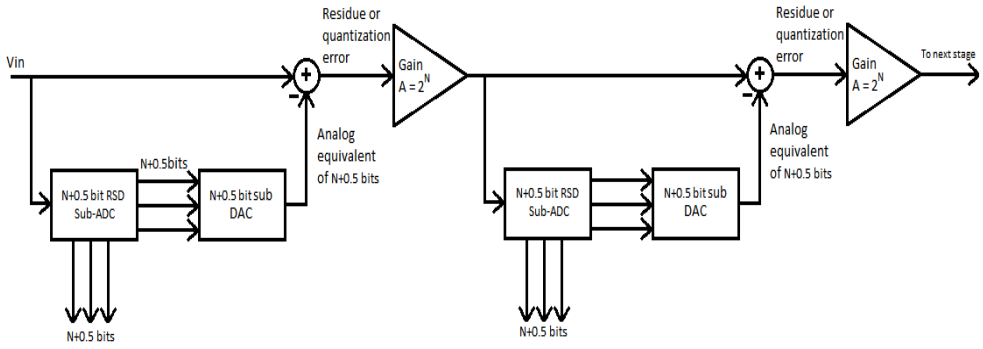

Figure 2- 4: RSD Architecture Pipeline

If there is a small offset in the comparator or the opamp and the decision threshold moves from either –Vref/2 or +Vref/2, then the residue output can cross the boundary and go outside the box as shown in Fig. This requires high precision comparators and given that they also need to work at high speeds, the design of these comparators can be very difficult. The residue can go over-range even if there is a small difference in the gain higher than the intended value, which is 2 for the case of a 1.5b stage.

To alleviate these issues, a technique called Redundant Signed Digit (RSD) is used. In the conventional architecture, a single stage of the pipeline generates M bits and if there are K stages, then the final resolution of the ADC is MxK bits. In the RSD

architecture, as will be seen, each stage generates M+1 bits per stage, however, the last bit is redundant and is combined with one bit from the next stage, hence the name, redundant sign digit. The architecture is shown in Fig 2-4.

Internally, the input is compared with three different voltage levels for a 1.5 bit stage of RSD at -Vref/4 and + Vref/4 and the residue voltages are calculated according to:

$$Vres = 2Vin + Vref; \quad if \quad Vin < \frac{-Vref}{4}$$

$$Vres = 2Vin; \quad if \quad \frac{Vref}{4} < Vin < \frac{-Vref}{4}$$

$$Vres = 2Vi - Vref; \quad if \quad Vin > \frac{Vref}{4}$$

The plot of the residue voltages are shown in Fig 2-5 along with the acceptable region denoted by the box around the residue voltages.

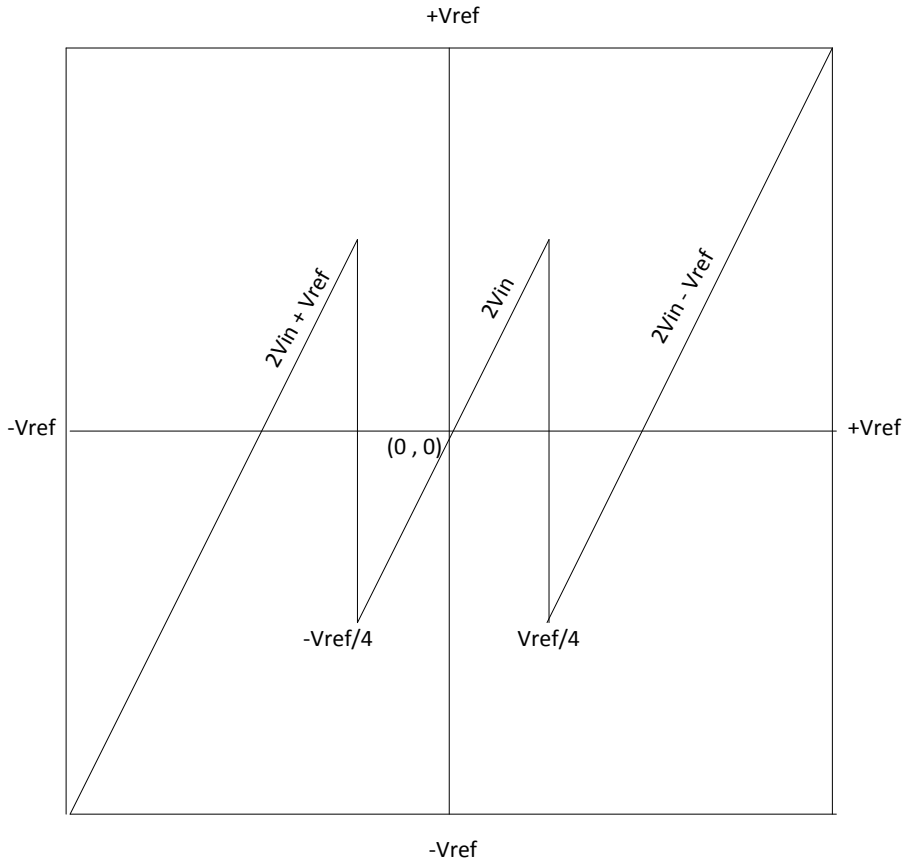

Figure 2-5: Residue plot of RSD stage

Now, if suppose there is an offset in the comparator or the opamp, then the trip points in the curve change, but provided that the comparator trip point is within Vref/4, the residue voltage would still remain within the box and will not saturate the consecutive stages. The gain can also have minor offsets and the residue voltage would not go out of range, but the gain however, as we will see, would set the resolution, so the gain is usually a tightly controlled parameter in pipeline ADCs. Fig shows a plot of the residue voltage with an opamp offset.

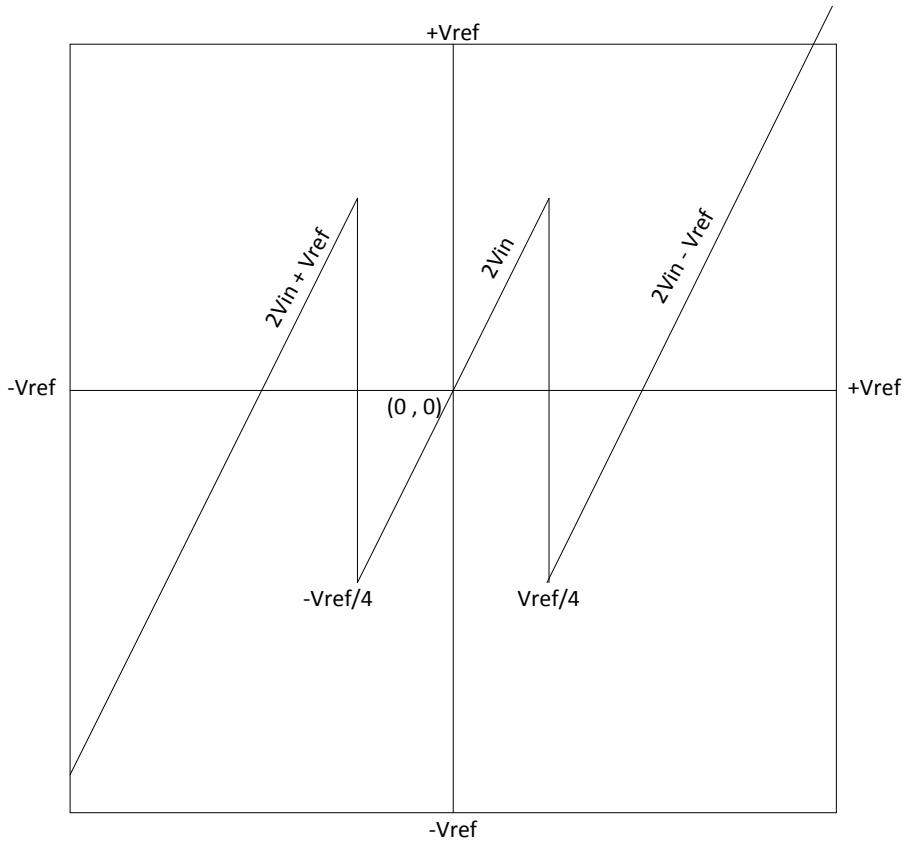

Figure 2-6: Residue plot with Opamp offset for RSD stage

2.4 Implementation of a single stage of the RSD Architecture

The block diagram of the sub-stage of the ADC was given in Fig. 2-4, this section describes the traditional silicon implementation of the same.

The coarse ADC is implemented as a flash ADC – two comparators that decide in which range the input lies. The ideal trip points of the comparator are –Vref/4 and Vref/4 in the input range of –Vref to +Vref, though these can be changed if the process can be better understood as to the offsets it creates. These comparators then produce the result as to which region in which the input lies and also the thermometer code

representation of the input which can be converted to digital using suitable digital error correction and recombination logic. The digital logic is presented in Chapter 7.

The comparators are implemented as shown in Fig 2-7.

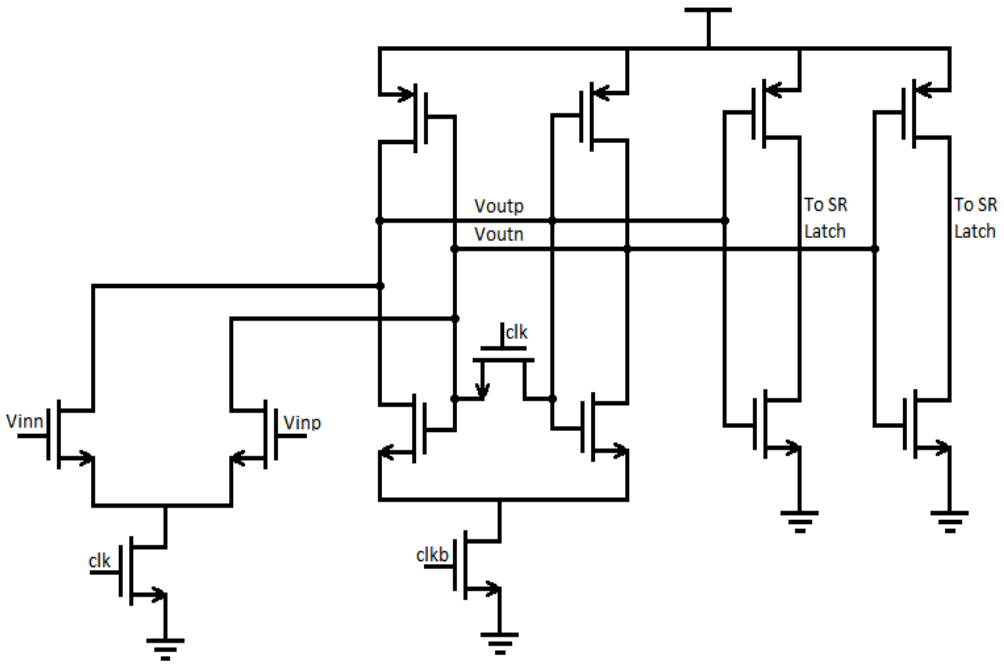

Figure 2-7: Implementation of Comparators

The digital bits are converted to suitable analog values and are subtracted from the input to produce the residue voltage. This requires a DAC stage, a subtraction block and a gain stage. All these blocks can be combined into a single switch capacitor block.

2.5 Switched-Capacitor Gain Stages

A switch capacitor block is a good choice for the gain stage as the gain of the stage can be set by using the ratio of the capacitors. The approach behind a conventional switch capacitor circuit is shown in Fig 2-9 as a hypothetical case. The essence of the switch capacitor circuit is to have two capacitors, here they are Cs and Cf and charge both capacitors up to the input voltage so the total charge would be (Cs+Cf)Vin, where Vin is the input voltage and then to transfer all of the charge onto capacitor Cf, thus the charge (Cs+Cf)Vin stores onto Cf. The corresponding voltage on Cf then becomes Vout. Thus, CfVout will equal (Cs+Cf)Vin, since no charge is wasted and all the charge from Cs has transferred to Cf. The hypothetical transfer is shown in Fig 2-9.

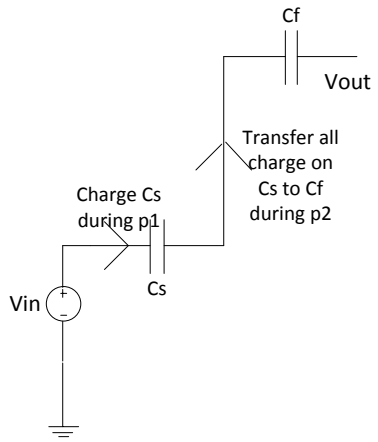

Figure 2-9: Hypothetical Charge transfer from one capacitor to another

$$Cf.Vout = (Cs + Cf).Vin$$

$$Vout = \frac{(Cs + Cf)}{Cf}.Vin$$

Thus,

$$Vout = \left(1 + \frac{Cs}{Cf}\right).Vin$$

Thus, the gain implemented here is (Cs+Cf)/Cf, which is purely a ratio of capacitors, which can be well controlled in CMOS processes. To force all the charge out of Cs and onto Cf, the voltage across Cs is made to zero, which flushes all the charge out of Cs and a path to Cf for the charge to flow is created. This can be produced by forcing a negative feedback through Cf and Cs connecting to the OpAmp input as in Fig 2-10.

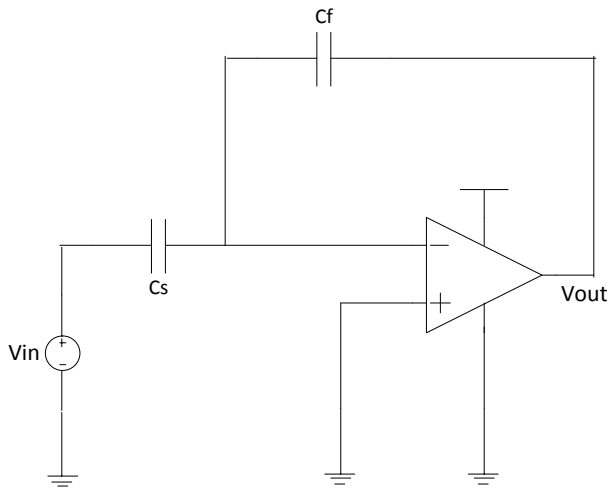

Figure 2-10: Flip Around switched capacitor stage without switches

Due to negative feedback the input terminal forces a virtual short which creates a virtual ground at the top plate of Cs, making the voltage across Cs go to zero and this forces charge out of Cs and onto Cf's top plate. Due to negative feedback, the opamp provides equal and opposite charge to the bottom plate of Cf. Thus, all the charge from Cs is transferred to Cf and the required gain is obtained.

Switches are required to disconnect the capacitors and then charge them up to Vin in the beginning and to connect them in the negative feedback architecture later. This is established using the circuits shown in Fig 2-11 or Fig 2-12.

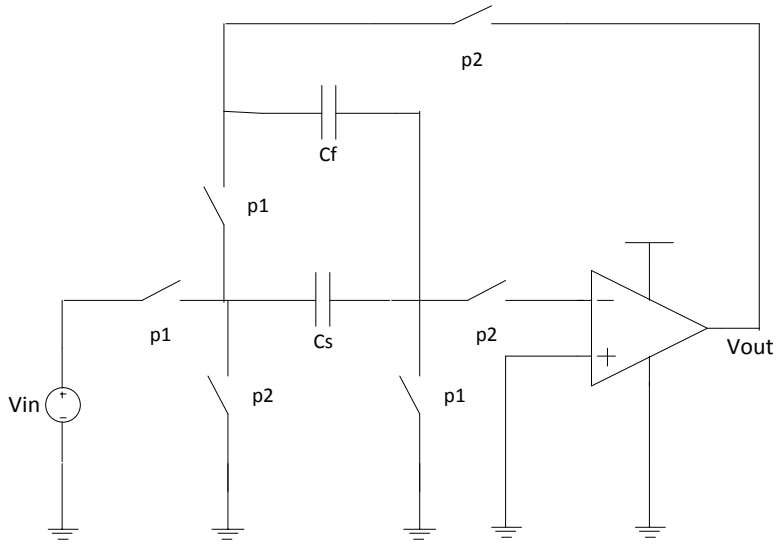

Figure 2-11: Flip Around Architecture

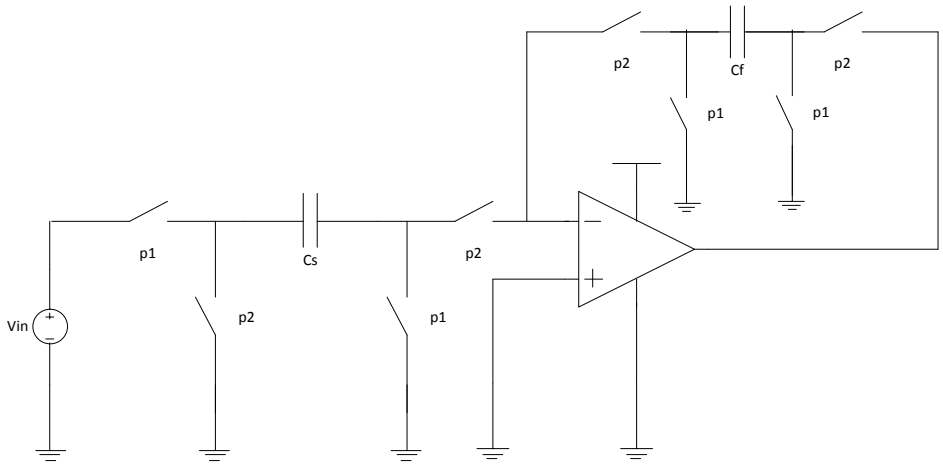

Figure 2-12 Charge Redistribution Architecture

These switches are operated using non-overlapping clocks since the entire circuit works based on charge transfer during two phases, overlap in the clocks will destroy the operation. During phase 1, the input charges the capacitors Cs and Cf and during phase 2, the capacitors are connected in negative feedback and the charge transfer and voltage gain takes place.

So far, the opamp was assumed to be ideal, however, in reality, the opamp has a finite gain and a finite bandwidth. Thus, assuming the opamp to be a single pole system and assuming that Cs at the instant it connects to the opamp input terminal is like a step input, the equation for the settling of the system can be obtained as:

$$Vout = (Vin - Vdac)\frac{(\beta A)}{(\beta A + 1)}\left(1 - e^{-t/\tau}\right)(1 + \frac{Cs}{Cf})$$

Where A is open loop gain of the amplifier, is the open loop bandwidth and β is the feedback factor. As can be seen, when A and GBW = $(1/\beta\tau)$ are infinite, then Vout is the input times the gain which is set by the ratio of the capacitors.

For the real life situation where A and GBW are finite, the error between the ideal output and the actual output are aimed to be less than an LSB/2. A margin is provided over this and the error is held below LSB/4. Based on this, the required gain and bandwidth are calculated for a given sampling speed. These give a good first estimate to the requirements and simulations are required to obtain the best values. Slewing is another effect that has to be taken into consideration as well.

During the amplification phase of the circuit, if a voltage of Vref is maintained across the sampling capacitor instead of zero, then a charge of Vref.Cs remains on Cs capacitor. Thus, a charge equal to VinCs-VrefCs is passed onto the feedback capacitor. This elegantly will implement the DAC and can be performed as shown in Fig 2-13.

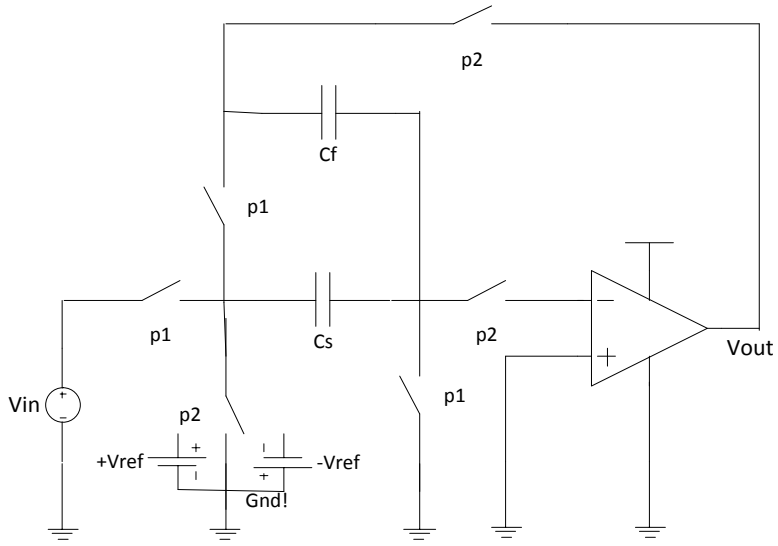

Figure 2-13: DAC Implementation

The entire schematic for a single pipeline stage is shown in Fig 2-14.

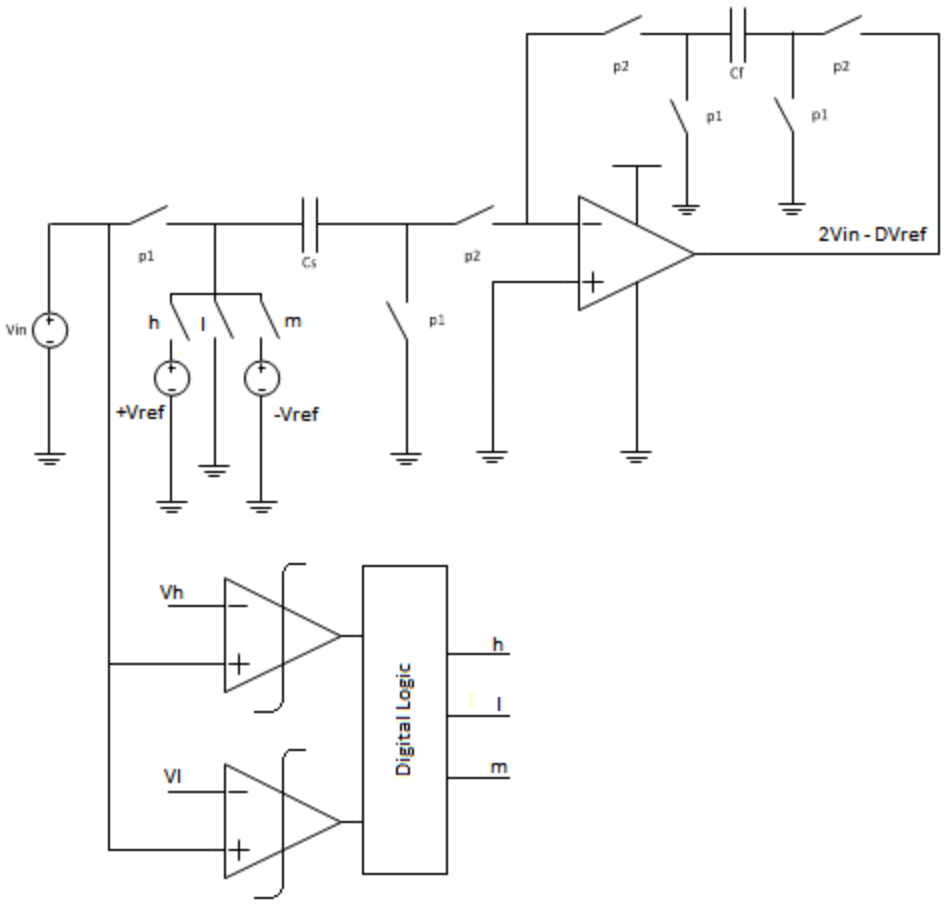

Figure 2-14: Entire Schematic of single stage of a pipeline

2.5 Conclusion

Chapter 2 presented the logic and implementation of the pipeline architecture along with the traditional switched capacitor techniques that are used to implement the stages of the pipeline ADC. The chapter also presented the details of the settling of the switched capacitor stages and how to size the gain and bandwidth of the amplifier to achieve the required accuracy and hence the resolution. The following chapter presents details on how the effects of finite opamp gain can be mitigated through novel techniques.

Chapter 3

CORRELATED DOUBLE SAMPLING, CORRELATED LEVEL SHIFTING AND SPLIT-CLS

3.1 Introduction

Chapter 2 described the basic working of a switch capacitor gain stage and the implementation details, the switch capacitor circuit relies on the virtual ground created by the high gain opamp to transfer charge from the sampling capacitor Cs to the feedback capacitor Cf. The charge transfer would be complete only if the virtual ground is perfect. But in reality, the gain of the opamp is finite and hence the opamp's input node sits at – Vout/A where Vout is the output voltage and A is the finite gain of the amplifier. Thus, a residual charge of Vout.Cs/A remains on the sampling capacitor and does not flow onto the feedback capacitor, creating an error equal to Vout.Cs/(A.Cf). This error affects the accuracy of the output.

Several techniques have been described in literature to overcome these imperfections. This chapter describes two techniques in specific – Correlated Double Sampling and Correlated Level Shifting.

3.2 Switch Capacitor Techniques to Compensate for Analog Imperfections

To overcome the analog errors due to opamp non-ideality, the gain of the amplifier is sized higher so that the error at the output is less than an LSB, this has been

the conventional approach. However, newer techniques have been developed more recently, that use an extra capacitor and/or an extra clock phase to correct the error. Two such techniques are Correlated Double Sampling (CDS) and Correlated Level Shifting (CLS).

Both techniques sample the signal during $\varphi_{1,}$ amplify the signal and give a coarse result at the end of φ_2 and adjust the value of amplified signal by removing the error due to finite gain of Opamps during φ_3 to produce a much more accurate output. It has been shown that the effective gain of amplifier in these switched capacitor networks is approximately the square of the gain of the amplifier. Thus a 30dB amplifier can function like a 60dB amplifier and have a proportionally high accuracy. Both correlated double sampling and correlated level shifting are explained in the following sections.

3.3 Correlated Double Sampling

There are many variations of the CDS technique [1-4], each offering a particular advantage. The Nagaraj CDS [4] is explained in this work, the circuit diagram for this is shown in Fig 3-1. This works on a two phase clock and has an extra capacitor at the input. This capacitor works in tandem with the sampling capacitor Cs to remove the Vout/A error and also additionally removes the offsets that may be present in the amplifier.

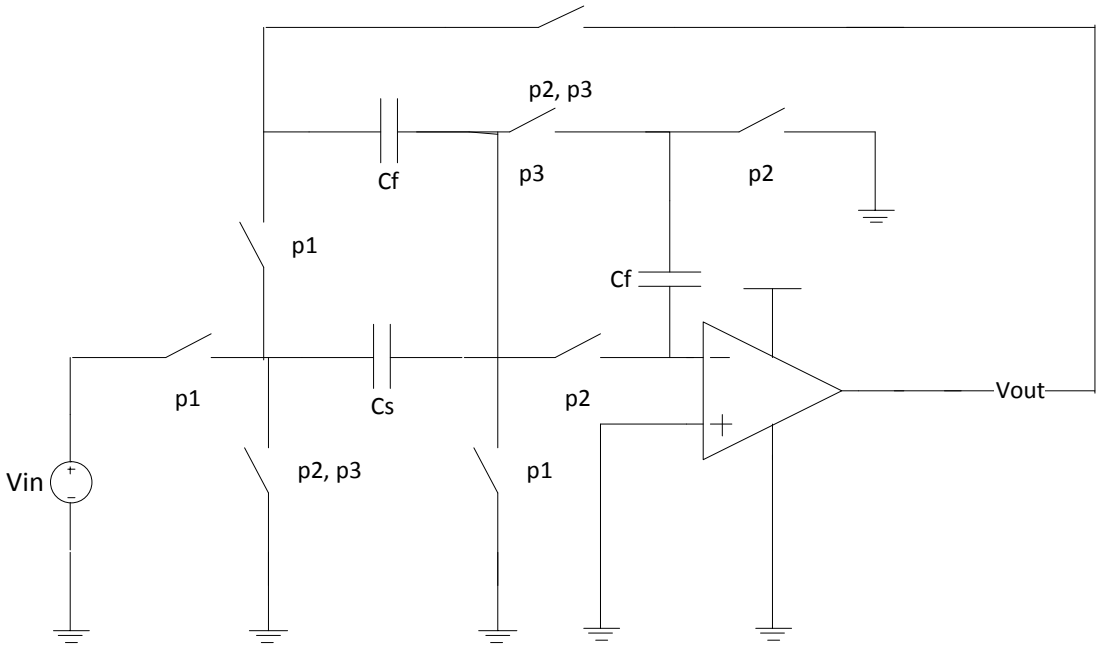

Figure 3-1: Correlated Souble Sampling

Since this rectification circuit works on the input side of the system, the noise that it contributes directly degrades the SNR at the input. Also, during the fine settling phase, the amplifier's output can be very close to the rails, where its gain is not the best. Thus, for a required gain, the range of the amplifier's input is restricted and is not true full scale. These disadvantages are however overcome in Correlated Level Shifting (CLS).

3.4 Correlated Level Shifting

Correlated Level Shifting (CLS) is a recently proposed technique [1-3] that works on a three phase clock. The traditional trend to reduce the Vout/A error at the input of the amplifier has been to increase the gain of the amplifier A. CLS on the other hand,

tries to reduce the Vout seen by the amplifier. In addition to the traditional switch capacitor amplifier, an additional capacitor is connected to the output of the amplifier this capacitor samples the rough output during the estimation phase. This capacitor is then connected in feedback as shown in Fig 3-2.

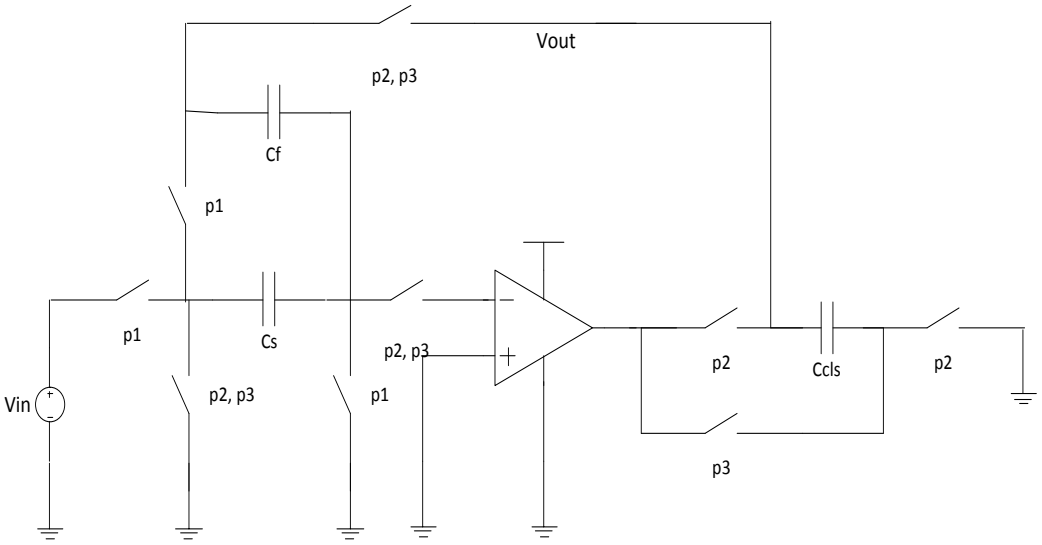

Figure 3-2: Correlated Level Shifting

The CLS capacitor is meant to act like a voltage source with the voltage Vout across it. Thus, the amplifier's output node "B" now sits very close to the AC ground potential or Vout/Aest to be accurate, where Aest is the gain the amplifier can provide during the estimate phase. This forces the input of the amplifier to now go to a voltage $(Vout/A_{est})/A_{fine}$, where A_{fine} is the gain of the amplifier in the fine settling phase. This is closer to the ground potential by a factor of A_{fine}, thus forcing more charge out of the sampling capacitor Cs onto the feedback capacitor Cf's top plate, charge for the bottom plate of Cf comes from the CLS capacitor. If the CLS capacitor is large and if the charge lost by the CLS capacitor is negligible, the total gain of the network is close to $A_{est}xA_{fine}$.

Afine as described is the gain of the amplifier in the fine settling phase. During the fine settling phase, the amplifier's input and output node are returned to the normal biasing conditions of the amplifier and hence the gain it provides is maximum. Thus, the effective gain is better than A_{est}^2 provided by CDS. This is shown in Fig 3-3.

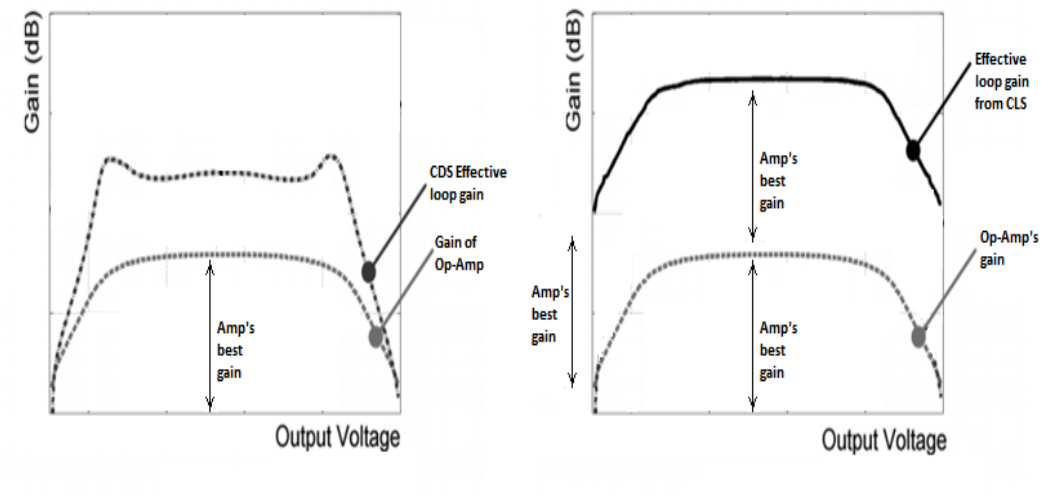

Figure 3-3: Plots of Effective Gains of CDS and CLS

As can be seen from the plot, the gain of the amplifier is higher over a larger input voltage range than a traditional circuit or a CDS network. Plus, the gain is more linear as it varies less than that in the CDS. The CLS network also operates only on the output of the circuit and hence, the noise it contributes is divided down by the loop gain of the network and hence is negligible. However, CLS does not take care of the DC offsets or the 1/f noise and hence an autozero can be utilized. The settling of the output is shown in Fig.

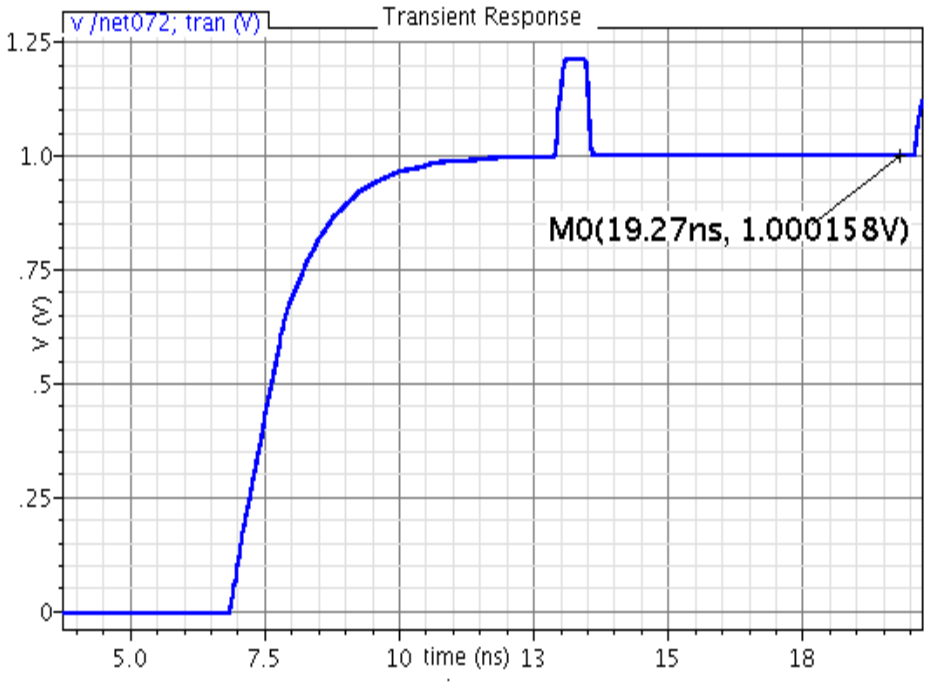

Figure 3-4: Settling of output of CLS

As can be seen in the plot, there is a glitch in the output voltage between the estimate phase and the fine settle phase. The glitch that occurs affects the settling accuracy of the entire network. The glitch is proportional to the ratio of Opamp output capacitance to the load capacitance [11] and can be reduced by making the size of the CLS capacitor larger. The problem was also addressed in a recent update from the same team that worked on the CLS technique with a solution called Split-CLS [13] as well. However, the motivation of this work to propose a technique similar to Split-CLS is different and will be presented here.

3.5 Split-CLS

During the fine settling phase of the network, the signal is removed from the active circuitry, this also means that the signal can be processed independently of the active circuitry during the fine settling phase. This helps realize that the amplifier used in the estimate phase need not be the same as the amplifier used in the fine settling phase.

To this end, the amplifier in the estimate phase can be replaced with another amplifier to be used in the fine settling phase. The circuit that does this is shown in Fig 3-5.

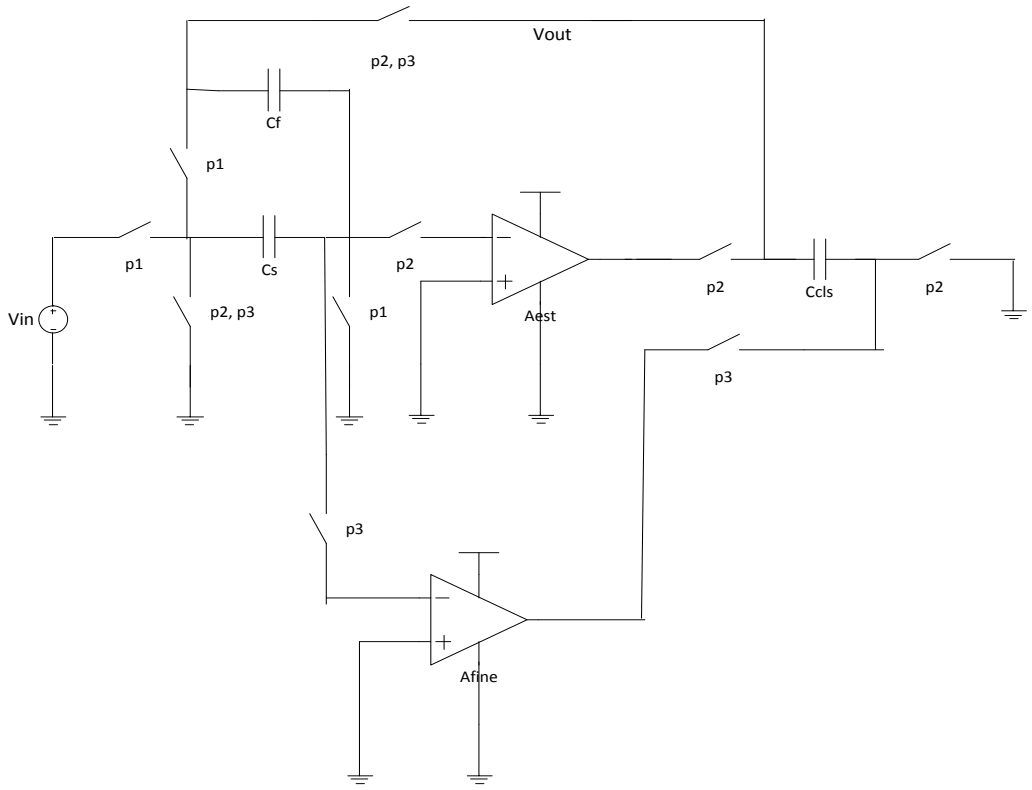

Figure 3-5: Split CLS

The amplifier used in the estimate phase charges up the feedback capacitor and the CLS capacitor to the approximate value of the accurate output. The fine settling amplifier then fine settles the output to the final accurate value. Thus, the amplifier used in the estimate phase requires an amplifier with output swing and slewing capability. A class AB amplifier or amplifiers with an optimized output stage are very suitable candidates for this amplifier.

After the estimate phase, the amplifier is returned very close to its biasing conditions and node A does not require to swing, thus this amplifier need not have very high output swings, but instead it can have a majority of the required total gain and bandwidth requirements. However, not all of the gain and bandwidth can be assigned to this amplifier.

Since the amplifiers are switched between the estimate and the fine settle phase, the parasitic capacitance at the input of the amplifier steals charge and does not transfer it to the feedback capacitor during the fine settle phase since it has been disconnected. This requires that the input parasitic capacitance be minimized for the estimation amplifier and the settling error Vout/A at the input node of the estimation amplifier be minimized so that the charge lost is less than the LSB/4 value, with a factor of 2 added for margin.

3.6 CLS-specific design margins

Since CLS does not take care of offsets or the 1/f noise, the input transistor size is better kept larger and since the input parasitic capacitance is directly associated with the input transistor's size, this presents a tradeoff. In this design, since higher resolution

is required with low offsets due to large gain, the input transistor was kept large with high gm and instead the settling behavior of the estimation amplifier was optimized for settling better than the required performance and the fine settling amplifier's gain and bandwidth were reduced to reduce power consumption. To this end, the estimate amplifier was chosen to be a folded cascode with a gain boost amplifier and the fine settling amplifier was selected to be a simple telescopic cascode.

Though the CLS technique provides nearly a squaring of the gain of the amplifier, since the CLS capacitor is finite and its loss of charge changes the voltage stored across it, a loss in accuracy is experienced. A 6-12dB loss from the square of the amplification in accuracy is to be expected from the system when the CLS capacitor size becomes comparable to the load capacitor.

The loss is also higher when there is a switching or variation of loading on the output between the estimation and the fine settling phase. This effect was more particularly noticed in the implementation of the 12b 125MS/s pipeline ADC for NASA's Jupiter Europa Space mission. Hence, a pair of sampling arrays was used instead of a single set and they worked in tandem to keep the loading on the system constant.

The estimate amplifier had a gain of 70dB and a bandwidth of 600MHz and the fine settling amplifier had a gain of 60dB and a bandwidth of 800MHz. Compared to a single amplifier with 110dB of gain and 1.2GHz of bandwidth, both these amplifiers are less complex to design and do not have compensation penalties.

3.7 Conclusion

This chapter presented the correlated double sampling, correlated level shifting and the split-CLS techniques in detail and compared them. It also describes the benefits of the techniques relating to the finite gain of the amplifier and the penalty they pay in terms of bandwidth. Chapter 4 discusses the details of the triple sampling technique in detail that helps overcome the bandwidth penalties paid by these architectures.

Chapter 4

DOUBLE SAMPLING AND TRIPLE SAMPLING

4.1 Introduction

Chapter 2 presented the details of how pipeline architectures are implemented in traditional architectures with the RSD technique to overcome the difficulties of comparator offsets, capacitor mismatches and opamp offsets and the shortcomings of the finite gain of the amplifier. Chapter 3 discussed the various switch capacitor techniques that are viable to be used to reduce the error because of the finite gain of the amplifier.

This chapter discusses the double sampling technique that is used to double the frequency of sampling while keeping power nearly constant and the crux of the thesis, the triple sampling technique that has been proposed that triples the frequency of sampling while reducing the requirements from the analog blocks and keeping power consumption nearly constant or lower.

4.2 Double Sampling Technique

As was presented in Chapter 2, the pipeline architecture consists of the gain stage that is implemented using the switched capacitor circuit that was shown and has reproduced here again for easier reference in Fig 4-1.

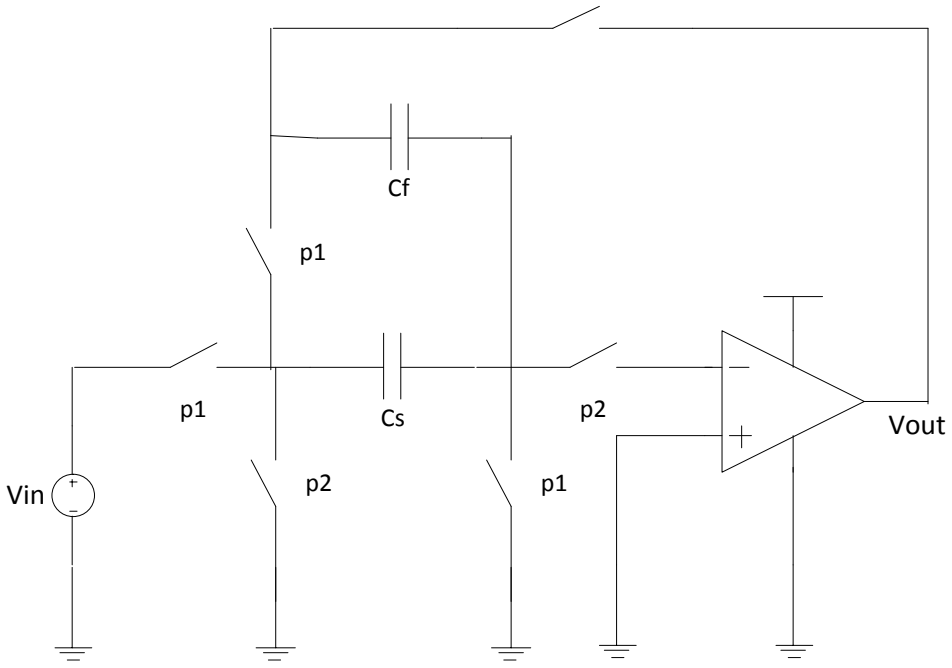

Figure 4-1: General Gain stage for pipeline

The circuit works on two clock phases, the sample and the gain phase. During the sample phase, the sampling capacitor Cs samples the input onto itself and holds it charge, the opamp remains idle during this phase. During the gain phase, the sampling capacitor Cs connects to the opamp input and the feedback capacitor, the virtual ground at the opamp's input node forces charge out of the sampling capacitor and onto the feedback capacitor. Thus the Opamp is needed during the gain phase and not the sample phase.

Thus, it is possible to create another set of sample and feedback capacitances Cs2 and Cf2 in addition to the original sample and feedback capacitances Cs1 and Cf1 and pipeline the operations. During phi1, Cs1 is connected to the input and samples a value from the input signal and during phi2, it connects to the opamp and produces an output on Cf1. Meanwhile, during phi2, the input is sampled by Cs2 and during phi1, it connects to the opamp and produces an output on Cf2. This is shown in Fig 4-2.

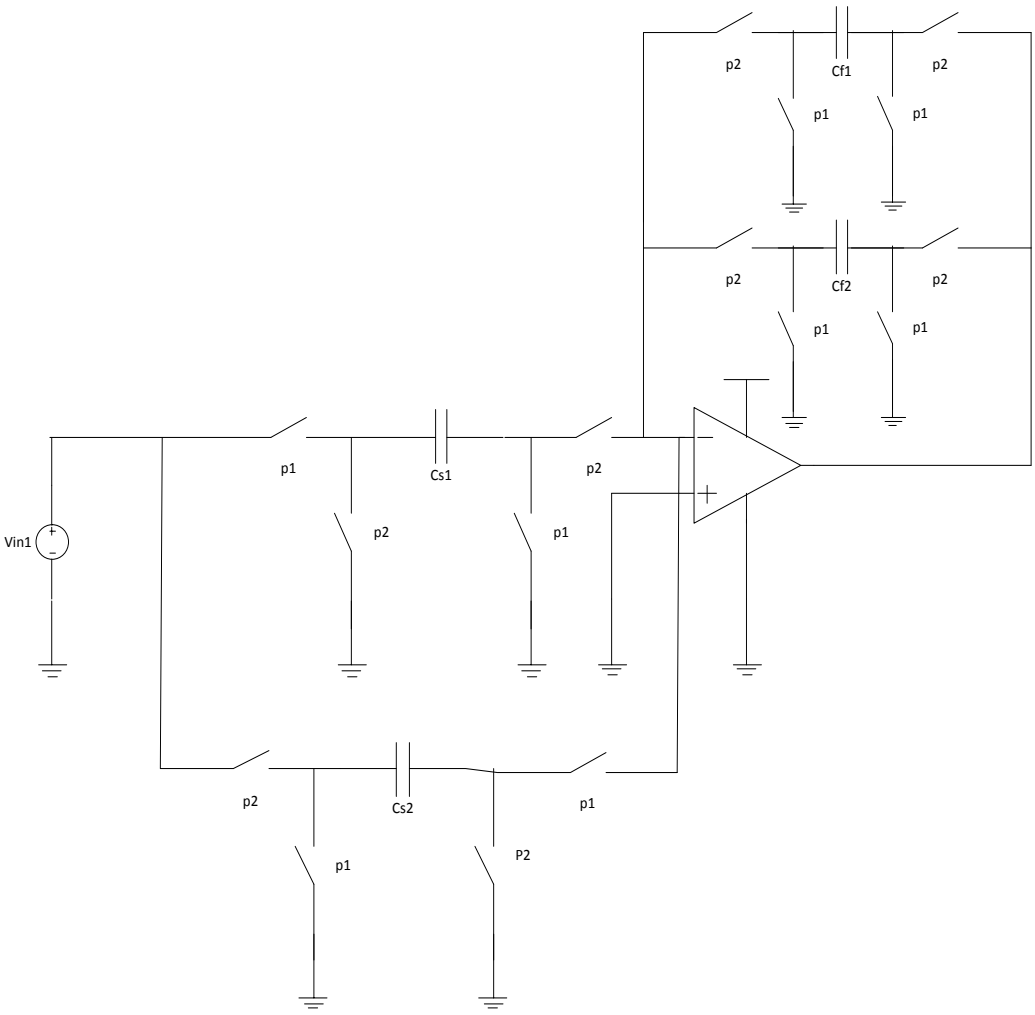

Figure 4-2: Double Sample a single signal, effective sampling frequency = 2Fs

Thus, the input signal is sampled during both phi1 and phi2 and outputs are produced during both phi1 and phi2, increasing the sampling frequency by a factor of 2 for a very little increase in the power consumption. The concept can also be extended to sample two different signals, such as the I and Q channels as in [9]. The circuit schematic is shown in Fig 4-3.

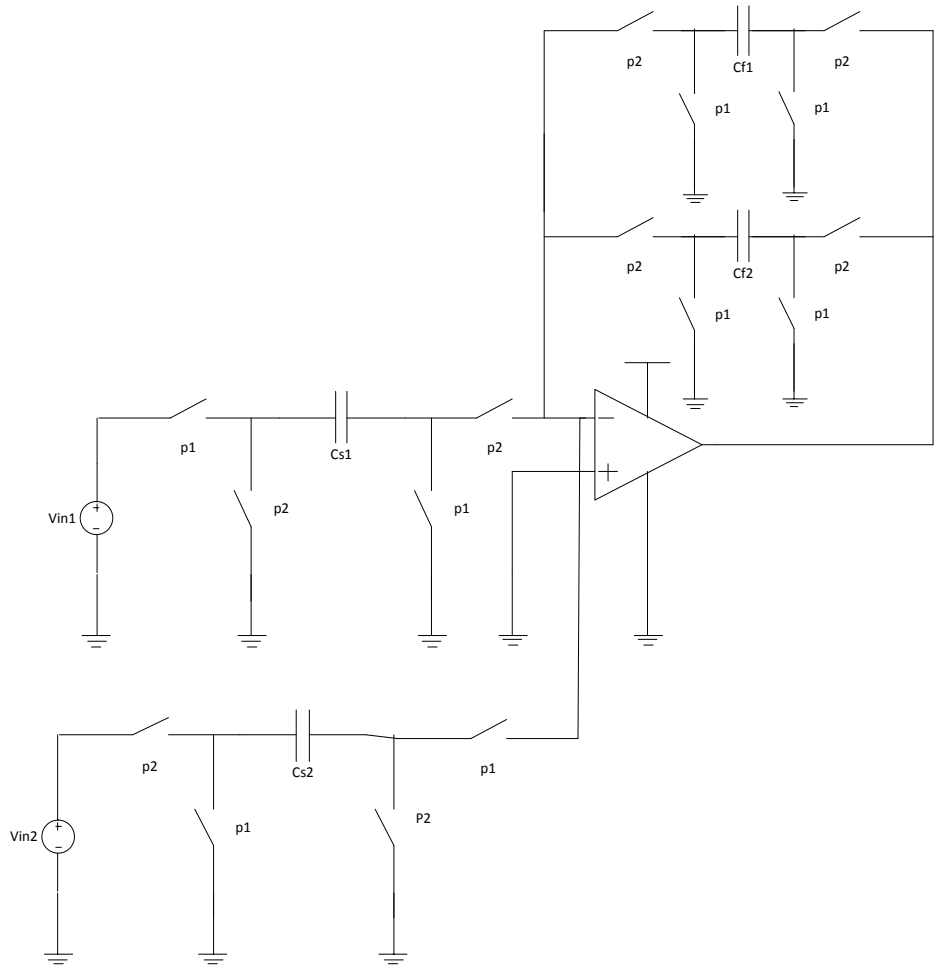

Figure 4-3: Double Sample I and Q Channels

This concept has been termed Double Sampling .

4.3 Triple Sampling

The concept Triple Sampling is proposed in this work and double sampling has been the motivation for it. As explained in Chapter 3, Split CLS uses two separate low complexity amplifiers to estimate and fine settle the signal in three different phases and the first phase is the sampling phase. Similar to double sampling, the Split-CLS technique can be made to have three distinct paths composed of path1 - Cs1, Cf1, CCls1; path2 - Cs2, Cf2,Ccls2 and path3 - Cs3, Cf3, CCls3.

These paths can then be pipelined during the three clock phases such that Cs1 samples the input during phi1, Cs2 samples the input during phi2 and Cs3 samples the input during phi3. Cs1 then connects to the estimation amplifier Aest during phi2, similarly, Cs2 connects to A_{est} during phi3 and Cs3 connects to A_{est} during phi1. Fine settling for path1 occurs during phi3 during which it requires the fine settling amplifier A_{fine}, but not the estimation amplifier A_{est}, thus A_{est} is free to be used for path 3, which requires it during this phase. Similarly, path 2 uses A_{fine} during phi1 and path 3 uses A_{fine} during phi2. The circuit that performs this is shown in Fig 4-4.

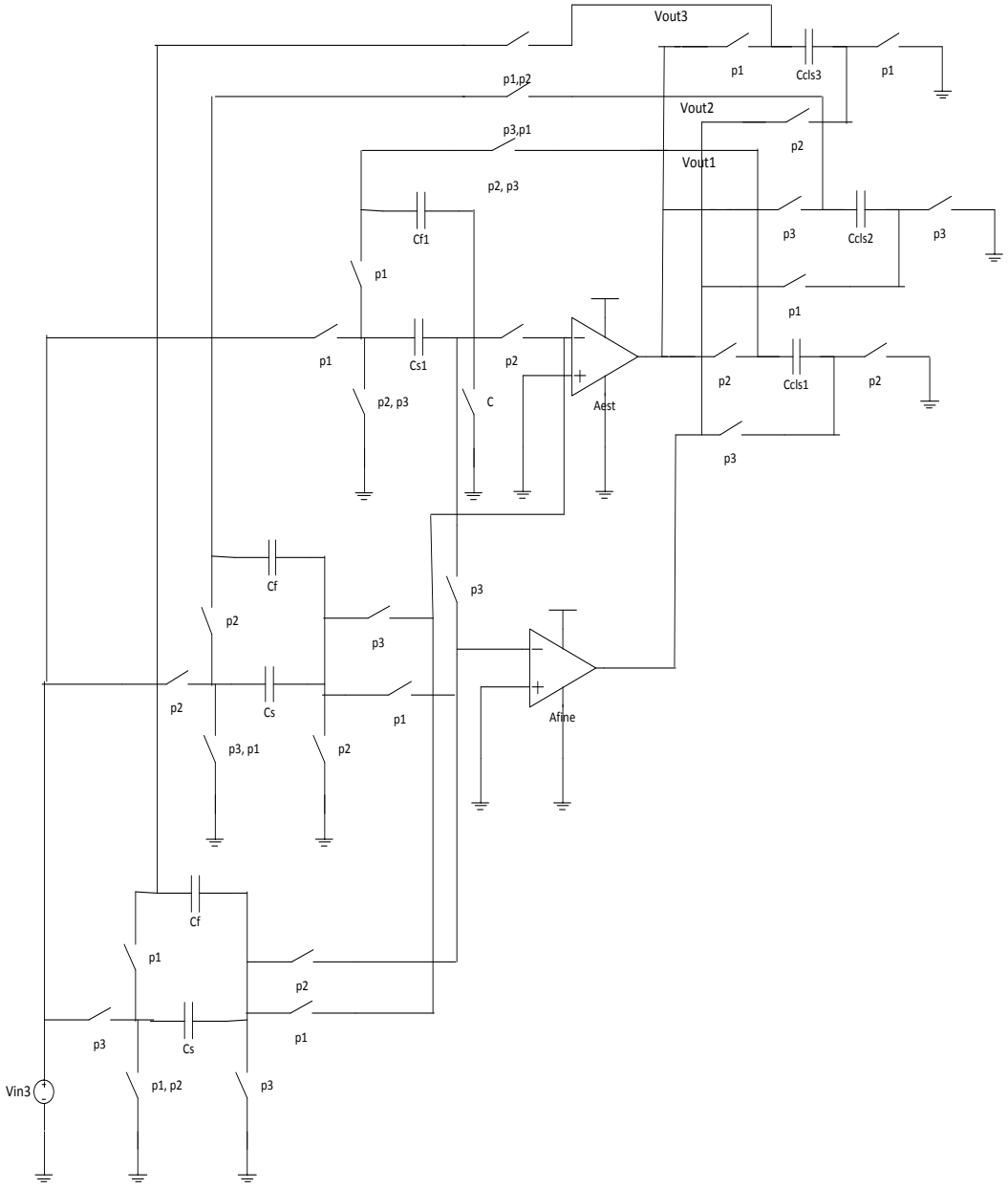

Figure 4-4: Triple Sampling a single signal, Effective sampling frequency = 3Fs

The clock phasing and the representation of the sharing of the amplifier elements are shown in Fig 4-5.

Figure 4-5: Clock phases and sharing of blocks

Similar to double sampling, triple sampling can be used to sample either the same signal at thrice the sampling rate or three independent signals at the same frequency. However, triple sampling, due to the nature of CLS, reduces the specification on the single amplifier. The requirements from the amplifier are shown in table 1.

Table1: Specifications of amplifiers in traditional and triple sampling technique

Parameter	Traditional Technique	Triple Sampling Technique
Gain	102 dB	60 dB, 60 dB
Bandwidth	1.16 GHz	150 MHz, 250MHz
Signal Swing required	Vdd	Vdd – 2Vt, 2Vt
Sampling Capacitance	4pF	3.2pF
Implementable?	Very Difficult – Low Yield, High Design costs, High power because of Compensation penalties	Easy to implement – Higher yield, lower design time, all amps can be output compensated if needed at all – lower power
Effective Sampling Freq	133 MHz	133 MHz

The output of triple sampling a single sine wave is shown in Fig. There are three outputs per clock cycle and each consecutive output represents one sample more of the sine wave, thus increasing the sampling frequency by a factor of three. Fig shows three independent inputs being processed. Three distinct sine waves are given to the system and three distinct outputs are seen in it.

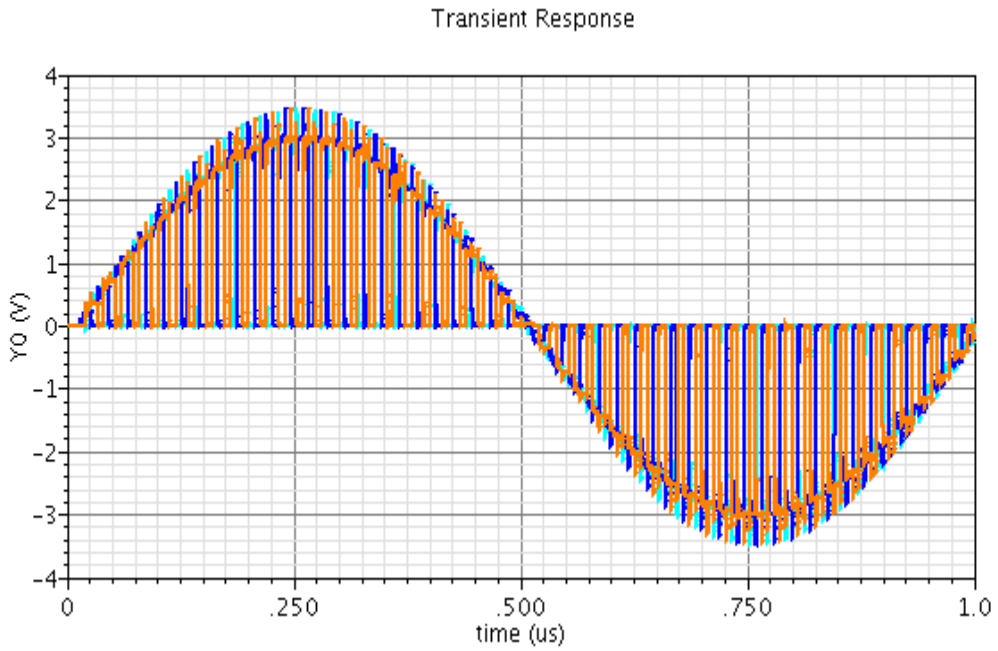

Figure 4-6.a: Triple Sampling output of a single sine wave

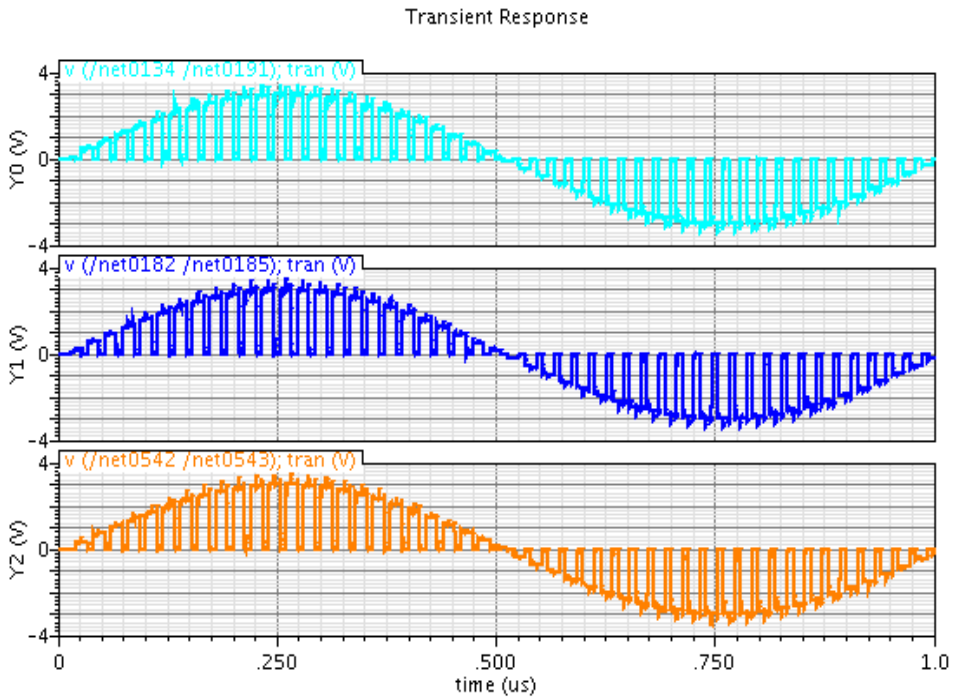

Figure 4-6.b: Three Independent Paths processing a single input

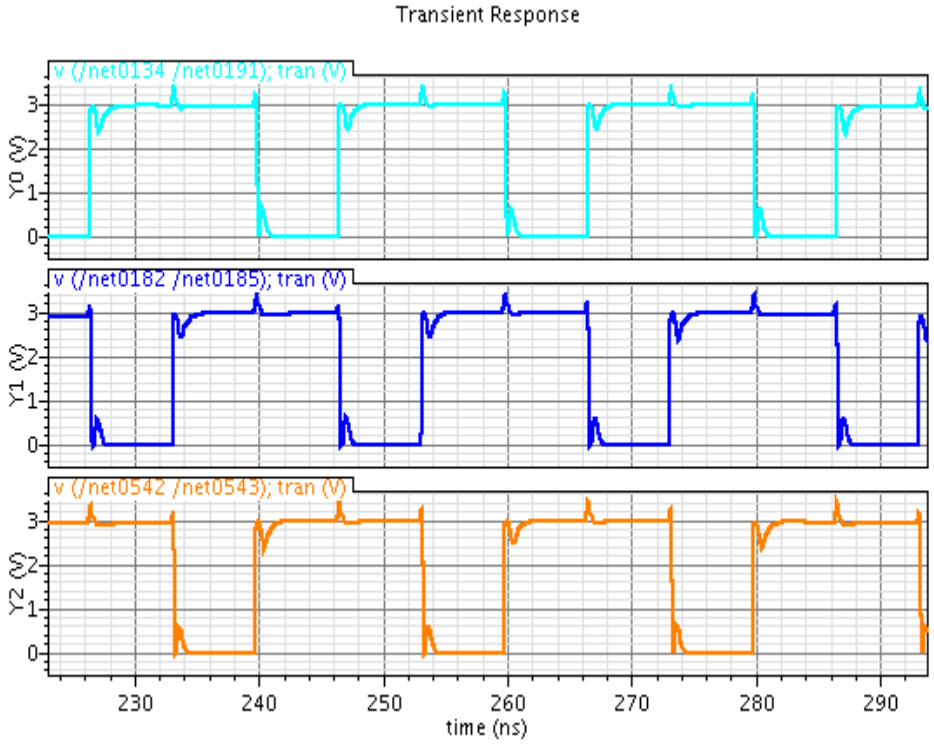

Figure 4-6.c: Three independent outputs and one output each clock phase

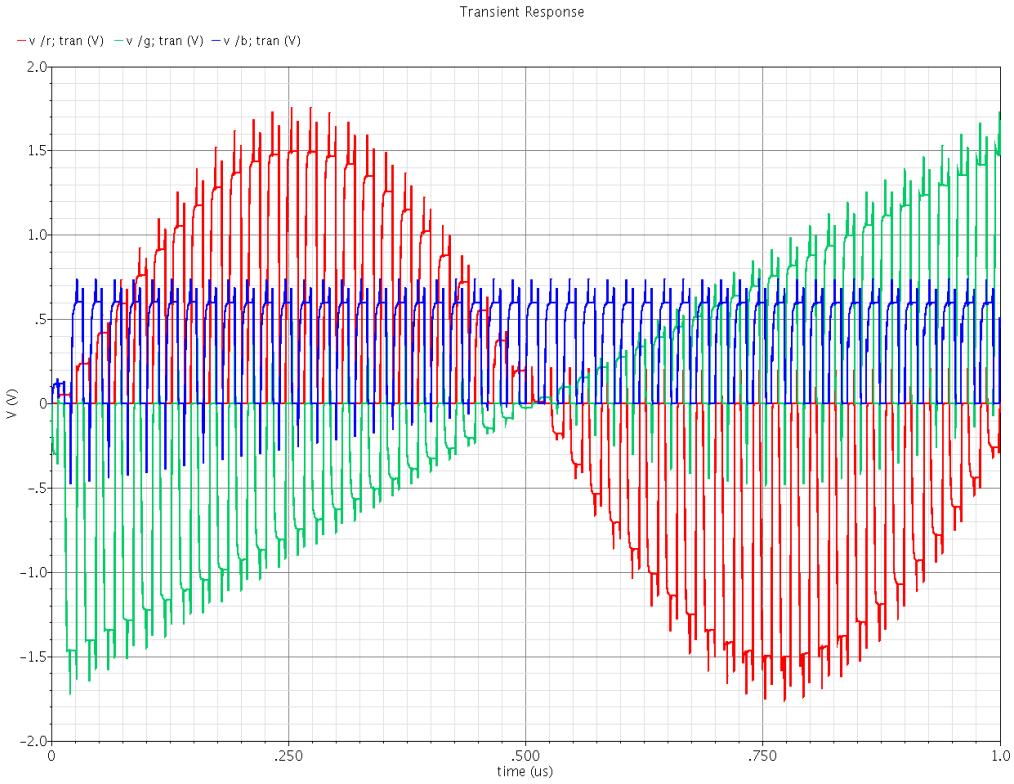

Figure 4-6.d: Output of Triple Sampling three independent input signals

Further, triple sampling needs to be amenable to RSD to be viable to be used in pipeline ADCs and it is. RSD can be incorporated as in any gain stage with the comparators making a decision between the sample and the estimate phase and the RSD value is applied to the bottom plate (subtraction node) of the sampling capacitor during the estimate phase and this value is applied during the fine settling phase as well. This is shown in Fig 4-7.

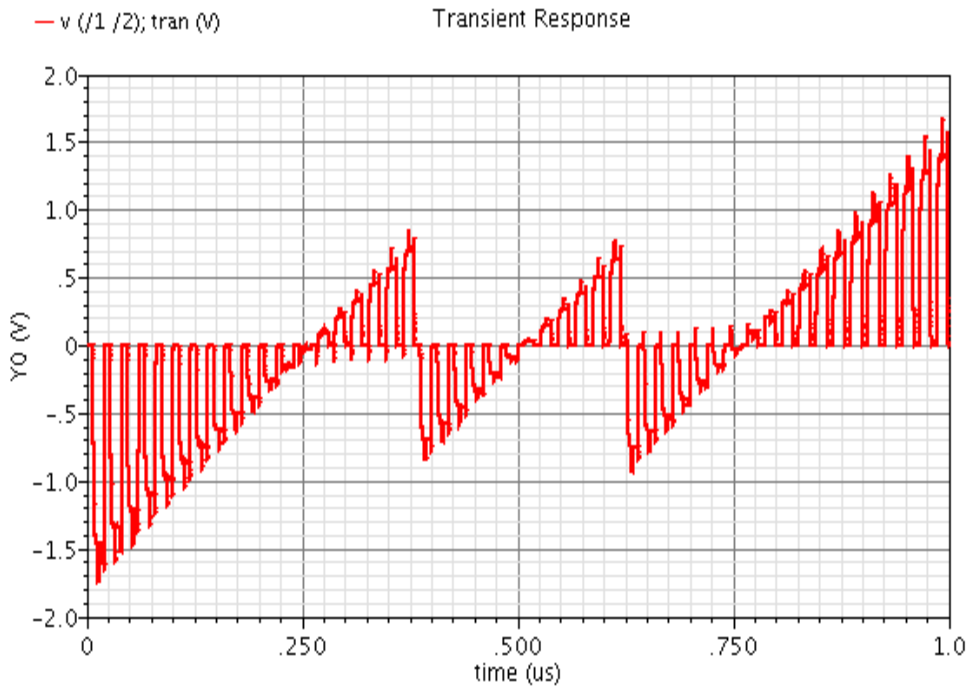

Figure 4-7: RSD Incorporated into triple sampling - single path

Fig shows the output of the RSD incorporated triple sampling stage to three independent inputs – two sine waves and a ramp. As can be seen, memory effect is at minimum and each path produces a distinct output. The standard RSD residue plot being generated for the ramp input can also be seen.

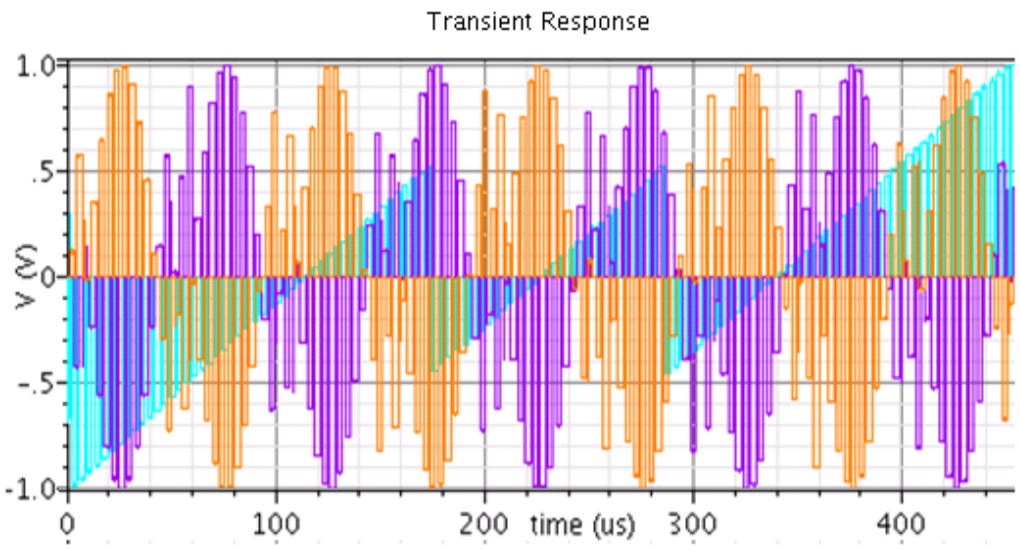

Figure 4-8: RSD incorporated triple sampling stage, processing three independent signals – two sine waves and a ramp

4.4 Conclusion

This chapter presented the crux of this work, the triple sampling technique and its advantages compared to the traditional techniques. It also presented how RSD is incorporated into triple sampling and can be used in data converters. Chapter 5 presents how the data converter is implemented and the trade-offs faced in the implementation of the triple sampling stages.

Chapter 5

AMPLIFIER SELECTION & IMPLEMENTATION

5.1 Introduction

As presented in Chapter 4, the amplifier used in the estimate phase of the operation requires that the amplifier be optimized for slewing and swing as the most important characteristic for low resolution, high speed applications. The amplifier's bandwidth and gain are considerably lower than required by fine settling amplifiers used in the third phase of operation in this application.

For high resolution, lower speed applications however, the amplifier's parasitic input capacitance begins to dominate the accuracy by stealing charge during the estimate phase and not restoring it during the fine settle phase. In this case, it is beneficial in terms of memory effect and settling accuracy to minimize the parasitic input capacitance of the input of the estimate amplifier, but detrimental in terms of 1/f noise and offsets to do so, hence this trade-off is addressed.

To investigate the possibilities, the architectures listed were tried:

1. Telescopic Cascode
2. Folded Cascode
3. Folded Cascode with Slew Rate Enhancement
4. Class AB Amplifier

5. Folded Cascode with gain boosting

This chapter describes the feasibility and application regimes that are possible with the architectures that are popular in analog design.

5.2 Architecture Implementations

As described in the previous section, the input parasitic capacitance at the estimation amplifier steals charge during the estimation phase and when the amplifier is switched, this charge does not get into the feedback capacitor in the intended path. This creates accuracy issues as well as memory effects.

The memory effect can be reduced to tolerable limits by adding more gain and bandwidth to the estimation amplifier helping it settle to the next value despite the memory effect. However, the loss in accuracy cannot be corrected by increasing the gain or bandwidth of either the estimation amplifier or the fine settling amplifier. Hence, the loss of charge must be maintained at a minimum.

The voltage that develops at the input of the estimation amplifier during the estimate phase is -Vout/Aest and a charge is stored proportional to this voltage on to the input parasitic capacitance. Thus, by reducing the voltage here by increasing the gain of the amplifier helps reduce the charge lost.

Also, by reducing the input parasitic capacitance, accuracy can be regained, however, to reduce this capacitance requires reducing the area of the input transistors and most

likely, its gm. This reduces the gain, bandwidth and increases the input referred noise as well as increasing the DC offsets. Hence, reducing the input transistor size has detrimental effects. Hence, increasing the performance of the estimation amplifier is a better trade off although it requires increasing the power consumption.

The following discussions are on the categories of the amplifiers that can be chosen to implement as the estimation amplifier and the performance that the architectures make available.

5.3 Telescopic Cascodes

Though almost all of the amplifiers worked to about 60-70 dB of SFDR, the requirements to make it work for 14b linearity requires large voltage swing at the output (though not as huge as in conventional techniques) of the estimation amplifier. Telecopic Cascodes shown in Fig 5-1 can be used for moderate resolutions, for up to about 10-12 bits, which is quite a common requirement for pipelines.

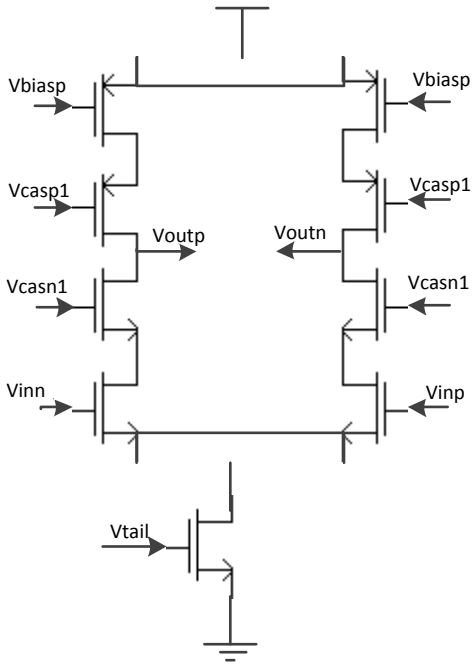

Figure 5-1: Telescopic Cascode

This would provide a very power effective solution, however, the requirement of finer settling during the estimation phase requires higher linearity over a broader output signal swing range and this architecture lacks linearity over a high signal output range.

5.4 Folded Cascodes

Folded cascode amplifiers are a very good choice for moderate resolution architectures as well. Folded cascode amplifiers provide a higher range of voltage range in which they are linear. However, for higher resolutions, the capacitance values determined by the thermal noise levels are big and the slew rate requirements for the folded cascodes are large. If not properly addressed, the limited slew rate will produce

large spurs in the frequency spectrum and reduce the SNDR. Fig 5-2 shows the result of having a lower slew rate than required.

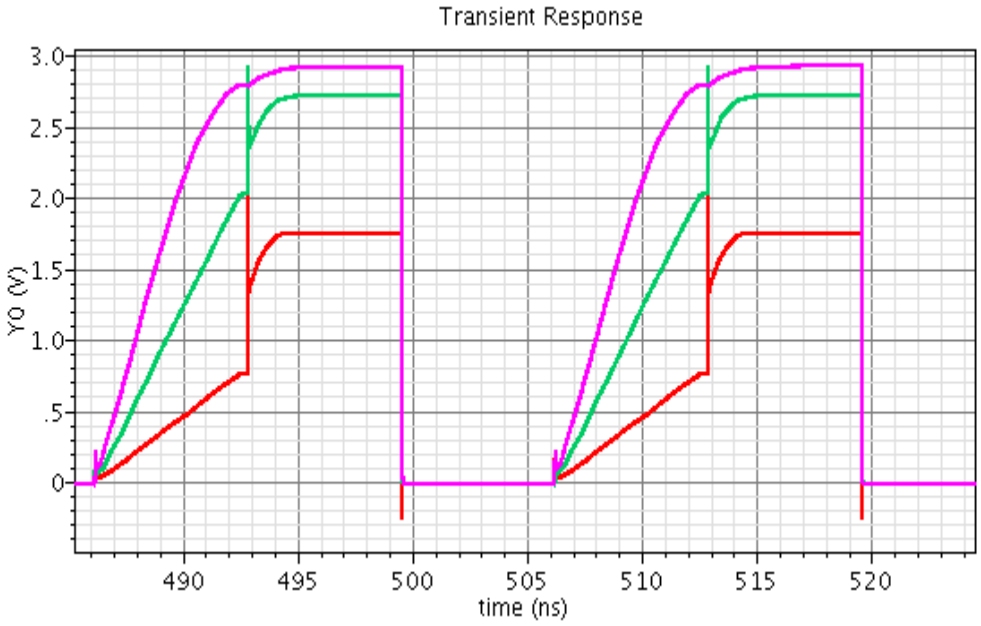

Figure 5-2: Slew rate limitations

It can be seen that with CLS, even if the slew rate is heavily restricted as in the bottom graph, the final output is still better than without CLS, this is due to the fine settling amplifier correcting for the error made by the estimation amplifier. However, the final error is huge and slew restricted settling will drastically affect the final accuracy.

Slew rate enhanced folded cascode amplifiers provide a solution to such conditions. Slew rate enhancement circuits provide higher slew without routing the current through the main output rails, as routing high currents through the core of the amplifier consumes large quiescent power. These amplifiers also easily provide 50-60 dB of gain and significantly good bandwidth. This eases the specifications further on the fine

settling amplifier. Fig shows the circuit that implements the slew rate enhancement of the folded cascode amplifier.

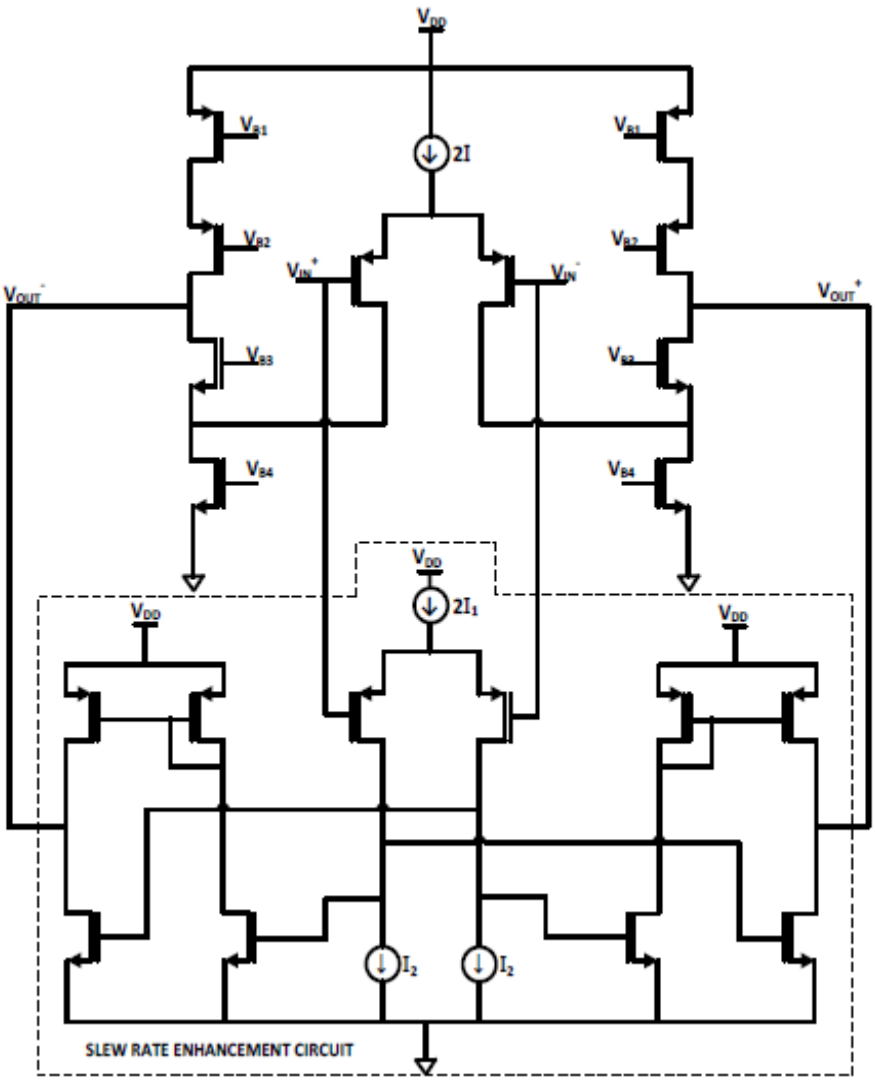

Figure 5-3: Slew rate enhancement circuit paired with a folded cascode amplifier

Unfortunately, the slew rate enhancement circuits cause too much 5^{th} order distortion and hence non-linearity for high resolution applications. Typically, a third order harmonic means a flattening of the peak of a sine wave as in clipping. A fifth order harmonic can be shown as in Fig 5-4.

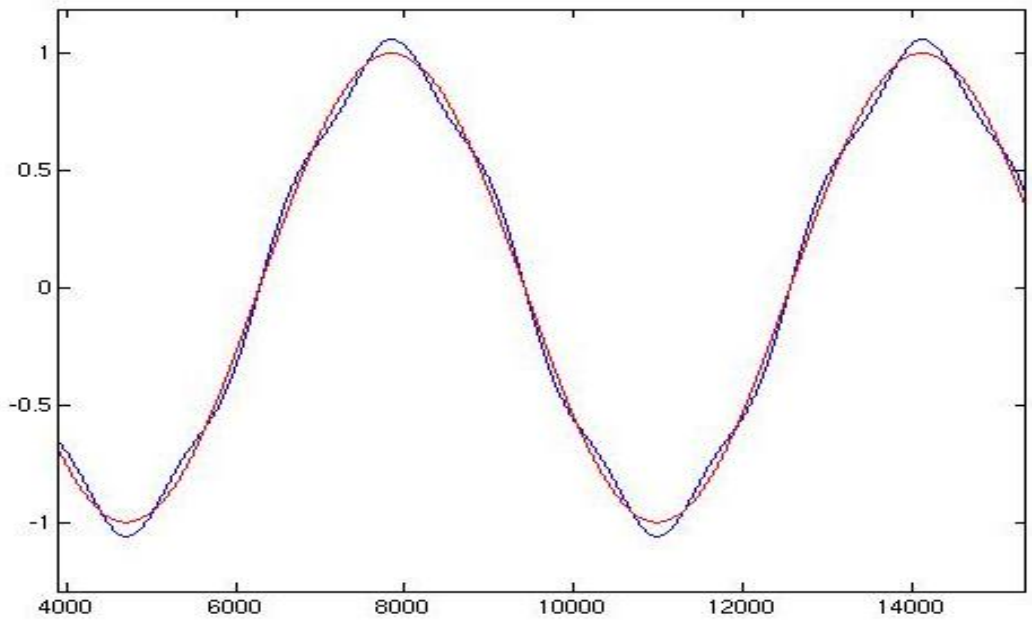

Figure 5-4: Time domain view of a dominant fifth harmonic distortion

A fifth harmonic as seen in Fig tends to "wiggle" the sine wave about itself – after the zero crossings of the sine wave, the fifth harmonic tends to pull the sine wave to a higher amplitude faster at first and then slows it down when the sine wave increases. The blue line is a sine wave with a fifth harmonic impurity and the red line a pure sine wave.

The slew rate enhancement circuit's behavior is inherently fifth order centric – at low input amplitudes, when slewing is not required, there is no slew rate enhancement,

hence the settled value is typically less than the actual value, though less than LSB/2. At reasonably high amplitudes, the slew rate enhancement kicks in and the final output typically overshoots the accurate value – generating a positive error in this region always. At higher amplitudes, both the main amplifier and the slew rate enhancement circuit are slewing, but the slew rate is less than ideal and hence the error is again negative – the output settles to values less than the accurate output. As can be seen, the error is dependent on the input value and is related to the input through the fifth harmonic, causing a strong fifth order spur as can be seen in Fig. Fig is the spectrum of the output.

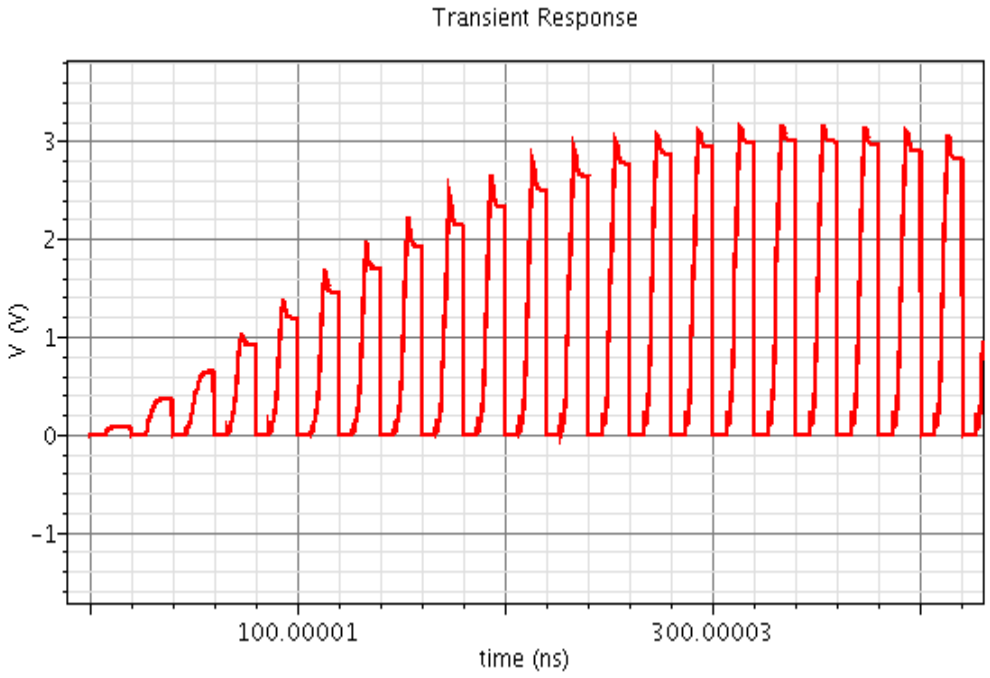

Figure 5-5: Fifth harmonic distortion caused by slew rate enhancement

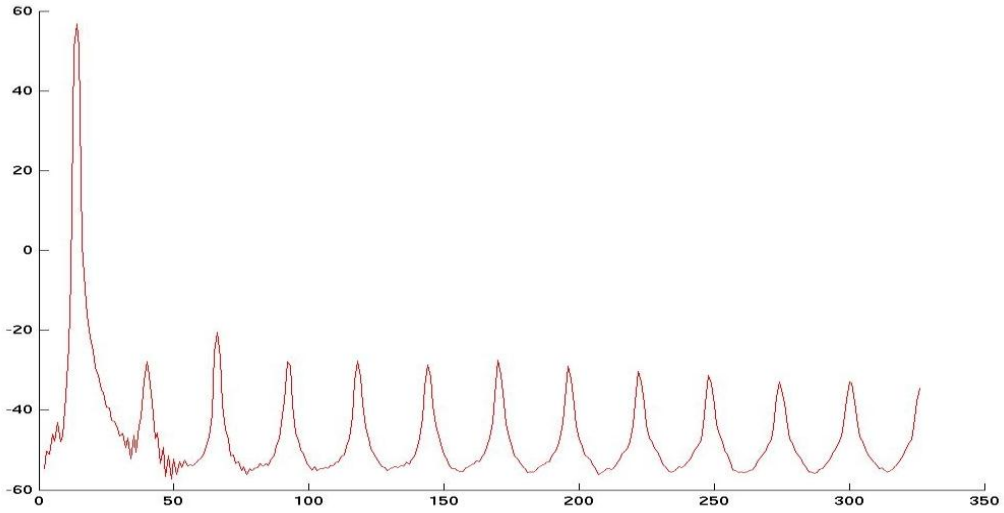

Figure 5-6: Dominant fifth order distortion seen in spectrum

However, the folded cascode with the slew rate enhancement is a very good candidate in case the resolution needed is less than 13b of accuracy. In fact, the choice of the amplifier for the Large Hadron Collider system developed with 12b 25MS/s pipeline was a slew rate enhanced folded cascode as shown in Fig 5-3. [Visu's thesis]

5.5 Class AB Amplifier

To get 90dB of dynamic range, a Class AB was implemented as in Fig 5-7. This category of amplifier consumes more power than a folded cascode with a slew rate enhancement circuit, but has higher output voltage swing and inherently provides a high slew rate. The amplifier that was implemented had 55 dB of gain and 100MHz of bandwidth. This in combination of the fine settling amplifier of 750MHz and 75dB of gain provides an SFDR of 90dB, enough for a 14b resolution.

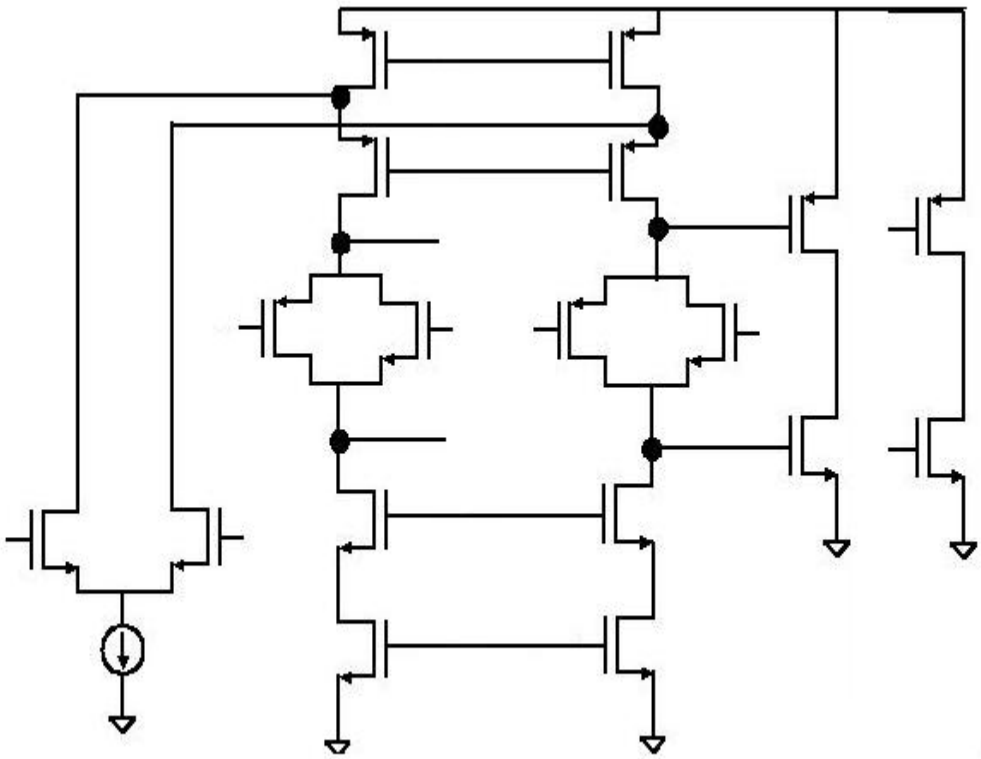

Figure 5-7: Implementtion of class - AB amplifier

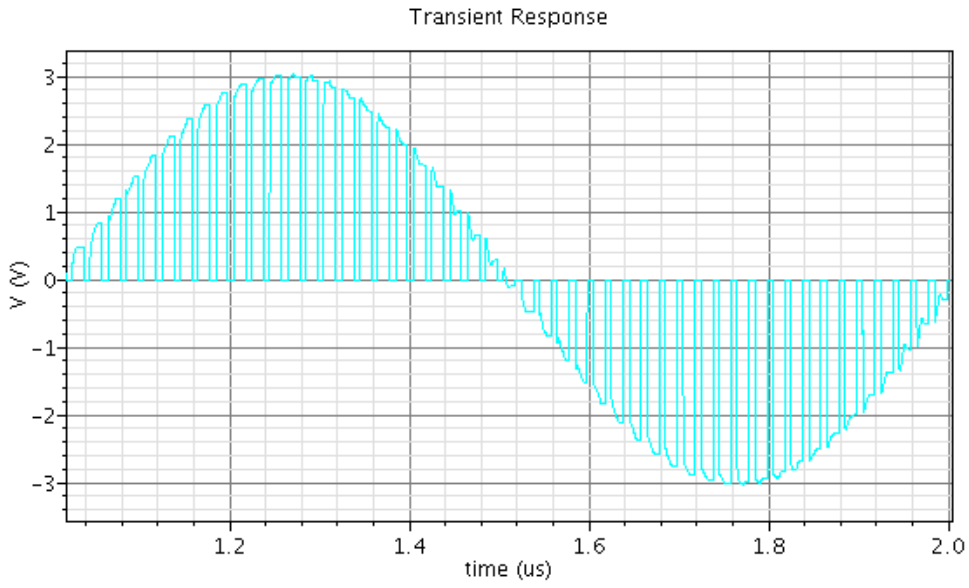

Figure 5-8: Time domain output of system with Class-AB estimation amplifier

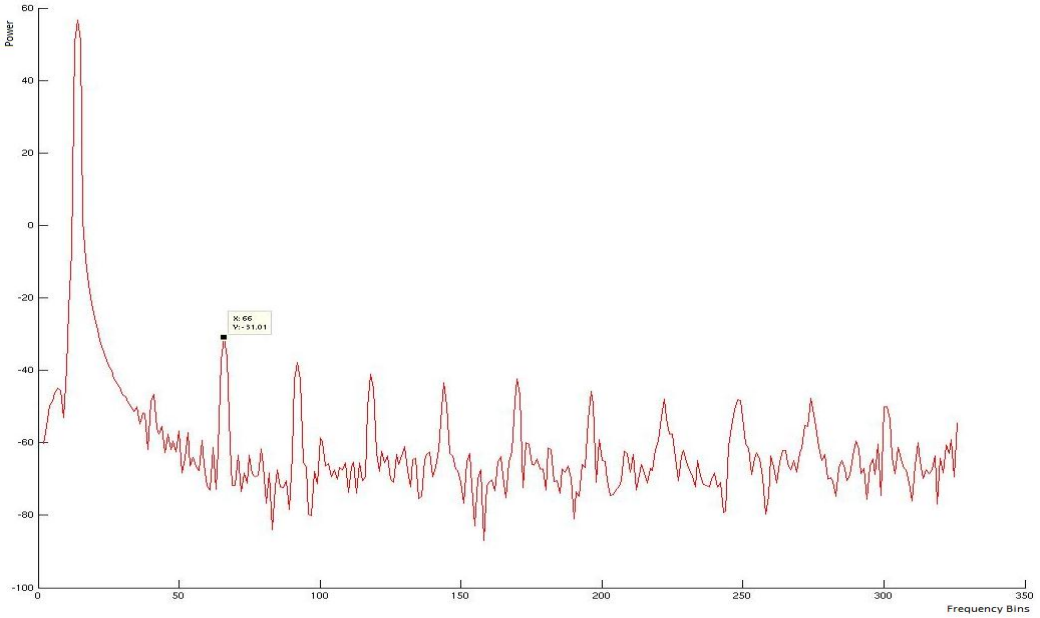

Figure 5-9 Spectrum of output with Class-AB estimation amplifier

Fig 5-8 shows the time domain output of the class-AB amplifier used as the estimation amplifier, as can been the output is better behaved than the slew rate enhanced amplifier. Fig 5-9 shows the spectrum of the output and as can be seen, the SNDR is better than 85dB and the THD3 is -103dB with the same number for the SFDR. However, the Class-AB amplifier consumes around 24 mW of power and also needs internal compensation with a huge capacitance. Hence, this adds to the memory issue and power consumption.

5.6 Gain-Boosted Folded Cascode Amplifier

To conserve power, a folded cascode amplifier with gain enhancement was implemented as the final choice, to provide moderate gain and bandwidth in the estimate phase to mitigate accuracy issues and memory effects by improving the settling behavior

in the estimate phase. The gain boosted folded cascode amplifier that was implemented as in Fig 5-10 had 70dB of gain and 300MHz of bandwidth.

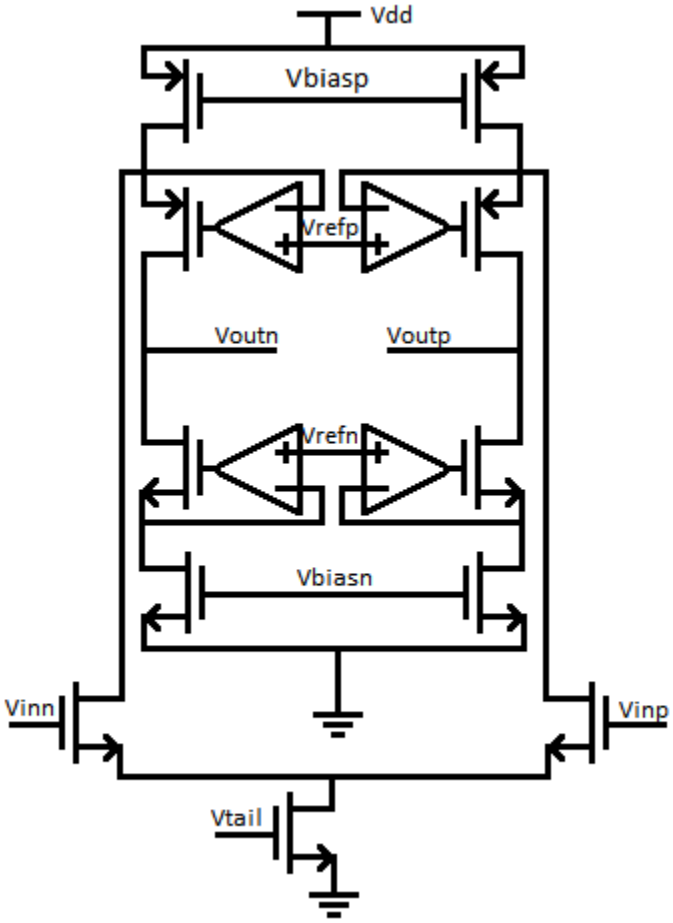

Figure 5-10: Gain boosted folded cascode amplifier

All simulations were done at worst case inputs, full signal swing of 3V with frequency of 1MHz. Sampling rate was calculated to provide 10Msps output from the cyclic ADC. The clock period for a single operation (sampling, estimating or fine settling) is 6ns. This represents an ENOB or 12.49b and a FoM of 16pJ/conversion.

5.7 Fine Settling Amplifier

The first amplifier provides the estimate of the final value and then the fine settling amplifier provides the final fine settled value. The margin of error depends on the resolution that is needed from the ADC and error requirement was determined to be 162uV provided 14b and a 3V signal swing. Hence the fine settled value for the first cycle has to be within half of 162uV from the final value to have a 14b resolution performance.

It was determined from these values that the required gain from the total system is 125dB (including 12dB reduction for CLS 1/3rd CLS capacitance value + 6dB design margin + 3dB architecture margin). Since in the split CLS technique the gain of the system is equal to the product of the gains of the two amplifiers, the total gain is equal to the sum of the gains in dB (This is assuming that the first amplifier linear settles during the estimate phase and not complete slewing). This allows the second amplifier to have a gain of just 70dB and a bandwidth of 750MHz. The cascode was implemented as a 11 transistor telescopic cascode as shown in Fig 5-12.

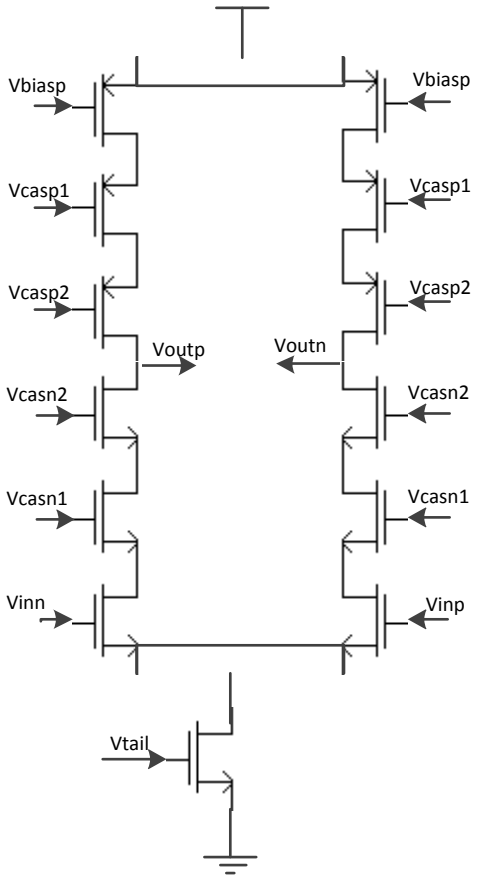

Figure 5-12: Telescopic cascode with triple cascode

Since the triple sampling technique allows to have a very low voltage swing amplifier at the fine settling phase, it is possible to use telescopic cascodes for this amplifier. In fact, a 9-transistor OTA as shown in Fig 5-13 with the required specifications was tried and there was no degradation in SNDR. This shows that the required gain and bandwidth can be easily achieved without having to worry about voltage swings or power hungry multi-stage OTAs.

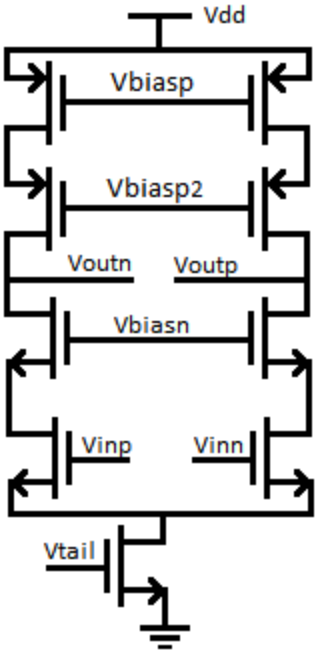

Figure 5-13: Final implementation of the fine settling amplifier

The final amplifier that was implemented in the system used a 9-transistor fully differential telescopic cascode with 70dB of gain and 700MHz of bandwidth.

5.8 Conclusion

This chapter presented the details of how the amplifiers are implemented and the details of the architectures that can be used for the estimation amplifier and the predominantly suitable architecture of telescopic cascodes for the fine settling amplifier. Chapter 6 discusses how the Cyclic ADC is built using these amplifiers in greater detail.

Chapter 6

CYCLIC ADC

6.1 Introduction

As presented in Chapter 2, a cyclic ADC is a sub-class of pipeline ADCs which uses the first stage of the pipeline to cycle its output onto its input. This kind of architecture is slower by a factor of the number of bits needed to resolve by the ADC, but is extremely area and power efficient. Such architectures are extremely suitable in areas such as automotive applications. This chapter discusses the implementation of the Cyclic ADC along with some techniques that reduce power consumption and in combination with Triple Sampling and the RSD technique.

6.2 Traditional Cyclic ADC Architectures

In a traditional architecture, the single stage of the pipeline ADC samples the input, takes the coarse decision and calculates the output residue voltage. This residue voltage is then sampled onto an additional capacitor and then passed on to the input of the same stage during the next sample phase. This way, one sample is obtained from the input during every N cycles for an N-bit ADC. By using 2 stages of a pipeline, this can be brought down to N/2 cycles for an N-bit conversion.

Existing cyclic ADCs typically use two stages or an explicit sample and hold amplifier and/or capacitor at the output of the stage. A dedicated sample and hold

architecture requires that the accuracy of the sample and hold amplifier be as good as the main amplifier itself. This requires high power and area and especially so for higher resolution converters.

In ADCs, the capacitors are sized according to the thermal noise and the resolution needed from the ADC. In pipeline ADCs, after the initial bit is resolved, the next stage input needs be accurate only to one less than the total resolution. This enables the scaling down of the capacitors along the stages. However, in case of the cyclic ADC, the same stage loops back onto itself and hence the same stage is recycled. This entails that the capacitors remain the same during the entire conversion and hence the power also is not optimized.

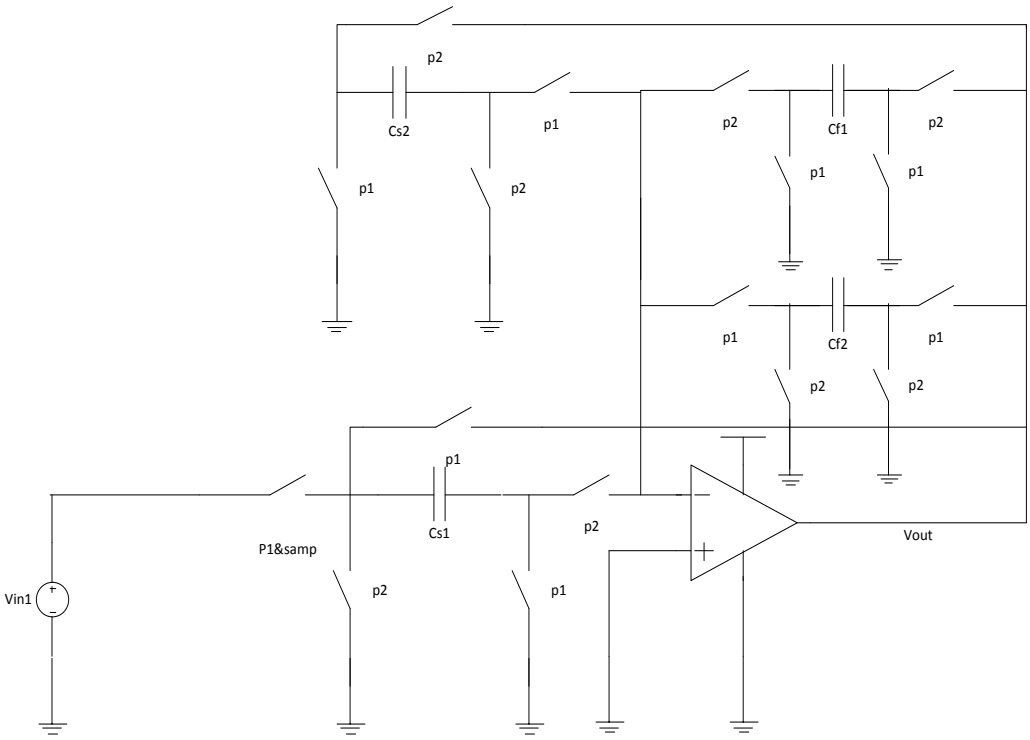

Figure 6-1: Cyclic ADC core without the RSD supplies

Fig 6-1 shows the skeleton of a traditional ADC, without the DAC or RSD supplies, to simplify the diagram. Cs1 samples the external input once every N clock cycles during phi1 and the corresponding output Vout1 is stored on Cf1 during the next clock phase phi2. This output Vout1 is sampled by Cs2 during the same phase phi2 and the corresponding output is stored on Cf2, which in turn is sampled by Cs1 during phi1 and the process continues in a cyclic fashion, hence the name Cyclic ADC. As can be seen, the ADC quickly gets capacitor intensive and considerable extra loading is placed on the amplifier.

For lower resolution converters as such, a dedicated sample and hold capacitor can altogether be eliminated and a simpler scheme which uses the CLS capacitor can be used. Since these two capacitors are charged up during normal gain operations, they do not need an extra sample and hold amplifier to charge them up to the output residue value. Thus the new architectures save on power and area. These techniques are explained in this chapter.

6.3 Non-dedicated Sample and Hold Architecture

The proposed technique makes use of the fact that single large capacitors are built using multiple unit capacitors that match well. In high resolution architectures, the capacitor size is determined by the thermal noise limit which is more than that required by matching and usually in the pF range, built out of smaller unit capacitors in the fF range. This gives the ability to split any capacitor in half as long as it not less than the

size of a unit capacitor or the capacitor becomes less compared to parasitic capacitors present.

As explained in Chapter 3, the pipeline stage is implemented using the gain stage made using the Correlated Level Shifting technique. The circuit has been shown again in Fig 6-2 for easier reference.

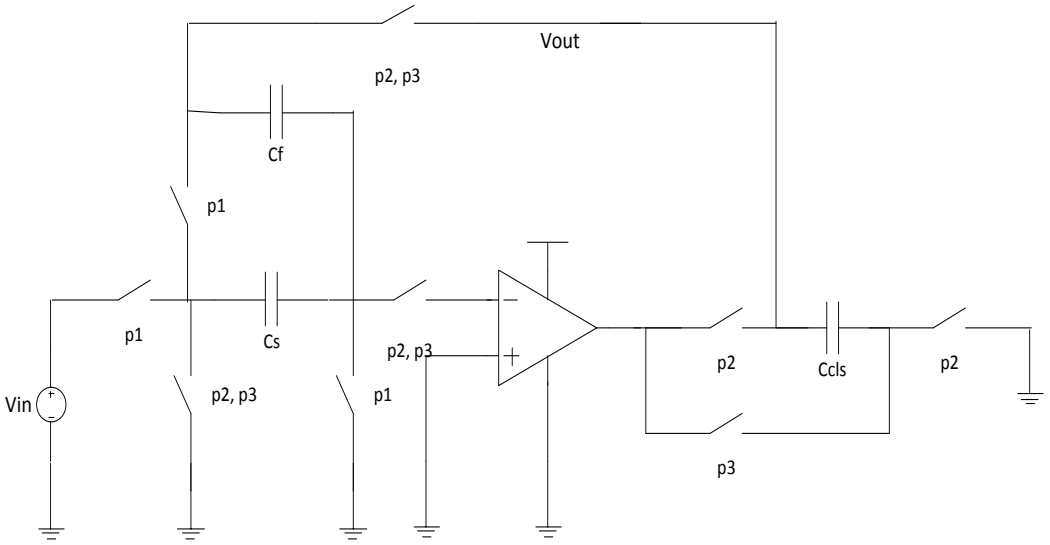

Figure 6-2: CLS gain stage

In the CLS operation, during the fine settling phase, the output is very close to the ideal output and the input terminal of the opamp is very close to ground potential. Hence, if the gain of the opamp is sized large enough, the feedback capacitor Cf sees almost the entire output voltage across itself. The actual voltage across the Cf capacitor is Vout-2Vout/(Aest.Afine) where Aest and Afine are the gains of the estimate and the fine settle amplifiers. If Aest and Afine are sized large enough, the feedback capacitor sees the entire output voltage across it, thus the feedback capacitor acts as an inherent sample and hold capacitor storing the output voltage.

During the next cycle, this capacitor can be split in two using switches and one half (for a 1.5b stage) can be connected between ground and the input terminal of the opamp. This forces charge out of the capacitor and onto the feedback capacitor which had the previous output stored on it. This operation is shown in Fig 6-3.

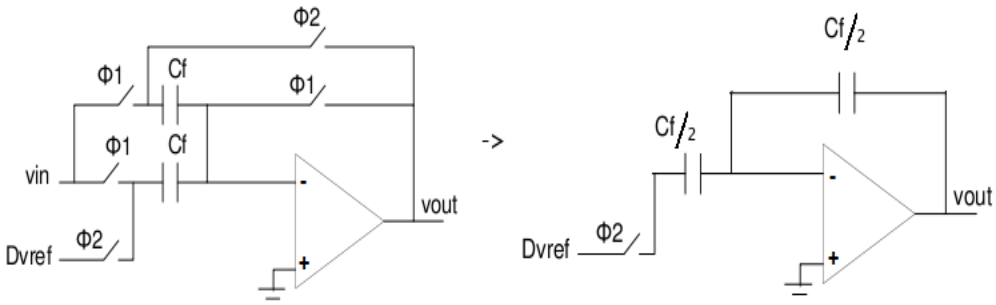

Figure 6-3: CLS with split feedback capacitor

This method of scaling the capacitors cannot be carried on indefinitely as, soon the capacitors will reach the matching limit and/or they become comparable to parasitic capacitance sizes. For low resolution converters, a similar scheme can be seen on the CLS capacitor. The CLS capacitor sees the opamp's output on one side and the output on the other node, for a well-designed system the output node of the opamp sits at Vout/Aest which is very small and if the CLS capacitor is large enough, the charge lost from it during the fine settling phase is small and the voltage across the CLS capacitor is very close to the final output. This thus inherently acts as a sample and hold capacitor as well.

This charged CLS capacitor is then connected in place of the sampling capacitor, this forces charge out of it and onto the feedback capacitor. The original sampling capacitor can be used in place of the CLS capacitor for this phase. If the sampling

capacitor and the CLS capacitor are made of the same size, this can be made to work in cyclic fashion to produce a circuit that provides continuous gain of two (for a 1.5b stage). The circuit is shown in Fig 6-4.

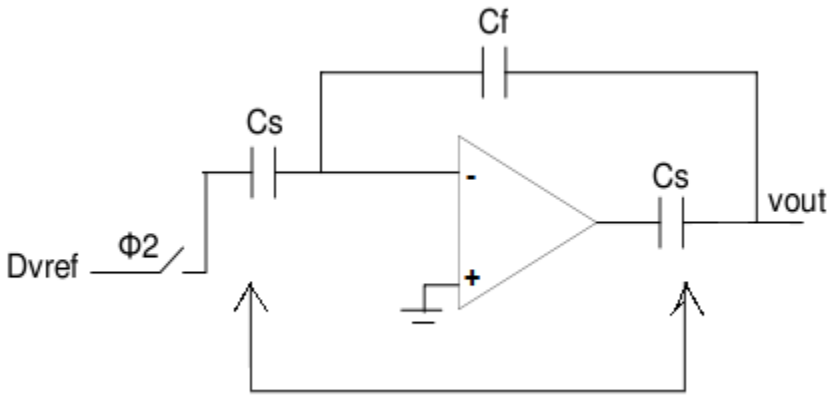

Figure 6-4: CLS capacitor switching with sampling capacitor

The application to Flip-Over Architecture entails much less error accumulation. The architecture is also amenable to capacitor scaling during multiple cycles. Fig 6-5 shows the circuit configured with unit gain cycling over 14 clock cycles. The accuracy is preserved across the cycles. The input voltage was at 33mV, a low input voltage, so that any loss of charges will be seen easily, but the outputs remain within margins of error as shown.

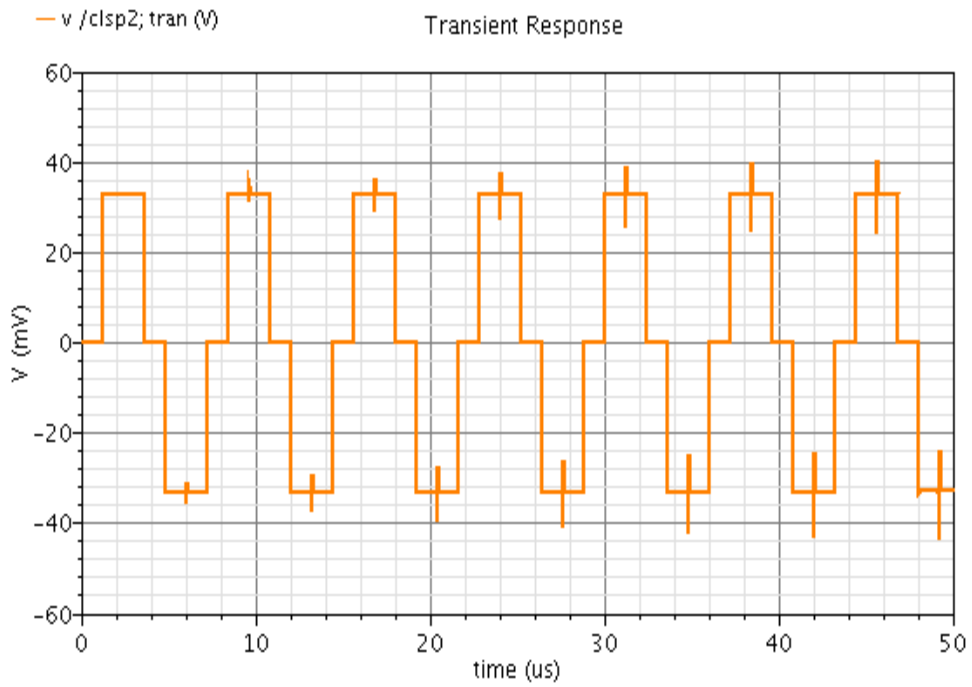

Figure 6-5: Cyclic gain stage output with gain = -1 with the proposed new architecture of CLS capacitor swapping

Fig 6-6 shows the same cyclic architecture with consecutive gains of 2 per each cycle as needed per the cyclic ADC requirements. The final output is very close to the maximum outputs expected with RSD incorporated and accuracy is preserved for these swings as well.

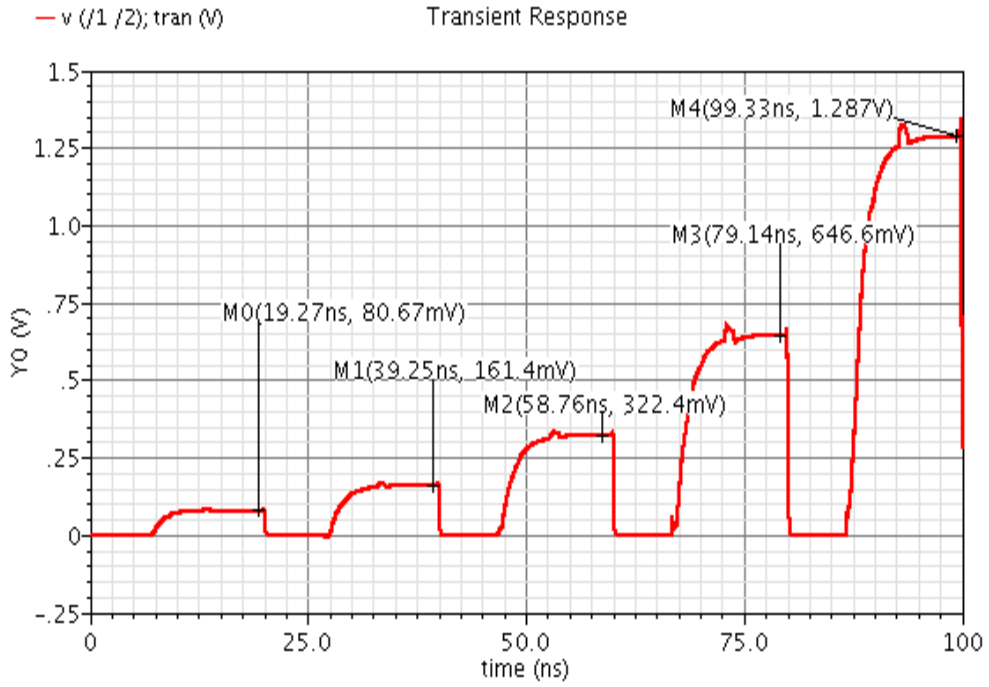

Figure 6-6 Cyclic amplifier with proposed architecture configured with gain of 2 and outputs for the first 5 cycles verifying accuracy

6.4 Cyclic ADC

The technique presented here makes use of the feedback capacitor for high resolution conversions, since a sample and hold capacitor for high resolution would be large. For lower resolution conversion steps, a simple additional sample and hold capacitor is used. These thereby eliminate extra area being spent on a large sample and hold capacitor and hence also saves power.

For the first conversion, when the resolution is accuracy is critical and the capacitance is large, Cf is split as Cf/2 and Cf/2. Both capacitors have the same charge and same voltage assuming they are matched well enough to the resolution needed from

the converter. One of the Cf/2 capacitors is left connected in the feedback path. This prevents the op-amp from being left open and also maintains the voltage across the feedback capacitor. The other capacitor is then grounded or applied to +/-Vref according to RSD during the estimate phase. This causes a charge of Vres-DVref to flow onto the feedback capacitor, which had the voltage Vres initially. Thus, this generates the 2Vin-DVref that is needed for the ADC operation. By incorporating the RSD architecture into this cyclic operation, the cyclic gain stage is converted into the Cyclic ADC.

Fig 6-7 shows the output with the accurate settling voltages. The input voltage is set such that the input sees the full 3V swing which triggers the worst case non-linearity in the switches and the amplifiers, but still the output settles to the accurate output value with the proper RSD output voltages. The first few cycles have also been shown in the plot to verify the accuracy and working of the cyclic ADC.

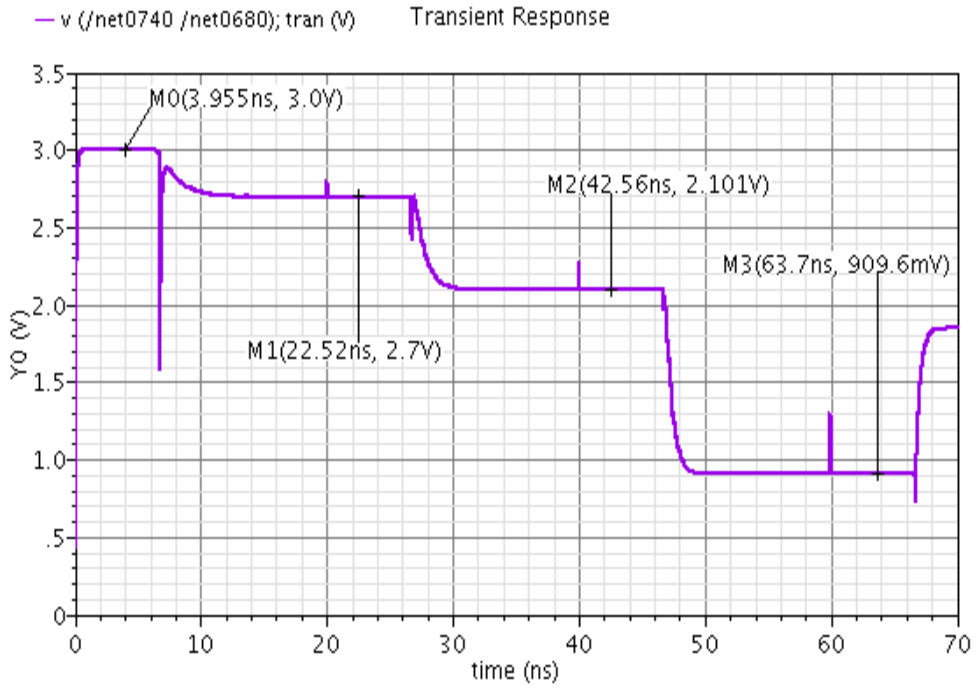

Figure 6-7: Cyclic ADC with the RSD output voltages

Also, since the capacitances have been reduced, the load that the op-amp sees is lower. This operation can be completely integrated with the CLS technique and hence Correlated Triple Sampling. But, the capacitors cannot be scaled down indefinitely as they may become less than the parasitic capacitances at the input of the opamp. Before this limit is reached, the capacitor scaling is stopped and the CLS caps are swapped with the sampling capacitor just as in the charge re-distribution architecture. In this work, capacitors are scaled starting from 6pF to 3pF. For lower resolutions, further scaling can be done. If swapping the CLS capacitor accumulates error larger than tolerable, a smaller sample and hold capacitor at the output can be used. The relatively small size of this capacitance does not hurt the power of the op-amp.

This can then be used as the normal cyclic converter operation. Both architectures were implemented, but configured as a cyclic gain stage rather than ADC

and looped 15 times. The technique of switching CLS capacitor with the sample capacitor however entails that a small error is accumulated over the cycles since the CLS capacitor is not at perfect virtual ground voltage. However, it can be shown that, by budgeting an extra 6dB gain for the amps, the error can be minimized below the LSB voltage levels thereby reducing the impact of this error voltage. Also, a good part of the gain can be dedicated to op-amp1 to minimize this error. It was seen that CLS swapping resulted in a final error of 1.2 V where the input range is supply is 3V. This error is less than LSB/2.

6.5 Conclusion

Chapter 6 presented the details of how the Cyclic ADC is implemented and the details of the tradeoffs involved. It also discussed the proposed non-dedicated sample and hold architecture that can be used to reduce power consumption and on-chip area. Chapter 7 concentrates on the background digital components and the calibration routine that has been proposed to correct for the non-idealities that may still be present.

Chapter 7

DIGITAL COMPONENTS

7.1 Introduction

The previous chapters explained how the analog components of the ADC function and how they are implemented. For modern processes, it is very cost effective and robust to push as much processing to the digital side and reduce the analog complexity. RSD algorithm for instance, makes the analog components very robust to process variations and reduces analog design overhead while pushing the recombination process to the digital domain.

7.2 Switch Reduction

Since the cyclic ADC is very switch and capacitor intensive, a lot of digital gating of clocks can be performed to minimize the number of switches while increasing the number gates involved in the processing of the clocks. This way, the amount of parasitics that load the main amplifier system are also reduced and saves on routing parasitics as well.

The digital components were implemented using standard digital logic blocks composed of static NAND, NOR, NOT and XOR gates. These logic gates were also used to process the clock signals to reduce the number of switches. The schematic with the reduced number of switches is shown in Fig 7-2 compared to the Fig 7-1 which does not have the reduction.

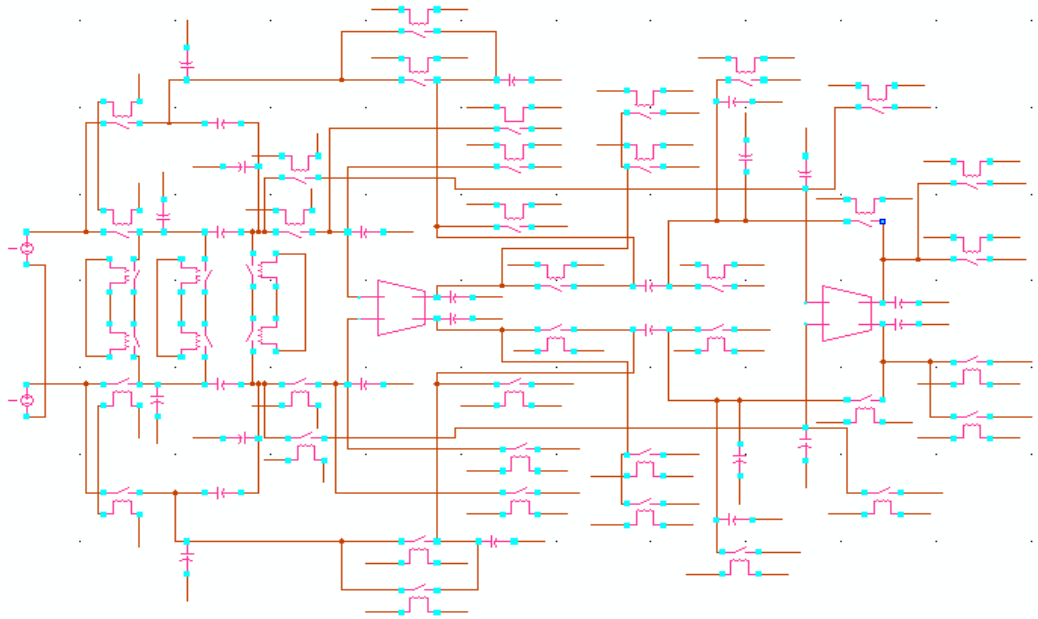

Figure 7-1: Schematic of a single path prior to switch reduction

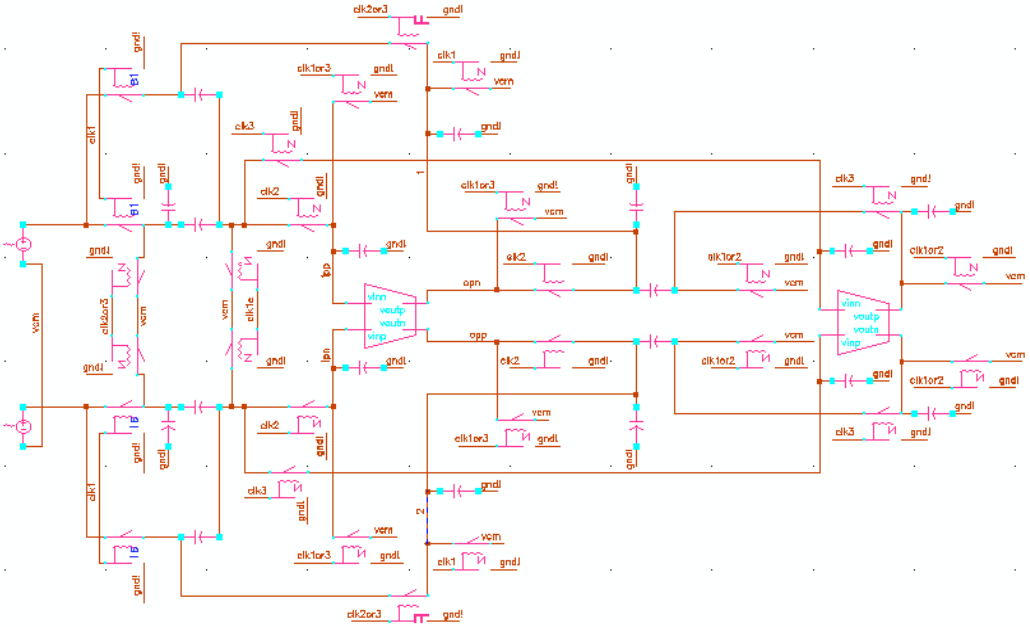

Figure 7-2: Schematic of single path after switch reduction

Since most clock signals are gated along with control logic, gating those instead using switches in parallel helps reduce switching transients and the number of switches that are involved while processing. This reduces parasitic capacitances attached to switching nodes.

7.3 D Flip Flops

The D Flip flops were designed using TSPC registers as shown in Fig 7-3.

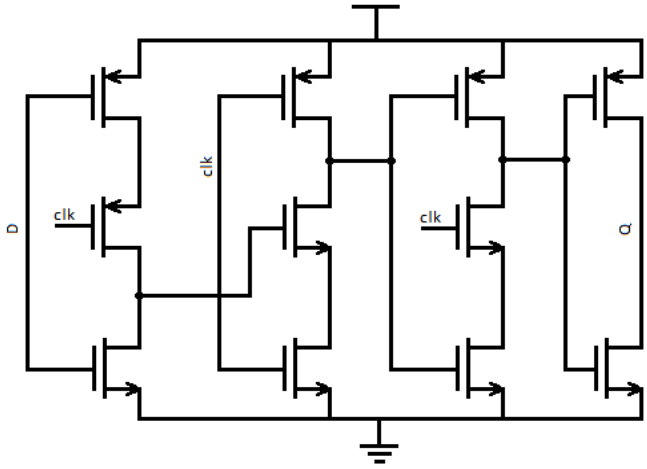

Figure 7-3: TSPC register used to implement the D Flip flops

7.4 Clock Generator

The clock generator used in this work has the following construction. Each clock phase is 6ns wide and has 250ps of non-overlap time and rise and fall times of 150ps. The circuit was carefully laid out to minimize any mismatch in the paths so as to reduce any

variation in the timing of the paths. The clock signal was as well routed with attention to detail to minimize any variation in the sampling times to eliminate spurs.

7.5 Digital Recombination block

The digital recombination block is composed of a serial to a parallel converter and full adders. The delay elements act by passing on the sampled comparator values during the previous clock phases through 14 delay elements. During the final clock phase of the conversion (14^{th} clock cycle), all the values are passed on in parallel to another set of 14 D Flip flops. This is then used by the set of 14 full adders with ripple carry logic to produce the final digital value.

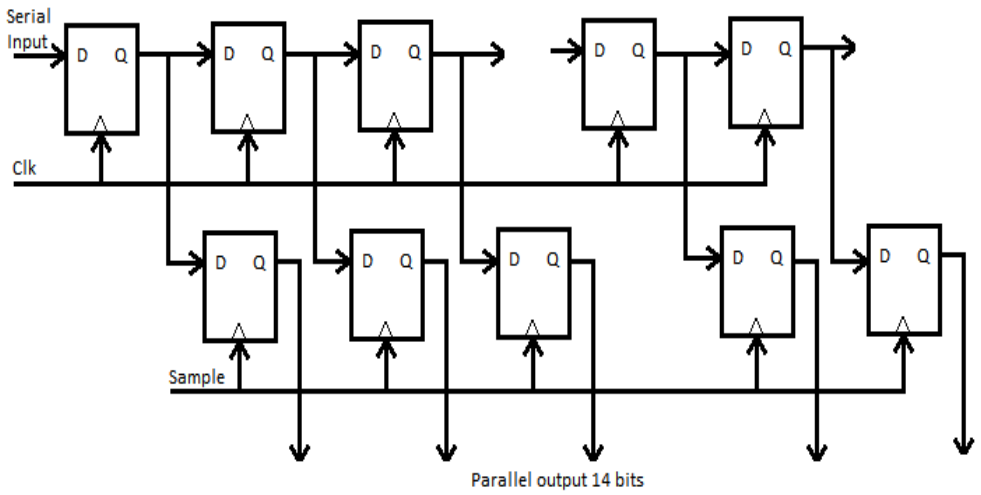

Figure 7-4: Serial to parallel converter

This way, each delay block only has to drive only one more digital block and have 14 clock cycles for the carry to ripple through the set of full adders. A serial input is required as the cyclic converter takes only one set of decisions during each clock phase.

7.6 Digital Calibration

To achieve 14b precision requires very careful design and layout along with good error margins and robustness against process variations, mismatches. However, once the limits on these fronts are reached, it becomes too power intensive to push them further. It is better instead to turn to digital calibration which is more power efficient, scalable, controllable and well suited to modern digital CMOS processes where the cost of addition of a transistor is immaterial.

There are digital and analog calibration techniques, but given the trend of reduced cost of digital logic and lower performance from analog side, digital calibration is a better choice. Digital calibration can be split into four major types, factory calibrations, offline calibration, online calibration and pseudo-online calibration techniques.

Factory calibration techniques such as trimming techniques can be performed during fabrication at the factory, but these techniques are very expensive as they take time and they do not track variations due to aging effects, temperature gradients and power supply variations on the chip which occur during either the life time of the chip or during shorter intervals during the operation of the chip.

The offline calibration techniques involve calibration at start up or interrupting normal operation at routine intervals and passing a test signal from which calibration detects the errors in the system from the way the system has modulated the test signal. These calibration techniques are very fast and can mostly track aging effects, but cannot

track temperature gradients and supply variations and also importantly involve interrupting routine operation of the component.

Online calibration is a background process and it happens without interrupting the normal operation of the ADC. However, these techniques are very slow and usually take millions of samples. They also eat into the signal dynamic range.

A good trade-off among all these techniques seems to be the pseudo-online calibration techniques. Some pseudo-online calibration techniques have been proposed earlier of which [8],[20] are especially note-worthy.

[20] involves the “Skip and Fill” method proposed by Dr.Moon; This involves skipping some input samples to generate a slot for calibration signal. The skipped samples are then retrieved using an interpolator. The technique however restricts the input signal frequency to about 1/3Fs and requires a 39^{th} order interpolator for this. Higher signal frequencies require higher order interpolators.

[8] proposed by Dr.Erdogan and Dr.Lewis proposes to use a queue based architecture wherein dedicated sample and holds are used to sample the input in a buffering fashion, while the ADC can convert more samples than in the buffer. This generates additional time when calibration signal can be fed in and calibrate the ADC. This technique again needs additional sample and holds which are as accurate and as fast or faster than the ADC's sample and holds and hence can be power hungry.

The pseudo-online calibration technique proposed in this work makes use of the fact that the cyclic ADC has 3 inputs, of which 2 can be dedicated to processing the input and the third path can be used to calibrate the ADC. Once this path is calibrated, it can be switched with the input signal and that path can be calibrated. By routinely calibrating the paths, we can track errors due to drifts, capacitance mismatch and opamp imperfections. However, this does not affect the routine operation of the ADC. If needed, the calibration can also be done offline at startup and use the third path as well to process inputs.

The proposed method was invented by Dr.Bahar Jalali Farahani to be applied to cyclic ADCs in general using the CLS techniques, but can also be applied to normal cyclic ADCs by setting the relevant coefficients to zero. The calibration algorithm uses a major carry jump approach and defines a cost function based on which the coefficients are then used to compute the correct value of gains by the LMS method.

Output of the cyclic ADC during phase 3 is given as:

$$Vout = [(1 + \alpha)Vin - \alpha VDAC]\beta$$

Where α and β are terms corresponding to capacitor mismatch and op-amp finite gain as in:

$$Vout = [\left(1 + \frac{C1}{C2}\right)Vin - \frac{C1}{C2}VDAC](\frac{\varepsilon(\gamma + \lambda + \varepsilon)}{(\varepsilon + 1)(\lambda + \varepsilon)})$$

Where ε, λ, and γ are functions of the size of the three capacitors (sampling, feedback and level shifting cap) as well as the Opamp gain. These two parameters are calculated for each path during the start-up calibration routine and are used to take into account the mismatch between the capacitors in different paths during online calibration routine.

Use Vcal=Vr/4 force d1=1, makes the digitized residue of the first cycle equal to:

$$D1 = [(1+\alpha)\frac{Vr}{4} - \alpha Vr]\beta$$

Similarly with forcing d1=0 for Vr/4,

$$D0 = [(1+\alpha)\frac{Vr}{4}]\beta$$

The error function is defined as:

$$e = (D0actual - D0ideal)^2 + (D1actual - D1ideal)^2$$

Minimizing the error function with respect to α and β gives the appropriate objective function for a Least-Mean-Square algorithm that updates the estimation of parameters:

$$\alpha(k+1) = \alpha(k) - \mu\frac{\partial e}{\partial \alpha}$$

$$\beta(k+1) = \beta(k) - \mu\frac{\partial e}{\partial \beta}$$

The output model with third order non-linearity is:

$$\overline{\overline{Vo}} = [\ (1+\alpha)Vin - \ \alpha Vdac]\beta + [(1+\alpha)Vin - \alpha Vdac]^3\gamma$$

Since the nonlinearities are most felt near the supply extremities, three measurements are made at Vr/4, Vr/2 and Vr.

$$e = (D2actual - D2ideal)^2 + (D1actual - D1ideal)^2 + (Doactual - Doideal)^2$$

Beta and Gamma have similar correction functions.

7.7 Conclusion

Chapter 7 presented the details of the implementation of the digital components that are present in the ADC. It also presented the novel calibration techniques that have been proposed to increase the linearity of the ADC. Chapter 8 presents the details of how the ADC has been laid out to achieve good matching effects and the area details of the ADC.

Chapter 8

LAYOUT

8.1 Introduction

As explained in Chapter 3, the gain of the switch capacitor stage is determined by the number of bits being resolved by the stage. This gain is then set by the ratio of the capacitances Cs and Cf and the accuracy of the gain is a key factor that determines the resolution that can be achieved by the gain stage and hence the entire ADC.

Thus, the gain must be as accurate as possible. The gain of the stage set by the capacitors is determined by how well the two capacitors are matched to each other. The capacitor matching is determined by the layout of the capacitors. Thus, extreme care was taken when laying out the capacitors.

8.2 Common centroid and unit cell layout for matching devices

It has been reported that matching of two components is directly proportional to the square root of area and inversely proportional to the physical distance between two components placed on a chip. Thus to get good matching between the two capacitors, the capacitors must be as close to each other as possible and as large as possible. Further, the environment that each component has must be identical [28].

These concepts are implemented by choosing a unit element and then replicating the unit elements to attain the required sizes of the components. To a second degree of accuracy, the current path through each element becomes important; hence each element is made such that current flows through them in both directions. Common centroid layout of components has been shown to be very good at matching two components and is very easy to implement using unit elements.

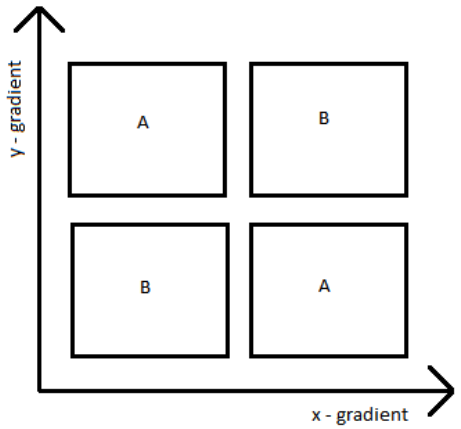

Figure 8-1: Common centroid layout

Fig 8-1 shows the concepts of common centroid layout. When there are linear variations across the chip, the gradient makes one side askew from the other, by splitting a single element into two and diagonally opposite it and by placing the component to match in par with them, the linear gradients tend to cancel out.

By using a single common-centroid laid out block as a higher level building block, bigger blocks are built. This way, when joined up, each block sees the exact same surroundings and hence matching is improved. Further, at the end of the entire block

dummies are placed to improve matching, Fig 8-2 shows building up of the unit blocks to form a bigger block.

The entire unit cell was built such that linking of the blocks can be accomplished merely by placing them adjacent to each other both vertically and horizontally. This technique has been derived from the usual digital layout which uses the concept for horizontal building for the power supply lines. This has been shown in Fig using a stick diagram and in Fig for the actual layout of a unit block transistor of size 10u/340nm.

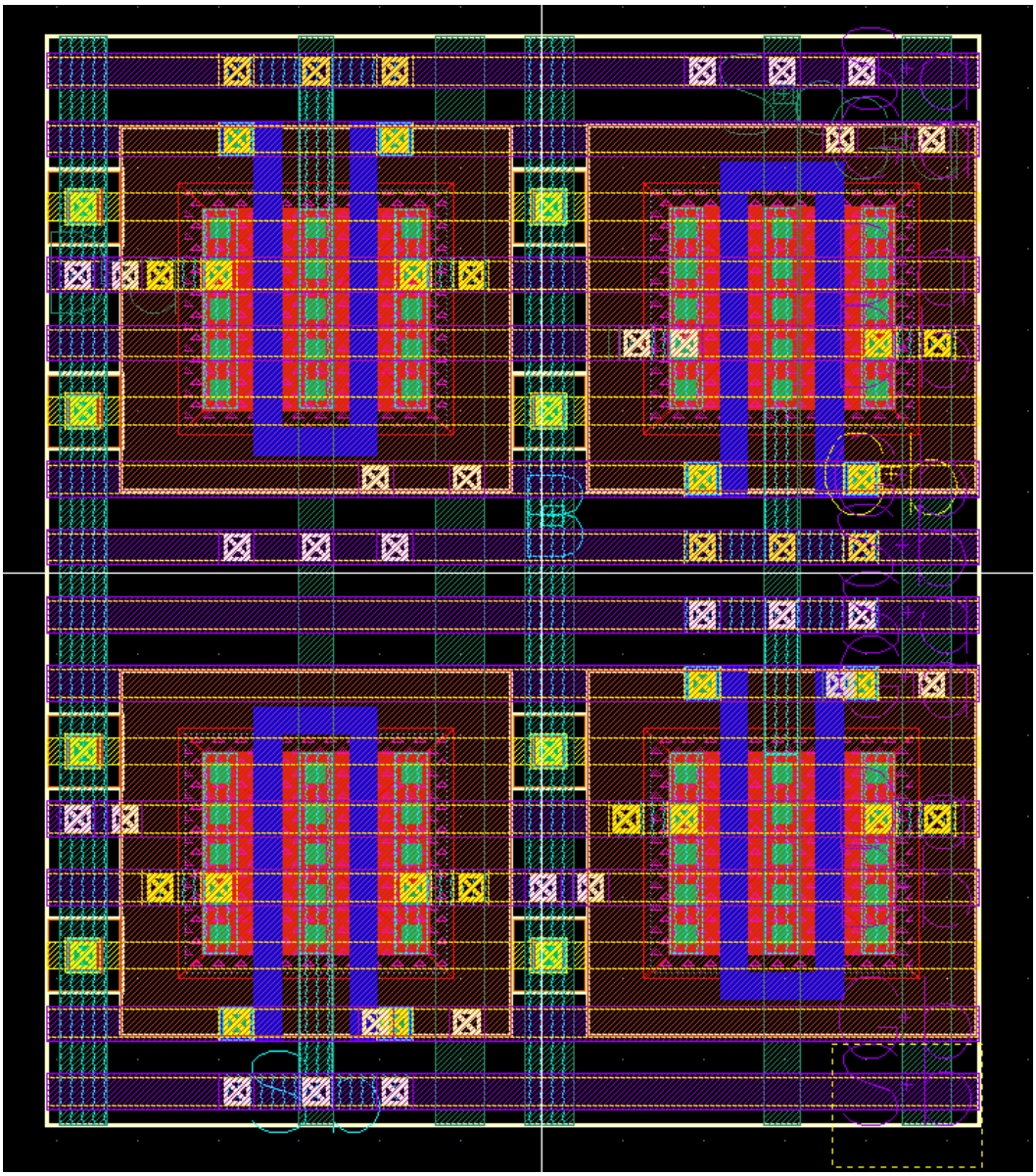

Figure 8-2: Common centroid unit cell layout for the matching transistors

Metals were sized to take care of current density and not too big so as to accumulate parasitic capacitances. Fig 8-3 shows the layout of the both Aest and Afine built from the unit cell transistors in common centroid pattern.

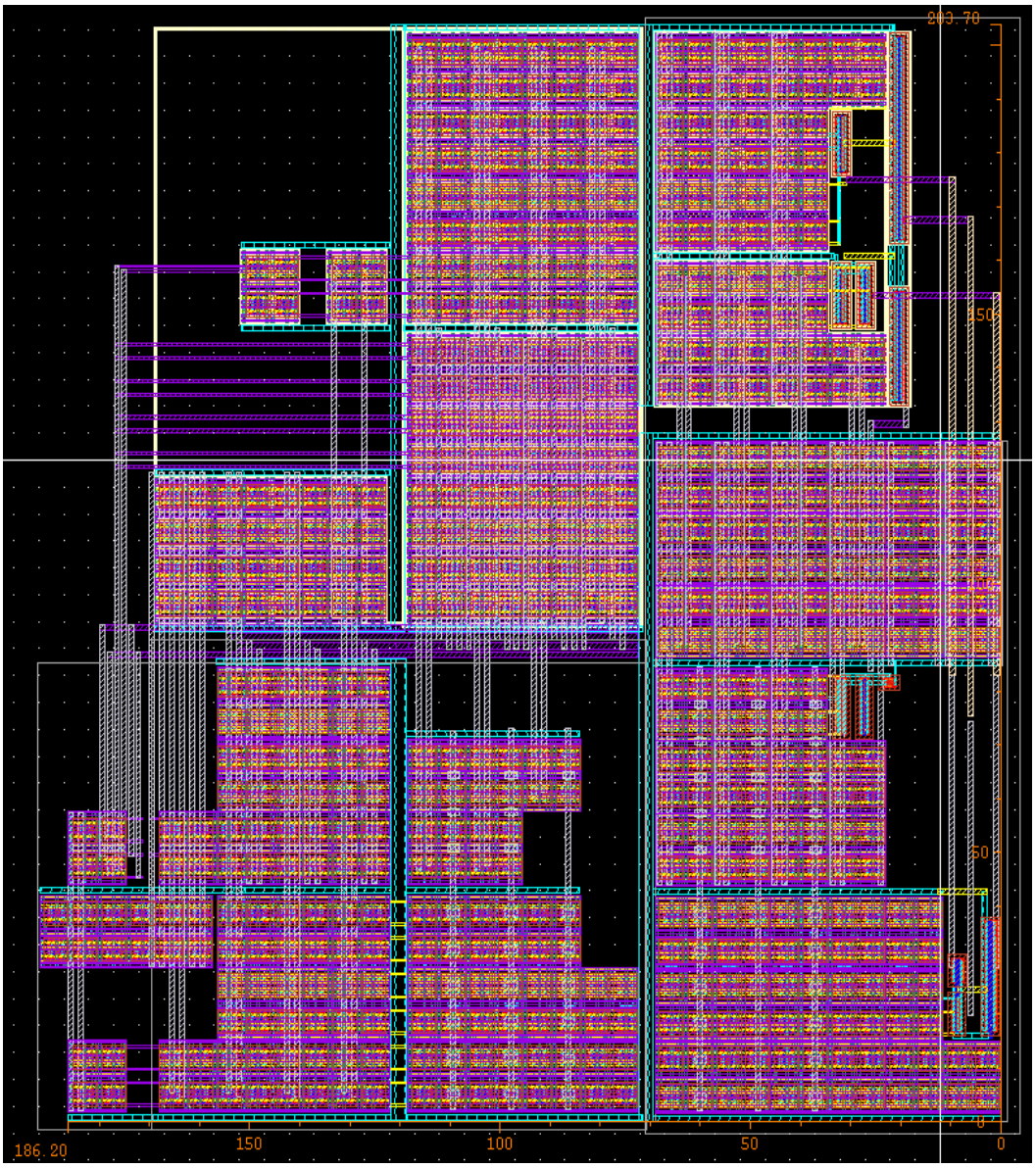

Figure 8-3: Aest and Afine layout

The capacitors are MiM capacitors and are composed of unit elements that are 50fF put together to form larger capacitors. Fig 8-4 shows the layout of the unit block and Fig 8-5 shows the layout of the bigger blocks. It can be seen that in the basic unit element, the capacitors are not completely connected; this is to make the capacitors totally symmetric, but when the adjacent capacitances are placed against each other, this forms connections and preserves symmetry.

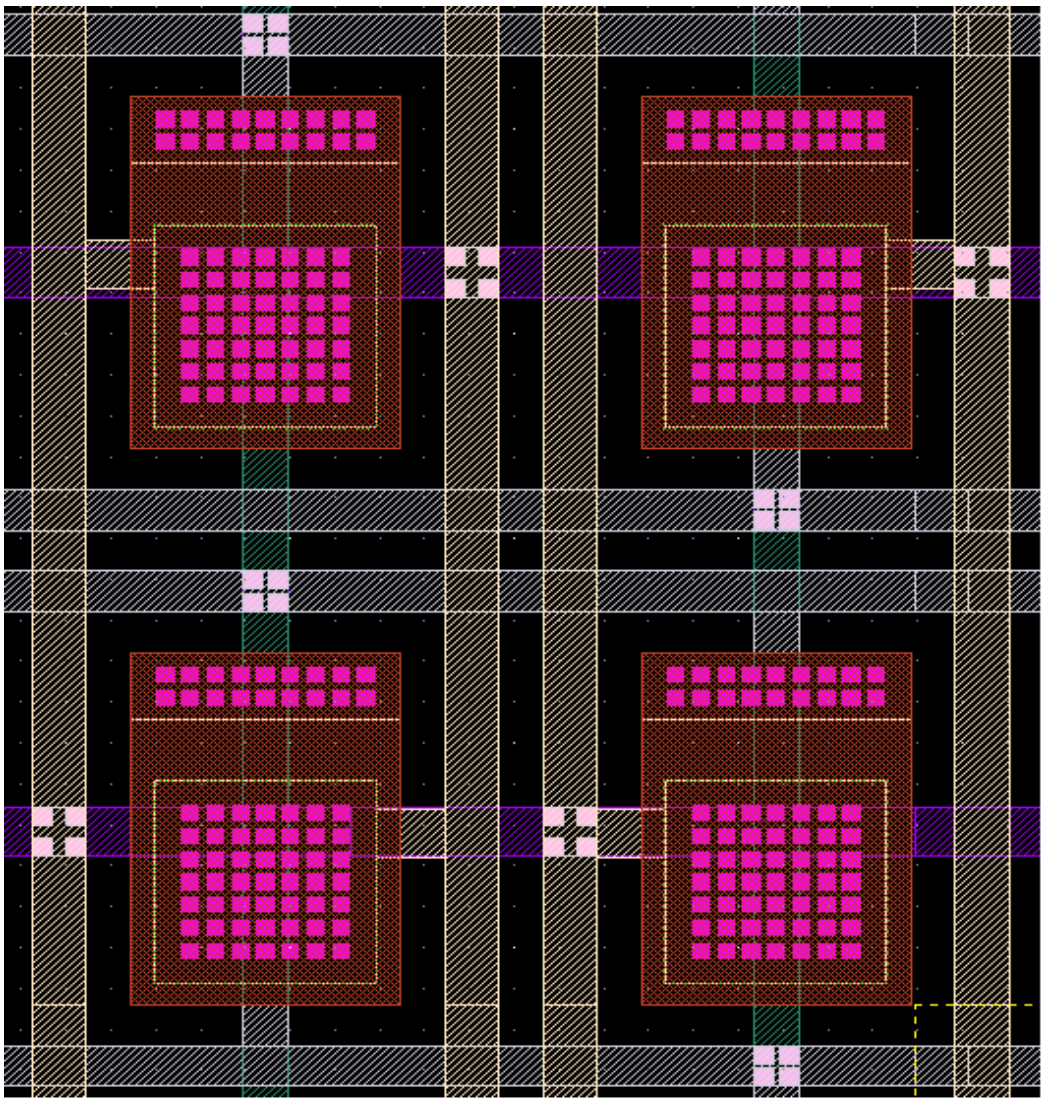

Figure 8-4: Unit cell common centroid layout for capacitors

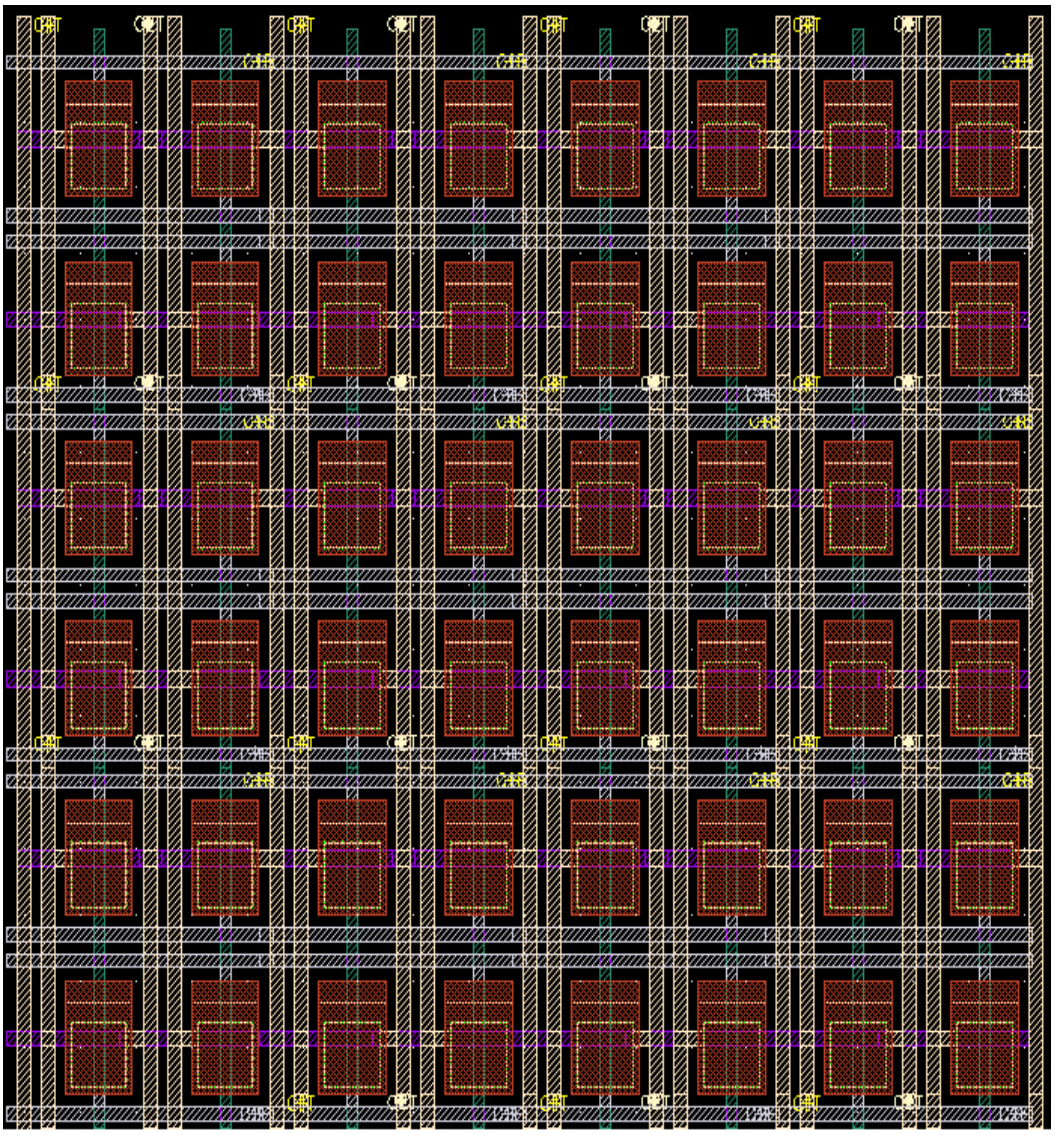

Figure 8-5: Block of capacitors laid out with common centroid concept

8.3 Floorplan

The analog parts are sensitive to noise and the digital components swing between the supply voltages, generating a lot of noisy components during the rise and fall of the clock signals. Hence, the components are separated as much as possible on the chip. Plus, the capacitances are placed in between these components to act as decoupling capacitors.

It has also been reported that, due to the mechanical stressed involved in modern CMOS processes, the components placed near the edges of the chip are more likely to suffer from varied stresses and hence varied electrical properties, hence it is better to place the matching critical components near the center of the chip, hence the capacitors are placed in the center of the set of blocks to improve upon their matching.

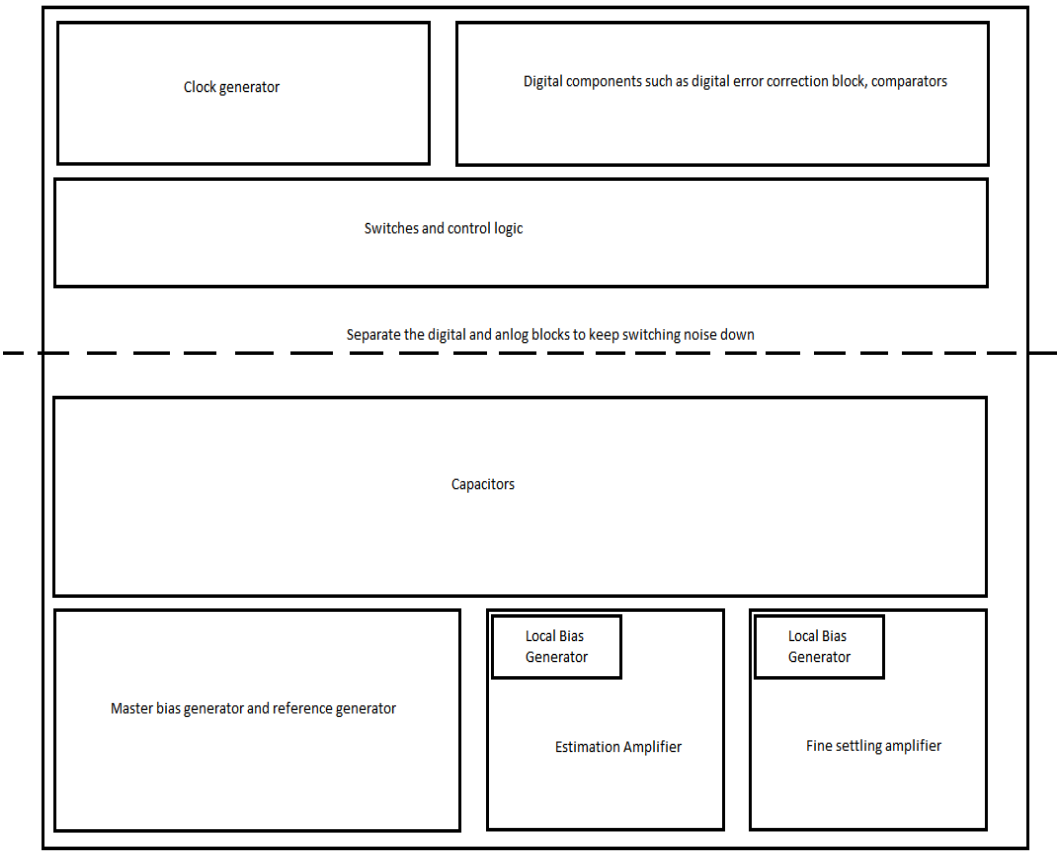

Figure 8-6: Chip floor-plan

Fig 8-6 shows the conceptual floorplan that a chip can use and Fig 8-7 shows the actual layout and the floorplan of the triple sampling channels. Fig 8-8 shows the layout of the entire triple channel cyclic ADC each channel working at 3.35MS/s and 14b

resolution and can be configured to work as a single channel ADC with 14b resolution and 10MS/s sample rate.

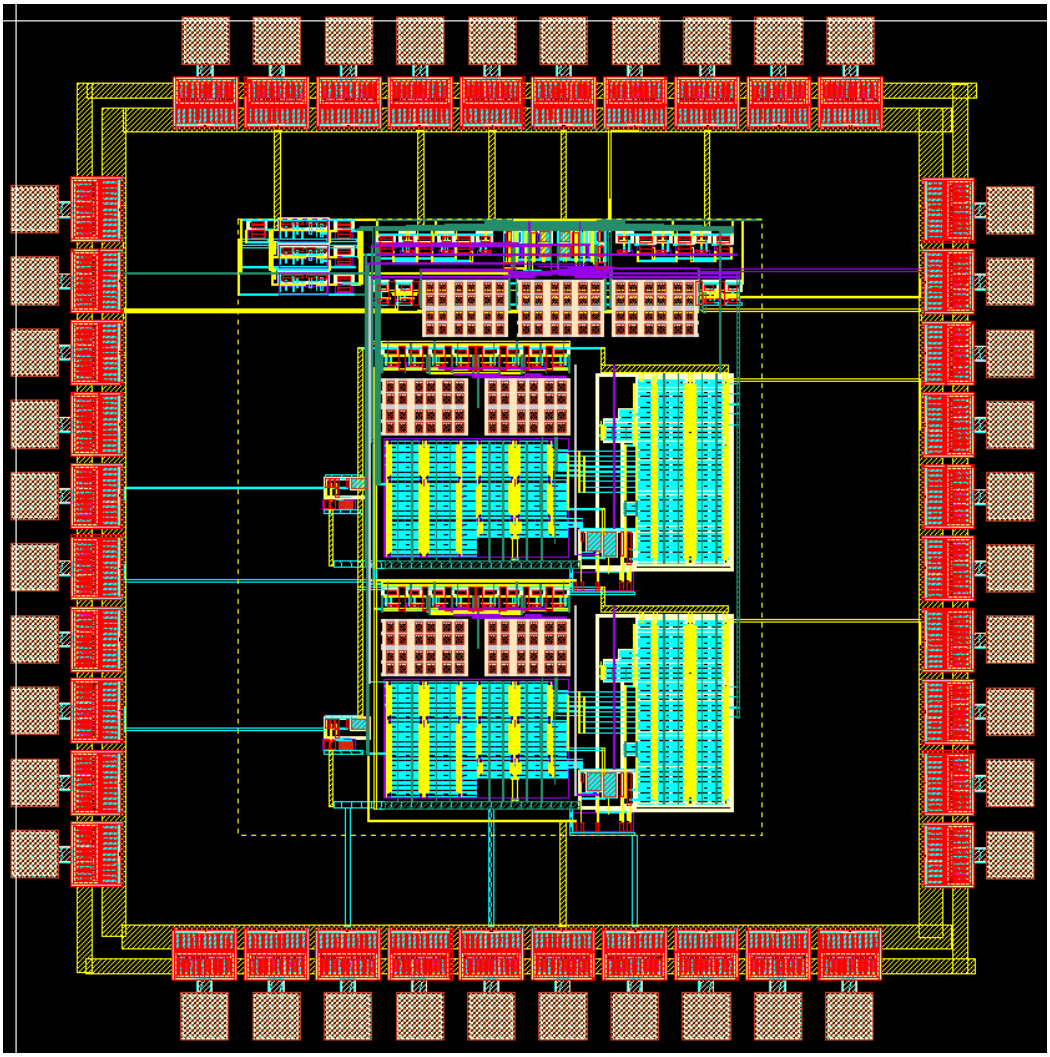

Figure 8-7: Triple sampling stages fabricated on UMC 180nm in March, 2012

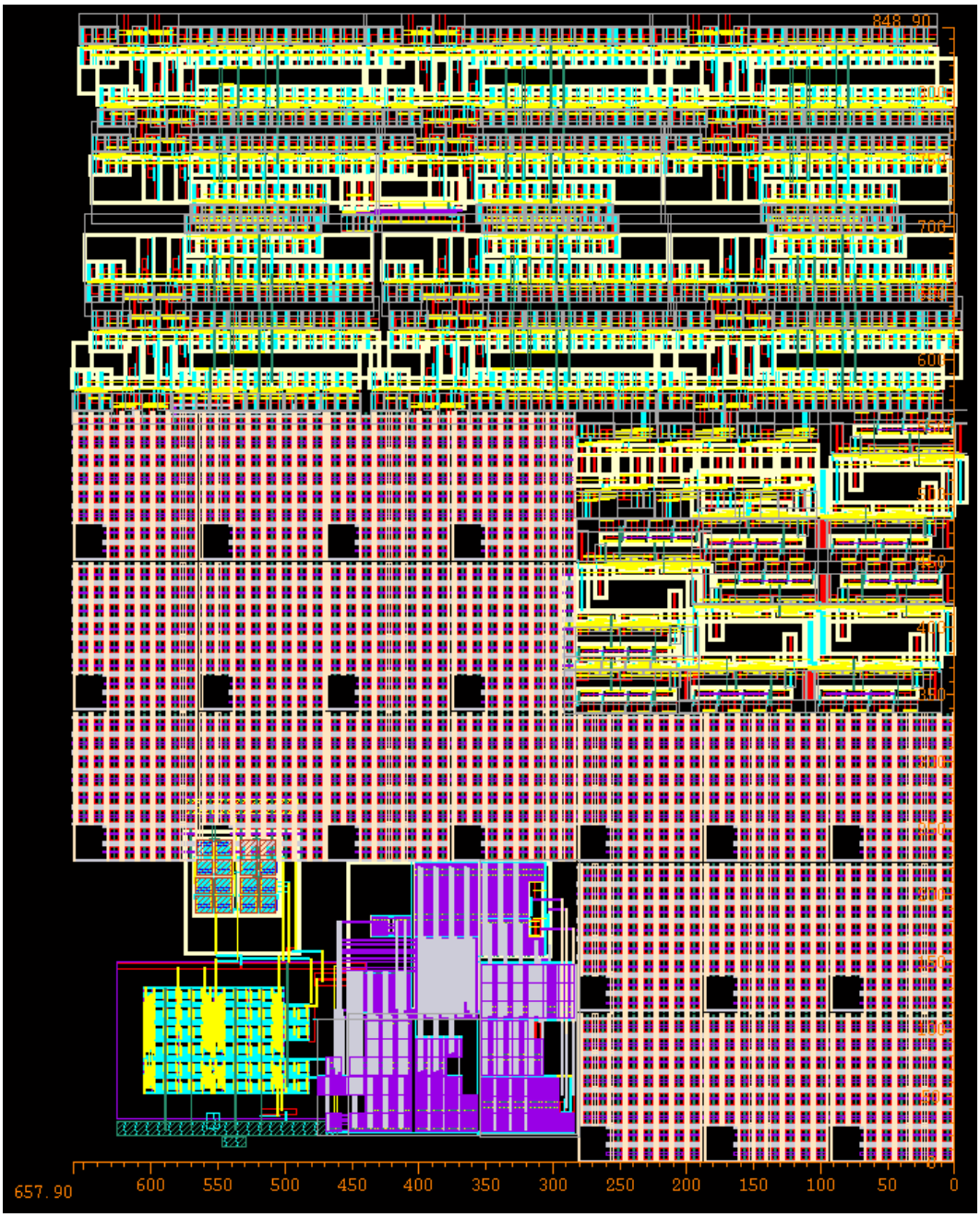

Figure 8-8: Top level layout of 14b 3.33MS/s triple channel cyclic ADC with triple sampling configurable to 14b 10MS/s single channel ADC

8.4 Conclusion

Chapter 8 presented the details of the physical layout of the Cyclic ADC and the care that has to be taken when implementing the ADC in terms of matching and floorplanning. The total area for the cyclic ADC including the capacitors is 650um x 850um = 0.5525mm2, which is small for a triple channel ADC, each working at 14b precision and 3.33MS/s or a single channel ADC working at 14b precision and 10MS/s. Chapter 9 presents the detailed results of the ADC and concludes the thesis.

Chapter 9

RESULTS AND CONCLUSION

9.1 Introduction

The triple channel Cyclic ADC, each working at 14b accuracy and 3.33MS/s was implemented in UMC 180nm. This chapter discusses the simulation results of the cyclic ADC.

9.2 Performance of the Split-CLS Architecture

This section discusses the performance of the split-CLS architecture which was used as the backbone for the triple sampling technique. The final architecture that was chosen for the estimation amplifier sided on accuracy rather than ease of design and a gain boosted folded cascode amplifier with low output swing was used. The fine settling amplifier was implemented as a simple telescopic cascode amplifier.

A worst case sine wave input was provided to the amplifier with peak signal swing of 1.5V (3V differential swing) and at the input frequency of 1MHz. The input frequency was chosen such that the sampling frequency does not become a multiple of the input frequency to avoid spectral tones while maintaining it as close to 1MHz as possible.

The output was set up to provide a gain of 2 and the output was recorded and ported to MatLAB. Post-simulation analysis was done using MatLAB. FFT was

performed on the output to check the linearity and the signal to noise and distortion ratio (SNDR) of the output. Since the dynamic range was high, a Blackmann-Harris window was used. Fig 9-1 shows the frequency spectrum of the output sine wave. The output has a dynamic range, SFDR and THD3 of 103 dB, a very respectable performance. The total SNDR was 86dB.

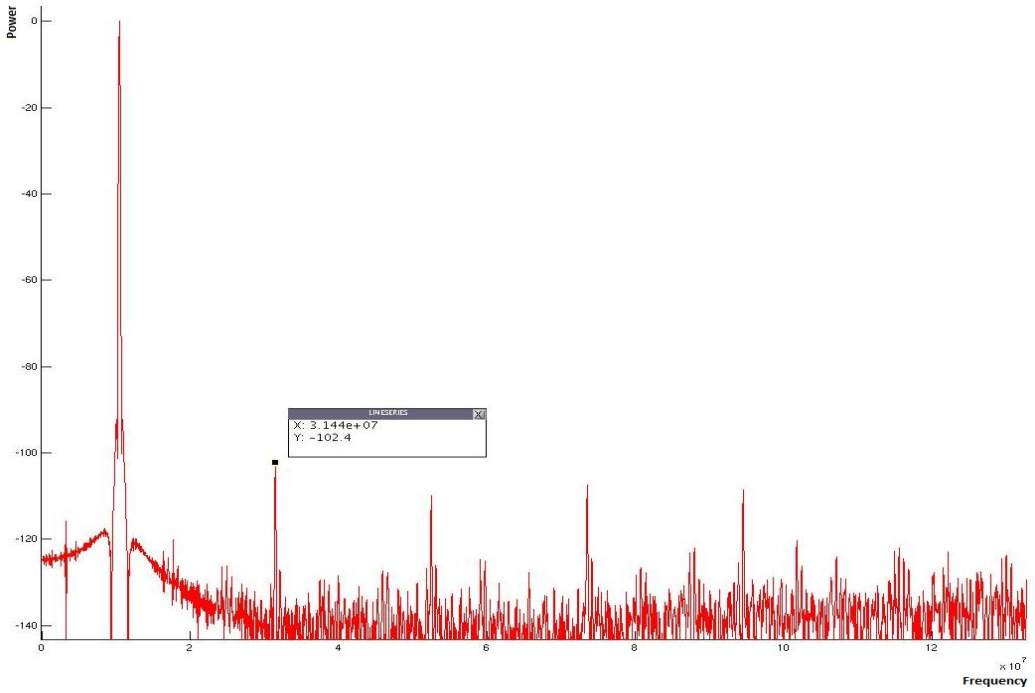

Figure 9-1: Spectrum of output from the split-CLS stage with input at 1.143MHz

Fig 9-2 shows the time domain output from the gain stage and ported to MatLAB. Fig 9-2 shows the sine wave from each path as a different colored sample, hence when the sine wave is sampled by the three channels, two more samples are added in between each sample to increase the oversampling ratio by a factor of three. The output in this case is shown in Fig 9-2. The SNR also correspondingly increases by 4.5dB which reflects an increase of oversampling ratio by a factor of 3.

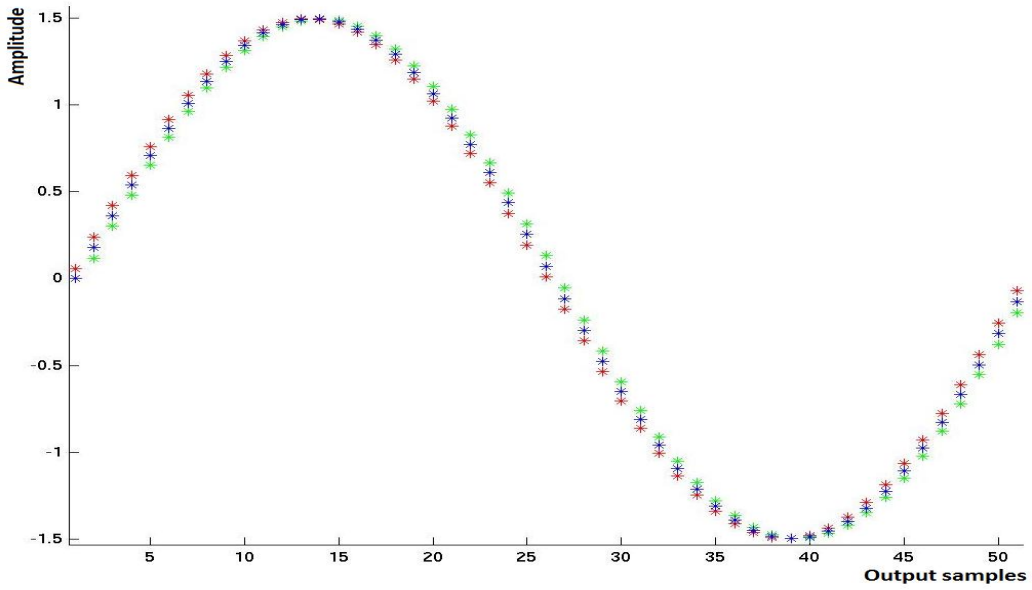

Figure 9-2: Reconstructed output from triple sampling a single sine wave

9.3 Performance of the ADC

After the gain stage was configured as an ADC using RSD and digital recombination by the serial to parallel converter and full adder stages and by recycling the output back to the input, the settling of the entire stage is analyzed. Given the 3V fully differential input swing and a 14b resolution, the LSB size is 187.5uV, the first stage resolves 1.5 bits and hence the second stage requires an input of 13b accuracy. If the input to the second stage is budgeted to be LSB/2, then the voltage accuracy level it requires is 187.5uV as well. Hence the first stage settling of the cyclic ADC needs to be accurate to within 187.5uV of the actual input. Fig 9-3 shows the output of the first cycle and the output is accurate to the final answer within 187.5uV as can be seen. Fig 9-4 shows the consecutive first three outputs each accurate to its own LSB requirement.

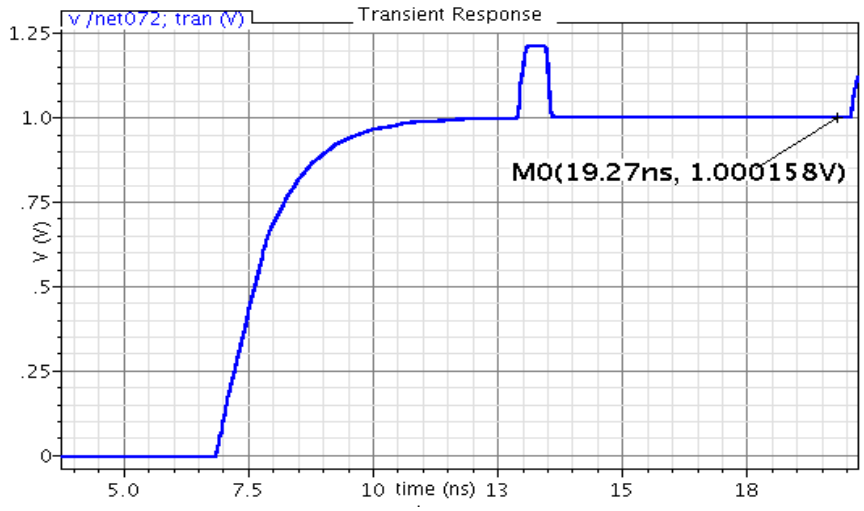

Figure 9-3: Settling accuracy of the ADC for the first cycle

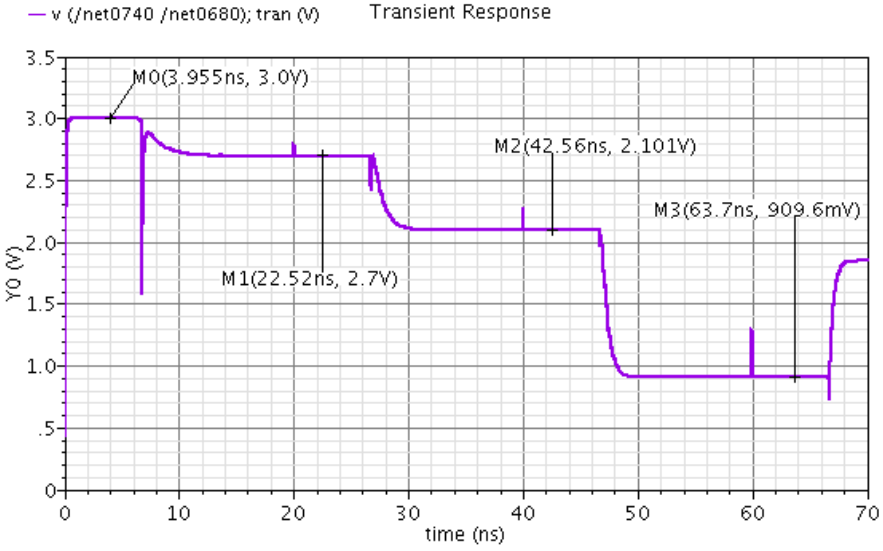

Figure 9-4: Settling accuracy of the ADC for the first 3 cycles

Fig 9-3 shows the settling accuracy of the ADC's first cycle. This is the most critical settling as this settling is the one that determines the overall accuracy of the ADC and the rest of the stage's errors are reduced by the gain of the previous stages.

A sine wave of maximum amplitude of 1.5V single ended and input frequency of 1.919MHz was given as an input to the ADC and a long transient was run. The digital output was again converted to analog by Verilog code and ported to MatLAB. This was then analyzed using FFT and Fig 9-shows the output spectrum.

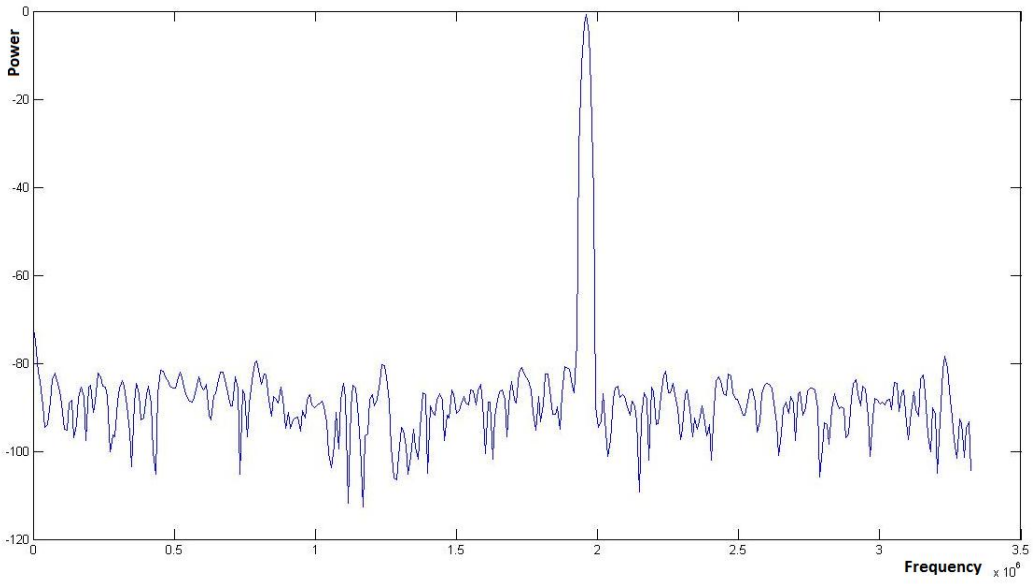

Figure 9-5: Spectrum from input of single sine wave at 1.919MHz and 1.5V input

The SNDR was observed to be 73.6 dB per channel. This reflects an ENOB of 11.93b per channel and 12.68b for the ADC. The total power consumption was split as 2.7mA of current from the estimation amplifier, 800uA of current for the fine settling amplifier and 500uA of current in the biasing from 3.3V supplies, resulting in 13.2mW of power consumption and a figure of merit of 405 fJ/conversion.

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