Modeling & Analysis of a Closed Loop Class D Audio Amplifier

For PSR Improvement

By

Bijeta Chakraborty

A Thesis Presented in Partial Fulfillment
of the Requirements for the Degree
Master of Science

Approved October 2012 by the
Graduate Supervisory Committee:

Bertan Bakkaloglu, Chair
Douglas Garrity
Sule Ozev

ARIZONA STATE UNIVERSITY

December, 2012

ABSTRACT

Class D Amplifiers are widely used in portable systems such as mobile phones to achieve high efficiency. The demands of portable electronics for low power consumption to extend battery life and reduce heat dissipation mandate efficient, high-performance audio amplifiers. The high efficiency of Class D amplifiers (CDAs) makes them particularly attractive for portable applications. The Digital class D amplifier is an interesting solution to increase the efficiency of embedded systems. However, this solution is not good enough in terms of PWM stage linearity and power supply rejection. An efficient control is needed to correct the error sources in order to get a high fidelity sound quality in the whole audio range of frequencies. A fundamental analysis on various error sources due to non idealities in the power stage have been discussed here with key focus on Power supply perturbations driving the Power stage of a Class D Audio Amplifier. Two types of closed loop Digital Class D architecture for PSRR improvement have been proposed and modeled. Double sided uniform sampling modulation has been used. One of the architecture uses feedback around the power stage and the second architecture uses feedback into digital domain. Simulation & experimental results confirm that the closed loop PSRR & PS-IMD improve by around 30-40 dB and 25 dB respectively.

ACKNOWLEDGMENTS

It has been an honour to be able to complete my Master of Science Degree from Arizona State University. First of all I would like to express my deep and sincere gratitude to Prof.Bertan Bakkaloglu. This research project would not have been possible without the support and constant guidance of Prof.Bertan Bakkaloglu. He has been abundantly helpful and offered timely support and guidance to me throughout. He has always shown confidence and trust in me which have kept me motivated.

I would also like to wholeheartedly thank Prof. Sule Ozev and Prof. Douglas Garrity for being a part of my committee member in spite of their busy schedule.

I wish to express love and gratitude to my beloved family members and few close friends; for their understanding & endless love & helping me throughout all the odd times of my life so far.

TABLE OF CONTENTS

Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

Figure Page

Chapter 1

INTRODUCTION

1.1 WHAT IS SOUND?

Sounds are pressure waves of air. If there wasn't any air, we wouldn't be able to hear sounds. There's no sound in space.

We hear sounds because our ears are sensitive to these pressure waves. Perhaps the easiest type of sound wave to understand is a short, sudden event like a clap. When you clap your hands, the air that was between your hands is pushed aside. This increases the air pressure in the space near your hands, because more air molecules are temporarily compressed into less space. The high pressure pushes the air molecules outwards in all directions at the speed of sound, which is about 340 meters per second. When the pressure wave reaches your ear, it pushes on your eardrum slightly, causing you to hear the clap.

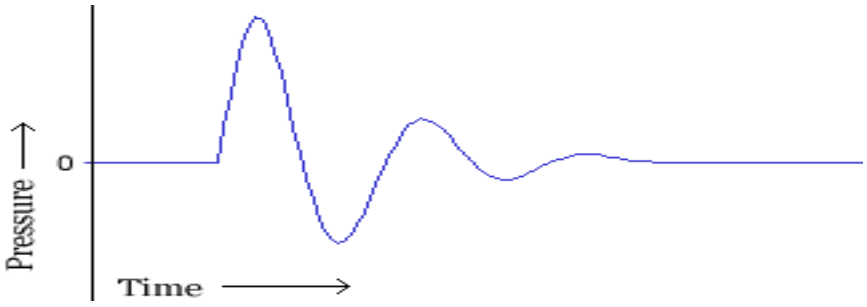


Figure 1: Sound Wave

The other common type of sound wave is a periodic wave. When you ring a bell, after the initial strike (which is a little like a hand clap), the sound comes from the vibration of the bell. While the bell is still ringing, it vibrates at a particular

frequency, depending on the size and shape of the bell, and this causes the nearby air to vibrate with the same frequency. This causes pressure waves of air to travel outwards from the bell, again at the speed of sound. Pressure waves from continuous vibration look more like this:

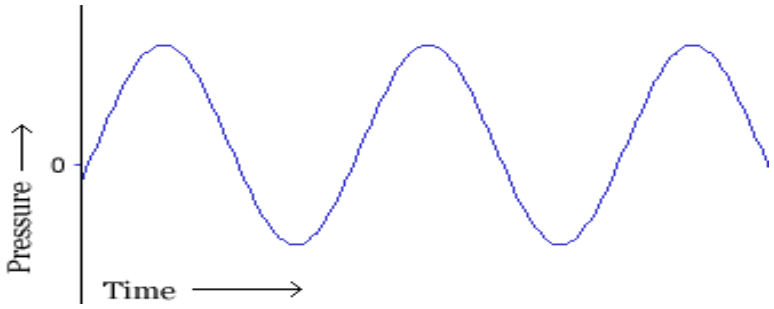


Figure 2: Periodic Sound Wave

RECORDING OF SOUND: ANALOG vs. DIGITAL

ANALOG RECORDING

An analog recording is one where a property or characteristic of a physical recording medium is made to vary in a manner analogous to the variations in air pressure of the original sound. Generally, the air pressure variations are first converted (by a transducer such as a microphone) into an electrical analog signal in which either the instantaneous voltage or current is directly proportional to the instantaneous air pressure (or is a function of the pressure). A microphone consists of a small membrane that is free to vibrate, along with a mechanism that translates movements of the membrane into electrical signals. (The exact electrical mechanism varies depending on the type of microphone.) So acoustical waves are translated into electrical waves by the microphone.

Typically, higher pressure corresponds to higher voltage, and vice versa. A tape recorder translates the waveform yet again - this time from an electrical signal on a wire, to a magnetic signal on a tape. When you play a tape, the process gets performed in reverse, with the magnetic signal transforming into an electrical signal, and the electrical signal causing a speaker to vibrate, usually using an electromagnet.

DIGITAL RECORDING

A digital recording is produced by converting the physical properties of the original sound into a sequence of numbers, which can then be stored and read back for reproduction. Normally, the sound is transduced (as by a microphone) to an analog signal in the same way as for analog recording, and then the analog signal is digitized , or converted to a digital signal, through an analog-to-digital converter and then recorded onto a digital storage medium such as a compact disc or hard disk .

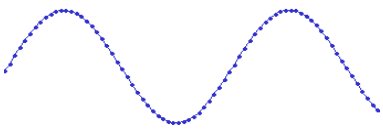


Figure 3: Sampled Audio

Each dot in the figure above represents one audio *sample*. There are two factors that determine the quality of a digital recording:

- Sample rate: The rate at which the samples are captured or played back, measured in Hertz (Hz), or samples per second.

An audio CD has a sample rate of 44,100 Hz, often written as 44 KHz for short. This is also the default sample rate that Audacity uses, because audio CDs are so prevalent.

- Sample format or sample size: Essentially this is the number of digits in the digital representation of each sample. Think of the sample rate as the horizontal precision of the digital waveform, and the sample format as the vertical precision. An audio CD has a precision of 16 bits, which corresponds to about 5 decimal digits.

HISTORY OF 44.1 KHz SAMPLING RATE AS STANDARD

Ref: From John Watkinson, *The Art of Digital Audio*, 2nd edition, pg. 104:

In the early days of digital audio research, the necessary bandwidth of about 1 Mbps per audio channel was difficult to store. Disk drives had the bandwidth but not the capacity for long recording time, so attention turned to video recorders. These were adapted to store audio samples by creating a pseudo-video waveform which would convey binary as black and white levels. The sampling rate of such a system is constrained to relate simply to the field rate and field structure of the television standard used, so that an integer number of samples can be stored on each usable TV line in the field. Such a recording can be made on a monochrome recorder, and these recording are made in two standards,

- 525 lines at 60 Hz
- 625 lines at 50 Hz.

Thus it is possible to find a frequency which is a common multiple of the two and is also suitable for use as a sampling rate.

The allowable sampling rates in a pseudo-video system can be deduced by multiplying the field rate by the number of active lines in a field (blanking lines cannot be used) and again by the number of samples in a line. By careful choice of parameters it is possible to use either 525/60 or 625/50 video with a sampling rate of 44.1 KHz.

In 60 Hz video, there are 35 blanked lines, leaving 490 lines per frame or 245 lines per field .Sampling Rate Given By: 60 X 245 X 3 = 44.1 KHz .In 50 Hz video, there are 37 lines of blanking, leaving 588 active lines per frame, or 294 per field, so the same sampling rate is given by Sampling Rate given By: 50 X 294 X 3 = 44.1 KHz. Note: The sampling rate of 44.1 KHz came to be that of the Compact Disc. Even though CD has no video circuitry, the equipment used to make CD masters is video based and determines the sampling rate.

1.2 BASICS OF CLASS D AUDIO AMPLIFICATION

A Class D delivers a set amount of power into the load for a given period. The Class-D creates a PWM signal that makes the output voltage switch between the supply rails, yielding very little voltage drop across the output transistors

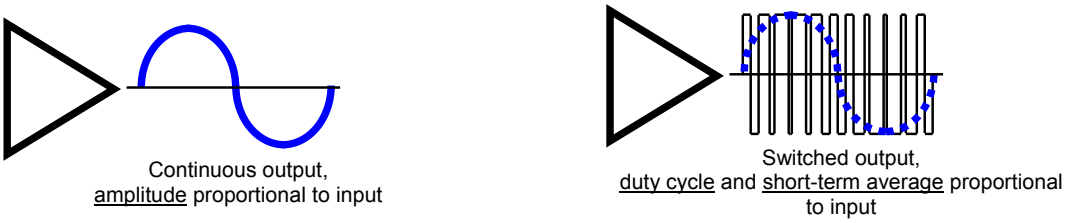


Figure 4: CLASS AB vs. CLASS D

Amplifier wastes power because they require high voltage across output devices with high load current. Class-AB amplifiers, traditional designs, waste power because they require high voltage across output devices with high load current. Class-D amplifiers operate with output devices switched fully off or fully on, so output devices support either low voltage or low current. Power dissipation is reduced significantly and efficiency is increase significantly in Class-D amplifiers.

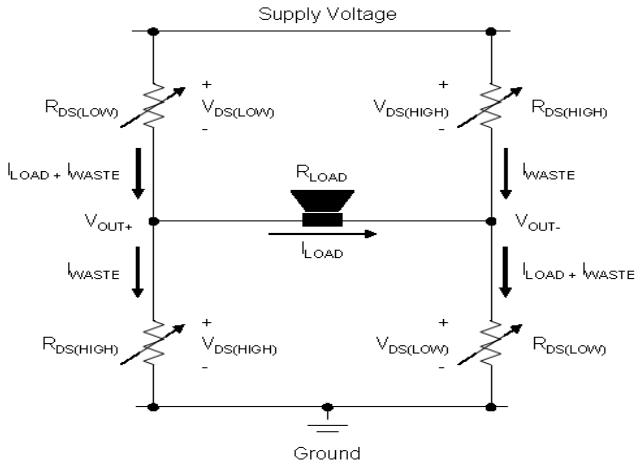


Figure 5: Simplified H-bridge for a Class-AB amplifier

The output MOSFETs are illustrated with variable resistors, whose resistance changes as a function of amplifier output voltage. These MOSFETs vary their drain-source resistance as the output voltage changes. The current flowing from the supply through the load causes a voltage drop across all the MOSFETs. It is these currents multiplied by the voltage drop across the MOSFETs that create the large power dissipation in the amplifier. This power dissipation in these MOSFETs is the reason why Class-AB amplifiers are so inefficient when compared to Class-D amplifiers. So, why do Class-D amplifiers dissipate less power?.

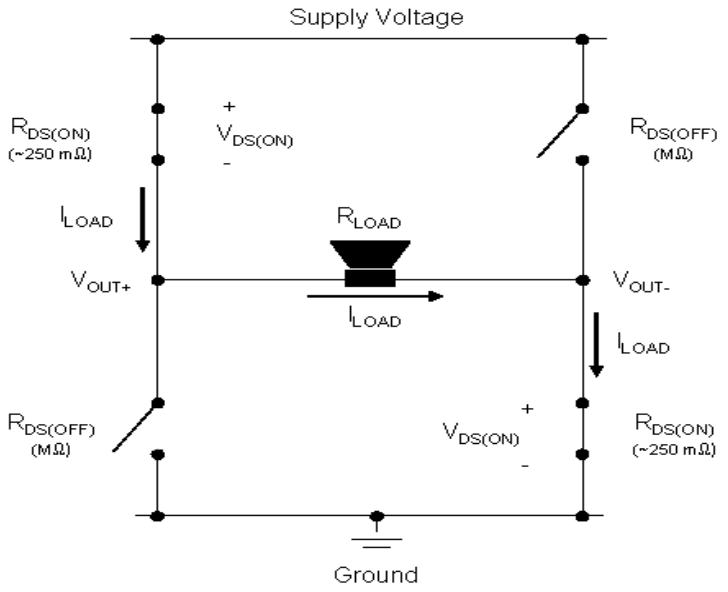


Figure 6: Simplified H-bridge for a Class-D amplifier

The optimal MOSFETs in the H-bridge for a class-D amplifier would have zero rDS(on) (drain-to-source resistance) when “ON” and infinite drain-to-source resistance when “OFF” rDS(off). In this case, the Class-D amplifier would supply an equal amount of power from the supply to the load. Due to the fact the all MOSFETs have some rDS(on) and a finite rDS(off) there is some power loss due to rDS(on) and rDS(off) of the MOSFETs. This is illustrated in Figure 3, where the MOSFETs are simplified by switches either that are either “ON” or “OFF”. In Figure 3, as the current flows from the supply through the first MOSFETs that is “ON”, through the load and finally through the last MOSFETs that is “ON”, there is a slight voltage drop across the MOSFETs. A voltage divider is formed by rDS (on), rDS (off) and the output load or speaker, RL. The rDS (ON) of the MOSFETs is very small, so that there is virtually no voltage drop across them. Since the value of rDS (off) for the MOSFETs that are “OFF” is large, there will be virtually no current flowing through them.

As a result, these amplifiers are very efficient since only a small amount of power is dissipated by the MOSFETs compared to Class-AB amplifiers.

Additionally, these output MOSFETs are typically switching at around 250 kHz. The reason for this frequency is to reduce the total harmonic distortion (THD) performance of the amplifier. If the amplifier was set to switch at a lower frequency, the resulting waveform would cause worse THD performance. If the switching frequency was increased, the amplifier would become less efficient due to increased loss during the switching periods. The 250 kHz switching rate is a good comprise between THD and efficiency performance.

Let us consider a sine output

- Vout = Vo sin(ωt)
- I out = Vout / R load
- Psupp. = Vps * Iout average
- Psupp. = 2 Vps * Vo /π Rload
- Pout = Vo ^ 2/2 Rload
- Efficiency = π Vo/4Vps = 78.5% maximum
- Net power in amp:
    - Pamp. = Psupp. – Pout

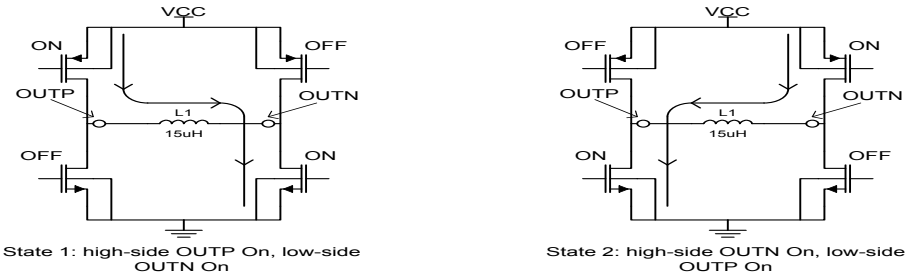


Figure 7: H – Bridge topology

In Class-D amplifiers most power losses occur in the output devices, typically FETs with low on resistances. Class-D amplifier efficiency depends only on a resistor ratio, so it is essentially constant.

$$\text{Efficiency} = \frac{\text{Pout}}{\text{Pout} + \text{Pamp}} = \frac{\text{Rload}}{\text{Rload} + \text{Rfets}}.$$

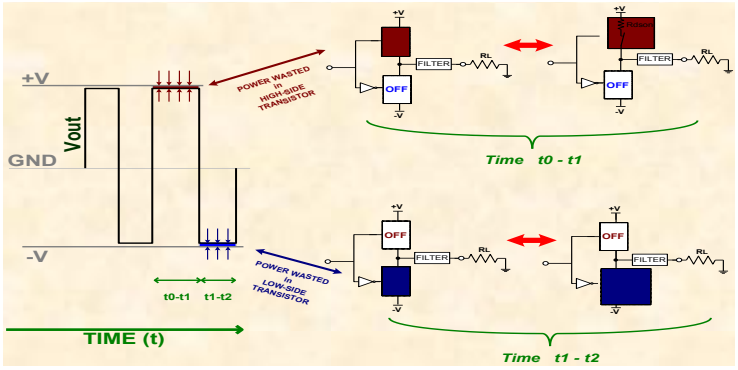


Figure 8: Power Dissipation –CLASS D

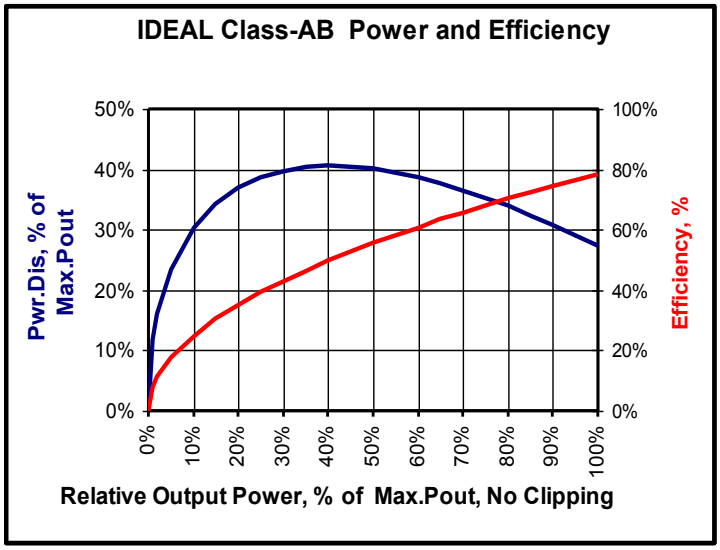


Figure 9: Efficiency comparison CLASS AB vs. CLASS D

1.2.1 ANALOG vs. DIGITAL CLASS D

There are two approaches to implement a class D amplifier modulator, namely analog and digital. Analog modulators use analog building blocks, such as op-amps and comparators to realize the PWM modulation. Integrated analog modulators require custom layout, and need to be redesigned for different technologies. Some of them are designed to include a feedback network in order to improve the performance. The feedback network implementation is straight forward because both the input and the output are analog signals. For consumer electronics applications, audio data is typically stored, processed, and transmitted in digital form. To use an analog class D amplifier, a DAC is required to convert the audio from digital to analog domain. The overall system performance, of course, will depend on the quality of DAC. An alternative approach is to implement the modulator using digital signal processing. The digital modulator is able to accept digital inputs from storage media and generate modulation signal directly. Adding a feedback network, in this case, is difficult because the input and output are across different signal domains. As a result, due to the lack of feedback networks, digital class D amplifiers operating in open loop typically have inferior performance, comparing to analog class D amplifiers in closed loop. On the other hand, digital class D amplifiers are more robust to process variations, more economical, easier to migrate between different technologies, more immune to noise and compatible with digital input directly. Some of the major performance indicators of a class D amplifier include efficiency, audio quality and Power Supply Rejection Ratio (PSRR).

The focus of this work is to improve the audio quality and PSRR for digital class D amplifiers.

Description of how a Digital CLASS D works:

The concept of Digital Audio in the field of audio rises a question – is it possible to convert the digital encoded signals (PCM) directly to a pulse modulated signal for subsequent power amplification? The motivation is of course the topological simplification in both the digital to analog conversion stage and the subsequent power amplification stage. Intuitively, it is advantageous to keep the signal digital "as long as possible" with the accuracy and rigidity that generally follows, but the However, fundamental problems have persisted within digital PMAs although the field has attracted significant attention within the last decade. Basically, the digital pulse modulation technique is used for the digital PMA. This involves also a fair amount of knowledge in the field of oversampling converters because the concept of noise shaping applies well to the audio amplifiers (digital) as the noise gets shaped and thrown out of the signal band towards the high frequency band where it is not audible to human ear.

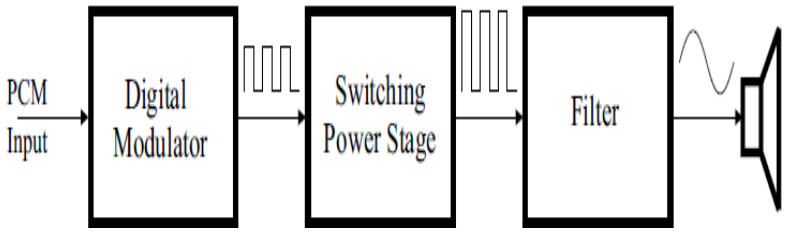


Figure 10: Digital Pulse Modulation topology

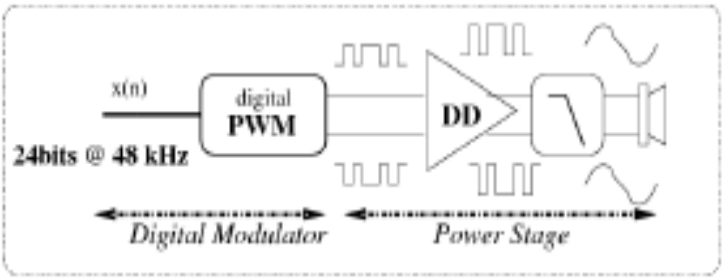


Figure 11: Direct Digital Pulse Modulation topology

Let say we have 24 bit Audio input digital word x (n) which is sampled at Fs = 48 KHz, this needs to be modulated in to a PWM in order to create a bit stream waveform. For this, the reference saw tooth signal of PWM have to sweep all the levels of *x(n)* during the sample time of one period.

Calculating the minimum frequency of the digital saw tooth waveform, which is required to sweep correctly all the levels of *x (n),* can be expressed as:

$$Fpwm = 2^n \times Fsamp. = 2^{24} \times 48 \times 1000 = 805GHz$$

Of course this is not a realizable frequency in a CMOS process. There comes the concept of noise shaping and use of Sigma Delta modulation before PWM so as to decrease the saw tooth frequency to a reasonable range. Indeed, in addition to the shaping of the noise quantification of x (n), ΣΔ modulation reduces the bit-depth of the signal. Let say if we have a 6 bit modulator with an OSR of 16 then the corresponding frequency of the digital saw tooth waveform required would be:

$$Fpwm = 2^n \times Fsamp. = 2^5 \times 48 \times 1000 \times 16 = 38.4MHz$$

The principles of ΣΔ modulation are the over sampling of the input signal and the shaping of quantification error out of the audio band.

1.3 MOTIVATION FOR CLOSED LOOP DIGITAL CLASS D

The performance of digital PWM open loop amplifiers is almost entirely limited by the non-idealities of the power stage and power supply. The switching power stage in a digital amplifier introduces nonlinearity and noise into the switched power output signal. Sources of nonlinearity include the nonlinear 'on' resistance of the switches, error during dead time or break-before-make (BBM) of the switching stage, and finite rise and fall time of the switching stage output. These nonlinearities not only degrade the total harmonic distortion (THD)performance but also reduce the SNR by mixing the out-of band quantization noise of the digital PWM driving signal into the audio pass band. The power supply can be an additional source of noise and nonlinearity. Standard PWM open loop power stages provide no power supply rejection. Loading of the digital amplifier, other loads connected to the same power supply, and power supply ripple can produce noise at the power supply to the digital amplifier. The output of a digital amplifier is a direct multiplication of the power supply and the digital PWM signal which can be seen as PS-IMD and PSRR in the audible band.

1.4 REPORT ORGANIZATION

In the following chapters, system level design constraints and implementation of a closed loop Class D Audio amplifier along with two types of feedback have been discussed. Chapter 2 talks about the various error sources in CLASS d amplifier power Stage, Chapter 3 talks about the system design of Class D amplifier and the various simulink models developed for that. Chapter 4 presents the power stage model developed for the CLASS D. Chapter 5 throws light on the system realisation and system design specs for the whole system

Chapter 2

DIGITAL CLASS D AMPLIFICATION

The motivation for Digital class D comes from the increasing trend and advancement in the field of DSP. Most of the times these days audio is recorded and stored digitally on CDs, DVDs etc. Digitally controlled class D are audio amplifiers with a digitally generated control that switches a power stage. No error control is present. Those that do have an error control can be shown to be topologically equivalent to an analog-controlled class D with a DAC in front. The continuing expansion of digital techniques in the field of audio rises a question – Is it possible to convert the digital encoded signals (PCM) directly to a pulse modulated signal for subsequent power amplification?. The clear answer is no. As explained in the report earlier in chapter 1, the need of a extremely high carrier frequency supports the very fact that the digital data should be crunched down before it can be used to generate a decent PWM which can drive the power stage. Though, it is advantageous to keep the signal digital “as long as possible” with the accuracy and rigidity that generally follows. However, fundamental problems have persisted within digital PMAs in terms of non linearity’s of the PWM generator stage and the non idealities of the power stage. Below listed are the different and important blocks required in building and implementing a Digital Class D amplifier.

- Interpolator & Noise Shaper
- Digital PWM Modulator
- Switching Power Stage
- Demodulation Filter

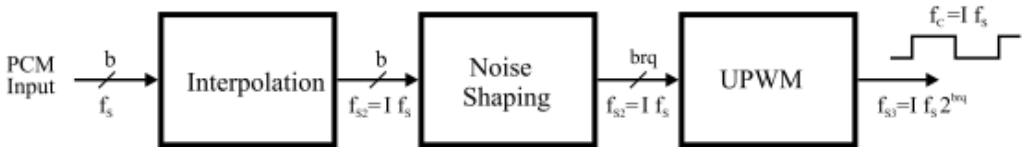


Figure 12: Practical Digital Pulse Modulation topology

2.1 INTERPOLATION AND NOISE SHAPING

The interpolation improves the linearity of the conversion process by providing a considerably carrier frequency to bandwidth ratio. The effective oversampling of the signal opens for effective noise shaping to reduce the pulse width resolution while maintaining base band performance. The increase in carrier frequency by interpolation will lower the efficiency. On the other hand, demodulation will become simpler.

The interpolation factor is a compromise between modulator linearity, dynamic range and factors relating to the power conversion as efficiency and power stage linearity. Since errors in the power stage are introduced on each switching action, the carrier frequency should be minimized.

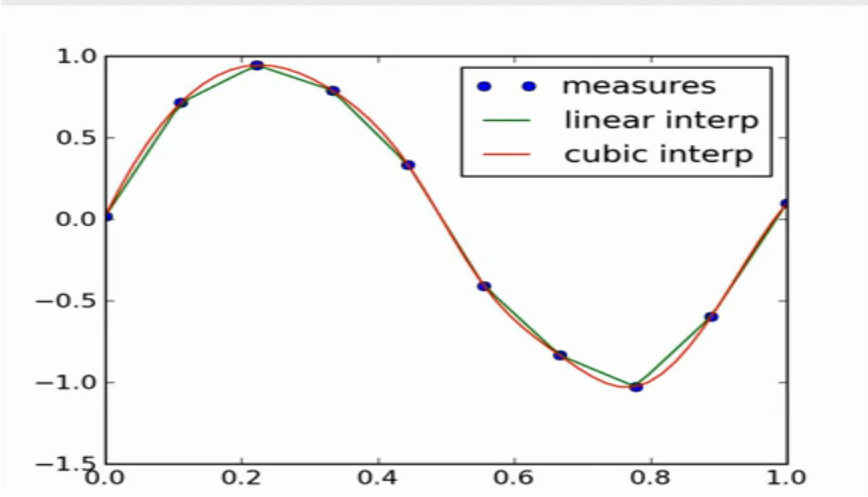


Figure 13: Interpolation

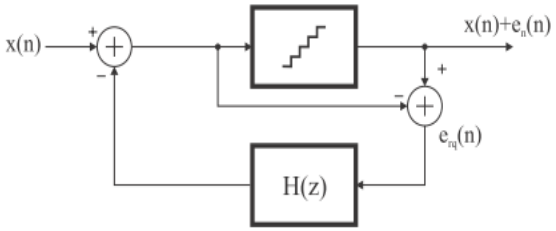
In terms of hardware an Interpolator can be implemented a series of Half Band IIR filters. Basically an interpolator is oversampling in time domain as it adds zero to the sampled PCM signal. Since we know that sampling will basically produce the replicas periodically at the sampling frequency, using an interpolator will increase the number of samples and hence the replicas of the frequencies will now be further apart.

One shortcoming of interpolator is that with the increase in the interpolation the low pass filter design to extract the original signal becomes stringent.

Basically, interpolator would be characterized by its pass band ripple & stop band ripple and the desired pass band cut off angular frequency.

NOISE SHAPING

The basic function of a noise shaper in digital pulse modulation system is to reduce the bit depth and maintain the Dynamic range within the baseband, while quantizing the signal to a lower resolution. Reduction in the PCM bits is needed as the system clock required by uniform pulse width modulation grows exponentially with the number of bits in the output signal.



$$\mathrm{STF}(z) = 1$$

$$\mathrm{NTF}(z) = \frac{E_n(z)}{E_{rq}(z)} = 1 - H(z)$$

Figure 14: 1st Order Noise Shaper

Noise shaping is extraordinary useful in this application, since the critical requirement for time resolution can be reduced by orders of magnitude by remarkably simple means. The signal transfer function remains unaffected whereas the noise gets reduced and pushed out of the audio band. Show below is an example plot of designed CIFB based modulator for audio bandwidth of 22 KHz.

ΔΣ-converters have won a strong place in conversion between digital and analog domains. This is due to the nature of ΔΣ modulators which trades precision in levels of signal amplitude for timing precision. This trade is highly desirable as it is far easier to obtain precise timing in the VLSI technologies used today. The possibility for a 1 bit output of the ΔΣ modulator makes it very interesting for controlling the power switches in a class D amplifier as well, and thus create a power D/A converter. ΔΣ derived technologies are used in most digital input class D amplifiers.

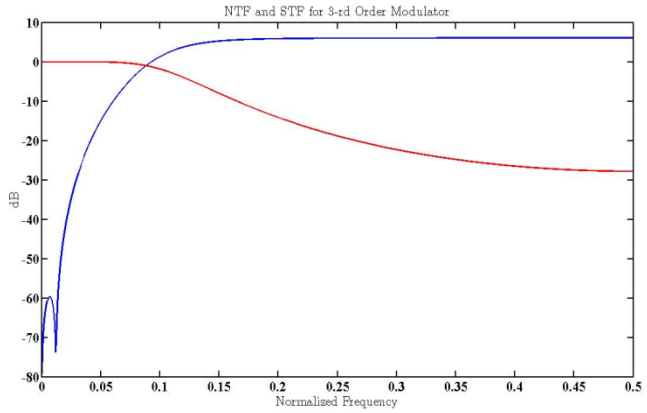


Figure 15: STF &NTF of a 3rd order CIFB modulator

2.2 DIGITAL PULSE MODULATION TECHNIQUES

Digital Pulse Width Modulation (DPWM) is one of the most important parts in digital control systems which control the power switch of the power converters. Modulation technique plays a vital role in causing control delays. There are several implementation schemes of digital pulse width modulation such as counter based DPWM, delay line based DPWM, and hybrid based DPWM.

The practical conversion of a digital PCM signal to a uniformly sampled pulse width modulated signal is remarkable simple. Figure below shows an example system that converts the b bit represented input to a uniformly sampled PWM signal at the carrier rate fc equal to the sample rate fs of the PCM signal. The digital modulator uses a high frequency b bit counter to define the timing edges. It is essential, that the conversion from PCM to UPWM is realized without loss of information. The requirement for counting speed is a fundamental limitation in digital PWM systems. Since audio systems operate with 16-24 bits and sampling frequencies of at least 44.1 KHz, the necessary counter speed in this direct implementation is orders of magnitude higher than what can be realized in hardware .A more fundamental problem however is the nonlinearity within PCM-PWM conversion, where exact mapping of PCM to PWM cannot be trusted.

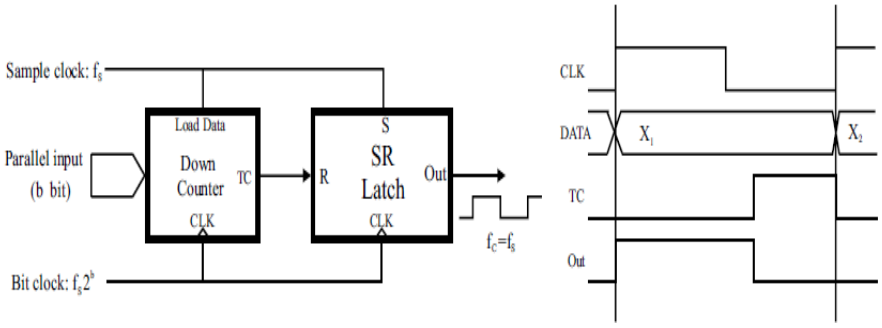


Figure 16: Direct PCM to PWM

Different sampling techniques are used in order to achieve the PWM output. Pulse width modulation is categorized in two major classes by the sampling method: natural sampled PWM (NPWM) and uniform sampled PWM (UPWM).Though hybrid methods also exist. Besides the sampling method it is also characterized by the edge modulation and by the class (AD & BD). Currently in this report only uniform sampling method has been discussed however there are better sampling techniques which can greatly reduce the harmonic distortions. The essential parameters for the comparison of PWM and their analysis is as mentioned below.

Maximal frequency ratio

The frequency ratio or normalized frequency fr is defined as the ratio between signal angular frequency and carrier angular frequency ω_c:

$$fr = \omega r = \frac{\omega}{\omega c}$$

The Nyquist sampling criteria puts a restriction on the allowable frequency ratio:

$$fr\max = \frac{1}{2}$$

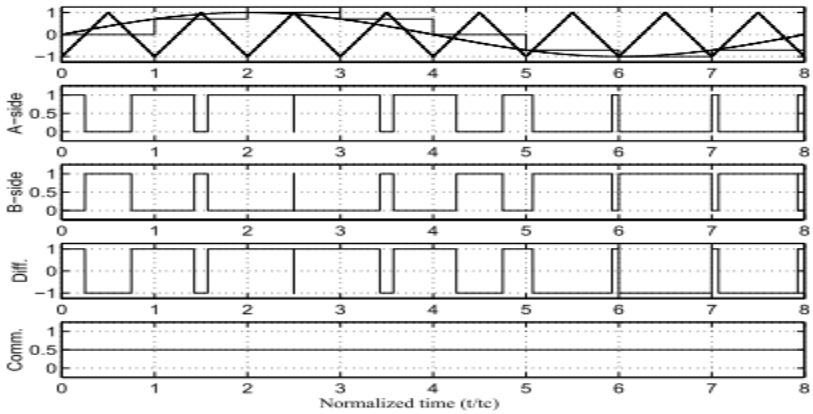


Figure 17: Uniform AD Double Sided Modulation

Another constraining factor for the maximal frequency ration is observed by considering the slew-rates of the carrier and modulating reference signal (assuming unity amplitudes on carrier and signal) for double sided modulation:

$$SRcarrier \geq SRreference$$

$$fr, \max = 2/\pi$$

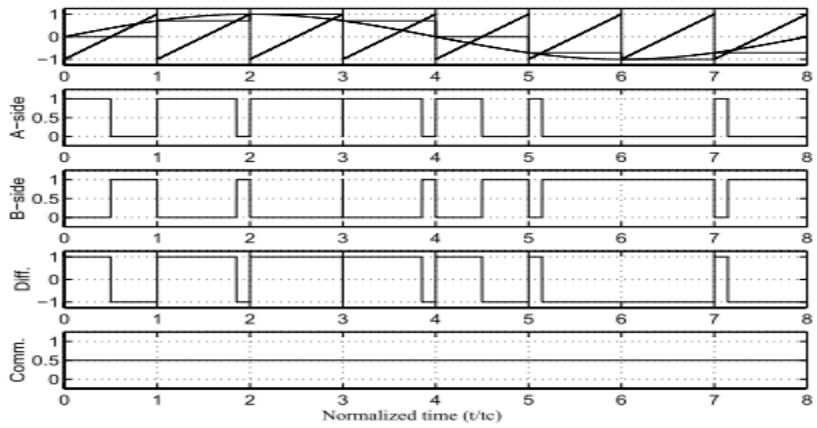


Figure 18: Uniform AD single Sided Modulation

Method	nth Harmonic of Signal	mth Harmonic of Carrier	IM component (mx±my)
UADD	$\frac{Jn(n\Pi(M/2)q)}{n\Pi q}\sin((q+1)n\Pi/2)$	$\frac{Jo(m\Pi M/2)}{m\Pi}\cos(m\Pi/2)$	$\frac{J((nq+m)\Pi M/2)}{(nq+m)\Pi}\sin((m+n(q+1))\Pi/2)$
UADS	$\frac{Jn(n\Pi Mq)}{n\Pi q}$	$\frac{(1-Jo(m\Pi M))}{m\Pi}\cos(m\Pi)$	$\frac{J((nq+m)\Pi M)}{(nq+m)\Pi}$

Table 1: Harmonic components UADD vs. UADS

The spectral analysis for the Uniform sampling based on DFS reveals that:

The intermodulation components are very pronounced at mx±ny and depend heavily on the modulation index M. This can be seen as ‘skirts’ around harmonics of the carrier, a general characteristic for pulse width modulation.

The idle spectrum has significant harmonic components around odd harmonics of the carrier. This is to expect since the idle spectrum is a pure square wave.

Only the components related to the even harmonics of the carrier reduce with M and are totally eliminated at idle.

There are different ways of implementing DPWM systems like using counters, delay line and hybrid. The counter can be a an up\down counter. In the first half of the switching cycle the counter acts as either up or down and in the second half of the cycle it acts either down or up, or vice versa. When the counter value is greater than duty cycle, then the DPWM pulse is set to high. Half of the switching cycle act as leading edge and other half of the switching cycle act as trailing edge.

2.3 POWER STAGE

A power stage is extremely important for driving high power speakers and load. This stage is one of the most important reasons for non idealities seen at the output of the CLASS D audio amplifier. As explained above Class D amplifiers work by generating a square wave of which the low-frequency portion of the spectrum is essentially the wanted output signal, and of which the high-frequency portion serves no purpose other than to make the wave-form binary so it can be amplified by switching the power devices.

The structure of a class D power stage is essentially identical to that of a synchronously rectified buck converter, a type of non-isolated switched-mode power supply. A class D amplifier delivers a constantly changing voltage into a fixed load, where current and voltage can independently change sign (four-quadrant operation). A switching amplifier must not be confused with any amplifier that uses an SMPS. A switching amplifier may use any type of power supply but the amplification process itself operates by switching.

An H Bridge Power Stage for a class D is as shown below. In real implementation, it is required to have a driver stage to provide high current and rail capabilities.

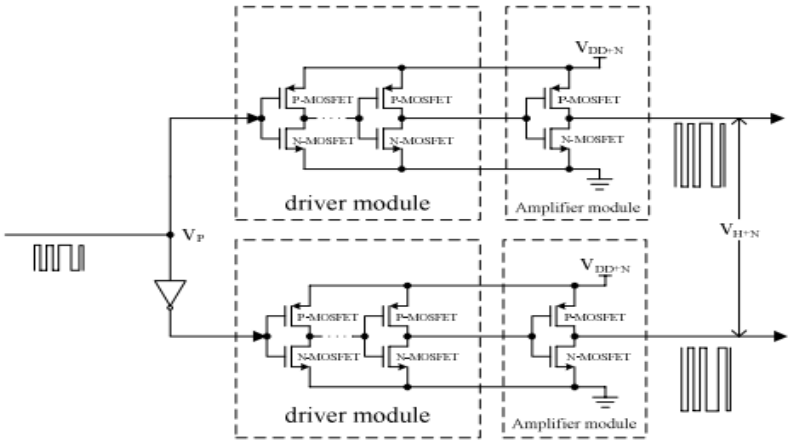


Figure 19: H Bridge Power Stage

Timing errors are introduced by the gate driver:

- Due to finite Rise/fall time, and finite turn ON/OFF time of the power transistors in the output stage.
- In addition, dead time is the major source of distortion audio amplifiers. Dead time is a brief period of time during a switching cycle when both the high side and low side switches are off.
- It is purposely introduced to the switching waveform to prevent shoot-through current from flowing between VDD and GND. This shoot-through current will reduce efficiency and in the extreme case, may lead to device breakdowns.

The output stage is also very sensitive to the power supply noise. In an open-loop class D amplifier, the Power Supply Rejection Ratio is typically very poor.

The power supply noise becomes another major source of distortion if the output stage is operated without using a well-regulated power supply.

Various other sources related to switching stage error and non ideal behavior will be explained in more detail in the following Chapter 3.

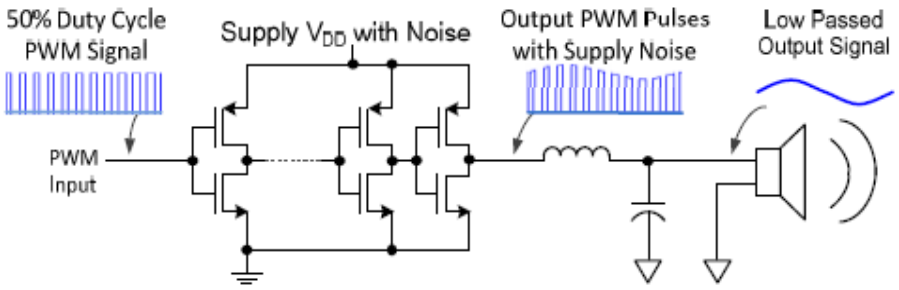


Figure 20: Supply noise on PWM

2.4 DEMODULATION FILTER

The output of the PWM stage must be filtered before reaching the speaker because the signal is a modulated pulse wave, not an analog audio signal that can serve as an output to the speaker. The inductor Capacitor and the resistive load all play a very important role in reconstructing the actual analog audio signal form the PWM waveform.

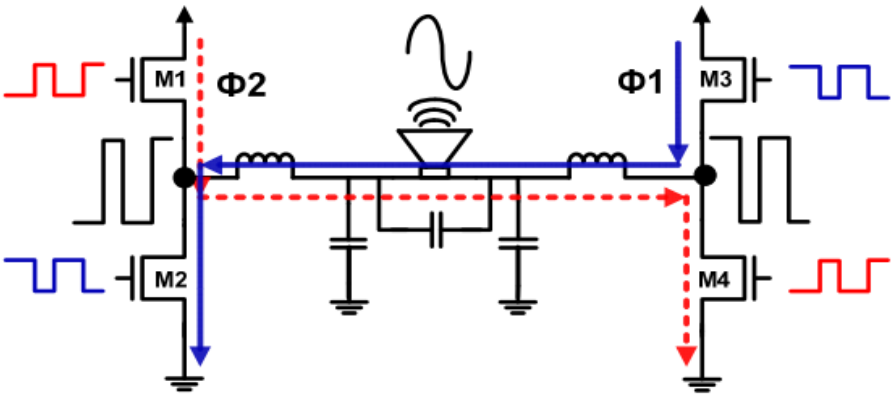


FIGURE 21: Zobel Network

Different kind of filters active, passive and transformers based can be used however it is a good practice to make sure that the filter doesn't cause additional distortion in the system owing to its active nature.

The three step method is generally followed for class D filter stage design. Decide the order of the filter based on the attenuation of the switching frequency given by:

$$At = 10 * \log\left(1 + \left(\frac{f}{fc}\right)^{2N}\right)$$

Design Butterworth filter and calculate the values of L& C accordingly.Then implement the Zobel network.

Chapter 3

SOURCES OF ERROR IN CLASS D POWER STAGE

For a pulse modulation system power conversion is the core. Ideally, a switching conversion system is linear and does not contribute to the other imperfections like noise, harmonics etc. In practice or in real world nothing can be ideal and some sort of switching loss will always exist in the system. It is of crucial importance to fundamentally analyse the error sources in the power conversion stage and the output stage as the core of CLASS D whether Digital /analog is dependent on the power conversion stage and the output stage. A fully Digital CLASS D amplifier will comprise of the following blocks. This type of system can take digital audio bits and finally after processing and amplifying the audio signal; it delivers the Pulse width modulated signal to a filter which finally extracts the analog audio signal which can be audible to human ear.

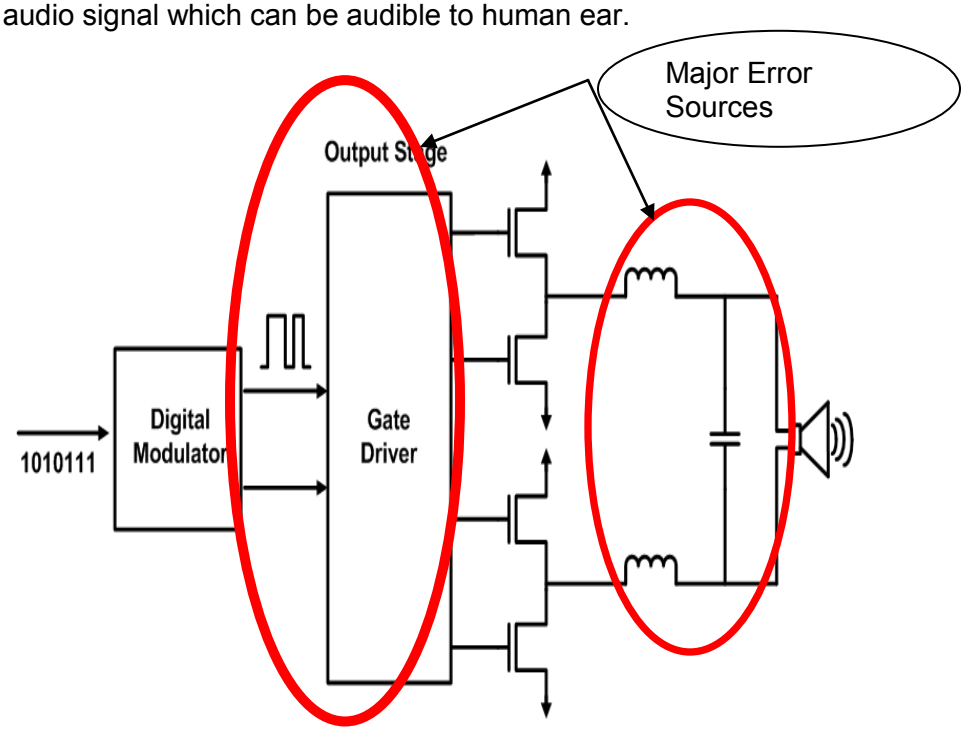


Figure 22: Digital CLASSD implementation showing major error source block

The deviations from the ideal case are caused by physical limitations within the switches, the driver hardware and the filter for demodulation (Low pass filter). The pulse distortion can be categorised as following:

- Pulse Timing Error
- Pulse Amplitude Error

Power Conversion involves the conversion of a pulse modulated signal to a power pulse modulated signal, realized by power switching devices connected in a structure to transfer energy from a DC power source to the load. The essential concerns for the design of the power conversion stage are linearity, complexity and efficiency. The power transistor technology has evolved over the past decade and switching devices are now clearly more ideal suited for switching power stages in audio applications but most of the error sources are accounted for the non ideality of the switches.

3.1 BRIEF OVERVIEW OF SWITCHING DEVICES

The ideal switch operates is fully shorted when ON, represents an infinite impedance when OFF and has infinitely fast transitions between states. Obviously, these requirements can never be met in practice. Within the power range of audio power amplification, Bipolar technology (BJT), MOSFET technology and IGBT (Insulated Gate Bipolar Transistor) switch technology are potential candidates for optimal switching power conversion.

The choice between the devices will depend on application. There are tradeoffs in selecting the type of switches also. The MOSFET is a majority carrier component. This minimizes the switching times.

The resistive nature of the device when turned ON provides good linearity and low output impedance which is specifically interesting in audio applications.

- MOSFET's are available up to 500V with good characteristics as low ON impedance and fast switching.
- BJT is a minority carrier component in which injected minority carriers recombine with majority carriers, which limits the device speed. Furthermore, the low input impedance of the BJT requires somewhat complex driver circuitry.
- The IGBT, being a mixture of the BJT and the MOSFET, is preferable in comparison to the BJT since it is voltage controlled. However, the turn off characteristics of IGBTs and the diode forward drop when turned ON with compromise both efficiency and linearity, unless very high output power is required.

The MOSFET is much closer to the ideal switch than the BJT and IGBT in "lower" power applications as audio (<2KW). It has been used in all the audio amplifiers as the basic switching device no matter whatever kind of switching techniques to be used for the modulation of the reference signal in audio CLASS D amplifier.

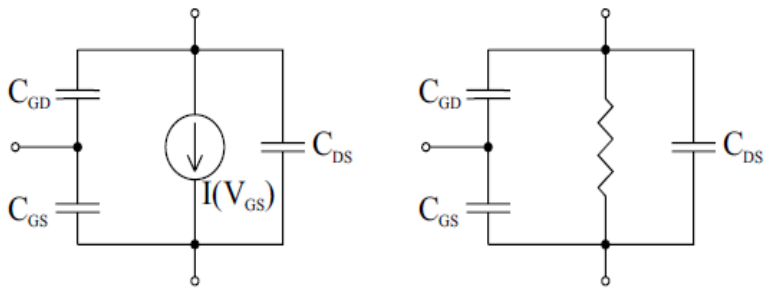


Figure 23: MOSFET model for switching analysis

The following parameters have important influence on the switching characteristics and error sources:

- Resistance between the Drain and the source strongly influences the time constants tdr, tr, tdf and tf. From the perspective of minimizing distortion, Rds should be as as small as possible.
- Cgd is the determining parasitic capacitance on tr and tf, i.e. s the Cgd should be as small as possible.
- Cgs is the determining parasitic capacitance on tdr and tdf, i.e. it should be as small as possible.
- Vg, Vth also influences tdr, tr, tdf and tf.

BASIC CAUSES OF PULSE TIMING ERRORS

- Finite Rise and Fall time
- Blanking Delay
- Turn on and Turn off delay

BASIC CAUSES OF PULSE TIMING ERRORS

- Perturbations on the power supply that feeds the switching power stage.
- Finite impedance for the power switches.
- High frequency resonant transients on the resulting pulse power signals.

Obviously, errors correlated with the modulating signal will generate distortion where as errors that are non-correlated will generate noise in the general power stages. Basically, the focus of this work is to get away with the Pulse amplitude error which happens to distort the PWM output for the audio.

Hence we will discuss a further more on how to analyse the Pulse amplitude errors.

3.2 ANALYSIS OF PULSE AMPLITUDE ERROR

Pulse Amplitude Errors is the general designation for error sources that distorts the amplitude of the modulated pulse train. Below is an analysis of the same with a practical example.

Different causes of the Pulse Amplitude error:

- Power supply perturbations
- Finite switch impedance effects
- Carrier generator jitter and noise (especially within the target bandwidth).
- Speed of the comparator, especially in terms of differential delay between turn-off and turn-on.
- Inherent offset within the comparator leads to edge jitter and has to be sufficiently small.
- Carrier symmetry errors in double sided modulation. The error source is introduced if the individual carriers are not symmetrical.
- DC offset errors. The error is represented relative to the amplitude of the carrier.

3.3 MATHEMATICAL DERIVATION OF PSRR & PS-IMD

Let say that we have a power supply V*s* (*t*) which is comprised of a DC component and also a sinusoidal component. We know that the power stage multiplies with the Vr(t) (Ideal PWM waveform coming from the modulator stage). Ideally the multiplication should be linear but due to the noise over riding over the power supply also modulates the clean pulse width modulates stream.

Due to non linearity of the system the output of the output stage would be:

$$Vout\,(t) = Vr(t)Vs(DC\ component\ of\ the\ Power\ Supply) + Vr(t)vs(t)$$

If the $vs(t)$ is considered harmonically perturbation in the power supply then it can be represented as:

$$vs(t) = \sum_{m=0}^{max} Acos(mwm(t))$$

A: represents the harmonic amplitudes relative to *VS*

The reference signal can be written as:

$$Vr(t) = Mcos(\omega rt)$$

Hence the resulting output would be:

$$Vout(t) = 1/2 \sum_{m=0}^{max} A[\cos(\omega rt + m\omega mt) + \cos(\omega rt - mwmt)$$

Clearly, any components on the perturbed power supply will directly intermodulate with the modulated signal and generate IM components with amplitude:

$$\frac{1}{2}MA\ \ at\ \omega r \pm \omega m$$

The intermodulation distortion is exclusively determined by the components of the perturbing signal.

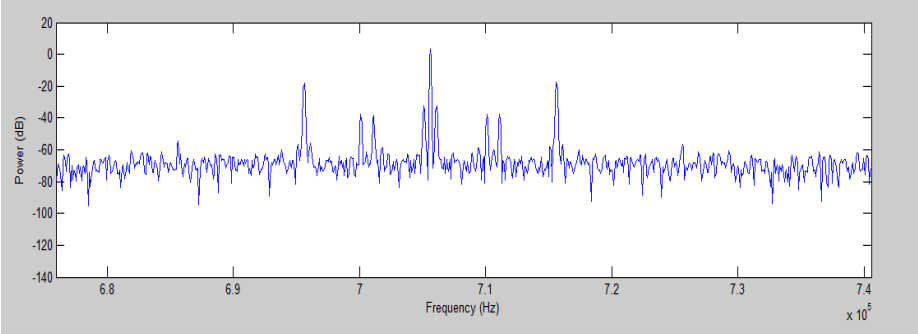


Figure 24: Sidebands around the Audio Signal due to power supply noise

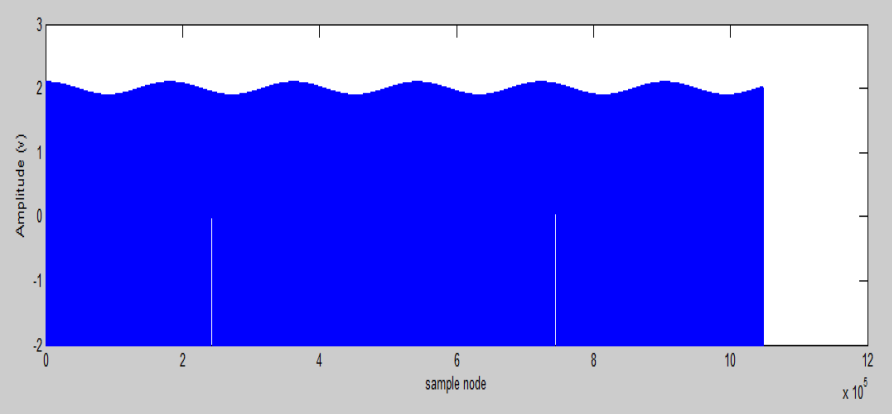


Figure 25: SIMULINK result showing the noise overriding the clean PWM

FINITE SWITCH IMPEDANCE EFFECTS

Another fundamental element that distorts the pulse amplitude is caused by the finite impedance of the power switch. The power MOSFET (I-V) characteristic when ON can be simplified to a resistor in parallel with a power diode. The body diode is modelled by a constant turn on voltage *and* a dynamic resistance. In general *RD* will be considerably lower that RDS (on) and the diode resistance will therefore dominate the reverse channel at high currents. When possible, reverse channel conduction through the body diode should be avoided totally by simply choosing a MOSFET.

Although the choice of power transistor is a compromise between several other parameters, and a very low ON-resistance compromises switching speed and

requires a more powerful driver circuitry. The finite switch impedance results in amplitude modulation. The pulse amplitude modulation can be expressed by the very simple relation:

$$vp,real = vp,ideal - Rds,on * IL,max$$

The error is linear and can be interpreted as a simple output impedance. At higher output currents where the Rds on relationship does't hold the finite switch impedance will introduce both linear and non-linear distortion. The error on *vp* will depend upon the polarity of the current leading to odd harmonic distortion of the modulating signal. However, The distortion only occurs at high output levels. The non-linear error contributions will be small relative to the signal and other contributions. A high peak output levels, *vp* the power stage will mostly in the stage which are free from the non linear distortion. In all applications the high ON resistance is simply not desirable from any point of view.

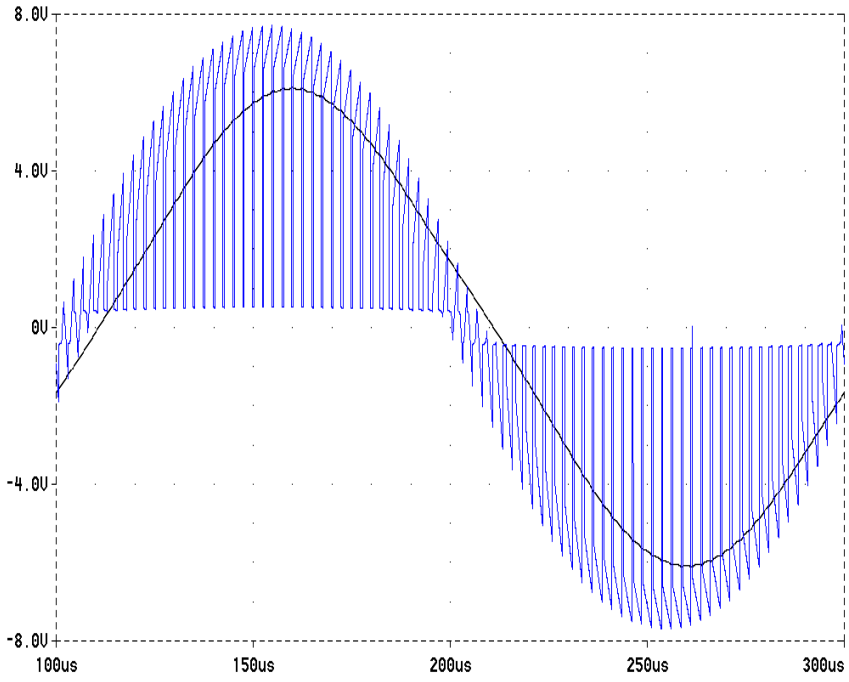


Figure 26: Pulse Amplitude error due to finite switch impedance

It is bound with considerable difficulty to realize the power conversion stage with sufficient linearity for high quality PMAs. With the documented error sources, closed loop error correction systems are concluded to be vital for practical, efficient and robust implementation of the power conversion stage in both analog and digital PMA systems.

Chapter 4

EXISTING FEEDBACK STRATEGIES FOR DIGITAL CLASS D

4.1 NON LINEAR FEEDBACK & PREDISTORTION

This feedback approach has two sub modules:

- Feedback controls non linearity caused by the Output Switches.
- Predistortion compensated for the PWM non Linearities
- Uses Internal Model Control - Decomposed the Feedback Design into two sub tasks :
- Optimization of the matching of the two parallel Signal Paths The PWM and the non linear simulator S ; helping achieve a better Stability Margin.
- Optimizations of the Feedback filter to achieve a balance between feedback at different audio frequencies.

INTERNAL MODE CONTROL

Important point about the IMC_ "It's benefit lies in the fact that it allows us to concentrate more on the controller design without having to worry too much about the control stability."

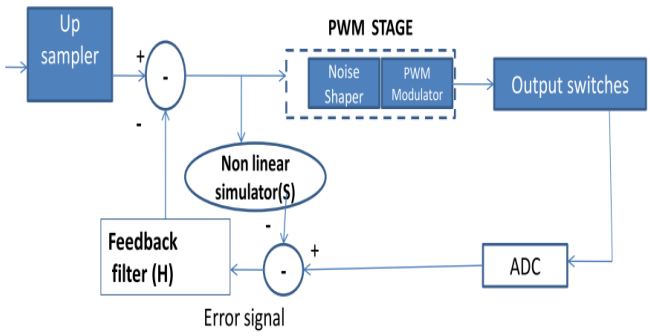


Figure 27: Feedback incorporating IMC principle

The Non linear Simulator S is assumed to model known non linearity of the PWM. The differencing unit D can isolate the Distortion produced from the power switches. This distortion then is fed to the feedback Filter. The error signal is applied as a correction signal to cancel the original error.

How this approach can help in achieving better Feedback Stability?

- The error signal generates the correction signal; applied equally to the PWM and the non linear simulator S.
- The correction signal affects both equally
- The two corrections cancel in the difference unit D
- No further recirculation and the loop is guaranteed to be stable.

TWO CANCELLATIONS IN THE BLOCK

- Cancellation in the difference unit D which helps stop recirculation in the loop.
- Cancellation of errors produced by the power switches.

Perfect cancellation of the errors caused by the power switches would require that the transfer function of H , the PWM , the ADC , the output Switches and any other component would be unity. It's inevitable to have one sample delay in any digital feedback Loop along with intrinsic delay. This requires a Phase Advance in H i.e. the feedback Filter which will give a rising amplitude response like one shown below :

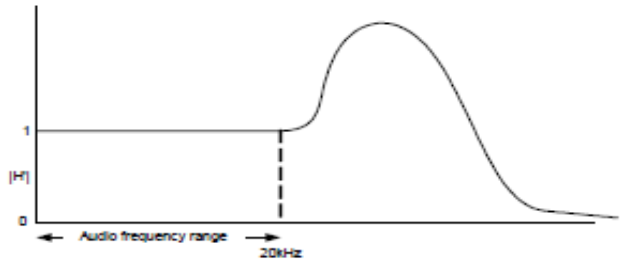


Figure 28: Noise Transfer function of Loop

LIMITATION TO THIS FEEDBACK

- Ideally the NTF need to be as small as possible which requires a big amount of feedback ;which can be achieved by tweaking the filter 'H'.
- "How Large transfer function H' large can |H'| prudently be made. Three basic factors that argue for the limits:"
- A distortion figure that rockets above 20kHz might not be viewed favourably
- Stability Consideration
- Circulation of ultrasonic noise, if the feedback signal is derived using an ADC having a rising ultrasonic noise floor

PREDISTORTION BLOCK

Why predistortion can be helpful in the Non - Linear IMC based Feedback??

- Non linearity inherent in PWM needs to be compensated.
- Negative Feedback calls for stability problems.

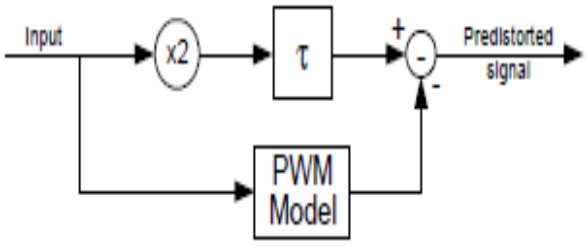


Figure 29: Pre-distortion block

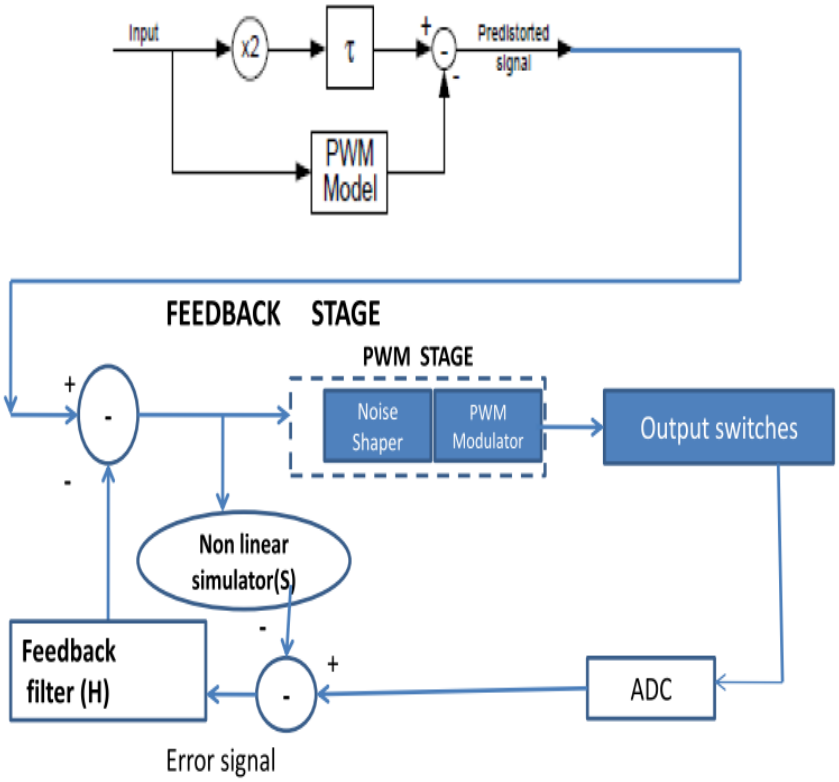


Figure 30: Overall Implementation of the IMC approach

4.2 DIGITAL CLASS D WITH ANALOG LOOP FEEDBACK

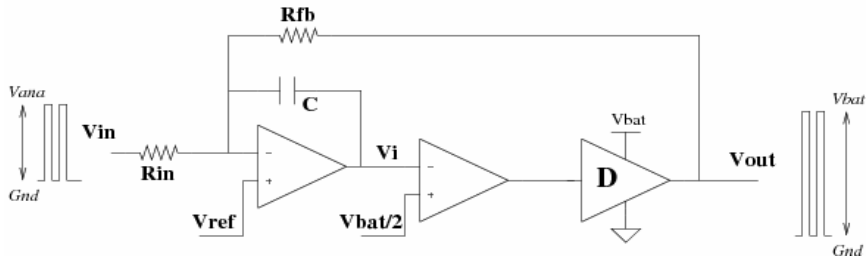


Figure 31: Control loop for Digital class D Amplifier

HOW IT WORKS?

- Closed Loop Gain of the analog loop for the audio frequencies

$$\frac{R_{fb}}{R_{in}} \geq \frac{V_{bat}}{V_{ana}}$$

- Above Condition ensures stability at the end of Phase 1,3.
- Basically, analog loop must have a minimum gain which should be equal to the ratio of supplies to ensure stability.
- Delay between the Vin and Vout due to delay of the gate drivers.
- Time constant of the first stage Integrator calculated using the delay parameters of the gate drivers.
- Resistors Rfb and Rin act like sources or sinks depending on the phase of Vin and Vout. They are like constant current sources which charges and discharges the Capacitor C.

Loop delay by characterizing the gate drivers across the process and temperature.If the time between the rising edge of the input pulse and the rising edge of the output pulse is not the same to the delay for the two falling edge. Equalizing the currents through the Capacitor should be equal IC3 = IC1 during the two working phase. This will ensure Linearity.

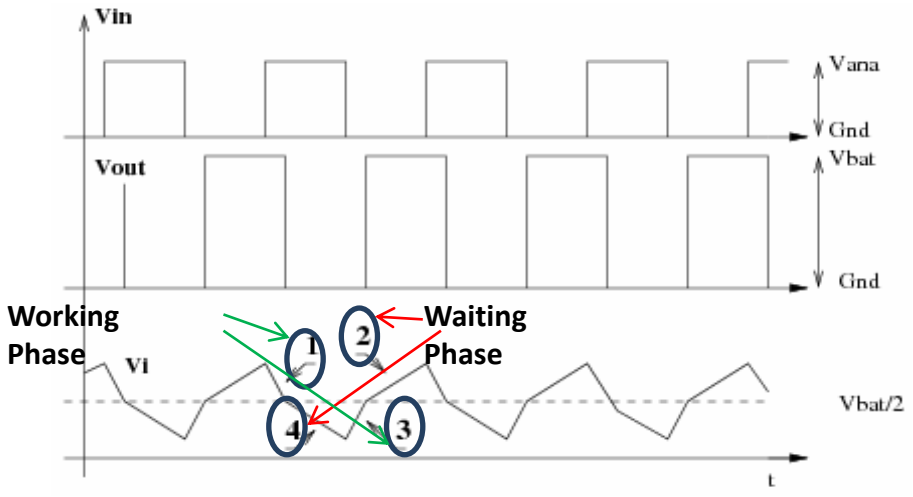


Figure 32: Timing Diagram of how the Phases Work?

- PHASE 1,3 : Working phases
- PHASE 2,4: Waiting Phase as the loop is waiting for a new event to happen.

Each channel gets a digital, 1bit PWM input based on a Regulated power supply into a cascade of two integrators that form the second-order loop-filter, followed by a high-speed comparator prior to being fed into the power transistor stages. The comparator switching decision, which is based on the integrator outputs, is utilized to control the operation of the output stage.

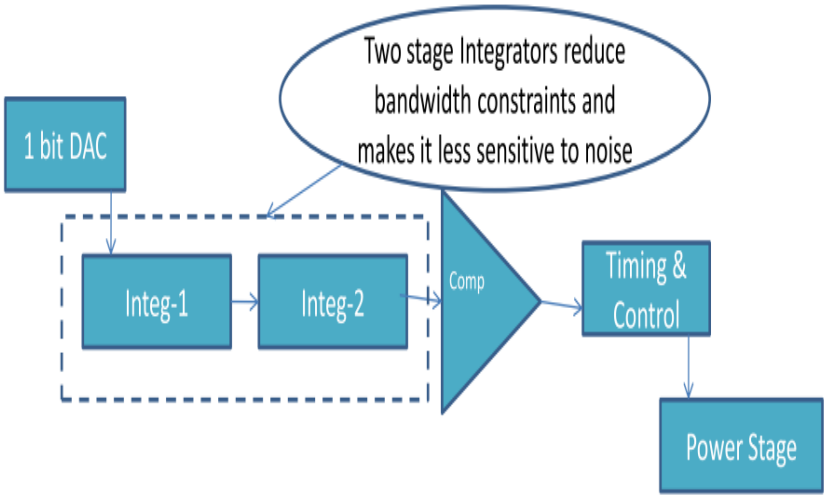


Figure 33: Block level Implementation

4.3 DIGITAL CLASS D AMPLIFIER WITH ERROR REMODULATION

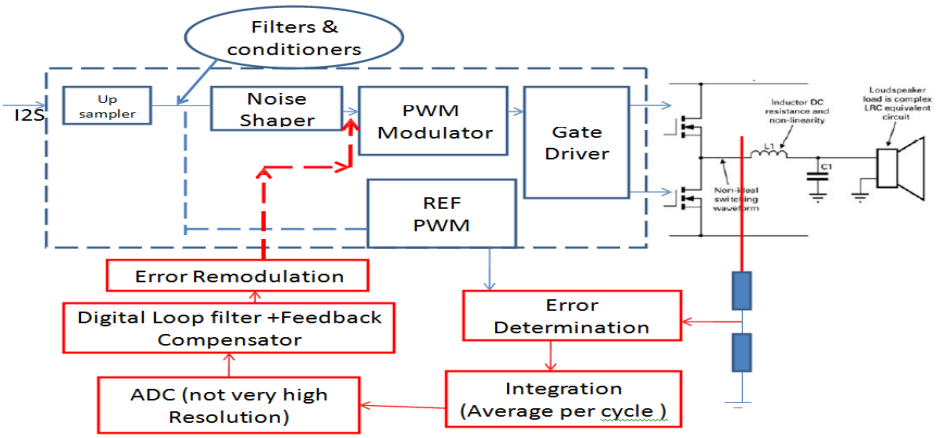


Figure 34: Direct Digital Feedback

Basic Idea of how it works?

All the corrupting factors in one way or the other either affect the width or the height of the modulation pulse. These are equivalent, in the fact that they affect the area under the pulse. Any error in the area would be directly equivalent to a voltage error at the load of the Digital Amplifier.

Direct Digital Feedback architecture operates simply by determining the pulse area error and passes this information back to the digital domain where feedback compensation can be made and remodulation of the error signal (integrated over cycle to cycle) can be performed.

- For implementing the digital correction process, the error information is passed to ADC which need not to be high resolution but should be fast enough for the recursive correction action. The overall System Dynamic range will not be limited by the range of the ADC.
- Having an accurate reference signal in order to establish the correct error level or to determine the instantaneous error. Critical design considerations are involved for this.

ERROR REMODULATION PROCESS:

- Extraction of an error signal from the difference between the reference pulse width modulation signal and power stage output
- The error PWM conversion system is then used to compensate for the power supply noise and nonlinearity of the power stage
- Basic Elements :
    - ANALOG DOMAIN : Integrator , Attenuator , Sample and Hold , comparator
    - DIGITAL DOMAIN : Digital Loop Filter , PWM

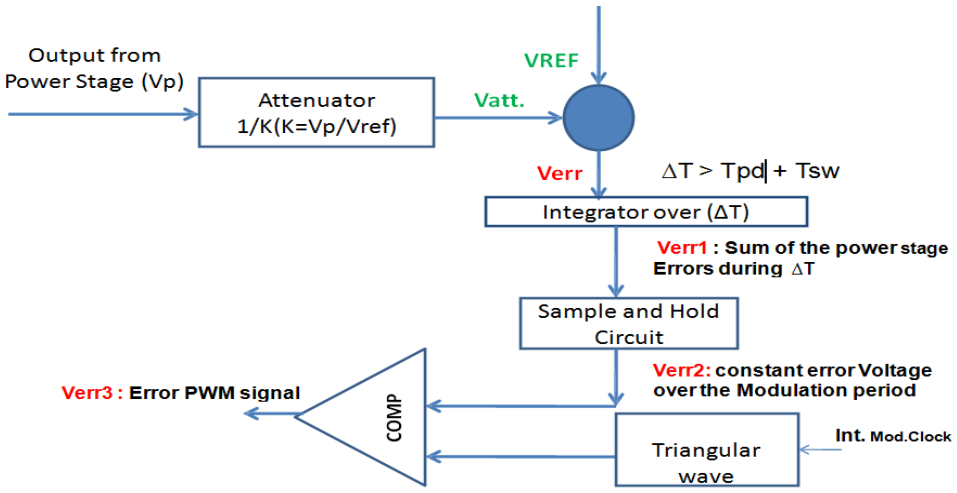


Figure 35: Analog part in the feedback

Conversion of Error PWM signal

- A negative Verr2 will narrow the error PWM signal Width
- A positive verr2 will widen the error PWM signal Width
- There by the width of the Verr3 controlled by the power stage error.
- The change in the error PWM will be determined by the slope of the triangular wave and the Integrator's gain.

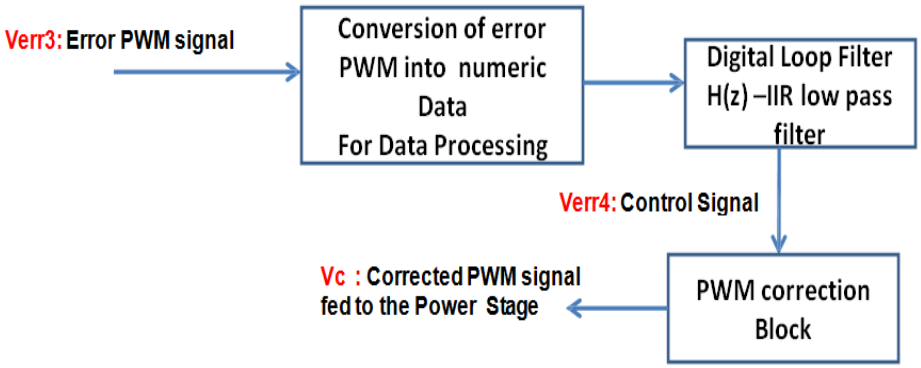


Figure 36: Digital part in the feedback

The Digital Loop filter used should be designed in such a way that there is a stable loop operation and nearly linear phase response in the audio band. Basically, whole idea of the digital feedback technique is if the energy of audio band distortions and noise are limited, it can be transformed to inaudible artificial noise in the hi-frequency band so that the sound quality in the specified audio range improves.

Chapter 5

DIGITAL CLASS D: MODELLING & SYSTEM DESIGN

5.1 MODULATOR DESIGN

The Class-D modulator converts audio data into power stage gating pulses. The choice of the gating pulse format directly effects power stage efficiency. There are four different existing methods for pulse modulation PAM, PDM, PWM &PPM. Of all these existing methodology PWM seems to give the best efficiency. However, direct conversion PWM of audio data is not practical in terms of real circuit implementation. To avoid deteriorating audio performance the modulator must be low distortion. At the same time it must also be computational efficient to satisfy power and silicon area constraints. This is because audio samples have long word-length, and therefore the clock speed required to modulate such signals is beyond realizable. For example, a clock running at closed to 1 THz is required to generate the digital ramp necessary for modulating audio signals with 24-bit word-length and 48 kHz sample rate. This is not a practical number for present semiconductor technology. Using a sigma delta modulator before the DPWM generation takes away this problem and also maintains the required resolution of the audio signal in the baseband.

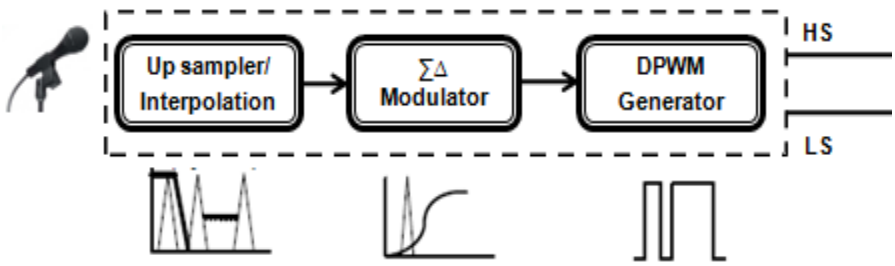


Figure 37: Digital Modulator Architecture

CIFB BASED MODULATOR DESIGN

A 6 bit CIFB modulator with an OSR of 32 and signal BW of 22 KHz was designed using the delsig Toolbox. Below shown is a graph plotted for order vs. SNR for different bit quantizer. This helped in the selection of order of the modulator and the bit in the quantizer also.

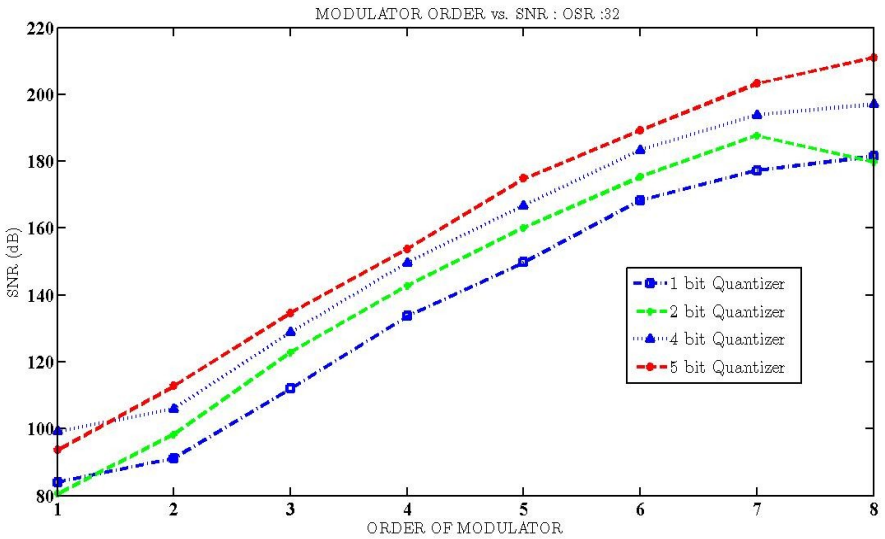


Figure 38: Modulator Order vs. SNR

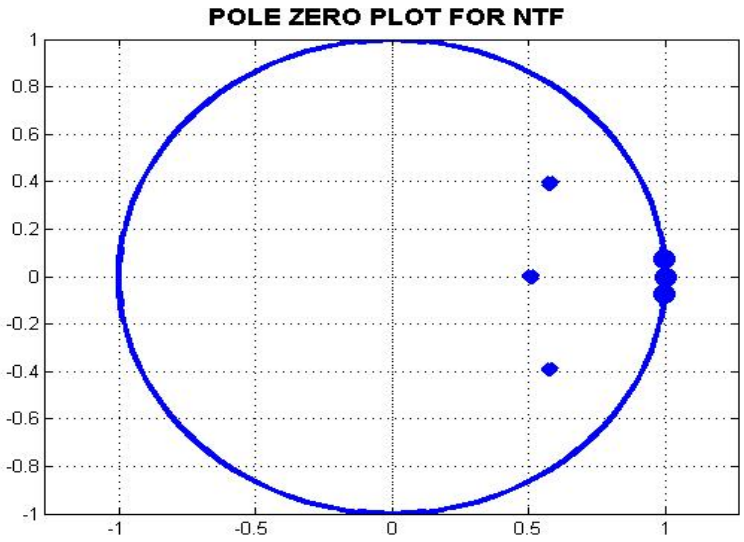


Figure 39: Pole Zero Plot for NTF

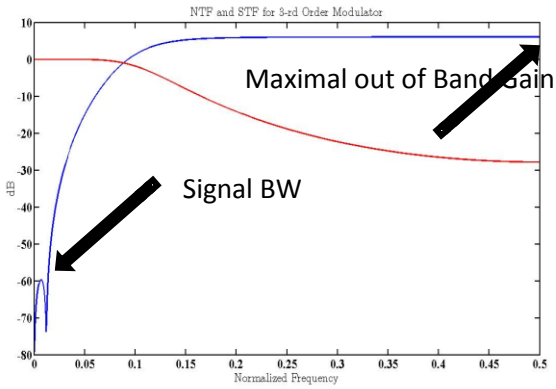


Figure 40: STF & NTF

>> STFq

Zero/pole/gain:

0.030041

(z-0.8499) (z^2 - 1.412z + 0.6119)

>> NTFq

Zero/pole/gain:

(z-1)^3

(z-0.8499) (z^2 - 1.412z + 0.6119)

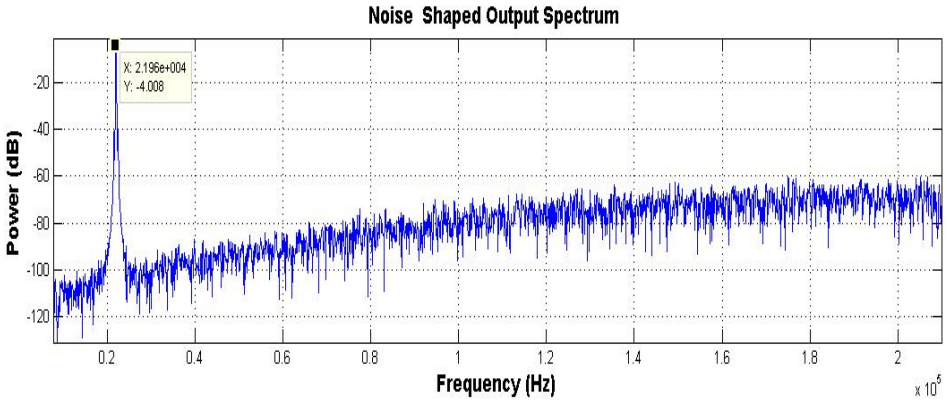


Figure 41: Zoomed in O/P spectrum with 22 KHz PCM audio input

Coefficients	OPTIMIZED	SCALED
a1,b1	.0025	2^{-9}
a2	.0057	$2^{-9} + 2^{-8}$
a3	.0126	$2^{-7} + 2^{-8}$
c1	0.3531	$2^{-2} + 2^{-4}$
c2	0.7930	$2^{-1} + 2^{-2} + 2^{-5}$
c3	63.4719	$2^{2} + 2^{4} + 2^{3} + 2^{5} + 2^{1} + 2^{0}$

Figure 42: Dynamically scaled coefficients

The above plots are a result of a designed 3 rd Order CIFB based modulator with Optimized zeroes in the NTF. The overall SNR performance of around 90dB was achieved in the audio band of interest. The coefficients used for the structure were also dynamically scaled and optimized using the delsig toolbox. The coefficient was further scaled in order to make sure the coefficients are in the integral power of 2. The STF and NTF get little altered due to this but however the effect is really small. In digital audio, the noise shaping is more as a truncation of the bit from high resolution to low resolution while maintaining the resolution in the audio bandwidth and pushing the bit truncation error out of the Audio band. The whole concept remains the same, loop architecture remains the same like cascaded and MASH based. Except for the thing that now integrators are replaced by accumulators (implemented by adders and flip flops) and the coefficients are now added or subtracted from the bit stream by left shift or right shift operation.The Quantizer in this case acts more as truncator (digital comparator). It is responsible for truncating the extra LSBs while preserving the MSBs. Once the Coefficients are obtained the next task is to determine the word

length for the arithmetic needed within the modulator loop. The word length is determines as below depending on the OSR (or interpolation used) where N1 is the word length of the first accumulator:

$$\frac{1}{a1^2}.\frac{(2^{-N1})\text{^}2}{3}.\frac{1}{OSR}$$

Considering a best case of having a -100dBFS level of in band Noise and a full scale sine wave power can be considered as M^2/2.

Number of bits in the first stage should satisfy:

$$\frac{1}{a1\text{^}2}.\frac{(2^{-N1})\text{^}2}{3}.\frac{1}{OSR} < 10^{-10}(M^2/2)$$

which comes out to be a 21 bit arithmetic in this case. Similarly, second and third stage modulator word length was determined by the below mentioned equations and using coefficients a1, c1 & c2.

Since the noise added to the second integrator would be first order noise shaped when referred to the modulator input which comes out to be 18 bit arithmetic:

$$\frac{1}{(a1.c1)^2}.\frac{(2^{-N2})}{3}.\frac{\pi}{3.OSR^3}^2$$

Similarly, the third integrator arithmetic comes out to be 14 bits.

$$\frac{1}{(a1.c1.c2)^2}.\frac{(2^{-N3})}{3}.\frac{\pi^4}{5.OSR^5}$$

The basic block diagram of the implementation is as shown below and the simulink based model snapshot has been added in the appendix. The loops are basically implemented using full adders, flip flops, shift register and delays.

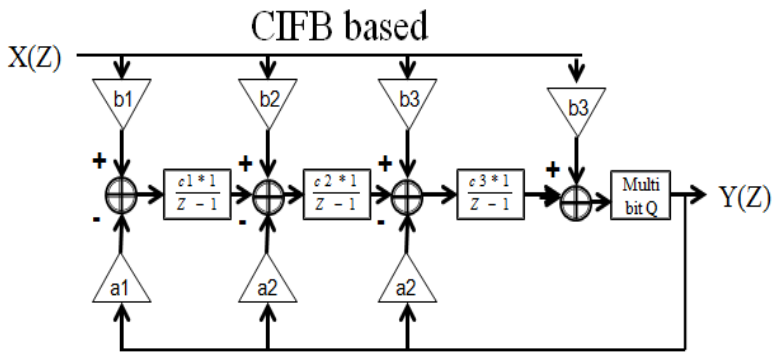


Figure 43: CIFB based Topology

5.2 SAMPLING TECHNIQUE – UPWM

After the PCM are reduced by the noise shaper, the next block implemented is a PWM generator. Uniform Sampling has been chosen for this work. There are different kinds of sampling techniques which helps in reducing the distortion in the resulting PWM wave. Few of them generate harmonics of the Carrier signal and the input signal while few also generate IMD products. The UPWM based double sided sampling is explained in the figure below. As seen, there are different sampling instants denoted by S and S'. The ones in red depict the real sampling instant where as the one in green depict the actual sampling instant. This is the major cause of distortion from different sampling techniques employed in a PWM modulator. Almost all of the sampling techniques will have some sort of distortion associated with them.

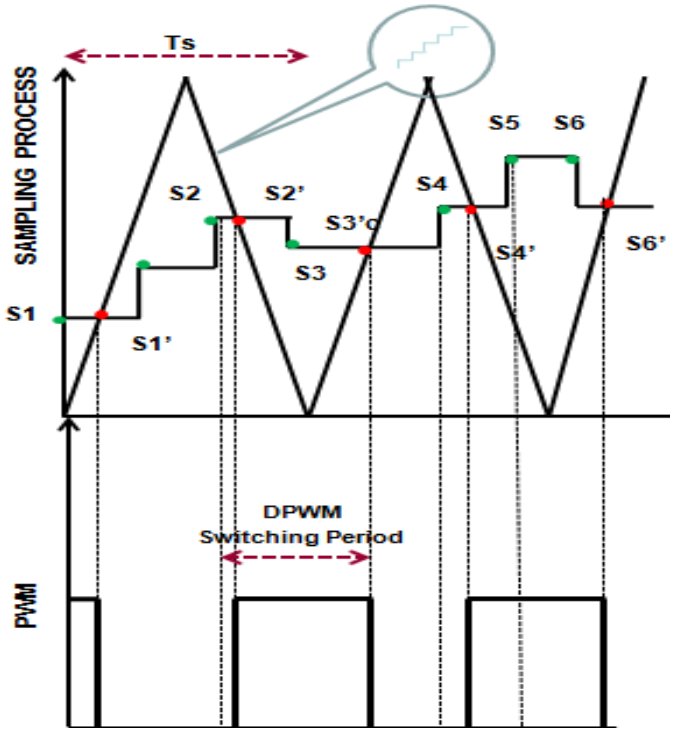


Figure 44: UPWM based Double sided Sampling

Any PWM sampling technique can be traditionally differentiated by the edge modulation and the class apart from the sampling technique itself. The edge modulation determines whether its single sided or double sided.

The double sided modulation doubles the information stored while the pulse frequency remains the same. Class AD and BD is another way of differential PWM wave; two state switching (AD) or three state switching (BD). Basically UADD type of Sampling technique & Algorithm has been implemented in this work. Uniform sampling AD based double sided sampling technique.

A counter based PWM generator block along with an UPWM Algorithm has been implemented using Simulink and Matlab. To generate a PWM each 6 bit of the noise shaped and oversampled bit stream is compared to a dual edge counter ramp. Input clock frequency of the counter is directly proportional to the sampling frequency and the number of bits of the noise shaped bits should be running with

a frequency of 90.316MHz (based on audio sampling rate of 44.1 KHz and using an OSR of 32).Basically, in order to create a bit stream waveform, the reference digital ramp or the saw tooth ramp has to be able to sweep all the levels of the input bit stream that's why the use of noise shaper in between gives an advantage of reducing the number of bits and hence the number of levels the counter has to sweep through. A Bidirectional counter was implemented using JK flips and Logic gates in simulink. The implemented block diagram is shown below. The PWM generator using the counter and the input stream was implemented in a MATLAB embedded function. The MATLAB code for the same has been included in the Appendix.

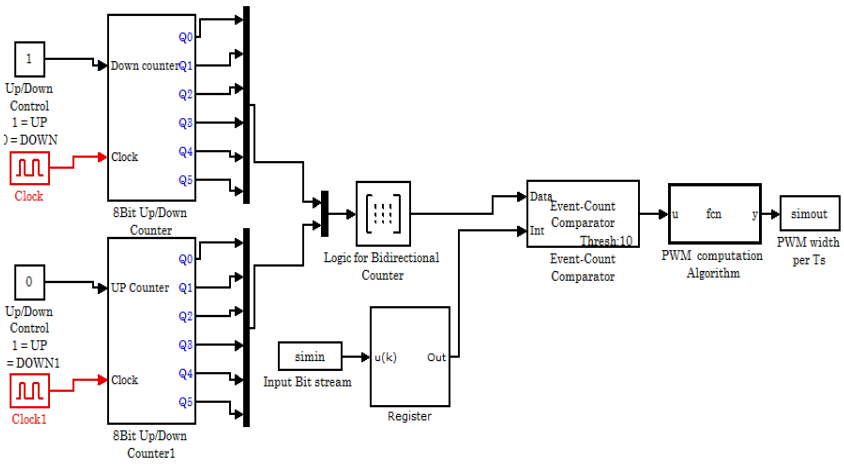


Figure 45: Implementation of UADD based DPWM

A counter based PWM implementation has been realized along with an Algorithm which computes the required duty cycle. This embedded matlab algorithm works for computing the duty ratios for the output DPWM pulses. So for example, a input noise shaped bit stream sequence of 6-bit at 44.1kHz, first, it calculates the duty cycle of a PWM signal, and of course, this value is still represented in 6-bit format, then, these new values are mapped to rectangular pulses whose duty cycles are exactly these results. If my nth input is X, then this algorithm will

predict that the pwm duty cycle to be Y (Y belongs to the range of 0~63), then the nth output pulse should have Y number of one's followed by 63-Y zeros. Similarly, it will form each output pulse this way to get a digital PWM pulse train. There are various constant and coefficients used for this and has been referred from reference [19] to come up with this algorithm.

Test case 1: DPWM generation

Input: 6 bit 5 KHz sampled at 44.1 KHz (128 samples).The duty ratios should be in the range of (0-63) as shown below in the figure. With these duty ratios, counter values are compared and hence the DPWM is generated.

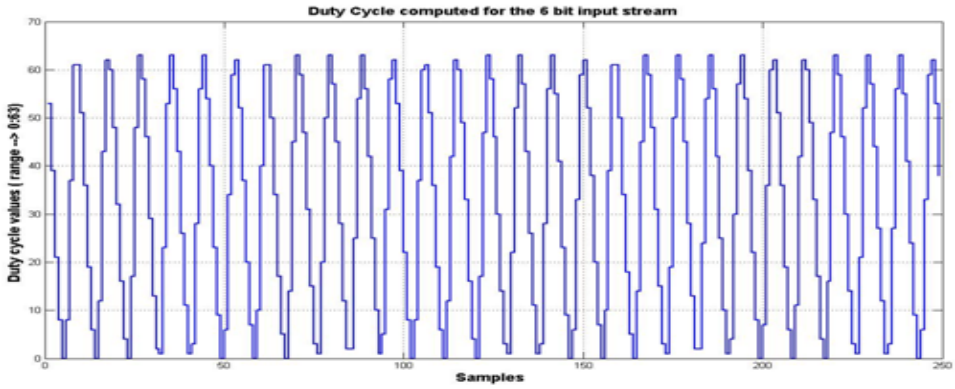


Figure 46: Duty cycle computed for the test case 1

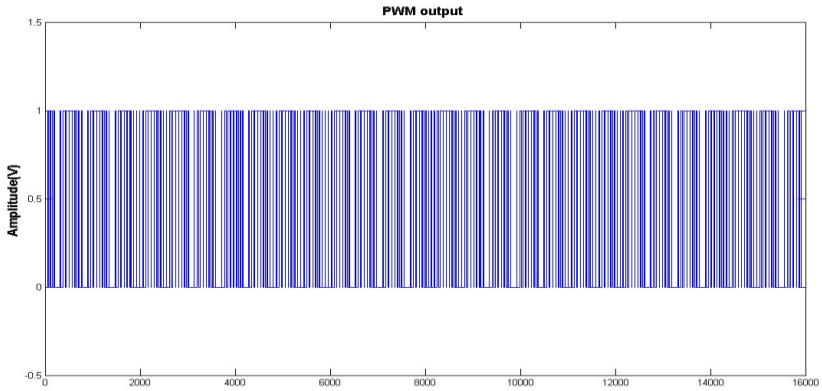


Figure 47: PWM reconstructed using Computed duty ratios

Test case 2: DPWM generation

Input: 8 bit 5 KHz sampled at 96 KHz (256 samples).The duty ratios should be in the range of (0-255) as shown below in the figure. With these duty ratios, counter values are compared and hence the DPWM is generated.

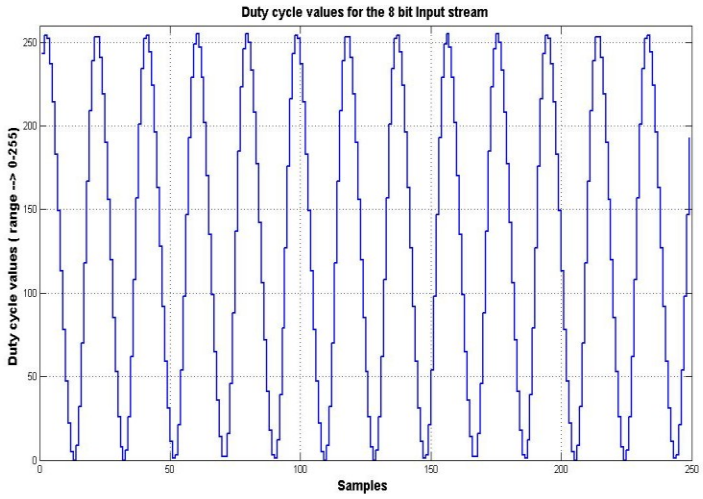


Figure 48: Duty cycle computed for the test case 2

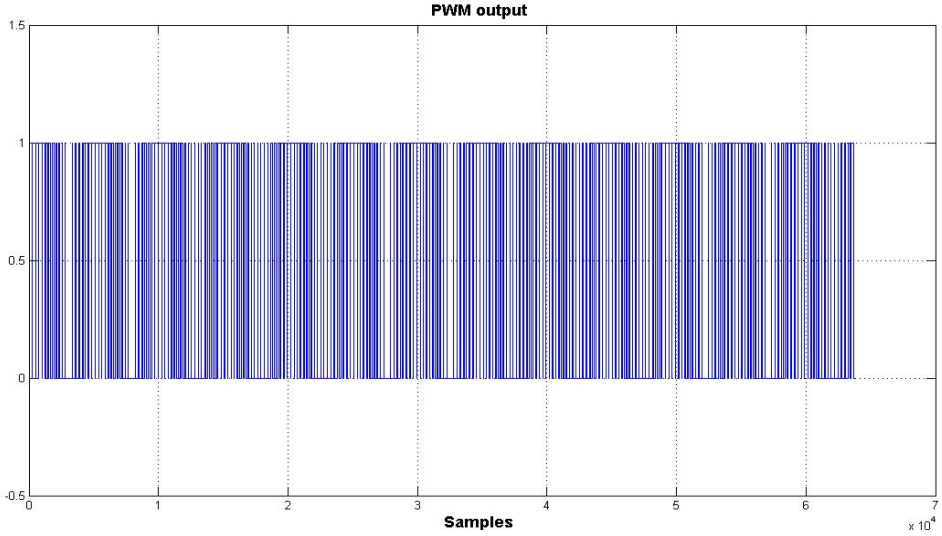


Figure 49: PWM reconstructed using Computed duty ratios

The Uniform sampling AD based Double sided modulation scheme has been used in this work. Single sided uniform sampling has also been analyzed using a

up going counter only. The PWM analysis for both of them revealed that single sided modulation scheme is suspected to more harmonics compared to double sided. A spectral analysis table has been provided in chapter 2.

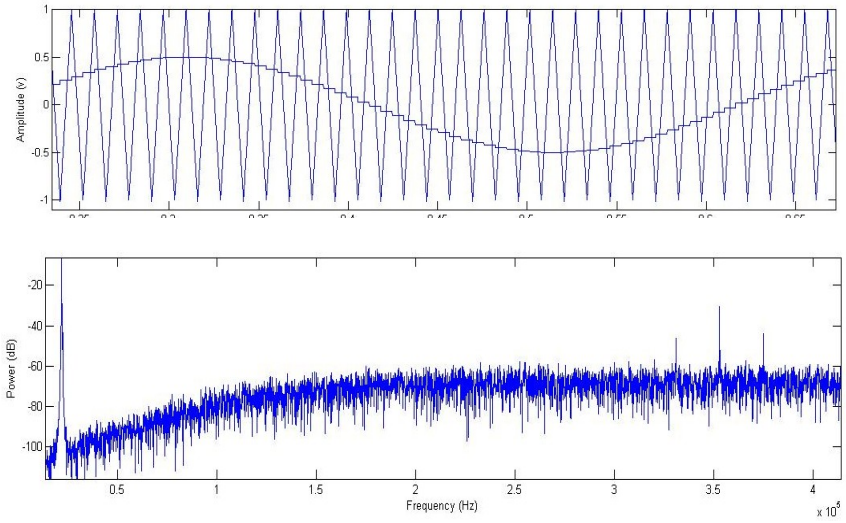


Figure 50: Spectrum of PWM o/p using UADD

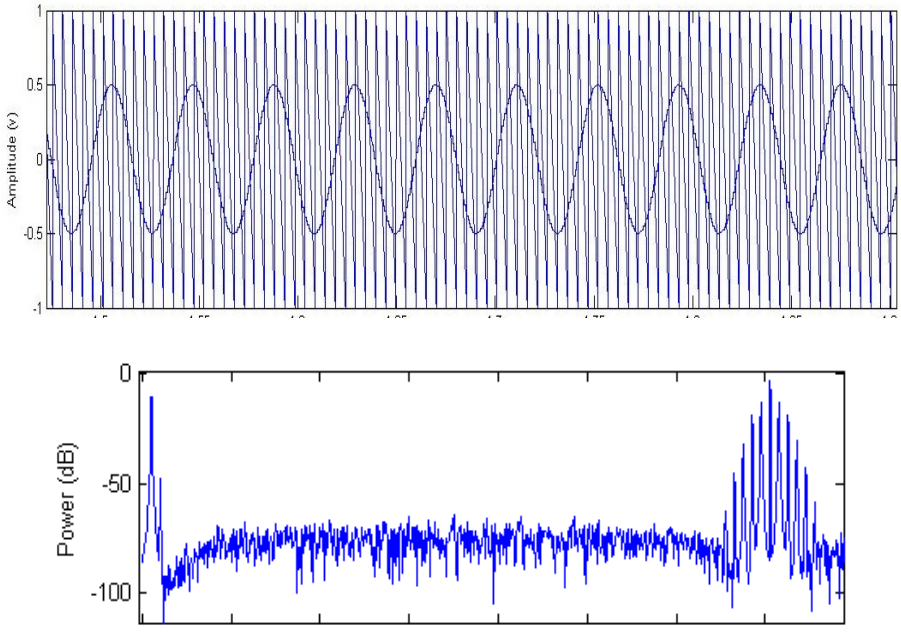


Figure 51: Spectrum of PWM o/p using UADS

5.3 POWER STAGE & DEMODULATION FILTER

The power stage model used here is based on a half bridge topology and a demodulation filter (Zobel network) has also been added at end along with a load.Simpower systems was used to model the power stage including the non idealities of noisy supply and blanking delay.The key source of non ideal behavior of the power stage are the blanking delays and the unstabilized power supply perturbations. Both the effects have been emulated in the model. The blanking delay has been implemented by replicating the incoming pulse signal. The blanking delays have to be in the power stage intentionally in order to avoid shoot through currents during the transition from ON to OFF state or vice versa. This saves the power stage from breakdown and short circuit current flow. It helps in reducing cross over distortion. However, the analysis of a blanking pulse in terms of frequency domain shows that it creates harmonics of the signal depending on the blanking delay time (td). Blanking Delay (td): the Dead Time between TON & TOFF of switching leg Appear as Error Voltage at PS output correlated with Load current and leads to Harmonic Distortion.

Derived Fourier Coefficients

$$An = \frac{2}{n\prod}(-\sin(tdn\prod/Tc)$$

$$Bn = \frac{2}{n\prod}(1+\cos(tdn\prod/Tc)$$

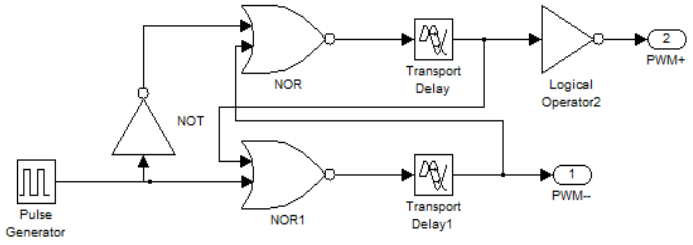


Figure 52: Simulink Model of Blanking delay generator

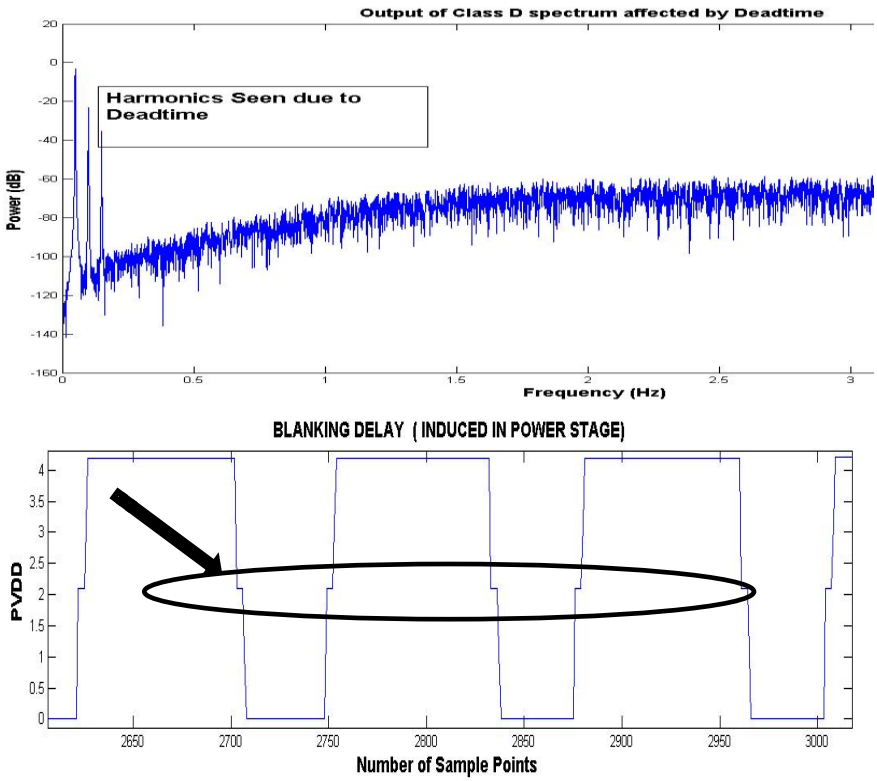


Figure 53: Generated Blanking delay in time domain & Frequency domain

The power amplification stage in class D is based on Metal-oxide-silicon field effect transistors (MOSFETs) instead of bipolar junction transistors (BJTs) because MOSFETs have a faster response time, ideal for high frequency operation. Class D amplifiers require two MOSFETs. They are either fully turned on or turned off for a very short period of time. When a MOSFET is fully turned on, the voltage drop across the transistor is small. When a MOSFET is turned off, the current across it is zero. The rapid switching of MOSFETs between these two stages makes it very efficient. In this model two MOSFETs in a half bridge connection have been used. These are the n-channel MOSFET (NMOS) and the p-channel MOSFET (PMOS). The parameters of the MOSFET in sim power systems have been chosen to emulate a real MOSFET available in silicon from IRF. Some analysis was also done on various MOSFET parameters from IRF

based on the datasheet available parameters including Rds_on, Cgs, and Ton & Toff. This was more for my understanding as to how with switching frequency range; power dissipation in a MOSFET varies as the switching speed is an important factor in the whole class D design. Using a higher switching speed might be a good option till the PWM generator stage as it will restore the input bit depth and resolution; however this might not be a good choice for the power amplification stage. It has been well described in chapter 3 that there have been many sources of error associated with switching leg of the power stage. So analysis of the dependence of different MOSFET parameters on the power dissipation with varying switching frequency should be taken into account. The below graph shows the operating frequency versus Power dissipation based on Rdson, Cgs, Ton and Toff.

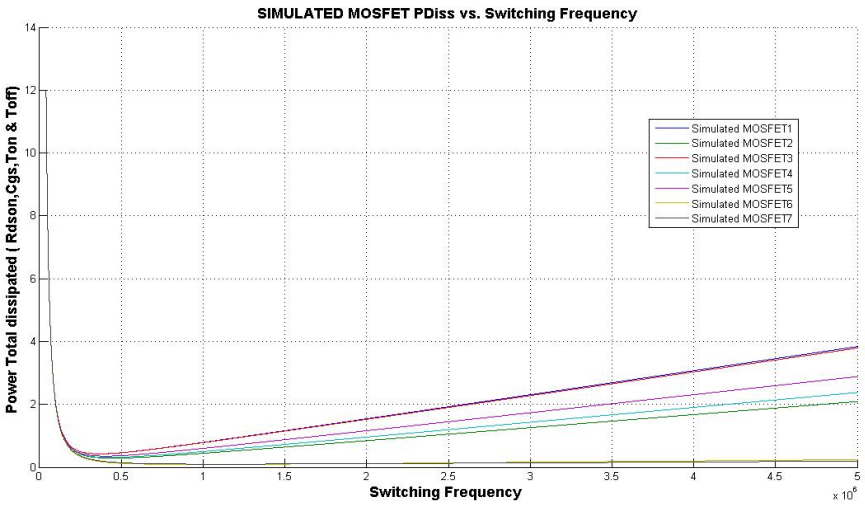
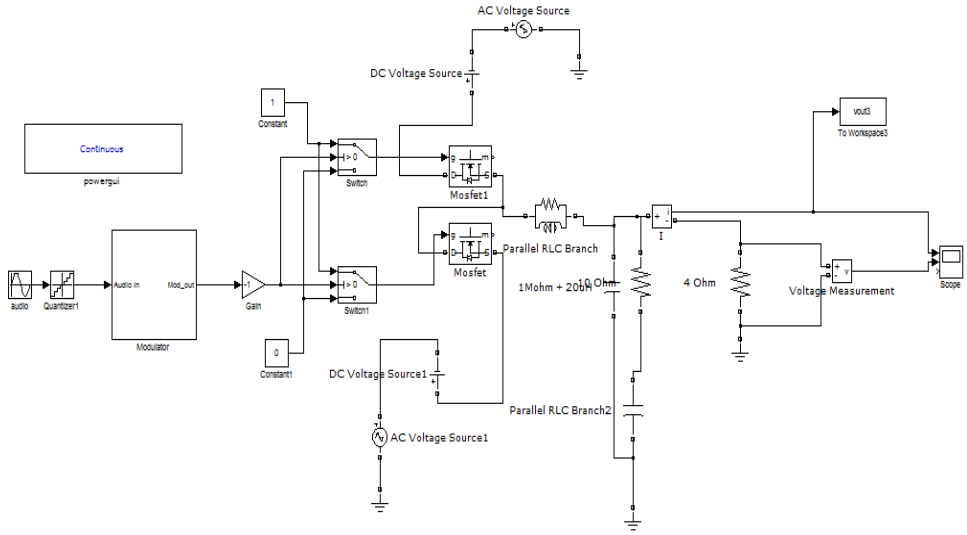


Figure 54: Simulated MOSFET P dissipation vs. Fsw

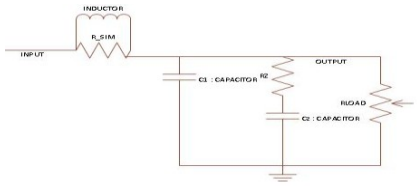
The power supply stage model in simulink is as shown below. The parameters of the MOSFET and the filter used were tweaked in order to make the simulation work. However the simulation along with the demodulation filter could not work fully due to convergence issues.

However, the demodulation filter is not required in this work as the feedback has to be taken from the power stage output and not the demodulation filter.



Parameters	Values
Rz	10Ω
Cz	1.13u
Lz	18u
Rsim	1MΩ
RLoad	4Ω
Cout	1.13u

Parameters	Values
Ron	36mΩ
Rd	1.13u
Lon	3.7uH
Rs	10Ω
Cs	470pF



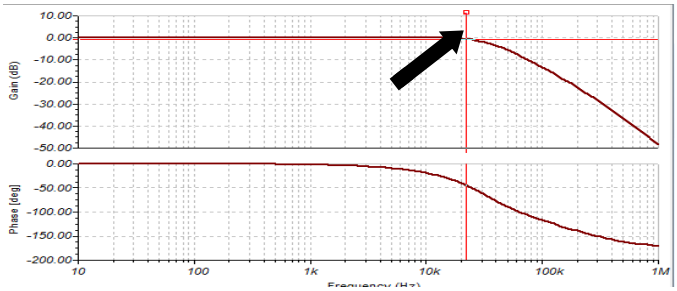


Figure 55: Power Stage Model in Simulink & Demodulation Filter

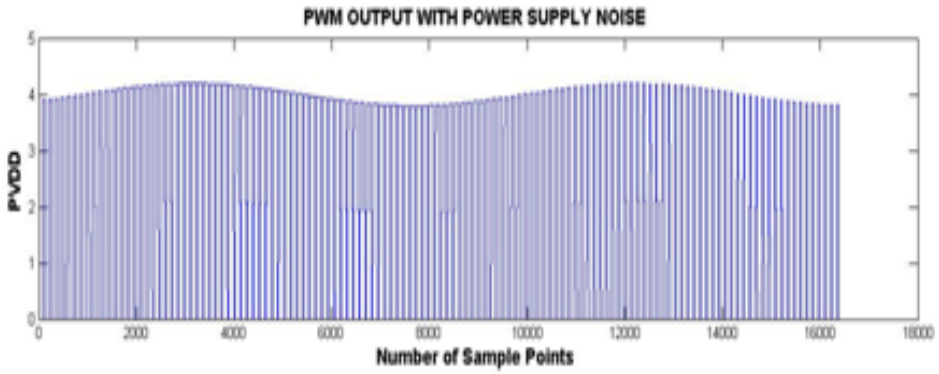


Figure 56: PWM with noise

The above plot shows the 500Hz noise overriding on the PWM generated from the Modulator (using an Audio input of 22 KHz). The spectrum for the same shows that the IMD products and the 500Hz ripple itself is seen to be reproduced in the audio band of interest. The IMD products are seen at 21.5 KHz and 22.5 KHz as expected from the result of the analysis of PS-IMD & PSRR.

$$V_{out}(t) = \frac{1}{2} \times M \times \sum_{m=0}^{M\max} A_m [\cos(\omega_r t + (m \times \omega_m t)) + \cos(\omega_r t - (m \times \omega_m t))]$$

$$IMD = \frac{\sqrt{2 \times \sum_{m=1}^{M} A_m^2}}{2(1 + A_0)}$$

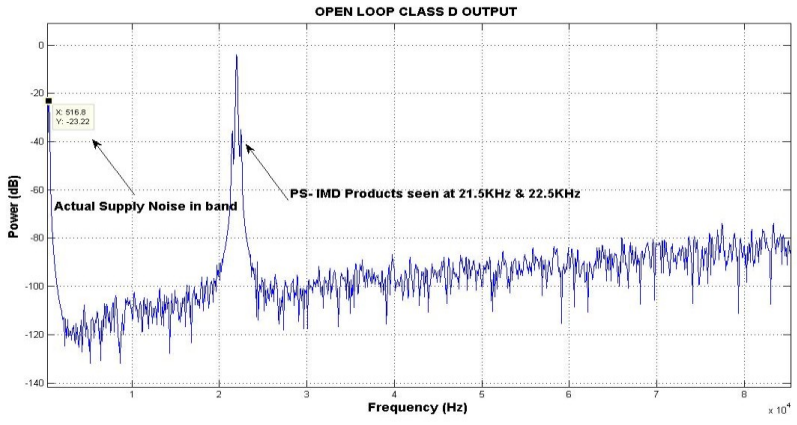


Figure 57: CLASS D o/p with noise

5.4 FEEDBACK STRATEGIES

Mostly available digital Class-D amplifiers can be termed as either “closed-loop” or“open-loop” systems based on the mechanisms that have been developed to provide real-time feedback to reject unwanted tones (ripple) generated by the power supply, or the noise coupled onto the power rail due to ripple currents flowing through large decoupling capacitors. Since the high sides of the power MOSFETs are connected directly to the power supply rail, all tones and associated harmonics generated on the power supply rail are coupled onto the output of the audio amplifier channel. The ripple on the power supply can either be seen as a tone itself in the audio band or it can be seen as modulated side bands around the audio tone. The PSR and PS-IMD were of key focus for this work. There are different feedback strategies involved in class D amplifiers. It can be either feedback around the power stage or feedback directly into the digital domain or it can be also divided into two parts (either feedback of amplitude information or feedback of Timing information.

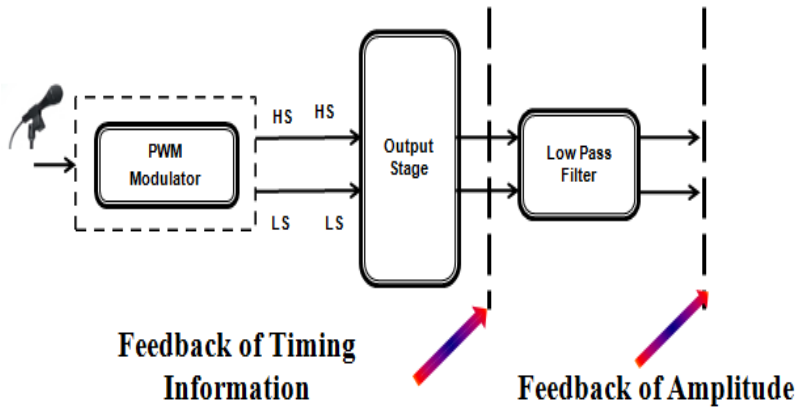


Figure 58: Different Feedback Strategies

A closed loop class D amplifier can have the ability to correct for both PWM generation based distortion and power supply perturbations.

However, the PWM based distortion requires a pre-distortion circuit which can very well predict the distortion and non linearities inherent in the PWM generator. In this work most of the focus was on the know power supply noise and means to get rid of it or at least reduce its amplitude in the output spectrum of the modeled Class D. The open loop Class D model and the performance of the CLASS D modeled is as shown below. It can be seen that a ripple on power supply of 500Hz is seen at the o/p along with the IMD products as sidebands to the input tone of 22 KHz audio. Power Supply Ripple: **100mV@ 500Hz**; Fin: **22 KHz**; PS - IMD seen at **-35dB**, PS ripple @ 500Hz: **-23.22dB**

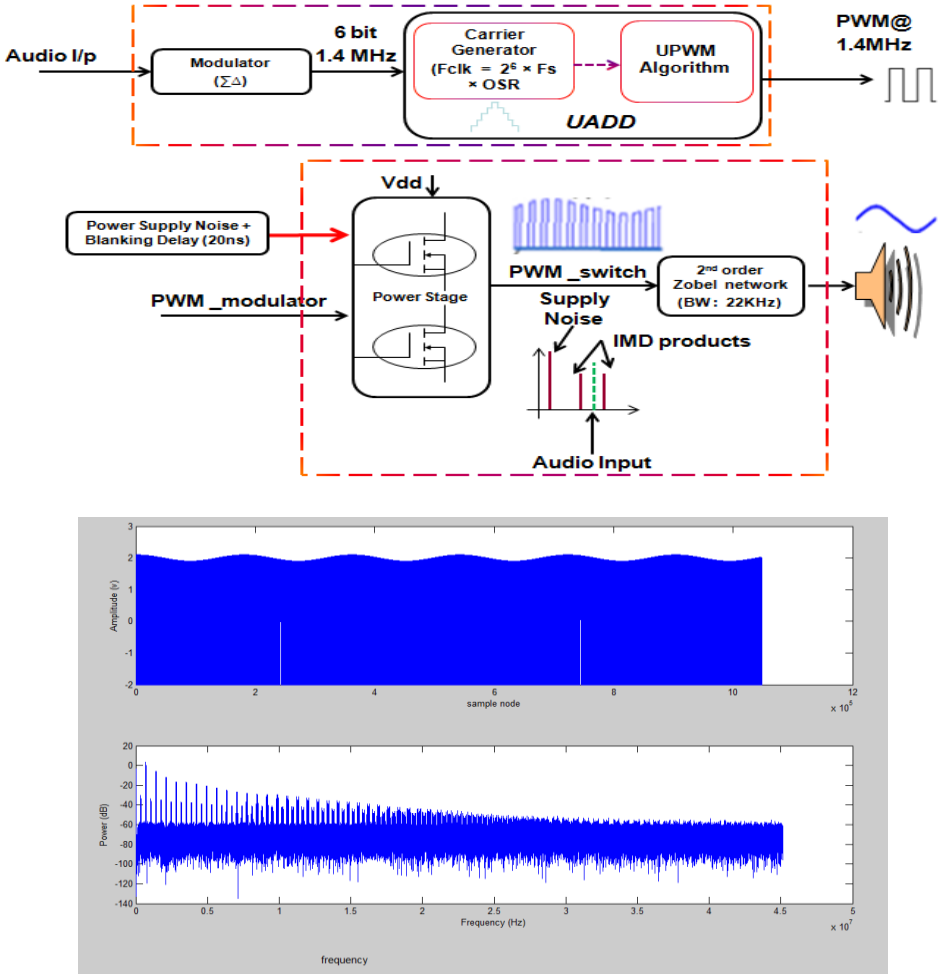


Figure 59: Open Loop Class D modeled in Simulink

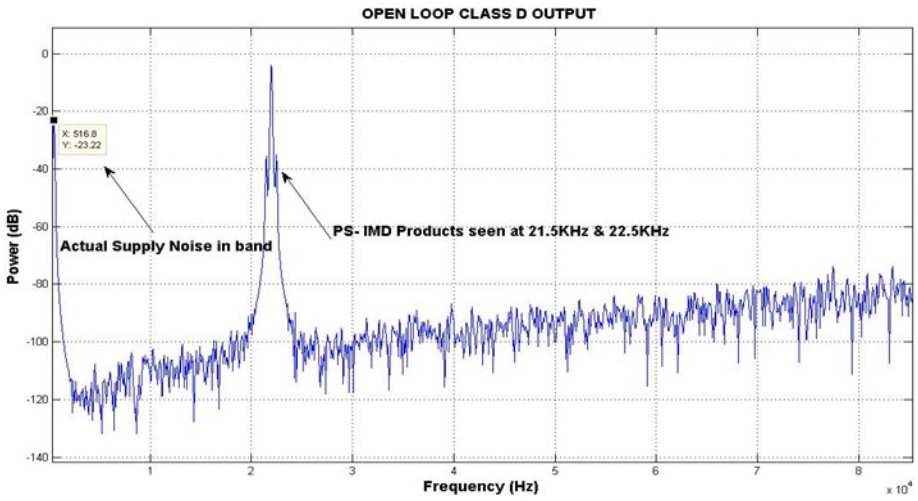


Figure 60: Open Loop CLASS D performance (with PSR & PS-IMD)

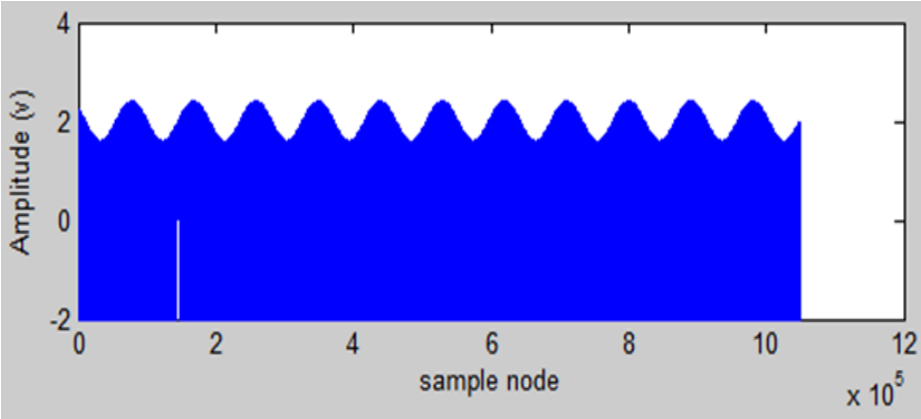


Figure 61: PWM o/p with Power Stage Noise couple

5.4.1 FEEDBACK INTO DIGITAL DOMAIN

One method of feedback into the digital domain is to use an ADC which can scale down the error in digital domain. The ADC based feedback method linearity and performance will be limited by the ADC BW and resolution, however if the ADC can sample the error signal as fast as twice the PWM switching frequency then the error can be easily cancelled or reduced. Below shown is the feedback topology developed for the class D model.

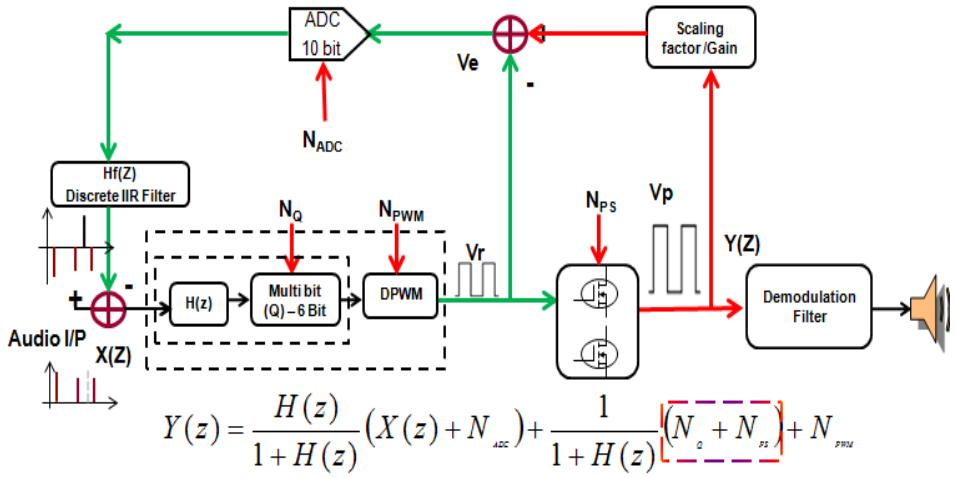


Figure 62: Feedback directly into the Digital Domain

In this model a 10 bit ADC is used to quantize/digitize the error signal and then it is passed through a discrete IIR filter and finally it is downsampled in order to be subtracted at the input. Below shown is the actual model implemented. Since the PWM signal generated at 1.411MHz hence the ADC needs to be at least sampling the error at 2.822 MHz.

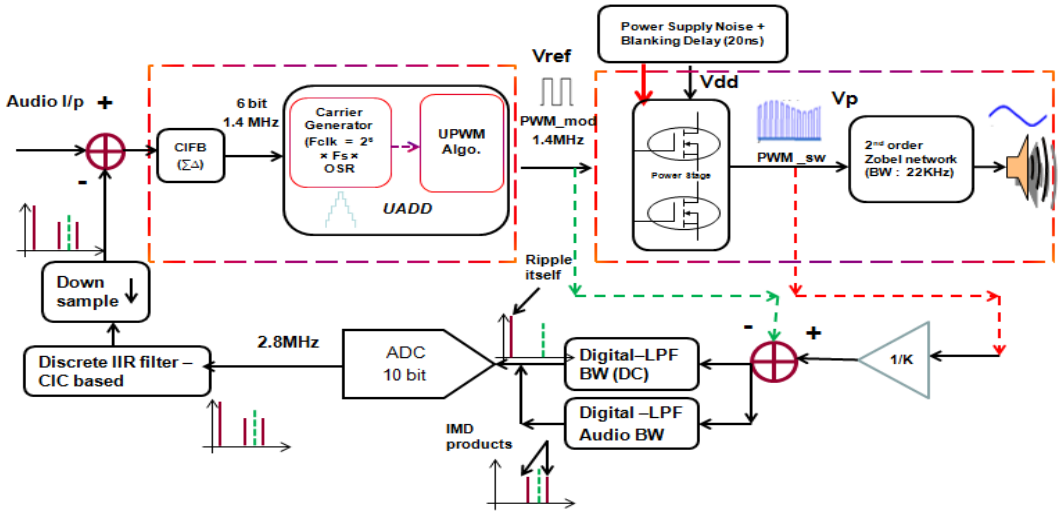


Figure 63: Closed Loop Architecture

The error signal and the IMD products can be easily seen prominent in the extracted error signal.

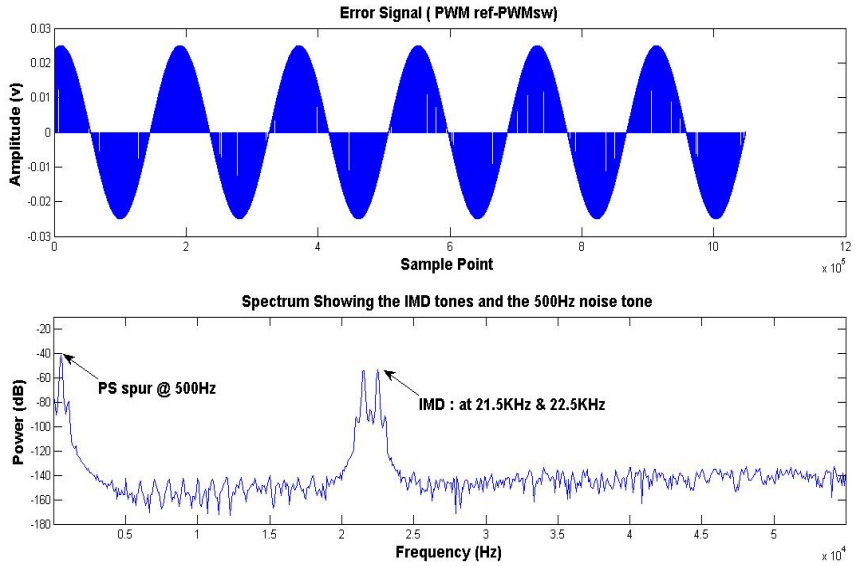


Figure 64: Extracted Error Signal (PWMscaled_SW-PWMref)

After the Error signal is generated, the error signal is digitized using an ideal ADC (10 bit) at more than twice the PWM frequency (5.4 MHz) followed by a Discrete FIR filter.

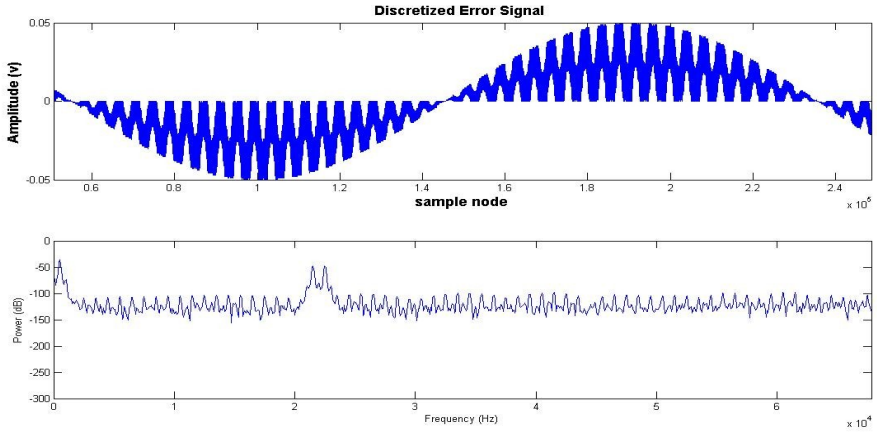


Figure 65: Discretized Error Signal

The discretized error is then down sampled by the OSR of the Modulator used so that it can be subtracted from the incoming signal. The input to the modulator after the feedback feeding back into the summer before the modulator is shown

below. This is more of a pre distorted input to the CLASS D which cycle over cycle will help in reducing the amplitude of the IMD and the noise spur itself. The improvement in the PSR and the PS-IMD reduction is shown below for a running closed Loop CLASS D amplifier model.

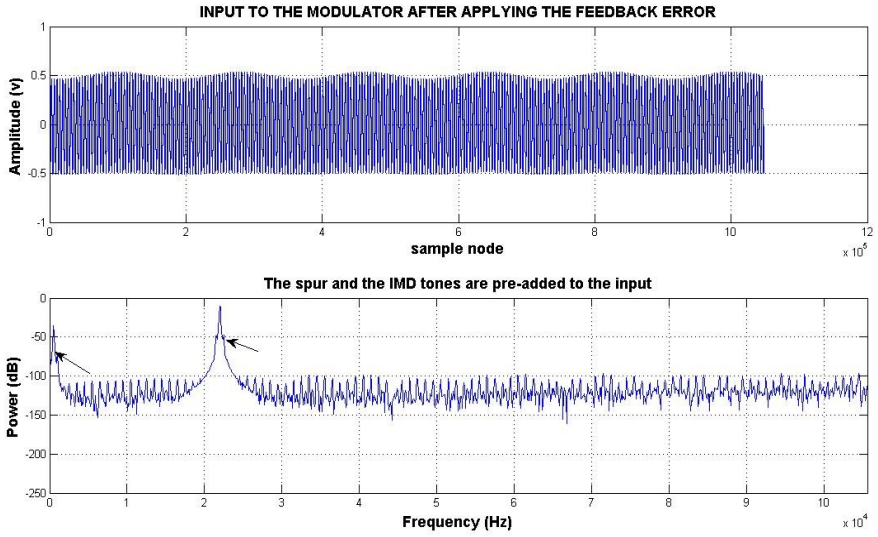


Figure 66: Pre-distorted Input

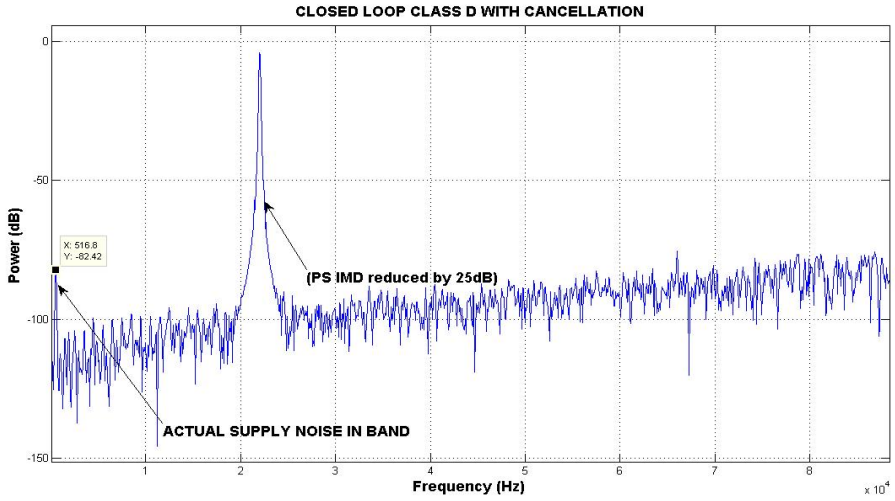


Figure 67: Closed Loop CLASS D performance (with PSR & PS-IMD)

Power Supply Ripple: 100mV@ 500Hz; Fin: 22 KHz PS - IMD seen at -**55dB**: PS ripple @ 500Hz: **-80dB**

5.4.2 DUTY RATIO CORRECTION BASED FEEDBACK

Another type of feedback topology was investigated, analyzed and implemented. This was based on feedback around the Power stage only. As discussed previously, two PWM pulse train can be considered same if their effective duty ratio are the same.

In short the integrated value of one cycle of a PWM over the switching period is a measure of the energy stored in it and it is dependent on its duty cycle, so if two PWM pulse integrated over a switching period gives different effective duty ratio value then the Pulses have different energy. Effective Duty Ratio determines whether two switching waveforms are identical or not even if their shapes are different.

A power supply stage modeled with non idealities & Supply Noise can be considered to have duty ratio error as Edist. It is assumed here that the modulator generates a PWM reference signal which does not have any distortion whereas the PWM output stage generates the Pulse amplitude and Pulse timing errors which owing to its supply fluctuations and dead time errors generated in the switching MOSFET.

If the Modulator output is considered as golden reference and the duty ratio of the same can be used to reconstruct the PWM cycle over cycle then the PWM stage related errors will slowly and gradually fade away. The basic block diagram for this implementation is shown below.

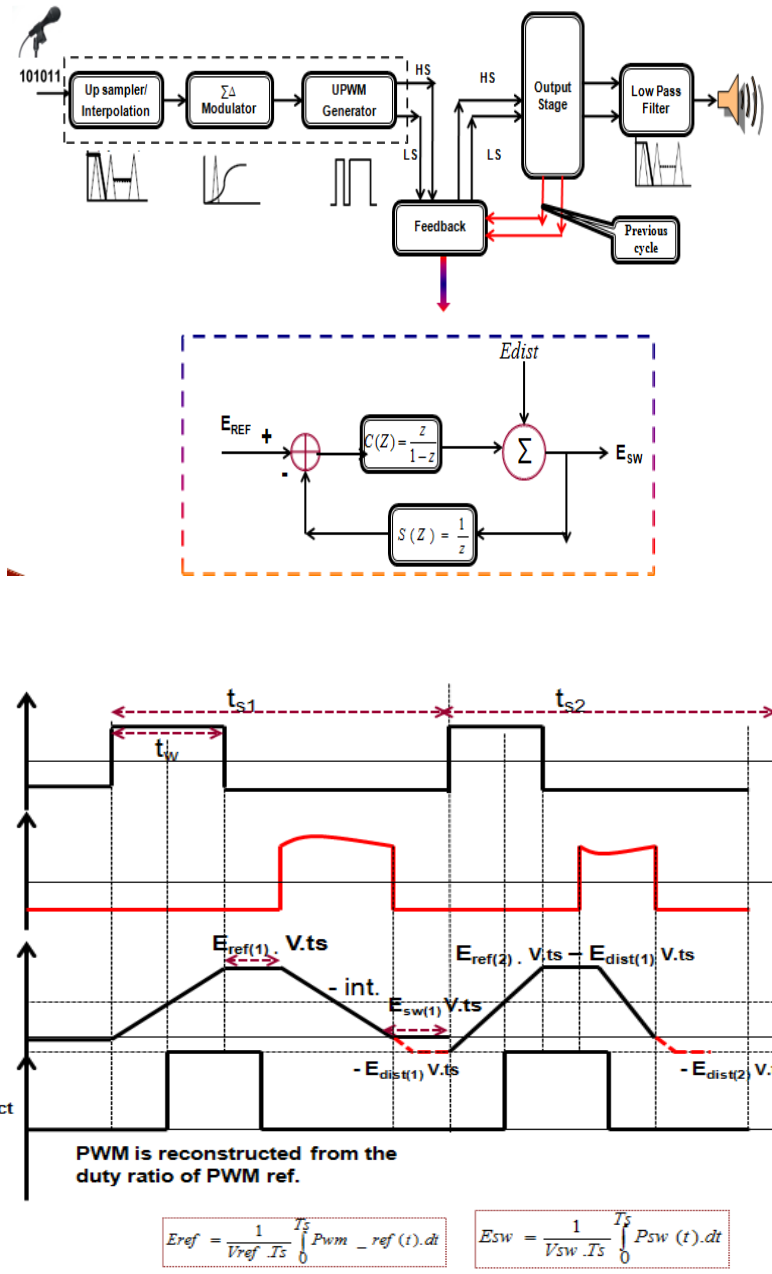


Figure 68: Block level of Feedback methodology

The hardware implementation for this kind of feedback can be done using integrator, comparator and an error correction circuit. However in simulink a replicate model and algorithm was developed. Duty ratio calculation for each switching period of the PWM reference & the PWM switch was done using

MATLAB function and was stored in separate vector. The difference in the duty ratio of the PWMref and PWMsw was also stored in a separate

$$Esw = \frac{1}{Vsw.Ts}\int_{0}^{Ts} Psw(t).dt \qquad Eref = \frac{1}{Vref.Ts}\int_{0}^{Ts} Pwm\_ref(t).dt$$

array and was used as Edist in the above shown block diagram. This vector was then passed through a feedback block as shown above. The equation shown below was used as a basis for calculating normalized duty ratios. An embedded MATLAB code (listed in Appendix A) was used to reconstruct the PWM from duty ratios calculated.

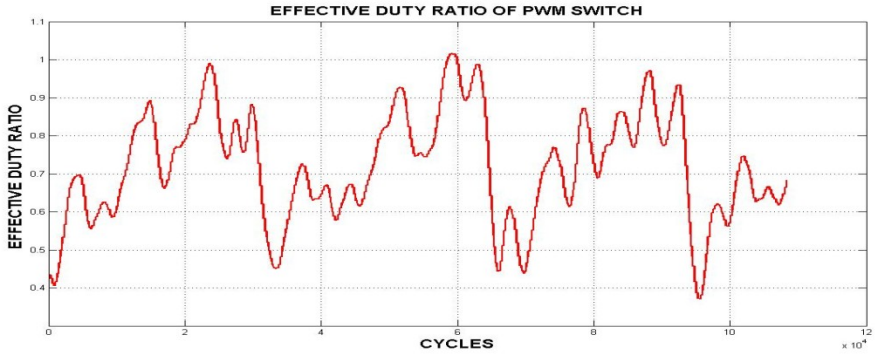


Figure 69: Duty Ratios calculated for PWM switch out

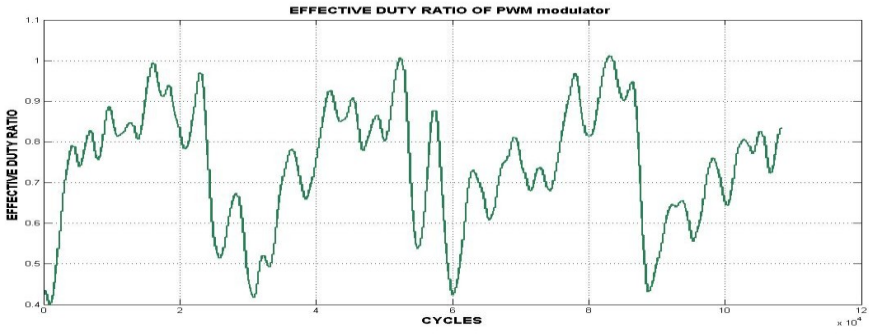


Figure 70: Duty Ratios calculated for PWM modulator

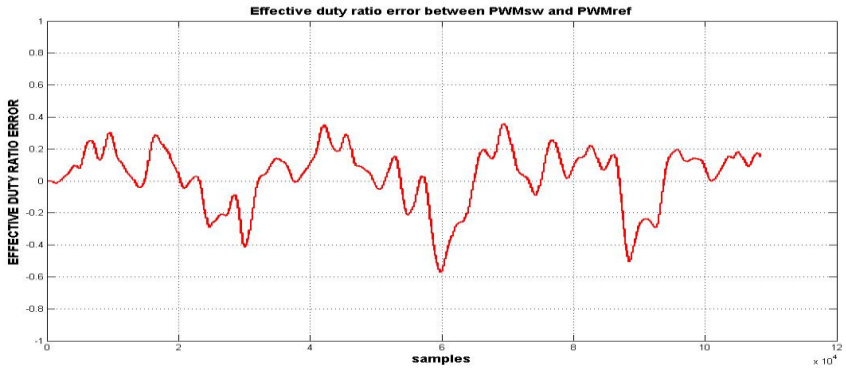


Figure 71: Duty Ratio error

From the plots shown above it might seem that both the plots are same, this is due to the fact that lot of samples were taken. This error in the duty ratio reduces from cycle over cycle thereby equalizing the Duty ratio of the PWM modulator and the PWM switch. However this implementation did not give successful results in terms of cycle to cycle error correction. The different blocks used for trying to implement this model was a PWM to duty ratio calculator & an Algorithm for PWM reconstruction from the corrected duty ratios.

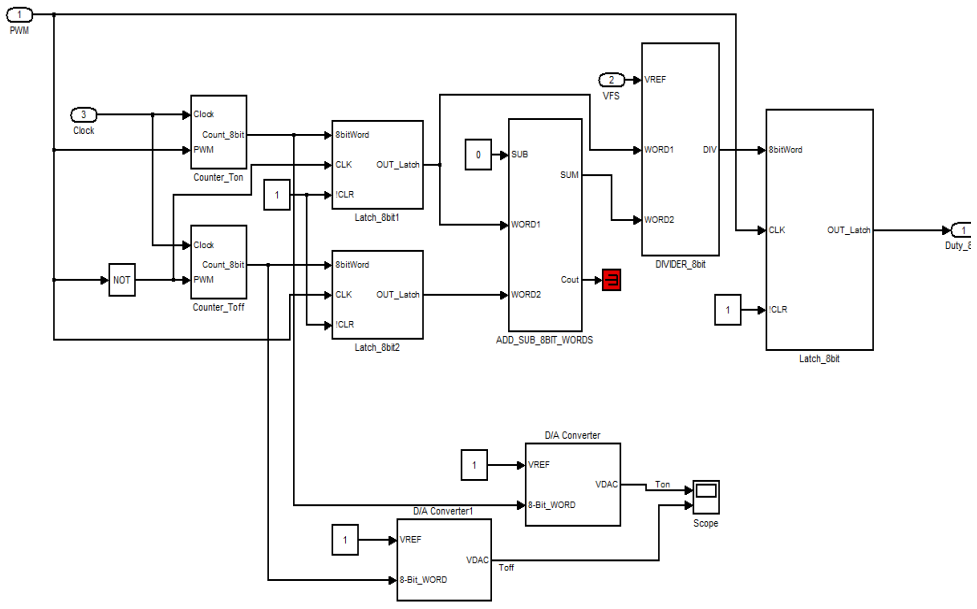


Figure 72: PWM to Duty Ratio Calculator

Few more result plot of a closed loop vs. open loop Class D PSR and PS-IMD performance improvement when there are multiple spurs on power supply. The plots are all zoomed in to the audio band till 22 KHz. The overall the output of a Class D amplifier will have lot of harmonics in frequency domain since it is PWM modulated but only the baseband signal bandwidth is inspected for Signal, noise and distortion products.

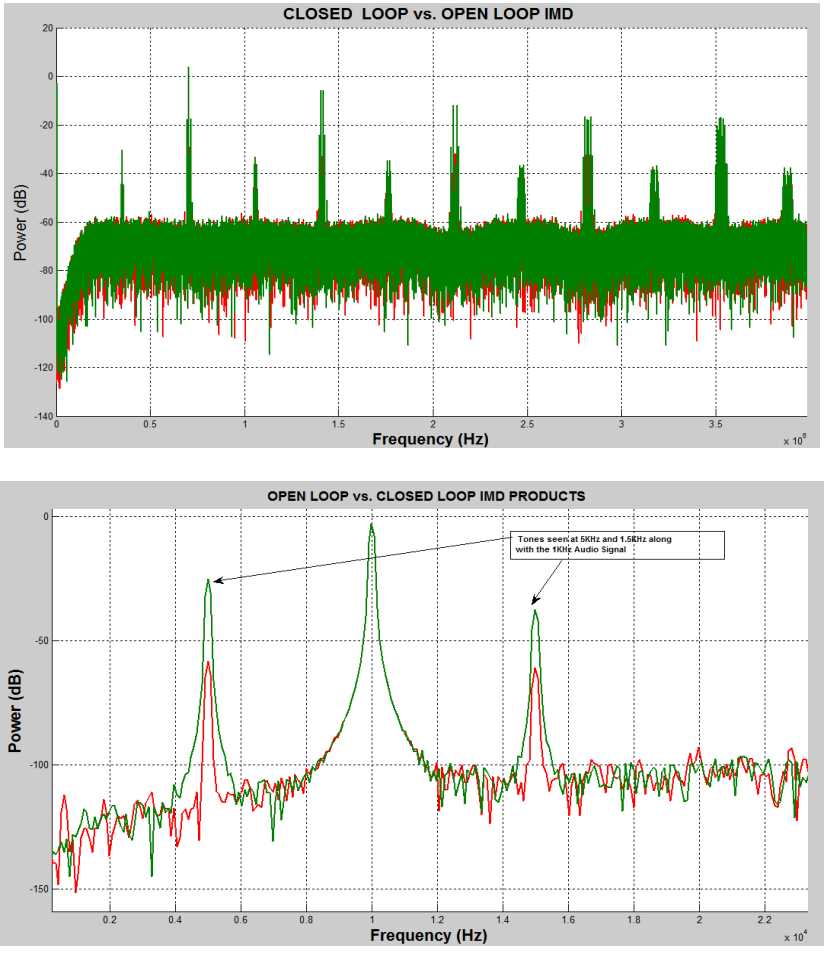


Figure 73: PS-IMD plot for the Class D Model

Chapter 6

CONCLUSION

A model of the Class-D amplifier including the modulator, the power stage, demodulation filter and the feedback loop has been simulated in MATLAB & SIMULINK for performance verification. To accurately emulate the non-ideal nature of the power stage, electrical circuit component models provided by the SimPowerSystems toolkits are used.

Feedback loop in class D amplifier is extremely important as it can be used to counteract the effect of power stage non-idealities and power supply noise so that low distortion level can be achieved without the need of well designed power stage, and expensive power supplies.

The main focus of this work was to improve the PSRR & PS-IMD of a CLASS D by feedback techniques. In order to achieve that a good amount of work was put into the modeling of the modulator, PWM generator, Power stage with Non idealities and demodulation filter for building a CLASS D which can be tested in open loop and closed loop configuration for comparison. Uniform AD modulation based Double sided Sampling algorithm was also implemented for minimizing distortion in the PWM generation method for the Class D.

Two types of Feedback techniques were proposed:

- The first one involves the use of feedback around the Power stage without involving the modulator.
- The second one is based on feeding the discretized error signal back into the modulator (pre-distortion).

However, only feedback into the digital domain based method have been giving good results for both slow varying and fast varying signal. Based on Simulation results, a closed loop versus Loop CLASS D PSR have shown improvement of about 30-40dB and PS-IMD of 30dB.

Audio Tone	PS spur	Open Loop (dB)		Closed Loop (dB)	
		PSR	PS-IMD	PSR	PS-IMD
2KHz , -3.2dB	500Hz , 20mV	-43	-54	-83	-70
5KHz , -3.2dB	500Hz , 50mV	-35	-47.4	-87.9	-72
10KHz,-3.2dB	2KHz , 50mV	-35.4	-47.18	-76	-74
22KHz -3.2dB	1KHz , 50mV	-35.9	-47	-76	-67
10KHz,-3.2dB	500Hz , 100mV	-29.4	-41	-82	-63.72
10KHz ,-3.2dB	400Hz,200mV	-23.72	-35.71	-78	-57

Table 2: PSR and PS-IMD (open loop vs. close loop) CLASS D

FUTURE SCOPE

The digital class D amplifier is an interesting solution to increase the efficiency of embedded systems such as mobile phones, PDAs etc. However, this solution is not good enough in terms of linearity and power supply rejection. An efficient control is needed to correct the error sources incorporating a global feedback. There can be different feedback strategies for a digital CLASS D depending on from where you extract the feedback signal; it can be from the power stage or it can be from the demodulation filter. Digital feedback control referenced to the digital source whereby the sampling cross points are changed seems to be efficient method but it will add significant delay into the overall system. The delay is problematic as the total delay allowed within the control loop is limited by the required phase margin, and thus the bandwidth. Thus, one scope of having this delay dealt with would be to use the A/D converter on the demodulated audio o/p hence within the audio bandwidth and thereby relaxing the delay requirement in the control loop. The road lies ahead open with the question that whether to use a digital control system can be implemented successfully for re-timing of the distorted pulse and compensate for errors from power stage & filter errors or use a high resolution high BW A/D . There will always be a trade off in terms of performance, cost and ease of implementation.

REFERENCES

[1] J. G. Kenney and L. R. Carley, "Design of Multibit Noise-Shaping Data Converters," Analog Integrated Circuits and Signal Processing, vol. 3, no. 3, pp. 259-272, May1993.

[2] R. Schreier and G. C. Temes, Understanding Delta-Sigma Data Converters. Wiley - IEEE Press, 2004.

[3] “A High Performance Class-D Power Amplifier using Error Feedback Architecture” Chintan Trehan and Kwong S. Chao

[4] R.E. Hiorns, R.G. Bowman, M.B. Sandler, “A PWM DAC for digital audio power conversion: from theory to performance,” Int. Con. On A/D and D/A Conversion, pp. 142-147, 1991.

[5]Jeong, J.H., Seong, H.H., Yi, J.H., Cho, G.H., “A class D switching power amplifier with high efficiency and wide bandwidth by dual feedback loops,” Consumer Electronics, Proceedings of International Conference,

[6] I. Mosely, P. Mellor, and C. Bingham, "Effect of Dead Time on Harmonic Distortion in Class-D Audio Power Amplifiers," Electronics Letters, vol. 35, no. 12, pp. 950-952, June 1999.

[7] M. Berkhout, "A Class-D Output Stage with Zero Dead Time," in Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International, 2003, pp. 134-135.

[8] K. Nielsen, “PEDEC-A novel pulse referenced control method for high quality digital PWM switching power amplification,” in Proc. IEEE Power Electronics Specialists Conf., vol. 1, 1998, pp. 200–207.

[9] “Feedback strategies in digitally controlled class-D amplifiers “ R. Esslinger G. Gruhlerand R.W. Stewart , Audio Engineering Society Convention Paper 5828 Presented at the 114th Convention 2003 March 22–25 Amsterdam, The Netherlands

[10] “Double Edge Trailing PWM Based Full Digital Audio Amplifier Design”
Seo Weon Heo and Jongsun Kim, Members, IEEE School of Electronic and Electrical Engineering, Hongik University, Seoul, Korea

[11] J. S. Chang, M. T. Tan, Z. Cheng, and Y. C. Tong, “Analysis and design
Of power efficient CDA output stages,” IEEE Trans. Circuits Syst. I, Fundamental. Theory Appl., vol. 47, no. 6, pp. 897–902, Jun. 2000.

[12] “Modeling and Technique to Improve PSRR and PS-IMD in Analog PWM Class-D Amplifier “Tong Ge and Joseph S. Chang

[13] “Waveform Distortion and Correction Circuit forPWM Inverters with Switching Lag-Times” YOSHIHIRO MURAI, ASSOCIATE MEMBER, IEEE, TOMOFUMI

WATANABE, AND HARUMITU IWASAKI, IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, VOL. IA-23, NO. 5, SEPTEMBER/OCTOBER 1987

[14] System Design Considerations for True Digital Audio Power Amplifiers, Kim Madsen and Ron Alexander TI Copenhagen

[15] The application of direct digital feedback for amplifier system control Audio Engineering Society Convention Paper 7226 Presented at the 123rd Convention 2007 October 5–8 New York, NY, USA

[16] E. Gaalaas, B. Liu, N. Nishimura, R. Adams, and K. Sweetland, “Integrated Stereo ΔΣ Class D Amplifier”, Solid-State Circuits, IEEE Journal of, vol. 40, no. 12, pp. 2388.2397, Dec 2005.

[17]“A hybrid modulation scheme for digital Class D amplifier modulators” Circuits and Systems for Medical and Environmental Applications Workshop (CASME), 2010 2nd

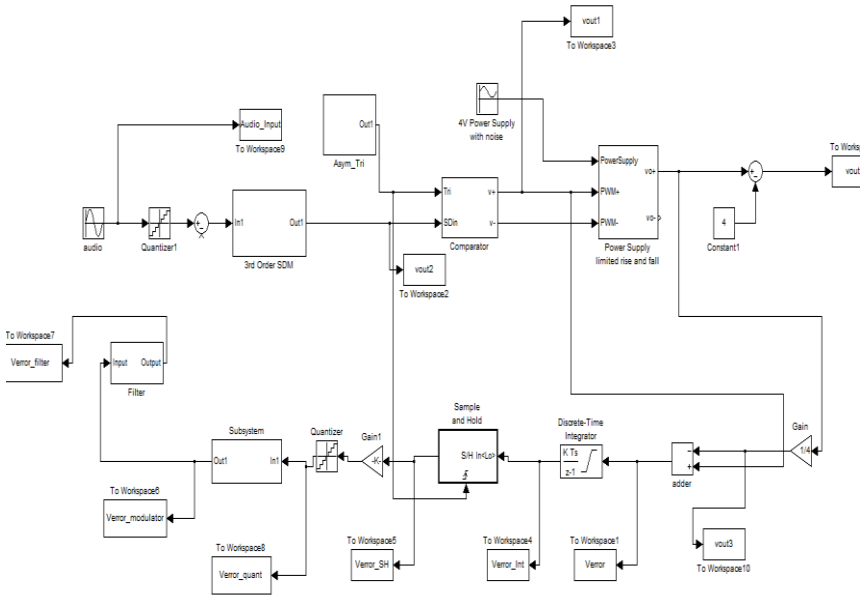
[18] P.T. Krein, “All-digital audio amplifier,” Ph. D. dissertation, University of Illinois at Urbana-Champaign, Urbana-Champagne, America, 2001.

[19]"KEY DESIGN CONSIDERATIONS FOR HIGH QUALITY AUDIO" ADC PERFORMANCE Duncan Macadie, Wolfson Microelectronics

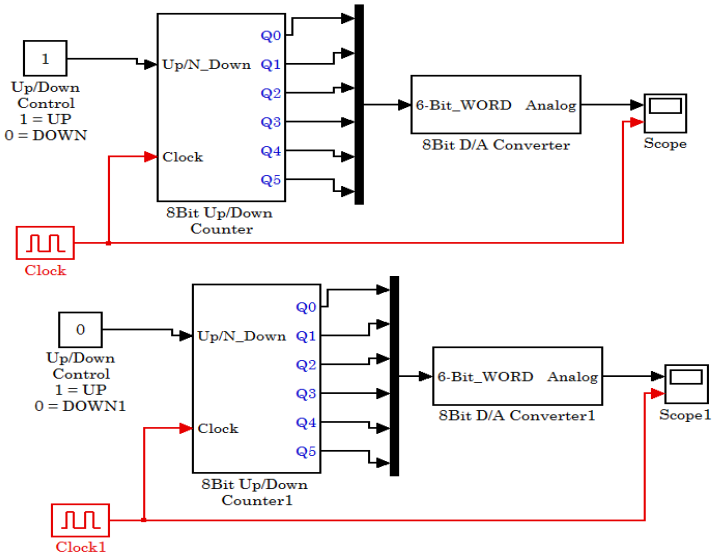
APPENDIX A

SIMULINK MODELS

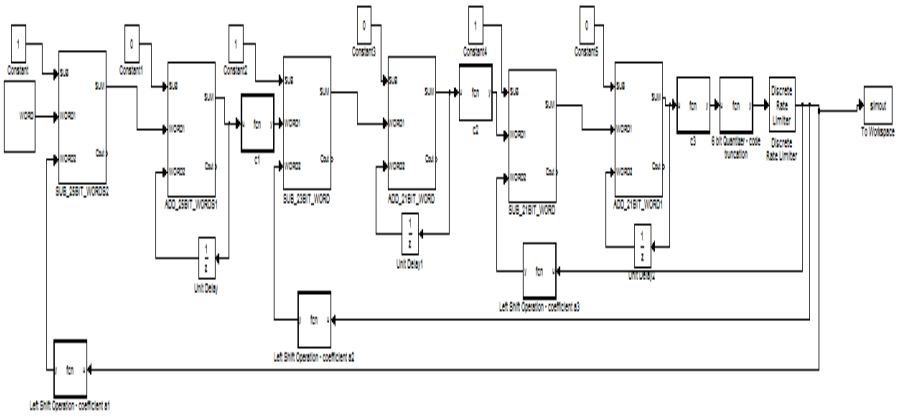
Closed Loop Class D with Error Extraction

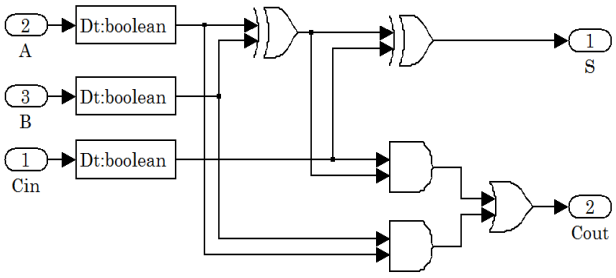


Counter for DPWM generator Block

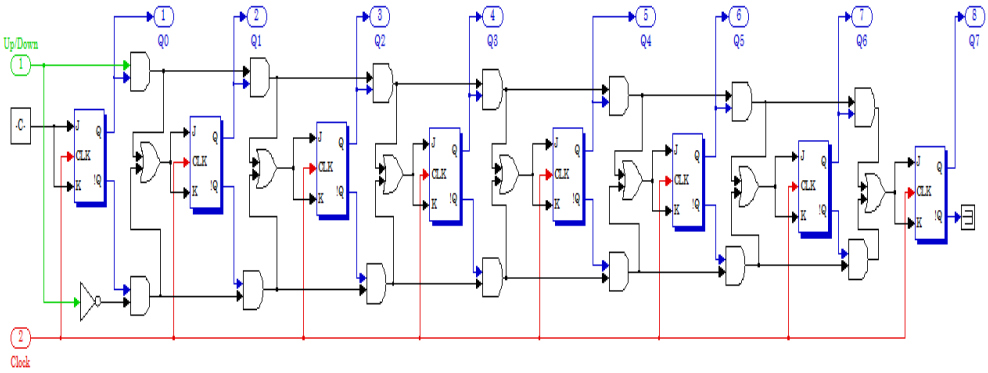


Structure of a Delta Sigma Modulator: Bit reduction using Accumulator, D Flip Flop and truncator.

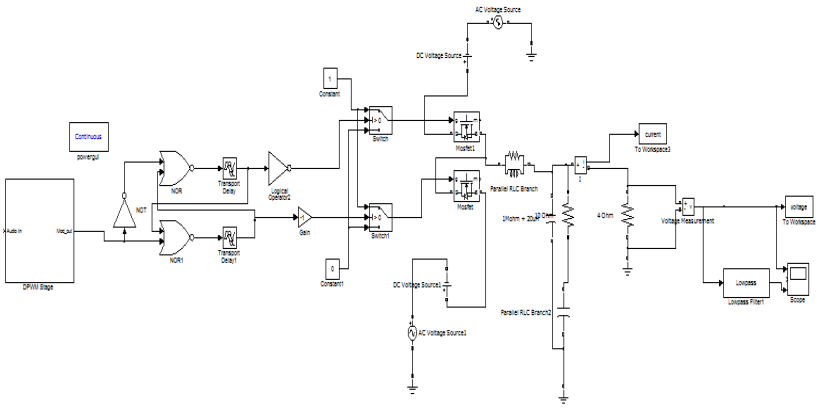




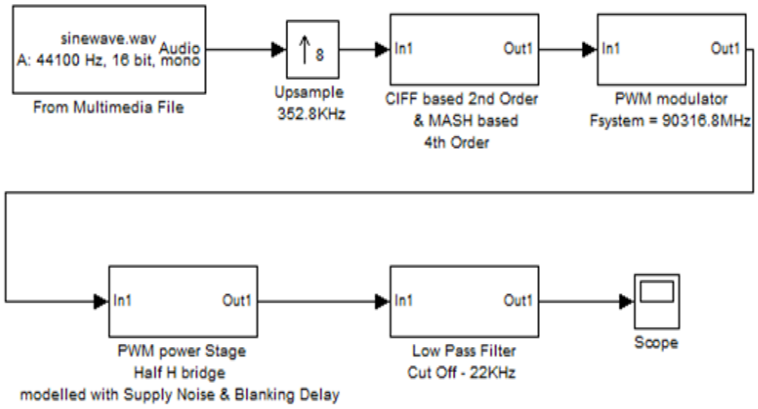
Bidirectional Counter using the JK flip-flops



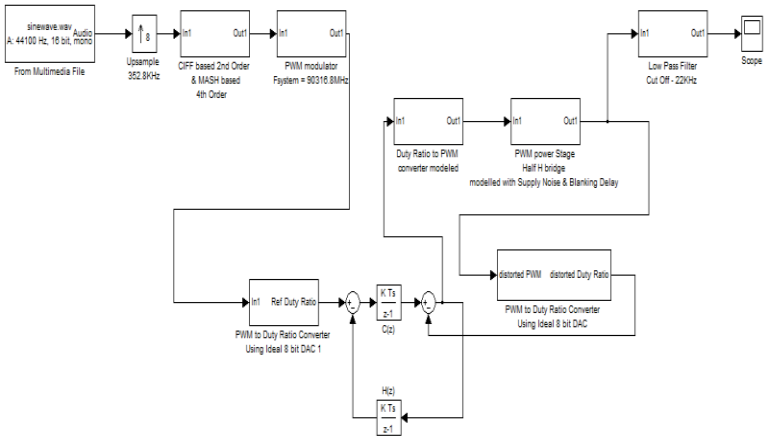
Power Stage Non-Idealities Model



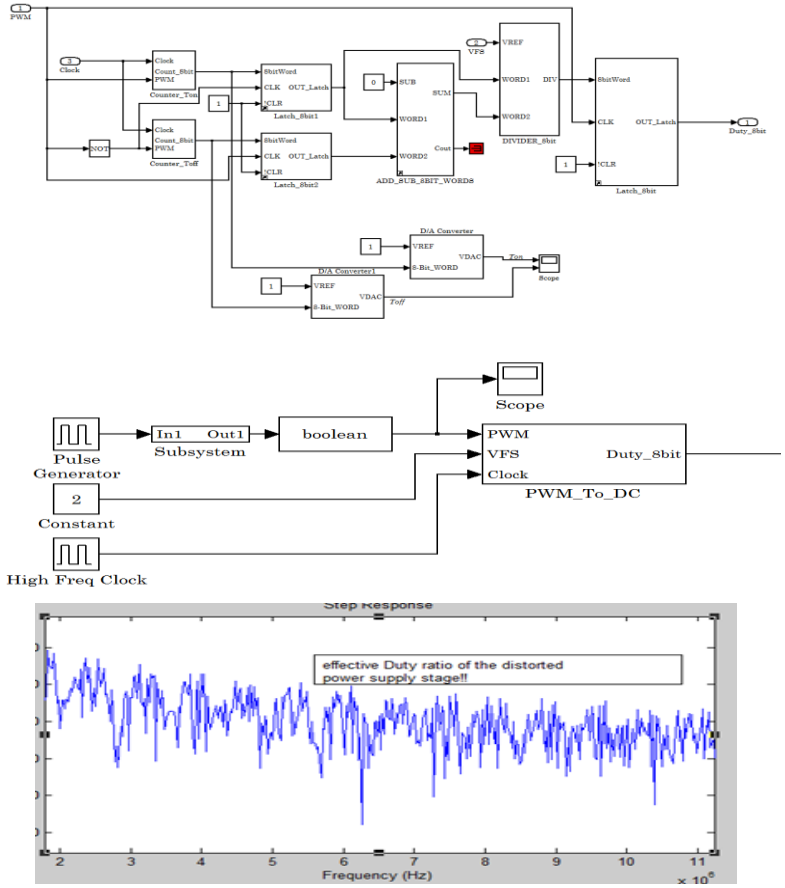
Open Loop Implementation



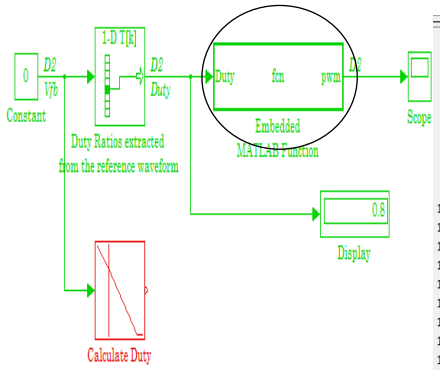
Effective Duty Ratio Based Implementation – Closed Loop



PWM Duty Ratio Extractor

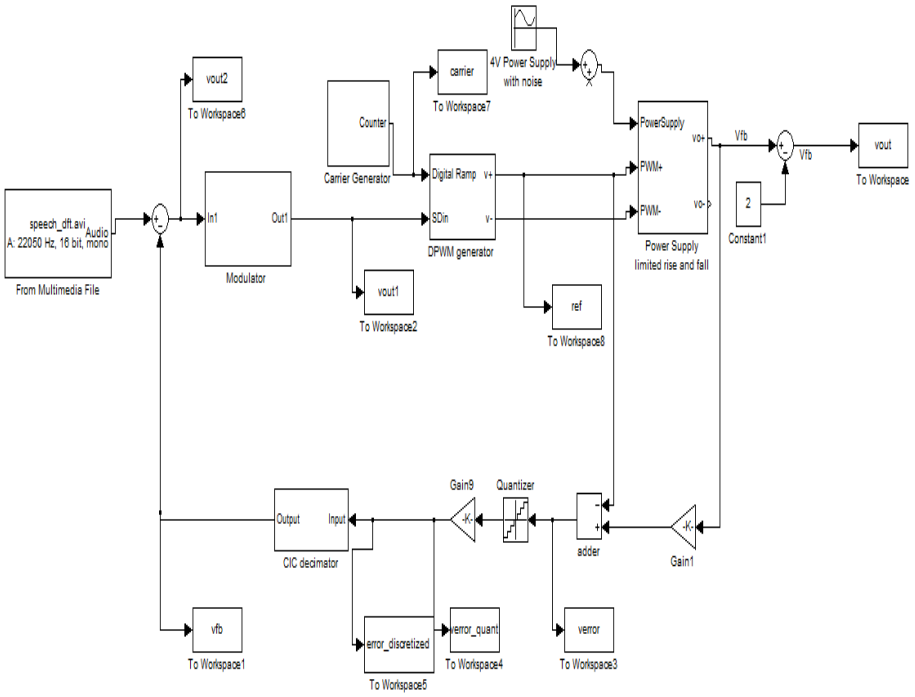


PWM Generator from Duty Ratio – Closed

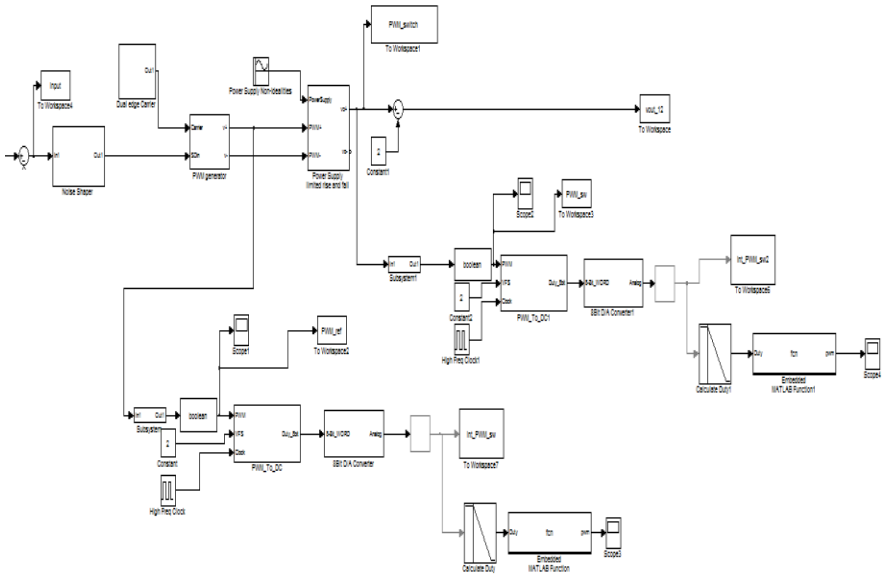



```
function pwm = fcn(Duty)
%#codegen
persistent counter T_on;
if isempty(counter)
    counter = 0;
    T_on = 1;   %Start in ON mode.
end

counter = counter+1;

if (Duty > 0)
    if T_on                          % Are we in on state?
        if (counter/100 >= Duty)        % Finished One cycle?
            counter = 0;
            T_on = 0;
        end
    else                             % In Off state
        if (counter/100 >=  (1-Duty))
            counter = 0;
            T_on = 1;
        end
    end

    if T_on
        pwm = 1;
    else
        pwm = 0;
    end
else
    pwm = 0;
end
```

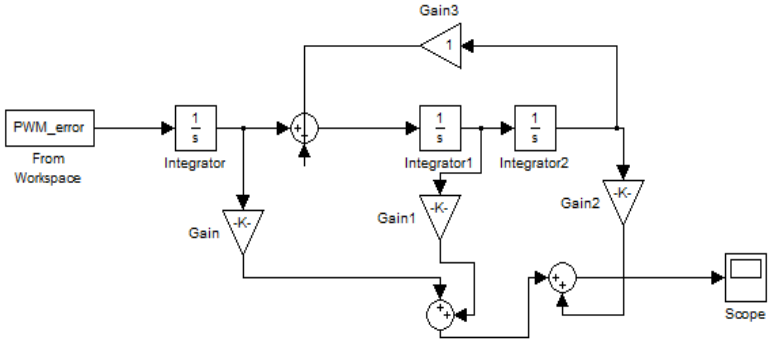
Class D Closed Loop Model



CLASS D Closed Loop Model Using Duty Ratio Correction



Integrating Error Amplifier



APPENDIX B

MATLAB ALGORITHMS & CODES

Code for CIC decimation filter

```
% Moving Average filter
N = 10;
xn = sin(2*pi*[0:.1:10]);
hn = ones(1,N);
y1n = conv(xn,hn);

% transfer function of Moving Average filter
hF = fft(hn,1024);
plot([-512:511]/1024, abs(fftshift(hF)));
xlabel('Normalized frequency')
ylabel('Amplitude')
title('frequency response of Moving average filter')

% Implementing Cascaded Integrator Comb filter with the
% comb section following the integrator stage
N = 10;
delayBuffer = zeros(1,N);
intOut = 0;
xn = sin(2*pi*[0:.1:10]);
for ii = 1:length(xn)
% comb section
combOut = xn(ii) - delayBuffer(end);
delayBuffer(2:end) = delayBuffer(1:end-1);
delayBuffer(1) = xn(ii);

% integrator
intOut = intOut + combOut;
y2n(ii) = intOut;
end

err12 = y1n(1:length(xn)) - y2n;
err12dB = 10*log10(err12*err12'/length(err12)); % identical outputs
close all

% Implementing Cascaded Integrator Comb filter with the
% integrator section following the comb stage

N = 10;
delayBuffer = zeros(1,N);
intOut = 0;
xn = sin(2*pi*[0:.1:10]);
for ii = 1:length(xn)
% integrator
intOut = intOut + xn(ii);

% comb section
combOut = intOut - delayBuffer(end);
delayBuffer(2:end) = delayBuffer(1:end-1);
delayBuffer(1) = intOut;
```

```
y3n(ii) = combOut;

end
err13 = y1n(1:length(xn)) - y3n;
err13dB = 10*log10(err13*err13'/length(err13)) % identical output

For decimation, having the CIC filtering before taking every other sample
D = 8; % decimation factor
N = 64; % delay buffer depth
delayBuffer = zeros(1,N); % init
intOut = 0;
xn = sin(2*pi*[0:.1:10]);
y6n = [];
for ii = 1:length(xn)
comb section
combOut = xn(ii) - delayBuffer(end);
delayBuffer(2:end) = delayBuffer(1:end-1);
delayBuffer(1) = xn(ii);

integrator
intOut = intOut + combOut;
y6n = [y6n intOut];

end
y6n = y6n(1:D:end); % taking every other sample – decimation

For efficient hardware implementation of the CIC filter, having the
integrator section first, decimate, then the comb stage
Gain : Reduced the delay buffer depth of comb section from N to N/D
D = 8; % decimation factor
N = 64; % delay buffer depth
delayBuffer = zeros(1,N/D);
intOut = 0;
xn = sin(2*pi*[0:.1:10]); % input
y7n = []; % output
for ii = 1:length(xn)
integrator
intOut = intOut + xn(ii);

if mod(ii,2)==1
comb section
combOut = intOut - delayBuffer(end);
delayBuffer(2:end) = delayBuffer(1:end-1);
delayBuffer(1) = intOut;
y7n = [ y7n combOut];
end

end
err67 = y6n - y7n;
err67dB = 10*log10(err67*err67'/length(err67)
```

UPWM algorithm for calculating the Duty cycle

```
clear all;
M =1024;      % number of samples
Fs = 352.8e3; % carrier freq, or switching freq
T = 1/Fs;      % carrier period
f0 = 6.67e3;      % input sine wave freq
N =6;        % word length (in bits)
A = 2^N-1;     % quantized amplitude of input
A0 = 1;      % modulating index
K = 4;
a = zeros(1, K);

s0 = A0*sin(2*pi*f0*((0:M-1)*T));
tau = zeros(1, M-7);
pwmout = zeros(1, M-7);

s = s0/2;
p = s0.^2;
 q = s0.^3;
 r = s0.^4;
 k =4:M-4;
  ds = A0*(2*pi*f0*T)*cos(2*pi*f0*T*(0:M-1));
  ds2 = -A0*(2*pi*f0*T)^2*sin(2*pi*f0*T*(0:M-1));
  ds3 = -A0*(2*pi*f0*T)^3*cos(2*pi*f0*T*(0:M-1));


 a = (1/60*(s(k+3)-s(k-3)) -3/20*(s(k+2)-s(k-2)) + 3/4*(s(k+1)-s(k-1)));
 b = ((1/90*(s(k+3)+s(k-3))-3/20*(s(k+2)+s(k-2)) + 3/2*(s(k+1)+s(k-1)) -
49/18*s(k)))/2;
 c = ((-1/8*(s(k+3)-s(k-3)) + (s(k+2)-s(k-2)) - 13/8*(s(k+1)-s(k-1))))/6;
 tau(k-3) = 1/2 + s(k).*((1+a).*(1+a.^2) + s(k).*(b.*(1+3*a) + s(k).*c));

% tau(k-3) = (1/2 + 1/2*s(k).*(1+a/2 + a.^2/4 + s(k).*b/8 + a.^3/8 + 3/16*s(k).*a.*b
+ 1/48*s(k).^2.*c) ;  for unscaled a, b, c

 d = (1/60*(p(k+3)-p(k-3)) -3/20*(p(k+2)-p(k-2)) + 3/4*(p(k+1)-p(k-1)));
 e = ((1/90*(q(k+3)+q(k-3))-3/20*(q(k+2)+q(k-2)) + 3/2*(q(k+1)+q(k-1)) -
49/18*q(k)));
 f = ((-1/8*(r(k+3)-r(k-3)) + (r(k+2)-r(k-2)) - 13/8*(r(k+1)-r(k-1))));
 tau(k-3) = 1/2+s(k)+(d/8+e/48+f/(384));
 pwmout= round(tau*A);
 if 1
 clear a b c;
 pout = zeros((M-7)*2^N, 1);
 for i = 1:length(pwmout)
    pout((i-1)*2^N+1:i*2^N) = [ones(pwmout(i),1); zeros(2^N-pwmout(i),1)];
 end
 pspec = pout - mean(pout); % remove DC for spectrum analysis
 Pxx = fft(pspec.*kaiser(length(pspec),9.5));
```

```
 w = (0:length(Pxx)-1)*Fs*2^N/length(Pxx);
 K = 1:1000;
 hold on;
 stairs(w(K),(Pxx(K)));
figure(2);
 plot(w,Pxx);
 hold off;
 end

// Modulator Scaling and Optimization
% modulator design and scaling of coefficients

% % Design example for a
% order = 3;
% osr = 32;
% nlev = 64;
% f0 = 0;
% Hinf = 1.5;

form = 'CIFB';
osr = 32;
[a,g,b,c] = realizeNTF(adc.ntf,'CIFB');
b(2:end) = 0;
ABCD = stuffABCD(a,g,b,c,'CIFB');
ABCDs = scaleABCD(ABCD,65);
[NTFs STFs] = calculateTF(ABCDs);
[as,gs,bs,cs] = mapABCD(ABCDs,'CIFB');
% ABCDq = stuffABCD(as,gs,bs,cs,'CIFB');
aq = [1/512 1/256+1/512 1/128+1/256];
a1q = 1/512; a2q =1/256+1/512 ; a3q = 1/128+1/256;
gq = 0;
bq = [1/512 0 0 0];
cq = [1/4+1/16 1/2+1/4+1/32 63];
c1q = 1/4+1/16; c2q = 1/2+1/4+1/32 ;c3q = 63;
ABCDq = stuffABCD(aq,gq,bq,cq,'CIFB');
[NTFq STFq] = calculateTF(ABCDq);
hold on;
figure(1);
plotPZ(NTFq, 'm',10);
plotPZ(adc.ntf, 'b',10);
hold off;
f = linspace(0,0.5,1000);
z = exp(2i*pi*f);
figure(2);
hold on;
plot(f,dbv(evalTF(STFq,z)));
plot(f,dbv(evalTF(NTFq,z)));
ylabel('Amp (dB)');
xlabel('Normalized Freq');
hold off;
```

```
sigma_H = dbv(rmsGain(NTFq,0,0.5/32));
amp=[-100:5:-10,-10:0];
[snr,amp] = simulateSNR(NTFq,32,amp,0,64);
figure(3);
plot(amp,snr);

% Word lenght for the integrators
M = 0.5;
bit_integ1 = -log2((M*a1q)*sqrt(1.5 *(10^(-10))*osr));
bit_integ2 = -log2((M*a1q*c1q)*sqrt(.45*(10^(-10))*(osr^3)));
bit_integ3 = -log2((M*a1q*c1q*c2q)*sqrt(.077*(10^(-10))*(osr^3)))

// Interpolator
 %  Original time axis
fsup = fs*100;   %  Upsampled frequency
taxup = min(taxis)+[0:floor((length(g))*fsup/fs)-1]/fsup;  % Upsampled time axis
upsig = zeros(size(taxup));   %  Initialize array to accumulated interplolated points

%  Big loop steps through each new point to be interpolated
for k = 1:length(taxup)
   % Inner loop weights all original signal points with sinc values to get
   % and adds up the products to get the new point
   for n = 1:length(g)
      upsig(k) = upsig(k)+g(n)*sinc(fs*(taxup(k)-taxis(n)));
   end
end
% Plot original and upsmpled signal
plot(taxis,g,'r',taxup,upsig,'b')
xlabel('seconds')
ylabel('Amplitude')
title('Original signal in red, upsampled in blue')

% Single Sided Spectrum
% Windowing of the Data
% w=hanning(64);
% W=fft(w);
Y=upsig;


% FREQUENCY DOMAIN ANALYSIS

sig_fft= abs(fft(Y,N));
% sig_fft=sig_fft(1:NUP);
mx1=sig_fft/N;
mx1= mx1.^2;
mx1 = mx1.*2;
sig_fft_dB= 10*log10(mx1);
semilogx(sig_fft_dB);
f = (0:NUP-1)*fsup/N;
```

```
% figure(4);
% semilogx(f,sig_fft_dB);
% title('SEMILOG FFT plot of the Modulator Output')
% xlabel('Frequency')
% ylabel('Power in dB')

figure(5);
plot(f,sig_fft_dB);
title('FFT plot of the Modulator Output')
xlabel('Frequency')
ylabel('Power in dB')
figure(6);
plot(f,sig_fft_dB);
xlim([0 222000]);
title('FFT plot of the Modulator Output Zoomed in')
xlabel('Frequency')
ylabel('Power in dB')


// Filter Coefficient generation for the Discrete Loop filter
close all;
clear all;
clc

syms z fs %Variables for bilinear transform
s=sym(2*fs*(1-z^-1)/(1+z^-1))
%Expression for bilinear transform
syms tauz1 tauz2 tauz3 taup1 taup2 taup3 kc
%Variables for compensator are created
c=sym(kc*(tauz1*s+1)*(tauz2*s+1)*(tauz3*s+1)/...
(taup1*s+1)*(taup2*s+1)*(taup3*s+1))
%Expression for compensator
 cnew=subs(c,s,s); %Bilinear transform
[cnum cden]=numden(cnew) %Nominator and denominator are separated

cnum=subs(cnum,tauz1,1/(2*pi*83e3));

cnum=subs(cnum,tauz2,1/(2*pi*83e3));
cnum=subs(cnum,tauz3,1/(2*pi*30e3));
cnum=subs(cnum,taup1,1/(2*pi*5e3));
 cnum=subs(cnum,taup2,1/(2*pi*5e3));
cnum=subs(cnum,taup3,1/(2*pi*3e6));
cnum=subs(cnum,kc,1000);
cnum=subs(cnum,fs,90.3168e6);
cnum=collect(cnum,z);

cden=subs(cden,tauz1,1/(2*pi*83e3));
cden=subs(cden,tauz2,1/(2*pi*83e3));
cden=subs(cden,tauz3,1/(2*pi*30e3));
cden=subs(cden,taup1,1/(2*pi*5e3));
```

```
cden=subs(cden,taup2,1/(2*pi*5e3));
cden=subs(cden,taup3,1/(2*pi*3e6));
cden=subs(cden,kc,1000);
cden=subs(cden,fs,90.3168e6);
cden=collect(cden,z)
close all
clear all
clc
syms z fs %Variables for bilinear transform
s=sym(2*fs*(1-z^-1)/(1+z^-1));
%Expression for bilinear transform
syms omega_0 Q
%Variables for compensator are created
R=sym(omega_0^2/(s^2+(omega_0/Q)*s+omega_0^2));
%Expression for compensator
Rnew=subs(R,s,s); %Bilinear transform
[cnum cden]=numden(Rnew) ;%nominator and denominator are separated
cnum=subs(cnum,omega_0,389249);
cnum=subs(cnum,Q,.513);
cnum=subs(cnum,fs,98.304e6);
cnum=collect(cnum,z);
cden=subs(cden,omega_0,389249);
cden=subs(cden,Q,.513);

% close all;
N=2^20;         % # of points
n=0:N-1;
% OSR=8;
%     fin=1023/65536;
fs=90316.8e3;
f=fs/N.*n;
x=double(vout(1:N));
y=double(vout_open(1:N));
% hold on;
figure(1);
% subplot(2,1,1)
plot(n,x);
% stairs(n,x)
% holf off;
xlabel('sample node')
ylabel('Amplitude (v)')
w=hann(N);
W=fft(w);
Y=x.*w;
Z=y.*w;
yfft=fft(Y);
yfft1=fft(Z);
ypwr=2/W(1)^2.*abs(yfft).^2;
ypwr1=2/W(1)^2.*abs(yfft1).^2;
ypwr(1)=ypwr(1)/2;
```

```
ypwr1(1)=ypwr1(1)/2;
ypwrlog=10*log10(ypwr);
ypwrlog1=10*log10(ypwr1);
figure(2);
hold on;
plot(f(1:N/2),ypwrlog(1:N/2),'r');
plot(f(1:N/2),ypwrlog1(1:N/2),'g');
hold off;
% aaplot=stem(f(1:N/2),ypwrlog(1:N/2),'.');
% set(aaplot,'basevalue',-300);
xlabel('Frequency (Hz)')
ylabel('Power (dB)')
Ps=0;

% signalBins = [13:35];
% s = norm(ypwr(signalBins));       % *4/(N*sqrt(3)) for true rms value;
% noiseBins = [36:64];
% n = norm(ypwr(noiseBins));
% if n==0
%     snr = Inf
% else
%     snr = dbp(s/n)
% end
signalBins = [40:77];
% signalBins = [1:32];
s = max(ypwr(signalBins));      % *4/(N*sqrt(3)) for true rms value;
noiseBins = [1:39,78:231];
% noiseBins = [33:64];
n = max(ypwr(noiseBins));
if n==0
   snr = Inf
else
   snr = dbp(s/n)
end
```