

A 1.2V 25MSPS Pipelined ADC Using Split CLS with Op-amp Sharing

by

Visu Vaithyanathan Swaminathan

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Graduate Supervisory Committee:

Hugh Barnaby, Chair
Bertan Bakkaloglu
Jennifer Blain Christen

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ABSTRACT

As the technology length shrinks down, achieving higher gain is becoming very difficult in deep sub-micron technologies. As the supply voltages drop, cascodes are very difficult to implement and cascade amplifiers are needed to achieve sufficient gain with required output swing. This sets the fundamental limit on the SNR and hence the maximum resolution that can be achieved by ADC. With the RSD algorithm and the range overlap, the sub ADC can tolerate large comparator offsets leaving the linearity and accuracy requirement for the DAC and residue gain stage. Typically, the multiplying DAC requires high gain wide bandwidth op-amp and the design of this high gain op-amp becomes challenging in the deep submicron technologies.

This work presents ‘A 12 bit 25MSPS 1.2V pipelined ADC using split CLS technique’ in IBM 130nm 8HP process using only CMOS devices for the application of Large Hadron Collider (LHC). CLS technique relaxes the gain requirement of op-amp and improves the signal-to-noise ratio without increase in power or input sampling capacitor with rail-to-rail swing. An op-amp sharing technique has been incorporated with split CLS technique which decreases the number of op-amps and hence the power further. Entire pipelined converter has been implemented as six 2.5 bit RSD stages and hence decreases the latency associated with the pipelined architecture – one of the main requirements for LHC along with the power requirement. Two different OTAs have been designed to use in the split-CLS technique. Bootstrap switches and pass gate switches are used in the circuit along with a low power dynamic kick-back compensated comparator.

Dedicated to my Parents

Mr. Swaminathan Mani Iyer and Mrs. Sudha Swaminathan

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LIST OF ABBREVIATIONS

A/D	Analog/Digital Converter
ADC	Analog-to-Digital Converter
CDS	Correlated Double Sampling
CLS	Correlated Level Shifting
CMFB	Common Mode Feedback Circuit
CMOS	Complementary Metal Oxide Semiconductor
D/A	Digital/Analog Converter
DAC	Digital-to-Analog Converter
DC	Direct Current
D-FF	Delay Flip Flops
ENOB	Effective Number Of Bits
EST	Estimation
FFT	Fast Fourier Transform
LHC	Large Hadron Collider
LS	Level Shifting

LSB	Least Significant Bit
MDAC	Multiplying Digital-to-Analog Converter
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
MSPS	Mega Samples Per Second
MUX	Multiplexer
NMOS	N-channel Metal Oxide Semiconductor
OTA	Operational Transconductance Amplifier
PMOS	P-channel Metal Oxide Semiconductor
RSD	Redundant Signed Digit
S/H	Sample and Hold
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
SNDR	Signal-to-Distortion Noise Ratio
SNR	Signal-to-Noise Ratio
UGF	Unity Gain Frequency

1 INTRODUCTION

The proliferation of digital computing and signal processing in electronic systems is often described as “the world is becoming digital every day”. The main attraction to move towards digital arises from the fact that digital circuits are less susceptible to noise and exhibit a high degree of robustness to supply and process variations. The factor that caused digital circuits and processors to be dominant in our day-to-day lives is its scalability. This allowed digital circuits to attain higher speed, lower power dissipation and low cost with the ease of integration which favors more functionality per chip.

Still naturally occurring signals in the world are analog and in order to interface digital processors with the analog world, data acquisition and reconstruction circuits must be used. Analog-to-Digital converters (ADCs) and Digital-to-Analog converters (DACs) bridge this gap and enable us to exploit the full benefits of digital circuits as mentioned earlier. This interface between the analog and digital worlds is illustrated in the Figure 1-1.

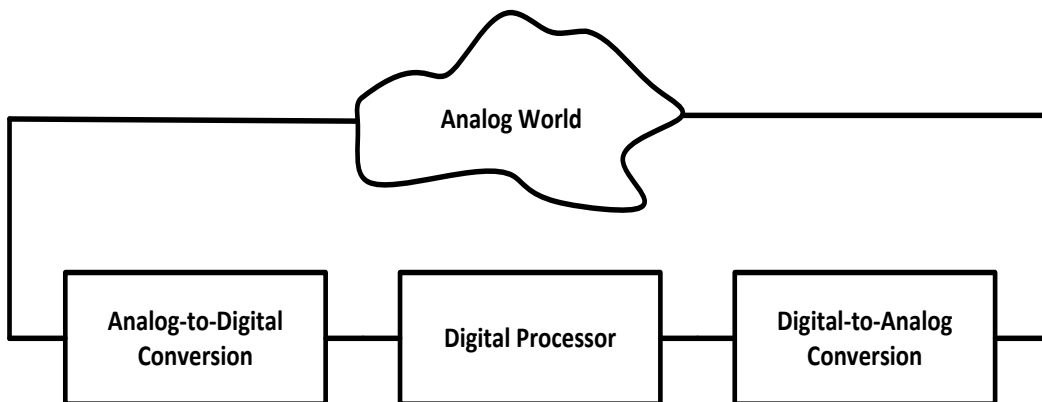


Figure 1-1 An interface between an analog world and a digital processor

The main challenges in data converter design are decreasing supply voltage, short channel effects in MOS devices, mixed signal issues, the development of design and simulation tools, and testability [1]. In analog-to-digital converters (ADCs), they need to be met at the same time as the requirements for sampling linearity; conversion rate, resolution, and power consumption are becoming tighter.

This work concentrates on low voltage issues in ADCs by searching for and developing techniques and circuit structures suitable for today's and future low voltage technologies. It focuses on reducing the effects of noise and distortion in pipelined analog to digital converters (ADCs) where the limited swing and finite operational amplifier (op-amp) gain are the main sources of distortion in the analog-to-digital data converters.

This thesis is organized as follows: Chapter 2 reviews the several analog-to-digital converter architectures. Chapter 3 discusses the system level architecture of pipelined ADC in detail and Chapter 4 presents switched capacitor circuit techniques such as Correlated Double Sampling (CDS), Correlated Level Shifting (CLS) and split Correlated Level Shifting that reduce the effects of op-amp imperfections along with a proposed technique for op-amp sharing in split-CLS. Chapter 5 presents the circuit level implementation used to construct the ADC and Chapter 6 provides the simulation results of a complete 1.2V 25MSPS 12 bit pipelined ADC. Finally this thesis is concluded in Chapter 7.

2 DATA CONVERTER ARCHITECTURES

In this chapter a brief overview of Nyquist rate analog-to-digital converter is presented along with different ADC architectures. Many ADC architectures have been developed and studied over the years. Each architecture has its own benefits and drawbacks and is best suited to particular type of application depending on the desired resolution, speed, die area and power consumption. This chapter presents the widely used types and ends with a brief overview of pipelined architecture which is the topic of this thesis.

2.1 ADC Definition

Analog signals are inherently continuous in amplitude and time. Digital systems operate on numbers in discrete time. Thus a conversion from continuous amplitude and time to quantized amplitude and discrete time constitutes an A/D conversion. Figure 2-1 shows a simplified flow diagram of the conversion process [2].

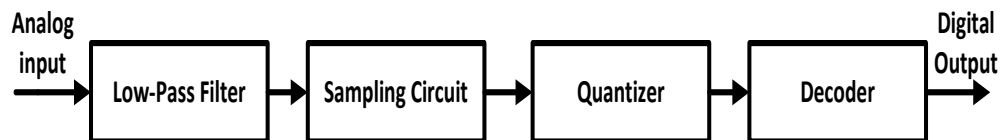


Figure 2-1 Simplified flow diagram of analog-to-digital interface

The analog signal is initially passed through a low pass filter called an anti-aliasing filter to band limit the input signal in order to remove any undesired frequency component. It is then passed through a sampling network to produce a discrete time signal. At this point, the signal is discrete in time domain but the

amplitude is still continuous. This signal is passed through a quantizer which converts the continuous amplitude signal into a discrete amplitude representation. This is accomplished by comparing a continuous amplitude signal to a set of fixed reference levels. To end the conversion process, a digital decoder takes the discrete amplitude signal and assembles it into a digital bit sequence which is the digital representation of an input analog signal.

2.2 Flash Converter

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Flash ADCs are the simplest and most straight forward way to do analog-to-digital conversion. Flash ADCs are made by cascading high-speed comparators. Figure 2-2 shows a typical flash ADC block diagram. For an N-bit converter, the circuit employs $2^N - 1$ comparators. A resistive-divider with 2^N resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a 1 when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is 0. Thus, if the analog input is between V_{X4} and V_{X5} , comparators X_1 through X_4 produce 1's and the remaining comparators produce 0's. The point where the code changes from ones to zeros is the point at which the input signal becomes smaller than the respective comparator reference-voltage levels. This architecture is known as

thermometer code encoding [3]. The thermometer code is then decoded to the appropriate digital output code.

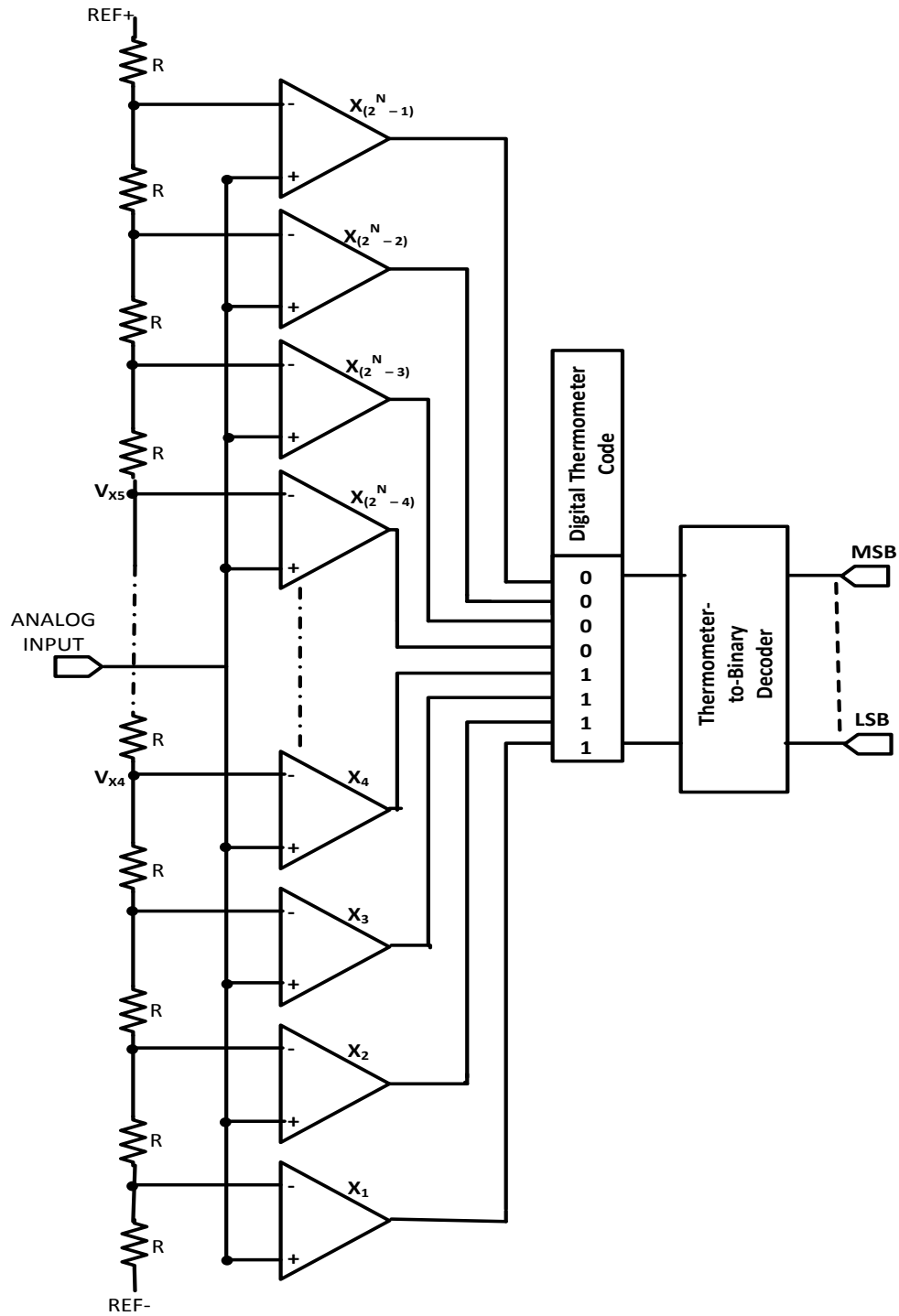


Figure 2-2 Flash ADC architecture

Flash ADCs are suitable for applications requiring very large bandwidths. However, these converters consume considerable power, have relatively low resolution, and can be quite expensive [4]. This limits them to high-frequency applications that typically cannot be addressed any other way.

2.3 Two-step Flash

Another type of flash converter is two-step flash converter or the parallel, feed-forward ADC. The basic block diagram of two step flash ADC is shown in Figure 2-3. The conversion is done in two steps by separating the conversion process with feed forward circuitry and allocating them to two separate flash ADCs. The first converter performs a rough estimate of the input while the second converter performs a fine conversion. The advantages of this architecture are that the number of comparators is greatly reduced from that of the flash converter – from $2^N - 1$ comparators to $2(2^{N/2} - 1)$ comparators. For example, 8 bit flash ADC requires 255 comparators whereas two step flash ADC requires only 30 comparators. The trade-off for savings in area and power is that conversion process takes two steps instead of one clock cycle as in flash ADC, with the speed limited by the bandwidth and settling time required by the residue amplifier and summer [5]. The conversion process is as follows:

- After the input is sampled, most significant bits (MSBs) are converted by the first flash ADC.
- The result is then converted back into an analog voltage by DAC and then subtracted from the input voltage.

- The result of the subtraction, known as residue, is then multiplied by $2^{N/2}$ and input into the second ADC. The multiplication not only allows two ADCs to be identical but also increases the quantum level of the input signal to the second ADC.
- The second ADC produces the least significant bits (LSBs) through the fine Flash conversion.

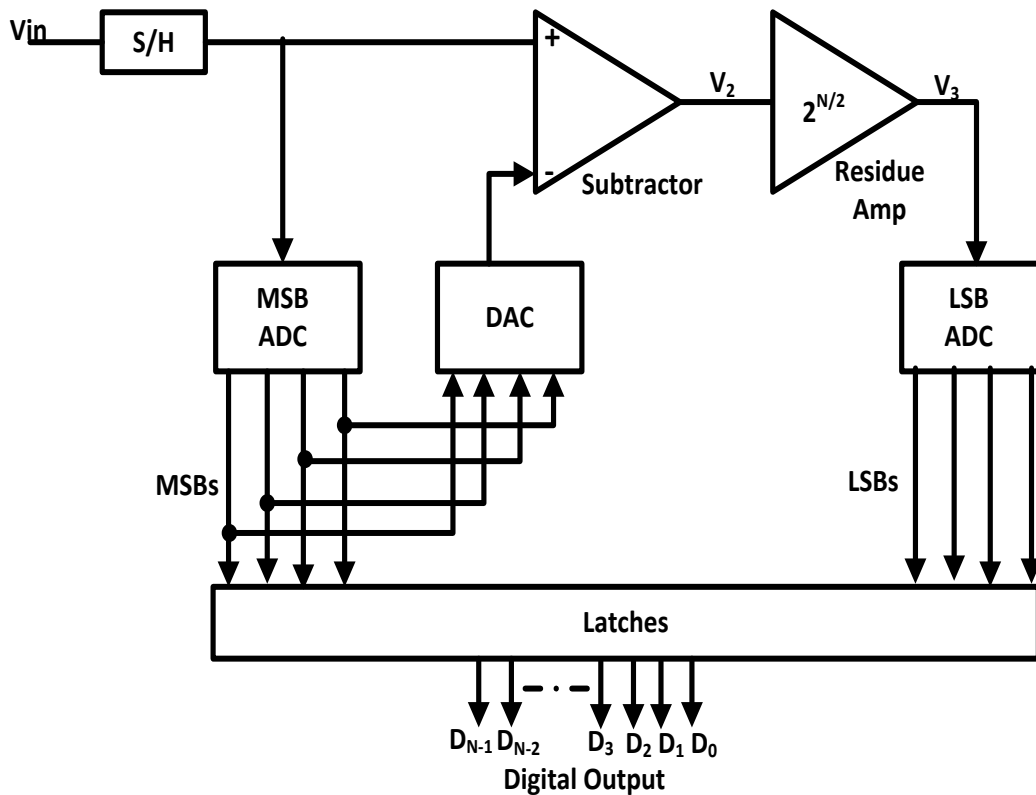


Figure 2-3 Block diagram of two step flash ADC

Figure 2-4 illustrates the two step nature of this converter. The first conversion identifies the segment in which the analog voltage resides. This is known as coarse conversion of MSBs. The result of the coarse conversion is then multiplied by $2^{N/2}$ in order to scale the references to the same level as that of the

first conversion. This second conversion is known as the fine conversion and will generate the final LSBs using the same Flash approach.

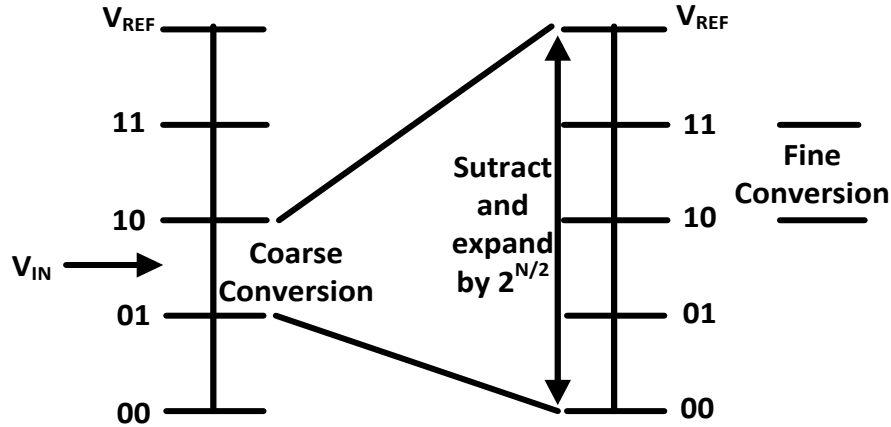


Figure 2-4 Coarse and fine conversions using a two-step ADC

2.4 Integrating dual slope ADC

The integrating converter architecture in the Figure 2-5 [5] is a much slower conversion technique but is usually much more accurate than the flash conversion-based architectures. Sample and hold front ends are needed for accurate conversion of continuously varying input analog signal. Integrating ADC performs the conversion by integrating the input signal and correlating the integration time with a digital counter. In this integrating dual slope ADC, two integrations are performed: one on the input signal and other on a known reference signal. The input voltage in this case is assumed to be negative so that output of the inverting integrator results in positive slope during the first integration. The first integration is of fixed length dictated by the counter, in which the sample and hold signal is integrated, resulting in a variable first slope.

Once the counter overflows and is reset, the reference signal is connected to the input of the integrator. Since V_{in} was negative and the reference voltage is positive, the inverting integrator begins discharging back down to zero with a constant slope. A counter measures the amount of time for the integrator to discharge back to zero thus measuring the digital output. An example conversion process of a dual slope ADC is shown in Figure 2-6.

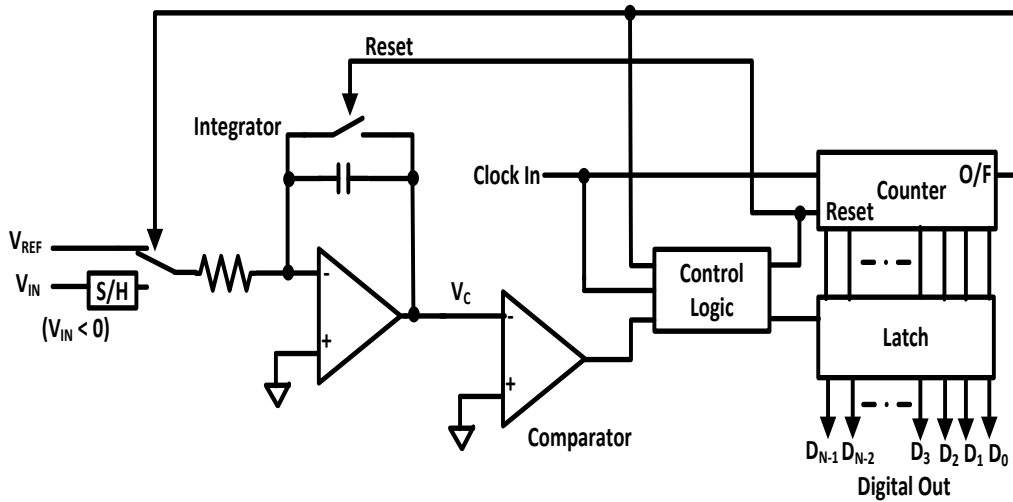


Figure 2-5 Block Diagram of a dual slope ADC

These ADCs are ideal for digitizing low bandwidth signals and provide high resolution analog-to-digital conversions. The longest conversion time occurs when $V_{in} = V_{ref}$ and the total number of clock cycles required to do the conversion is $2^{(N+1)} * T_{clk}$. For example, to obtain 10-bit resolution, you would integrate for 1024 (2^{10}) clock cycles, and then discharge for up to 1024 clock cycles (giving a maximum conversion of 2×2^{10} cycles). For more resolution, the number of clock cycles has to be increased. This tradeoff between conversion time and resolution is inherent in this implementation.

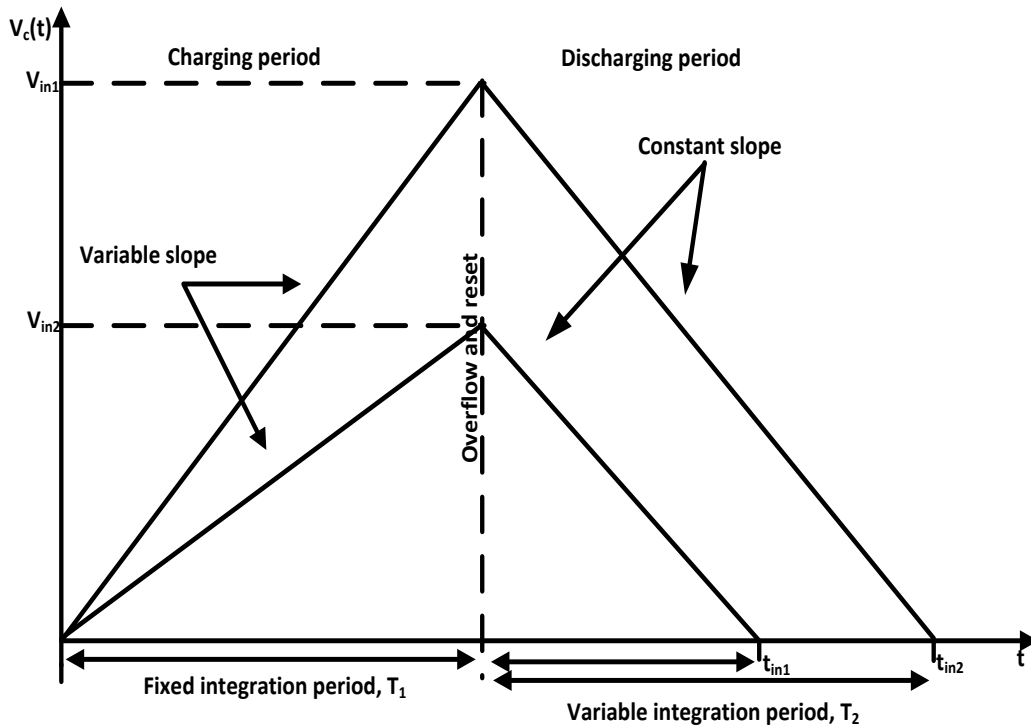


Figure 2-6 Integration periods for two separate samples of a dual-slope ADC

2.5 SAR ADC

The Successive-Approximation Register (SAR) architecture can be thought of as being at the other end of the spectrum from the flash architecture. While a flash converter uses many comparators to convert in a single cycle, a SAR converter conceptually uses a single comparator over many cycles to make its conversion. SAR converters are used in applications that require medium to high resolution and low to medium frequencies.

Figure 2-7 shows a block diagram of a typical SAR converter architecture. It is made up of four blocks; a sample and hold network, a comparator, a successive approximation register which includes control logic, and a digital-to-analog converter (DAC).

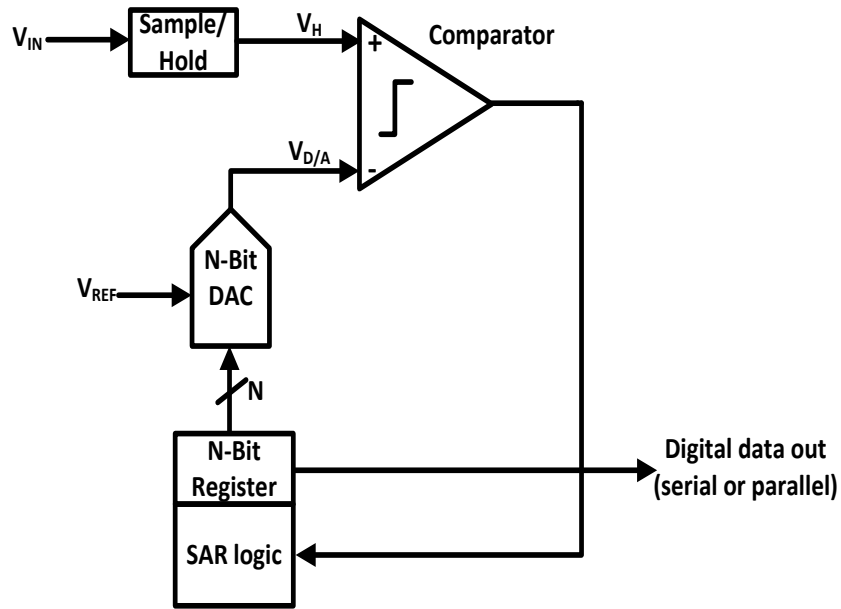


Figure 2-7 Simplified N-bit SAR ADC architecture

The SAR converter uses a “binary search” algorithm to convert the input signal to a digital output word. The digital output word is determined one bit at a time beginning with the MSB and ending with the LSB. A conversion proceeds as follows; first the input signal V_{in} is sampled and held. Next the DAC output voltage $V_{D/A}$ is set to the midscale of the reference voltage V_{ref} and then the comparator determines the polarity of $V_H - V_{D/A}$. If $V_H > V_{D/A}$ the MSB is set to 1, or if $V_H < V_{D/A}$ then the MSB is set to 0. Once the decision has been made, the process is repeated over and over again until all of the bits have been resolved. Conversion latency is determined by the number of bits that need to be resolved. For example, a 12 bit SAR A/D converter requires 12 clock cycles before the digital output is valid.

Most SAR converters implement the DAC using charge redistribution architecture. These DACs are made up of capacitors and switches; in high-

resolution SAR converters the ratio of the smallest to largest capacitor can be quite large. This leads to a very large input capacitance as well as large silicon area. Techniques have been developed [6] to reduce the capacitor size using monotonic capacitor switching procedures. Another problem with the DAC in SAR converter is that its settling dictates the amount of time it takes to resolve one bit. Therefore the maximum conversion rate is constrained by the speed of the DAC.

2.6 Oversampling ADC

Data converters may sample the input signal at the Nyquist rate or higher to prevent aliasing and thus allow complete reconstruction. The use of higher sampling rates, referred to as oversampling allows improvement in resolution but typically yields low signal bandwidth. The dynamic range of a system that uses a sampling frequency higher than the Nyquist rate is given by,

$$\mathbf{SNR}_{\text{oversampled}} = 2^{n-1} \sqrt{3 \cdot \frac{f_s}{f_{\text{signal}}}} \quad (2-1)$$

Thus oversampling the input leads to a higher SNR and hence improves the dynamic range of the system, as long as the SNR is the limiting criterion for dynamic range. This along with noise shaping is put to practice in oversampling ADCs. The ADC usually comprises of a sigma delta modulator followed by a digital decimator, as shown in the Figure 2-8. The Σ - Δ modulator typically consists of a discrete time analog integrator, followed by a quantizer with a DAC in the feedback path. The decimator consists of a low pass filter and the down sampler. Since linearity and speed are of prime importance in the feedback loop,

often just a 1-bit quantizer (comparator) and a 1-bit DAC are used. To achieve higher resolution, higher order integration and thus more integrators may be needed. Loop stability is however a consideration in single loop higher-order system [7]. The modulator acts as a low pass filter to the signal and as a high pass filter for the quantization noise. The output of this modulator is an over-sampled representation of the signal in the digital domain, and an averaging of this digital signal leads to an accurate digital representation of an analog input. The low pass filter is a digital filter that can be built with a sharp cut-off improving the digital estimate of the analog signal. Σ - Δ modulators achieve the highest resolutions (≥ 20 bits), but are conventionally limited to audio band signal frequencies due to the large oversampling ratios needed [8].

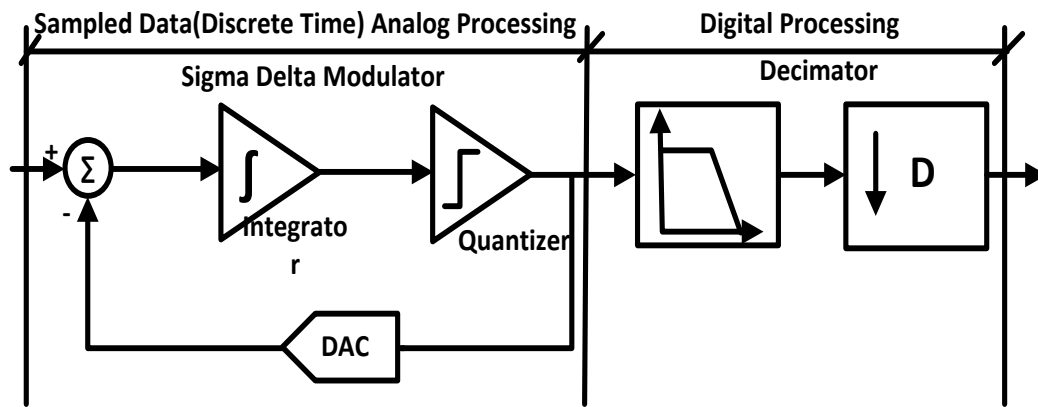


Figure 2-8 Sigma Delta ADC architecture

2.7 Cyclic ADC

A Cyclic converter, also known as an Algorithmic converter, is similar in operation to the successive approximation converter. However, in the case of the Cyclic ADC, the reference voltage is not altered. Instead, the error (or residue) of

the amplifier is doubled. Figure 2-9 shows a block diagram of a cyclic A/D converter. The cyclic converter consists of six main blocks: a multiplexer (mux), a sample and hold, ADC, DAC, a subtractor and a “gain of 2” amplifier.

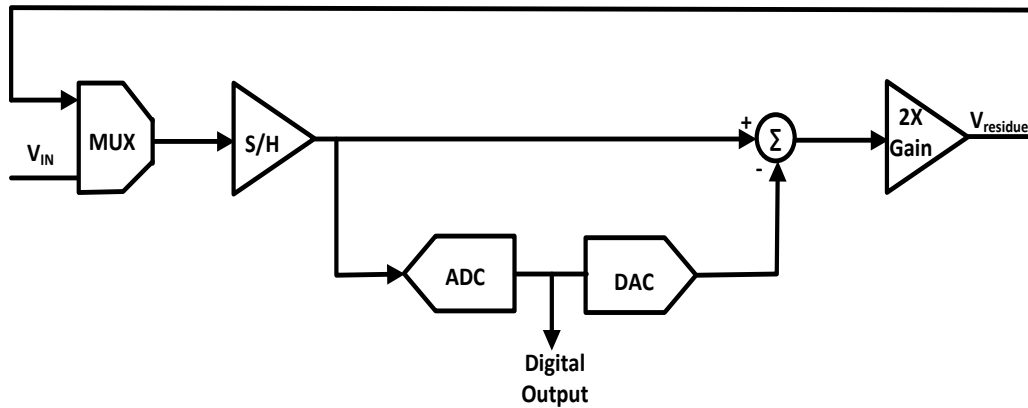


Figure 2-9 Block diagram of a cyclic A/D Converter

The operation of the cyclic converter functions in the following manner: First, the mux is set to allow the input voltage and is then sampled by the sample-and-hold block. That value is then compared to a threshold voltage, upon which a digital decision is made, determining a bit value in the final sequence of the number sampled. A reference voltage is generated by a 1-bit digital-to-analog converter which is dictated by the digital decision previously made. At the same time, the input value is amplified by a factor two (ideally). The amplified value is then summed to a reference voltage $\pm V_{REF}$, leaving a residue voltage. The residue voltage then becomes the input of the residue amplifier by switching the mux. This cycle is repeated enough times required to achieve the desired resolution, earning the device its name.

The advantage of the cyclic architecture over the SAR architecture is that it can be configured to generate multiple bits per clock cycle thereby reducing the

associated conversion time. As an example, a N-bit SAR ADC takes N clock cycles to produce the digital output whereas a N-bit cyclic ADC that produces 2 bits per clock cycle takes only N/2 clock cycles. Also, the Cyclic ADC is more area efficient than SAR ADC [9]. It should be noted that as the number of bits that are converted per clock cycle in the cyclic converter increases, the complexity of the circuitry in the ADC, DAC, and subtractor also increases.

2.8 Pipelined ADC

In a pipelined A/D converter, quantization is distributed along a pipelined signal chain resulting in an effective architecture for high resolution high speed ADCs. The pipelined architecture is very similar to the cyclic architecture in that each stage can produce multiple bits per clock cycle. The main difference between these two architectures is that instead of looping the residue voltage around the same stage N times to resolve the N-bits, N numbers of identical stages are cascaded, resulting in an analog pipeline. Figure 2-10 shows a system level block diagram of both the cyclic and pipelined architectures.

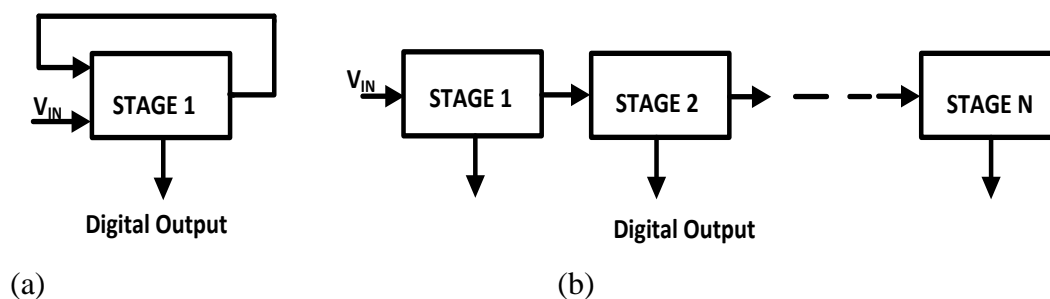


Figure 2-10 System level block diagrams (a) Cyclic architecture (b) pipelined architecture

The bit outputs however need to be corrected in a digital pipeline to compensate for the delay in processing each sample stage wise. This leads to higher power consumption as compared to a cyclic converter. The main advantage of using a pipelined architecture over a cyclic is that for every clock cycle a digital word is being output. This leads to a higher throughput although the speed of any single conversion still has a latency of the number of stages it has to go through.

Most modern processes can provide 10-12 bit capacitor matching, and gain stages with signal-to-noise ratios (SNRs) in excess of 100dB achieving very high speeds [10]. Pipelined converters are also conducive to formation of parallel architectures achieving higher speeds. The versatility of a pipelined converter lies in the fact that 16 bit accuracy can also be achieved if the speed is compromised and digital error correction and special sampling techniques are used to mitigate the effects of process variability [11]. Having considered the versatile nature of a pipelined ADC, this work is a basic implementation of this architecture at a very low supply voltage.

3 SYSTEM LEVEL ARCHITECTURE OF PIPELINED ADC

In this chapter, a system level architecture of pipelined ADC is presented in detail. The chapter begins by discussing the basic architecture and the issues associated with a conventional numerical division algorithm. It then proceeds into the Redundant Signed Digit algorithm as a solution to the problems posed by the conventional numerical division algorithm, followed by switch capacitor techniques used to implement the RSD logic. A simple ‘1’ and ‘1.5’ bit stage is used in this chapter for explanation purposes only. The implemented ADC consists of 2.5 bit stages.

3.1 General Pipelined Architecture

Pipelined ADCs offer an attractive combination of speed, resolution low power consumption and small die size. As its name suggests the pipelined ADC employs several pipelined stages to achieve high speed and high resolution. Figure 3-1 shows a general block diagram of a pipelined ADC [12]. It consists of “k” low-resolution ADCs, delay logic for synchronizing the output and digital correction logic to remove redundancy.

Each stage has $B+r$ bit resolution, where B represents effective stage resolution and r represents redundancy for the comparator offset correction algorithm. The first $k-1$ stages employ similar architectures and usually have the same resolution. The last stage does not have redundancy, so it is a B -bit(s) flash ADC. The total resolution N of a pipelined ADC with k stages can be expressed as,

$$N = \sum_{i=1}^k B_i + b_k, \quad (3-1)$$

where, B_i is effective resolution of the corresponding stage for the first $k-1$ stages and B_k is the resolution of the last stage. Two successive stages operate on non-overlapping clock phases. Digital outputs from each stage are delayed according to the position of the stage in the pipelined ADC for synchronization. The synchronized output is then fed to the correction logic. Figure 3-2 depicts a single stage of a pipelined ADC, consisting of a sample-and hold, a sub-ADC, a DAC, a subtractor and an amplifier.

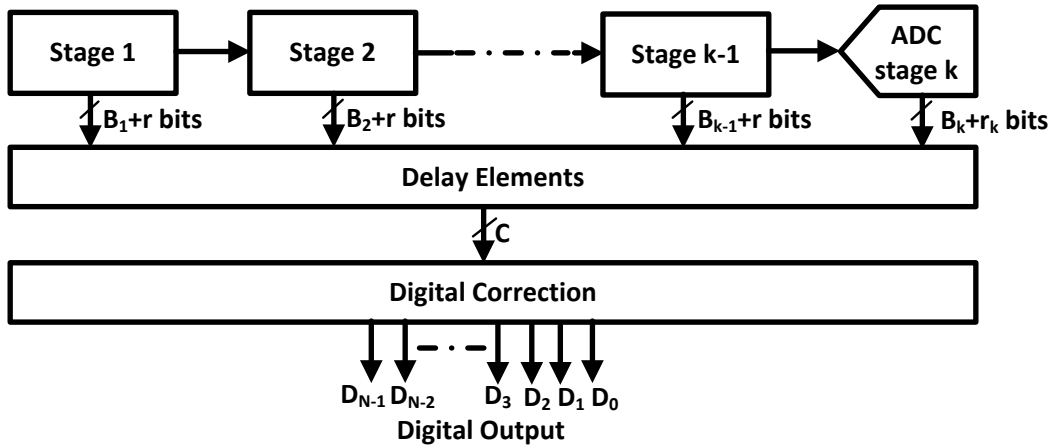


Figure 3-1 General block diagram of a pipelined ADC

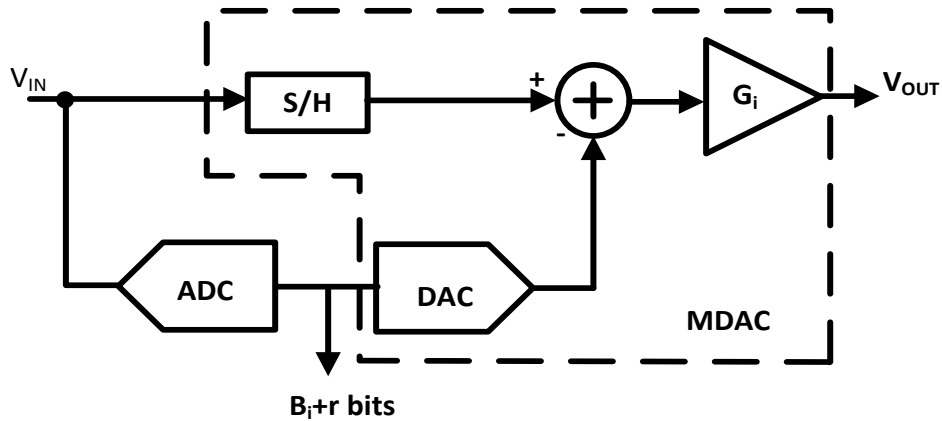


Figure 3-2 A single stage of pipelined ADC

The analog input is held constant by a sample-and-hold module and at the same time it is also converted into digital form by a sub-ADC. The digital encoded number is converted back to analog value by the DAC. Then output of DAC is subtracted from output of the sample-and-hold resulting in the stage residue. Then the residue is amplified by the gain given in equation 3-2 [12] for the next stage.

$$G_i = 2^{B_i + 1 - r} \quad (3-2)$$

Each stage operates concurrently, i.e., the first stage works on the most recent sample and the second stage works on a sample delayed by one time unit and so on. In principle each stage can be as low as 1-bit. But due to comparator offset errors the 1-bit stage is not used in practical implementations. This problem and its solution are discussed in next section. The output residue for a 1-bit is obtained according to equation,

$$V_{\text{residue}} = \begin{cases} 2V_{\text{in}} + V_{\text{ref}} & \text{if } b = 0 \\ 2V_{\text{in}} - V_{\text{ref}} & \text{if } b = 1 \end{cases} \quad (3-3)$$

where, V_{ref} is the reference voltage.

A residue plot for a 1-bit stage in an ideal case and with non-idealities is shown in Figure 3-3 [13]. The non-idealities may be the result of a slight gain error, other component mismatch, or an offset, either in the comparator, the switching circuitry or the amplifier. The transfer curve is off scale and such a condition leads to missing codes right in the middle of the input voltage range – a very serious error in an ADC. If one were to avoid the problem with just accurate components, all offsets would have to add up to less than one LSB. This condition

is not impossible, but is extremely stringent and would severely compromise speed and power. Algorithmic correction for most of the major issues is however possible, as with the RSD algorithm described next.

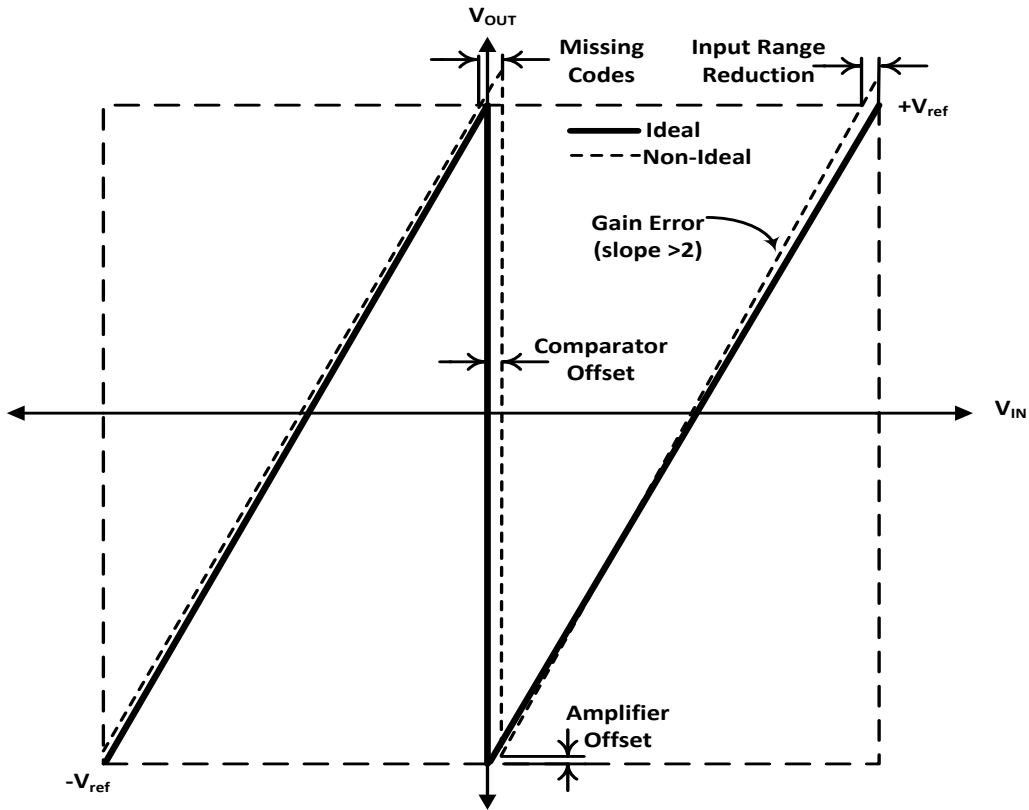


Figure 3-3 1-Bit Numerical division algorithm

3.2 RSD algorithm

A sophisticated digital correction algorithm, called redundant sign digit (RSD) coding, with 1 bit of redundancy ($r = 1$) in each stage is commonly used in pipeline A/D converters to relax the quantization accuracy specifications in sub-ADCs [14]. Adding a redundant bit means increasing the stage resolution by one bit minus one quantization level. Thus, the amount of redundancy is commonly

referred as 0.5 bits. By introducing redundancy in a 1-bit stage, the number of quantization levels is increased from two to three while the gain is kept at two. Furthermore, compared to the 2-bit stage, there is one quantization level less in the 1.5-bit stage.

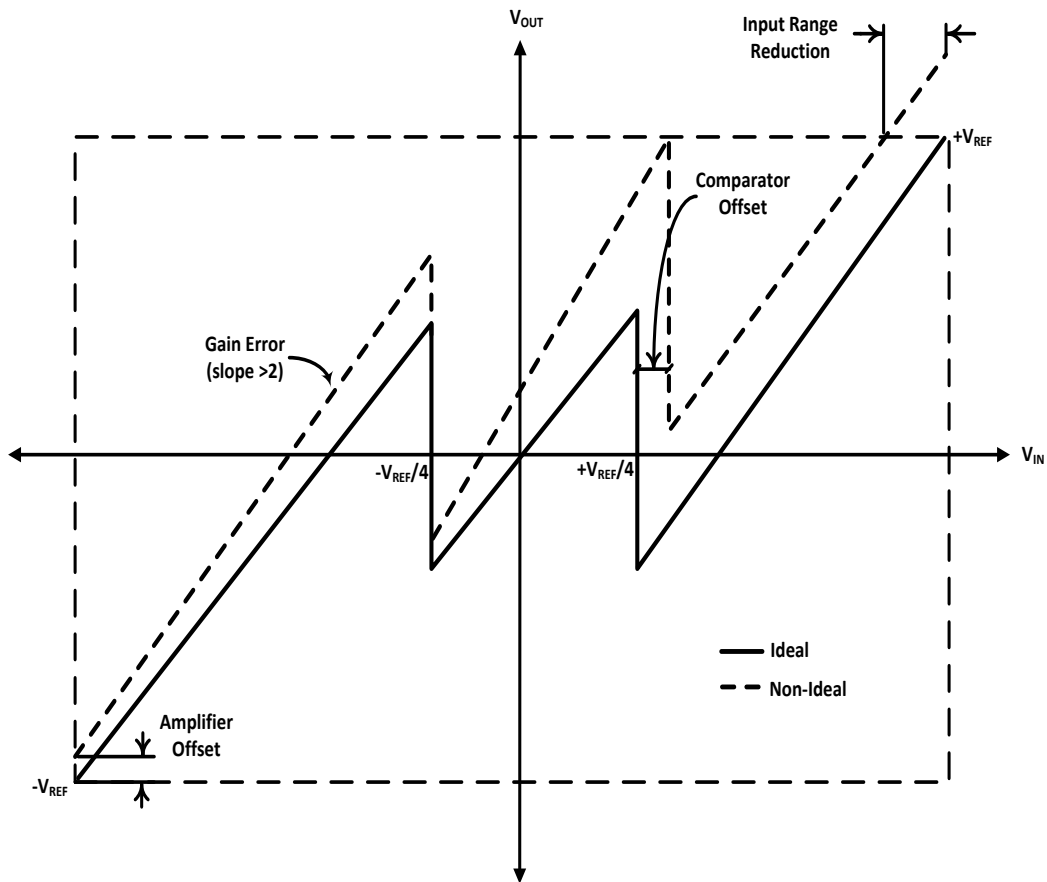


Figure 3-4 1.5-bit Redundant Signed Digit Algorithm

Figure 3-4 shows the transfer curve for a RSD algorithm based conversion [15][16]. For offset errors in the range $\pm V_{ref}/4$, the curve is not off-scale excluding the corners of the plot. These off-scale regions of the curve can be eliminated by redefining the input voltage ranges. Intuitively, the RSD correction is based on gathering errors and correcting them after the accumulated error is

enough to determine a bit value. The modified voltage relation for the RSD algorithm is now given by,

$$V_{\text{residue}} = \begin{cases} 2V_{\text{in}} - V_{\text{ref}} & \text{if } b = +1 \\ 2V_{\text{in}} & \text{if } b = 0 \\ 2V_{\text{in}} + V_{\text{ref}} & \text{if } b = -1 \end{cases} \quad (3-4)$$

Such large offset tolerances allow the use of very fast high offset comparators. Since the RSD stage generates a 1.5 bit output, two digital bits are used to code the output. In the case of 2.5 bit stage, 3 digital bits would be used. Digital error correction as explained in the section 5.5 will be used to get the final output.

3.3 Circuit Partitioning

There are three basic blocks that make up an RSD stage: a comparator, a sample and hold/multiply by 2 block and a digital logic block that controls a reference voltage subtraction/addition circuit.

Figure 3-5 shows a block diagram [17] and it shows that the RSD stage is partitioned into two sections: a switched capacitor network block and a comparison block. The switched capacitor network block consists of a sample-and-hold network, a multiply by two block and a reference addition/subtraction block. The comparison block consists of comparators and digital logic. This block determines the digital output bits and also controls the reference voltage additions and subtractions that are performed in the switched capacitor network block.

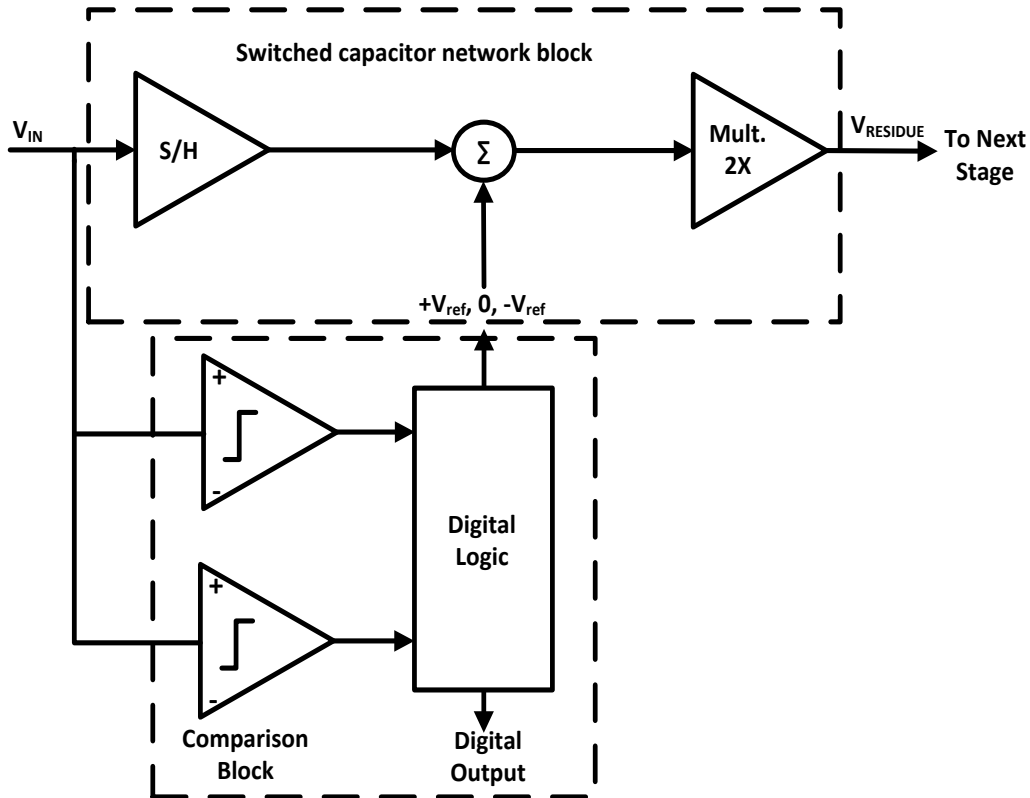


Figure 3-5 Combined simplified block diagram of an RSD stage.

3.4 Switched Capacitor Network

The flip-around architecture was selected for use in the present design due to its higher feedback factor, faster speed, and precision advantages over the charge-redistribution topology [18]. Both networks correctly perform the multiply by two (multiply by 4 in the case of 2.5 bit stage which is used in this ADC design) and RSD algorithm functions.

Figure 3-6 shows the single ended version of each topology. It should be noted that all the designs in the ADC were actually implemented using fully differential circuitry for improved dynamic range and power supply rejection. The single ended version is shown here for instructive purposes only.

The following example will show that the feedback factor for the flip-around topology is higher than that of the charge-redistribution topology. The feedback factor for each topology is defined as

$$\beta = \frac{C_1}{C_1 + C_2} \quad (3-5)$$

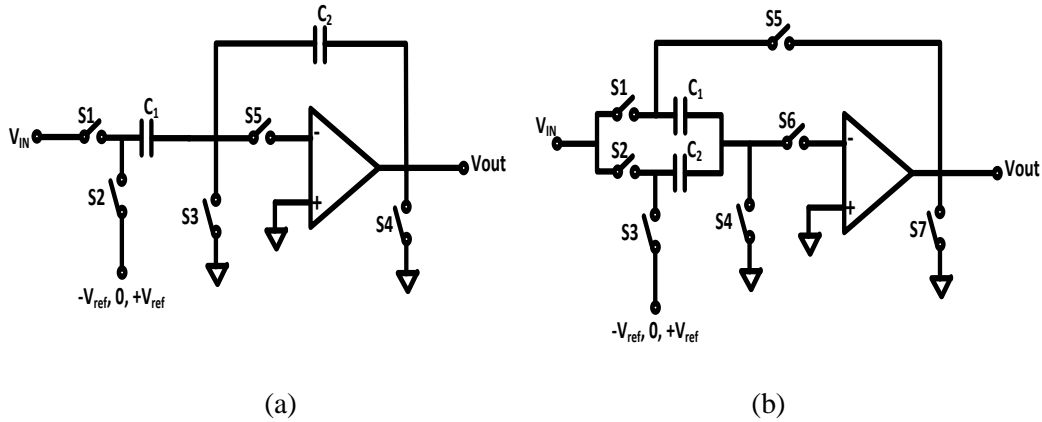


Figure 3-6 (a) Charge-redistribution topology (b) Flip-around topology

In the charge-redistribution topology circuit, $C_1 = 2C_2$. $C_2 = C$ and by substituting these values into equation (3-5) we get the following equation:

$$\beta = \frac{C}{2C + C} \quad (3-6)$$

Cancelling the C terms leave $\beta = 1/3$. For the flip-around topology circuit, $C_1 = C_2$. Letting $C_1 = C$ and substituting this value into equation (3-5) yields the following equation

$$\beta = \frac{C}{C + C} \quad (3-7)$$

Again, cancelling the C terms give $\beta = 1/2$. From this simple analysis it can be seen that the flip-around circuit has a higher feedback factor of $1/2$ compared to $1/3$ for the charge-redistribution topology. It is shown that a higher feedback

factor reduces the open loop DC gain and bandwidth requirements of the OTA [19].

Figure 3-7 shows the flip-around topology with its associated phases. During phase 1 (sampling phase) all of the Φ_1 switches are closed and the input signal voltage is sampled on capacitors C_1 and C_2 . On phase 2 (amplifying phase) the Φ_1 switches are opened and Φ_2 switches are closed. During this phase, all the charge is transferred from C_2 onto C_1 , effectively multiplying the input signal voltage by two. At the same time the subtraction/addition of the references is also being performed through the appropriate connection of $-V_{ref}$, 0, $+V_{ref}$ to C_2 as shown in Figure 3-7.

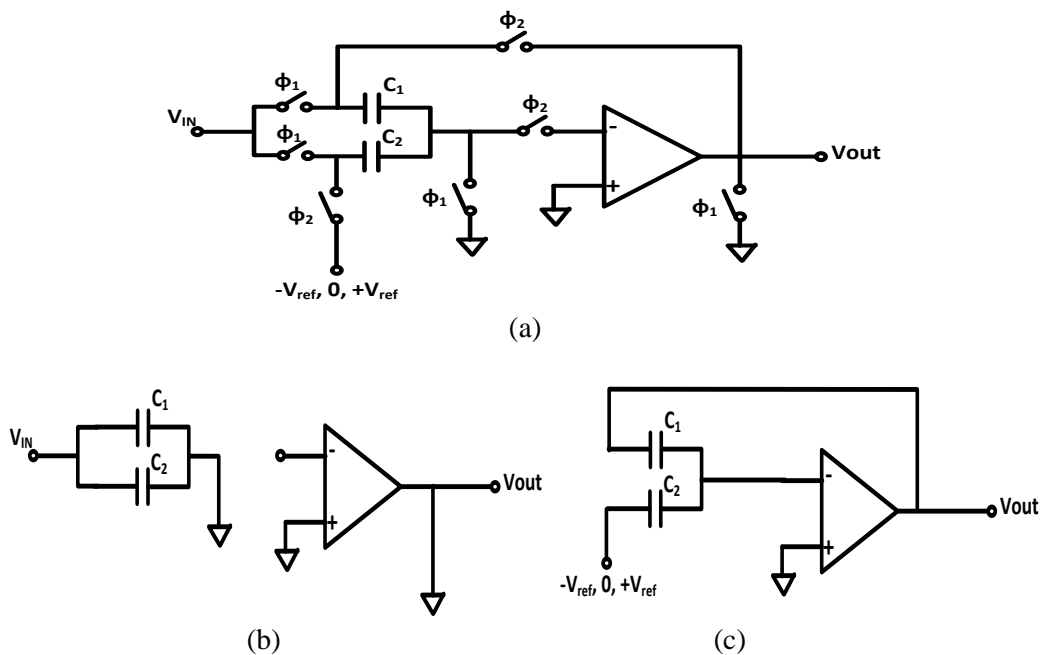


Figure 3-7 (a) Flip-around topology with switch phases shown (b) Φ_1 (sampling phase)
(c) Φ_2 (Output phase).

The transfer function for the flip around topology circuit in Figure 3-7 is shown to be [17]

$$V_{\text{out}} = \left(1 + \frac{C_1}{C_2}\right) V_{\text{in}} \pm \frac{C_1}{C_2} V_{\text{ref}} \text{ (or 0)}. \quad (3-8)$$

As explained in this section, the multiplying DAC (MDAC) is the most critical block and is the bottleneck in achieving higher accuracy at lower voltage supplies. Thus the focus in the next chapter will be on modification in the switched capacitor techniques to address the issues associated with the switched capacitor MDAC.

4 SWITCHED CAPACITOR CIRCUIT TECHNIQUES TO REDUCE THE EFFECT OF OP-AMP IMPERFECTIONS

Data conversion regimes can be split broadly based on the resolution and the sampling speed of the data conversion requirement. As discussed in the previous chapter moderate to high resolution and moderate to high speed data conversion is dominated by pipelined ADCs. This mainly is because of their parallel conversion of data at high speeds and capability to work as a Nyquist rate data converter. Thus a pipelined ADC is the most suitable ADC for the Large Hadron Collider application and the ADC works up to 30MSPS and churning out 12 bits at that speed.

Since this ADC is targeted for application in radiation environments, it is desirable to use a process which is robust to radiation damage. Thin oxide devices have been shown to be more robust to radiation than thicker oxide devices [20]. Thus, to be able to use thinner oxide devices, more advanced processes with lower gate lengths are used. But this entails many challenges especially for analog design such as reduced signal to noise ratio, low gain, incompatibility of trusted architectures to low supply voltages, and larger parasitics [21]. Thus, newer and clever circuits need to be designed. However, newer processes also enable higher speeds and also provide better matching between components [22].

Op-amps that are built in the newer process have characteristically higher bandwidths and low gains and signal swing. With the RSD algorithm, the sub-ADC can tolerate large comparator offsets leaving the linearity and accuracy requirements for the DAC and residue gain stage. Typically, the MDAC requires

a high gain bandwidth op-amp. The design of this high op-amp becomes challenging in deep sub-micron technologies. Thus, circuits that can compensate for the lower gains of the ultra sub micron process are very attractive option. Op-amps that are used in switch capacitor circuits can have their performance enhanced by switch capacitor techniques such as double sampling [1], correlated double sampling [23] and correlated level shifting [24]. The advantages and disadvantages of these techniques are explained in the following sections and it is shown that correlated level shifting is very suitable for the targeted application. This chapter starts with pros and cons associated with technology scaling and describe different switched capacitor techniques developed to combat those effects. It then concludes with a new proposed technique that can be used alongside the existing switched capacitor technique called split CLS

4.1 Scaling of the device

The scaling of devices on the surface improves speed, but it is not the only effect that it has and there are many challenges that need to be taken care of when designing at low feature sizes. A brief discussion has been given on this effect here.

- Gain - The gain of devices drop as L (length of the transistor) decreases because of lower output resistance. This makes the design of high gain amplifiers turn to multiple stages which entail large bandwidth penalties due to Miller compensation.

- Signal Swing – Since with lower feature size, the gate oxide is also thinner, the devices can tolerate only lower voltages and hence designers are faced with lower supply voltages and lower signal swing levels. This leads to bigger input sampling capacitors to reduce the noise floor to meet a given Signal to Noise Ratio (SNR) specification. This consumes more power compared to older process technologies.
- Matching – With thinner oxides, device matching has improved for a given area. This helps with the design of pipelined data converters that are dependent on capacitor matching to provide accurate conversions.
- Speed – the speed of a device often characterized by unity gain frequency (ft) is inversely proportional to the square of the minimum feature size (L). Thus, as length scales down, frequency of operation increases as a square.
- Op-amp architectures – Limited voltage supplies do not allow for traditional stacking of transistors as in cascode devices to get higher gain with required signal swing from a single stage.

From the above discussion, it becomes clear that a pipelined ADC can take advantage of the better matching and higher speed, but the design must battle low gain issues and low signal swings which lead to excessive power consumption in conventional designs. The methods presented in this chapter overcome the short-comings of low gain and signal swing while not losing on speed and matching.

4.2 Op-amp requirement

The gain and bandwidth requirement of the op-amps are based on the resolution and speed of the ADC. The output equation of the MDAC stage which uses the op-amp is given by equation (4-1) [25]

$$V_{out} = (V_{in} - V_{dac}) \frac{\beta A}{\beta A + 1} \left(1 - e^{-\frac{t}{\tau}}\right) \left(1 + \frac{C_s}{C_f}\right), \quad (4-1)$$

where, V_{in} is the input voltage to the MDAC stage, V_{dac} is the DAC reference voltage, β is the feedback factor (determined by the gain of the switch capacitor stage set by sampling capacitor, C_s and feedback capacitor, C_f), A is the open loop gain of the op-amp, t is the time for linear settling (determined by the sampling rate), τ is the time constant of the op-amp in closed loop, set by the unity gain frequency of the op-amp and the load capacitance.

In an ideal case, the op-amp has infinite gain and bandwidth, that is, A is infinite and τ is zero. But this is not the actual case as there is always a residual error in the MDAC stage, which is dependent on the gain and bandwidth of the amplifier. During design, this error is made less than that required for a particular resolution.

Using the conventional switch capacitor techniques, it can be shown that to meet the requirement of 12 bit and 25MSPS requires the first stage amplifier to have more than 81dB of gain and 455MHz unity gain frequency as calculated in the section 5.3. This requirement is in addition to a requirement of 2V of signal swing at the input and output. Radiation tolerance specifications further increase these requirements.

These requirements, though not impossible, are very tough and power hungry to design using conventional methods. However, switch capacitor techniques like correlated double sampling and correlated level shifting can greatly reduce the requirements of the amplifier making the designs feasible at lower supply voltages.

4.3 Correlated Double Sampling (CDS)

Correlated double sampling is one of the earliest approaches developed in the switched capacitor techniques to mitigate the imperfections. The main principle behind the operation of switched capacitor circuits is the charge transfer mechanism between capacitors. Due to the finite gain of op-amp, the inverting inputs of the op-amps do not form a perfect virtual ground, causing errors in the charge transfer between capacitors. The underlying principle of the correlated double sampling technique is to compensate for the finite gain error by using the error stored. A preliminary operation is performed during each clock interval using a set of auxiliary capacitors which are matched to the main capacitors (the input conditions for this operation are the same as those for the final desired operation). This preliminary operation provides us with a close approximation for the finite gain error, which is stored and used for correction during the final operation. This scheme requires more chip area but achieves a much higher precision [23].

The CDS architecture along with three phases of operation is given in Figure 4-1. The operation of the circuit is as follows: During the preliminary

operation called as estimation phase, the amplification is done using the capacitors C_{S_P} and C_{F_P} . Due to finite gain of the op-amp, the inverting input will not be equal to zero and the output corresponding to this phase is given as V_o' . The voltage at the inverting node '1' of the amplifier is given by $V_2 = -V_o'/A$ and is stored on the auxiliary capacitor C_{CDS} . During the second phase called as level shifting phase, amplification is performed using capacitors C_S and C_F with C_{CDS} placed in series with the inverting input of the amplifier. Now the voltage at the node '1' is given by a new

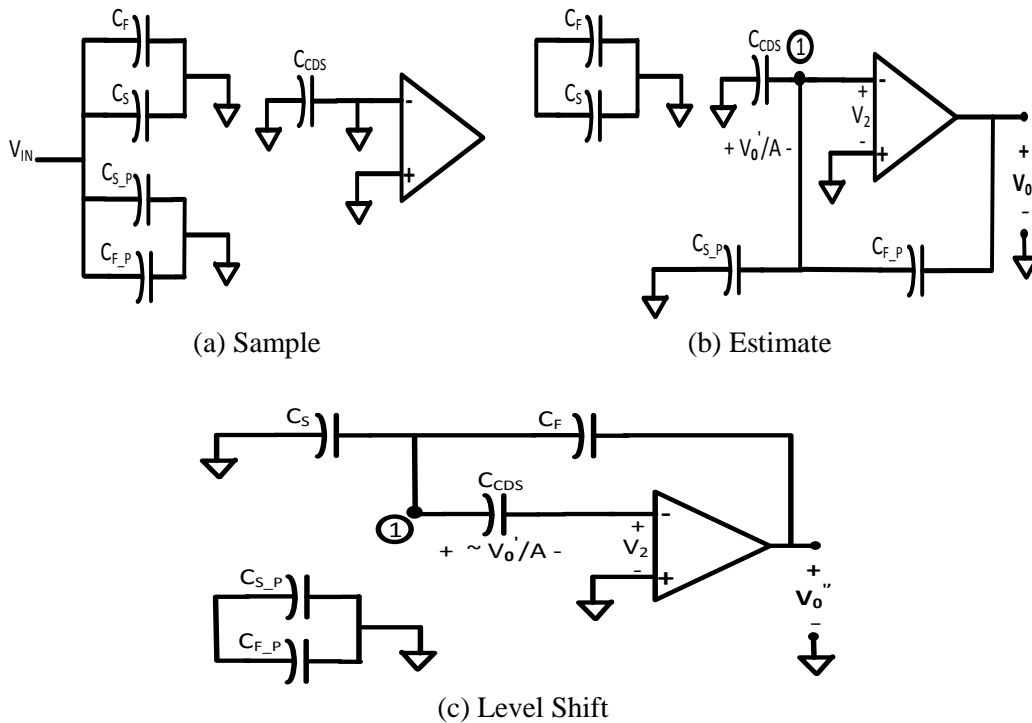


Figure 4-1 Three phases of correlated double sampling

value of V_2 minus old value stored in C_{CDS} . This difference is very small because of the preliminary operation and thus the error in charge transfer is significantly reduced. It can be easily shown that finite gain error is now inversely proportional

to A^2 [23]. During the estimation phase, the input referred offset and low frequency input referred noise are also stored on the auxiliary capacitor and hence will be eliminated during the final phase of the operation.

4.4 Correlated Level Shifting (CLS)

Correlated level shifting is a very attractive switch capacitor technique that provides an effective gain more than the square of the actual gain of the amplifier,

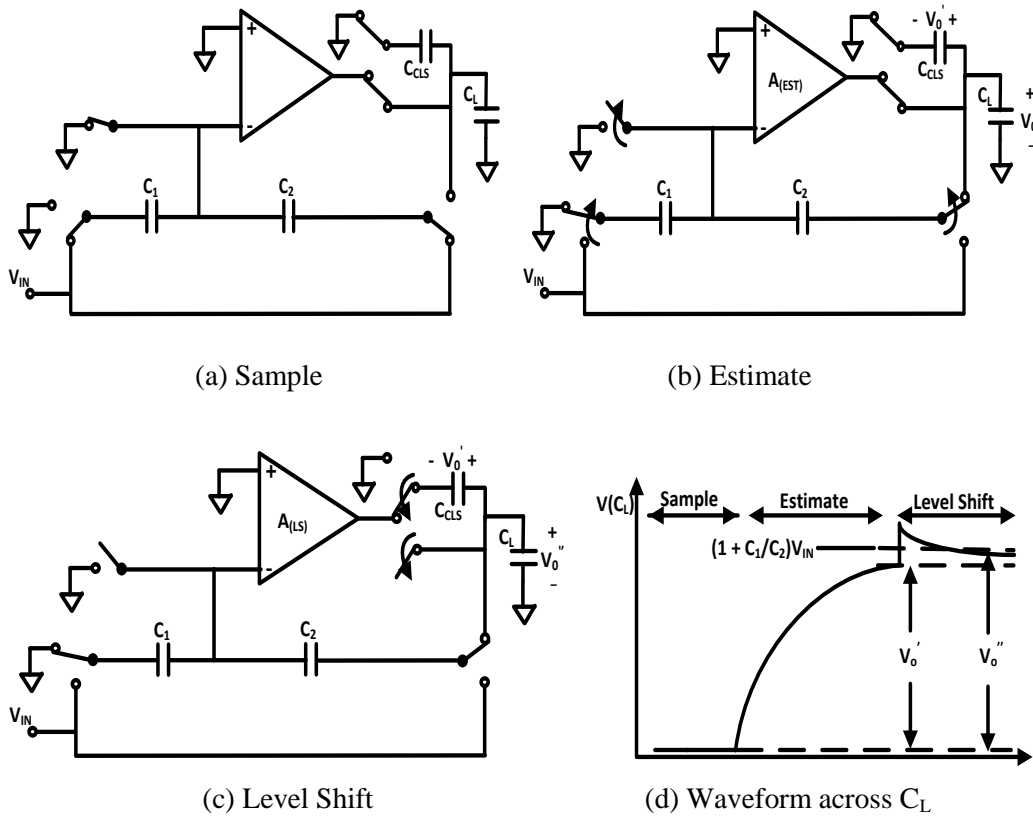


Figure 4-2 Three phases of correlated level shifting (CLS) and the waveform at the load.

similar to CDS. It also increases the signal swing range and reduces non-linearity [24]. Similar to CDS, CLS also uses three phase clocks and feeds the error back into the MDAC stage, reducing the error. The CLS architecture and the three

phases associated with it are given in Figure 4-2. The differences in the techniques arise from where they operate: CDS feeds its error back in at the input whereas CLS operates at the output and tries to remove the signal from the active circuit.

4.5 Error reduction analysis

The circuit in Figure 4-2 can be analyzed to show that the output voltage at the end of the estimation phase [26] is given by equation (4-2).

$$V_o' = V_{in} \left(1 + \frac{C_1}{C_2}\right) \left(\frac{1}{1+T}\right) \quad (4-2)$$

where, $T = \frac{A_{(EST)} \cdot C_2}{(C_1 + C_2 + C_{IN})}$ is the op-amp loop gain during the estimation phase. This first estimate (V_o') is less than the error-free output (i.e. $V_o = V_{IN}(1+C_1/C_2)$) because the finite op-amp gain produces an imperfect virtual ground so C_1 does not completely transfer its charge to C_2 . The residual voltage on C_1 from the imperfect virtual ground is

$$V_{C1(EST)} = \frac{-V_o'}{A_{EST}} \quad (4-3)$$

Traditionally this error is reduced by making the op-amp DC gain (i.e. A) as large as possible, but notice that the error could also be reduced by making the output of the op-amp small. This is what CLS does: it removes the signal from the active circuitry by storing the first estimate of the output voltage on C_{CLS} and then removes that signal from the output of the op-amp in the level-shift phase (Figure 4-2). Thus the residue voltage on C_1 is much smaller at the end of the

level-shift phase. If we neglect the charge lost from C_{CLS} , the voltage at the inverting node at the end of the level shifting phase is [24]:

$$V_{C1(LS)} = - \frac{(V_o'' - V_o')}{A_{LS}} \quad (4-4)$$

where, V_o'' is referred to as the second estimate. This is much smaller than (4-3), which means that the charge from C_1 is closer to being completely transferred to C_2 . The output voltage can be found as

$$V_o'' = V_{in} \left(1 + \frac{C_1}{C_2} \right) \left(\frac{1}{1 + T_{eq}} \right), \quad (4-5)$$

where the equivalent loop gain is, $T_{EQ} = T(2+T) \approx T^2$. Equation (4-5) neglects the charge loss from C_{CLS} and sets $A_{(EST)} = A_{(LS)}$. Charge transfer from C_{CLS} to the load will reduce the equivalent gain. Recently, a technique has been developed to overcome the loop gain degradation in the level shifting phase [27].

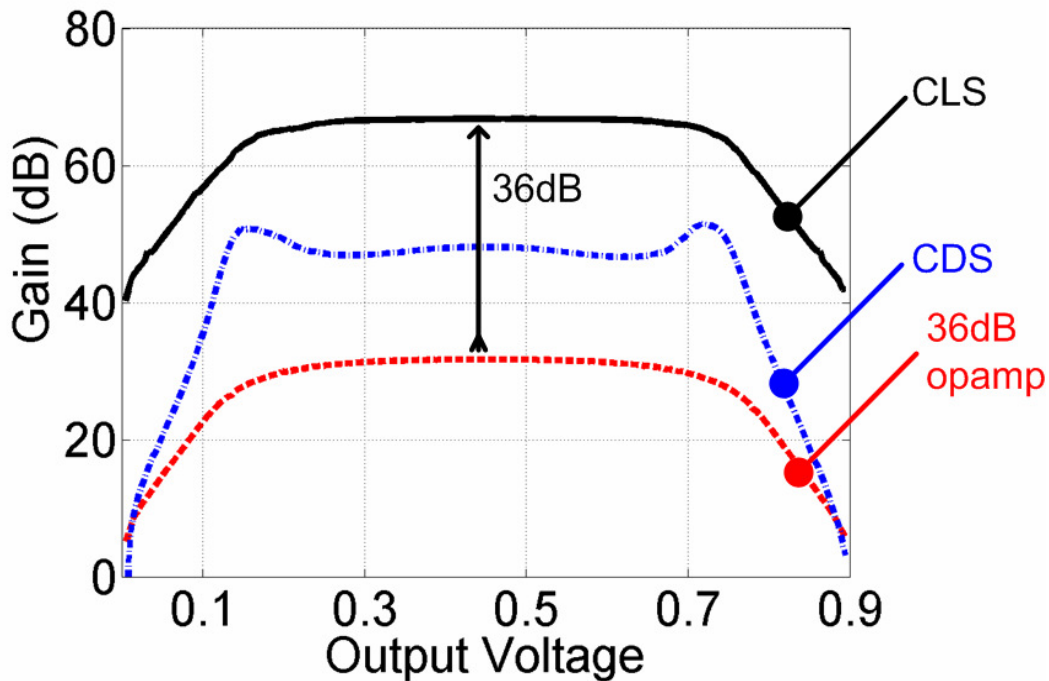


Figure 4-3 Open loop gain Vs output voltage using CLS or CDS with a 36dB op-amp

In CLS, the level-shift phase returns the op-amp output towards the mid-rail, where op-amp gain will be the largest. This is especially important when the output is close to the rails because $A_{(EST)}$ will be very small. Figure 4-3 shows the performance differences with and without CLS [26]. Note how the equivalent open-loop gain for CLS is shifted up by $A_{(LS)}$ over the entire output range. The CLS equivalent loop gain is much better than the CDS equivalent loop gain, which is just the op-amp gain squared with some significant attenuation due to charge sharing.

CLS removes, almost entirely, the signal from the active circuit and returns the active circuit to its best biasing conditions. Thus this technique provides an effective gain equal to the gain of the amplifier multiplied by the best gain of the amplifier. The best gain of the amplifier is when the amplifier is in its best biasing conditions. The gain depends on the input signal level as shown in Figure 4-3. The gain is lower at the extremities as some transistors can go into the triode region.

4.6 Transient behavior and Speed

To show the effectiveness of this technique, a comparison between the settling of a conventional 60dB amplifier and a 30dB amplifier with CLS are shown in Figure 4-4 [26]. It can be seen that in CLS, there is a transient jump at the beginning of the level shifting phase. This jump depends on the output capacitance and the height of the jump depends on the relative size of output capacitance compared to CLS capacitance. Though this reduces the settling time

by 10-20% [24] compared to conventional op-amp with the same phase margin and bandwidth, the CLS still has an upper hand. This is because compared to 60dB op-amp, a 30dB op-amp with CLS requires just half of the power and it also increases the input and output signal swing which reduces the required size of the input sampling capacitor to achieve the required SNR. This further reduces the power consumed by the op-amp. Hence CLS already starts with a settling time close to the conventional op-amp and definitely has speed advantage (5X) when its power consumption is made equal to the conventional op-amp. It must be noted here that 30dB of gain is not difficult to obtain with normal amplifiers. But 60dB of gain may require multiple stages with bandwidth penalties and much higher power.

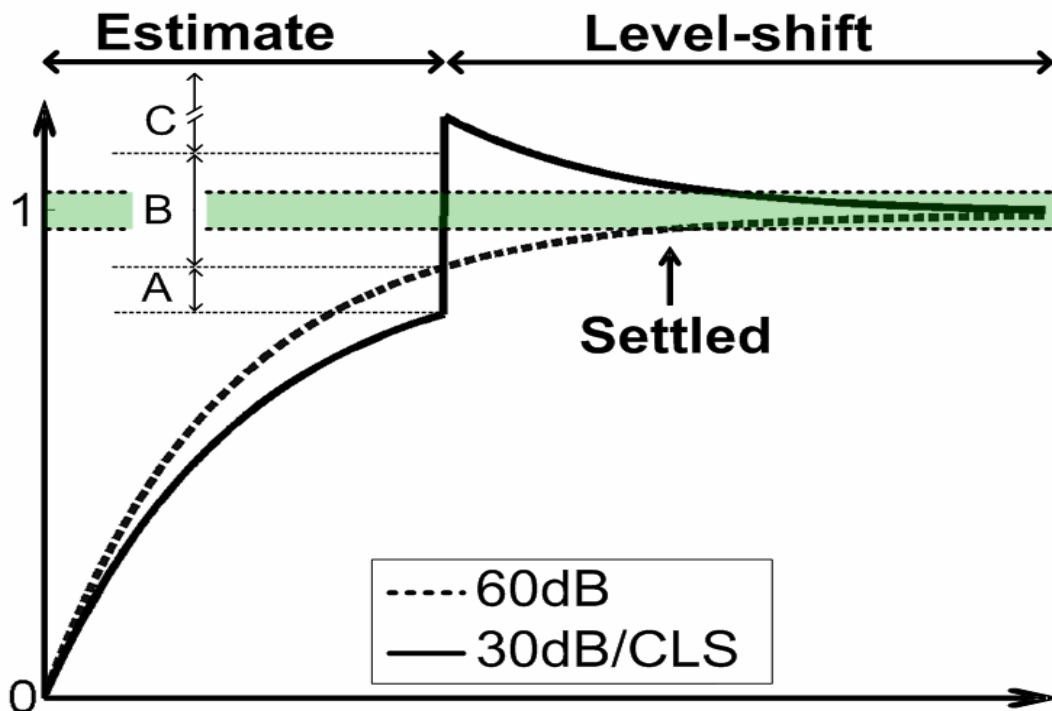


Figure 4-4 Transient response of a 30dB amplifier using CLS compared to conventional 60dB op-amp

4.7 Split-CLS

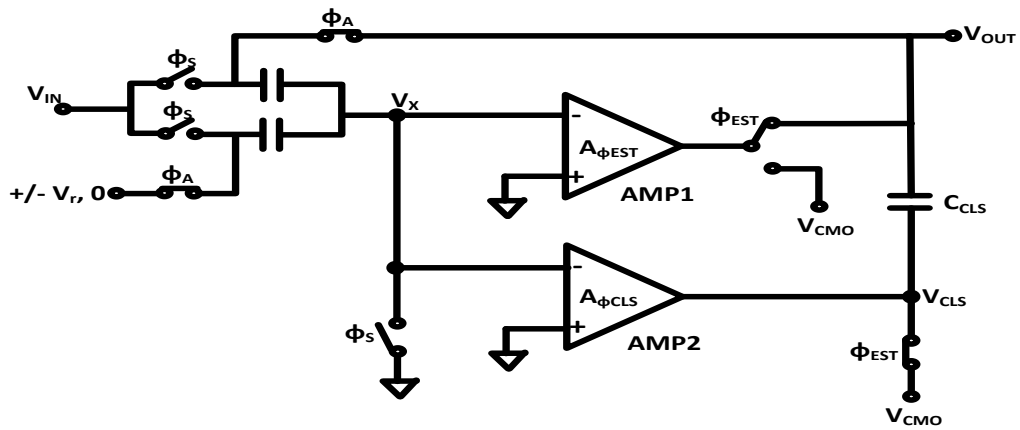
CLS on its own can reduce the power consumption and can enable design in lower voltage supplies. But a modification to it, called “split-CLS” [28] can address the tradeoffs between “signal swing and gain” and between “slew rate and gain”.

Split-CLS relies on the essential operation of CLS itself and takes it a step further. CLS operation can be intuitively thought of as having three steps: 1) sample the input, 2) provide a rough estimate, 3) subtract the rough estimate and settle to the accurate value.

Thus it becomes intuitive that the op-amp not being used to sample the input does not require high gain and bandwidth. It does need to be able to charge up the attached load capacitances during this instant. It then becomes clear that the amplifier needs to be optimized for slew rate and can be relaxed in terms of gain and bandwidth in this operation. During the fine-settling phase, the amplifier needs to fine-settle the final output which is already very close to the accurate value, thus it requires very little signal swing and slew rate and thus can be optimized for gain and bandwidth. The gain now is equal to the gain of the amplifier in both of the phases.

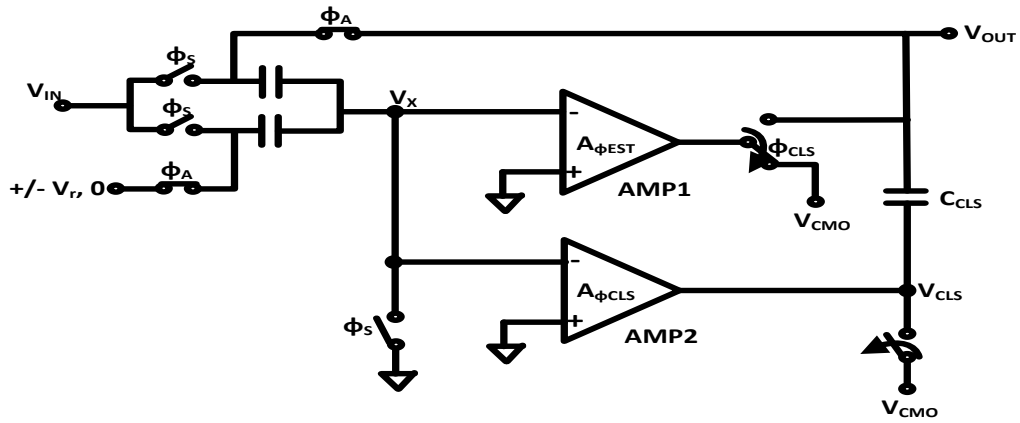
These two different operations can now be performed by two specialized amplifiers, hence the name “split”. The estimation amplifier can be a simple folded cascode or active-load differential amplifier that has good output swing capability and slew rate. The fine-settling amplifier can be a triple-stack telescopic cascode that provides enough gain and bandwidth. It must be noted that

both the amplifiers are low specification amplifiers and the power they consume is much less compared to the power consumed by a 80 dB, 455 MHz, 2 V signal-swinging amplifier that would be needed in a standard pipeline ADC. The design also does not need large capacitors for amplifier stability compensation nor does it suffer from any bandwidth or power penalties. Thus this technique enables design with robust low performance amplifiers that dissipate low amounts of power. The split-CLS architecture is shown in Figure 4-5.



ϕ_S – Sampling Phase; ϕ_A – Amplification Phase ($\phi_{EST} + \phi_{CLS}$)

(a) Estimation Phase



ϕ_S – Sampling Phase; ϕ_A – Amplification Phase ($\phi_{EST} + \phi_{CLS}$)

(b) Level Shifting Phase

Figure 4-5 Split CLS structure during the a) estimation and b) level-shifting phases.

The Split-CLS technique also has an advantage in that it removes any signal spiking behavior that may occur due to parasitic capacitances at the output of the amplifier between the estimate and level shift phase [28]. This removes reliability concerns during long space missions.

4.8 Proposed Op-amp Sharing in Split-CLS

The CLS operation as described above can be split into these three modes: sampling, estimation, and fine-settling. The op-amp as a block is needed only during the estimation and fine settling phases. That is, it is not needed during the sampling phase. In the split-CLS technique as explained earlier, the estimation amplifier is active only during the second phase and is idle during the sampling and fine-settling phase. In the same way, the fine-settling amplifier is idle during first two phases namely sampling and estimation phases, respectively. Thus, to use these amplifiers effectively an op-amp sharing technique is proposed which shares the two amplifiers across three stages. This greatly reduces the number of amplifiers from six (without op-amp sharing) to only two (with op-amp sharing). This technique thus enhances the advantages of the Split-CLS in terms of power and area by a large factor. The three stages along with their phases and amplifiers used are given below in Figure 4-6. Figure 4-6 shows the proposed op-amp sharing in split-CLS with the help of three 1.5 bit MDAC stages. This saves 20% more power than just CLS [29].

Memory effects are to be expected with this type of scheme. However, since the split-CLS is being used, at the end of the level shifting phase the input

voltage of the fine settling amplifier would be closer to the common mode level. Hence the charge stored on the gate capacitance of the input transistor pairs

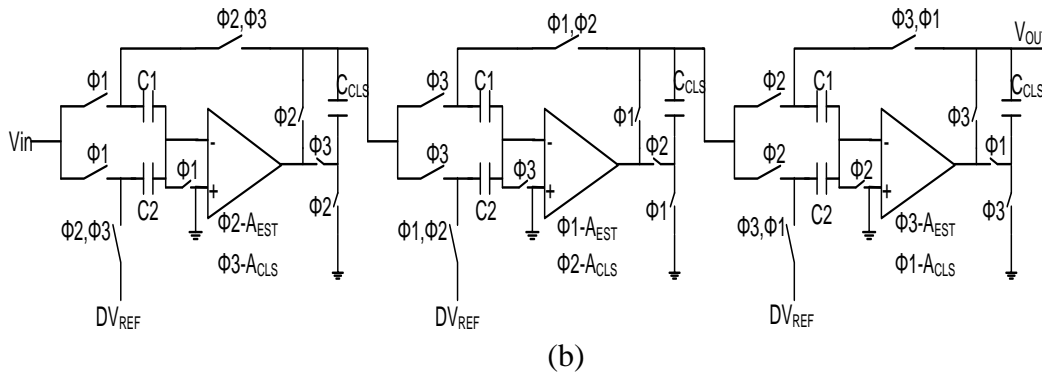
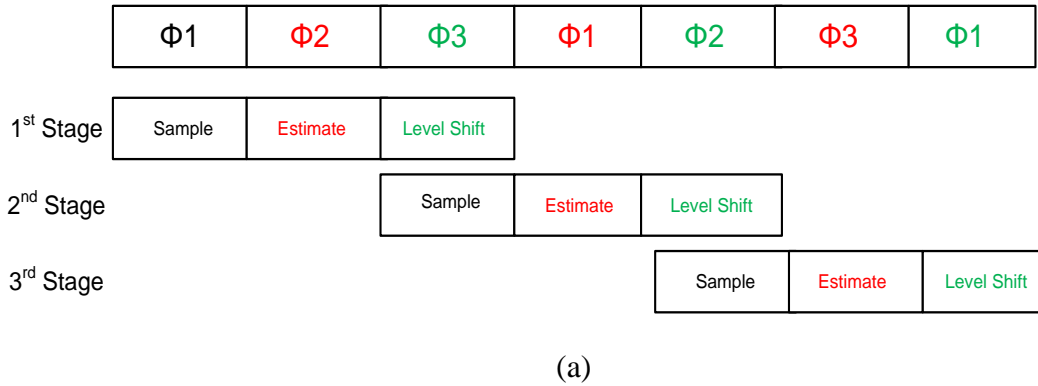


Figure 4-6 Split-CLS with op-amp sharing (a) Three stages with their corresponding phases (b) Three 1.5bit stages with op-amp sharing

will have a negligible effect. In the case of estimation amplifier, since only a rough estimate has been performed using this amplifier during estimation phase, memory effects would be minimal. For this reason, there is no need for any extra reset phase that would have been required otherwise if we wanted to deploy op-amp sharing in a conventional method.

5 CMOS IMPLEMENTATION

This chapter focuses on the circuit level implementation of switches (bootstrapped and a normal transmission gate), two different OTAs for the estimation and fine settling phases and a comparator used in the sub-ADC block. It then concludes with the digital error correction logic and the power calculation. The design is aimed at a minimum speed of 25MSPS at a typical supply of 1.2V. Circuit level analysis, design and simulation results are presented for each major circuit block.

5.1 Switch Design

Generally the threshold voltage of MOS transistors does not scale well with the supply voltage, and it becomes a large portion of the supply voltage leading to problems when MOS transistors are used as switches at low voltages. In this thesis, very low-voltage switched capacitor operation has been achieved using a special low-voltage bootstrapped switch [30]. The basic idea of this switch is demonstrated in Figure 5-1. The signal switch is transistor MNSW while the five additional switches S1-S5 and the capacitor C_{offset} constitute the bootstrap circuit. The clock signal Φ_2 switches S3 and S4 charging the capacitor to Vdd while switch S5 fixes the gate voltage of MNSW to Vss to make sure that the transistor is in the off state. Clock signal Φ_1 switches S1 and S2 connecting the precharged capacitor between the gate and the source of MNSW such that its gate-source voltage V_{GS} is equal to the voltage across the capacitor. This switch configuration allows rail-to-rail signal switching since the gate-source voltage is

always constant during Φ_1 and independent of the input signal. A transistor-level implementation of the bootstrapped switch, which is fully compatible with modern low-voltage CMOS processes, is given in Figure 5-2.

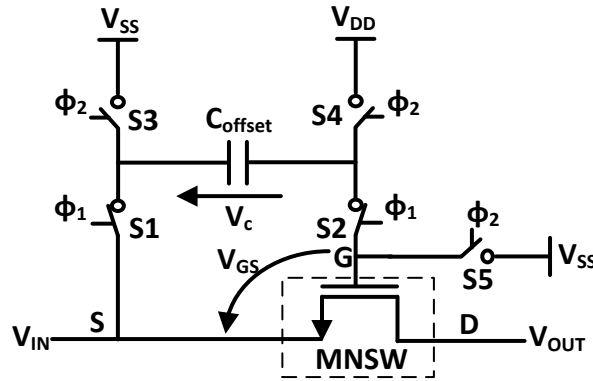


Figure 5-1 Basic switch bootstrapping circuit

Transistors MNI, MP2, MN3, MP4 and MNS correspond to the five ideal switches S1- S5 shown in Figure 5-1, respectively. Additional transistors and modified connectivity shown in Figure 5-2 were introduced to extend all switch operations from rail to rail while limiting all gate-source voltages to V_{DD} . It is evident that the worst case input signal (with respect to switch operation) is that of $V_{in} = V_{DD}$ which is the value attributed to V_{in} in the following discussion. An apparent problem is that of the n-transistor MNI which has to switch V_{DD} . This is the same problem as that of MNSW. The gate of MNI is tied to that of MNSW where a gate-source potential of V_{DD} assures its high conductivity during Φ_1 . The gate potential then drops to zero during Φ_2 , to cut off both transistors.

Additional problems arise at nodes B and G as their voltages reach $2V_{DD}$: First of all, transistor MP4 must remain OFF during Φ_1 in order not to lose the charge stored on C_{offset} during Φ_2 . If the clock is used to drive it as shown in

Figure 5-1, its gate-source voltage would be $-V_{DD}$ and the transistor would not be able to be turned OFF. This is why its gate is connected to node G which provides a voltage of $2V_{DD}$ during Φ_1 , cutting-off the transistor, and a voltage of V_{SS} during Φ_2 which ensures its high conductivity. Secondly, transistor MP2 has a technological problem. Using the clock to drive it as shown in Figure 5-1, its gate-source voltage would be $-2V_{DD}$ during Φ_1 . In Figure 5-2 a solution to this problem is proposed; transistor MN6 is used to connect the gate of MP2 to node A thus keeping its gate-source voltage equal to $-V_{DD}$ (the voltage across C_{offset}) during Φ_1 . During Φ_2 , transistor MP6 connects it to V_{DD} turning it OFF.

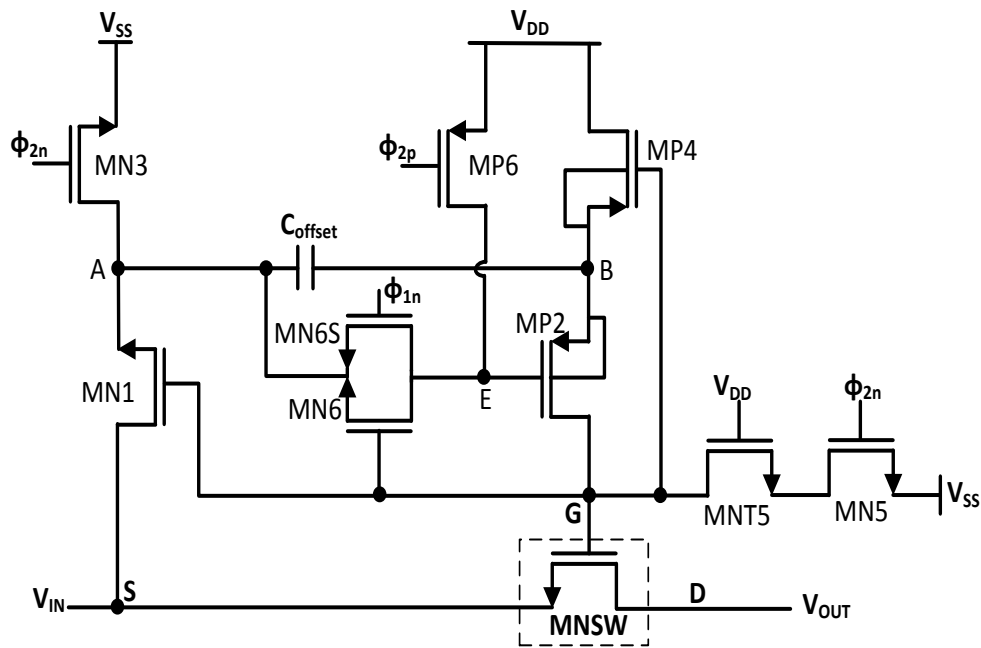


Figure 5-2 Transistor-level implementation of the bootstrapped switch

The gate of n-transistor MN6 is tied to node G to keep it conducting as the voltage on node A rises to V_{DD} during Φ_1 . Therefore a dependency loop is present. In order that MN6 conducts, it must have a sufficient gate-source voltage,

i.e., MP2 must then be conducting. Transistor MN6S is then necessary as a startup to force transistor MP2 to conduct. The clock is used to drive MN6S as it is assumed to conduct only when the voltage of node A is close to zero (which is the case at the beginning of Φ_1). When MP2 conducts the voltage on node G rises to $2V_{DD}$ while that on node A rises to V_{DD} thus MN6S turns OFF while MN6 remains ON.

Finally, transistor MNTS has been added in series with MN5 to prevent the gate-drain voltage of the latter from reaching $2V_{DD}$ during Φ_1 . The bulk of MNTS is however tied to V_{SS} . During Φ_1 when it is OFF, its drain-bulk diode junction voltage reaches a reverse bias voltage of $2V_{DD}$. This must be compatible with the technology limits. It should be noted that for an n-well process, the bulk of transistors MP2 and MP4 must be tied to the highest potential, i.e. node B, and not to V_{DD} .

Bootstrap switches are used in the critical (signal) path of the first stage in order to increase linearity. The above switch configuration is chosen since none of the terminal voltages (V_{gs} , V_{ds} , V_{gd}) exceed V_{DD} even with a rail-rail input swing [31]. The gate-bulk voltage of the input switch can go above V_{DD} and hence the input NMOS is replaced with triple well structure. This gives better isolation and also high linearity. Thus the switch has higher reliability and linearity. The achieved R_{on} value is almost flat for the entire input range and is close to 20 ohms. Since R_{on} is almost constant irrespective of the input voltage level, it helps in improving the linearity. The output spectrum of bootstrapped

switch is shown in Figure 5-3 and it can be clearly seen that the linearity is high equal to 94dB higher than that of the required linearity for 12 bits.

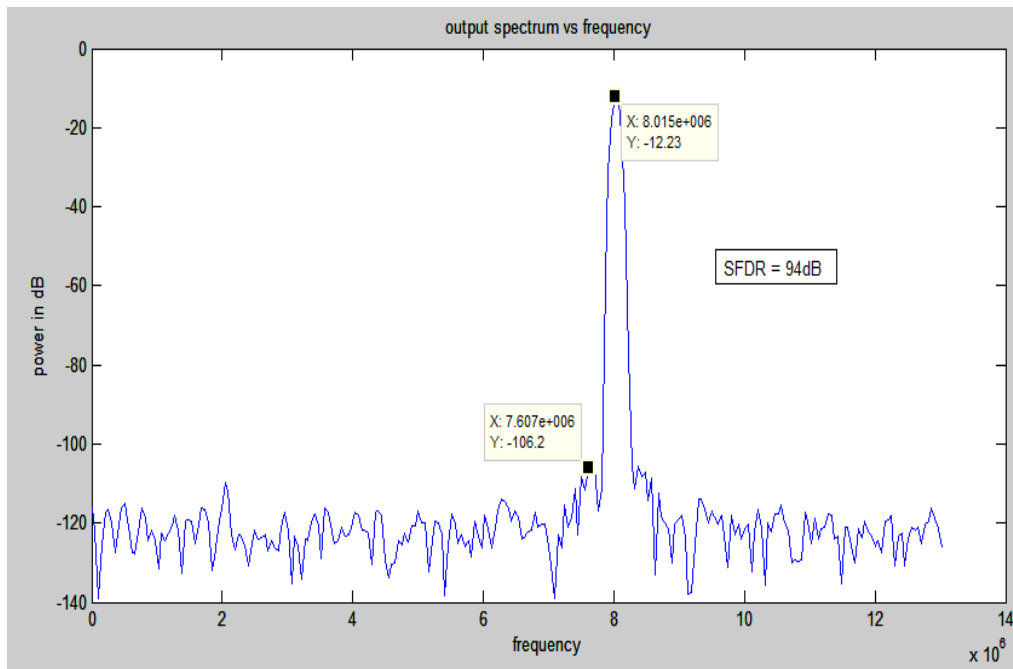


Figure 5-3 Linearity of bootstrapped switch

5.2 Transmission gate

For the switches that are not as critical as the first stage signal path switches, bootstrapped switches are not required since the linearity requirement is not as stringent. However, if a NMOS transistor is used, the output voltage cannot charge to the full scale value of the input and if a PMOS transistor is used, then the output capacitor will not be able to sample any input values less than the threshold voltage of the PMOS transistor. The CMOS transmission switch solves the problem. It does this by using a NMOS and PMOS switch in parallel as shown in Figure 5-4. Therefore when the two transistors are combined the switch

resistance will remain somewhat constant across the input voltage range. Using a CMOS transmission switch for the sampling switch helps keep the

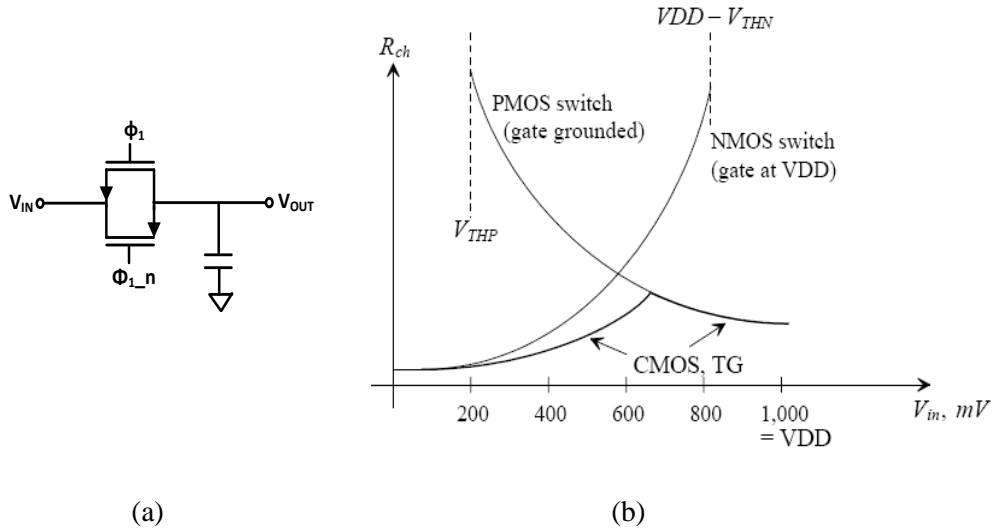


Figure 5-4 (a) Sample and hold network with CMOS transmission gate (b) ON-resistance of a CMOS transmission switch.

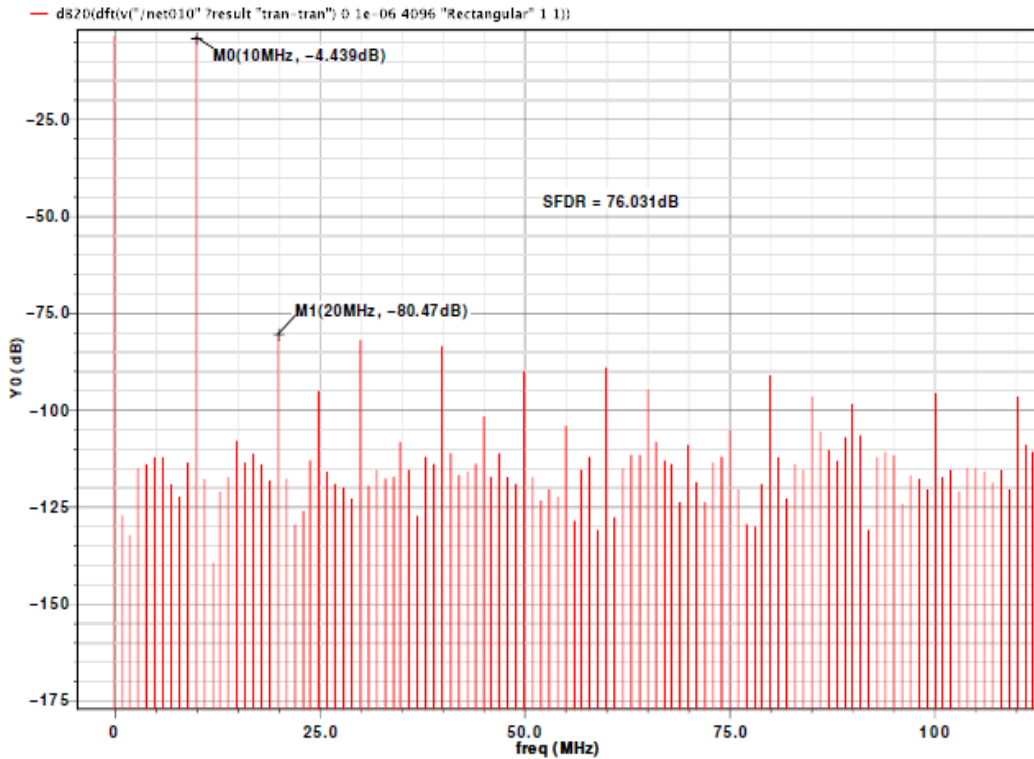


Figure 5-5 Linearity of transmission gate switch

on-resistance across the input range somewhat constant and allows the circuit to fully sample the complete input voltage range [5]. The linearity of the switch is given in Figure 5-5.

5.3 Operational Trans-conductance Amplifiers (OTAs)

As discussed earlier for split CLS with op-amp sharing, two amplifiers are required for three stages of pipelined ADC – one for the estimation phase and other for the fine settling phase.

It was discussed previously, that the estimation amplifier needs to have a higher slew rate with the relaxed specification on gain and bandwidth. On the other hand, the fine settling phase should be able to settle to the required accuracy and hence needs to have a higher gain bandwidth product. It should be noted that for the reasons previously discussed in the section 4.5 the fine-settling amplifier does not need to have a higher output swing. The following calculation shows the gain and bandwidth required for a 12 bit 25MSPS pipelined ADC.

With the 2.5 bit stage as the first stage, the required gain and bandwidth can be calculated from the maximum tolerable gain and settling error as follows [25]:

$$\frac{1}{1+A\beta} = \frac{1}{2} * \frac{1}{2^{10}} \rightarrow \text{from gain error with half LSB accuracy} \quad (5-1)$$

$$e^{-\frac{t}{\tau}} = \frac{1}{2} * \frac{1}{2^{10}} \rightarrow \text{from settling error with half LSB accuracy} \quad (5-2)$$

Where, $\beta = 1/5$ for 2.5 bit stage and $t = T/3 = 13.33\text{ns}$ (time available for one phase in the case of 25MSPS). The calculated gain and unity gain frequency comes to 81dB and 455MHz, respectively.

cascode amplifier. The folded cascode amplifier used during the estimation phase is a PMOS input folded cascode amplifier with continuous time common mode feedback circuit to set the common mode of the differential outputs. The frequency response is given in Figure 5-7 which shows that gain achieved is 42dB with phase margin of 82 degrees.

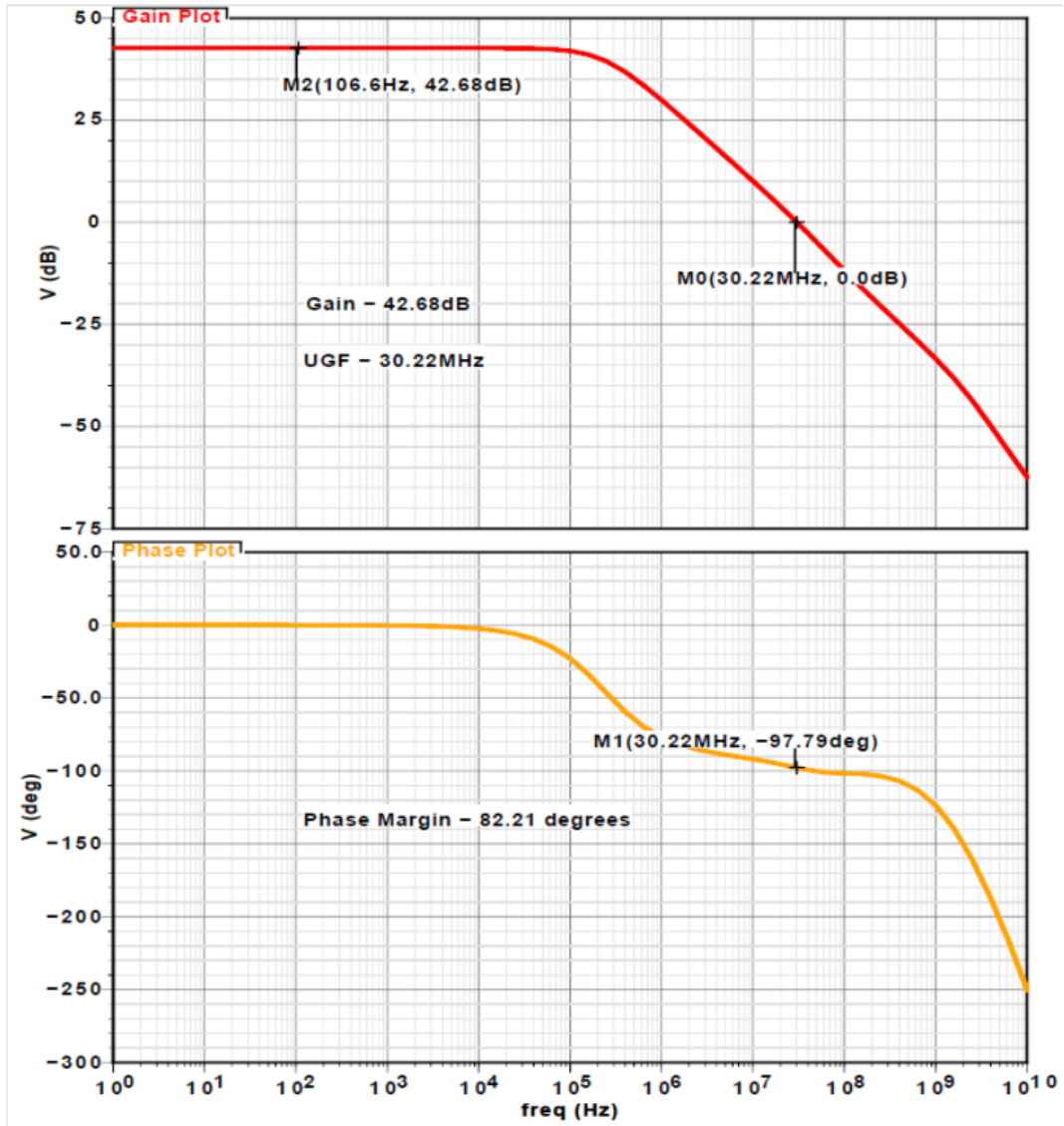


Figure 5-7 Frequency response of estimation amplifier

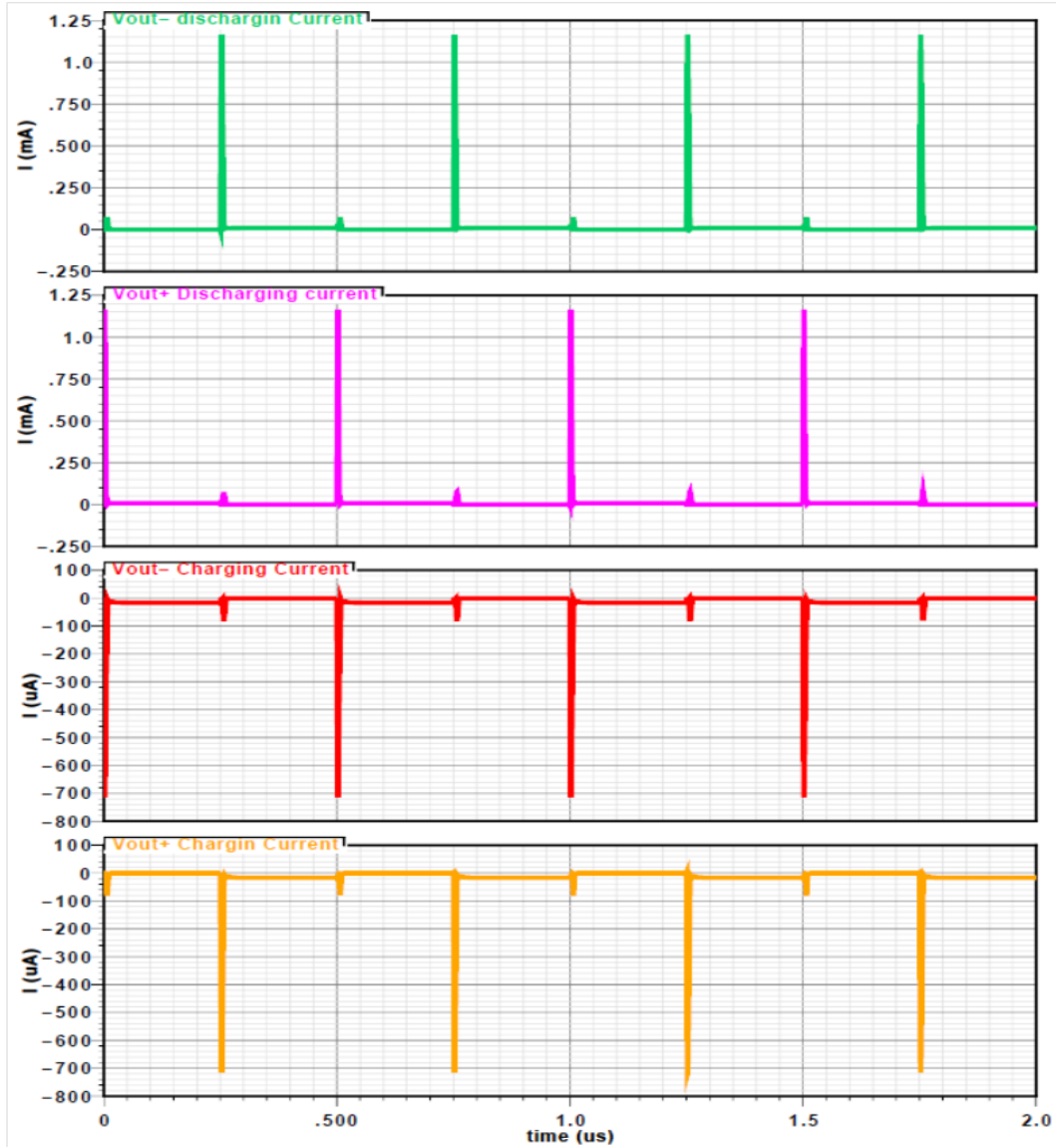


Figure 5-8 Charging and discharging current with slew rate enhancement circuit

Since the estimation amplifier needs to have a larger current drive during the transients, a slew rate enhancement technique is used with the folded cascode amplifier as shown in Figure 5-6. This auxiliary circuit will be active only during the input transients providing large amount of current and will be off consuming very little current otherwise. Since the circuit is active only during the transients,

it does not have an effect on the small signal ac response during the normal operation [32].

The large amount of charging and discharging current at the output nodes which are required to achieve higher slew rate is shown in the Figure 5-8. As expected, the current is very low during the normal operation other than the transients (essentially only the quiescent current) and hence helps in power reduction. The step response of the folded cascode with slew rate enhancement is given in Figure 5-9 and shows that slew rate is greatly enhanced for the folded cascode amplifier which is the most critical requirement during the estimation phase.



Figure 5-9 Step response of estimation amplifier with and without slew rate enhancement

low power supply has given only 40dB of gain in the typical case. Although the gain required from this amplifier is 40dB (i.e. the collective gain $A_{EST} + A_{CLS} > 80\text{dB}$) and a single stage barely meets this, it is better to have gain greater than 100dB [28]. This will make sure that the accuracy is met across Process, Voltage and Temperature..

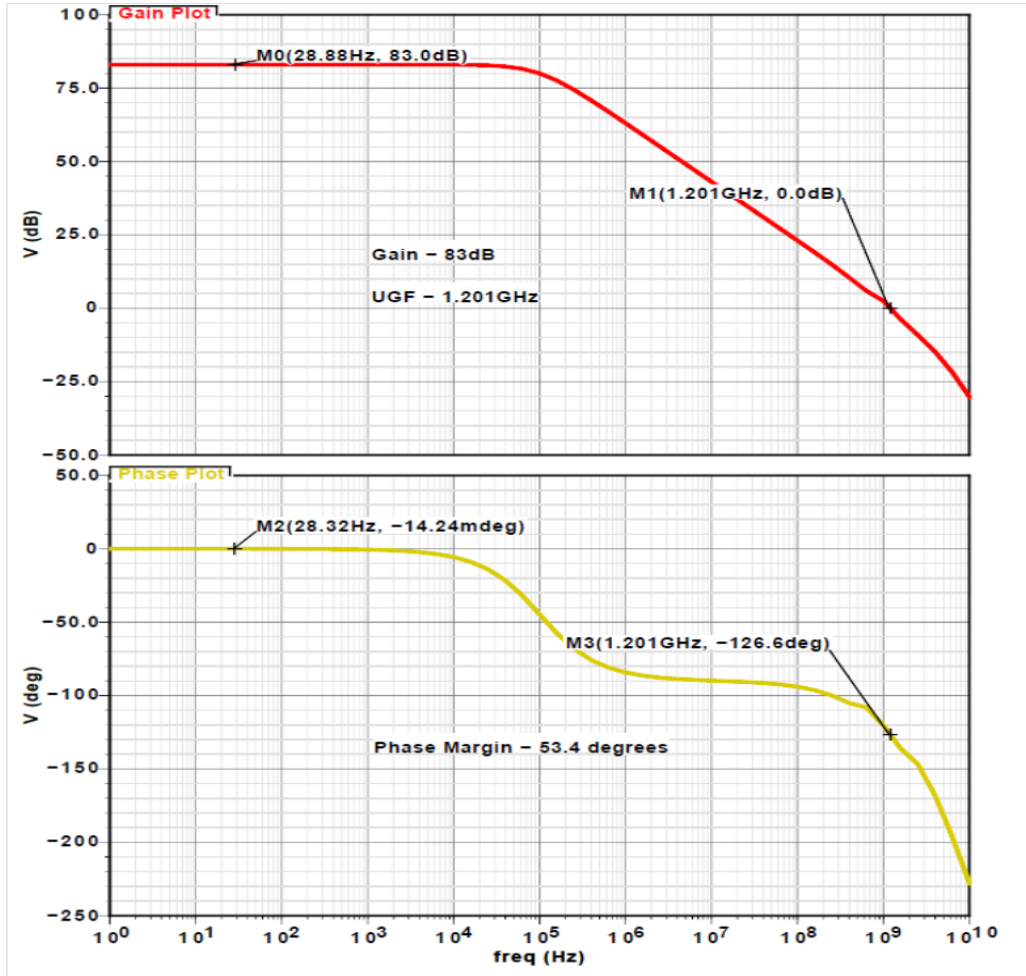


Figure 5-11 Frequency response of fine settling amplifier

Adding to this, since op-amp sharing has been used across the three stages, it is good to have higher gain than required to combat the memory effects. Otherwise, an additional phase should be used solely for resetting the amplifier

which will decrease the available conversion time and also adds complexity. Keeping this in mind, a gain boosting amplifier is chosen to achieve high gain without deteriorating the gain bandwidth product much [10]. The gain boosted amplifier used is given in the Figure 5-10. Thanks to the Split-CLS technique, the output swing of this amplifier does not need to be high. Care has been taken that the pole-zero doublet occurs after the Unity Gain Frequency UGF that it doesn't affect the settling time. The gain achieved is 83dB with the unit gain frequency of 1.2GHz with capacitance load of 350fF which will meet the required specifications across PVT. The frequency response of the amplifier is given in Figure 5-11.

5.4 Comparator

The next major block in pipelined stage is the comparator which is used in sub-ADCs. As all the stages used in the pipelined ADC are 2.5 bits, each stage will have six comparators. Thus the power consumed by a single comparator plays an important role in overall power consumption. Having said that, a dynamic comparator is preferred over a switched capacitor input comparator (preamp + latch) in terms of power consumption. Also, the switched capacitor input comparator has loaded the previous stage heavily resulting in a settling error. However, in terms of accuracy, a switched capacitor input comparator will be better than a dynamic comparator, which has a kick back noise. To reduce the error from the kick-back in a dynamic comparator, a kick-back compensated comparator is used. It is shown in the Figure 5-12.

The operation of this comparator is as follows: When the clock is low the comparator is in equalization mode, disconnecting the pull-down networks from ground while equalizing the two output nodes. The two cross coupled inverters will then pull the two nodes towards $V_{DD}-V_{th}$. When the clock goes high the circuit goes into regenerative mode and current starts to flow through the pull-down paths. A voltage difference on the inputs will be translated to a current imbalance causing one of the output nodes to be discharged faster than the other.

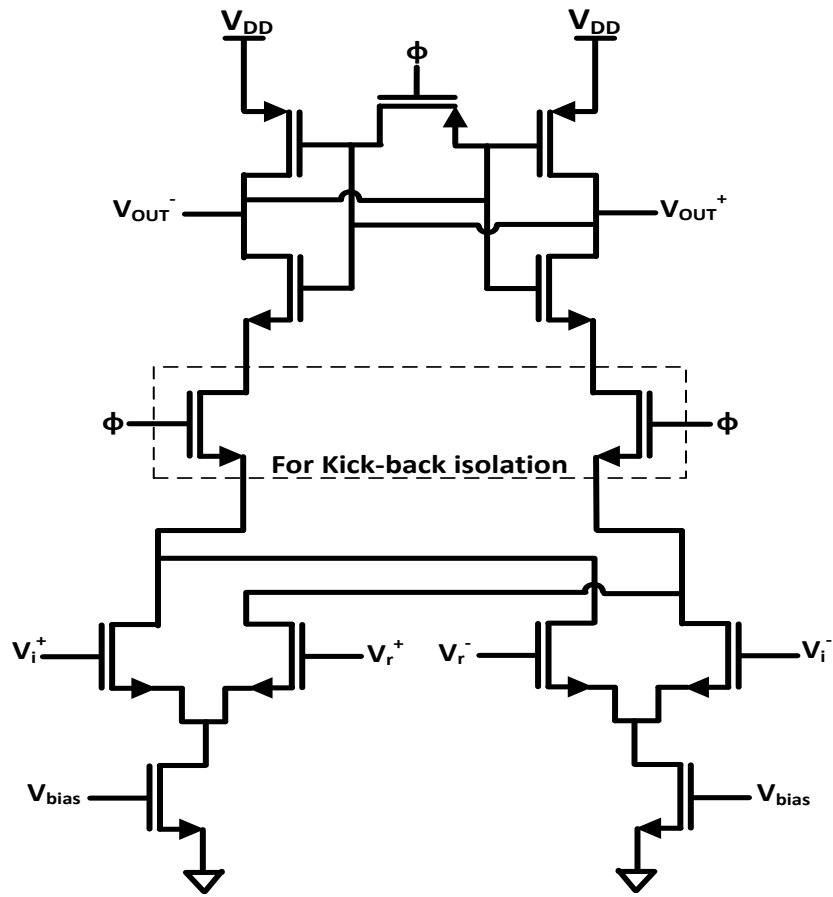


Figure 5-12 Kick-back reduced comparator

When the two output nodes approach the trip-point of the two cross-coupled inverters, the voltage difference will be amplified to full swing. This

comparator architecture is very suitable for low power applications since large currents are only drawn from the power supply during the decision time of the regenerative phase. To reduce the kick-back, the comparator is designed to reduce the voltage swing at the drain and source terminals of the input transistors [33].

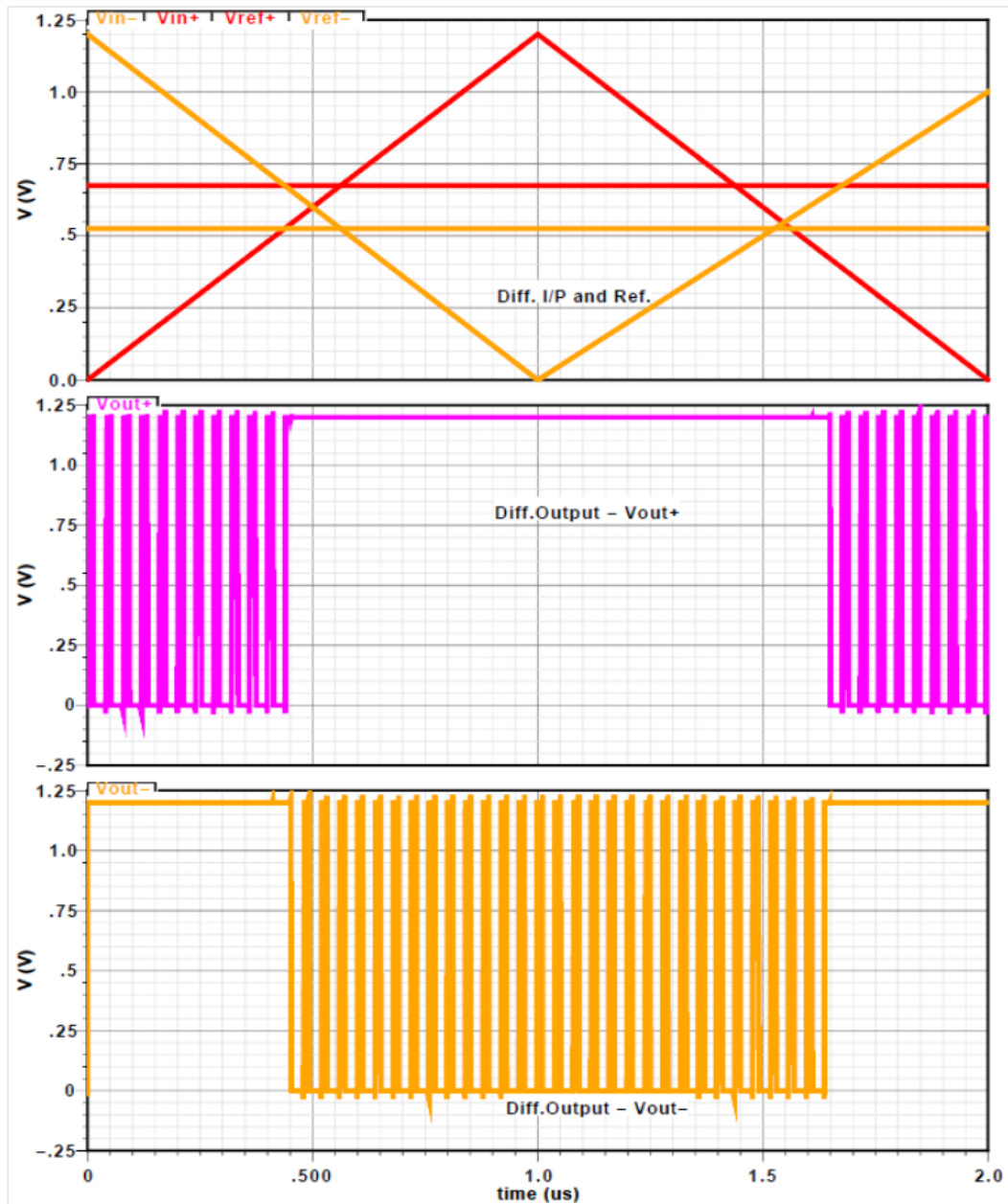


Figure 5-13 Differential comparator output for ramp input

The clocked transistors are placed between the cross-coupled inverter-pair and the input transistors preventing the drain and source terminals of the input transistors from being charged during the equalization phase. Feed-through from the clock still causes a pulse at the drain terminal of the input transistors, which will cause a kick-back to the inputs. The comparator output is shown in Figure 5-13 for differential inputs ramping V_{in+} and V_{in-} ramping from 0 to 1.2V and 1.2V to 0V respectively with the reference voltages V_{ref+} and V_{ref-} being at 675mV and 525mV.

5.5 Digital Error correction

The output from the analog pipeline is non-binary and has redundancy included, since the RSD algorithm is being used. The processing of a particular analog sample is distributed in time by the analog pipeline. This creates a problem since all the bits need to be run through the digital correction logic at the same time. In order to synchronize all the bits, D-flip-flops are used to delay the bits from each RSD stage such that they all arrive at the digital correction logic simultaneously.

Figure 5-14 shows a block diagram of the ADC with the delay flip flops and digital correction logic. Due to the mapping of the RSD stage output bits into a standard binary code format, addition is the only operation needed to perform the digital correction and is made up of 12 full binary adders.

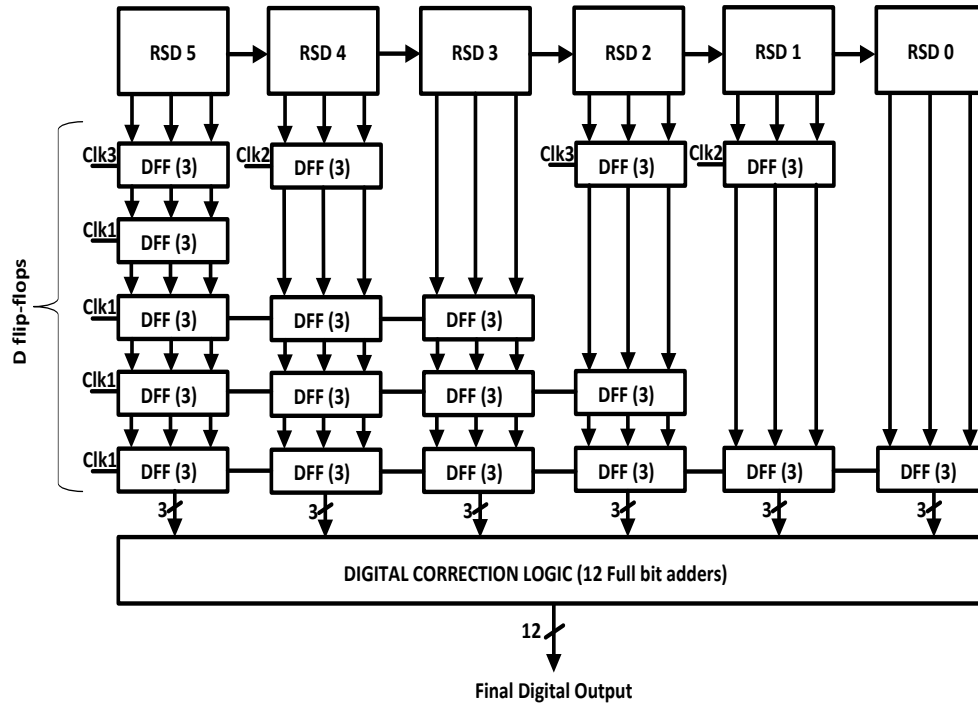


Figure 5-14 Top level block diagram of ADC with D-FF and digital correction logic

5.6 Power Calculation

The following calculation gives an idea about the overall power consumption from the analog parts of pipelined ADC. Major components that contribute to overall power consumption with their respective power consumption is given.

The total quiescent current in the gain boosted amplifier (including the two auxiliary gain boosting amplifiers) is 2.45mA. This gives the total power contribution from the fine settling amplifier of 2.94mW. In the same way, the quiescent current in the slew rate enhanced folded cascode amplifier is calculated to be 600uA. Thus the total power consumed by the estimation amplifier is 720uW. In the case of dynamic comparator, since static power consumption is

negligible, only dynamic switching power has been taken into account. The worst case dynamic power can be assumed as 10uW for 25MSPS [33].

Also, the last 3 stages need only lower specification amplifiers and hence power consumption from the two amplifiers used for last three stages will typically be low. Considering the design time trade-off, similar amplifiers used for the first three stages have been used for the last stages too. Thus the total power consumption from amplifiers and comparators comes to [34]

$$\text{Power} = 2.94 * 2 \text{ mW} + 720 * 2 \text{ uW} + 36 * 10\text{uW} = 8\text{mW} . \quad (5-3)$$

This gives the enough margins to accommodate the power from the other digital circuits, reference generators and clock buffers. The total power is expected to be less than 25mW including the power from buffers and digital circuits.

6 SIMULATION RESULTS

After integrating all the building blocks, simulations for the designed pipeline ADC are conducted at the transistor level. A 10-MHz input signal is sampled at 26MHz. Simulation results show that the designed pipeline ADC achieves the SNDR of 69.7dB, which demonstrates successful design of each individual building block. This chapter starts by showing the simulation results of a single stage ADC using split CLS that includes the output voltage signal showing $2V_{P-P}$ voltage swing and its FFT spectrum. It then extends to show the simulation results of a complete 1.2V 12 bit pipelined ADC and concludes with the measured results showing ADC's dynamic performance.

6.1 Single stage Split CLS

A single stage of a pipelined ADC is implemented without op-amp sharing. The first stage implemented is a 2.5bit stage and its Cadence implementation is shown in the Figure 6-1.

6.1.1 FFT Spectrum

The FFT of the output spectrum with different input frequencies is measured for 2048 samples and the corresponding SNDR, SFDR and ENOB are given in the Table 6-1. Windowing has been used to avoid spectrum leakage in the case of incoherent sampling and the window used for this particular design is 'blackman-harris'.

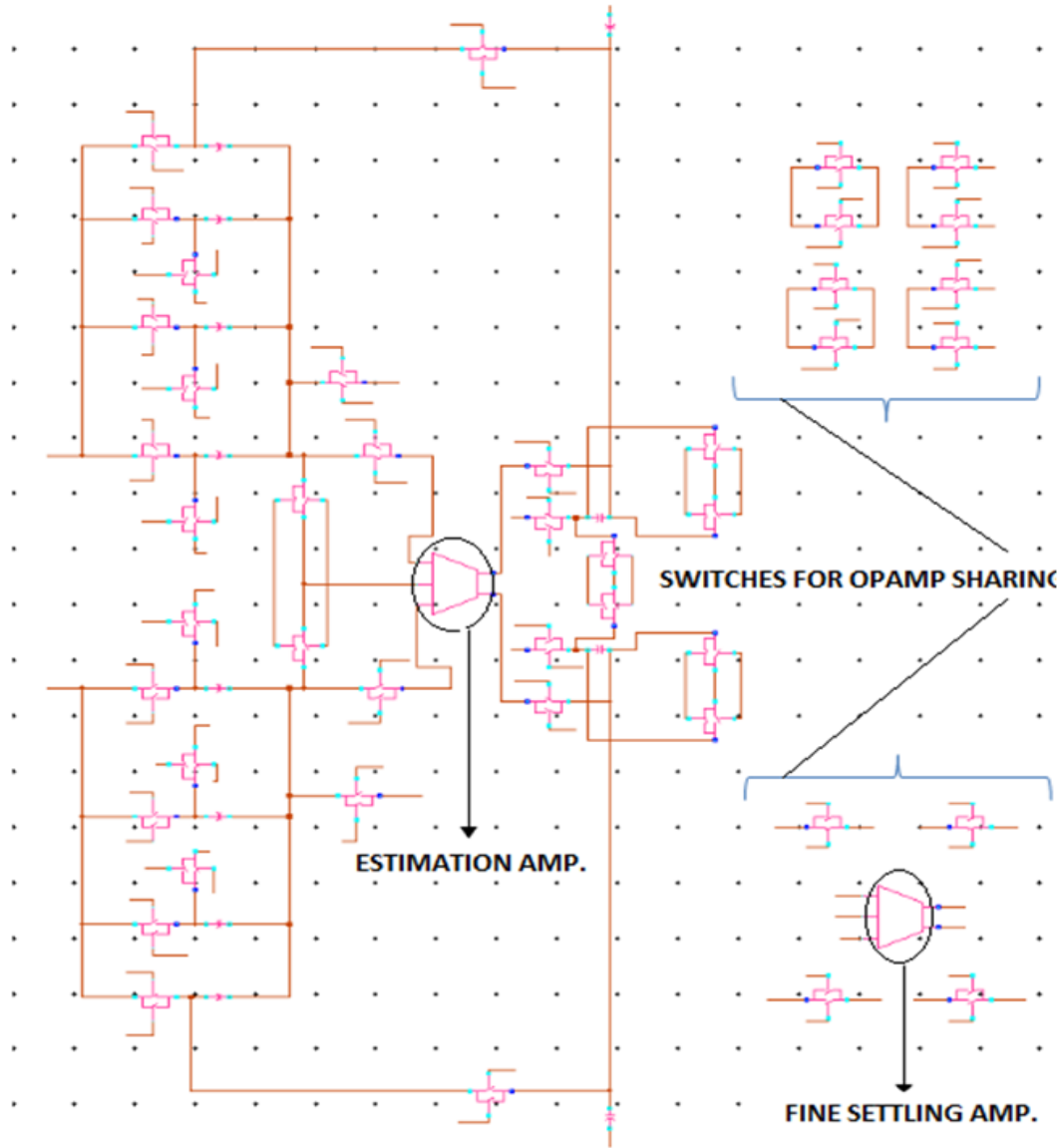
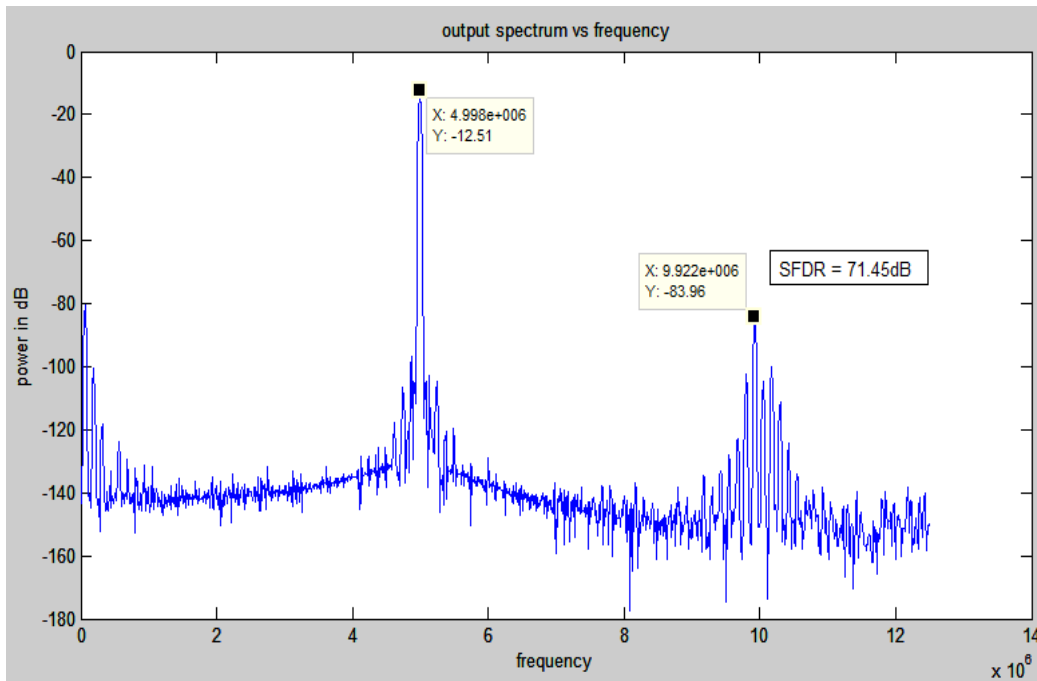


Figure 6-1 Single stage split CLS

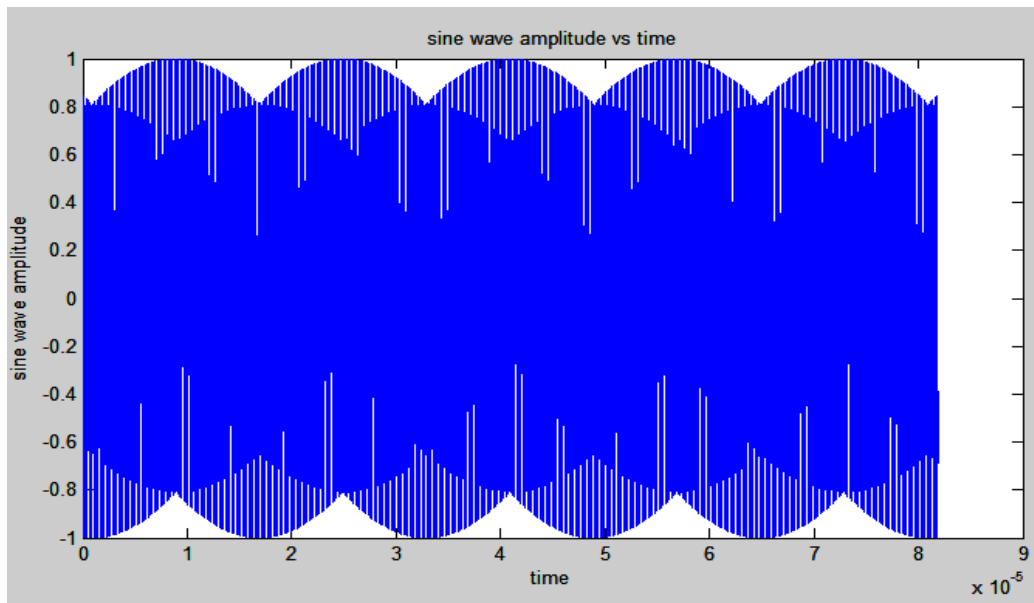
Figure 6-2 shows the output spectrum when the input frequency is 5MHz and the input signal is $250\text{mV}_{\text{P-P}}$ and the corresponding $2\text{V}_{\text{P-P}}$ output signal when configured for the closed loop gain of four. The voltage at the output of the first stage is also shown in the Figure 6-2.

Fin (MHz)	SFDR (dB)	SNDR(dB)	ENOB (bits)
5	71.45	66.52	10.8
8	74.6	72.07	11.7
12.5	67.47	66.48	10.78

Table 6-1 Dynamic performance of a single 2.5bit stage using Split-CLS.



(a)



(b)

Figure 6-2 (a) FFT Spectrum of single stage split-CLS (b) 2VP-P differential output.

6.2 1.2V 12 Bit 25MSPS Pipelined ADC

A complete pipelined ADC with the proposed op-amp sharing technique is constructed with six 2.5bit stages. The corresponding FFT output spectrum for a differential input voltage swing of $2V_{P-P}$ and with input frequency of 10MHz is shown in the Figure 6-3. The SFDR and SNDR are found to be 73.96dB and 69.70dB corresponding to the ENOB of 11.32 bits.

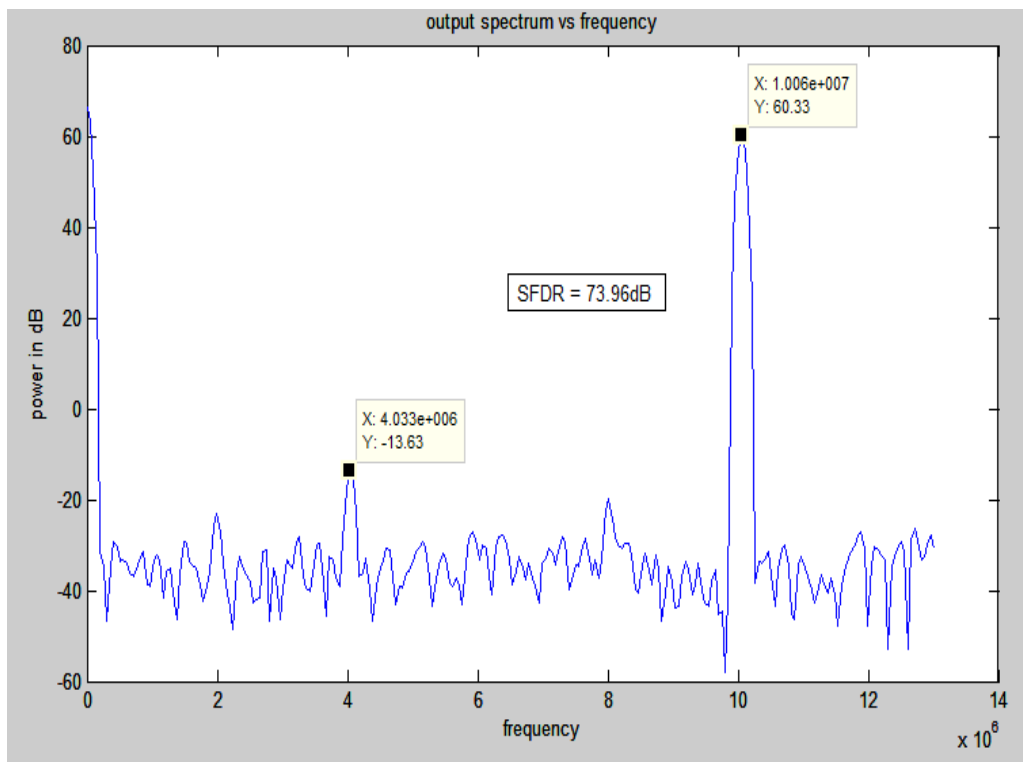


Figure 6-3 FFT Spectrum of 12 bit ADC.

6.3 ADC dynamic performance

The dynamic performance of the proposed ADC is measured by analyzing a Fast Fourier Transform (FFT) of the digital output codes as explained earlier. The performance of ADC is studied for different input frequencies with

differential input signal swing of $2V_{P-P}$ and with power supply of 1.2V. The SFDR, SNDR, and ENOB as a function of input frequency are shown in Figure 6-4 and Figure 6-5. The measured results are summarized in Table 6-2. The achieved specifications for the designed Pipelined ADC using the proposed technique are summarized in Table 6-3.

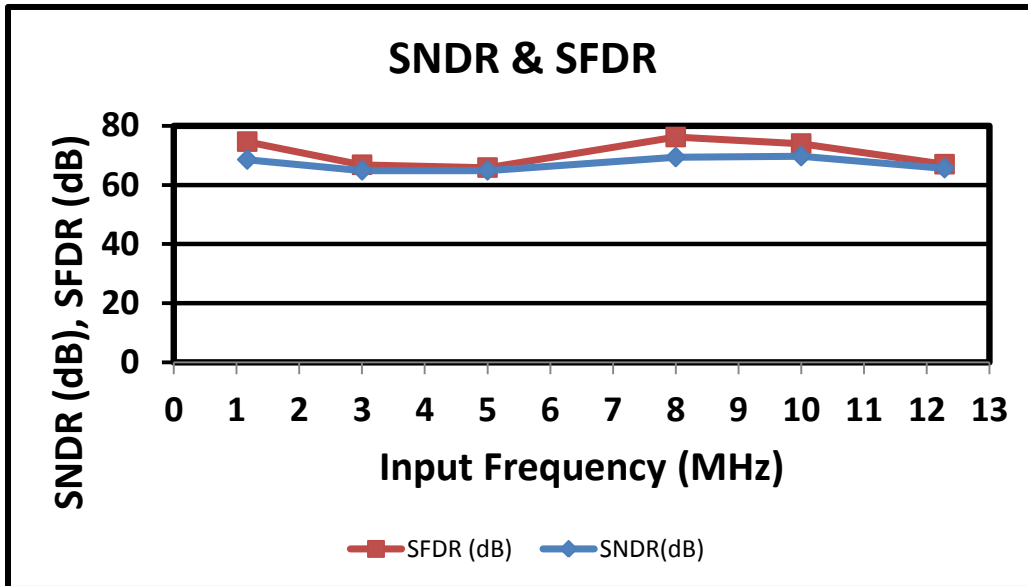


Figure 6-4 SNDR and SFDR for 12 Bit 25MSPS ADC up to Nyquist input frequency.

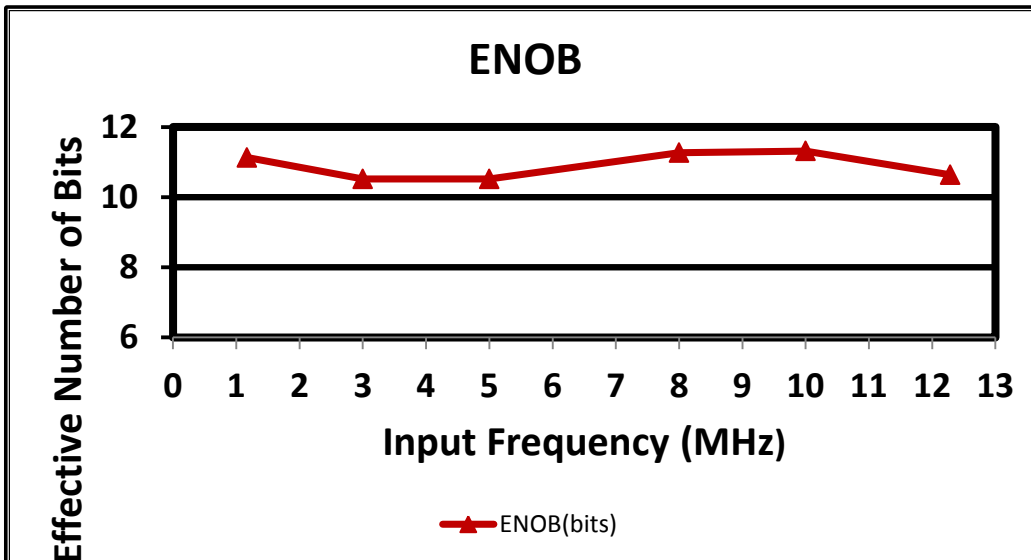


Figure 6-5 ENOB for 12 Bit 25MSPS A/D converter up to Nyquist input frequency.

Fin (MHz)	SFDR (dB)	SNDR(dB)	ENOB (bits)
1.169	74.62	68.5456	11.13
3	66.781	64.891	10.52
5	65.839	64.8825	10.52
8	76.17	69.3882	11.27
10	73.96	69.7018	11.32
12.286	66.971	65.6268	10.64

Table 6-2 Dynamic Performance of a 12bit ADC using Split-CLS with op-amp sharing

SNDR	69.7 dB
Power dissipation (analog)	8mW
Input voltage	2 V _{pp}
max INL/DNL	0.75 / 0.5 LSB
Technology	130nm IBM 8HP
Power Supply	1.2 V

Table 6-3 Achieved specifications of the pipelined A/D converter.

7 CONCLUSION

7.1 Conclusion

This thesis has presented the design of a 1.2V, 12-bit 25MSPS pipelined ADC in 130nm IBM8HP process. An op-amp sharing technique has been successfully implemented with a Split-CLS technique. The targeted specifications are met with the simulations in the schematic level and it has been shown that power consumption of the ADC using correlated level shifting is low. With the proposed technique, the power consumption has been further reduced (analog power less than 8mW) with a lesser number of op-amps and hence further increased the effectiveness of Split CLS architecture. Thanks to the Split-CLS technique, the designed ADC has demonstrated a performance of greater than 10.5 bits of accuracy over the entire input frequency range with 2V differential peak-peak voltage swing and with the power supply of 1.2V. The peak ENOB of the ADC is measured to be 11.32 bits and the ADC can be clocked up to 30MHz.

7.2 Future Work

The entire design has to be laid out and will be fabricated in IBM 130nm process. At the time of this documentation, the layout for the schematics has been started and will be used in the Large Hadron Collider once the chip is taped out. There are two possible areas of improvement in this design: 1) one possible improvement that could be realized for this design is on the fine settling amplifier. The bandwidth of this amplifier can be increased and as a result the speed of ADC

can be improved. The ADC is operating up to 30MHz and with the improvement it is expected to work up to 40MHz; 2) another improvement that could be realized is to use a lower specification amplifier for last three 2.5bit stages as they do not require the higher specification power hungry amplifiers used in the first three stages. This could result in the further reduction of power and hence result in increase of ADC's figure of merit.

REFERENCES

- [1] M. Waltari, "Circuit techniques for low voltage and high speed A/D converters", PhD Thesis, Helsinki university of technology, 2002.
- [2] B.Razavi, "Principles of Data Conversion System Design," IEEE Press, 1995.
- [3] Maxim, "Understanding Flash ADCs", <http://www.maxim-ic.com/app-notes/index.mvp/id/810>, Tutorial 810, 2010.
- [4] P. Scholtens and M. Vertregt, "A 6-b 1.6-Gsample/s Flash ADC in 0.18 μ m CMOS Using Averaging Termination", IEEE Journal of Solid-State Circuits, Vol. 37, No. 12, pp. 1599-1609, December 2002.
- [5] R. Baker, "CMOS – Circuit Design, Layout, and Simulation, Second Edition", Wiley-IEEE Press, 2008.
- [6] C. Liu, S. Chang, G. Huang and Y. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure", IEEE Journal of Solid-State Circuits, Vol. 45, No. 4, pp. 731-740, April 2010.
- [7] R. Schreier and G. Temes, "Understanding Delta-Sigma Data Converters", IEEE Press, 2005.
- [8] M. Kim, G. Ahn, P. Hanumolu, S. Lee, S. Kim, S. You, J. Kim, G. Temes, and U. Moon "A 0.9 V 92 dB Double-Sampled Switched-RC Delta-Sigma Audio ADC", IEEE Journal of Solid-State Circuits, Vol. 43, No. 5, pp. 1195-1206, May 2008.
- [9] H. Zhang, Q. Li and E. Sanchez-Sinencio "Minimum current/area implementation of cyclic ADC", IEEE Electronics Letters, Vol. 45, No. 7, pp. 351-352, March 2009
- [10] K. Bult and G. Geelen, "A fast-settling CMOS op amp with 90dB DC-gain and 116MHz unity-gain frequency", IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 108-109, 1990.
- [11] S. Hisano and S. Sapp, "A 16-Bit, 20MSPS CMOS Pipeline ADC with Direct INL Detection Algorithm", IEEE Custom Integrated Circuits Conference, pp. 417-420, 2003.
- [12] L. Sumanen, "Pipeline Analog-to-Digital Converters for Wide-Band Wireless Communications", PhD Thesis, Helsinki university of technology, 2002.

- [13] R. Tadepalli, “10 Bit, 15 MSPS, 1.2V, Pipelined Analog to Digital Converters”, Master’s Thesis, Arizona State University, May 2004.
- [14] B. Ginetti, P. Jespers, “A 1.5 Ms/s 8-bit Pipelined RSD A/D Converter,” IEEE European Solid-State Circuits Conference Digest of Technical Papers, pp. 137–140, Sep. 1990.
- [15] J.E. Robertson, “A new class of digital division methods”, IRE Transactions on Electronic Computers, Vol. EC-7, pp. 218-222, Sep. 1958.
- [16] K. Hwang, “Computer Arithmetic: principles, architecture and design”, Wiley, 1979.
- [17] L. Cascio, “A 10 Bit, 30 MegaSample Per Second, Pipelined Analog-to-Digital Converter”, Master’s Thesis, Arizona State University, December 2002.
- [18] B.Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw-Hill, 2001.
- [19] M. Yoshioka, M. Kudo, K. Gotoh, Y. Watanabe, “A 10b 125MS/s 40mW Pipelined ADC in 0.18um CMOS”, IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 282-598, 2005.
- [20] C. Hu, “Future CMOS Scaling and Reliability,” Proc. of the IEEE, pp. 682-689, 1993.
- [21] Y Chiu, P. Gray, and B. Nikolic “A 14-b 12-MS/s CMOS Pipeline ADC With Over 100-dB SFDR”, IEEE Journal of Solid-State Circuits, Vol. 39, No. 12, pp. 2139-2151, December 2004.
- [22] M. Pelgrom, A. Duinmaijer, A. Welbers, “Matching Properties of MOS Transistors”, IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, pp. 1433-1439, October 1989.
- [23] K. Nagaraj, T. Viswanathan, K. Singhal, and J. Vlach, “Switched-Capacitor Circuits with Reduced Sensitivity to Amplifier Gain”, IEEE Transactions on Circuits And Systems, Vol. CAS-34, No. 5, pp. 571-574, May 1987.
- [24] B. Gregoire, and U. Moon, “An Over-60 dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Op-amp With Only 30 dB Loop Gain”, IEEE Journal of Solid-State Circuits, Vol. 43, No. 12, pp. 2620-2630, December 2008.

- [25] C. Cho, "A Power Optimized Pipelined Analog-To-Digital Converter Design in Deep Sub-micron CMOS Technology", PhD Thesis, Georgia Institute of Technology, December 2005.
- [26] B. Gregoire, "Correlated Level Shifting as a Power-Saving Method to Reduce the Effects of Finite DC Gain and Signal Swing in Op-amps", PhD Thesis, Oregon State University, Dec. 2008.
- [27] T. Musah and U. Moon, "Correlated level shifting technique with cross-coupled gain-enhancement capacitors", IEEE Electronics Letters, Vol. 45, No. 13, pp. 672-674, June 2009.
- [28] B. Hershberg, S. Weaver, and U. Moon, "Design of a Split-CLS Pipelined ADC with Full Signal Swing Using an Accurate But Fractional Signal Swing Op-amp", IEEE Journal of Solid-State Circuits, Vol. 45, No. 12, pp. 2623-2633, December 2010.
- [29] B. Sivakumar, E. Mikkola, "A 12b 125Msps Robust Rad-Hard Pipelined ADC", Internal Report, Ridgetop Group Inc., August 2011.
- [30] M. Dessouky and A. Kaiser, "Very Low-Voltage Digital-Audio $\Delta\Sigma$ Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping", IEEE Journal of Solid-State Circuits, Vol. 36, No. 3, pp. 349-355, March 2001.
- [31] M. Dessouky and A. Kaiser, "Input switch configuration suitable for rail-to-rail operation of switched op-amp circuits", IEEE Electronics Letters, Vol. 35, No. 1, pp. 8-10, January 1999.
- [32] K. Nagaraj, "CMOS Amplifiers Incorporating a Novel Slew Rate Enhancement Technique", IEEE Custom Integrated Circuits Conference, pp. 11.6/1-11.6/5, 1990.
- [33] T. Sundström, and A. Alvandpour, "A Kick-Back Reduced Comparator for a 4-6-Bit 3-Gs/S Flash ADC in a 90nm CMOS Process", in Proc.Int. Conf. Mixed Design of Integrated Circuits and Systems, pp. 195–198, 2007.
- [34] J. Goes, J. Vital, and J. Franca, "Systematic Design for Optimization of Pipelined ADCs", Kluwer Academic Publishers, 2001.