Design of NMOS and CMOS Thin Film Transistors and Application to Electronic Textiles

by

Korhan Kaftanoglu

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Graduate Supervisory Committee:

David R. Allee, Chair
Michael Kozicki
Keith Holbert
Jann Paul Kaminski

ARIZONA STATE UNIVERSITY

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ABSTRACT

The field of flexible displays and electronics gained a big momentum within the recent years due to their ruggedness, thinness, and flexibility as well as low cost large area manufacturability. Amorphous silicon has been the dominant material used in the thin film transistor industry which could only utilize it as N type thin film transistors (TFT). Amorphous silicon is an unstable material for low temperature manufacturing process and having only one kind of transistor means high power consumption for circuit operations.

This thesis covers the three major researches done on flexible TFTs and flexible electronic circuits. First the characterization of both amorphous silicon TFTs and newly emerging mixed oxide TFTs were performed and the stability of these two materials is compared. During the research, both TFTs were stress tested under various biasing conditions and the threshold voltage was extracted to observe the shift in the threshold which shows the degradation of the material. Secondly, the design of the first flexible CMOS TFTs and CMOS gates were covered. The circuits were built using both inorganic and organic components (for nMOS and pMOS transistors respectively) and functionality tests were performed on basic gates like inverter, NAND and NOR gates and the working results are documented. Thirdly, a novel large area sensor structure is demonstrated under the Electronic

Textile project section. This project is based on the concept that all the flexible electronics are flexible in only one direction and can not be used for conforming irregular shaped objects or create an electronic cloth for various applications like display or sensing. A laser detector sensor array is designed for proof of concept and is laid in strips that can be cut after manufacturing and weaved to each other to create a real flexible electronic textile. The circuit designed uses a unique architecture that pushes the data in a single line and reads the data from the same line and compares the signal to the original state to determine a sensor excitation. This architecture enables 2 dimensional addressing through an external controller while eliminating the need for 2 dimensional active matrix style electrical connections between the fibers.

To

My family

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INTRODUCTION

Overview

Amorphous silicon (a-Si) is the non crystalline form of the silicon which can be deposited at low temperatures to various substrates. While the performance of amorphous silicon suffers significantly compared to the crystalline silicon used widely in the semiconductor industry, its ability to be deposited as thin films on low temperatures on large areas introduced different fields of application for this material.

The optical properties of amorphous silicon were first observed in 1967 by Chittick et al. in Standard Telecommunication Laboratories in UK (C., 1969) and it was the first property of the material that caught wide attention. Today, amorphous silicon is widely used in active matrix liquid crystal displays, large area sensor arrays, and multijunction solar cells. Here at the Flexible Display Center at Arizona State University, we have been developing low power, light weight flexible displays and driving circuitry that can be rolled and folded, and durable for rough field operations. Recently we've expanded our field of research to large area sensor arrays to detect anything from light to chemicals in the air.

Motivation

Intelligence has always been an important part of warfare. Knowing when and where the enemy will hit brings significant advantage in preparation for an attack. As the weapons systems become smarter and more destructive, and the world unfortunately becoming more hostile, the need to detect a threat from as far away and as early as possible is increasing dramatically. Therefore big investments are made in research and development of sensors that are capable of detecting from the radiation levels in the air to a micron wide wire crossing a path. However, these sensors (if not completely software based) are mostly either stationary, or installed on vehicles. For handheld field applications, they mostly come in bulky gadget form to be rugged for field conditions and to incorporate a long lasting power source. This means another source of weight to soldiers already equipped with heavy equipment, causing them to be more immobile, and vulnerable. Therefore, the next generation of sensors to be equipped should be light weight, non disruptive and requiring minimum power for operation while maintaining the ruggedness required for operations.

Laser technology has found its place in military application a long time ago with the most popular applications being the laser

guidance for missiles and smart bullets as well as range finding and targeting for snipers.

Laser guidance mostly uses a technology called Semi-Active Laser Homing. With this technique, a laser is kept pointed at the target and the laser radiation bounces off the target and is scattered in all directions (this is known as “painting the target”, or “laser painting”). The missile, bomb, etc. is launched or dropped somewhere near the target. When it is close enough for some of the reflected laser energy from the target to reach it, a laser seeker detects which direction this energy is coming from and adjusts the projectile trajectory towards the source. Note that laser guidance is not useful against targets that do not reflect much laser energy, including those coated in special paint which absorbs laser energy. This is likely to be widely used by advanced military vehicles in order to make it harder to use laser rangefinders against them and harder to hit them with laser-guided munitions.

Equipping a firearm with a laser sighting device can provide the extra confidence and technical advantage. Lasers helps new shooters learn sight picture and trigger control much more quickly enabling them to increase their targeting accuracy. Lasers also greatly assist aiming in low light, stress fire conditions, shooting accuracy and speed.

Laser guides are commercially available as a personal weapon accessory enabling every aggressor to be more dangerous for the target. The targets for these kinds of attacks are usually humans that cannot be coated with laser absorbing paint as in the case explained above.

Our research is to create a smart textile that can detect laser beams pointed at it and be worn as an additional thin layer by the person that can potentially be a target. Once completed as a product, it should be in the form of a thin jacket weighing only a few grams, and capable of detecting a laser beam pointing at it, warning the person wearing it, and provide information about the direction of the aggressor.

Organization of Thesis

This thesis is composed of five main chapters. In the second chapter, first an overview of flexible displays is covered explaining the architecture of active matrix displays and the enabling the flexible displays. Then the design and manufacturing of flexible electronic circuits are explained. Later in the chapter flexible sensor arrays and smart textile design are discussed. Chapter 3 provides an extensive look on the manufacturing and characterization of both amorphous

silicon nMOS TFTs and pentacene pMOS TFTs and a hybrid CMOS manufacturing process in two different fabs. Later in the chapter new materials like mixed oxide nMOS TFTs are explored and are compared to more mature a-Si process. Chapter 4 contains the main thesis topic of the smart detection fabric. First the design and simulations of the optical detection circuitry are shown. Later in the chapter the experimentation and the optical characterization, and the functionality testing are covered. Chapter 5 discusses the future work to be completed to make this system a final product; and Chapter 6 is the conclusion and the summary of the output of these three major research and development projects.

BACKGROUND

Amorphous Silicon

The first amorphous semiconductor materials that attracted attention as functional materials were the chalcogenides(Tanaka, 1999) which are materials containing the elements sulfur, selenium and tellurium; such as As_2Se_3, GeS_2 (Street, 1991). The study of chalcogenides was promoted even more when xerography was first discovered in 1938 by Chester F. Carlson (Chester F. Carlson, ; Chester F. Carlson,). The first successful copier was made in 1956 using amorphous selenium as the photoconductive material.(Street, 1991).

Amorphous silicon made its place in the research field relatively late since in the early research, the material was prepared by either sputtering or by thermal evaporation and had very high defect density which prevented all the desirable characteristics of a useful semiconductor like doping, photoconductivity etc. It was in 1969 when Chittick et al. first made a-Si:H using glow discharge as the deposition technique, this material started to get some attention in the amorphous semiconductor research field.

Early experiments demonstrated the deposition of silicon films, low defect density and increased conduction due to impurities(C., 1969).Further research in the upcoming years showed the material had good electrical transport properties with fairly high carrier (Le Comber, P. G. and Spear, W. E., 1970), and strong photoconductivity due to very low defect density (Spear, Loveland, & A.Al-Sharbaty, 1974). a-Si:H was successfully n-type and p-type doped by the addition of phosphine (PH_3) or diborane (B_2H_6) to the deposition gas in 1975 by Spear, (Spear & Le Comber, 1975) and this form of amorphous silicon saw a great interest in the following years.

RCA Laboratories made significant amount of research on a-Si:H to develop photovoltaic devices in the late 70 during the oil crises. The first amorphous silicon solar cell was made in 1976 using p-i-n structure with an efficiency of 2.4% in AM-1 sunlight (D. Carlson, 1976). Within a year after the first a-Si:H solar cells with p-i-n structure, different structures like heterojunction cells and Shottky barrier cells were manufactured with the front-illuminated Schottky barrier structure producing the highest conversion efficiency of 5.5% (D. E. Carlson, 1977). Further research by RCA and other groups increased the cell efficiency by roughly 14% by 1989 by increasing it

roughly 1% each year. The limit for amorphous silicon solar cells was estimated to be 14 to 15%. (D. Carlson, 1976).

The use of a-Si solar cells attracted attention mainly for two reasons. First, it absorbs the light very efficiently. A thin film with a thickness of less than 1μm is capable of absorbing the sunlight versus a crystalline structure which requires hundreds of micrometers. Secondly, a-Si films are very easy to deposit at temperatures around 300°C and pressure about 1 torr (Street, 2000).

The first a-Si:H field effect transistor was announced in 1978 (Snell, 1981). Silicon nitride gate dielectric was combined with the SiH_4 and NH_3 gases in the same plasma reactor. Plasma nitride was an important innovation that allowed the manufacturing of thin film transistors (TFT) on glass at low temperature with a very high on/off ratio. (Street, 2000).

LeComber et al. suggested hydrogenated amorphous silicon as a solution for application in an X-Y addressable transistor matrix like a liquid crystal display panel since it was satisfying the following basic requirements for the thin-film transistor in the matrix:

- a minimum on-off current ratio of 300

- an on-resistance $R_{on} < 9 \times 10^6\ \Omega$ to allow sufficiently rapid charging of the capacitance of the liquid crystal element

- an off-resistance $R_{off} > 3 \times 10^9\ \Omega$, preventing excessive decay of the charge between scans.(P. G. le Comber, Spear, & Ghaith, 1979)(Brody, Asars, & Dixon, 1973).

a-Si:H TFT emerged as the best solution to the fabrication of matrix addressed arrays for displays and image sensors since it could satisfy all the requirements. The first commercial devices to use it were the linear sensor arrays for the FAX machines in the 1980s followed by active matrix liquid crystal displays.(Street, 2000) The display industry has evolved through 10 generations of glass substrate with the 10^{th} generation glass substrate size being 2,880 x 3,130 mm(Sharp Corporation, 2009). This manufacturing base has opened the way for other electronic devices, most significantly of which are the image sensor arrays for X-ray medical diagnostic imaging.

Manufacturability in ultra low temperatures enabled the use of new substrates for for a-Si:H TFTs. Sheets of stainless steel, plastic and materials alike made their place in research centers for the first time in late 1990s. In 1996, the first amorphous silicon thin film transistor was built on a 200μm stainless steel substrate that is

capable of withstanding significant mechanical shocks, as well as macroscopic deformation of the substrate, while remaining functional. This work demonstrated that transistor circuits can be made on a flexible, nonbreakable substrate; and it was suggested that such circuits would be highly useful in reflective or emissive displays, and in other applications that require rugged macroelectronic circuits.(Theiss & Wagner, 1996). In 1998, the first fully flexible amorphous silicon thin film transistor on ultra thin substrate of 25μm thick stainless steel roll was demonstrated in Material Research Society's Spring Meeting Symposium A – Amorphous & Microcrystalline Silicon Technology(E.Y. Ma and S. Wagner, 1998). The same conference included research on plasma enhanced deposition of hydrogenated amorphous silicon TFTs on transparent plastic substrates. This low temperature (<150°C) RF plasma enhanced chemical vapor deposition of silicon and silicon nitride thin films lead to sufficient electronic quality for thin film transistor fabrication and operation. (Gregory N. Parsons, Chien-Sheng Yang, Tonya M. Klein and Laura Smith, 1998).

Active Matrix Display

Active matrix liquid crystal display is the dominant consumer electronic display technology of the day. They are widely used from personal computer screens to flat panel TVs due to their low weight,

quick response time, and low power consumption while maintaining a stellar image quality. The display medium is liquid crystal and each picture element (pixel) is driven by active devices like diodes or transistors. In color displays, each of the pixels is composed of 3 subpixels with each of them having a red, green or blue filter layer on. All the pixels are electrically isolated from each other to avoid a crosstalk problem on the bigger size displays.

Thin film addressed liquid crystal displays (TFT LCD) are characterized by their resolution and diagonal sizes. The pixel density is a measurement of the resolution of the display devices. The highest pixel density reported is a 0.44" SVGA LCD with 2272 pixels per inch (PPI) pixel density. The highest resolution display standard for the commercially available TVs for now is 1920 x 1080 pixels; and the largest commercially available TFT LCD display is 70" diagonally. While this size and resolution yields to a mere 31.47 pixel per inch (PPI) pixel density, the fact that the whole display area should be free of defects for the units to have commercial value drives the price up for these panels.

In a TFT LCD system, the liquid crystal molecules are encapsulated between two glass substrates precisely spaced to a specific value all over the area. One of these glass substrates is the

TFT and the other is the color filter substrate already mentioned above. The TFT substrate consists of a TFT array that is connected to the driver circuitry which provides the required video signals to each of the pixels.

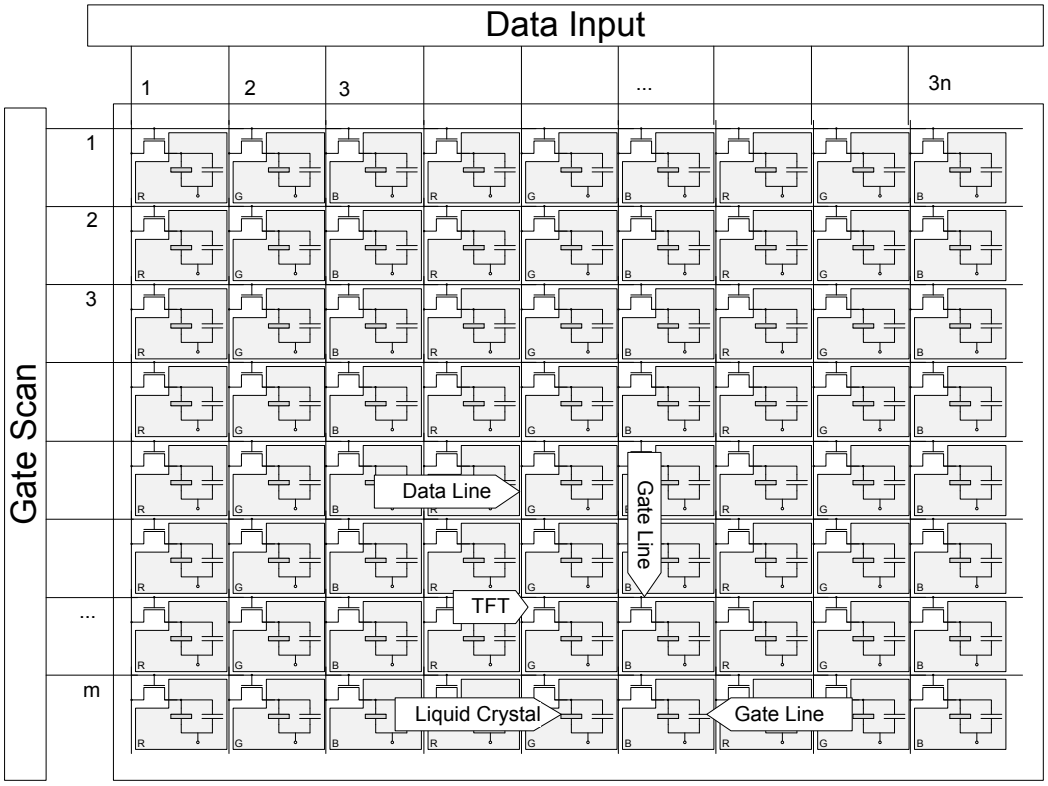

Figure 1. TFT arrays

Each pixel is composed of three subpixels; and each of the R, G, and B subpixels are coated by red, green and blue color filters to create the desired color from that pixel. The view of a RGB color filter on TFT pixel is shown below. The color of the pixel is the combination of these red green and blue subpixels.

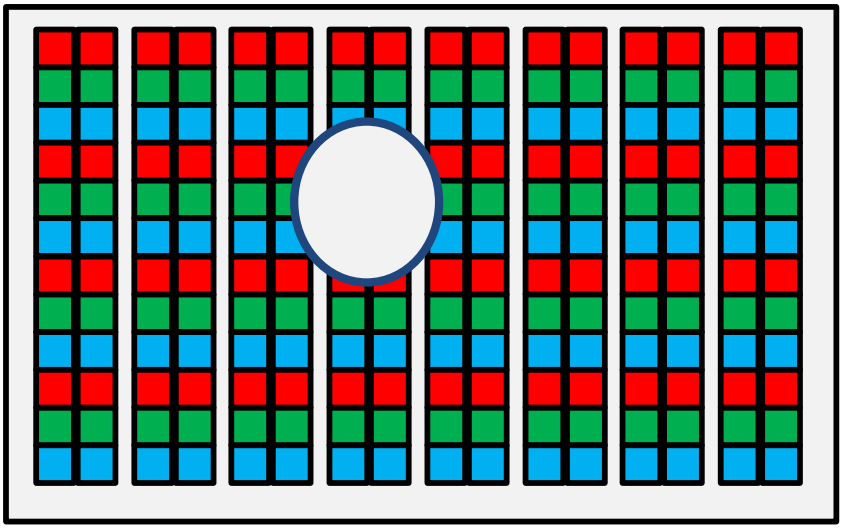

Figure 2. Subpixels in a TFT pixel

Active matrix TFT displays operate one line at a time. The gate driver enables each row of pixels by applying a gate voltage pulse signal for a brief time period. The data for each row of pixels are fed into the bus lines from video signal through a source driver when the gate driver enables that row of pixels. The maximum amount of time allotted for each row of TFTs is given as $t_{ON} = (m\ f_F)^{-1}$ where m is the number or rows in the display, and f_F is the frame rate of the video signal. In a display with 640x480 resolution with 60Hz frame rate, there are 480 rows of pixels that are being refreshed 60 times a second, making t_{ON} 34.7μs. During this time period, the charging of both the liquid crystal cell and the storage capacitance has to be completed.(Street, 2000).

Large Area Sensor Arrays

Large area sensors play an important role to gather accurate information in a short period of time. They are widely used in commercial and medical imaging as well as information acquisition about the medium like temperature or presence of a particle, or electronic artificial skins. Amorphous silicon is especially the choice of material in imaging due to its photoconductive properties. However it is not the only material used in the field of large are sensor arrays. Organic materials like pentacene are also used widely in TFT based large area sensors. These materials are used mostly in thermal and pressure sensing applications like the electronic skin.

Large Area Image Sensor Arrays

Amorphous silicon has not only been used to display images, but also to sense them as well. While the first image sensor arrays were 1 dimensional, it has evolved to the 2d arrays very soon. TFTs, photoconductors and p-i-n diodes were the active devices in most of these image sensor arrays. The structure of the two dimensional arrays of imaging pixels is quite similar to the ones used in the active matrix TFT displays discussed earlier. Each pixel senses the radiation that impinges on it and stores the corresponding charge until it is transferred to the external electronics for processing. Unlike the

displays, the information is gathered through the pixels and is sent out to the external electronics. The pixel contains a sensor that responds to incident radiation, a charge storage capacitor to hold the charge until it is read out, and a pixel switch to control the readout. (Street, 2000). A typical image sensor with a TFT addressing unit is shown in the figure below.

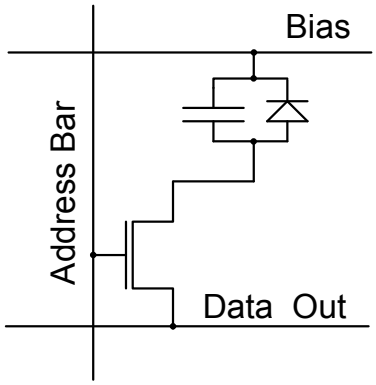

Figure 3. A typical image sensor with a TFT addressing unit

Addressing of the TFT arrays is done in a similar fashion as the TFT LCD displays mentioned above. Each cycle is referred as the frame time and consists of 3 operations within the pixel. These are signal acquisition, signal readout and reset. When the address bar is zero and the TFT is off, the photodiode which has a significant capacitance is charged to the bias voltage. As the pixel absorbs light through photons hitting the surface, electron-hole pairs are formed which drift to the contacts and discharge the sensor. When the TFT is

on, the data line restores the sensor to the original state and the charge required for restoring is recorded through the external circuitry. Therefore signal reading and resetting is done at the same time.

Large Area X-Ray Photoconductor Arrays

Although amorphous silicon p-i-n sensors are efficient detectors of visible light, they are not sensitive to X-rays due to their weak absorption. However this is achieved by introducing phosphor to the sensor array structure. A thick layer of phosphor absorbs X-rays and emits light that is sensed by the array as described earlier. Using phosphor to convert x-rays to visible light has been used for more than 100 years with X-ray films. However the addition of a thick layer of phosphor results in a structure with a thickness of roughly 500μm versus an ordinary image sensor with a thickness of roughly 1μm.

Large Area Temperature Sensing

As discussed earlier, amorphous silicon is not the only material used in the large are sensors. While photoconductive properties of a-Si make it a perfect material for imaging, organic materials are preferred for thermal sensing. Large area temperature sensing arrays with pentacene based OTFTs have been reported to be 22 times more responsive than the MOSFET equivalent. There are two reasons for

the OTFT sensing array to outperform MOSFETs. When biased at a constant drain current the OTFT's V_{SG} is approximately 20 times more responsive to temperature than MOSFET's V_{SG} moreover OTFT's current increases with temperature in both subthreshold and above threshold regions in contrast to MOSFET's above threshold current which decreases with temperature.(He et al., 2010)

Electronic Artificial Skins

It is clear that robots will be a part of human life in the future for not only work but also entertainment purposes and developers have been working on smooth human interaction with the prototypes. Sight and voice recognition are two crowded areas in this field of research however large area pressure sensing for electronic skin is a field that has just drew attention due to the recent advancement of flexible substrates. The first pressure sensing array on a flexible substrate using organic TFTs and attaching pressure sensitive rubber sheet and copper electrode to the bottom of the flexible substrate was built in 2004 by Takao et al. (Someya et al., 2004). The manufacturing process flow and an actual photograph can be seen in the original article. The same group later incorporated temperature sensors with the pressures sensors built by laminating the isolated arrays back to back with a half pitch shift to further mimic a real human skin.(Someya et al., 2005)

Flexible Substrates

The substrate is the main element enabling manufacturing of flexible circuitry. Flexible substrates can be made from polymers, stainless steel sheets, or thin glass. There are many constraints in picking the right flexible substrate. These constraints include user acceptance, supply chain investments, display technology development like OLED or e-paper. Significant research is done today to develop special plastic based materials which will fully function in finished devices. The plastic substitute of the glass should be able to offer similar properties as the glass like clarity, dimensional stability, thermal stability, solvent resistance, low coefficient of thermal expansion (CTE) as well as a smooth surface. Since there is yet a single plastic film that offers all these properties in one, multi layer structures may need to be formed.

Optical properties. For bottom emitting displays, the clarity of the film is vital since the image will be viewed through the film and a total light transmission (TLT) of 85% over 400-800nm coupled with a haze of less than 0.7% are typical of what is required. For top emitting displays, the display devices are built on non transparent substrates or layers and therefore clarity is not a metric. (Crawford, 2005) At the Flexible Display Center, the choice of flexible substrate is polyethylene

naphthalate (PEN) and both bottom and top emission displays are built. Some basic properties of PEN are tabulated below.

Table 1

Basic Properties of PEN film

Property	PEN
CTE (-55 to 85 °C) ppm/C	13
Transmission at 400 – 700 nm (%)	>85
Water absorption (%)	0.14
Young's modulus (GPa)	6.1
Tensile strength (MPa)	275

Thermal Properties. Thermal and dimensional stability are two vital factors in enabling a film to withstand the high temperatures required during the deposition of some layers, and to ensure precision alignment of different layers in the device while withstanding thermal cycling during the manufacturing process. Due to the molecular relaxation events associated with the increased mobility of the polymer chains and in addition to the 'shrinkage' or 'expansion' associated with the relaxation of residual strain within the oriented parts of the film structure, plastic films also undergo a variable and undesirable change in dimensions at the glass transition temperature - Tg. Therefore Tg is an obvious characteristic to focus on initially.

As stated previously, the substrate undergoes temperature swings during the manufacturing. Shrinkage is caused on films each time the temperature is raised and cooled back to the original levels. Low levels of shrinkage are desired to make accurate alignments on the substrate after each thermal processing step. The alignment is also affected by the coefficient of linear thermal expansion (CLTE). A low CLTE typically less than 20 ppm/°C is desirable to match the thermal expansion of the base film to the layers which are subsequently deposited.

While the glass transition temperature of PEN of 120°C is too low, its dimensional stability can be enhanced by a heat stabilization process which involves exposing to temperatures of up to 180°C for 30 minutes. The shrinkage is reduced to typically less than 0.05% and T_g effects are negated up to 200°C. The CLTE of a heat-stabilized PEN over temperatures covering the glass transition temperature are shown below.

Table 2

CLTE of Heat Stabilized PEN

Temperature Range (°C)	Elongation (%)	CLTE (ppm/°C)
20-150	0.30	23
20-160	0.37	26
20-180	0.42	26
20-200	0.36	20

Moisture and solvent resistance. A wide range of chemicals and solvents are used when manufacturing various layers in displays depending on the processing steps involved. Amorphous polymers in general have poor solvent resistance compared to semicrystalline polymers like PEN, which typically absorbs around 1400 ppm of moisture at equilibrium (Crawford, 2005).

Surface treatment. The surface quality is demonstrated to be controllable by the recipe of the plastic and film process. The surface smoothness and cleanliness are essential to ensure the integrity of subsequent layers.

FLEXIBLE TFT MANUFACTURING & CHARACTERIZATION

Introduction

Flexible Display Center successfully manufactured flexible nMOS thin film transistors using various inorganic materials including hydrogenated amorphous silicon and mixed oxide materials like Indium-Galium-Zinc-Oxide. In addition, with a collaboration of University of Texas – Dallas, the center developed the first CMOS TFTs using a-Si:H nMOS TFTs and pentacene pMOS TFTs.

TFT Structure & Fabrication

TFTs can be manufactured in three basic structures. These are

- Staggered TFTs – also known as the top gate TFTs
- Inverted Staggered TFTs – also known as the bottom gate TFTs
- Coplanar TFTs

Inverted staggered TFTs can also be manufactured in two different ways that vary slightly in structure. These two types are known as bi layer and tri-layer structures. Staggered and inverted staggered structures are widely used for manufacturing a-Si:H TFTs. The inverted staggered structure also bears the ability to be used for manufacturing poly-Si TFTs as well. Coplanar structure, on the other

hand is almost exclusively for poly-Si TFTs and only in rare occasions for a-Si:H. In general, the inverted staggered structure has better device characteristics than the staggered structure because of the superior a-Si:H/gate dielectric properties like a lower interface density of states(Kuo, 2004).

The cross sections of all these structures are shown in the figure below.

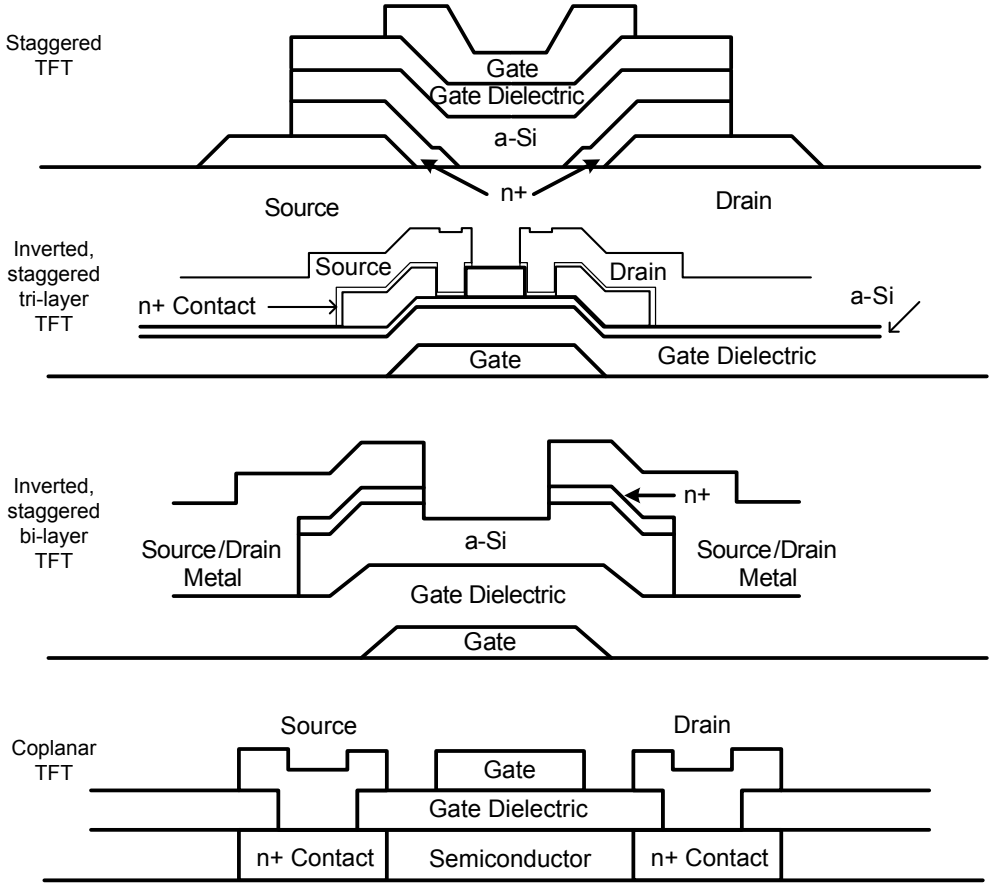

Figure 4. Cross section of different structures of TFT

Fabrication of staggered TFTs. The staggered TFT structure requires only two or three masking steps but in general, three masking steps are used. The source/drain metal and the n+ layers can be defined with the same or different masks, or the a-Si:H, gate dielectric, and gate metal layer can be defined with the same mask or two different masks.

At first, the source and the drain metals are patterned on the substrate and hen the n+ layer using selective deposition process. As the next step, amorphous silicon, gate dielectric and the gate metal are deposited on top of the structure respectively using the same mask. Below is the detailed cross section of a thin film transistor with top gate structure.

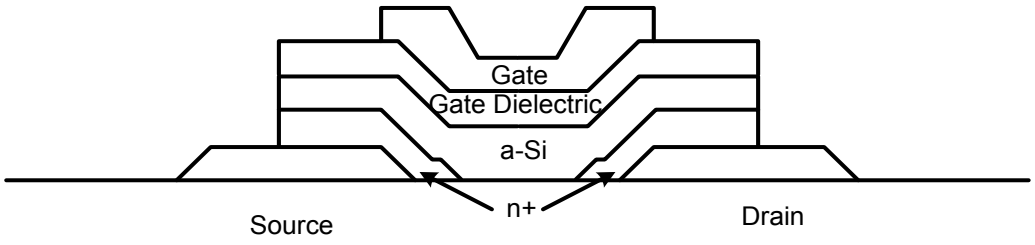

Figure 5. Cross section of a top gate TFT

Fabrication of bi-layer inverted staggered TFTs. Bi-Layer inverted staggered structure, also known as the back channel etched (BCE) structure generally uses three masking steps for gate, a-Si:H island and the source/drain.

First the gate is patterned on the substrate and then three thin film layers – the gate dielectric, a-Si:H and n+ layers are deposited respectively on top of the gate. The a-Si:H island and the n+ film is defined by the second mask. Using the third mask, the source/drain metal is patterned and n+ layers are etched. The n+ etch step is crucial for the success of the process. It requires a highly selective n+ to intrinsic a-Si:H etch process or a thick intrinsic a-Si:H layer. Below is the detailed cross section of a thin film transistor with bottom gate structure.

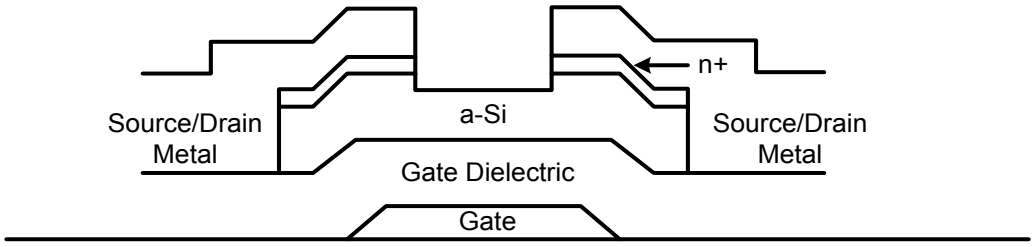

Figure 6. Cross section of a abi-layer bottom gate TFT

Fabrication of Tri-Layer Inverted Staggered TFTs. Tri-Layer inverted staggered structure, also known as the channel passivated structure (CPS) is the chosen structure for FDC manufacturing process. This structure requires a total of four mask steps, one for each of the bottom gate metal, a-Si:H island, source/drain vias, and top metal/n+ patterning.

The gate is patterned on the substrate using the first mask, and the subsequent three layers of gate dielectric, amorphous silicon, and the back channel protection dielectric are shaped by the second mask. The third mask is used to etch the source/drain vias, which are opened through etching the back channel protection layer. Finally the last mask is used for patterning the source/drain lines and the underneath n+ layer.

Amorphous Silicon TFTs at FDC

Fabrication. The Figure 7 below is the cross section of the a-Si:H TFT designed for low temperature (180°C) fabrication and manufactured at the Flexible Display Center.

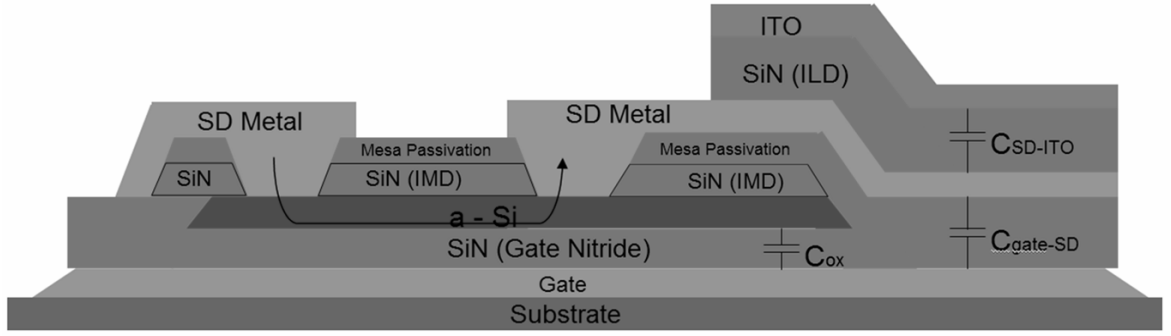

Figure 7. Cross section of a TFT manufactured at the Flexible Display Center

The substrate is a heat stabilized polyethylene naphthalate (PEN) plastic substrate bonded to a silicon carrier wafer. Below are the key specs and the process details for this specific TFT:

- The gate metal is molybdenum
- The gate dielectric is silicon nitride (SiN_X)
- The active layer is hydrogenated amorphous silicon (a-Si:H)
- A nitride passivation step is performed before the contacts are etched
- Source/Drain metal is sputtered on as an n+ amorphous silicon/aluminum bilayer

It should be noted that for display operations, additional vias and metal layers of molybdenum and indium tin oxide are added to the stack.

While the architecture remains unchanged, the process at the Flexible Display Center is in constant evolution to surface better operating thin film transistors.

Step and Repeat Manufacturing

The invention of step and repeat camera in 1970 enabled a new technique for integrated circuit manufacturing. It was originally

designed to be used as both a reduction camera, and through the use of a moving X-Y stage, precision placer for arrays of images on a master mask to be used in manufacturing (Alles et al., 1970).The steppers are now used in lithography equipment during wafer manufacturing and the patterns on the reticles are exposed repeatedly across the surface of the wafer in a grid. This is accomplished by moving the wafer in the X-Y direction under the lens of the stepper, a similar concept to the original idea (Wikipedia, 2012). The current step and repeat and the step and scan systems are evaluated thoroughly by Van den Brink et al in 1996 (van den Brink, Jasper, Slonaker, Wijnhoven, & Klaassen, 1996).Stepping on flexible substrates however requires further processing than stepping on silicon wafers since flexible substrate are neither dimensionally nor thermally stable. For precise stitching during the photolithography process across an individual layer and during the registration of subsequent layers, an active compensation architecture has to be developed, which means intrinsic and process-induced distortion effects have to be pre measured and must be accommodated for during-stitching and overlay procedures in addition to the alignment algorithms(Gardner, 2006).

An example of a reticle is shown in Figure 8. Each numbered structure is stepped at least once during the manufacturing process.

While some of these numbered structures can be highly repeating patterns like in VLSI circuit manufacturing, or large area TFT manufacturing, some of them may as well be used once for routing purposes. For the tools used in FDC fab, the structures have to be at least 3.5mm away from each other which increases the design challenge of finding appropriate sized repeating structures

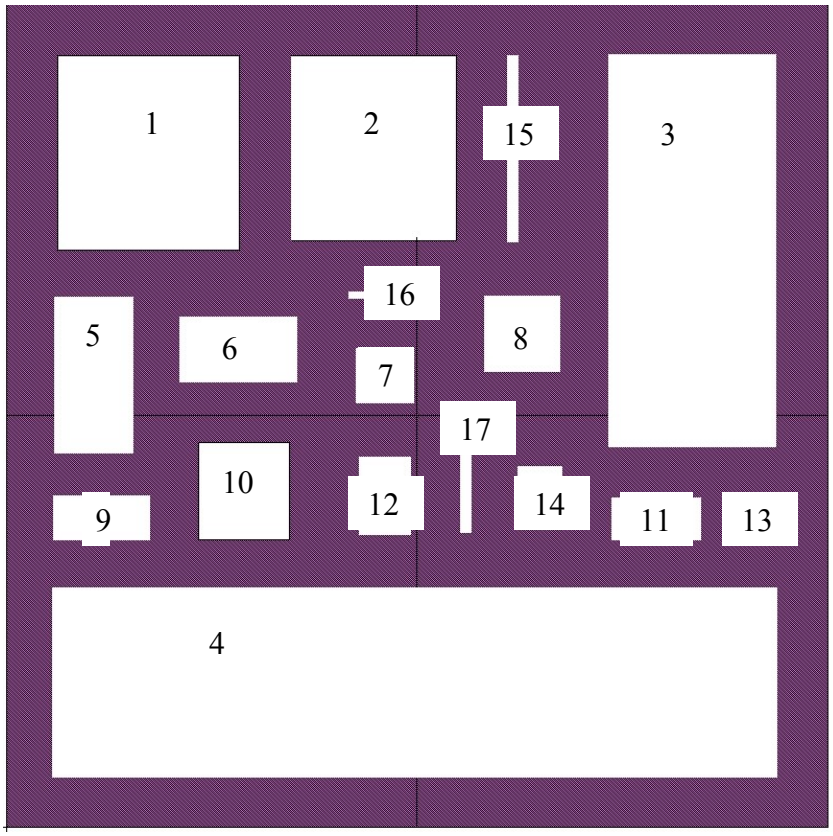

Figure 8. Sample reticle set

Characterization

The current voltage characteristics for our typical 96/9 µm TFT are shown in Figure 9. The device performance represents state-of-the-art for a-Si:H TFTs in a manufacturing environment.

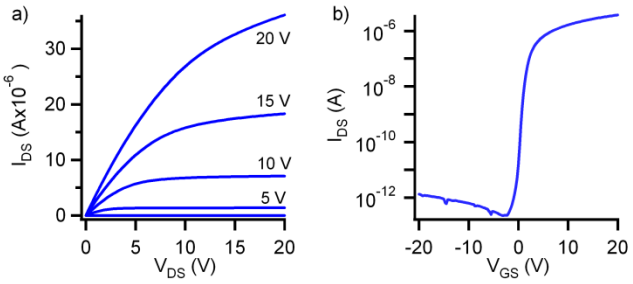

Figure 9. Typical I-V characteristics of an a-Si:H TFT. Left: I_D vs V_{DS} on a linear scale with V_{GS} as a parameter. Right: I_D vs V_{GS} on a log scale showing the subthreshold slope and reverse leakage current.

The saturation mobility is 0.8 cm^2/Vs with an on/off ratio greater than 10^7. The subthreshold slope is approximately 0.4 V/decade with a threshold voltage of a slightly greater than 1 V after fabrication. The hysteresis between forward and reverse sweeps of the drain-source voltage is also approximately 0.2 V(D. R. Allee et al., 2009a). As stated previously, the process has been constantly evolving at the FDC and the plots above show the measurements taken 2008.

An increase of a several volts in the threshold voltage (V_{th}) has been observed in the a-Si:H thin film transistors. However this is not an unusual phonomena as degredation in nMOS and pMOS devices have been previously reported and modeled both in silicon circuits (Leblebici, 1996; Roblin, Samman, & Bibyk, 1988)and in a-Si:H thin film transistors(Gleskova & Wagner, 2001). The threshold voltage increase is larger for lower temperature processes designed for flexible substreates and increasing the process temperature from 150°C to 350°C which is commonly used for glass LCD processes can reduce this V_{th} shift up to 10 times less(Long et al., 2006). The amount of threshold shift is linearly proportional to the electric field in the channel or equivalently to the charge in the channel. This shift can be reduced by increasing the drain to source voltage (V_{DS}) during the gate voltage stress(Kaneko, Sasano, & Tsukada, 1991). The threshold voltage shift over time follows a power law and is typically proportional to $t^{0.3}$. The shift is duty cycle dependent, and reducing this duty cycle for a pulsed stress improves the lifetime (Oritsuki, 1991). It is also possible to have a negative threshold shift with negative gate voltage stress, however the effect is weaker and not permanent. While the negative Vth shift is frequency dependent, positive V_{th} shift is not. Pulsed negative gate voltages greater than approximately 10 to 100 Hz are unable to reduce the threshold voltage (Huang-Chung Cheng, 1998; Oritsuki, 1991). V_{th}

shift for low temperature a-Si:H process with positive and negative V_{GS} with and without applied V_{DS} is shown in Figure 10 and Figure 11 for our devices.

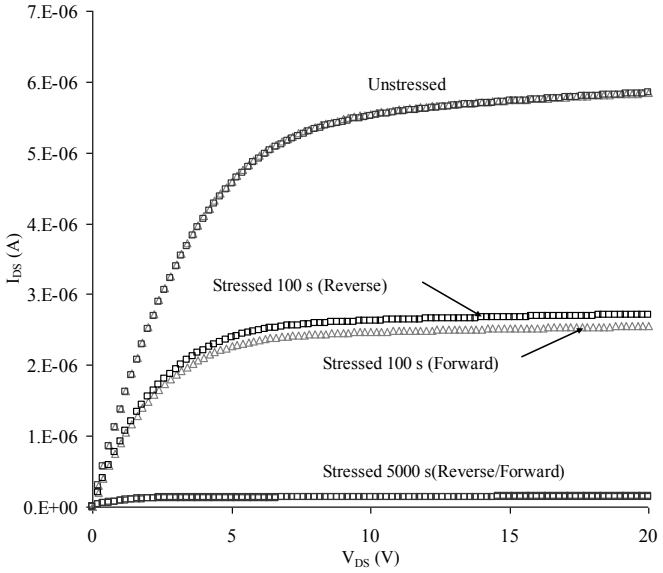

Figure 10. I_{DS} vs V_{DS} characteristics measured in forward and reverse configurations in linear mode stress

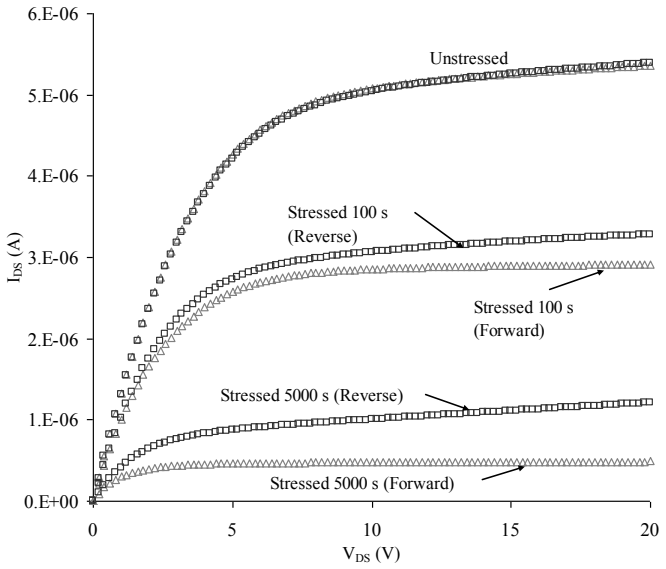

Figure 11. I_{DS} vs. V_{DS} characteristics measured in forward and reverse configurations in saturation mode stress

From the V_{th} shift measurements made on an N-type TFT, a time-dependent semi-empirical description of ΔV_{th} is given by

$$\Delta V_{th}(t) = A \cdot exp\left(-\frac{E_A}{kT}\right) \cdot t^{\beta} \left(V_{GS} - \eta V_{DS} - V_{th,0}\right)^{n} . \quad (1)$$

Where k is the Boltzmann constant, T is the absolute temperature, and t is the bias stress time duration. E_A is the mean activation energy. A is the degradation rate. β and n are process related constants. The additional V_{DS} term in (1) is attributed to the decrease in mobile carriers at the SiN_x/a-Si:H interface for TFTs in saturation. Alternate expressions for ΔV_{th} essentially equivalent to (1) have been reported(Karim, 2004)(Ibaraki, 1989)(Aoki, 1996).

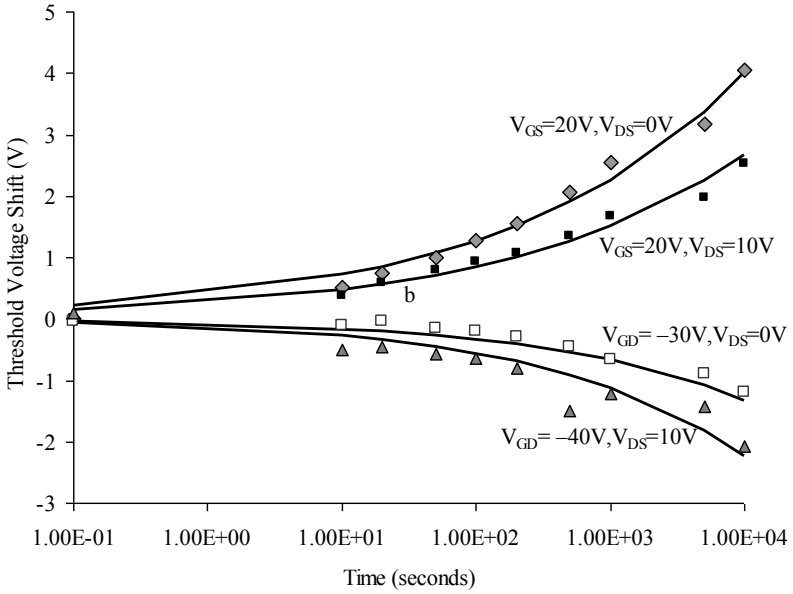

Figure 12. Threshold-voltage shift vs. time for positive and negative gate voltages with and without elevated drain voltages

The measured V_{th} shift curves from Figure 12 are fitted to (1). giving $Ae^{-EA/kT} = 0.025$, n = 1.0, ß = 0.25 for the positive shift (ΔV_{th} (+)) caused as a result of the $V_{GS} > 0$. The magnitude of ΔV_{th} when $V_{DS} > 0$ is corrected by $\eta \cdot V_{DS}$ where $\eta = V_{GS}/(V_{GS} + V_{DS})$. Subsequently, $Ae^{-EA/kT} = 0.0025$, n = 1.1, ß = 0.29 for the negative shift (ΔV_{th} (+)) when $V_{GS} < 0$, the parameter η is computed as before. The lower value of $Ae^{-EA/kT}$ for $V_{GS} < 0$ is due to the higher hole, vs. electron, activation energy. Other TFT parameters are also affected by applied voltages. In particular, subthreshold slope increases with the square root of time, and there is

a minor decrease in mobility(Gleskova & Wagner, 2001)(D. R. Allee et al., 2009a)

Mechanisms. The a-Si:H TFT V_{th} degradation has two mechanisms—charge injection in the silicon nitride (SiNx) gate insulator and creation of defect states in the a-Si:H conducting channel (M. J. M. J. Powell, 1989). Under low to medium positive V_{GS} stress, defect creation is dominant, whereas for large positive V_{GS} charge trapping is the dominant instability mechanism.

SiNx gate charge injection is mainly due to tunneling of carriers from extended states in the a-Si:H layer to the trap states in the nitride (M. M. J. Powell, 1983)(M. M. J. Powell, 1992). These charges are located at the SiN_x/a-Si:H interface and add to the insulator fixed charge. Charge injection into the gate insulator is reversible.

Field-effect experiments have suggested that mobile carriers are responsible for breaking the weak Si–H bonds resulting in the creation of charged defect states (dangling bonds)(M. J. M. J. Powell, 1989)(Hepburn, 1986) (Deane, 1993). Hydrogen is used to passivate the dangling Si bonds which form traps in the bandgap, reducing the trap density by four orders of magnitude. Without hydrogen passivation, the trap density is $10^{26}/cm^3$ which pins the Fermi level and prevents

transistor action. The passivated Si-H-H-Si bonds are fragile and can be broken in the presence of mobile carriers in the channel. The dangling bonds have a distribution of energies (and hence strengths) so the weakest bonds degrade rapidly when the device is initially biased, and stronger bonds survive longer until a "lucky" event provides enough energy to break the bond. The density of created defect states is proportional to the number of mobile carriers, which affects the Fermi level position, producing a V_{th} shift. Creation of charged defect states is significantly less reversible than insulator charge injection.

Localization of degradation. Extending techniques used to localize hot electron degradation in MOSFETs, we have localized the degradation of a-Si:H TFTs to the gate dielectric/a-Si:H channel interface. In bulk-silicon MOSFETs degradation occurs only at the drain where hot electrons are injected (Leblebici, 1996; Roblin et al., 1988). This results in different post-stress linear vs. saturation current characteristics that depend on the direction of current flow during stress and measurement (Tsividis, 1987). A similar experiment on a-Si:H TFTs shows that the gate voltage induced ΔVth mechanism is similarly localized in the TFT channel.

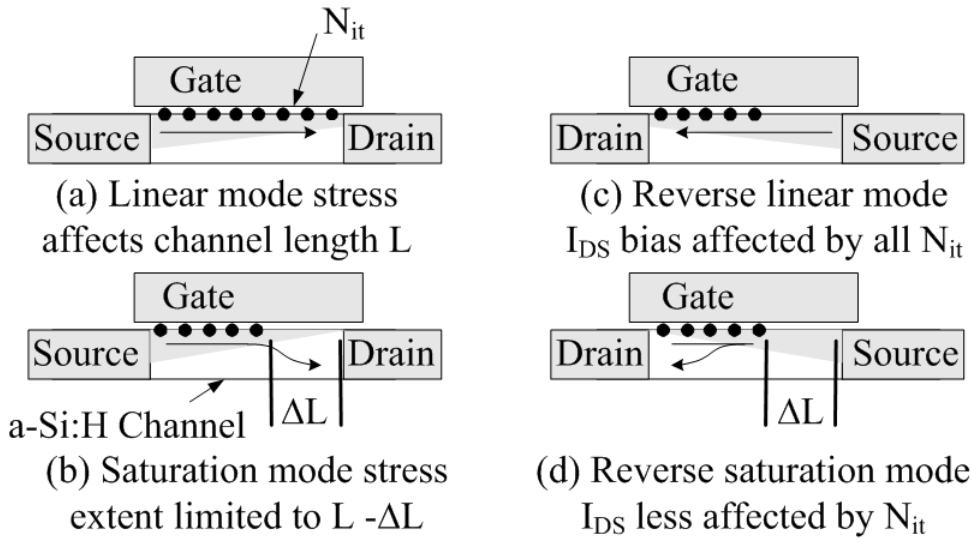

Figure 13. Schematic representation of the different stress conditions for TFT operation in linear and saturation regimes. N_{it} is the additional induced interface-trap density.

The concept is illustrated in Figure 13. When the TFT is exposed to a gate voltage at low V_{DS} (linear mode stress) in the forward configuration, the ΔV_{th} mechanism is distributed throughout the channel extent Figure 13a resulting in maximum V_{th} degradation. When exposed to the same gate voltage at a higher V_{DS} (saturation mode stress), the ΔV_{th} mechanism is limited to L-ΔL Figure 13b since carriers are at the interface only until the pinch off point. Channel length modulation localizes the traps towards the source. The drain current in saturation following a saturation mode stress shows depressed ΔV_{th} (higher I_{DS}) when the measurement is made in the

reversed configuration Figure 13c. In the linear operating region (after saturation mode stress), carrier flow is over the whole extent of the damage (L-ΔL) in the forward and reverse configurations Figure 13d. Hence reversing the source and drain maximizes the current flow in the unaffected region.

TFT's in Figure 10 and Figure 11 were subjected to a gate bias stress of 20 V with V_{DS} = 0 V (linear mode stress) and V_{DS} = 20 V (saturation mode stress) at logarithmically spaced time intervals. During each stress interval the I_{DS}-V_{DS} characteristics were measured in the forward and reverse configurations. V_{DS} was varied from 0 V to 20 V with V_{GS} = 20 V. The I_{DS}, vs. V_{DS} in both the pre and post-stress conditions is shown. Linear mode stress with V_{GS} = 20 V and V_{DS} = 0 produces essentially identical I_{DS}/V_{DS} curves for the post-stress case in both the forward and reverse configuration measurements. Degradation in I_{DS} is greater when the transistor is stressed in linear mode as expected. Saturation mode stress with V_{GS} = 20 V and V_{DS} = 20 V shows less I_{DS} degradation when V_{DS} increases in the reverse configuration. Assuming all defect states (N_{it}) created at the silicon/insulator interface are charged, the linear drain current ($I_{DS,lin}$) degradation can be expressed as

$$\frac{\Delta I_D}{I_{D,lin}} = K \cdot \frac{L - \Delta L}{L} \cdot N_{it} \qquad (2)$$

where K is a constant related to the effective vertical electric field. Equation (2) shows that degradation reduces as V_{DS} increases. Higher V_{DS} moves the pinch off point toward the transistor source and produces a decrease in excess carriers, affecting ΔV_{th}. The effect is mild, since the transistors have long channels and $\Delta L/L$ is not large (Karim, 2004).

Reversing the source and drain maximizes current flow in the unaffected region and allows the pinch off point to sweep across the traps that create the V_{th} degradation. The source to channel barrier appears unaffected by the ΔV_{th} mechanism since the drain current in the linear operating region after the linear mode or saturation mode stress is less affected in the reverse measurement configuration. Reduced ΔV_{th} occurs at the drain end, where electric fields drive the carriers away from the surface after the channel pinch-off point. These measurements are consistent with the ΔV_{th} mechanism as suggested in (Shringarpure, 2008).

Organic TFTs at UT-D

A joint effort to build CMOS architecture on flexible substrates resulted in hybrid structures manufactured by University of Texas-

Dallas and Flexible Display Center. The next chapter will cover the CMOS in detail.

Fabrication. The fabrication of pMOS process starts with the ILD deposition and patterning to define the metal gate vias and channel region of the aluminum layer already manufactured in the FDC process. The flowchart for manufacturing is shown in Figure 14 below

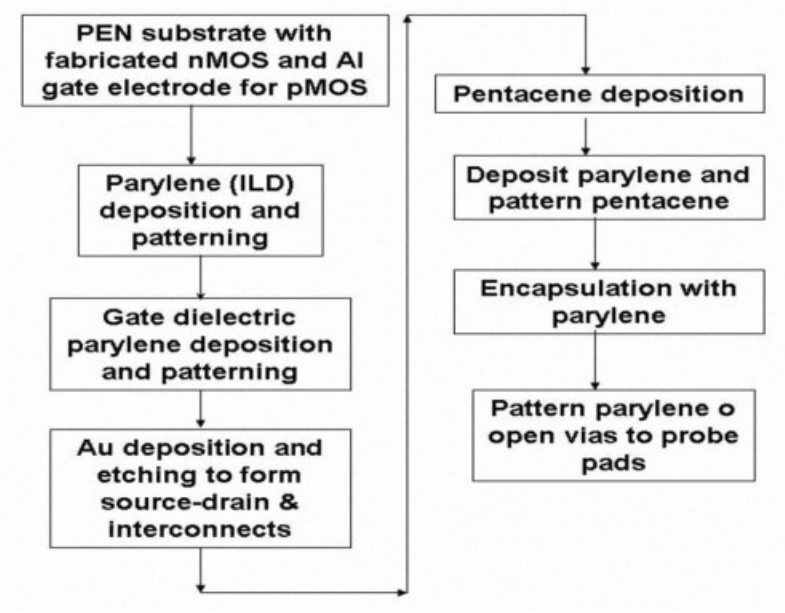

Figure 14. Flowchart for organic TFT manufacturing on pre-fabricated FDC substrates

This approach insures that a pristine and hydrophobic gate insulator surface is used, which provides a good starting surface for pentacene growth. If the gate dielectric layer is patterned before

patterning the ILD layer, the gate dielectric surface becomes hydrophilic due to exposure to the RIE oxygen plasma during patterning of the ILD, which degrades the quality of the deposited pentacene.

Characterization. The I_D-V_D characteristics of pentacene transistors using this flow is shown in Figure 15. The drain source voltage (V_{DS}) is swept from 0V to -25V for different gate voltages (V_{GS}). The mobility (0.08cm2/Vs) and threshold voltage of -1.4V were obtained from the transfer characteristics shown in Figure 16.(Gowrisanker et al., 2009)

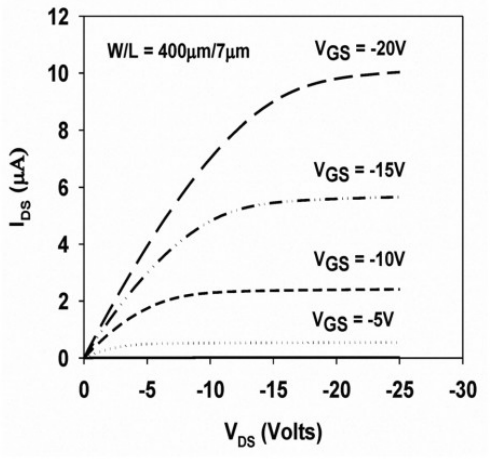

Figure 15. I_{DS} vs. V_{DS} curves of organic TFTs

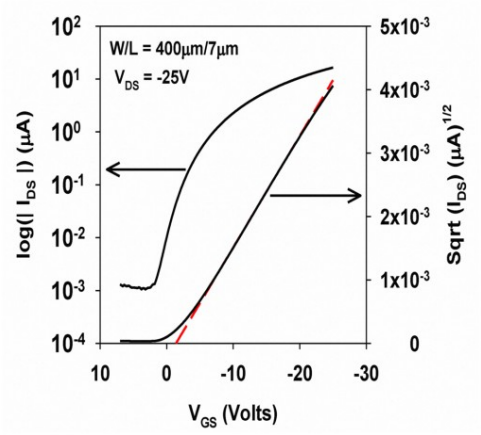

Figure 16. I_{DS} vs. V_{GS} curves of organic TFTs

Mixed Oxide TFTs at FDC

Fabrication. Thin film transistors based on amorphous silicon are currently used in the display industry to form the transistor backplanes for LCD displays. There is ongoing research in other TFT technologies such as mixed oxide (InGaZnO, InZnO, ZnSnO) TFTs, since initial research show that these devices have better threshold voltage stability and greater mobility compared to amorphous silicon TFTs. Here at the Flexible Display Center, we are developing a low temperature (200 °C) Indium Zinc Oxide (IZO) process compatible with flexible substrates. The IZO TFTs fabricated at FDC are n-type enhancement mode devices. The cross sections as well as the manufacturing steps of the TFT are shown in Figure 17 below.

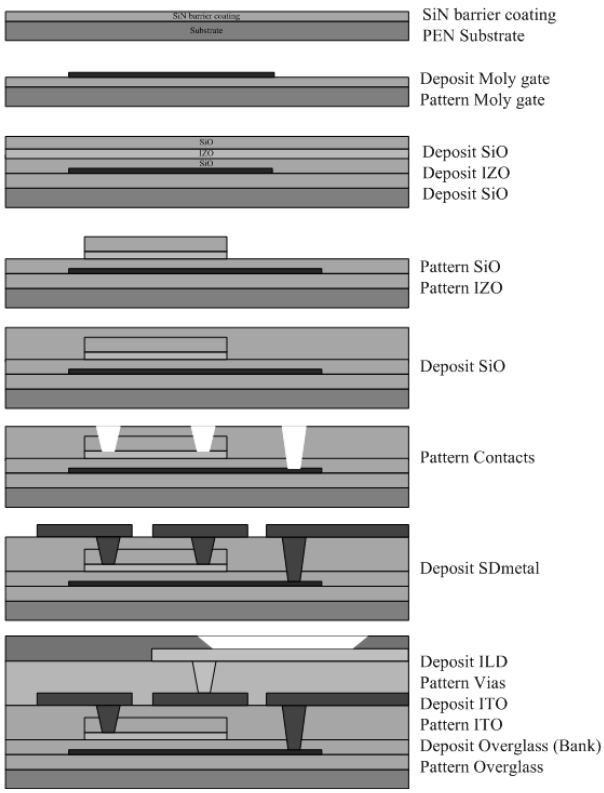

Figure 17. Cross section and manufacturing steps of mixed oxide TFTs

The IZO TFTs are fabricated as follows. The substrate used is a 6" silicon wafer with a thin layer of SiO. The gate metal is molybdenum and is deposited using a sputtering process. After patterning the gate layer, a stack of SiO, IZO and SiO (Inter-metal dielectric) is deposited. The IZO has a Zn:In ratio of 60:40 and is deposited at temperature between 77 and 91 °C and top layer of SiO is deposited at 180 °C. Another layer of SiO is deposited which forms the mesa passivation layer. The IZO is patterned and the source-drain metal (moly) is sputtered to form the source and drain contacts of the TFT. A second metallization step involves the deposition of an inter-layer dielectric

(ILD) and patterning of Indium-tin-oxide (ITO) which acts as the top metal connecting to the electrophoretic material in an active matrix display. After the overglass etching process, the entire wafer is annealed at 200 °C for 1 hour and this is the maximum process temperature used which is compatible with TFT fabrication on plastic substrates such as PEN and stainless steel foils.

Characterization of mixed oxide TFTs at FDC. The transfer characteristics of an IZO TFT with W/L equal to 108/9 μm/μm are shown in Figure 18 and Figure 19. TFTs were characterized using Keithley 4200 Semiconductor Characterization System (SCS). An average V_{th} of -1.7V, saturation mobility of 14.2 cm^2/Vs and a subthreshold slope of 0.22 V/dec were obtained. Although, the mobility is low, for active matrix backplanes, the V_{th} stability is more important than higher speed. The on/off ratio for drive current was more than 10^9. Also, there is no appreciable hysteresis.

Stress measurement results. The IZO TFTs with the size of 108μm/9μm and dielectric thickness of 1000Å have been electrically stressed continuously for extensive periods of time under various DC bias conditions. Below is the description of various stress measurements taken using a probe station and semiconductor parameter analyzer.

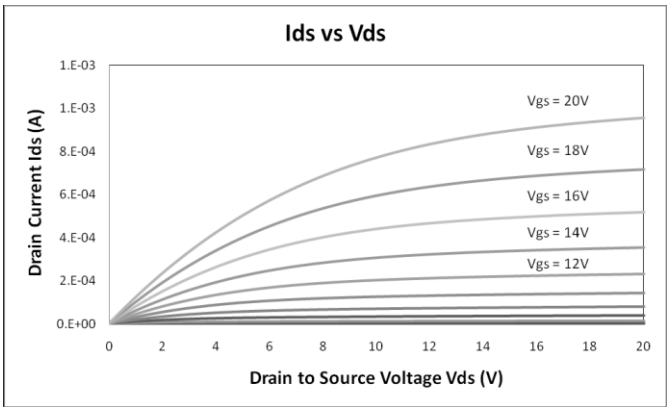

Figure 18. I_{DS} vs V_{DS} Curves of an IZO TFT

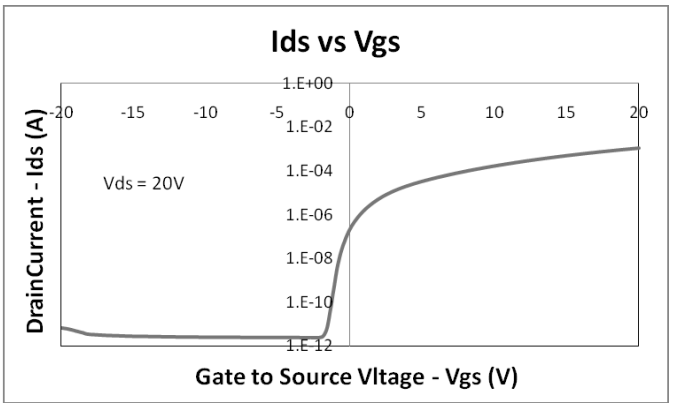

Figure 19. I_{DS} vs. V_{GS} curve of an IZO TFT

DC Stress. For the DC stress test, the gate and drain of the TFTs were connected to a DC bias, varying from -20V to +20V using a semiconductor parameter analyzer. At regular intervals, the SCS disconnects the DC bias and measures the Ids vs. Vgs characteristics of the TFT. The TFTs were stressed for 10,000 seconds. The change in threshold voltages (ΔV_{th}) were extracted for each test and plotted as shown in Figure 20 and Figure 21. To extract ΔV_{th}, current per unit width approach has been followed. An appropriate reference current was selected from the unstressed TFT characterization plots, and

corresponding gate voltages for that reference current were noted for different stress times. The difference in the observed gate voltages is determined to be the V_{th} shift caused by the stress tests. As seen in the Figure 20, change in V_{th} is within 2.5V for IZO TFTs for both positive and negative voltage stresses. Figure 21 shows this change in V_{th} is up to 10V for positive and 2.5V for negative voltage stress for a-Si:H TFTs for the same 10,000 seconds of stress period. Our TFTs are showing the same behavior for negative voltage stress, but IZOs are clearly more stable in positive voltage stress.

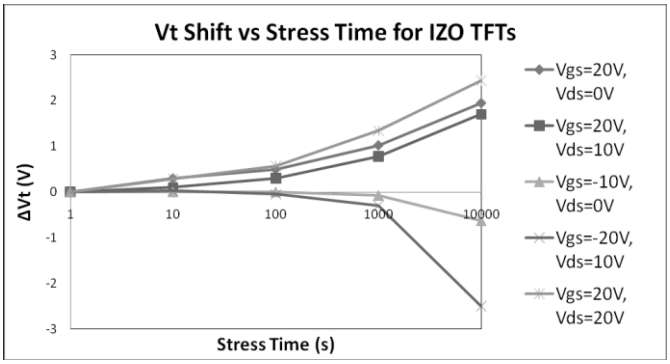

Figure 20. V_{th} Shift vs. Stress Time for IZO TFTs

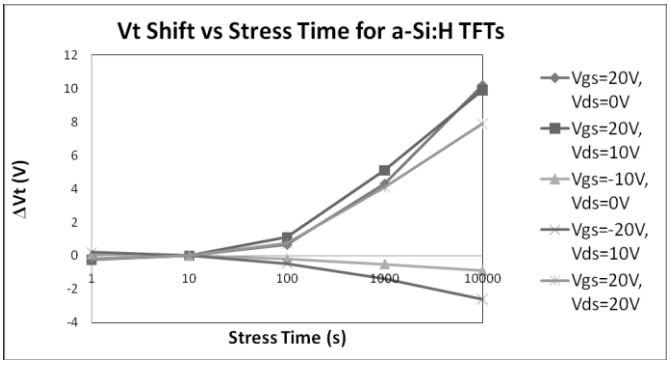

Figure 21. V_{th} Shift vs. Stress Time for a-Si:H TFTs

Constant current source. In analog circuits, a constant current source circuit is very important. In order to simulate the behavior seen in analog circuits, a TFT was stressed with $V_{GS} = V_{DS} = 20V$. This will keep the TFT in a constant current source mode. Figure 22 shows the plot of change in saturation drain current vs. time for IZO and a-Si:H TFTs. In the constant current mode, the change in saturation current is about 19% in IZO TFTs while this is 71% in a-Si:H.

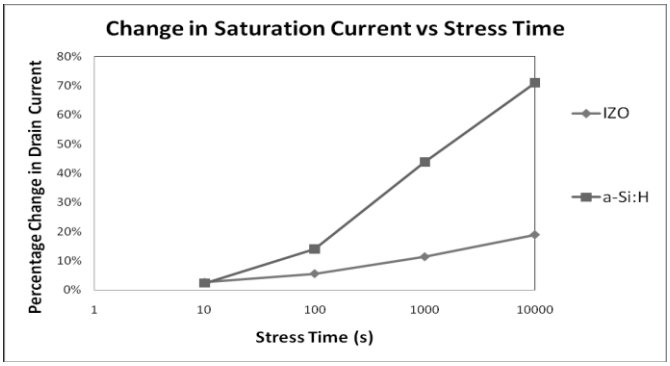

Figure 22. Change in the saturation current of the IZO and a-Si:H TFTs after 10,000 seconds of DC stress

Mechanisms. The V_{th} shifts (ΔV_{th}) for IZO and a-Si:H TFTs are plotted in Figure 20 and Figure 21 for different V_{GS} and V_{DS} combinations. In Figure 20, the ΔV_{th} curves follow more of a logarithmic dependence on time, generally a signature of charge trapping(Suresh, 2008).

$$\Delta V_{th} = r_0 \log\left(\frac{t}{t_0}\right) \qquad (3)$$

where r_0 and t_0 are empirical parameters extracted from measurements. The large negative shifts under negative bias stress also point out to charge trapping in the channel interface (Cross & De Souza, 2007), as state creation dominates in presence of mobile carriers that are absent under negative bias. The charge trapping takes place mainly at the interface because it has also been observed that the TFTs tend to revert back to their original characteristics when left unstressed for long time (Wager, 2003).

From Figure 21, however, it is clear that the ΔV_t curves follow the familiar stretched exponential equation (M. M. J. Powell, 1992)

$$\Delta V_{th} = \left(V_{GS} - V_{th}\right)\left(1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right) \qquad (4)$$

where ß and τ are empirical parameters extracted from measurements. The ß and τ values for our process are 0.25 and $5x10^4$ respectively. The stretched exponential behavior of ΔV_{th} is a signature of state creation, as has been found out under numerous experimentations (M. M. J. Powell, 1992). Moreover the TFTs do not revert back to their original characteristics, unless annealed (M. J. Powell, Easton, & Nicholls, 1982). All these observations point out to state creation being the dominant degradation mechanism under both gate bias stress for a-Si:H TFTs.

FLEXIBLE CMOS

Introduction

Complementary metal–oxide–semiconductor (CMOS) is a technology for making integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for a wide variety of analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. Frank Wanlass successfully patented CMOS in 1967 (US Patent 3,356,858). The word "complementary " refers to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor-transistor logic (TTL) or nMOS logic, which uses all n-channel devices without p-channel devices. CMOS also allows a high density of logic functions on a chip. It was primarily this reason why CMOS won the race in

eighties and became the most used technology to be implemented in VLSI chips (Wikipedia, 2011).

The development of flexible CMOS circuits reduces the power consumption by ~50X compared to n-type or p-type only thin film transistor digital circuits, thus enabling many technologies of great interest. CMOS flexible electronics is of great interest due to the potential for low-power and large area applications. Potential applications for large area flexible CMOS are thin, light-weight flexible displays and drivers, low-cost RFID tags on PEN, large area solar panels with built in power control, and large area sensors with control logic.

Fabrication of CMOS

With the collaboration of University of Texas – Dallas (UTD) and Flexible Display Center, CMOS TFTs were manufactured by incorporating the organic pMOS transistors manufactured at UTD on top of the nMOS transistors manufactured at the FDC. The process flow is explained below.

After nMOS fabrication, pentacene-based pMOS TFTs are fabricated at UT-Dallas. pMOS TFTs are also fabricated using a bottom gate approach. In the process, the gate insulator (parylene) is deposited after the inter-level dielectric (ILD). This fabrication process

includes aluminum as gate metal, parylene as ILD (500 nm), parylene (100 nm) as gate dielectric and gold as source-drain contacts and interconnect metallization. The pMOS fabrication process starts with the ILD (0.5 lm of parylene) deposition over Al gate metal formed during nMOS fabrication. The ILD is deposited at room temperature and patterned to define the metal gate vias and channel region. Next, gold (100 nm) is deposited by e-beam evaporation and patterned to form source-drain contacts and interconnects. Pentacene (150 nm) is then deposited at room temperature to create the active channel. Finally, the devices are capped using a parylene encapsulation process and vias are opened for device testing (Gowrisanker et al., 2009).

This integration process is shown in the Figure 23 below:

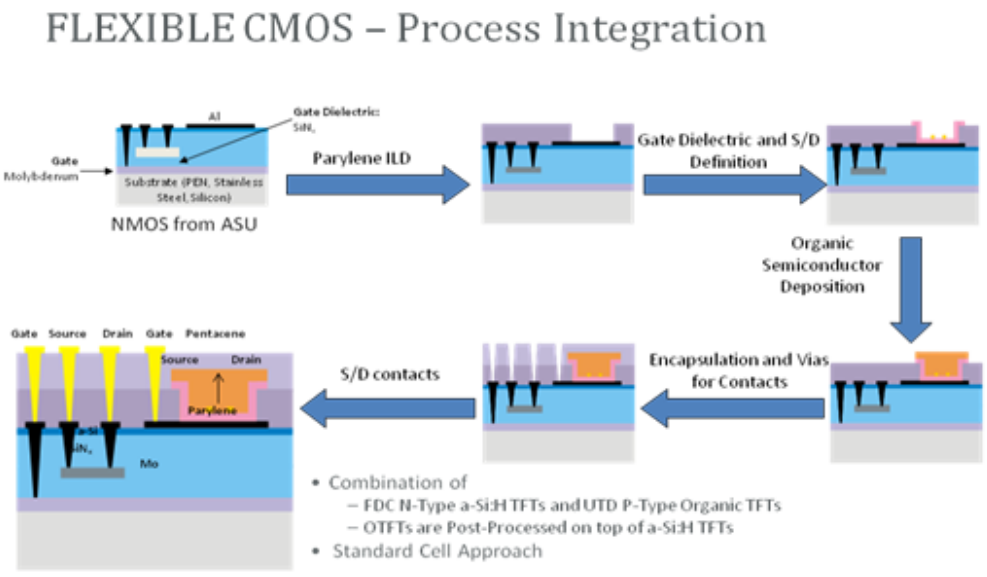

Figure 23. Flexible CMOS – Process Integration

Flex CMOS Design

For the initial purpose of testing a hybrid structure manufacturing, basic logic gates (NAND, NOR and INV) were designed at different W/L ratios. The figure below shows the initial layout of these circuits.

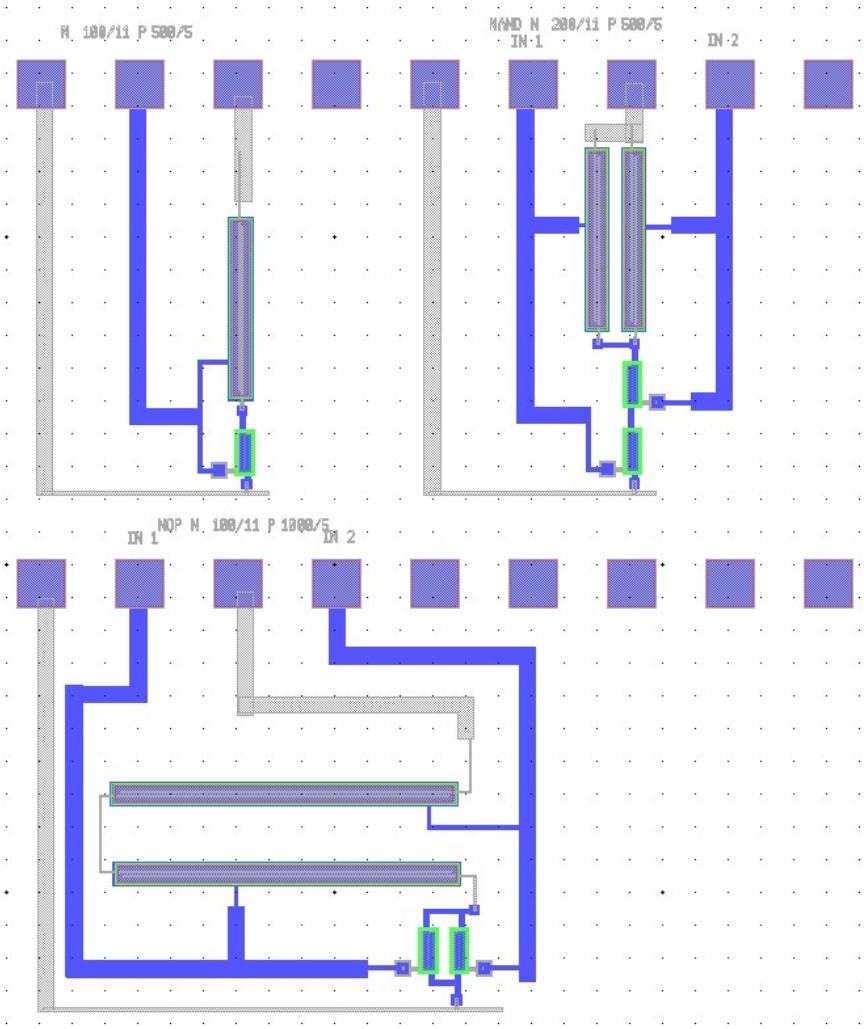

Figure 24. The layouts of CMOS inverter, NAND and NOR gates

The optical image of hybrid CMOS inverter on PEN is shown in Figure 25 below. The typical voltage transfer curve is obtained with the fabricated CMOS inverter with W/L for pMOS and nMOS 500/5 and 100/11μm respectively. The inverter transition point is at $V_{DD}/2$ as expected and the maximum DC gain was 16.

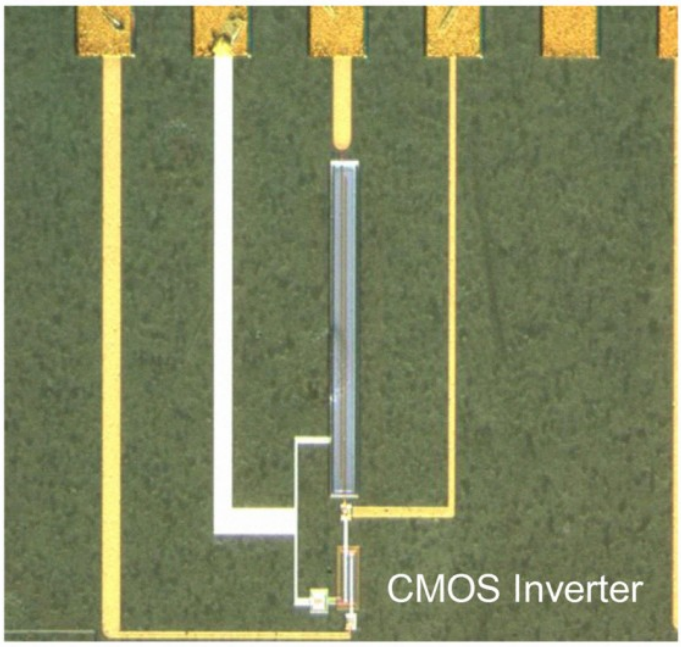

Figure 25. The picture of the first flexible CMOS inverter manufactured by FDC and UT-D

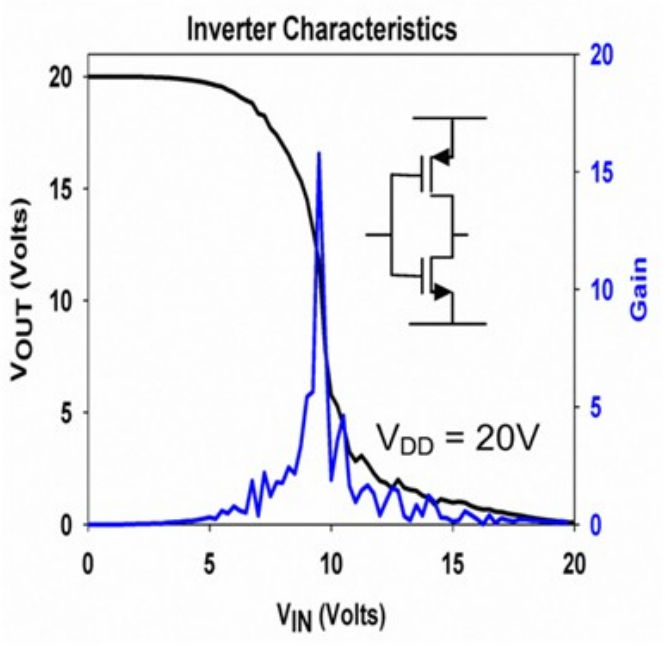

Figure 26. The characteristics of the flexible CMOS inverter

Figure 27 and Figure 28 show the logic verification of the 2-input NAND gate and the NOR gate respectively. A square wave input with a 20ms period and 50% duty cycle is input to A of the NAND gate, and a square wave with a 40ms period and 50% duty cycle is input to B of the NAND gate. The output stays high except when both A and B are logic high. When the same inputs are applied to the NOR gate, the output is high only when both the inputs are logic low.

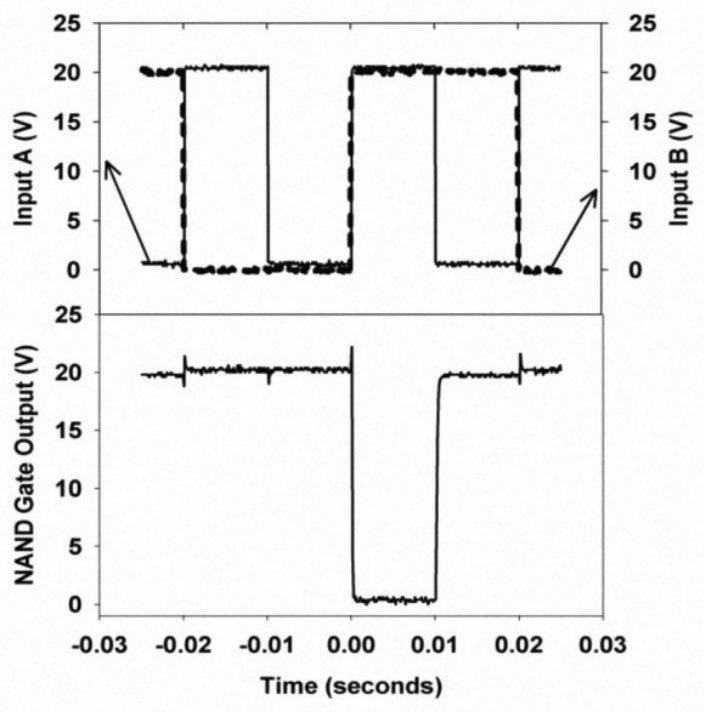

Figure 27. NAND gate operation plots

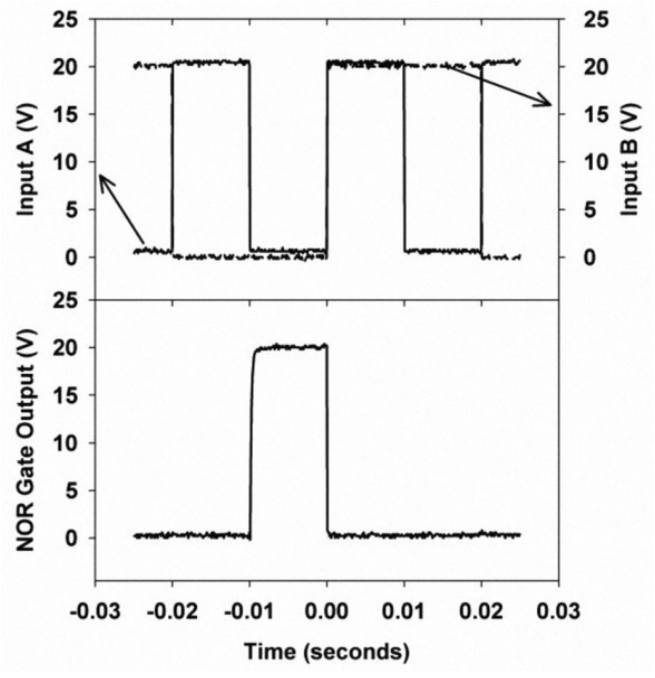

Figure 28. NOR gate operation plots

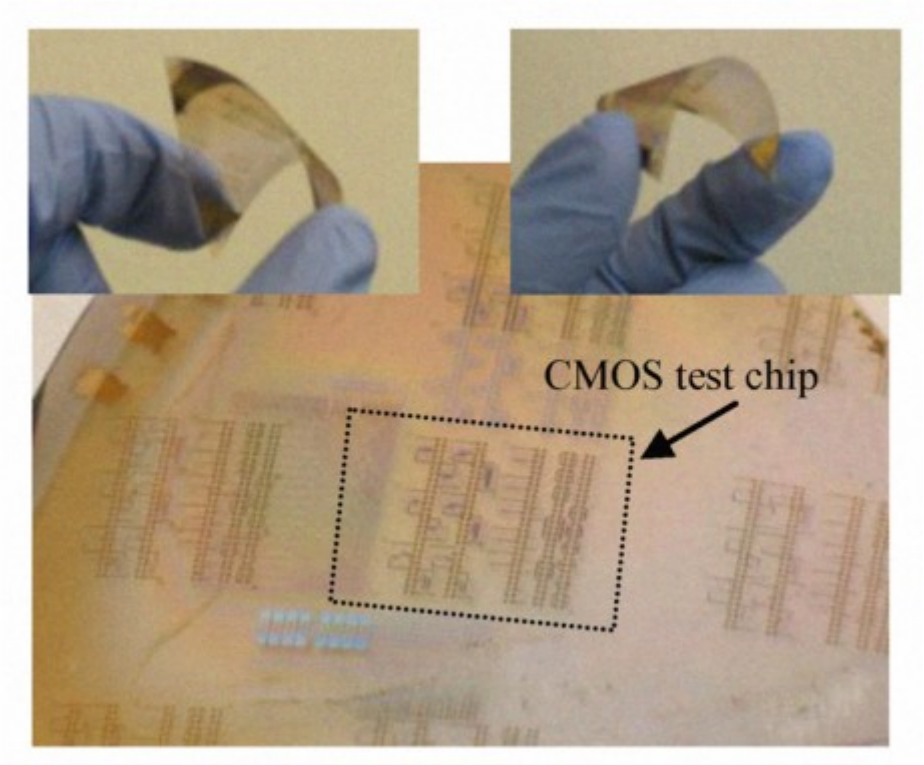

Figure 29. Photograph of hybrid CMOS test circuits fabricated on PEN substrate

An extensive flexible CMOS circuit library was designed as well for a flexible IR-Tag project. This library includes more complex logic gates like 8-bit XOR gate as well as an 8-bit decoder, a 32 bit ROM, a D-Flip-Flop, and a 6 bit counter.

Simulations comparing the current drawn from the power supply as a function of time for the a-Si:H only and CMOS source drivers (Figure 30) reveal the significant reduction in power possible with any integrated flexible CMOS source driver. The a-Si:H only design clearly draws continuous current whereas the CMOS design

only draws current on the clock edges when the logic state changes. For a sample QVGA electrophoretic display operating at 15Hz frame rate, the ensemble of source drivers consume only 2.3mW for the CMOS case versus 700mW for the a-Si:H only case, a 308X reduction in power. (D. R. Allee et al., 2009b)This is a perfect example for the need of flexible CMOS electronics for the battery dependent applications.

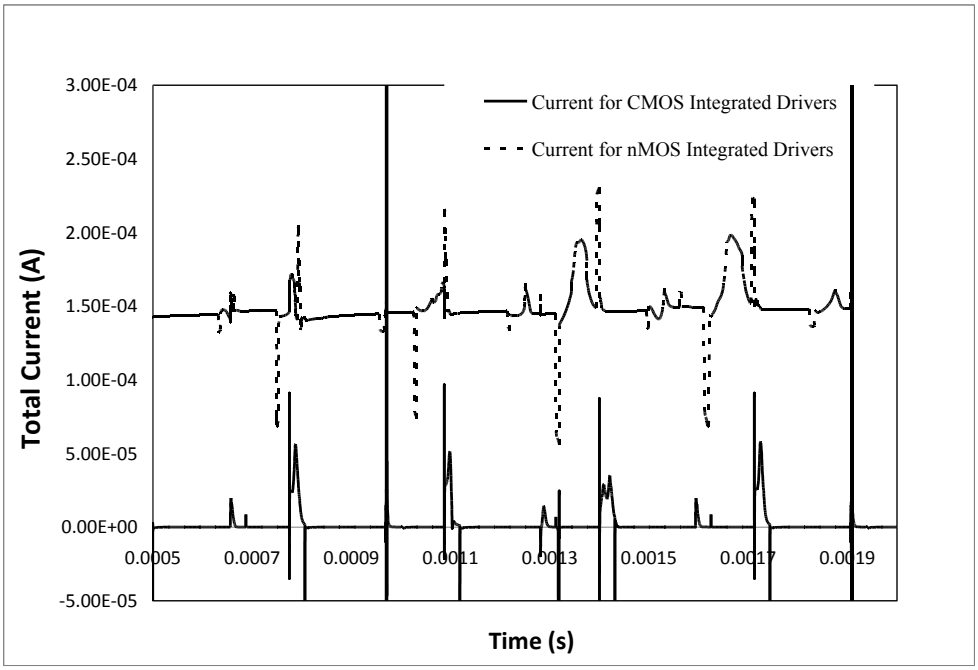

Figure 30. Power consumption comparison of current CMOS integrated drivers vs current nMOS integrated drivers

Electrical stability of a hybrid CMOS structure. Most types of TFTs are electrically unstable, and their performance degrades with electrical usage. The threshold voltage, V_{th}, of an a-Si:H thin film transistor increases by several volts over a few hours with a DC

voltage applied to the gate. This degradation is common to all a-Si:H and is larger for lower temperature processes designed for flexible substrates (Long et al., 2006). The threshold shift and change in mobility and the mechanisms for these in amorphous silicon were discussed in the previous chapter. Similar phenomena are observed in organic TFTs (Mathijssen, 2007)and are frequently modeled with the same equations.

In Figure 31 and Figure 32, measured threshold voltage shift and mobility reduction for an a-Si:H TFT and a pentacene TFT are shown for +/-20V (+ for a-Si:H, - for pentacene) gate voltage stress as a function of time. Interestingly with electrical stress, the pentacene TFT becomes easier to turn on (less negative threshold voltage) whereas the a-Si:H TFT becomes harder to turn on (more positive threshold voltage). However, both devices suffer decreased mobility, 15% reduction for the a-Si:H TFT and 35% reduction for the pentacene TFT at 10,000s continuous stress.

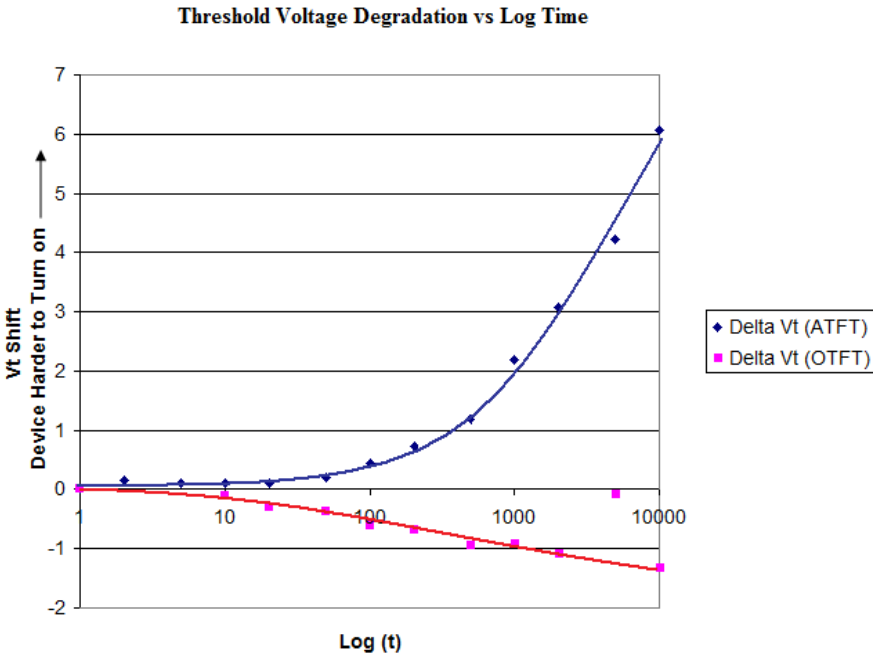

Figure 31. Threshold Voltage Degradation vs. log time

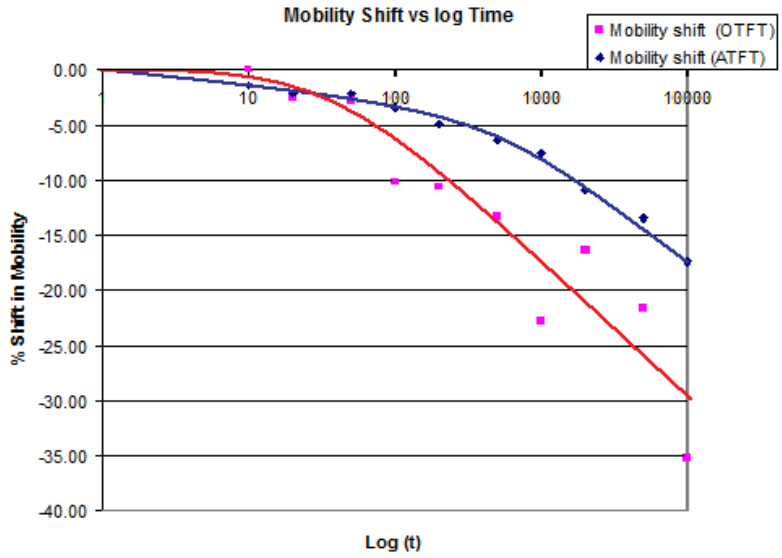

Figure 32. Mobility shift vs. log time

The impact of these competing effects on the operation of a flexible CMOS inverter can be seen in Figure 33. The inverter is

operated continuously with a 50% duty cycle input signal. The output voltage is plotted after various periods of time. The inverter performance degrades very little over the first 6 hrs of operation. The cause of the failure at 19 hours is likely the parylene gate dielectric based on preliminary analysis.

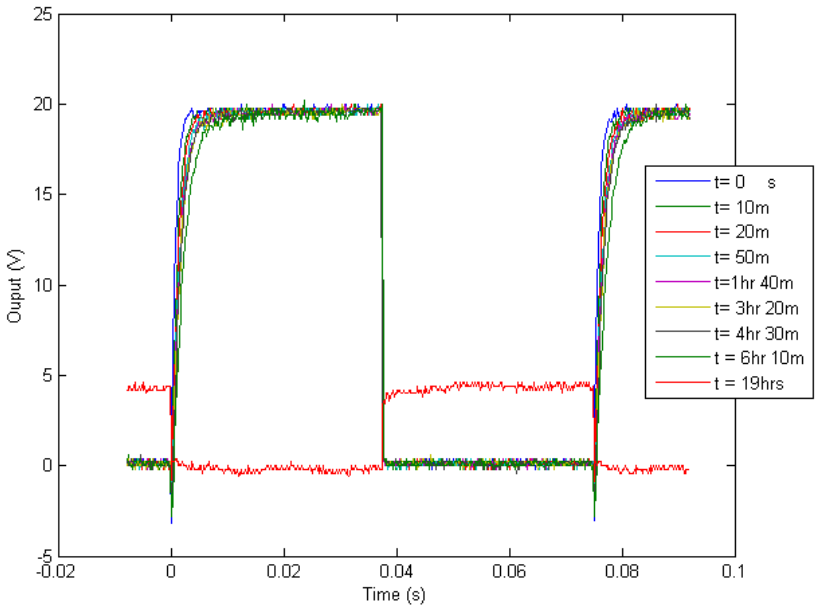

Figure 33. The impacts of competing effects in CMOS inverter

Comments

Integrated flexible CMOS design can cause a significant leap in the commercially available fully flexible products like e-newspapers or e-textile however there are some important drawbacks in the manufacturing process and in the materials used. Pentacene, being extremely sensitive to the oxygen and the moisture, degrades even without electrical stress. Unless an appropriate barrier layer is

introduced, the products would have a limited shelf life. Also the drive strength of the nMOS type transistors was significantly higher than the organic pMOS transistors even though the transistors were sized accordingly, causing stuck logic values on complex circuits. The IR-Tag project was cancelled due to the high number of pMOS gates and yield problems in the UTD fabrication line, also because of the extra strength in the nMOS logic due to the lower than expected threshold voltage for nMOS transistors manufactured at the FDC due to process improvements.

ELECTRONIC TEXTILE

Background

Incorporating electronics into clothing has been investigated for many years. One of the early adaptations is an "Antistatic Garment" (Harold H. Webber & Pauline F. Riordan, 1972) which introduces conductive fabric in the yarn to give antistatic properties to the cloth. The concept of introducing conductive elements into the fabric was adopted for other applications than clothing as well. In 1980 a patent for an "Electrically Conductive Fabric" was filed for detecting rips in the conveyor belts. The fabric would be formed by introducing conductive carbon particles into an insulating filler material then be incorporated to the materials used in conveyor belts. The conducting particles would act as equally spaced antennae and couple an electrical signal from a transmitter probe to the receiver probe as they pass by in the moving conveyer belt (Blalock, 1981).

Electronic textile was also used in context awareness and biomedical monitoring fields as e-textile based health monitoring systems, because of their close coupling with the human body, providing a promising substrate for the deployment of sensors, and wide area sensor distribution which enables functions not feasible with monolithic box-based ambulatory sensing systems while making it possible to successfully annotate medical data with diverse context

information without user intervention (Edmison, Lehn, Jones, & Martin, 2006). The circuits used in these applications however are composed of discrete components that are located into the fabric using pockets thus only creating an electronic included textile versus an electronic textile. Farringdon et al, on the other hand used knitted stretch sensors which give linearly increasing asymptotic resistance with stretch and can be stretched up to 50% of the length, and knitted conductive fiber for transmitting an electrical signal instead of wiring the sensors to the terminals.(Farringdon, Moore, Tilbury, Church, & Biemond, 1999).

An alternative approach to make a fabric more electronic was to construct the discrete components on the textile substrate. E. Post et al. in a study published in 2000 evaluated the various methods of implementing the discrete components on the textile substrate and how to provide connections between the components. Evaluated connection methods included e-broidery, conductive yarns (various forms of conductive stainless steel yarns either with 100% stainless steel conductive steel fibers, or various composites of polyester and/or nylon added stainless steel or other conductive fibers), as well as metallic silk (finely woven silk fabric with a thin gold helix wrapped around each thread) (E. R. Post, Orth, Russo, & Gershenfeld, 2000). Component integration and package design in textile circuitry is also

evaluated in the same study and is later patented (E. R. Post, Orth, Cooper, & Smith, 2001).

Another method for incorporating electronics into textile was securing a flexible circuit board into a fabric thus eliminating the needs for custom tailoring conductive yarns in the textile (Farrell, Nguyen, Teverovsky, Slade, & Powell, 2004).

However, none of the methods researched used circuits fabricated on polymers which are then weaved to make a textile. The closest invention at this time is found in a patent awarded in 2009 and is described as

> a woven article having an electronic function interwoven therein, comprising at least one electrically conductive yarn and at least one functional yarn comprising a flexible elongated insulating electronic substrate, and has a plurality of electronic devices disposed on and mechanically affixed to the said flexible substrate(Hill et al., 2009) .

This patented idea is the closest to our implementation of an electronic textile since a functional substrate is used in the weaving process but it still requires electrical signals to be delivered through other conductive yarns and the discrete components are still mounted on the functional substrate.

i-Textile

Electronic textile and the e-textile terms have always been used for electronic components mounted on textiles however it lacks the interactivity since the fabric itself is not interactive which the sensors and sensor networks are associated with, and is at most used as a substrate. Therefore a new term i-Textile is proposed where the fabric does indeed become the computer eventually (Jayaraman, Kiekens, Grancaric A.M., NATO Public Diplomacy Division, & NATO Programme for Security through Science, 2006). The "Electronic Textile Project" is the first to demonstrate the functional yarns that can be weaved to create an interactive fabric.

Electronic Textile Project

Current flexible large area sensors have limited axial curvatures and may not be used to cover an irregularly shaped object. That's why a different approach is necessary in the manufacturing process of these large area sensor arrays if they are meant to be integrated on complex geometrical objects like clothes. In the proposed detection textile, PEN wafers with long arrays of sensor structures are cut in strips and weaved to make a textile which can conform to complex shapes. The textile design is shown in Figure 34 below:

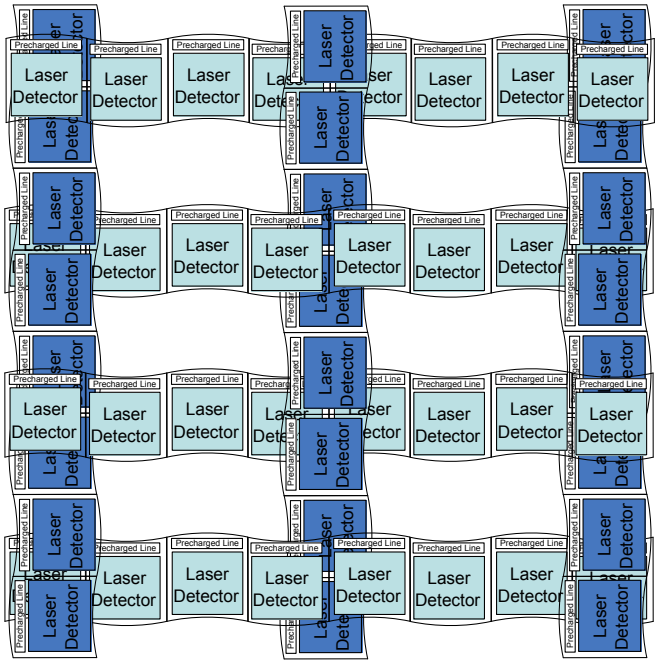

Figure 34. Weaved textile design

Laser Detector Circuit

The laser detection circuit is a subcircuit composed of 3 TFTs, two of which are light shielded by additional opaque layers while the third unshielded TFT is diode connected and is used for light detection. The circuit is shown in Figure 35 below.

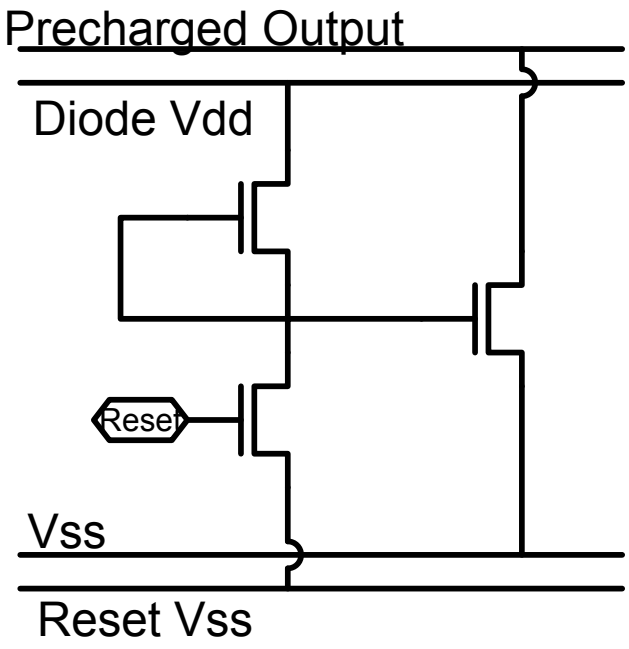

Figure 35. Laser Detection Circuit

A diode connected TFT approach is chosen because during the design period, Flexible Display Center was not capable of manufacturing flexible diodes. Preliminary tests on amorphous silicon TFTs with laser diodes and other light sources showed two to three orders of magnitude change in reverse bias current.

Testing Procedure

96/9 μm (W/L) size amorphous silicon TFTs manufactured on PEN substrate were connected to a Keithley 4200 parametric analyzer using a probe station. First, an I_d vs V_{gs} plot was obtained under no illumination, then the same plot was obtained while the TFT was illuminated using a green laser pointer. The parametric analyzer setup can be seen at the table below.

Table 3

The Parametric Analyzer Setup for Light Sensitivity of TFTs

Device Terminal	Source	Drain	Gate
Instrument	SMU3	SMU4	SMU5
Name	SourceV	DrainV	GateV
Forcing Function	Voltage Bias	Voltage Step	Voltage Sweep
Master/Slave	N/A	Master	Master
Start/Level	0	5	-20
Stop	N/A	20	20
Step	N/A	5	0.1
Number of Points	0	4	401
Compliance	0.1	0.1	0.001
Measure I	No	Measured	Measured
Measure V	No	Programmed	Measured
Range I	Limited Auto=1uA	Auto	Limited Auto=1uA
Range V	Best Fixed	Best Fixed	Best Fixed
Range C	N/A	N/A	N/A
Dual Sweep Mode	N/A	N/A	Disabled
Pulse Mode	Disabled	N/A	Disabled
Hold	N/A	N/A	N/A
Frequency	N/A	N/A	N/A
Frequency 2	N/A	N/A	N/A
Number of Pts.	N/A	N/A	N/A
AC Voltage	N/A	N/A	N/A

Figure 36 and Figure 37 below show the drain current measured with the drain voltage V_{DS} = 5V and V_{DS} = 20V respectively. Unfortunately the brightness of the laser diode changed occasionally causing slight bumps in the curves obtained. In both cases, a 2 orders of magnitude shift in current was observed under illuminated conditions at V_{GS} = -20V and about 1 order of magnitude shift at V_{GS} = -5V.

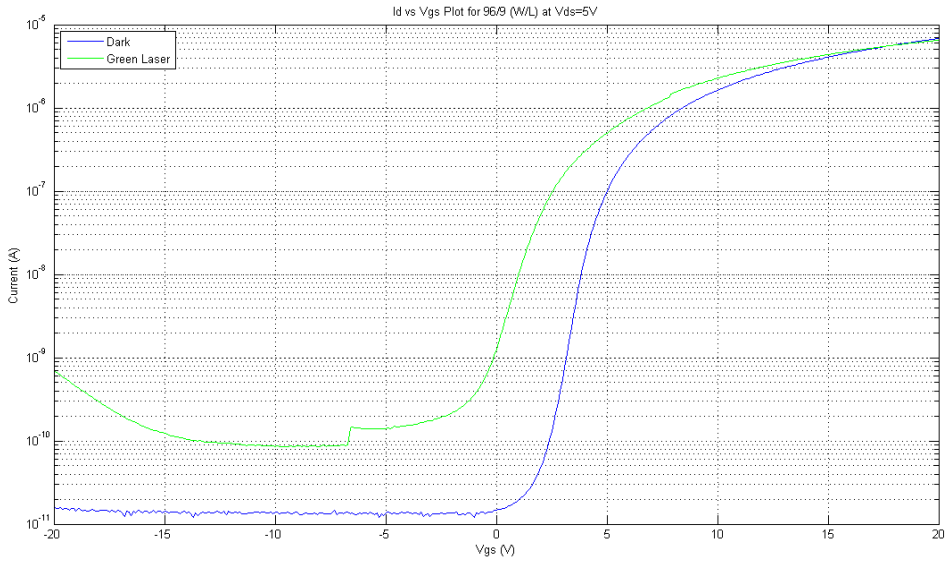

Figure 36. Id vs Vgs Plot for a 96/9 µm (W/L) amorphous silicon TFT under dark and illuminated conditions. Vds=5V

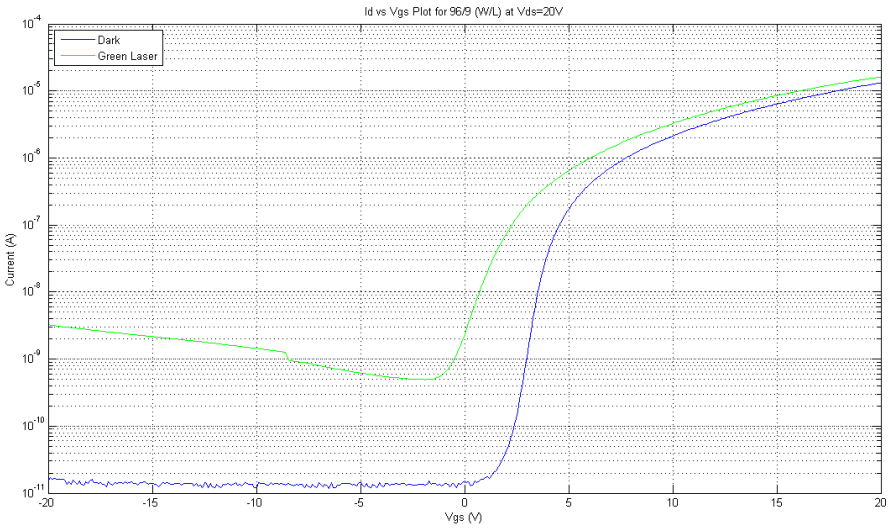

Figure 37. Id vs Vgs Plot for a 96/9 µm (W/L) amorphous silicon TFT under dark and illuminated conditions. Vds=20V

For the second part of the preliminary tests, the drain and source of the TFTs were connected together using a T shape adapter at the probe station and a diode characterization test was run using the same Keithley semiconductor characterization tool. These tests were performed at TFTs of different lengths and widths under no illumination, 2 intensities of white light, and green laser pointer. The new settings for the tool are shown in Table 4 below.

Table 4

The parametric analyzer setup for light sensitivity of diode connected TFTs

Device Terminal	Cathode	Anode
Instrument	SMU3	SMU5
Name	CathodeV	AnodeV
Forcing Function	Common	Voltage Sweep
Master/Slave	N/A	Master
Start/Level	N/A	-20
Stop	N/A	20
Step	N/A	0.05
Number of Points	N/A	801
Compliance	0.105	0.1
Measure I	N/A	Measured
Measure V	N/A	Programmed
Range I	N/A	Auto
Range V	N/A	Best Fixed
Range C	N/A	N/A
Dual Sweep Mode	N/A	Disabled
Pulse Mode	N/A	Disabled
Hold	N/A	N/A
Frequency	N/A	N/A
Frequency 2	N/A	N/A
Number of Pts.	N/A	N/A
AC Voltage	N/A	N/A

Three TFTs with the 96/9 μm (W/L) sizes were measured and the results can be seen in the next three figures below. While both of the white light illuminations were uniform in the area and was targeting the TFTs perfectly, the green laser illumination was through a point source aiming the general area. Due to safety reasons, the green laser was pointed to the probe station needle tips and the beam location was not fine tuned under the microscope. This is the reason in the following plots the laser illumination sometimes gives the same results as the 10,000 lux light source and other times as much as the high illumination source. The results were plotted using a semi logarithmic plot due to significant amount of change in magnitude in current during the sweeps. For proper plotting purposes, the absolute values of all the negative values are taken. The notches in the plots show the x-intercept points of the corresponding illuminations, and the current at the left side of the notch is in fact negative.

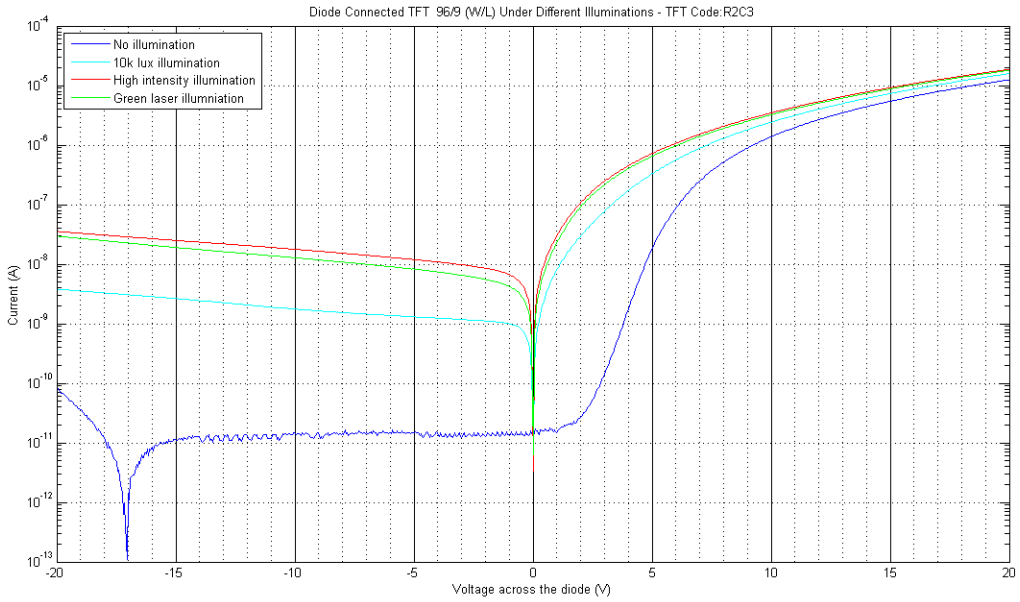

Figure 38. Diode Connected TFT 96/9 µm (W/L) Under Different Illuminations - TFT Code: R2C3

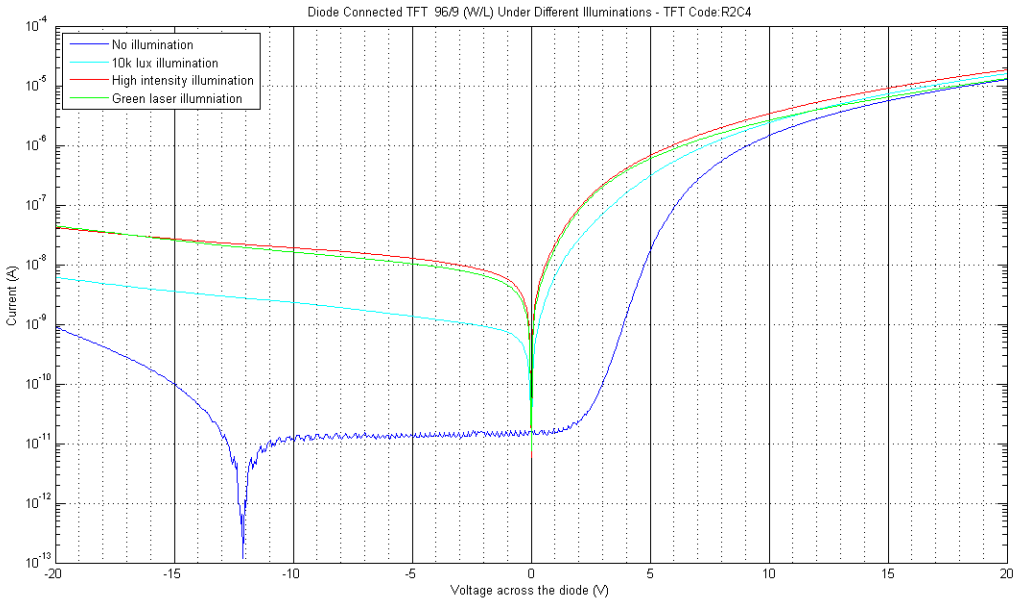

Figure 39. Diode Connected TFT 96/9 µm (W/L) Under Different Illuminations - TFT Code: R2C4

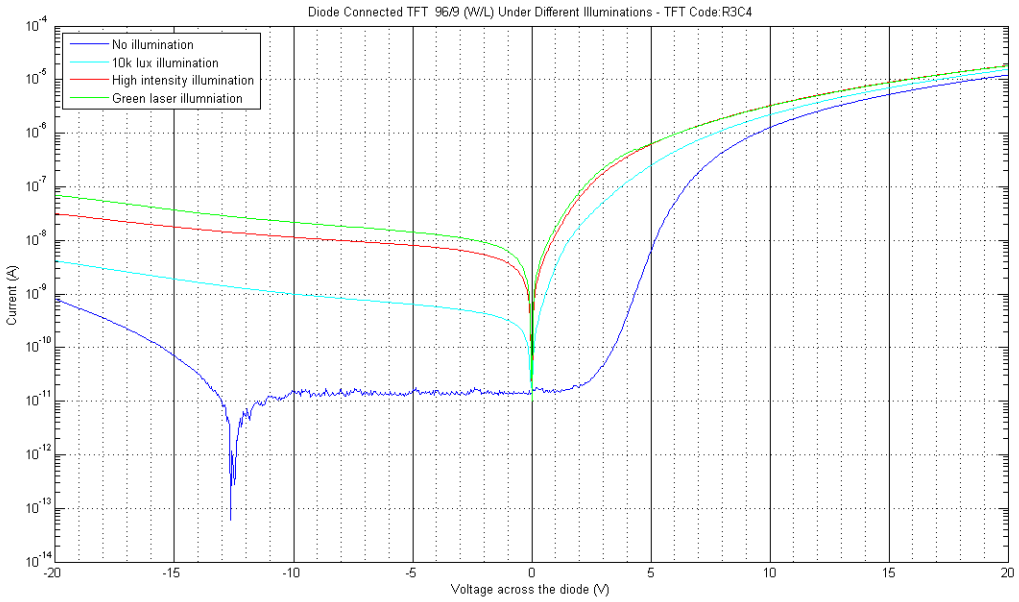

Figure 40. Diode Connected TFT 96/9 µm (W/L) Under Different Illuminations - TFT Code: R3C4

All the TFTs showed around 2 orders of magnitude shift in the reverse bias current when illuminated with 10,000 lux white light source when a diode voltage of V_D = -5V was applied across the terminals. The shift was even greater, even exceeding 3 orders of magnitude with higher intensities of light.

In all these three TFTs, it was observed that the transistors were indeed acting like a photodiode when the gate was connected to the source or the drain terminal. To further speculate this observation, other TFTs with different sizes were measured under the same conditions as well. Below are the plots for three TFTs with sizes of 108/27 and 108/54 µm (W/L) and a 432/9 µm (W/L).

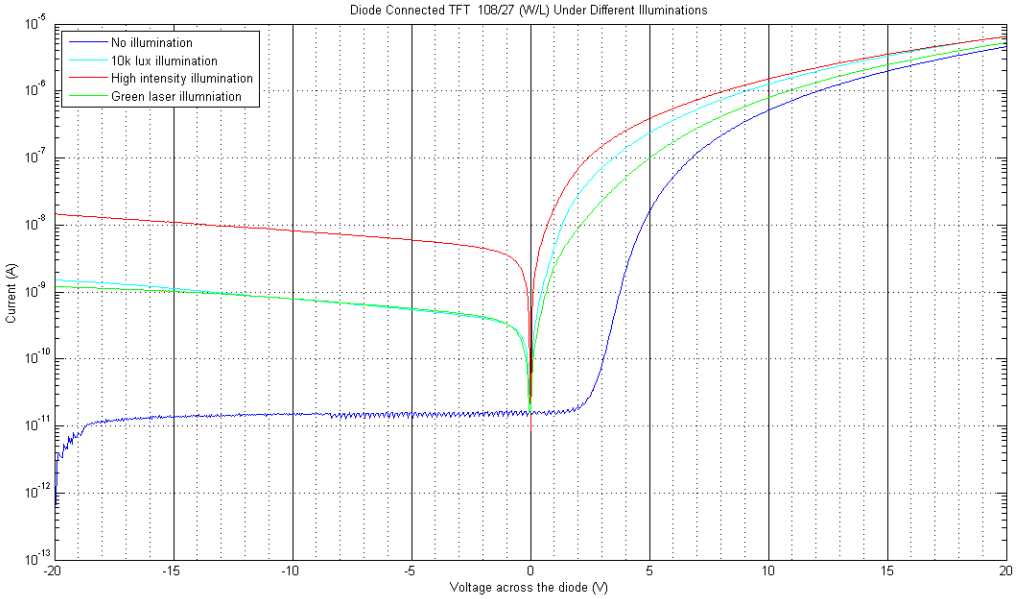

Figure 41. Diode Connected TFT 108/27 µm (W/L) Under Different Illuminations

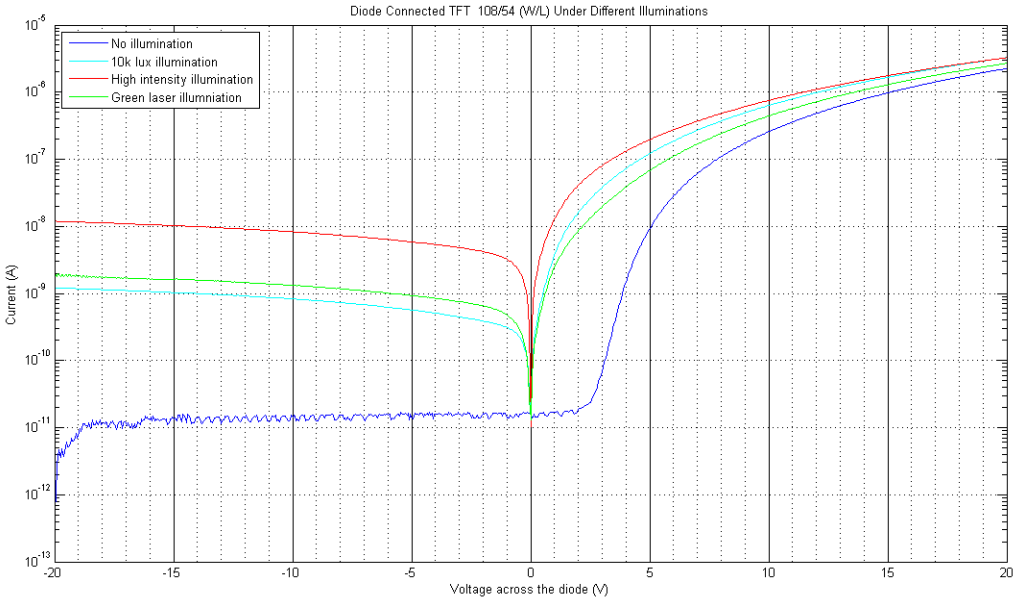

Figure 42 - Diode Connected TFT 108/54 µm (W/L) Under Different Illuminations

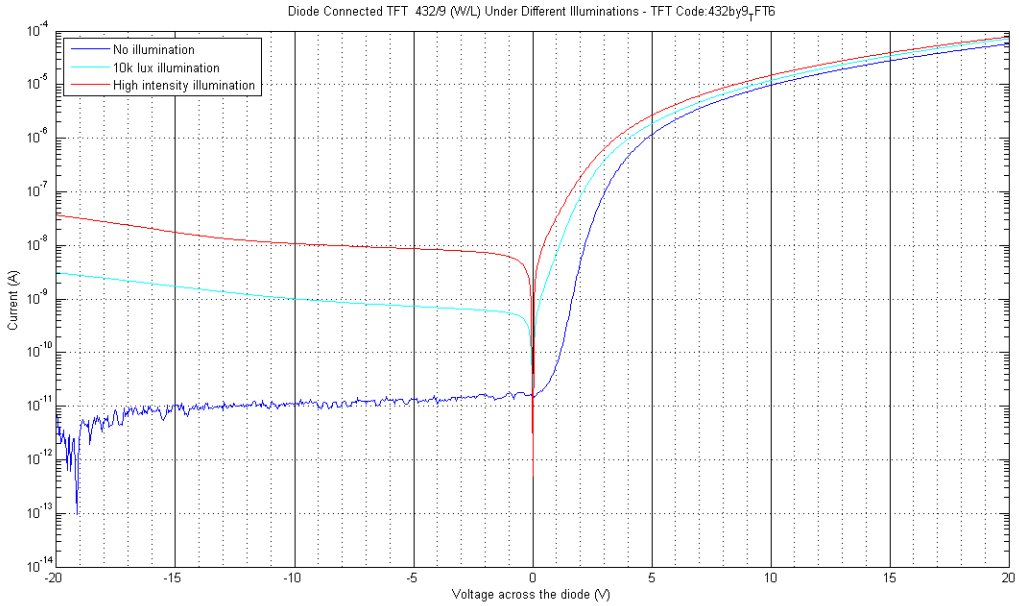

Figure 43. Diode Connected TFT 432/9 µm (W/L) Under Different Illuminations

Unfortunately, the plots for these transistors showed that the current values under reverse bias voltage are almost the same thus preventing to come to a final conclusion. As can be seen from Figure 44, the TFTs with the length of 9µm only have 3µm of length where the active material (amorphous silicon) can be illuminated because of the design rules.

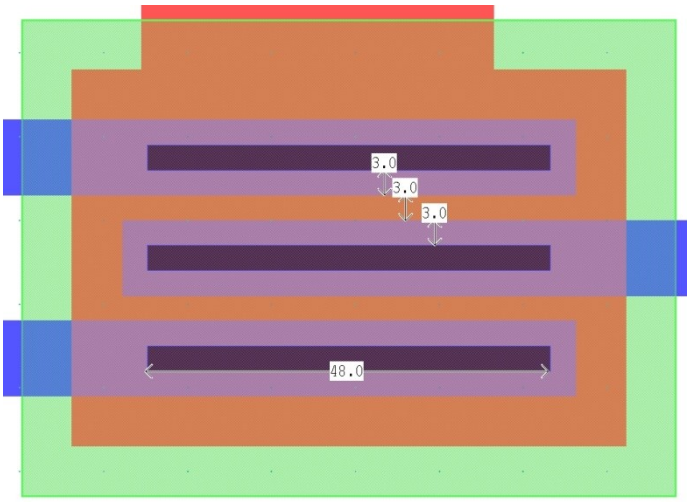

Figure 44. Layout of a 96/9 µm (W/L) TFT

On the other hand, a TFT with a larger length like 108/54 µm (W/L) TFT tested here, the length of the active area that can be illuminated is 48 µm. The area that can be illuminated in a 108/54 µm (W/L) TFT is 5184 μm^2 versus 288 μm^2 in a 96/9 µm (W/L) TFT however the majority of the electrons created are thought to be regenerated before reaching the contacts due to the significant increase in the distance. To further understand the operation of the device, simulations using programs like Silvaco Atlas are required.

Circuit Design

Based on the data obtained from the illumination tests on diode connected amorphous silicon TFTs, the following circuit was designed.

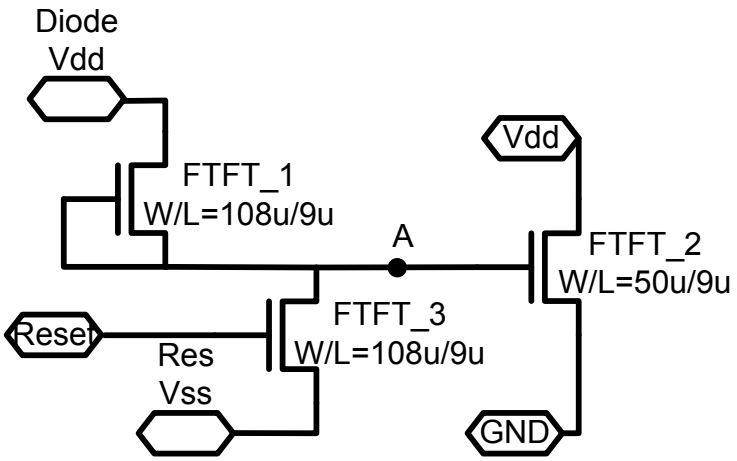

Figure 45. Laser detection circuit

In this schematic, FTFT_1 is the diode connected transistor with its anode connected to a diode voltage that will be supplied by a constant voltage source. FTFT_2 is the output transistor which has its drain terminal connected to a precharged output line, and FTFT_3 is the reset transistor with its gate connected to a clock input. The circuit operation can be explained as the following:

- While the RESET signal is high, FTFT_3 is on and the node A is discharged to RESVSS level. FTFT_2 is off, and OUTPUT is precharged to VDD.
- When the RESET signal is low, the supply for the OUTPUT goes to high impedance mode and the node floats.
- If there is no light source, the dark current from the diode connected TFT slowly increases the potential at node A which

was floating at ResVss level by charging the built in Cgs and Cgd capacitances of the FTFT_2 and FTFT_3 at a rate of 10 pico Coulombs per second.

- The RESET signal goes high again before enough charges accumulate in node A to turn FTFT_2 on. The OUTPUT level is read right before the RESET signal is high again. Under calibrated conditions, the output should still be in logic high levels.

- If there is a laser source targeting FTFT_1, then the built in capacitances are charged at an a lot higher rate (1n Coulombs / sec) and the voltage at node A rises enough to turn FTFT_2. The floating OUTPUT line is discharged through FTFT_2 to VSS level.

- The OUTPUT is read before the RESET signal goes high.

Below is a sample simulation circuit setup which contains two blocks of laser detection subcircuits, one of which is illuminated, and the other one is not. The diode connected TFT in the subcircuit targeted with a laser source is replaced by two current sources, one for the dark current and the other for the reverse current caused by the illumination. Both blocks are connected to the same supply and output signals. The output signal is then connected to the source terminal of a

TFT that is connected to a voltage source on the drain, and RESET signal on the gate. This TFT is used for precharging the ROW line when the RESET signal is high.

During the preliminary tests, the ROW line is connected to an op-amp connected in unity gain configuration and the output is read from the output of the buffer amplifier. The unity gain amplifier is not included in the simulations.

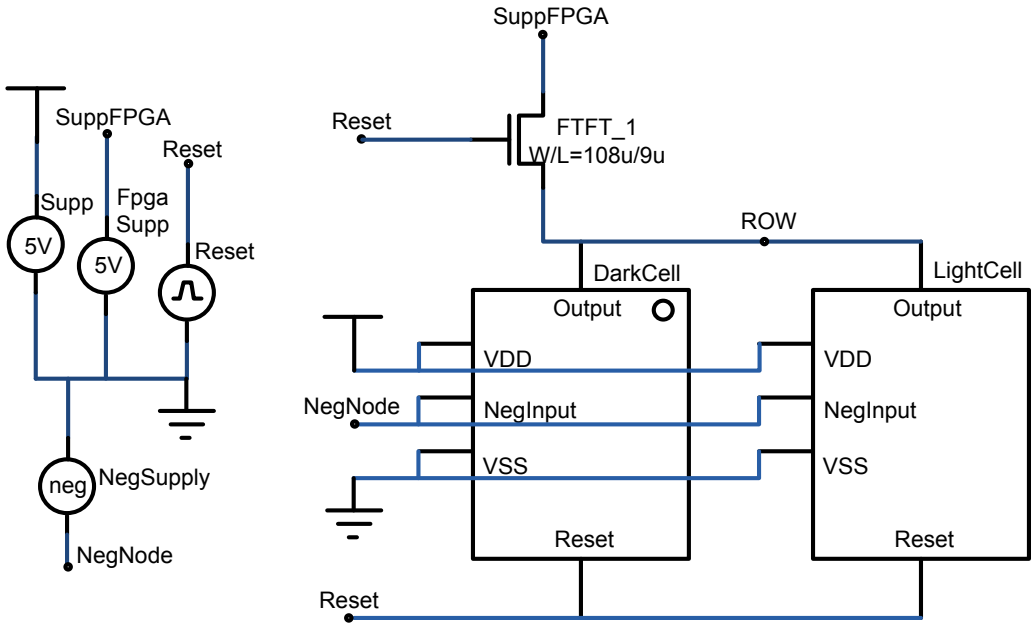

Figure 46. Test setup

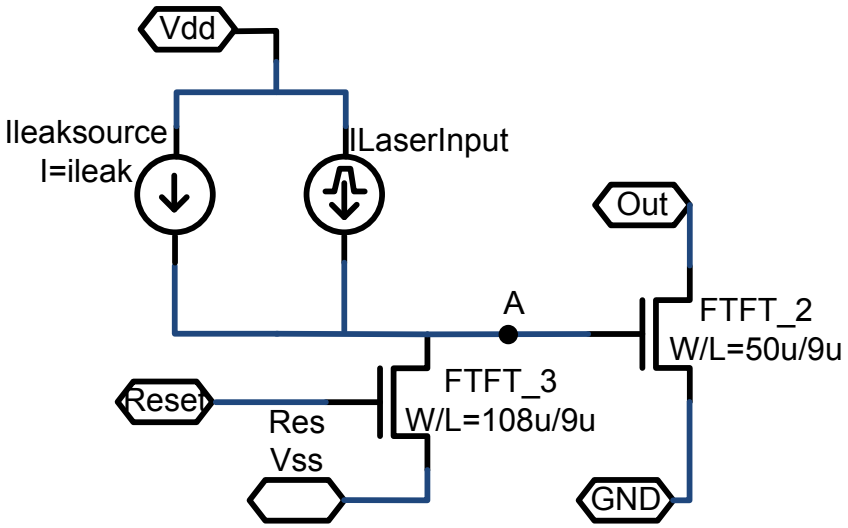

Figure 47. Simulation of a laser targeted subcircuit

The parameters for the simulation are given in the table below: The simulation output can be seen in Figure 48 below. The first row is the RESET signal; the second row is "Node A" of the non illuminated block; the third row is the "Node A" of the illuminated block and the last row is the output signal.

Table 5

Parameters for the 2 Block Simulation

Parameters		Value
TFT Sizes (W/L) (µm)	FTFT_1 (Diode connected TFT)	108/9
	FTFT_2 (Output TFT)	50/9
	FTFT_3 (Reset TFT)	108/9
Biasing	Supp (For DiodeVdd)	5V
	SuppFPGA (For precharging)	5V
	NegSupply (For ResVss)	-1V
	Vss	0V
	Reset (Pulse)	High: 5V Low: -1V
	Ileak (Dark current)	10pA
	ILaserInput (Reverse bias current)	High:1nA Low:10pA
Timing	Reset Pulse Width	10ms
	Reset Period	20ms
	ILaserInput Pulse Width	1s
	ILaserInput Period	2s
	IlaserInput Delay	40ms

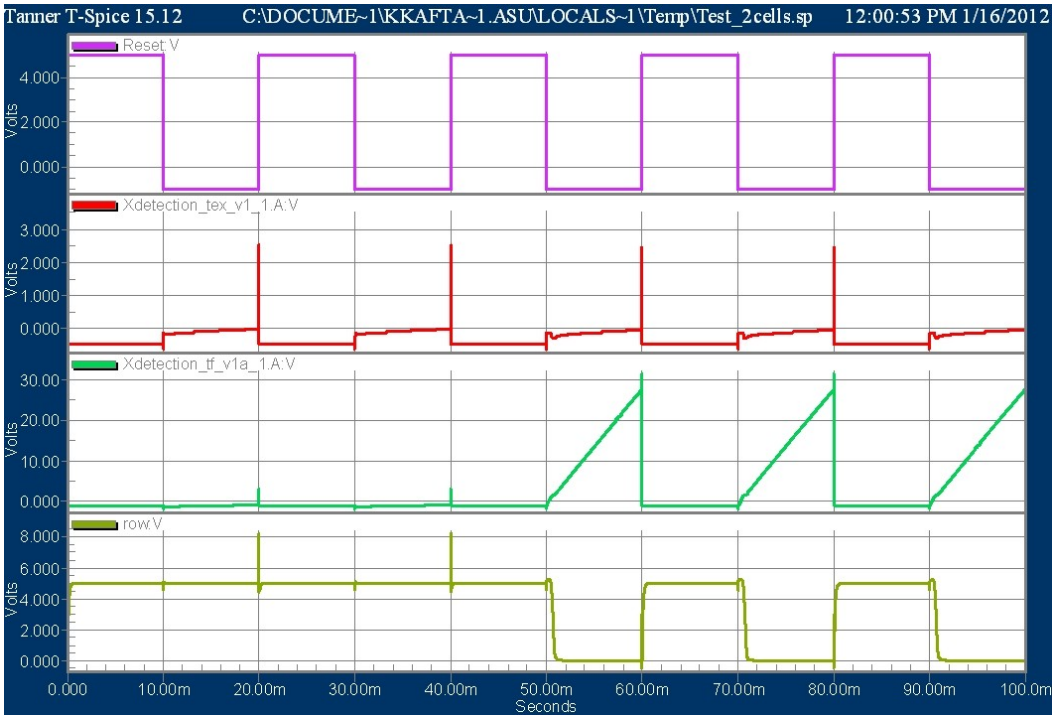

Figure 48. Two block simulation output

As can be seen from the plot, the potential of "Node A" of the dark block is held at a negative value while RESET is high and a slow increase is observed while RESET is low. The same observations can be made for the illuminated block for the first two cycles as illumination starts at the third cycle. During the first two cycles when both blocks are not illuminated, the output remains at the precharged value. At the third cycle and after, one of the blocks is illuminated and "Node A" of the illuminated block sees a much higher rate of a potential increase. Before the RESET is high again, we see that "Node A" reaches to 27V from -1V. This 28V change in potential is about the same as expected value since the parasitic capacitance was estimated

to be about 307fF from the layout and the calculations below show the parasitic capacitance is simulated to be 357fF:

$$I = \frac{\partial Q}{\partial t}$$
$$Q = \int_{0}^{10 m\sec} (1nAmp)\partial t$$
$$Q = 10\,pCoulombs$$
$$Q = C * V$$
$$C = \frac{10\,pCoulombs}{28V}$$
$$C = 357\,fF$$

The Circuit Layout

The layout of the subcircuit is shown in Figure 49. Each subcircuit is 185 μm wide and 1.4mm high. The diode connected TFTs on the top are placed further from the circuit but for documentation reasons are brought closer by 700μm to the rest of the circuit. These subcircuits are arrayed to create strips of various lengths. As in the simulation, each row only had one pull up TFT at the output. The biggest textile array manufactured is 1 inch by 1 inch in size and is composed of 11 rows of 140 sensors each. Each output row is routed to a different pad thus enabling 2D point addressing in the finalized gadget. The layout of the 1" x 1" textile layout is shown in Figure 50.

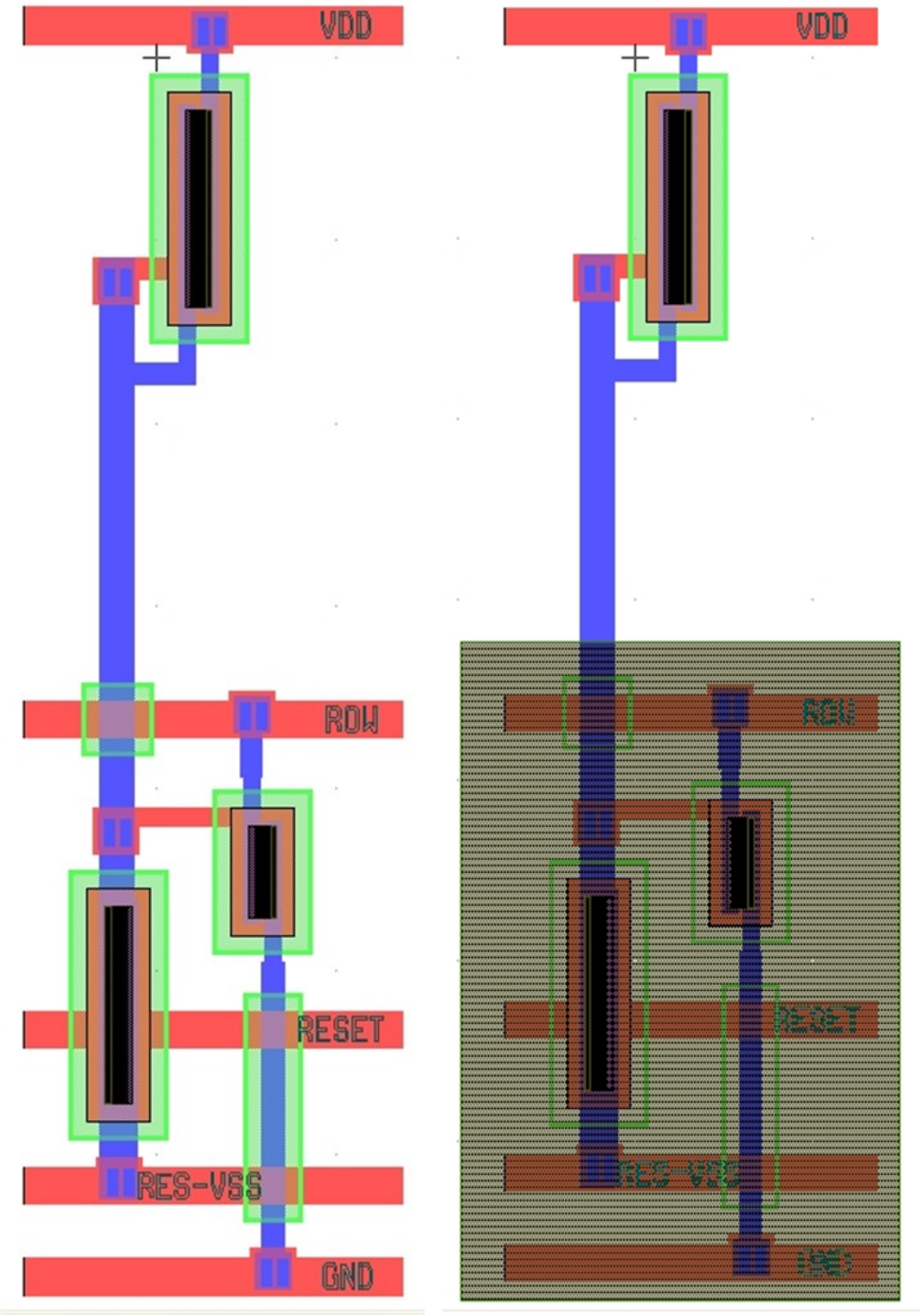

Figure 49. The layout of the subcircuit without and with the light blocking layers

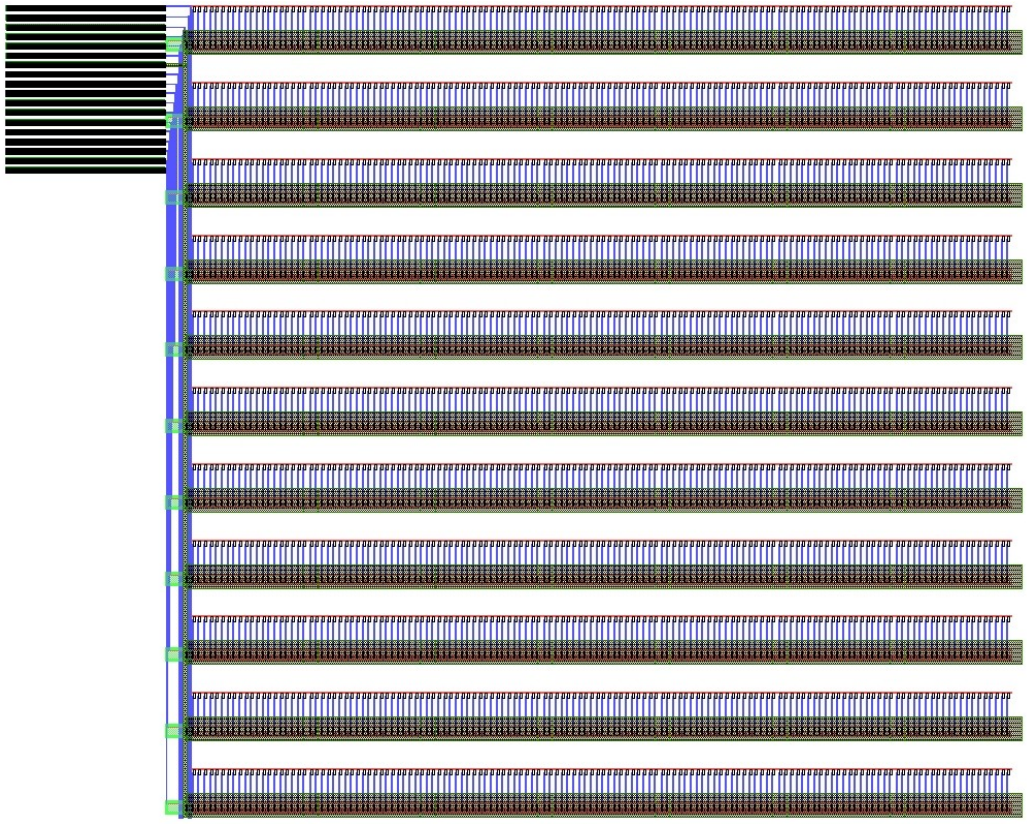

Figure 50. 1" x 1" Laser detection sensors

Circuit Testing

Initial post manufacturing strip tests. After the circuits are fabricated at the FDC, initial tests were performed on the single strips by the same method as described in the simulations. While the tested circuits performed as they were expected to, tuning on the biasing and the frequency of the RESET signal was required. The plots obtained from the oscilloscope can be seen in figure Figure 51 and Figure 52. In these tests, the RESET signal was oscillating between –5 volts and +10V with a 500ms period and 100ms pulse width. The VDD and

DiodeVDD were both at +10V while VSS and RESVSS were both at 0V.

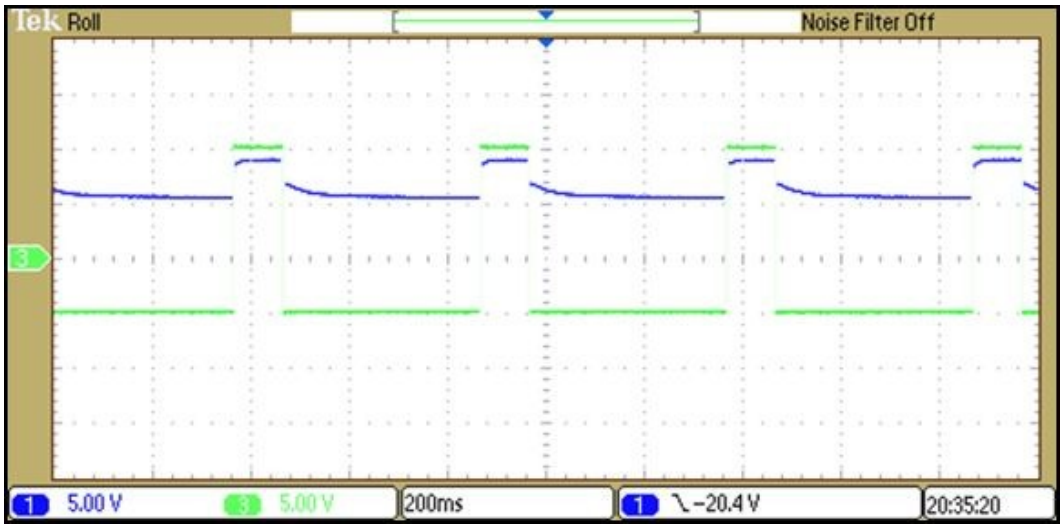

Figure 51. Output of a non illuminated array

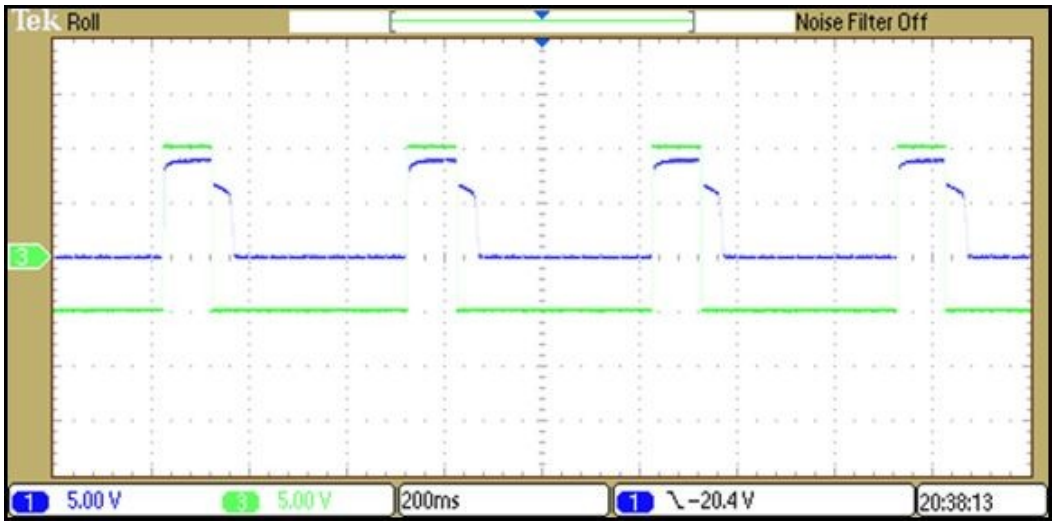

Figure 52. Output of an illuminated array

Functionality test. One biggest block, a 1" by 1" structure composed of 11 lines each of which had 140 sensor pixels was separated from the wafer and was heat sealed from the pads to a

flexible ribbon with a connector adaptor at the other side (Figure 53). The test structure can be seen in Figure 54 below. For a live functionality test, the following test setup was built on a breadboard.

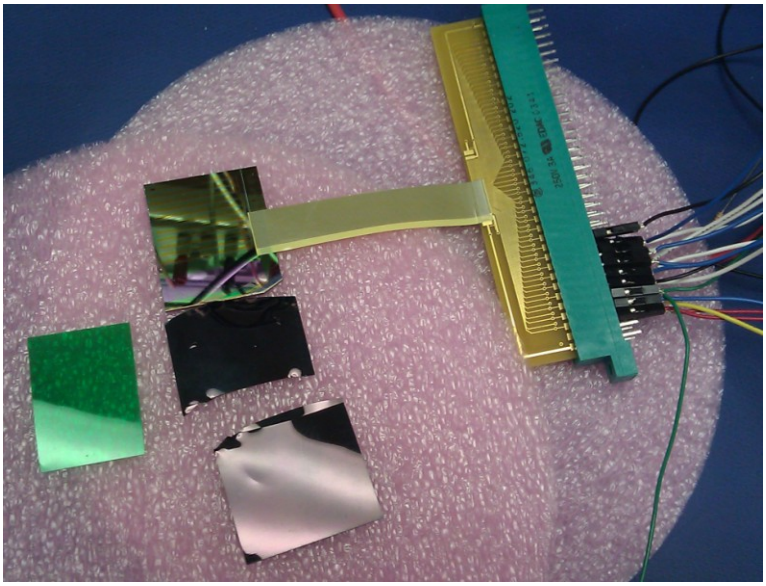

Figure 53. Bonded 1"x1" test circuit with the color filters

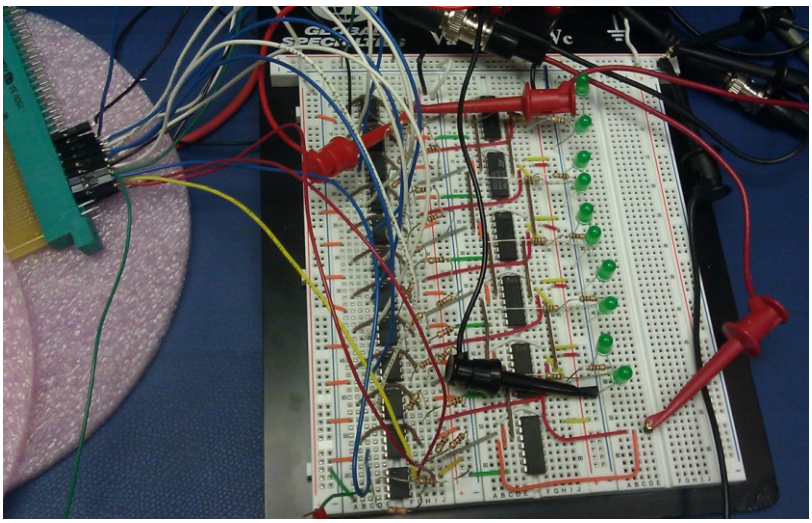

Figure 54. Test setup

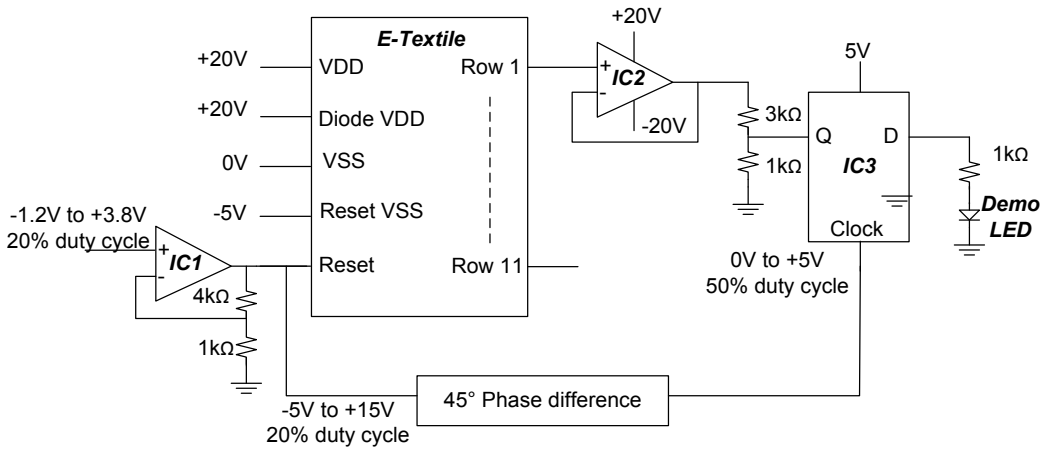

Figure 55. Test setup diagram

IC1 is an operational amplifier connected with a 5X voltage gain setup to provide an input voltage swing of -5V to 15V from the signal generator since the generator was not capable of providing a 20V swing. IC2 is another operational amplifier with a unity gain setup. This setup was necessary to provide a high-impedance on floating line side to avoid any leakage through the reading circuitry, and to be able to drive the following ICs. Each output of the textile row was connected to a separate op-amp for individual readings of the lines. The output of the IC2 was between 0 and 20Vs, which was higher than the input limitations voltage limitation of the IC3 – 74LN74 D Flip Flop- therefore a 4 to 1 voltage divider circuit was implemented between the output of the IC2 and the input of the IC3. The output of the IC3 was connected to a 1k ohm resistor and an LED for visual demonstration.

Two signal generators were used for this circuit. One for providing the reset signal to the textile which discharged the sensing node, and precharging the output node, and one for clock input of the flip flops. Since a certain time period is necessary for the sensing node to reach a certain potential even when activated immediately after the circuit is reset, a time delay is necessary between the reset and the clock signal. Signal generator 2 which provided the clock signal was set to be triggered by the rising edge of the signal generator 1 with a 45° phase shift. This phase shift enabled enough set up time for the output signal.

One of the outputs (line 1) was also connected to an oscilloscope to observe the signal values in addition to the visual inspection by the LEDs. Several plots shown below are screenshots obtained from the oscilloscope during a demo. For all the screenshots below, the color coding is the following:

Table 6

Oscilloscope Output Legend

Channel	Color	Signal
1	Blue	Output
2	Red	Reset (No amp)
3	Green	Clock
4	Pink	Input for IC3

Since the sensors went active on the laboratory lighting conditions without additional excitement through a laser source, 3 color filters were located on top of the sensor structure acting as a band pass filter for the green light. However, while these filters were blocking the majority of the spectrum, they were also significantly reducing the green light transmission. In Figure 1 the rows are not excited by any light source and the measurement was made with the filters on the circuit while the lab is illuminated.

As can be seen, the output is precharged to 18V while the RESET signal is high. However it is yanked down to 12V when the RESET signal goes to -5. This is due to the charge sharing in the capacitances between the RESET signal bar and the floating OUTPUT signal bars due to overlap in the layout. We see that the output gradually increases to 14V within a period and this can be explained by the charge sharing between the sensing node (which has been denoted as NODE A previously) and the OUTPUT signal bar due to

the Cgd capacitance of the output transistor - FTFT_2. The frequency of the signal generators was set to 2Hz which prevented enough charge to accumulate in NODE A, and increase the node potential above the threshold voltage of the output transistor. With the new cycle, the OUTPUT signal is again set to 18V.

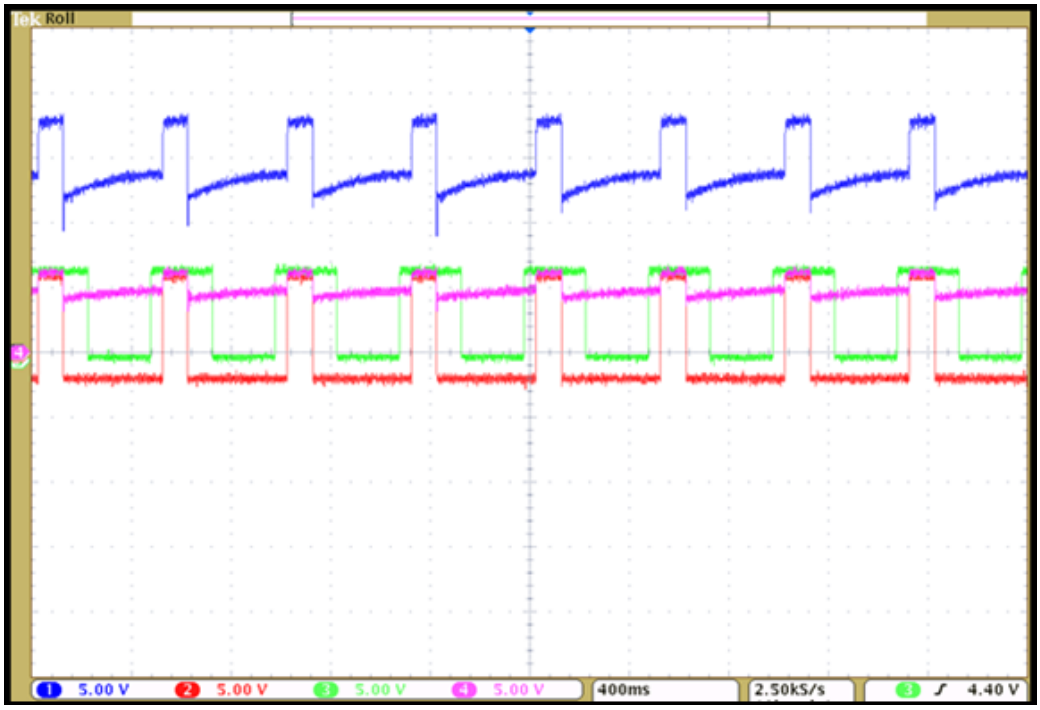

Figure 56. 1"x1" Textile test output 1

Figure 57 shows a change in the output signal as the green laser is introduced to the circuit. While the laser is directly pointing at the sensor itself, as in cycle 4, the sensing node voltage is increased (which can be observed from the coupled OUTPUT signal from the oscilloscope) until the potential is higher than the threshold voltage of the output transistor – which is then turned on thus bringing the

floating OUTPUT signal to ground level. As the laser pointer is moved away from the sensor, it takes longer time for the sensing node voltage to increase, thus taking more time for the output to react as can be seen on cycle 5 and 6. The sensor TFTs can still be excited by the diffracted laser light passing through the 3 layers of filters. While it causes an eventual voltage drop in the OUTPUT signal, it is either not caught by the latch due to the input voltage level being in the uncertainty region when the flip flop is acquiring the data as in cycle 0, or the circuit is reset by the RESET signal as in cycle 2 or 3.

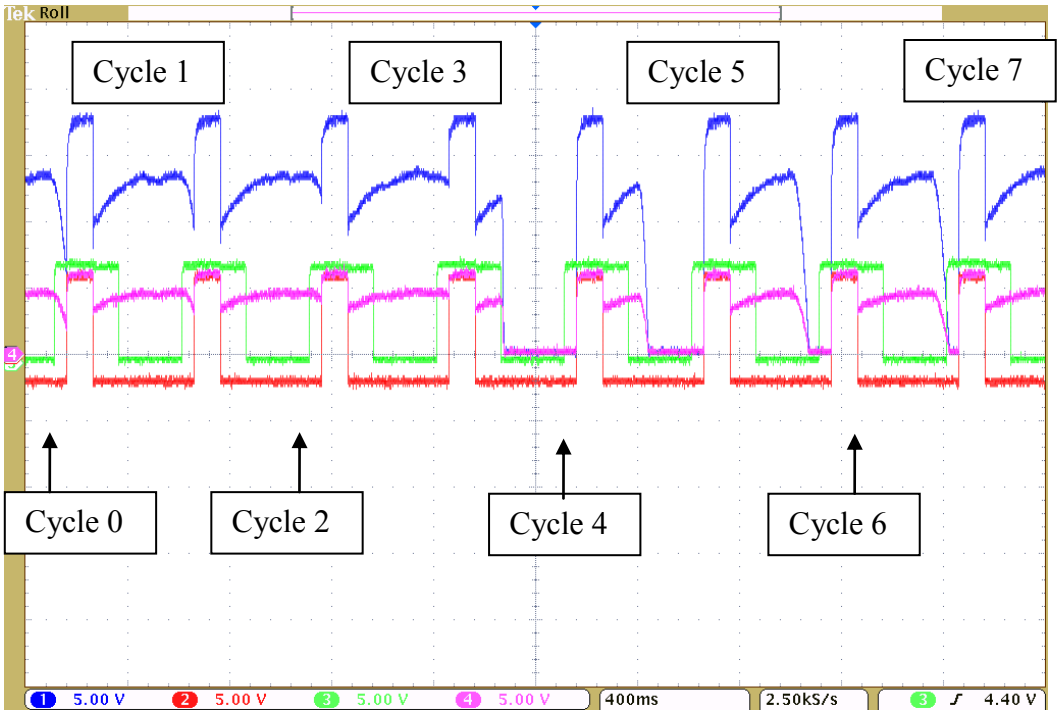

Figure 57. 1"x1" Textile test output 2

Next Gen Manufacturing

The size of the textile array is limited to the wafer used for manufacturing. The original design was laid out based on single shot UV exposure and is not expandable to a larger size. A different version of the array is laid out for next generation manufacturing methods that use step and repeat exposure where individual sections of a reticle are stepped in a pre-programmed pattern and enable manufacturing of very large area circuits with a smaller mask. This method is also used for mass manufacturing of ICs in the foundries where hundreds or thousands of ICs are manufactured on 300mm or 450mm wafers (Clarke, 2012).

The circuit layout is enhanced based on the measurements and new design criteria as can be seen in Figure 58. VDD line has been widened to 60µm from 20µm, also the metal layer is changed gate metal layer to SDMetal which has a resistivity of 0.15Ω/square versus 1 Ω/square that gate metal layer had. Therefore the voltage drop due to line resistance is decreased 20X compared to the previous version. The OUTPUT line is also changed in the same manner as the width is increased from 20µm to 80µm and the metal layer is changed to SDMetal from gate metal layer. The line is now 26.6X less resistive. This would significantly increase the signal integrity at the output node.

The new layout of the pad structure eliminates the crossing of the RESET signal the OUTPUT signal thus the coupling created due to the overlap capacitance. The new pad structure can be seen Figure 59.

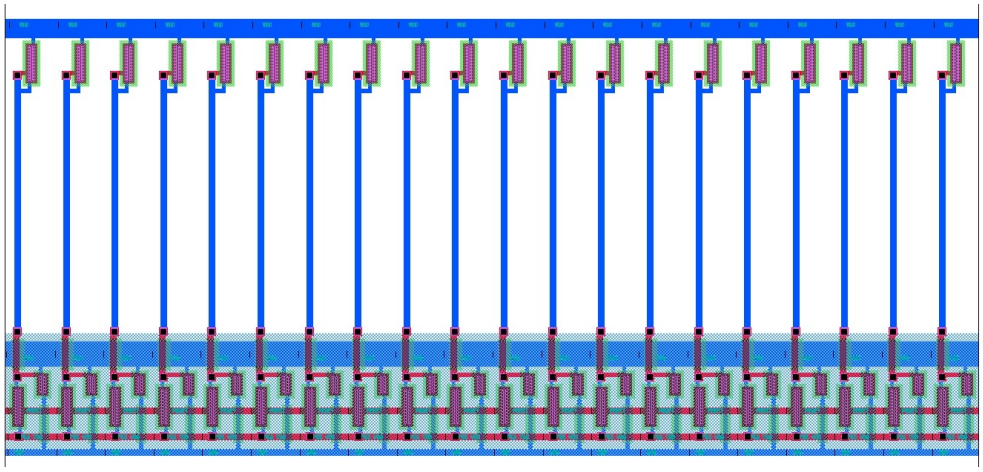

Figure 58. Revised sensor array repeating structure for step & repeat manufacturing technique

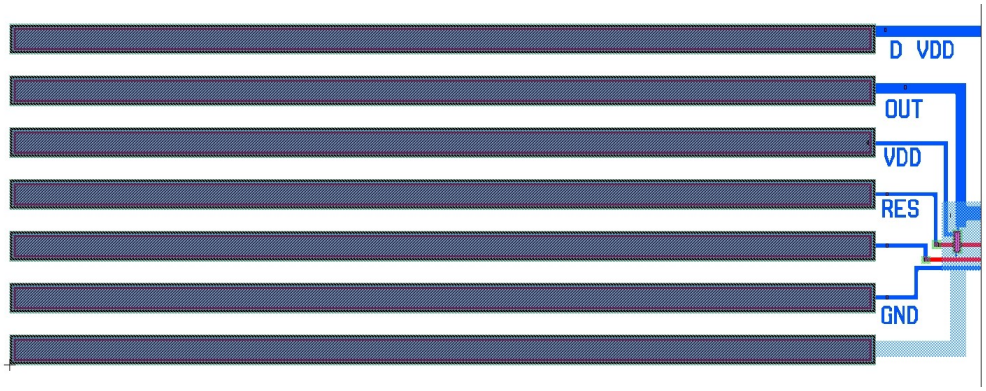

Figure 59. Revised pad structure for step & repeat manufacturing technique

Alternative Design with PIN Diode

Flexible Display Center is now capable of manufacturing p-i-n diodes at its facilities; therefore an alternative design is prepared for a step & repeat type manufacturing with p-i-n diodes as the sensors. The layout for the repeating structures can be seen in Figure 60 below. The diode connected TFT on the top of the layout is now replaced with p-i-n diode structures that are significantly larger. A sensor layer covers the whole upper area and is also used for providing the VDD signal to the p-i-n diodes. This new routing structure required new pads to be designed which can be seen in Figure 61. Again in this revision, the OUTPUT bar is 26.6X less resistive.

These two revised circuit layouts were included in one of the GEN II FDC masks however are not programmed to be manufactured yet. The layout for the reticle includes both of the revisions in the same structure; therefore each strip has a version with the proven-to-be-working diode connected TFT as well as the new p-i-n diode. This was necessary as it was the only way for fitting these layouts in the reticle due to the spacing constraints. The layout of these circuits in the reticle can be seen in Figure 62. If manufactured, each GEN II wafer can output 70 strips with each of them being 45cm long.

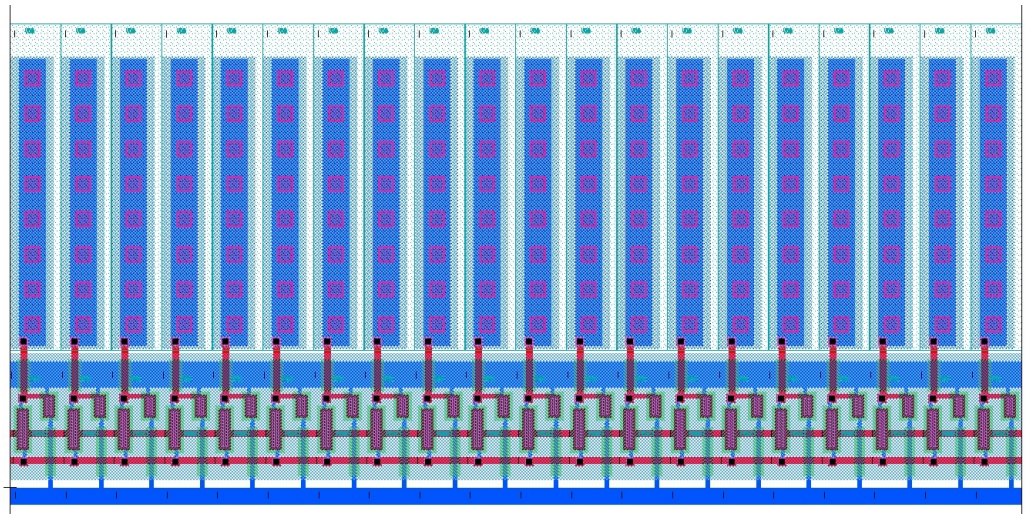

Figure 60. Alternative PIN diode sensor array repeating structure for step & repeat manufacturing technique

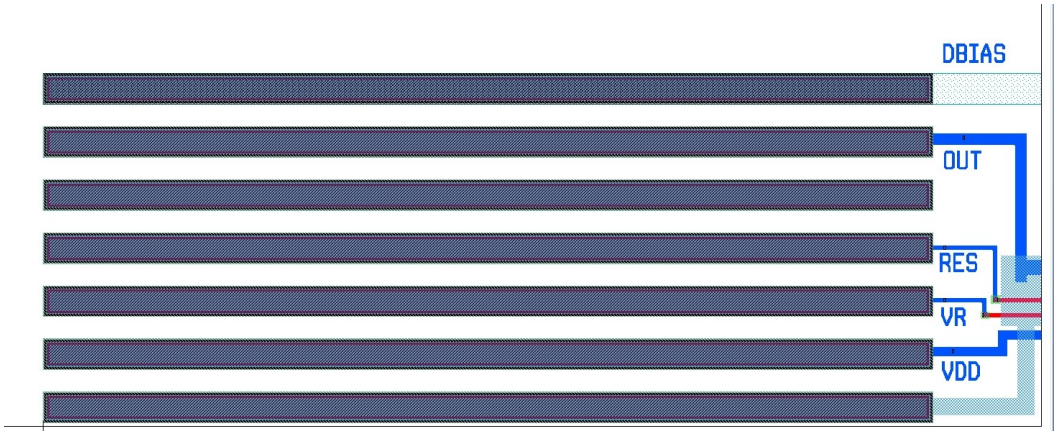

Figure 61. Revised pad structure for sensors manufactured with PIN diodes

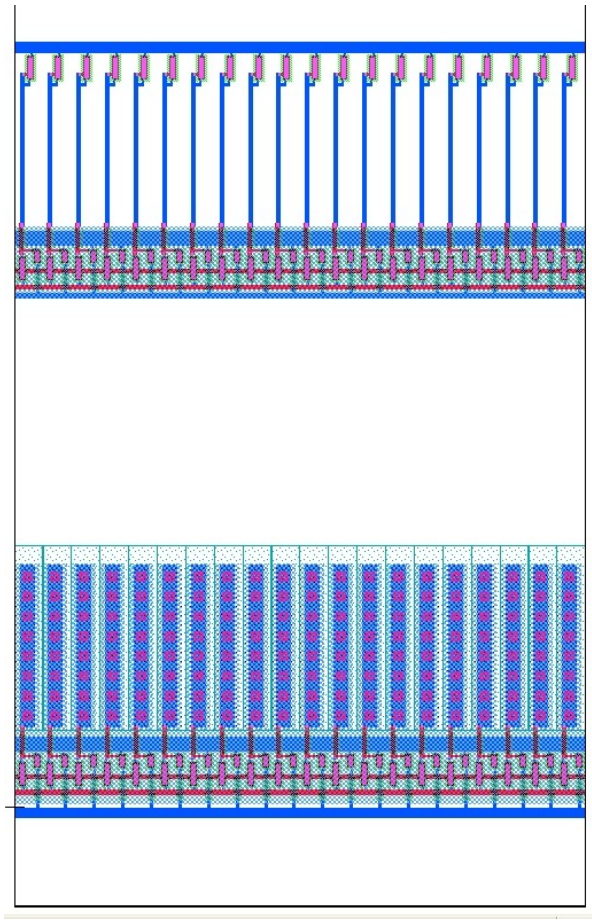

Figure 62. Reticle layout for the GEN II repeating arrays

FUTURE WORK

Creating a real textile

The layouts that got manufactured were only manufactured on a silicon wafer but not on PEN due to some fabrication issues at the time. Therefore the circuits could not be cut and weaved to each other as originally planned. However if the new GEN II layouts are manufactured on PEN, they can be weaved to create a fabric as big as 45cm by 45cm. Once the wafer is sliced precisely with an automated tool to isolate individual strips of 5mm width, these strips can be weaved at linear pitch of 7mm. A weaved fabric of 45cm by 45cm would require about 128 strips at this density which can be achieved by two GEN II panels. The signal routing can be done with the ACF bonding to a 2 sided flexible circuit board by the onsite build labs. The proposed flex would be at least 2 layers thick to accommodate the amount of individual signals. The cost of the flexible circuit board which is dependent on the amount of layers used as well as the pitch the connections would be the main determining factor of the flex design. A proposed two layer design is shown in Figure 63.

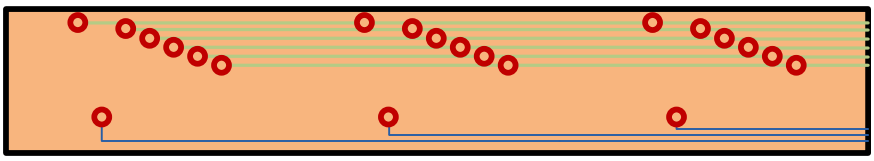

Figure 63. Proposed 2 layer flexible circuit board design

The red circles in the figure are for the contact points with the pads. The green lines are as busses for the common signals like VDD or RESET. The blue lines are connected to the individual OUTPUT pads and are not connected to the other output lines to enable addressing. The output lines can be routed on one side of the flexible circuit board while the other side carries the supply signals. Figure 64 shows a section of a proposed flex connection to a patch of a textile.

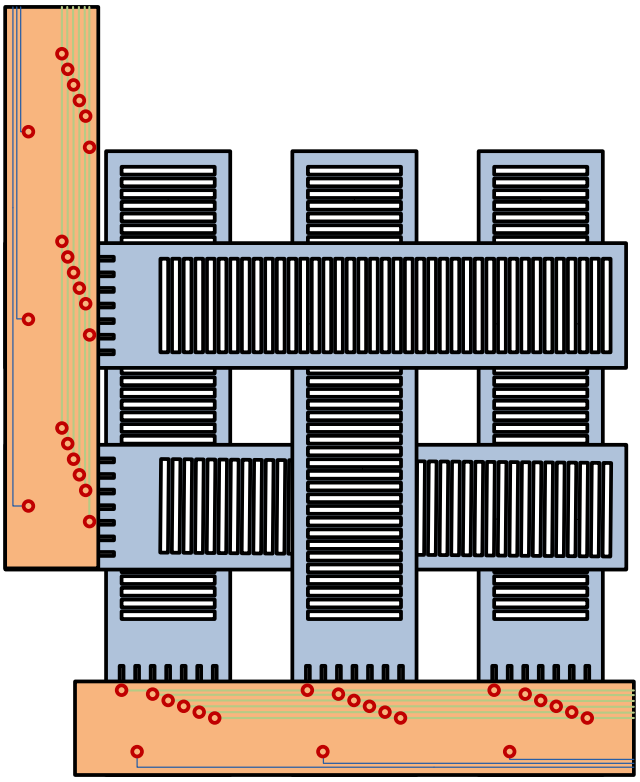

Figure 64. Electronic textile with proposed flex connection for signal routing

One way to reduce the cost of the individual flexible circuit board is to reduce the amount of OUTPUT signal routings per flex,

thus eliminating the need for expensive ultra fine pitched lines. This can be achieved by only having only a partial amount of OUTPUT signals per flex and using multiple flexes on the side of the textile.

Yet another way to reduce the amount of outputs to be processed is to decrease the resolution of the textile either by weaving it less dense or connecting every other output together. The first option of weaving it less dense however may cause the patch to lose its form unless the individual strips making the textile are mechanically fixed relative to each other at the ends. The second option relies on the idea that a laser beam aiming at the sensor from a distance will diverge and will excite more than one sensor. This is called beam divergence and was already observed by the lab tests of the 1" by 1" sensor strips layout. However the downside of this option in addition to the loss of resolution is a potential decrease in the response time in an unlikely case that the laser signal is narrow enough to only excite one row of sensor strip since the charge on both lines now will be taken down to 0V instead of just one line. However, excitation of only one line is expected to be quite a rare occasion especially considering that the source will be moving the laser on the target for a certain period of time for pinpointing, thus creating an opportunity for multiple sensor strips to be excited.

An FPGA should be used for providing necessary biasing and the clocking as well as analyzing the output data from the individual strips to adjust the textile sensitivity based on the medium and as well as perform its function of addressing a sensor trigger. The illumination level of the medium has a great impact on how fast the sensor node potential exceeds the threshold voltage of the output transistor thus, changing the output of the whole sensor strip. While this period can be as long as a few seconds when there's no illumination present, in a bright lab environment the strips gave a positive response within 50ms. The FPGA should be able to detect how bright the medium is and adjust the timing of the circuit accordingly. This can easily be achieved by evaluating how many of the outputs are giving a positive response at a given time and if these are spread across the textile or are local. If the entire fabric is giving positive results, the FPGA should realize that the medium is now brighter and it's a false positive and should adjust the RESET signal frequency to a higher level until the fabric does not give a false positive output. Live calibration can be made more accurately by also incorporating a photodiode in the flexible circuit board.

The main function of the FPGA is of course providing an accurate address of the triggered location. Since the laser is expected to diverge and activate multiple lines, it will be activating both a

horizontal and a vertical strip as in Figure 65. Knowing the exact location of the horizontal and vertical strips would then enable addressing the location the textile senses the laser.

It should also be noted that current military grade laser guidance tools use 1550nm wavelength due to the beams being invisible to even night vision goggles unlike the shorter 1000nm infra red lasers. However amorphous silicon is not responsive to these wavelengths therefore the laser detection circuit demonstrated in this project is only for the visible lasers like the laser pointer used in the experiments. Even if the material was responsive to the wavelengths used in military systems, the circuit would not be able to detect the laser since these systems use coded pulses for the signal not to be buried in solar spectrum as well as for increasing the accuracy of laser guidance as it is demonstrated that increased pulse rate increases the accuracy of the system. Current equipments use pulse rates in hundreds of kilohertz (Csanyi & Toth, 2006). Amorphous silicon is not responsive enough to detect pulses that are used in these military equipments.

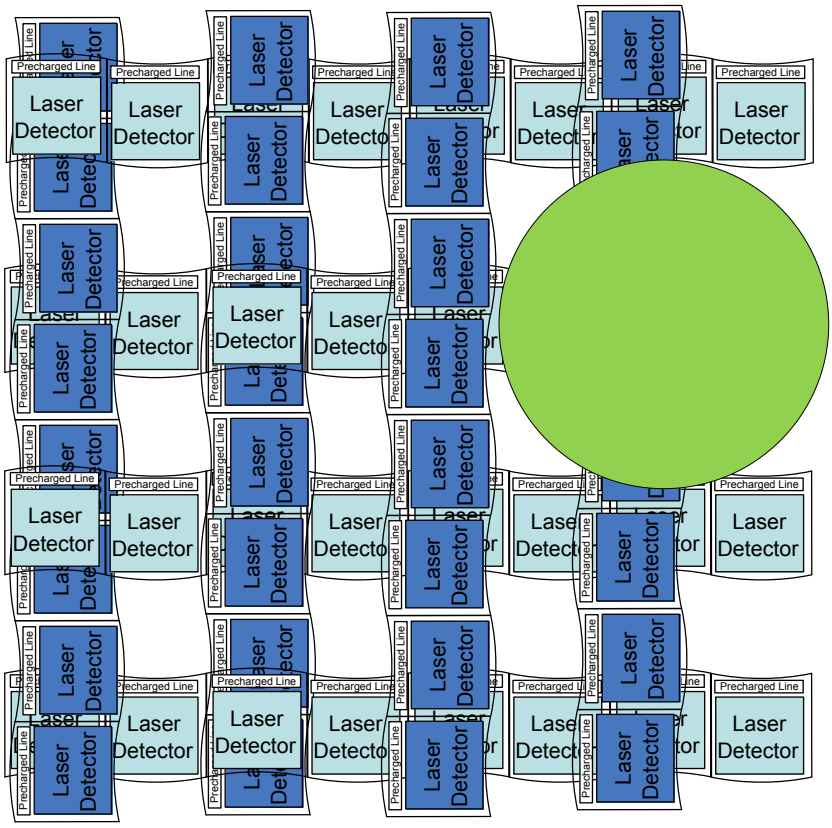

Figure 65. Demonstration of spot illumination

CONCLUSION

Amorphous silicon technology has been used for imaging and display operations for decades however building on flexible substrates for ruggedness, thinness, and flexibility has recently caught the attention over the last decade. Experience in successful manufacturing of thin film transistors on these substrates, and cheap manufacturing opportunity led to seeking more fields of research and products.

The first flexible CMOS TFT by combining both organic and inorganic materials in two different fabs was designed, manufactured, tested and characterized. Basic logic gates using this new technique were demonstrated and the results – which showed dramatic decrease in power consumption as expected- were published in conferences and journals.

As the development for alternative materials to amorphous silicon were gaining traction, TFTs manufactured with variation of metal oxides were tested under the same conditions as the amorphous silicon counterparts, characterized and were compared for stability. A paper was published based on the results of this study.

Electronic textile is a novel product that was designed to be significantly different than the previously shown concepts under the same name. It is the first example of an electronic textile that is not

using the existing fabrics to mount commercial components but actually is created weaving a flexible substrate that accommodates functioning circuits that are manufactured on the substrate in the fab and are not just mounted on commercial products. It is also the first design of its kind to be able to give a 2 dimensional address without having a two dimensional matrix connection. This was achieved by a unique technique that pushes the data to a line (precharging) and reading (pulling) it from the same line and comparing it to a given state. This is a significantly different approach than the current active matrix approach used in large area sensors. This product, which is ready for mass manufacturing can cover an area of roughly 45 cm x 45cm which is an unforeseen size for a single gadget. Unlike the current flexible large area sensors, the weaving of strips also enable the patch to conform any shapes needed. The laser detection circuits implemented on these strips that make the textile are for demonstration of the data push pull architecture. This architecture can be used in various forms of sensors. The individual strips can be weaved at any density as long as the pitch of the sensor strips smaller than the object –or in this case the laser beam- to be detected. The analogy is the same as using different density of fish net for different size of fish to be caught. A journal paper and a patent filing is currently in process for this project.

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