Scalable Surface-Potential-Based Compact Model of High-Voltage LDMOS Transistors

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved May 2012 by the
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May 2012

ABSTRACT

Lateral Double-diffused (LDMOS) transistors are commonly used in power management, high voltage/current, and RF circuits. Their characteristics include high breakdown voltage, low on-resistance, and compatibility with standard CMOS and BiCMOS manufacturing processes. As with other semiconductor devices, an accurate and physical compact model is critical for LDMOS-based circuit design.

The goal of this research work is to advance the state-of-the-art by developing a physics-based scalable compact model of LDMOS transistors. The new model, SP-HV, is constructed from a surface-potential-based bulk MOSFET model, PSP, and a nonlinear resistor model, R3. The use of independently verified and mature submodels leads to increased accuracy and robustness of an overall LDMOS model. Improved geometry scaling and simplified statistical modeling are other useful and practical consequences of the approach. Extensions are made to both PSP and R3 for improved modeling of LDMOS devices, and one internal node is introduced to connect the two component models.

The presence of the lightly-doped drift region in LDMOS transistors causes some characteristic device effects which are usually not observed in conventional MOSFETs. These include quasi-saturation, a sharp peak in transconductance at low V_{D}, gate capacitance exceeding oxide capacitance at positive V_{D}, negative transcapacitances C_{BG} and C_{GB} at positive V_{D}, a "double-hump" $I_{\mathrm{B}}(V_{\mathrm{G}})$ current, and expansion effects. SP-HV models these effects accurately; it also includes a scalable self-heating model which is important to model the geometry dependence of the expansion effect.

SP-HV, including its scalability, is verified extensively by comparison both to TCAD simulations and experimental data. The close agreement confirms the validity of the model structure. Circuit simulation examples are presented to demonstrate its convergence and robustness.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my Ph.D. advisor, Professor Gennady Gildenblat, for his guidance, encouragement, and financial support throughout my study and research at Arizona State University. I appreciate all his contributions of time, ideas, and efforts to make my Ph.D. experience productive.

I am indebted to Dr. Colin C. McAndrew for his continuous support and guidance. This dissertation would not have been possible without his efforts. His expertise, insights, enthusiasm, and commitment to research always inspire and motivate me. It is an honor and pleasure to work with him.

I would like to thank Alexandra Cassagnes, John Bates, and Margaret Kniffin from Freescale Semiconductor for providing all the experimental data for model validation and some of the circuit simulation examples in this dissertation, for illuminating discussions on device physics and compact modeling of LDMOS transistors, and for continuous collaboration during every step of the model development.

I also want to thank Dr. Weimin Wu and Dr. Yong Liu from Texas Instruments for their efforts at the beginning of this research task.

I would like to thank all my fellow graduate students in our research group, Dr. Xin Li, Dr. Zeqin Zhu, and Gajanan Dessai for their friendship. It was a great experience working together with these guys. I really appreciate their company during the past years.

I am thankful to the committee members, Professor Hugh Barnaby, Professor Yu Cao, and Dr. Colin C. McAndrew for their suggestions to this work and reading this dissertation.

This work was partly funded by the Semiconductor Research Corporation.

To my lovely wife for her never ending love, support, and encouragement

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CHAPTER 1

INTRODUCTION

Lateral Double-diffused MOS (LDMOS) transistors are commonly used in power management applications, high voltage/high current, and RF integrated circuits. Their characteristics include high breakdown voltage, low on-resistance, and compatibility with standard CMOS and BiCMOS manufacturing processes [1–6]. As with other semiconductor devices, an accurate and physical compact model is important for LDMOS-based circuit design. [5, 7–9]

LDMOS transistors show the electrical behaviors observed in conventional MOSFETs such as bias-dependent mobility and velocity saturation. In addition, they exhibit some device characteristics, not usually observed in conventional MOSFETs, that should be taken into account in a compact model of LDMOS transistors. These physical effects include:

- Quasi-saturation
- Complex transcapacitances
- Impact ionization in the drift region
- Self-heating
- The so-called expansion effect

There are presently several techniques for compact modeling of LDMOS transistors [8, 9]. The most popular is the sub-circuit based approach.

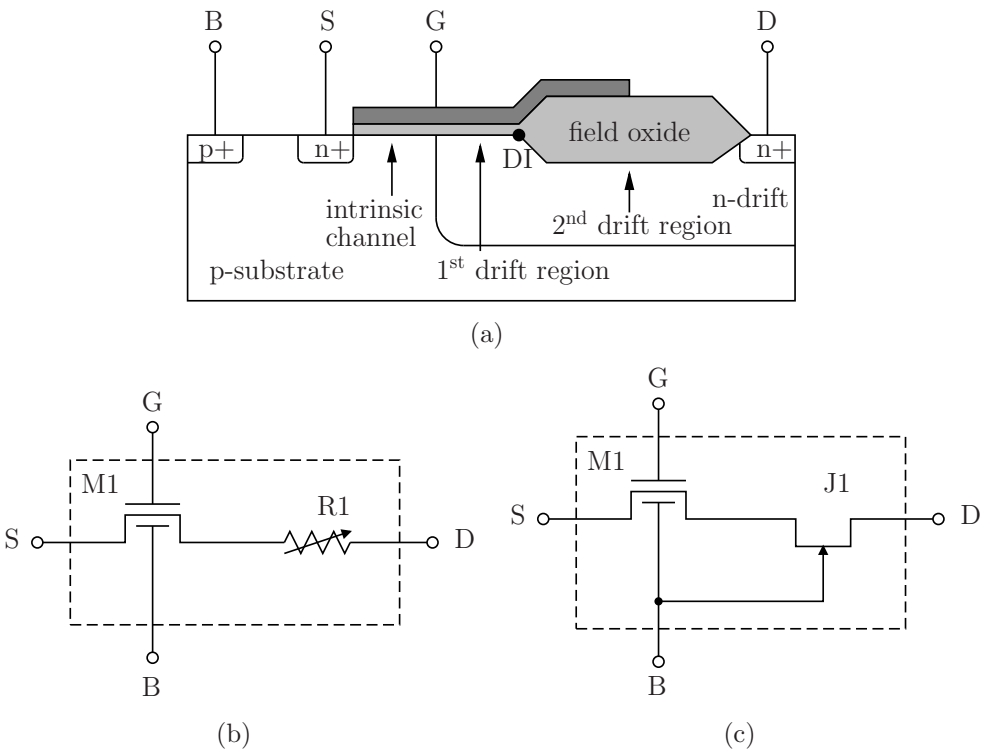


Figure 1.1: Sub-circuit-based approaches for modeling LDMOS transistors.

1.1 Modeling LDMOS Transistors with Sub-circuits

In a sub-circuit-based approach, an LDMOS transistor is represented by a network composed of active and passive components [8, 10–33]. There is a well-defined node interface between the sub-circuit and the external circuit, where the sub-circuit appears as a single effective device. The components in the sub-circuit are selected and connected such that the LDMOS characteristics are reproduced as accurately as possible. Furthermore, the sub-circuit-based approach allows high flexibility. A sub-circuit can be easily adapted by adding more elements to the network or removing elements from it. Another advantage in a sub-circuit-based model is its transportability across many circuit simulators. The most popular approach is to combine a compact model of the intrinsic MOSFET region of the device with a resistor

[cf. Fig. 1.1(b)] [8,10,11,23,24,27,32] or JFET [cf. Fig. 1.1(c)] [8,14,16,17,26], for the drift region. Inductors and capacitors are sometimes introduced to improve the RF behavior modeling [8, 10–14, 16, 24, 25, 29].

The major disadvantage of the sub-circuit-based approach is an inability to change or intertwine bias dependencies of the elements, which leads to model inaccuracy. In addition, the simulation time is increased due to a large effective number of circuit nodes and elements. The sub-circuit-based approach also has limited capability to model self-heating and the impact ionization current in the drift region.

Some compact models have been developed to overcome the deficiencies of the sub-circuit-based models. State-of-the-art LDMOS compact models include HV-EKV, MM20, and HiSIM_HV.

1.2 HV-EKV

The HV-EKV model has been developed by the Swiss Federal Institute of Technology (EPFL) [9, 34–45]. It uses the inversion-charge-based EKV MOSFET model [46–48] for the intrinsic MOSFET while the drift region is modeled with a bias dependent resistance [40, 45].

The HV-EKV model employs a single substrate current component [40], which is insufficient because the impact ionization process may primarily take place in either the intrinsic MOSFET or the drift region depending on the bias conditions [49–51]. As a result, HV-EKV fails to reproduce LDMOS characteristics such as the double-hump $I_{\mathrm{B}}(V_{\mathrm{G}})$ as well as the expansion effect.

1.3 MM20

MOS Model 20 (MM20) is an asymmetric, surface-potential-based LDMOS model. It is developed by NXP Research (formerly Philips Research) Laboratories [53–56]. It combines the surface-potential-based MOSFET model MM11 [57, 58] with a physical model of the first drift region which is the drift region under the thin gate oxide [cf. Fig. 1.1(a)]. To increases the model flexibility the second drift region under the field oxide is not directly included but is accounted for using a separate element in a sub-circuit. The component for the second drift region may be a constant resistance [56] or a MOSFET in accumulation mode [59, 60]. MM20 does not model the length scalability of the intrinsic MOS or drift regions, or the expansion effect.

1.4 HiSIM_HV

The HiSIM_HV model has been developed by the Hiroshima University modeling research group [61–64]. It uses the surface-potential-based HiSIM2 (Hiroshima University STARC IGFET Model) to describe the intrinsic MOSFET [65, 66]. A semi-empirical scalable description is used to model the drift region [67, 68].

HiSIM_HV has some critical deficiencies. The major shortcoming is its semi-empirical description of the drift region, in which a singular velocity saturation model is used. Velocity saturation in [68] is modeled by

$$v = \frac{\mu E}{1 + \frac{\mu |E|}{v_{sat}}} \tag{1.1}$$

where μ is an effective mobility, v_{sat} is the saturation velocity, and E is the lateral field. Although v in (1.1) is symmetric with respect to the zero field point and is continuous for all field, its derivative at $E = 0$ does not exist

because $|E|$ is not smooth around $E = 0$ [69]. It is also known that the velocity saturation model (1.1) inaccurately describes experimental data for diffused resistors and hence for the LDMOS drift region [70, 71].

In addition, the scaling trend of the drift region resistance in [67, 68] is incorrect. In particular, in [67,68] the drift region resistance reduces when the length of the first drift region increases which is apparently unphysical. The problem can be traced to the oversimplified spatial current density pattern used in [67, 68] in which the width x_{ov} of the current tube in the first drift region is used as the width of the second drift region to evaluate its resistance.

Besides, HiSIM_HV models the expansion effect by body-biasing [72], which is unphysical and will be discussed in detail in Chapter 6.

1.5 SP-HV

An alternative approach for LDMOS modeling is needed to overcome the deficiencies of sub-circuit-based models and the existing compact models. This is the objective of the development of SP-HV (Surface-Potential-based High-Voltage MOS) model [51, 52].

This work presents a surface-potential-based model for LDMOS transistors. We take advantage of a physics-based compact model of diffused resistors, R3 [70,71,73]. This model has been extensively verified for both accuracy and convergence, and consequently serves as a natural candidate to describe the second drift region of an LDMOS transistor. In particular, the SP-HV model inherits from R3 a specific velocity saturation model which has been experimentally demonstrated to increase the accuracy of diffused resistor modeling [70, 71] and so is relevant to the drift region model. Its other advantage is the resulting modular structure of the LDMOS model which simplifies both

coding of the model and parameter extraction.

The SP-HV model relies on the PSP surface-potential-based model [74, 75] to describe the intrinsic MOS portion (without the drift region) of an LDMOS transistor. The first drift region is described using an independent physics-based approach and the second drift region is modeled with R3, as explained above. As in other compact models such as HV-EKV, MM20, and HiSIM_HV [9, 34–45, 53–56, 61–64] only one internal node is needed in this formulation. The use of independently verified and mature submodels leads to increased accuracy and robustness of an overall LDMOS model. Improved geometry scaling and simplified statistical modeling are other useful and practical consequences of the approach.

This dissertation is organized as follows:

In Chapter 2, the modeling approach of this work is introduced. The SP-HV model is constructed from a surface-potential-based bulk MOSFET model, PSP, and a non-linear resistor model, R3. Extensions are made to both PSP and R3 for improved modeling of LDMOS transistors, and one internal node is introduced to connect the two component models. The accuracy is verified with both TCAD simulation and experimental data with fixed device geometry. Quasi-saturation, self-heating, the impact ionization current in the drift region, and the complex behavior of transcapacitances are accurately modeled by SP-HV.

In Chapter 3, the model scalability is extensively verified. We depend on TCAD simulations to verify the scaling of the drift region, including the length of the drift region and the doping concentration in the drift region, because these process parameters are almost always fixed in the manufactured devices. Experimental data are used for intrinsic MOSFET scaling verification.

The generalized Berglund relation in LDMOS transistors is derived and validated in Chapter 4. It is applied as a benchmarking test for both measurements and compact models.

In Chapter 5, the scalable self-heating model in SP-HV is introduced. Its interaction with the impact ionization is important to capture the width dependence of the expansion effect.

In Chapter 6, the impact ionization current in the drift region is modeled. The "double-hump" $I_{\mathrm{B}}(V_{\mathrm{G}})$ characteristics and the expansion effect are accurately reproduced. The interaction between the self-heating effect and impact ionization is well modeled. This interaction explains the width dependence of the expansion effect observed in experimental data.

In Chapter 7, circuit simulation examples are presented to verify model convergence.

The last chapter summarizes the major research results.

CHAPTER 2

MODELING APPROACH USED IN SP-HV

Fig. 2.1 shows a cross-section of a typical LDMOS transistor, and the equivalent circuit used in SP-HV is shown in Fig. 2.2. An essential feature of LDMOS devices is the presence of the lightly doped n-type drift region, which is introduced to increase the breakdown voltage. It is convenient to separate the drift region into two parts: a first drift region, under the thin gate oxide; and a second drift region, under the field oxide. The internal node (DI) is placed at the boundary between these two drift regions; the transistor M_n shown in Fig. 2.2 therefore represents both the intrinsic device and the first drift region. The validity of using a single internal node is justified by comparison of the model to TCAD simulations and experimental data. The polysilicon gate is often extended over field oxide to leverage the RESURF (REduced SURface Field) effect [76]. Hence the resistance of the second drift region is weakly affected by the gate bias. In addition this resistance depends on the body bias, which modulates the thickness of the depletion region around the n-drift/p-substrate junction. The bias dependence of the resistance of the first drift region is also modeled [see (2.1), (2.2)].

Also included in Fig. 2.2 is the current source I_{bdr} which describes the impact ionization in the second drift region and is essential to model the experimental data presented in Section 2.4. The current source I_{bn} describing the impact ionization under the thin gate oxide is included in the compact model of the transistor M_n. Physically, the use of two current sources is justified by the fact that impact ionization is mostly localized in two places [49, 50]. Even more detailed description of the impact ionization is necessary to describe the

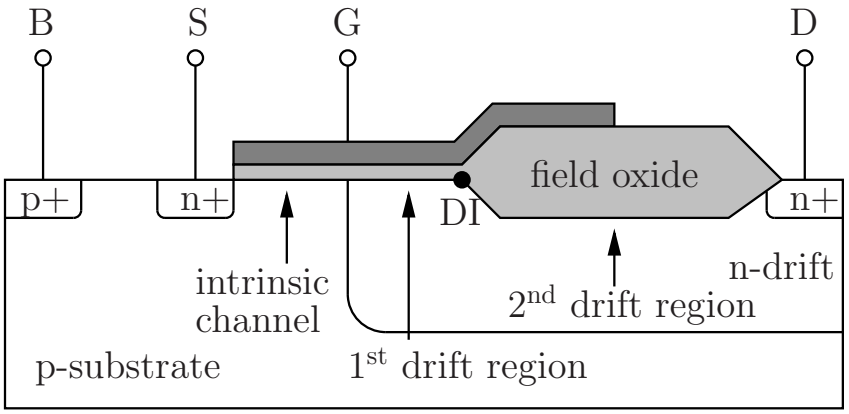


Figure 2.1: Cross-section of a typical LDMOS transistor.

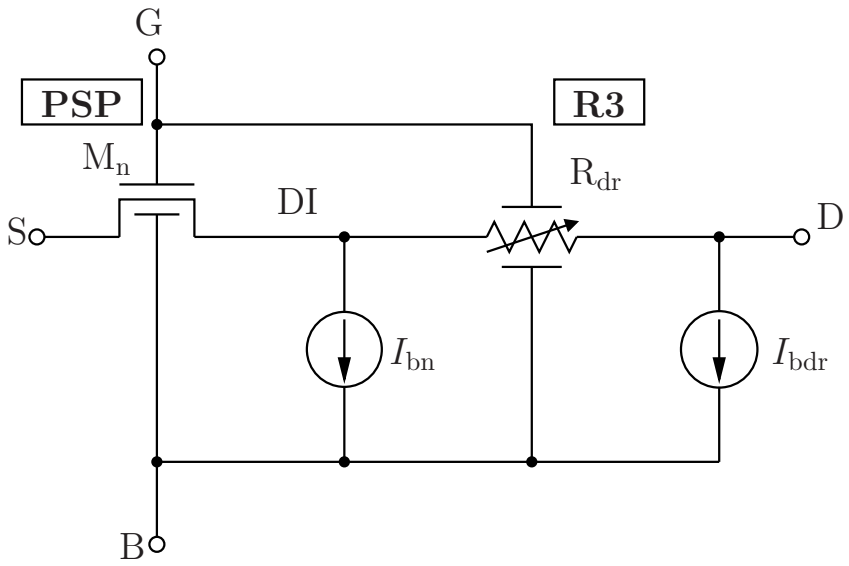


Figure 2.2: Equivalent circuit of SP-HV.

so-called "expansion effect" in LDMOS transistors [77,78]. These subjects will be discussed in detail in Chapter 6.

2.1 Basic Building Blocks of SP-HV

There are two main building blocks of SP-HV: PSP for the intrinsic MOSFET and the first drift region; R3 for the second drift region resistance.

Overview of PSP

PSP is a surface-potential-based bulk MOSFET compact model [74, 75]. It is physical in both the intrinsic channel region and the gate-to-source/drain overlap regions. Some of the physical effects in PSP include mobility reduction by the vertical electric field, velocity saturation, drain-induced barrier lowering, gate tunneling current, quantum effects, and poly-silicon depletion. PSP is scalable so the intrinsic channel region of SP-HV is scalable as well. In SP-HV, the charge model for the gate-to-drain overlap region is modified to model the charges in the first drift region. There are a separate submodel and parameters for the gate-to-source overlap region.

Overview of R3

R3 is a nonlinear three-terminal compact model for diffused and poly-silicon resistors and JFETs [70,71,73]. It has an accurate depletion pinching formulation and an empirical velocity saturation model. Indeed, the accurate velocity saturation model of R3 is critical for modeling quasi-saturation in LDMOS transistors. R3 is fully scalable, which enables us to model the geometry dependence of the second drift region in an LDMOS transistor.

2.2 Extensions to PSP and R3 Included in SP-HV

The internal node DI is used to connect PSP and R3. Extensions are made to both of them for improved modeling of LDMOS transistors.

Current Model

In SP-HV, the second drift region is described by R3 and the resistance of the first drift region is modeled by the series resistance in PSP. The effect of the series resistance of the first drift region on current is included in the model by modifying the effective mobility, given by the expression [75]

$$\mu_{\rm eff} = \frac{\mathbf{U_O} \cdot \mu_{\rm x}}{1 + (\boldsymbol{\mu_E} \cdot E_{\rm eff})^{\boldsymbol{\theta_\mu}} + \mathbf{C_S}\left(\frac{q_{\rm bm}}{q_{\rm im}+q_{\rm bm}}\right)^2 + G_{\rm R}} \tag{2.1}$$

in which $G_{\rm R}$ accounts for the resistance of the first drift region. In (2.1) $\mathbf{U_O}$ is the low-field mobility, and the parameters $\boldsymbol{\mu_E}$ and $\boldsymbol{\theta_\mu}$ account for the mobility degradation caused by the surface roughness and phonon scattering at the effective field $E_{\rm eff} = (q_{\rm bm} + \eta \cdot q_{\rm im})/\epsilon_{\rm Si}$ with $\eta = 1/2$ for electrons [79] and $\eta = 1/3$ for holes [80]. The parameter $\mathbf{C_S}$ accounts for Coulomb scattering [81], and $q_{\rm im}$ and $q_{\rm bm}$ are the (normalized magnitudes of the) inversion charge and bulk charge at the surface-potential midpoint of $\rm M_n$. The factor $\mu_{\rm x}$ describes mobility nonuniversality effects. The bias dependence of $G_{\rm R}$ is given by the expression

$$G_{\rm R} = \mathbf{U_O} \cdot \frac{W}{L} \cdot q_{\rm im} \cdot \mathbf{R_S} \cdot \frac{1 + \mathbf{R_{SB}} \cdot V_{\rm SB}}{1 + \mathbf{R_{SG}} \cdot q_{\rm im}}\,, \tag{2.2}$$

where $\mathbf{R_S}$, $\mathbf{R_{SG}}$ and $\mathbf{R_{SB}}$ are model parameters. The bias dependence of $G_{\rm R}$ is inherited from PSP. The channel current in SP-HV is then formulated as

$$I_{\rm ch} = \mu_{\rm eff} \cdot \frac{W}{L} \cdot q_{\rm im} \Delta\psi \tag{2.3}$$

where $\Delta\psi = \psi_{\rm sdi} - \psi_{\rm ss}$ is the surface-potential variation across the channel of $\rm M_n$ and $\psi_{\rm ss}$ and $\psi_{\rm sdi}$ are the surface-potentials at the source and internal drain, respectively. While the mobility model (2.1) is essentially the same as in PSP, the physical meaning of $G_{\rm R}$ is different in SP-HV. In PSP $G_{\rm R}$ refers to the access resistances at the ends of the channel (including from lightly-doped

drain and source/drain extension regions) while in SP-HV it also accounts for the first drift region (cf. Fig. 2.1).

An "Early voltage parameter" $\mathbf{V_A}$ is added to R3 to model the effect of $V_{\mathrm{D,DI}}$, the voltage drop across the second drift region, on the resistance of this region. Also a V_{G}-modulation parameter $\boldsymbol{\theta_{ACC}}$ is added to R3 to model the effect of the gate voltage over the thick field oxide on the conductance of the second drift region. Physically, as V_{G} increases so does the carrier concentration in the second drift region, making its conductivity dependent on V_{G}. With these modifications, the current in the second drift region is given by

$$I_{\mathrm{dr}} = I_{\mathrm{dr0}} \cdot \left(1 + \frac{V_{\mathrm{D,DI}}}{\mathbf{V_A}}\right) \cdot (1 + \boldsymbol{\theta_{ACC}} \cdot V_{\mathrm{GS}}) \tag{2.4}$$

where I_{dr0} is the current predicted by the R3 model without considering the effects of the $V_{\mathrm{D,DI}}$ and V_{GS} modulation. $V_{\mathrm{D,DI}}$ is determined during circuit simulations from current continuity. The V_{BS} dependence of I_{dr} is included through I_{dr0} and $V_{\mathrm{D,DI}}$.

Charge Model

The G_{R} term in (2.1) accounts for the series resistance of the first drift region but not for the contributions of charges in that region. These can be modeled physically using the overlap capacitance submodel in SP [82] or PSP [75], which is based on a surface-potential formulation. There is, however, an essential difference. In the bulk MOSFET structure considered in [75, 82] the contribution of minority carriers to the overlap region charge can be neglected. In LDMOS devices, for sufficiently negative gate bias the surface of the first drift region may become inverted because this region is lightly doped, hence minority carriers (holes) must be included for this region. The corresponding

equation for the surface-potential [82] therefore takes the same form as for the intrinsic MOS region, with the polarity changed:

$$\left(V_{\mathrm{G,DI}} - V_{\mathrm{FBov}} - \psi_{\mathrm{sov}}\right)^2 / (\gamma_{\mathrm{ov}}^2 \phi_{\mathrm{T}}) = e^{-x} + x - 1 + e^{-\frac{2\phi_{\mathrm{Bov}} + V_{\mathrm{B,DI}}}{\phi_{\mathrm{T}}}} \left[e^{x} - x - 1 - \chi(x)\right] . \tag{2.5}$$

Here ψ_{sov} is the surface potential at the internal node DI. For the sake of simplicity we neglect the lateral variation of surface potential in the first drift region (the justification being the reasonable agreement with TCAD simulations and experimental data presented in Section 2.3 and 2.4). In (2.5)

$$\gamma_{\mathrm{ov}} = \frac{\sqrt{2 \cdot q \cdot \epsilon_{\mathrm{Si}} \cdot N_{\mathrm{drift}}}}{C_{\mathrm{oxov}}} \tag{2.6}$$

is the body factor, N_{drift} is the n-type doping concentration in the first drift region, C_{oxov} is the oxide capacitance per unit area, $\phi_{\mathrm{T}} = k_{\mathrm{B}}T/q$ is the thermal voltage, $x = \psi_{\mathrm{sov}}/\phi_{\mathrm{T}}$, $\phi_{\mathrm{Bov}} = \phi_{\mathrm{T}} \ln(N_{\mathrm{drift}}/n_i)$, and n_i is the intrinsic carrier concentration. The term

$$\chi(x) = \frac{x^2}{x^2 + 2} \tag{2.7}$$

is introduced to correct the problem inherent in the traditional form of the surface potential equation near the flat-band region [75,83,84]. This modification does not affect modeling of the device characteristics.

The contributions of the first drift region to the integrated gate, inversion and body charges are then given by

$$Q_{\mathrm{GOV}} = C_{\mathrm{oxov}} W L_{\mathrm{dr1}} \left(V_{\mathrm{G,DI}} - V_{\mathrm{FBov}} - \psi_{\mathrm{sov}}\right) , \tag{2.8}$$

$$Q_{\mathrm{IOV}} = \frac{C_{\mathrm{oxov}} W L_{\mathrm{dr1}} \phi_{\mathrm{T}} G^2 D}{u_{\mathrm{oxov}} + G\sqrt{e^{-x} + x - 1}} , \tag{2.9}$$

and

$$Q_{\mathrm{BOV}} = Q_{\mathrm{GOV}} - Q_{\mathrm{IOV}} . \tag{2.10}$$

Here

$$G = \gamma_{\rm ov} \Big/ \sqrt{\phi_{\rm T}}\,, \tag{2.11}$$

$$D = \exp\left(-\frac{2\phi_{\rm Bov} + V_{\rm B,DI}}{\phi_{\rm T}}\right)\left[e^{x} - x - 1 - \chi(x)\right]\,, \tag{2.12}$$

and

$$u_{\rm oxov} = (V_{\rm G,DI} - V_{\rm FBov} - \psi_{\rm sov})/\phi_{\rm T}\,. \tag{2.13}$$

The partitioning of electrons is a difficult problem. Generally speaking, for laterally non-uniformly doped devices the Ward-Dutton partitioning [85] cannot be done rigorously [43, 86–90]. But as a practical matter, all modern compact models are charge-based so one needs to come up with some partition scheme. In SP-HV, the inversion charge (holes) in the first drift region is attributed to the body terminal, while all accumulation charge (electrons) is attributed to the intrinsic drain node. The expressions for the total terminal charges become

$$Q_{\rm G} = Q_{\rm G}^{\rm (i)} + Q_{\rm GOV} + Q_{\rm sov} + Q_{\rm ofs} + Q_{\rm ofd} + Q_{\rm subov}\,, \tag{2.14}$$

$$Q_{\rm S} = Q_{\rm S}^{\rm (i)} - Q_{\rm sov} - Q_{\rm ofs}\,, \tag{2.15}$$

$$Q_{\rm D} = Q_{\rm D}^{\rm (i)} - Q_{\rm BOV} - Q_{\rm ofd}\,, \tag{2.16}$$

$$Q_{\rm B} = Q_{\rm B}^{\rm (i)} - Q_{\rm IOV} - Q_{\rm subov}\,. \tag{2.17}$$

Here the symbols with superscripts (i) are the terminal charges of the intrinsic MOSFET, $Q_{\rm sov}$ and $Q_{\rm subov}$ are the charges induced by gate-to-source and gate-to-substrate overlap capacitances, respectively, and $Q_{\rm ofs}$ and $Q_{\rm ofd}$ are the charges induced by the outer fringing capacitance on source and drain.

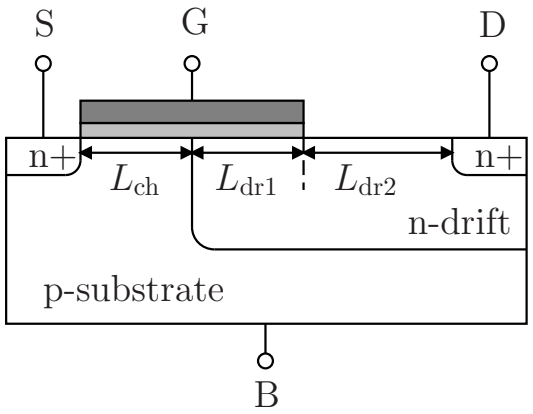


Figure 2.3: Device structure used in TCAD simulation. $T_{ox} = T_{oxov} = 30$ nm, $L_{ch} = 2$ μm, $L_{dr1} = 2$ μm, $L_{dr2} = 5$ μm, $N_{ch} = 5 \times 10^{16}$ cm^{-3}, $N_{drift} = 5 \times 10^{16}$ cm^{-3}.

2.3 Local Model Verification with TCAD Simulations

Prior to fitting experimental data the SP-HV model was extensively verified by comparison to TCAD simulations. Some simplifications were made to the device structure of Fig. 2.1 for TCAD simulations, as shown in Fig. 2.3: there is no gate over the thick field oxide; a separate body terminal is added so the body effect for both the intrinsic MOSFET and the n-type drift region can be investigated. The additional terminal is also useful for the study of transcapacitances (C_{GB}, C_{BG} etc.). For simplicity, both the p-type substrate region and the n-type drift region are uniformly doped. Model comparison with more complex device structures is performed in Section 2.4 using experimental data. $V_{Gmax} = 12$ V and $V_{Dmax} = 20$ V are used for TCAD simulations. In this section self-heating and impact ionization are not included to make the comparison more direct. These effects are briefly discussed in Section 2.4 and discussed in detail in Chapters 5 and 6.

Figs. 2.4 through 2.6 show the transfer characteristics at different body biases. The drain current is modeled accurately on both linear and semi-

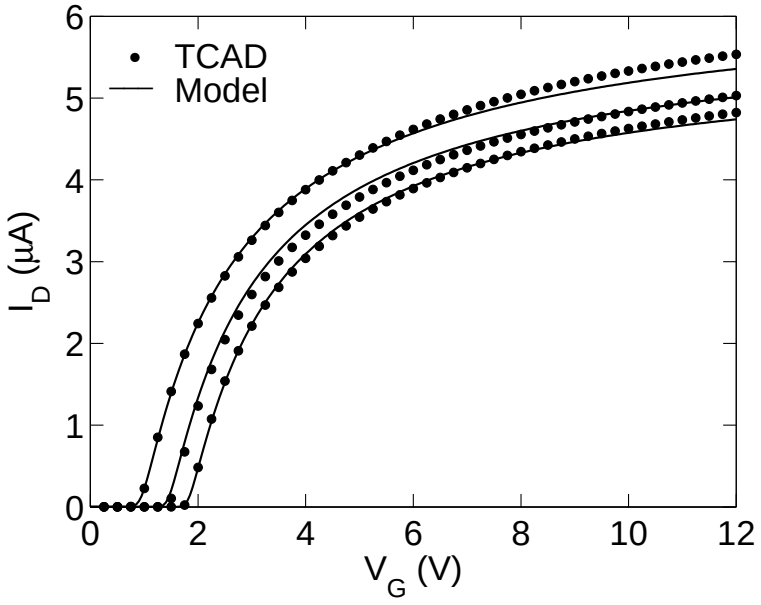


Figure 2.4: TCAD verification of the transfer characteristics. Drain current as a function of the gate bias at different body biases on a linear scale. $V_{\mathrm{D}} = 100$ mV, $V_{\mathrm{B}} = 0, -1, -2$ V.

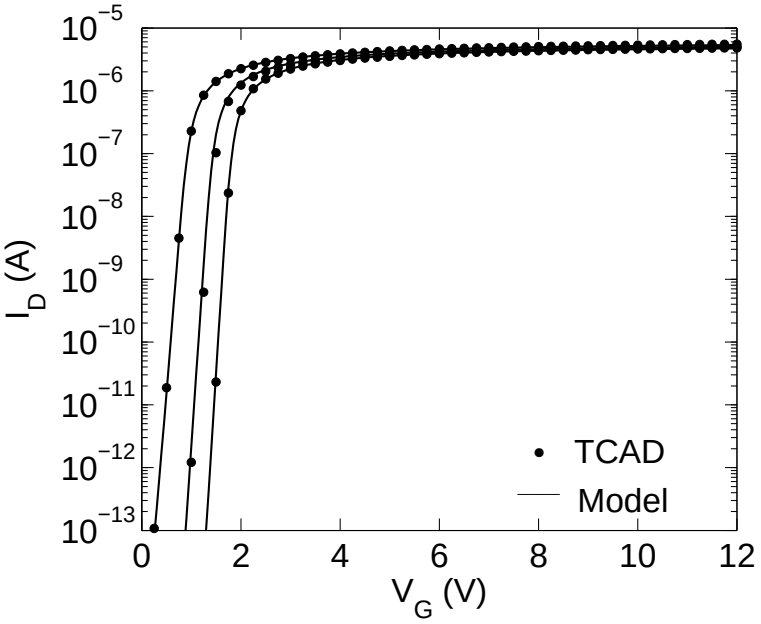


Figure 2.5: TCAD verification of the transfer characteristics. Drain current as a function of the gate bias at different body biases on a semi-logarithmic scale. $V_{\mathrm{D}} = 100$ mV, $V_{\mathrm{B}} = 0, -1, -2$ V.

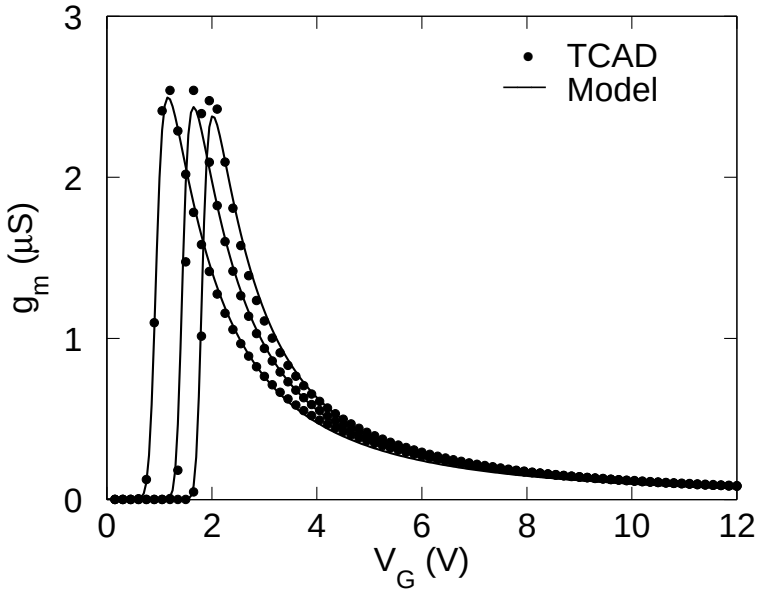


Figure 2.6: TCAD verification of the transfer characteristics. Transconductance as a function of the gate bias at different bulk biases. $V_{\mathrm{D}} = 100$ mV, $V_{\mathrm{B}} = 0, -1, -2$ V.

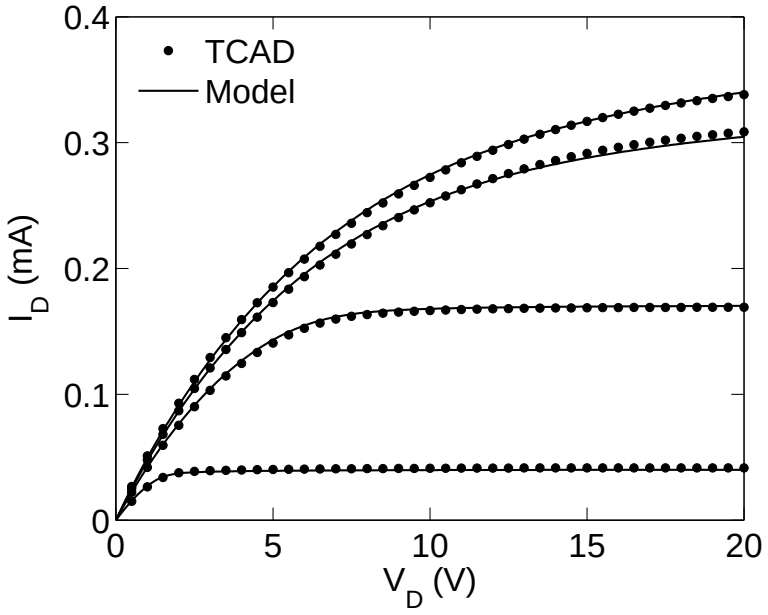


Figure 2.7: TCAD verification of the output characteristics. Drain current as a function of the drain voltage at different gate biases. $V_{\mathrm{B}} = 0$, $V_{\mathrm{G}} = 3, 6, 9, 12$ V.

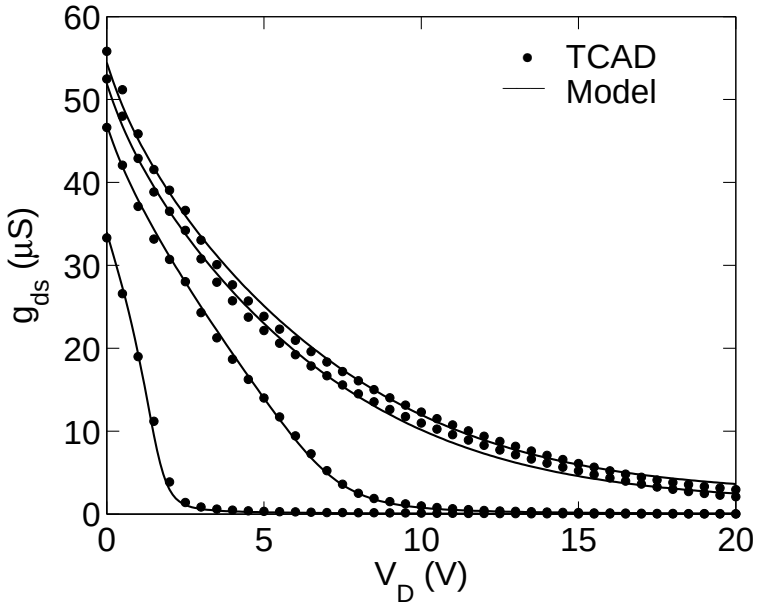


Figure 2.8: TCAD verification of the output characteristics. Output conductance as a function of the drain voltage at different gate biases on a linear scale. $V_{\mathrm{B}} = 0$, $V_{\mathrm{G}} = 3, 6, 9, 12$ V.

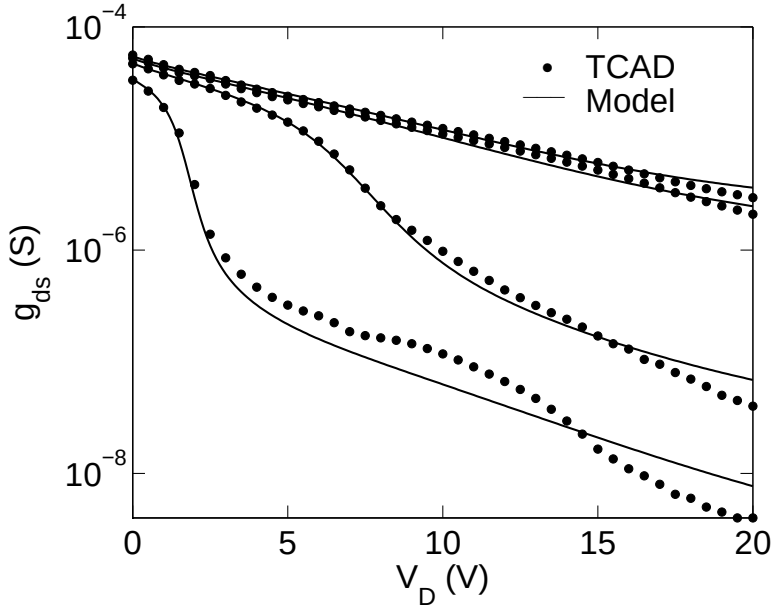


Figure 2.9: TCAD verification of the output characteristics. Output conductance as a function of the drain voltage at different gate biases on a semilogarithmic scale. $V_{\mathrm{B}} = 0$, $V_{\mathrm{G}} = 3, 6, 9, 12$ V.

logarithmic scales. The transconductance dependence on gate bias is also well reproduced by the model, including the sharp peaks in G_{m}, which are characteristic of LDMOS transistors [38, 61, 91].

Figs. 2.7 through 2.9 show output characteristics for different gate biases. In the $I_{\mathrm{D}}(V_{\mathrm{D}})$ curves, the quasi-saturation effect is clearly visible at high V_{G} [15, 18, 56, 61, 91–98]. Physically, quasi-saturation is caused by the reduction of the intrinsic MOSFET channel resistance for high V_{G} when the overall device resistance is dominated by the drift region. This brings about the reduced gate bias dependence of the drain current at high V_{G} shown in Fig. 2.7. The SP-HV model captures this behavior automatically without any need for additional model parameters beyond those included in PSP and R3. In particular, velocity saturation in the drift region [99], which is important for accurate modeling of the quasi-saturation effect, is already included in R3 [70, 71]. Figs. 2.8 and 2.9 show SP-HV fits to output conductance on linear and semi-logarithmic scales, respectively.

One difficulty encountered in subcircuit models for LDMOS devices is poor fitting of capacitances [12, 19, 28, 33, 100–108]. Fig. 2.10 shows the gate capacitance as a function of V_{G} for different drain voltages. The shape of the capacitance curves is complex: there are peaks in the positive gate voltage range for $V_{\mathrm{D}} > 0$; also the curves for different V_{D} differ for negative gate voltages, whereas they coincide for bulk MOSFETs. The peaks in capacitance for positive gate voltage are caused by the large resistance of the second drift region. The drain bias dependence for negative gate voltages is caused by inversion of the first drift region. Therefore, accurate modeling of LDMOS capacitances requires accurate modeling both of drift region resistance and of inversion charge in the first drift region.

As Figs. 2.10 and 2.11 show, the charge model (2.8) through (2.17) rep-

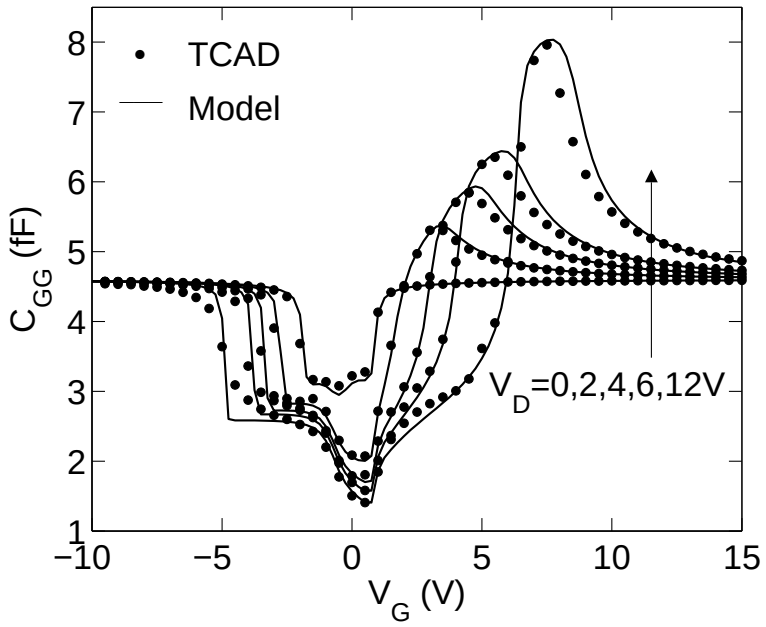


Figure 2.10: TCAD verification of gate capacitance. $V_{\rm D} = 0, 2, 4, 6, 12$ V.

resents the gate and drain bias dependencies of the gate capacitance $C_{\rm GG}$ and various transcapacitances reasonably well. The transcapacitances are not always available experimentally, making TCAD simulations particularly valuable for charge model verification. Some of the relevant details modeled in Figs. 2.10 and 2.11 include the shift in the position and the change of the magnitude of the peaks of $C_{\rm GG}$, $C_{\rm DG}$, and $C_{\rm GD}$ over bias.

One of our model predictions confirmed by TCAD simulation in Fig. 2.11 is negative $C_{\rm GB}$ and $C_{\rm BG}$ for positive $V_{\rm G}$ when $V_{\rm D}$ is positive. To trace the cause of these negative transcapacitances, the p-substrate/n-drift region junction must be taken into account. Consider the change of $Q_{\rm B}$ with $V_{\rm G}$ when $V_{\rm D} > 0$. As $V_{\rm G}$ increases, $V_{\rm DI}$ (cf. Fig. 2.1) decreases, because the resistance of the intrinsic MOSFET goes down. The decrease of $V_{\rm DI}$ reduces the reverse bias on the substrate-to-drift region junction, which in turn increases $Q_{\rm B}$, resulting in a negative $C_{\rm BG}$.

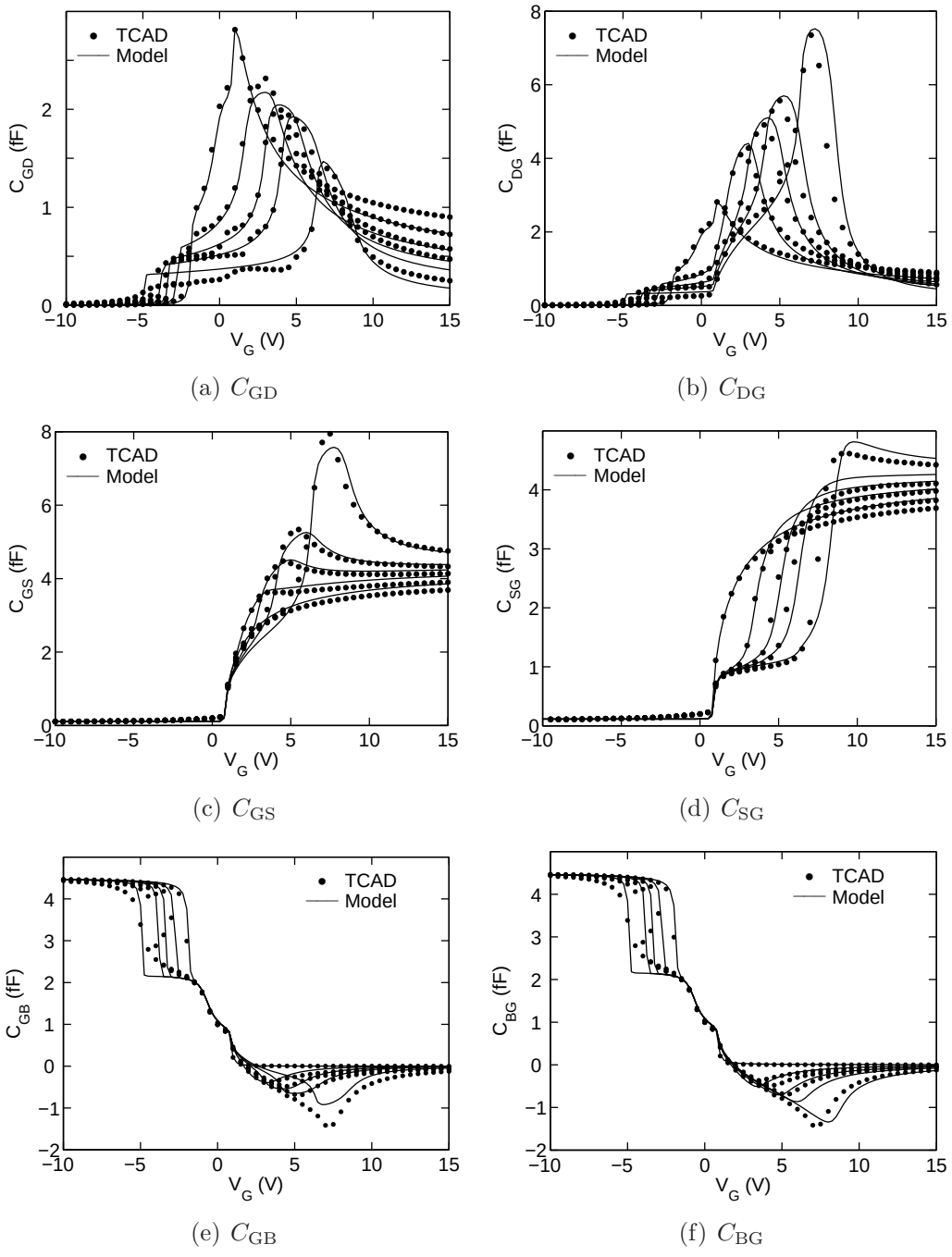


Figure 2.11: TCAD verification of other transcapacitances. $V_{\mathrm{D}} = 0$, 2, 4, 6, 12 V.

Another interesting effect, captured by the SP-HV charge model, is that $C_{\mathrm{GD}} \neq C_{\mathrm{GS}}$ even for $V_{\mathrm{DS}} = 0$. Physically, this is caused by the lateral asymmetry of the LDMOS transistor. In symmetric bulk MOSFETs $C_{\mathrm{GD}} = C_{\mathrm{GS}}$

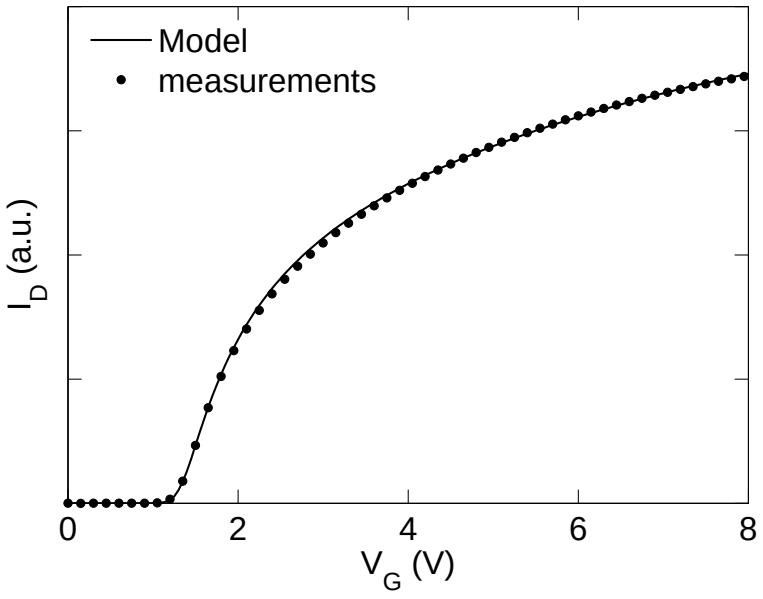


Figure 2.12: Measurement verification of the transfer characteristics. Drain current as a function of gate voltage at $V_{\rm D} = 100$ mV on a linear scale.

for $V_{\rm DS} = 0$ [109, 110].

2.4 Local Model Verification with Experimental Data

SP-HV is also verified against measurement data. The transfer characteristics at low $V_{\rm D}(= 100$ mV) and moderate to high $V_{\rm D}(= 4.1, 8.1, 12.1, 16.1, 20.1$ V) are shown in Figs. 2.12 through 2.15. The sharp $G_{\rm m}$ peak for low $V_{\rm D}$, characteristic of LDMOS devices, is faithfully reproduced by the new model. At high $V_{\rm D}$, the LDMOS transistor operates in saturation or quasi-saturation. In both the $I_{\rm D}(V_{\rm G})$ curves and the $G_{\rm m}(V_{\rm G})$ curves, the transition between the saturation and quasi-saturation can be clearly seen and SP-HV captures this behavior.

Figs. 2.16 and 2.17 show fitting of output characteristics. The quasi-saturation effect is well reproduced. The negative output conductance, observed between the "dips" in output conductance plot, are caused by self-

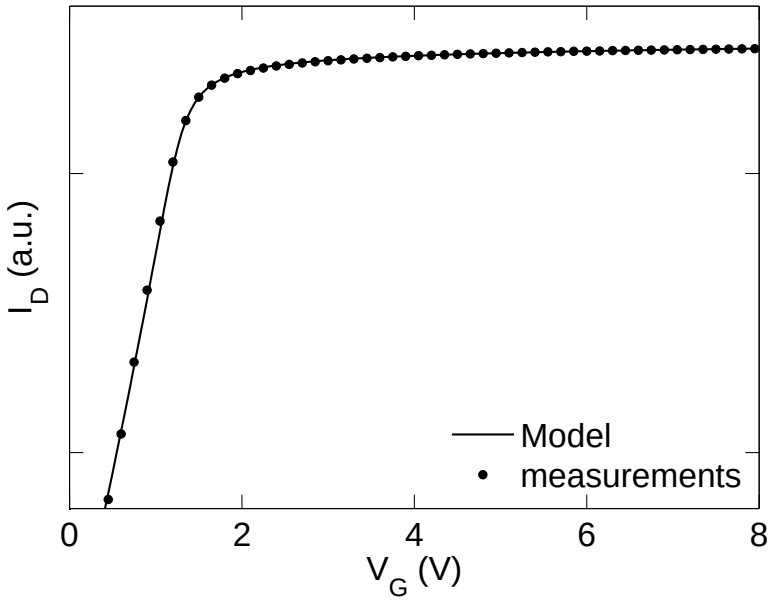


Figure 2.13: Measurement verification of the transfer characteristics. Drain current as a function of gate voltage at $V_{\mathrm{D}} = 100$ mV on a semi-logarithmic scale.

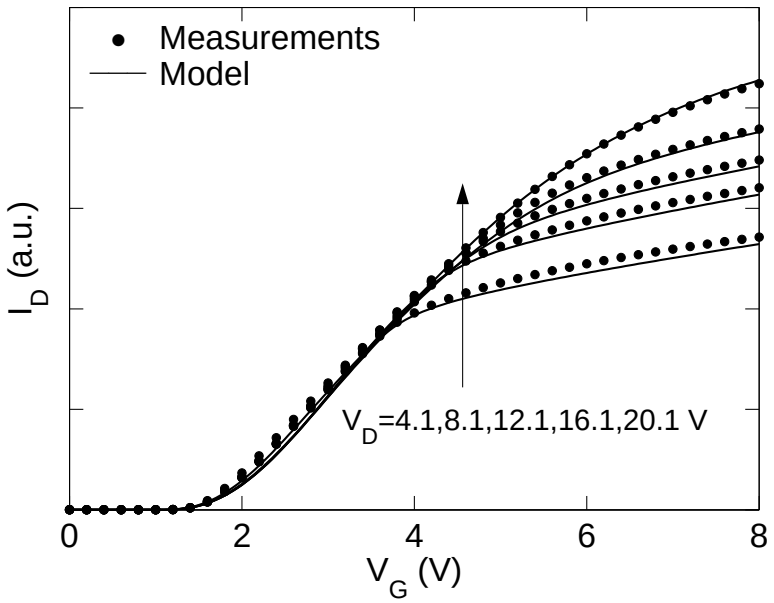


Figure 2.14: Measurement verification of the transfer characteristics. Drain current as a function of gate voltage at $V_{\mathrm{D}} = 4.1, 8.1, 12.1, 16.1, 20.1$ V.

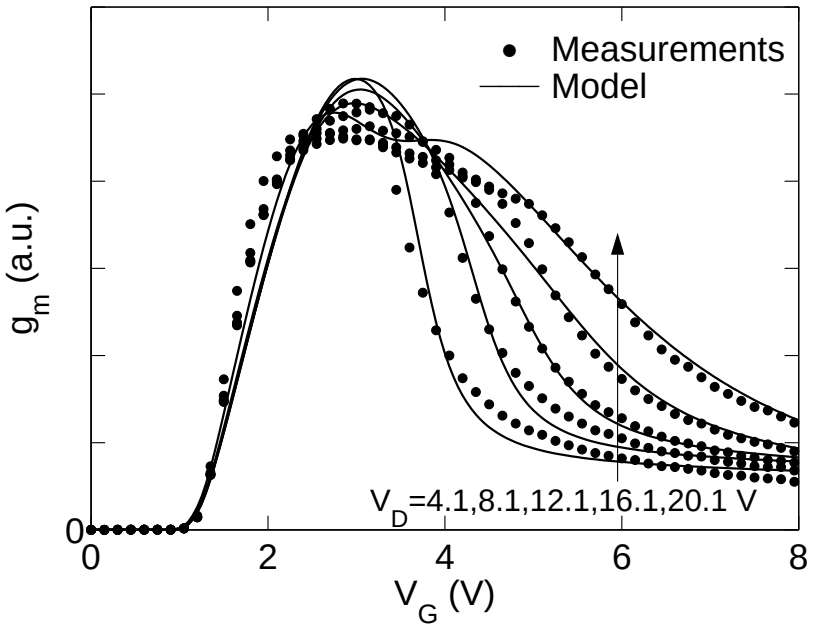


Figure 2.15: Measurement verification of the transfer characteristics. Transfer conductance as a function of gate voltage at $V_{\mathrm{D}} = 4.1, 8.1, 12.1, 16.1, 20.1$ V.

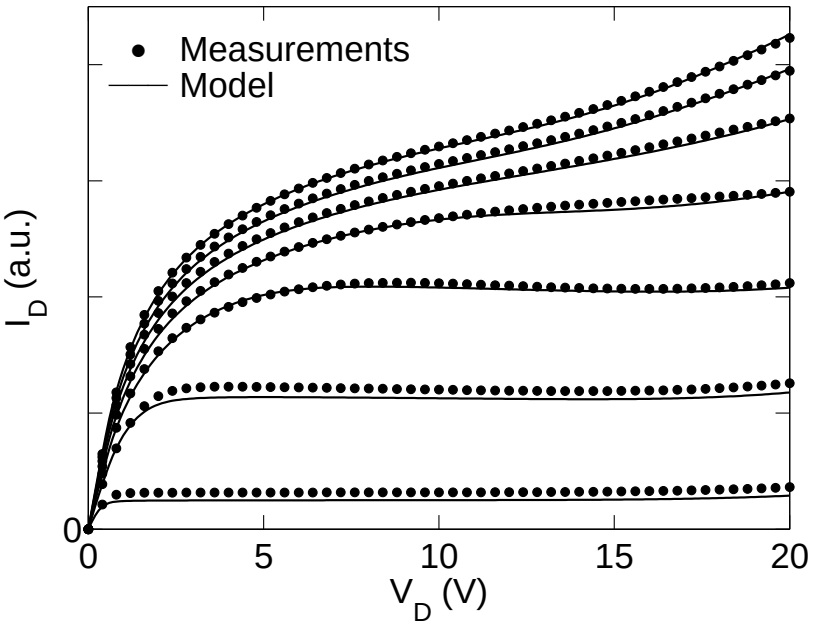


Figure 2.16: Measurement verification of the output characteristics. Drain current as a function of drain voltage at $V_{\mathrm{G}} = 2$ V to 8 V by step of 1 V.

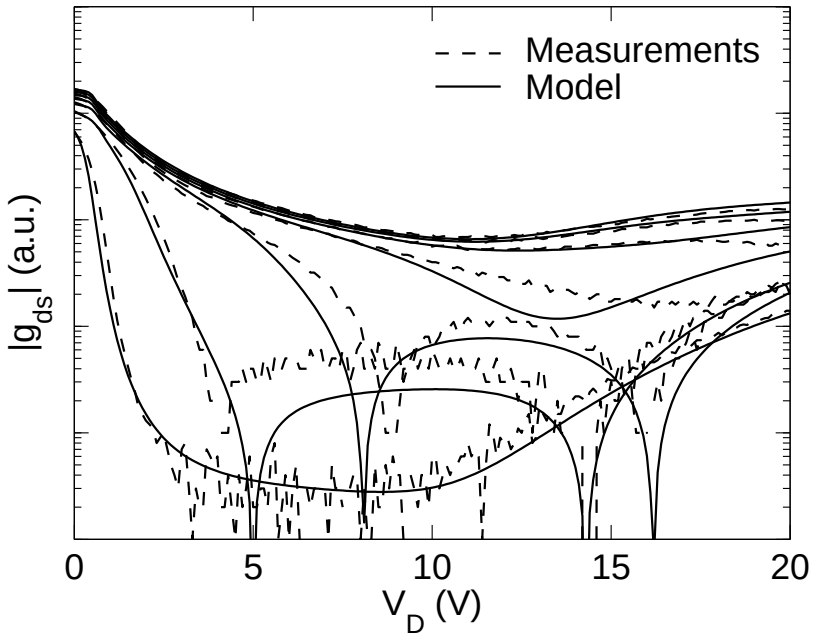


Figure 2.17: Measurement verification of the output characteristics. Output conductance as a function of drain voltage at $V_{\mathrm{G}} = 2$ V to 8 V by step of 1 V.

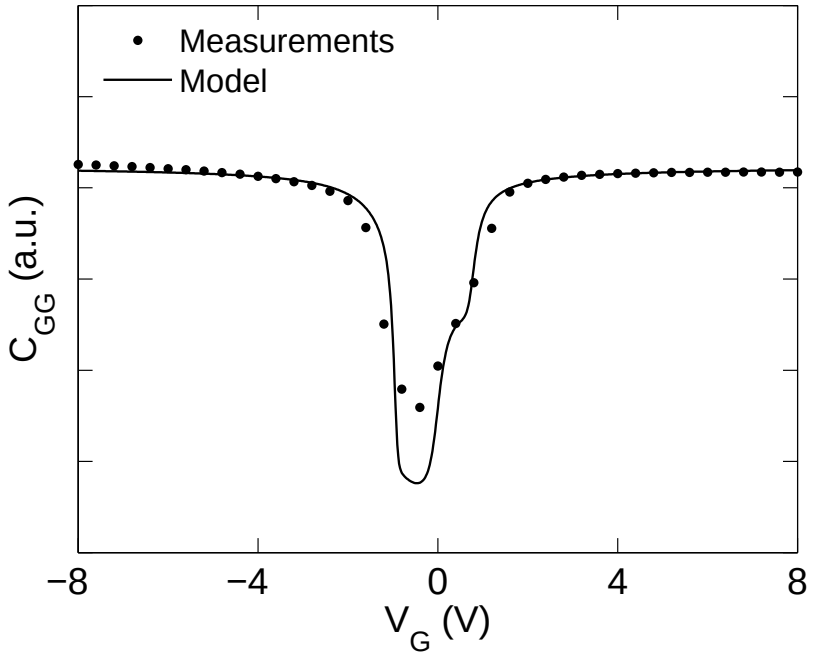


Figure 2.18: Fitting of the measured gate capacitance as a function of gate voltage; $V_{\mathrm{DS}} = 0$.

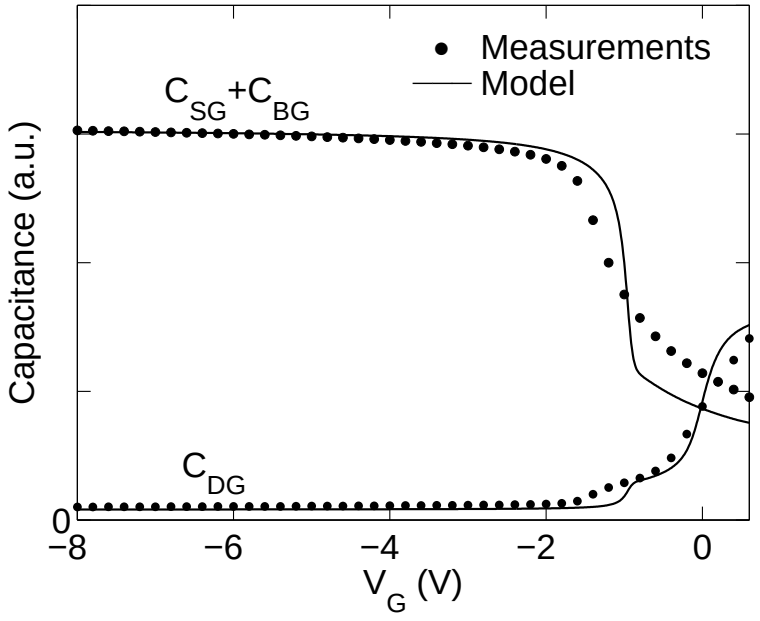


Figure 2.19: Fitting of the measured $C_{\mathrm{SG}} + C_{\mathrm{BG}}$ and C_{DG} as a function of gate voltage; $V_{\mathrm{DS}} = 0$.

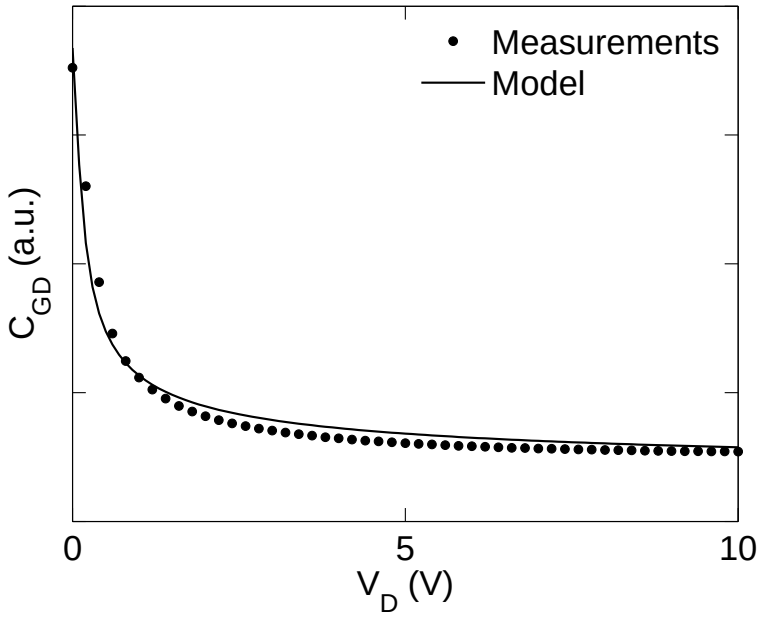


Figure 2.20: Fitting of the measured transcapacitance C_{GD} as a function of drain voltage; $V_{\mathrm{GS}} = 0$.

heating. At high drain and high gate biases, the drain current is enhanced by impact ionization in the drift region.

Figs. 2.18 through 2.20 show the fitting of the measured C_{GG}, C_{DG} and $C_{SG} + C_{BG}$ (in the test structure, the source and body terminals are shorted). In Fig. 2.18, there is a "step" in the model results around $V_G = 0.6$ V. In the measured data, this step is present but is less pronounced due to the lateral non-uniform doping near the transition from intrinsic channel to the first drift region (cf. Fig. 2.1). This conclusion has been verified by TCAD simulations presented in [111]. Similarly, the step near $V_G = -1$ V in Fig. 2.19 is associated with the onset of inversion in the first drift region (cf. Fig. 2.1). Again, TCAD simulations confirm that it is less pronounced in the measured data due to the lateral doping non-uniformity effects, which are not included in the present version of SP-HV. The lateral non-uniformity has little effect on the $C_{GD}(V_D)$ dependence shown in Fig. 2.20.

2.5 Summary

This Chapter has presented the modeling approach of the new LDMOS model, SP-HV, which is based on a combination of the PSP and R3 models, both modified to better reflect details of LDMOS device structure and behavior. In particular, a new charge model is developed that accounts for charge in the first drift region. This leads to an accurate prediction of the transcapacitances. The essential physical content of the model, including quasi-saturation, self-heating, impact ionization in the drift region and the complex behavior of transcapacitances, is verified against both TCAD simulations and experimental data.

CHAPTER 3

MODEL SCALABILITY

In the previous Chapter, the modeling approach is selected and validated with both TCAD simulations and experimental data. But the model scalability, one of the advantages of SP-HV over most existing LDMOS transistor models, has not yet been verified. In this chapter, model scalability is extensively verified with both TCAD simulations and experimental data.

3.1 Structure of SP-HV

The SP-HV model has a hierarchical structure, similar to that of PSP [74,75]. This means that there is a strict separation of the geometry scaling in the global level and the electrical model in the local level. As a consequence, SP-HV can be used at either one of two levels.

- **Global level** One uses a global parameter set, which describes a whole geometry range. Combined with device geometry (such as L and W), a local parameter set is internally generated by "scaling rules" which are equations describing the geometry dependencies of the *local* level model parameters.

- **Local level** One uses a local level parameter set and the model electrical equations to simulate the transistor.

The use of the hierarchical structure facilitates the model parameter extraction as one can extract the local parameters for each geometry separately and then use scaling equations to obtain the global parameters for the relevant

range of geometries. For example, the scaling rule of $\mathbf{C_S}$ is given by [112]

$$\mathbf{C_S} = \left[\mathbf{C_{SO}} + \frac{\mathbf{C_{SL}}}{L_{\text{eff}}^{\mathbf{C_{SLEXP}}}}\right] \cdot \left(1 + \frac{\mathbf{C_{SW}}}{W_{\text{eff}}}\right) \cdot \left(1 + \frac{\mathbf{C_{SLW}}}{W_{\text{eff}} \cdot L_{\text{eff}}}\right) \tag{3.1}$$

in which $\mathbf{C_{SO}}$, $\mathbf{C_{SL}}$, $\mathbf{C_{SLEXP}}$, $\mathbf{C_{SW}}$, and $\mathbf{C_{SLW}}$ are global level model parameters that determine the value of local model parameter $\mathbf{C_S}$ through scaling rule (3.1). With properly selected scaling rules, the SP-HV global level model gives a good description over the whole geometry range of LDMOS technologies.

3.2 Scaling Equations

This section shows the key equations in SP-HV which enable its scaling with device geometry: W and L for the intrinsic MOSFET; W_{dr1} and L_{dr1} for the first drift region; W_{dr2} and L_{dr2} for the second drift region. Some of the equations have already been introduced in Chapter 2 and they are repeated below for convenience and completeness.

Fig. 3.1 shows a cross-section view and a top view of a typical LDMOS transistor. The drawn widths of the intrinsic MOSFET and the drift regions are usually the same except for "racetrack" devices.

Intrinsic MOSFET and the First Drift Region

The geometry dependent current of the intrinsic MOSFET and the first drift region is given by

$$I_{\text{ch}} = \mu_{\text{eff}} \frac{W_{\text{eff}}}{L_{\text{eff}}} q_{\text{im}} \Delta\psi \tag{3.2}$$

where $\Delta\psi = \psi_{\text{sdi}} - \psi_{\text{ss}}$ is the surface-potential variation across the channel and ψ_{sdi} and ψ_{ss} are the surface-potentials at the internal drain and the source, respectively. q_{im} is the normalized magnitude of the inversion charge at the

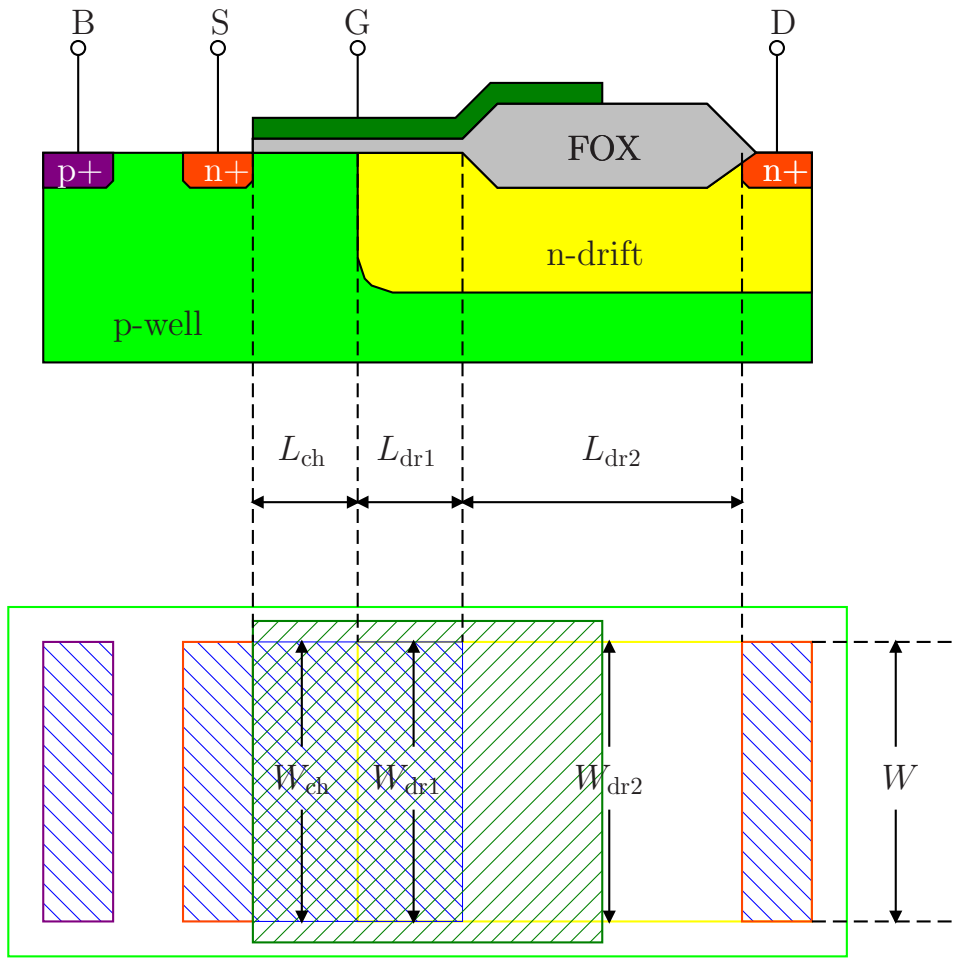


Figure 3.1: Simplified cross-section view and top view of a typical LDMOS transistor. The lengths and widths of different regions are labeled.

surface-potential midpoint. W_{eff} and L_{eff} are the effective width and length of the intrinsic MOSFET, respectively, which are given by

$$L_{\mathrm{eff}} = L_{\mathrm{ch}} + \mathbf{L_0} \cdot \left(\frac{\mathbf{L_L}}{L_{\mathrm{ch}}}\right) \cdot \left(\frac{\mathbf{L_W}}{W_{\mathrm{ch}}}\right) - \mathbf{L_{AP}} \tag{3.3}$$

$$W_{\mathrm{eff}} = W_{\mathrm{ch}} + \mathbf{W_0} \cdot \left(\frac{\mathbf{W_L}}{L_{\mathrm{ch}}}\right) \cdot \left(\frac{\mathbf{W_W}}{W_{\mathrm{ch}}}\right) - 2 \cdot \mathbf{W_{OT}} \tag{3.4}$$

where $\mathbf{L_0}$, $\mathbf{L_L}$, $\mathbf{L_W}$, $\mathbf{L_{AP}}$, $\mathbf{W_0}$, $\mathbf{W_L}$, $\mathbf{W_W}$, and $\mathbf{W_{OT}}$ are model parameters that account for the offsets of the device width and length.

The effect of the series resistance of the first drift region on current is included in the model by modifying the effective mobility, given by the ex-

pression [74, 75]

$$\mu_{\text{eff}} = \frac{\mathbf{U_O} \cdot \mu_{\text{x}}}{1 + (\boldsymbol{\mu}_{\mathbf{E}} \cdot E_{\text{eff}})^{\boldsymbol{\theta}_{\boldsymbol{\mu}}} + \mathbf{C_S} \left(\frac{q_{\text{bm}}}{q_{\text{im}}+q_{\text{bm}}}\right)^2 + G_{\text{R}}} \tag{3.5}$$

in which G_{R} accounts for the resistance of the first drift region, given by

$$G_{\text{R}} = \mathbf{U_O} \cdot \frac{W_{\text{eff}}}{L_{\text{eff}}} \cdot q_{\text{im}} \cdot \mathbf{R_S} \cdot \frac{1 + \mathbf{R_{SB}} \cdot V_{\text{SB}}}{1 + \mathbf{R_{SG}} \cdot q_{\text{im}}}, \tag{3.6}$$

where

$$\mathbf{R_S} = \mathbf{R_{S1}} \cdot \frac{L_{\text{dr1}}}{W_{\text{dr1}}} \left(1 + \mathbf{R_{S2}} \cdot \frac{1}{W_{\text{dr1}}}\right), \tag{3.7}$$

$\mathbf{R_{S1}}$ and $\mathbf{R_{S2}}$ are model parameters. The bias dependence of G_{R} is inherited from PSP [74, 75].

In addition, the local electrical parameters such as $\boldsymbol{\mu}_{\mathbf{E}}$, $\boldsymbol{\theta}_{\boldsymbol{\mu}}$, and $\mathbf{C_S}$ in (3.5) are dependent on the geometry of the intrinsic MOS device. These geometry dependencies are referred to as "scaling rules" in the model as described in Section 3.2. Equation (3.7) is another example of scaling rules, describing the scaling of the first drift region resistance. The scaling rules of the intrinsic MOSFET are inherited from PSP and one can refer to [112] for details.

The G_{R} term in (3.5) accounts for the series resistance of the first drift region but not for the contribution of charges in the same region. These can be modeled physically by modifying the overlap capacitance submodel in SP [82] or PSP [74], which is based on a surface-potential formulation. The modification includes the inversion of the first drift region as introduced in Section 2.2. With this modification, the contributions of the first drift region to the integrated gate, inversion and body charges are then given by

$$Q_{\text{GOV}} = C_{\text{oxov}} W_{\text{dr1}} L_{\text{dr1}} \left(V_{\text{G,DI}} - V_{\text{FBov}} - \psi_{\text{sov}}\right), \tag{3.8}$$

$$Q_{\text{IOV}} = \frac{C_{\text{oxov}} W_{\text{dr1}} L_{\text{dr1}} \phi_{\text{T}} G^2 D}{u_{\text{oxov}} + G\sqrt{e^{-x} + x - 1}}, \tag{3.9}$$

and

$$Q_{\mathrm{BOV}} = Q_{\mathrm{GOV}} - Q_{\mathrm{IOV}}\,. \tag{3.10}$$

Here

$$G = \gamma_{\mathrm{ov}} \Big/ \sqrt{\phi_{\mathrm{T}}}\,, \tag{3.11}$$

$$D = \exp\left(-\frac{2\phi_{\mathrm{Bov}} + V_{\mathrm{B,DI}}}{\phi_{\mathrm{T}}}\right) \cdot \left[e^{x} - x - 1 - \chi(x)\right]\,, \tag{3.12}$$

and

$$u_{\mathrm{oxov}} = (V_{\mathrm{G,DI}} - V_{\mathrm{FBov}} - \psi_{\mathrm{sov}})/\phi_{\mathrm{T}}\,. \tag{3.13}$$

The geometry dependence of charges in the first drift region is included in SP-HV through (3.8)–(3.10).

The Second Drift Region

The current in the second drift region is given by

$$I_{\mathrm{dr}} = I_{\mathrm{dr0}} \cdot \left(1 + \frac{V_{\mathrm{D,DI}}}{\mathbf{V_A}}\right) \cdot (1 + \boldsymbol{\theta}_{\mathbf{ACC}} \cdot V_{\mathrm{GS}}) \tag{3.14}$$

Its dependence on the second-drift-region geometry is included through I_{dr0} which is the current predicted by the R3 model [70, 71] without considering the effects of the $V_{\mathrm{D,DI}}$ and V_{GS} modulation. I_{dr0} can be expressed by

$$I_{\mathrm{dr0}} \propto \frac{1}{\mathbf{R_{SHDR}}} \cdot \frac{W_{\mathrm{dr2}} + \mathbf{X_W} + \mathbf{X_{WW}}/W_{\mathrm{dr2}}}{L_{\mathrm{dr2}} + \mathbf{X_L} + \mathbf{X_{LW}}/W_{\mathrm{dr2}}} \tag{3.15}$$

where $\mathbf{R_{SHDR}}$ is the sheet resistance of the second drift region, $\mathbf{X_W}$, $\mathbf{X_{WW}}$, $\mathbf{X_L}$, and $\mathbf{X_{LW}}$ are the width/length offset parameters. This geometry dependence is simplified from the original R3 model [70,71,73,113] to remove effects that are not seen in LDMOS drift regions.

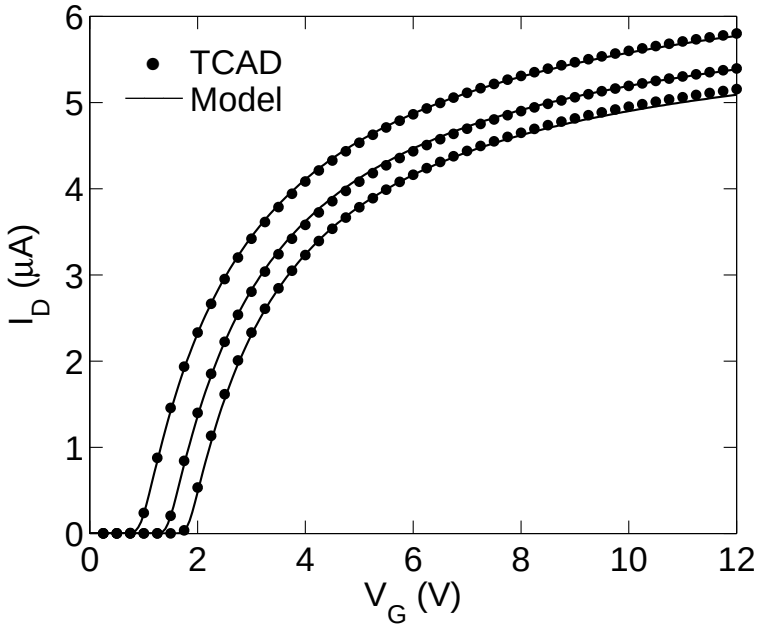
3.3 Global Model Verification with TCAD Simulations

TCAD simulations are used to verify the scaling properties of the drift region since the length and the doping concentration of the drift region in manufactured LDMOS transistors are usually fixed. The scaling with the geometry of the intrinsic MOSFET is verified with experimental data in Section 3.4.

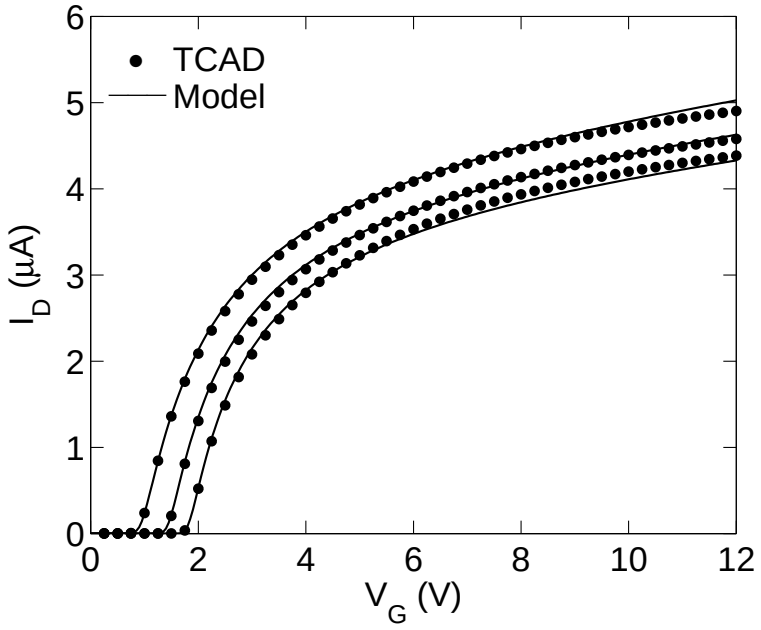
Length of the First Drift Region

Figs. 3.2 through 3.5 show the fitting of TCAD results with different lengths of the first drift region. $L_{\rm dr1} = 1$ μm and $L_{\rm dr1} = 4$ μm are used in the TCAD simulations. The length of the first drift region has a small effect on current in Figs. 3.2 through 3.4 because the overall drift region resistance is dominated by the contribution of the second drift region; the effect is nevertheless modeled well. In contrast [note the vertical scale differences in Figs. 3.5(a) and 3.5(b)], the gate capacitance significantly increases as $L_{\rm dr1}$ increases, and this is accurately modeled through (3.8).

For both $L_{\rm dr1}$ values in Fig. 3.5, it can be observed that at high $V_{\rm D}(= 12\,{\rm V})$, the TCAD data show a more gradual transition around $V_{\rm G} = -5$ V than the compact model results. The "softer" transition is caused by the lateral depletion at the p-substrate/n-drift region junction. For a longer first drift region, the effect of the junction lateral depletion is less pronounced because the depletion width is relatively small compared to $L_{\rm dr1}$. So TCAD results for long $L_{\rm dr1}(= 4$ μm) in Fig. 3.5(b) show a sharper transition than the results for short $L_{\rm dr1}(= 1$ μm) in Fig. 3.5(a). This lateral depletion has not been taken into account in SP-HV so that the compact model results show an abrupt transition. Also note that at $V_{\rm D} = 0$ when the lateral depletion is insignificant, the compact model results match TCAD data nicely.

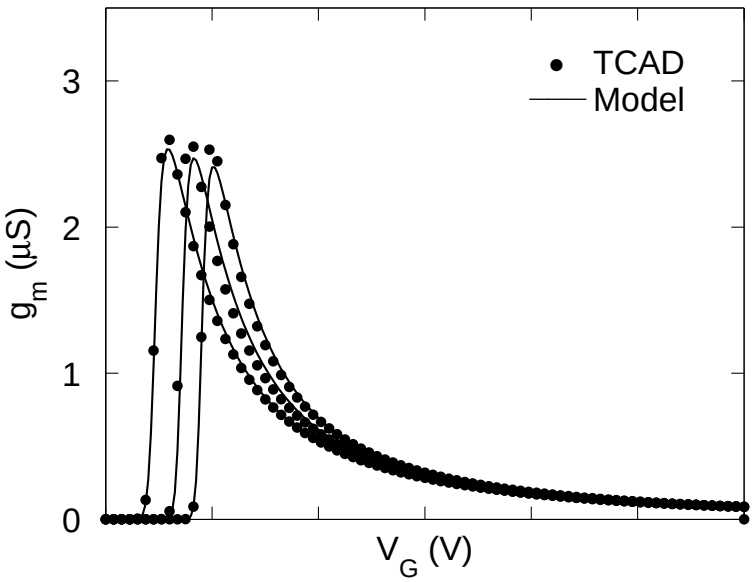


(a) $L_{\mathrm{dr1}} = 1\ \mu\mathrm{m}$

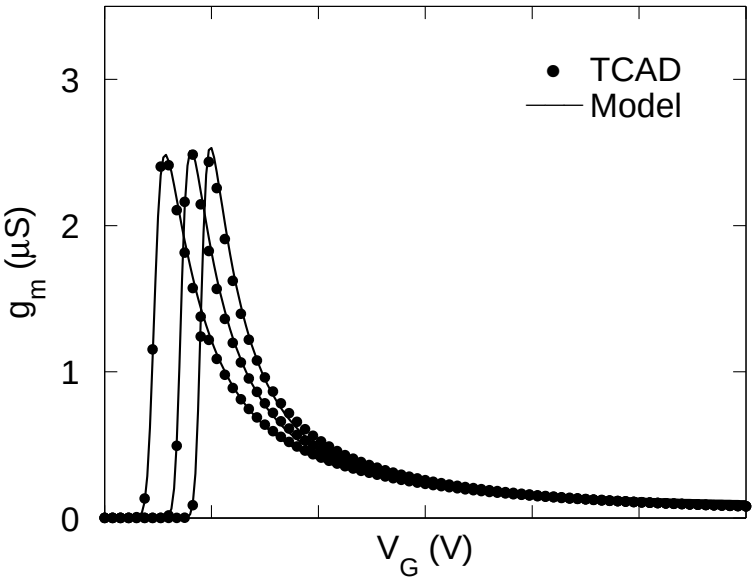


(b) $L_{\mathrm{dr1}} = 4\ \mu\mathrm{m}$

Figure 3.2: TCAD verification of the transfer characteristics. Drain current as a function of gate voltage at $V_{\mathrm{D}} = 100$ mV and $V_{\mathrm{B}} = 0, -1, -2$ V. Device parameters are given in Fig. 2.3 except L_{dr1} for scaling verification of the first drift region.

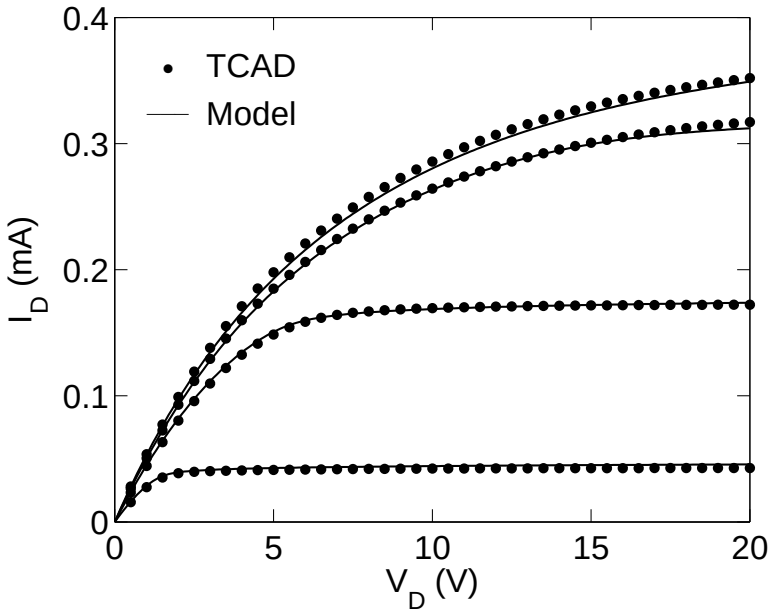


(a) $L_{\mathrm{dr1}} = 1\ \mu\mathrm{m}$

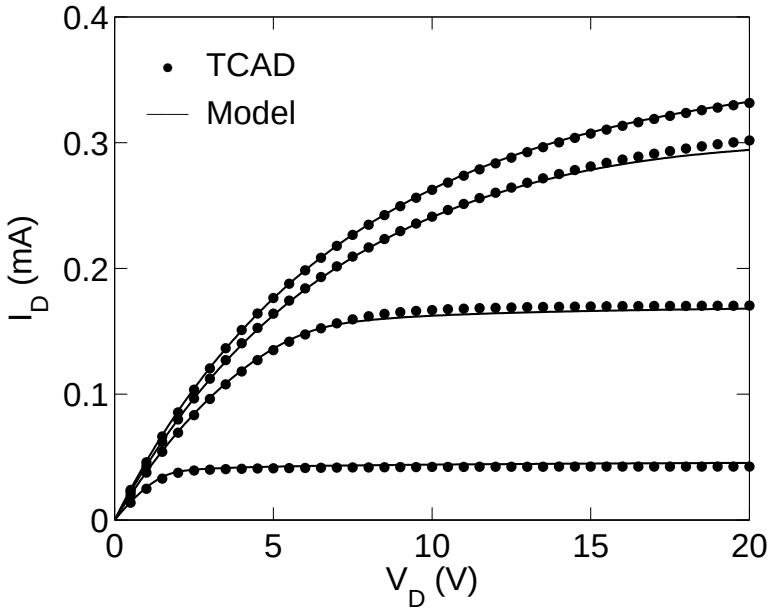


(b) $L_{\mathrm{dr1}} = 4\ \mu\mathrm{m}$

Figure 3.3: TCAD verification of the transfer characteristics. Transconductance as a function of gate voltage at $V_{\mathrm{D}} = 100$ mV and $V_{\mathrm{B}} = 0, -1, -2$ V. Device parameters are given in Fig. 2.3 except L_{dr1} for scaling verification of the first drift region.

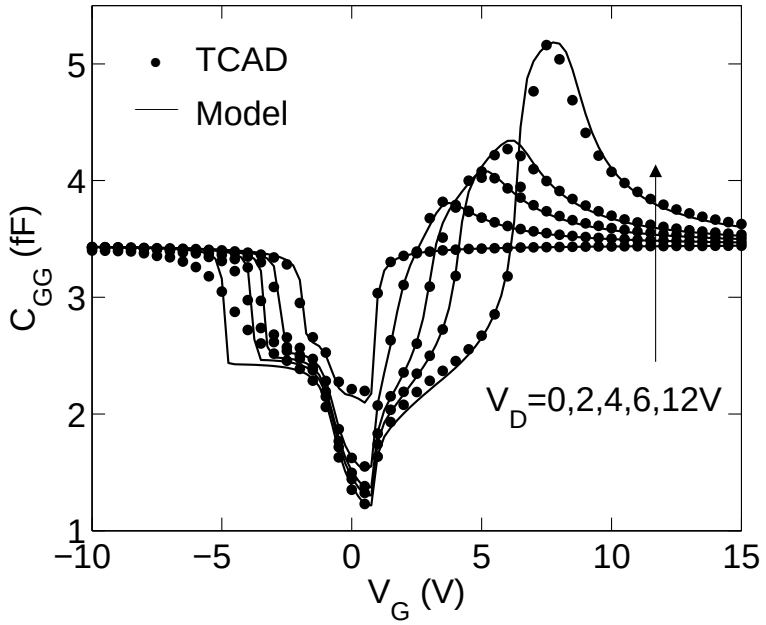


(a) $L_{\mathrm{dr1}} = 1\ \mu\mathrm{m}$

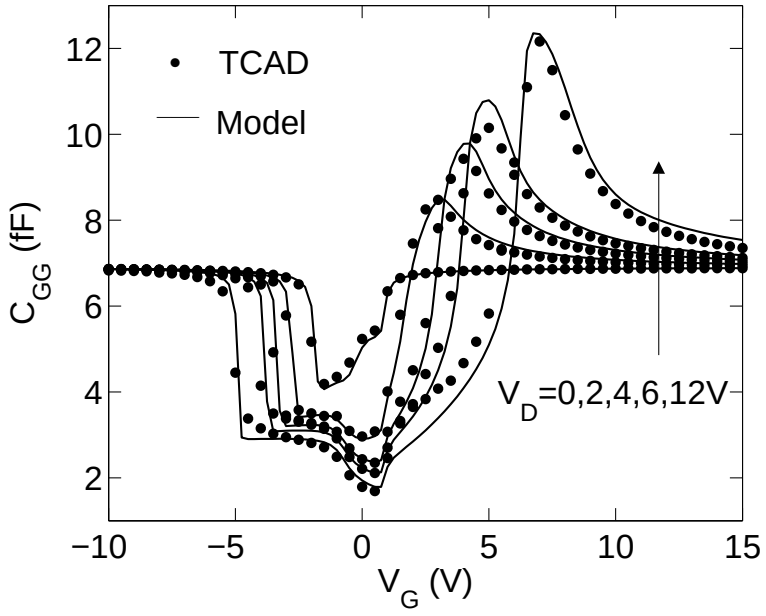


(b) $L_{\mathrm{dr1}} = 4\ \mu\mathrm{m}$

Figure 3.4: TCAD verification of the output characteristics. Drain current as a function of drain voltage at $V_{\mathrm{B}} = 0$ and $V_{\mathrm{G}} = 3, 6, 9, 12$ V. Device parameters are given in Fig. 2.3 except L_{dr1} for scaling verification of the first drift region.



(a) $L_{\mathrm{dr1}} = 1\ \mu\mathrm{m}$



(b) $L_{\mathrm{dr1}} = 4\ \mu\mathrm{m}$

Figure 3.5: TCAD verification of the gate capacitance. $V_{\mathrm{B}} = 0$. Device parameters are given in Fig. 2.3 except L_{dr1} for scaling verification of the first drift region.

Length of the Second Drift Region

Figs. 3.6 through 3.9 show the fitting of TCAD results with different lengths of the second drift region. $L_{\mathrm{dr2}} = 1\ \mu$m and $L_{\mathrm{dr2}} = 5\ \mu$m are used in the TCAD simulations. For short length of the second drift region, the resistance of the drift region is reduced, and the device shows less significant LDMOS effects: the peaks in g_{m} are less sharp in Fig. 3.7 and the quasi-saturation effect is less pronounced in Fig. 3.8.

Fig. 3.9 shows the fitting of the gate capacitance for different lengths of the second drift region. Both the magnitude and the position of the peaks in C_{GG} are changed due to the different drift region resistances. The variation in C_{GG} is well captured by the new model, which further validates the scalability of the second drift region.

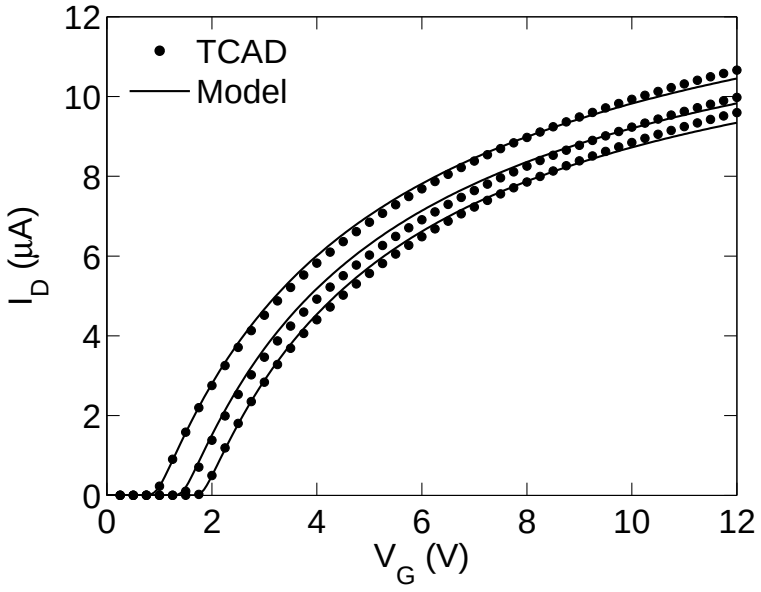
Doping Concentration in the Drift Region

Figs. 3.10 through 3.12 show the fitting of two different doping concentrations in the drift region. For heavily doped drift region, the drift region resistance is small and the device shows less significant LDMOS effects: the peaks in g_{m} are less sharp in Fig. 3.11 and the quasi-saturation effect is less pronounced in 3.12.

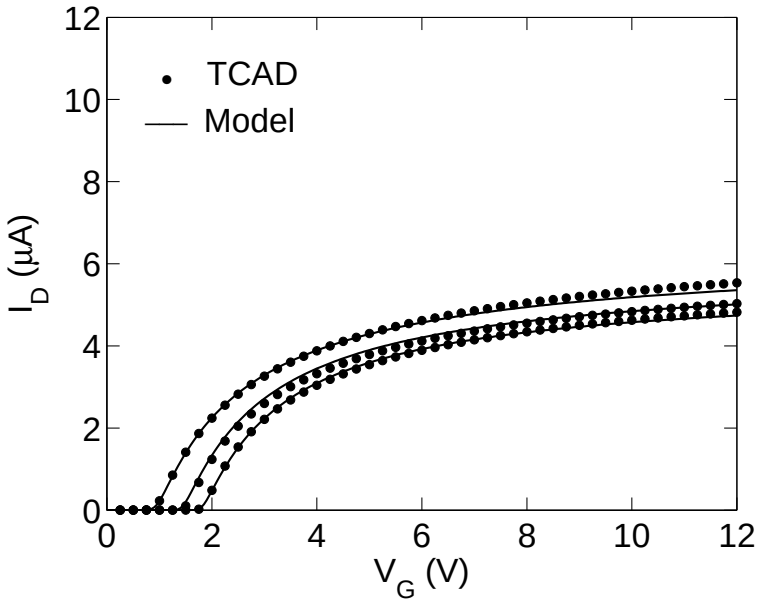
The close agreement over different drift region parameters in Figs. 3.2 through 3.12 verifies the scalability of the drift region model in this work.

3.4 Global Model Verification with Experimental Data

Measurement data are used to verify both the width and length scaling of the intrinsic MOSFET region. Fig. 3.13 shows the transfer characteristics at low

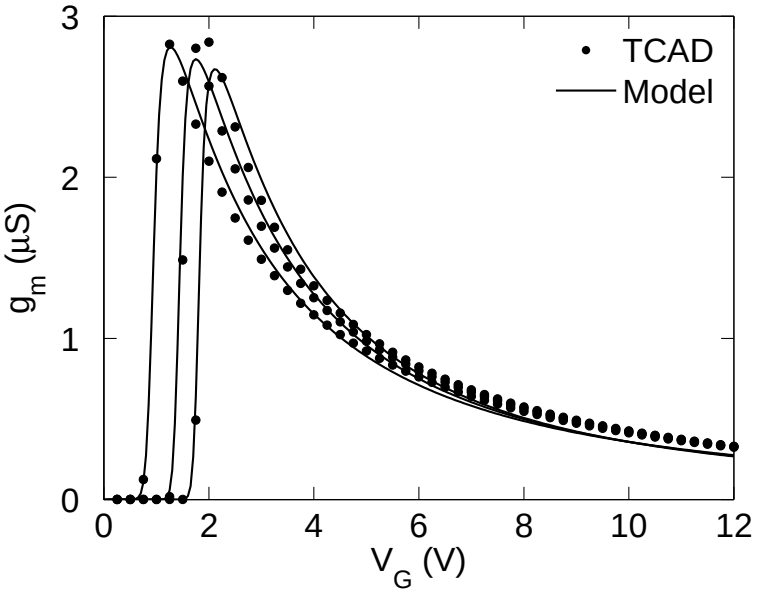


(a) $L_{\mathrm{dr2}} = 1\ \mu\mathrm{m}$

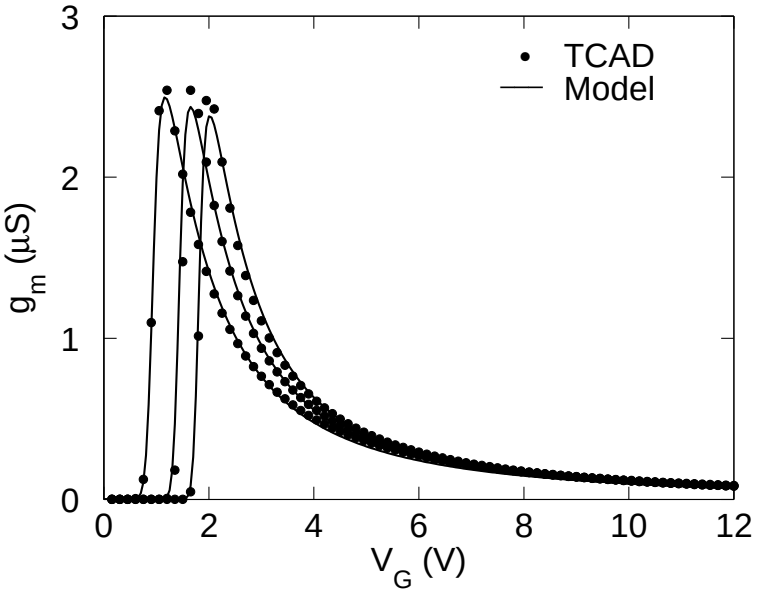


(b) $L_{\mathrm{dr2}} = 5\ \mu\mathrm{m}$

Figure 3.6: TCAD verification of the transfer characteristics. Drain current as a function of gate voltage at $V_{\mathrm{D}} = 100$ mV and $V_{\mathrm{B}} = 0, -1, -2$ V. Device parameters are given in Fig. 2.3 except L_{dr2} for scaling verification of the second drift region.

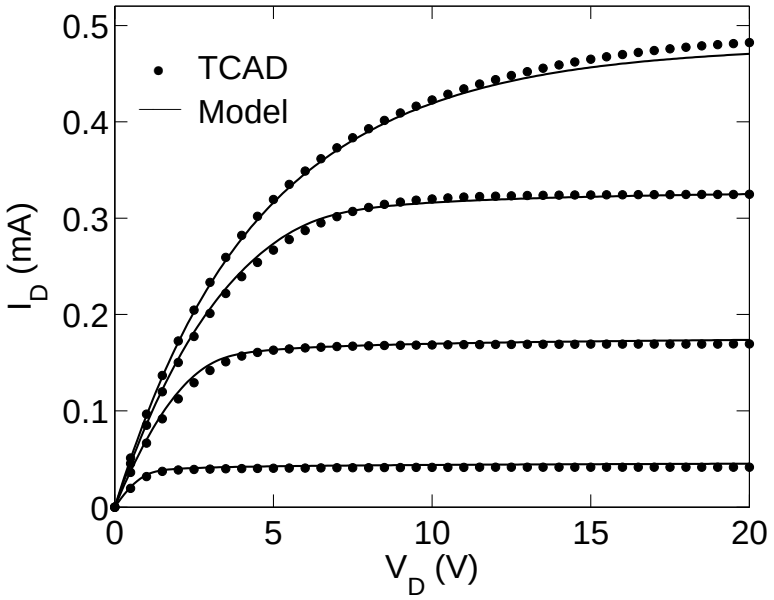


(a) $L_{\mathrm{dr2}} = 1\ \mu\mathrm{m}$

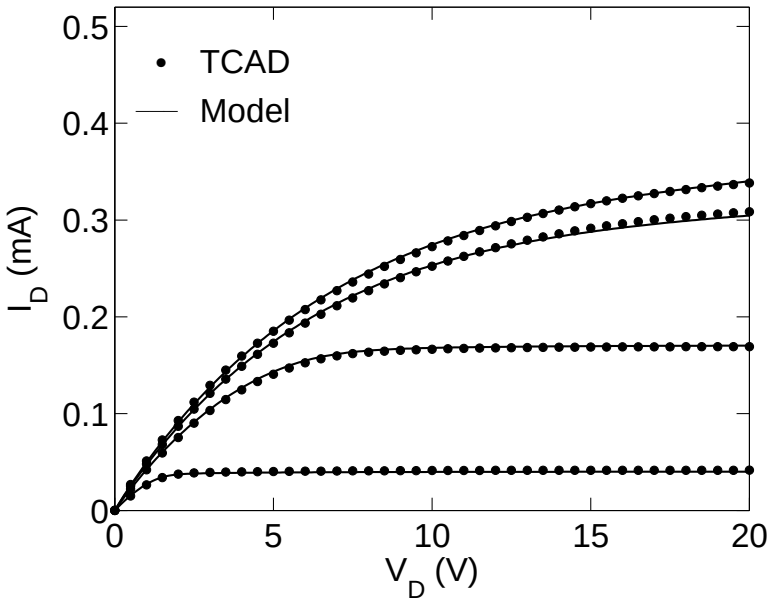


(b) $L_{\mathrm{dr2}} = 5\ \mu\mathrm{m}$

Figure 3.7: TCAD verification of the transfer characteristics. Transconductance as a function of gate voltage at $V_{\mathrm{D}} = 100$ mV and $V_{\mathrm{B}} = 0, -1, -2$ V. Device parameters are given in Fig. 2.3 except L_{dr2} for scaling verification of the second drift region.

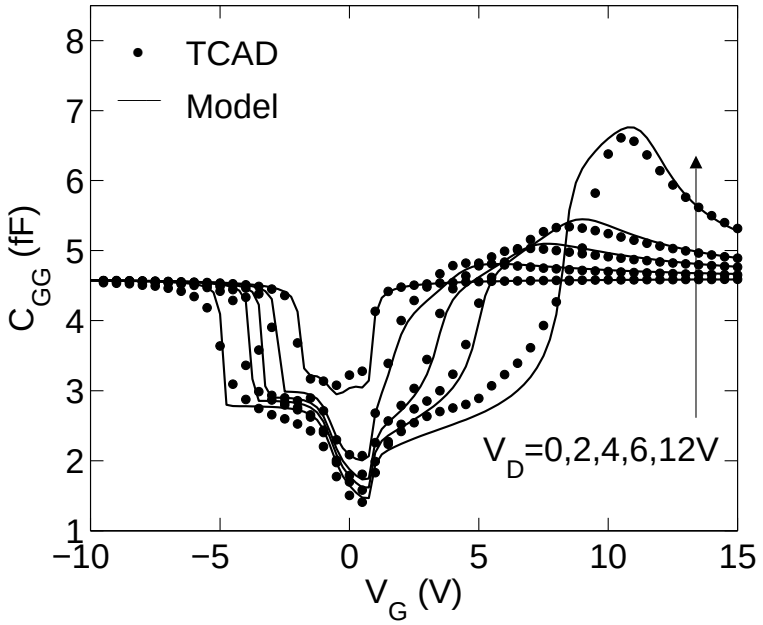


(a) $L_{\mathrm{dr2}} = 1\ \mu\mathrm{m}$

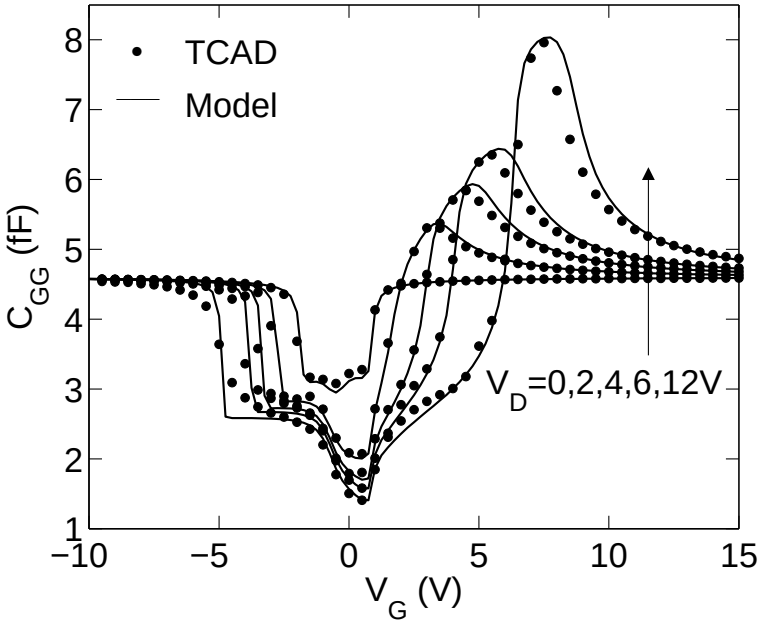


(b) $L_{\mathrm{dr2}} = 5\ \mu\mathrm{m}$

Figure 3.8: TCAD verification of the output characteristics. Drain current as a function of drain voltage at $V_{\mathrm{B}} = 0$ and $V_{\mathrm{G}} = 3, 6, 9, 12$ V. Device parameters are given in Fig. 2.3 except L_{dr2} for scaling verification of the second drift region.

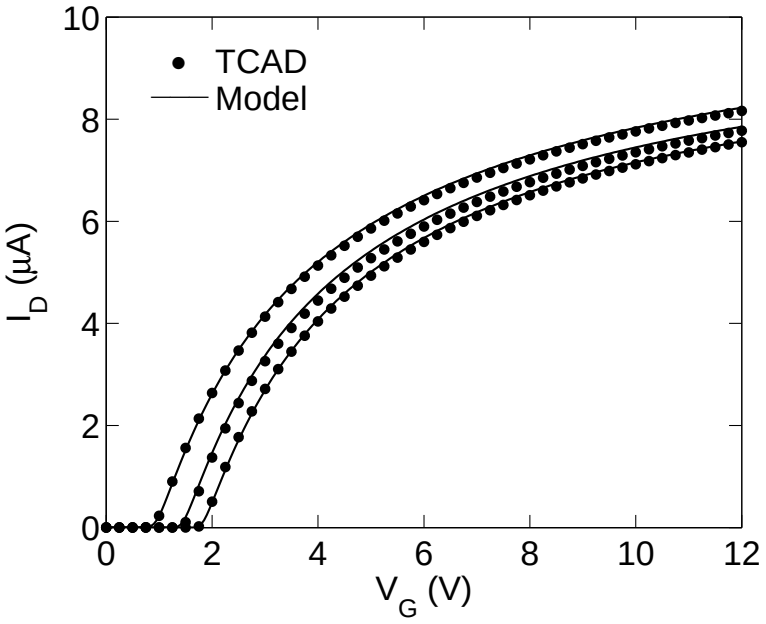


(a) $L_{\mathrm{dr2}} = 1\ \mu\mathrm{m}$

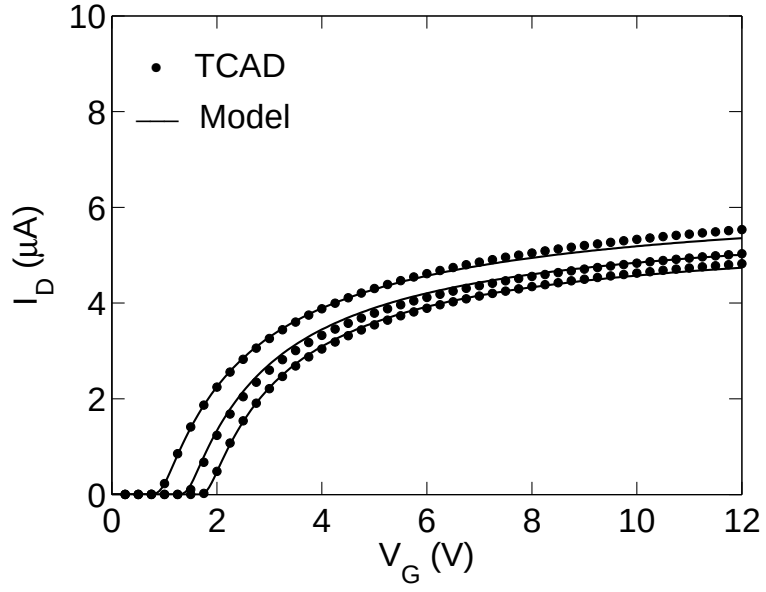


(b) $L_{\mathrm{dr2}} = 5\ \mu\mathrm{m}$

Figure 3.9: TCAD verification of the gate capacitance. $V_{\mathrm{B}} = 0$. Device parameters are given in Fig. 2.3 except L_{dr2} for scaling verification of the second drift region.

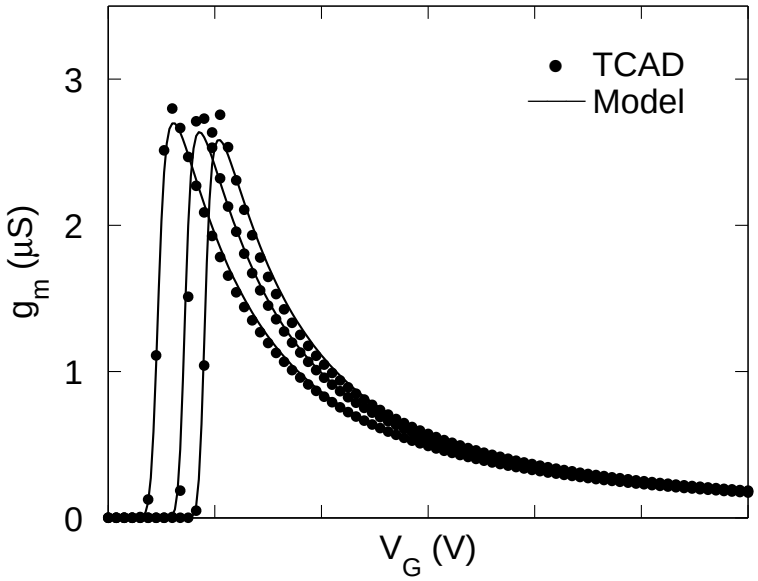


(a) $N_{\text{drift}} = 1 \times 10^{17}$ cm^{-3}

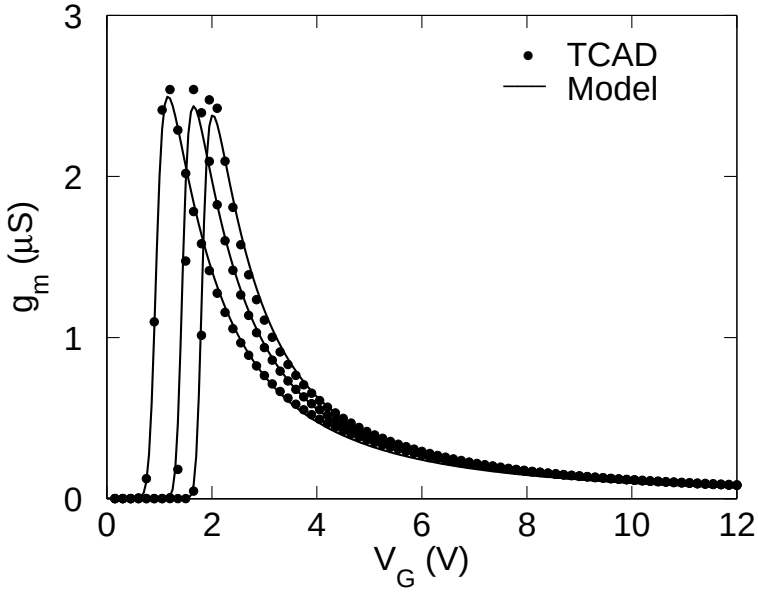


(b) $N_{\text{drift}} = 5 \times 10^{16}$ cm^{-3}

Figure 3.10: TCAD verification of the transfer characteristics. Drain current as a function of gate voltage at $V_{\text{D}} = 100$ mV and $V_{\text{B}} = 0, -1, -2$ V. Device parameters are given in Fig. 2.3 except N_{drift} for scaling verification of the doping concentration in the drift region.

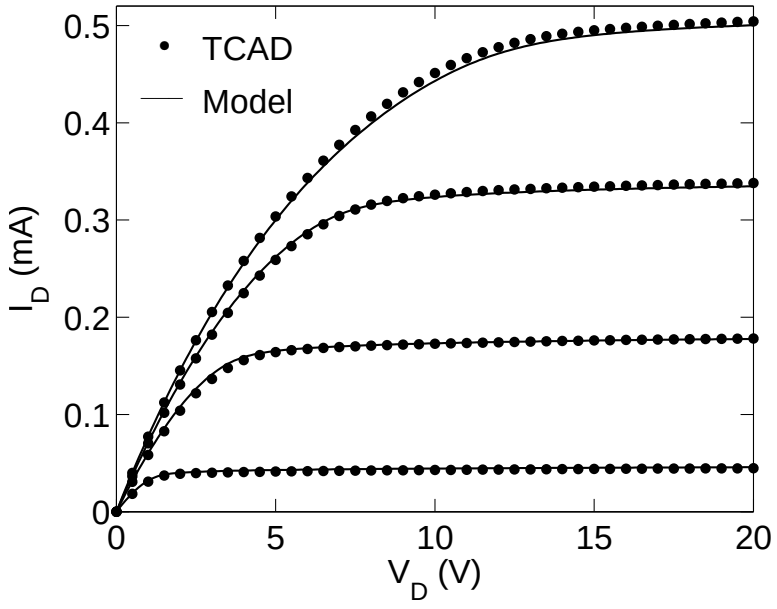


(a) $N_{\text{drift}} = 1 \times 10^{17}$ cm^{-3}

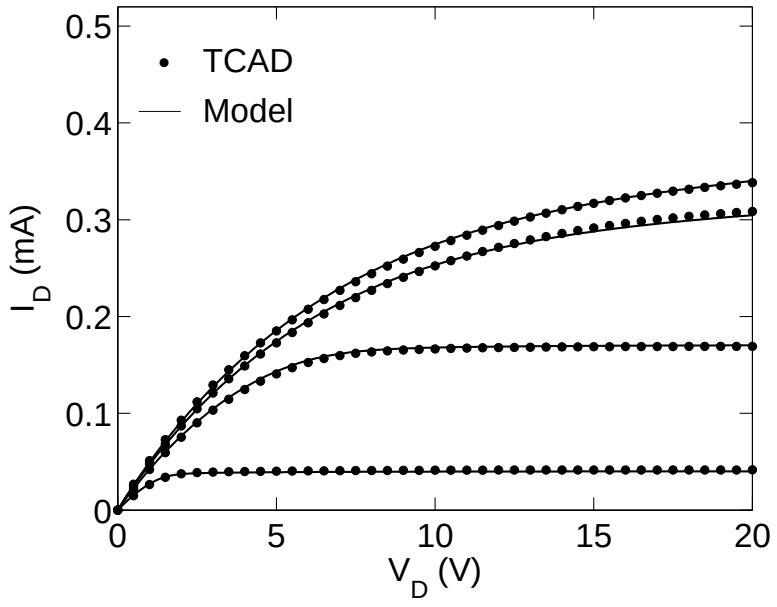


(b) $N_{\text{drift}} = 5 \times 10^{16}$ cm^{-3}

Figure 3.11: TCAD verification of the transfer characteristics. Transconductance as a function of gate voltage at $V_{\text{D}} = 100$ mV and $V_{\text{B}} = 0, -1, -2$ V. Device parameters are given in Fig. 2.3 except N_{drift} for scaling verification of the doping concentration in the drift region.

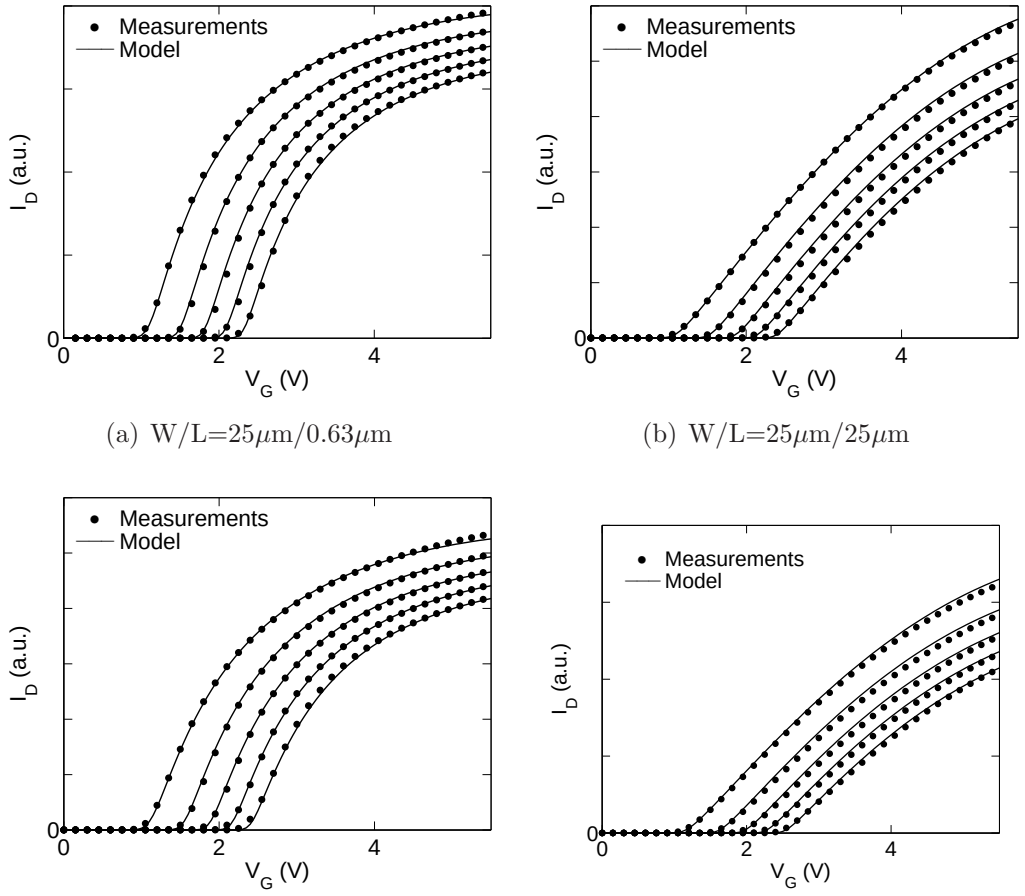


(a) $N_{\text{drift}} = 1 \times 10^{17}$ cm^{-3}



(b) $N_{\text{drift}} = 5 \times 10^{16}$ cm^{-3}

Figure 3.12: TCAD verification of the output characteristics. Drain current as a function of drain voltage at $V_{\text{B}} = 0$ and $V_{\text{G}} = 3, 6, 9, 12$ V. Device parameters are given in Fig. 2.3 except N_{dr2} for scaling verification of the second drift region.



(a) W/L=25μm/0.63μm

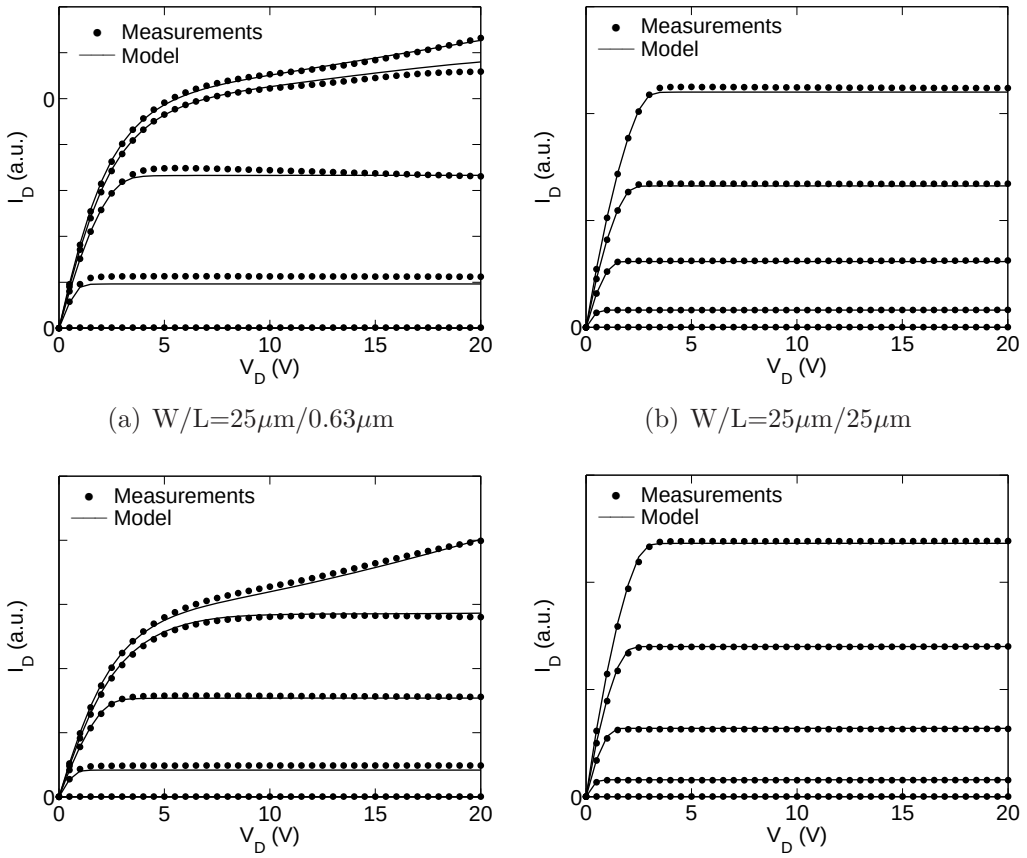
(b) W/L=25μm/25μm

(c) W/L=3.01μm/0.63μm

(d) W/L=3.01μm/25μm

Figure 3.13: Measurement verification of the transfer characteristics for different intrinsic MOSFET geometries. $V_{\mathrm{D}} = 100$ mV and $V_{\mathrm{B}} = 0$ to -4 V with a -1 V step.

V_{D} with V_{B} as a parameter, and Fig. 3.14 shows the output characteristics at $V_{\mathrm{B}} = 0$ with V_{G} as a parameter. In the output characteristics, the long-channel devices behave electrically like conventional MOSFETs since the drift region resistance is insignificant, as compared to the resistance of the intrinsic MOSFET. On the other hand, for the short-channel devices, quasi-saturation is clearly observed. A single global level parameter set can model all geometries, which verifies the scalability of the new model in terms of the intrinsic MOSFET width and length.



(a) W/L=25μm/0.63μm

(b) W/L=25μm/25μm

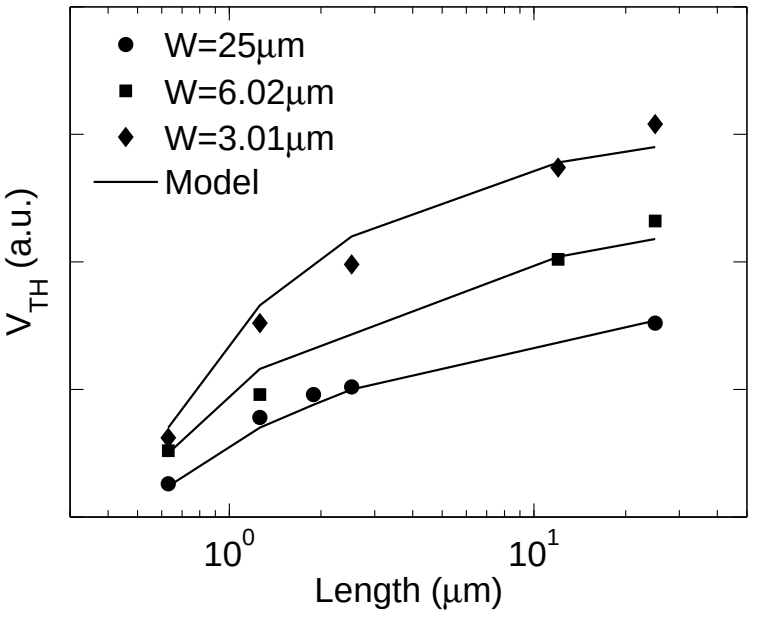
(c) W/L=3.01μm/0.63μm

(d) W/L=3.01μm/25μm

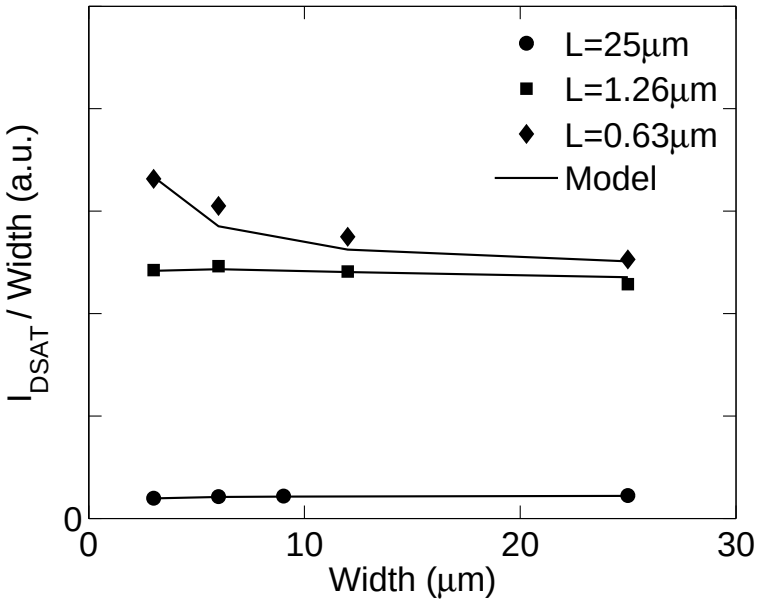
Figure 3.14: Measurement verification of the output characteristics for different intrinsic MOSFET geometries. $V_{\mathrm{B}} = 0$ V and $V_{\mathrm{G}} = 1.1$ V to 5.5 V with a 1.1 V step.

Fig. 3.15 compares the threshold voltage and the normalized I_{DSAT} for the measurement data and the new model over intrinsic MOSFET geometries. Both the short channel effect and the narrow width effect can be observed in the V_{TH} variation and they are accurately captured by SP-HV.

Fig. 3.16 shows the gate capacitance as a function of gate voltage for several intrinsic MOSFET lengths. For each $C_{\mathrm{GG}}(V_{\mathrm{G}})$ curve, there is a "step" around $V_{\mathrm{G}} = -2$ V. Physically, this step corresponds to the onset of the inversion of the first drift region. The transitions in simulated $C_{\mathrm{GG}}(V_{\mathrm{G}})$ curves are abrupt because in the compact model we assume both the intrinsic channel and the

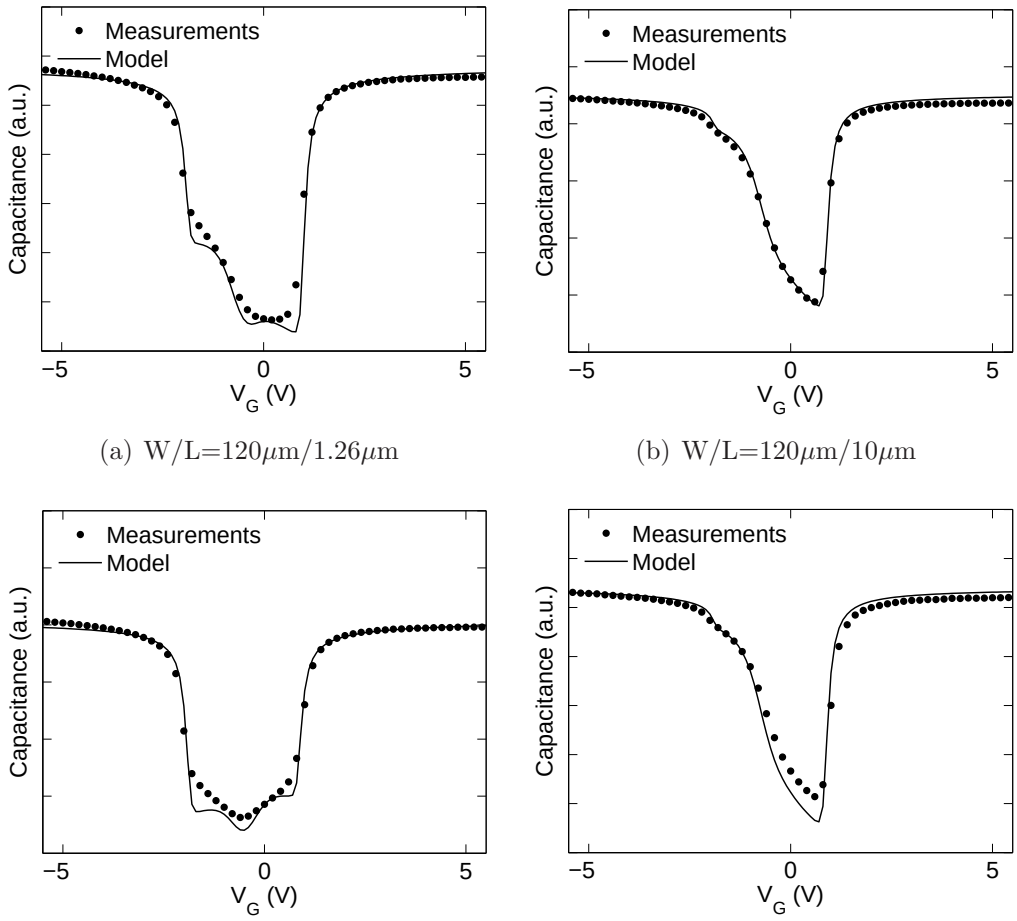


(a)



(b)

Figure 3.15: Measurement verification of the variation of threshold voltage and I_{DSAT} with intrinsic MOSFET geometries. I_{DSAT} is determined at $V_{\mathrm{G}} = 5.5$ V, $V_{\mathrm{D}} = 20$ V, and $V_{\mathrm{B}} = 0$. Symbols represent values from measurements and lines stand for model results.



(a) W/L=120μm/1.26μm

(b) W/L=120μm/10μm

(c) W/L=120μm/0.63μm

(d) W/L=3.01μm/10μm

Figure 3.16: Measurement verification of gate capacitance as a function of V_{G} for different intrinsic MOSFET lengths.

drift region are uniformly doped, whereas there is a gradual doping variation in between these two regions in actual devices.

Experimental data from another technology is also used to verify the scalability of SP-HV with device width. Fig. 3.17 shows the fitting of the normalized I_{DSAT} over device width at two bias conditions. The bias values are selected so that I_{DSAT1} is predominantly determined by the second drift region resistance and I_{DSAT2} is predominantly determined by the intrinsic MOS device behavior. The two curves in Fig. 3.17 show that the width dependencies

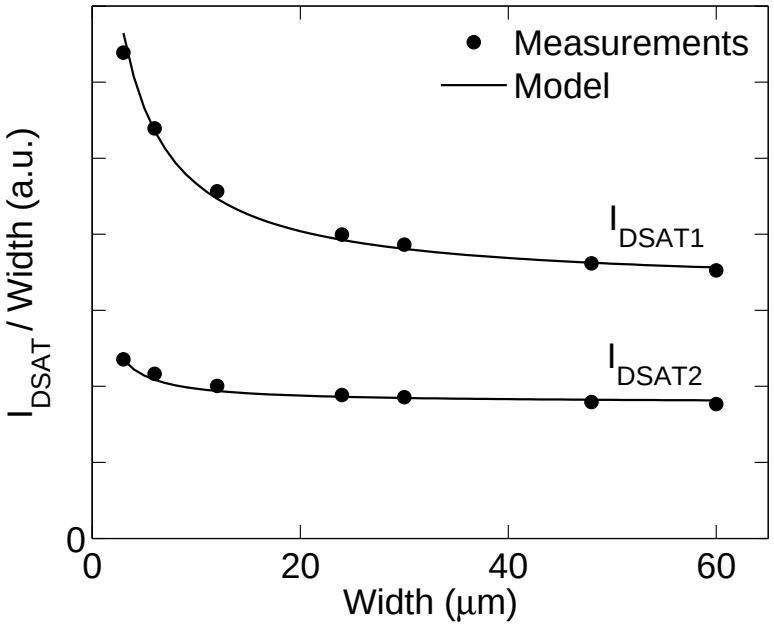


Figure 3.17: Normalized I_{DSAT} by device width at two different bias conditions as a function of device width. I_{DSAT1}: $V_{\mathrm{D}} = 20$ V and $V_{\mathrm{G}} = 8$ V; I_{DSAT2}: $V_{\mathrm{D}} = 20$ V and $V_{\mathrm{G}} = 4$ V;

of the two regions are slightly different, and both scaling trends have been well captured by the new model.

3.5 Summary

In this Chapter, the model scalability is extensively verified. The scalability of the drift region model is verified with TCAD simulations, including the length of the drift region and the doping concentration in the drift region. The scalability of the intrinsic MOSFET, with varying width and length, is verified with experimental data. The close agreement between the model results and the TCAD simulations/experimental data confirms the model scalability.

CHAPTER 4

BERGLUND RELATION IN LDMOS TRANSISTORS

Berglund related a certain area associated with the normalized MOS C(V) curve to the energy gap of silicon. Despite the fact that in LDMOS transistors the gate capacitance exhibits complicated behavior associated with the presence of the drift region, it turns out that the Berglund relation remains valid, as confirmed by both measurements and TCAD simulations.

4.1 Berglund Relation in MOSFET

For an ideal MOS capacitor

$$\int \left[1 - \frac{C\left(V_{\mathrm{G}}\right)}{C_{\mathrm{ox}}}\right] dV_{\mathrm{G}} \approx \frac{E_{\mathrm{g}}}{q} \tag{4.1}$$

where $C(V_{\mathrm{G}})$ denotes the overall quasi-equilibrium capacitance at the gate voltage V_{G}, C_{ox} is the oxide capacitance, E_{g} is the energy gap of silicon and q is the absolute value of the electronic charge [114]. The integral is taken from deep accumulation through strong inversion. This result, sometimes called the "Berglund Relation," is approximate since it ignores surface quantization, leakage currents, and polysilicon depletion. Furthermore, C_{ox} is seldom known precisely and is typically taken as the value of C somewhere deep in accumulation. Fig. 4.1 illustrates the original Berglund relation in a MOS capacitor. The area of the shaded region in the plot equals to E_{g}/q approximately.

Apart from providing a direct illustration of quantum mechanics (the existence of the energy gap) in a simple manner, the Berglund relation is useful as a practical tool: it allows one to check that the ramp rate during a $C(V_{\mathrm{G}})$ measurement is sufficiently slow so that the measured $C(V_{\mathrm{G}})$ curve can be regarded as quasi-equilibrium. In addition, (4.1) can serve as a qualitative

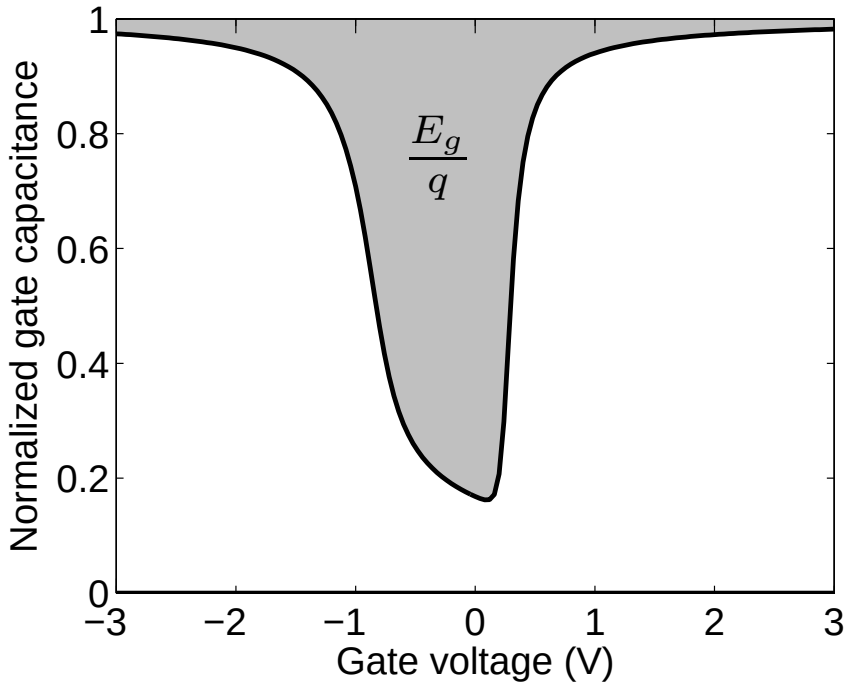


Figure 4.1: Illustration of the original Berglund relation in MOS capacitor. The area of the shaded region approximately equals $E_{\rm g}/q$.

benchmark during the development of analytic models of MOS devices.

4.2 Berglund Relation in LDMOS Transistors

In [114] (4.1) was obtained for a simple MOS capacitor in which the surface potential ψ_s is position independent. A simple analysis shows that (4.1) remains valid for a MOSFET with a laterally uniform channel as long as there is no drain bias, i.e. $V_{\rm DS} = 0$. For $V_{\rm DS} \neq 0$ quasi-equilibrium conditions do not apply and (4.1) with C changed into $C_{\rm GG}$ is not valid. Here we will show that for $V_{\rm DS} = 0$ the Berglund relation remains valid in the presence of lateral doping non-uniformity in the MOSFET channel. In fact, we consider the most extreme case of lateral non-uniformity–the LDMOS device [8, 43] where not only the doping may vary in the horizontal direction but $C_{\rm GG}$ includes

contributions from regions of opposite polarity (cf. Fig. 2.1). For this device the surface potential is position dependent even for $V_{\rm DS} = 0$ so we consider the gate capacitance $C_{\rm GG}$ as a parallel combination of N capacitors C_k and assume that (4.1) applies to each of them. For the sake of generality we do not assume $C_{\rm ox}$ to be the same and introduce $C_{{\rm ox}k}$ – the oxide capacitance for the k-th capacitor. Then

$$q \int (C_{{\rm ox}k} - C_k)\, dV_{\rm G} \approx C_{{\rm ox}k} E_{\rm g} \tag{4.2}$$

and after summation we recover (4.1) with

$$C = \sum_{k=1}^{N} C_k \tag{4.3}$$

and

$$C_{\rm ox} = \sum_{k=1}^{N} C_{{\rm ox}k}\,. \tag{4.4}$$

4.3 Verification with TCAD Simulations and Experimental Data

Despite the simplicity of this analysis it is confirmed by both TCAD simulations and experimental data from LDMOS transistors. Typical results are shown in Fig. 4.2. Since the oxide thickness is about 20 nm for the device of Fig. 4.2 surface quantization effects and gate leakage current are negligible. The polysilicon depletion effect can be seen in the experimental data but is small: $C(V_{\rm G})$ is reduced by 1-2%. The numerical value of the integral in (4.1) (from -8 V to $+8$ V with $C_{\rm ox}$ assigned the value of $C_{\rm GG}$ at $V_{\rm G} = -8$ V) is 1.1 V, for both the experimental and TCAD data, which is, indeed, close to $E_{\rm g}/q$. The TCAD data were generated for two different cases: laterally uniform and graded doping within the p-type and n-type regions. Comparison with the experimental data clearly shows that laterally non-uniform doping is

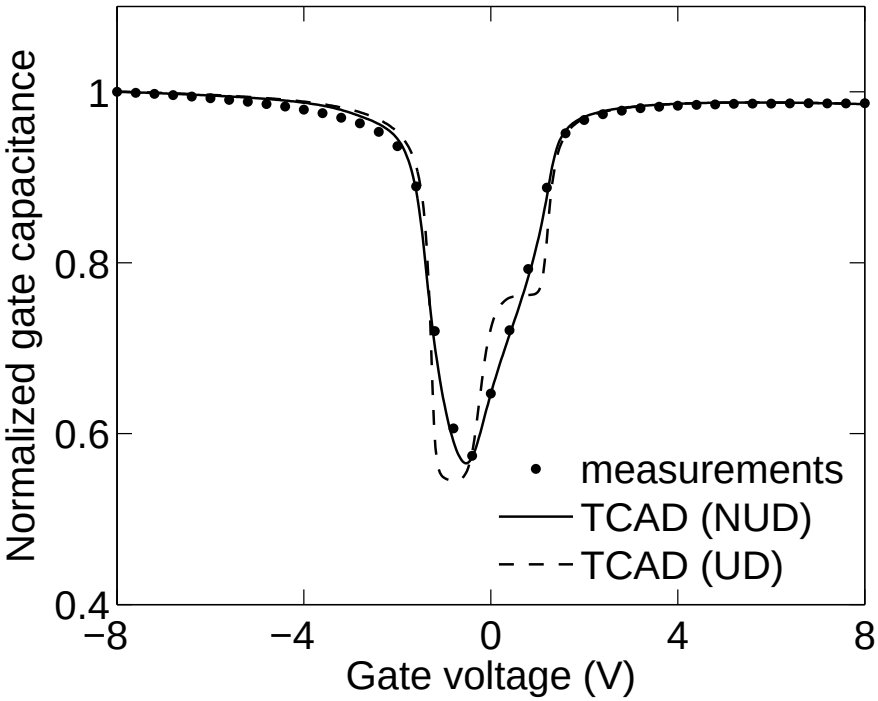


Figure 4.2: Normalized gate capacitance as a function of gate voltage.

present in this particular LDMOS transistor. The shape of the $C_{\mathrm{GG}}(V_{\mathrm{G}})$ curve for the non-uniformly doped device agrees with that in [43]. This, however, does not affect the validity of the Berglund relation.

Experimental data from devices with different structures (LDMOS or MOS), types (n or p), oxide thicknesses, widths, lengths, and number of fingers are used to verify the Berglund relation. Table 4.1 summarizes the results of the numerical integrations of the experimental data. The value ranges from 1.0 V to 1.2 V, which is close to the band gap of silicon, confirming the validity of the generalized Berglund relation in MOS devices.

4.4 Benchmarking of SP-HV with the Berglund Relation

The Berglund relation can also be used as a benchmark test of compact models of LDMOS transistors. The the normalized $C_{\mathrm{GG}}(V_{\mathrm{G}})$ curve simulated with a

T_{ox} (Å)	Device	W (μm)	L (μm)	N_G	$\int[1 - C/C_{ox}]dV_G$ (V)
300	nldsl65_C				1.02
	nldscale_0.77C				1.05
	nldscale_1.05C				1.14
200	nld10	1000		52	1.23
		500		26	1.21
		100		2	1.12
		10		2	1.12
	nld25	1000		32	1.11
		500		16	1.11
		100		2	1.15
		10		2	1.15
	nld65	200		2	1.00
		100		2	1.04
		80		10	1.08
		80		4	1.12
		20		2	1.04
		10		2	1.05
	pld45	1000		36	1.10
		500		18	1.10
		100		2	1.15
		10		2	1.16
140	nmv45	120	10.01		1.19
		120	1.26		1.12
		120	0.63		1.09
57	nmos	50	50		1.19
		50	0.56		1.09
		1.05	50		1.19

Table 4.1: Summary of numerical integration of experimental data from different devices.

compact model can be numerically integrated. The model passes the benchmarking test if the result is close to the theoretical value–E_g/q. Fig. 4.3 shows SP-HV fitting to the measured gate capacitance. The numerical integration of the modeled $C_{GG}(V_G)$ curve equals to 1.09 V. The close agreement to the theoretical value verifies the quality of the SP-HV model.

There is a "step" in the model result in Fig. 4.3, whereas the experimental data show a more gradual variation. This is because in the compact model

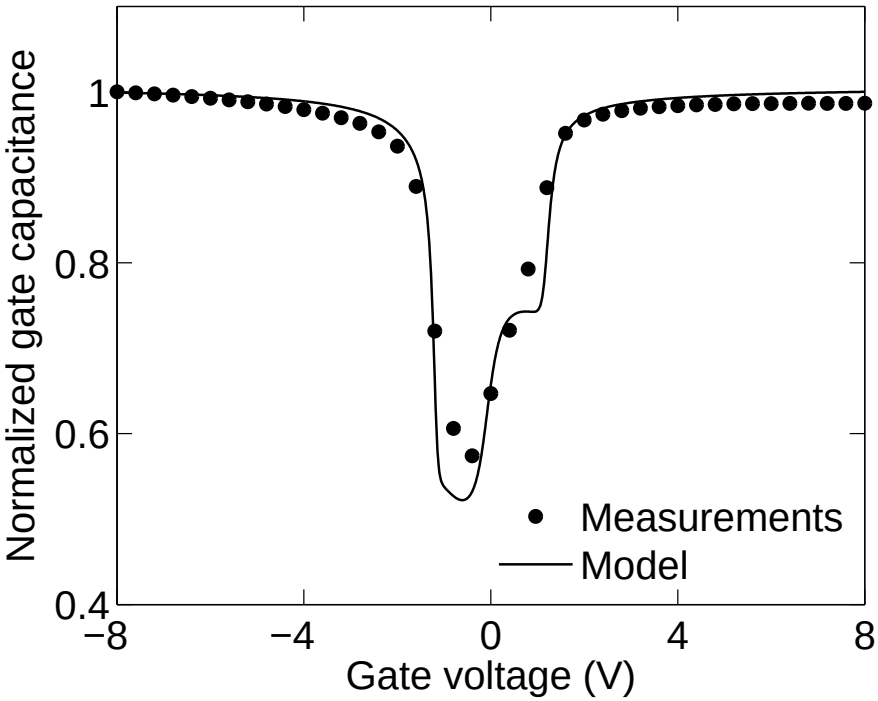


Figure 4.3: Normalized gate capacitance as a function of gate voltage.

we assume both the intrinsic channel and the drift region are doped uniformly whereas in the fabricated LDMOS transistor the doping variation is gradual. This is verified by the TCAD simulations in Fig. 4.2, in which the $C_{\mathrm{GG}}(V_{\mathrm{G}})$ curve in the uniform doping case shows a similar "step" as observed in compact model result whereas the $C_{\mathrm{GG}}(V_{\mathrm{G}})$ curve in the non-uniform doping case fits the measured data very well.

4.5 Summary

In this Chapter, the Berglund relation is extended to MOS devices with laterally non-uniform channel doping, including LDMOS transistors. It is verified extensively with TCAD simulations and experimental data. It is also used as a benchmark test for LDMOS compact models and SP-HV passes this test.

CHAPTER 5

SELF-HEATING MODEL

The self-heating effect in LDMOS transistors has been extensively studied since the devices are often used in high-voltage/high-current applications and it is also encountered during the parameter extraction process [21, 31, 37, 40, 53, 115–125]. Self-heating in SP-HV is modeled via an auxiliary thermal network [126]. The scalable thermal resistance and capacitance are simplified from Brodsky's model [127, 128].

5.1 Simplified Scalable Thermal Resistance and Capacitance

Brodsky's model has been developed to model self-heating effect in SOI MOSFETs [127]. A simplified version has been employed to address the bulk MOSFETs in the self-heating version of PSP [75]. Here the same simplification is adopted in SP-HV [51, 111].

Fig. 5.1 shows the simplified SOI MOSFET structure used for the thermal model derivation in [127, 128]. The structure parameters are defined in Table 5.1. The geometry dependent thermal resistance in [127] is given by (the notations are those of [127])

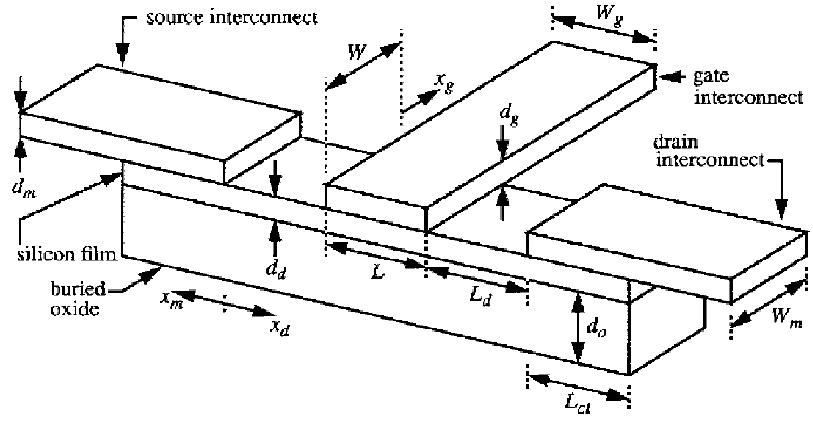
$$R_{\mathrm{TH}} = \left[\frac{2\sqrt{m_d} k_d d_d W \left(\mathrm{arg1} - \mathrm{arg2}\right)}{\mathrm{arg1} + \mathrm{arg2}} + \sqrt{m_g} k_g d_g W_g + h_d W L \right]^{-1} \tag{5.1}$$

in which

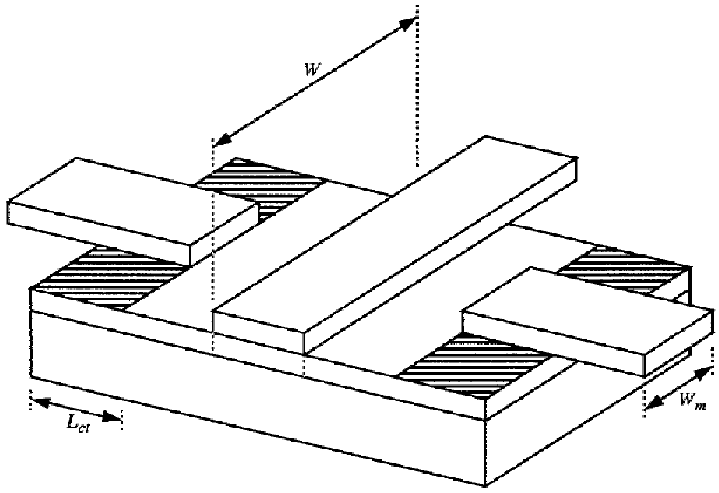
$$\mathrm{arg1} = e^{\sqrt{m_d} L_d} \left[\sqrt{m_d} k_d d_d W + h_d \left(W - W_m\right) L_{ct} + \sqrt{m_m} k_m d_m W_m \right] \tag{5.2}$$

$$\mathrm{arg1} = e^{-\sqrt{m_d} L_d} \left[\sqrt{m_d} k_d d_d W - h_d \left(W - W_m\right) L_{ct} - \sqrt{m_m} k_m d_m W_m \right] \tag{5.3}$$

where $m_i = h_i/(k_i d_i)$ is the square of the inverse characteristic thermal length in the respective cooling fin and $h_i = k_o/d_{io}$ is the heat transfer coefficient



(a)



(b)

Figure 5.1: (a) Simplified SOI MOSFET structure (not to scale), where $W \approx W_m$ used for the thermal model derivation. (b) Simplified SOI MOSFET structure (not to scale), where $W > W_m$,used for the thermal model derivation. After [127].

for that fin (d_{io} is the total thickness of the oxide between the fin and the substrate). The physical constants are listed in Table 5.2.

Examining (5.1), one can find that the last term can be approximately regarded as an "area" heat conducting component, which is proportional to ($W.L$); the first and second term can be considered as the "perimeter" components which are proportional to W and L, respectively; note that $L = W_g$ in Fig. 5.1(a). With these approximations, the geometry dependent thermal

Parameter	Definition
W	width of channel
W_m	width of drain/source interconnect
W_g	width of gate interconnect
L	length of channel
L_d	length between gate and drain/source contact
L_{ct}	length of drain/source contact opening
d_o	thickness of buried oxide
d_{go}	total thickness of oxide between gate interconnect and substrate
d_{mo}	total thickness of oxide between drain/source interconnect and substrate
d_d	thickness of silicon film
d_g	thickness of gate interconnect material
d_m	thickness of drain/source interconnect material
x_d	position along drain/source fin
x_g	position along gate interconnect fin
x_m	position along drain/source interconnect fin
T_d	temperature along x_d
T_g	temperature along x_g
T_m	temperature along x_m
T_0	temperature at buried oxide/substrate interface

Table 5.1: Parameters for the simplified device structure in Fig. 5.1. After [127].

conductance $G_{\rm TH} = 1/R_{\rm TH}$ is simplified to

$$G_{\rm TH} = (\mathbf{G_{TH0}} + \mathbf{G_W} \cdot W + \mathbf{G_L} \cdot L + \mathbf{G_{WL}} \cdot WL) \cdot (T_{\rm KR}/T_{\rm KD})^{\mathbf{ST_{GTH}}} \quad (5.4)$$

where $\mathbf{G_{TH0}}$, $\mathbf{G_W}$, $\mathbf{G_L}$, $\mathbf{G_{WL}}$, and $\mathbf{ST_{GTH}}$ are model parameters. $\mathbf{G_{TH0}}$ is introduced to improve the model flexibility and $\mathbf{ST_{GTH}}$ is used to describe the temperature dependence of the thermal resistance. Similarly, the scalable thermal capacitance is simplified to

$$C_{\rm TH} = \mathbf{C_{TH0}} + \mathbf{C_W} \cdot W + \mathbf{C_L} \cdot L + \mathbf{C_{WL}} \cdot WL \quad (5.5)$$

where $\mathbf{C_{TH0}}$, $\mathbf{C_W}$, $\mathbf{C_L}$, and $\mathbf{C_{WL}}$ are model parameters. In this work we concentrate on the static $I(V)$ characteristics so $C_{\rm TH}$ in Fig. 5.3 is included for the sake of completeness.

Parameter	Definition	Value
k_o	thermal conductivity of oxide	0.014 W/(cm·°C)
k_d	thermal conductivity of drain/source silicon film	0.63 W/(cm·°C)
k_m	thermal conductivity of drain/source interconnect material	2.39 W/(cm·°C)
k_g	thermal conductivity of gate interconnect material	2.39 W/(cm·°C)
ρ_o	density of oxide	2.19 g/cm^3
ρ_d	density of silicon film	2.328 g/cm^3
ρ_m	density of drain/source interconnect material	2.7 g/cm^3
ρ_g	density of gate interconnect material	2.7 g/cm^3
c_{po}	specific heat of oxide	1.4 J/(g·°C)
c_{pd}	specific heat of silicon film	0.7 J/(g·°C)
c_{pm}	specific heat of drain/source interconnect material	0.9 J/(g·°C)
c_{pg}	specific heat of gate interconnect material	0.9 J/(g·°C)

Table 5.2: Physical constants for self-heating model. After [127].

Fig. 5.2 shows the geometry dependent thermal resistance calculated by the original Brodsky's model given by (5.1) and the simplified model given by (5.4). The close agreement verifies that the simplified scalable thermal resistance provides sufficiently accuracy for the purpose of compact modeling.

5.2 Self-Heating Model

Fig. 5.3 shows the auxiliary thermal network, which is standard, used to model self-heating [126]. The voltage at the node $T_{\rm SH}$ describes the temperature rise from self-heating relative to the ambient temperature which is represented by ground in the thermal network. This temperature rise is fed back into the temperature dependence equations for the $I(V)$ model. The simulator then self-consistently solves for the device currents in the presence of self-

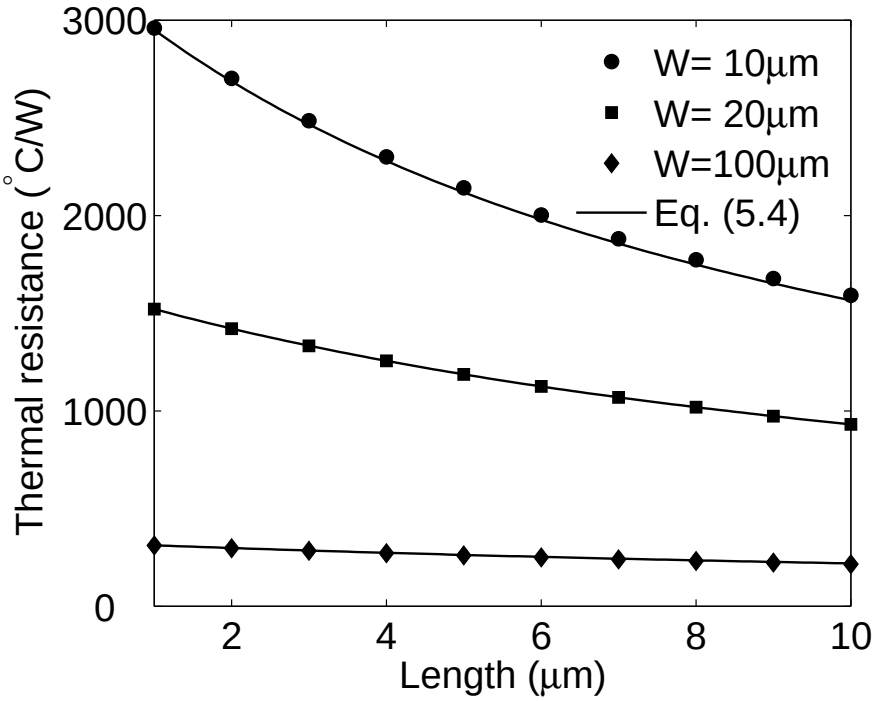


Figure 5.2: Comparison of thermal resistance as a function of device length for $W = 10$, 20 and 100 μm calculated by Brodsky's model given by (5.1) and by the simplified model given by (5.4).

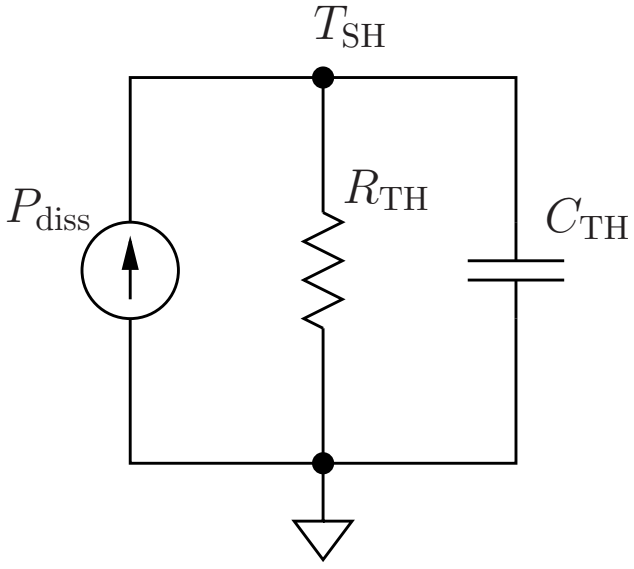


Figure 5.3: Auxiliary thermal network for self-heating model.

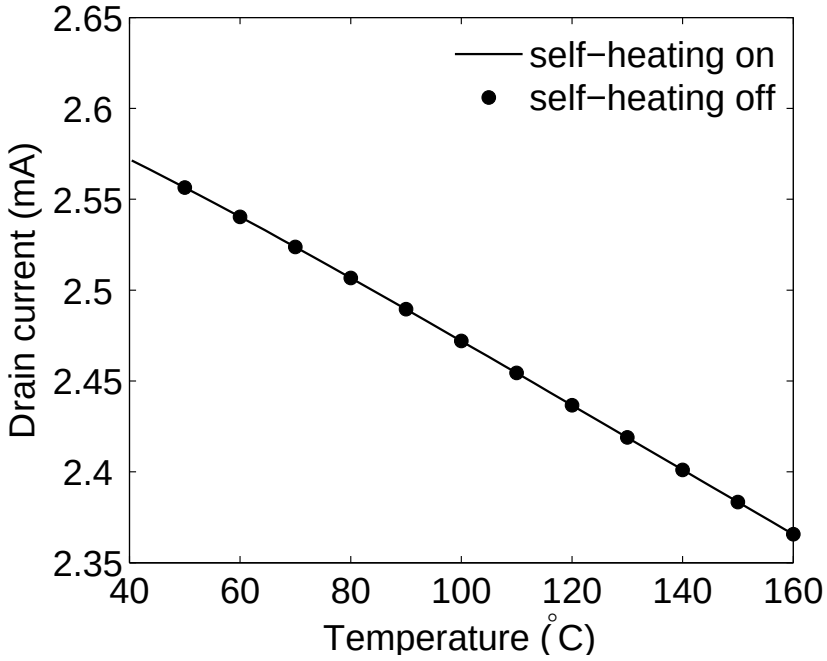


Figure 5.4: Benchmarking test results of self-heating model implementation in SP-HV.

heating [71]. The overall power dissipation P_{diss} is given by

$$P_{\text{diss}} = V_{\text{DI,S}} \cdot I_{\text{ch}} + V_{\text{D,DI}} \cdot I_{\text{dr}} + V_{\text{DI,B}} \cdot I_{\text{bn}} + V_{\text{DB}} \cdot I_{\text{bdr}} \tag{5.6}$$

The contribution from the drift region to the overall power dissipation is given by $V_{\text{D,DI}} \cdot I_{\text{dr}}$ and $V_{\text{DB}} \cdot I_{\text{bdr}}$ (cf. Fig. 2.2). In the next Chapter we will see that when the expansion effect takes place, the impact ionization terms ($V_{\text{DI,B}} \cdot I_{\text{bn}} + V_{\text{DB}} \cdot I_{\text{bdr}}$) are comparable to the power dissipation in the intrinsic MOS device and hence need to be included in the model. (cf. Figs. 6.7 and 6.8). In our TCAD simulations and experimental data the gate tunneling and junction leakage currents are negligible so are not included in the P_{diss} calculation.

The scalable self-heating model given by (5.4), (5.5), and Fig. 5.3 is implemented in the SP-HV model and a benchmark test is run to verify whether it has been implemented correctly [109, 129, 130]. Fig. 5.4 shows the results of

the benchmarking test. The test has been performed in two steps. In the first step, the self-heating model is turned off. The device temperature is swept and the drain current at a given bias condition is plotted as a function of temperature.In the second step, the self-heating model is turned on. The thermal resistance is swept and the drain current at the same bias condition is plotted against the device temperature, which is T_{SH} higher than the ambient temperature due to the self-heating effect. Fig. 5.4 shows that the drain currents in the two steps are exactly the same whether the device temperature is raised directly or it is raised by self-heating. This verifies that the self-heating model is correctly implemented in SP-HV.

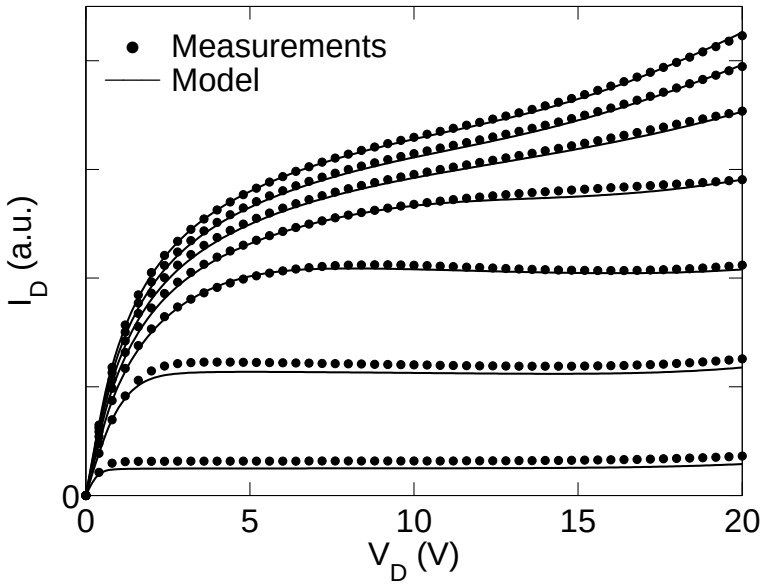
5.3 Model Verification with Experimental Data

The model is used to fit experimental data affected by self-heating. Fig. 5.5 shows the output characteristics of an LDMOS transistor. The negative output conductance, observed between the "dips" in the output conductance, is caused by self-heating.

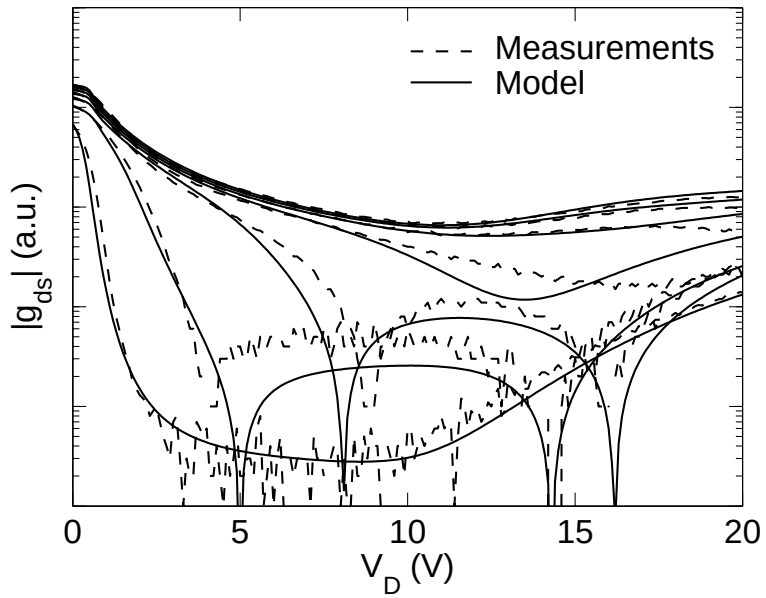
In this section, experimental data from a single device is used to verify the essential physics of the self-heating model. More detailed scalability verification will be performed in the next Chapter, where we will find that the interplay between self-heating and impact ionization in the drift region plays a key role in modeling the geometry dependent expansion effect.

5.4 Summary

In this Chapter, the scalable self-heating model in SP-HV is presented, benchmarked, and experimentally verified.



(a) $I_{\mathrm{D}}(V_{\mathrm{D}})$



(b) $g_{\mathrm{ds}}(V_{\mathrm{D}})$

Figure 5.5: Self-heating model verification with experimental data. $V_{\mathrm{G}} = 2$ V to 8 V by step of 1 V.

CHAPTER 6

MODELING OF IMPACT IONIZATION IN LDMOS TRANSISTORS

This chapter describes compact modeling of the impact ionization current in LDMOS transistors [52]. Depending on bias conditions, the impact ionization process in LDMOS transistors may occur primarily in the intrinsic MOSFET or in the drift region, leading to a "double-hump" substrate current behavior and enhanced drain current when both V_{G} and V_{D} are high. Impact ionization in the drift region also causes the "expansion" effect, which is modeled by making the drift region resistance a function of the impact ionization current in the same region. The new model is verified by comparison with TCAD simulations and experimental data. The width dependence of the expansion effect is captured through the interaction between the temperature dependence of impact ionization in the drift region and the geometry dependence of self-heating [52].

6.1 Impact Ionization in LDMOS Transistors

Depending on the bias conditions, impact ionization in LDMOS transistors occurs primarily either in the intrinsic MOSFET or in the drift region, leading to a "double-hump" characteristics in substrate current. The first and second increases in I_{B} are caused by the two impact ionization components, respectively [49, 50, 131, 132]. Since substrate current may trigger the parasitic bipolar device to turn on, and cause potential reliability issues related to hot electron injection [133, 134], it is critical for a compact LDMOS model to predict the substrate current accurately. An accurate model of the impact ionization current in the drift region is also a prerequisite for modeling the expansion effect.

The "expansion" effect [72, 77, 78, 135] in LDMOS transistors is a "step" increase in $I_{\rm D}(V_{\rm D})$ in saturation for sufficiently large gate biases. This effect was first observed experimentally in [77, 135] and investigated in detail through TCAD simulations in [78], which concluded that the expansion effect is caused by impact ionization in the drift region. A compact model of the expansion effect based on the drift region impact ionization current (denoted here as $I_{\rm bdr}$) was developed in [72]. The key aspect of the model in [72] is that the increase of the drain current is caused by an increase in $I_{\rm bdr}$ which in turn causes the source-substrate junction of the intrinsic MOSFET to become forward biased. The model in [72] has been calibrated versus TCAD simulations but not compared with experimental data for devices exhibiting the expansion effect. The expansion effect was also modeled in [136] with a current source controlled by the electric field in the drift region. Details such as how the electric field is computed, comparison with TCAD simulations, or experimental verification have not been presented. Thus at present the expansion effect is observed experimentally, reasonably well understood physically, and two approaches to its inclusion into compact LDMOS models have been suggested but not experimentally verified.

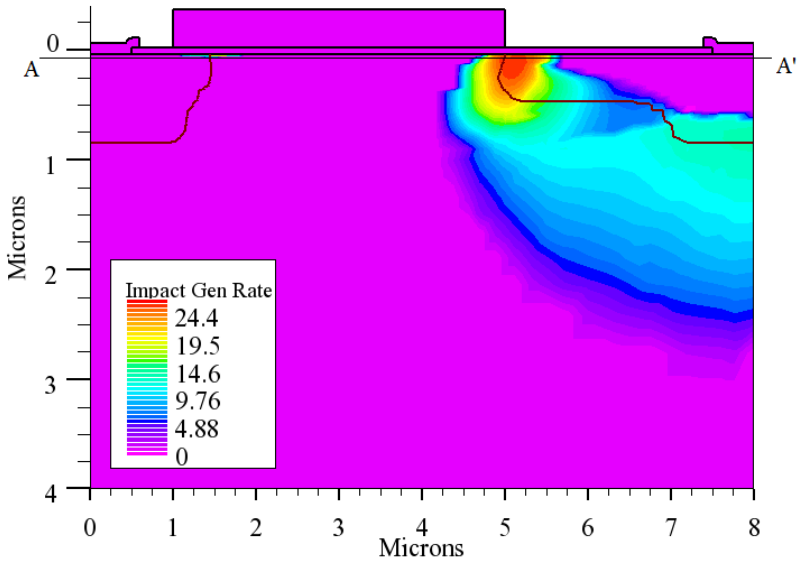
The purpose of this work is to provide an experimentally verified physics-based compact model of impact ionization in LDMOS transistors. This chapter proceeds as follows. First, impact ionization in the drift region is investigated and a new compact model of impact ionization in the drift region is presented and verified. Then we describe a compact model of the expansion effect and verify it by comparison to both TCAD simulations and experimental data. In particular, the interplay between the expansion and self-heating effects is investigated experimentally and reproduced by the new model. To the best of our knowledge, this represents the first analysis of the interaction between

impact ionization and self-heating as a function of LDMOS geometry.

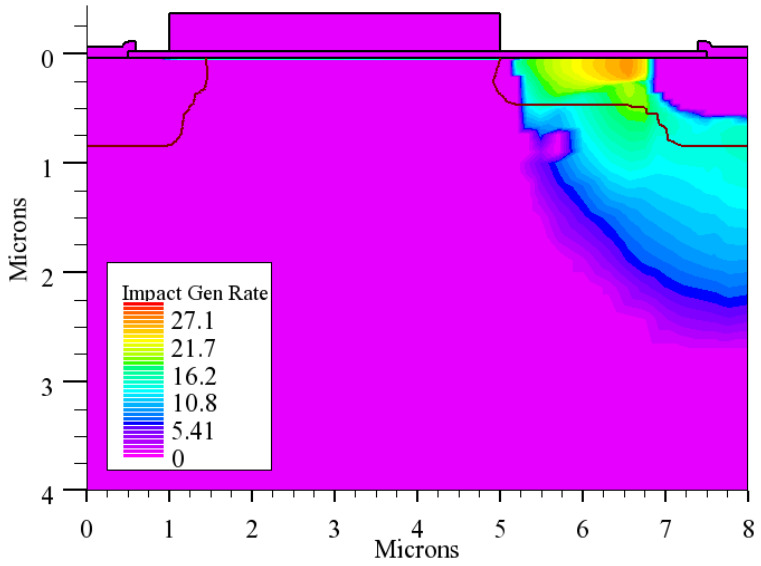
Two-dimensional TCAD simulations show that depending on bias conditions, the peak impact ionization occurs either in the intrinsic MOSFET, near the p-substrate/n-drift junction, or in the drift region, near the n-drift/n^+-diffusion junction, as shown in Fig. 6.1 [49, 50].

At low V_{G} the maximum impact ionization occurs in the intrinsic MOSFET near the p-substrate to n-drift junction. This impact ionization component is similar to that in a conventional MOSFET; it causes the first peak in the $I_{\mathrm{B}}(V_{\mathrm{G}})$ curve. At high V_{G}, impact ionization primarily occurs in the drift region near the n^+ drain diffusion region and results in the second increase in the $I_{\mathrm{B}}(V_{\mathrm{G}})$ curve.

Fig. 6.2 shows the lateral electric field at three different gate biases along the cut-line AA' in Fig. 6.1(a). It clearly shows the shift of the maximum field position with V_{G}. Physically, the impact ionization generation rate increases with electric field and it is proportional to the current density. At low $V_{\mathrm{G}}(= 4$ V), the intrinsic MOSFET dominates and the maximum potential variation occurs at the p-substrate/n-drift junction [cf. Fig. 6.2(b)], and the maximum lateral electric field and impact ionization generation rate locate in this region. When V_{G} increases, the resistance of the intrinsic MOSFET goes down and the device is gradually taken over by the drift region and large portion of potential variation takes place in the drift region. At high $V_{\mathrm{G}}(= 20$ V), the device is dominated by the drift region. The maximum potential variation occurs in the drift region close to the n^+-diffusion, and the maximum lateral electric field and impact ionization generation rate occur at the same place.

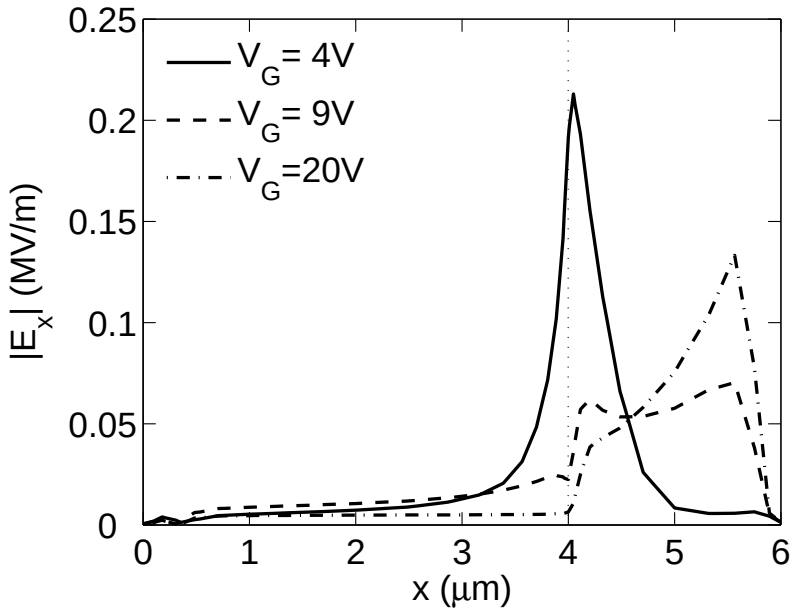


(a) Impact ionization generation rate distribution at $V_{\mathrm{D}} = 15$ V and $V_{\mathrm{G}} = 4$ V.

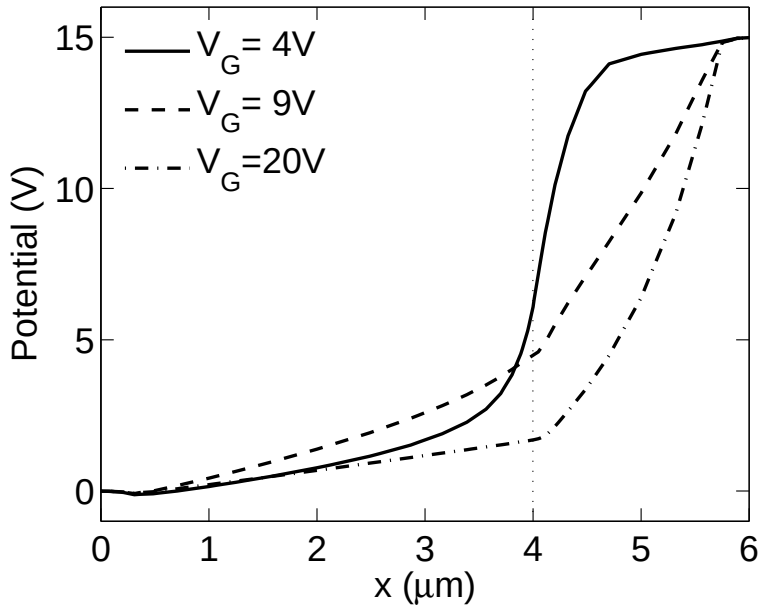


(b) Impact ionization generation rate distribution at $V_{\mathrm{D}} = 15$ V and $V_{\mathrm{G}} = 20$ V.

Figure 6.1: Distribution of the impact ionization generation rate in the LDMOS simulated by ATLAS. (a)At bias condition $V_{\mathrm{D}} = 15$ V, $V_{\mathrm{G}} = 4$ V and $V_{\mathrm{B}} = V_{\mathrm{S}} = 0$ V, the maximum impact ionization generation rate occurs at the pinch-off region near the p-substrate/n-drift junction. (b)At bias condition $V_{\mathrm{D}} = 15$ V, $V_{\mathrm{G}} = 20$ V and $V_{\mathrm{B}} = V_{\mathrm{S}} = 0$ V, the location of the maximum impact ionization generation rate is in the drift region near the n-drift/n^{+}-diffusion junction.



(a) $|E_{\mathrm{x}}|$



(b) Potential

Figure 6.2: Lateral electrical field and potential variation along cut-line AA' in Fig. 6.1(a). $V_{\mathrm{S}} = V_{\mathrm{B}} = 0$, $V_{\mathrm{D}} = 15$ V, and V_{G} =4, 9, and 20 V. The boundary between the intrinsic MOSFET and the drift region is located at $x = 4$ μm.

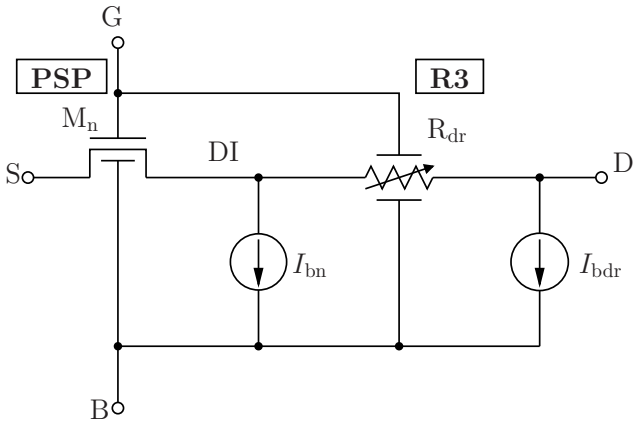


Figure 6.3: Equivalent circuit of the SP-HV model, which is the same as in Fig. 2.2. Repeated here for convenience.

6.2 Compact Model of Impact Ionization in the Drift Region

To physically describe these phenomena, two current sources I_{bn} and I_{bdr} are implemented to model the impact ionization components in the intrinsic MOSFET and in the drift region, respectively (cf. Fig. 6.3). The current source I_{bn} is included in the compact model of the transistor $\mathrm{M_n}$ [74, 137]. The impact ionization current I_{bdr} in the drift region is modeled as follows [138, 139]:

$$I_{\mathrm{bdr}} = a_{\mathrm{dr1}} \cdot E_{\mathrm{dr}} \cdot I_{\mathrm{DS}} \cdot \exp\left(-a_{\mathrm{dr2}}/E_{\mathrm{dr}}\right) , \tag{6.1}$$

where

$$a_{\mathrm{dr1}} = \mathbf{A_{DR1}} \cdot \left[1 + \mathbf{A_{DR4}} \cdot \left(\sqrt{V_{\mathrm{SB}} + \phi_{\mathrm{B}}} - \sqrt{\phi_{\mathrm{B}}}\right)\right] , \tag{6.2}$$

$$a_{\mathrm{dr2}} = \mathbf{A_{DR2}} \cdot \left(T_{\mathrm{KD}}/T_{\mathrm{KR}}\right)^{\mathbf{ST_{ADR2}}} , \tag{6.3}$$

$$E_{\mathrm{dr}} = \left(V_{\mathrm{DB}} - a_{\mathrm{dr3}} \cdot V_{\mathrm{DI,B}}\right)/L_{\mathrm{dr2}} , \tag{6.4}$$

and

$$a_{\mathrm{dr3}} = \mathbf{A_{DR3}} \cdot \left[1 + \mathbf{A_{DR5}} \cdot \left(\sqrt{V_{\mathrm{SB}} + \phi_{\mathrm{B}}} - \sqrt{\phi_{\mathrm{B}}}\right)\right] . \tag{6.5}$$

E_{dr} is the average electric field in the drift region and $\mathbf{A_{DR1}}$ through $\mathbf{A_{DR5}}$ are model parameters. The parameter $\mathbf{ST_{ADR2}}$ models the temperature dependence, and T_{KD} and T_{KR} are the device temperature and the reference

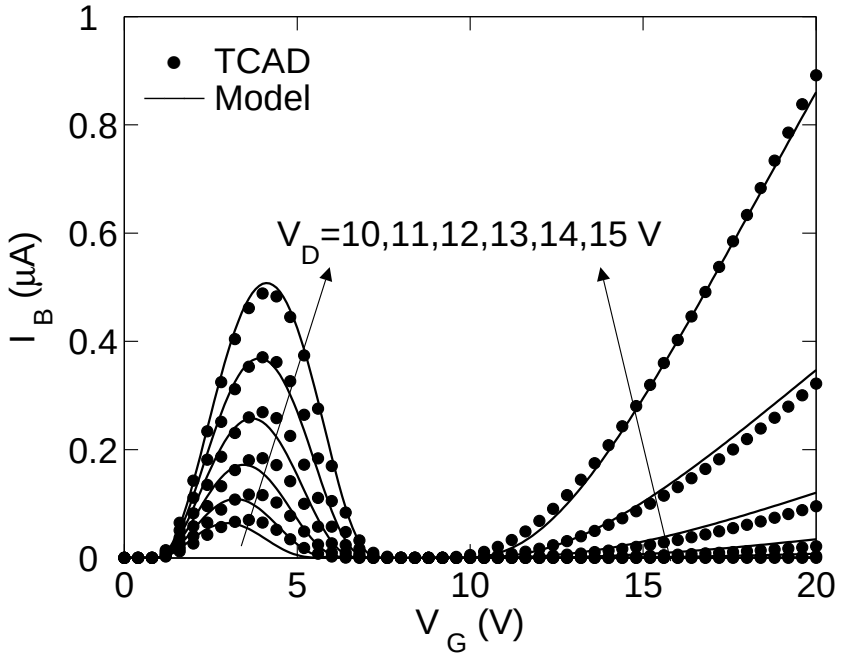
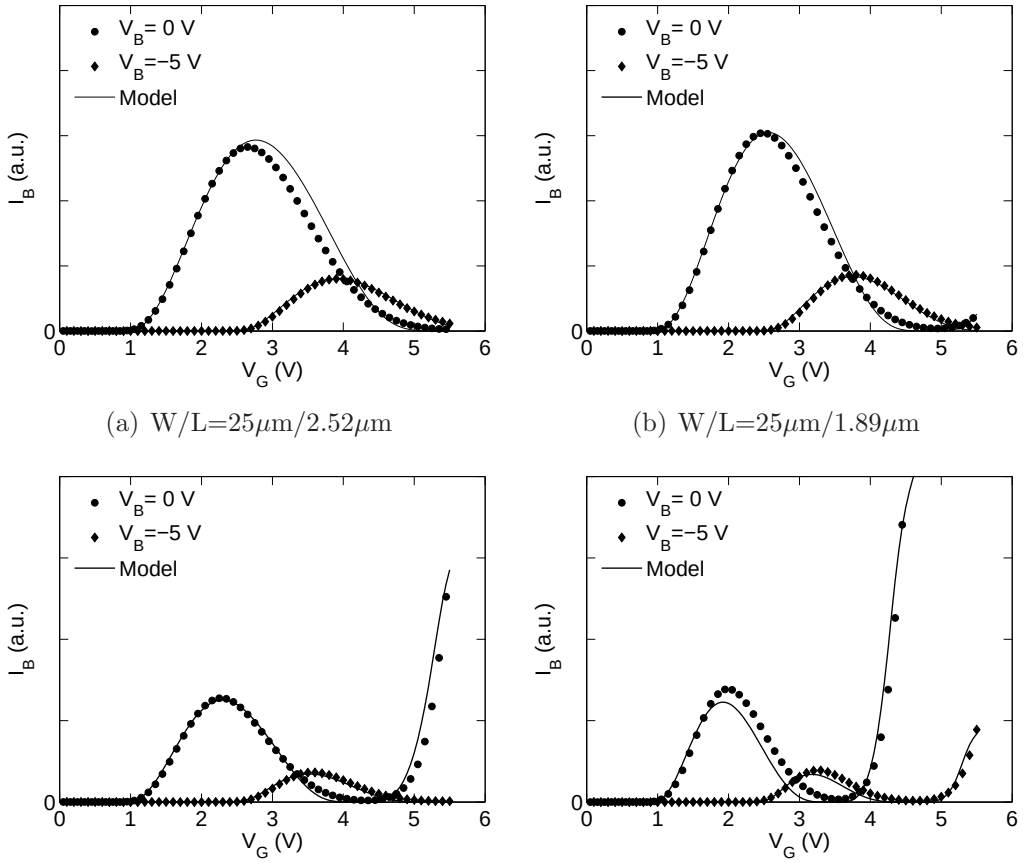


Figure 6.4: TCAD verification of the substrate current as a function of gate bias at different drain biases. $V_{\rm D} = 10, 11, 12, 13, 14, 15$ V, $V_{\rm B} = 0$.

temperature, respectively. The parameters $\mathbf{A_{DR4}}$ and $\mathbf{A_{DR5}}$ are introduced to empirically model the body-bias dependence. Note that the $I_{\rm B}$ dependence on $V_{\rm G}$ is included through $I_{\rm DS}$ and $V_{\rm DI,B}$. The expression (6.1) for $I_{\rm bdr}$ is similar to that used in [74] for $I_{\rm bn}$ and is conceptually based on [138]. The essential difference is that $E_{\rm dr}$ is used to reflect the fact that $I_{\rm bdr}$ is generated in the drift region.

6.3 Model Verification

The impact ionization model in Fig. 6.3 is verified against both TCAD simulations and measurement data. Fig. 6.4 shows TCAD simulation of $I_{\rm B}$ as a function of $V_{\rm G}$ for different drain voltages. At low $V_{\rm G}$, the maximum impact ionization occurs in the intrinsic MOSFET. This impact ionization process causes the peak in the $I_{\rm B}(V_{\rm G})$ curves, which is modeled by $I_{\rm bn}$. At high $V_{\rm G}$,



(a) W/L=25μm/2.52μm

(b) W/L=25μm/1.89μm

(c) W/L=25μm/1.26μm

(d) W/L=25μm/0.63μm

Figure 6.5: Experimental verification of the experimental data for devices with different intrinsic channel lengths. In all cases $L_{\rm dr1} = 1.05$ μm, $L_{\rm dr2} = 2.38$ μm, and $V_{\rm D} = 20$ V.

impact ionization in the drift region dominates and causes the second hump (i.e. increase) in the substrate current, which is modeled by $I_{\rm bdr}$ given by (6.1). Fig. 6.4 shows that the model captures both impact ionization components and accurately reproduces the $I_{\rm B}(V_{\rm G}, V_{\rm D})$ dependence.

The model is also verified against experimental data. Fig. 6.5 shows $I_{\rm B}(V_{\rm G})$ curves for devices with different intrinsic MOSFET lengths. The shortest device, $L = 0.63\mu$m, shows the most significant double-hump shape while the longest device, $L = 2.52\mu$m, shows almost no second hump. Long devices show less significant LDMOS effects than short devices because their drift

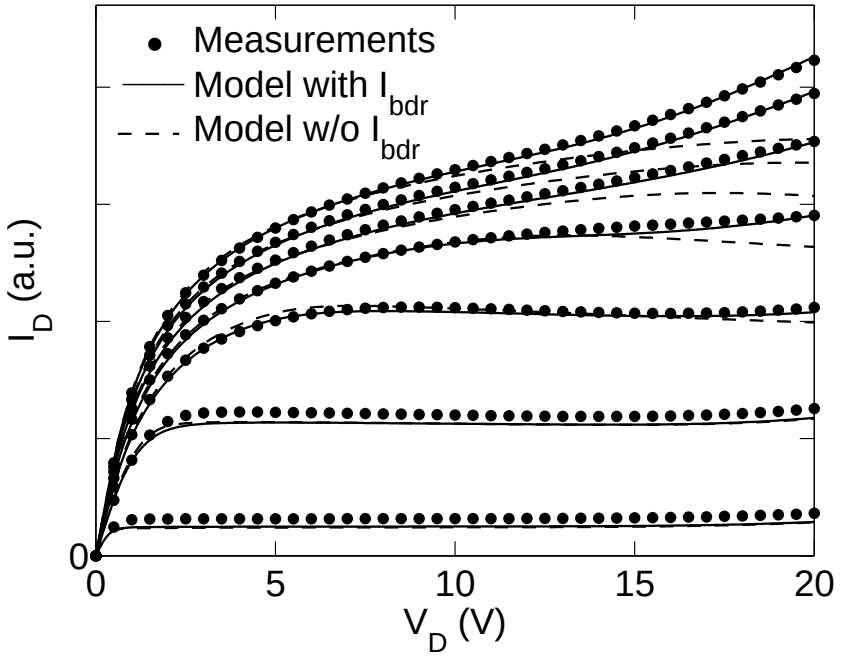


Figure 6.6: Measurement verification of the output characteristics. The device geometry is $W/L = 60\mu\text{m}/0.75\mu\text{m}$, $L_{\text{dr1}} = 0.42\mu\text{m}$, $L_{\text{dr2}} = 1.5\mu\text{m}$. $V_{\text{D}} = V_{\text{B}} = 0\text{V}$, $V_{\text{G}} = 1\text{V}$ to 8V with a step of 1V. Symbols: measurements; solid lines: model with impact ionization in the drift region; dashed lines: model without impact ionization in the drift region.

region resistance is relatively smaller compared to the resistance of the intrinsic MOSFET. Fig. 6.5 shows that the $I_{\text{B}}(V_{\text{G}})$ characteristics, together with their length scaling, are well captured by the model.

Accurate modeling of I_{B} also enables accurate modeling of the increase in output conductance for high V_{D} and high V_{G}. Fig. 6.6 shows fitting of experimental output characteristics of an LDMOS transistor; model results with and without I_{bdr} are shown. (Model output without I_{bdr} is obtained by setting $\mathbf{A_{DR1}} = 0$.) The significant improvement in fitting when impact ionization in the drift region is taken into account is apparent.

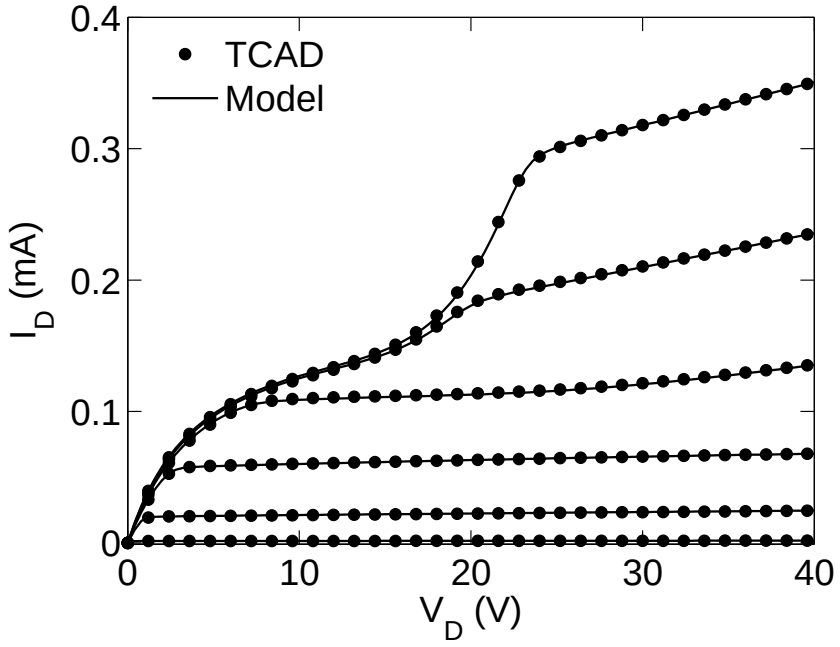
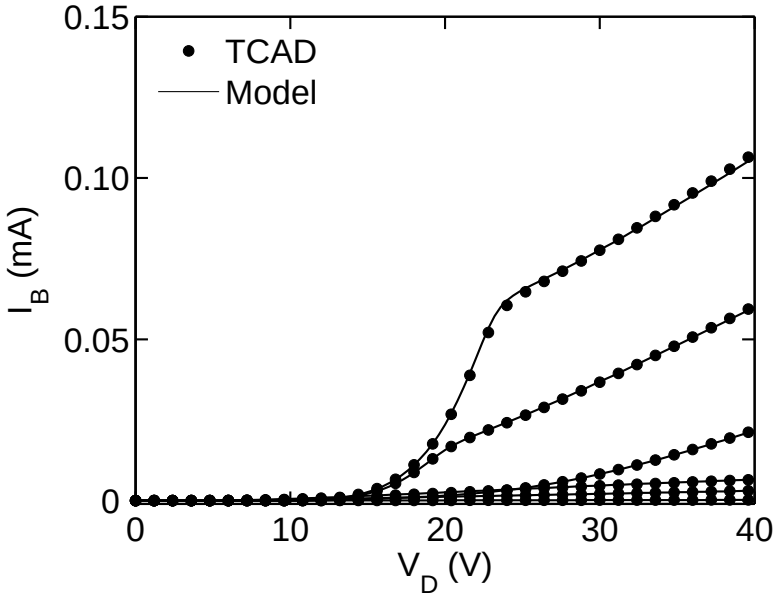


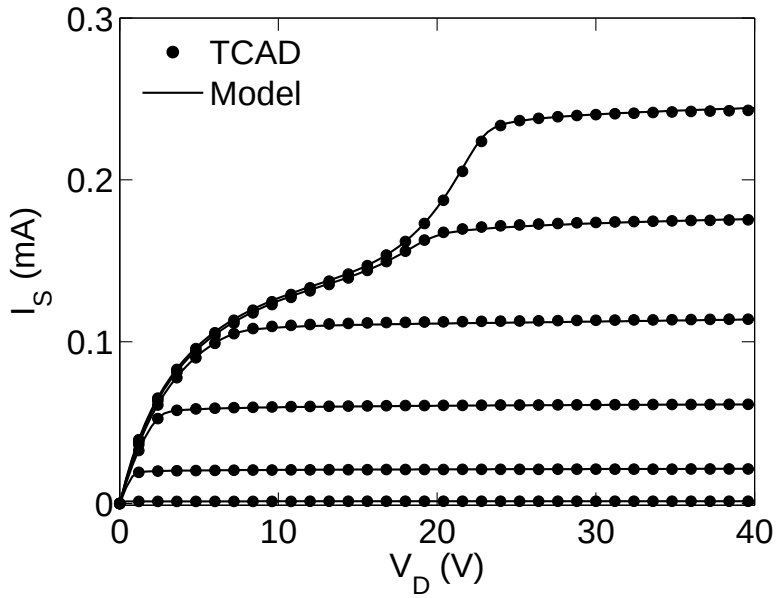
Figure 6.7: TCAD verification of the drain current as a function of drain voltage at different gate biases. V_{G} varies from 2 V to 7 V with a step of 1 V and $V_{\mathrm{S}} = V_{\mathrm{B}} = 0$.

6.4 Expansion Effect in LDMOS Transistors

Another interesting phenomenon in LDMOS transistors is the "expansion" effect, the "step" increase in $I_{\mathrm{D}}(V_{\mathrm{D}})$ for sufficiently large gate biases. Fig. 6.7 shows output characteristics from 2D TCAD simulation in which the expansion effect can be observed. The TCAD simulations used the drift-diffusion model and the new University of Bologna impact ionization model [140]. In Fig. 6.7, quasi-saturation is clearly visible for $V_{\mathrm{G}} > 5$ V and $V_{\mathrm{D}} < 20$ V. Physically, this is caused by the reduction of the intrinsic MOSFET channel resistance for high V_{G}, hence the overall device resistance becomes dominated by the drift region resistance and becomes relatively independent of the intrinsic channel resistance. This causes the reduced gate bias dependence of drain current at high V_{G} and low $V_{\mathrm{D}}(< 20$ V).

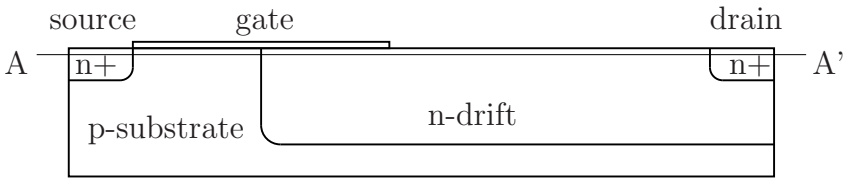


(a) $I_{\mathrm{B}}(V_{\mathrm{D}})$

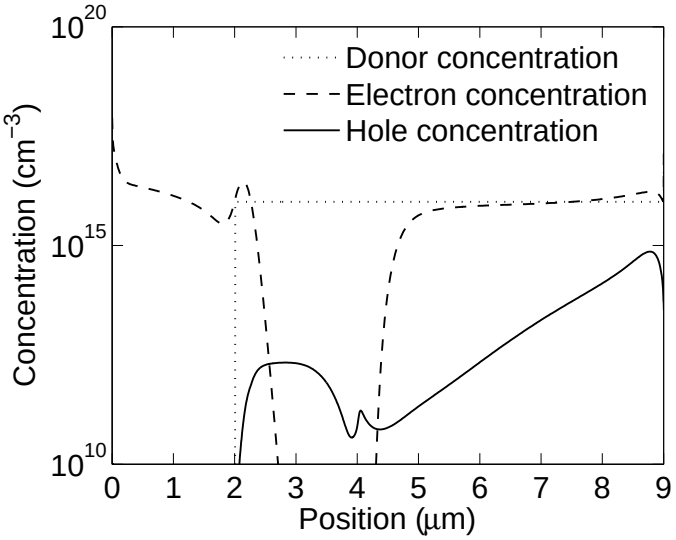


(b) $I_{\mathrm{S}}(V_{\mathrm{D}})$

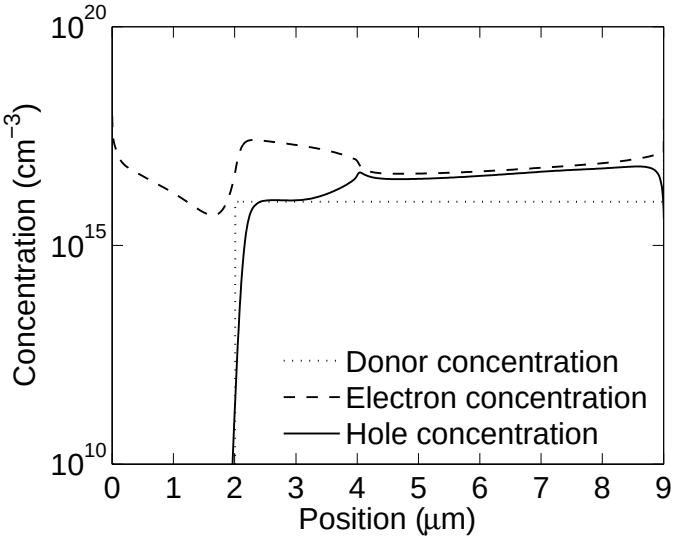
Figure 6.8: TCAD verification of body current and source current as a function of drain voltage at different gate voltages. The bias condition is the same as Fig. 6.7.



(a) Cross section of the LDMOS transistor for TCAD simulation



(b) $V_{\mathrm{G}} = 2$ V and $V_{\mathrm{D}} = 40$ V



(c) $V_{\mathrm{G}} = 7$ V and $V_{\mathrm{D}} = 40$ V

Figure 6.9: Cross section of the LDMOS device used in TCAD simulation. Cut-lines along the line A-A' of the carrier concentration and donor doping concentration at two different bias conditions.

For high V_G and $V_D > 20$ V, the drain current shows a rapid increase, which is caused by impact ionization in the drift region as described in the previous Section.

As V_D increases above 25 V the drain current again saturates. This "step" in $I_D(V_D)$ takes place simultaneously with a rapid increase in substrate current, see Fig. 6.8(a). However, the I_D increase is not caused simply by the addition of the substrate current since, as Fig. 6.8(b) shows, the source current increases as well. Thus there is more to the expansion effect than just the direct increase in impact ionization in the drift region.

Comparison of TCAD simulations of the electron and hole concentrations for $V_D = 40$ V and $V_G = 2$ and 7 V in Fig. 6.9 shows that when both V_D and V_G are high the electron and hole concentrations in the drift regions increases dramatically and assume values well in excess of the donor concentration. This was first demonstrated in [78] and implies that the impact ionization in the drift region not only increases the substrate current but also reduces the drift region resistance by increasing the carrier concentration (cf. Fig. 6.9). When this happens the overall LDMOS device behavior approaches that of the intrinsic MOSFET. More precisely, once the expansion effect takes place, I_D exceeds the value expected for the intrinsic device alone due to the contribution of the substrate current associated with the impact ionization in the drift region. This is the essential physics of the expansion effect that needs to be included in a simplified manner in an LDMOS compact model.

In [72], the increase of the source current was explained by the forward biasing of bulk-to-source junction caused by the bulk current, which is unfortunately inexact. As a result, the expansion effect submodel based on this explanation is unphysical. A series of TCAD simulations have been run to check the explanations about the I_S increase at high V_D in this work and

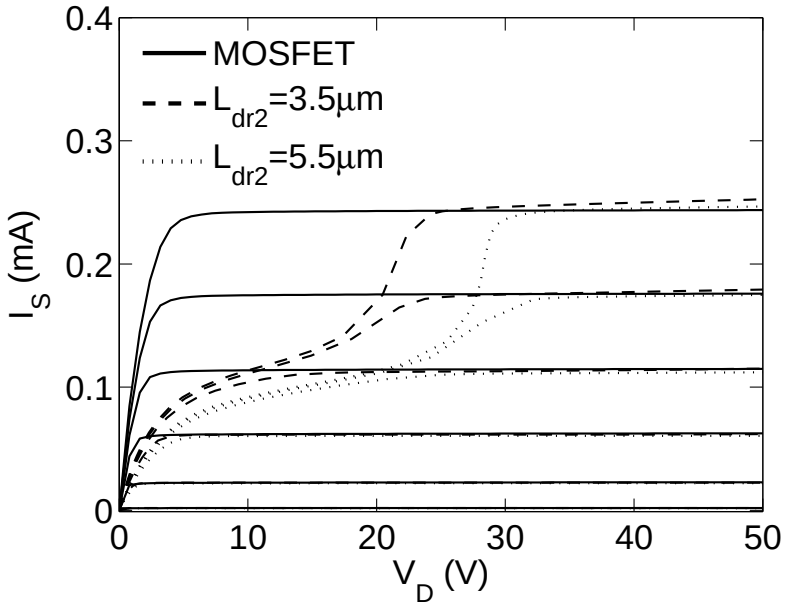
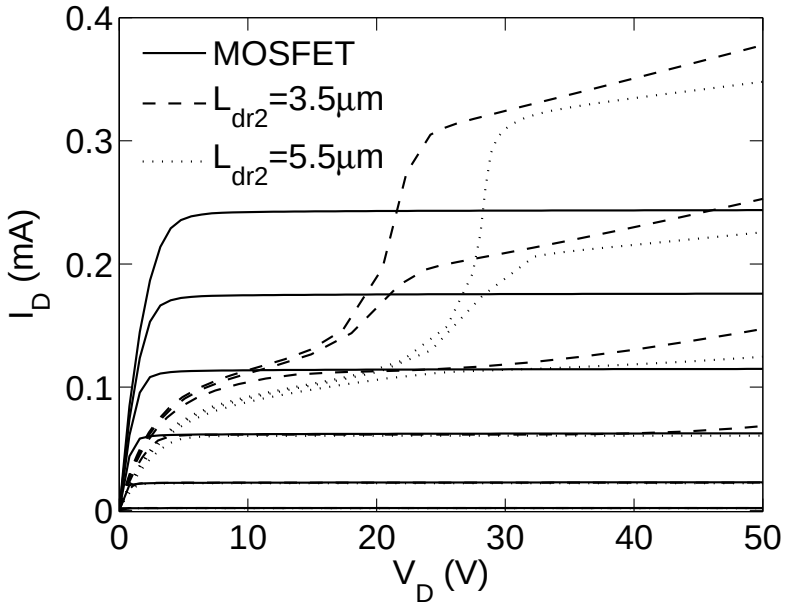


Figure 6.10: Source current simulated with three devices structures. $V_{\rm G}$ varies from 2 V to 7 V with a step of 1 V and $V_{\rm S} = V_{\rm B} = 0$. $T_{\rm ox} = 25$ nm, $L_{\rm ch} = 1$ μm, $L_{\rm dr1} = 1$ μm, $N_{\rm ch} = 2 \times 10^{17}$ cm^{-3}.

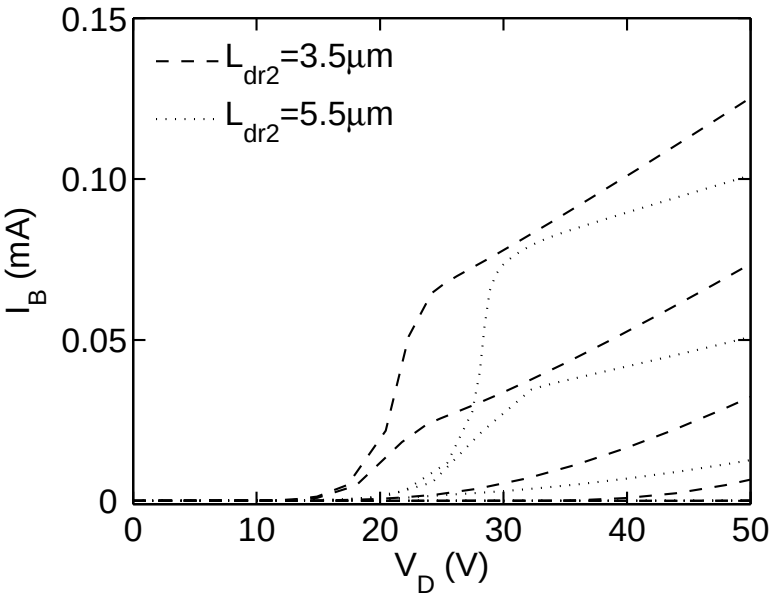
in [72]. Three device structures are used in TCAD simulations. Two structures are LDMOS transistors with different lengths of the second drift region and the other one is the intrinsic MOSFET. The source, drain, and substrate current are shown in Figs. 6.10 and 6.11.

One can find that the source currents from all three structures are almost equal to one another at high $V_{\rm D}$ when the LDMOS works in the "expansion" regime. This observation suggests that it might be better to call this phenomenon the "recovery" effect because the intrinsic MOSFET behavior is recovered in this region. This result also shows that the body-biasing effect is insignificant and should not be used as the explanation for the $I_{\rm S}$ increase when the LDMOS transistor works at the transition from quasi-saturation to expansion regions.

Another set of TCAD simulation has been run with different substrate



(a) $I_{\mathrm{D}}(V_{\mathrm{D}})$



(b) $I_{\mathrm{B}}(V_{\mathrm{D}})$

Figure 6.11: Drain and body currents simulated with three devices structures. Device structure parameters and bias conditions are the same as those in Fig. 6.10.

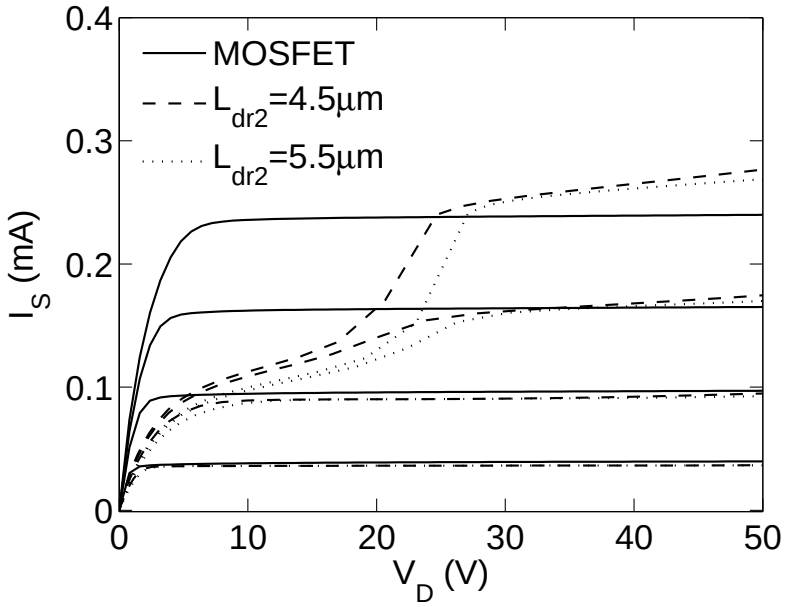
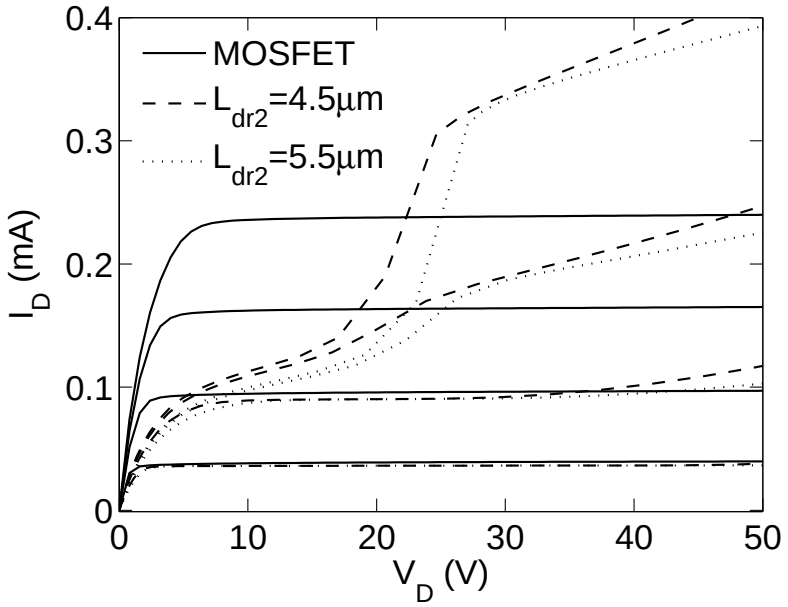


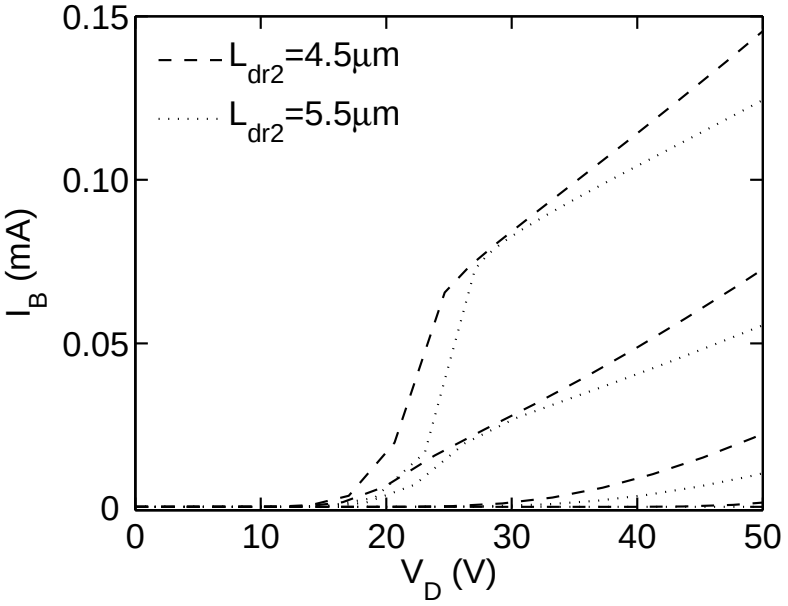
Figure 6.12: Source current simulated with three devices structures. $V_{\rm G}$ varies from 2 V to 5 V with a step of 1 V and $V_{\rm S} = V_{\rm B} = 0$. $T_{\rm ox} = 25$ nm, $L_{\rm ch} = 1$ μm, $L_{\rm dr1} = 1$ μm, $N_{\rm ch} = 5 \times 10^{16}$ cm^{-3}.

doping. The substrate doping concentration has been reduced so that the body biasing effect should be more significant. Figs. 6.12 and 6.13 shows the results. The effect of body biasing is more pronounced and it raises the channel current above the current of the intrinsic MOSFET. The results also show clearly the region where the body biasing effect is pronounced–the "expansion" region. Therefore it is improper to account for the channel current increase before the device reaches expansion region as has been done in [72].

An interesting aspect of the TCAD simulations concerns the substrate current variation with drain bias in Fig. 6.8(a). On the $I_{\rm B}(V_{\rm D})$ curve for $V_{\rm G} = 7$ V (the top curve) there is a distinct change from the rapid (approximately exponential) variation of $I_{\rm B}$ with $V_{\rm D}$ to a slower variation after $V_{\rm D}$ reaches 25 V. This effect (previously observed in TCAD simulations in [72, 78]) is caused by the saturation of the drain current in the intrinsic MOSFET and is auto-



(a) $I_{\mathrm{D}}(V_{\mathrm{D}})$



(b) $I_{\mathrm{B}}(V_{\mathrm{D}})$

Figure 6.13: Drain and body currents simulated with three devices structures. Device structure parameters and bias conditions are the same as those in Fig. 6.12.

matically included in the proposed model without any additional parameters. Experimental data for $I_{\rm B}$ are not available since the body is connected to the source in the manufactured LDMOS devices which show the expansion effect.

6.5 Compact Modeling of the Expansion Effect

The expansion effect is modeled by modulation of $R_{\rm dr}$ (the resistance of the drift region) by the impact ionization current $I_{\rm bdr}$. Physically, this represents a modulation of the drift region conductance described in [78] and illustrated in Fig. 6.9. Empirically we have found that we can model of this effect via

$$R_{\rm dr} = \frac{1}{g_{\rm eff} + \mathbf{B_1} \cdot I_{\rm bdr} + \mathbf{B_2} \cdot I_{\rm bdr}^2} \tag{6.6}$$

where $g_{\rm eff}$ denotes the effective conductance of the drift region in the absence of impact ionization and the next two terms introduce the modulation effect described above. $\mathbf{B_1}$ and $\mathbf{B_2}$ are (non-negative) model parameters that are extracted by comparison with experimental data or TCAD simulations. $\mathbf{B_1}$ is scalable:

$$\mathbf{B_1} = \mathbf{B_{1O}} + \frac{\mathbf{B_{1L}}}{L_{\rm dr2}} + \frac{\mathbf{B_{1W}}}{W_{\rm dr2}}\,, \tag{6.7}$$

where $\mathbf{B_{1O}}$, $\mathbf{B_{1L}}$ and $\mathbf{B_{1W}}$ are scaling parameters. Analysis of the experimental data available at this time shows no need to scale $\mathbf{B_2}$ with device geometry. The dependence of $I_{\rm bdr}$ on $I_{\rm DS}$, which in turn is affected by $I_{\rm bdr}$, is handled iteratively by the circuit simulator.

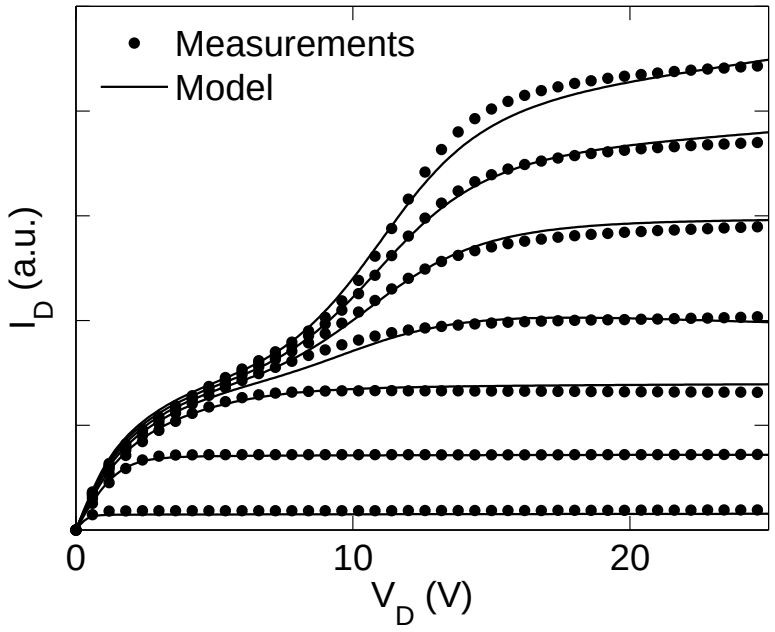
TCAD verification of the proposed model of the expansion effect is illustrated in Fig. 6.7 for a fixed device geometry. Note that in Fig. 6.8(a) $I_{\rm B} = I_{\rm bn} + I_{\rm bdr}$ was fitted using equations for $I_{\rm bn}$ from [75] and $I_{\rm bdr}$ given by (6.1). The results presented in Fig. 6.7 are representative of numerous TCAD simulations and confirm the validity of the expansion effect modeling based on the equivalent circuit of Fig. 6.3 and equation (6.6).

One advantage of TCAD simulation is that effects like self-heating can be turned off to simplify compact model verification. This was done for the simulations in Figs. 6.7 and 6.8. For the experimental data that show the expansion effect (where both I_{D} and V_{D} are high), self-heating is usually present and cannot be turned off. Hence any comparison of a compact model with experimental data is possible only after self-heating is modeled. In the present investigation we use the scalable self-heating model introduced in Chapter 5.

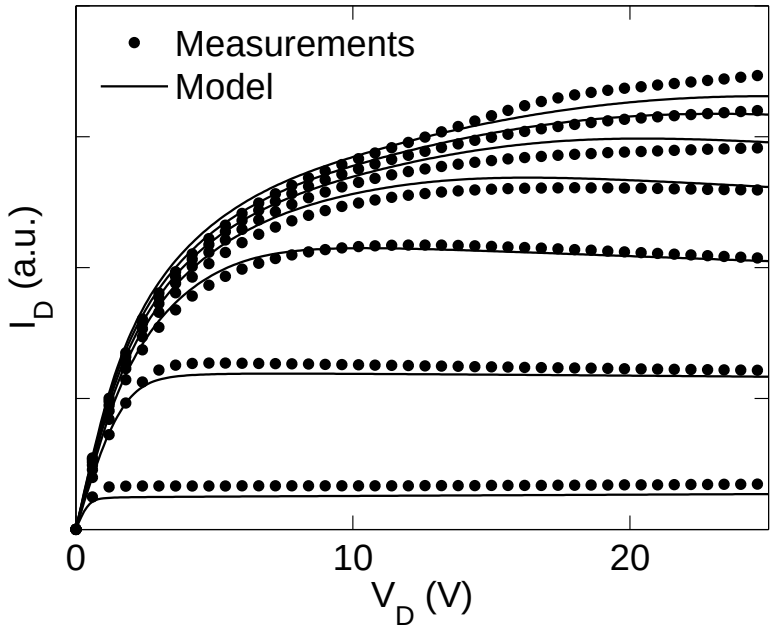
6.6 Model Verification

Figs. 6.14 and 6.15 compares the new model with experimental data for LDMOS transistors with different widths. Good agreement is achieved in all cases and the data illustrate the role of self-heating in the analysis of the expansion effect. Heat removal for the narrow device ($W = 3$ μm) is more efficient than heat removal for the wide devices, because the narrow device has a relatively larger perimeter component of the thermal conductance. Consequently, the self-heating is relatively smaller, and the expansion effect is more pronounced. In contrast, for the wide device ($W = 60$ μm) self-heating is more pronounced and the impact ionization current responsible for the expansion effect is suppressed due to the reduced mean-free-path at high temperature. As a result, the wide device shows almost no expansion effect.

This interpretation is further confirmed by the experimental data for the $W = 12$ μm device in Fig. 6.15, which shows an expansion effect intermediate between those of the narrow and wide devices. The new compact model captures the interplay between self-heating and the expansion effect through the physical geometry dependence of the thermal conductance coupled with accurate modeling of the temperature dependence of the impact ionization

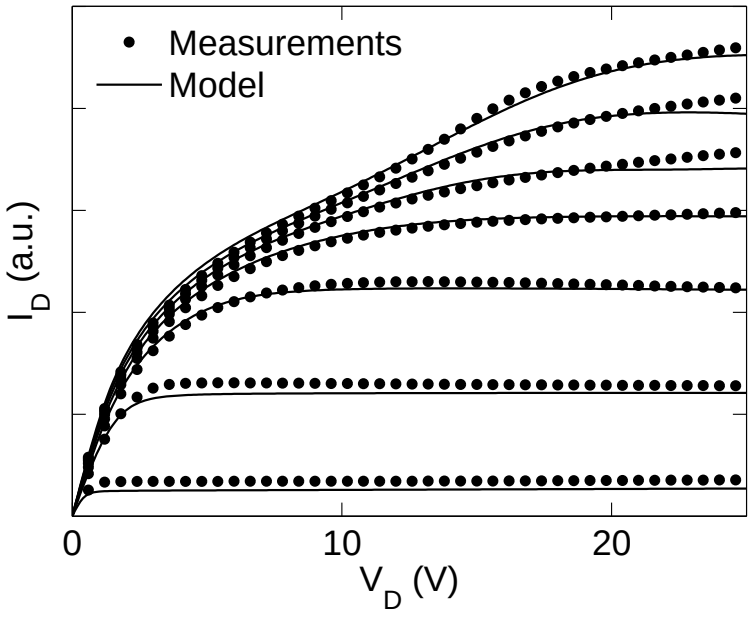


(a) $W = 3\ \mu\mathrm{m}$



(b) $W = 60\ \mu\mathrm{m}$

Figure 6.14: Measurement verification of drain current as a function of drain voltage at different gate voltage for devices with varying width. V_{G} varies from 2 V to 8 V with a step of 1 V and $V_{\mathrm{B}} = 0$.



(a) $W = 12$ μm

Figure 6.15: Drain current as a function of drain voltage at different gate voltage for a device with intermediate width. $V_{\rm G}$ varies from 2 V to 8 V with a step of 1 V and $V_{\rm B} = 0$.

currents. In Figs. 6.14 and 6.15, a single parameter set is used to cover all the devices with varying width.

The scalability of the new model with respect to W is further illustrated in Fig. 6.16 for two bias conditions. The bias values are selected so that $I_{\rm DSAT1}$ is predominantly determined by the drift region resistance and $I_{\rm DSAT2}$ is predominantly determined by the intrinsic MOS device behavior. For wide devices self-heating effectively quenches impact ionization so that the higher gate bias $I_{\rm DSAT1}$ is most affected by quasi-saturation, i.e. depends primarily on the drift region resistance. For narrower devices there is less self-heating, impact ionization increases and $I_{\rm DSAT1}$ is primarily determined by the expansion effect. Fig. 6.16 shows that the new model accurately captures the bias and geometry dependence of these interrelated effects.

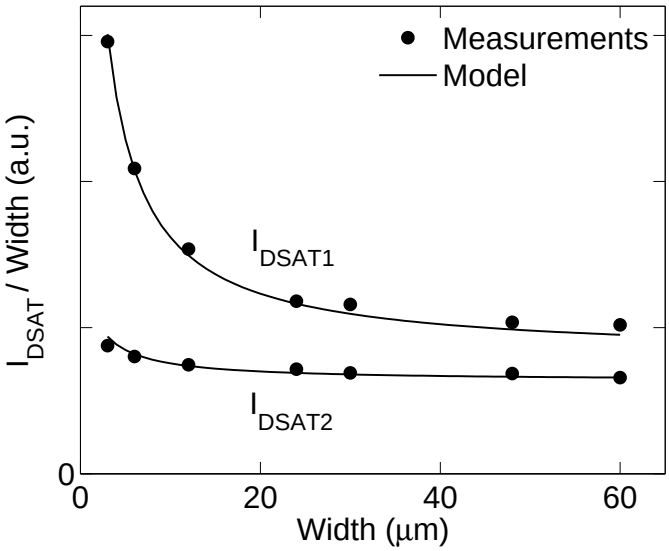
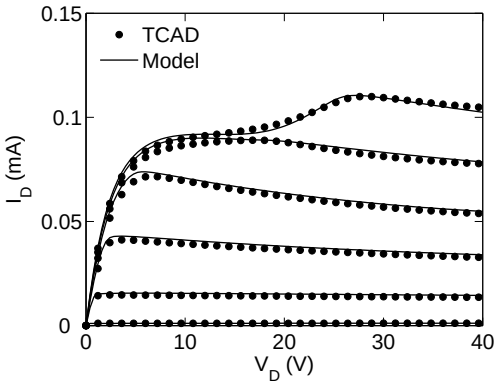


Figure 6.16: Normalized I_{DSAT} by device width at two different bias conditions as a function of device width. I_{DSAT1}: $V_{\mathrm{D}} = 25$ V and $V_{\mathrm{G}} = 8$ V; I_{DSAT2}: $V_{\mathrm{D}} = 25$ V and $V_{\mathrm{G}} = 4$ V. Please note that this is a different device from that of Fig. 3.17.

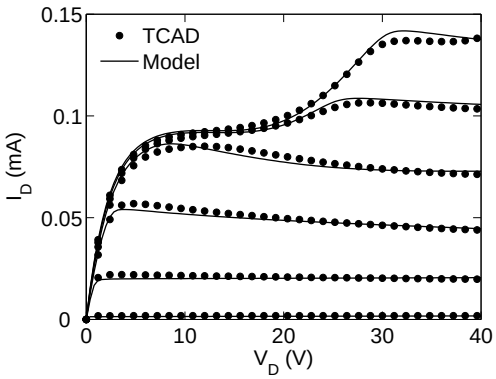
Experimental data for the scalability over channel and drift region lengths are not available to us (or in the literature) at the present time. Hence we rely on TCAD simulations, which this time include self-heating and the thermal boundary is a thermal contact placed at the bottom of the device at 300 K. Typical results shown in Fig. 6.17 confirm the model scalability with channel and drift region lengths.

6.7 Summary

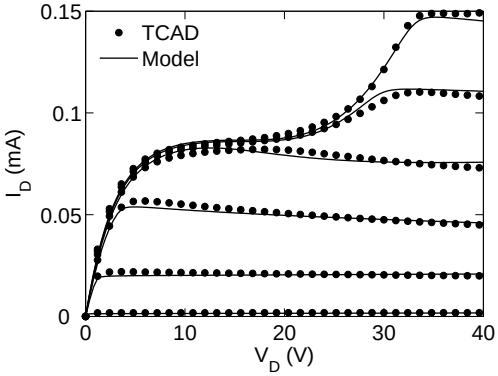
A compact model of impact ionization in LDMOS transistors is developed. This description follows the device physics [49, 50] and allows one to capture the effect of impact ionization on LDMOS output characteristics. The expansion effect is modeled by modulating the drift region resistance by the impact ionization current in the same region. The model is verified against



(a) $L_{\rm ch} = 1.5$ μm and $L_{\rm dr2} = 3.5$ μm



(b) $L_{\rm ch} = 1.0$ μm and $L_{\rm dr2} = 3.5$ μm



(c) $L_{\rm ch} = 1.0$ μm and $L_{\rm dr2} = 4.5$ μm

Figure 6.17: Measurement verification of drain current as a function of drain voltage at different gate voltage for devices with varying width. $V_{\rm G}$ varies from 2 V to 7 V with a step of 1 V and $V_{\rm B} = 0$.

both TCAD simulation and experimental data. The width dependence of the expansion effect is captured through the interaction between the temperature dependence of impact ionization in the drift region and the geometry dependence of self-heating.

CHAPTER 7

MODEL CONVERGENCE AND CIRCUIT SIMULATION EXAMPLES

Convergence is an important aspect for a compact model because it determines whether a compact model can be used by designers for circuit simulations. In this Chapter, some examples are presented to demonstrate the convergence property of SP-HV.

7.1 Simple Circuits: Ring Oscillator and Inverter Tree

In this Section, two simple circuits, a ring oscillator and an inverter tree, are used as the first step of model convergence demonstration. Figs. 7.1 and 7.2 show the waveforms of the SPICE simulations. In these simulations, the Verilog-A code has been used.

7.2 10 Volt Regulator

In this Section, a 10-V voltage regulator is used for model convergence demonstration. In the circuit, the low-voltage MOSFETs are modeled by PSP103 [141] and the LDMOS devices are described by SP-HV [51]. Fig. 7.3 shows the schematics of the circuit and Fig. 7.4 shows the simulation results.

7.3 Automatic C-code Generation and Runtime Test

In this Section, the Verilog-A code is compiled by ADMS (Automatic Device Model Synthesizer) [142] and the generated C-code is used to test the speed of SP-HV. Fig. 7.5 shows the runtime test results. The linear shape of the plot indicates there are no major problems in SP-HV. Besides, this test also

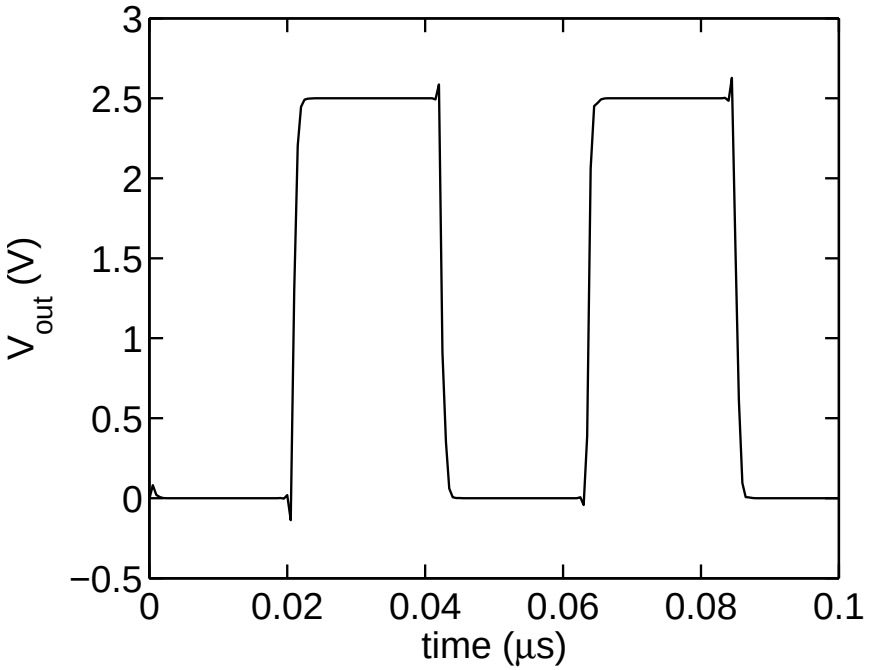


Figure 7.1: Waveform of the 51-stage ring oscillator.

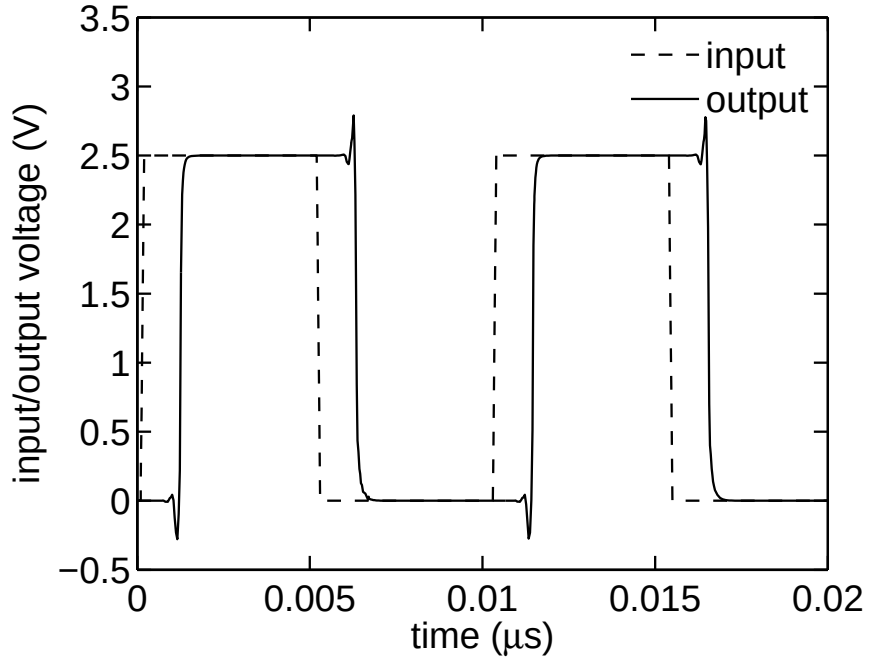


Figure 7.2: Waveform of the inverter tree.

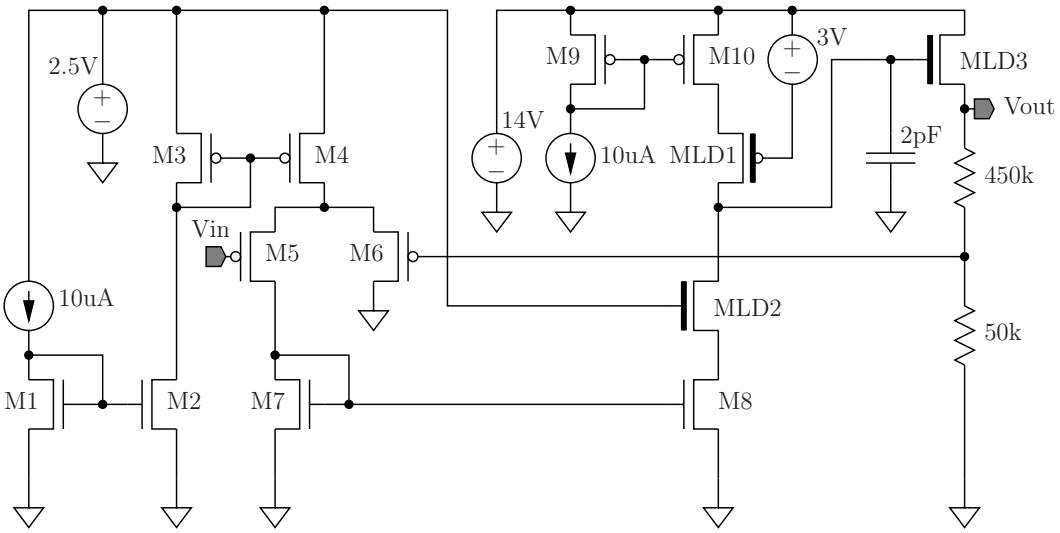


Figure 7.3: Schematic of the 10-V regulator. (Courtesy of A. Cassagnes, Freescale Semiconductor, with permission.)

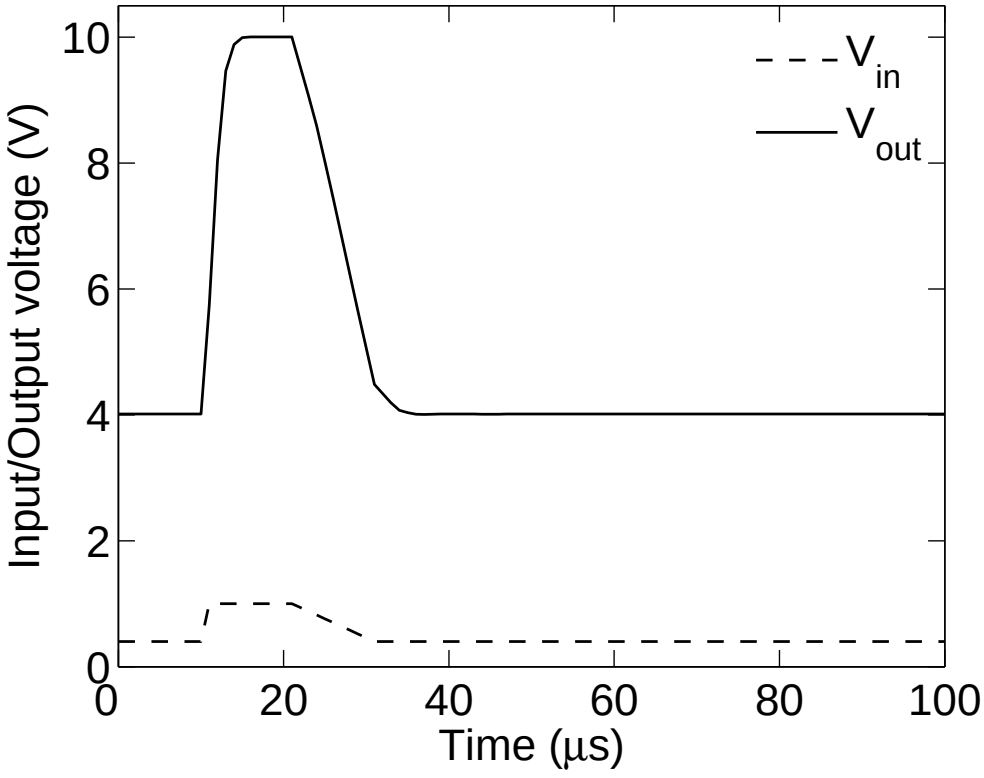


Figure 7.4: Waveform of the 10-V regulator.

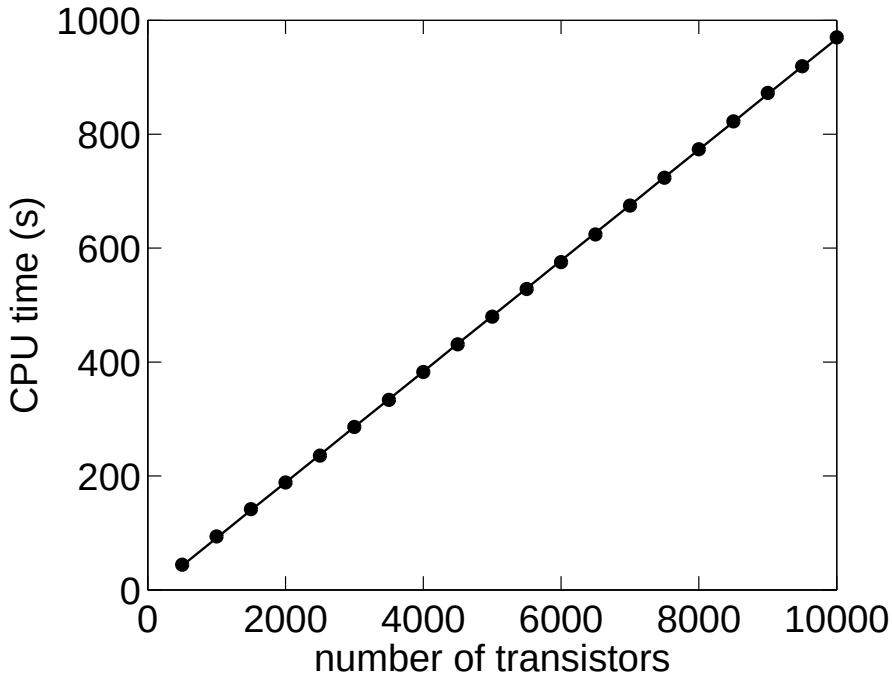


Figure 7.5: Results of the runtime test with C-code generated by ADMS.

verifies the possibility of automatic C-code generation.

CHAPTER 8

CONCLUSIONS

This dissertation has presented a new scalable surface-potential-based compact LDMOS model, SP-HV, which is based on a combination of the PSP and R3 models, both modified to better reflect characteristics of the LDMOS device structure and behavior. In particular, a new charge model has been developed, which accounts for charge in the first drift region. This leads to an accurate prediction of the transcapacitances.

The generalized Berglund relation has been extended to LDMOS transistors and it has been used to verify the quality of the charge model in SP-HV.

A new compact model of impact ionization in the drift region has been presented. The model is based on device physics and captures the double-hump $I_{\mathrm{B}}(V_{\mathrm{G}})$ and the effect of impact ionization on LDMOS output characteristics. The expansion effect is modeled by modulating the drift region resistance by the impact ionization current in the same region. The width dependence of the expansion effect is captured through the interaction between the temperature dependence of impact ionization in the drift region and the geometry dependence of self-heating.

The model, including its scalability, has been verified against both TCAD simulation and experimental data. The model is coded in Verilog-A, assuring its portability. Simulation examples have been presented to demonstrate the convergence and robustness of the model.

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APPENDIX A

SP-HV PARAMETER EXTRACTION PROCEDURE

The parameter extraction strategy for SP-HV consists of four main steps:

1. Measurements
2. Extraction of local parameters at room temperature
3. Extraction of temperature scaling parameters
4. Extraction of geometry scaling (global) parameters

The above steps will be briefly described in the following sections. Note that the description of the extraction procedure is not 'complete' in the sense that only the most important parameters are discussed and in cases at hand it may be advantageous (or even necessary) to use an adapted procedure.

Throughout this section bias and current conditions are given for an n-channel transistor only; for a p-channel transistor, all voltages and currents should be multiplied by -1.

As explained in Chapter 3, the hierarchical setup of SP-HV (local and global level) allows for the two-step parameter extraction procedure described in this section; this is the recommended method of operation. Nevertheless, it is possible to skip the first steps and start extracting global parameters directly. This procedure is not described here, but the directions below may still be useful.

A.1 Measurements

The parameter extraction routine consists of six different DC-measurements (two of which are optional) and four capacitance measurements.[1] Measure-

[1]The bias conditions to be used for the measurements are dependent on the supply voltage of the process. Of course it is advisable to restrict the range of voltages to their maximum values. Otherwise physical effects atypical for normal transistor operation—and therefore less well described by the compact model—may dominate the characteristics.

ments V and VI are only used for extraction of gate-current, avalanche, and GIDL/GISL parameters.

- **Measurement I** ("idvg"): I_{D} vs. V_{G}

  $V_{\mathrm{G}} = 0 \ldots V_{\mathrm{G,max}}$ (with steps of maximum 50 mV).

  $V_{\mathrm{D}} = 25$ or 50 mV

  $V_{\mathrm{B}} = 0 \ldots -|V_{\mathrm{B,max}}|$ (3 or more values)

  $V_{\mathrm{S}} = 0$

- **Measurement II** ("idvgh"): I_{D} and I_{B} vs. V_{G}

  $V_{\mathrm{G}} = 0 \ldots V_{\mathrm{G,max}}$ (with steps of maximum 50 mV).

  $V_{\mathrm{D}} = 0.1 \times V_{\mathrm{D,max}} \ldots V_{\mathrm{D,max}}$ (3 or more values)

  $V_{\mathrm{B}} = 0 \ldots -|V_{\mathrm{BS,max}}|$ (3 or more values)

  $V_{\mathrm{S}} = 0$

- **Measurement III** ("idvd"): I_{D} vs. V_{D}

  $V_{\mathrm{G}} = 0 \ldots V_{\mathrm{G,max}}$ (5 or more values)

  $V_{\mathrm{D}} = 0 \ldots V_{\mathrm{D,max}}$ (with steps of $V_{\mathrm{D,max}}/100$).

  $V_{\mathrm{B}} = 0$

  $V_{\mathrm{S}} = 0$

- **Measurement IV** ("idvdh"):I_{D} vs. V_{D}

  $V_{\mathrm{G}} = 0 \ldots V_{\mathrm{G,max}}$ (5 or more values)

  $V_{\mathrm{D}} = 0 \ldots V_{\mathrm{D,max}}$ (with steps of $V_{\mathrm{D,max}}/100$).

  $V_{\mathrm{B}} = -|V_{\mathrm{B,max}}|$

$V_S = 0$

- **Measurement V** ("igvg", optional): I_G and I_B vs. V_G

  $V_G = -V_{G,max} \ldots V_{G,max}$ (with steps of maximum 50 mV).

  $V_D = 0 \ldots V_{D,max}$ (3 or more values)

  $V_B = 0$

  $V_S = 0$

- **Measurement VI** ("igvgh", optional): I_G and I_B vs. V_G

  $V_G = -V_{G,max} \ldots V_{G,max}$ (with steps of maximum 50 mV).

  $V_D = 0 \ldots V_{D,max}$ (3 or more values)

  $V_B = -|V_{B,max}|$

  $V_S = 0$

- **Measurement VII** ("cggvg"): C_{GG} and C_{BG} vs. V_G

  $V_G = -V_{G,max} \ldots V_{G,max}$ (with steps of maximum 50 mV).

  $V_D = 0$

  $V_B = 0$

  $V_S = 0$

- **Measurement VIII** ("cdgvg"): C_{DG} and C_{SG} vs. V_G

  $V_G = -V_{G,max} \ldots V_{TH}$ (with steps of maximum 50 mV).

  $V_D = 0$

  $V_B = 0$

$V_S = 0$

- **Measurement IX** ("cgdvd"): C_{GD} vs. V_D

  $V_G = 0$

  $V_D = 0 \ldots V_{D,max}$ (with steps of $V_{D,max}/100$).

  $V_B = 0$

  $V_S = 0$

- **Measurement X** ("cgsvs"): C_{GS} vs. V_S

  $V_G = 0$

  $V_D = 0$

  $V_B = 0$

  $V_S = 0 \ldots V_{G,max}$ (with steps of maximum 50 mV).

For the extraction procedure, the transconductance g_m (for Measurement I and II) and the output conductance g_{DS} (for Measurement III and IV) are obtained by numerical differentiation of the measured I-V-curves.

For devices with source and body terminals connected internally, V_B cannot be biased independently and is fixed at 0. Meanwhile, C_{BG} in Measurement VII and C_{SG} in Measurement VIII are equal to each other. Measurement X cannot be performed on such devices.

The local parameter extraction measurements I through VI have to be performed at room temperature for every device. In addition, capacitance measurements VII and VIII need to be performed for at least a long/wide and a short/wide (i.e., $L = L_{min}$) transistor (at room temperature). Furthermore, for the extraction of temperature scaling parameters measurements I, III, and

V have to be performed at different temperatures (at least two extra, typically $-40\,^{\circ}\mathrm{C}$ and $125\,^{\circ}\mathrm{C}$) for at least a long wide and a short wide transistor.

A.2 Extraction of Local Parameters at Room Temperature

General remarks

The simultaneous determination of *all* local parameters for a specific device is not advisable, because the value of some parameters can be wrong due to correlation and suboptimization. Therefore it is more practical to split the parameters into several small groups, where each parameter group can be determined using specific measurements. In this section, such a procedure will be outlined.

It is not the case that all local parameters are extracted for every device. Several parameters are only extracted for one or a few devices, while they are kept fixed for all other devices. Moreover, a number of parameters can generally be kept fixed at their default values and need only occasionally be used for fine-tuning in the optimization procedure. Details are given later in this section.

It is recommended to start the extraction procedure with the long(est) wide(st) device, then the shortest device with the same width, followed by all remaining devices of the same width in order of decreasing length. Then the next widest-channel devices are extracted, where the various lengths are handled in the same order. In this way, one works one's way down to the narrowest channel devices. In some technologies, the length of the intrinsic MOSFET is fixed. This situation will be discussed later separately in Section A.6.

AC-parameters

Some parameters (such as **TOX** and **NP**) that do affect the DC-behavior of a MOSFET can only be extracted accurately from C-V-measurements. This should be done before the actual parameter extraction from DC-measurements is started. In Tables A.1 through A.3 the extraction procedure for the AC-parameters is given.

Table A.1: AC-parameter extraction for a wide MOSFET

Step	**Optimized parameters**	**Fitted on**
1	**CGOV**, **NOV**, **CFR**	X:C_{GS}
2	**CGOVD**, **NOVD**, **CFRD**	IX:C_{GD}

Table A.2: AC-parameter extraction procedure for a long channel MOSFET.

Step	**Optimized parameters**	**Fitted on**
1	**VFB**, **NEFF**, **DPHIB**, **NP**, **COX**	VII: C_{GG}
2	Repeat Step 1	

Table A.3: AC-parameter extraction procedure for a short channel MOSFET. The values of **VFB** and **NP** are taken from the long-channel case.

Step	**Optimized parameters**	**Fitted on**
1	**NEFF**, **DPHIB**, **COX**	VII: C_{GG}
2	**CGOV**, **NOV**	VIII: C_{SG}
3	**CGOVD**, **NOVD**	VIII: C_{DG}
4	Repeat Steps 1 – 3	

Starting from the default parameter set and setting **TOX** to a reasonable value (as known from technology), **VFB**, **NEFF**, **DPHIB**, **COX**, and **NP** can be extracted from C_{GG} in Measurement VII for a long, wide device.

In general, one can assume **TOXOV** = **TOXOVD** = **TOX**.

The value of **TOX** can be determined from **COX** $= \epsilon_{\mathrm{ox}} \cdot L \cdot W/$**TOX**. If the device is sufficiently long and wide, drawn length and width can be

used in this formula. Even better, if Measurement VII is available for a few short/wide devices of different lengths, one can extract **TOX** and ΔL from a series of extracted values of **COX** vs. L_{draw}.

Some remarks:

- If C-V-measurements are not available, one could revert to values known from the fabrication process. Note that **TOX** and **TOXOV** are *physical* oxide thicknesses; poly-depletion and quantum-mechanical effects are taken care of by the model. If the gate dielectric is not pure SiO_2, one should manually compensate for the deviating dielectric constant.

- In general, **VFB** and **NP** can be assumed independent of channel length and width (so, the long/wide-channel values can be used for all other devices as well). Only if no satisfactory fits are obtained, one could allow for a length dependence (for **NP**) or length *and* width dependence (for **VFB**).

- The value of parameter **TOX** profoundly influences both the DC- and AC-behavior of the SP-HV model and thus the values of many other parameters. It is therefore very important that this parameter is determined (as described above) and *fixed* before the rest of the extraction procedure is started.

If desired (e.g., for RF-characterization), parameters for several parasitic capacitances (gate-bulk overlap, fringe capacitance, etc.) can be extracted as well (**CGBOV** and **CFR**). However, this requires additional capacitance measurements.

The obtained values of **VFB**, **TOX**, **TOXOV**, **NP**, and **NOV** can now be used in the DC-parameter extraction procedure. The above values of **NEFF**

and **DPHIB** can be disregarded; they will be determined more accurately from the DC-measurements.

In devices with strong lateral non-uniform doping, the threshold voltage and substrate doping in AC-measurements may deviate significantly from those in DC-measurements. If that is the case, values for **NEFF** and **DPHIB** obtained from DC-measurements may not be satisfactory to describe AC-measurements. Then, one has the option to set

$$\mathbf{SWDELVTAC} = 1\,,$$

$$\mathbf{DELVTAC} = \mathbf{DPHIB}_{\mathrm{ac}} - \mathbf{DPHIB}_{\mathrm{dc}}\,,$$

and

$$\mathbf{FACNEFFAC} = \mathbf{NEFF}_{\mathrm{ac}}/\mathbf{NEFF}_{\mathrm{dc}}$$

to get a good description of both the DC and AC measurements. The extraction flow is illustrated in Fig. A.1 indicating that AC readjustment is an optional part which increases computation time because of the extra surface potential calculation.

DC-parameters

Before the optimization is started a reasonably good starting value has to be determined, both for the parameters to be extracted and for the parameters which remain constant. For most parameters to be extracted for a *long* channel device, the default values from Section 2 in [143] can be taken as initial values. Exceptions are given in Table A.4. Starting from these values, the optimization procedure following the scheme below is performed. This method yields a proper set of parameters after the repetition indicated as the final step in the

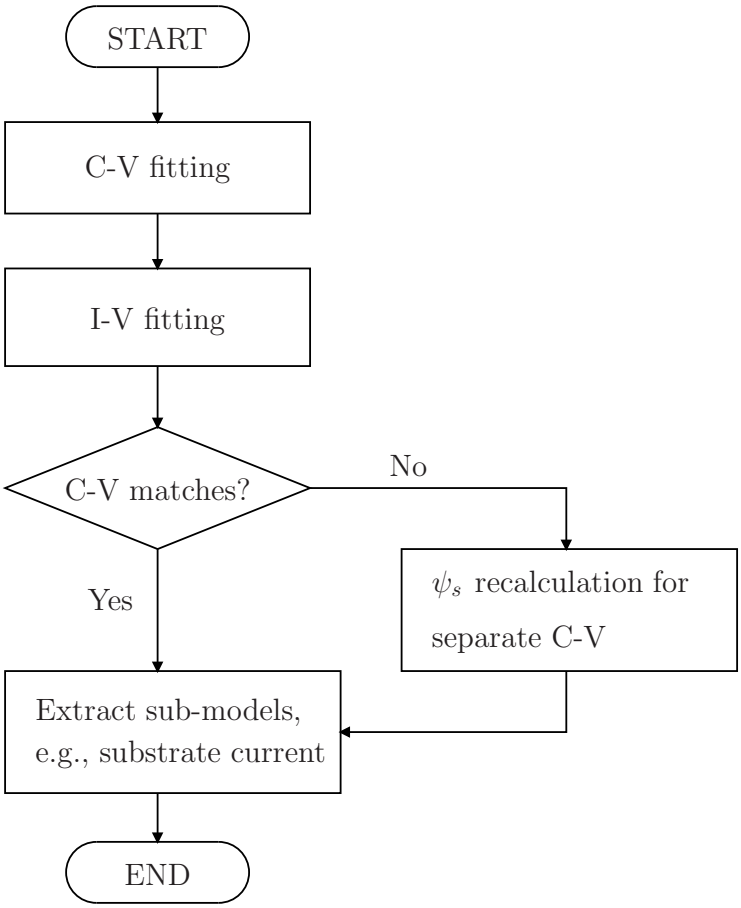

Figure A.1: Parameter extraction procedure which allows the separate surface potential calculation for currents and charges.

scheme. Experiments with transistors of several processes show that repeating those steps more than once is generally not necessary.

For an accurate extraction of parameter values, the parameter set for a long-channel transistor has to be determined first. In the long-channel case most of the mobility related parameters (i.e. **MUE** and **THEMU**) are determined and subsequently fixed for the shorter-channel devices.

In Table A.5 the complete DC extraction procedure for long-channel transistors is given. The magnitude of the simulated I_{D} and the overall shape of the simulated I_{D}-V_{GS}-curve is roughly set in Step 1. Next the parameters **NEFF**, **DPHIB**, and **CT**—which are important for the subthreshold behavior—are

Table A.4: Initial values for local parameter extraction for a *long*-channel device. For parameters which are not listed in this table, the default value (as given in Section 2 in [143]) can be used as initial value.

Parameter	**Initial value**
BETN	$0.03 \cdot W/L$
RS	0
THESAT	0.1
AX	12
A1	0

Table A.5: DC-parameter extraction procedure for a long-channel MOSFET. The parameters **VFB**, **TOX**, **TOXOV**, **NP**, and **NOV** must be taken from C-V-measurements.

Step	**Optimized parameters**	**Fitted on**
1	**NEFF**, **BETN**, **MUE**, **THEMU**[a]	I: I_{D}
2	**NEFF**, **DPHIB**, **CT**	I: I_{D}
3	**MUE**, **THEMU**[a], **CS**, **XCOR**, **BETN**	I: I_{D}, g_{m}
4	**THESAT**	III: I_{D}
5	**ALP**, **ALP1**, **ALP2**, **VP**[a], (**AX**)	III: g_{DS}
6	**THESAT**	II: I_{D}
7	**IGINV**, **GC2**[a], **GC3**[a]	V: I_{G}
8	**IGOV**, (**GCO**[a])	V: I_{G}
9	**A1**, **A2**[a], **A3**	II or V: I_{B}
10	**A4**	II or VI: I_{B}
11	**AGIDL**, **BGIDL**[a]	V: I_{B}
12	**CGIDL**[a]	VI: I_{B}
13	Repeat Steps 2 – 12	

[a]Only extracted for the *widest* long channel device and fixed for all other geometries.

optimized in Step 2, neglecting short-channel effects such as drain-induced barrier-lowering (DIBL). After that, the mobility parameters are optimized in Step 3, neglecting the influence of series-resistance. In Step 4 a preliminary value of the velocity saturation parameter is obtained, and subsequently the conductance parameters **ALP**, **ALP1**, **ALP2**, and **VP** are determined in Step 5. A more accurate value of **THESAT** can now be obtained using

Table A.6: DC-parameter extraction procedure for a short-channel MOSFET. Parameters **MUE**, **THEMU**, **VP**, **GCO**, **GC2**, **GC3**, **A2**, **A4**, **BGIDL**, and **CGIDL** are taken from the corresponding long-channel case.

Step	Optimized parameters	Fitted on
1	**NEFF**, **DPHIB**, **BETN**, **RS**[a], **RSHLDD**	I: I_{D}
2	**NEFF**, **DPHIB**, **CT**	I: I_{D}
3	**BETN**, **RS**[a], **XCOR**, **RSHLDD**	I: I_{D}, g_{m}
4	**THESAT**	III: I_{D}
5	**ECRIT**, **ECORN**, **DU**, **ATS**, **THEACC**	III:I_{D}
6	**RSHLDD**, **ECRIT**, **ECORN**, **RVA**	III:I_{D}
7	**ALP**, **ALP1**, **ALP2**, **CF**, (**AX**)	III: g_{DS}
8	**CFB**[b]	IV: g_{DS}
9	**THESAT**, **THESATG**[b], **THESATB**[b], **THEACC**	II: I_{D}, g_{m}
10	**IGINV**, **IGOV**	V: I_{G}
11	**A1**, **A3**	II or V: I_{B}
12	**AGIDL**	V: I_{B}
13	**ADR1**[a], **ADR2**[b], **ADR3**[a], **ADR4**[a], **ADR5**[a]	II:I_{B}
14	**BIDR1**[a], **BIDR2**[b]	III:I_{D}
15	Repeat Steps 2 – 14	

[a]Only extracted for the *shortest* channel of each width and fixed for all other geometries.
[b]Only extracted for the *shortest widest* device and fixed for all other geometries.

Step 6. The gate current parameters are determined in Steps 7 and 8, where it should be noted that **GCO** should only be extracted if the influence of gate-to-bulk tunneling is visible in the measurements. This is usually the case if $V_{\mathrm{G}} \gtrsim |\mathbf{VFB}|$. This is followed by the weak-avalanche parameters in Step 9 and (optionally) 10, and finally, the gate-induced leakage current parameters are optimized in Step 11 and (optionally) 12.

After completion of the extraction for the long-channel device, it is recommended to first extract parameters for the shortest-channel device (of the same width). The mobility-reduction parameters (**MUE**, **THEMU**) found from the corresponding long-channel device should be used. The extraction procedure as given in Table A.6 should be used. Some of the drift region impact-ionization parameters (**ADR1**, **ADR3**, **ADR4**, **ADR5**) may not be

able to be extracted from the longest device because the long channel devices are usually dominated by the intrinsic MOSFET so that these parameters have almost no effect to device electrical behavior. Therefore, they should be extracted for the shortest channel of each width and fixed for all other device lengths.

Note that once the value for **RS** and the drift region resistance parameters has been found from the shortest device, they should be copied into the long-channel parameter set and steps 2–3 in Table A.5 should be repeated, possibly leading to some readjustment of **MUE** and **THEMU**. If necessary, this procedure can be repeated. Similarly, once the value of **THESATG** and **THESATB** have been determined from the shortest widest channel device—steps 4, 5, and 6 of the long-channel extraction procedure (Table A.5) may be repeated to obtain updated values for **THESAT**, **ALP**, **ALP1**, and **ALP2**.

If consistent parameters have been found for the longest and shortest channel device, the extraction procedure as given in Table A.6 can be executed for all intermediate channel lengths. The extracted parameter values of the next-longer device can be used as initial values.

Finally, the parameters **GFACNUD**, **VSBNUD**, and **DVSBNUD** should only be used if the description of the body effect is not satisfactory otherwise. For this, the non-uniform doping model must be invoked by setting **SWNUD** = 1.

A.3 Extraction of Temperature Scaling Parameters

For a specific device, the temperature scaling parameters can be extracted after determination of the local parameters at room temperature. In order to do so, measurements I, II and IV need to be performed at various temperature

Table A.7: Temperature scaling parameter extraction procedure for a long wide channel MOSFET. This scheme only makes sense if measurements have been performed at one or (preferably) more temperatures which differ from room temperature.

Step	Optimized parameters	Fitted on
1	**STVFB**[a]	I: I_D
2	**STBETN**[a], **STMUE**, **STTHEMU**, **STCS**, **STXCOR**	I: I_D
3	**STTHESAT**[a]	II: I_D
4	**STIG**	V: I_G
5	**STA2**	V: I_B
6	**STBGIDL**	V: I_B

[a]Also extracted for one or more long *narrow* devices.

values (at least two values different from room temperature, typically $-40\,^{\circ}\mathrm{C}$ and $125\,^{\circ}\mathrm{C}$), at least for a long wide device and a short wide device. If the reference temperature **TR** has been chosen equal to room temperature (as recommended in Section A.2), the modeled behavior at room temperature is insensitive to the value of the temperature scaling parameters. As a first-order estimate of the temperature scaling parameter values, the default values as given in Section 2 in [143] can be used. Again the parameter extraction scheme is slightly different for the long-channel and for the short-channel case.

For an accurate extraction, the temperature scaling parameters for a long-wide-channel device have to be determined first. In the long-wide-channel case the carrier mobility parameters can be determined, and they are subsequently fixed for all other devices. In Table A.7 the appropriate extraction procedure is given. In Step 1 the subthreshold temperature dependence is optimized, followed by the optimization of mobility reduction parameters in Step 2. Next the temperature dependence of velocity saturation is optimized in Step 3. In the subsequent steps, parameters for the temperature dependence of the gate current, the impact ionization current and gate-induced

Table A.8: Temperature scaling parameter extraction procedure for short-channel MOSFETs (both wide and narrow). This scheme only makes sense if measurements have been performed at one or (preferably) more temperatures which differ from room temperature.

Step	Optimized parameters	Fitted on
1	**STVFB**	I: I_{D}
2	**STBETN**, **STRS**[a], **TC1**, **TC2**	I: I_{D}
3	**STTHESAT**	II: I_{D}
4	**STADR2**	II:I_{B}

[a]Only extracted for a short *narrow* device and fixed for all other geometries.

drain leakage are determined. The determined values of the mobility reduction temperature scaling parameters (i.e., **STMUE**, **STTHEMU**, **STCS**, and **STXCOR**) are copied to all other devices and kept fixed during the remainder of the temperature-scaling parameter extraction procedure. Step 1 and 2 could then be performed on one or more long narrow devices as well (for **STVFB**, **STBETN**, and **STTHESAT** only).

Next the extraction procedure as given in Table A.8 is carried out for several short devices of different widths. Preferably, the extraction is done first for a short narrow device, such that the determined value of **STRS** can be used during the extraction of the wider devices.

Note that previous extraction procedure applies to the case when self-heating effect is insignificant (**SWSHE** = 0). It is recommended to always turn off self-heating effect(SHE) unless it is necessary. Turning-on SHE might increase simulation time and cause difficulty in convergence. It also causes difficulty in parameter extraction. Theoretically, thermal resistance R_{TH} and capacitance C_{TH} can only be accurately extracted when self-heating-free data are available, for example, data from pulse measurement with sufficiently short pulse. The model parameters can be extracted as mentioned before and R_{TH} can be extracted from the data with SHE. In the cases when self-heating-free

data are not available, R_{TH} can be treated as a fitting parameters and be extracted. The suggested parameter extraction procedure is as follows:

1. Extract model parameter as aforementioned by setting **SWSHE** $= 0$.
2. Extract **STVFB**, **STBETN**, **STMUE**, **STTHEMU**, **STCS**, **STXCOR**, **TC1**, **TC2** from I:I_{D} vs. V_{G} at low V_{D} when self-heating effect is insignificant
3. Set **SWSHE** $= 1$ and extract **RTH**, **STTHESAT**, **THESAT**, **THESATG** from III:I_{D} vs. V_{D}.
4. Extract **STIG**, **STA2**, **STADR2**, **STBGIDL** after self-heating parameters are fixed.
5. Repeat 2–4 if necessary.

A.4 Extraction of Geometry Scaling Parameters

The aim of the complete extraction procedure is the determination of the geometry scaling parameters (global parameters), i.e., a single set of parameters (see Chapter 3) which gives a good description of the MOSFET-behavior over the full geometry range.

Determination of ΔL and ΔW

An extremely important part of the geometry scaling extraction scheme is an accurate determination of ΔL and ΔW, see Eqs. (3.3) and (3.4). Since it affects the DC-, the AC- as well as the noise model and, moreover, it can heavily influence the quality of the resulting global parameter set, it is very important that this step is carried out with care.

Traditionally, ΔW can be determined from the extrapolated zero-crossing in **BETN** versus mask width W. In a similar way ΔL can be determined from 1/**BETN** versus mask length L. For modern MOS devices with pocket implants, however, it has been found that the above ΔL extraction method is no longer valid [144, 145]. Another, more accurate method is to measure the gate-to-bulk capacitance C_{GB} in accumulation for different channel lengths [145,146]. In this case the extrapolated zero-crossing in the C_{GB} versus mask length L curve will give ΔL. Similarly, the extracted values for **COX** (from the procedure in Table A.2 and A.3) vs. mask length L may be used for this purpose.

Finally, **LOV** can be obtained from (a series of) extracted values of **CGOV** from one or more short devices.

From local to global

Once the values of ΔL and ΔW are firmly established (as described above), **LAP** and **WOT** can be set and the actual extraction procedure of the geometry scaling parameters can be started. It consists of several *independent* sub-steps (which can be carried out in random order), one for each geometry dependent local parameter.

To illustrate such a sub-step, the local parameter **CS** is taken as an example. The relevant geometry scaling equation is

$$\mathbf{CS} = \left(\mathbf{CSO} + \frac{\mathbf{CSL}}{L_{\mathrm{eff}}^{\mathbf{CSLEXP}}}\right) \cdot \left(1 + \frac{\mathbf{CSW}}{W_{\mathrm{eff}}}\right) \cdot \left(1 + \frac{\mathbf{CSLW}}{W_{\mathrm{eff}} \cdot L_{\mathrm{eff}}}\right) \qquad \text{(A.1)}$$

It can be seen that **CSO**, **CSL**, **CSLEXP**, **CSW**, and **CSLW** are the global parameters which determine the value of **CS** as a function of L_{eff} and W_{eff}. First, the extracted **CS** of each device in a length-series of measured (preferably wide) devices are considered as a function of L_{eff}. In this context **CSO**,

CSL, and **CSLEXP** are optimized such that the fit of Eq. (A.1) to the extracted **CS**-values is as good as possible, while keeping **CSW** and **CSLW** fixed at 0. Then **CSW** is determined by considering the extracted **CS**-values from a length-series of measured narrow (preferably long) devices. Then **CSLW** is determined by considering the extracted **CS**-values from a series small area devices. Finally, the five global parameters may be fine-tuned by optimizing all four parameters to all extracted **CS**-values simultaneously. All other parameters can be extracted in a similar manner.

Note that in many cases it may not be necessary to use the full flexibility of SP-HV's parameter scaling, e.g., for many technologies **NP** and **VFB** may be considered as independent of geometry. If such a geometry-independence is anticipated, the corresponding local parameter should be fixed during local parameter extraction. Only if the resulting global parameter set is not satisfactory, the parameter should be allowed to vary during a subsequent optimization round.

Fine tuning

Once the complete set of global parameters is found, the global model should give an accurate description of the measured I-V-curves and capacitance measurements. Either for fine tuning or to facilitate the extraction of global parameters for which the geometry scaling of the corresponding extracted local parameters is not well-behaved, there are two more things that can be done.

- Local parameters for which the fitting of global parameters was completed satisfactorily could be replaced by the values calculated from the geometrical scaling rules and fixed. Then one could redo (parts of) the local parameter extraction procedure for the remaining local parameters,

making them less sensitive for cross-correlations.

- Small groups of global parameters may be fitted directly to the measurements of a well-chosen series of devices, using the global model.

A.5 Summary – Geometrical Scaling

Summarizing, for the determination of a full parameter set, the following procedure is recommended.

1. Determine local parameter sets (**VFB**, **NEFF**, ...) for all measured devices, as explained in Section A.2 and A.3.
2. Find ΔL and ΔW.
3. Determine the global parameters by fitting the appropriate geometry scaling rules to the extracted local parameters.
4. Finally, the resulting global can be fine-tuned, by fitting the result of the scaling rules and current equations to the measured currents of all devices simultaneously.

A.6 Parameter Extraction for Devices with Fixed Channel Length

For some technologies, the length of the intrinsic MOSFET is fixed. The parameter extraction procedure need to be adjusted accordingly.

AC-parameters

In Table A.9, the extraction procedure for the AC-parameters is given.

Table A.9: AC-parameter extraction for a wide MOSFET

Step	**Optimized parameters**	**Fitted on**
1	**CGOV**, **NOV**, **CFR**	X:C_{GS}
2	**CGOVD**, **NOVD**, **CFRD**	IX:C_{GD}
3	**VFB**, **NEFF**, **NP**, **COX**	VII:C_{GG}
4	Repeat Steps 1 – 3	

DC-parameters

Because the long-channel device is not available, the mobility parameters cannot be extracted as usual from the I_{D} in Measurement I. Instead, the mobility parameters have to be extracted together with the velocity saturation parameters from the I_{D} vs. V_{G} at high V_{D} in Measurement II when the device is dominated by intrinsic MOSFET. The drift region resistance parameters are then extracted from I_{D} in quasi-saturation region and I_{D} in Measurement I. Iterations may be required before a good overall fitting can be achieved.

Table A.10: DC-parameter extraction procedure for a fixed-channel-length MOSFET. The parameters **VFB**, **TOX**, **TOXOV**, **NP**, and **NOV** must be taken from C-V-measurements.

Step	**Optimized parameters**	**Fitted on**
1	**NEFF**, **DPHIB**, **CT**	I, II:I_{D}
2	**NEFF**, **BETN**, **MUE**, **THEMU**, **THESAT**, **THESATG**	II: I_{D}, g_{m}
3	**RSHLDD**, **BETN**, **MUE**, **THEMU**, **RS**	I:I_{D}, g_{m}
4	**ECRIT**, **ECORN**, **DU**, **ATS**, **THEACC**	III:I_{D}
5	**RSHLDD**, **ECRIT**, **ECORN**, **RVA**	III: I_{D}
6	**ALP**, **ALP1**, **ALP2**, **VP**, **AX**	III:g_{DS}
7	**CFB**	IV:g_{DS}
8	**THESAT**, **THESATG**, **THESATG**, **THEACC**	II:I_{D}, g_{m}
9	**IGINV**, **GC2**, **GC3**	V: I_{G}
10	**IGOV**, **GCO**	V: I_{G}
11	**A1**, **A2**, **A3**, **A4**	II: I_{B}
12	**AGIDL**, **BGIDL**	V: I_{B}
13	**CGIDL**	VI: I_{B}
14	**ADR1**, **ADR2**, **ADR3**, **ADR4**, **ADR5**	II:I_{B}
15	**BIDR1**, **BIDR2**	III:I_{D}
16	Repeat Steps 2 – 15	