Any-Cap Low Dropout

Voltage Regulator

by

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ABSTRACT

Power management plays a very important role in the current electronics industry. Battery powered and handheld applications require novel power management techniques to extend the battery life. Most systems have multiple voltage regulators to provide power sources to the different circuit blocks and/or sub-systems. Some of these voltage regulators are low dropout regulators (LDOs) which typically require output capacitors in the range of 1's to 10's of μF. The necessity of output capacitors occupies valuable board space and can add additional integrated circuit (IC) pin count. A high IC pin count can restrict LDOs for system-on-chip (SoC) solutions.

The presented research gives the user an option with regard to the external capacitor; the output capacitor can range from 0 – 1μF for a stable response. In general, the larger the output capacitor, the better the transient response. Because the output capacitor requirement is such a wide range, the LDO presented here is ideal for any application, whether it be for a SoC solution or stand-alone LDO that desires a filtering capacitor for optimal transient performance. The LDO architecture and compensation scheme provide a stable output response from 1mA to 200mA with output capacitors in the range of 0 – 1μF. A 2.5V, 200mA any-cap LDO was fabricated in a

proprietary 1.5μm BiCMOS process, consuming 200μA of ground pin current (at 1mA load) with a dropout voltage of 250mV.

Experimental results show that the proposed any-cap LDO exceeds transient performance and output capacitor requirements compared to previously published work. The architecture also has excellent line and load regulation and less sensitive to process variation. Therefore, the presented any-cap LDO is ideal for any application with a maximum supply rail of 5V.

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CHAPTER I

INTRODUCTION

As system-on-chip (SoC) solutions gain more popularity, the need for integrated power management designs increases. Novel circuit ideas are required in the power management systems to prolong the battery life in handheld devices. With added features and more complex functions, maintaining high power efficiency can be difficult. A complete power management solution incorporates multiple subsystems which can include linear regulators, switching regulators, and charge pump regulators. Each DC/DC converter has its advantages and disadvantages and contributes to the entire power system to optimize efficiency, noise, EMI, and power requirements.

The presented research focuses on low dropout (LDO) linear voltage regulators. LDOs provide a constant voltage supply and are a very important part of a power management system. At input voltages close to the output voltage, the LDO regulator is much more efficient over conventional linear regulators. In addition to efficiency improvements, LDOs have more advantages over linear regulators making them more suitable for SoC power management solutions.

Power management systems typically contain multiple LDOs and switching regulators. Conventional LDOs require an output

capacitor in the 1's – 10's of μF that occupy valuable board space and increase IC pin count. The output capacitor provides LDO loop stability and great transient response [5]. A required output capacitor for SoC solutions is less than desirable which makes cap-less LDOs more attractive. However, large load steps can cause cap-less LDOs to have large output voltage overshoots and undershoots which makes them less attractive. The system blocks that receive power from the multiple LDOs have different power requirements. Some blocks need to have very quiet rails whereas some can tolerate more noisy rails. Typical cap-less LDOs become unstable if capacitance is added to the output. The presented research focuses on a LDO that is stable from 0 – 1μF output capacitors to facilitate SoC and/or stand-alone LDO applications.

A. LDO Regulator Applications

LDOs are mostly used in analog applications that generally require low noise and very accurate power supply rails. Voltage regulators provide a constant voltage supply rail under all loading conditions. LDO loading conditions consist of slowly varying load current in addition to large load current steps requiring the LDO to respond quickly to deliver the full current to the load at the regulation voltage.

LDO regulators are used in a wide range of applications from automotive, telecommunications, handheld battery devices, RF, etc. If digital ICs and analog ICs are mixed in a system (typical), then 1 LDO will drive the digital chips and 1 LDO will power the analog circuitry. Analog circuitry usually requires a very quiet supply rail for optimal performance whereas digital circuitry can typically tolerate noisier supplies.

In SoC solutions, the LDO regulator output supplies power to both the digital and analog circuitry. The digital circuitry can run off a cap-less LDO but the analog circuitry should run off an LDO that's stable with an external filtering capacitor for optimal transient performance. For simplicity of design layout, and bill of materials, it's best to use the same LDO for each the analog supply and digital supply, however, most previous work is either stable for no output capacitor or a large output capacitor which requires the design and layout of SoC solutions to be more difficult. The work presented here is stable for any capacitor value up to 1μF, making it suitable for just about any application.

B. Linear and LDO Linear Regulator Architectures

There are two different linear regulator topologies: a conventional linear regulator and a low dropout (LDO) linear

regulator. The main difference in these linear regulator topologies is the configuration of the pass transistor. The pass transistor in the conventional linear regulator is in a source-follower or emitter-follower configuration. The pass transistor in the LDO linear regulator is in a common-source or common-emitter configuration. The linear regulator topologies are shown in Figure 1 below.

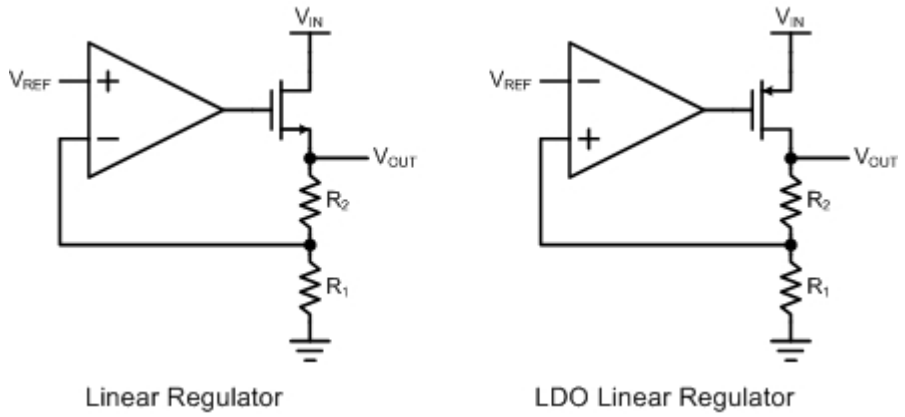

Figure 1: Conventional and LDO Linear Regulator Topologies

Both of the linear regulator topologies use the same feedback path (with the exception of the error amp polarity) to regulate the output voltage. In the conventional linear regulator, the highest the gate voltage of the pass transistor can be is V_{IN}, which implies that the highest V_{OUT} can be is $V_{IN} - V_{GS}$. Therefore, the conventional linear regulator is not sufficient for low voltage applications. Because the pass device is a source-follower (gain of 1 and low output impedance), the stability of the conventional linear regulator is great under most loading conditions.

The LDO linear regulator is more sufficient for low voltage applications because the pass device is in a common-source configuration. The error amp can pull the gate voltage as low as ground which fully turns on the pass transistor and can pull the output as high as $V_{IN} - V_{DSAT}$ which is a higher output voltage than what the conventional linear regulator can do. Unfortunately, the LDO regulator is inherently unstable due to the common-source configuration of the pass device. A common-source stage has an inverting gain greater than 1 and has increased output impedance making the compensation of the LDO more difficult than the conventional linear regulator [9][11]. Figure 2 below shows 1st and 2nd order poles of the conventional and LDO linear regulators.

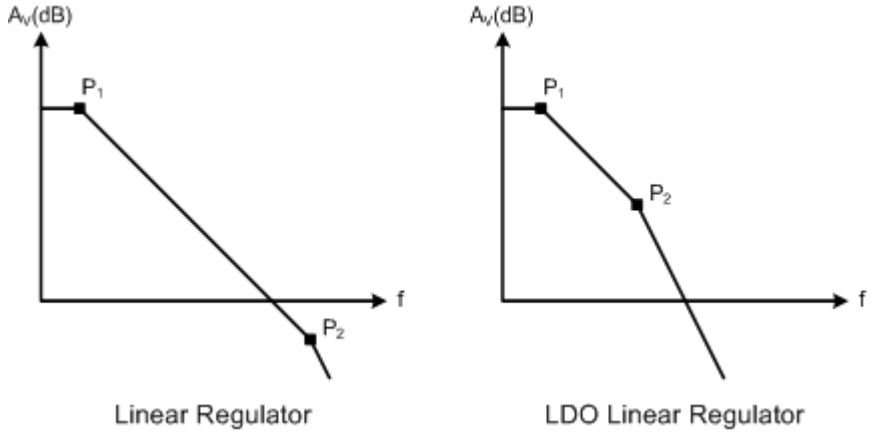

Figure 2: Pole Locations of the Conventional and LDO Linear Regulator w/out Compensation

The dominant pole, P1, in the linear regulator resides at the output of the error amplifier. The 2nd order pole, P2, comes from the

output of the regulator but is usually at high frequency due to the low impedance at the output of the regulator. The output pole is usually below 0dB and results in a stable regulator. The dominant pole, P1, in the LDO regulator resides at the output of the regulator due to the large output capacitor and large output impedance of the regulator. The 2nd pole, P2, is due to the output of the error amplifier and is usually in close proximity to the dominant pole and results in an unstable regulator. A typical way to compensate the LDO is to use the ESR of the output capacitor to add a zero into the frequency response [8]. If the zero is close to the P2 frequency, then the zero cancels out P2 and the frequency response looks close to a single pole system. Figure 3 below shows the LDO with ESR compensation.

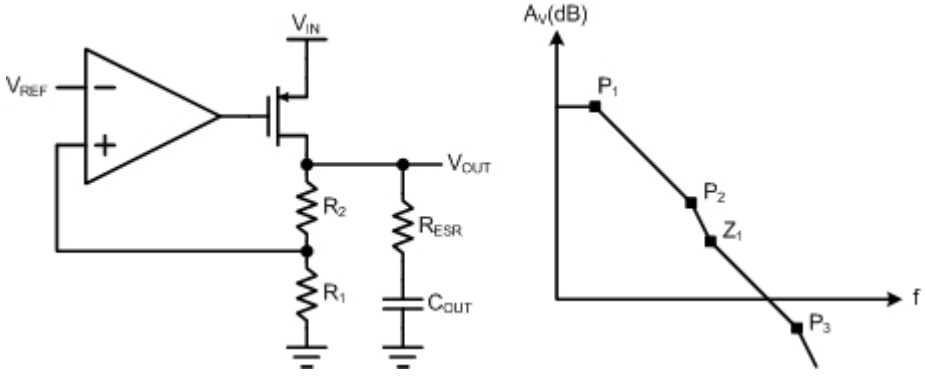

Figure 3: LDO Compensation using C_{OUT} ESR

Unfortunately, the ESR also adds an additional pole, P3 which should be at a higher frequency than the gain-bandwidth to have a stable LDO. As the ESR increases, the zero, Z1, moves to lower

frequency which is optimal to cancel out P2 but the pole P3 also decreases in frequency and can lower the overall phase margin. As ESR decreases, Z1 and P3 increase in frequency which can also decrease the phase margin, so typical LDOs specify a range of ESR values to have a stable LDO. Internal compensation can be used to eliminate the need of ESR for stability by using adaptive pole-zero tracking [7]. The presented research uses internal compensation to eliminate the need for ESR and also gives the user the option to use a very wide range of external capacitor values for a stable response. The fundamental concepts were used as building blocks to design the any-cap LDO.

C. LDO Linear Regulator Specifications

There are many specifications that characterize the performance of the LDO regulator. The LDO's DC specifications include load regulation, line regulation, dropout voltage, maximum load current, temperature drift, and current efficiency. The LDO's AC specifications include power supply rejection (PSR) and output noise. The LDO's transient performance includes overshoot, undershoot, and response time for a particular load step.

1. LDO DC Specifications

The load regulation is defined as how much the output voltage varies with load current which depends on the LDO loop gain, Aß, and the output impedance of the pass device, r_{op}. Figure 4 below is the diagram that can be used as reference for all the DC specifications.

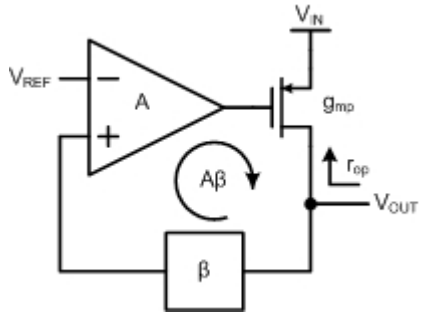

Figure 4: LDO Regulator Parameters

Ideally, the LDO output voltage is independent of load current. If the open-loop gain of the LDO was infinite, then the load regulation would be approximately zero. Also, the smaller the output impedance of the pass device, the better the load regulation. The load regulation is approximately the ratio of the pass device output impedance to the loop gain. Since the output impedance of the pass device can't really be controlled, the loop gain should be designed to be high for best load regulation.

The line regulation of the LDO is defined as the output voltage variation due to input voltage variation. The output voltage should be

independent of input voltage, so the ideal line regulation is zero. With a perfect input voltage reference, the dependent variables are loop gain, Aß, and the gain of the pass device, $g_{mp}r_{op}$. The line regulation is approximately the ratio of the pass device gain to the loop gain.

The dropout voltage of the LDO is defined as the minimum voltage drop across the pass device to maintain regulation. This tells the user what the minimum input voltage is for a particular output voltage. The dropout voltage is typically specified at maximum load current. At dropout, the pass device typically operates in the linear region, so the dropout voltage is the maximum load current times the on-resistance of the pass device.

The R_{DSON} of the pass device can be decreased by increasing the source-gate voltage, V_{SG}, and/or increasing the W/L aspect ratio. In practical circuits, the power rails to the IC are V_{IN} and ground, so the lowest the gate voltage can be is ground, implying that the maximum V_{SG} is V_{IN}. The channel length of the pass device is typically the minimum channel length of the process technology, so the channel width is controlled by the designer. The width is typically set by the die area constraint, so the size of the pass device is usually as big as it can be to fill up the maximum allowed die area. The main challenge in minimizing the R_{DSON} is being able to pull the gate as close to ground as possible.

The maximum load current specification usually determines the size of the pass device, dropout voltage, and power dissipation constraints. As the maximum load current specification increases, the overall die area of the pass device and the control circuitry increases and the ground pin current increases to be able to drive the additional parasitic capacitances of the increased device sizing. Meeting area and ground pin current specifications can be quite difficult if the maximum load current is rather high.

Ideally, the output voltage of the LDO or any linear regulator for that matter should remain constant over temperature changes. Any variations in the reference voltage over temperature and any error amplifier offset voltage will contribute to a temperature drift in the LDO output voltage.

The efficiency of any voltage regulator is very important. For the case of LDO regulators, it's best to look at current efficiency because the pass device voltage is simply the difference between input and output voltage making power efficiency of an LDO horrible if the input is much higher than the output. Ideally, the LDO will consume very little Q current even at light load currents, so that the input current is almost the same as the load current.

2. LDO AC Specifications

The power-supply rejection (PSR) is defined as how the output voltage changes with high frequency noise on the input voltage. Ideally, the output voltage doesn't vary with high frequency input noise, therefore the PSR would be zero. The PSR is dependent on the pass device's parasitic capacitances and LDO loop gain.

Since the LDO regulator consists of active devices that generate noise, the output of the LDO will have some noise even if the input rail has zero noise. The output noise is primarily dominated by the transconductance of the input devices in the error amplifier. In general, the larger the g_m of the input devices, the lower the output noise. The output noise specification of the LDO is very important for RF applications because the noise can interfere with the high frequency signals.

3. LDO Transient Specifications

There are two types of transients; load and line. Load transients occur when the output current rapidly changes levels, such as a 1mA to 200mA step in load current. Line transients are when the input voltage rapidly changes levels, such as a 4V to 5V step. Line

transient is also part of the PSR specification. For both load and line transients, important specifications are overshoot, undershoot, and response time and are usually shown as a plot with a particular output capacitor.

D. Any-Cap LDO Linear Regulator

As previously mentioned, the any-cap LDO regulator gives the user complete flexibility with choosing the output capacitor. The any-cap LDO should be stable with any output capacitor value ranging from 0 – 1μF. This requires the analysis of LDOs requiring an external capacitor and cap-less LDOs to understand merging the two topologies together. Conventional LDOs use roughly a 1μF output capacitor and the cap-less LDOs typically have 100pF on internal capacitance at the output [3]. If the dominant pole is set by the output of the error amplifier and the 2nd pole is set by the output pole, then the gain-bandwidth of cap-less LDOs is generally higher than conventional LDOs. The above comments are illustrated in the figure below.

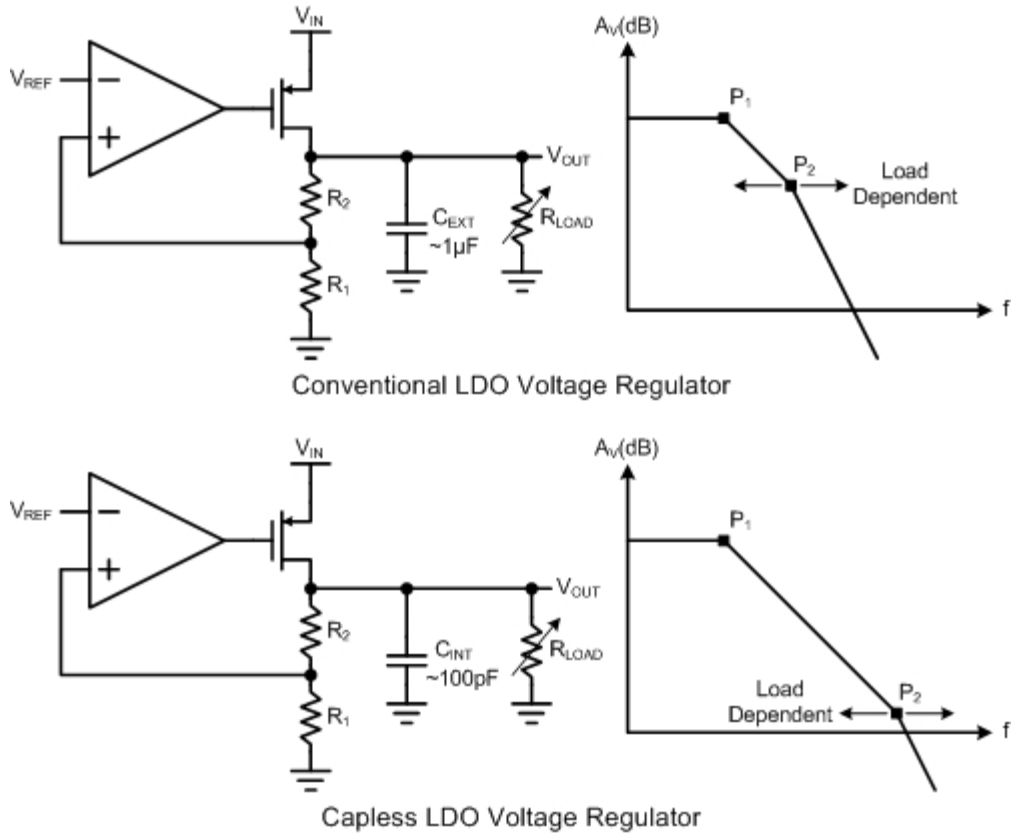

Figure 5: Conventional and Cap-less LDO Regulator Poles

As the load current increases, the output pole, P2, pushes to higher frequency making the compensation easier for higher load currents. Proper compensation pushes the dominant pole, P1, to much lower frequency such that the LDO is stable over the entire load current range. This would imply that the conventional LDO should be stable with extremely small output capacitors since P2 resides at much higher frequency than the conventional LDO. However, this isn't the case due to other parasitic poles moving lower in frequency and 2nd

order and/or complex pole peaking occur as the output capacitor decreases causing instability.

A high bandwidth provides for faster transient response. A cap-less LDO can be stable with a relatively high bandwidth, however conventional LDOs are typically not stable due to the output pole residing at much lower frequency. Thus the focus of this research starts with the design of a conventional LDO regulator and then designing the necessary circuits to facilitate stability for the any-cap LDO.

E. Previous Academic Work

Numerous work has been done on conventional LDO regulators. The common concept to improve the conventional LDO is to add a zero in the loop which cancels the load pole (pole/zero tracking). The papers concentrate on different methods for the pole/zero tracking. The most straight forward approach is to add a series RC in the loop where the R varies with load current [7]. An example is shown in the diagram below.

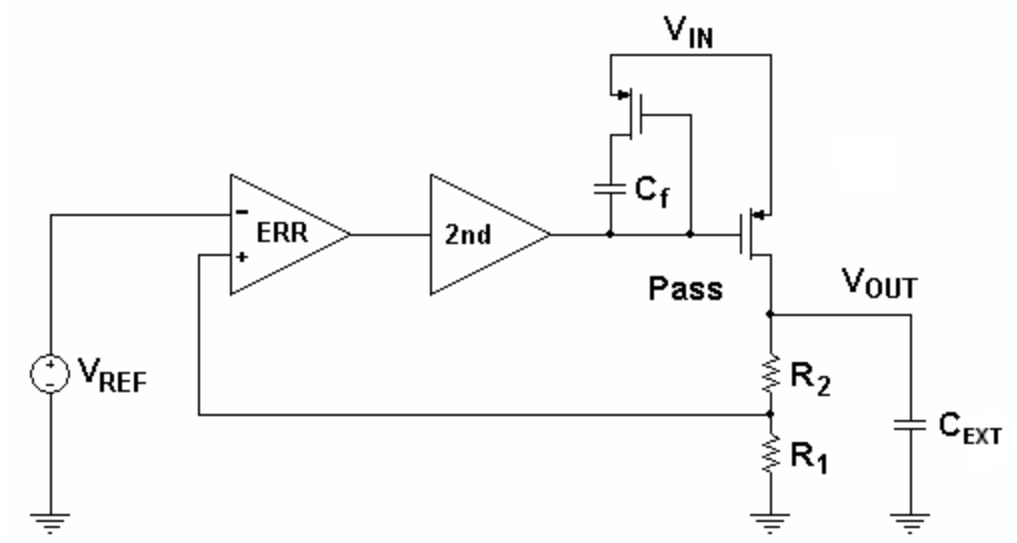

Figure 6: Pole/Zero Tracking LDO

The PMOS which drives the capacitor, Cf, acts as a linear resistor which varies with the load current since it mirrors the current of the pass device. Care must be taken if using this approach because this method may not be stable over the entire load current range. It's also common to see miller compensation where a capacitor is placed from Vout to the output of the error amplifier. This makes the dominant pole change with load current because the gain of the pass device changes with load current.

Cap-less LDO publications have been ramping up over the recent years with the demand of fully integrated solutions. The design tends to be more difficult than designing conventional LDOs because the large signal transient response isn't nearly as good due to the absence of the large output charge storage device. One example of

published for a cap-less LDO uses a DFC block to set a fixed internal dominant pole [2]. The LDO architecture is shown below.

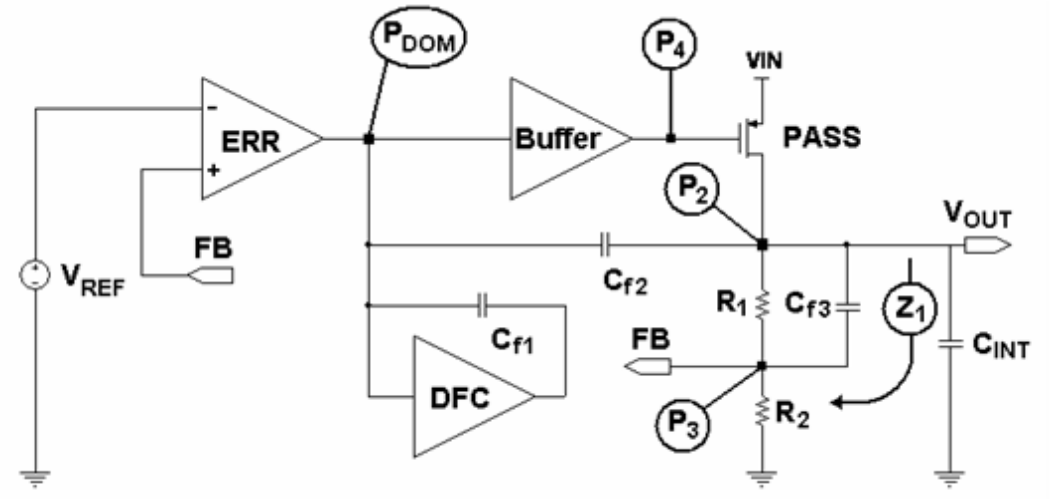

Figure 7: Cap-less LDO

The capacitor Cf1 creates a pole/zero pair where the zero cancels out the load pole P2. Below is the location of the poles and zeros.

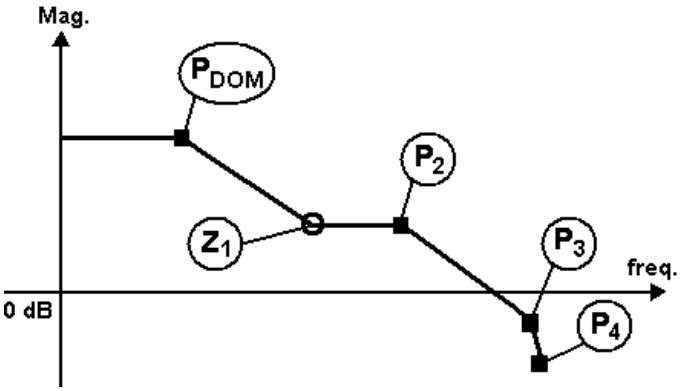

Figure 8: Poles & Zeros Locations for Cap-less LDO

As with every design, there are some problems with this LDO. Since P2 is located fairly close to the cancelation zero Z1, the effect of cancelling out the load pole is greatly reduced. Also, Z1 does not move

with load current and can cause stability problems because the load pole can move by several decades. This is mainly evident at light load conditions as this LDO is not stable with load currents less than 10mA.

F. Any-Cap LDO Design Direction

A new LDO architecture is needed to have a LDO that is stable with good transient response for output capacitors ranging from 0 – 1µF. Starting from a conventional LDO design where an output capacitor is present, a fast feedback path is required to give the LDO good transient response for light and cap-less loads. The fast feedback path must slew the gate of the pass device very quickly since the bandwidth is fairly low and cannot offer a fast enough response when the output capacitor is very small. Also, the LDO should be stable at light load currents. The initial architecture for the any-cap LDO is shown in the figure below.

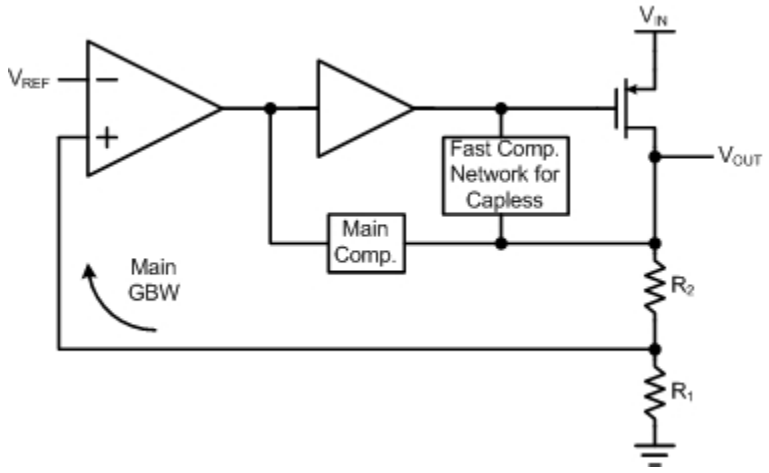

Figure 9: Initial Any-Cap LDO Design Architecture

The LDO architecture without the fast compensation network is pretty much the same architecture as most conventional LDO designs. The fast compensation network is needed to quickly slew the gate of the pass device when the output capacitor is small. The compensation network itself may need to be compensated due to its high speed. The fast network must be faster than the gain-bandwidth in order for the loop to remain stable.

This architecture sets the foundation for the presented research. The full analysis and design is presented in the next chapter.

CHAPTER II

ANY-CAP LDO REGULATOR ANALYSIS

The any-cap LDO regulator will attempt to combine a miller-compensated LDO and a cap-less LDO. The stability of these two LDOs must be analyzed before designing the any-cap LDO. Let's first take a look at the miller-compensated LDO. Figure 10 shows a block diagram of a miller-compensated LDO consisting of an error amplifier, voltage buffer, and PMOS pass device [6][2].

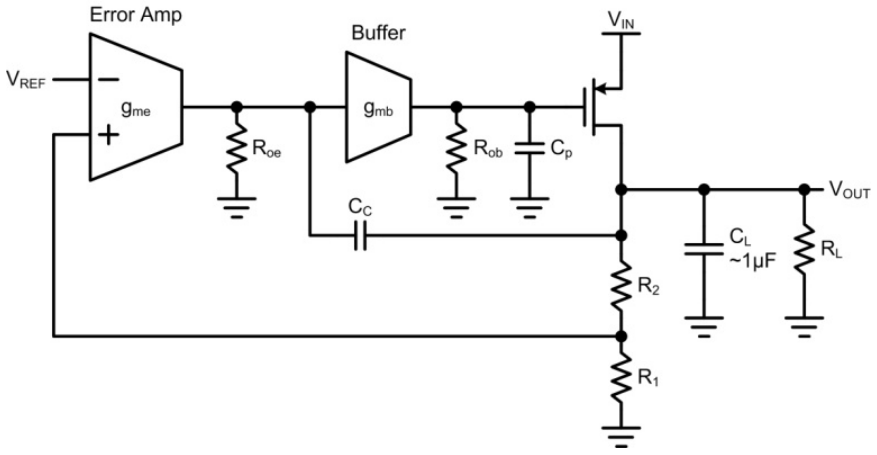

Figure 10: Block Diagram of a Miller-Compensated LDO Regulator

Poles exist at each of the gain stage outputs; error amplifier output, buffer output, and the LDO's output. Figure 11 shows the relative locations of the 3 poles.

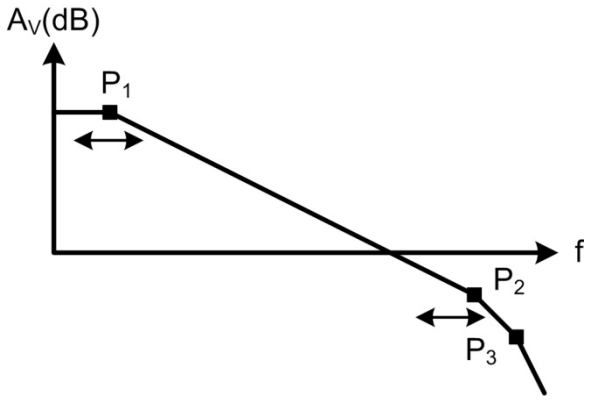

Figure 11: Pole Locations for Miller-Compensated LDO Regulator

The dominant pole, P_1, sits at the output of the error amplifier and varies with load current. The miller compensation capacitor, C_C, changes its effective capacitance seen at the output of the error amplifier with the gain of the pass device, which changes with load current. The equation for P_1 is below:

$$P_1 = \frac{1}{2\pi R_{oe} C_C \left(1 + A_{VB} A_{VP}\right)} \tag{1}$$

where A_{VB} is the gain of the buffer and A_{VP} is the gain of the pass device. A_{VP} reduces with increased load current.

The 2nd pole, P_2, is the output pole which varies with load capacitance and load current. The equation for P_2 is below:

$$P_2 = \frac{1}{2\pi \left(R_L \,//\, \left(R_1 + R_2\right) // \, r_{oP}\right) C_L} \tag{2}$$

where r_{oP} is the output resistance of the pass device. The output resistance of the pass device is inversely proportional to the load current or directly proportional to the load resistance, R_L.

P_3 is the pole at the output of the buffer which varies with load current. The parasitic capacitance at the output of the buffer, C_P, is mainly the capacitance of the pass device and the self miller capacitor of the device changes with the gain of the pass device. The equation for P_3 is below:

$$P_3 = \frac{1}{2\pi R_{ob} C_p} \tag{3}$$

It's convenient that these 3 poles vary in the same direction with load current because making the LDO stable with no load is fairly simple using miller compensation. It's obvious that if C_L increases beyond a certain point, the LDO will become unstable because it starts to approach the dominant pole frequency. However, it appears that C_L could decrease to zero and the LDO should remain stable, but that's not the case since the output pole is used to suppress all other poles beyond unity-gain frequency.

As the output capacitor decreases, the unity-gain bandwidth of the LDO needs to increase to have good transient performance. This implies that the pole at the output of the buffer must increase to maximize the UGF. Figure 12 shows a diagram of a cap-less LDO.

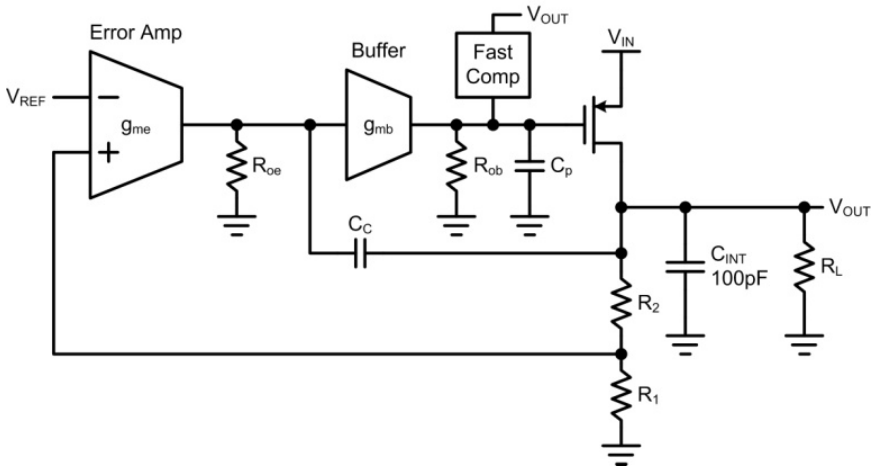

Figure 12: Block Diagram of a No-Cap LDO Regulator

The cap-less LDO still uses miller compensation and the output capacitor is replaced with an internal 100pF capacitor. Also, the output resistance of the buffer, R_{ob}, should decrease in value compared to the miller-compensated LDO to push its pole to higher frequency. In order to improve transient performance, a fast compensation network may need to exist at the gate of the pass device.

The relative locations of the 3 poles should remain the same as the miller-compensated LDO, but the pole frequency should increase to maximize the UGF to get the best transient performance. Perhaps the fast compensation network doesn't affect the AC frequency response, but improves the transient performance.

It seems like an any-cap LDO can be achieved by combining the miller-compensated LDO with the cap-less LDO. Some work may need

to be done to stabilize the LDO with moderate output capacitors. Merging these two circuit problems creates a difficult design challenge.

It seems impractical to make an LDO stable with zero to infinite output capacitance, since the output pole would vary by an infinite magnitude. A more practical design target would be to design the LDO to be stable with zero output load capacitance to 1's of μF.

For stability, the UGF of the any-cap LDO should be high for low value output capacitors and low for high value output capacitors. This implies that the dominant pole should ideally track the output pole (load current and output capacitance). Making the dominant pole move that much can be quite difficult since for a given load current, the output pole can vary by as little as 10^4 (assuming a minimum 100pF internal capacitance and a maximum 1μF output capacitance). An alternative method is to add a zero that cancels out the output pole, which poses the same problems as having the dominant pole perfectly track the output pole.

Another design challenge with any LDO is open-loop DC gain vs. stability. In general, the lower the gain, the easier it is to stabilize the loop [2]. The downside of decreasing the loop gain is the load regulation reduces.

The design target for the presented LDO is a 2.5V output, 200mA max output current, 200mV dropout, load regulation < 0.5%, and stable with zero output capacitance to 1's of μF.

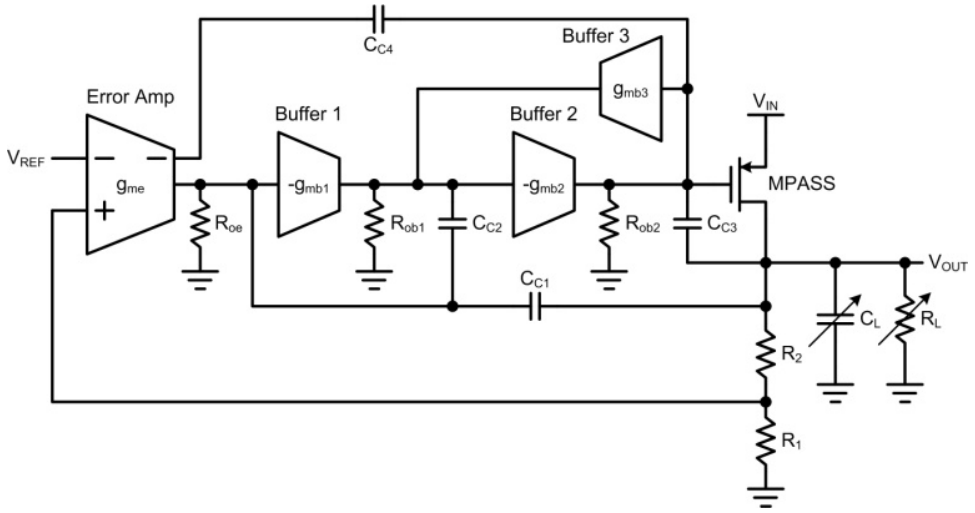

Figure 13: Block Diagram of Initial Any-Cap LDO Regulator

The compensation capacitor, C_{C1}, is the miller compensation capacitor and sets the dominant pole [4]. The capacitor, C_{C2}, is a local feedback compensation capacitor for the gain stage formed by $g_{mb1}R_{ob1}$. The capacitor, C_{C3}, is the 100pF internal capacitor. Connected the way it is, C_{C3} is more effective than placing it from V_{OUT} to ground as in the traditional cap-less LDOs. Capacitor C_{C4} is a small value capacitor to improve transient response for higher cap loads.

CHAPTER III

ANY-CAP LDO CIRCUIT DESIGN

For starting the circuit design, the block diagram in Figure 12 will be the starting point. The topology for the error amplifier and buffer must be decided.

A. Error Amplifier Topology

The threshold voltage of the NMOS devices on this process is 0.75V, so with a 1.25V reference, using an NMOS input pair on the error amplifier is adequate. Having an NMOS input pair can be beneficial because the g_m of NMOS devices is 2 – 3 times higher than comparable PMOS devices, which translates to a higher LDO bandwidth. Now that the input pair is decided, it's time to pick the OTA (operational transconductance amplifier) structure. The simplest OTA would be the current mirror load with differential input pair as shown below in figure 14.

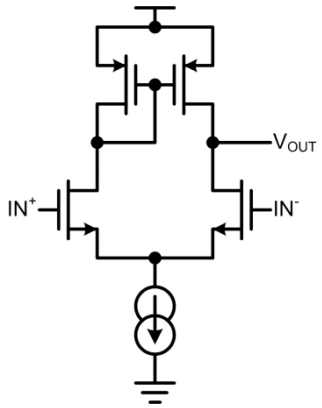

Figure 14: NMOS Differential Pair with PMOS Current Mirror Load OTA

This OTA is small and simple which has the advantage of fewer poles and zeros. The output cannot swing rail to rail which might be ok. To optimize PSR, the output should drive a rail referenced device such as the gate of a PMOS with the source tied to the top rail. Another consideration is the connection of the miller compensation capacitor in the LDO. It connects from the LDO output to the output of the error amplifier. If this amplifier is used, then the miller capacitor would connect between a ground referenced voltage (Vout) and a rail referenced voltage (output of error amplifier) which is bad for PSR. To fix that, the NMOS input pair could be cascoded and the miller capacitor can connect to the source of the cascode device that's in the signal path of the error amplifier output as shown in Figure 15.

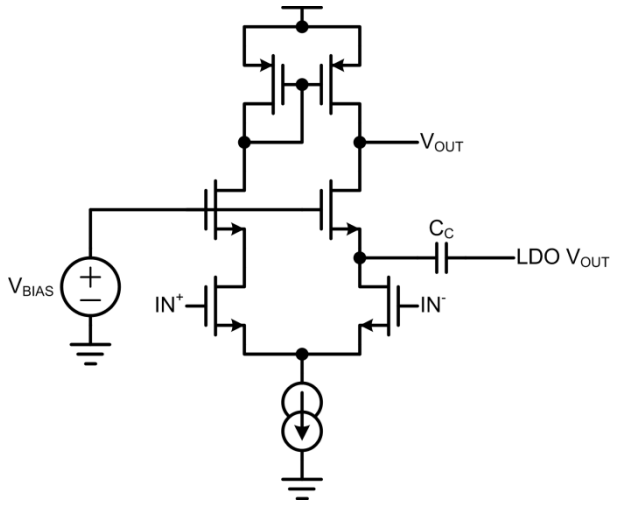

Figure 15: Modified Circuit from Figure 13 of How to Connect C_C

Cascoding the input pair causes the gain to increase a bit because the output impedance increases. Connecting the compensation capacitor in this manner can be called cascode compensation. Often times, the compensation capacitor can decrease in value compared to the traditional miller compensation because the current through C_C gets gained up by the g_m of the cascode device. Adding the cascode devices decreases the output swing a bit. Since the buffer stage isn't defined, some wide output swing OTA's should be explored.

There are a couple different OTA architectures that converts the previous OTA design to have wide output swing. One is the folded cascode OTA and the other is the current mirror OTA. The current mirror OTA has the nice advantage of easily adjusting the amplifier's g_m with keeping the DC gain the same. The circuit below is the

current mirror OTA with adding cascode devices in the output's signal path for adding the LDO's compensation capacitor.

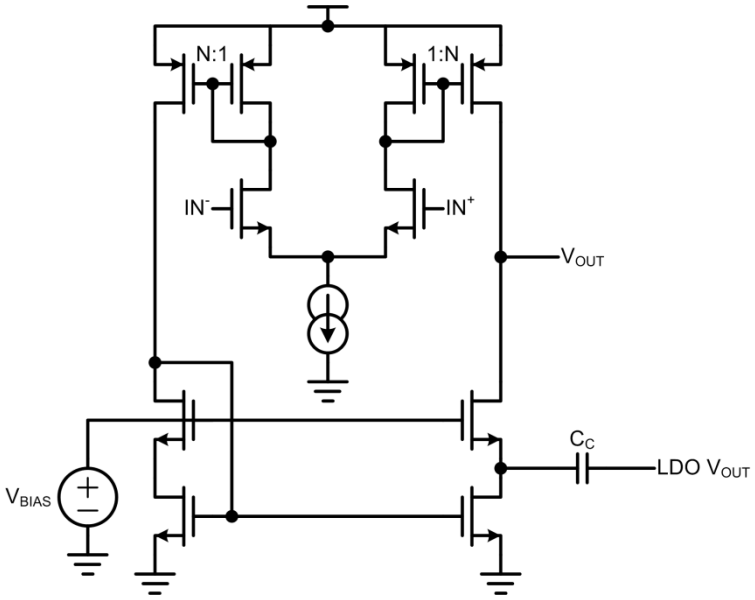

Figure 16: Current Mirror OTA

The output swing of the current mirror OTA is pretty close to rail-to-rail. The g_m of the amplifier can be adjusted by varying the PMOS mirror ratio, N. The DC gain however does not change as N changes because the output impedance is inversely proportional to the current through the output stage. Now onto the folded cascode amplifier.

The folded cascode amplifier also achieves wide output swing but with fewer devices than the current mirror OTA. The DC gain of all 3 of these OTAs would be roughly the same, although this folded cascode OTA would have the highest gain due to the pull-up and pull-

down current sources in the output stage being cascoded. Below is one way to draw a folded cascoded OTA.

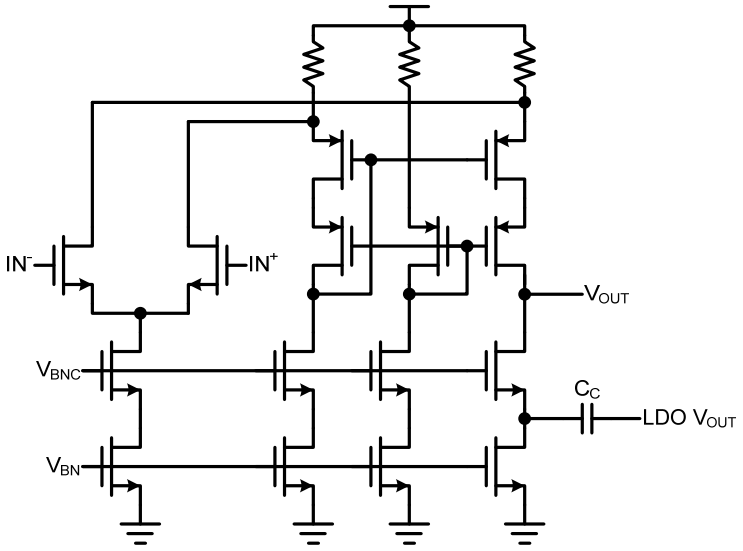

Figure 17: Folded Cascode OTA

Since the drain voltages of the NMOS differential pair is an IR drop below the rail as opposed to a VGS of a PMOS as in the previous OTAs, the folded cascode OTA has a wider input range. Since the threshold voltage of the PMOS devices is 1.25V on this process, using the folded cascode OTA could lower the minimum operating VIN voltage for the LDO. The way the folded cascode is drawn, it's meant to drive the gate of a PMOS device since the output stage has a PMOS mirror. If the folded cascode needs to drive the gate of an NMOS device, it's easy to reconfigure the output stage to have an NMOS mirror rather than a PMOS mirror. It seems like the folded cascode

OTA will be the best and most versatile choice for the LDO error amplifier.

B. Buffer Topology

Now that the error amplifier topology is chosen, it's time to decide on the topology of the buffer. In order to use miller compensation, the buffer must be non-inverting. Since the buffer is driving the gate of the PMOS pass device, which could be high capacitance, it may be necessary to make the output of the buffer low impedance so that the gate of the pass device doesn't introduce a low frequency pole. The simplest low impedance buffer is a source follower as shown in figure 18 below.

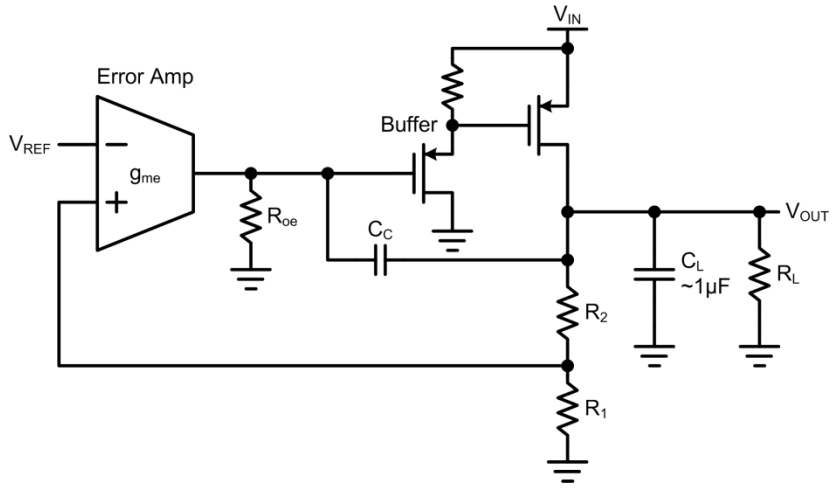

Figure 18: LDO with Source-Follower Buffer Stage

The obvious drawback to this buffer is voltage headroom. As previously mentioned, the threshold voltage for PMOS devices on this

process is 1.25V, so if the output of the error amplifier could pull down to 0V, then the lowest voltage on the gate of the pass device would be 1.25V. Since the LDO's output voltage is 2.5V, the minimum VIN would be a maximum of 2.5V, implying that the pass device would barely be able to turn on with a PMOS source follower buffer stage.

A way to improve the source-follower buffer is to use a diamond buffer which is an up-down buffer in parallel with a down-up buffer. The diamond buffer in the LDO is shown in figure 19.

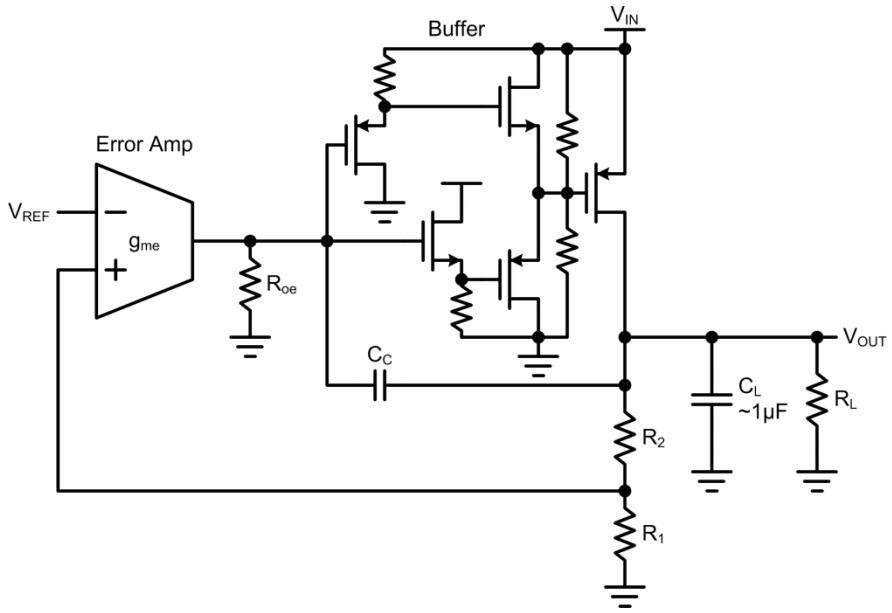

Figure 19: LDO w/ Diamond Buffer Stage

First off, the 4 resistors in the diamond buffer can be replaced with current sources to ensure the VIN pin current can drop to zero if the LDO is in shutdown. This buffer does solve the headroom problem of the source-follower buffer, however, since the threshold voltage of the

PMOS and NMOS are quite different (1.25V and 0.75V respectively), there could be some dead time of the buffer and/or some odd stability problems during transition of the NMOS turning on and PMOS turning off or vice versa.

Two non-inverting buffers without inversion stages have been explored and ruled out. An alternative non-inverting buffer is to cascade two inverting gain stages. Below is two inverting gain stages cascaded to make a non-inverting buffer.

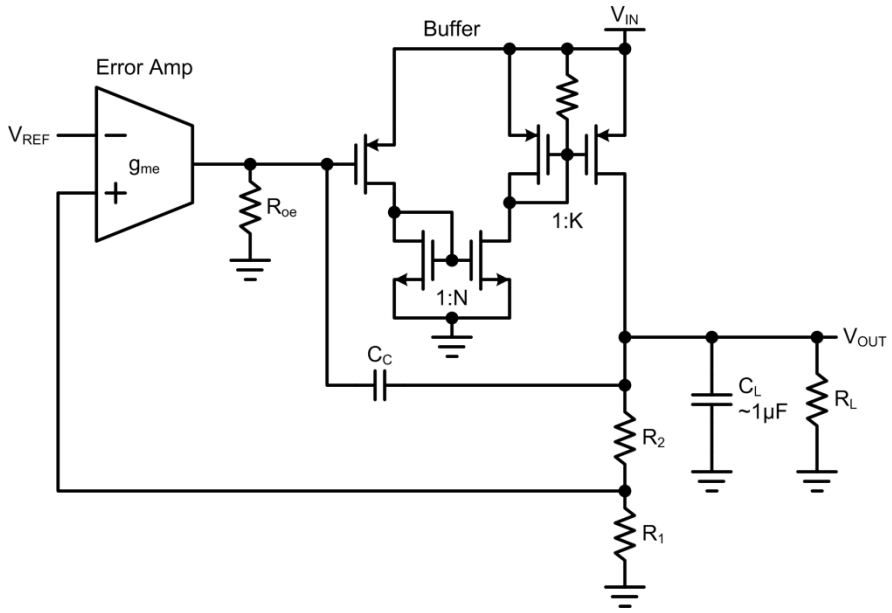

Figure 20: LDO w/ Dual Inverting Buffer Stage

This buffer easily satisfies the headroom requirement as the NMOS device can pull the gate of the PMOS pass device nearly to ground. With an NMOS pulling down on the gate of the pass device, the pull-down strength is very fast. In the event of the load stepping from low

to high, the NMOS can slew the gate of the pass device very quickly. However, when the load steps from high to low, the pull up speed of the pass device is primarily set by the pull-up resistor from the gate to VIN and the parasitic capacitance of the pass device, which is slower than the pull-down speed. This may be fine for the case of higher load capacitances but it could cause large overshoots in the case of very small load capacitances. An open-loop speed enhancer may be needed to address this issue. The gain of this buffer is relatively low, possibly even less than 1 because the load of each inverting stage is a diode connected device. This buffer satisfies the voltage headroom requirement and also has the benefit of being able to adjust the gain, so this buffer topology will be used.

Now that the error amplifier and buffer topologies are chosen, below is the preliminary LDO design.

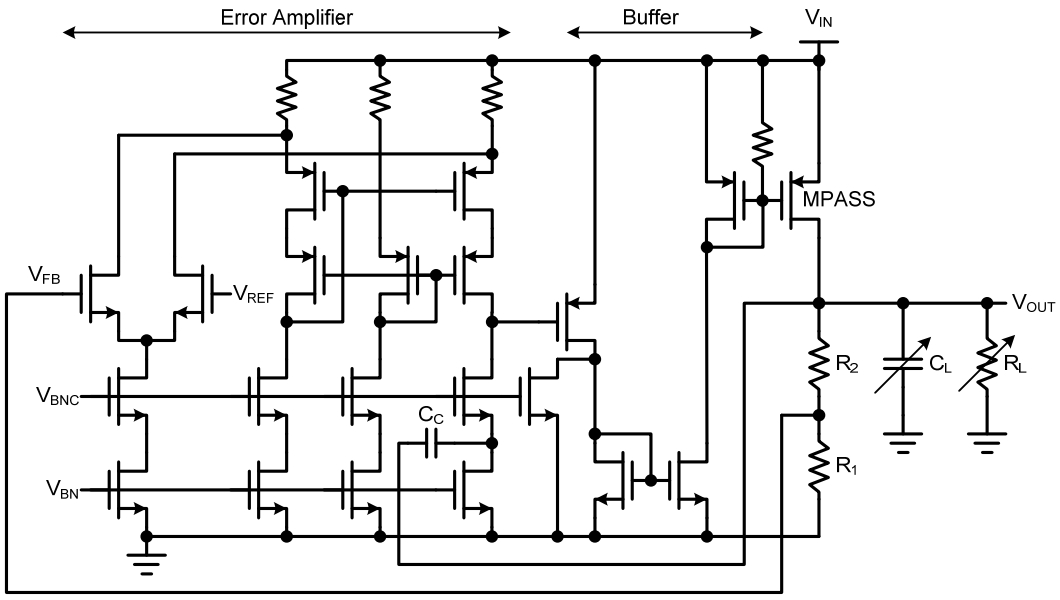

Figure 21: Initial LDO Topology Design

C. Error Amplifier Transistor Design

In order to design the error amplifier, a general idea about device sizing should be understood. For starters, the input pair should be sized for high g_m, so a high W/L ratio. The PMOS mirror can affect the gain of the error amplifier, so the higher the g_m, the higher the gain of the amp. The current source load in the output stage of the error amp should just be sized for good matching. The output impedance of the current sources will be high since they're cascoded. A rough, 1st order equation for the DC gain of the error amplifier should be defined to understand the parameters to adjust for DC gain.

This particular folded cascode amplifier has a slightly different DC gain equation than the traditional folded cascode where the resistive load on the input pair is replaced with current sources. The traditional folded cascode amplifier has a DC gain of $g_m R_O$, where g_m is the input pair g_m and R_O is the output resistance on the output stage. This folded cascode amplifier has 2 gain terms due to the resistive load on the input pair; $(g_{mI}R)\bullet(g_{mP}R_O)$ where g_{mI} is the input pair g_m, R is the resistive load, g_{mP} is the g_m of the PMOS mirror, and R_O is the output resistance of the output stage. This gain assumption will be verified or altered after running AC simulations on the error amplifier.

Choosing input pair tail current and output stage current sources to be 10μA each, some device sizing can be chosen. The input pair should be high gm or high W/L so choose 200/2. The PMOS mirror could also be high gm so choose 100/2. The NMOS current sources should match fairly well so choose 40/10 for the rail devices and 50/2 for the NMOS cascode devices. Below is the folded cascode error amplifier with device sizing labeled.

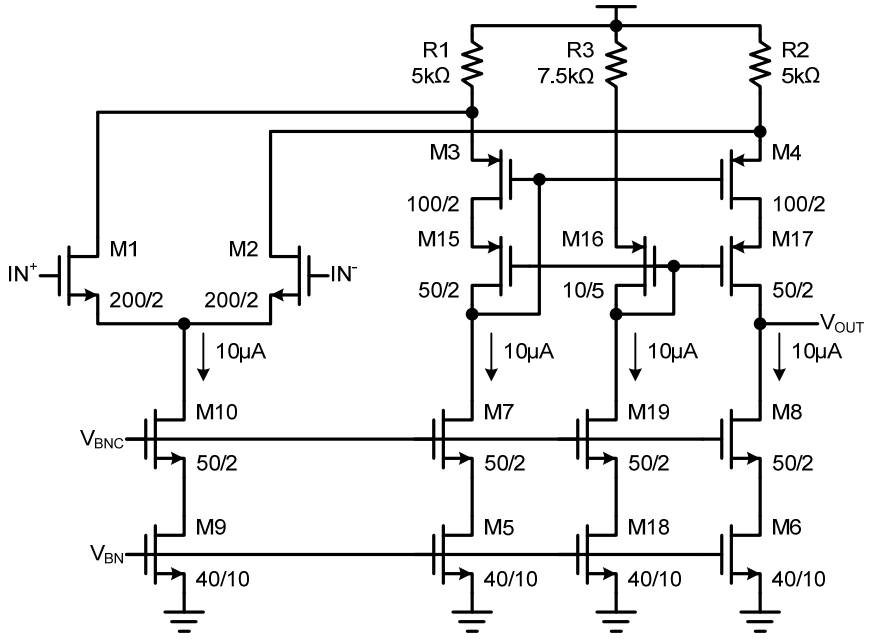

Figure 22: Folded Cascode Error Amplifier w/ Device Sizing and Currents

Running AC simulations can give the DC gain, Gm, and R_O of the amplifier. Simulations show the input pair g_m to be about 54µA/V and the DC gain is ~67dB. So far, this circuit seems quite viable for the LDO. There's no point in diving into this further because the performance needs to be looked at in the entire LDO circuit.

D. Buffer Transistor Design

The gain of the buffer stage is related as ratios of g_m's and can be made to have a gain of greater than or less than unity. The mobility of electrons is about 3 times greater than the mobility of holes which implies that a PMOS device should have 3 times the current density

(I_D/W/L) of a NMOS device to give the same g_m. First thoughts would be to design the gain of the buffer to be roughly unity. However, considering how the buffer is being used, the buffer is mirroring the LDOs load current. If the gain of the buffer is unity, the current through the buffer could get quite high at heavy loads. The output impedance of the buffer should be low which would imply that the buffer would consume a lot of current at heavy loads. As the gain increases above unity, the current consumption in the buffer would decrease. So, initial design of the buffer will have a gain of roughly 5V/V. Below is the schematic of the buffer with device sizing.

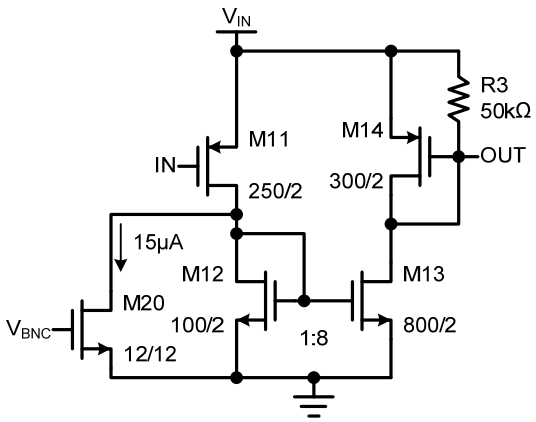

Figure 23: Buffer w/ Device Sizing and Currents

Based on sizing inspection, the gain of this buffer, neglecting R3 (since the $1/g_m$ of M14 will be much lower than R3), would roughly be $\left(\frac{250/3}{100}\right)\bullet\left(\frac{800}{300/3}\right)=8\bullet\left(\frac{250}{300}\right)=6.67=16.5dB$. Simulations show the gain of the 1st stage (M11 to M12) to be 24.4dB and the 2nd stage is 5.7dB (M13 to

OUT) for a total gain of 30.1dB (32V/V). The gain of the buffer is much higher than expected because at light load currents, the NMOS mirror is doing very little current, whereas M11 is conducting at least 15μA which causes the gain of the 1st stage of the buffer to be quite high at light loads. The gain of the 1st stage decreases as the load current increases. A way to reduce the gain of the buffer without affecting the current consumption would be to source degenerate the input PMOS, M11. This will be done if needed.

E. Pass Device Design

The PMOS pass device should be sized for dropout. The goal is to have an LDO capable of delivering up to 200mA with a dropout voltage of 200mV which implies the on-resistance of the pass device should be 1Ω. Since the regulated output voltage is 2.5V, the pass device should be 1Ω when the input voltage is 2.5V. The NMOS device in the buffer stage, M13, can't pull the gate of the pass device all the way to ground, so assume it can pull down to 400mV which gives a V_{SG} of 2.1V. Without giving process parameters, the size of the pass device is 85000/2. Now it's time to build the LDO.

F. Initial LDO Design

The basic building blocks of the error amplifier, buffer, and pass device have been designed, and the complete LDO schematic without compensation is shown below.

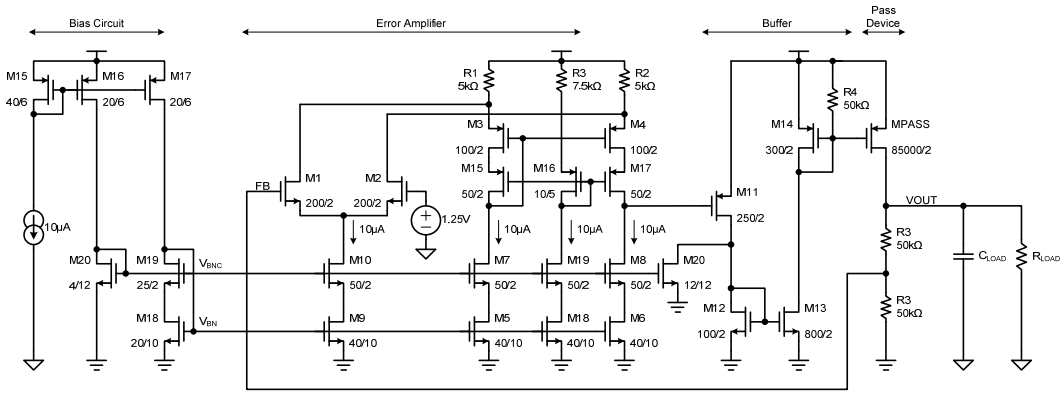

Figure 24: Initial LDO w/ Device Sizing

The gate-source connection of M15 in the bias circuit is pinned out, so the 10µA current source is external. The 1.25V reference is an external reference as well. The first thing to look at is to make sure the output voltage goes to the right DC voltage. Even though it's not compensated yet, a DC simulation doesn't care about stability because all caps act as if they're open. With a 1.25V input, the output goes to 2.5006V which indicates the open-loop gain is relatively high. The next thing to look at is AC simulations so that the LDO can be compensated.

Below is the setup used to run the AC simulations:

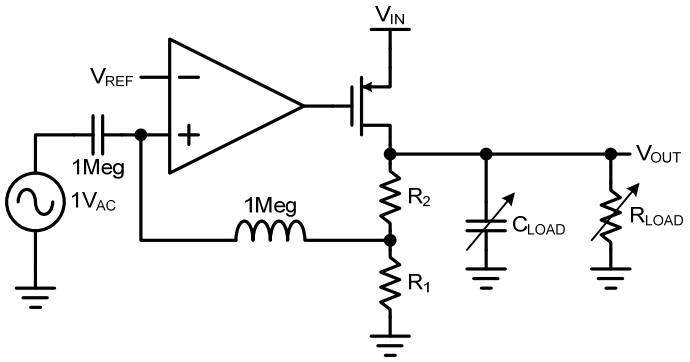

Figure 25: LDO Regulator AC Simulation Setup

Bode plots are shown below for the initial LDO design. The load current is stepped from 1mA to 200mA and output capacitors are stepped from 0 to 1µF.

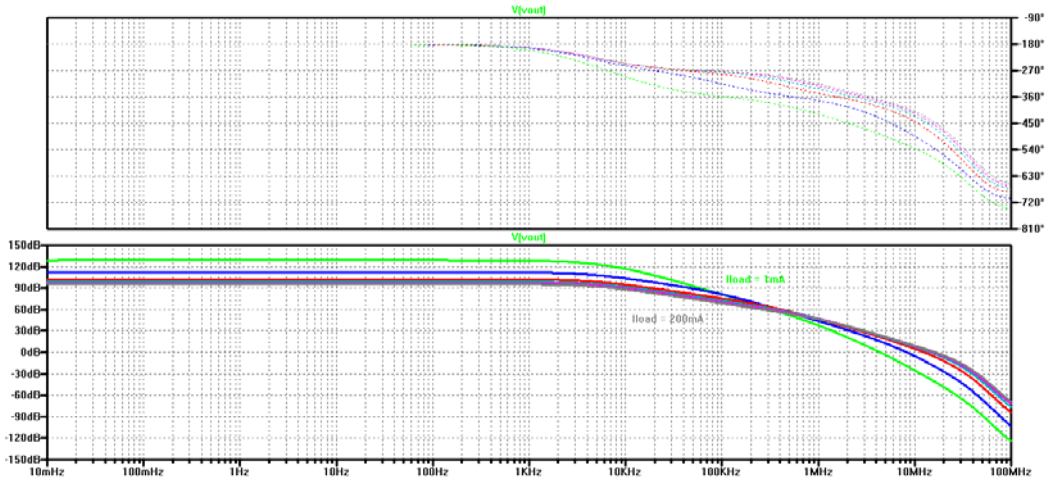

Figure 26: Uncompensated LDO Bode Plot with Load Current stepped from 1mA to 200mA and the output cap is 1nF

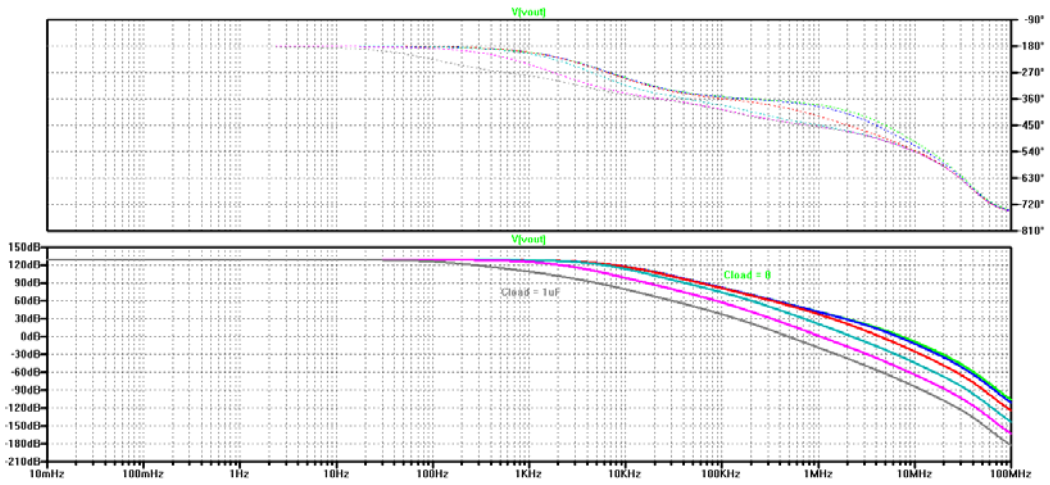

Figure 27: Uncompensated LDO Bode Plot with Output Cap stepped from 0 to 1µF with a 1mA Load Current

As expected, the LDO is unstable as the phase margin is well below 0°. The DC gain with 1mA load is ~128.8dB which should give pretty good load regulation. The gain of the error amplifier, buffer, and pass device is 66.6dB, 30.1dB, and 32.1dB respectively. Now it's time to compensate the LDO.

G. Compensating the LDO

The first compensation method to try is miller compensation. This involves connecting a capacitor across an inverting gain stage and typical miller compensation for an LDO has one end of the capacitor connected at the LDO's output. Below is the revised schematic with the added miller cap and the bode plots.

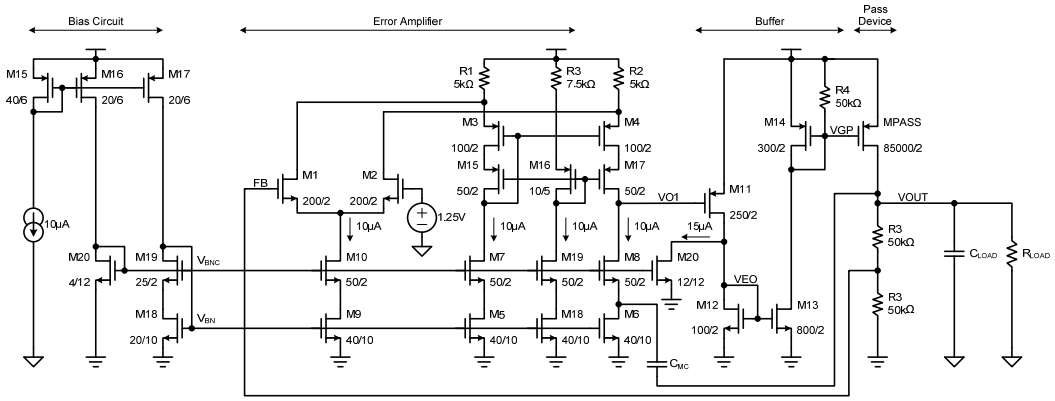

Figure 28: Initial LDO Schematic w/ Miller Compensation

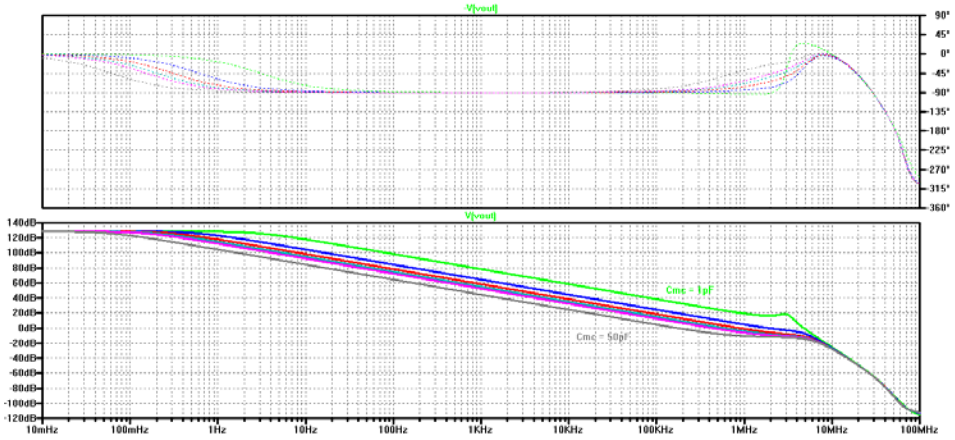

Figure 29: Bode Plot with Cmc stepped from 1pF to 50pF at 1mA load and 1nF Output Cap

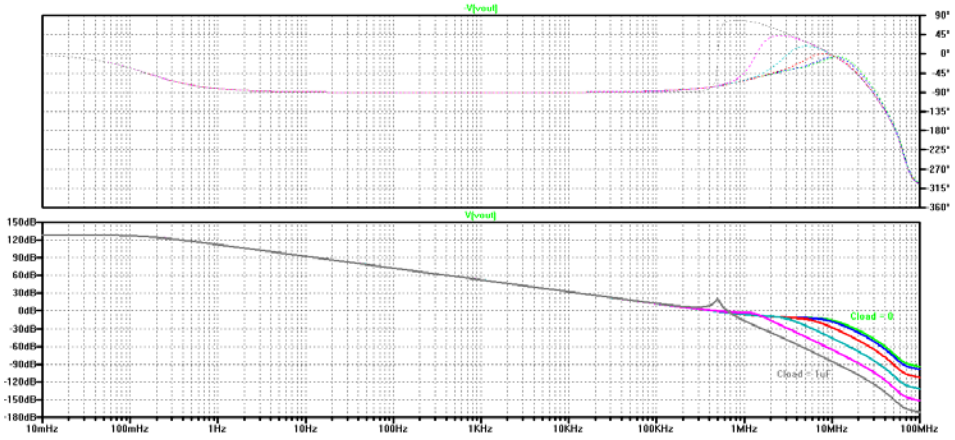

Figure 30: Bode Plot with Cmc at 20pF and 1mA Load and Output Cap stepped from 0 to 1µF

It seems like the LDO is unstable due to the phase going from -90° to just ~0° rather than going more negative. A transient simulation is run just to prove the instability. Reducing the gain is one way to improve the stability of the LDO.

The gain of the error amplifier or the buffer could be reduced. The gain of the pass device can't be reduced because it's sized for dropout. For better input referred offset of an amplifier, it's better to have the highest gain in the 1st gain stage as opposed to the later stages because you don't want to amplify the offset of the 1st gain stage. So, the gain of the buffer will be reduced by lowering the g_m of the PMOS M11 in the buffer. Rather than reducing the aspect ratio of M11, degenerating can reduce the g_m. After running the AC simulations, the frequency response looks pretty much the same but the gain of the LDO reduces to ~123.8dB. It's good to look at the AC response of the LDO during the initial design phase, but I like to compensate the LDO by looking at the transient response after investigating the AC response.

H. Compensating by Transient Performance

Simulating a load step on the LDO gives the true stability of the closed system, whether the load step is small or big. AC simulations

show the small signal response of the LDO and may not indicate what the response would be with a large load step. First, the load step will be looked at with a 1mA to 200mA step with a 100nF output cap. After the LDO looks good with 100nF output cap, the output cap will be reduced to zero. Below is the transient response with the miller compensation and reduced gain buffer.

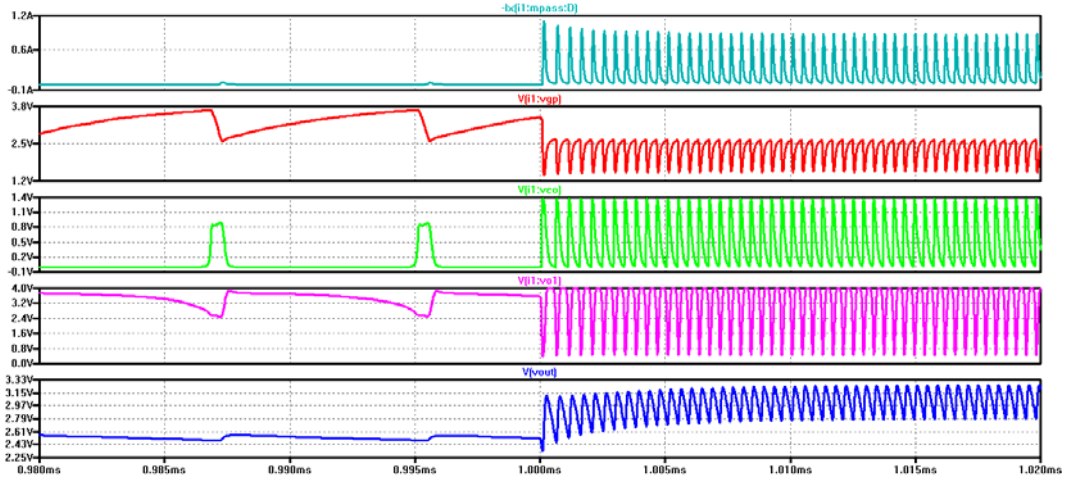

Figure 31: 1mA to 200mA Load Step w/ 100nF Output Cap

Clearly the LDO is unstable. From top to bottom, this plot shows the pass device drain current, the gate voltage of the pass device, the gate of the NMOS mirror in the buffer, the output voltage of the error amplifier, and the LDO's output voltage. The load current steps from 1mA to 200mA. The frequency of oscillation is 120kHz and 2.4MHz when the load current is 1mA and 200mA respectively. When the load current is 200mA, the output of the error amp and gate of the NMOS mirror in the buffer is slewing pretty quickly and indicates that

those nodes need to slow down. Below is a transient simulation with adding a 10pF cap from VEO to the same cascode node that the main miller cap is connected to.

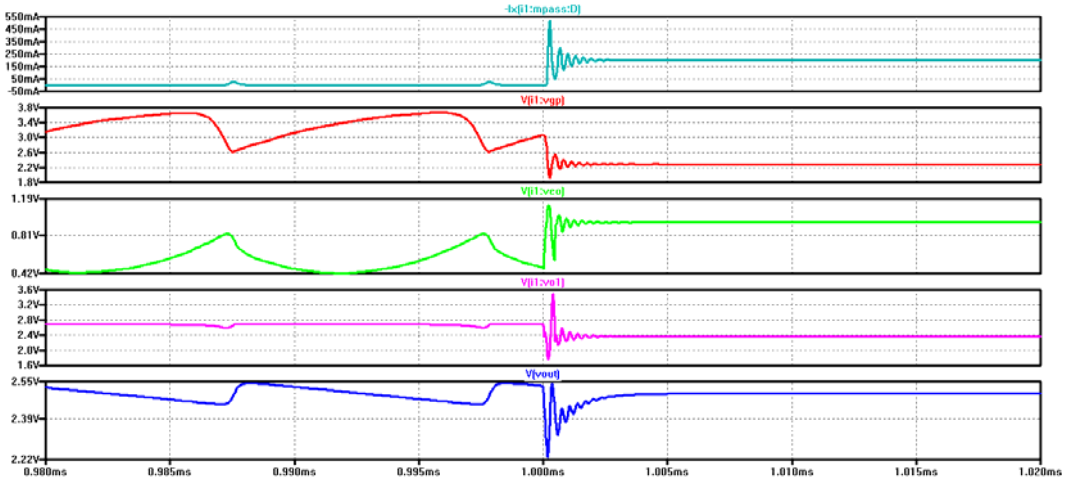

Figure 32: 1mA to 200mA Load Step w/ 100nF Output Cap with additional compensation around M11

The stability of the LDO is better than the previous run. At 200mA, the LDO settles out and is stable, given the stability isn't great because there's still some ringing right after the step. The LDO is still unstable at 1mA but the output of the error amplifier looks better as the voltage is bounded in a smaller window.

Compensating the LDO at light load current is more difficult than with high load current because the open-loop gain is higher [3]. In fact, reducing the open-loop gain might be enough to stabilize the loop at light load because the previous run was heading in the right direction of stability. Reducing the g_m of the PMOS mirror in the error

amplifier is one way to reduce the gain of the loop. This is done by degenerating the PMOS mirror with 30kΩ. When doing this, the bias of the cascode voltage needs to change as well (i.e. changing R3 to 37.5kΩ). Below is the new schematic and transient plot with this change as well as the added 10pF cap added in the last step.

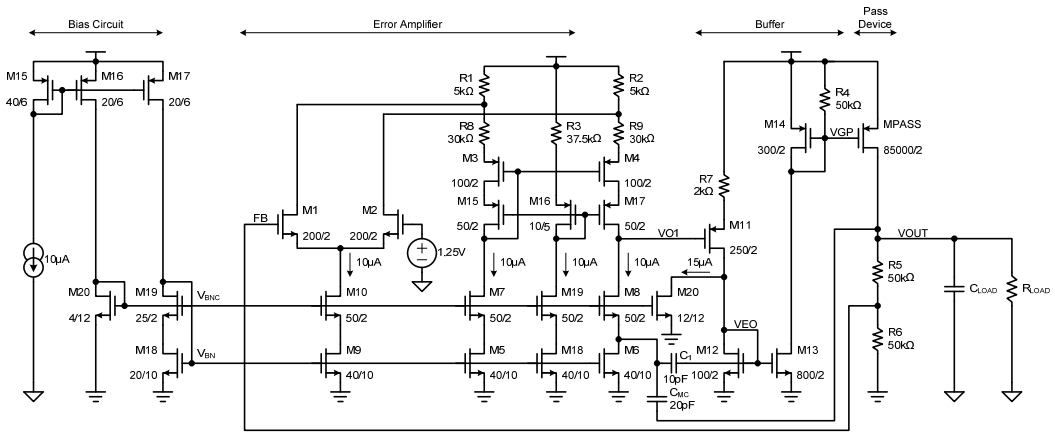

Figure 33: LDO Schematic with Added Compensation as Previously Discussed

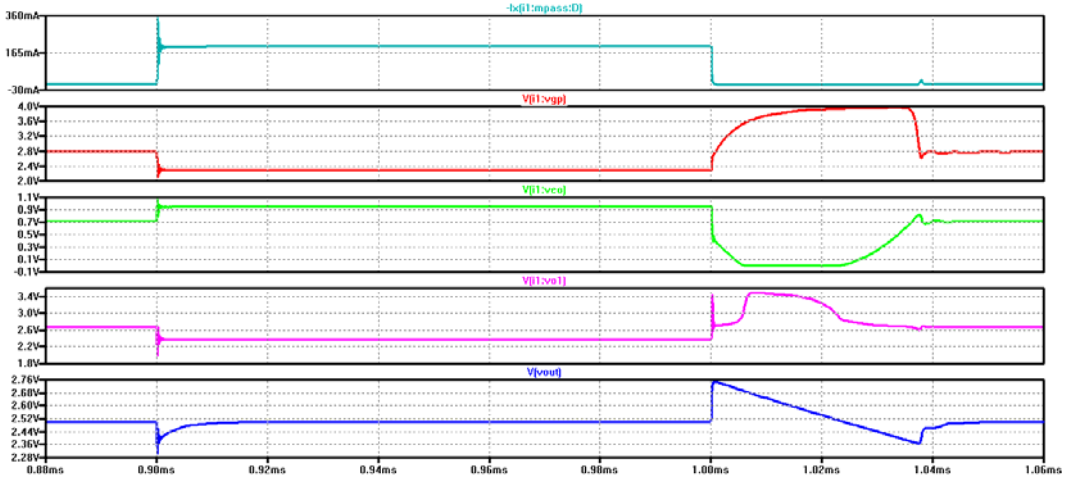

Figure 34: 1mA to 200mA Load Step with 100nF Output Cap with Reduced Error Amplifier Gain

The above transient simulation shows now that the LDO is stable. There is some ringing when the load current steps from low to high so the phase margin is poor.

By looking at the VGP node (gate of pass device), the voltage pulls down fast and undershoots which then the loop has to compensate and the causes the ringing because the loop is still too fast. There is a way to slow the loop down during this event. If the loop gain could dynamically decrease when the gate of the pass device undershoots, then the loop should be able to stabilize without having excessive ringing. There's a way to do this to the buffer stage. First, degenerate the NMOS mirror. This doesn't decrease the gain because the mirror ratio is still in the same. Then if another device is tied to the gate of the pass device to mirror the pass device current, that current can be injected into the source of M13 (the output NMOS of the buffer mirror). This forms a feedback loop such that if the NMOS mirror overshoots in current, then the PMOS mirror will lift up on the source of M13 which will then reduce the current. Also, this loop should be quite fast and can dampen out some ringing when the load current is high. Below is the modified LDO schematic and the transient plot.

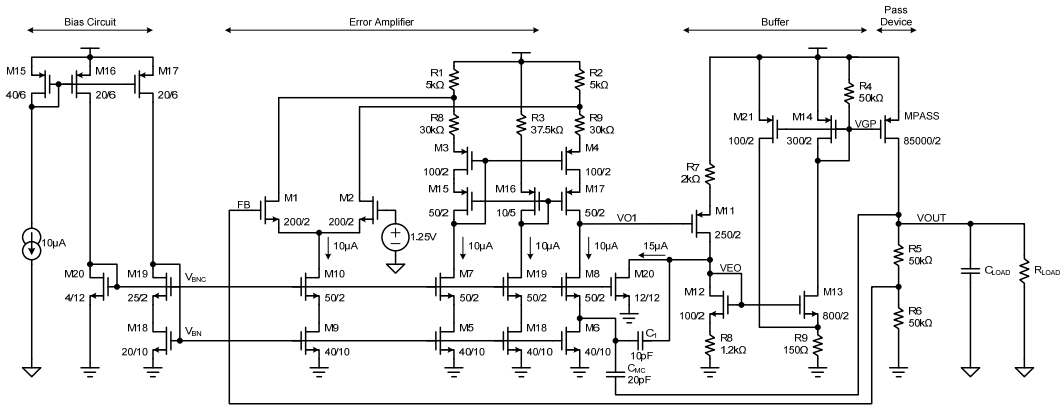

Figure 35: LDO Schematic w/ Dynamically Reduced Gain

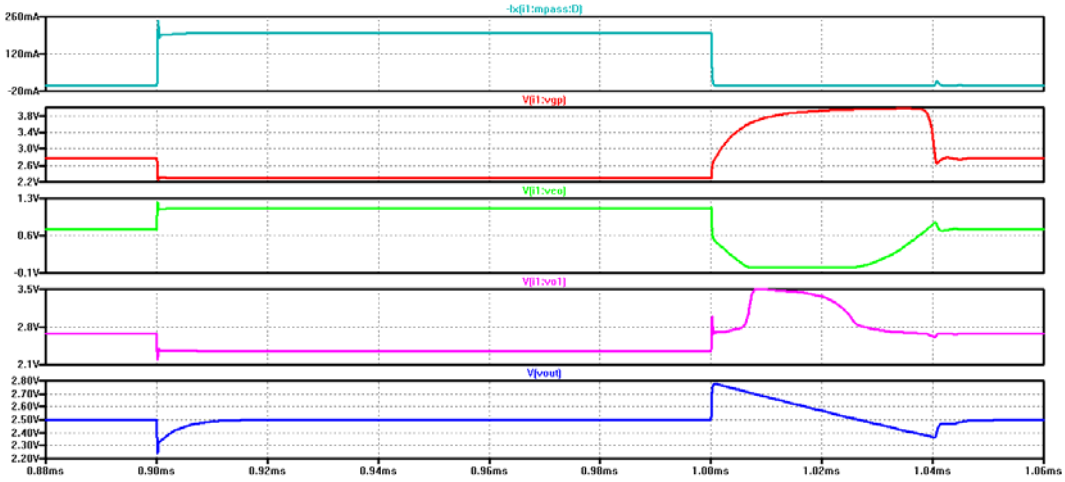

Figure 36: Load Step Sim with LDO in Figure 35

The low to high current load step shows much less ringing as the previous simulation. The dynamically reduced gain buffer works as described. The high to low current load step looks the same as before. The transient performance isn't great, but it's stable, so now it's time to look at the transient performance with no cap on the output. Below is the simulation plot with no output cap.

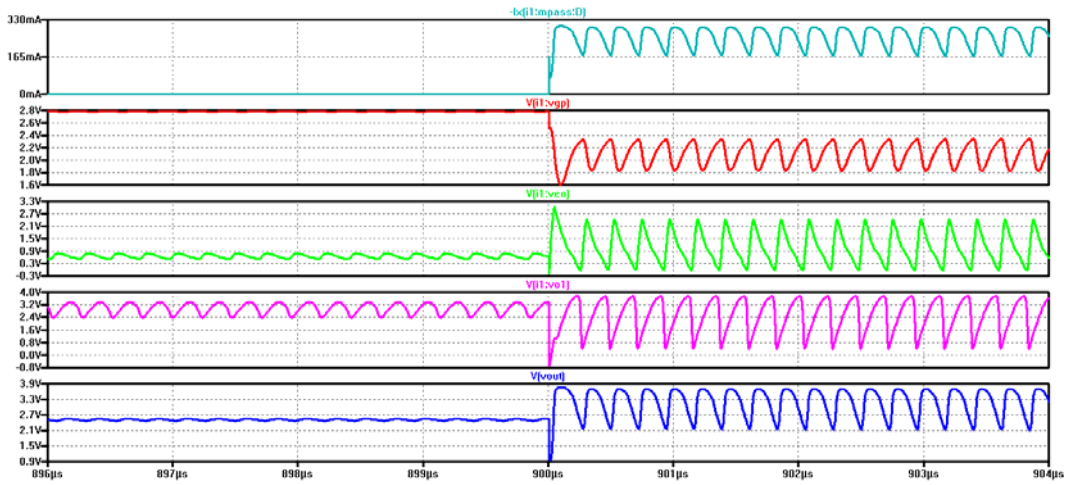

Figure 37: 1mA to 200mA Load Step Sim with LDO in Figure 35 & No Output Cap

As shown in the above simulation plot, the LDO is unstable with no output cap. In a transient sense, it's difficult for LDOs to be stable with no output cap because there's no charge storage device on the output to absorb load steps [3]. So without an output cap, when the load current changes abruptly, it's very plausible that the loop rails out and then can overshoot when it comes back into the gain region. The loop can sometimes stay in this mode where it's railing out on both the low and high end. Looking at the sim plot, this doesn't quite seem to be the case, especially when the load current is 1mA because the oscillations are bounded. However, when the load current steps to 200mA, the output voltage drops down to ~900mV, which means the feedback divider is at ~450mV which is the input to the error amplifier. This completely rails out the error amplifier and causes the

output voltage to then overshoot and reach the input voltage and then sustains the oscillation.

It seems necessary to have some charge storage on the output of the LDO in order for the LDO to be stable with no external output capacitor. It's not unreasonable to have ~100pF of on-chip capacitance, so let's try putting a 100pF cap from the LDO's output to ground. The simulation shows the LDO is stable when the load current is 1mA but then goes unstable when the load current switches to 200mA. The edges on VOUT when the load current steps are quite fast and it seems like using the 100pF internal output cap would be better used as a miller cap to provide some fast negative feedback. The problem with using a 100pF miller cap is if it connects to a high impedance node, then the frequency of that pole will shift too low and could interfere with the dominant pole and can cause the LDO to go unstable. If the 100pF miller cap connects from VOUT to a low impedance node, then the frequency of the pole is still relatively high and the cap works more like current feedback. A relatively low impedance node that is inverting from the output would be the gate of the PMOS pass device. Below is the 1mA to 200mA to 1mA load step simulation with no output cap and an internal 100pF cap connected from VOUT to the gate of the pass device.

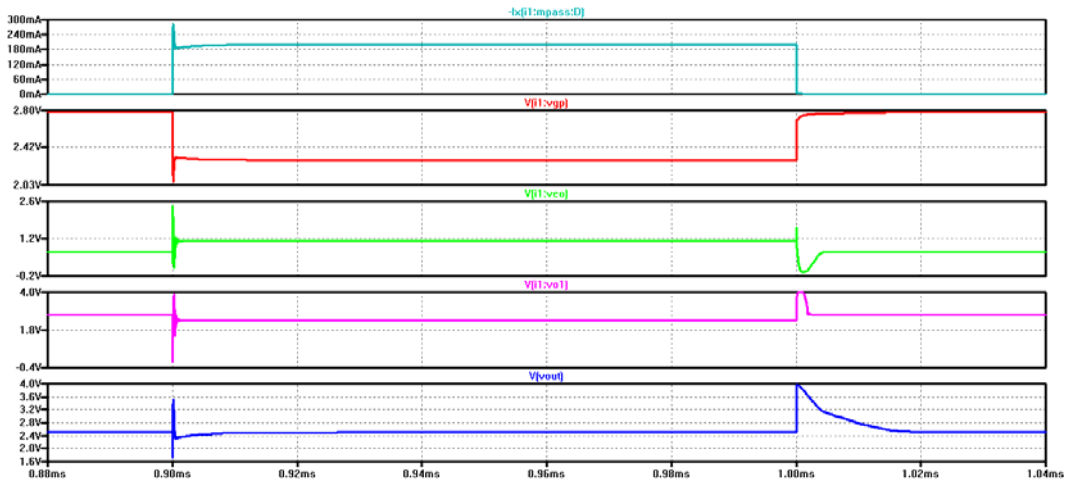

Figure 38: Load Step Sim with No Output Cap and 100pF Miller Cap Around Pass Device

The LDO is now stable with no output cap and with a 1mA to 200mA load step. The 1mA to 200mA transition has some overshoot in there so it'd be nice to clean that up. The 200mA to 1mA transition looks fine except that the output voltage goes all the way up to VIN and the output takes a decent amount of time to come back to regulation. A way to make the 100pF cap look bigger is to insert some resistance in series with the gate of the pass device and connect the cap directly to the gate of the pass device. The resistor somewhat isolates the circuitry before the pass device so then the miller cap is able to slew the gate of the pass device easier. Below is the new schematic and simulation plot.

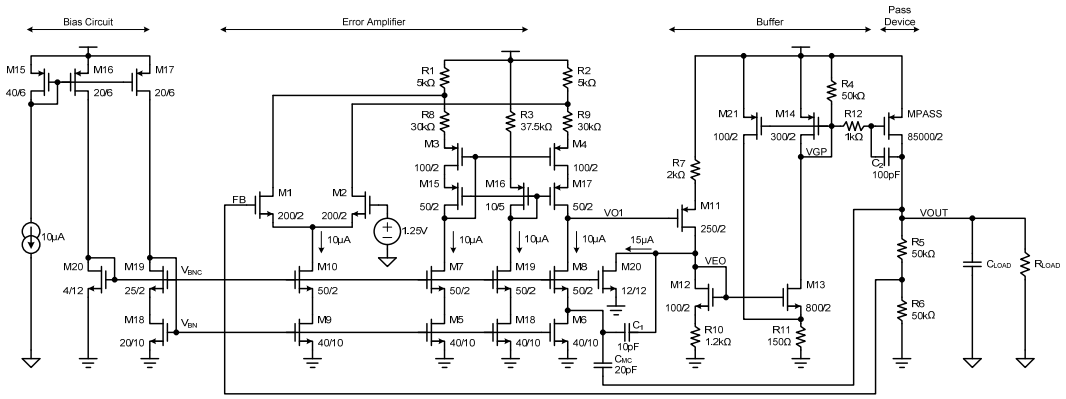

Figure 39: LDO Schematic with 100pF Internal Miller Cap Around Pass Device

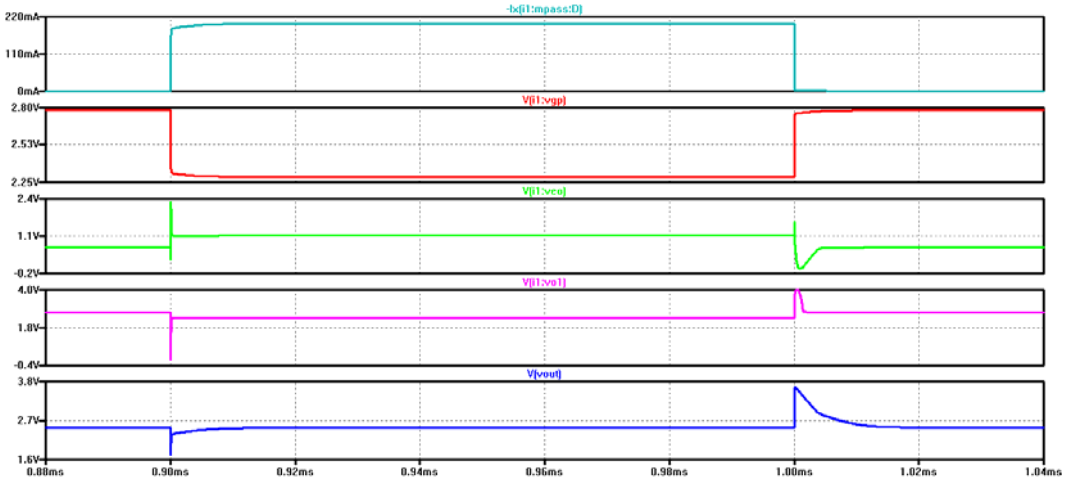

Figure 40: Transient Sim with Figure 39 LDO and No Output Cap

The transient response looks better with the 100pF miller cap and 1kΩ in the gate of the pass device. The 1mA to 200mA load step looks much better because the output voltage drops and then just comes back into regulation rather than overshooting. Also, when the voltage drops, it drops to ~1.74V as opposed to ~900mV which is a vast improvement. In the 200mA to 1mA load step, the output voltage comes up to ~3.63V, so the output isn't railing out as it previously was.

Now it's time to look at the same simulation while stepping the output cap from 0 to 1µF (0, 100pF, 1nF, 10nF, 100nF, and 1µF). Below is the simulation plot.

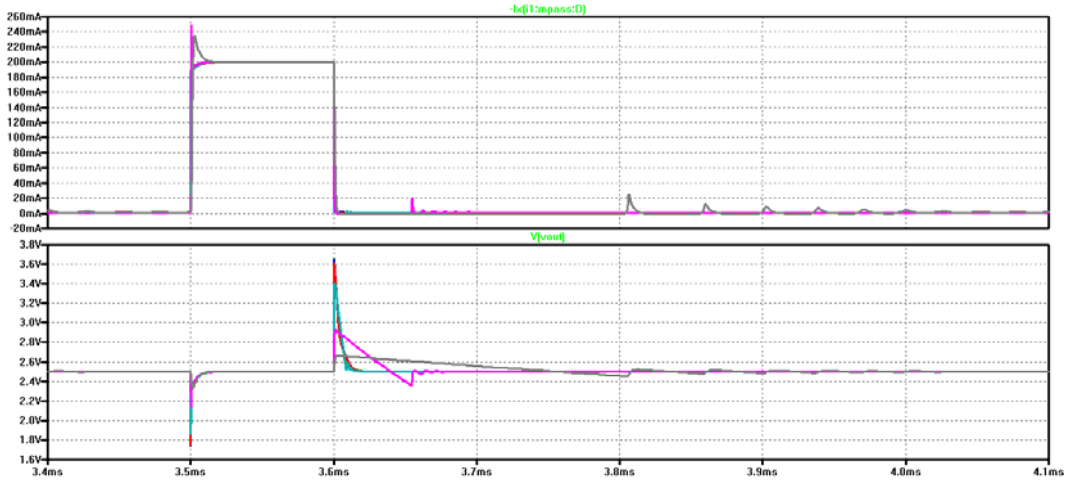

Figure 41: Transient Sim with Figure 39 LDO and Stepping the Output Cap

The LDO is stable with 0 – 1µF, but the stability at 1mA load current is a bit marginal with the higher output caps. It's not really desirable to lower the gain further since it's already been reduced in a few spots to improve stability. However, a high frequency pole could be added to dampen out some ringing. Currently, there are 2 miller caps connected to VOUT and another miller cap connected across 1 inverting gain stage. Two of the miller caps are connected to the error amplifier's output (well at the cascode point but still in phase with the output). The other side of the output stage of the error amplifier is much lower impedance since the PMOS mirror is diode connected and

may be a good place to connect a small miller cap. The gate of the pass device could be the other connection of the miller cap because the phase is inverting. Since the voltage at the gate of the pass device is referenced to VIN, the other side of the miller cap should connect to a voltage that's referenced to VIN as well so that the cap doesn't disturb the output voltage with movements in the input supply. When connecting the cap to the diode connected side of the error amplifier, try connecting it to the cascode point of the PMOS current mirror (common source and drain connection of M15 and M3). This approach somewhat matches the cascode compensation of the main miller cap, Cmc. Below is the new schematic and a simulation plot with the output cap at 1µF and this new miller cap stepped from 0 to 1pF.

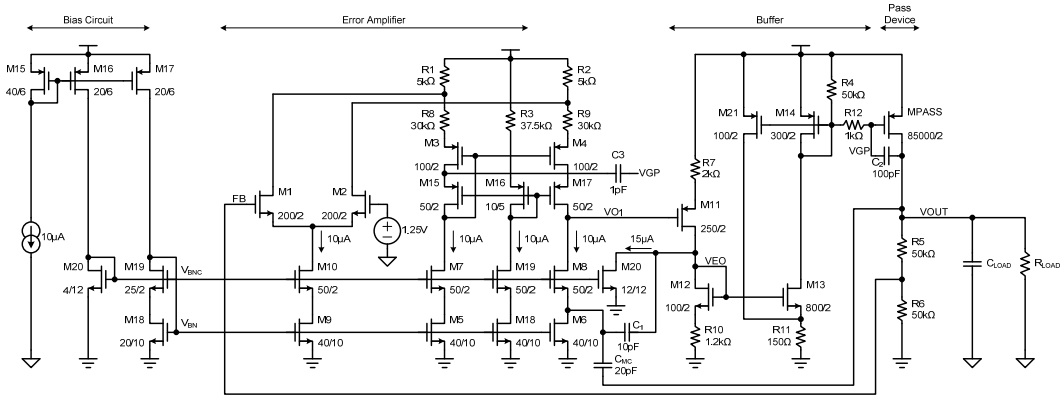

Figure 42: New LDO Schematic with C3 Added

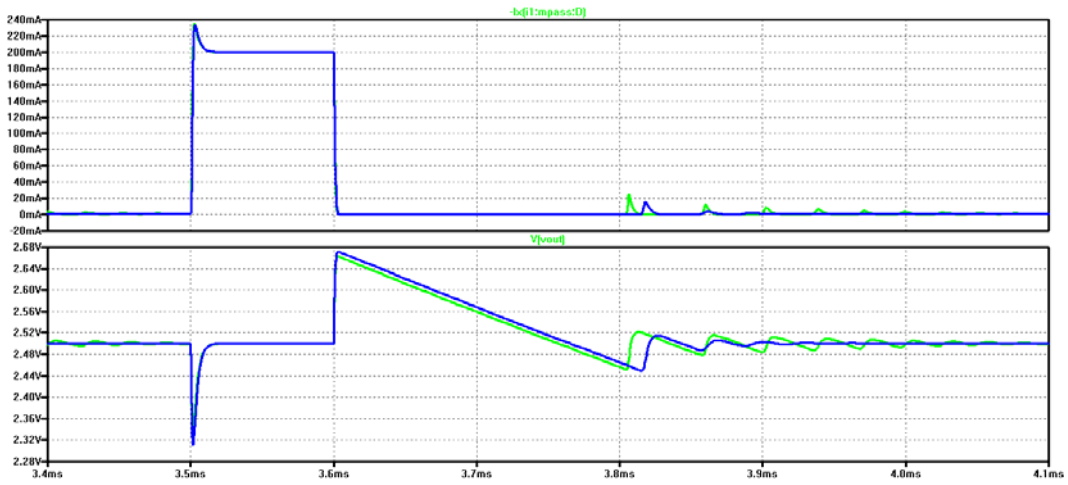

Figure 43: Transient Sim with Figure 42 LDO with 1µF Output Cap and Stepping C3 from 0 to 1pF

The waveform with lower oscillation is when C3 is 1pF, so it helps the stability. If the cap is stepped above 5pF, the loop goes unstable at light load, so the cap shouldn't go higher than 1pF to leave enough margin. The response looks better with 100nF output cap as well. For small output caps, the response is almost unchanged.

It'd be good to check the AC response now to look at the DC gain and phase and gain margin. Below is the AC simulation plot with a 1mA load current and the output cap being stepped from 0 to 1µF.

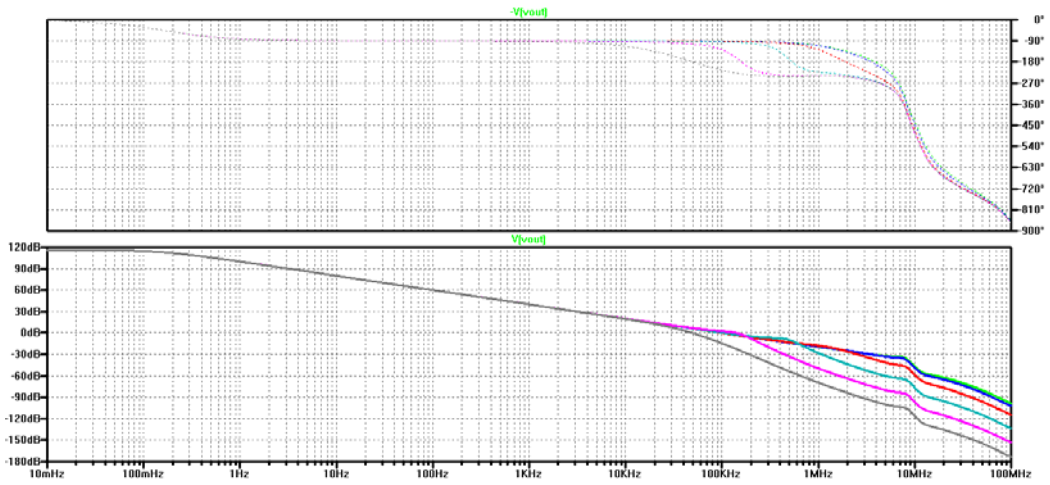

Figure 44: AC Sim with Figure 42 LDO with 1mA Load Current & Output Cap stepped from 0 to 1µF

The DC gain dropped down to ~116dB which is still relatively high. The phase margin with caps from 0 to 10nF is about 85°. The phase margin drops to 18° and 1° with an output cap of 100nF and 1µF respectively. If the AC source is moved such that the resistor divider is in the loop, the gain drops by 6db because the feedback voltage is half the output voltage. The phase margin also goes to 73° and 21° with 100nF and 1µF output caps respectively. These phase margins are more indicative of the transient response when the load current steps down to 1mA. The phase margin is unchanged for output caps smaller than 100nF. When the output cap is 1µF, the phase margin increases to ~78° when the load current is 200mA. The LDO is stable with output caps from 0 to 1µF and with load currents of 1mA to 200mA.

I. Slew Rate Enhancement

The LDO is stable for a wide output cap range, but the transient response is much slower than desired when the load current switches from 200mA to 1mA with no output cap. Below is the response and shows a settling time of ~14µs during the high to low load step.

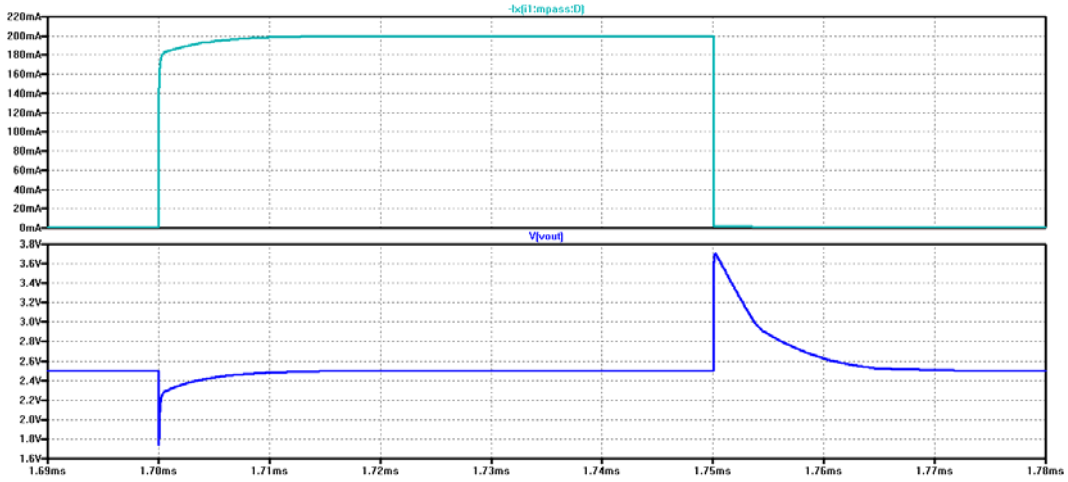

Figure 45: 1mA to 200mA Load Step Sim with No Output Cap

When the load current steps from 200mA to 1mA, the pass device current should drop to zero current because the output overshoots. However, the pass device current drops to ~1.5mA and then decays down to 1mA. A circuit is needed to detect the output voltage overshooting and then pulls up on the gate of the pass device.

A possible way to do this is to take a cap that's connected between VOUT and the gate of an NMOS. Since the gate of the NMOS is really high impedance, the cap will couple the AC response on VOUT directly to the gate of the NMOS. When the output overshoots, the

NMOS will turn on and can be used to pull down on the gate of a PMOS device which can then pull up on the gate of the pass device. To make the circuit fast, the nodes should be pre-biased such that the devices are just barely off. The less the nodes have to slew during the output overshooting, the faster it will respond. Below is the schematic of the proposed slew rate enhancement circuit.

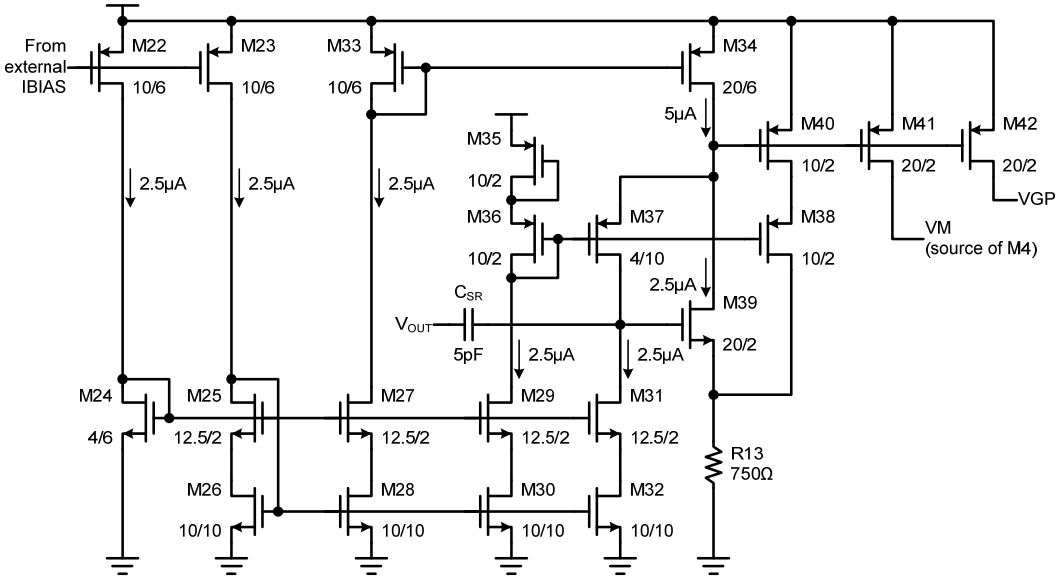

Figure 46: Slew Rate Enhancement Circuit

As previously described, this circuit pre-biases the node voltages. The gate of NMOS M39 is biased to run at a current of 2.5μA and the gate of the PMOS devices, M40-M42, is biased such that they're off but the VGS voltage is just less from conduction. The feedback loop formed by M39 and M37 achieves pre-biasing both of these voltages and at the same time, keeping the gate of M39 at high impedance. Keeping the impedance at the gate of M39 is crucial to the

operation of this circuit because whatever movement happens on VOUT, gets reflected directly to the gate of M39. In this manner, the cap, Csr, acts as a voltage source. If the impedance was low, then the cap acts as an AC current source, which is not what this circuit requires. The loop M40 that injects current into R13 slightly reduces the gain of the circuit when the output voltage overshoots. With the value of the slew rate cap and the 2.5µA current, this circuit only responds to very fast rising edge rates on VOUT. When the output cap is larger in value, this circuit is invisible. Also, since the circuit only responds to transients, this circuit doesn't affect the AC performance of the LDO. Below is the load step simulation with and without the slew rate enhancement circuit with no output cap.

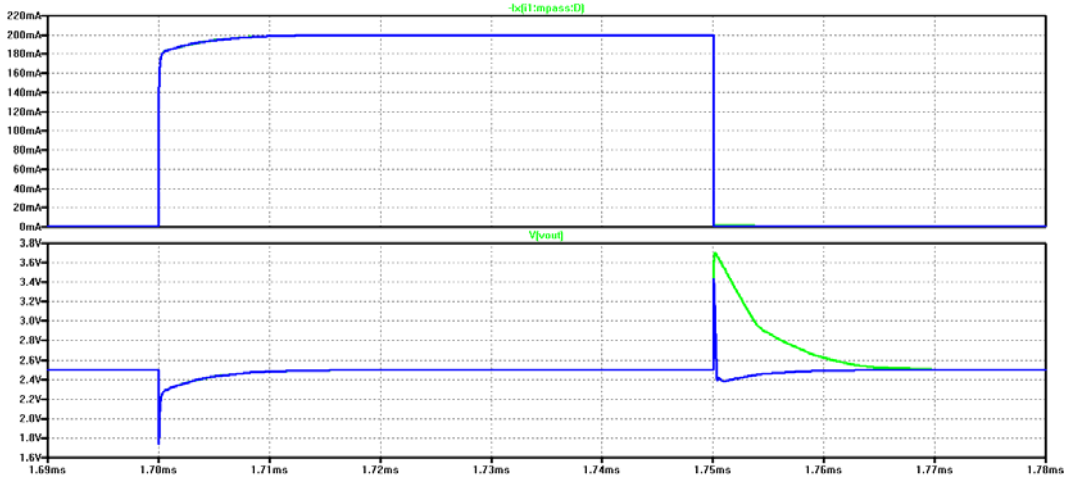

Figure 47: Load Step Simulation with & without Slew Rate Enhancement Circuit with No Output Cap

The transient response with the slew rate enhancement circuit shows a vast improvement in the settling time and overshoot when the load current steps from 200mA to 1mA. The 1mA to 200mA response is unchanged even though there's a rising edge which proves that the added circuit only responds to really fast rising edges on VOUT. The AC response remains unchanged. Now that the LDO is stable and the transient performance is improved for small cap loads, it's time to look at power supply rejection (PSR), line and load regulation, and dropout voltage.

J. Power Supply Rejection

Power supply rejection is looked at by inserting an AC signal into the input voltage and looking at the response of the output voltage. Then a transient simulation is run to have a step in the input voltage and then look at the response at the output. Ideally, the LDO will remain perfectly regulated when any movement in the input voltage. Below is the AC power supply rejection simulation followed by the transient simulation with ±100mV steps on VIN with 100ns edge rates.

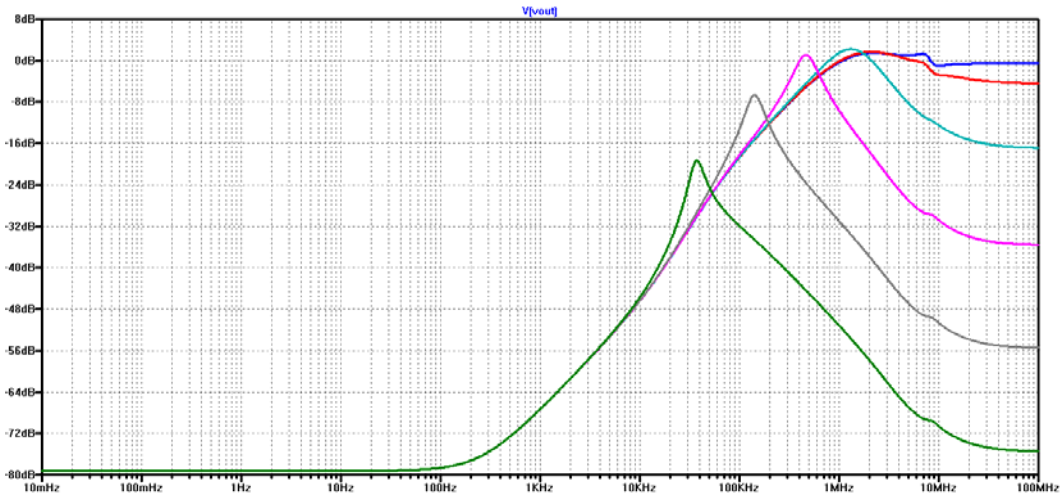

Figure 48: Power Supply Rejection AC Simulation w/ 1mA Load and Output Cap Stepped from 0 to 1µF

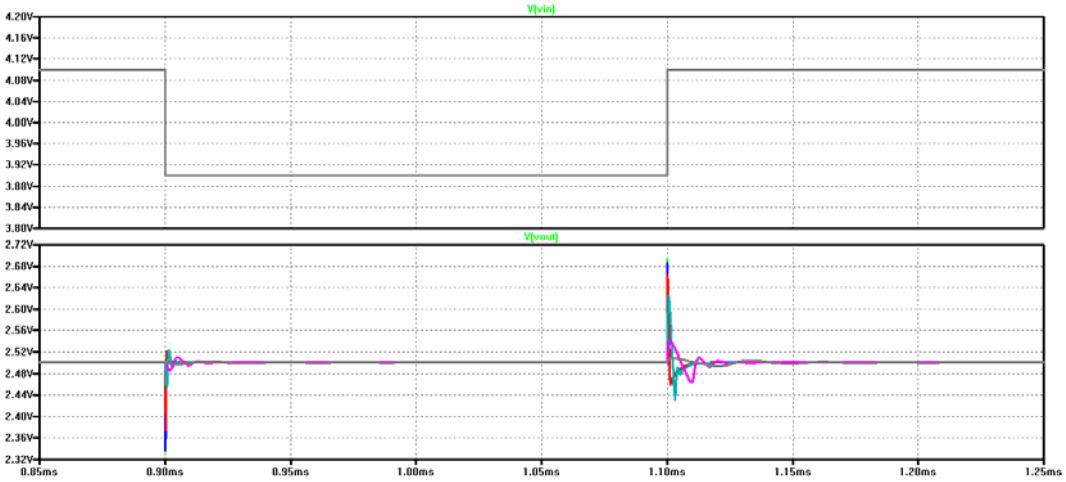

Figure 49: Power Supply Rejection Transient Simulation w/ 1mA Load and Output Cap Stepped from 0 to 1µF

The DC power supply rejection is ~-79dB which implies that the line regulation of the LDO should be pretty good. As the frequency increases, the smaller the output cap, the higher the gain. The transient simulation looks ok. The overshoot and undershoot is higher with smaller output caps, which is to be expected. The output does

show some ringing and takes some time to settle, but the output does settle and is stable. When the load current increases to 200mA, the ringing in the output is essentially gone and the overshoot and undershoot is a bit better.

K. Dropout Voltage, Line & Load Regulation, & Temperature Regulation

The dropout voltage of the LDO is defined as the difference between the input and output voltage when the input is at the regulated output voltage (2.5V) and the load current is at its maximum (200mA). When the input voltage is 2.5V, the output voltage is 2.27336V, which gives a dropout voltage of 226.64mV. The pass device current at dropout is 200.023mA which gives an Rdson of 1.133Ω. This is a bit worse than the design target of 1Ω. The gate voltage of the pass device is 452mV which isn't as low as expected.

The pass device current is a mirrored current of M14. The mirror is a perfect ratio when the VDS of the pass device is the same as the VGS of the diode connected PMOS in the mirror. Well at dropout, the pass device is in triode, whereas the diode connected PMOS, M14, is in saturation which will make the pass device current less than the size ratio dictates. There's a couple ways to fix this; (1) use a cascode device to bias up the drain of M14 to be the same as

VOUT, or (2) insert a resistance in the drain of M14 such that the voltage at the drain at M14 is roughly VOUT. The first method is the best way but takes more devices than the second method. The second method is cheap and dirty and will work good enough. After all, the goal is to make the VDS's roughly the same so that the gate voltage of the pass device pulls down to a lower voltage which should decrease the Rdson of the pass device. Inserting 2kΩ in the drain of M14 lowers the gate voltage to 230mV and gives a dropout voltage and Rdson of 169.55mV and 0.848Ω respectively.

This is a better dropout and Rdson than the design target, but this will leave room for bondwire resistance and pass device metal routing resistance. The dropout voltage implies that the minimum input voltage is 2.66955V for Vout to be 2.5V at a load current of 200mA. After adding resistance in the drain of M14, this could affect the load step performance of the LDO, which is shown below. The case with no output cap shows a slight difference when the load current steps from 1mA to 200mA, but it's still stable and doesn't show any ringing. When the output cap is 1μF, the load step performance is unchanged.

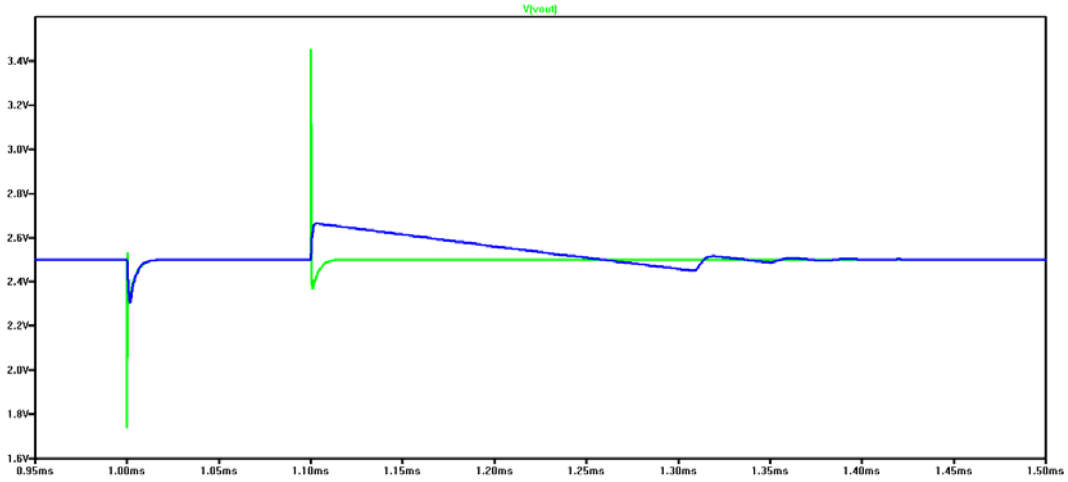

Figure 50: 1mA to 200mA Load Step Sim w/ Output Cap of 0 & 1µF

Line regulation is measured by sweeping the input voltage from 2.75V to 5V with stepping the load current from 1mA to 200mA. Below is the DC simulation with 1mA and 200mA load current.

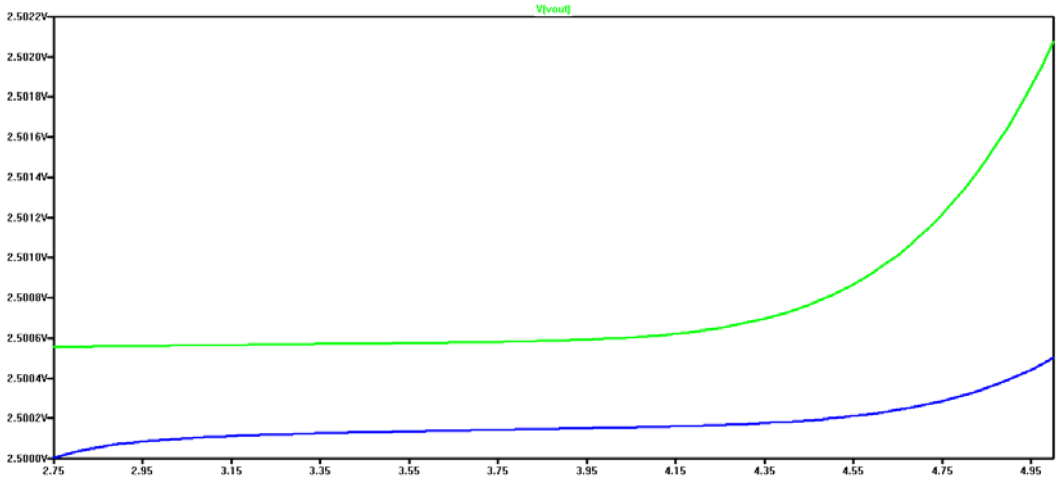

Figure 51: Line Regulation of Sweeping VIN from 2.75V – 5V with 1mA and 200mA Load Current

When the load current is 1mA, the output voltage changes by 1.52mV for a 2.25V change in VIN which gives a line regulation of 0.676mV/V or 0.027%/V. When the load current is 200mA, the output voltage

changes by 0.5mV which gives a line regulation of 0.222mV/V or 0.009%/V.

Load regulation is done by sweeping the load current from 1mA – 200mA while stepping VIN at 2.75V, 3.6V, and 5V. Below is the DC simulation.

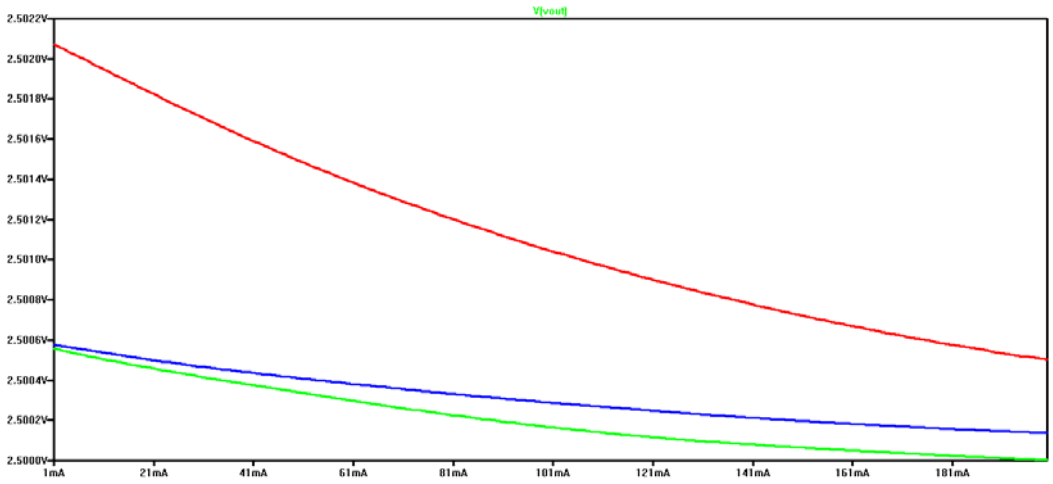

Figure 52: Load Regulation of Sweeping Load Current from 1mA – 200mA and Stepping VIN at 2.75V, 3.6V, & 5V

From the top plot to the bottom plot, VIN is 5V, 3.6V, and 2.75V respectively. The load regulation is -2.8mV/A (0.11%/A), -2.2mV/A (0.09%/A), and -7.9mV/A (0.32%/A) for VIN of 2.75V, 3.6V, and 5V respectively.

The LDO's regulation voltage should also be looked at over temperature. Below is the plot that shows the output voltage with sweeping the temperature from -50°C to 150°C with 1mA and 200mA of load current.

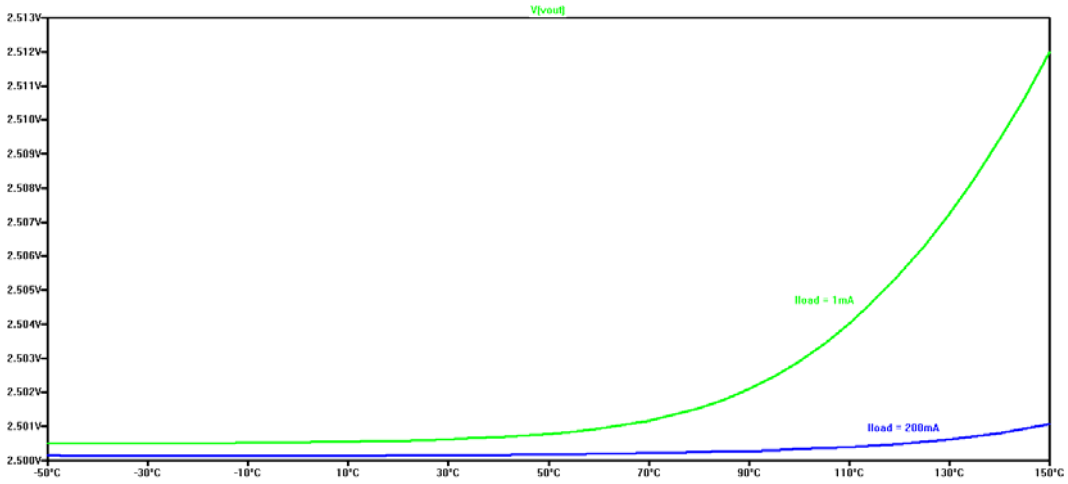

Figure 53: Temperature Regulation from -50°C to 150°C with 1mA and 200mA of Load Current

The temperature regulation is 57.5µV/°C and 4.67µV/°C at 1mA and 200mA respectively.

CHAPTER IV

LAYOUT

The any-cap LDO was fabricated on a proprietary 1.5µm BiCMOS process with 2 layers of metal (minimum gate length is 2µm). The die size is 40mil x 62mil (2480mil^2) or 1.016mm x 1.575mm (1.6mm^2). Care was taken to handle ESD events on any given pin using ESD cells and secondary ESD protection.

CHAPTER V

EXPERIMENTAL MEASUREMENTS

Below is the schematic used for bench evaluation.

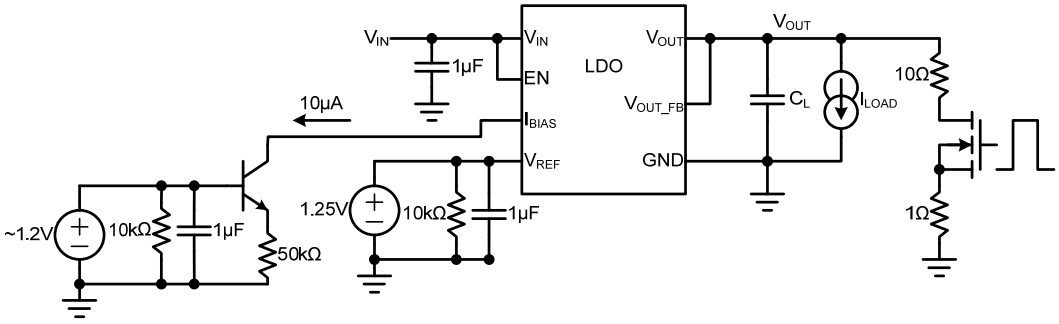

Figure 54: Lab Bench Evaluation Schematic

The external NMOS with 10Ω in the drain and 1Ω in the source is used for the load step evaluation. The 1Ω source degeneration resistor is an accurate current sense resistor so that a voltage probe can be placed across it to look at the load step current with a scale of 1A/V. The gate voltage of the NMOS can be varied to give a desired load step current less than 227mA.

At first power up, the LDO output regulates to ~2.5V with a 1.25V reference voltage. The minimum load current for stability is <1mA, but 1mA will be used for the minimum load. The input current with a 1mA load is 1.2mA meaning that the chip is consuming 200µA.

A. Dropout Voltage

Dropout voltage is looked at by driving the input voltage to 2.5V and measuring the output voltage with a 200mA load. Under these conditions, the output voltage measures 2.258V which gives a dropout of 242mV and a pass device Ron of ~1.21Ω. The last simulated pass device Ron was 0.848Ω which is significantly lower than the measured Ron. With previous experience of the package this LDO went in to, the source and drain (Vin and Vout respectively) bondwires are ~75mΩ each which would take the simulated Ron to ~1Ω which still leaves ~0.21Ω unaccounted for. If I re-run the dropout simulation with 75mΩ in series with the input voltage and 75mΩ in series with the output voltage, the dropout voltage is 202mV which gives an Ron of the pass device of ~1.01Ω. Metal resistance shouldn't be on the order of hundreds of mΩ, so that can't make up the rest of the Ron. In order to figure out why the dropout isn't coming closer to the simulated dropout, micro-probing would be needed to measure internal node voltages, which wasn't available to me at the time.

B. Load Regulation

Load regulation is measured by sweeping the load current from minimum to maximum load and the input voltage can be stepped as well. In this case, the load current was swept from 1mA to 200mA

while stepping the input voltage at 2.8V, 3.6V, and 5V. Below is the load regulation plot.

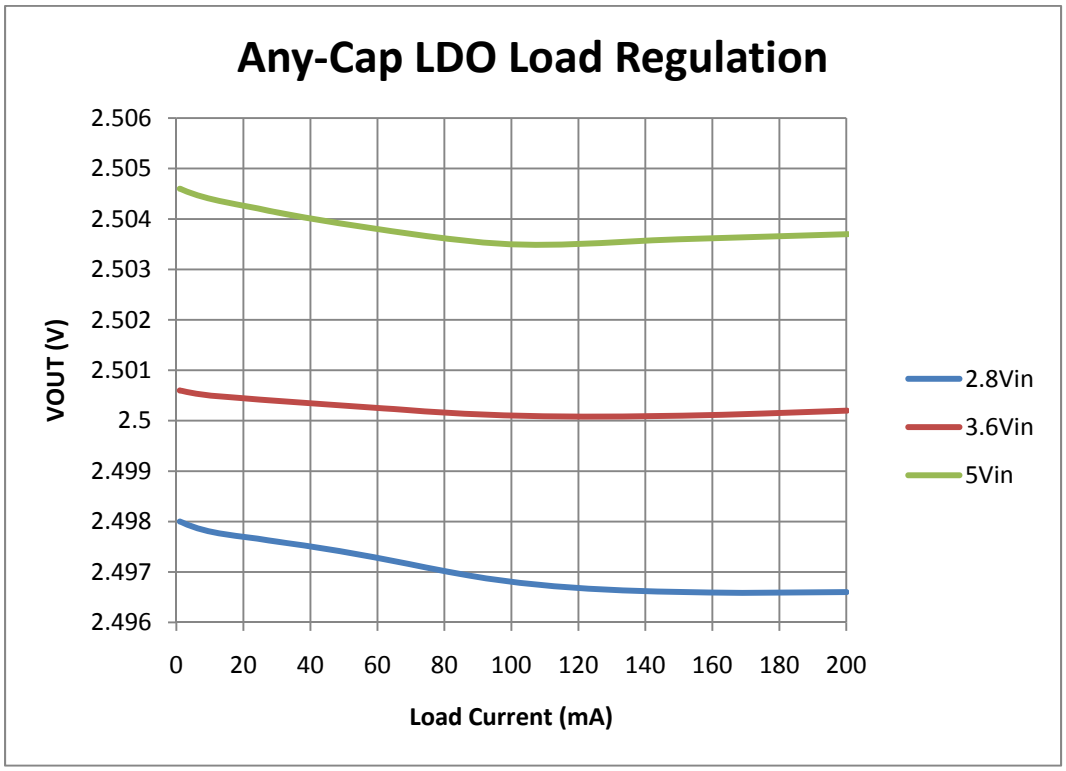

Figure 55: Measured Load Regulation

The load regulations measured at -7.03mV/A, -2.01mV/A, and -4.51mV/A at 2.8V, 3.6V, and 5V respectively. These numbers aren't exactly what the simulator predicted, but they're close enough.

C. Line Regulation

Line regulation is measured by seeing the change in output voltage with changes in the input voltage. With this LDO, the input

voltage was swept from 2.8V to 5V with stepping the load at 1mA and 200mA. Below is the line regulation plot.

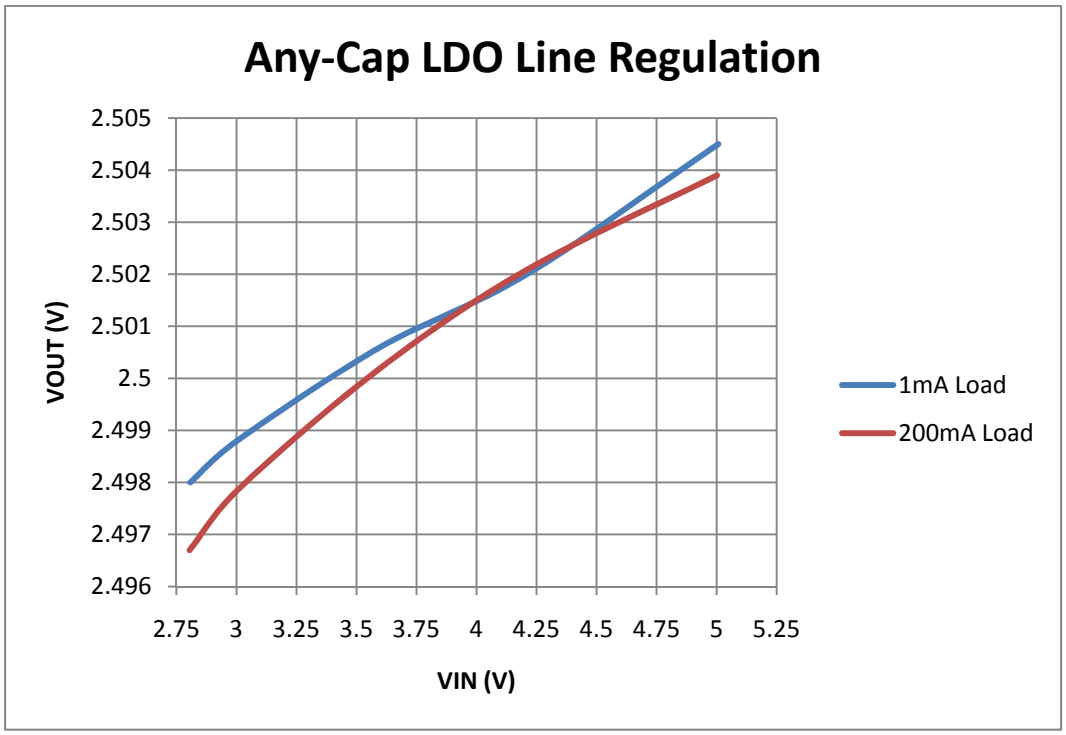

Figure 56: Measured Line Regulation

The line regulations measured at 2.95mV/V and 3.28mV/V at 1mA and 200mA respectively. These numbers are worse than the simulations, but it's not horrible.

D. Load Step Response

Now that the DC characteristics are measured, it's time to look at load steps to investigate the stability of the any-cap LDO. The LDO is setup to measure the response for a 1mA to 200mA load step with no

output cap and 1µF output cap. Below is the load step response of both cases.

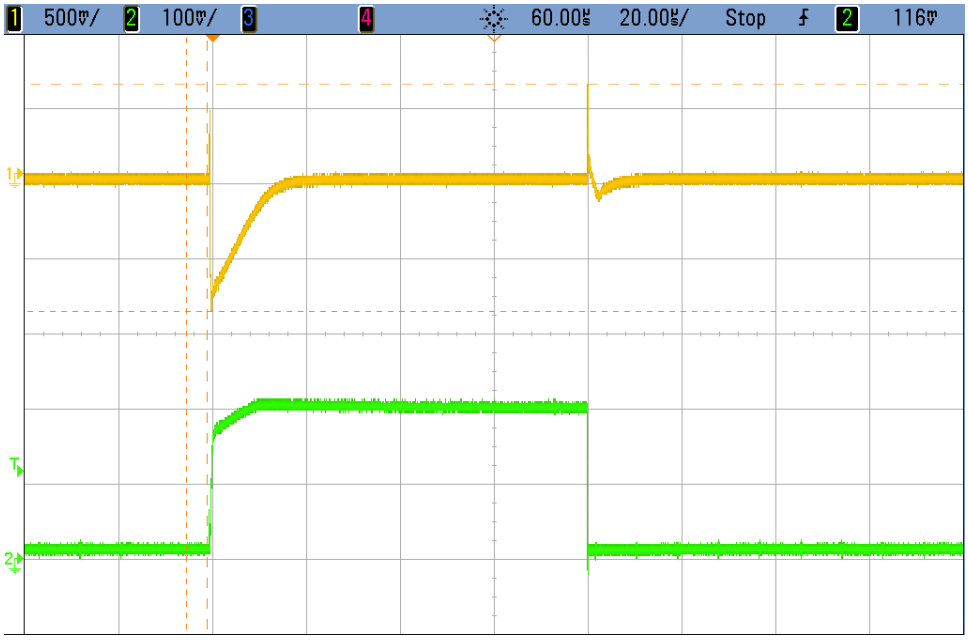

Figure 57: Measured 1mA to 200mA Load Step w/ No Output Cap

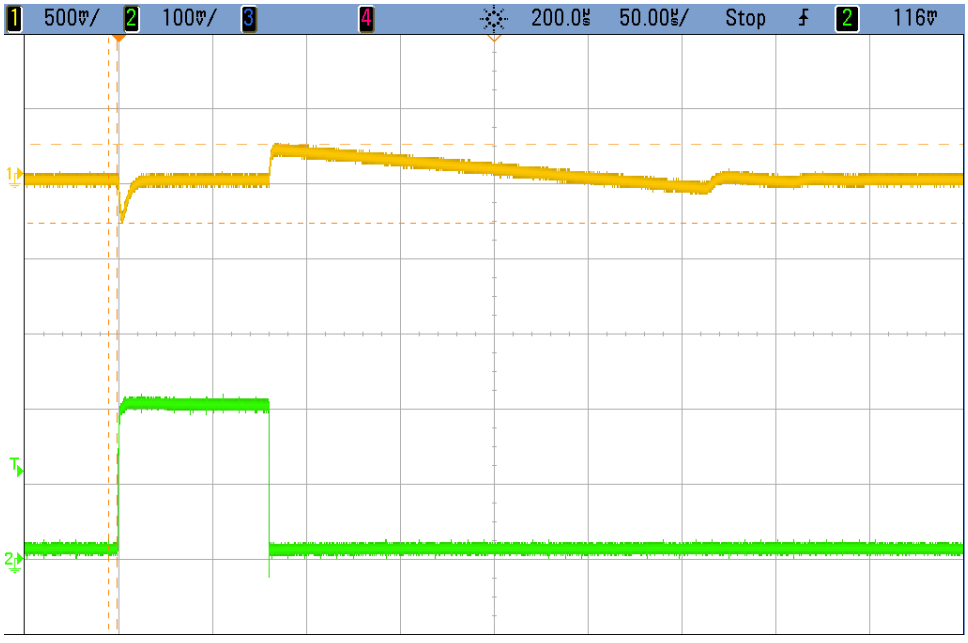

Figure 58: Measured 1mA to 200mA Load Step w/ 1µF Output Cap

For both plots, the top waveform is the output voltage AC coupled at 500mV/div, and the bottom waveform is the stepped load current at 100mA/div. As shown, the LDO is stable with no output cap and 1µF output cap as designed. The output voltage undershoot and overshoot with no output cap is 920mV and 600mV respectively. The simulated is 750mV and 950mV. With no output cap, the settling time is roughly 12.5µs and 4µs for the low-hi current and hi-low current load steps respectively which is worse than simulations but not by much. Fortunately, the LDO is still stable with no output cap. With a 1µF output cap, the output undershoot and overshoot is 330mV and 200mV respectively which matches simulations pretty closely (300mV and 180mV respectively). The load step response with 1µF output cap looks very similar to simulations. Intermediate output caps and intermediate load steps were checked for stability, and it is stable, but not shown in this paper.

CHAPTER VI

COMPARISON TO PREVIOUS WORK

There have been numerous works in the area of capacitor-less LDOs, but there hasn't been much work in the area of LDOs that are stable with a very wide range of output caps. Some of the previous work is tailored towards capacitor-less operation that is also stable with higher output caps, but some sacrifices are made such as minimum load current.

Work [1] focuses on designing a LDO that is stable with a wider output cap range than this presented work, however there are some pitfalls. Output voltage overshoots and undershoots with no output cap are more than twice of this presented work along with the settling times being much longer. Also, the loop gain is only about 40dB making line and load regulation much worse. The dropout voltage is also higher, making the minimum input voltage higher as well. The main advantage of [1] LDO is that it's stable with no output current, whereas the presented LDO requires a minimum 1mA load for stability.

The LDO designed in [2] works as an any-cap LDO without the need of an internal 100pF internal capacitor for capacitor-free operation. The loop gain is quite high which compares well to the

proposed LDO. The load step response of [2] appears to be better, although the scope shots given are with the PMOS pass device operating in its linear region which can make the results which can make the load step response look better. When using output caps with [2], ESR is needed in the output cap on the order of ~1Ω which adds cost and board area. Capacitor-free operation requires a minimum load of 10mA which is 10% of its full range output current. The presented LDO is more robust when comparing the caveats of output caps.

CHAPTER VII

CONCLUSION

A novel LDO design has been presented that allows a wide range of output capacitors to be used. This allows the LDO to be used as a system-on-chip LDO with no output cap or as a stand-alone LDO where an output cap is normally used. A thorough discussion was given in Section III as to how this any-cap LDO was designed.

First, a conventional LDO was designed where an output capacitor is used and the LDO was internally compensated using miller compensation. Then a fast path (100pF miller capacitor on pass device) was added to make the LDO stable with no output caps. Then to improve the hi-lo load transient response with no output cap, a slew-rate enhancement circuit was added to quickly turn off the pass device and allow the output voltage to settle faster.

The LDO was primarily compensated by looking at load transient response because it gave more insights of how to make the loop behave. Designing the LDO to be stable from 0 – 1μF output caps is difficult enough, but adding high current capability and high gain make the task much more difficult. Making the LDO capable of higher current makes the pass device bigger and hence higher gate capacitance. High

gain and stability are typically conflicting design performance parameters, but the presented LDO achieved both.

The any-cap LDO was fabricated on a proprietary 1.5μm BiCMOS process with 2 layers of metal (minimum gate length is 2μm). The die size is 40mil x 62mil (2480mil^2) or 1.016mm x 1.575mm (1.6mm^2). Experimental results show that the LDO is stable over 0 – 1μF range of output caps from 1mA – 200mA with excellent load regulation.

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