Electron Transport Properties in One-Dimensional III-V Nanowire Transistors

by

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ABSTRACT

Semiconductor nanowires are featured by their unique one-dimensional structure which makes them promising for small scale electronic and photonic device applications. Among them, III-V material nanowires are particularly outstanding due to their good electronic properties. In bulk, these materials reveal electron mobility much higher than conventional silicon based devices, for example at room temperature, InAs field effect transistor (FET) has electron mobility of 40,000 cm2/Vs more than 10 times of Si FET. This makes such materials promising for high speed nanowire FETs. With small bandgap, such as 0.354 eV for InAs and 1.52 eV for GaAs, it does not need high voltage to turn on such devices which leads to low power consumption devices. Another feature of direct bandgap allows their applications of optoelectronic devices such as avalanche photodiodes. However, there are challenges to face up. Due to their large surface to volume ratio, nanowire devices typically are strongly affected by the surface states. Although nanowires can be grown into single crystal structure, people observe crystal defects along the wires which can significantly affect the performance of devices.

In this work, FETs made of two types of III-V nanowire, GaAs and InAs, are demonstrated. These nanowires are grown by catalyst-free MOCVD growth method. Vertically nanowires are transferred onto patterned substrates for coordinate calibration. Then electrodes are defined by e-beam lithography followed by deposition of contact metals. Prior to metal deposition, however, the substrates are dipped in ammonium hydroxide solution to remove native oxide layer formed on nanowire surface.

Current vs. source-drain voltage with different gate bias are measured at room temperature. GaAs nanowire FETs show photo response while InAs nanowire FETs do not show that. Surface passivation is performed on GaAs FETs by using ammonium surfide solution. The best results on current increase is observed with around 20-30

minutes chemical treatment time. Gate response measurements are performed at room temperature, from which field effect mobility as high as 1490 cm2/Vs is extracted for InAs FETs. One major contributor for this is stacking faults defect existing along nanowires. For InAs FETs, thermal excitations observed from temperature dependent results which leads us to investigate potential barriers.

DEDICATION

To my father and mother.

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My grateful acknowledgements to my academic advisor, Dr. Hongbin Yu, who provides me such great opportunity of working on this exciting project, also for his inspiring advice, instructions and guidance. It's a great privilege to work in his group.

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Chapter 1

INTRODUCTION

1.1 Motivations

Semiconductor nanowires (NWs) are considered to be potential building blocks for small scale electronic and photonic devices applications due to their unique one-dimensional structure. Nanowires typically have diameter of below or around 100 nm, while the lengh can be as long as several micrometers. Among the materials that are able to grown into nanowires, III/V materials are considered as promising candidates of building into high speed field-effect transistors (FETs). People have demonstrated that III/V materials such as GaAs, InAs etc. show very high field-effect mobility in bulk devices. At room temperature, InAs bulk material can achieve electron mobility of 40,000 cm^2/Vs, while GaAs bulk material is reported to have electron field-effect mobility as good as 8,500 cm^2/Vs. However, to achieve such high field-effect mobility, people have to synthesis high quality material with nearly perfect single crystal structure within the bulk. This requires strict conditions of synthesis, which includes high temperature with precise feedback control to stabilize the temperature fluctuations, proper pressure, sources with high quality, etc. In other words, it's very hard to grown perfect single crystal bulk material. It's relatively easy to get high quality single crystal thin film of one material, but when it's come to thin films of different materials, for example hetero-structure, then the lattice mismatch of different materials becomes the major contributor for degrading the crystal quality. In the case of nanowires, people find out that the lattice mismatch tolerance for nanowire structure are much larger then for thin films (e.g. ~ 11% for the InAs nanowire on Si substrate system)[1]. Hence, it's easier for nanowire structures to achieve high single crystal quality. People have made successes in this nanowire growth field to synthesis hetero-structure nanowires[2], core-

shell structure nanowires[3], super-lattice structure nanowires[4], III-V nanowires grown on silicon substrate[5] etc., with high single crystal quality.

Comparing to bulk or thin film structures, nanowires can be grown into higher quality single crystal structure, however, they are still experiencing some crystal defects, like stacking faults[6], which can significantly affect such nanowires' electrical or optical properties. Possible reasons to explain the origins of these defects are fluctuations of temperature and pressure during growth process, purity of sources, different catalysts used for growth. A group from Princeton University have demonstrated that they intentionally change temperature during growth process to create nanowires which have different densities of defects along the wire corresponding to different growth temperature[7]. Then they fabricate transistors out of such nanowires which show different transport properties in areas with different densities of defects.

1.2 Nanowire Growth Method

The growth methods of nanowires can be generally divided into two categories, catalyst assisted growth and catalyst free (or self-catalyst) growth[1].

One commonly used catalyst assisted growth method is vapor-liquid-solid (VLS) growth method. It was originally proposed by Wagner and Ellis[8], who used $SiCl_4$ gas diluted in H_2 and flown onto a heated Si surface decorated with Au, in order to grow Si nanowires. Following works have reported that metals such as gold, indium, aluminum, nickel have been used as catalysts. Here we use gold particle as example to illustrate the mechanism of catalyst assisted VLS growth method in the following figure 1. With this method, diameters of nanowires are determined by the size of catalyst seeds, while lengths of nanowires are depending on the growth duration. Among candidates of catalysts, people have found out that comparing with gold seeds, catalysts such as indium,

aluminum and nickel are not satistactoy in terms of growth control and tailoring of nanowire properties. However, gold catalyst can potentially be unintentional impurities incorporated into nanowires which can degrade device performances. For example, Au behaves as an impurity in Si by trapping electrons and holes by deep level recombination centers[9]. Inevitably, some traces of Au contaminate the process equipment or end up incorporated in the nanowire growth. Hence, Au is not compatible with modern CMOS technology.

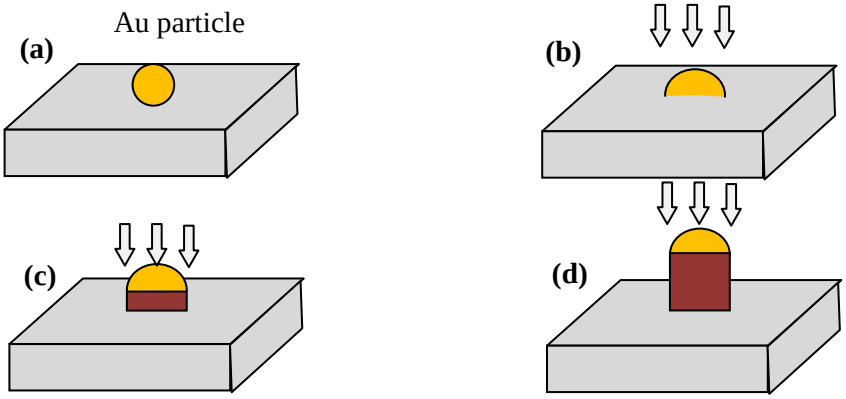


Figure 1. Catalyst assisted nanowire growth process. (a) Metal seed particles are formed and/or deposited onto a substrate. (b) The sample is heated to a desired growth temperature and growth materials introduced, whichever alloy with the particle. (c) When an appropriate supersaturation of growth material is achieved, nucleation occurs at the particle-crystal interface. (d) Nanowire growth occurs at the particle-wire interface. [10]

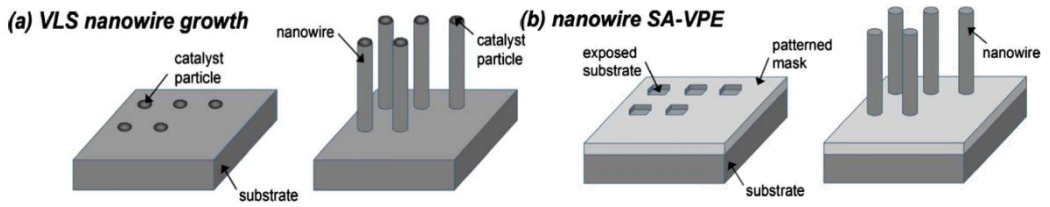


Figure 2. Schematics of (a) catalytic VLS nanowire growth and (b) non-catalytic nanowire SA-VPE.[1]

Motivated to eliminate unintentional incorporations of impurities, people have proposed non-catalytic growth methods. Figure 2 shows catalytic and non-catalytic growth methods side by side. Figure 2 (b) demonstrates selective area vapor-phase epitaxy (SA-VPE) growth method[11]. First of all, a less than 50 nm thick electric mask is patterned on a substrate, following with wet/dry etch to open windows of generally 50-200 nm diameters. Then metallorganic or gaseous precursors are flown onto the heated substrate. In this case, growth only occurs in the exposed substrate regions. People have argued whether III/V SA-VPE could be considered 'pure' epitaxy since the group-III species such as Ga and In during nanowire growth are partially served as catalysts. Therefore, SA-VPE is more often termed 'self-catalytic'. Experiments of selective-area metallorganic vapor-phase epitaxy (SA-MOVPE) of InAs nanowires on Si substrate have reported nanostructures of quality comparable to those grown by VLS[12].

Nanowire devices discussed in this thesis are grown by SA-VPE strategy by Professor Diana L. Huffaker's group in University of California at Los Angeles. Detailed growth conditions will be discussed in experiment part. Figure 3 shows the scanning electron microscopy (SEM) images of GaAs nanowires with 1 μm pitch, and InAs nanowires with 300 nm pitch. Such nanowires show hexagonal morphology from the top views which indicates high quality single crystal structures of the nanowires. From tunneling electron microscopy (TEM) image, the InAs nanowire shows existence of

stacking faults defects, which can be related to electrical measurement results detailed in experiment session.

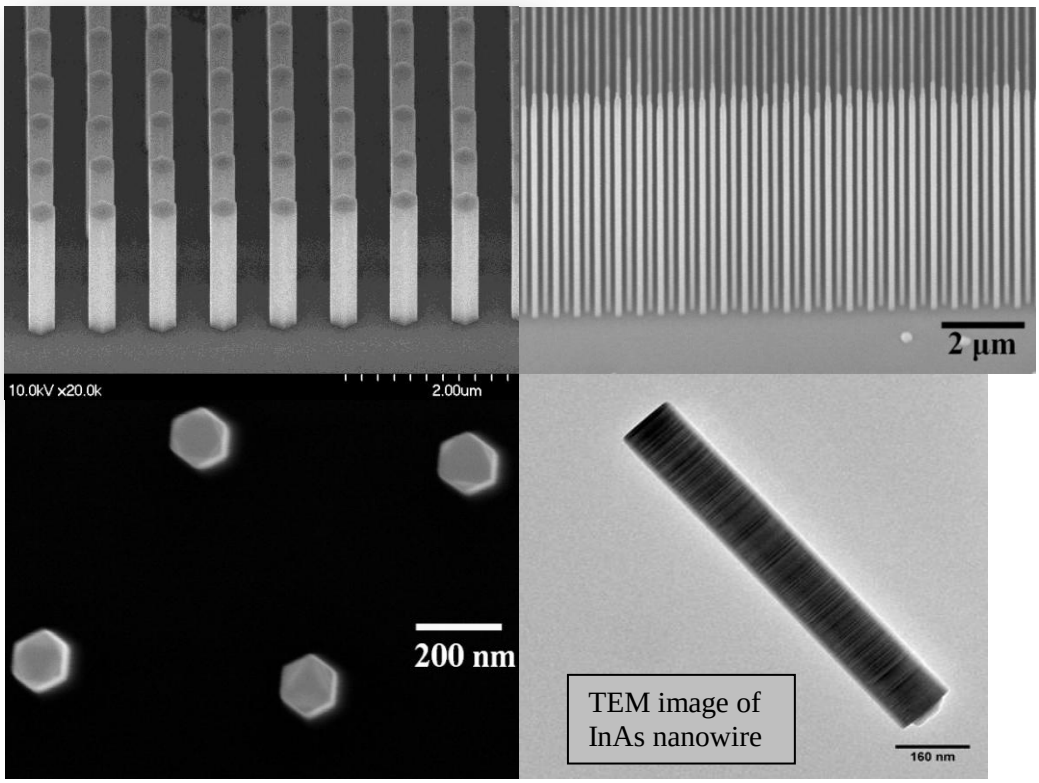


Figure 3. *Scanning electron microscopy (SEM) images of (a) GaAs nanowires with 1 μm pitch, (b) InAs nanowires with 300 nm pitch, (c) InAs nanowires top views, and (d) tunneling electron microscopy (TEM) image of a InAs nanowire, with scale bar of 160 nm. Nanowires are grown by our collaborated group in UCLA using SA-MOCVD growth method. TEM image is taken by Andrew Lin from UCLA group.*

1.3 Issues Of Device Performance

One affecting factor for nanowire device performances is crystal defects coming from growth process, the other major factor is surface condition of nanowires. Comparing to other structures such as bulk or thin film, nanowire structure has much larger surface to

volume ratio which causes strong effects from surface conditions. From device point of view, people often observe several orders current level increase for nanowire devices after applying surface passivation[13]. Hence surface plays a important role in nanowire devices. In our GaAs nanowire devices, we also observe clear current level increase after surface passivation of certain time. However, no clear trace for InAs nanowire devices have been observed in this work.

There are ways to take advantage of this large surface to volume ratio of nanowires. One of the future work for this nanowire device project is to define surrounding gate[14] along the nanowires which theoretically will give better control of carriers within the nanowires than bulk devices. Other possible ways to take advantage of large surface structure is to make sensors[15], since larger surface to volume ratio of nanowires in theory will enhance the sensitivity of detection.

1.4 Scope Of The Work

The scope of this project covers fabrications and electrical measurements on GaAs and InAs nanowire devices. Both type of nanowires are fabricated into devices through similar processes, including electron beam lithography (EBL), thermal vapor deposition of metals, and some other processes. For GaAs nanowire devices part, discussions will be mainly focused on lateral devices. It will cover current-voltage measurement results, transport properties, surface passivations, and some of device failures. For InAs nanowires, discussions will be focused on lateral devices. In this part, it will cover I-V measurement results, gate response, temperature dependent results.

Chapter 2

GALIUM ARSENIDE NANOWIRE GROWTH, FIELD-EFFECT TRANSISTORS FABRICATION AND DATA ANALYSIS

2.1 Background

GaAs, is one of the most promising III/V semiconductors for devices such as light emitting diodes (LEDs)[5], lasers[16], field effect transistors[17], and monolithic microwave integrated circuits[18]. GaAs has five times higher electron mobility than Si, which makes it promising for high speed and low power consumption integrated circuits. Meanwhile, GaAs offers the highest energy conversion efficiency in photovoltaic devices. On the other hand, vertical devices are attractive for implementation beyond the 22-nm node because an improved electrostatic control within the channel can be achieved by applying wrap gate technology[14]. Recently, Intel has announced new technology of FinFET[19]. With wrap gate, a more aggressive scaling of the gate length is allowed. Besides, the coaxial structures such as core-shell p-n junctions realize high optical absorption.

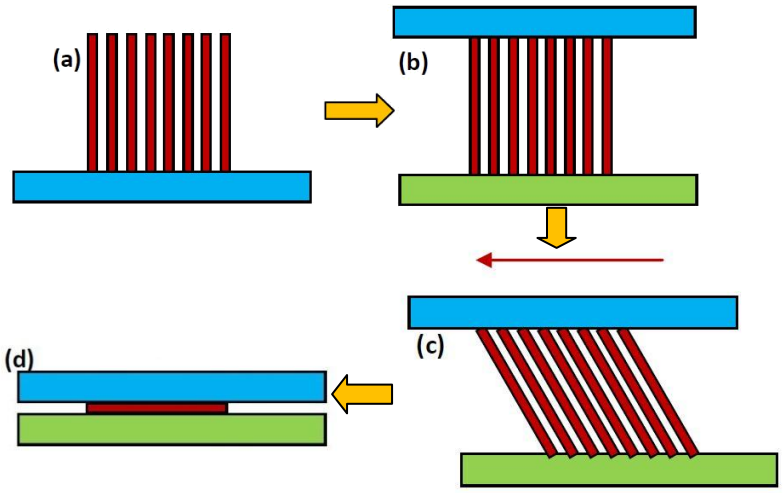
In this work, we start with lateral devices, in which we study transport properties, experiment processes to improve device performance and make analysis of failure mechanisms.

The GaAs nanowires are grown through catalyst-free MOCVD growth method by our collaborating group in UCLA. Growth substrate is heavily doped (n^+) GaAs (111) B wafer which has doping concentration of around 1×10^{18} cm^{-3}. The growth substrate is coated with a SiO_2 template with thickness of 25 nm. After spin coat with PMMA, electron beam lithography (EBL) is used for patterning windows which have diameters of 200 nm and pitch of 300/600 nm. After develop, etch through SiO_2 within the windows to expose the growth substrate. Following that, nanowires grows from the windows through

such catalyst-free MOCVD. P-type GaAs nanowires are grown by introducing Zn as p-type doping during the growth and the doping concentration is 3×10^{18} cm^{-3}. The grown nanowires typically have diameters of 100 nm and length of around 5 μm.

2.2 Method Of Mechanical Transfer

From growth substrates, we mechanically transfer the vertical nanowires onto other substrates to make them lateral for device fabrications. Figure 4 shows schematics of the mechanical transfer of nanowires. We place the growth substrate onto a clean Si piece. This Si piece is typically spin-coated with HMDS to help nanowires stick with Si piece. Then gently press the growth substrate and slowly slide it along one direction. After several times of such transfers, trace of nanowires on the Si piece can be observed. From microscope, one can see most of transferred nanowires are lying down with a direction consistent with mechanical transfer direction. On this so called 'first transferred' substrate, nanowires are tended to form clusters which makes them hard for fabricating into devices. Therefore, nanowires used for fabricating devices are transferred again from the first-transferred Si piece to another patterned piece. Such transfer is an intrinsically low temperature process, therefore can be applied to various substrate, including flexible polymer substrate.



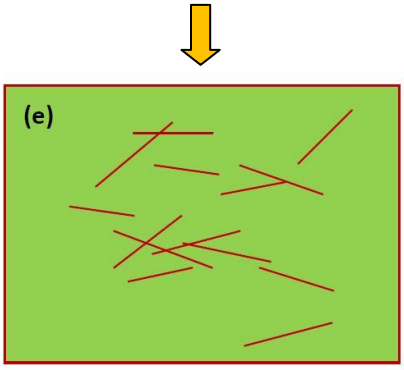


Figure 4. Schematics of nanowire transferring mechanically from growth substrate to Si piece to make them lateral. (a) Vertical GaAs nanowires on growth substrate, in this case heavily doped (n^+) GaAs (111) B substrate. (b) Place the growth substrate onto a silicon piece. (c) Gently press the growth substrate onto Si piece and slowly slide the piece along the direction pointed by the arrow. (d) After long enough sliding distance, vertical nanowires are supposed to be lateral to the Si piece. Some of the nanowires are attached to the Si piece. (e) After first transfer, the density of nanowires on Si piece is very dense and nanowires are tended to be clusters.

2.3 Patterned Substrates For Nanowire Coordinates Calibration

As mentioned before, nanowires fabricated into devices are transferred onto patterned substrates from first transferred Si piece. There are two types of alignment markers applied to this project.

The first type is T shape markers with 20 μm in line width and 140 μm in length. The whole single chip design is made by 24 x 24 arrays of T shape patterns with the pitch of 400 μm. Thus, the area of the single chip is around 1 cm by 1 cm, which is suitable to assemble to chip carrier for various measurements. These markers are designed for calibrating positions of nanowires by SEM or optical microscope depending on the accuracy to achieve and for providing global markers for EBL system to perform

alignment. Different number of small bars are added to both sides of T-shape patterns with a pitch of every four rows and columns, so that a position of nanowire correlating to one of the T shape patterns with bars is easy to tell. Providing with the four global markers, one can easily find the center of the chip and rotate the chip if necessary. Steps for fabricating T shape markers onto Si pieces are shown in figure 5.

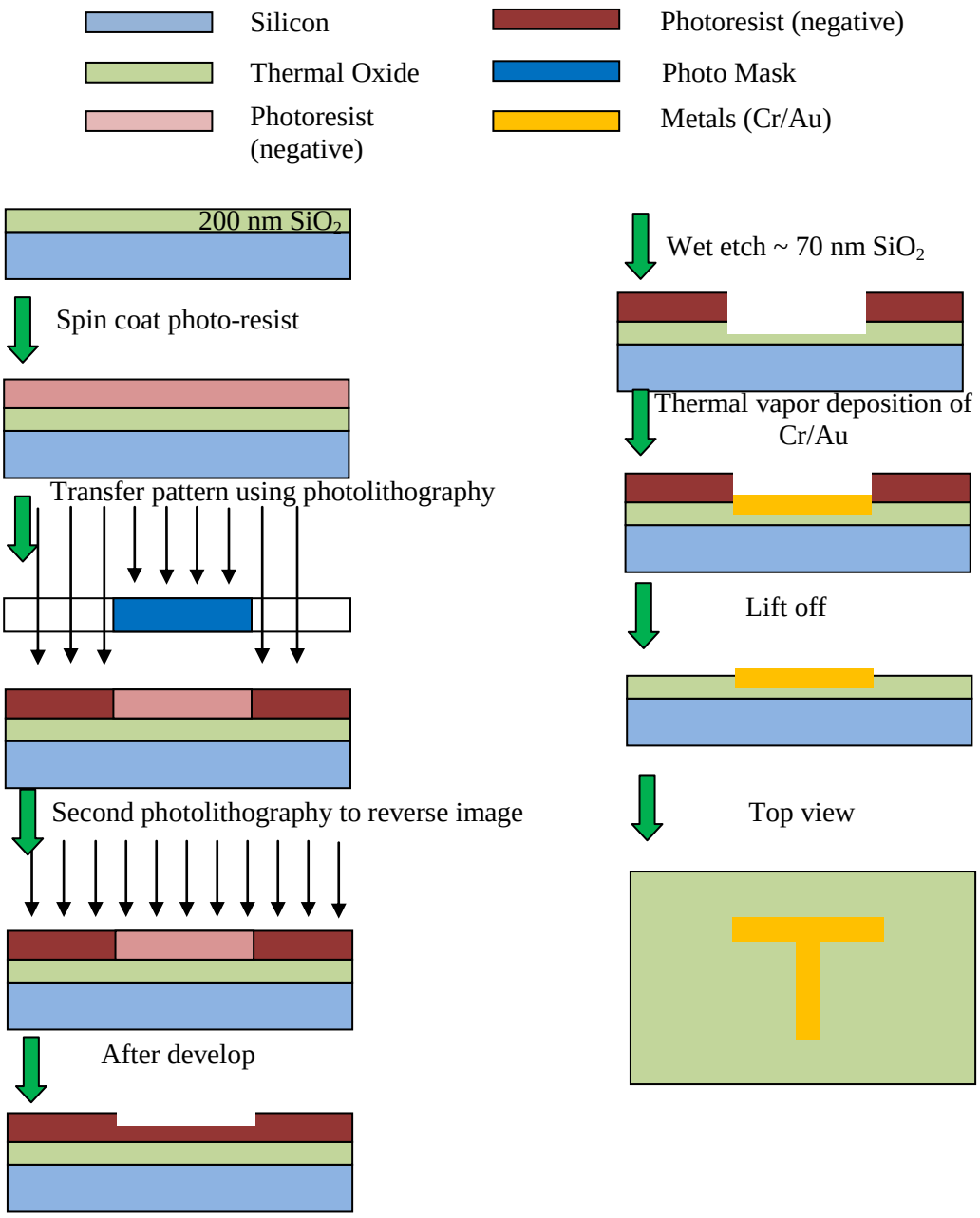


Figure 5. Schematics show steps of fabricating T-shape markers. Intentionally make T-markers to be flat with chip's surface to avoid nanowires trapping at edges of markers during mechanical transfers.

Before deposition of metals, wet etch process is introduced to etch away around 70 nm SiO_2. In this way, after deposition of Cr/Au, surface of such patterned piece is relatively flat which effectively avoids nanowires clustered at edges of T-shape markers. Also for these patterned substrates, back gate is made before nanowire dry transfer. Processes include spin-coat photoresist AZ 4330 and bake, then BOE etch of 200 nm SiO_2, finally deposit metals.

There are pros and cons of using such T shape markers, which are listed in table 1. We started with such T shape markers and were not satisfied with the accuracy of placing electrodes onto single nanowires, which motivated us to design better markers for our devices.

Table 1. Pros and cons of using T shape markers for nanowire position calibrations.

Pros	Cons
(1) High yield fabrication process. Able to fabricate one wafer for each run, which can contain tens of working pieces. (2) Large enough size of markers for optical microscope. (3) Flattened T markers avoids trapping nanowires around edges.	(1) Not effective using SEM to calibrate positions. (2) Hard to achieve high accuracy of EBL alignment. (3) Pitch is too large to effectively finding nanowires.

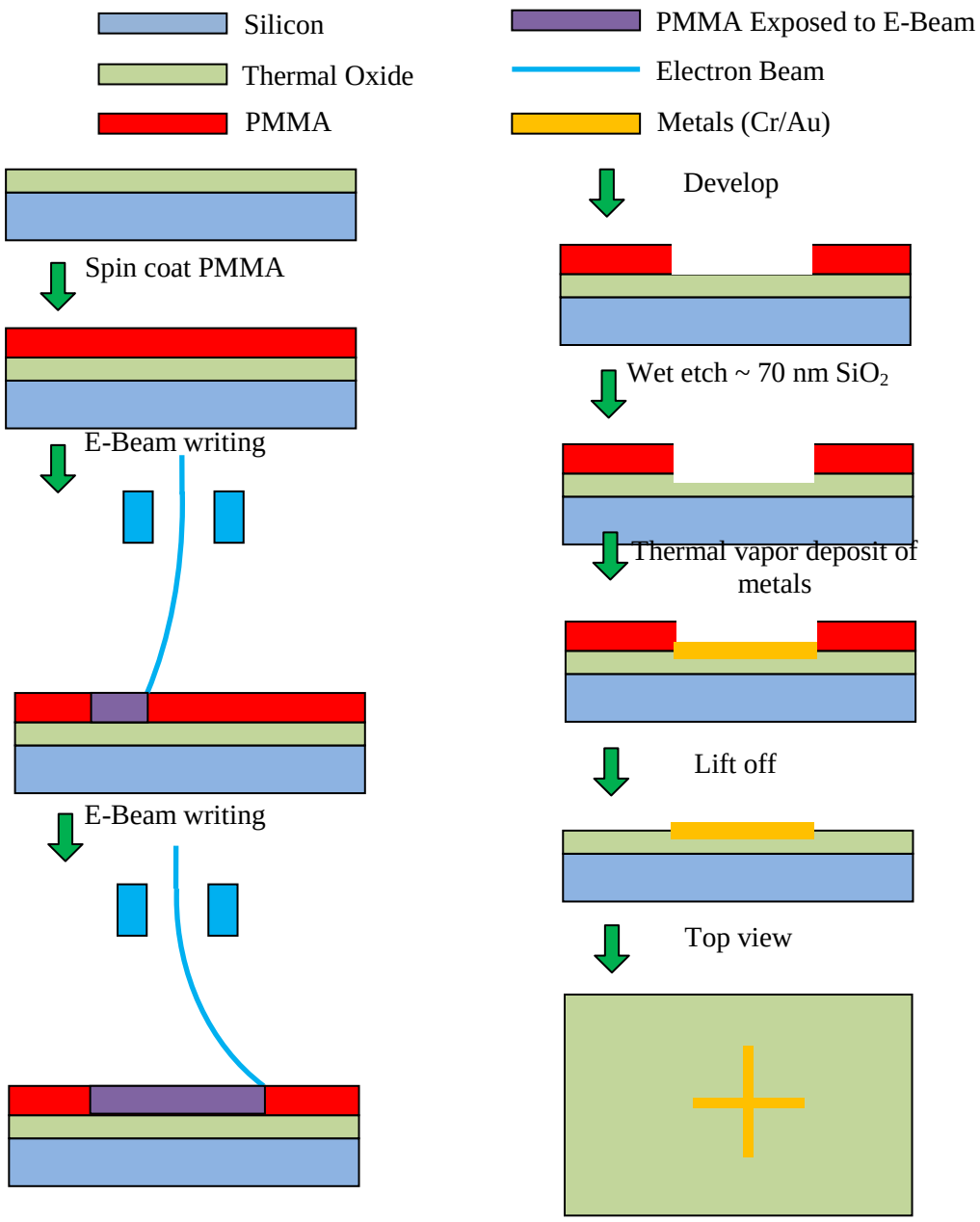


Figure 6. Schematics of steps of fabricating cross shape markers using EBL.

Cross shape markers have line width of 3 μm, length of 50 μm and pitch of 150 μm with a design of 55 x 55 arrays in a single chip. Similar to T shape markers, small numbers are added to both sides of cross shape markers with a pitch of every four rows and columns. Different from T shape markers, cross shape markers are fabricated by EBL

instead of photo-lithography. Consequently, cross shape markers are smaller in size, finer in features and denser in separations than T shape markers. With the changes of markers, we are able to locate nanowire positions more effectively by using SEM and with better accuracy. In addition, these markers provide finer alignment in the step of EBL writing electrodes patterns. In this way, more electrodes can be defined along a single nanowire which increase the yield of devices. The drawbacks of using such patterned pieces are the low yield and high cost of using EBL. Steps of fabricating cross shape markers are shown in figure 6.

After transferring nanowires onto patterned chips, we calibrate positions of nanowires regarding to markers. An effective way of performing this calibration is described as follow. Firstly, record rough positions of nanowires through optical microscope observations. In this step, choose those spots where one single nanowire is sitting with clean surroundings. With general ideas of nanowire candidates' rough positions, one can easily find those nanowires using SEM. Then take zoom-in images of proper nanowires for further calibration. The requirements for nanowires are that such nanowires are close enough to the nearest marker so that one is able to take a proper zoom in image with both nanowire and the center of nearest marker showing in the image, meanwhile, such nanowires are not too close to the marker to place electrodes over the nanowire without getting short circuit. Figure 7 (a) shows a good candidate of nanowires for device fabrication. Based on calibrated positions of nanowires, we design electrodes onto single nanowire, and then define large pads and connect them with electrodes for electrical measurements (figure 7 (b)).

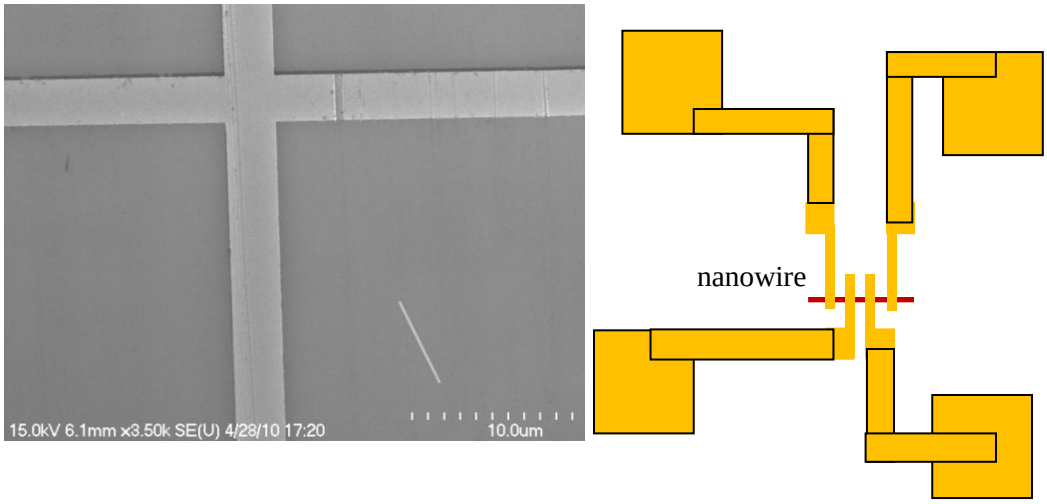


Figure 7. (a) SEM image of a single nanowire close to a cross shape marker. (b) Schematic of single nanowire FET design.

2.4 Device Fabrication

After EBL writings of device patterns and development, several cleaning steps are necessary to be done before contact metal deposition. Use oxygen plasma to remove PMMA residue with 50 watts for 30 seconds. Then dip chips into ammonium hydroxide solution (NH_4OH : H_2O = 1 : 20) for 10 seconds to remove native oxide. After these cleaning steps, deposit contact metals for GaAs nanowire devices. Since nanowires we have are p type GaAs, contact metals combinations chosen here are Cr/Au or Ti/Au. Typically, we use Edwards#2 to deposit Cr/Au, or e-beam evaporation to deposit Ti/Au. Right after lift-off, we typically perform rapid thermal anneal of GaAs nanowire devices at 400° C. Figure 8 shows SEM image of GaAs single nanowire FETs. For this batch of devices, electrodes are not designed to be uniformly distributed onto a single nanowire. The reason for this design is to compare transport behaviors of devices with different channel lengths. Electrodes A and D are designed to be fatter than electrodes B and C for better chance of covering the nanowire at edges. However this design also introduces

asymmetric electrical behavior to measurements taken for electrode combinations of AB or CD.

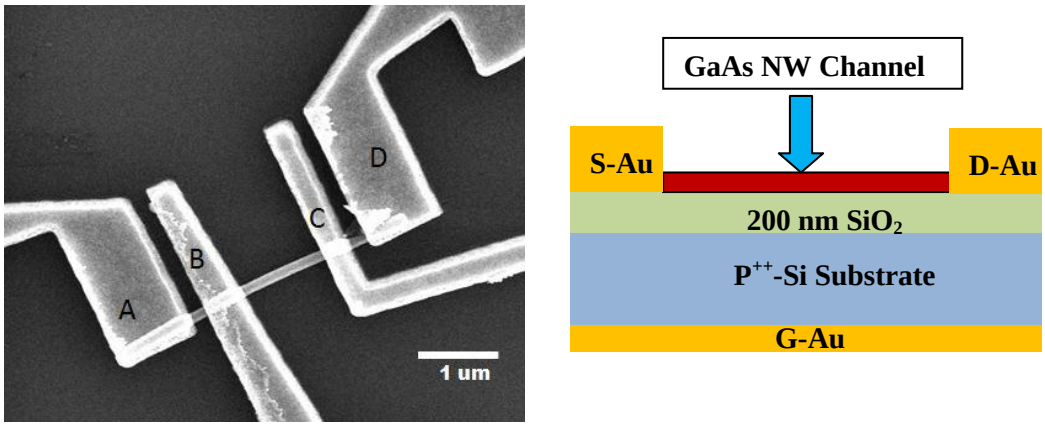
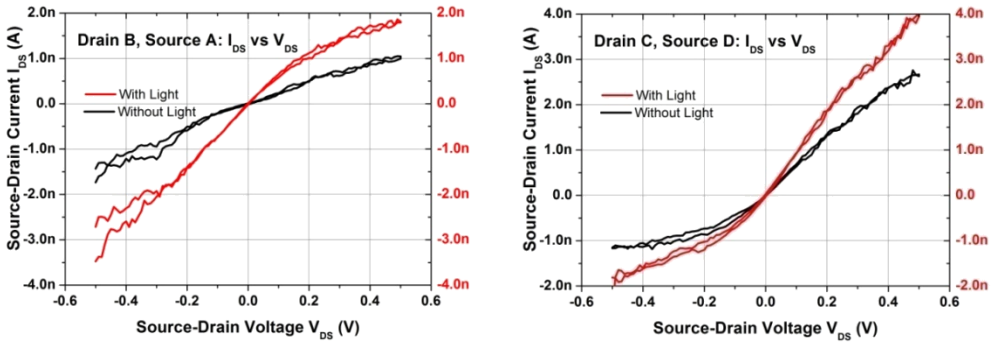


Figure 8. SEM image (left) of GaAs nanowire FETs. Four electrodes are placed onto a single nanowire. Backside of whole chip is deposited with metals to serve as global back gate. Schematic (right) of one FET device structure on single GaAs nanowire.

2.5 Electrical Measurement Results



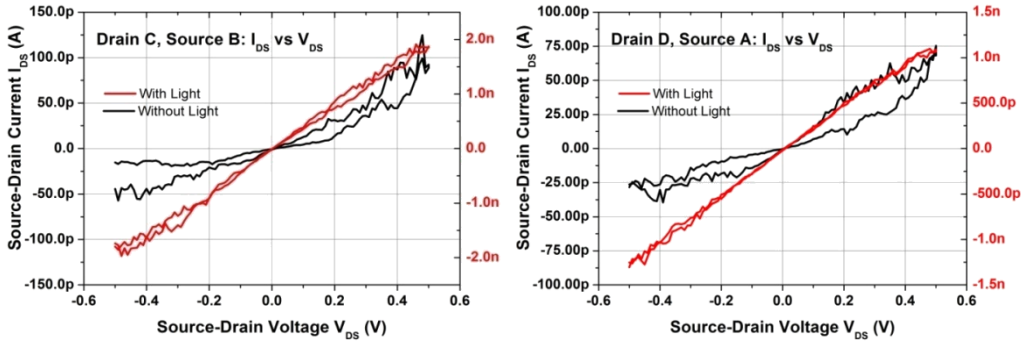


Figure 9. Plots of source-drain current vs. source-drain voltage measurement results from devices of a single GaAs nanowire. Onto this nanowire, four electrodes are successfully attached. Four electrode pairs are chosen for I-V measurements.

Source-drain current (I_{DS}) vs. source-drain voltage (V_{DS}) measurement results are shown in figure 9. In this batch of devices, contact metals are Ti/Au, where Ti is adhesion layer. The measurements are taken under room temperature without backside gate bias. These results are measured from device show in figure 8 SEM image. During the measurement, V_{DS} are swept from -0.5 V to +0.5 V with increment of 0.01 V and with forward and backward sweeps. As expected, I-V curves show more symmetric behaviors for electrode-pairs AD and BC than electrode pairs AB and CD. None of four electrode-pairs indicates existence of Schottky barrier. All devices show sensitivity of light presence. With longer channel length, measured electrode-pair experiences a larger difference with light shining on device. For electrode-pairs BC and AD, this difference caused by light is around 20 times, while difference for AB and CD is around twice. This can be explained with the assumption that with fixed intensity of light, such light induced extra carriers per length within the nanowire channel is constant. However, it is not exactly scaled with channel length. To explain this, one have to consider that the channel length of AB and CD electrode pairs is around 200 nm which is much shorter than the wavelength components in light source (mostly within visible light range). Hence, only

evanescent wavelength can be absorbed by these channels. In the case of long channel length without light shining on the device, it is clear to see hysteresis when we perform dual sweeps. However, with presence of light, this hysteresis becomes less obvious. This may indicate the existence of surface states[20] for such GaAs nanowires. With higher concentration of carriers by shining light on channel, surface states are filled out and becoming less significant in affecting device performance. Devices have very low current levels, from which a resistance of around 10^{10} ohmn/μm is calculated.

Results of I_{DS} vs. V_{DS} with different backside bias are plotted in figure 10. With more negative backside bias, larger source-drain current I_{DS} is observed, which indicate p-type behavior of such GaAs FETs. In this figure, V_{DS} is swept to 2 V, only positive side of V_{DS} range is presented.

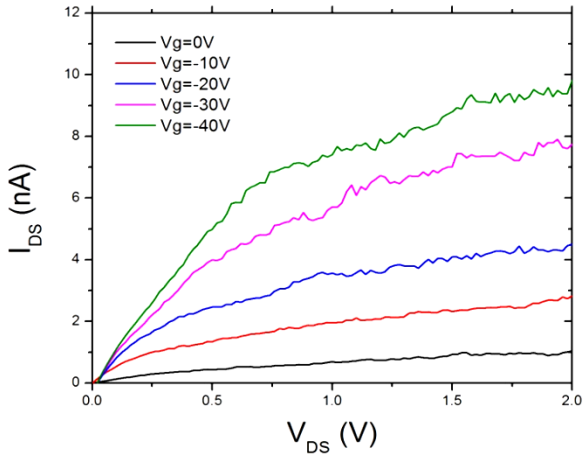


Figure 10. Plots of I_{DS} vs. V_{DS} with different backside gate bias V_g. The more negative V_g is, the larger I_{DS} is, which indicates p-type behavior.

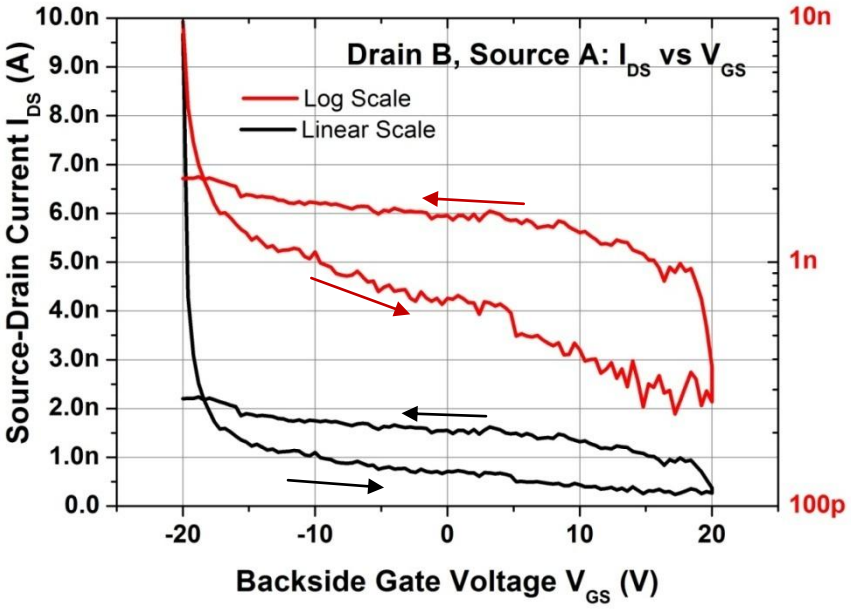


Figure 11. Plots of gate response results for electrode-pair AB, in linear scale and log scale. Arrows shows the sweep directions.

Figure 11 is gate response results for electrode-pair AB in linear and log scales, with SEM image shown in figure 8. During this measurement, backside gate voltage V_{GS} are swept from -20 V to +20 V with increment of 0.4 V and with dual sweep directions. Also source-drain voltage is biased at 0.5 V.

2.6 Surface Passivation

From tunneling electron microscopy (TEM) images, non-uniform oxide layers are found on GaAs nanowire surface, see in figure 12. TEM work is done by Luying from Dr. David Smith's group in physics department. Consider nanowires' large surface to volume ratio, such oxider layers grown on surface can have strong effect of device performance. To eliminate this possible killing factor, attempts of surface passivation have been done on these GaAs FETs. In this surface passivation process, ammonium surfide solution is used to etch away native oxide layer on GaAs nanowire surface. We

dip chips into ammonium surfide solution for different time period and then perform electrical measurements to check device performance. Surface passivation results are shown in figure 13. We observes a small current increase after 10 minutes dip in ammonium hydroxide solution. Then we perform another 10 minutes of chemical treatment with total time period 20 minutes, and achieve further increase of current. With another 10 minutes (30 minutes in total), current level almost remains the same as 20 minutes in total. However, when time of chemical treat increases to 80 minutes, current level drops a lot. Several of our devices appear same trend. Around 20 to 30 minutes gives us best results. During such surface passivation process, the number of working devices gradually decreases as total chemical treatment increases. Longer than 80 minutes total chemical treatment time, no device survives. Figure 14 shows SEM images of two devices after surface passivation process. Left image shows non-uniform diametr along the wires, while the right image shows a nanowire broken into two parts. Theory is when dipped in ammonium sulfide solution electrochemical effect occurs which leads to non-uniformly etching along nanowires.

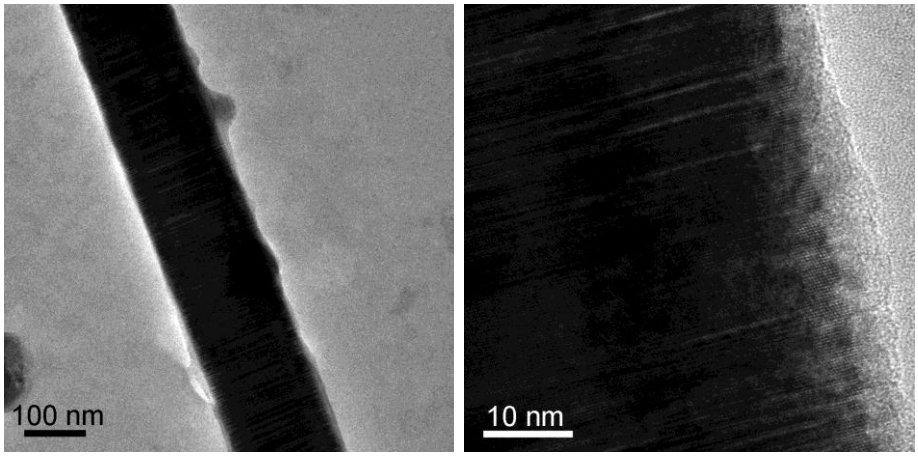


Figure 12. Tunneling electron microscopy (TEM) images of a single GaAs nanowire. At edges of nanowires, non-uniform layer of oxide is observed. TEM images are taken by Luying Li from our collabrating group in physics department.

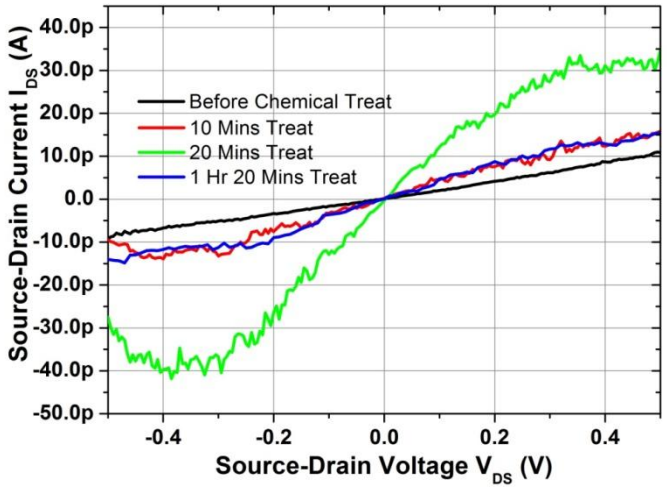


Figure 13. Results of surface passivation with varying time periods. Ammonium sulfide solution is used. 20 minutes treatment includes two seperate 10-minute treatment. After each 10-minute, electrical measurement is taken. 1 hour 20 minutes treatment includes two 10-minute and afterwards two 30-minute chemical treatments.

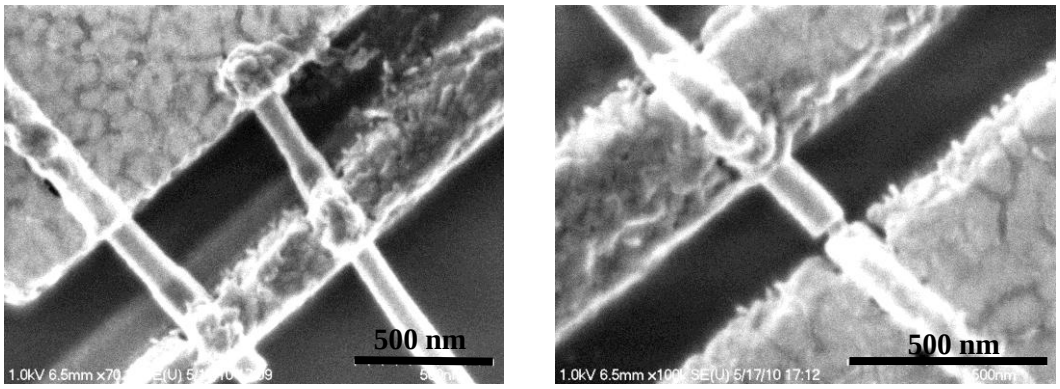


Figure 14. SEM images of GaAs nanowires after surface passivation process. In left one, one can see diameter of nanowires become non-uniform. In the left one, a single nanowire seems to break into two parts.

Chapter 3

INDIUM ARSENIDE NANOWIRE GROWTH, FIELD-EFFECT TRANSISTORS FABRICATION AND DATA ANALYSIS

3.1 Background

This chapter covers work on InAs nanowires.

Bulk InAs material shows good electrical properties which motivate us to study on InAs nanowires. InAs bulk materials have high mobility, around 40,000 cm^2/Vs at room temperature, which is promising for fabricating high-speed devices. Also bulk InAs has a small bandgap of 0.354 eV, which makes it promising for low power devices. Because of it's a direct bandgap material, it is considered to be candidate for opto-electronic devices as well, such as avalanche photodiodes[21]. Vertically placed nanowires directly grown on the substrate of interest would enable high-density integration of such devices and new functionalities. It has been shown these vertically aligned nanowires can be grown at desired locations on the nano-patterned surface prepared through lithographic processes. However, detailed electrical characterization of nanowires grown with such technique is necessary to understand their properties.

3.2 Device Fabrication

InAs nanowires are first grown on semi-insulating InAs (111)B substrates without doping using a catalyst-free technique via selective-area MOCVD growth. InAs nanowire arrays are designed to have a pitch of 300 nm / 600 nm. Typically, after such growth process, nanowires are 5 μm - 7 μm in length and have diameters of around 100 nm. From SEM top view, we can see nice hexagonal structure which indicates high quality of single crystal growth. (Figure 3)

Lateral devices were made out of InAs nanowires. Nanowires are mechanically transferred from the growth substrate onto the highly doped p type Si substrate with 200 nm thermal-growth oxide layer. Here patterned substrates with cross-shaped markers are used for calibrating nanowires' positions. Electrodes are defined by e-beam lithography (EBL). Before deposition of contact metals, samples are dipped in ammonium hydroxide to remove native oxide layer. Following that step, 20 nm Cr and 250 nm Au are deposited as metal contacts. After lift-off, we spin-coat 80 nm PMMA covering the surface of the devices and baked PMMA for 170˚C for 15 minutes to protect the surface of devices, in addition, contact metals are annealed during this step.

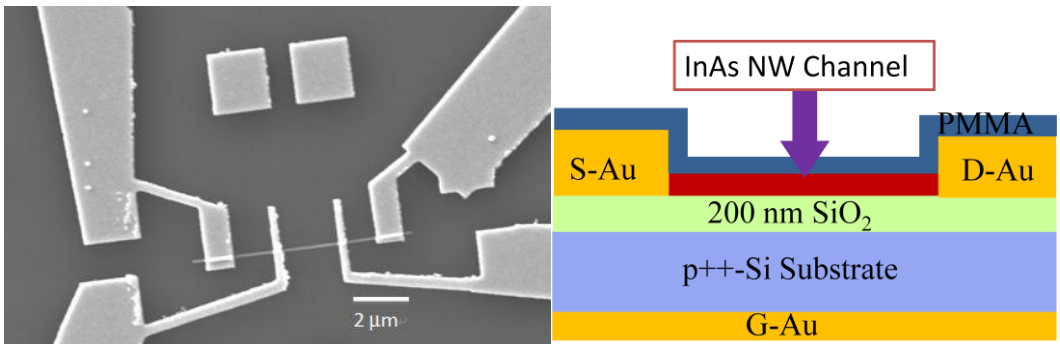


Figure 15. (a) SEM image of FETs made of a single InAs nanowrie with scale bar of 2 µm. (b) Schematic of device structure of InAs NW FET. After lift-off, 80 nm PMMA is spin-coated to cover the whole device for surface protection.

3.3 Electrical Measurements And Field Effect Mobility Extraction

Then electrical measurements at room temperature are taken upon the devices. Source-drain voltage V_{DS} are swept from -0.8 V to +0.8 V. Source-drain current I_{DS} shows symmetric behavior. I_{DS} vs. V_{DS} with different backside gate bias V_{GS} are measured where V_{GS} starts from -10 V to + 5 V with increment of 2.5 V. I-V results are plotted in figure 16. At small V_{DS} range, devices are working under linear region. I_{DS}

starts to saturate at around 0.2 V. All devices show n type behaviors, since current level increases as backside bias goes more positive. From I-V curve with V_{GS} = 0 V, one obtains resistance roughly to be 100 kΩ/μm, which agrees with other groups work on InAs FETs[22, 23]. In log-log scale, one can get a better view of separation of curves and their linear behavior at V_{DS} < 0.2 V region.

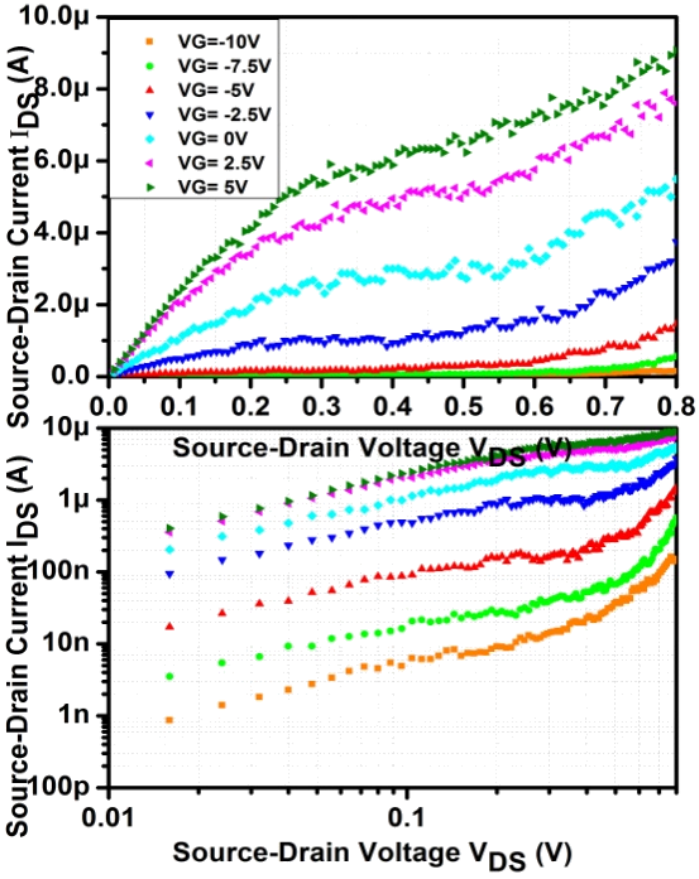


Figure 16. I-V measurement results at room temperature with different backside bias, linear-linear plot (top) and log-log plot (bottom). Channel length is around 1 μm.

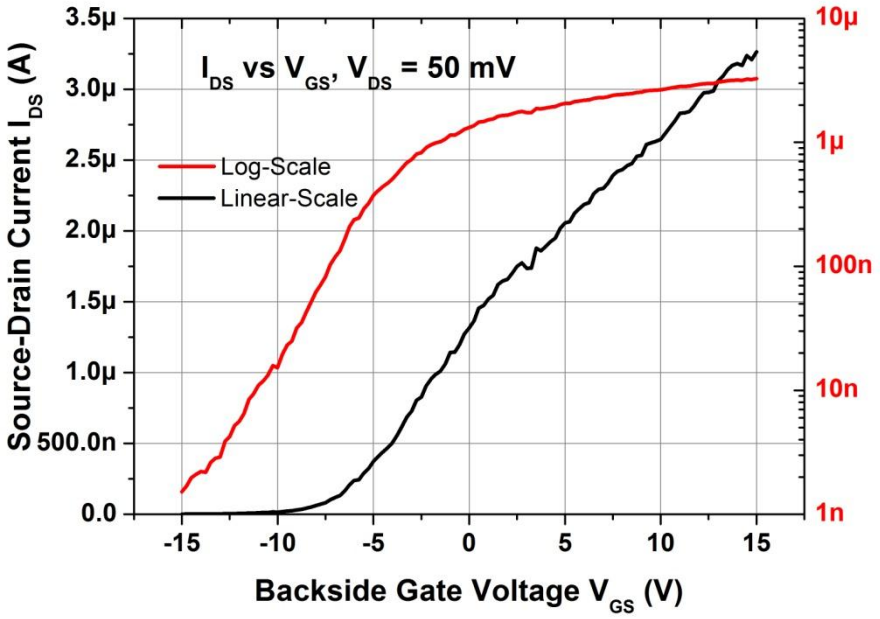


Figure 17. Plots of gate-response measurement results, in linear scale and log scale. Source-drain voltage is biased at 50 mV, which indicates device working at linear region according to I_{DS}-V_{DS} plot. Only forward sweep (V_{GS} swept from -15 V to + 15 V) is presented here. Sweep rate of V_{GS} is 1 V/s. Dual sweep shows hysteresis.

Figure 17 shows gate response results. In this measurement, source-drain voltage is set to be 50 mV, and backside gate voltage is swept from -15 V to + 15 V with increment of 0.25 V. From gate response measurement results one can extract field-effect mobility and carrier concentration. Formulas used for calculations are,

$$\mu_{FE} = g_m \frac{L_G^2}{C_g V_{DS}} \qquad n = \frac{I_{DS} L_G}{q \mu_{FE} V_{DS} A}$$

where $C_g = \dfrac{2\pi\varepsilon L_G}{\ln\left(\dfrac{t_{ox}+r}{r}\right)}$ and $g_m = \left.\dfrac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}=const}$

From figure 17, we obtain field-effect mobility of 551 cm^2/Vs and carrier concentration of 3.91×10^{17} cm^{-3}. The correlated parameters for calculations are shown in Table 2. Calculated field effect mobility and carrier concentration for 26 devices are plotted in figure 18.

Table 2. Correlating parameters for one device to calculate field-effect mobility and carrier concentration.

Parameter	dI_{DS}/dV_{GS}	L_G	C_g	V_{DS}	I_{DS}	t_{ox}	r
Unit	S	nm	J/K	mV	A	nm	nm
Value	2.00E-07	650	3.27E-17	50	8.77E-7	200	35

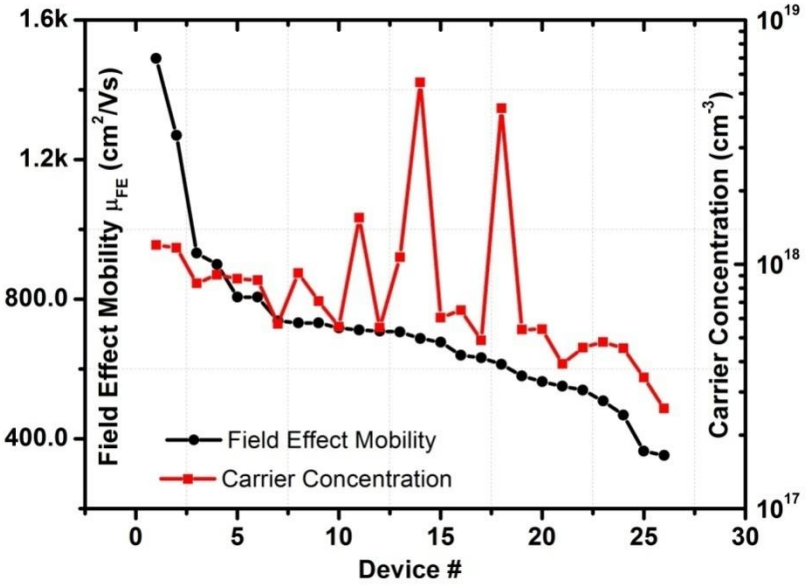


Figure 18. Plots of extracted field effect mobility and carrier concentration of 26 devices. Field effect mobility is plotted in linear scale (left axis), while carrier concentration is plotted in log scale (right axis).

Among all 26 working devices, most of them have field-effect mobility sitting between 400 to 1000 cm^2/Vs. Two devices achieve field effect mobility beyond 1000 cm^2/Vs. The highest number acquired is 1500 cm^2/Vs. Meanwhile, two devices have field effect mobility even below 400 cm^2/Vs. Figure 19 summarizes field effect mobility obtained by these 26 devices from the same batch of device fabrication. As shown in figure 1, TEM image of such InAs nanowire shows clearly stacking faults along the wire, which are not uniformally distributed. These stacking faults play an important role in device performances.

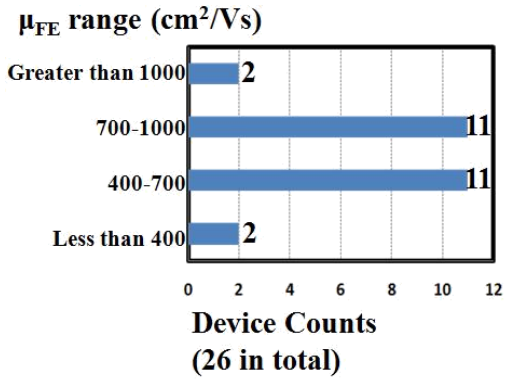


Figure 19. Summary of Calculated field effect mobility for all 26 devices from one batch of device fabrication.

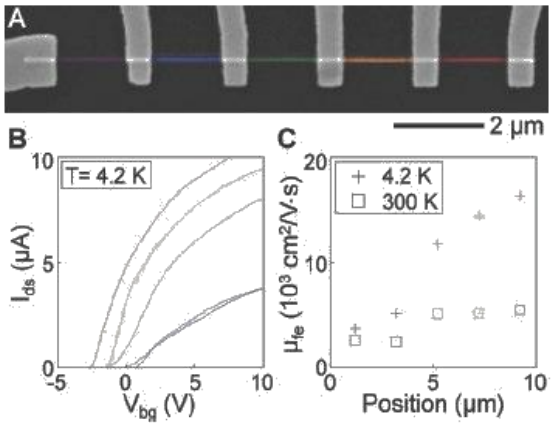


Figure 20. (a) False color SEM image of a device with six electrical contacts. (b) I_{ds} as a function of V_{bg}, while V_{ds} = 100 mV. (c) μ_{fe} extracted from (b).[7]

It has been reported that defects play an important role in devices performance[7]. In the work, people intentially grew nanowires with different density of defects at different segments by varying growth temperature and fabricated devices out of such nanowires. Deivce SEM image is presented in figure 20 (a). What they observed from gate reponse measurements (figure 20. b) is that with lower density of defects, I-V curve has steeper slote which leads to higher field-effect mobility (figure 20. c). At room temperature, 2x difference of field-effect mobility is observed. An even more pronouced 4.4 x difference is observed at low temperature of 4.2 K.

3.4 Temperature Dependent Measurements And Activation Energy

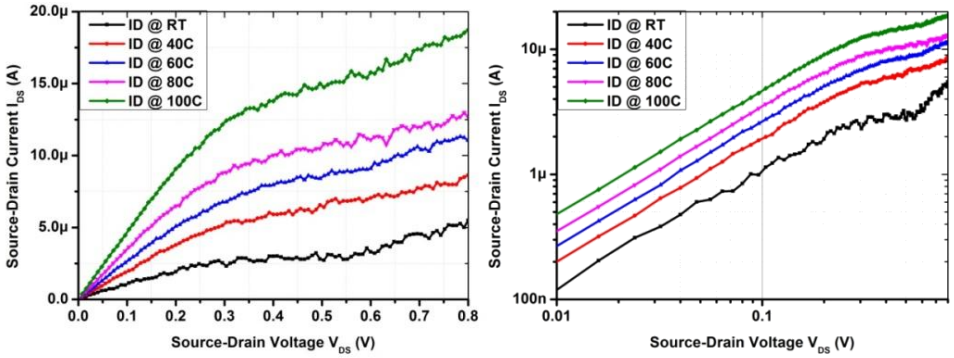


Figure 21. Plots of temperature dependent measurement results in linear-linear scale (left) and log-log scale (right). RT stands for room temperature and is 26˚C in this case. Measurements are taken under zero backside bias, with five different temperature points.

Temperature dependent measurements are also conducted on these devices to investigate thermal excitations. Figure 21 shows results of temperature dependent measurements with zero backside bias and with temperature varies from room temperature (26˚C) to 100˚C. Current level increases as temperature goes up, which suggests that thermal excitations occur here. There are four possible origins of thermal excitations, Schottky contacts, impurity dopants and traps, surface and potential barrier.

I_{DS} vs. V_{DS} curves for these devices have quite high current level and symmeteric behavior for both positive and negative sides of source-drain voltage which indicates ohmic contact. Considering devices have been annealed for contacts, it is also unlikely to have Shockley barriers existing in these devices. Impurity dopants and traps are not considered to be contributers here, because these InAs nanowires are grown by catalyst-free growth method, which as mentioned before, is considered as 'pure' growth method. For these devices, we intentionally spin-coat PMMA to protect the surface. Hence we don't consider affects by surface either. Therefore, we investigate relationships between potential barriers and thermal excitations.

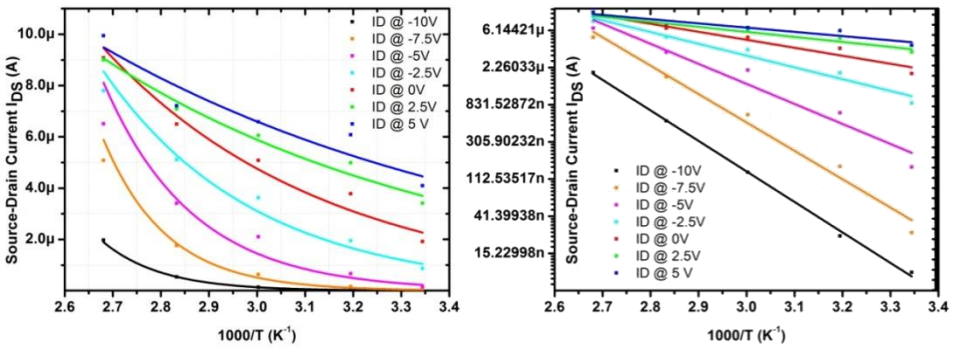


Figure 22. Arrhenius plots in linear scale (left) and natural log scale (right), with different backside bias. Dots are raw data, lines are natural log fitting trend lines.

Plots in figure 22 are Arrhenius plots[24]. Extraction of Arrhenius plot includes following steps. For each backside bias, we extract I_{DS} value at V_{DS} equals to 0.2 V from I-V plot similar with Figure 21. In this way, five current points according to five temperature points are obtained. Plot I_{DS} vs. inverse temperature times 1000 with different backside bias to get plot shown in figure 22. Arrhenius plot helps us to extract activation energy by utilizing following equations,

$$I_{DS} = Ae^{(-\frac{E_a}{kT})} \Rightarrow E_a = -k\frac{\partial \ln I_{DS}}{\partial(\frac{1}{T})}$$

Here E_a is denoted as activation energy, which is correlated with potential barriers. According to equations, activation energy is proportional to slopes of curves. Figure 22 also reveals that with more negative backside bias, the extracted activation energy is higher, which indicates with more negative backside bias, electrons experience higher potential barrier. Results for four devices are listed in table 3, also plotted in figure 23.

Table 3. Activation energies for four devices with different backside bias.

Backside Bias (V)	Device#1 Ea (eV)	Device#2 Ea (eV)	Device#3 Ea (eV)	Device#4 Ea (eV)
-10V	0.71	0.71	0.65	0.67
-7.5V	0.62	0.62	0.62	0.63
-5V	0.48	0.44	0.47	0.47
-2.5V	0.31	0.26	0.28	0.26
0V	0.19	0.18	0.18	0.15
2.5V	0.11	0.10	0.10	0.10
5V	0.077	0.087	0.065	0.074

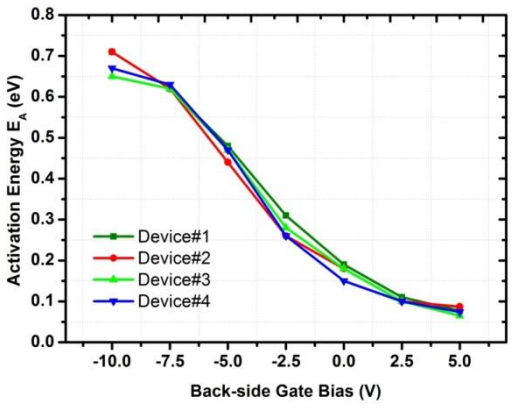


Figure 23. Plots of calculated activation energies for four devices. X-axis is backside bias.

Chapter 4

CONCLUSIONS AND FUTURE WORK

In this work, GaAs and InAs nanowire field effect transistors are built for electrical measurements. Both of those nanowires are grown through catalyst-free growth method, which is considered as 'pure' growth without unintentionally doped impurities possibly introduced by catalysts.

Lateral p-type GaAs nanowire FETs are fabricated. Electrical measurement results show very low current level of pA and large hysteresis which leads us to investigate surface passivation method for device improvement. Ammonium surfide solution is used for etching away native oxide layer on nanowire surface. With 20-30 minutes of such chemical treatment, largest current level increase is achieved.

Unintentionally doped InAs nanowires are fabricated into similar lateral FETs. Electrical measurements reveal n-type behavior of such devices. The highest field effect mobility extracted from devices is 1490 cm^2/Vs. From TEM images, dense stacking faults are observed along the wires, which can be a factor relating to device performance. Temperature dependent measurements lead us to investigate potential barriers. However, further measurements along this way are required for more information. This is one part of the future work.

Another part of the future work is to fabricate nanowire devices onto insulation substrates so that instead of applying DC signal to FETs, pulsed signals can be applied for better heat dissipation.

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