Measurement of Quadrature Transmitter Impairments Using BIST

By

Nitin Goyal

A Thesis Presented in Partial Fullfillment of the Requirements for the Degree Master of Science

Approved November 2011 by the Graduate Supervisory Committee

Sule Ozev, Chair Tolga Duman Bertan Bakkaloglu

ARIZONA STATE UNIVERSITY

December 2011

ABSTRACT

In this thesis, a Built-in Self Test (BiST) based testing solution is proposed to measure linear and non-linear impairments in the RF Transmitter path using analytical approach. Design issues and challenges with the impairments modeling and extraction in transmitter path are discussed. Transmitter is modeled for I/Q gain & phase mismatch, system non-linearity and DC offset using Matlab. BiST architecture includes a peak detector which includes a self mode mixer and 200 MHz filter. Self Mode mixing operation with filtering removes the high frequency signal contents and allows performing analysis on baseband frequency signals. Transmitter impairments were calculated using spectral analysis of output from the BiST circuitry using an analytical method. Matlab was used to simulate the system with known test impairments and impairment values from simulations were calculated based on system modeling in Mathematica. Simulated data is in good correlation with input test data along with very fast test time and high accuracy. The key contribution of the work is that, system impairments are extracted from transmitter response at baseband frequency using envelope detector hence eliminating the need of expensive high frequency ATE (Automated Test Equipments).

ii

TABLE OF CONTENT

		TAGE
LIST	OF TABLES	iv
LIST	OF FIGURES	v
CHA	PTER	
1	INTRODUCTION	6
2	BACKGROUND LITERATURE	9
3	ARCHITECUTRE AND MODELING	14
	3.1 Quadrature Transmitter Architecture	14
	3.2 Quadrature Transmitter Impairments	15
	3.3 Envelope Detector Architecture	17
	3.4 Mathematical System Model	
4	ANALYTICAL ANALYSIS	21
	4.1 Linear Parameter Extraction	22
	4.2 Non-Linear Parameter Extraction	25
5	RESULTS	29
6	CONCLUSION AND FUTURE WORK	34
REF	RENCES	35

LIST OF TABLES

TABLE	
1. RMS Error Calculations	

FIGURE PAG		
1. System Architecture 7		
2. BiST Based Methods 10		
3. Test Method for IQ Imbalance and Time Skew12		
4. Envelope Detector Used in [28]13		
5. I/Q Modulation Transmitter15		
6. Transmitter with Impairments and Envelope Detector16		
7. Output Frequency Spectrum for Low Power Input Signals 23		
8. Output Frequency Spectrum for High Power Input Signals26		
9. Gain Imbalance Extraction Error30		
10. Phase Imbalance Extraction Error		
11. Transmitter Path Gain Extraction Error		
12. IDC Extraction Error		
13. Qdc Extraction Error32		
14. IIP3 Extraction Error32		
15. IIP2 Extraction Error		

LIST OF FIGURES

Chapter 1

INTRODUCTION

Continuous CMOS scaling to improve performance along with systemon-chip (SoC) implementations are key factors for establishing a market share in the ever competitive consumer market. But both, SoC implementation and shrinking of devices add to stringent specification requirement due to high operating frequencies, and limit the availability of test point locations which won't impact the system performance. These challenges require having expensive automated test equipments (ATEs) which can add to significant HVM test cost and ultimately final product cost. To overcome these challenges significant work has already been done and continuously being done for alternative test methods. In order to reduce the reliance of expensive RF testers, one desirable test approach is to use built-in-self-test. BiST circuitry can be designed using existing design components or may require additional circuitry.

There are two classes of BiST methods. One set of approaches use the loop-back configuration to down-convert the high frequency transmitter output using the receiver on the same chip and conducts all the analysis in the baseband domain [14-21]. Another set of BiST approaches convert the RF signal to low-frequency equivalent using on-chip circuitry and analyze this low-frequency signal for test purpose [22-29].

6

Loop-back based BiST is advantageous since it does not require any additional circuitry. However, it requires the transmitter and receiver be active at the same time, and may suffer from leakage issues between the two paths. For some designs, it may be feasible. Thus, in some cases, it may be necessary to resort additional circuitry that can analyze the transmitter path using low-frequency outputs.

For BiST methods, transmitter pose a more difficult challenge since the output is in the RF domain and it requires converting a complex RF signal into low-frequency domain.

Several techniques have been proposed to enable the RF to lowfrequency conversion [22-29]. Peak or power detectors are simple in terms of implementation [26-29] and introduce very little overhead. Using these kinds of detectors it is possible to measure the amplitude (or power) of the signal based on sine-wave approximation. Thus, parameters, such as 1 dB compression point, gain and third order input intercept can be measured.

For Transmitter, however, it is essential that several other performance parameters, such as IQ imbalance, DC offsets and non-linearity coefficients of power amplifier, be measured. In order to measure these parameters, more information needs to be preserved in the signal. One alternative to enable preserving more information is to use the lowfrequency envelope of the RF signal for analysis. This kind of an envelope

7

detector would require more area and the higher complexity but it is one of the few choices available to enable the characterization of the parameters that are required for the testing the performance of the device.

In this thesis work, we use and envelope detector to convert the high frequency equivalent while preserving the necessary baseband information about important performance parameters. Target parameters in this work are Quadrature imbalances, such as gain and phase mismatch, DC offsets, 2nd and 3rd order non-linearity coefficients.





Figure 1 show the high level system architecture and analysis approach for the proposed method. First we derive the complete mathematical model of the transmitter output including transmitter impairments and response of the envelope detector. Second we design specialized test signal so as to decouple the effect of various impairments from one another. These test signals ensure that the amplitudes of various frequency components are correlated to the impairments that we wish to compute. In order to make these amplitude measurements, we use FFT on the low-frequency digitized signal. Digitization and signal processing can be done using already existing components in the system as most SOCs contain several house-keeping ADCs and several processing units. The next step is to correlate these measured amplitudes to the target parameters using the analytical relations and compute the target parameters using these expressions. As a result, this approach is computationally efficient and very fast compared to approaches that require non-linear solvers. Transmitter impairments such as I/Q gain and phase mismatch, DC offsets and non-linearity (IIP3 and IIP2) are successfully extracted through analytical analysis on the spectrum of envelope detector.

Next section of the thesis discusses the previous work done in much more detail and later sections include details of architecture, modeling simulations, results and future work opportunities.

Chapter 2

BACKGROUND LITERATURE

Continuous advancement in CMOS scaling and circuit integration techniques (SoC) are pushing RF devices to perform better and faster over previous generation and at the same time extremely competing consumer market is pushing manufacturer towards reducing cost. Both of these scenarios are creating exciting and new challenges in the testing area as described in [4], [5] and [6].

Authors in [4] describe the test cost, time and equipment limitations associated with different blocks of the SoC such as digital circuits, mixed signal circuits and memory. Main factors for higher manufacturing cost, which may reach 50% of the total production cost, include capital as well as infrastructure cost. Measures to reduce the manufacturing cost include reducing ATE capital and operational cost as well as increasing throughput per ATE. BiST based DFE address both of these measures by reducing test time as well as enabling measurement of complex circuitry using low cost testing solutions.

Several BiST based methods have been introduced to overcome test challenges related to RF devices [7]-[29]. Some BiST designs use the existing circuitry and some BiST include a external circuitry to perform specialized functions, such as generating baseband signals or creating digital signature based on the performance. BIST solutions can be included to test a particular circuit block, such as LNA [7] [8], a PA or entire transmitter chain [14-[21]. The proposed BIST based method in this study includes a BIST circuitry (envelope detector) and tests the entire transmitter chain.



Fig. 2. BiST Based Methods

To be able to better and easily understand the BiST based pervious work on similar RF Transceivers, they are divided into two parts (figure 2). First part of methods is based on RF sensors [22] –[29]. Second part of methods is based on Loop-Back based BiST [14] -[21].

A sensor based approach is presented in [22 23]. In this method, multiple sensors are placed in accessible test point of the transmitter. The responses from these sensors are fed into a non-linear mapping tool to obtain the target parameters. The authors also propose a sensor selection algorithm to select ideal sensor locations. The non-linear mapping is enabled through using Multivariate Adaptive Regression Splines (MARS). This model is extracted using training samples that are representative of the entire population of devices. The target parameters in this work are gain and IIP3 of the LNA and the mixer. IQ imbalances are not targeted in this work.

In [24 25], the authors propose a power detector based sensor method to predict the Gain, NF and P1dB of a variable gain amplifier. In this method, two power detectors were added at the input and output of the amplifier and from the output response of the both detectors specification of the amplifier were estimated.

Authors in [14] propose a loopback BiST based method to predict the Gain and IIP3 of the Transceiver. In this method, a specified bit stream is applied at the input of the transmitter and output of the transmitter is looped back into the receiver. The output of the response is analyzed using FFT and a MARS non-linear regression model is used to map the information in the spectrum to the target parameters of IIP3 and Gain of the transmitter and receiver.

In [15], a loopback based method is presented to estimate gain/phase imbalance, dc offsets, time skew and IIP3 of the transmitter and the receiver path. A specified baseband signal is used as the test point at the input of the transmitter and output response from transmitter is looped back into the receiver input and system impairments are estimated through using NLS method on the output of the receiver, as show in Figure (3).



Fig. 3. Test Method for I/Q Imbalance and Time Skew ([15]) In [18], the authors present a loopback based BiST method to measure SNR of the transceiver through signature analysis at the output of the receiver.

Envelope detector based BiST methods are described in [26]-[29]. These methods have gained a lot of attention due their characteristic of preserving information during down conversion of signals from high frequency domain to low frequency domain. In [26], RF transmitter gain and IIP3 are calculated using envelope detector. Transmitter is excited using a two-tone stimulus and spectrum signature is obtained at the output of the transmitter using an envelope detector. Signature from envelope detector is compared against pre-defined acceptable ranges, to enable a go/no-go decision. In [28], the authors use an envelope detector based approach to estimate system Gain and IIP3. The system is excited with a two-tone amplitude modulated test signals and the output response from the envelope detector is compared against the MARS prediction model built using wavelet coefficients from Monte Carlo simulation. Envelope Detector used in [28] is shown in figure below.



Fig. 4. Diode based Envelope Detector Used in [28]

From above discussion it is clear that most of the previous work focus on measuring gain, IIP3 and NF of the RF devices. However, I/Q imbalance and DC offsets are important parameters for proper functionality of Transceivers and hence needs to be characterized.

Chapter 3

ARCHITECUTRE AND MODELING

Analytical approaches generally require working with very complex mathematical equations. Designing test signals in a way to reduce this complexity is essential to enable such analytical approaches. In this work, we aim at separating out various components of the system response in the frequency domain by using a carefully crafted multi-tone signal at the I and Q inputs. To remove the requirement of having expensive equipments, down-conversion of high frequency system output was also need. For that purpose, we use a Self-mixing envelope detector which preserves the information on the impairments during this down-conversion process.

3.1 QUADRATURE TRANSMITTER ARCHITECTURE

In I/Q modulation scheme I and Q signals are modulated using a sine and a cosine signal at the same frequency, which are orthogonal. Thus two uncorrelated bit streams can be modulated at the same time without increasing the bandwidth requirement. However, to ensure proper operation, orthogonality is essential.



Fig. 5. I/Q Modulation Transmitter

A low cost I/Q modulating transmitter with block diagram is depicted in figure 5. Transmitter signals are processed digitally and converted to analog for transmission and receivers at the other end receives the analog signals and convert/process the signals digitally. A local oscillator and 90° phase shifter adds orthogonality for I and Q channels and converts I and Q signals to carrier frequency from baseband frequencies. Signals are amplified using a power amplifier (PA) before transmission.

3.2 QUADRATURE TRANSMITTER IMPAIRMENTS

Orthogonality between I and Q channels preserves the information, however, this also makes the transmitter sensitive to mismatches between I and Q arms. Orthogonality requires that the two arms present with the same signal gain and there is exactly 90 degree difference in phase (one carrier being sine and one carrier being the cosine). Any deviation from this ideal point will cause leakage from I to Q and vice versa. This leakage acts as noise and degrades the transmission quality. Thus IQ imbalances are important parameters for the transmitters. Similarly, DC offsets generate carrier leakage, which can be problematic in some systems, particularly if DC frequency carries information. For more complex schemes, such as WLAN, this is less of a problem. Nonetheless, DC offsets may saturate the receiver path. Thus they need to be characterized for the transmitter. In addition to these parameters, the non-linearity of the power amplifier needs to be characterized since it both degrades modulation quality and results in spectral growth into other bands/channels.

In order to accurately account for the impairments in transmitter path, mathematical model needs to be developed for impairment effects. Impairments are inserted as gray shaded blocks in figure 6.



Fig. 6. Transmitter with impairments and Envelope Detector Error due to phase mismatch can be modeled as additional phase shift in Quadrature carrier signal of local oscillator. Therefore, LO signals are initially modeled as $cos(wc^*t)$ and $sin(wc^*t+\phi)$ for the transmitter I and Q channels respectively.

Error due to gain mismatch can be modeled as amplification due to gain error. Q channel signal is amplified with (1+gtx) where gtx is gain mismatch.

DC offsets are modeled as separate DC value for I and Q channels. Idc is DC level for I channel and Qdc is DC level for Q channel and difference between Idc and Qdc is the DC offset for the transmitter.

Non-linearity of the transmitter path is modeled as second and third order polynomial gain function covering for the power amplifier. Extracting parameters for individual component is extremely difficult due to too many non-linear gain function coefficients. However, impairments can be extracted for overall transmitter path using analytical approach as described in this thesis.

3.3 ENVELOPE DETECTOR ARCHITECUTRE

The envelope detector used in thesis is comprised of a self mixer and a 200MHz filter as shown in the BiST part of figure 6. Self mixing operation eliminates the need of having a local oscillator to down convert the high frequency transmitter output signal. Self mixing operation generates signals at DC, baseband frequency range and at carrier frequency range. The filter removes the high frequency components and keeps only DC and baseband frequency components for spectral analysis. From spectral analysis of envelope detector outputs, frequency bins in spectrum are multiple of baseband frequencies so it is important to choose baseband frequencies in such a way that frequency bins don't overlap each other to ensure success of the analytic approach described.

3.4 MATHEMATICAL SYSTEM MODEL

Selection of baseband input signals was one of most important criteria to ensure success of the described analytical approach. Sine waves were selected for the input stimulus to the model because performing mathematical analysis is much easier on sine waves compare to other forms to signals. Frequencies for I and Q path were selected such that multiples of baseband frequencies won't overlap after self-mixing operation of envelope detector. For example multiples and combination of frequencies w1 and w2 in equations (1) and (2) such as 2*w1, 2*w2, w1+w2, 2*w1+w2 etc should not be equal to each other.

$$I = A * Cos(w1 * t) + Idc \tag{1}$$

$$Q = A. Cos(w2 * t) + Qdc$$
⁽²⁾

I and Q from equations (1) and (2) are the baseband signals with different baseband frequencies but same signal amplitude. Both I and Q have DC values Idc & Qdc associated with them respectively. Difference between the Idc and Qdc is the DC offset impairment for the transmitter path.

Baseband I and Q signals are up converted to carrier frequency using local oscillator LO and a mixer. Since different mixer components are used for both I and Q channels, gain mismatch due to different mixer components will be introduced which is described as 'gtx' in equation (4). To achieve the orthogonality between I and Q signals a 90 degree phase shifter is included. Due to imperfect nature of components and an imperfect phase shift needs to be modeled also.

$$I1 = I * Cos(wc * t) \tag{3}$$

$$Q1 = Q * Sin(wc * t + \emptyset) * (1 + gtx)$$

$$\tag{4}$$

Equations (3) and (4) are the output after the mixing operation of the transmitter. 'phi' and 'gtx' in equation (4) are the phase and gain imbalance of the Quadrature transmitter.

Addition of I1 and Q1 is the input to the power amplifier.

$$PA_{Input} = I1 + Q1 \tag{5}$$

$$PA_{output} = a1 * PA_{input} + a2 * (PA_{input})^{2} + a3 * (PA_{input})^{3}$$
 (6)

Equation (6) describes the output of the power amplifier. Where a1 is gain of the PA and a2 and a3 are second and third order non-linear coefficient

respectively. Gain of the individual components in transmitter path and in envelope detector cannot be extracted separately because linear addition so a1 is considered as overall system gain. PA_{output} from equation (6) is the output from Transmitter amplifier. This signal is routed to Peak Detector circuit.

$$SelfMix_{output} = PA_{Output} * PA_{Output}$$
(7)

$$SelfMix_{output} = (a1 * x + a2 * x^{2} + a3 * x^{3})^{2}$$
(8)

Equations (7) and (8) describe the first stage self-mode mixing operation of the envelope detector. Second stage of envelope detector removes the frequency component above 200MHz. Spectral analysis will be performed on the filtered version of the $SelfMix_{output}$ signal.

Chapter 4

ANALYTICAL ANALYSIS

Proposed BiST is composed of 2 sets of tests. First set of test is performed at low power signal inputs. This ensures that the non-linear behavior of the power amplifier is not excited. Thus the system can be modeled with a linear behavior model of the individual block. I/Q gain/phase mismatch and DC offset can be computed using analytical expression obtained from the system behavior. Second set of test is performed at high power signal inputs. This ensures that the non-linearity of the PA is excited which also would require us to use a non-linear model for the power amplifier. This non-linearity will make the system equations complex. However, in this step, some of the impairments can be treated as known since they already have been measured. Non-linearities of the PA, IIP2 and IIP3 can be extracted through performing analytical analysis on the output based on high power input signals.

$$\mathbf{x} = PA_{input} \tag{9}$$

$$SelfMix_{output} = a1^{2} * x^{2} + 2a1a2 * x^{3} + (2a1a3 + a2^{2}) * x^{4} + 2a2a3 * x^{5} + a3^{2} * x^{6}$$
(10)

Equation (9) and (10) shows the expansion the equations after selfmixing operation. 'x' in equation (10) is PA_{input} from equation (5).

4.1 LINEAR PARAMETER EXTRACTION

Overall system response will include the non-linear errors but if the input signal is small enough then the non-linear terms will be suppressed and system can be analyzed as linear system. From equation (10) all the terms expect for $a1^2 * x^2$ have non-linear terms so only $a1^2 * x^2$ can be used to extract linear parameters such as gain/phase mismatch, DC offset and overall system gain and other parameters can be ignored for now assuming they have negligible impact. Filtering $a1^2 * x^2$ signal with 200MHz signal, following parameters remain.

$$a1^2 * x^2 =$$

$$Aa1^{2}IdcCos[tw1] + \frac{1}{4}A^{2}a1^{2}Cos[2tw1] + Aa1^{2}gtx^{2}QdcCos[tw2] + \frac{1}{4}A^{2}a1^{2}gtx^{2}Cos[2tw2] + \frac{1}{2}Aa1^{2}gtxQdcSin[phi - tw1] + \frac{1}{2}Aa1^{2}gtxQdcSin[phi + tw1] + \frac{1}{2}Aa1^{2}gtxIdcSin[phi - tw2] + \frac{1}{4}A^{2}a1^{2}gtxSin[phi - tw1 - tw2] + \frac{1}{4}A^{2}a1^{2}gtxSin[phi + tw1 - tw2] + \frac{1}{4}A^{2}a1^{2}gtxIdcSin[phi - tw1 + tw2] + \frac{1}{4}A^{2}a1^{2}gtxSin[phi + tw1 + tw1] + \frac{1}{4}A^{2}a1^{2}gtxSin[phi + tw1 + tw1] + \frac{1}{4}A^{$$

From Equation (11), it is clear that we need to have separate frequency bins for different terms otherwise it will be difficult to differentiate magnitude contributor from each other. We can calculate different parameters by measuring the magnitude from frequency (11).



Fig 7. Output Frequency Spectrum of Low Power Input signals

Figure 7 shows the frequency spectrum of the transmitter signals based on low power input signals with baseband frequency for I at 2MHz and for Q at 2.5MHz. From spectrum in Figure 4 frequency peaks at w1 (2MHz), w2 (2.5MHz) and 2*w2 (5MHz), 2*w1 (4MHz) are clearly visible. From equation (10), at frequency point 2*w1 the only unknown parameter is a1 so measuring the magnitude from frequency spectrum (figure 4) and using term for 2*w1, we can calculate the value for a1 or overall system gain.

Magnitude from FFT spectrum (fig.7) at $2^*w1 = \frac{1}{4} * A^2 * a1^2$

So,
$$a1 = \sqrt{mag_{at\ 2*w1} * \frac{4}{A^2}}$$
(12)

Analyzing Equation (10) since we know value of a1 from calculation from equation (12), we can calculate the value of gtx using term at frequency '2*w2' and measuring magnitude from FFT spectrum (figure 7) at the same frequency.

Magnitude from FFT spectrum at $2^*w^2 = \frac{1}{4} * A^2 * a1^2 * gtx^2$

So,
$$gtx = \sqrt{\frac{mag_{at\ 2*w2}*4}{A^2*a1^2}}$$
 (13)

Since the value of 'a1' and 'gtx' is now known, looking back at equation (11) we can calculate the value of phi from frequency 'w1+w2' because phi is the only unknown parameter in that frequency bin.

Magnitude from FFT spectrum at w1+w2 = $\frac{1}{2} * A^2 * a1^2 * gtx * \sin(\emptyset)$

$$So,\phi = asin \left(2 * \frac{mag_{at w1+w2}}{A^2 * a1^2 * gtx}\right)$$
(14)

Now only remaining linear terms to be calculated are DC offset for I and Q channels, Idc and Qdc. Analyzing equation (11), we don't see any individual frequency bin that contains only Idc or Qdc terms. However, terms at frequency points 'w1' and 'w2' both contains Idc and Qdc and all other parameters are known at those frequency point so we can calculate Idc and Qdc algebraic 2 equations and 2 unknowns method.

Magnitude at frequency point w1 = x3(15)Magnitude at frequency point w2 = y3(16)
$$Qdc = (x3*y1-y3*x1)/(x2*y1-y2*x1);$$
(17) $Idc = (x3-x2*Qdc)/x1;$ (18) $x1 = A*a1^2;$ (19) $x2 = A*a1^2*(1+gtx)*sin(\phi);$ (20) $y1 = A*a1^2*(1+gtx)*sin(\phi);$ (21)

$$y^2 = A^*a^{1/2}(1+gtx)^2;$$
 (22)

Measuring the magnitudes at frequency point w1 and w2 from figure 4 and using equation from (15) through (20), DC offset parameters ldc and Qdc can be calculated.

4.2 NON-LINEAR PARAMETER EXTRACTION

Once linear parameters are calculated, system is excited with high power input signals so that non-linear parameters can have significant impact on system output. Equation based model for the non-linear system is very complex, but since all the linear parameters have already been calculated, non-linear parameters can be calculated with some careful observations.



Fig 8. Output Frequency Spectrum for High Power Input Signals
Figure 8 shows the frequency spectrum of the high power signals.
Comparing figure 4 and figure 5, impact of adding non-linearities is clearly
visible. Many frequency bins including 2*w1, 2*w2, w1+w2, 4*w1,
2*w1+2*w2 are dominant.

Expanding equation (10) for both linear and non-linear terms and removing the high frequency terms (filter operation), no single frequency point was available which could be used to calculate either a2 or a3 so again 2 equation/ 2 unknown approach was required to calculate values of non-linearities. Frequency point 'w1+w2' and '2*w1+2*w2' were selected to calculate values for a2 and a3 using 2 equation/ 2 unknown approach. These frequencies were selected because of clearly visible magnitude points in figure 8 and less terms needed to be analyzed after expanding equation (10). Other frequency bins can also be used.

$$\begin{split} \text{Magnitude at frequency location 'w1+w1' = 3A^2a4gtx^2 \text{IDcQDcCos}[tw1 + tw2] - \frac{3}{4}A^2a4gtx^2 \text{IDcQDcCos}[2phi + tw1 + tw2] + \frac{9}{32}A^4a4gtx\text{Sin}[phi + tw1 + tw2] + \frac{9}{8}A^2a4gtx\text{Sin}[phi - tw1 + tw2] + \frac{9}{8}A^2a4gtx\text{Sin}[phi + tw1 + tw2] + \frac{1}{4}A^2a1^2gtx\text{Sin}[phi + tw1 + tw2] + \frac{1}{4}A^2a1^2gtx\text{Sin}[phi - tw1 - tw2] + \frac{1}{4}A^2a1^2gtx\text{Sin}[phi + tw1 + tw2] + \frac{135}{16}A^4a3^2gtx^4\text{IDcQDcCos}[tw1 + tw2] + \frac{135}{16}A^4a3^2gtx^4\text{IDcQDcCos}[tw1 + tw2] + \frac{45}{16}A^4a3^2gtx^2\text{IDcQDcCos}[tw1 + tw2] + \frac{45}{4}A^2a3^2gtx^4\text{IDcQDcCos}[tw1 + tw2] + \frac{45}{16}A^4a3^2gtx^2\text{IDcQDcCos}[2phi + tw1 + tw2] - \frac{45}{16}A^4a3^2gtx^2\text{IDcQDcCos}[2phi + tw1 + tw2] - \frac{15}{16}A^4a3^2gtx^2\text{IDcQDcCos}[2phi + tw1 + tw2] - \frac{15}{16}A^2a3^2gtx^2\text{IDcQDcCos}[2phi + tw1 + tw2] - \frac{15}{256}A^6a3^2gtx^2\text{Sin}[phi + tw1 + tw2] + \frac{405}{512}A^6a3^2gtx^3\text{Sin}[phi + tw1 + tw2] + \frac{75}{256}A^6a3^2gtx^3\text{Sin}[phi + tw1 + tw2] + \frac{225}{64}A^4a3^2gtx^3\text{IDc}^2\text{Sin}[phi + tw1 + tw2] + \frac{405}{64}A^4a3^2gtx^3\text{IDc}^2\text{Sin}[phi + tw1 + tw2] + \frac{75}{64}A^4a3^2gtx^3\text{IDc}^2\text{Sin}[phi + tw1 + tw2] - \frac$$

$$\frac{45}{128}A^{4}a3^{2}gtx^{3}QDc^{2}Sin[3phi + tw1 + tw2] - \frac{45}{32}A^{2}a3^{2}gtx^{3}IDc^{2}QDc^{2}Sin[3phi + tw1 + tw2]$$
(21)

$$a4 = 2a1^*a3 + a2^2$$
 (22)

Magnitude at frequency location '2*w1+2*w2' = $\frac{3}{16}A^4 a4gtx^2 Cos[2tw1 + 2tw2] - \frac{3}{64}A^4 a4gtx^2 Cos[2phi + 2tw1 + 2tw2] + \frac{9}{16}A^3 a4gtx1DcSin[phi + 2tw1 + tw2] - \frac{15}{128}A^6 a3^2 gtx^2 Cos[2phi - 2tw1 - 2tw2] - \frac{15}{128}A^6 a3^2 gtx^4 Cos[2phi - 2tw1 - 2tw2] - +\frac{405}{128}A^4 a3^2 gtx^3 IDcQDcSin[phi + 2tw1 + 2tw2] - \frac{45}{128}A^4 a3^2 gtx^3 IDcQDcSin[3phi + 2tw1 + 2tw2] - \frac{45}{64}A^4 a3^2 gtx^2 IDc^2 Cos[2phi - 2tw1 - 2tw2] - \frac{45}{64}A^4 a3^2 gtx^4 QDc^2 Cos[2phi - 2tw1 - 2tw2]$ (23)

Calculating magnitudes from frequency spectrum and solving for equations (21) (22) & (23), non-linear parameter a2 and a3 can be calculated. Careful observation needed to ensure that no other terms overlap in the same frequency bins. At frequency point w1+w2; there were additional terms that did not include non-linear parameters a2 or a3 so magnitude from this term needed to be subtracted to ensure accurate calculation can be made.

Chapter 5

RESULTS

Matlab based model was generated for the transmitter path shown in figure3. Monte Carlo simulations were performed ensure model is stable and results are consistent across wide range of input parameters. In each Monte Carlo simulation iteration, random values for all impairments were selected. System was modeled after the WiMax standard which has the bandwidth of 10MHz so 2 MHz and 2.5MHz of input signals were chosen for I and Q path to ensure that signals fall within the specified bandwidth but still enough apart to not overlap frequency bins. 2.5GHz of local oscillator was used for up-conversion of signals. RMS errors based on 500 iteration of Monte Carlo simulation are shown in Table 1. Results show that RMS errors are negligible for device operation. Table 1 also includes the comparison results based on [15] and [28].

Table 1

Input	Parameter	RMS	Results	Results
Parameter	Range	Error	[15]	[28]
a1	5-0.1	0.46%	n/a	3.4%
a2	10-50	1.20%	n/a	n/a
a3	20-100	0.28%	1.7%	6.7%
gtx	± 20%	1.5%	3.8%	n/a
phi	1-5	0.24°	0.21°	n/a
ldc	1mV-20mV	0.4 mV	5.66 mV	n/a
Qdc	1mV-20mV	0.15 mV	6.33 mV	n/a

RMS Error Calculations for Impairments



Fig. 9. Gain Imbalance Extraction Error



Fig. 10. Phase Imbalance Extraction Error



Fig. 11. Transmitter Path Gain Extraction Error







Fig. 13. Qdc Extraction Error



Fig. 15. IIP2 Extraction Error

Figure 9 through 15 shows the error estimation results for all the impairments calculated through all 500 Monte Carlo Simulation Trials.

Chapter 6

CONCLUSION AND FUTURE WORK

This Thesis presents a new BiST based method for measuring Transmitter impairments using Analytical approach. Test Response spectrum using envelope detector was used to calculate values for impairments. A realistic system model with gain/phase mismatch, overall system non-linearity and DC offset was derived. Values extracted through simulation are in good correlation with the test input values. Low complexity, high accuracy and fast test time are the key highlights of the proposed BiST method.

Future work will require verifying the proposed method through measurements to ensure practical implementation of the BiST and also time skew also needs to be characterized along with window impact.

REFRENCES

- [1] B. Razavi, "RF Microelectronics," Prentice Hall, NJ 1998.
- [2] Thomas H. Lee, "The Design of CMOS Radio-Frequency Integrated Circuits," Cambridge University Press, second edition.
- [3] J. Proakis, M. Salehi, "Communication Systems Engineering," Prentice Hall, second edition.
- [4] F. Poehl, F. Demmerle, J. Alt, H. Obermeir, "Production Test Challenges for Highly Integrated Mobile Phone SOCs- A Case Study" in 15th IEEE European Test Symposium, May 2010.
- [5] Frank Demmerle, "Integrated RF-CMOS Transcievers Challenge RF Test" in IEEE International test conference, Oct 2006.
- [6] Chatterjee, A. Keshavarzi, A. Patra, S. Mukhopadhyay, "Tutorial: Test Methodologies in the Deep Submicron Era –Analog, Mixed-Signal and RF," Proc. International Conf. on VLSI Design, Embedded Systems Design, 2005.
- [7] Gopalan, T. Das, C Washburn, P.R. Mukund, "An Ultra-Fast, On-Chip BiST for RF Low Noise Amplifier," International Conf. VLSI Design, IEEE, 2005
- [8] K. Jayaraman, Q. A. Khan, P. Chiang, Baoyong Chi, "Design and Analysis of 1-60GHz, RF CMOS Peak Detectors for LNA Calibration," Automation and Test, VLSI Design, IEEE, 2009
- [9] D. Han, S. Akbay, S. Bhattacharya, A. Chatterjee, W. Eisenstadt, "On-chip Self-Calibration of RF Circuits Using Specification-Driven Built-In Self Test (S-BIST)," On-Line Testing Symposium, IEEE, 2005
- [10] B. R. Veillette, G. W. Roberts, "A built-in self-test strategy for wireless communication systems," Proc. Int'l Test Conf., 1995
- [11] Robert Staszewski, Imran Bashir, Oren Eliezer, "RF Built-in Self Test of a Wireless Transmitter," Circuit and Systems, IEEE, 2007
- [12] Yaning Zou, C. Munker, R. Stuhlberger, M Valkama, "Calibration and Self-Test of RF Transceivers," Circuits and Systems, IEEE, 2010

- [13] Jee-Youl Ryu, B.C. Kim, I. Sylla, "A New Low-Cost RF Built-In Self-Test Measurement for System-on-Chip Transceivers" in IEEE instrumentation and measurement, April 2006.
- [14] Halder, S. Bhattacharya, G. Srinivasan, A. Chatterjee " A Systemlevel Alternate Test Approach for Specification Test of RF Transceivers in Loopback Mode" in IEEE Embedded System Design, 2005.
- [15] Erdem S Erdogan, Sule Ozev "Detailed Characterization of Transceiver Parameters Through Loop-Back Based BiST" in IEEE VLSI Vol 18, June 2010.
- [16] E. S. Erdogan, Sule Ozev, "Single-Measurement Diagnostic Test Method for Parametric Faults of I/Q Modulating RF Transceivers," in Proc. 26th VLSI Test Symp., May 2008.
- [17] Marvin Onabajo, Jose Silva-Martinez, Felix Fernandez, Edgar Sanchez-Sinencio " An On-Chip Loopback Block for RF Transceiver Built-In Test" in IEEE Circuits and Systems Vol 56, June 2009.
- [18] D. Lupea, Udo Pursche, H. Jentschel "RF-BIST: Loopback Spectral Signature Analysis" Proceedings of Design, Automation and Test in Europe Conference and Exhibition.
- [19] J. Dabrowski, "Loopback BiST for RF Front-Ends in Digital Transceivers," System-on-chip, IEEE, 2003
- [20] J. Dabrowski, J. Bayon, "Mixed loopback BiST for RF Digital Transceivers," Defects and Fault Tolerances in VLSI Systems, IEEE, 2004
- [21] M. Onabajo, J. Silva-Martinez, F. Fernandez, E. Sanchez-Sinencio, "An On-Chip Loopback Block for RF Transceiver Built-In Test," Circuit and Systems, IEEE, 2009
- [22] S. Bhattacharya, A. Chatterjee, "Use of Embedded Sensors for Built-in-Test RF Circuits" in proceedings ITC 2004.
- [23] S. Bhattacharya, A. Chatterjee, "A Built-in Loopback Test Methodology for RF Transceiver Circuits using Embedded Sensor Circuits" in 13th Asian Test Symposium, 2004.
- [24] H. Hsieh, L. Lu, "Integrated CMOS Power Sensors for RF BIST Applications" in 24th IEEE VLSI Test Symposium, May 2006.

- [25] Y. Huang, H. Hsieh, L. Lu, "A Low-Noise Amplifier with Integrated Current and Power Sensors for RF BIST Applications," VLSI Test Symposium, IEEE, 2007
- [26] M.J. Barragan, R Firoelli, D Vazquez, A Rueda, J.L. Huertas, "Low-Cost Signature Test of RF Blocks Based on Envelope Response Analysis" in IEEE European Test Symposium, 2010.
- [27] K. Yanagisawa, N. Matsuno, T. Maeda, S. Tanaka, "A New DC-Offset and I/Q-Mismatch Compensation Technique for a CMOS Direct-Conversion WLAN Transmitter" in IEEE Microwave Symposium, June 2007.
- [28] D. Han, A. Chatterjee, "Robust Built-in Test of RF ICs Using Envelope Detectors" in 4th Asian Test Symposium, December 2005.
- [29] M. Barragan, R. Firoelli, D. Vazquez, A. Rueda, J. Huertas, "Low-Cost Signature Test of RF Blocks Based on Envelope Response Analysis" in 15th IEEE European Test Symposium, May 2010.