Mixed Signal Design in Thin Film Transistors

by

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Doctor of Philosophy

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ABSTRACT

Thin film transistors (TFTs) are being used in a wide variety of applications such as image sensors, radiation detectors, as well as for use in liquid crystal displays. However, there is a conspicuous absence of interface electronics for bridging the gap between the flexible sensors and digitized displays. Hence is the need to build the same.

In this thesis, the feasibility of building mixed analog circuits in TFTs are explored and demonstrated. A flexible CMOS op-amp is demonstrated using a-Si:H and pentacene TFTs. The achieved performance is ≈ 50 dB of DC open loop gain with unity gain frequency (UGF) of 7 kHz. The op-amp is built on the popular 2 stage topology with the 2nd stage being cascoded to provide sufficient gain. A novel biasing circuit is successfully developed modifying the g_m biasing circuit to retard the performance degradation as the TFTs aged.

A switched capacitor 7 bit DAC is developed in only nMOS topology using a-Si:H TFTs, based on charge sharing concept. The DAC achieved a maximum differential non-linearity (DNL) of 0.6 least significant bit (*LSB*), while the maximum integral non-linearity (INL) was 1 *LSB*. TFTs were used as switches in this architecture; as a result the performance was quite unchanged even as the TFTs degraded. A 5 bit fully flash ADC is also designed using all nMOS a-Si:H TFTs. Gray coding was implemented at the output to avoid errors due to comparator meta-stability. Finally a 5 bit current steering DAC is also built using all nMOS a-Si:H TFTs. However, due to process variation, the DNL was increased to 1.2 while the INL was about 1.8 *LSB.*

Measurements are made on the external stress effects on zinc indium oxide (ZIO) TFTs. Electrically induced stresses are studied applying DC bias on the gate and drain. These stresses shifted the device characteristics like threshold voltage and mobility. The TFTs are then mechanically stressed by stretching them across cylindrical structures of various radii. Both the subthreshold swing and mobility underwent significant changes when the stress was tensile while the change was minor under compressive stress, applied parallel to channel length.

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Finally, I would like to thank ASU's Flexible Display Center and Army Research Laboratory for underwriting my project and providing their fabrication facility to design my circuits.

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ABBREVIATIONS

a-Si:H	Amorphous Silicon Hydride
ADC	Analog to Digital Converter
AC	Alternating Current
BSIM	Berkeley Short Channel IGFET Model
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DAC	Digital to Analog Converter
DNL	Differential Non-Linearity
FPGA	Field Programmable Gate Array
IC	Integrated Circuit
INL	Integrated Non-Linearity
IGZO	Indium Gallium Zinc Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
Mo	Molybdenum
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
N	Nitrogen
OLED	Organic Light Emitting Diode
OSR	Over Sampling Ratio
OTFT	Organic TFT

PEN	Polyethylene Napthalate
PECVD	Plasma Enhanced Chemical Vapor Deposition
SiO_2	Silicon Dioxide
SAR	Successive Approximation Register
SFDR	Spurious Free Dynamic Range
SiN_x	Silicon Nitride
SPICE	Simulation Program with Integrated Circuit Emphasis
TFT	Thin Film Transistor
UGF	Unity Gain Frequency
VLSI	Very Large Scale Integration
ZIO	Zinc Indium Oxide

LIST OF SYMBOLS

A	Ampere
C_M	Miller capacitance
C_{dg}	Drain to Gate Capacitance
C_{sg}	Source to Gate Capacitance
C_{ox}	Gate Oxide Capacitance per unit area
E	Electric field
g_{ds}	Conductance
g_m	Transconductance
I_{DS}	Drain to Source Current
I_{off}	Off state Current
I_{on}	On state Current
k	Boltzman Constant
L	TFT Channel Length
ln	Natural Logarithm
n_i	Intrinsic Carrier Concentration
nm	Nano meter
nV	Nano Volt
poly	Poly Silicon
q	Electronic Charge
Q_i	Inversion Charge per Unit Area
S	Subthreshold Swing

T	Absolute temperature in Kelvin
t_{si}	Silicon Film Thickness
t_{ox}	Oxide thickness
V	Volt
V_{DS}	Drain to Source Voltage
V_{GS}	Gate to Source Voltage
V_{th}	Threshold Voltage
V_t	Thermal voltage
Y	Young's Modulus

Greek Symbols

ε_{si}	Permittivity of silicon
ε_{ox}	Permittivity of SiO_2
ε	Strain
μ_0	Low Field Mobility
μ_{eff}	Effective Mobility Dependent Channel Charge
	Trapping
μm	Micrometer

Chapter 1
INTRODUCTION

1.1 Background

TFT technology has become quite mature for producing large displays on flexible substrates, to make them rugged, lightweight and roll able. Applications of these displays range from displays and sensors for military applications to commercial portable displays. The main substrate used is polyethylene napthalate (PEN) which is flexible, light weight but has to be processed at low temperatures of 200° C. As a result conventional silicon with a processing temperature of close to 1000° C cannot be used for the purposes. Hence hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) have been developed for this special purpose. These devices can have low processing temperatures of less than 200° C and hence are compatible with PEN. Although there has been a steady rise in a-Si:H technology, organic TFTs developed on pentacene is another device that is gaining popularity with displays, especially OLEDs. Recently the stability and device performance of some of the mixed oxide TFTs are being investigated for large area sensor applications like X-ray detector, neutron detector, *e.t.c.* However there is a conspicuous absence of interface electronics that connects the analog signals from the sensors to digitized displays. This is the main objective of the thesis.

1.2 Motivation

A-Si:H TFTs are being used in a wide variety of applications such as image sensors, radiation detectors and large area electronic printing in addition to their conventional use in flexible displays. This flexibility, in turn, opens up a new

technology area which can be used in variety of low cost applications like e-paper, automotive displays, smart cards and foldable maps. The Flexible Display Center (FDC) at ASU is one center of its kind, determined to bring these flexible electronics to the small volume manufacturing stage.

Recently there has been a surge of activities on building conformable and portable large area sensors, both for military and commercial applications. Moreover the improved stability and performance of mixed oxide TFTs have promised new applications in large area sensors. However, analog to digital converters (ADCs) and digital to analog converters (DACs) are required to digitize the analog sensor signals for display systems. While commercial silicon based data converters can be used, these would be prohibitively costly for the above targeted applications. Hence is the current effort in exploring the feasibility of building these data converters in TFTs and analyzing their performance and limitations on different material system combination.

At the heart of most data converters is a high gain operational amplifier (henceforth referred to as op-amp). The op-amp is characterized by not only its open loop DC gain, but also its frequency response which in turn determines the response speed and settling time. Unfortunately, the TFTs have extremely low mobility, which results in low transconductance (g_m), leading to low DC gain and unity gain frequency (UGF). To get significant performance increasing the sizes of the individual component transistors enormously becomes neccessary, which results in huge area as well as parasitic capacitances, rendering almost no improvements. Moreover these TFTs are unstable and tend to degrade with

electrical stress. This implies that with continuous use the performance of the op-amp will degrade and eventually stop working. The above drawbacks have thwarted the development of analog circuitry in TFTs. Fortunately for large area flexible sensor applications high speed op-amps are not required.

Similar to op-amps, data converter circuits like ADCs and DACs also face similar difficulty in being implemented in TFTs. Moreover the TFT process being a relatively new one, is prone to large variations. These variations cause mismatches between critical circuit parts, ultimately leading to loss in resolution. Since speed is not critical in these applications alternative architectures are sought for which might be able to circumvent the problem of TFT degradation.

In light of the sluggish response and instability of a-Si:H and pentacene TFTs, some of the mixed oxide TFTs fabricated at FDC have also been studied in the past. However for complete operation of these devices in analog and digital circuits, electrical, mechanical and thermal stress testing needs to be executed. Electrical stress helps to ascertain how the circuits will degrade with time and usage. Mechanical stress helps to determine how these devices will behave when stretched or folded. And finally thermal stress is necessary to determine the performance and stability when used under extreme environment. Finally, as for a-Si:H TFTs, it needs to be determined if post fabrication annealing would actually improve the device properties.

1.3 Objectives and Scope

In view of the above discussion, the main objectives of the present work can be summarized as

1) to demonstrate the feasibility of building a CMOS TFT op-amp with a sufficient gain as well as reasonable frequency response. Also to simulate different op-amp topology for the best performance. Develop novel biasing circuitry for op-amps to retard the performance degradation even as the TFTs degrade.

2) to design and develop ADCs on TFTs with sufficient resolution and speed to be used as interface electronics in large area sensor applications.

3) to design and develop DACs on TFTs with sufficient resolution and speed to be used as interface electronics in large area sensor applications.

4) to test the performance stability of the newer mixed oxide TFTs in presence of electrical, mechanical and electromechanical stress and investigate how the device characteristics critical to analog and logic design change with these changes.

1.4 Organization of the Thesis

The present dissertation is divided into eight chapters the contents of which are outlined below

Chapter 2 starts with a discussion on the present TFT technology being used for state of the art display technology. This is followed by summary of logic circuits on TFTs. A brief introduction on op-amp design in TFTs is discussed next. A brief survey of the published work on the diverse efforts on building analog and mixed analog circuits on various TFTs including a-Si:H and organic TFTs is then presented. Finally, various stress experiments done on some of the newer mixed oxide TFTs are discussed.

Chapter 3 discusses the various TFT structures with their individual performance and limitations. In the first half a-Si:H and pentacene TFTs are covered along with their stress data while the second half discusses some of the mixed oxide TFTs developed at FDC.

Chapter 4 presents the effect of external stress, both electrical and mechanical, on the newly developed mixed oxide TFTs. Device characteristics like threshold voltage, subthreshold swing and mobility are measured and changes in these properties are analyzed to find the dominant mechanism of degradation in these TFTs

Chapter 5 focuses on the current effort on building a CMOS TFT op-amp at the FDC. Although all nMOS op-amp has been built, these are low gain designs. Low gain limits the resolution of ADCs and DACs. In this chapter the feasibility of building a CMOS TFT op-amp is demonstrated using a-Si:H and pentacene TFTs. Various other op-amp configurations are also demonstrated with their advantages and limitations, showing that all nMOS enhancement-depletion topology might be the best suited in TFT technology for achieving good DC gain and frequency response.

Chapter 6 focuses on the design and fabrication of DACs on TFTs. A full 7 bit switched capacitor DAC based on charge sharing concept is built using all nMOS topology in a-Si:H TFT. The DAC achieves a DNL of $< \pm 0.6$ LSB and INL of $< \pm 1$ LSB without any external calibration. The DAC was operated at speed of 500 Hz with a power consumption of 14 μW. A 5 bit current steering DAC is discussed next on a-Si:H TFTs, which does not require an external buffer.

It is also built in nMOS a-Si:H TFTs, exploiting the high output impedance of the TFTs. However, because of inherent mismatches in TFT process the DNL and INL goes upto 1.2 LSB and 1.8 LSB.

Chapter 7 discusses a 5 bit fully flash ADC on a-Si:H TFT technology. It uses dynamic comparators to speed up performance as well reduce kickback noise. Gray coding is employed at the output to reduce errors due to comparator meta-stability. The logic circuits are built using bootstrapped versions to have rail to rail swing. Due to mismatch and comparator offset the DNL and INL rises to 1.3 and 2 *LSB* respectively. Also the ADC consumes a power of 36 mW at 2k samples/sec.

Finally, the conclusions and scope for future work are presented in Chapter 8.

Chapter 2

CIRCUIT DESIGN in TFTs: A REVIEW

2.1 Introduction

In this chapter, a brief overview of the ongoing efforts on developing flexible displays and electronics on plastic substrates is presented. The present state of the art TFT technologies are discussed. A complete review of TFT op-amp and data converters along with their performance and limitations are summarized. A review of stress testing of mixed oxide TFTs concludes this section.

2.2 Overview of Compact Flexible Displays

The journey to flexible electronics begins with an effort to make commercial displays flexible. Flexible displays are defined as displays which are conformable on different surfaces as well being roll-able. Special electro-optic materials exists are used for fabricating on flexible substrates. The basic structure of a flexible display is shown in Fig. 2.1

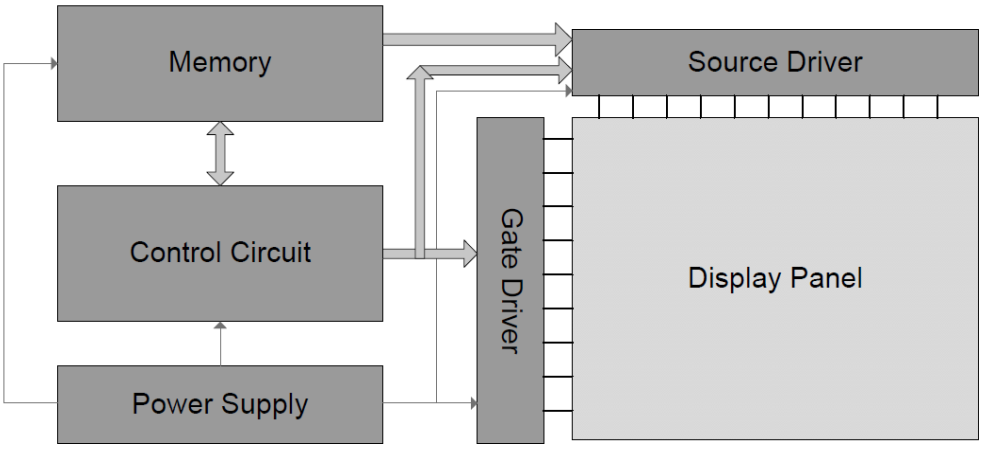

Fig. 2.1 Architecture of a flat panel display.

A typical display system consists of display panel driven by external source and gate drivers, a memory, power supply and a control logic unit. A typical QVGA TFT backplane display system on plastic is shown in Fig. 2.2.

Fig. 2.2 QVGA electrophoretic display backplane on plastic.

A-Si:H TFTs are the dominant device for flexible displays as they are able to withstand high voltage power supplies (20 -30 V) to drive the TFTs.

2.2.1 Flexible Substrates

The substrates which can be used for flexible electronics include metal foils, thin flexible glass to a variety of plastics. The substrate plays a vital role in evaluating the feasibility of the flexible displays as a competitive product in the market. A substrate is chosen for a flexible technology with certain unique properties such as the barrier layer to protect from oxygen and water, cost, handling during manufacture, co-efficient of thermal expansion (CTE), and other chemical performance.

Plastic is a strong contender for such substrates. However, it is dimensionally unstable at temperatures greater than 200°C and highly permeable to water and oxygen compared to glass. Polyethylene napthalate (PEN) is an

important plastic substrate [1]. Another contender is stainless steel, which can withstand high temperature and acts as a good barrier. While it has a low coefficient of thermal expansion, close to that of silicon [2], it can only be used with displays that do not need optical transparency of substrates.

2.2.2 Active Matrix

An active matrix (AM) backplane is essentially a DRAM consisting of TFTs arranged in a matrix format as shown in Fig. 2.3. Each transistor is like a switch and controls one picture element or "pixel". The gate of all the transistors in each row are connected together to form select lines (G1 and G2). Similarly, the source terminals of all transistors in each column are connected together to form data lines (S1 – S3). To transfer data voltage to a particular row, say G1, the select line G1 is enabled by applying a positive voltage (+V) switching "on" all the TFTs in that row. The required data voltage is provided on the data lines S1 – S3. The electro-optic material is charged to the data voltage applied on the data lines. As an example, pixel 2 is charged to +V while pixels 1 and 3 are discharged to 0V. Then the row G1 is turned "off" and row G2 is turned "on". The electro-optic material and an additional storage capacitor holds the data voltage in row G1 for the entire frame time provided the drain to source leakage currents of the TFTs are low. In this way, all the rows are enabled sequentially and data is fed through the data lines until the entire display is addressed. AM backplanes with as many as 6.22 million pixels has been demonstrated [3].

2.3. Logic Circuits on TFTs

All logic circuits developed on TFTs have focused mostly with only one type of devices; either nMOS a-Si:H TFT circuits or pMOS organic circuits. Only recently have a-Si:H and pentacene pMOS TFTs have been integrated to a CMOS structure. Lack of complementary pull-up devices mandate the minimization of the number of pull-up transistors for TFT logic circuits. This suggests programmable logic arrays (PLA) as the fundamental building block of combinational logic circuits in the flexible a-Si:H technology due to their high fan-in and ability to generate many logic outputs with a minimum number of load devices.

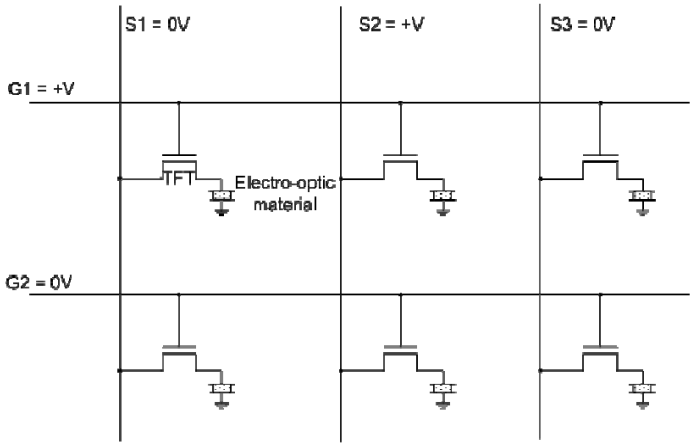

Fig. 2.3 Active Matrix on a-Si:H backplane.

Other problems also plague a-Si:H TFT circuit design: Firstly, low electron mobility, ranging from 0.5 cm^2/Vs to 1.0 cm^2/Vs, which is about 500 × less than that for single crystal silicon, making a-Si:H circuitry necessarily slow [4]. Secondly, availability of only N-type a-Si TFTs necessitates dynamic NMOS circuit design techniques [5]. The conventional diode-connected inverter circuit

can only drive the output voltage to $V_{DD} - V_{th}$ [6]. To obtain a rail to rail voltage swing the well known bootstrap inverter is preferred. Hence the bootstrapped inverter is used in the static and dynamic PLA's as input and output buffers [7].

2.3.1 Static PLA

The static a-Si:H PLA is a 12-input PLA supporting 35 min-terms and 24 sums. It functions as the instruction decoder in a flexible microcontroller. The PLA NOR gates for both logic planes, as NOR gates with high fan-in, are efficient when implemented in pseudo-NMOS logic [8]. The first stage comprising of bootstrap inverters buffers the inputs to the PLA (Fig. 2.4) [9].

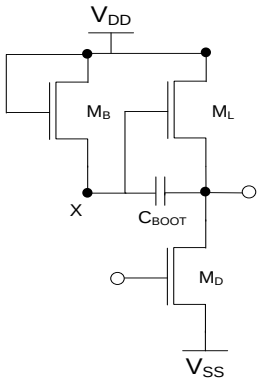

Fig. 2.4 Schematic of bootstrapped inverter.

The pull-up (M_L) to pull-down (M_D) transistor ratio in the bootstrap buffers was 1-to-8. This aspect ratio (A) is obtained from the expression [7],

$$A = \frac{\left(\frac{W}{L}\right)_{MD}}{\left(\frac{W}{L}\right)_{ML}} \geq \frac{V_H^2}{2 \cdot (V_H - V_{TD}) \cdot V_L}, \tag{2.1}$$

where V_H and V_L are the input high and low voltages. $V_H = V_{DD} - V_{TL}$, where V_{TL} is the threshold of the load TFT and $V_L \leq V_{TD}$, where V_{TD} is the threshold voltage

of the driver TFT. The circuit operates with a V_{DD} = 25 V and V_{SS} = 0 V. The width of the TFT's in the input bootstrap buffers depends on the number of N-channel TFT's it drives to generate the min-terms in the AND-plane. The number of TFT's driven by the input buffer in the static PLA varies from 1 to 13.

The buffered inputs drive the NMOS NOR gates in the AND plane to generate the min-terms. The OR plane is driven by the outputs of the AND plane, generating the sum-of-product terms (see Fig. 2.5). The pseudo-NMOS static a-Si:H PLA is attractive due to its timing simplicity, although there is static power consumption and slow low-to-high output transition. It also suffers from poor noise margins, which are further degraded by gate bias induced V_{th} shift. The goal is to integrate the PLA with other logic circuits in the digital system therefore output buffers are not designed for a specific load capacitance.

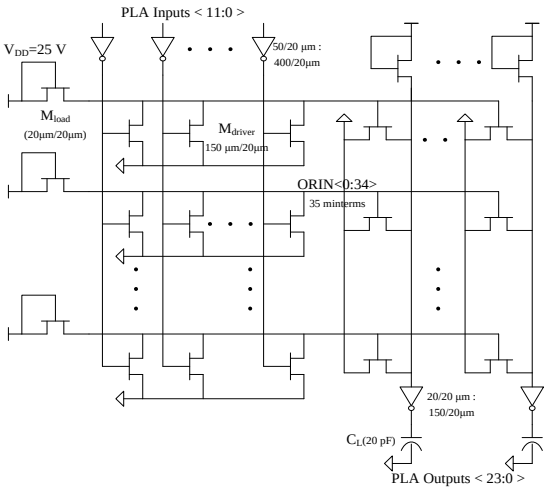

Fig. 2.5. AND-OR static PLA after [9]

2.3.2 Dynamic PLAs

Dynamic approaches, in which the pull up transistors are clocked, is an attractive alternative as they limit the static power consumption. Specific dynamic

circuit topologies can also mitigate the V_{th} shifts [8]. A dynamic a-Si:H PLA implementing the same functions as the static PLA was investigated in [9]. The dynamic PLA has footed dynamic NOR gates in the AND and OR planes as shown in Fig. 2.6. Two non-overlapping clocks $\mathbf{\Phi_1}$ and $\mathbf{\Phi_2}$ are used in dynamic NOR gates. When clock $\mathbf{\Phi_1}$ is high the AND plane pull-up TFT's are active and the outputs (product terms labeled ORIN) are pre-charged to V_{DD}-V_{th}. During $\mathbf{\Phi_2}$ the product terms evaluate to the state determined by the AND plane pull-down network. The dynamic nodes in the AND/OR planes are prone to charge leakage through the pull-down TFT's for low input voltages (i.e. V_L) during the evaluation phase.

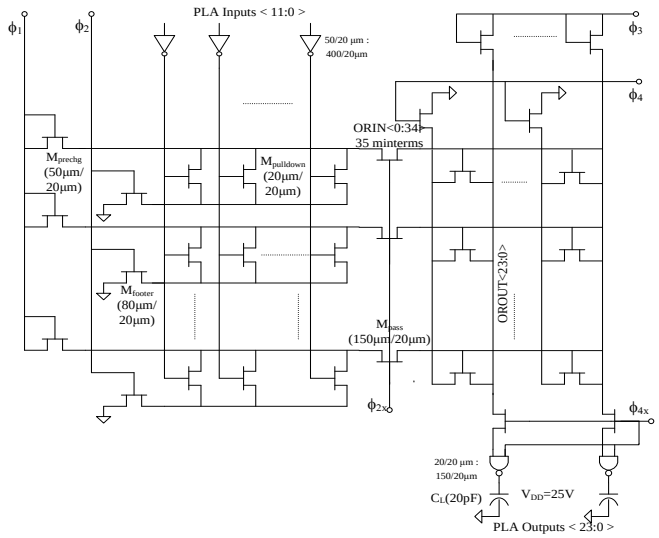

Fig. 2.6. AND-OR Dynamic PLA after [9].

The AND plane output drives the OR plane directly, violating monotonicity conditions required by dynamic circuits [8]. As large DC currents are created by replica circuits, another non-overlapping clock set ($\mathbf{\Phi_3}$ and $\mathbf{\Phi_4}$) are asserted after completion of AND plane. The OR-plane NOR gates pre-charge

during $\mathbf{\Phi_3}$ and evaluate during $\mathbf{\Phi_4}$. The OR plane output is captured by the pass-transistors isolating the min-terms of the AND-plane. The pass-transistors are ON until the next $\mathbf{\Phi_1}$ phase pre-charges the ORIN lines and asserted by the $\mathbf{\Phi_{2X}}$ clock which is essentially the logical OR of clock phases: $\mathbf{\Phi_2}$, $\mathbf{\Phi_3}$, and $\mathbf{\Phi_4}$. For PLA based state machines the OR-plane outputs must be latched to hold the state in the subsequent phase. Delaying the result on the PLA output nodes until $\mathbf{\Phi_3}$ is asserted eliminates the need for latches.

2.3.3 Non-volatile Memories

The flexible non-volatile memory (NVM) cell has a similar structure and layout in comparison to a 6 transistor SRAM cell with the PMOS loads in the back-to-back inverters removed (Fig. 2.7). All n-type a-Si:H TFTs are used in this NVM circuit [10]. Transistors M3 and M4 provide access. A bit of information is stored as the V_{th} difference of the differentially accessed back-to-back TFTs, M1 and M2.

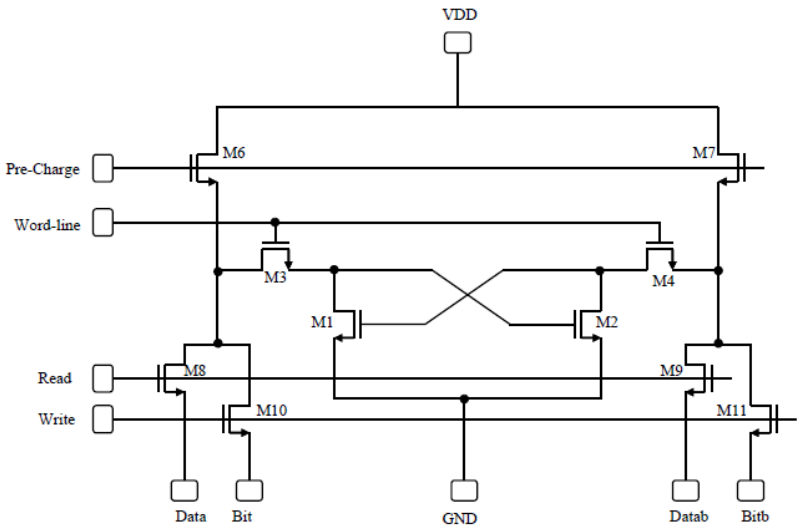

Fig. 2.7. Schematic of all nMOS non-volatile memory after [10].

The cell state is programmed by electrically stressing one of the two devices and increasing its V_{th}. The positive feedback configuration of M1 and M2 will cause the device with the lower V_{th} to discharge its drain more quickly while the other drain remains at an elevated potential. The differential structure eliminates any ambiguity in the absolute value of the V_{th} due to processing variations, and the NVM cell stores a bit of information based solely on the relative magnitudes of the two V_{th}s.

Specifically, a write operation is accomplished by asserting the word line which connects a row of cells into their respective bit and bit-bar lines through M3 and M4. The write signal is asserted connecting the externally driven data onto the bit lines and into the selected cells. With logic '1' = 30 V, this stress time results in a threshold voltage shift of approximately 2 V for the device with a '1' on its gate. The other device with 0V on its gate is unstressed with no change in its V_{th}.

2.3.4 CMOS Inverters on TFTs using A-SiH and Pentacene TFTs

An all nMOS (or for that matter all pMOS) TFT circuits have a large static power dissipation due to the existence of a direct path from supply to ground. Such power dissipation would prevent it from being used in battery operated portable systems. Thus the obvious choice is to integrate the a-Si:H nMOS TFT with pentacene pMOS TFT in a complete CMOS structure. This was first shown in a paper by Bonse *et al* [11]. Using CMOS structure, inverters, NOR and NAND gates and ring oscillators were designed. The highest gain of inverter was however only 22 at a supply of 20 V due to the low mobility of both a-Si:H and

pentacene TFTs. With these inverters an 11 stage ring oscillator was designed which had a delay of 5 µs/stage, consuming a power of 0.2 µW. However the entire circuit was designed on glass and hence was not flexible.

Flexible CMOS TFTs have also been fabricated at the FDC and University of Texas at Dallas. Fig. 2.8 shows a logic circuit built on flexible CMOS. The detailed fabrication process of CMOS integration is outlined in Section 3.3 of Chapter 3. Fig. 2.9 shows the transfer characteristics of the inverter and also the gain as the input voltage is swept from low voltage to rail [12].

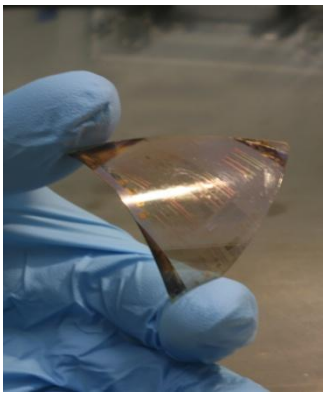

Fig. 2.8 Flexible CMOS logic circuit after [12].

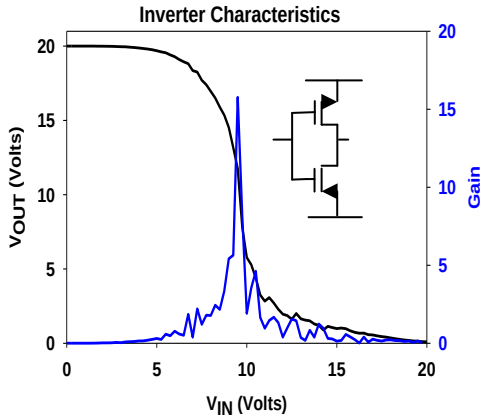

Fig. 2.9 Inverter characteristics and gain on flexible CMOS after [13].

As stated earlier, the threshold voltage (V_{th}) of these devices degrades due to application of electrical stress. There are two main causes for the degradations:

defect state creation in the bandgap of the materials and charge trapping in the insulator-semiconductor interface. It has been speculated that for a-Si:H and pentacene the first mechanism dominates. As such an empirical stretched exponential equation has been formed to quantify the change in V_{th} with time. The equation depicting such a change is as follows [14]

$$\Delta V_{th}(t) = (V_{GS} - V_{th})\left[1 - \exp\left\{-\left(\frac{t}{\tau}\right)^{\beta}\right\}\right] \tag{2.2}$$

where V_{GS} is the gate to source voltage and τ and β are empirical parameters. The typical values of β and τ are 0.53 and 0.23 and $5x10^4$ and $5x10^8$ respectively for a-Si:H and pentacene TFTs. All measurements were made with Keithley 4200-SCS parametric analyzer. Degradation of individual TFTs results in degradation of the overall circuit itself. The impact of these is shown in Fig. 2.10 for a CMOS inverter. The inverter is operated continuously with a pulse of 50% duty cycle and the output is plotted at different time intervals [13].

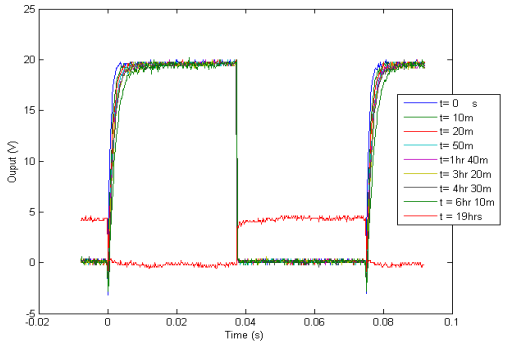

Fig. 2.10 Degradation of inverter characteristics with time after [13].

2.3.5 Inverters in Mixed Oxide TFTs

Apart from using a-Si:H and pentacene TFTs, logic circuits, lately have been demonstrated in mixed oxide TFTs also. To avoid low gain due to lack of

complementary devices as load and to have rail to rail swing, depletion mode TFTs have been developed in zinc tin oxide [15]. Both enhancement and depletion mode TFTs with channel length = 15 μm were simultaneously fabricated on the same substrate. With a supply voltage of 10 V, a gain of 10.6 was obtained. The low and high noise margin was 2.1 V and 3.9 V respectively. Previously reported gain was much lower with 1.7 at a voltage of 18 V, due to use of diode connected load [16].

2.4 Flexible Analog and Mixed Analog Circuits

Like logic circuits there has been a widespread effort to develop analog circuits in TFTs. However there has been no reported effort to develop CMOS circuits with TFTs. Lack of complementary devices result in lower gain. Also lower g_m due to low mobility results in low unity gain frequency (UGF). Moreover analog circuits depend largely on biasing circuits to provide constant bias voltages and currents. As the TFTs degrade, the biasing current and voltages also degrade resulting in circuit failure. To make things worse large process variation induces mismatch in the TFTs resulting in severe performance limitations especially restricting the resolution of the ADCs and DACs.

2.4.1 TFT Differential Amplifier and Op-amp

Kane *et al* built a differential amplifier with organic pentacene TFTs, operating with a differential gain of -5 to -10 [17]. The differential amplifier consisted of a source coupled pair with depletion mode loads to boost the gain. The input offset voltage due to process mismatch was found to be 0.6 V. TFTs had length = 10 μm.

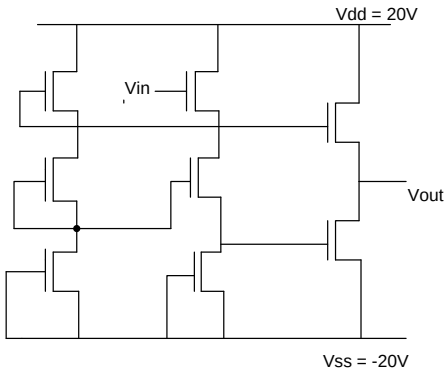

Fig. 2.11 Cascode common source amplifier after [18].

A cascode common source amplifier was built in pentacene pMOS TFTs [18]. Due to cascoding, the DC gain was around 10dB with a bandwidth of 1.4 kHz. Fig. 2.11 shows the structure of the cascode amplifier. Power supply used was 10V.

The first op-amp in TFT was a single stage op-amp designed in a-Si:H nMOS TFT [19]. Due to the lack of complementary pMOS TFT or depletion mode TFTs, diode connected enhancement nMOS TFTs were used as loads. However such a configuration would give an extremely low gain. Hence a positive feedback was implemented by connecting an amplifier between the source and gate of the load transistor to boost the gain. The amplifier was implemented by cascading two common source stages. However the feedback factor was kept less than 1 to avoid self oscillations. The entire schematic of the op-amp with the corresponding TFTs is shown in Fig. 2.12. The op-amp achieved a DC open loop gain of 43 dB and a UGF of 30 kHz with a load cap value of 20 pF. The power consumed was 3.55 mW, while the area was 3.4x1.5 mm^2. The output swing was quite low, equaling 3 V and was achieved with a power supply

of 25 V. However, all the biasing voltages were derived from voltage sources, instead of from a single current source.

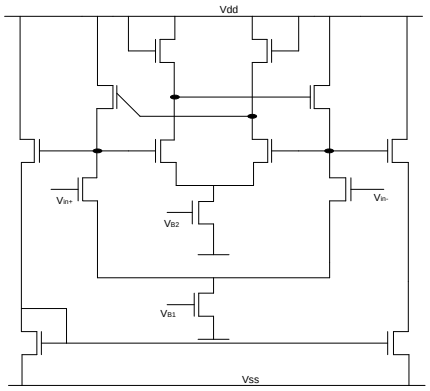

Fig. 2.12 Schematic of an all nMOS op-map with gain boosting after [19].

2.4.2 ADCs and DACs in TFTs

Just like op-amps, there have been several attempts in fabricating ADC and DAC with moderate resolution and speed. These are necessary to interface the analog sensor output with digital display. Similar to op-amps, the fabrication of these circuits is plagued by low mobility, instability and mismatch due to process variation. The first attempt to build any data converter circuits was a 4 bit charge redistribution DAC using pentacene organic TFTs [18]. It operated at a clock speed of 100 Hz sampling 25 data per samples, which was enough for slow varying temperature or pressure or biological signals.

Subsequently an attempt was made to build a full fledged 6 bit DAC with organic TFTs by Xiong *et al* from Stanford [20]. A switched capacitor architecture was chosen based on charge sharing concept to avoid any errors due to transistor mismatch and TFT degradation. As the TFTs act just as switches, the precision of the currents matter little. To minimize mismatch among capacitors,

large unit capacitors were chosen according to analog design rule [21]

$$\sigma = \frac{k}{\sqrt{Area}} \tag{2.3}$$

where σ is the standard deviation of the mismatch and k is process dependent constant. Thus 0.04 mm^2 unit sized cap were chosen with 280 pF. With unit cap of 280 pF, the largest cap value would be (2^6-1) 280 pF, which is prohibitively large in terms of area as well as for the OTFTs to drive. Hence a C-2C architecture was chosen, so that the maximum value was 560 pF, easily achievable in pentacene technology. The entire structure on glass is shown in Fig. 2.13.

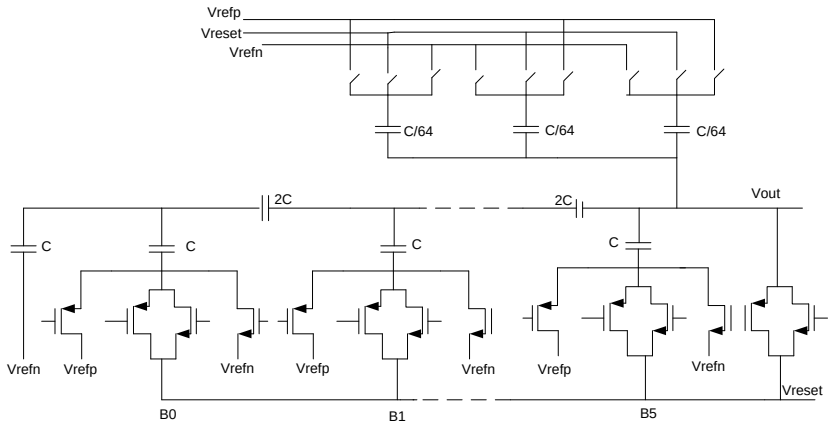

Fig. 2.13 6 bit C-2C DAC after [20].

The DAC operated at a speed of 100 Hz and achieved a DNL and INL of 0.6 and 0.8 *LSB* respectively. However due to mismatch between the TFTs, external calibration was required to obtain the above DNL and INL. The power supply used was 3 V. The spurious free dynamic range (SFDR) was 24 dB.

The success of the above fabricated 6 bit DAC inspired a couple of different ADCs on TFTs. One of them is a successive approximation register

(SAR) type 6 bit ADC built in organic TFTs by Xiong *et al* [22]. The TFTs consisted of three major parts: 1) a 6 bit C-2C DAC which reused the design described above, 2) an external FPGA for digital SAR logic and 3) a single bit comparator. Fig. 2.14 shows the schematic of the comparator. A cascade of inverter stages were chosen to make the design simple, to avoid any performance degradation due to mismatch and to make the circuit self-biased. The circuit works in two phases. In the first phase, the input and output of every inverter is shorted by a transmission gate, thereby fixing a stable operating point and nullifying any offset whatsoever. Also the DAC voltage is applied to the top plate of $C_{S1.}$ In the compare phase the transmission gate shuts off. The voltage at the bottom plate of C_{S1} (V_{in} - V_{DAC}) is thus amplified to full rail making a logic decision of '1' or '0'. Because of possible capacitor leakage, the ADC sampled every clock cycle, rather than every sixth clock cycle usually done in SAR.

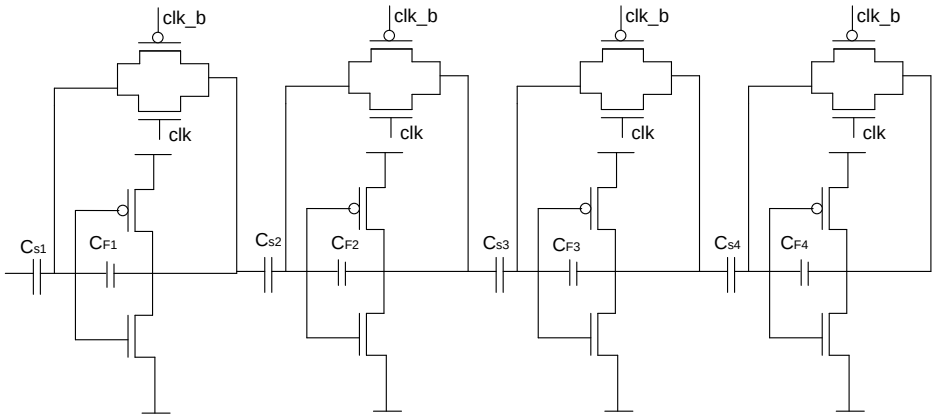

Fig. 2.14 Comparator for 6 bit SAR ADC after [22].

For a 2 V full scale range with 0.5 V LSB resolution, a gain of 96 was required, which could be achieved with 3 cascaded inverter stages. However a 4th stage was also added to shift the output closer to $V_{DD}/2$. At 100 Hz, the DNL and

INL were 1.5 and -3 *LSB* respectively, while the power consumed was 3.6 μW. The power supply was again 3 V. The area consumed was 2.8x2.2cm^2.

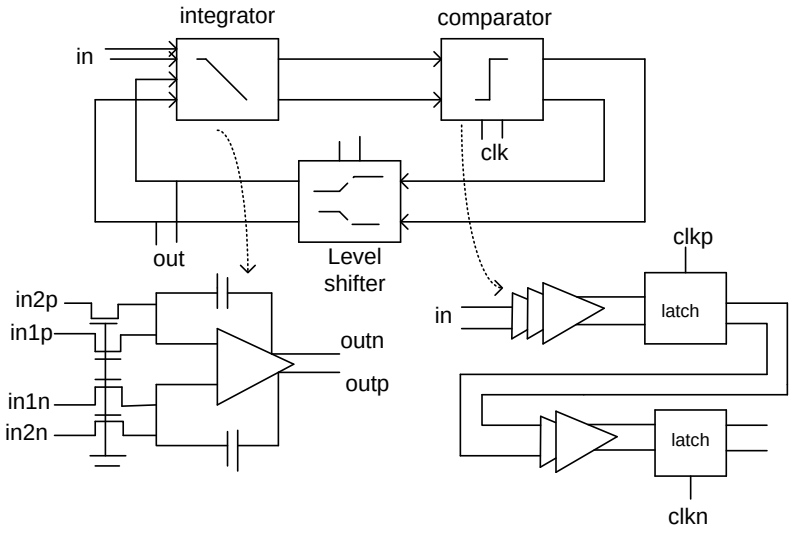

Fig. 2.15. 1st order continuous time ΣΔ ADC in OTFT after [23].

Similar to the SAR ADC, a sigma delta was also built in organic pentacene TFTs with a resolution of 26.4 dB (around 4 bits) at an OSR of 16 [23]. The schematic of the ADC with the integrator and comparator is shown in Fig. 2.15.

The ADC was a 1st order sigma delta modulator consisting of an integrator and a comparator. The integrator was implemented by a 3 stage fully differential amplifier compensated by Miller capacitors for pole splitting. Linear common mode feedback was implemented to suppress any output variation due to degradation of V_T. The op-amp achieved a DC gain of 23 dB and a unity gain frequency of 500 Hz at a phase margin of 70°. The comparator was a cascaded array of 3 single stage amplifiers and the first latch and then a second array of amplifiers followed by a second latch. The latch was clocked differentially and

the comparator operated upto a speed of 1kHz. The circuit consumed a power of 1.5mW. The power supply was 15V.

2.4.4 Analog Circuits in Poly Silicon TFTs

It should be mentioned in passing that high performance telescopic cascode op-amp (DC gain of 53 dB and UGF of 6 MHz) have already been fabricated using polycrystalline TFTs [24] using single grain TFT technology. Also a 5 bit flash ADC operating at 3 Ms/sec has also been fabricated using laser crystallized polysilicon TFTs [25]. However, for both cases the processing temperature is > 350ºC, which makes them incompatible for plastic substrates and hence flexible electronics.

2.5. Compact Modeling of TFTs

For proper simulation of analog circuits, accurate, simple and reliable compact models of TFTs, valid in all regions of operation are needed. Basically there are two compact models for a-Si:H TFTs. One is the RPI model developed by Michael Shur *et al*, at Renesselaer Polytechnic Institute [26,27]. In this approach drain current (I_{DS}) and charges are expressed as a function of terminal voltages through inversion charge density. While this results in a unified approach, it requires analytical solution of several implicit equations making the model and complex and difficult to implement in circuit simulator. The second approach was to use one of the existing MOSFET models and modify it for TFTs [28]. The major modification was to adapt the 4 terminal BSIM 3v3 MOS model [29] to a 3 terminal model suitable for the TFTs. Hence, in this model, the bulk terminal in the BSIM model is connected to the most negative supply and the

parasitic bulk-source and bulk-drain diodes are disabled by nullifying the bulk effect related BSIM 3 parameters. The insulator thickness had to be changed to an effective thickness as BSIM models use SiO_2 as the default insulator, while SiN_x is the insulator for a-Si:H TFTs. Also as these TFTs degrade with electrical stress, this additional phenomenon was included in the modified model using (2.2). Fig. 2.16 shows a comparison obtained this model and measured data for I_{DS} vs V_{DS} characteristics.

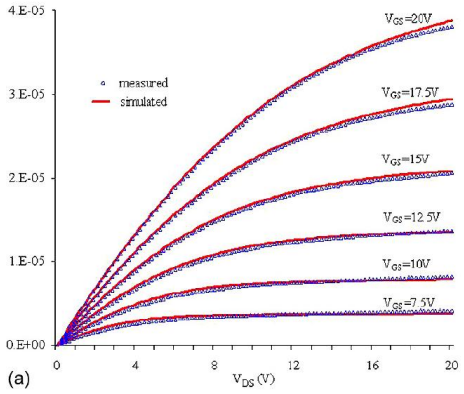

Fig. 2.16. Comparison of measured data with that obtained from the model.

Along with the model, a parameter extraction software NGExtract was also developed at the FDC using *Perl* programming. The extraction was based on Levenburg-Marquardt non linear least squares algorithm [30] to achieve best possible fit and is currently being used to extract circuit simulation parameters for TFTs. The above model along with the extraction software serves the purpose of analog designs in TFTs.

2.6 Stress Testing of TFTs

The TFT characteristics degrade in presence of electrical stress with time. The main cause of such degradation has been attributed to defect state creation in

the semiconductor bandgap due to the breaking of Si-H dangling bonds and due to charge trapping in the semiconductor insulator interface [31-33]. In a-Si:H and pentacene, it has been found that defect state creation is the dominant degradation mechanism. This is evident in the degradation of the subthreshold swing and that the degradation follows the stretched exponential model (2.2) with electrical stress. The values of the parameters for both these TFTs have been noted previously from our experiment. Organic pentacene TFTs, apart from electrical stress degradation, degrade also in ambient conditions, in presence of oxygen and moisture [34,35]. Thus experiments with pentacene TFTs, including testing of circuits in pentacene are usually done in an inert atmosphere of nitrogen.

However, for the case of metal oxide semiconductors like indium zinc oxide (IZO) and indium gallium zinc oxide (IGZO), it has been found that charge trapping is more dominant [36-38]. As such there is no or little degradation of subthreshold swing even after extended period of stress. Also the degradation model was found to obey the logarithmic model associated with charge trapping [39]. This model is as shown in equation (2.4).

$$\Delta V_{th} = r_0 \log\left(\frac{t}{t_0}\right) \tag{2.4}$$

However there has been some evidence of defect creation as well, as reported in [33] for very high gate bias stress. Moreover some studies have shown that the degradation model actually follows the stretched exponential model [40]. It has also been found that the degradation mechanism depends somewhat on the insulator [41] and also the manner in which it is deposited. Thus while with SiO_2

as the insulator the degradation follows the stretched exponential, with HfO_2 as the insulator deposited via atomic layer deposition (ALD) or sputtering, it neither follows (2.2) nor (2.4). In fact while ALD shows less degradation, sputtering shows far worse degradation when compared to (2.2). Moreover it was found that low temperature thermal annealing also improved the characteristics and stability of these devices [41].

2.7 Summary

In this chapter a brief overview of the different TFT display technology was presented including a summary of the existing logic circuit and op-amp designing on TFTs is included. Different data converter design topologies for TFTs to be applicable for large area sensors were discussed. A brief overview of the compact model used for circuit simulation in these TFTs was included. Finally stress testing and their impact on device characteristics along with the degradation mechanism was also surveyed.

Chapter 3

A-Si:H, PENTACENE and MIXED OXIDE TFTs

3.1 Introduction

In this chapter the device fabrication process and TFT characteristics of a-Si:H, pentacene pMOS and indium zinc oxide (IZO) nMOS TFTs, fabricated at the FDC and the University of Texas at Dallas are outlined. A-Si:H and pentacene TFTs are discussed first followed by the newer IZO TFTs.

3.2 A-Si:H TFTs

A-Si:H is currently the most dominant TFT technology, being widely used for flexible displays. The most commonly used a-Si:H TFT structure is the inverted staggered structure (or bottom gate structure) due to its superior a-Si:H / gate dielectric interface properties such as lower interface density of states [42]. There are two types of inverted staggered structure: back channel etched structure and the channel passivated structure.

3.2.1 Fabrication Process

The a-Si:H TFT developed at the FDC has a channel passivated bottom gate inverted staggered structure as shown in Fig. 3.1.

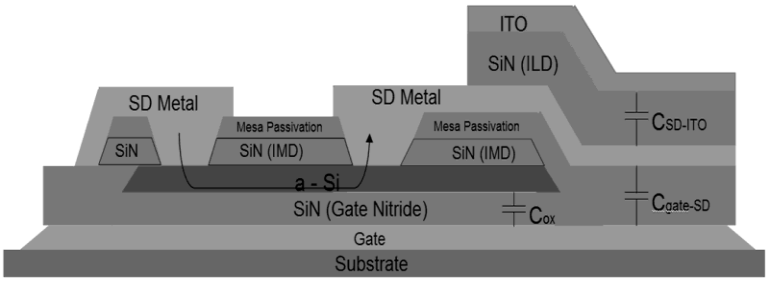

Fig. 3.1. Cross section of a-Si:H TFT structure with different layers.

The development of A-Si:H TFTs on flexible substrates such as stainless steel and heat stabilized PEN, is tuned to a low temperature process (180^{o} C). Molybdenum patterned on the substrate is the gate metal. The gate dielectric is silicon nitride (SiN_X) and the active layer is hydrogenated amorphous silicon deposited with plasma enhanced chemical vapour deposition (PECVD). SiN_X is preferred over SiO_2 as the former has less number of defect states. A nitride passivation step is performed before the contacts are etched to prevent the contamination of the back channel during process steps. The source/drain metal is sputtered on as an N+ amorphous silicon / aluminum bi-layer. Another metallization step using indium tin oxide (ITO) is carried out. The circuits are annealed after fabrication at 180^{o}C in nitrogen atmosphere for 3 hours to stabilize contact metallurgy. The tri-layer process needs four mask steps:

1. bottom gate metal
2. a-Si:H island creation
3. source/drain vias
4. top metal/n+ patterning

The first mask defines the gate metal pattern. The second mask step is used to create the three thin films, i.e. gate dielectric, a-Si:H and back channel protection dielectric. The third mask step creates the source/drain vias which are the openings through the back channel protection dielectric (i.e. SiN_x) to connect to the top metal. Finally the fourth masks define the source/drain metals including the n+ layer.

3.2.2 Device Characteristics

The a-Si:H TFT acts very similar to a MOSFET. The I-V transfer characteristics of a-Si:H TFT is shown in Fig. 3.2. The typical V_{th} is about 1 V with the mobility being 0.8 – 1 cm^2/V-sec. The subthreshold swing is about 0.5 V/decade while the on-off current ratio is about 10^9.

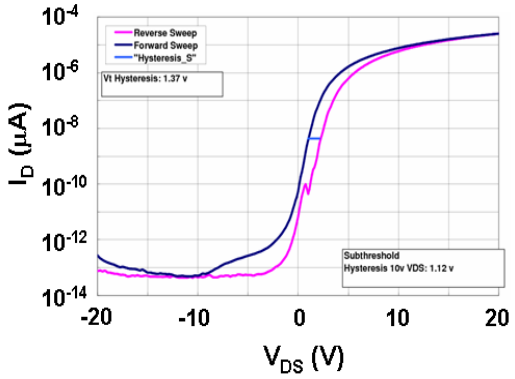

Fig. 3.2. Measured transfer characteristics of a-Si:H TFTs.

As previously mentioned, a-Si:H TFTs degrade with time in presence of electrical stress [31]. These electronic states in amorphous silicon are split into three categories: *Extended states* are located at the valence and conduction band edges and are the result of the spatial disorder in a-Si:H, *band tail states* are the electronic states formed due to weak Si-Si bonds (WB's) which are distributed from the band edges to the mid-gap energy and the *deep states* which are formed due to dangling bonds (DB's) and are localized deep within the band gap, shown in Fig. 3.3. Deep states are created due to continuous electrical stress [43]. This is manifested in the increase in subthreshold swing due to electrical stress. Also, along with subthreshold swing the mobility too decreases due to increased

scattering from trapped carriers in these defect states. Moreover, because of permanent dangling bonds [32], the defect states created are also permanent and so the stressed devices do not recover [44].

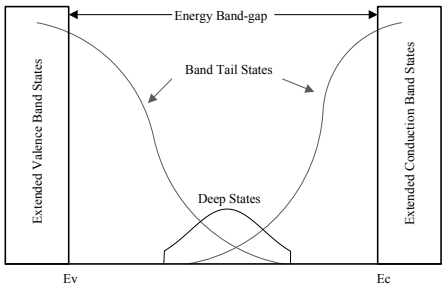

Fig. 3.3. Band tail and deep states within a-Si:H bandgap.

3.3 Pentacene TFTs

Organic pentacene TFTs form the pMOS counterpart of a-Si:H TFTs. They have also become mainstream TFT devices with flexible OLED displays.

3.3.1 Device Fabrication

The organic pMOS TFTs developed at University of Texas, Dallas use pentacene as the active layer. Aluminum acts as the gate metal and parylene as the gate dielectric of thickness 0.5 μm. The dielectric is patterned next to define metal gate vias and channel. Next, gold (100 nm) is deposited by e-beam evaporation and patterned to form source-drain contacts. Pentacene (150 nm) is deposited at room temperature. Finally the device is capped with parylene and vias are opened.

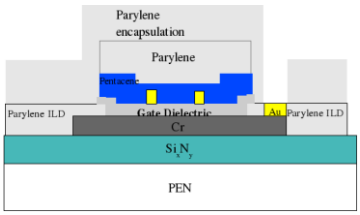

Fig. 3.4. Cross section of pentacene TFT structure with different layers.

3.3.2 Device Characteristics

The typical transfer characteristic is shown in Fig. 3.5. Saturation mobility is about 0.08 cm^2/Vs with an I_{on}/I_{off} ratio greater than 10^5. The threshold voltage is slightly less than -1.4.

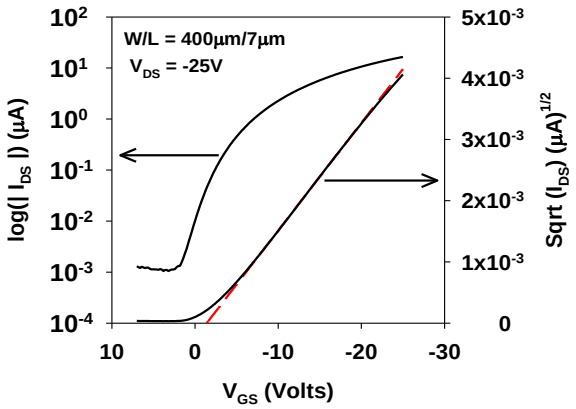

Fig. 3.5. Measured transfer characteristics of pentacene TFTs.

Like a-Si:H TFTs, pentacene TFTs also degrade with electrical stress. However, in addition these TFTs degrade in ambient conditions too [32,33].

3.4 Flexible CMOS

Together a-Si:H from FDC and pentacene from University of Texas at Dallas yield CMOS circuitry. Fig. 3.6 shows the cross section of the Flex CMOS.

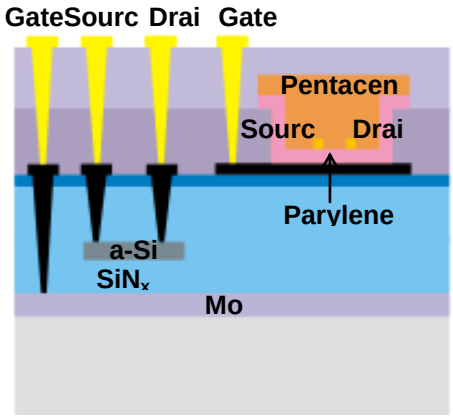

Fig. 3.6. Cross section of a-Si:H/pentacene CMOS TFT with different layers after [13].

The a-Si:H part is done at FDC after which the rest of pMOS development part including the passive encapsulation is done at UT Dallas. Several vias are formed to enable arbitrary connection of nMOS and pMOS TFTs to form any kind of CMOS circuit. The process steps for a-Si:H and pentacene TFTs have already been outlined before. Not only for logic circuits, CMOS TFTs were also used in source drivers reducing power by 300x, compared to nMOS drivers [13].

3.5 ZIO TFTs

Recently mixed oxide TFTs like ZIO, Indium gallium zinc oxide (IGZO) and Zinc-Tin oxide have shown promise as the next generation TFTs with improved device performance and stability. ZIO is presently being fabricated and tested at the FDC as the future TFT device to replace a-SI:H TFTs.

3.5.1 Fabrication Process

The a-ZIO TFTs have a bottom gate inverted staggered structure fabricated at 180° C. Molybdenum is used as gate and is sputtered and patterned (thickness = 150 nm). A stack of SiO_2 (thickness = 100 nm), ZIO (thickness = 50 nm) and SiO_2 (thickness = 100 nm) is deposited next. The ZIO deposition is done between 77 and 91 °C and top layer of SiO_2 is deposited at 200 °C. The ZIO is patterned and molybdenum is sputtered to form source/drain contacts, followed by inter-layer dielectric (ILD) deposition. Indium-tin-oxide (ITO) is patterned as connecting metal to the electrophoretic material in an active matrix display. Finally the TFTs are annealed in an atmosphere of nitrogen for 1 hour. Fig. 3.7 shows the schematic of the device with the different layers. The composition of the active a-ZIO is 60% Zinc and 40% Indium.

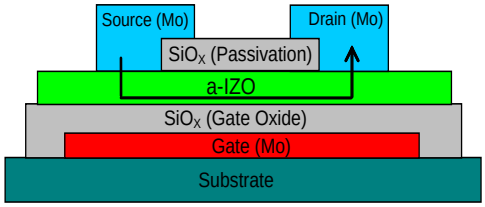

Fig. 3.7. Cross section of a-ZIOTFT structure with different layers.

3.5.2 Device Characteristics

Arrays of TFTs with *W/L* equal to 96/9 were fabricated. An average threshold voltage (V_{th}) of -0.4V, linear mobility varying between 4-5 cm^2/Vs and a subthreshold swing variation of 0.61-0.81 V/dec was obtained with the TFTs. The typical I_{on}/I_{off} ratio was 10^9. Fig. 3.8 shows the transfer characteristics.

It has been found that these mixed oxide TFTs are much more electrically stable than a-Si:H or pentacene TFTs. Moreover, the TFTs revert back to their virgin state when left unstressed for extended periods of time. They obey the logarithmic model of decay, as shown in (2.4). All these point out by and large electrical stress degradation is mainly caused due to charge trapping.

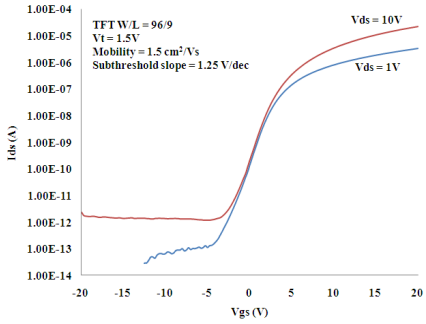

Fig. 3.8. Measured transfer characteristics of a-ZIO TFTs.

3.6 Summary

This chapter presented an overview of the different TFT structures that are used for flex electronics and displays. A complete discussion on the device

fabrication, materials used and device characteristics like subthreshold swing and mobility were presented along with schematics of the device structure and transfer characteristics.

Chapter 4

EFFECT of EXTERNAL STRESS on the PERFORMANCE OF ZIO TFTs

4.1. Introduction

Amorphous zinc indium oxide (a-ZIO) TFTs are a strong candidate for replacing amorphous silicon as the dominant thin film device for large area electronics (LAE) [42]. Large area electronic devices need to be rollable and able to withstand mechanical strain in bent condition conditions. The potential applications include X- ray detectors, neutron detectors, smart medical bandages, *etc*. In this chapter the impact of electrical, mechanical stability under external stress is determined. The dominant degradation mechanism is in these devices is also investigated.

4.2 Electrical Stability of ZIO TFTs

The ZIO TFTs with the size of 108µm/9µm and dielectric thickness of 1000Å have been electrically stressed continuously for extensive periods of time under various DC bias conditions. Below is the description of various stress measurements taken using a probe station and semiconductor parameter analyzer.

4.2.1 DC Bias Stress

For the DC stress test, the gate and drain of the TFTs were connected to a DC bias, varying from -20V to +20V using a semiconductor parameter analyzer. At regular intervals, the DC bias was disconnected and the I_{ds} vs. V_{gs} characteristics of the TFT measured. The TFTs were stressed for 10,000 seconds. The change in threshold voltages (ΔV_{th}) were extracted for each test and plotted as shown in Fig 4.1. To extract ΔV_{th}, current per unit width approach has been

followed. An appropriate reference current was selected from the unstressed TFT characterization plots, and corresponding gate voltages for that reference current were noted for different stress times. The difference in the observed gate voltages is determined to be the V_{th} shift caused by the stress tests. As seen in Fig 4.1 the change in V_{th} is within 2.5V for ZIO TFTs for all voltage stress.

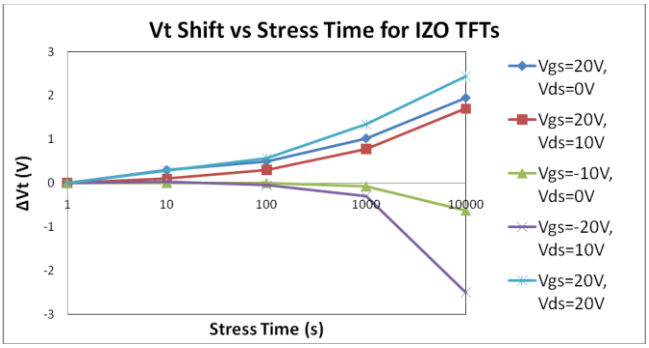

Fig. 4.1 Change in V_{th} after 10,000 seconds of DC stress for ZIO TFTs.

In analog circuits, a constant current source circuit is very important. In order to simulate the behavior seen in analog circuits, a TFT was stressed with V_{gs} = V_{ds} = 20 V. This will keep the TFT in a constant current source mode. Fig 4.2 shows the plot of change in saturation drain current vs. time for ZIO and a-Si:H TFTs. In the constant current mode, the change in saturation current is about 19% in ZIO TFTs while this is 71% in a-Si:H.

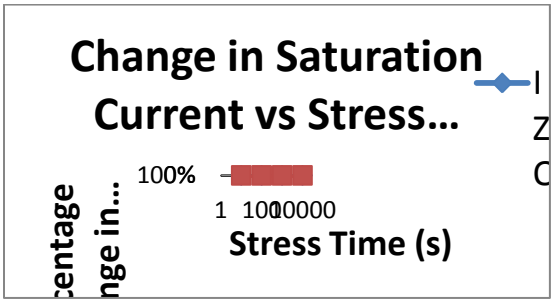

Fig. 4.2 Change in saturation current of ZIO and a:Si TFT after 10,000 sec of DC stress.

4.3 Localization of Gate Bias Induced Stress

In this chaper a test is reported which shows the effect of drain bias on stability of the TFTs, both under positive and negative gate bias stress.

4.3.1 Rationale

In bulk MOSFETs hot electron degradation occurs only at the drain end of the channel where electric fields are higher. This creates a difference in the drain current between operation in forward mode (i.e., when the source and drain are the same as for the device under stress) and reverse mode (i.e., with source and drain nodes interchanged) [45,46]. This helps to localize the region of degradation in the channel. In a-Si:H TFTs similar stress experiments showed that the degradation due to defect creation was also localized in the channel where carriers were present [47]. This also created a difference in the forward and reverse mode current, but the nature of difference was quite distinct from MOSFETs under electron trapping. Thus measurement of post stressed forward/reverse current helps us to localize the region of degradation as well as the mechanism. Studying the impact under reverse mode of operation is also important where the devices act as bi-directional switches.

4.3.2 Experiment

Here a similar experiment on a-ZIO TFTs fabricated at FDC to ascertain the impact of drain bias [47,48] as also the effect of source/drain reversal on post stressed drain current, is performed. All stress measurements are made with a Keithley 4200C parametric analyzer. The measurements were made by biasing the gate and drain with certain bias (grounding the source) and measuring the I-V

characteristics at regular interval of time as specified. The idea behind the experiment is as follows: Stressing the TFTs in linear mode of operation, (i.e. V_G-$V_T > V_D$, where V_G and V_D denote the gate and drain bias respectively) and saturation mode, the post stressed drain current in both the forward and reverse mode of operation is measured.

4.3.3 Results and Analysis

Stressing the TFTs in linear mode, the measured currents in both forward and reverse mode are the same as shown in fig. 4.3a and 4.3b. This happens because in the linear mode of operation, the channel charge is more or less uniformly distributed across the channel and the electric field is quite uniform across the channel. As a result, charge trapping in the insulator-semiconductor interface takes place throughout the channel. Thus both modes show same stressed currents, within experimental error.

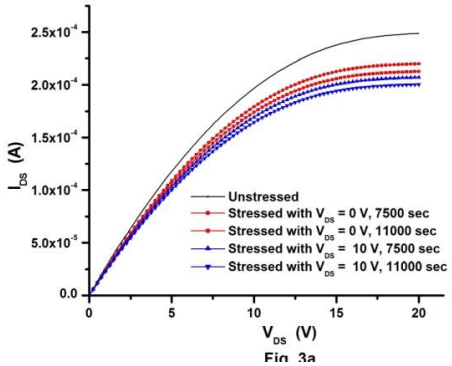

Fig. 4.3a. Stressed in linear mode. V_{GS} = 20 V and V_{DS} = 10 V. Forward and reverse mode currents coincide.

For saturation mode stress, the post stressed saturation current shows considerable asymmetry in forward and reverse configurations in the saturation

regions, as can be seen in fig. 4.4a and b This is in stark contrast with what has been observed for a-Si:H [47], where reverse current was greater than forward, due to defect creation being the dominant instability mechanism.

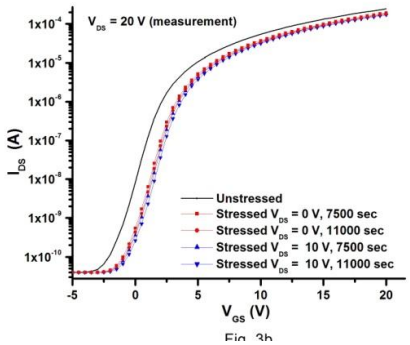

Fig. 4.3b. I_{DS} vs V_{GS} plot. Stressed in linear mode showing same current in both modes.

The nature of the post stressed forward/reverse currents are very similar to those observed in MOS transistors under hot electron trapping [46]. Thus under saturation mode stress, charge trapping is believed to dominate over defect creation. As a result the difference can be qualitatively explained in terms of effective channel length and mobility μ reduction, as in MOSFET [46]. Both the un-stressed and stressed saturation current is proportional to effective mobility and inversely to L_p, where L_p is the channel length from source to pinch-off point.

$$I_{Dsat} \alpha \frac{\mu}{L_p}. \tag{4.1}$$

As V_D increases L_p decreases and I_{DSAT} increases. This increase in L_p persists in both forward and reverse modes in a virgin device. However the channel shortening effect is greater in forward mode for a degraded device [46]. This is possibly because of higher channel resistance at the drain in stressed

device, which results from reduced mobility and greater charge trapping near the drain. This introduces asymmetry in the threshold voltages near source and drain ($V_{TD} > V_{TS}$: see fig. 4.5).

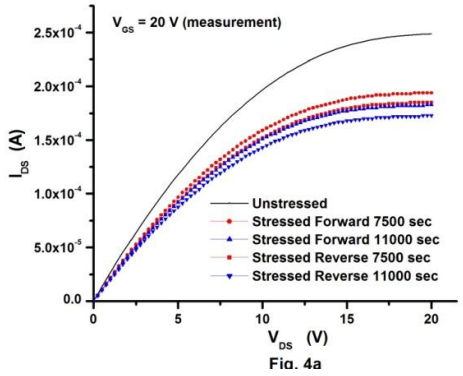

Fig. 4.4a. I_{DS} vs V_{DS} plot. Stressed in saturation mode. V_{GS}=20 V and V_{DS} = 20 V.

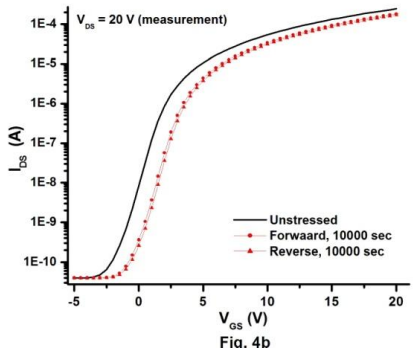

Fig. 4.4b. I_{DS} vs V_{GS} plot. Stressed in saturation mode.

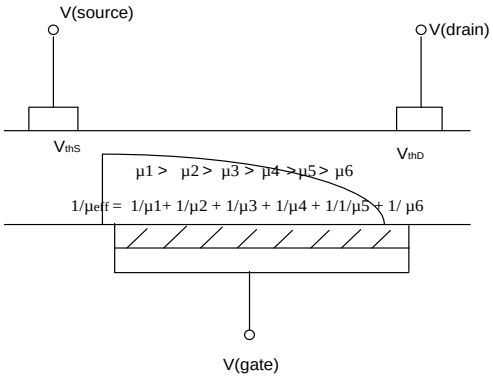

Fig. 4.5. Schematic showing effective mobility and V_{th} across channel in post stressed forward and reverse currents.

It has also been found out that mobility decreases with stress [37]. This reduction, is believed due to Coulomb scattering of channel electrons by trapped charge [49,50]. Fig. 4.6 shows the relative reduction in mobility with bias stress. Here μ_0 denote the mobility of the virgin device. The mobility shown here is linear mode mobility, calculated from transfer characteristics (V_{GS} = 20 V and V_{DS} = 1 V).

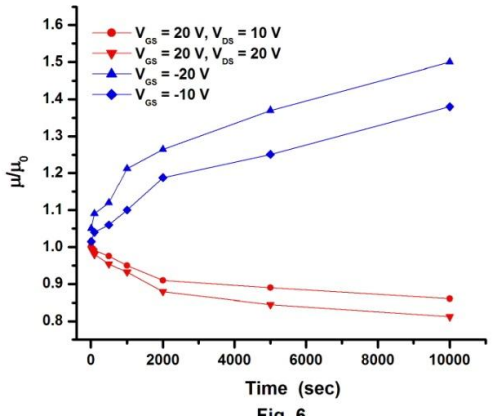

Fig. 4.6. Relative mobility change due to gate & drain bias stress with time (μ_0 is the virgin mobility).

The reduction in mobility is more pronounced in reverse mode than forward mode. The effective mobility is the average of inverse mobility from source to pinch off point [46]. As this pinch off point move towards the source with V_D increase, this average value will increase for forward operation and decrease for reverse operation. This is shown qualitatively in fig. 4.5. This is because region of low mobility is near the drain in forward mode (where there are fewer carriers) and near the acting source in reverse mode (where there are copious carriers). As a result of both these effects, the reverse current is lower

than the forward.

Fig. 4.7 shows the variation in V_{th} with V_{DS} over time. A good match between the measurements and the simple log model for ΔV_{th} is observed as in [39]. Usually a log fit curve is associated with charge trapping. A greater V_{DS} indicates greater lateral electric field, hence more charge trapping near the drain end and thus larger ΔV_{th}. This has been modelled by an empirical expression involving V_{DS} as discussed below.

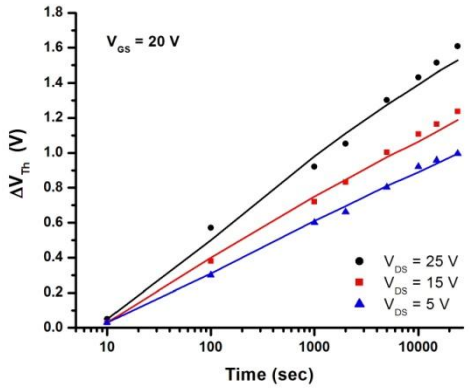

Fig. 4.7. Degradation of ΔV_{th} vs time and bias stress. Symbols indicate measured data.

The ΔV_{th} model as applicable to degradation in metal oxide TFTs due to charge trapping is given as [39]

$$\Delta V_{th} = r_0 \log\left(\frac{t}{t_0}\right) \tag{4.2}$$

where r_0 and t_0 are fitting parameters, with r_0 proportional to the trapped charge. The value of t_0 used here is 8.47 sec. Since trapped charge is proportional to V_{DS}, this is modelled using the following empirical relation

$$r_0 \propto 0.4e^{V_{DS}/25} \tag{4.3}$$

During the stress time the subthreshold swing also was found to degrade

somewhat, but recovered when relaxed. This suggests that such a degradation is mainly caused by pre-existing traps and not by state creation [51]. Also it was found out that the transfer characteristics of the TFTs tend to revert back to the virgin state when kept unstressed for extended period of time. This is shown in fig. 4.8. Such a reversal is consistent with charge trapping in insulator-semiconductor interface [38]. However, charge trapping in the oxide is generally considered irreversible [52], and hence it is believed that trapping mainly in the channel interface. In presence of defect creation, reversal of transfer characteristics does occur, but it usually requires some external stress [52-53].

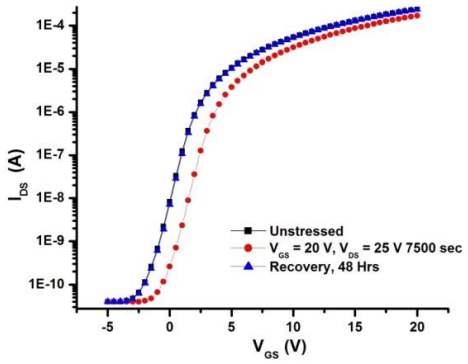

Fig. 4.8. Transfer characteristics recovery for V_{GS} =20 V and V_{DS} = 25 V stress.

For negative V_{GS} channel charge trapping is the dominant instability mechanism. Although some papers have reported no V_{th} shift with negative gate bias [39,40], evidence of negative V_{th} drift have been found in the present work [36]. Moreover varying the drain voltage seems to have no impact on the post stressed forward and reverse currents (shown in fig. 4.9a and 4.9b). This is because the charge trapping is mainly due to holes which are more or less uniformly distributed throughout the channel, independent of drain voltage. When

source-drain is reversed, since the holes are thermally generated there is no channel pinch off at high V_{DS}, and hence the current in both modes of operation remains constant, within experimental errors. Also the trapped holes screen the electrons and reduce Coulomb scattering, which is manifested in the form of mobility increase, as shown in fig.4.6. The negative V_{th} shift cannot be attributed to defect state creation (dominant in amorphous silicon), as such a mechanism only operates in the presence of mobile carriers [32], (absent in negative bias conditions) and is drain bias dependent.

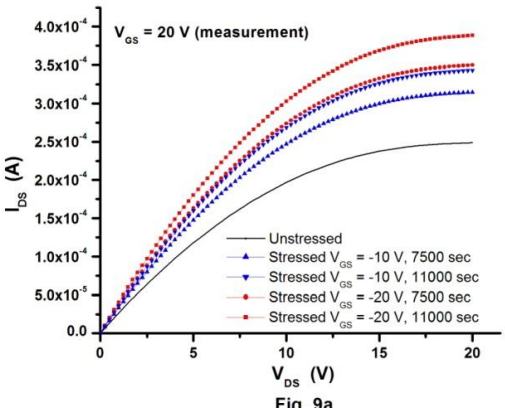

Fig. 4.9a. I_{DS}-V_{DS} characteristics. Negative bias stress.

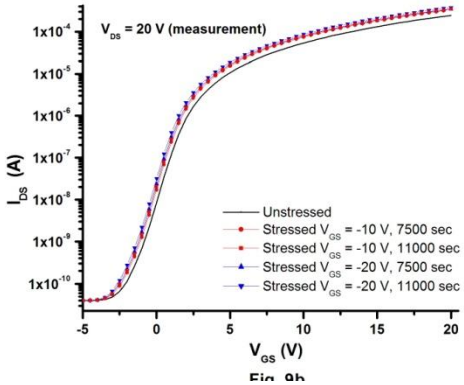

Fig. 4.9b. I_{DS}-V_{GS} characteristics. Negative gate bias stress. Both forward and reverse mode currents coincide.

4.4 Mechanical and Electromechanical Stress Testing of ZIO TFTs on Plastic

For these applications organic polymers like poly-ethylene napthalate (PEN) is used as deformable substrates. Thus, it becomes important to study the effect of mechanical stress on the electrical properties of the devices. Studies of mechanical stress on a-Si:H have been previously reported [54-56]. Although extensive studies of gate bias stress have been reported [36,37,57], to the best of author's knowledge mechanical stress of ZIO TFTs has not been reported yet.

The processed TFTs on PEN were cut into cylindrical shape and were later rolled around various radii tubes. All the measurements were made with a HP 4155B semiconductor parameter analyzer. Since all bending was done on cylindrical surfaces, the stress was essentially uniaxial. Tensile stress was obtained by bending the devices outward, while compressive stress was obtained by bending them inward. For electromechanical stress the flexible substrate with TFTs were rolled around the cylindrical surface and taped at the ends while taking the measurements. The largest and smallest diameters in our experiment were 11.43 and 1.52 cm, respectively. All I-V characteristics were measured with gate to source bias (V_{GS}) varying from - 20 to 20 V at a constant drain to source bias (V_{DS}) = 10 V and 1 V. The off state current (I_{off}) was calculated as the least current value for V_{DS} = 10 V. The linear mode mobility (μ) for both the virgin devices and stressed ones (V_{GS} = 20 V and V_{DS} = 1 V) was calculated from the following equation:

$$\mu = \frac{g_m (= \partial I_d / \partial V_{GS})}{(W/L) C_{ox} V_{DS}} \tag{4.4}$$

where g_m is calculated in the linear region and C_{ox} is the oxide capacitance per unit area. All measurements were taken in 3 sets and then averaged to reduce possible errors. All bending radii (R) are converted to % strain (ε) using the formula [58]:

$$\varepsilon = \left(\frac{1}{R}\right)\frac{d_f + d_s}{2}\left(\frac{\chi\eta^2 + 2\chi\eta_1 + 1}{\chi\eta^2 + (1+\chi)\eta + 1}\right) \tag{4.5}$$

where d_f and d_s are the corresponding thicknesses of the film and the PEN substrate. Y_f and Y_s are the respective Young's modulii. Values of Y_f and Y_s are 145 GPa [59] and 5.5 GPa [60]. Also $\chi = Y_f/Y_s$ and $\eta = d_f/d_s$.

Fig. 4.10 shows the change in subthreshold swing (S) and μ, when the TFTs were subjected to parallel stress, both tensile and compressive.

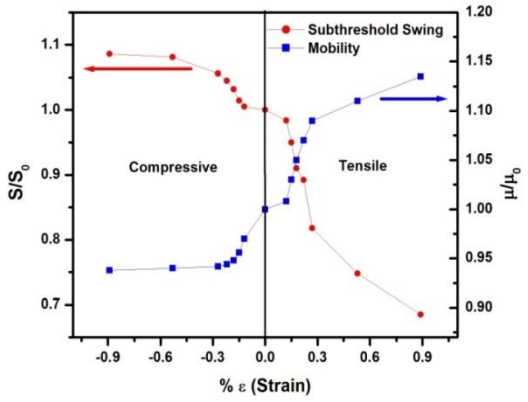

Fig. 4.10. Relative S and μ as function of applied strain (ε). V_{GS} varying from - 20 to 20V.

For both cases the same TFTs were bent for 5 minutes successively on cylindrical surfaces in descending radius and then probed on a flat surface in between the bending, to measure their electrical characteristics. For a given stress the change in the electrical parameters remained constant during the time of measurement (about 1 min). S_0 and μ_0 denotes the slope and mobility of the virgin

device. While S showed a reduction, μ showed an increase as the tensile stress increased by bending TFTs across smaller radii. Reverse changes were obtained for compressive stress. These effects are similar to that obtained for a-Si:H [54-57], although the magnitude of variation was found smaller in the present case.

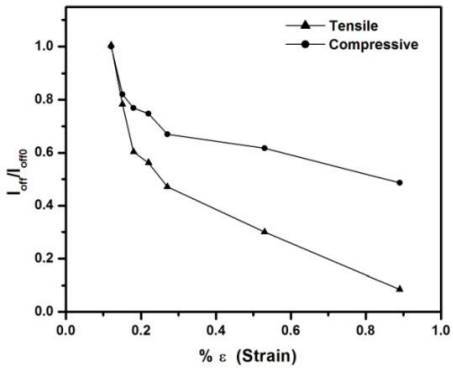

Fig. 4.11. Relative I_{off} due to tensile and compressive stress vs % strain (ε). V_{GS} varying from - 20 to 20 V at V_{DS} = 10V.

Fig. 4.11 shows the I_{off} for both compressive and tensile stress. Here I_{off0} denotes the off current for the virgin device. The I_{off} decrease is again much more for tensile stress than compressive stress. These changes are not permanent and the I-V characteristics have been found to revert back to the virgin characteristics, when left for unstressed in flat state for long period of time (*i.e.* about a day).

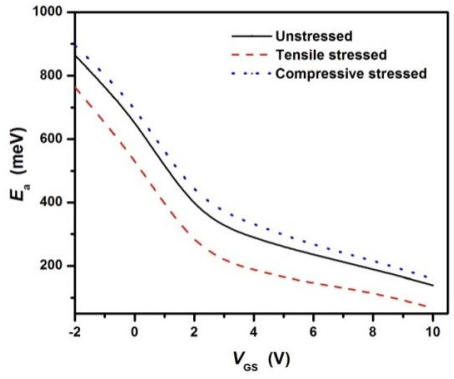

Fig. 4.12. Activation energy vs gate bias (bending diameter = 5.08 cm, ε = 0.27 %).

The cause of these changes is not clear and is possibly due to change in band-gap and/or defect creation at the interface [61]. Density of defect states (tail states) (D_{it}) was found to reduce (increase) with uniaxial tensile (compressive) stress [61-62] for a-Si:H. Density of defect states has been demonstrated to be inversely proportional to the slope of activation energy (E_a) w.r.t V_{GS} [62]. To measure E_a I_{DS}-V_{GS} curves for different temperatures were obtained, from 25°C to 125°C, at an interval of 25°C and plotted log(I_{DS}) vs 1000/T, for different V_{GS}. Fig. 4.12 shows the E_a as a function of V_{GS}, for virgin, tensile stressed and compressively stressed TFTs.

The slope of E_a was found to be more (less) for tensile (compressive) stress compared to the E_a for unstressed device, indicating a decrease (increase) in D_{it} for tensile (compressive). Increase in D_{it} increases S and reduces μ via charge trapping. Mobility in presence of charge trapping is given by [63]

$$\mu = \mu_0 \left(\frac{t_{free}}{t_{trap} + t_{free}} \right) \tag{4.6}$$

where t_{free} and t_{trap} are the average time spent by carriers in free and trap states respectively and μ_0 is the free electron mobility. Also smaller (larger) E_a implies a smaller (larger) Urbach energy (which is the valence band tail slope) [64], in general. Because tail states are associated with network disorders, such as bond angle and length distortion, there is a possible correlation of the conduction band tail state and Urbach energy, as shown for a-Si:H [65], *i.e.* a smaller (larger) Urbach energy implies smaller (larger) tail states. So measurement of E_a or Urbach energy confirms that tensile stress reduces defect states. This reduction in conduction band tail states implies higher (lower) linear electron mobility [66] by

(4.6). Hence is the observed results. Moreover it has been found that for a-Si:H the Urbach energy increases with decrease in bandgap [67], which in turn decreases with compressive stress [68]. Increased Urbach energy results in increased conduction band tail states, which in turn implies lower mobility. Thus reduction in bandgap might also be cause of mobility reduction under compression. Similar mobility reduction due to residual stress has also been observed for ZnO [69]. Also the above reasoning based on changes in density of defect states does not contradict the observation that devices recover at room temperature.

To confirm that indeed stress affects D_{it} and in turn S and μ, the following experiments were conducted. The TFTs were first stressed electrically with V_G = 20 V, grounding the source/drain on a flat surface [57]. In another experiment the same procedure was adopted; however in this case the TFTs are now held in bent position on a cylindrical diameter of 5.08 cm under tensile stress with simultaneous electrical stress. The current voltage characteristics were measured *in situ* conditions from 100 seconds onwards, without relaxing the device on a flat surface. The relative changes in S and μ are shown in Fig. 4.13.

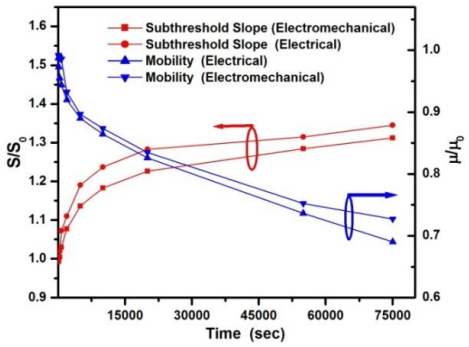

Fig. 4.13. Electrical and tensile electro-mechanical stress (dia = 5.08 cm, ε = 0.27 %).

Electrical stress induces traps which reduce the mobility [63] and increases S. Tensile stress reduces D_{it} and thereby improves both S and μ, as discussed in the previous sections. The overall effect is a reduction in change, when compared to only electrical stress being applied.

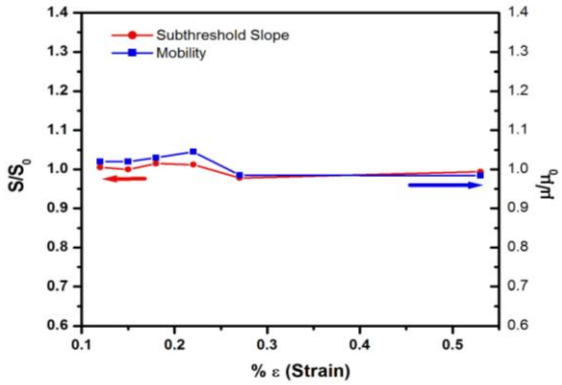

Fig. 4.14. Relative S and μ as function of the applied ⊥ strain (ε). V_{GS} from - 20 to 20 V.

A separate set of experiments were also conducted by orienting the wafers such that the resultant stress were perpendicular to the channel length. Both tensile and compressive stress was applied, as was done for parallel stress. However, the changes in S, μ and I_{OFF} were minor and within experimental error. Fig. 4.14 shows the results for tensile stress. Hence it was concluded that there is almost most no change under perpendicular stress. Similar results have also been observed for a-Si:H TFTs [58,70].

4.5 Summary

The results of both positive and negative gate bias stress in IZO TFTs were documented. Experiments using both positive and negative gate voltage bias along with varying V_{DS} point out the possible degradation effects under drain bias.

The measurements also showed that charge trapping is the possible degradation mechanism. Finally, the simple model presented in this article helped to quantify the impact of drain voltage stress on the TFTs under positive gate bias. ZIO TFTs were also stressed mechanically by bending them inward and outward around cylindrical structure of various radii. The subthreshold slope, mobility and I_{off} showed changes that depended on the direction and duration of the applied stress. Tensile stress showed a decrease in S and increase in μ. Compressive stress showed reverse changes. The reason is believed to be due to change in the band-gap and density of states with stress. Although these changes are similar to that observed in a-Si:H, further investigation is on way to evaluate the exact cause. However, none of the changes were catastrophic.

Chapter 5

PERFROMANCE AND LIMITATION of OP-AMPS in TFTs

5.1 Introduction: Need for Op-amp in TFT Technology

Although primarily targeted for active matrix display systems on glass, TFT circuits are making progress for more general applications on flexible substrates [71]. Examples include logic circuits and display drivers based on a-Si:H TFTs as discussed previously in Chapter 2. Recently, there has been considerable interest in flexible electronic systems such as flexible X-ray detectors to line litters, 'smart' medical bandages to monitor the healing of wounds and adaptive chemical sensors [72]. A key requirement for these applications is an analog block, which will serve as an interface between the sensor outputs and digital circuits. Op-amps are essential for this interface. A brief summary of analog designing in TFTs has already been presented in section 2.4 of chapter 2. In this chapter various op- amp topologies are analyzed, incorporating thin film transistors of various materials and determine the expected performance and feasibility of TFT operational amplifiers. The materials considered here are a-Si:H and ZnO as n-channel and pentacene as p-channel devices. In addition, the impact of the well known threshold voltage shift of TFTs with electrical usage on operational amplifier performance are examined.

The first design, described in this paper, is that of a classic two stage CMOS op-amp with a-Si:H n-channel transistors and pentacene p-channel transistors. Fig. 5.1 gives a micrograph of the fabricated chip with p-channel input

stage followed by n-channel 2nd stage, fabricated at low temperature of 180 °C. It is shown that the aforementioned design gives moderate gain and a relatively low unity gain frequency (UGF) due to the low mobility of both the pentacene and a-Si:H TFTs. In all of the subsequent simulated designs the a-Si:H were replaced with ZnO n-channel transistors. However, because of the incorporation of pentacene p-channel devices, the performance is still below par with only a moderate unity gain frequency. The final topology consists of an all n-channel enhancement-depletion op-amp. This configuration gave a gain of 100dB and a unity gain frequency of over 1MHz.

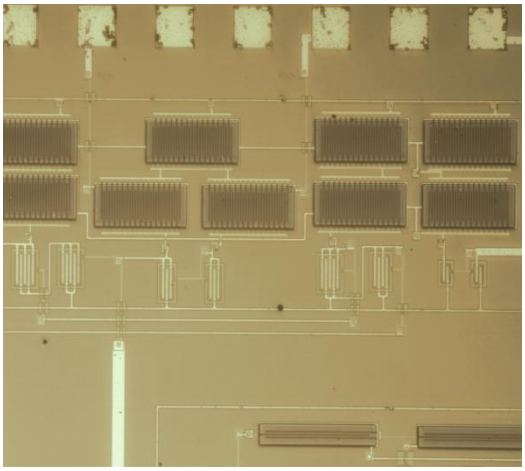

Fig. 5.1 p-channel input 2 stage op-amp fabricated with amorphous silicon and pentacene TFTs.

5.2 Design of CMOS Op-Amp in TFTs

5.2.1 Two stage Miller Compensated

Fig. 5.2 shows the classic design of a two stage compensated CMOS operational transconductance amplifier (OTA) with Miller capacitance and nulling resistor for both n-channel input and p-channel input differential pairs.

Consider first the p-channel input differential pair followed by an n-channel cascoded common source amplifier (Fig. 5.2a). The open loop gain and UGF (in Hz) of the classic two

stage configuration can readily be derived

$$Gain = \left(\frac{g_{mp3} g_{mn6}}{g_{dsp3} + g_{dsn4}} \right) \left(\frac{g_{dsp8} g_{dsp9}}{g_{mp8}} + \frac{g_{dsn7} g_{dsn6}}{g_{mn7}} \right)^{-1} \tag{5.1}$$

and

$$UGF = \frac{g_{mp3(stage1)}}{2\pi C_M} \quad . \tag{5.2}$$

where g_{mp} and g_{mn} denote the transconductance of the p-channel and n-channel devices respectively and g_{dsp} and g_{dsn} denotes the output conductance of the devices respectively. Here C_M denotes the Miller capacitance and $g_{mp3(stage\ 1)}$ denote the transconductance of the first stage input TFT (in this case of a p-channel device).

Using a-Si:H for the n-channel devices and pentacene for the p-channel devices, an optimized design was achieved for the CMOS topology with p-channel input. The power supplies were ± 20 V, driving a 20 pF load, and a phase margin of 55^o. All simulations were done with HSpice. The resulting simulated DC gain was 58 dB with a unity gain frequency of 7 kHz, limited by the low mobility, and hence the transconductance g_m, of both a-Si:H and pentacene TFTs. The nulling resistor has been chosen, in all our designs to have $R_z = \frac{1}{1.2 g_{m1}}$, assuming $R_Z >> g_{m2}$ (transconductance of second stage input TFT) [73]. Fig. 5.3a shows the simulated response of the OTA in Fig. 5.2a. Based on the design and simulations the topology of Fig. 5.2a (Fig. 5.1) was fabricated, with a class A output buffer to drive resistances of 100 kΩ and cap values upto 100 pF, typical

of electrochemical cells for which it is intended. Fig. 5.3b shows the gain response of the fabricated op-amp. The power supply used was reduced to ± 15 V as the TFTs could withstand a max supply rail of 30 V. Table 5.1 gives the detail specifications.

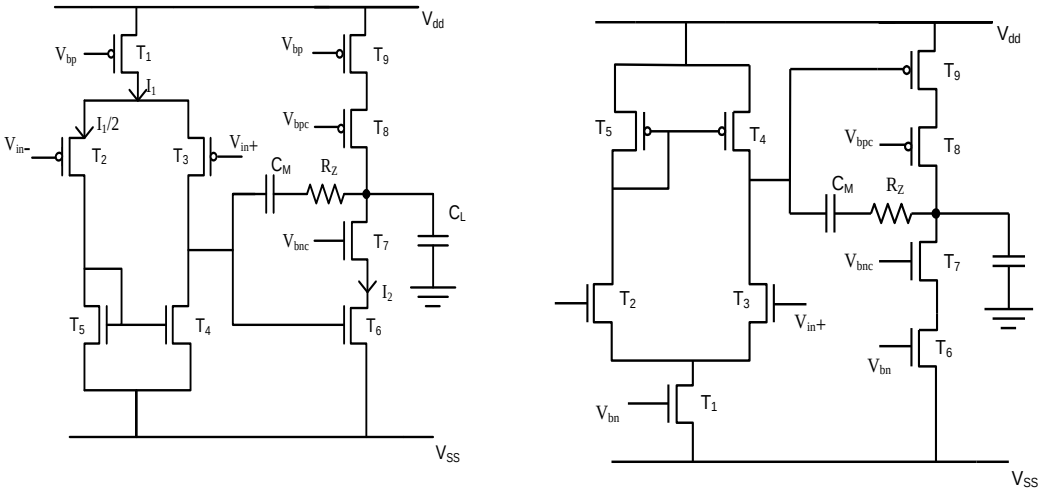

Fig. 5.2a) 2 stage Miller compensated OTA with pMOS 1st stage; b) 2 stage Miller compensated OTA with nMOS 1st stage.

Unlike the op-amp in ref [19], an external source to bias the different transistors was not used. Instead biasing circuits were used for the fabricated op-amp using DC current source Also due to a CMOS structure, the gain is higher than in [19], although the UGF is considerably lower due to slow pMOS TFTs.

DC gain	49 dB
Unity Gain Frequency	4.5 kHz
Output Swing	±8.2 V
Power Consumption	8.4 mW
Area Consumption (including pads)	4 mm^2
Input Common mode Range	±10.6 V
Offset Voltage	0.34 V
R_z and C_M	31 kΩ and 61 pF

Table 5.1. Fabricated op-amp characteristics.

For the same topology but with n-channel input device (Fig. 5.2b), the simulated bandwidth is even smaller, giving a UGF of only 2 kHz, the gain remaining almost the same. The results are summarized in Table 5.2. For all subsequent simulations ±20 V power supplies have been used, maintaining a power consumption of 9 mW, driving a load capacitance of 20 pF maintaining a phase margin of 55^{o}.

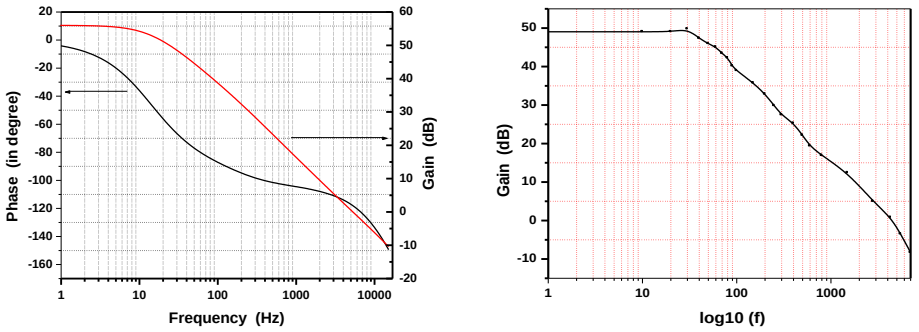

Fig. 5.3a) Simulated gain and phase vs frequency response; b) Measured gain response of fabricated op-amp.

It is evident that the p-channel input design gives a larger unity gain frequency than the n-channel input design. The open loop gain, however, remains invariant for both topologies (as can be seen in (1)). This phenomenon can readily be explained by the position of the non-dominant pole (p_2). To maintain a significant phase margin, the UGF should be placed at certain fraction of the second non-dominant pole frequency to maintain a given phase margin. If the UGF is at a given fraction 'k' of p_2, (where k determines the phase margin) then the following relation exists

$$\frac{g_{m1}}{2\pi C_M} = k\frac{g_{m2}C_M}{2\pi(C_{in}C_M + C_{in}C_{out} + C_M C_{out})} \tag{5.3}$$

where subscripts 1, 2 denote the stage number and C_M, C_{in} and C_{out} denote the input and output capacitance of the second stage respectively. (C_{out} includes the load capacitance.) Eq (5.3) can be solved for C_M as

$$C_M = \frac{1}{2k}\frac{g_{m1}}{g_{m2}}(C_{in}+C_{out}) + \sqrt{\frac{g_{m1}^2}{4k^2 g_{m2}^2}(C_{in}+C_{out})^2 + \frac{g_{m1}}{kg_{m2}}C_{in}C_{out}} \quad .(5.4)$$

Substituting C_M back in equation (5.3) an expression for UGF in terms of the device parameters is given as

$$UGF = \frac{g_{m2}}{\frac{1}{2k}(C_{in}+C_{out}) + \frac{1}{2}\sqrt{\frac{1}{k^2}(C_{in}+C_{out})^2 + \frac{4g_{m2}}{kg_{m1}}C_{in}C_{out}}} \quad .(5.5)$$

From equation (5.5), it is clear that a low g_{m2} or transconductance of the second stage device gives a low UGF. Also, it is clear that with a higher g_{m1}, the denominator becomes smaller, giving a boost in UGF. Hence using p-channel first stage and an n-channel second stage gives a much improved UGF because the higher mobility device is setting the position of the non-dominant pole. The gain, however, remains the same as given in equation (5.1). Furthermore, equation (5.4) shows C_M is larger for an n-channel first stage, due to higher g_{m1}/g_{m2} ratio and/or higher size of second stage (needed to obtain high g_{m2}) reducing the slew rate.

All subsequent designs used zinc oxide (ZnO) n-channel transistor with device model parameters extracted from measured transfer characteristics. Both OTAs in Fig. 5.2 were re-designed using ZnO n-channel and pentacene p-channel TFTs. Both the p-channel and n-channel input designs gave a much higher gain of 110dB. The p-channel input design had a unity gain frequency of 236 kHz whereas the n-channel input design had a UGF of only 24 kHz. The complete results with power consumed and area are given in Table 5.2.

A two stage design with the second stage being a simple common source amplifier instead of being cascoded, is especially useful as it achieves the same signal swing at a much lower area (a higher over-drive voltage can be tolerated for individual transistors at the expense of smaller widths) and also reduces the capacitance, reducing C_M and thus gives a better UGF and slew rate. Furthermore, this approach eliminates the extra cascoded pole thereby enhancing the UGF even further. This is evident from the two stage CMOS design without cascode, which gives an UGF of 266 kHz for the p-channel input and 68 kHz (Table 5.2) for the n-channel input. However, without cascode, the gain decreases by about 30 dB.

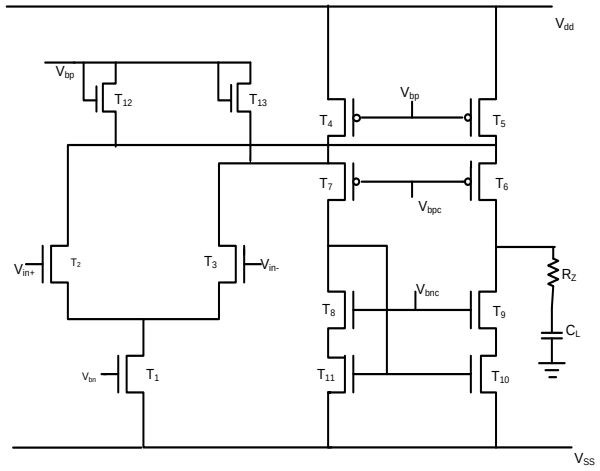

Fig. 5.4 Folded cascode nMOS input OTA.

5.2.2 Single stage Folded Cascode

The Miller capacitance in a multistage OTA limits the bandwidth. To avoid such a bandwidth loss, a single stage folded cascode OTA was also designed, both with n-channel and p-channel inputs with the same criteria as the topologies discussed above, i.e. phase margin of 55^o, swing of ±12 V and power consumption of 9 mW (Fig. 5.4). An n-channel input gives much better frequency

response than the p-channel input due to higher mobility, hence achieving a gain and bandwidth of 81dB and 395 kHz respectively (Table 5.2). For the case of the two stage OTA, where g_{m2} dictated the position of the non-dominant pole, the p-channel input had higher UGF than n-channel input as described previously. For the single stage folded cascode, the non dominant pole at the folding nodes is at a much higher frequency and so the UGF is solely determined by g_{m1}. Thus, for a p-channel input, the response is poor with a UGF of only 66 kHz, as the mobility and hence g_m of the input p-channel is extremely low. However, the overall performance in n-channel input is still limited by the low mobility of the two large p-channel current sources, T_4 and T_5. These large devices contribute to significant capacitance, which reduces the non-dominant pole frequency and hence the UGF, to maintain stability. An increase in the size of T_6 and T_7 increases the g_m required to increase the non-dominant pole frequency but this would also increase the capacitance at the nodes, bringing little benefit. As it is a single stage configuration, it has a lower gain.

5.3 Limitation of CMOS Op-amp:All nMOS Enhancement-Depletion Op-Amp

From the above discussion it is quite clear the bottleneck in all the above topologies is the pentacene p-channel TFTs. Although moderate UGF could be achieved with them, none of them come close to matching the specifications of the earliest monolithic silicon OPA 741 from Fairchild [74]. In this section the design methodologies of an all n-channel op-amp is outlined along with their advantages over CMOS structures. Although design of all n-channel op-amps has almost become a lost art due to unavailability of depletion mode devices in

modern CMOS processes, through simulations it is shown that it gives the best performance in the present case.

Design of all n-channel op-amps requires both enhancement and depletion mode devices for adequate gain [75-77]. Both enhancement (positive V_{th}) and depletion (negative V_{th}) mode ZnO TFTs have been fabricated successfully [15,78]. The gain enhancement with depletion mode loads is even better for TFTs than for silicon MOS devices, as in the latter, the output conductance is dominated by body biasing, which is absent in TFTs. In TFTs, the output conductance is solely determined by the channel length modulation and hence, open loop gain is much higher.

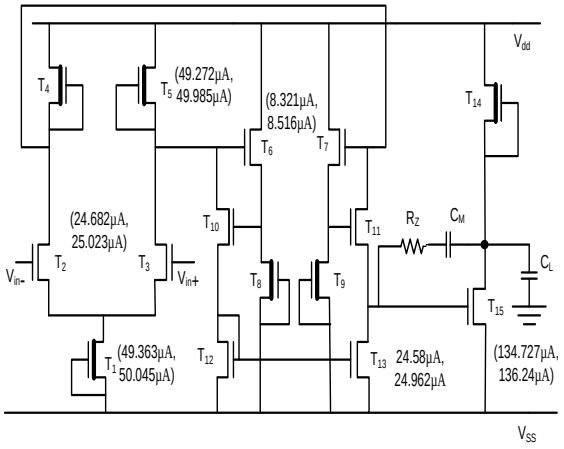

Fig. 5.5 All n-channel enhancement-depletion topology.

Fig. 5.5 shows the topology of the enhancement-depletion OTA, which is actually the self biased version of [75]. Since there is no p-channel TFT, a proper biasing of the corresponding common source stage is achieved through a level shifter, implemented using T_6-T_{13}. Also the current through T_4 (or T_5) should be made greater or equal to T_1 so as to maintain the slew rate. But if a large current is

allowed to flow through T_4 (or T_5), it decreases the gain. So the current through T_1, T_4, T_5 is choosen to be almost the same. Similarly the current through T_{14} should be optimized to meet the slew rate requirement, as well as give sufficient gain. One of the modifications of the circuit from [75], is that all the constant current sources (T_1, T_8, T_9 and T_{14}) are implemented by depletion mode n-channel TFTs, making the circuit a self biased one. As a result, no power is consumed by the biasing circuitry. Self biasing was difficult in silicon op-amps [75-77] using lower power supplies, as a depletion mode device requires a threshold voltage drop to keep it in saturation, thereby reducing the swing. Also, the power supply used is ±18 V for this all n-channel topology to drive more current for the same power and hence achieve a better UGF (this is the minimum supply to maintain ±12 V swing). This reduction, however, does not affect signal swing, as all TFTs being n-channel ZnO, have higher mobility (and hence small V_{OV}), subsequently lower supplies can be used. Since, this topology consists of only ZnO, it achieves a gain of 100dB and a UGF of greater than 1MHz.

The OPA 741 from Fairchild [74] achieved a gain of 100dB, a unity gain frequency of 1.1 MHz and a signal swing of ±12V at a power supply of ±15 V. Although with the current all nMOS enhancement-depletion topology the 741 specifications have not reached, the results nevertheless look promising.

Design Type	DC Gain	Unity Gain Bandwidth	Power	Miller Cap	Null Resistor	Area (mm^2)
2 stage CMOS OTA with n-channel input and cascoded 2nd stage (a-Si:H and Pentacene)	60dB	2kHz	8.97mW	40pF	35 kΩ	2.657
2 stage CMOS OTA with p-channel input and cascoded 2nd stage (ZnO	110dB	236kHz	8.9mW	20pF	21kΩ	1.237

and Pentacene)						
2 stage CMOS OTA with n-channel input and cascoded 2nd stage (ZnO and Pentacene)	111dB	24.2kHz	8.84mW	200pF	50.5kΩ	2.168
2 stage CMOS OTA with p-channel input and simple 2nd (ZnO and Pentacene)	81dB	266kHz	9.07mW	16pF	21kΩ	0.438
2 stage CMOS OTA with n-channel input and simple 2nd (ZnO and Pentacene)	80dB	68kHz	8.9mW	105pF	48kΩ	0.435
Single stage n-channel Folded Cascode (ZnO and Pentacene)	80dB	392kHz	8.84mW			0.788
Single stage p-channel Folded Cascode (ZnO and Pentacene)	73dB	66kHz	8.9mW			1.543
2 stage all n-channel Enhancement-Depletion (ZnO)	100dB	1.07MHz	9.05mW	24pF	11kΩ	0.813

Table 5.2. Performance Characteristics of different op-amp topologies in different material systems.

5.4 Impact of TFT Aging on Op-amp Topologies

It has been reported widely in the literature that TFTs degrade with gate bias stress and time. The threshold voltage degradation has been shown to follow the stretched exponential equation (2.2) [14], repeated here for convenience.

$$\Delta V_{th}(t) = (V_{GS} - V_{th})\left[1 - \exp\left\{-\left(\frac{t}{\tau}\right)^{\beta}\right\}\right] \quad . \tag{5.6}$$

where τ the time constant [79] and β in (5.6) is a fitting parameter. The corresponding β and τ values for a-Si:H and pentacene are 0.53 and 0.23 and $5x10^4$ and $5x10^8$ respectively as derived from our prior measurements [13,71]. These stress data of TFTs were obtained by measuring the I-V characteristics at periodic intervals of time, under a constant DC voltage at the terminals. The I-V characteristics were measured with a Keithley 4200-SCS. Although equation (5.6) was first formulated for a-Si:H and organic TFTs, it has been found to have a

good fit for Zinc Indium Oxide [40]. The values of τ and β used this paper for ZnO were extracted from our data and are $1.873x10^9$ and 0.25, respectively (shown in Fig. 5.6).

Using equation (4.6) and the above parameters for a-Si:H, pentacene and ZnO, the lifetime of the op-amp was simulated and predicted. The results for p-channel input op-amp biased with a constant g_m biasing circuit, and simulated p-channel input two stage ZnO/pentacene op-amp (also biased with g_m bias) are shown in Table 5.3. Results indicate that the I_{DS} of the TFTs increase with degradation for a continuous operation of 100000 seconds (roughly 1.5 day). Fig. 5.7 shows a modified g_m biasing circuit. For now, consider the portion within the dashed box, which is the general constant g_m biasing circuit used presently.

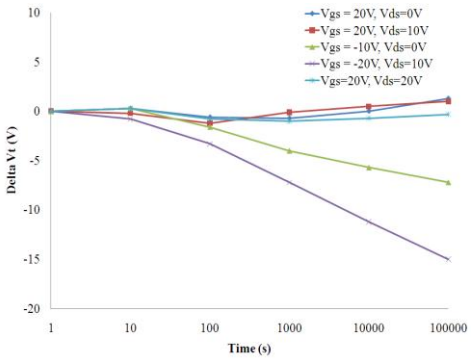

Fig. 5.6 Change in V_{th} with constant DC stress of ZIO [62].

Two stage Miller compensated CMOS op-amp with p-channel inputs followed by n-channel cascode stage (I_1 and I_2 refer to branch currents in Fig. 3)	a-Si:H/pentacene op-amp		ZnO/pentacene op-amp (biased with g_m biasing circuit)	
	Initial	Final (100000 sec)	Initial	Final (100000 sec)
I_1	79.26 µA	119.82 µA (g_m bias) 73.5 µA (DC current)	86.22 µA	93.87 µA

I_2	109.27 μA	165.84 μA (g_m bias) 102.3 μA (DC current)	118.689 μA	127.337 μA

Table 5.3. Simulated degradation of op-amps in a-Si:H and ZIO TFTs, both for g_m and DC current source.

results of the degradation are summarized in Table 5.3, where I_1 and I_2 are the leg currents shown in Fig. 5.2a. This increase is a result of transistors T_1 and T_2 aging differently in Fig. 5.7. T_1 and T_2 have different gate to source voltages which lead to different threshold voltages over time. For a constant g_m biasing circuit, the V_{GS} of the T_1 and T_2 at any time t are related by

$$V_{GS1}(t) = V_{GS2}(t) + I_{DS}(t)R, \tag{5.7}$$

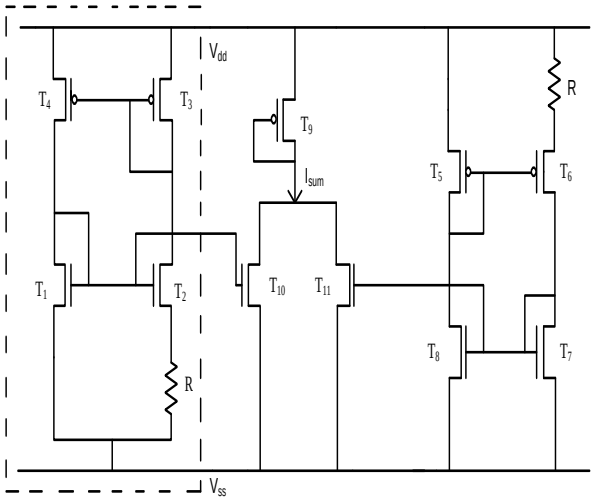

Fig. 5.7 Modified constant g_m biasing circuit.

where R is the resistance in Fig. 4.7. For TFTs in saturation, equation (5.7) can be written as

$$\sqrt{\frac{2I_{DS}}{\mu(W/L)_1 C_{ox}}} + V_{T1} = \sqrt{\frac{2I_{DS}}{\mu(W/L)_2 C_{ox}}} + V_{T2} + I_{DS}R \tag{5.8}$$

.

Because initially $V_{GS1} > V_{GS2}$, it is clear that V_{T1} degrades more than V_{T2} following equation (5.6), such that the difference (V_{T1} - V_{T2}) increases with time. This in turn, from equation (5.8), implies that I_{DS} in both legs of the constant g_m circuit

increases, resulting in an increase in the gate overdrive voltage (V_{OV} = V_{GS}- V_{th}). An increased V_{OV} results in reduced signal output signal swing for the op-amp. Also increase in I_{DS} results in further increase in V_{GS1}-V_{GS2} and this effect feeds on itself. A simple analytical expression to predict the evolution of I_{DS} with time can be derived as follows. From equation (5.7),

$$\sqrt{2I_{DS}}\,(\sqrt{M_1}-\sqrt{M_2}) = I_{DS}R - \delta V_T \tag{5.9}$$

where $M_{1,2} = \left(\mu (W/L)_{1,2} C_{ox}\right)^{-1}$ and $\delta V_T = V_{T1} - V_{T2}$. Now, for a constant g_m bias circuit $M_1 = 4M_2$. So equation (5.9) can be solved for I_{DS} as

$$I_{DS}(t) = \frac{\delta V_T}{R} + \frac{M_2}{R^2} + \sqrt{\frac{M_2^2}{R^4} + \frac{2\delta V_T M_2}{R^3}}\,. \tag{5.10}$$

Note that equation (5.10) reduces to g_{m1} =1/R when δV_T = 0. An expression for δV_T can be derived as

$$\delta V_{th} = V_{th} + \Delta V_{th1} - (V_{th} + \Delta V_{th2})\,. \tag{5.11}$$

Here $\Delta V_{th1,2}$ denote the change in V_{th} (initial threshold voltage of both devices) due to gate bias stress. Substituting expression for $\Delta V_{th1,2}$ from equation (5.6),

$$\delta V_{th} = (V_{GS1} - V_{GS2})_{initial}\, f(t) = I_{DS(initial)} R f(t) \tag{5.12}$$

where $f(t) = \left[1 - \exp\left\{-\left(\frac{t}{\tau}\right)^{\beta}\right\}\right]$. Substituting $\Delta V_{th1,2}$ expressions from equation (5.12), an expression for the final I_{DS} is derived as

$$I_{DS}(t) = (1/2 + f(t)) I_{DS(initial)} + \sqrt{\frac{I_{DS(initial)}^2}{4} + I_{DS(initial)}^2 f(t)}\,. \tag{5.13}$$

It is clear that the increase in I_{DS} with time is proportional to the initial I_{DS}. The degradation of the two stage fabricated op-amp with p-channel input, with respect to power consumed and output signal swing over time are shown in Fig.

5.8. The power consumption increases due to an increase in the current. Also an increase in the current, with other device parameters remaining the same, implies an increase in the gate overdrive (V_{OV}), resulting in lower output swing. This also suggests, to minimize the degradation, initial I_{DS} should be as small as possible.

Equation (5.13) predicts that the rate of increase of I_{DS} is proportional to the initial value. Since initial I_2 (I_{DS} in second stage) is larger in the second stage (to make a stable amplifier as seen from equation (5.5)), it increases more than I_1. Hence g_{m2} increases more than g_{m1}. Thus, other elements remaining same, from equation (5.5), the UGF increases. Simultaneously, due to greater current flowing through the circuit, the gain reduces. Also, since g_{m2} increases with time, the nulling resistor no longer matches g_{m2}, thereby decreasing the phase margin and reducing stability. This can be, of course, compensated by the technique of multipath zero cancellation [80]. With this technique, a feed-forward transconductance path is added, which provides an out of phase small signal current to cancel the feed forward small signal current through the Miller capacitance. For this to happen, g_{m1} has to be equal to the transconductance of the feed forward path (g_{mf}). Since g_{m1} degrades with gate bias stress, g_{mf} will also degrade in a similar fashion and hence the stability will not be affected.

5.4.1 Novel Basing Schemes to Retard Degradation

A novel biasing scheme to retard such degradation is shown in Fig. 5.7. It can be seen that increase in I_{DS} is due to differential aging of transistors T_1 and T_2 and that ΔV_{th} increases with time for n channel TFTs (i.e. it becomes harder to turn on the TFTs). A similar decrease in I_{DS} is brought about by differential aging

of p-channel TFTs (T_5 and T_6) using the constant g_m biasing scheme shown in the right side of Fig. 5.7. This is due to increasingly negative ΔV_{th} for pentacene p-channel TFTs [13] (i.e. it becomes easier to turn on the TFTs). As a result if I_{DS} is kept in both the left and right g_m biasing scheme same, the sum I_{sum} flowing in T_9 will be more or less constant. It won't be exactly constant as the rate of degradation ($f_n(t)$ and $f_p(t)$ for n and p channel respectively) are different for the different materials. If $f_n(t) > f_p(t)$, as for a-Si:H and pentacene, I_{sum} will increase slightly, although not as much when only n-channel g_m biasing scheme is available. On the other hand if $f_p(t) > f_n(t)$, as for ZnO and pentacene, I_{sum} decreases slightly. However, because current decreases in the p-channel g_m biasing topology, this type of architecture is valid until the current decreases to very low value in the right side of Fig. 5.7. In Fig. 5.8 the dashed red line shows the simulated increase in power using this type of biasing circuit for a-Si:H/pentacene OTAs.

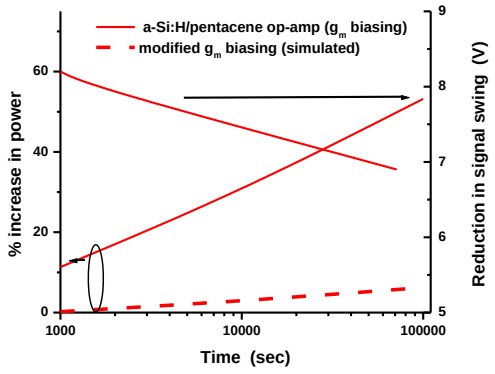

Fig. 5.8. Increase in power and reduction in signal swing using constant g_m biasing circuit, as the TFTs age with electrical usage. The red dashed line shows reduced degradation for a-Si:H/pentacene using the novel bias circuit.

Another way to retard the degradation is to use a constant DC current bias and replicate it using current mirror to bias all the TFTs [81]. Using constant DC biasing current maintains same current in each branch. This implies the V_G of individual TFTs adjust to maintain the same overdrive V_{GS}-V_{th}. With reference to fig. 5.2, it is seen that the only two transistors which are fed with external V_G are the input transistors. As a result the degradation is reduced. This reduction in aging is shown in Table 5.3 for our now biased with a DC current source of 3 µA. While there is no control over the V_G of these transistors, the overdrive can be reduced by making the TFTs large. Since degradation depends on overdrive, the aging of the devices are reduced to a great extent using this scheme if TFTs are made larger in size.

An enhancement depletion OTA is expected to have much better lifetime than the other topologies. Reports in literature point to gate bias stress as the primary source of V_T degradation As a result, depletion mode TFTs with lower gate bias are found to degrade much less, as recently seen for depletion mode a-Si:H [82]. Although depletion mode ZnO TFTs have been reported, their V_T degradation has not been investigated thoroughly [14,51]. Nonetheless, it is expected to be extremely slow (considering that the degradation of enhancement mode only is slow). Moreover, in our design, since V_{GS} is zero, the TFTs are expected to act as constant current sources for a very long time, without any significant degradation (as long as the V_{DS} of the depletion mode TFTs remain large enough to keep it in saturation and thus make it act as a constant current source). Assuming the depletion mode TFTs do not degrade much, the initial and

final current values (after 1 million seconds of continuous operation) in Fig. 5.5 remain almost the same.

5.5 Summary

A couple of different op-amp topologies were simulated to find out the best choice to be used as a buffer in electrochemical cell. A 2 stage pMOS input op-amp was fabricated in a-Si:H/pentacene CMOS topology. The op-amp achieved a gain of 54 dB and a UGF of 7 kHz. Based on the simulations, the all n-channel enhancement-depletion OTA showed the best possible performance for building reliable op-amps. It gave the best combination of gain, unity gain frequency and signal swing, while consuming the same power as the CMOS architectures and being much more reliable. A novel biasing circuitry was constructed with both nMOS and pMOS β multiplier circuits to retard the degradation, if a DC source was not available as an alternative.

Chapter 6

DIGITAL TO ANALOG CONVERETERS in TFTs

6.1 Introduction

The need for data converters in TFTs have already been discussed in chapter 2. In this chapter the design of a 7 bit switched capacitor DAC in a-Si:H is presented. Although a 6 bit DAC has already been reported [20] and discussed in section 2.4 of chapter 2, it uses organic TFT, which suffers from severe matching problem [20]. This necessitates the use of calibration techniques, complicating the circuit as a whole. Moreover, it is widely known that most organic semiconductors degrade in contact with moisture and air [34,35]. A-Si:H, on the other hand, has much better matching properties. Also a-Si:H being a mature technology in the flexible electronics industry [71], it is easy to incorporate it in upcoming applications. A 5 bit current steering all nMOS DAC build in a-Si:H TFTs is discussed next. Unlike the switched capacitor architecture, the current steering DAC do no require an external buffer at the output.

6.2 7 Bit Switched Cap nMOS DAC in a-Si:H TFTs

In this work, the DAC uses only n-channel a-Si:H TFTs in switched capacitor array structure. The TFTs are fabricated on glass and polyethylene napthalate (PEN) at a temperature of 180ºC. Since TFTs implemented as switches are most immune to aging effects and device variation, the DAC used switched capacitor architecture.

6.2.1 DAC Architecture

Various DAC architectures exist, using resistor and capacitor ratios, current steering and switched capacitor techniques. For a resistor DAC, the number of resistors increases exponentially with the number of bits. This however can be solved with the R-2R architecture. A limit of the R-2R DAC is that the input-output characteristics is not intrinsically monotonic [83], and is highly sensitive to the resistor mismatch, especially the MSB resistors. On the other hand, current steering DACs also suffer from similar mismatch problem. For an n-bit DAC the maximum allowed mismatch is given by [83]

$$\frac{\Delta I}{I} < 0.39 \times 2^{-n/2} \ . \tag{6.1}$$

Thus for a 7 bit DAC the mismatch allowed is only 3.44% for a DNL of ±1 LSB. Fig. 5.1 shows the matching of I_{DS} obtained with the a-Si:H TFTs at FDC. Assuming the mismatch to be Gaussian, 99.7% of the TFTs fall within ±7% of device variations. The wafer under measurement is an array of 240x320 TFTs. Although the present process is quite uniform, to avoid the constraints of current steering architectures (6.1) and device aging effects of a-Si:H TFTs. current steering architectures are not used.

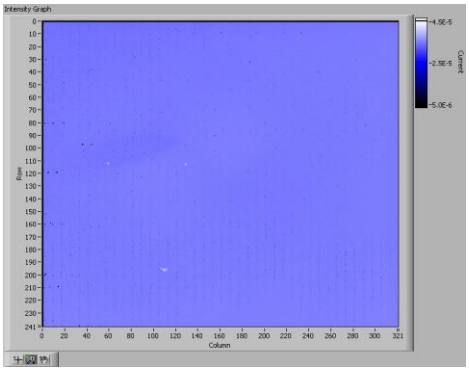

Fig. 6.1 Distribution of I_{DS} across the wafer from FDC.

A basic resistor DAC architecture is shown in Fig. 6.2a. However, as discussed earlier, it is difficult to directly obtain large resistors sizes with good accuracy in TFT technology. As the result the resistors in the proposed DAC circuit were emulate using a capacitor array in geometric progression and n-channel devices as switches [84], as shown in Fig. 6.2b. During charging (ph1), each of the ratioed capacitors are charged to either V_{ref} or discharged to ground, depending on the logic represented by the individual bits. During evaluation there occurs a redistribution of charge among the ratioed capacitors and the output cap, settling the output voltage at the correct analog value. An advantage of this architecture, compared with the capacitive divider DAC, is that it offers the isolation between the output and the input during the evaluation (ph2).

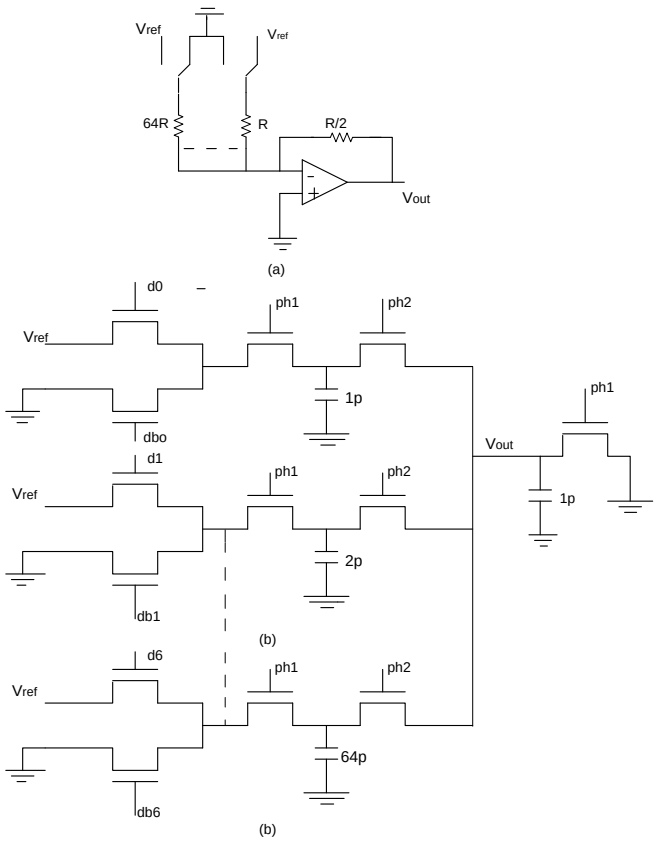

Fig. 6.2. Circuit Schematic of 7 bit switched cap DAC.

A second advantage is that the performance of the DAC circuit does not directly rely on the TFTs since they only act as switches, as long as the TFTs can provide enough On/Off resistance ratio. It has been seen that the TFT devices offer significantly high on/off resistance ratio compared with typical silicon device and therefore very suitable for the switched capacitor circuit implementations. Although the leakage current in a a-Si:H TFTs are negligible, nevertheless at very slow speeds of operation (e.g. DC condition), there can be potential charge leakage from the output capacitor. To prevent such leakage, the capacitors are refreshed every clock cycle as shown in the architecture in Fig. 5.2b.

The most critical device in the proposed DAC circuit is the capacitor array. But because of their simple geometry, large allowable size and high immunity to aging effects, capacitor match has been easily achieved without calibration on TFT process. In the present design an array of unit sized caps is used to achieve good matching. The area of each unit cap was about 5800 μm^2. The capacitor was made with Al as the top plate, molybdenum as the bottom with Si_3N_4 as dielectric, having a thickness of 400nm.

6.2.2 Speed of Operation

A transistor's unity gain frequency (f_t) is a measure of how fast it can operate and is given by [85]

$$f_t = \frac{g_m}{2\pi C_C} = \frac{\mu}{2\pi L\left(2L_{overlap} + \frac{2}{3}L\right)}(V_{GS} - V_{th}) \ . \qquad (6.2)$$

Thus from (2) it is clear the f_t depends on both device parameters and process parameters The typical values in our process are L = 11 µm, $L_{overlap}$ = 11 µm, V_{GS}

= 20 V, V_{th} = 1.2V and μ = 0.8 cm^2/Vs. With these, f_t is evaluated as 682.5 kHz, which is about 225 times higher than that for organic semiconductors [20].

Also the other constraint remains that the transistors must be able to deliver (or extract depending on the logic represented by the bit) the required charge to the corresponding capacitors during ph1 (i.e. half the clock cycle T_{clk}). The time is maximum in case of the MSB which has to charge 64 pF in ph1. The time required to charge this cap at a W/L=22, for the MSB TFT is approximately given by

$$t = \frac{CV_{ref}}{I_{avg}} \tag{6. 3}$$

where

$$I_{avg} = \frac{\mu C_{ox}}{V_{ref}} \frac{W}{L} \int_0^{V_{ref}} (V_{logic} - V_T - \tfrac{1}{2}(V_{ref} + V))(V_{ref} - V)dV . \tag{6.4}$$

Substituting appropriate values t is 60 µs, which is well below $T_{clk}/2$, even at 500Hz. This 't' sets the upper limit of operation to about 8.5 kHz.

6.2.3 Experimental Results

The DAC uses 8 capacitors in geometric progression of 2 (e.g. 1,2,..,64pF) and a single capacitor of 1pF to store the output charge. Each capacitor is built from unit size capacitors of 1pF. The DAC in total contains 28 n-channel a-Si:H TFTs. All TFTs have lengths of 11 µm. Fig. 5.3 shows the complete layout of the 7 bit DAC.

A voltage of 20 V has been used for logic '1' bit (V_{logic}) and also clock high signals (ph1 and ph2). The reference voltage (V_{ref}) is kept at 10V for fast operation of the switched cap circuit. Since the mobility of the TFTs is significantly higher than organic semiconductors and the circuit has reduced

capacitances, it essentially operates at a much higher speed than that in [20]. Since the MSB TFTs drive larger capacitances, they are designed with larger widths of 220 µm while the least significant bit (*LSB*) TFTs have 110 µm. Fig. 6.4 shows the complete circuit fabricated on PEN.

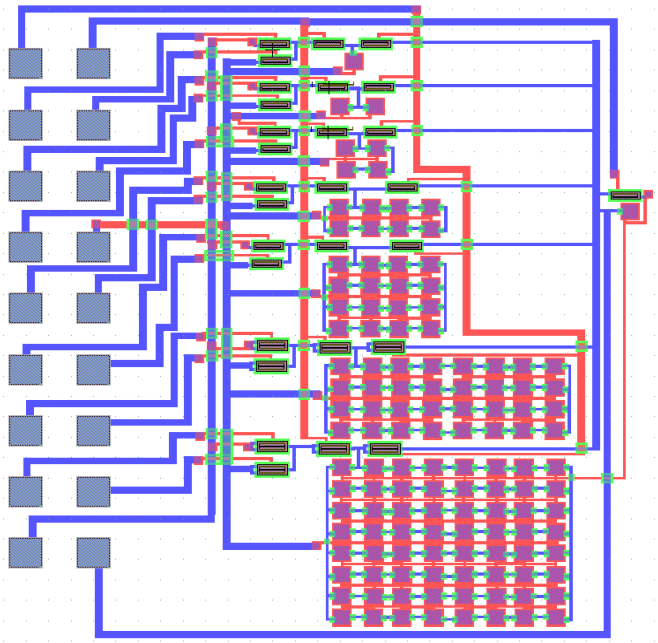

Fig. 6.3 Layout of the DAC.

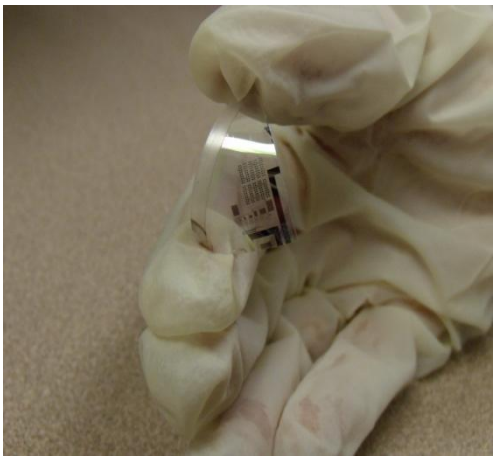

Fig. 6.4 Photo of the DAC on PEN.

Fig 6.5a and 6.5b respectively shows the measured differential and integral non linearity (DNL and INL respectively) relative to the *LSB*. The DAC shows a

maximum value of about ±0.6 *LSB* while the INL is always less than ±1 *LSB* at a conversion rate of 200 Hz and 500 Hz. These values were measured by comparing the voltages difference between adjacent digital codes to *LSB*. The *LSB* was in turn obtained by dividing the maximum output voltage with 128.

Fig. 6.6 shows the excellent linearity curve obtained from our measurement, without any calibration. The maximum output voltage for the full code (1111111) is slightly less than V_{ref}, which is likely due to the charge sharing of the loading capacitance of the probe in the measurement setup.

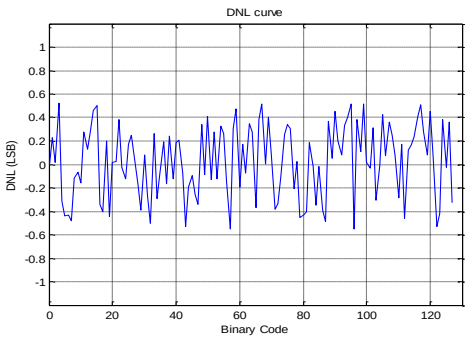

Fig. 6.5a DNL measurement.

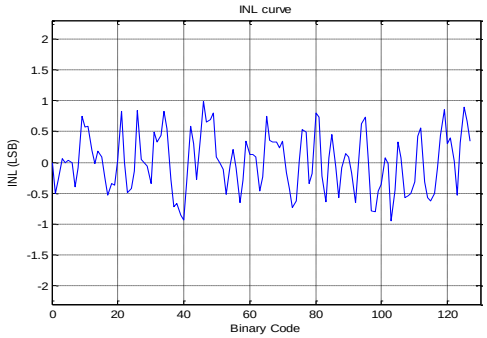

Fig. 6.5b INL measurement.

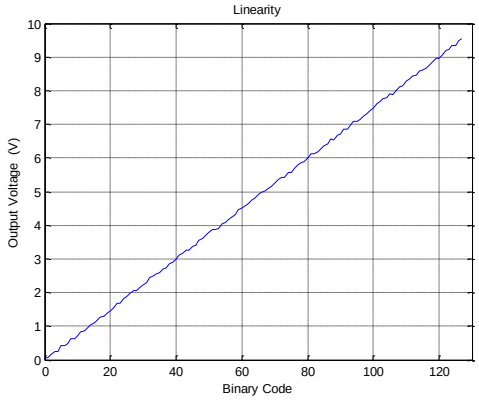

Fig. 6.6 Linearity curve from switched capacitor DAC.

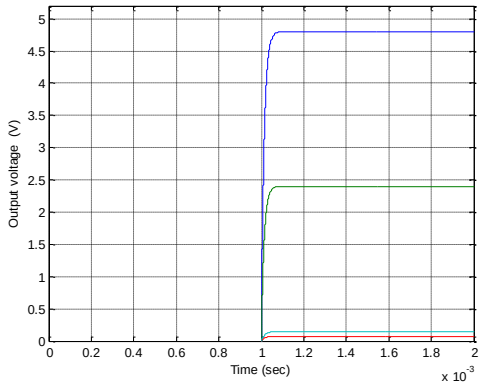

Fig.6.7 Output response with the bits changing from 0 to 1, one at a time with other bits at logic 0.

Fig. 6.7 shows the settling time measurements when the 1st, 2nd, 6th, and 7th bits are switched from logic '0' to '1' with the clock frequency being 500 Hz (other bits being at logic '0' when each individual bit is switched). This was done to check the settling time of the analog outputs, which is maximum when a single bit is switching at a time. The total area was about 8 mm^2. The worst case power dissipation was about 14 µW at 500 Hz.

6.3 5 Bit Current Steering DAC in a-Si:H TFT

The switched capacitor DAC, as mentioned above, requires a buffer with infinite input impedance, to be implemented at its output for proper operation. However, obtaining a buffer is difficult in TFT design due to low gain of the op-amps [86]. An external buffer can be added, but it generally adds additional capacitance slowing the performance. Hence a 5 bit current steering DAC architecture is built in a-Si:H TFT. Because a-Si:H TFTs have high output conductance, building an almost ideal current source is easier. The ultimate resolution is limited by the ratio of the load resistance (R_{out} as shown in Fig. 6.8)

and current source output impedance. However due to large process variation in TFTs, the DNL and INL is expected to degrade.

6.3.1 Current Steering Architecture

An n bit current steering DAC switches k out of 2^n-1 unity current source toward the output under the control of an n bit digital word. With a binary weighted control, 2^i unity elements are connected in parallel and switched together. With unary current generators it is needed to transform the binary code to thermometer code to switch the current generators one by one. However, for both architectures the DAC experiences performance degradation, as none of the current sources are ideal and has finite output conductance. As a result of finite impedance, the analog output to a digital code 'k' is given by

$$V_{out} = I_u R_{out} \frac{k}{1+\alpha k} \tag{6.5}$$

instead of just kI_uR_{out} for the ideal case. Here I_u denote the unit current element. Here $\alpha = R_{out}/R_N$ and $R_N = R_{on} + R_u$ with R_{on} being the on resistance of the nMOS switches and R_u is the output impedance of the current source. Equation (6.5) is a non-linear relationship and hence deteriorates the INL and causes distortion. To obtain an INL < 1LSB, $R_u > 2^{2n-2}R_{out}$. For an R_{out} = 500 Ω, this means R_u > 0.5 MΩ, which is easily satisfied by the cascading structure as shown in Fig.6.8 [87]. The cascode current source is initiated by the Vbias signal at the gate, when the Select signal is high. Similarly, to turn it off quickly additional transistors are initiated with Select_bar signal which pulls down the charge at the gate of the cascode transistors and thus shuts it off. This helps in fast settling of the final value. MD provides a low impedance discharge path when the unit is deselected.

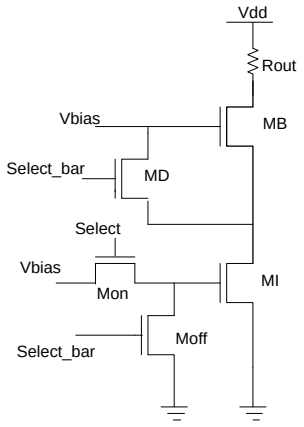

Fig.6.8. Cascode current source in current steering DAC.

Unary architecture is chosen over binary as the magnitude of glitching is proportional to the number of current source that are switching [83]. In contrast, when using binary selection, the number of elements that switch is not proportional to the change in input code; namely at the mid-scale transitions all the switched are exercised; and all but one at one quarter and three quarters of the full scale. Going across these points by one LSB causes a large glitch. In contrast the thermometric approach switches a number of elements that is proportional to the amplitude of the step. The result is that nonlinearity is minimized. Even worse than the glitching errors, the binary selection method has poor DNL at critical points. The worst case is again the mid-point. This gives a large INL on the same points caused by a large step variation in DNL. The unary method, on the other hand, gives the same maximum DNL equal to $2\Delta I_r/I_o$ for all codes (I_r being the reference current).

In the present architecture also, unary current source is implemented. The unity current sources are often arranged in a symmetric square like two dimensional array with $2^{n/2}$ lines and columns. The simplest thermometric

selection is sequential by lines and columns, starting from one corner of the array. The lines and columns are selected using all nMOS NAND decoders. Thus for any digital output, only one switch remains off. To obtain full rail to rail swing, the decoders were implemented as bootstrapped logic [88]. Fig. 6.9 shows the prototype for a 4 bit array with the input code '1011'. The switches were implemented using simple a-Si:H nMOS TFTs.

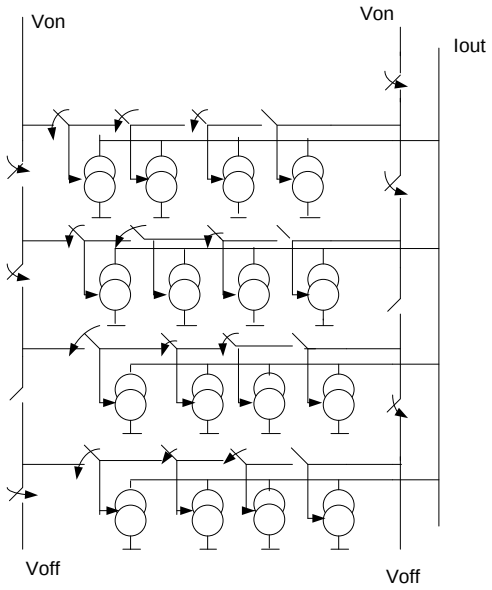

Fig. 6.9. 4 bit array of current steering DAC with 1011 input code.

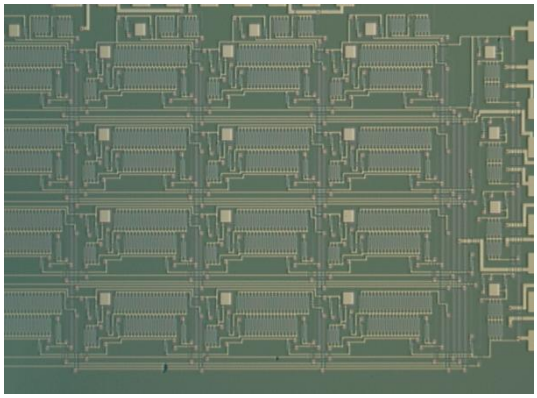

Fig. 6.10. Chip micrograph of 5 bit current steering DAC architecture.

6.3.2. Experimental Results

The DAC in total contains 362 n-channel a-Si:H TFTs. All TFTs have lengths of 11 µm. Fig. 6.10 shows the chip image with all the logic circuitry of the 5 bit DAC with. A voltage of 10 V has been used for logic '1' bit (V_{logic}) and 0 V for logic '0'. Since the mobility of the TFTs is significantly higher than organic semiconductors and the circuit has reduced capacitances, it essentially operates at a much higher speed than that in [8]. I_{out} is converted into voltage by connecting a resistance (R_{out}) of 500Ω between the output and V_{on} (Fig 6.8). The resistance was implemented using Indium Tin Oxide (ITO) strip. While [87] used a resistance of 160Ω, a higher resistance was used here to detect lower current levels in the case of TFTs. The V_{bias} (in Fig 6.8) was chosen to ensure the TFTs never go into linear region. Individual cells conducted 100 µA current, yielding 50 mV as LSB.

Fig. 6.11 shows the DNL (< 1.2 LSB) and INL (<1.9 LSB) from the DAC.

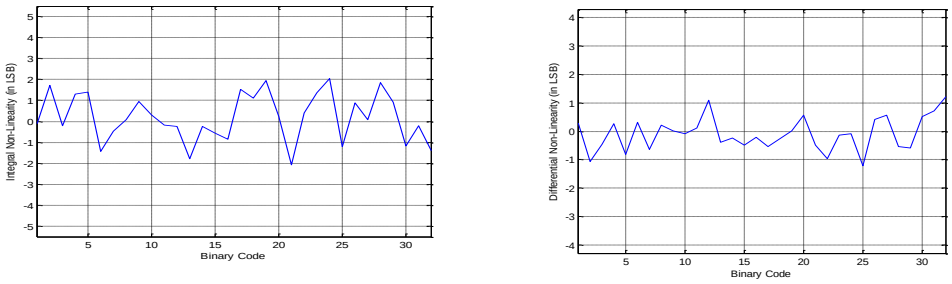

Fig. 6.11 (a) INL and (b) DNL characteristics.

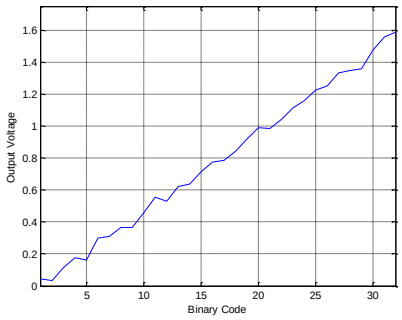

Fig. 6.12. Linearity curve obtained from DAC.

Fig. 6.12 shows the linearity curve obtained from our measurement, without any calibration. The total area was about 60 mm^2. The sampling circuit was tested with output load of 500 Ω. To reduce linearity errors further an averaging technique was employed. For each digital code 'k', two outputs were taken and averaged them to get the final output. For the second output V_{on} and V_{off} were interchanged and complimented the input code bits. It can be easily seen (with respect to Fig. 6.9 as example) that under such conditions, the same number of current sources was chosen, but from a different section. Thus any error due to mismatch was evened out.

6.4 Summary

In this the working of two important DAC architecture in a-Si:H TFTs were demonstrated. The switched capacitor architecture is the most immune to TFT process variation and also to TFT ageing due to electrical stress. However for correct performance, it needs an output buffer, due to its low output impedance. A current steering avoids the problem by employing a cascode current source and thereby enhancing the output impedance. However it does suffer from mismatch. The 7 bit switched cap architecture achieved a DNL of ± 0.6 LSB and INL of ±I *LSB* and showed excellent settling time even at 500 Hz. The current steering DAC, on the other hand achieved a DNL of 1.2 and INL of 1.8, due to large process variation in TFT process.

Chapter 7

FLASH ANALOG to DIGITAL CONVERTER in TFT

7.1 Introduction

The importance of data converters in TFTs have already been discussed with reference to the requirement of building accurate and reliable sensor systems. The last chapter focused on TFT DACs. In this chapter an overview of the ongoing efforts to build TFT full flash ADC is discussed. A 5 bit full flash ADC with gray coding at the output has been designed, simulated and laid out. It operates at 2k samples per second and consumes a power of 0.16 mW.

7.2 Full 5 Bit Flash ADC

Various kinds of ADC architecture exist in the market. Flash ADC is the simplest and fastest while at the same time consuming the largest area. As discussed in chapter 2, a 6 bit SAR ADC in OTFT has been already been built [22]; however it requires an external FPGA to implement the digital logic. Similarly a 1^{st} order sigma delta modulator has also been built in OTFT with only 26.4 dB resolution [23] and operating at only 20 Hz sampling rate. Other architectures like pipelined and cyclic ADCs [89,90] require high gain op-amps to boost the resolution.

7.2.1 Comparator Architecture

At the heart of any flash ADC lies the comparator. The accuracy and speed of the comparator determines the ultimate performance of the ADC. Fig. 7.1 shows some of the common comparators used in flash ADCs [91]. A class AB comparator is very fast but has a large ‘kickback’ noise due to capacitive coupling between the input and output nodes. This is expected to be severe for TFT design

as the device sizes are quite large. The ‘kickback’ noise causes large dynamic offsets, decreasing the resolutions and causing metastability problems. The class A comparator reduces the ‘kickback’ noise somewhat; but itself comes with the problem of static power dissipation. The auto-zeroed comparator eliminates the comparator offset and is immune to ‘kickback’ noise, but is slower than the other architectures. The best choice is the dynamic comparator which retains the speed due to positive feedback, yet eliminates the kickback noise to a large extent.

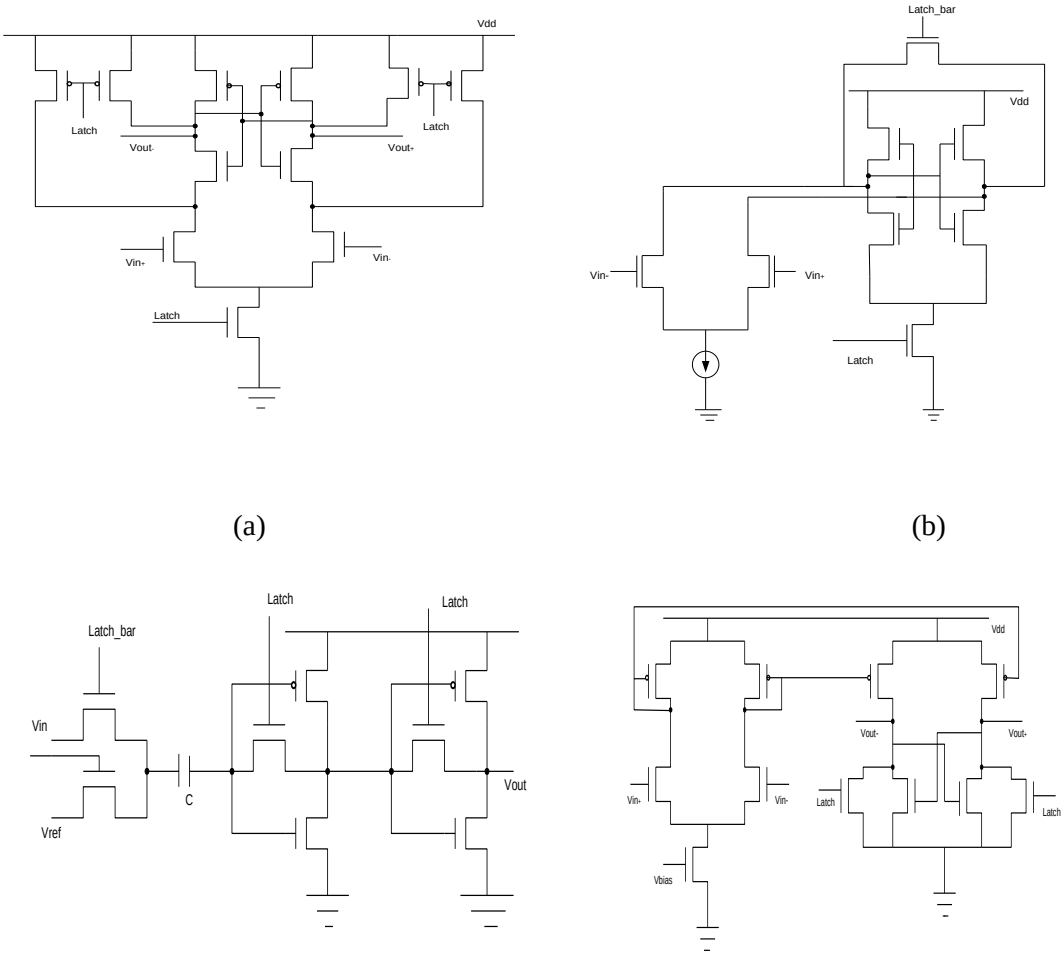

Figure 7.1 Comparators for flash ADC: (a) Class AB, (b) Dynamic, (c) Auto-zeroed and (d) Class A.

In the present case the preferred choice dynamic comparator. However, due to poor yield of pentacene OTFTs and their reliability issues an all nMOS topology was chosen. Thus the pMOS pull up transistors were implemented using a-Si:H NMOS TFTs. As a result static power dissipation could not be avoided. Also rail to rail swing could not be achieved. However this is not a problem for the present case which uses a high voltage supply of 20 V and 0V and thus there is a clear distinction between logic '0' and logic '1' voltage. To reduce kickback noise due to a minimum in spite of parasitic capacitances, the self neutralization technique was employed [91]. When the drain voltages V_{DN1} and V_{DN2} vary, the preceding circuit must provide charge for C_{GD} of the differential pair. This disturbance is called 'kickback' noise. Adding two extra capacitance $C = C_{GD}$ as shown in Fig. 7.2 reduces the kickback noise to first order, if the drain voltage variation is complementary. This is because the charge now comes from C and not from preceding circuit. The arrow in Fig. 7.2 shows the current flowing when V_{DN1} decreases and V_{DN2} increases. However, cancellation is not perfect as the voltage variations in regeneration nodes are not perfectly balanced.

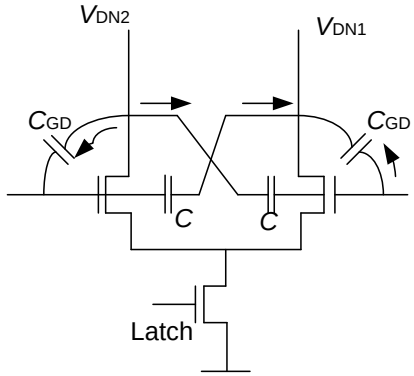

Fig. 7.2. Self neutralization technique using extra *C*.

7.2.2 Flash Architecture

A complete 5 bit flash ADC is built in a-Si:H nMOS TFTs using 31 comparators and logic circuits. The block diagram is shown in Fig. 7.3.

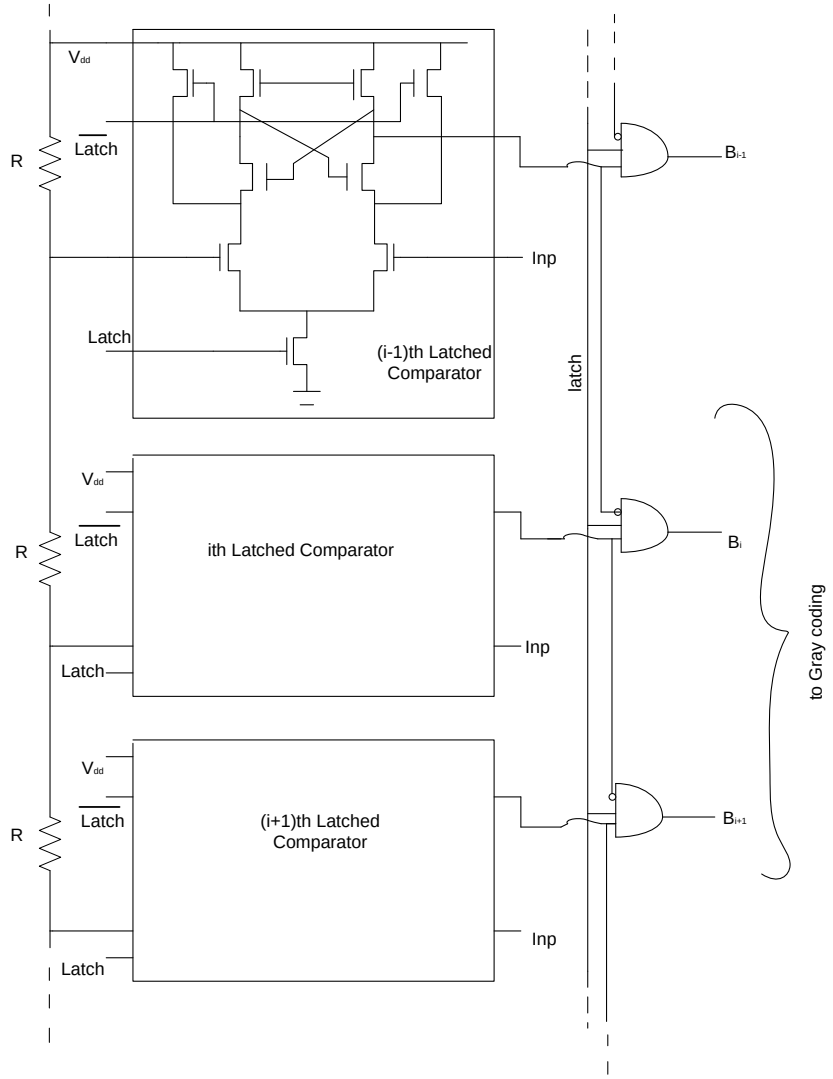

Fig. 7.3. Block diagram of the 5 bit ADC.

The logic circuits have been implemented using bootstrapped concept to have rail to rail swing. Bootstrapping capacitors were chosen to be 1.5 pF. A common error in flash ADC is comparator meta-stability in which case a comparator is unable to make the correct decision. This problem plagues the a-

Si:H circuits more, due to their slow speed and hence larger regeneration time. This results in faulty output if a simple binary code is used. Gray coding has been implemented with bootstrapped topology at the output, to reduce the above problem. Since sequential Gray codes differ by a single bit, when these are converted to binary, there is an error of at most 1 *LSB* [92]. The ADC has been shown to operate satisfactorily at 2k samples per second, typical in sensor applications for large area flexible and wearable electronics. The Kelvin resistance divider (R) was chosen to be 200 Ω to optimize power consumption as well as reduce kickback noise at 2k samples/sec. The resistance divider was implemented using a poly metal strip.

A typical factor that reduces the resolution of the flash ADC is comparator offset, apart from power and area considerations. Typically mismatch in the process parameters, especially V_{th} result in comparator offset. However, to reduce monotonicity or no missing codes the maximum tolerable offset has to be less than 0.5 *LSB* divided by the number of sigma needed to obtain the desired yield [83]. Since the present process is prone to mismatch the resolution was limited to 5 bits. An off chip reference voltage of low output impedance and value = 15 V was used. A 15 V square wave was chosen as the *Latch_bar* signal, supplied from a signal generator. Also a 20 V square wave was chosen as the *Latch* signal. Since it is an all nMOS circuit the pull down nMOS TFTs are made much wider than the pull up ones. Also the *Latch* signal is made 20 V while the V_{DD} is at 15 V, simply to provide the extra overdrive to the pull down nMOS transistors, especially for input voltages closer to 0 V. The full circuit required 803 nMOS

transistors. The ADC consumes a power of 36 mW at 2k samples/sec and an area of 1.856 cm^2. Power was mostly consumed in the resistor ladder. The complete chip micrograph of the ADC is shown in Fig. 7.4.

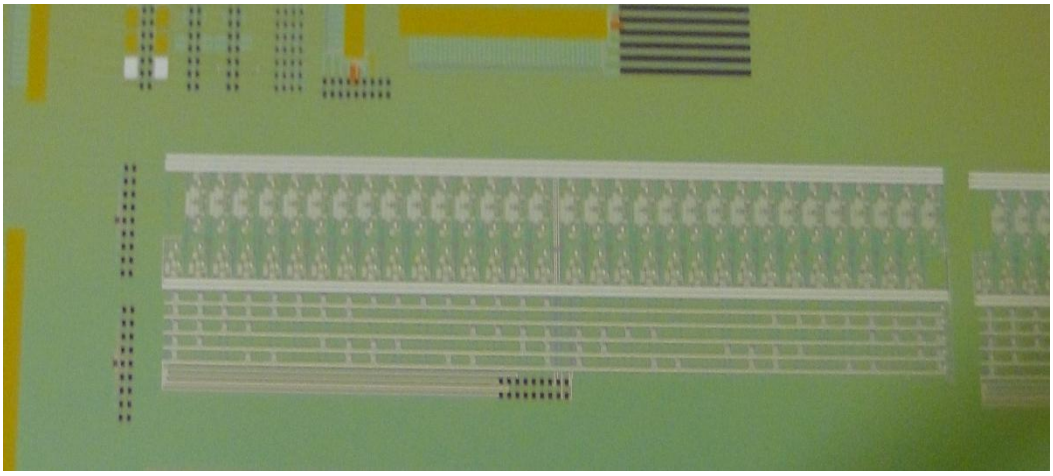

Fig.7.4. Chip micrograph of the full 5 bit ADC with 31 comparators and Gray coding at output.

7.2.3 Experimental Results

The measured DNL and INL obtained are shown in Fig. 7.5 (a) and (b)

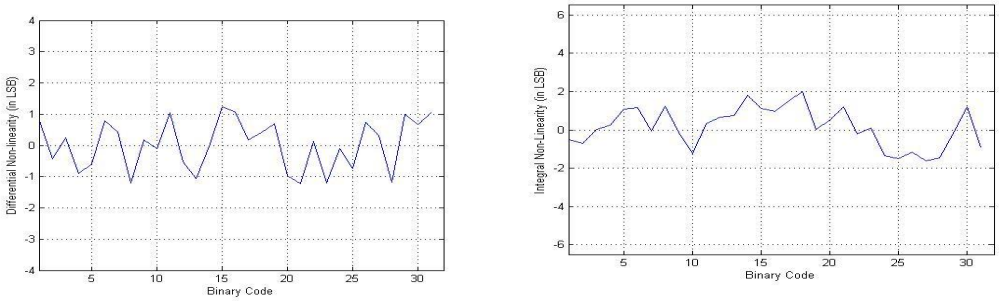

Fig. 7.5 (a) Measured DNL and (b) measured INL from 5 bit ADC.

Fig. 7.6 shows the measured linearity for the full 5 bit flash ADC. The offset was measured to be about 0.8 *LSB* by least square fitting. Both the DNL and INL were affected by the absence of pre-amplifiers as well as process induced mismatch resulting in latch offset. A better approach would have been the use of

pre-amplifiers, which would not only have reduced the latch offset, but reduced the kickback noise further. However it would have also increased the circuit complexity of the ADC as 31 preamplifiers had to be designed.

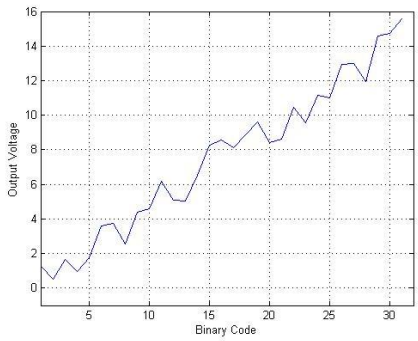

Fig. 7.6 Measured linearity of 5 bit flash ADC.

7.3 SUMMARY

In this chapter the working of a 5 bit flash ADC architecture in a-Si:H TFTs was demonstrated. Four different comparator architectures were chosen and simulated. Out of the four, the dynamic comparator was chosen to reduce kickback noise as well as have sufficient speed due to positive feedback. Since a CMOS structure is difficult to build in TFTs due to severe reliability issues, an all nMOS topology was resorted to. Bootstrapping was employed in the logic circuits to have rail to rail swing. To reduce meta-stability errors, Gray coding was employed at the output, instead of the usual binary coding. The ADC was tested for a maximum speed of 2k samples/sec and consumed a power of 36 mW at that speed. It had a total area of 1.865 cm^2.

Chapter 8

CONCLUSIONS and SCOPE for FUTURE WORK

8.1 Conclusion

In the present thesis various aspects of mixed signal design in TFTs were analyzed and presented. The work can be broadly divided into four sections i.e. a) evaluation of circuit performance of mixed oxide n-channel TFTs under electrical and mechanical stress along with efforts to find the dominant degradation mechanism; b) fabrication and performance analysis of various TFT op-amps; c) design, simulation and post fabrication analysis of two popular types of DACs in TFTs; and d) design and fabrication of full 5 bit flash ADC with gray coding in the output.

The highlights of the present work are given below

8.1.1. Stress Testing of ZIO TFTs

A-ZIO TFTs have been shown to have better stability than a-Si:H TFTs. Extensive electrical bias stress testing of a-ZIO TFTs fabricated at the FDC was carried out. It clearly showed that a-ZIO TFTs are much more stable and have better mobility. Also effect of drain bias degradation on these TFTs were carried out and post stressed current in both forward and reverse mode were measured. These experiments supported charge trapping in the semiconductor-insulator interface as the chief degradation mechanism and not defect creation in the bandgap as has been the case for a-Si:H TFTs. Further, mechanical stress testing of these TFTs was carried out to evaluate their performance when bent and deformed on cylindrical surfaces. It was clear that tensile stress parallel to the channel does reduce some defect states in the semiconductor bandgap. However

compressive stress introduces more defect states, while stress perpendicular to channel, (both tensile and compressive), have negligible effect whatsoever.

8.1.2 Operational Amplifiers in TFTs

A high DC gain (50 dB) and unity gain frequency of 7 kHz operational amplifier has been fabricated using CMOS configuration of a-Si:H and pentacene TFTs. The op-amp achieved a swing of ±8 V with a supply of ±15 V. Complete analysis and simulation of different popular op-amp topologies like folded cascode, in different material combinations were made showing that an all nMOS enhancement-depletion topology yields the best possible solution. Degradation analysis of the different topologies with respect to individual TFT degradation is carried out with different biasing circuits. It was found that biasing with a DC current source makes the topology immune to degradation. However, using the popular β multiplier circuit makes the op-amp topology more prone to degradation. A novel biasing scheme has been implemented that keeps the biasing current somewhat constant with respect to time, to retard the performance degradation due to individual TFTs.

8.1.3 DAC Architectures in TFTs

As discussed in the relevant sections, DAC design in TFTs has been plagued by numerous factors like process induced mismatch, low mobility and degradation due to electrical stress. As a result a switched cap architecture is the best choice. In switched cap architecture, the TFTs act as switches only and hence the performance does not depend much on the current carried by the TFTs. A 7 bit architecture was built in all nMOS TFTs and achieved a DNL of 0.6 LSB and an

INL of 1 LSB, without external calibration. The power supply used was 20 V. It consumed a power of 8 µW at a speed of 500 Hz. However, as switched cap architecture is based on charge sharing concept, it needs an external buffer to be implemented at the output. Hence a 5 bit current steering DAC has also been designed simulated and laid out. The architecture has been laid out in a symmetric manner to reduce mismatch due to process variation. The DAC achieves a DNL of 0.6 *LSB* and an INL of 1 LSB.

8.1.4 Full 5 bit Flash ADC in a-Si:H TFTs

A full 5 bit flash has been designed, simulated, laid out and sent for fabrication. It consists of 31 comparators and has gray coding at the output. The entire structure has been built out of a-Si:H all nMOS TFTs. Class AB comparators have been chosen to enhance speed as well as reduce 'kickback' noise. However due to difficulty in implementing pentacene pMOS TFTs, all pMOS have been replaced by nMOS. However, all nMOS topology do not permit rail to rail swing and expends static power. Resistor strings of value 200 Ω were used to avoid voltage drooping at the comparator output and at the same time reducing power. The simulated power consumption has been found to be 0.16 mW at a speed of 2 k samples/sec.

8.2 Scope for Future Work

Based on the present work some extensions are outlined:

(i) Electrical and mechanical stress testing of these TFTs have been accomplished extensively. However, the reasons for degradation of mobility and subthreshold slope are still not clear and further investigations

need to be performed. Also thermal testing of these TFTs need to be performed to ascertain the behavior of these TFTs under extreme environmental conditions.

(ii) TFT op-amps have been built in CMOS topology using a-Si:H nMOS and pentacene pMOS. However it has been shown through simulation that all nMOS topology implemented in enhancement-depletion mode topology would be the best choice. Hence, an effort could be made to fabricate depletion mode TFTs and integrate them seamlessly to make an op-amp. Moreover the entire structure and the CMOS version could be implemented with mixed oxide TFTs to get better performance and stability.

(iii) Just like op-amps, data converter circuits like ADCs and DACs could also be built in mixed oxide TFTs and tested for better performance. Also several other architectures like SAR ADC and sigma delta modulator could also be tried to get a higher resolution. Moreover digital calibration techniques can be implemented to increase the resolution to overcome errors due to mismatch.

(iv) The reliable operation of the data converters (be it in a-Si:H or mixed oxide TFTs) could be tested to evaluate how these structures degrade with electrical usage. Novel architectures or additions can be incorporated to retard the degradation.

(v) Novel biasing circuits have been designed to retard the degradation of the TFT opamps. It is well known that with continuous electrical stress the

TFTs degrade with positive shifts in V_T. This change the biasing current which ultimately degrade the opamp DC gain and bandwidth. A solution to the problem is to use an external biasing current. With an external DC current source the gate voltages of individual TFTs adjust in a way so as to keep the current flowing through them constant, in spite of the V_{th}s changing. However, when such a solution is not available a novel solution using the widely used β multiplier is proposed and designed in this thesis. The structure of such a circuit is shown in Fig. 5.7.

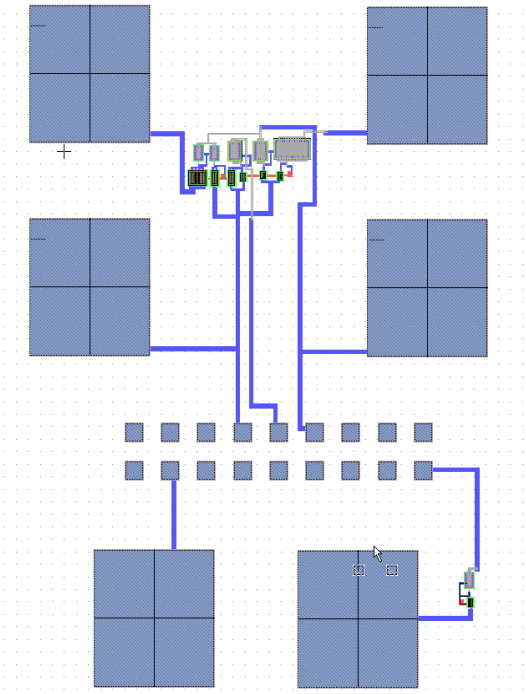

Fig. 8.1. Layout of the novel biasing circuit in CMOS TFT.

The left half of the circuit is the usual β multiplier. As V_T of the nMOS TFTs increase the current in the left branch increase. However in the right branch, V_{th} of the pMOS TFTs also increase, increasing the branch current. The middle portion sums the current. As the sum remains constant, the biasing voltage remains the same. However the current does not exactly

remains the same as degradation rate of pMOS and nMOS TFTs are not the same. This is shown in Fig. 5.8. Such a circuit has been designed and the layout is shown in Fig. 8.1. However, as the pMOS degrades in ambient conditions, it has been very difficult to test these circuits.

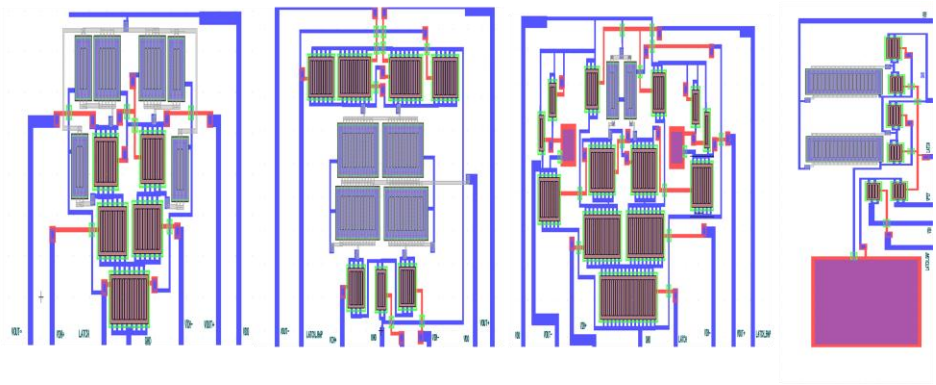

Fig. 8.2. Layout of different comparators for flash ADC in CMOS TFTs.

(vi) As discussed in section *7.2.1*, several comparators were designed in CMOS TFTs to test their speed and resolution performance. The layouts of the comparators are shown in Fig. 8.2. However, as the comparators were designed in CMOS topology, it was difficult to test them. This is because of the fact that the pMOS organic TFTs degrade even in ambient conditions, in presence of moisture and air. The author hopes that in future it might be possible to come up with organic TFTs (or inorganic ones like CdS, PbS) which do not degrade in ambient conditions.

(vii) A few improvements could be made in the existing flash ADC architecture. First auto-zeroing could be used in comparators to reduce process induced mismatches. Pre amplifiers can be employed to enhance the gain and hence reduce comparator regeneration time. Also the output logic circuit can be

modified to have a 3 input NAND gate, to detect a 011 instead of 01 to reduce ‘sparkle errors’ [93].

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6. Korhan Kaftanoglu, Sameer M. Venugopal, **Aritra Dey**, Michael Marrs, James R. Wilson, Edward Bawolek, David R. Allee and Doug Loy, *'Flexible Electrophoretic Display using Low temperature IZO TFT Backplane on PEN substrates',* accepted in IEEE Journal of Display Technology.

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1. **Aritra Dey** and David Allee, '*Mechanical Stress Testing of a-ZIO TFTs Fabricated at Low Temperature',* Proc. Flexible Electronics and Display Conference, Feb, 2011, Phoenix, Az.
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2. **Aritra Dey,** '*Novel Compensating Biasing Scheme for Thin Film Transistor Operational Amplifier*,' US patent filed on Oct. 2010.