Simulation of MOSFETs, BJTs and JFETs

At and Near the Pinch-off Region

by

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ABSTRACT

Semiconductor devices are generally analyzed with relatively simple equations or with detailed computer simulations. Most text-books use these simple equations and show device diagrams that are frequently very simplified and occasionally incorrect. For example, the carrier densities near the pinch-off point in MOSFETs and JFETs and the minority carrier density in the base near the reverse-biased base-collector junction are frequently assumed to be zero or near zero. Also the channel thickness at the pinch-off point is often shown to approach zero. None of these assumptions can be correct. The research in thesis addresses these points.

I simulated the carrier densities, potentials, electric fields etc. of MOSFETs, BJTs and JFETs at and near the pinch-off regions to determine exactly what happens there. I also simulated the behavior of the quasi-Fermi levels. For MOSFETs, the channel thickness expands slightly before the pinch-off point and then spreads out quickly in a triangular shape and the space-charge region under the channel actually shrinks as the potential increases from source to drain. For BJTs, with collector-base junction reverse biased, most minority carriers diffuse through the base from emitter to collector very fast, but the minority carrier concentration at the collector-base space-charge region is not zero. For JFETs, the boundaries of the space-charge region are difficult to determine, the channel does not disappear after pinch off, the shape of channel is always tapered, and the carrier concentration in the channel decreases progressively.

After simulating traditional sized devices, I also simulated typical nano-scaled devices and show that they behave similarly to large devices. These simulation results provide a more complete understanding of device physics and device operation in those regions usually not addressed in semiconductor device physics books.

ACKNOWLEDGEMENT

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CHAPTER 1

INTRODUCTION

Overview

The research in this thesis focuses on the basic semiconductor devices: MOSFET, BJT and JFET. Relevant properties such as the carrier concentration, potential, electric field, current density, I-V curve, band diagram and quasi-Fermi level are simulated and analyzed in two-dimensional models using software ATLAS (SILVACO). I am particularly concerned with the “pinch-off” regions in these devices. Simple theories and most device physics books show the carrier densities to approach zero as they enter the reverse-biased space-charge regions (drain, collector). This, of course, cannot be true and my goal is to simulate the carrier densities, potentials, electric fields etc. in these regions to discover exactly what happens there for a more complete understanding of device physics and device operation.

Device Background

1) Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

MOSFETs are commonly used in the semiconductor industry for amplifying or switching electronic signals. The first letter M means "metal"; early MOSFET gates (gate electrode) used metal as the material, but with the development of semiconductor technology, the modern silicon MOSFET gate has been replaced with polysilicon.

Based on the carrier type in the channel between source and drain, the p-type channel MOSFET with holes in the channel is named PMOSFET or PMOS; the n-type channel MOSFET with electrons in the channel is named NMOSFET or NMOS. However, PMOS and NMOS are complementary structures and have the same operating principles. The NMOS basic structure is shown in Fig. 1-1.

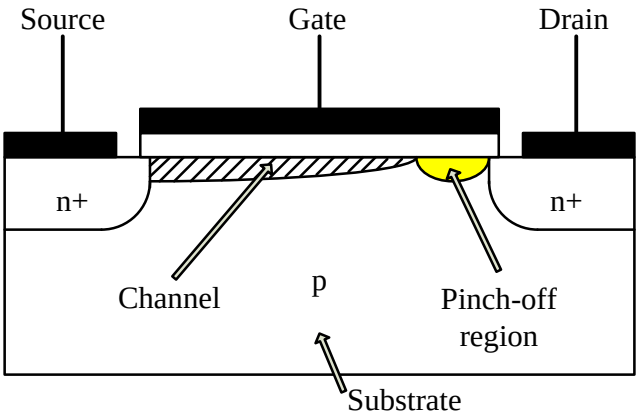

Figure 1-1. NMOS vertical cross sectional view

Source and drain are two n^+ regions implanted into a p-type substrate, under the gate there is a SiO_2 layer formed by thermal oxidation. Most MOSFETs are four-terminal devices. Substrate and source are usually grounded. For NMOS, when applying a positive gate voltage (above threshold voltage) on the gate, the p-type substrate becomes depleted and inverted with an n-channel formed between source and drain. The gate voltage V_g applied on the gate is separated into two components: oxide voltage V_{ox} and potential drop in the silicon Φ_s.

$$V_g = V_{ox} + \Phi_s = \frac{-Q_s}{C_{ox}} + \Phi_s \tag{1.1}$$

$$C_{ox} = \frac{K_{ox}\varepsilon_o}{t_{ox}} \tag{1.2}$$

where Q_s is the unit area charge in the silicon substrate, C_{ox} is the oxide unit area capacitance, and t_{ox} is the oxide thickness. The negative sign in Eq. (1.1) means the charge in the gate is always opposite to the charge in silicon.

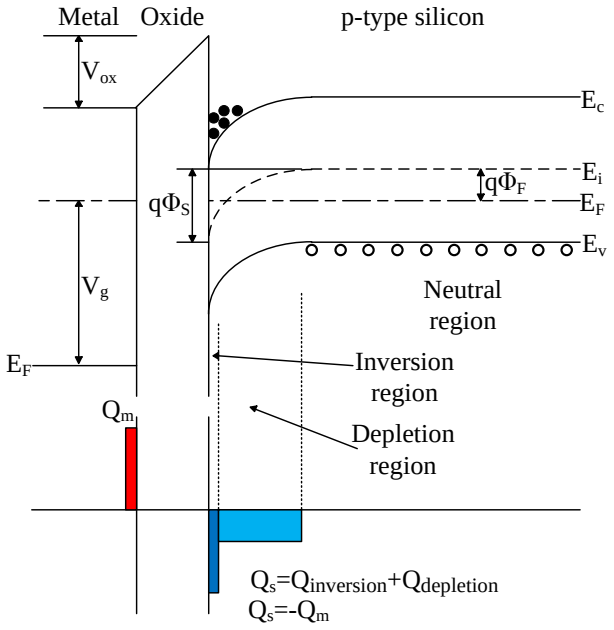

Figure 1-2. NMOS band diagram with positive gate voltage (above threshold voltage) charge distribution for inversion [1]

Figure 1-2 shows the band diagram and charge distribution of an n-channel MOSFET. In the basic model, oxide and interface traps are assumed to be zero. The voltage drop in the oxide and band bending are clearly shown. From the charge distribution plot, an inversion layer forms when $\Phi_s \geq 2\Phi_F$.

The carrier mobility in the channel is lower than in the substrate, because of interface scattering. When a positive drain voltage is applied, drain current flows and due to the resistance in the channel, there is a voltage drop between source and drain. The channel is generally shown to become thinner from source to drain and disappears at the pinch-off region near the drain, as schematically shown in

Fig. 1-1. Due to the voltage drop along the channel, the gate voltage induced vertical electric field is reduced from source to drain providing less attraction for channel electrons. Consequently the channel becomes thicker as it approaches the drain as shown in my simulation. The behavior of electrons/holes at and near the pinch-off region of MOSFETs, bipolar junction transistors and junction FETs is the main topic of this thesis.

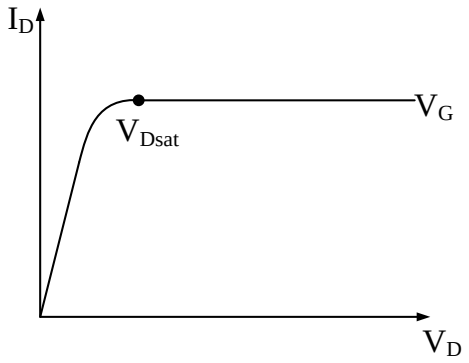

Figure 1-3. Drain current-drain voltage plot

On the drain current-drain voltage plot of Fig. 1-3, the pinch-off condition occurs where the drain current begins to saturate. The drain voltage at this point is the saturation drain voltage V_{Dsat}. The drain current is approximately constant beyond V_{Dsat} for long-channel MOSFETs.

2) Bipolar Junction Transistor (BJT)

BJTs are also used in the semiconductor industry for amplifying or switching electronic signals. In semiconductor development history, BJTs were developed before MOSFETs. BJTs are three-terminal devices. In addition, BJTs are current

controlled devices with low input impedance, high power driving ability, long lifetime, and high reliability.

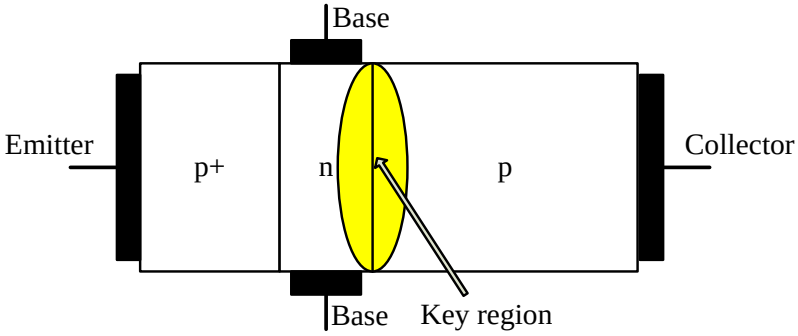

Figure 1-4. BJT vertical cross sectional view (PNP)

A bipolar junction transistor has two PN junction diodes connected back to back as shown in Fig. 1-4. In the common base connection, the emitter-base junction is forward biased and the collector-base junction is reverse biased. Holes are injected from the emitter into the base to be collected in the collector. Most of the holes diffuse through the base from emitter to collector very fast, which means the base transit time is much shorter than the base minority carrier lifetime, and recombination of minority carriers in the base is negligible. The emitter current is approximately the collector current as the base current is very small ($I_E = I_B + I_C$), and the current gain is slightly lower than unity.

Actually most high-speed bipolar transistors are NPN junction structures [2]. Because the electron mobility is about three times the hole mobility, using NPN structures will shorten the response time and increase the speed. However, here I use PNP structures to demonstrate and simulate because most semiconductor books use PNP structures.

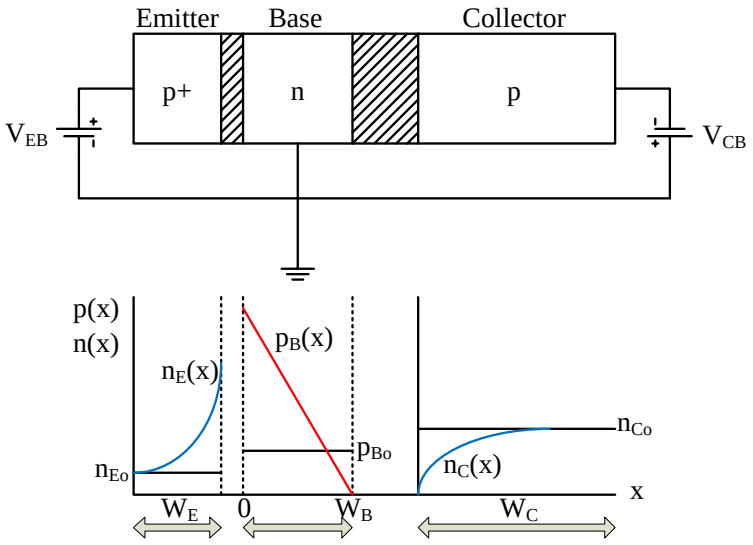

Figure 1-5. BJT common base connection with minority carrier concentration plot [3]

Figure 1-5 shows the minority carrier concentrations with the emitter-base forward biased. The minority carrier concentration at the e-b space-charge region edge, $p_B(0)$, is proportional to $\exp(qV_{EB}/kT)$; the collector-base is reverse biased and the minority carrier concentration at the c-b space-charge region edge, $p_B(W_B)$, is proportional to $\exp(-qV_{CB}/kT)$ which is approximately equal to zero.

The base minority carrier (hole) distribution is determined by the continuity equation and boundary conditions,

$$\frac{\partial^2 \Delta p_B}{\partial x^2} - \frac{\Delta p_B}{{L_B}^2} = 0 \tag{1.3}$$

$$\Delta p_B(0) = p_{B0}\left(e^{qV_{EB}/kT} - 1\right) \tag{1.4}$$

$$\Delta p_B(W_B) = p_{B0}\left(e^{qV_{CB}/kT} - 1\right) \tag{1.5}$$

giving [4]

$$\Delta p_B(x) = \frac{p_{B0}\left\{\sinh\left[\frac{(W_B - x)}{L_B}\right]\left(e^{\frac{qV_{EB}}{kT}} - 1\right) + \sinh\left[\frac{x}{L_B}\right]\left(e^{\frac{qV_{CB}}{kT}} - 1\right)\right\}}{\sinh\left(\frac{W_B}{L_B}\right)}$$

(1.6)

For narrow base $W_B \ll L_B$ and

$$p_B(x) \approx p_{B0}\left[(1 - x/W_B)\left(e^{qV_{EB}/kT} - 1\right) + x/W_B\left(e^{qV_{CB}/kT} - 1\right)\right] + p_{B0}$$

(1.7)

For wide base $W_B \gg L_B$ and

$$p_B(x) \approx p_{B0}\left[e^{-x/L_B}\left(e^{qV_{EB}/kT} - 1\right) + e^{-(W_B - x)/L_B}\left(e^{qV_{CB}/kT} - 1\right)\right] + p_{B0}$$

(1.8)

From eq. (1.7), the narrow-base minority carrier concentration is linear; for wide base in eq. (1.8), the minority carrier concentration is exponential. At the collector-base side of the base, $p_B(W_B) \approx 0$.

The highlighted region in Fig. 1-4 is the region which will be discussed in my simulation research. In reality, the minority carrier concentration cannot be zero at the edge of the space-charge region which is similar to the MOSFET pinch-off where the channel cannot disappear.

3) Junction Gate Field-Effect Transistor (JFET)

The JFET concept of a field effect was proposed about two decades earlier than the BJT. When the JFET was proposed, it was not possible to manufacture it with the industrial technology at that time and the first practical JFET was made many years after the BJT. Compared with the BJT, the JFET has high input

impedance, low noise, high frequency limit, low power consumption, wide temperature range, and a simple manufacturing process [5]. As the charge-storage effect is small, the reverse recovery time is short, so JFETs have high switching speed and high frequency response and has been widely used in various digital and microwave circuits.

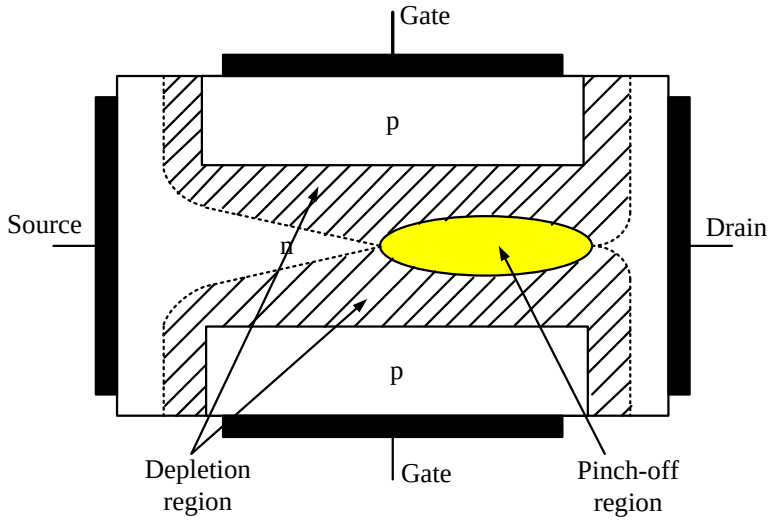

Figure 1-6. JFET vertical cross sectional view (n-channel)

The JFET is a voltage-controlled device similar to MOSFETs, but it is a majority carrier device. There are two types of JFET: p-channel and n-channel. Fig. 1-6 shows an n-channel JFET.

As shown in Fig. 1-6, between the p-type gate and n-channel, there are depletion regions formed by the negatively-biased gate. When positive drain voltage is applied, there is a current flow in the middle layer (n-channel). Due to the channel resistance, there is a voltage drop between source and drain and the channel will become narrower and narrower from source to drain. Once the drain voltage is increased to a certain voltage the two depletion regions touch and the

channel disappears. This voltage is the saturation voltage V_{Dsat} similar to a MOSFET. This disappearance of the channel at pinch-off leads to constant saturation current I_{Dsat} when the channel is pinched off. The term "pinch-off" was first introduced in the JFET and later adopted for the MOSFET.

The highlighted region in Fig. 1-6 is the region which is fully explored by simulation in this research. The majority carriers have to traverse the pinch-off region. This is similar to the MOSFET pinch-off.

In this section, I discussed the basic operation principles of semiconductor devices: MOSFET, BJT and JFET. I also pointed out the key regions that are explored in the simulation research. The next section will demonstrate the simulation related concepts, equations, models, and software.

CHAPTER 2

SIMULATION METHOD

Basic Semiconductor Equations

Years of development of research on semiconductor devices has provided a series of mathematical models with fundamental physics equations of basic device operation. Simulation is based on these physics equations. These equations, which are solved in SILVACO (ATLAS), are derived from Maxwell's equations, Poisson's equation, the continuity equations and transport equations [6].

1) Poisson's Equation

Poisson's equation is

$$\nabla^2\Phi = -\frac{\rho}{\varepsilon_0} \tag{2.1}$$

where Φ is the electrostatic potential, ρ is the space charge density, ε_0 is the vacuum permittivity [7]. For simulation in ATLAS, the space charge density is the sum of mobile charges and fixed charges which includes holes, electrons and ionized impurities; the reference electrostatic potential is the intrinsic Fermi potential and the electric field is the derivation of electrostatic potential [8],

$$\mathcal{E} = -\nabla\Phi \tag{2.2}$$

2) Carrier Continuity Equations

The continuity equation is the description of the behavior of the carriers in a partial differential equation. In semiconductor physics, it is always used for electron and hole concentration gradients with current densities.

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla J_p + G_p - R_p \tag{2.3}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla J_n + G_n - R_n \tag{2.4}$$

$$\frac{\partial \Delta p_n}{\partial t} = D_p \frac{\partial^2 \Delta p_n}{\partial x^2} - \frac{\Delta p_n}{\tau_p} + G_L \tag{2.5}$$

$$\frac{\partial \Delta n_p}{\partial t} = D_n \frac{\partial^2 \Delta n_p}{\partial x^2} - \frac{\Delta n_p}{\tau_n} + G_L \tag{2.6}$$

where p and n are the hole and electron concentrations, J_p and J_n are the hole and electron current densities, G_p and G_n are the hole and electron generation rates, R_p and R_n are the hole and electron recombination rates, q is the charge of an electron, p_n and n_p are minority carrier concentrations, τ_p and τ_n are minority carrier hole and electron lifetimes, and the generation rate G_L usually equals zero. D_p and D_n are the hole and electron diffusion coefficients, which I can obtain from μ_p and μ_n which are the hole and electron mobilities through the Einstein relationship,

$$D_p = \frac{kT}{q}\mu_p \tag{2.7}$$

$$D_n = \frac{kT}{q}\mu_n \tag{2.8}$$

3) Transport Equations

The transport equations are usually simplified from the Boltzmann transport equation. Different hypothesis can be described as different transport models such as the drift-diffusion transport model, the Energy Balance Transport Model in ALTAS simulations. In addition, different transport models will lead to different generation-recombination models [6].

Drift-Diffusion Transport Model

In semiconductor devices, there are three ways of carrier transport: drift, diffusion and generation-recombination. All will lead to current flow. In device characterization, electrons and holes both contribute to current. For the drift-diffusion transport model, I obtain the hole and electron current densities as [9]

$$J_p = J_{p/drift} + J_{p/diff} = q\mu_p p\mathcal{E} - qD_p\nabla p \tag{2.9}$$

$$J_n = J_{n/drift} + J_{n/diff} = q\mu_n n\mathcal{E} + qD_n\nabla n \tag{2.10}$$

Drift current depends on the carrier mobility, carrier concentration and electric field, diffusion current depends on the diffusion coefficient and the gradient of carrier concentration. The total current density is [9]

$$J = J_p + J_n \tag{2.11}$$

which is the combination of hole and electron current densitites [3].

The current densities in terms of quasi-Fermi potentials Φ_{Fp} and Φ_{Fn} are

$$J_p = q\mu_p p\nabla\Phi_{Fp} \tag{2.12}$$

$$J_n = q\mu_n n \nabla \Phi_{Fn} \tag{2.13}$$

The quasi-Fermi levels are obtained from

$$p = n_{ie} \exp\left[\frac{q\left(\Phi_{Fp} - \Phi\right)}{kT}\right] \tag{2.14}$$

$$n = n_{ie} \exp\left[\frac{q(\Phi - \Phi_{Fn})}{kT}\right] \tag{2.15}$$

where n_{ie} is the effective intrinsic concentration and

$${n_{ie}}^2 = {n_i}^2 \exp\left(\frac{\Delta E_g}{kT}\right) \tag{2.16}$$

Then transform the equations (2.14) and (2.15) to

$$\Phi_{Fp} = \Phi + \frac{kT}{q} \ln\left(\frac{p}{n_{ie}}\right) \tag{2.17}$$

$$\Phi_{Fn} = \Phi - \frac{kT}{q} \ln\left(\frac{n}{n_{ie}}\right) \tag{2.18}$$

Substituting the equations into (2.12) and (2.13) gives

$$J_p = -q\mu_p p \nabla \Phi - qD_p \nabla p + \mu_p p[kT \nabla(\ln n_{ie})] \tag{2.19}$$

$$J_n = -q\mu_n n \nabla \Phi + qD_n \nabla n - \mu_n n[kT \nabla(\ln n_{ie})] \tag{2.20}$$

If takes account of the effects of band gap narrowing, because effective intrinsic concentration n_{ie} depends on the temperature T, and the electric fields are described as

$$\mathcal{E}_p = -\nabla\left[\Phi - \frac{kT}{q} \nabla(\ln n_{ie})\right] \tag{2.21}$$

$$\mathcal{E}_n = -\nabla\left[\Phi + \frac{kT}{q} \nabla(\ln n_{ie})\right] \tag{2.22}$$

Energy Balance Transport Model

The energy balance transport model is a higher order solution to the Boltzmann transport equation. The current density expressions compared to drift-diffusion model are more detailed. The current density expressions are

$$J_p = -qD_p\nabla p - q\mu_p p\nabla\Phi - qpD_p\nabla T_p \tag{2.23}$$

$$J_n = -qD_n\nabla n - q\mu_n n\nabla\Phi + qpD_n\nabla T_n \tag{2.24}$$

where T_p and T_n are the hole and electron carrier temperatures [6].

a) Carrier Statistics - Fermi-Dirac and Boltzmann Statistics

The Fermi-Dirac distribution can be used to describe the probability of an electron state being occupied by an electron with energy E in thermal equilibrium

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)} \tag{2.25}$$

where T is the temperature, E_F is the Fermi level energy and k is Boltzmann's constant. It can be simplified for $E - E_F \gg 3kT$ as [10]

$$f(E) \approx \exp\left(\frac{E_F - E}{kT}\right) \tag{2.26}$$

This is the Boltzmann distribution. It's is much simpler to use the Boltzmann distribution than the Fermi-Dirac distribution. Therefore, normally in ATLAS simulation, Boltzmann statistics is the primary choice. But Fermi-Dirac statistics are very important when simulating highly-doped semiconductor material. It is much more accurate than the simplified equation (Boltzmann distribution) [11].

Software ATLAS Process

Figure 2-1 shows the procedure of ATLAS simulations. Most ATLAS simulations have two kinds of input files. One is the command input text of ATLAS grammar, the other one is the structure file defined in ATLAS environment. All the simulations in this research are in command text files.

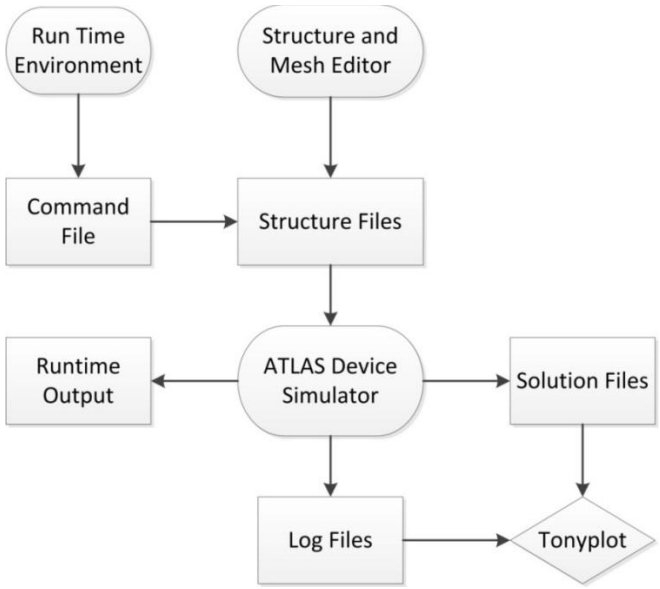

Figure 2-1. ATLAS Inputs and Outputs [6]

There are three types of output files: runtime output, log files and solutions files. Runtime output shows the details of simulation progress and warning or error messages when the simulation is running. Log file saves all the voltage and current data from the simulation calculations. The output file stores 2D and 3D data which are the values of solutions at a given bias voltage [12].

Order of ATLAS Commands

The order of ATLAS commands input shows the procedures of ATLAS working. There are five groups of statements defined in Table 1. If the order and command grammar are not obeyed, there may be an error or warning message leading to incorrect results or termination of the simulation.

Table 1. ATLAS Command Groups with the Primary Statements in each Group

Group	Statements
1. Structure Specification	MESH REGION ELECTRODE DOPING
2. Material Models Specification	MATERIAL MODELS CONTACT INTERFACE
3. Numerical Method Selection	METHOD
4. Solution Specification	LOG SOLVE LOAD SAVE
5. Results Analysis	EXTRACT TONYPLOT

For example, if the order of the mesh definition, structural definition, and solution groups are set in the incorrect order, then the program will be terminated [6].

In this section I discussed the basic semiconductor equations: Poisson's equation, carrier continuity equations, transport equations which are used in ATLAS simulation, drift-diffusion transport model, energy balance transport model are the models related to the transport method calculation. I also briefly introduced the ATLAS working procedures and commands order. The detail of simulations of MOSFET, BJT and JFET are analyzed in the next section.

CHAPTER 3

SIMULATION RESULT

Metal-Oxide-Semiconductor Field Effect Transistors

As mentioned earlier I am mainly interested in the behavior of the channel from source to drain with particular emphasis on the region near the drain before and after pinch off. This region is rarely shown or discussed in device physics books. [13]

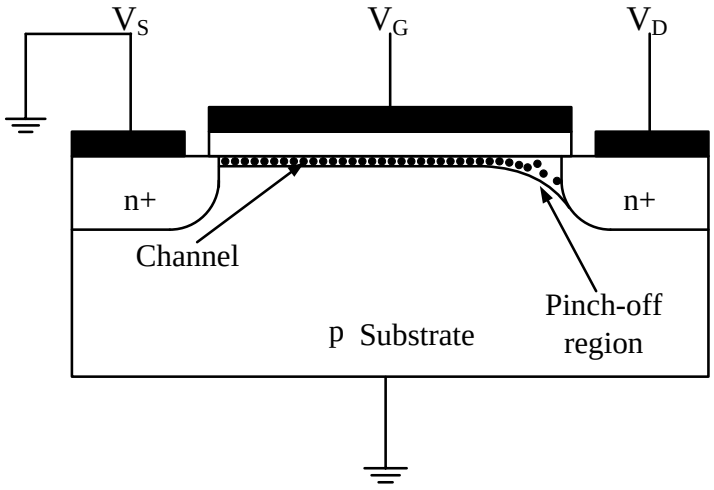

Figure 3-1. MOSFET with gate and drain voltage

Consider the MOSFET in Fig. 3-1 with $V_G=V_D$. Near the source, the gate voltage–induced vertical electric field is high, forcing the channel electrons towards the SiO_2/Si interface. At the drain end of the channel, however, the vertical electric field vanishes for $V_G=V_D$, and the channel spreads in the vertical direction. For $V_D=0$, the channel will, of course, be uniform from source to drain [3]. It is this channel behavior that is of main interest in these simulations.

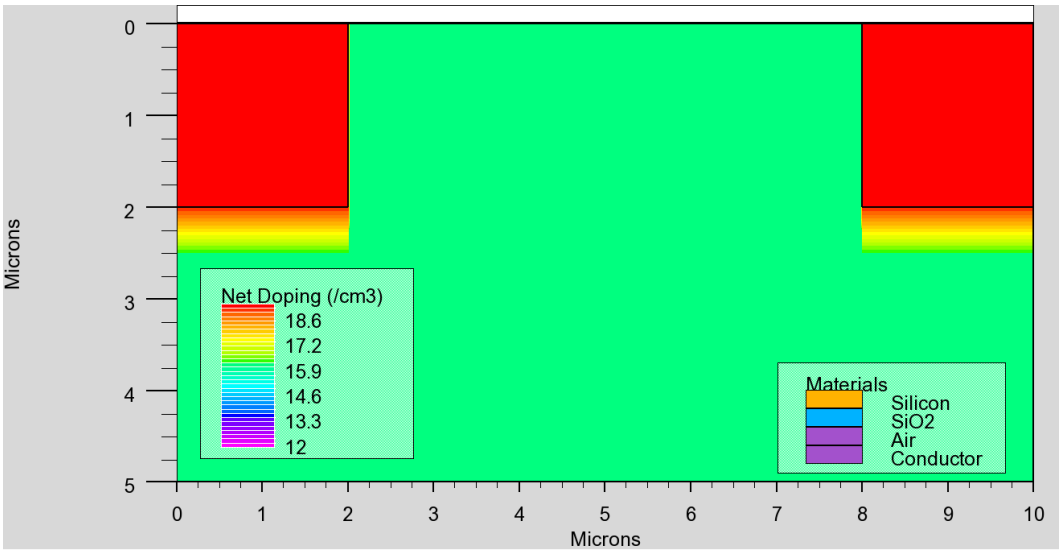

Figure 3-2. 2-D MOSFET structure and net doping concentrations

I simulated MOSFETs in two-dimensional structures as shown in Fig. 3-2. The substrate is p-type and the doping concentration is $10^{16}/\text{cm}^3$, the geometry is defined as 10 microns long, 5 microns deep. The source and drain are n-type and the doping concentration is $10^{19}/\text{cm}^3$, 2 microns long and 2 microns deep, which are implanted into the substrate at the upper left and right corners. A gate oxide 10 nm thick on the upper surface of the substrate between the source and drain has some overlap on the source and drain. All the contacts of gate, source and drain are Ohmic-contacts [14].

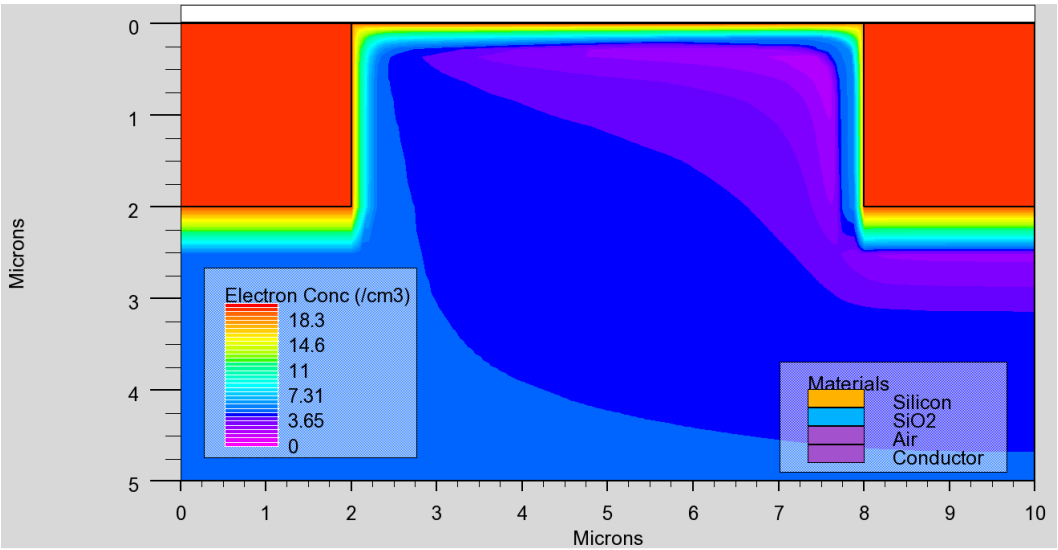

Figure 3-3. Electron concentration contour plot before pinch off, V_G=1.5V, V_D=1V

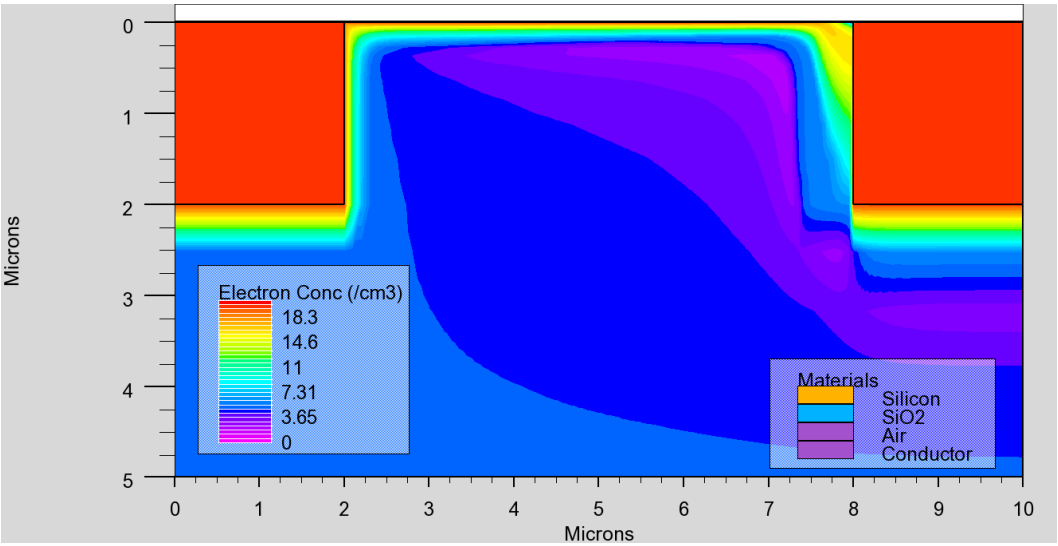

Figure 3-4. Electron concentration contour plot after pinch off, V_G=1.5V, V_D=5V

Figure 3-3 shows the electron concentration before pinch off, with V_G=1.5V and V_D=1V. Source and substrate are connected to ground. Compared with Fig. 3-3, Fig. 3-4 shows the electron concentration after pinch off, for the same gate voltage and V_D=5V. Let us focus on the channel pinch-off region to see the

difference of the channel shape before and after pinch off, shown in Figs. 3-5 and 3-6.

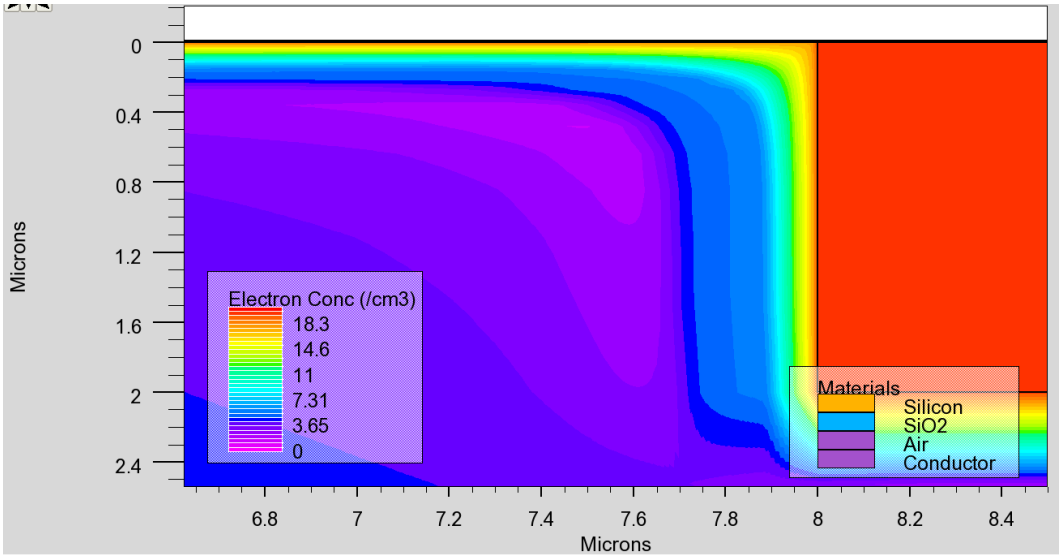

Figure 3-5. Electron concentration contour plot of pinch-off region before pinch off, V_G=1.5V, V_D=1V

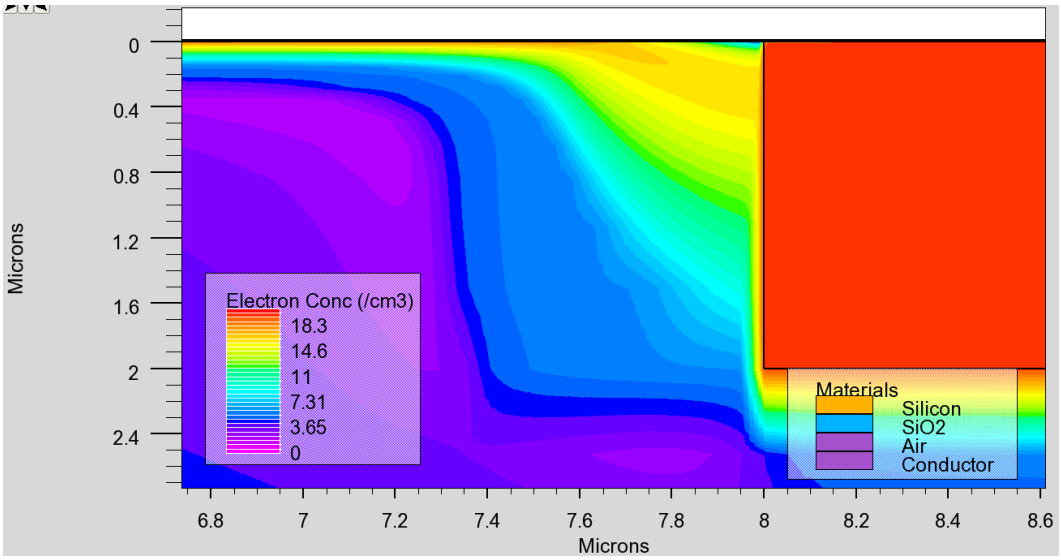

Figure 3-6. Electron concentration contour plot of pinch-off region after pinch off, V_G=1.5V, V_D=5V

It is clear that before pinch off, the channel thickness does not change much from source to drain. The closer the channel is to the SiO_2/Si interface, the higher the electron concentration, as shown in Fig. 3-5, the electron concentration decreases in the vertical direction as expected. However, after pinch off, the channel shape becomes triangular towards the drain; the electron concentration spreads out from the pinch-off point to the drain. In the triangular region, the electron concentration peak is no longer close to the SiO_2/Si interface, as shown in Fig. 3-6, with the electron concentration peak region bending down as it approaches the drain. Then the electron concentration above the peak region decreases rapidly and forms a low electron concentration triangular area at the corner next to the drain, as shown in Fig. 3-7.

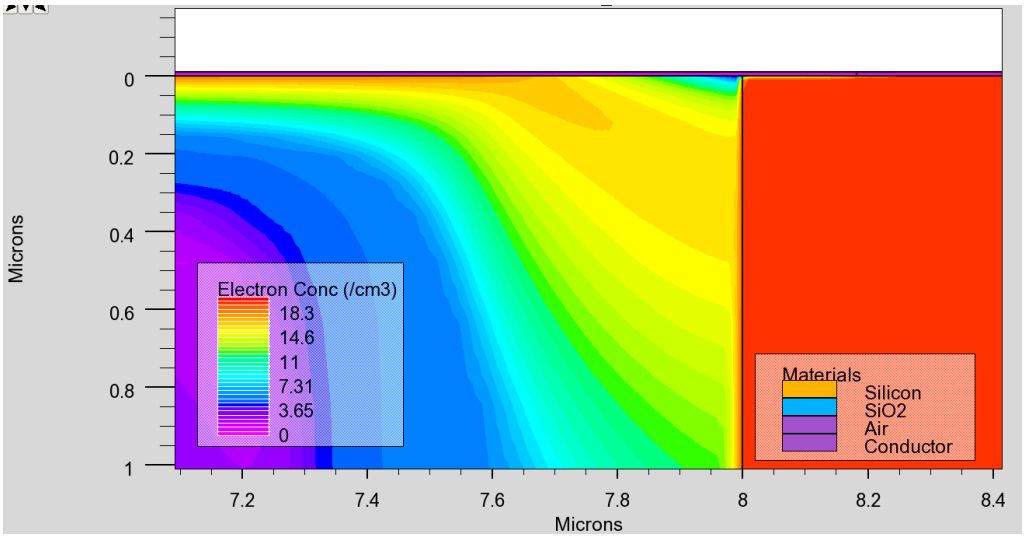

Figure 3-7. Electron concentration contour plot of pinch-off region after pinch off in the area next to the drain, V_G=1.5V, V_D=5V

Figures 3-8 and 3-9 show the horizontal cutline plots of electron concentration before and after pinch off. Comparing these two plots, I see that

either before or after pinch off, the electron concentration decreases from source to drain (before pinch-off point when after pinched off). In figure 3-9, after the pinch-off point the electron concentration falls sharply near the drain. The electron concentration is very sensitive to the distance from the SiO_2/Si interface. As shown in Fig. 3-10, at 0.025 microns below the interface near the source, the electron concentration drops fairly rapidly to $10^4/cm^3$, then Fig. 3-11 shows the vertical electron concentration around the pinch-off point, the electron concentration varies smoothly and at 1 micron below the interface the concentration is about $10^9/cm^3$, the peak is still at the SiO_2/Si interface. In Fig. 3-12, the vertical electron concentration plot close to the drain continuously expands and the peak moves away from the SiO_2/Si interface. That is the reason why in Fig. 3-9, the electron concentration falls sharply at 4 nm below the SiO_2/Si interface.

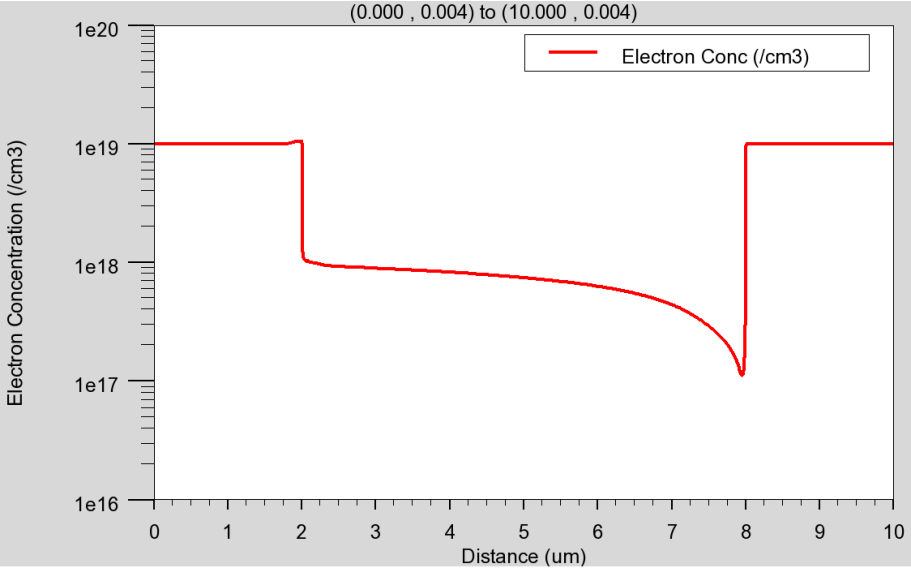

Figure 3-8. Electron concentration horizontal cutline plot before pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=1V

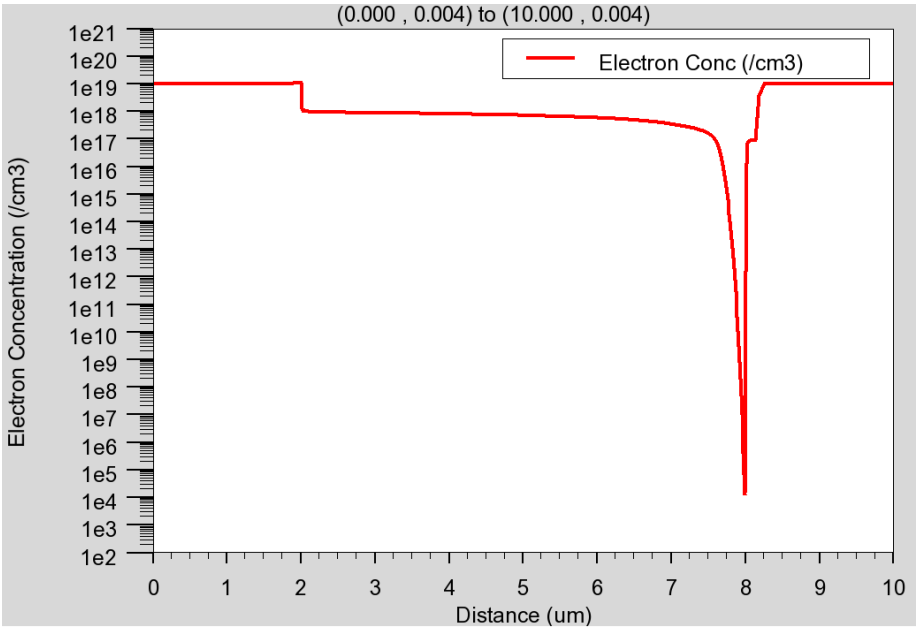

Figure 3-9. Electron concentration horizontal cutline plot after pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=5V

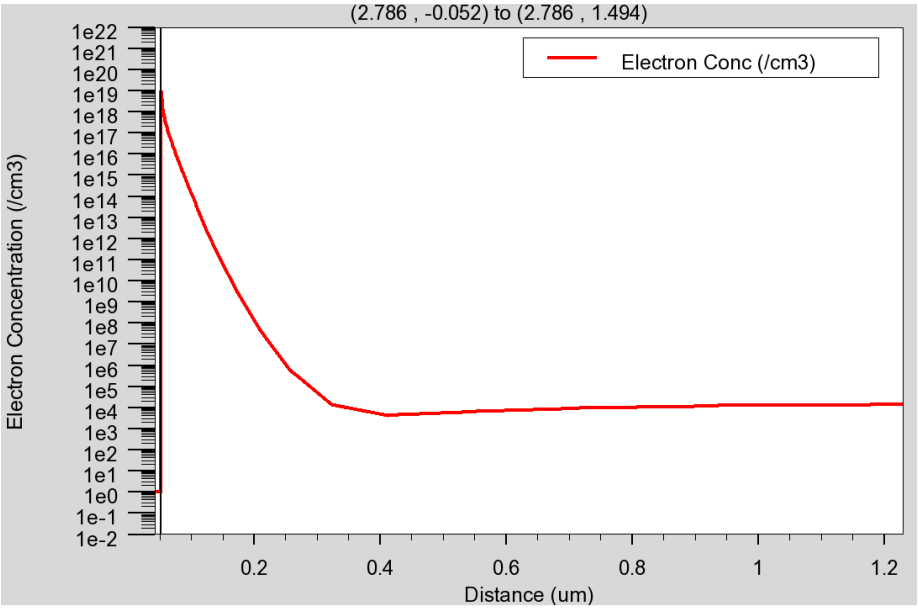

Figure 3-10. Electron concentration vertical cutline plot after pinch off at 2.786 microns near the source, V_G=1.5V, V_D=5V

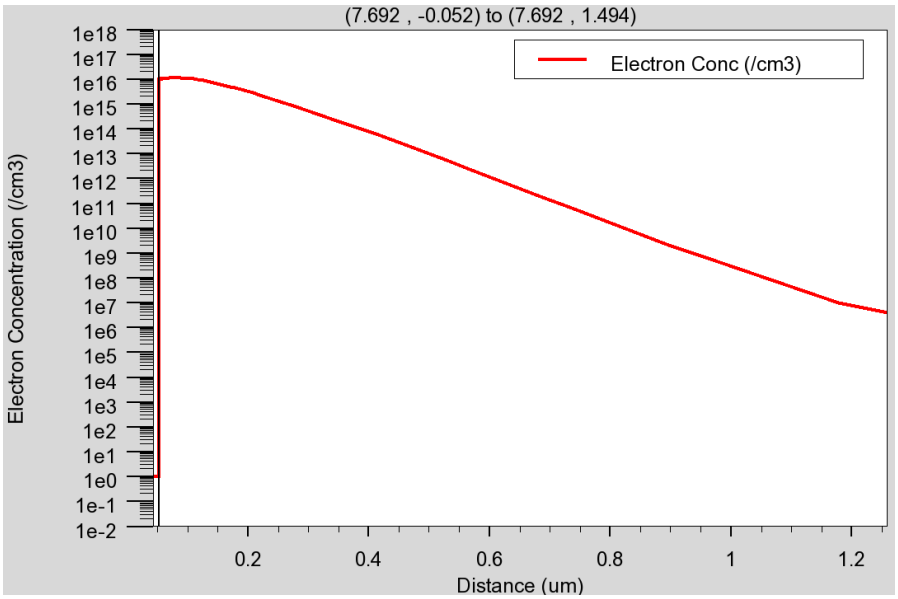

Figure 3-11. Electron concentration vertical cutline plot after pinch off at 7.692 microns around the pinch-off point, V_G=1.5V, V_D=5V

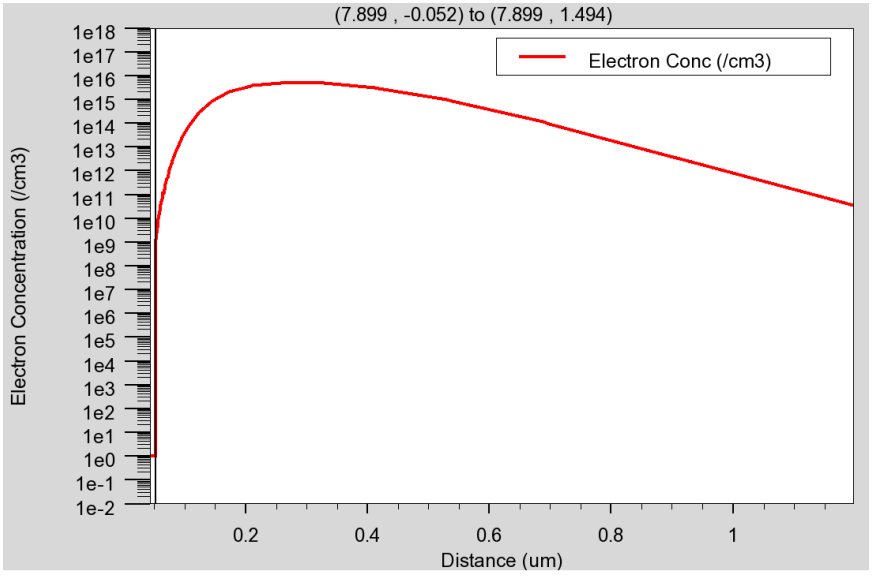

Figure 3-12. Electron concentration vertical cutline plot after pinch off at 7.899 microns near the drain, V_G=1.5V, V_D=5V

Figures 3-13 and 3-14 potential plots show the voltage drop from source to drain. Before pinch off, the potential curve slope varies fairly smoothly, but after pinch off, it drops very quickly in the "spread out" triangular area. Because of the high voltage drop in the pinch-off region, the electric field in the pinch-off region is very high.

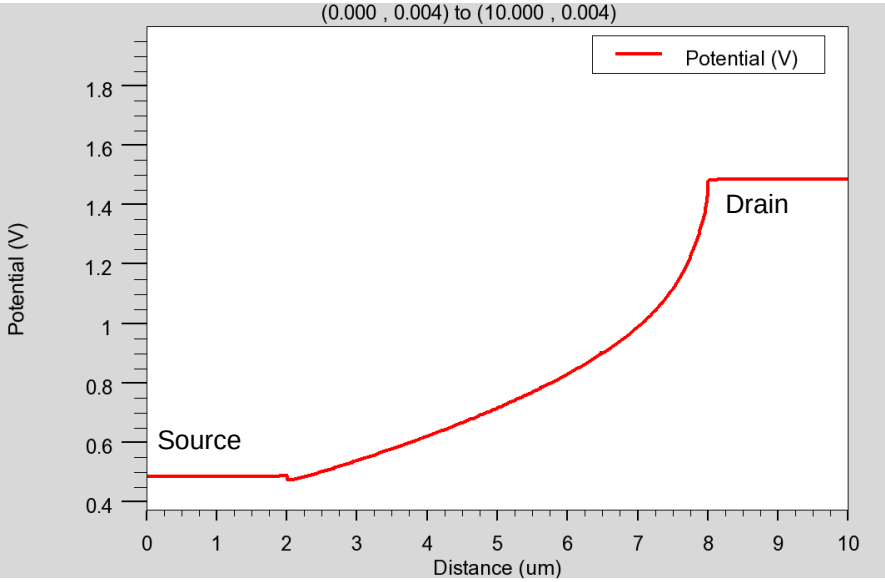

Figure 3-13. Potential horizontal cutline plot before pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=1V

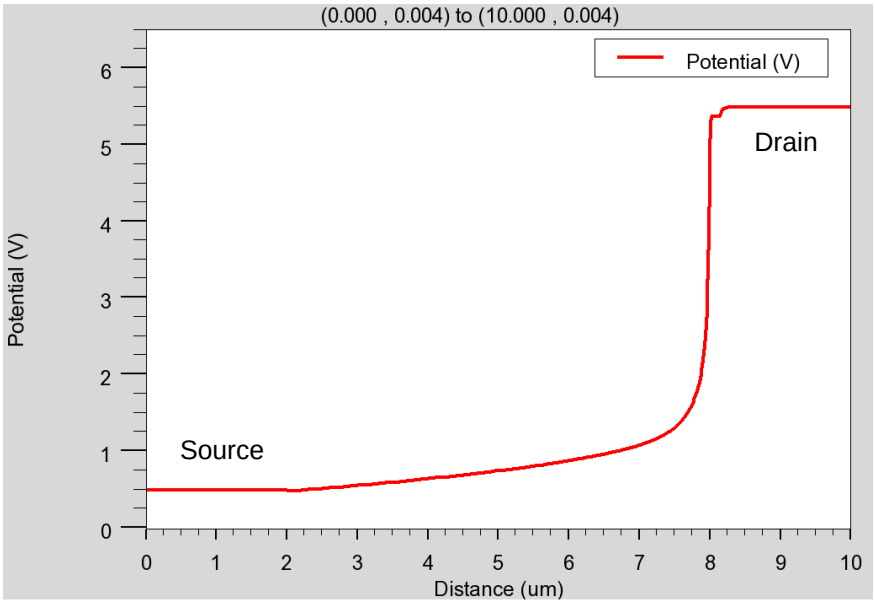

Figure 3-14. Potential horizontal cutline plot after pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=5V

As shown in Fig. 3-15, with a peak value of horizontal electric field about 5×10^4 V/cm, which is about one eighteenth of the peak value after pinch off in Fig. 3-16. The peaks near the source and drain are due to abrupt junctions, because of uniform doping, the step changes cannot be avoided. In Figures 3-17 and 3-18, the vertical electric field also decreases slightly as the potential increases in the channel before pinch off or before the pinch-off point after pinch off. After the pinch-off point, the vertical electric field becomes negative and the absolute value increases rapidly to 7×10^5 V/cm at the edge of the drain.

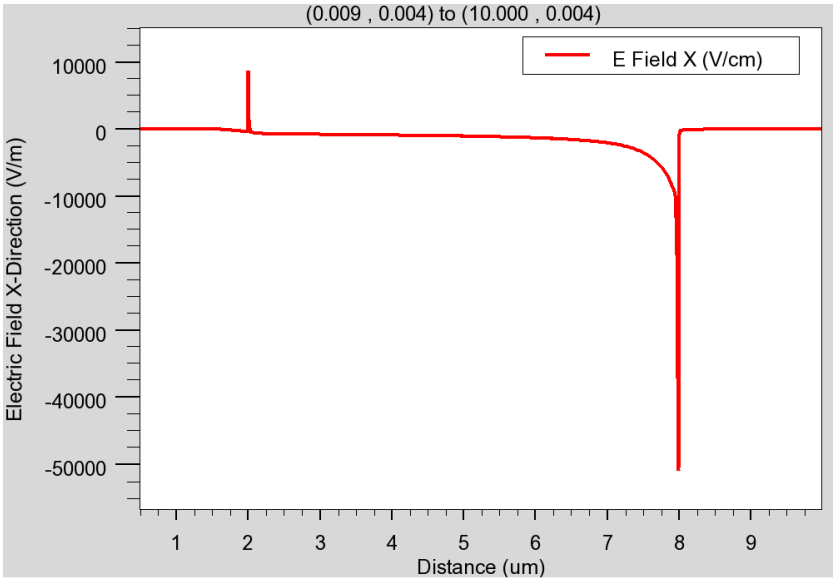

Figure 3-15. Horizontal electric field cutline plot before pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=1V

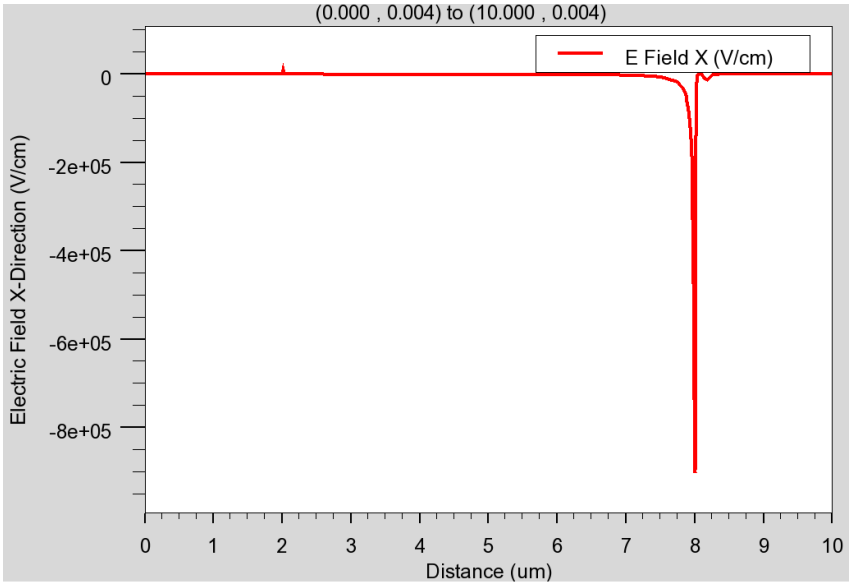

Figure 3-16. Horizontal electric field cutline plot after pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=5V

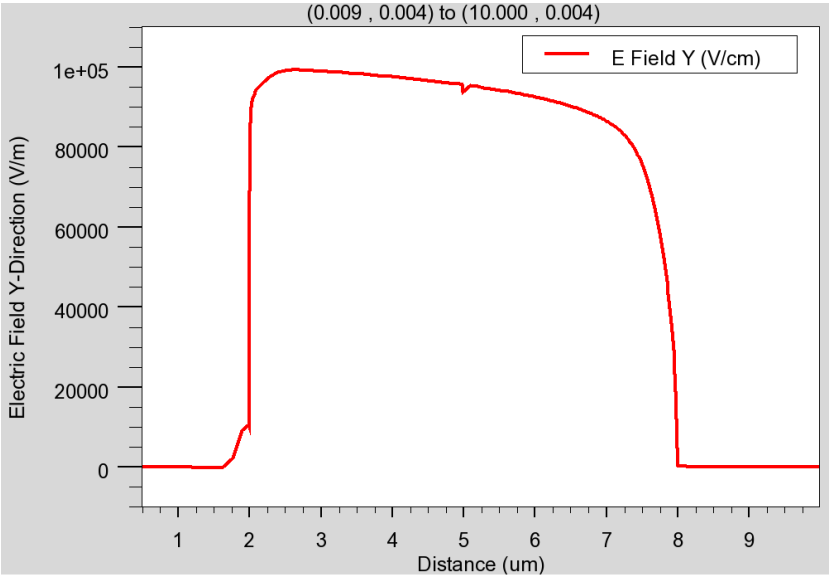

Figure 3-17. Vertical electric field cutline plot before pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=1V

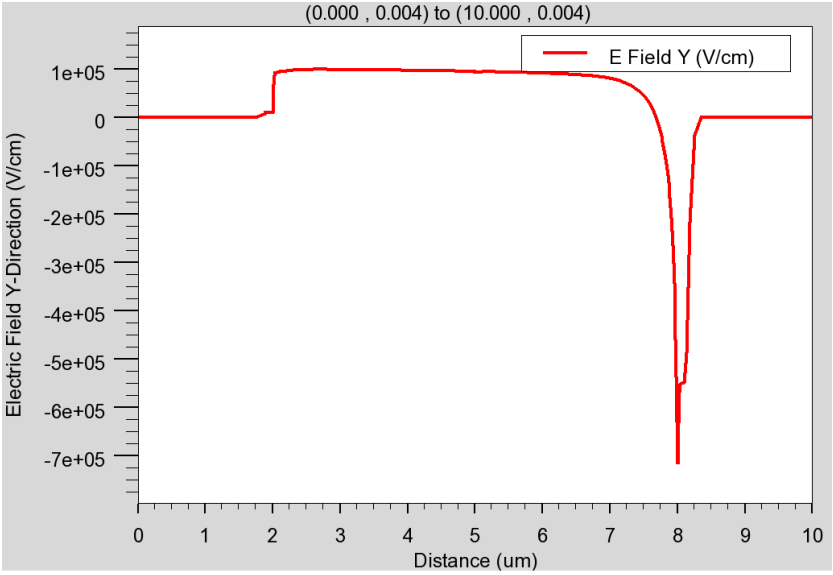

Figure 3-18. Vertical electric field cutline plot after pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=5V

Figures 3-19 and 3-20 show the total current density contour plots. The current density is higher when it close to the source and the peak is very close to

the SiO_2/Si interface, then the current density decreases and expands when it approaches the drain, and it decreases rapidly as the high density region disappears quickly after pinch off.

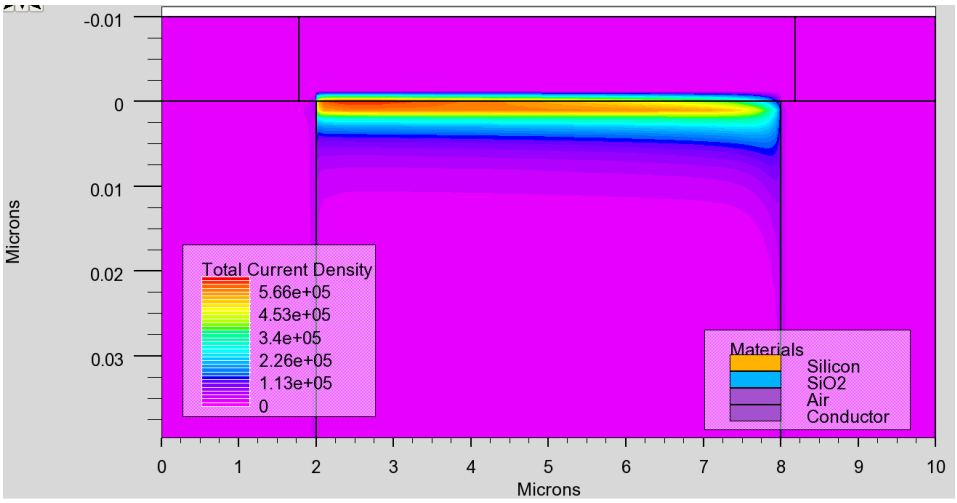

Figure 3-19. Total current density contour plot before pinch off, V_G=1.5V, V_D=1V

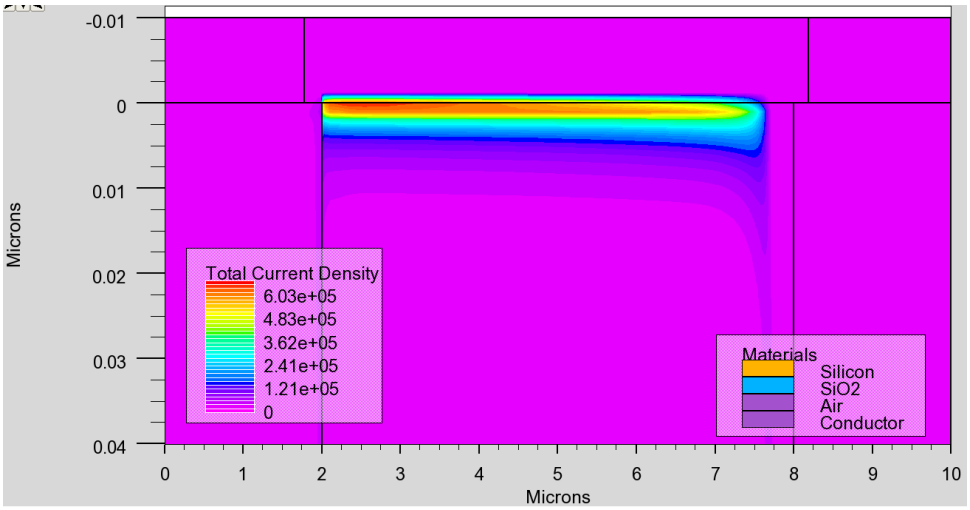

Figure 3-20. Total current density contour plot after pinch off, V_G=1.5V, V_D=5V

As shown in Figs. 3-21 to 3-26, the current density vertical distributions represent the channel shapes because most of the current flows through the

channel. Before pinch off, the channel expands slightly as the potential in the channel increases from source to drain; the peak of the current density moves away from the SiO_2/Si interface from source to drain because the vertical electric field decreases from source to drain, leading to less and less attraction to electrons. Then after pinch off, the vertical electric field becomes negative and decreases rapidly, the peak of the current density moves away from the interface and decreases. The distribution spread out is shown in Fig. 3-26.

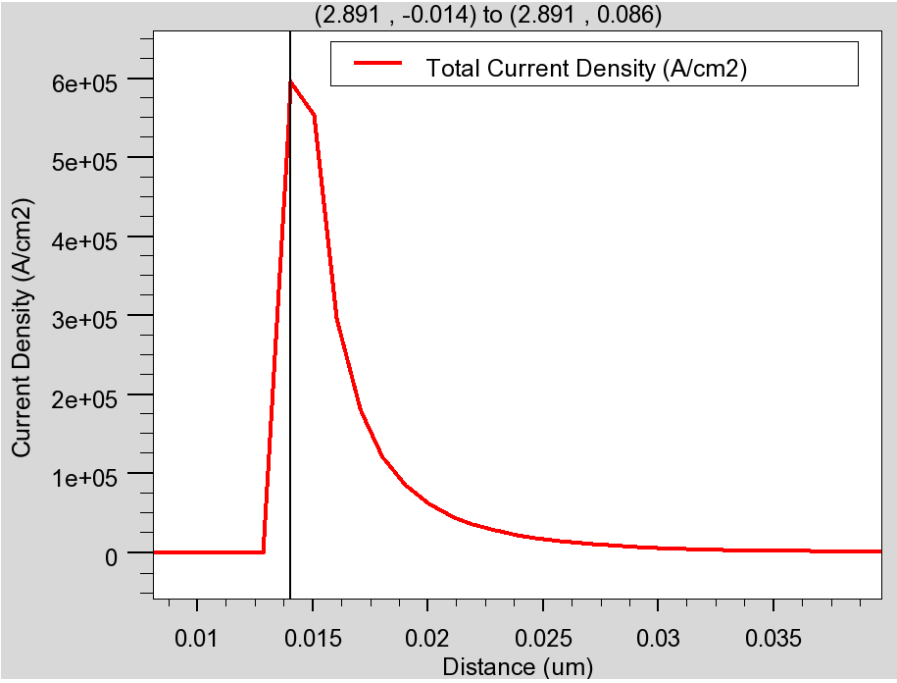

Figure 3-21. Total current density vertical cutline plot before pinch off at 2.891 microns near the source, V_G=1.5V, V_D=1V

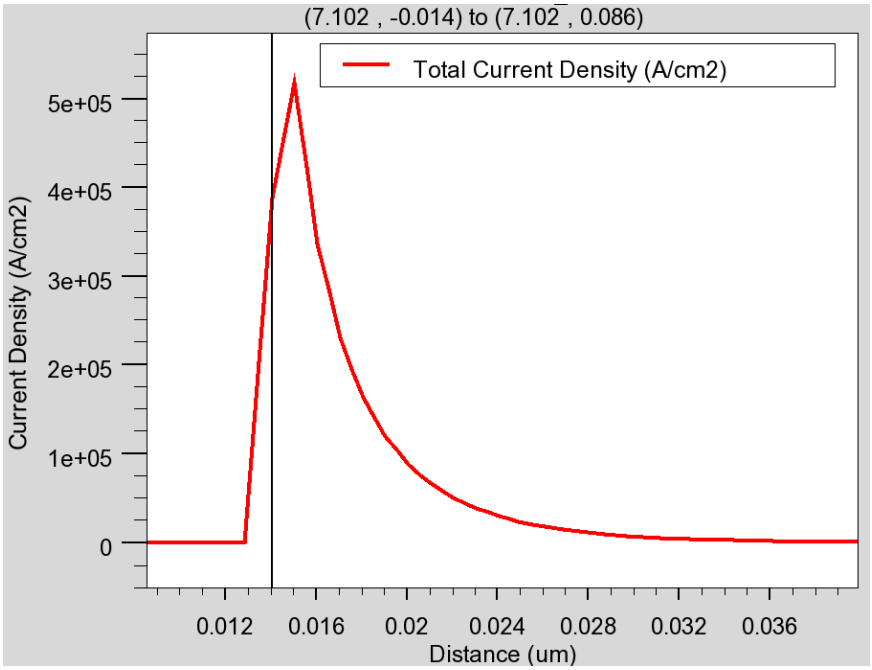

Figure 3-22. Total current density vertical cutline plot before pinch off at 7.102 microns near the drain, V_G=1.5V, V_D=1V

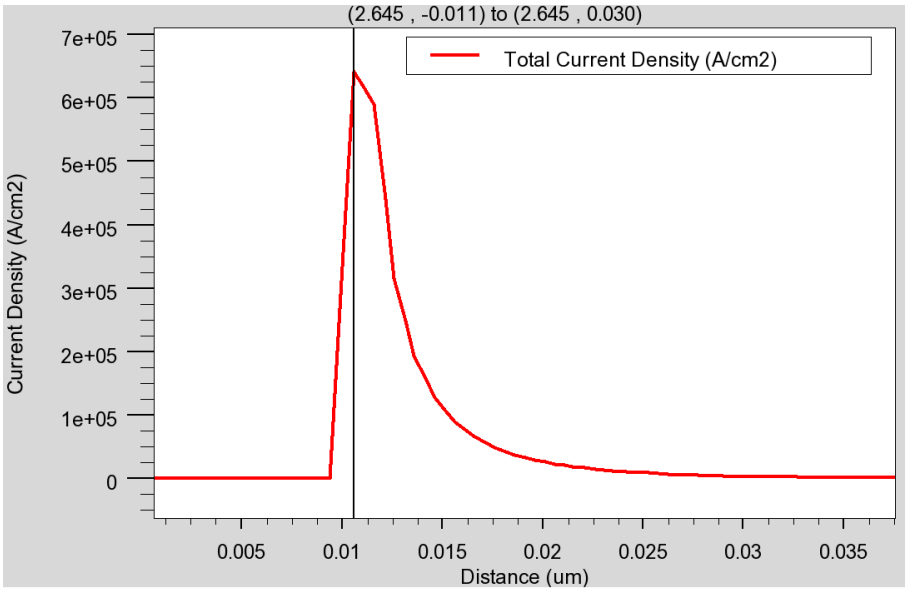

Figure 3-23. Total current density vertical cutline plot after pinch off at 2.645 microns near the source, V_G=1.5V, V_D=5V

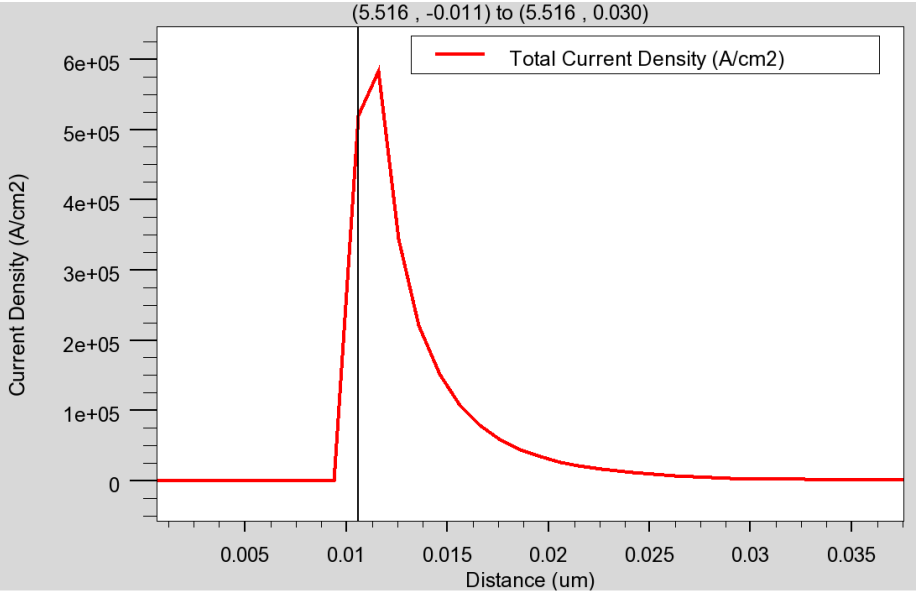

Figure 3-24. Total current density vertical cutline plot after pinch off at 5.516 microns in the middle, V_G=1.5V, V_D=5V

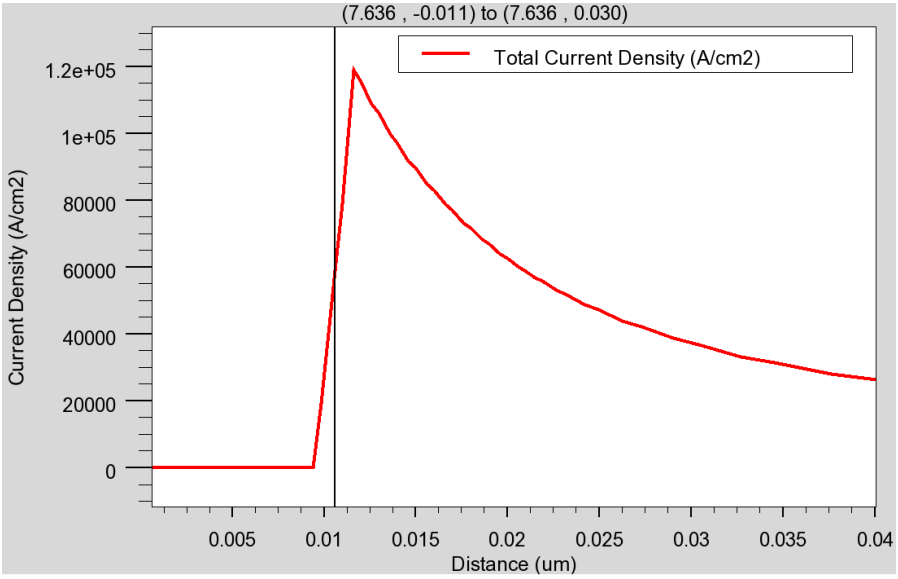

Figure 3-25. Total current density vertical cutline plot after pinch off at 7.636 microns around the pinch-off point, V_G=1.5V, V_D=5V

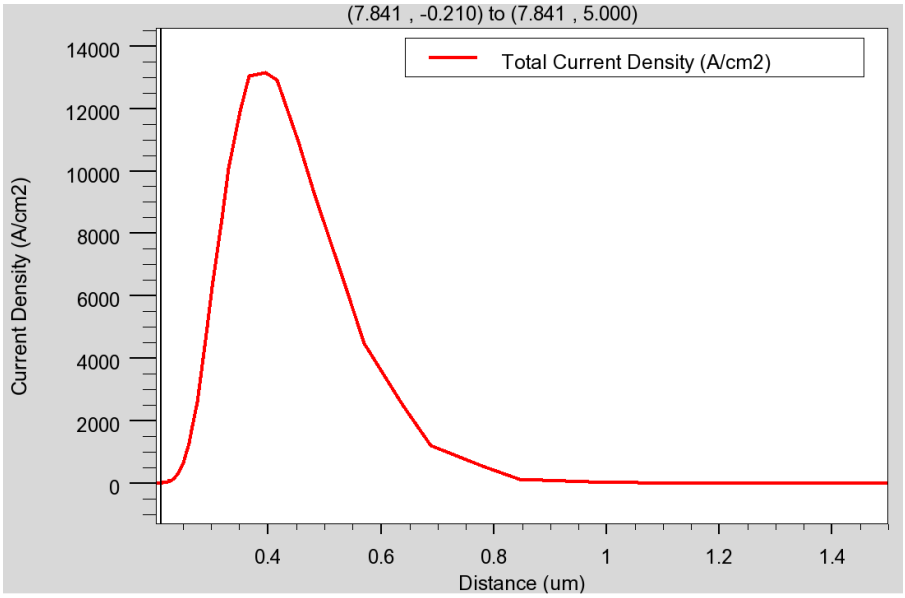

Figure 3-26. Total current density vertical cutline plot after pinch off at 7.841 microns near the drain, V_G=1.5V, V_D=5V

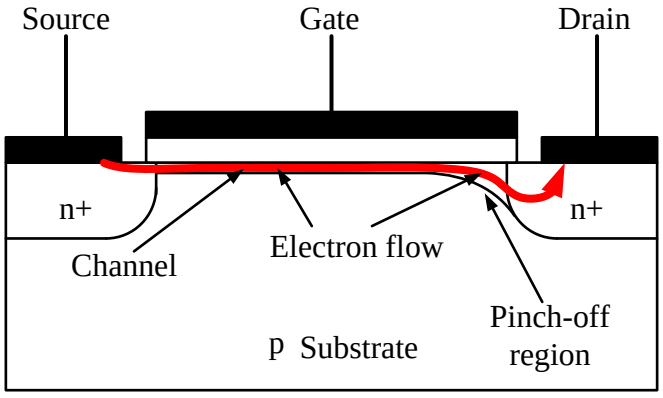

Figure 3-27. Current flow path from source to drain

After pinch off, the total current density cutline plots from Figs. 3-23 to 3-26 show how the current flows from source to drain. The electron flow is shown schematically in Fig. 3-27. Electrons flow close to the SiO_2/Si interface for most of the channel length and then spread out towards the drain.

The band diagram in Fig. 3-28 shows a small discontinuity at the source/substrate interface. This is due to a slight band gap narrowing of the

heavily-doped source. The electron quasi-Fermi level (QFL) lies quite parallel to the conduction band. The hole quasi-Fermi level, however, lies above the electron QFL. This can be understood from the equation [3]

$$p = n_i \exp\left(E_i - E_{Fp}\right)/kT \tag{3.1}$$

which gives the location of the hole QFL E_{Fp} as

$$E_{Fp} = E_i - kT\ln\left(\frac{p}{n_i}\right) \tag{3.2}$$

In a neutral semiconductor, where $p \gg n_i$, E_{Fp} lies below E_i. However, in the n-channel the hole concentration is well below n_i. For example, for $p = 1\ cm^{-3}$, I find

$$E_{Fp} = E_i + 0.59eV \tag{3.3}$$

for Si with $n_i = 10^{10} cm^{-3}$. This equation shows that E_{Fp} lies close to or even inside the conduction band as shown in Fig. 3-28. It is interesting to note that the electron and hole QFLs diverge in the channel from the source to approximately the middle of the channel and then remain reasonably constant to the drain.

As the drain voltage is increased to 5V, the electron QFL moves close to E_V and the hole QFL moves close to E_C, illustrated in Figs. 3-29 and 3-30 near the drain. The electron QFL is [3]

$$E_{Fn} = E_i + kT\ln\left(\frac{n}{n_i}\right) \tag{3.4}$$

leading to

$$E_{Fn} = E_i - 0.59eV \tag{3.5}$$

for $n = 1\ cm^{-3}$.

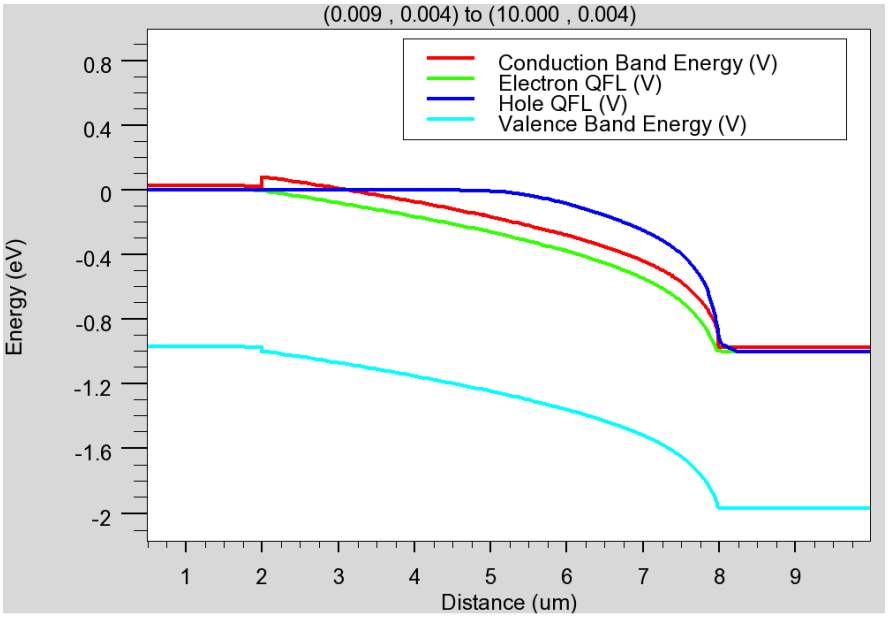

Figure 3-28. Band diagram of horizontal cutline before pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=1V

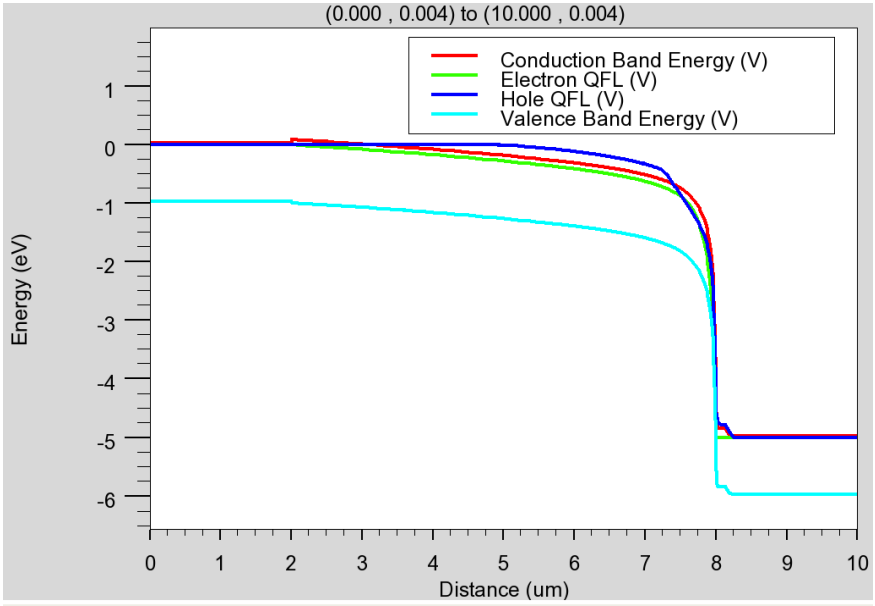

Figure 3-29. Band diagram of horizontal cutline after pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=5V

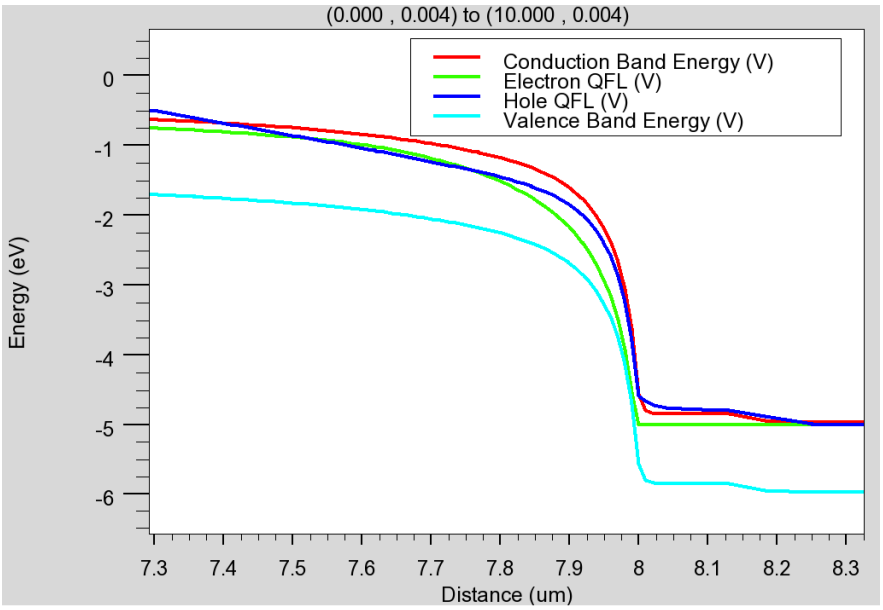

Figure 3-30. Enlarged view of the band diagram of horizontal cutline near the drain after pinch off at 4 nm below the SiO_2/Si interface, V_G=1.5V, V_D=5V

Figure 3-31 shows the I-V curve of the MOSFET. The saturation gate voltage is about 0.8 V. After saturation, due to the Early effect [15], there is a non-zero slope of the drain current.

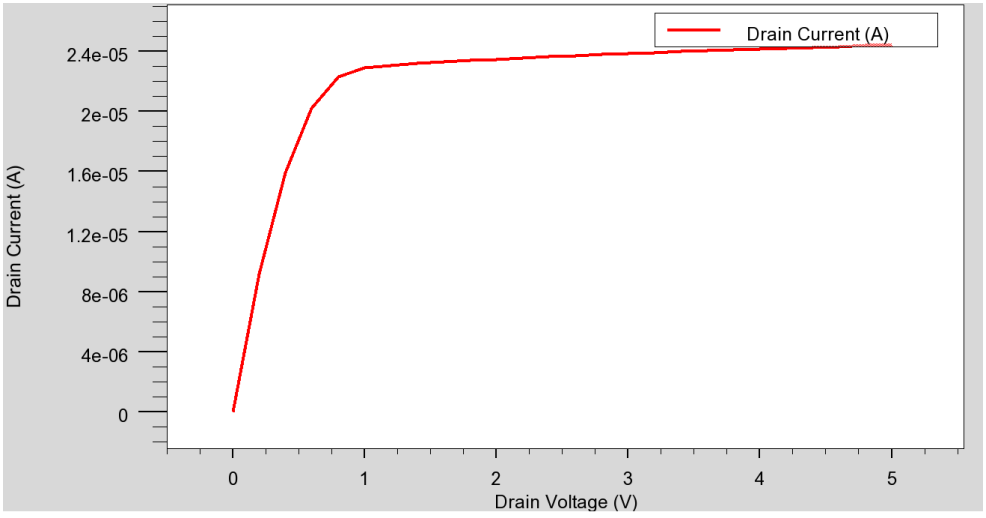

Figure 3-31. I-V curve of MOSFET, V_G=1.5V, V_D=0 to 5V

In conclusion, the MOSFET channel expands slightly before the pinch-off point and then spreads out quickly in a triangular shape near the drain. The electron concentration plot shows the space-charge region expands as the potential increases from source to drain. The gate voltage induced vertical electric field is reduced from source to drain. When the vertical electric field disappears, the traditional "channel" disappears and the current spreads out as it approaches the drain. The real channel expands as shown in Fig. 3-32. Actually the channel is very thin, it is about 10 nanometers.

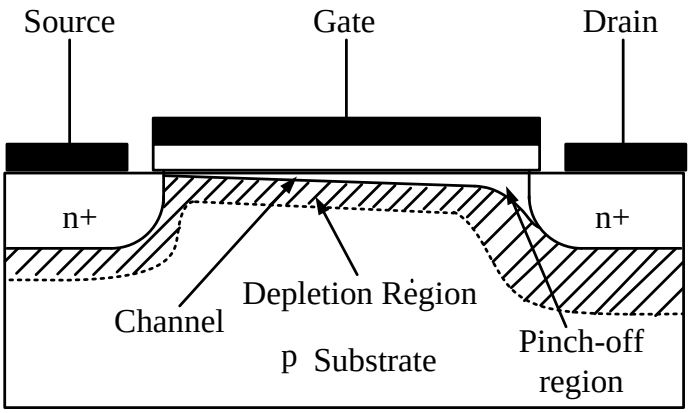

Figure 3-32. MOSFET real shapes of the channel

However, real MOSFET channels are not 6 microns long. The modern MOSFETs have already reached nanometers scaling. Hence, I simulated the MOSFETs of 30 nm channel length. The substrate is p-type and the doping concentration is $10^{18}/\mathrm{cm}^3$, the source and drain are n-type and the doping concentration is $10^{20}/\mathrm{cm}^3$, the gate oxide is 1.5 nm thick.

Figure 3-33 shows the electron concentration contour plot, which is similar to Fig. 3-4. Due to the scaling, the channel-region doping concentration is increased to prevent punch-through.

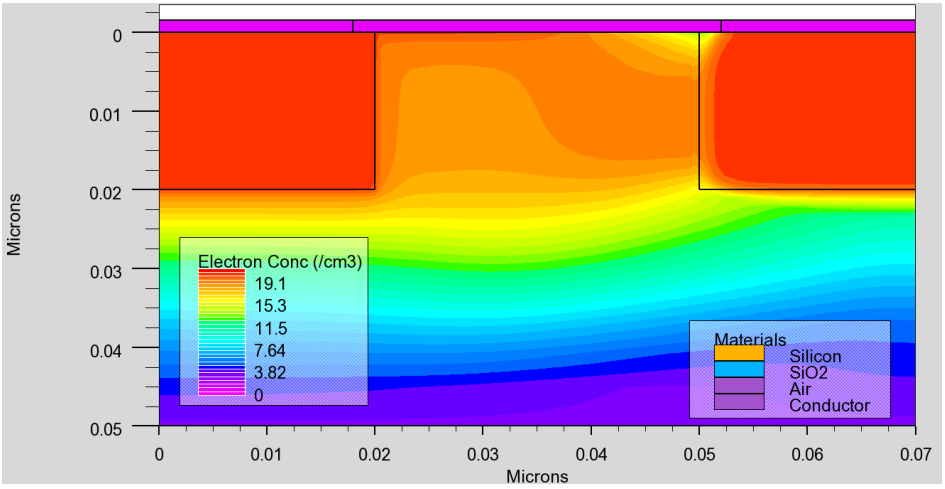

Figure 3-33. Electron concentration contour plot after pinch off, V_G=1V, V_D=2.5V

Figure 3-34 shows the current density contour plot. The channel expands from source to drain and spreads out after the pinch-off point, which is similar to the current flow in Fig. 3-20.

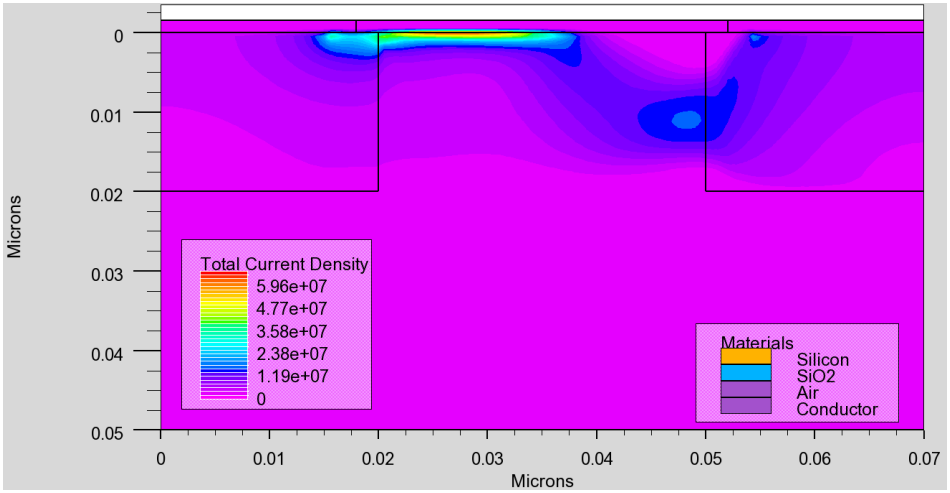

Figure 3-34. Total current density contour plot after pinch off, V_G=1V, V_D=2.5V

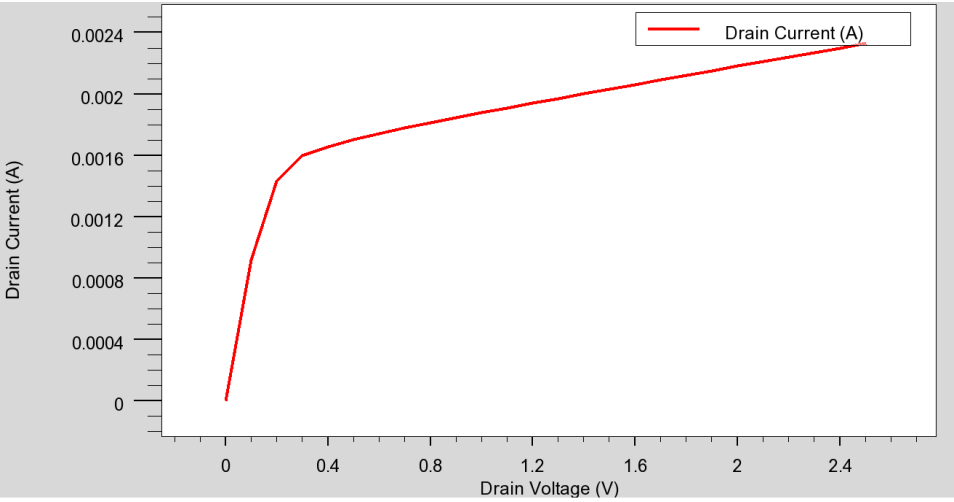

Figure 3-35. I-V curve of MOSFET, V_G=1V, V_D=0 to 2.5V

Compared to Fig. 3-31, the I-V curve of nanometer scaled MOSFET in Fig 3-35 has a higher slope. Because the channel is much shorter, the current is higher and also due to the Early effect [15], it has a higher slope after the saturation point.

Bipolar Junction Transistors

In bipolar junction transistors, the region of my interest is the base-collector space-charge region (scr) and the base near that scr. In particular, the behavior of the base minority carriers as they approach the b-c scr and as they drift through that scr. The simple analysis says that the minority carrier density tends to zero as the carriers approach the b-c scr and that velocity tends to infinity [16]. Neither of these approximations is, of course, real.

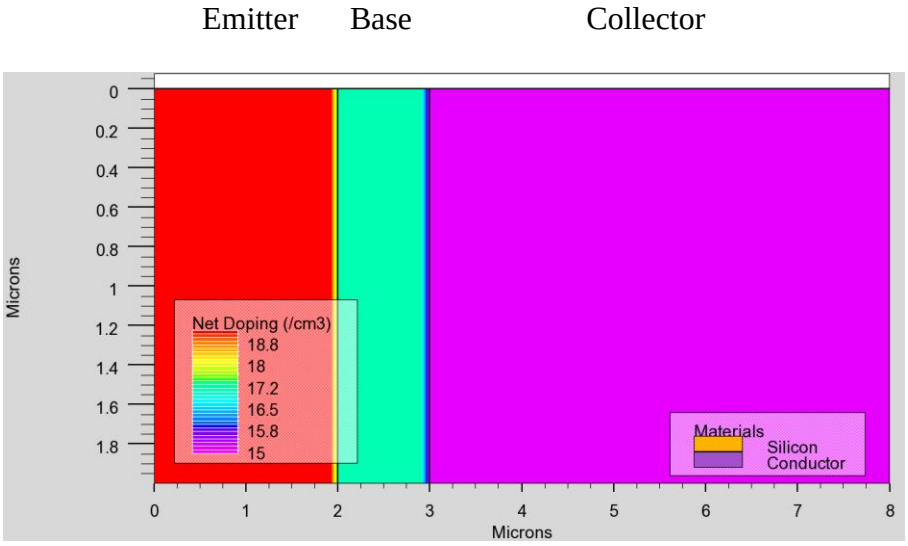

Figure 3-36. 2-D BJT structure and net doping concentrations

I simulated the two-dimensional BJT structure shown in Fig. 3-36. The base width is 1 micron. The emitter is p-type and the doping concentration is $10^{19}/\text{cm}^3$, it is 2 microns long. The base is n-type with doping concentration of $10^{17}/\text{cm}^3$, 1 micron wide. The collector is p-type with doping concentration of $10^{15}/\text{cm}^3$, 5 microns long. The emitter, base and collector contacts are Ohmic-contacts, and due to the symmetrical structure, both top and bottom sides of the base have contacts [17] [18].

Figure 3-37 shows the hole concentration in the emitter, base and collector in the common base connection, the emitter-base junction is forward biased to 0.7 V, and the collector-base junction is also forward biased to 1 V. Holes are injected from the emitter and the collector into the base, and the hole concentration in the base is about $10^{13} - 10^{15}/\text{cm}^3$(Fig. 3-39) and the c-b space-charge region is very narrow because the c-b junction is forward biased. Figure 3-38 is also in the common base connection as in Fig. 3-37, but the collector-base junction is reverse

biased to -5 V. The hole concentration in the base is about $10^{13} - 10^{15}/\text{cm}^3$(Fig. 3-40) too, but the c-b space-charge region is much wider because the c-b junction reverse biased.

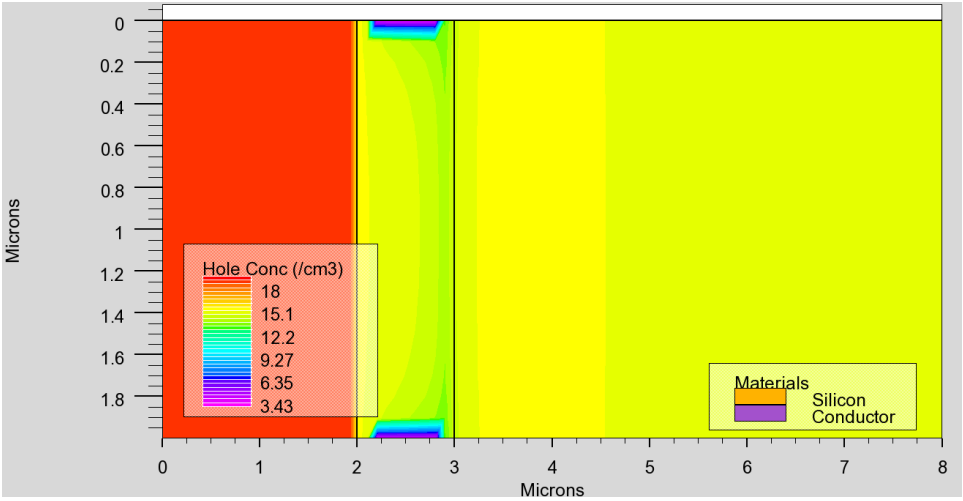

Figure 3-37. Hole concentration contour plot with e-b and c-b forward biased, V_{EB}=0.7V, V_{CB}=0.5V

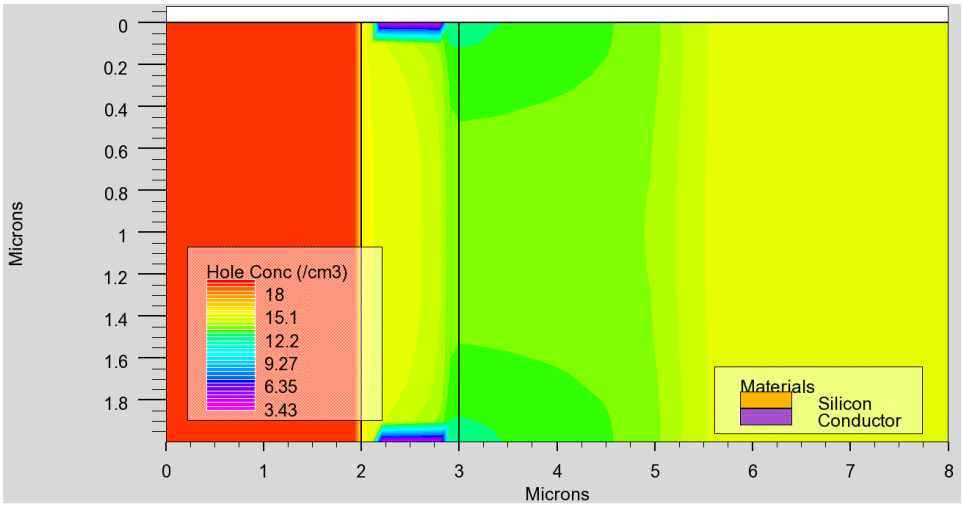

Figure 3-38. Hole concentration contour plot with e-b forward biased and c-b reverse biased, V_{EB}=0.7V, V_{CB}=–5V

The hole concentration cutline plot is shown in Figs. 3-39 and 3-40. The hole concentration in the base at the e-b scr edge is ~ $10^{15}/\mathrm{cm}^3$(equilibrium value $p_{n0} = 10^3/\mathrm{cm}^3$) and decreases towards the collector where it reaches ~ $2 \times 10^{13}/\mathrm{cm}^3$ at the b-c scr edge. The value $p_n(0) \approx 10^{15}/\mathrm{cm}^3$ is approximately consistent with $p_n(0) = p_{n0}\exp(qV_{EB}/kT) = 5.7 \times 10^{14}/\mathrm{cm}^3$. For V_{EB}=0.5 V, the hole concentration $p_n(0)$ decreases from $10^{15}/\mathrm{cm}^3$ to $2 \times 10^{11}/\mathrm{cm}^3$, the curve shape is similar. This shows that the minority carrier concentration in the base at the b-c scr edge is clearly not zero as usually assumed in textbooks, although it is quite low. On the other side of the c-b space-charge region in the collector, when reverse biased, the electron concentration (minority carriers) in the collector increases from $10^4/\mathrm{cm}^3$ to $10^5/\mathrm{cm}^3$. As shown in Fig. 3-38, near the base contacts and collector there are two fan shaped regions. Because the most of the current flows in the middle the base diffuses through the base, the holes diffuse near the base will be collected by the base, therefore, the hole concentrations in the fan shaped regions are lower.

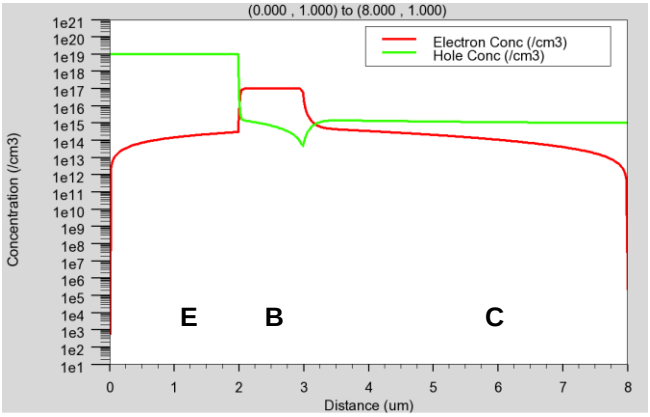

Figure 3-39. Hole concentration horizontal cutline plot with e-b and c-b forward biased, V_{EB}=0.7V, V_{CB}=0.5V

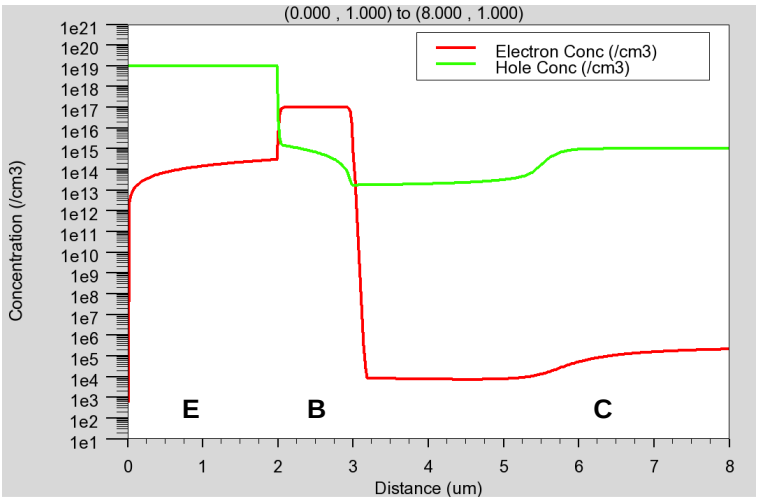

Figure 3-40. Hole concentration contour plot with e-b forward biased and c-b reverse biased, V_{EB}=0.7V, V_{CB}=–5V

The potential plots in Figs. 3-41 and 3-42 show the barriers at the e-b junction which the holes injected from the emitter into the base have to surmount to be collected in the collector. The barrier height at the e-b junction is unchanged since V_{EB} is constant, but the b-c barriers height changes with V_{CB}.

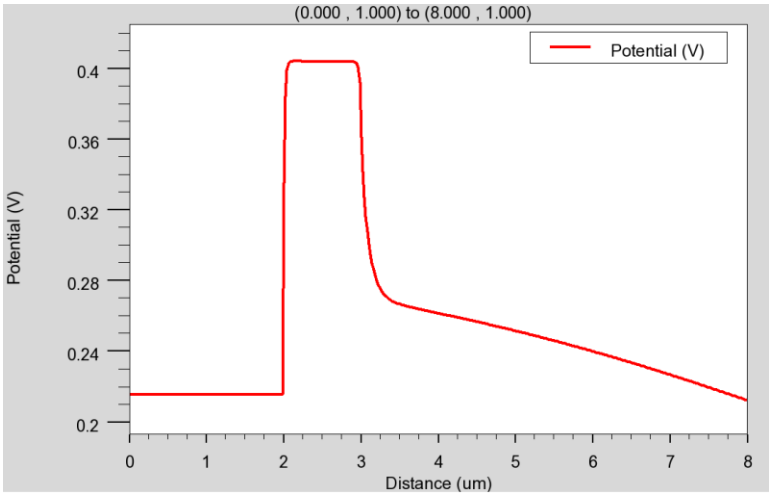

Figure 3-41. Potential horizontal cutline plot with e-b and c-b forward biased, V_{EB}=0.7V, V_{CB}=0.5V

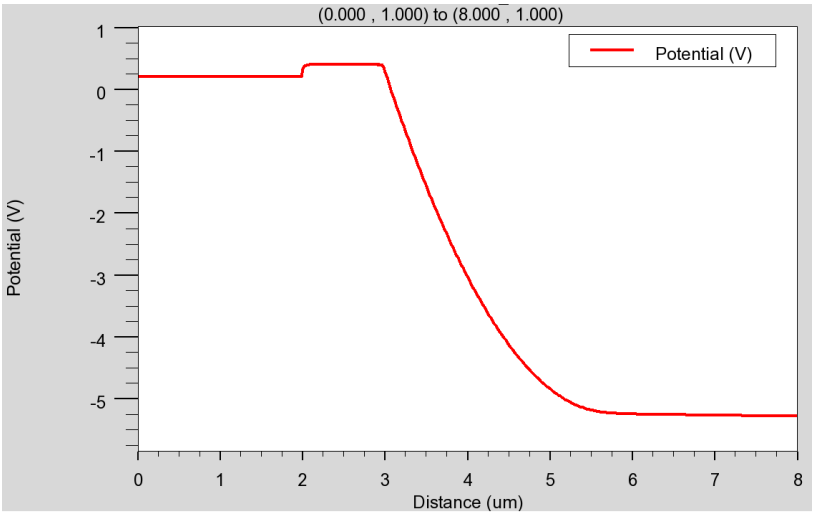

Figure 3-42. Potential horizontal cutline plot with e-b forward biased and c-b reverse biased, V_{EB}=0.7V, V_{CB}=–5V

The electric field plots are shown in Figs. 3-43 and 3-44. For the same V_{EB}, both plots have the same peak value about 55,000 V/cm at the e-b junction. The doping concentrations of emitter, base and collector are: $10^{19}/\text{cm}^3$, $10^{17}/\text{cm}^3$, $10^{15}/\text{cm}^3$. When the c-b is reverse biased, the c-b space-charge region extends mainly into the collector as shown in Fig. 3-44. The electric field in the reverse-biased c-b scr approximates a triangular shape, as predicted by first-order equations in the depletion approximation.

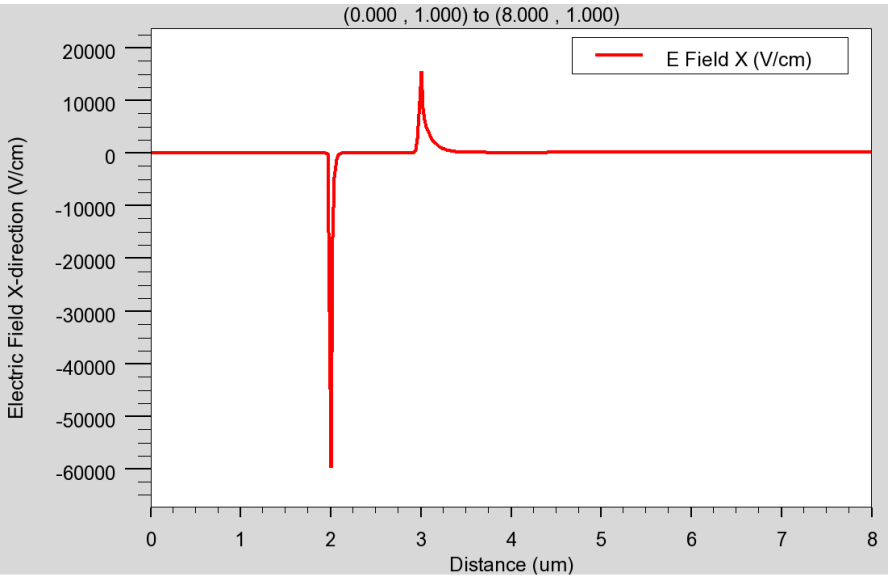

Figure 3-43. Horizontal electric field cutline plot with e-b and c-b forward biased, V_{EB}=0.7V, V_{CB}=0.5V

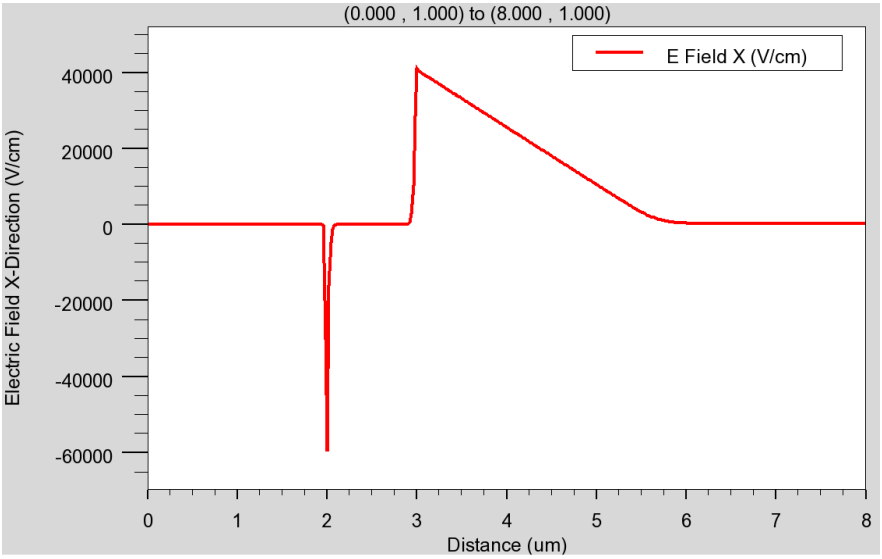

Figure 3-44. Electric field horizontal cutline plot with e-b forward biased and c-b reverse biased, V_{EB}=0.7V, V_{CB}=–5V

Figures 3-45 and 3-46 show the current density plots. The current density increases in the emitter and reaches a peak value at e-b junction then decreases

linearly in the base and then keeps spreading out in the collector. In the base, the collector current is [3]

$$I_{Cp} = -qAD_B \frac{dp_B}{dx} \tag{3.6}$$

From the Fig. 3-40, the hole concentration in the base decreases linearly (shown in Fig. 3-40 as nonlinear in logplot). The current through the device is constant. However, the current density plots of Figs. 3-45 and 3-46 are not constant, although the variation is small (~7%). Since the current density is [3]

$$J_{Cp} = I_{Cp}/A \tag{3.7}$$

it means the area of current flow changes slightly through the device. The color variation on the contour plots is too small to see these area changes.

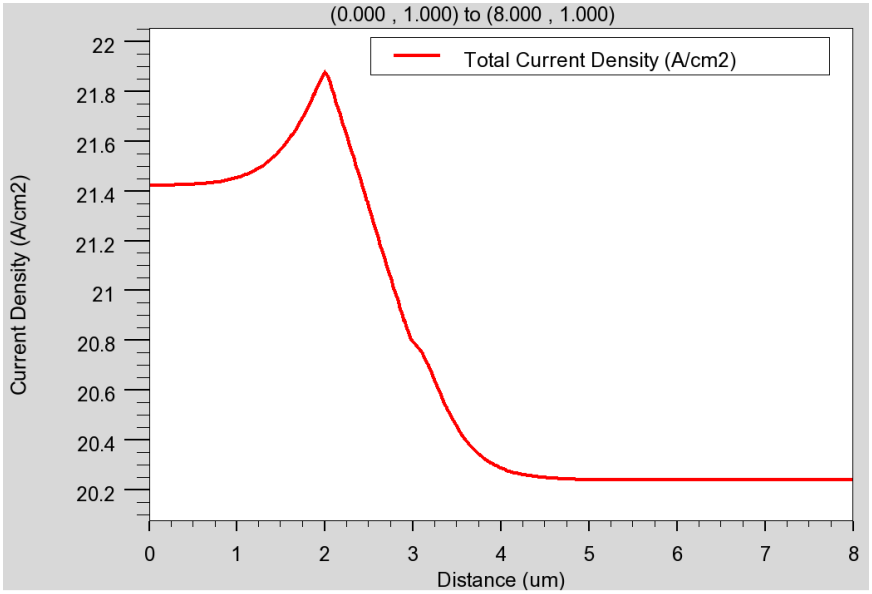

Figure 3-45. Total current density horizontal cutline plot with e-b and c-b forward biased, V_{EB}=0.7V, V_{CB}=0.5V

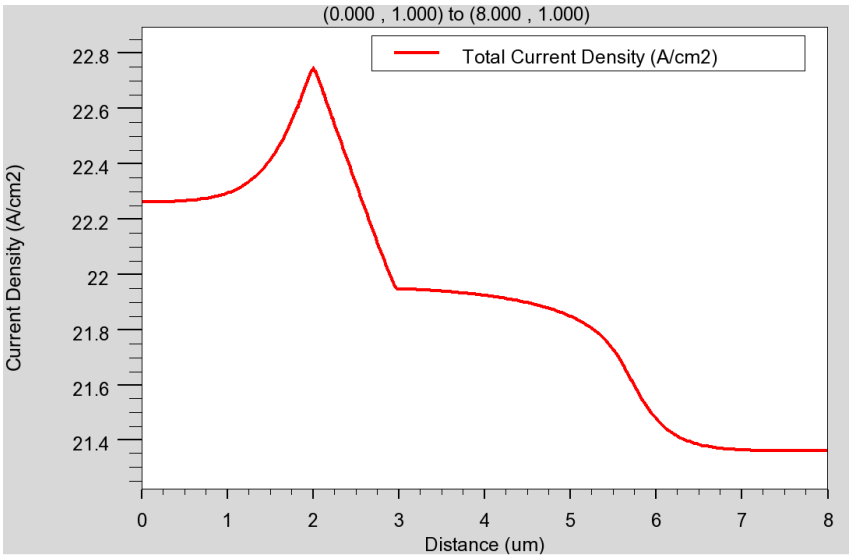

Figure 3-46. Total current density horizontal cutline plot with e-b forward biased and c-b reverse biased, V_{EB}=0.7V, V_{CB}=–5V

Figures 3-47, 3-48 and 3-49 show the band diagrams. In Fig. 3-47, the electron quasi-Fermi level and hole quasi-Fermi level split at the beginning of the emitter, and join again at the collector ohmic contact. In Fig. 3-48, the e-b junction is zero biased with no Fermi level splitting as expected. In the reverse-biased c-b scr, the hole QFL is close to the conduction band and the electron QFL is close to the valence band in agreement with Eqs. (3-2) and (3-4). The base-collector junction is just a simple diode in this case, with very few electrons and holes in the scr.

In Fig. 3-49, however, holes from the emitter drift through the c-b scr and the hole QFL shifts towards the valence band. The electron QFL remains relatively unchanged. The QFLs in the emitter and the e-b scr are now split by the forward bias with their separation approximately equal to V_{EB}. These plots show very

clearly how the QFLs behave with few and many holes in a reverse-biased scr. Such plots are almost never shown in textbooks.

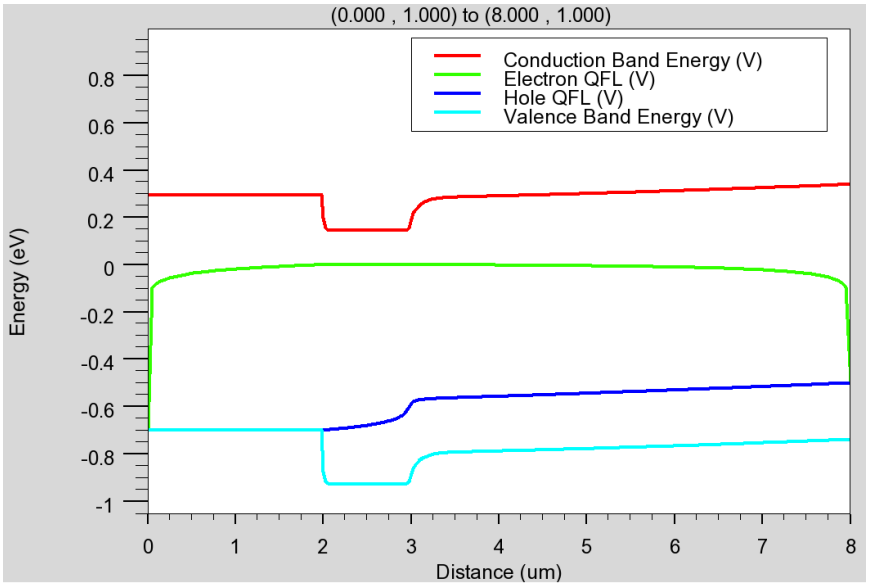

Figure 3-47. Band diagram of horizontal cutline plot with e-b and c-b forward biased, V_{EB}=0.7V, V_{CB}=0.5V

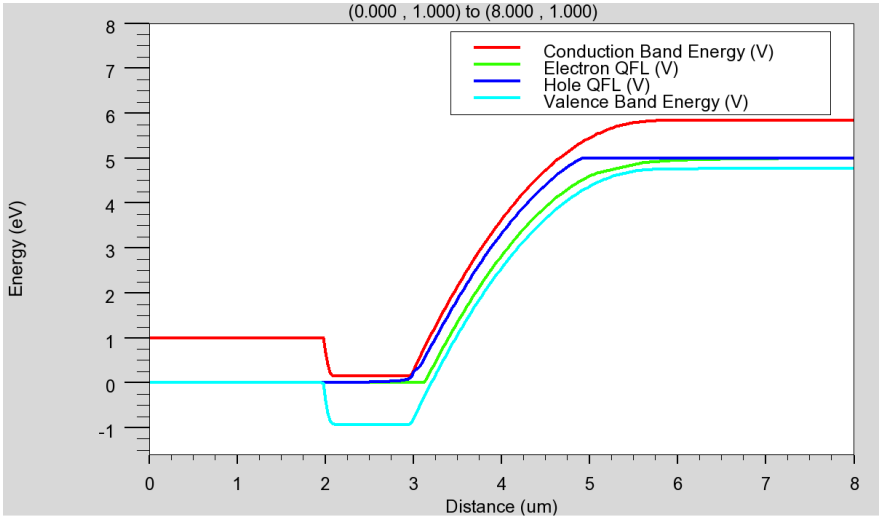

Figure 3-48. Band diagram of horizontal cutline plot with e-b zero biased and c-b reverse biased, V_{EB}=0V, V_{CB}=–5V

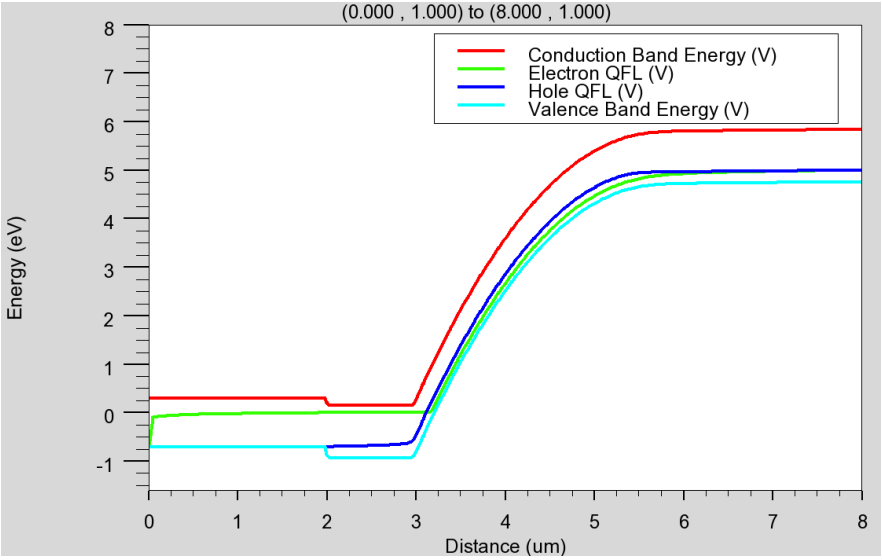

Figure 3-49. Band diagram of horizontal cutline plot with e-b forward biased and c-b reverse biased, V_{EB}=0.7V, V_{CB}=–5V

In conclusion, the hole concentration distribution in the base of a BJT depends on the e-b and c-b voltages. However, the hole concentration cannot be zero at the edge of the space-charge region which is similar to the MOSFET pinch-off where the channel cannot disappear. So the minority carrier concentration plot in figure 1-5 which is frequently found in textbooks is incorrect as shown by the simulation result in figure 3-40. In addition to carrier densities, electric field, etc. I have also simulated the current-voltage behavior of the devices. The I_C-V_{CB} plot of this BJT is shown in Fig. 3-50. As expected, the current does not saturate in the saturation region due to the Early effect [15].

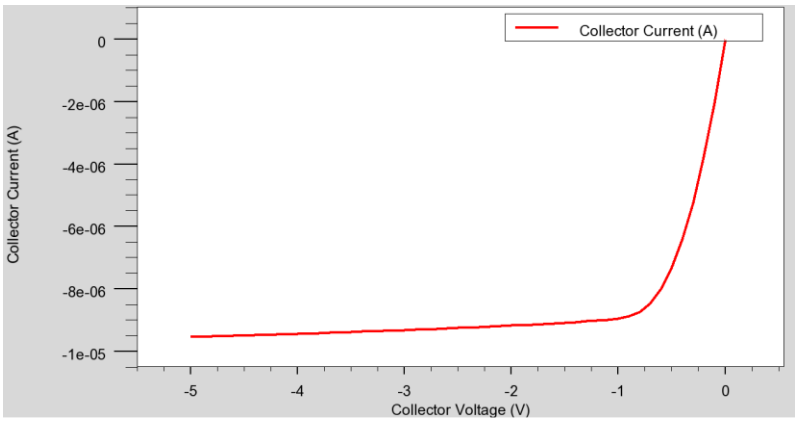

Figure 3-50. I-V curve of BJT, V_{EB}=0.7V, V_{CB}=0 to –5V

However, real BJTs are not like the simple structure simulated thus far and they are usually smaller. Hence, I simulated the BJTs of the structure shown in Fig. 3-51. The emitter is p-type and the doping concentration is $10^{19}/\text{cm}^3$, the base is n-type and the doping concentration is $10^{18}/\text{cm}^3$, the collector is p-type and the doping concentration is $10^{17}/\text{cm}^3$ and the substrate is n-type and the doping concentration is $10^{15}/\text{cm}^3$. The hole concentration contour plot is shown in Fig. 3-52.

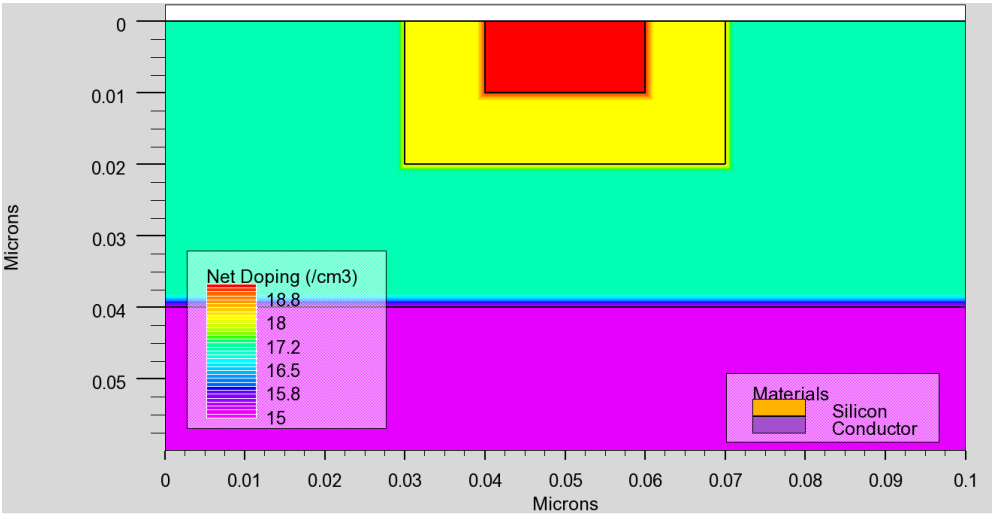

Figure 3-51. Small BJT structure and net doping concentrations

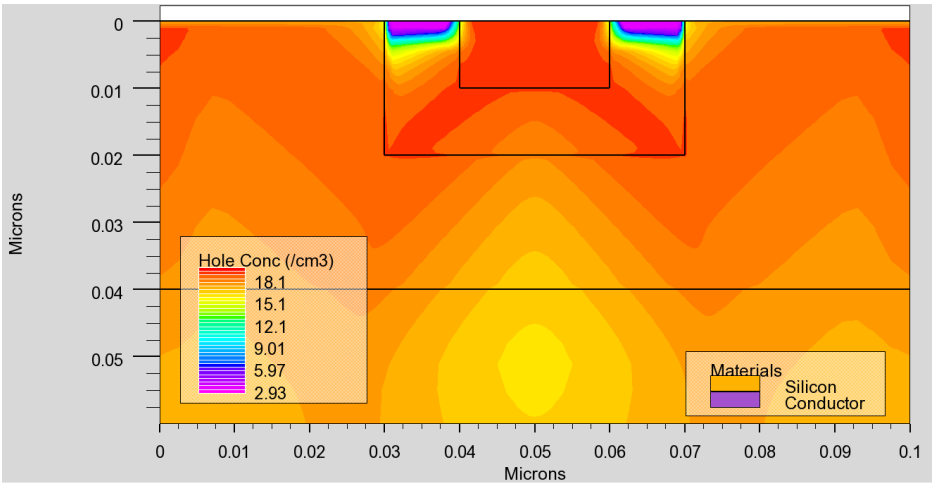

Figure 3-52. Hole concentration contour plot of small BJT with e-b forward biased and c-b reverse biased, V_{EB}=0.7V, V_{CB}=−10V

Figure 3-53 shows the total current density plot. In the small BJT, the current density is higher at the corners of the emitter, and the current flows from the emitter through the base and reaches the collector with a current path in a "W" shape.

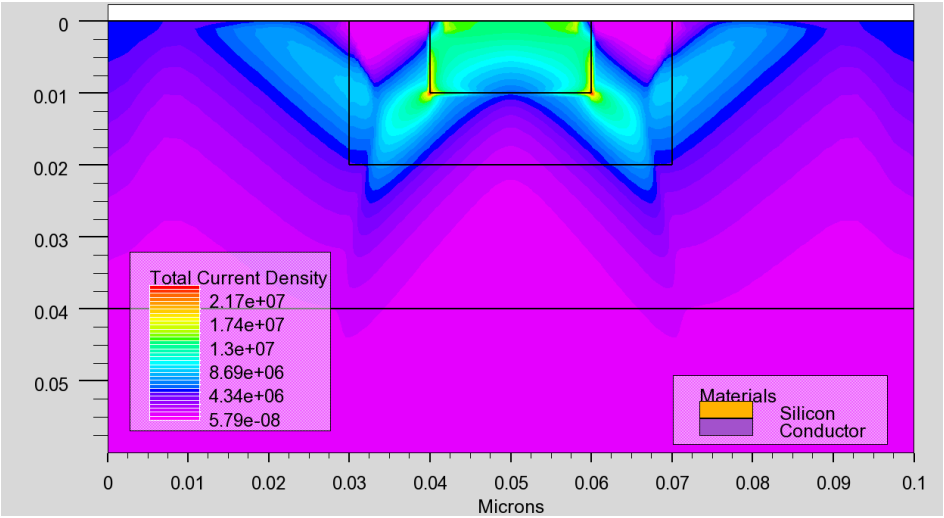

Figure 3-53. Total current density contour plot of small BJT with e-b forward biased and c-b reverse biased, V_{EB}=0.7V, V_{CB}=−10V

The higher emitter corner current is due to the base resistance, as illustrated in Fig. 3-54. With base current flowing laterally to supply electrons for recombination with holes in the base that were injected from the emitter, the lateral base voltage drop results in the corner region of the e-b junction being more forward biased than the central portion of the junction. Hence corner injection and corner current density is higher than in the middle.

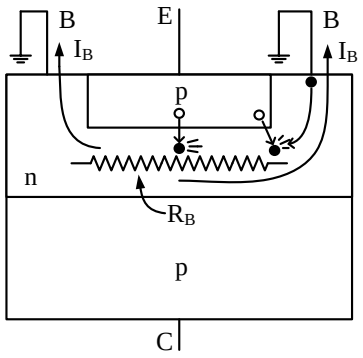

Figure 3-54. BJT showing effect of lateral base resistance

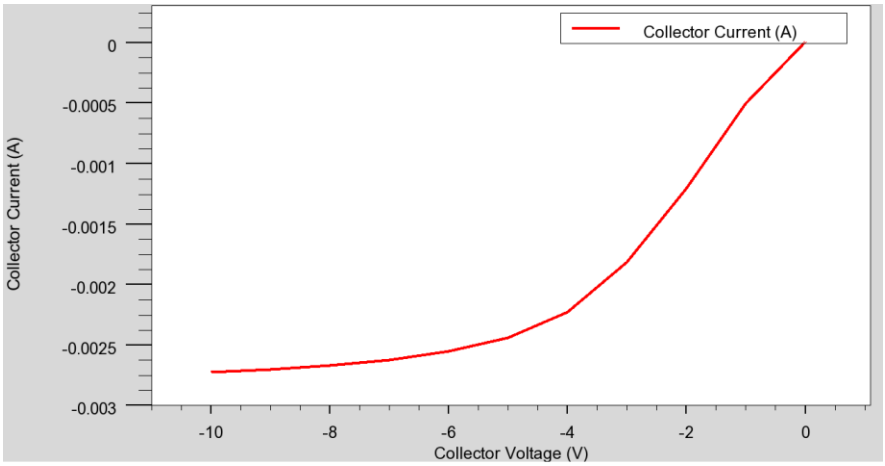

Figure 3-55. I-V curve of real BJT structure, V_{EB}=0.7V, V_{CB}=0 to –10V

The I-V curve of the small device is shown in Fig. 3-55. The current is higher than that of the larger BJT and the saturation point shifts to about -5V. The curve also a higher slope in the saturation region due to the Early effect [15].

Junction Field Effect Transistors

In junction FETs, the key region is the channel from source to drain. This channel thickness is controlled by the gate voltage through the pn junction space-charge regions. JFETs come in two versions: normally on and normally off illustrated in Fig. 3-56. In the more common "normally on" device, the electron channel is not depleted and drain current flows for V_G=0. The gates must be reverse biased to cut off the drain current. The channel in the "normally off" JFET is sufficiently thin for the two space-charge region to touch for V_G=0 and I_D=0. For drain current flow, the gate-channel junction is forward biased to reduce the scr width. However, the forward bias must be low enough for the gate-channel pn junction not to be too much forward biased since that leads to significant gate current.

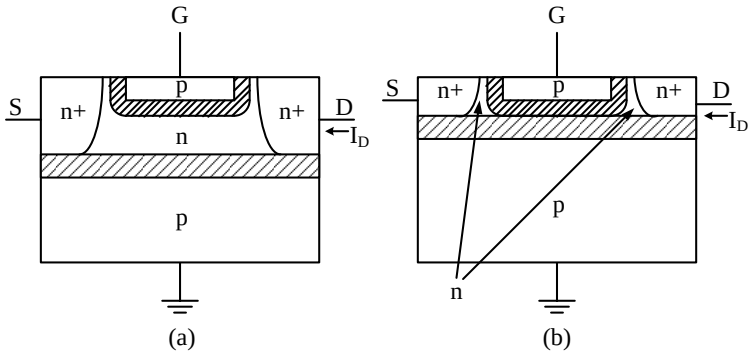

Figure 3-56. (a) Normally on and (b) normally off JFETs

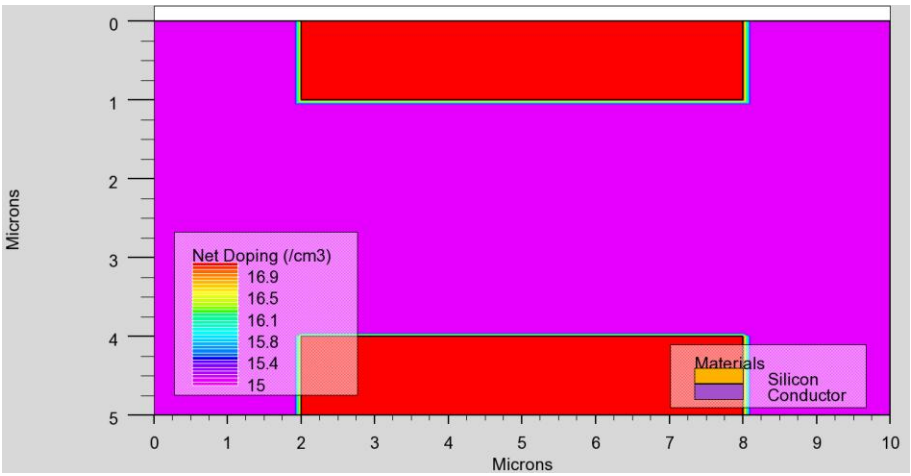

Figure 3-57. 2-D JFET structure and net doping concentrations

The two-dimensional JFET structure is shown in Fig. 3-57. The substrate is n-type and the doping concentration is $10^{15}/\text{cm}^3$, 10 microns long, 5 microns deep. The two gates are p-type and the doping concentration is $10^{17}/\text{cm}^3$, 6 microns long and 1 microns deep, which are implanted into the substrate at the upper and lower middle position [19]. The source and drain are defined at the left and right side of substrate. The contacts of gate, source and drain contacts are Ohmic-contacts.

Figure 3-58 shows the electron concentration before pinch off with -0.7 V applied on the gates and 0.4 V applied on the drain; the source is connected to ground. Figure 3-59 shows the electron concentration after pinch off, for the same gate voltage and 5 V applied on the drain. The channel boundaries are not clearly defined; it is difficult to tell where the exact pinch-off region is because the current flows through the center of the substrate. The electron concentration plot cannot distinguish the depletion region area clearly.

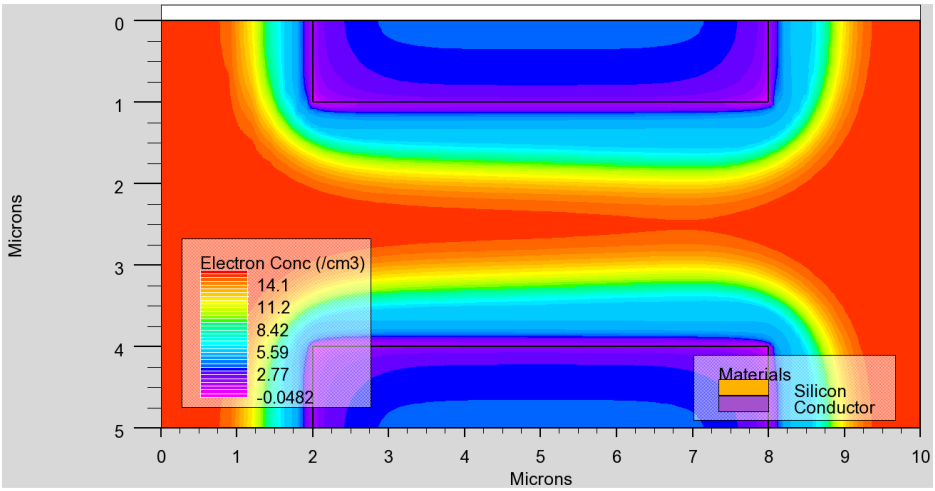

Figure 3-58. Electron concentration contour plot before pinch off, V_G=-0.7V, V_D=0.4V

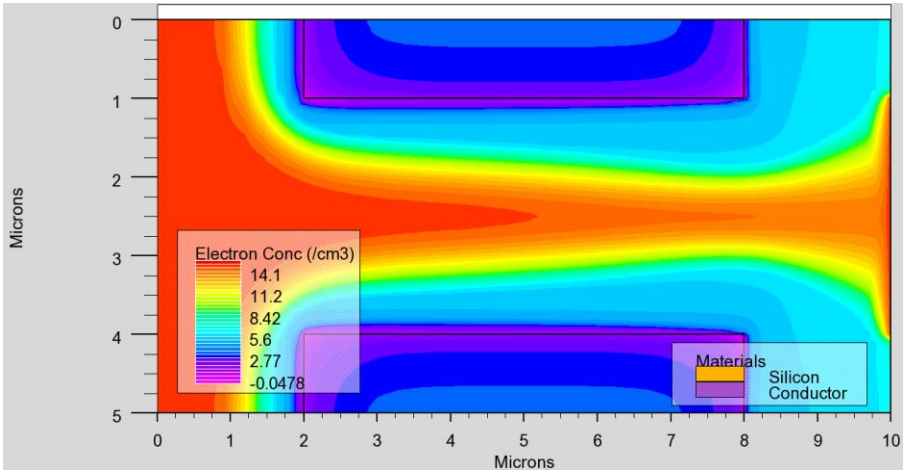

Figure 3-59. Electron concentration contour plot after pinch off, V_G=-0.7V, V_D=5V

Let me see what happens along the horizontal cutline plot of the electron concentration. In Fig. 3-60, due to the resistance in the channel, the electron concentration decreases from $10^{15}/\text{cm}^3$ to $4\times10^{14}/\text{cm}^3$ as the channel becomes narrower, and beyond 7.5 microns along the channel it returns to $10^{15}/\text{cm}^3$. After pinch off (Fig. 3-61), the electron concentration decreases from

$10^{15}/\text{cm}^3$ to $10^{14}/\text{cm}^3$ but not close to zero. The point of lowest electron concentration is very close to the drain about 9.8 microns along channel. I also simulated various drain voltages from 0.1 volts to 8 volts, and compared with the I-V curve to determine the saturation voltage. Before pinch off, the lowest points are before and around 8 microns along the channel where the gate ends; after pinch off, the lowest points are after 8 microns along the channel.

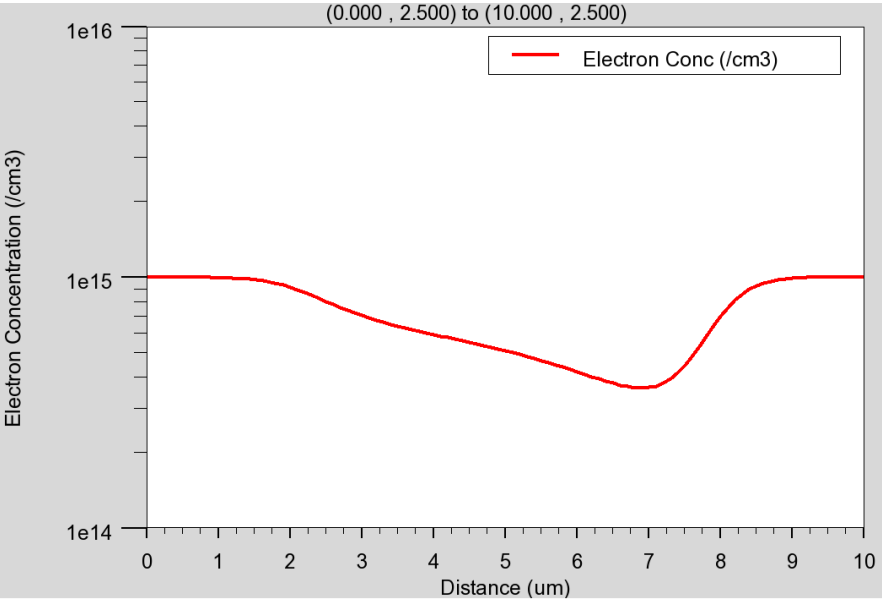

Figure 3-60. Electron concentration horizontal cutline plot before pinch off, V_G=-0.7V, V_D=0.4V

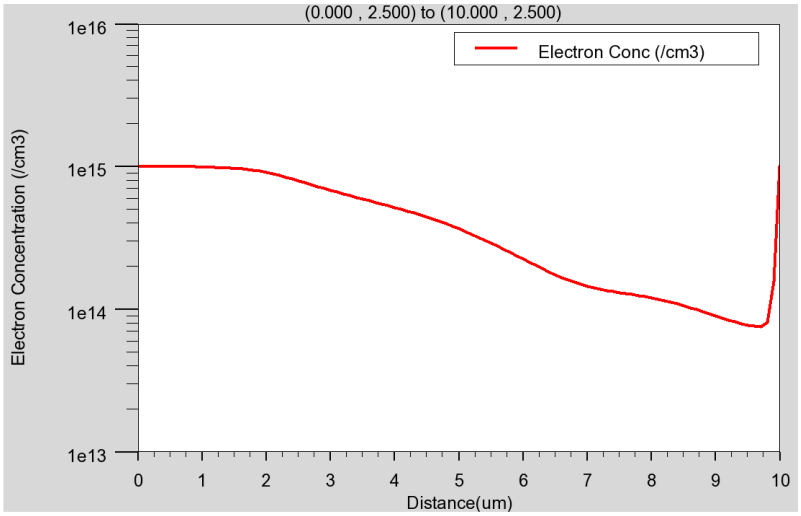

Figure 3-61. Electron concentration horizontal cutline plot after pinch off, V_G=-0.7V, V_D=5V

Figures 3-62, 3-63 and 3-64 show the vertical electron concentration distributions. The distributions are similar but the concentration peak will decreases and the shape of the distribution narrows, i.e. the channel thickness shrinks as it approaches the drain.

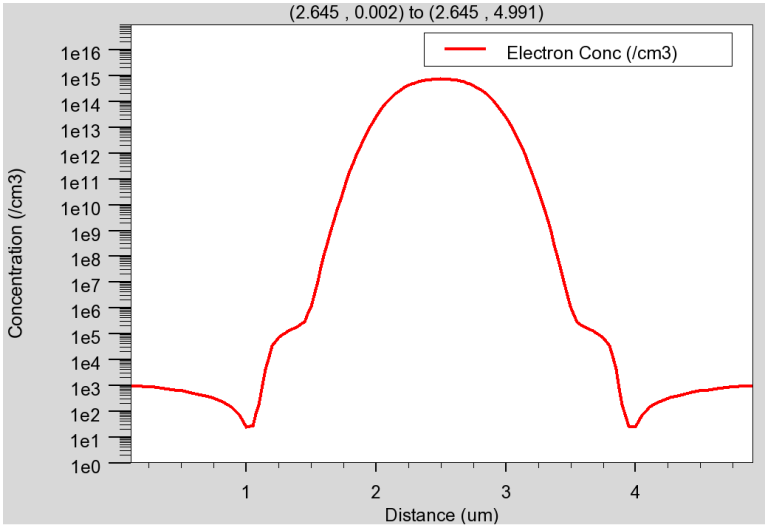

Figure 3-62. Electron concentration vertical cutline plot after pinch off at 2.645 microns along the channel, V_G=-0.7V, V_D=5V

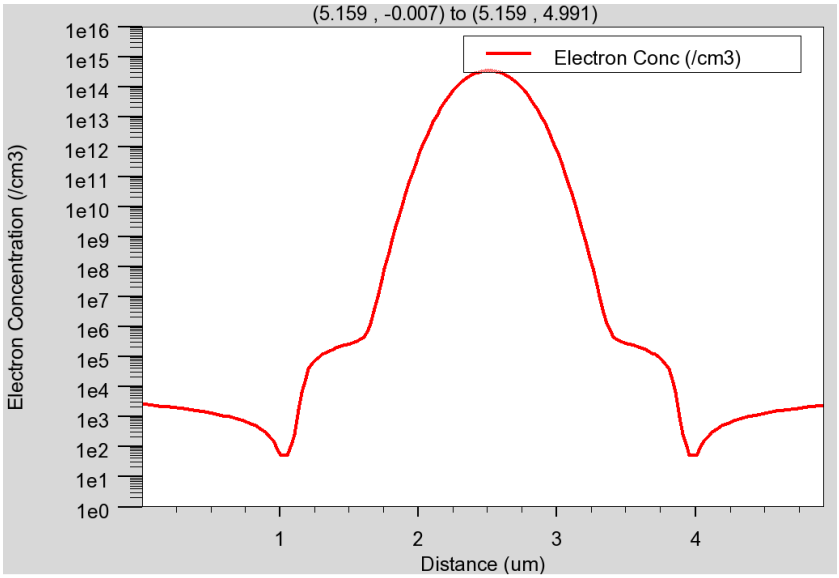

Figure 3-63. Electron concentration vertical cutline plot after pinch off at 5.159 microns along the channel, V_G=-0.7V, V_D=5V

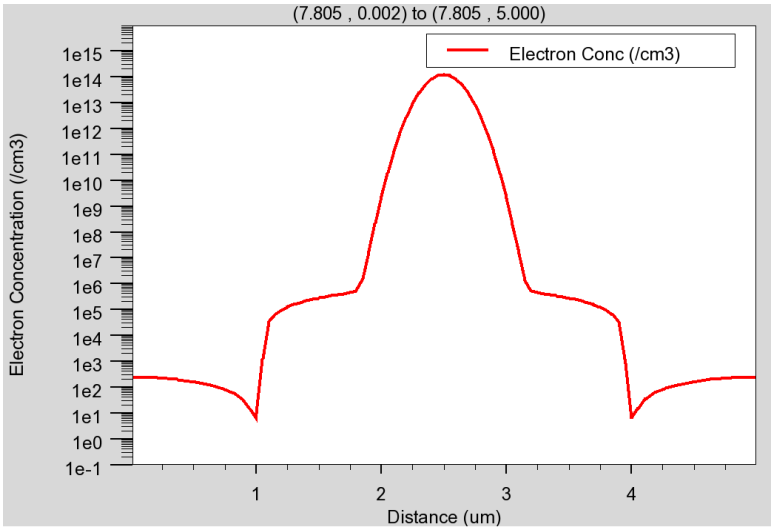

Figure 3-64. Electron concentration vertical cutline plot after pinch off at 7.805 microns along the channel, V_G=-0.7V, V_D=5V

Figures 3-65 and 3-66 show the potential plots. Before pinch off, the potential increases from source to drain and after 8 microns along the channel the

potential gain slows down; after pinch off, the potential increases up to the region very close to the drain and still has a high slope.

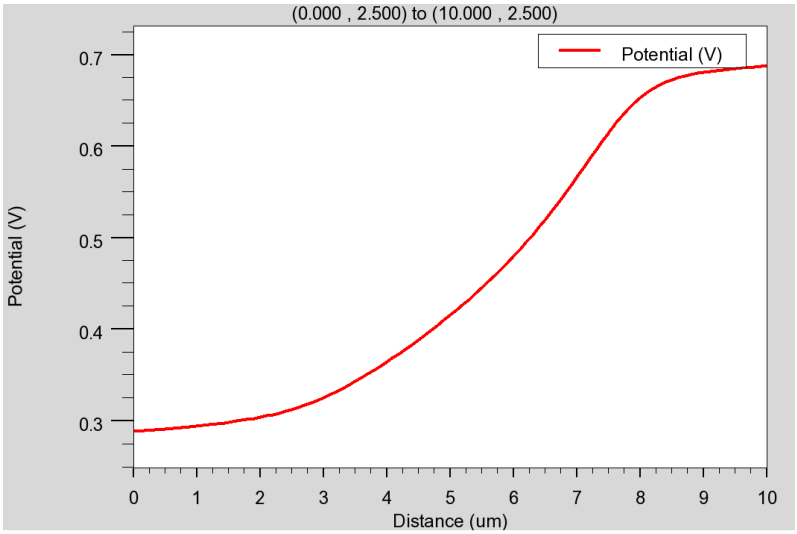

Figure 3-65. Potential horizontal cutline plot before pinch off, V_G=-0.7V, V_D=0.4V

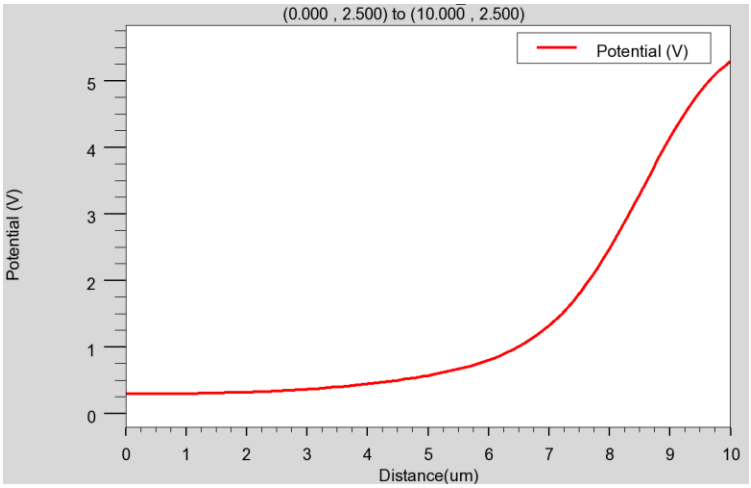

Figure 3-66. Potential horizontal cutline plot after pinch off, V_G=-0.7V, V_D=5V

The horizontal electric fields are shown in Figs. 3-67 and 3-68. Before pinch off it starts near zero and reaches a peak 1,000 V/cm, then falls back to near zero at the drain. After pinch off, the electric field increases to about 17,500 V/cm near

the drain and decreases to 6,000 V/cm at the drain shown in Fig 3-68. The higher the electric field, the faster the carriers drift through the pinch-off region until the velocity reaches its saturation velocity value.

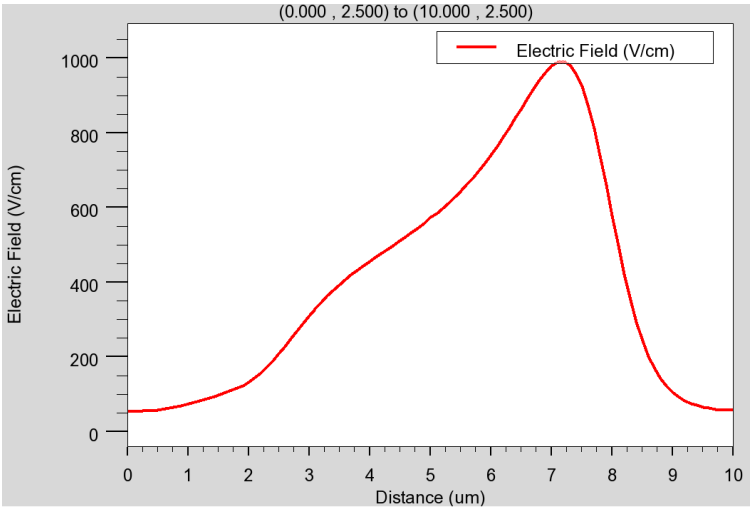

Figure 3-67. Electric field horizontal cutline plot before pinch off, V_G=-0.7V, V_D=0.4V

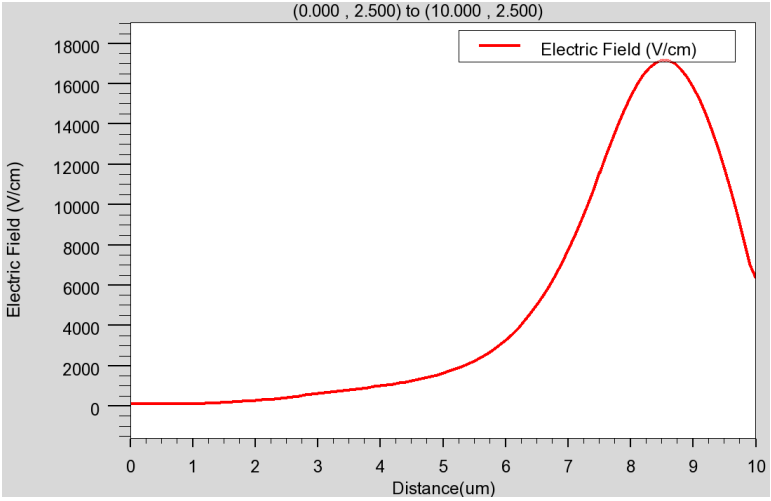

Figure 3-68. Electric field horizontal cutline plot after pinch off, V_G=-0.7V, V_D=5V

The total current densities in Figs. 3-69 and 3-70 show a peak values at 8 microns along the channel where the gate ends. The current is, of course, constant. The current density varies along the channel because the channel thickness changes. Although the current density increases with increasing drain voltage, the shape remains similar.

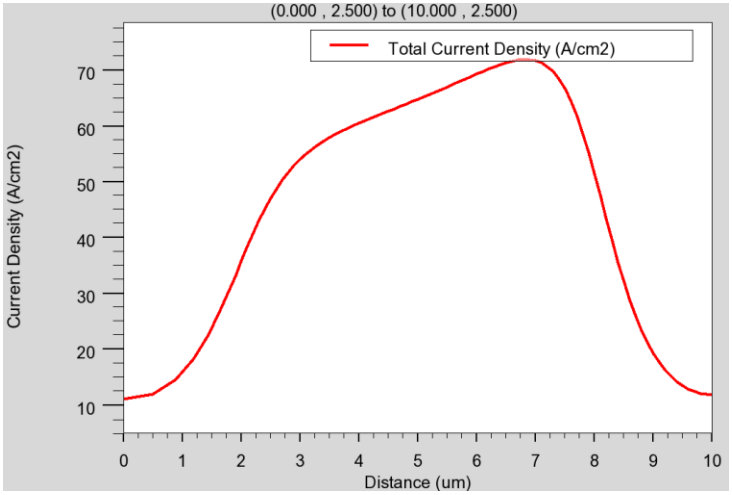

Figure 3-69. Total current density horizontal cutline plot before pinch off, V_G=-0.7V, V_D=0.4V

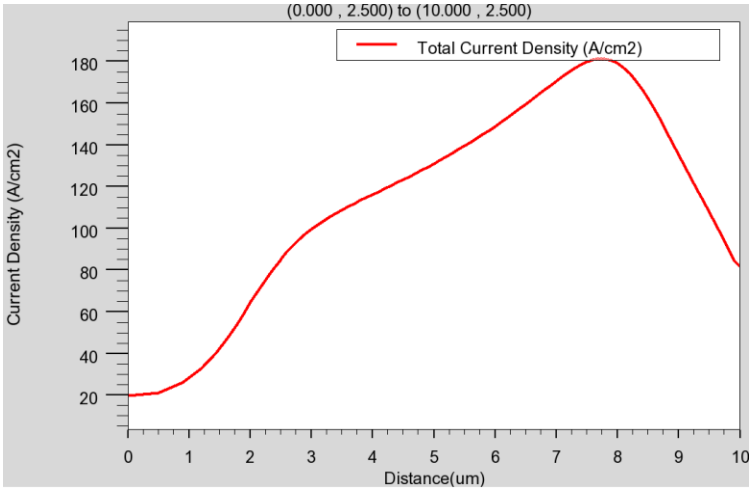

Figure 3-70. Total current density horizontal cutline plot after pinch off, V_G=-0.7V, V_D=5V

Figures 3-71 and 3-72 show the current density contour plots. Before pinch off, the channel spread out after the gate ends. After pinch off, the channel is narrower and it expands a little beyond the gate.

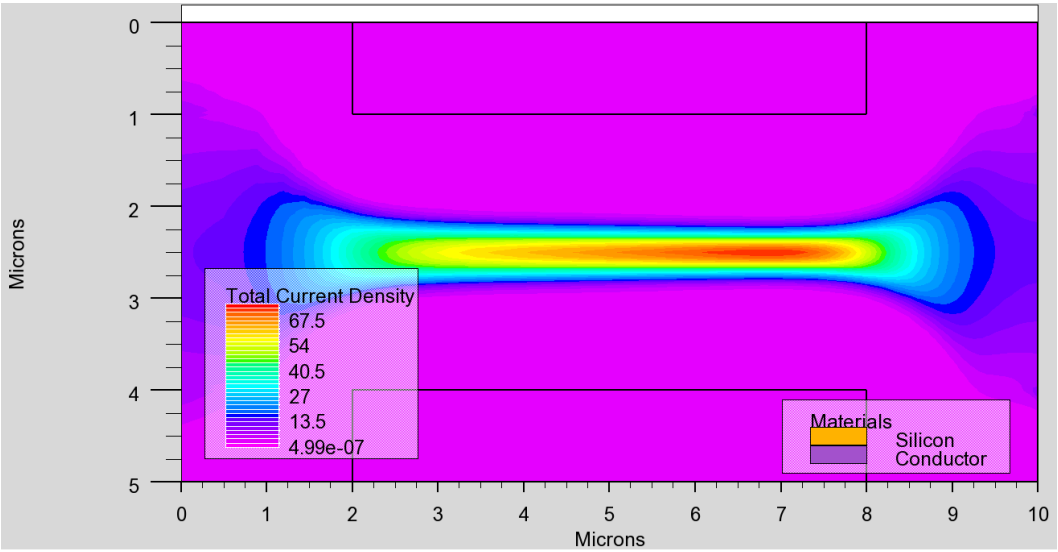

Figure 3-71. Total current density contour plot before pinch off, V_G=-0.7V, V_D=0.4V

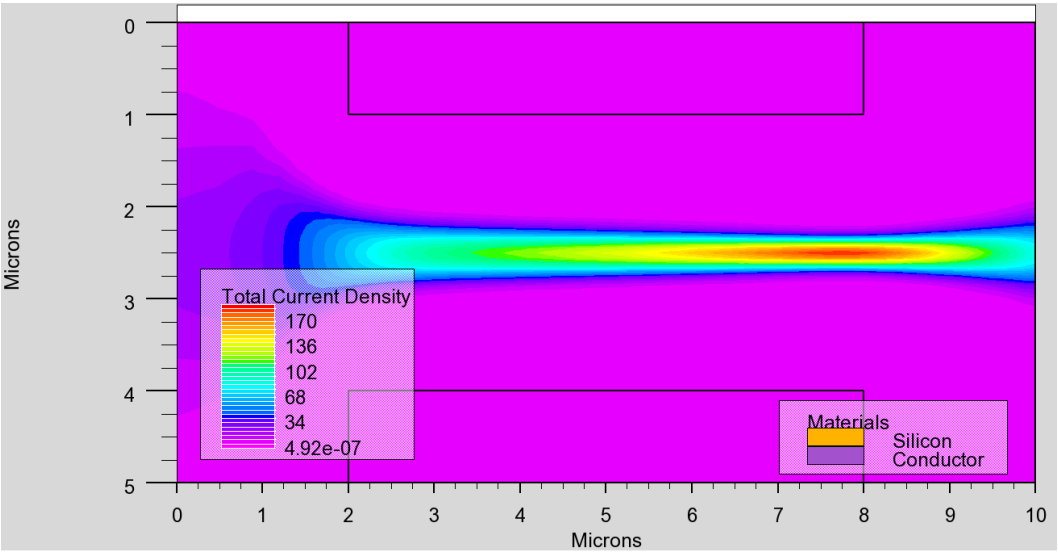

Figure 3-72. Electron concentration contour plot after pinch off, V_G=-0.7V, V_D=5V

Figures 3-73, 3-74 and 3-75 show the vertical cutline plots of current density after pinch off. The peak of current density peak increases and the distribution shrinks as it approaches the drain.

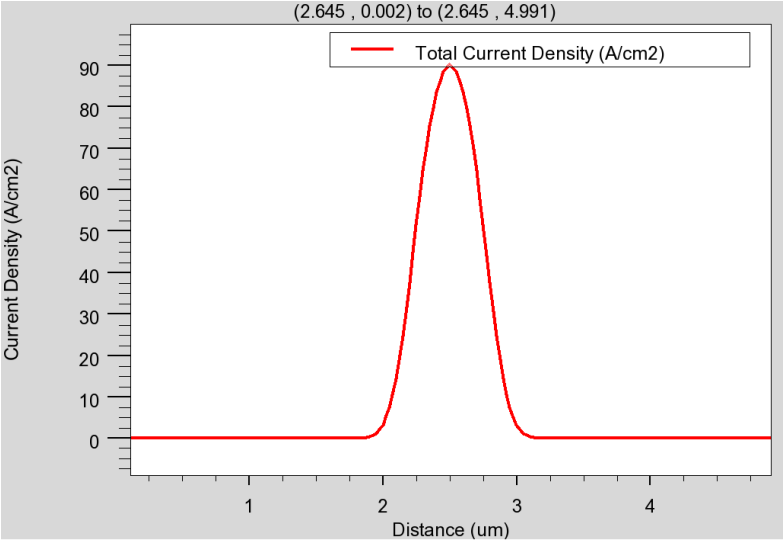

Figure 3-73. Total current density vertical cutline plot after pinch off at 2.645 microns along the channel, V_G=-0.7V, V_D=5V

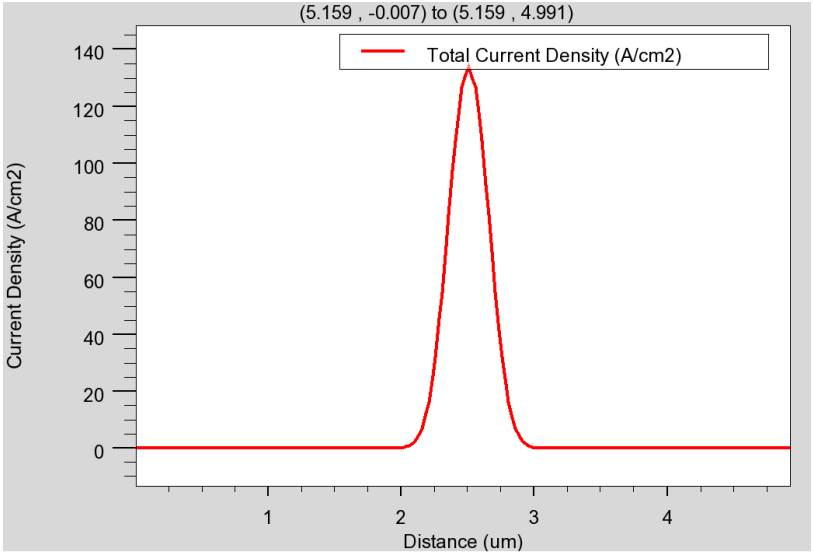

Figure 3-74. Total current density vertical cutline plot after pinch off at 5.159 microns along the channel, V_G=-0.7V, V_D=5V

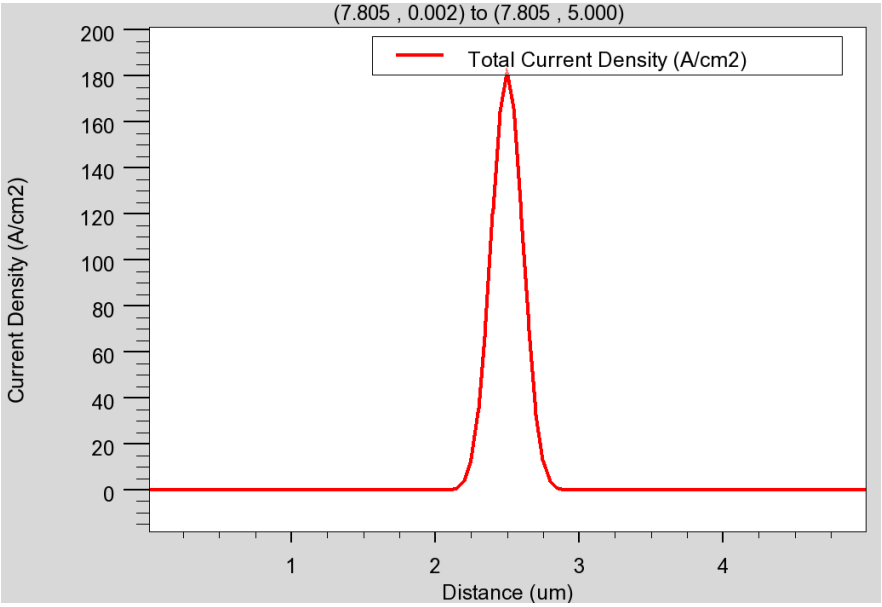

Figure 3-75. Total current density vertical cutline plot after pinch off at 7.805 microns along the channel, V_G=-0.7V, V_D=5V

Figures 3-76 and 3-77 show the band diagrams. The electron quasi-Fermi level is parallel to the conduction band. The hole quasi-Fermi level splits at the beginning of the channel and rises for a while then bends down the same as the electron quasi-Fermi level and they meet near the drain. The behavior of the hole QFL is akin to that in the MOSFET in Figs. 3-28 to 3-30. The separation of the quasi-Fermi levels is approximately the voltage along the channel. Therefore, the voltage along the channel remains constant before pinch off, after pinch off, at the pinch-off region the voltage decreases to zero at the drain. Since the channel/drain junction is an n/n^+ junction, the QFLs near the drain are very different than near the p/n^+ junction of MOSFETs where the hole QFL is near E_C and the electron QFL is near E_V.

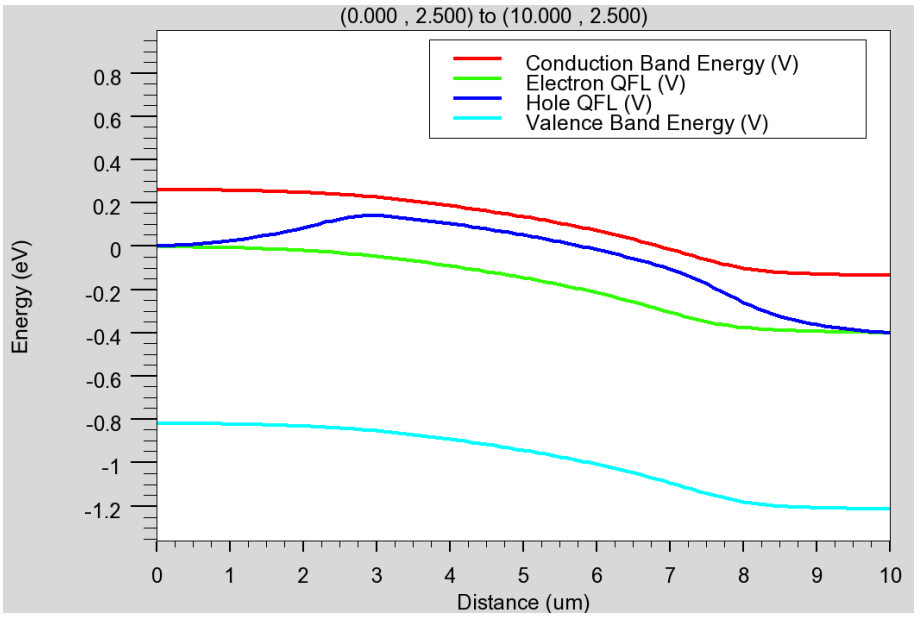

Figure 3-76. Band diagram of horizontal cutline plot before pinch off, V_G=-0.7V, V_D=0.4V

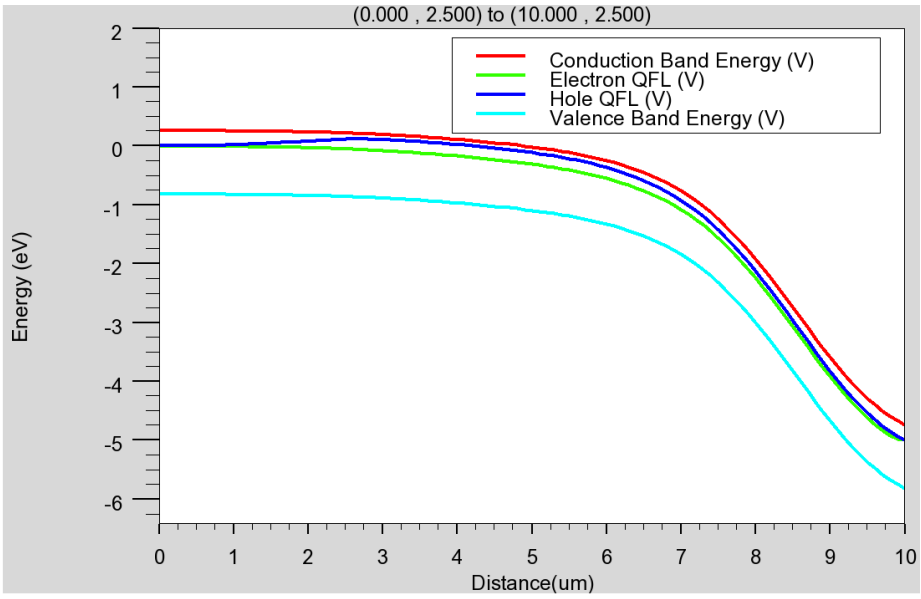

Figure 3-77. Band diagram of horizontal cutline plot after pinch off, V_G=-0.7V, V_D=5V

Figure 3-78 shows the I-V curve of the JFET. The saturation gate voltage is about 0.8 V. After saturation, due to the Early effect [15], there is a small slope of the drain current.

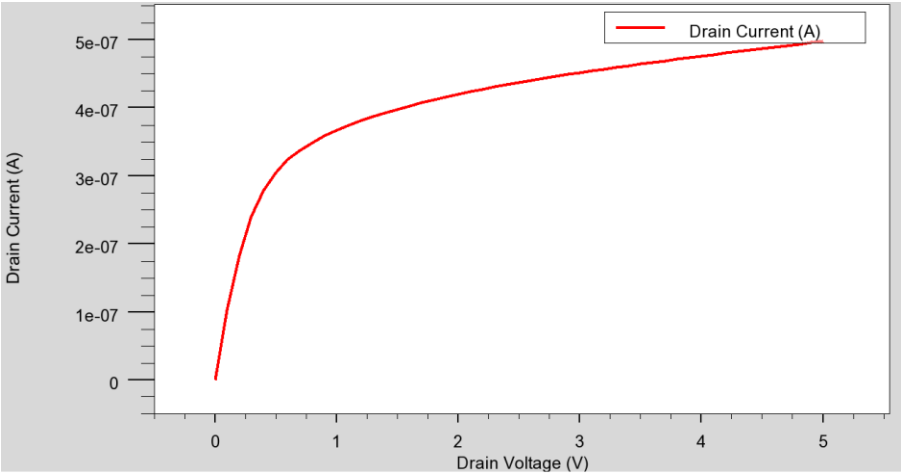

Figure 3-78. I-V curve of JFET, V_G=-0,7V, V_D=0 to 5V

However, the real JFET channel is much smaller, therefore, I simulated a JFET of 30 nm gate length. The substrate is n-type and the doping concentration is $10^{17}/\text{cm}^3$, the gates are p-type and the doping concentration is $10^{19}/\text{cm}^3$.

Figure 3-79 shows the electron concentration contour plot of this device; it is similar to Fig. 3-59. Due to the scaling, the doping concentration is increased to keep the device as a "normally on" JFET.

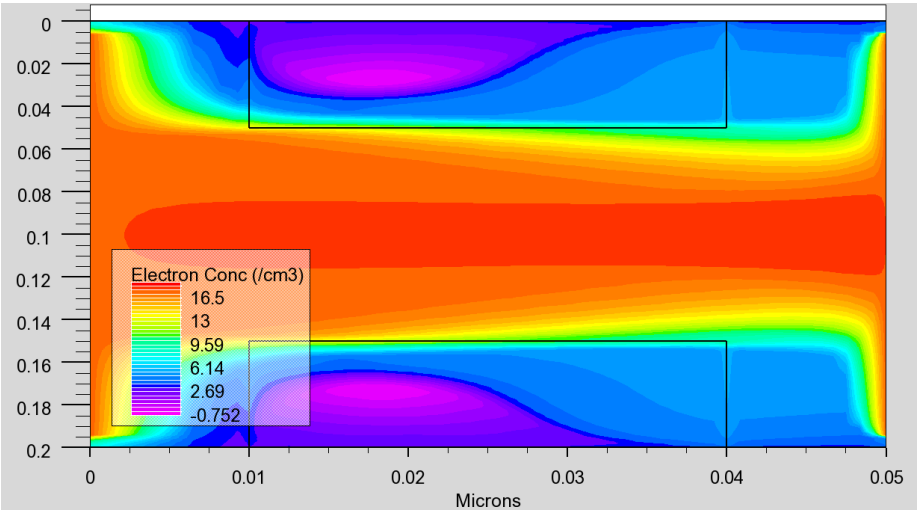

Figure 3-79. Electron concentration contour plot after pinch off, V_G=-0.7V, V_D=5V

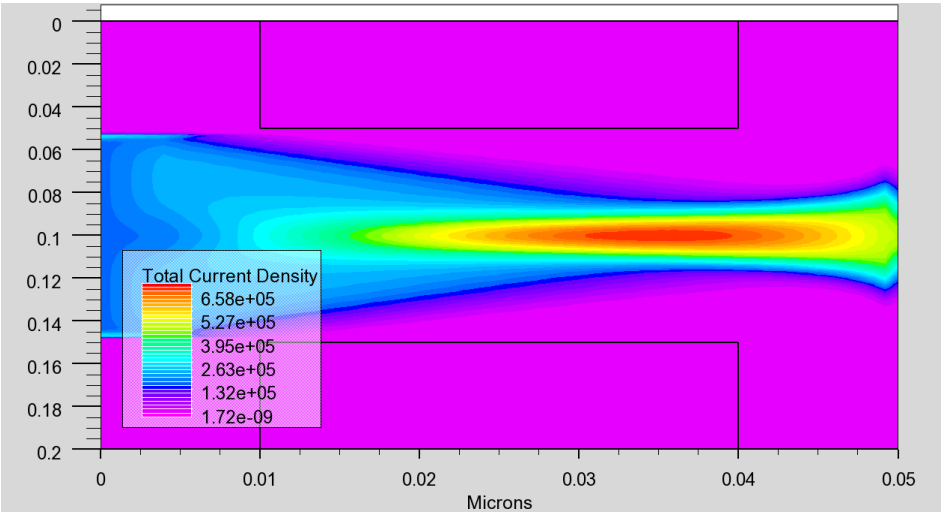

Figure 3-80. Total current density contour plot after pinch off, V_G=-0.7V, V_D=5V

Figure 3-80 shows the current density contour plot. The channel shape is similar to the current density contour plot in Fig. 3-72. The channel thickness at the pinch-off region is about 40 nm.

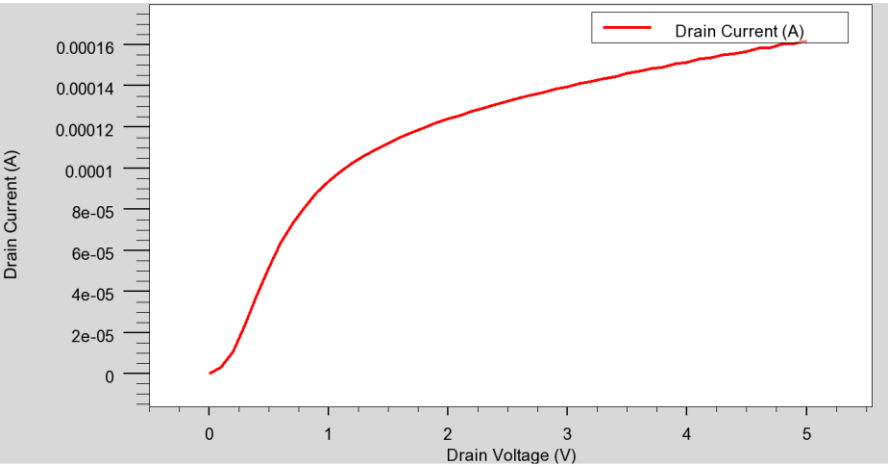

Figure 3-81. I-V curve of JFET, V_G=-0.7V, V_D=0 to 5V

Compared to Fig. 3-78, the I-V curve of nanometer scaled JFET in Fig 3-81 has a higher slope. It is similar to a MOSFET, because the channel is much shorter, the current is higher and also due to the Early effect [15], it has a higher slope after the saturation point.

In conclusion, the JFET channel is not clearly seen because the boundaries of the space-charge region are difficult to recognize. The channel does not disappear after pinch off, the shape of channel is always tapered, the carrier concentration in the channel decreases progressively and it is not very low and the pinch-off region in JFETs is also difficult to define.

In this section I simulated the carrier concentrations, potentials, electric fields current densities and quasi-Fermi levels of MOSFETs, BJTs and JFETs and analyzed and discussed what happens at and near the pinch-off regions. I also simulated typical nano-scaled devices and show that they behave similarly to large devices. The simulation results showed that some of the figures typically shown in semiconductor device physics textbooks are incorrect.

CHAPTER 4

CONCLUSION

The simulation results of the carrier concentrations, potentials, electric fields current densities and quasi-Fermi levels of MOSFETs, BJTs and JFETs at and near the pinch-off regions. Compared with some plots and diagrams in textbooks, the simulation plots show different behavior.

The MOSFET channel is very thin (about 10 nm), and it expands from source to drain rather than pinching off at the pinch-off point and disappearing after the pinch-off point. In addition, the space-charge region under the gate expands from source to drain as the potential increases. After the pinch-off point, the channel broadens because the vertical electric field decreases, and the current spreads out as it approaches the drain.

The BJT minority carrier concentration distribution in the base depends on the e-b and c-b voltages. However, in simulation plots, the hole concentrations are not zero in the base at the edge of the c-b space-charge region with the c-b reverse-biased, which is different to the plots shown in some textbooks where the minority carrier concentration approaches zero.

The JFET channel as well as the space-charge region is difficult to determine because the boundaries are not clearly seen. However, the channel does not disappear, it exists after pinch off and the shape of the channel is tapered. In addition, the majority carrier concentration decreases progressively along the channel.

In summary, these simulation results show how practical devices operate and behave and thereby provide a better understanding of device physics.

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APPENDIX

THE REVERS-BIASED PN JUNCTION

The simulations in this thesis were precipitated by the incorrect band diagrams in many text-books that are in current use. In particular, the reverse-biased pn junction band diagrams are frequently drawn incorrectly. I show some examples in Fig. A-1. The quasi-Fermi levels in the depleted space-charge regions (scr) in all of these figures are qualitatively correct but they lie substantially beyond the band gap which is not possible.

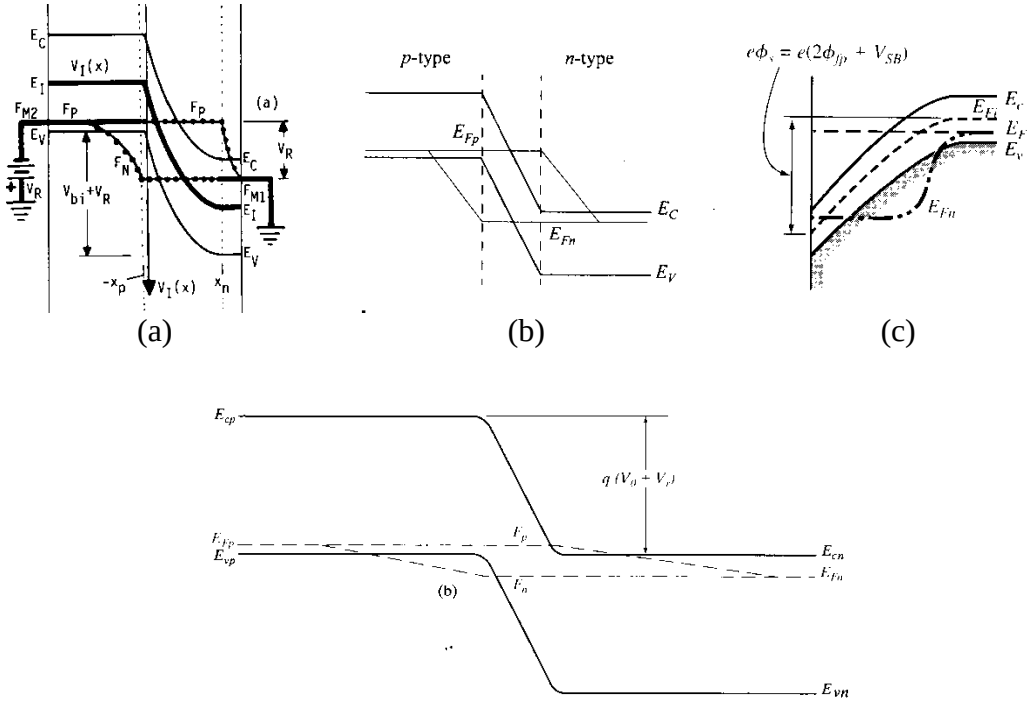

Fig. A-1. Band diagrams taken from (a) C.T. Sah, *Fundamentals of Solid-State Electronics*, World Scientific, Singapore, 1991, (b) S.M. Sze and K.K. Ng, *Physics of Semiconductor Devices*, 3rd ed., Wiley-Interscience, Hoboken NJ, 2007, (c) D.A. Neamen, *Semiconductor Physics and Devices*, 3rd ed., McGraw Hill, Boston, MA, 2003, (d) B.G. Streetman and S.K. Banerjee, *Solid State Electronic Devices*, 6th ed., Pearson Prentice Hall, Upper Saddle River, NJ, 2006.

Why are these band diagrams incorrect? The quasi-Fermi levels are given by

$$E_{Fn} = E_i + kT\ln\left(\frac{n}{n_i}\right);\ E_{Fp} = E_i - kT\ln\left(\frac{p}{n_i}\right)$$

Now what are the carrier densities in the scr under reverse bias? They are clearly not zero since there is a leakage current flowing through the device. If I assume $n \approx p \approx 10\ cm^{-3}$, $n_i = 10^{10}\ cm^{-3}$, $E_G = 1.1$ eV and T = 300K, I get

$$E_{Fn} = E_i + 0.53eV;\ E_{Fp} = E_i - 0.53eV$$

i.e., the quasi Fermi levels lie very near the band edges. This is shown qualitatively in Fig. A-2. Even for $n \approx p \approx 1\ cm^{-3}$ the quasi-Fermi levels lie just slightly in the conduction and valence bands, but nowhere near as much as in Fig. A-1. A simulation of the band diagram of a reverse-biased junction is shown in Fig. A-3, confirming the qualitative band diagram of Fig. A-2.

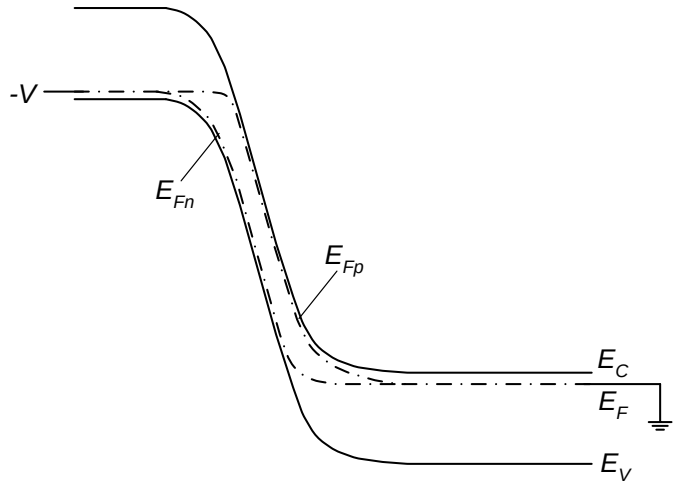

Fig. A-2. Reverse-biased pn junction with quasi-Fermi levels.

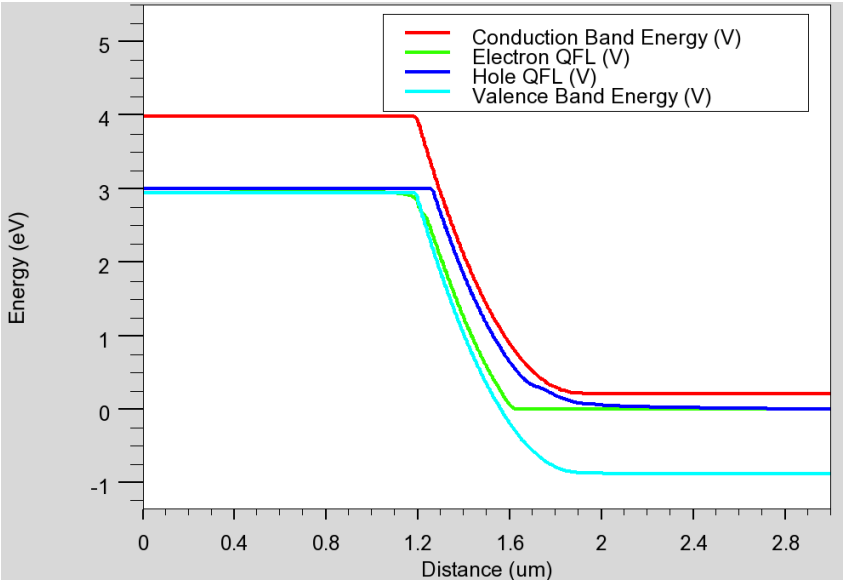

Fig. A-3 Simulated reverse-biased pn junction with quasi-Fermi levels.

Si, $N_A=10^{18}$ cm^{-3}, $N_D=10^{16}$ cm^{-3}, V=-3V.