Comparative Analysis of Simulation of Trap Induced Threshold Voltage Fluctuations for 45 nm Gate Length n-MOSFET and Analytical Model Predictions

by

Nabil Shovon Ashraf

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved October 2011 by the
Graduate Supervisory Committee:

Dragica Vasileska, Chair
Dieter Schroder
Stephen Goodnick
Michael Goryll

ARIZONA STATE UNIVERSITY

December 2011

ABSTRACT

In very small electronic devices the alternate capture and emission of carriers at an individual defect site located at the interface of Si:SiO2 of a MOSFET generates discrete switching in the device conductance referred to as a random telegraph signal (RTS) or random telegraph noise (RTN). In this research work, the integration of random defects positioned across the channel at the Si:SiO2 interface from source end to the drain end in the presence of different random dopant distributions are used to conduct Ensemble Monte-Carlo (EMC) based numerical simulation of key device performance metrics for 45 nm gate length MOSFET device. The two main performance parameters that affect RTS based reliability measurements are percentage change in threshold voltage and percentage change in drain current fluctuation in the saturation region. It has been observed as a result of the simulation that changes in both and values moderately decrease as the defect position is gradually moved from source end to the drain end of the channel. Precise analytical device physics based model needs to be developed to explain and assess the EMC simulation based higher V_T fluctuations as experienced for trap positions at the source side. A new analytical model has been developed that simultaneously takes account of dopant number variations in the channel and depletion region underneath and carrier mobility fluctuations resulting from fluctuations in surface potential barriers. Comparisons of this new analytical model along with existing analytical models are shown to correlate with 3D EMC simulation based model for assessment of V_T fluctuations percentage induced by a single interface trap. With scaling of devices beyond 32 nm node,

halo doping at the source and drain are routinely incorporated to combat the threshold voltage roll-off that takes place with effective channel length reduction. As a final study on this regard, 3D EMC simulation method based computations of threshold voltage fluctuations have been performed for varying source and drain halo pocket length to illustrate the threshold voltage fluctuations related reliability problems that have been aggravated by trap positions near the source at the interface compared to conventional 45 nm MOSFET.

ACKNOWLEDGMENTS

At the outset, I sincerely submit myself to God who enabled me completing my Doctoral research. I am forever grateful to my Ph.D. supervisor and chair of the Defense Committee Professor Dr. Dragica Vasileska for her superior guidance and encouragement at every phase of this research. Her constant encouragements at critical junctures of this research have made the dissertation to be completed in time. I am grateful to Professor Dr. Dieter K. Schroder, member of my Doctoral defense Committee, for his illuminating advice with regard to some of the concepts of my Doctoral research contents where his clarifications to my questions made valuable impact on my research outcomes. I am grateful to Professor Dr. Stephen M. Goodnick, member of my Doctoral defense Committee, for his valuable and amiable guidance, support and encouragement to see the research through to completion. I am grateful to Dr. Michael Goryll, member of my Doctoral defense Committee, for discussing the research outcomes at different phases of this Doctoral research where his kind and sincere diligent approach to give me valuable suggestions is worth mentioning. Finally, I would heartily thank all the members of Computational Electronics research group and my revered Faculty Members of Electrical Engineering department for their generous interactions and support during my entire Ph.D. program in Arizona State University.

TABLE OF CONTENTS

Page

LIST OF TABLES …………………………………………………..................viii

LIST OF FIGURES…………………………………………………………ix

CHAPTER

1 INTRODUCTION……………………………………………...1

2 HISTORICAL TRENDS AND SURVEY OF PAST SEMINAL RESEARCH ARTICLES ON UNDERSTANDING AND CHARACTERIZATION OF RANDOM TRAP AND DOPANT FLUCTUATIONS RELATED ATTRIBUTES............................. 8

3 ELECTROSTATICS OF SI:SIO$_2$ INTERFACE AND OXIDE TRAPS...25

3.1 Multiphonon Capture And Emission Process...............28

4 REAL SPACE TREATEMENT OF THE ELECTRON-ELECTRON AND ELECTRON-ION INTERACTIONS 31

4.1 Corrected Coulomb Approach………………………...34

4.2 Particle-Particle-Particle-Mesh Method……………….35

4.3 Fast Multipole Method 38

5 DESCRIPTION OF ANALYTICAL MODELS FOR RANDOM DOPANT FLUCTUATIONS (RDF) AND RANDOM INTERFACE TRAP INDUCED THRESHOLD VOLTAGE FLUCTUATIONS ASSESSMENT……………………………...43

CHAPTER Page

5.1 Dopant Number Fluctuation Based Analytical Model……………………………………………….44

5.2 Percolation Theory Based Conduction Modulation Incorporated Analytical Model ………………………..49

5.3 Proposed Mobility Fluctuation Based Analytical Model With Inherent Number Fluctuation From Channel Dopants………………………………………………...54

6 SIMULATION RESULTS CONDUCTED ON THRESHOLD VOLTAGE EXTRACTION AND ITS FLUCTUATION INDUCED BY INTERFACE TRAPS………………………………………58

6.1 Simulation Results For The Case of A Single Charged Trap By Using EMC Device Simulation Method………………………………………………...59

6.2 Simulation Results For The Case of Two Charged Traps By Using EMC Device Simulation Method………………………………………………...64

6.3 Analytical Model Based Computations of V_T And Its Fluctuations in Presence of a Single Interface Trap for 45 nm n-MOSFET……...65

6.3.1 V_T Extraction and Its Fluctuations Assessment By The Newly Proposed

CHAPTER Page

Mobility Fluctuations Based Model………...70

6.3.2 V_T Extraction and Its Fluctuations Assessment Using 3-D EMC Device Simulation Scheme For Conventional and Halo Pocket Implanted 45 nm MOSFET…...75

6.4 Simulation Results from 3-D Ensemble Monte Carlo Based Device Simulation On Drive Current (saturation) Fluctuations Induced By a Single And Double Interface Traps In The Channel Of a 45 nm MOSFET…………..79

7 CONCLUSIONS 82

8 FUTURE WORK……………………………………......................85

REFERENCES 87

LIST OF TABLES

Table | Page

3.1 The calculated threshold voltage values for dopant number distributions as arranged in the cell……………………………………………………………..46

LIST OF FIGURES

Figure Page

3.1 Configuration coordinate diagram. The energy zero of the system corresponds to the empty defect with the electron at the Fermi level 30

4.1 Typical flow-chart of a particle-based device simulator..........................31

4.2 Philosophy behind the (A) corrected Coulomb approach, where correction force is used in the molecular dynamics routine, and (B) the fast multipole method where the full Coulomb interaction is being considered to get the force on the electrons in the free-flight portion of the Monte Carlo transport kernel……………………………………………………….34

4.3 Illustration of the P^3M approach…………………………….................38

4.4 Conventional evaluation of contribution from distant particles: $O(N^2)$ algorithm…………………………………………………………….41

4.5 Evaluation with the multipole moment and the local expansion: $O(N)$ algorithm...41

5.1 Cellular arrangement of random dopant ions shown for two random channel dopant configurations extracted from random dopant implant subroutine used in numerical EMC device simulation. The cell size is 10 nm spaced gate width (horizontal direction and 10 nm spaced channel along source to drain (vertical) direction………….................................46

5.2 Cellular arrangement of random dopant ions and an interface trap located at a particular gate width (horizontal) and channel (vertical) direction

Figure Page

positioned cell (For this cellular arrangement, V_{th} = 2068 V and $V_{th}(j)$ = 0.1178 V)………………...47

5.3 Examples of conducting [a and b] and non-conducting [c and d] arrays (Adopted from Ref. [9].)………………………………………………….51

5.4 Calculation of threshold voltage shown in presence of an interface trap in the middle of the gate width for two different random dopant configurations using the equations (13)-(23). The hatched cell designate the trap's interaction zone…………………………………………….....54

6.1 Threshold voltage fluctuations due to random dopant fluctuatios (without traps) for a statistical ensemble of 20 devices with different number and different distribution of the impurity atoms………………………………59

6.2 Threshold voltage variation for single trap's position (averaged over twenty random dopants per trap position) along the channel. In the X-axis, x = 0 denotes the source end of the channel………………………..61

6.3 Threshold voltage fluctuation due to single trap's position along the channel (averaged over twenty random dopants per trap position). x=0 denotes source end of the channel………………………………………..62

6.4 Schematic explanations of the results presented in Figure 4.3…………...63

6.5 Extracted threshold voltage standard deviation as a function of trap position averaged over 20 random channel dopants (x=0 is source end of the channel)………………………………………………………………63

Figure Page

6.6 Percentage threshold voltage due to two traps located at the semiconductor/oxide interface and different positions along the middle section of the channel. 20 device with different random dopant distributions have been averaged out. x=0 denotes source end of the channel…………..64

6.7 Threshold voltage standard deviation as a function of two traps' positions showing well behaved spatial correlation when sufficient number of random dopants are considered. x=0 denotes the source end of the channel 65

6.8 Threshold voltage as a function of different discrete random dopant configuration in the channel region when no interface random trap is present…………………………………………………………………...67

6.9 Threshold voltage fluctuations computed by the additional analytical model adjusted for random interface trap's interactions with channel electrons and EMC simulation method…………………………………………………...67

6.10 The errorbar plot of threshold voltage fluctuation percentage for interface trap positions near source and away from source along the channel for the cases of (i) EMC simulation method, (ii) analytical model 1 and (iii) EMC simulation method with no short range e-e and e-ion-trap force consideration..69

6.11 Threshold voltage fluctuation as a function of trap position at the interface in the channel region of the MOSFET for the first of the two analytical models and EMC simulation models with and without short range Coulomb

Figure Page

force corrections……………………………………………………………...70

6.12 Effective channel mobility values for different statistical set of random dopants………………………………………………………………...72

6.13 Effective channel mobility fluctuation as a function of trap position at the interface between source and drain junctions in the channel of the MOSFET………………………………………………………………...72

6.14 Threshold voltage values extracted for the two existing models in the literature along with the new analytical model and EMC device simulation for a statistical set of random dopant types designated as integer numbers…………………………………………………………………73

6.15 Percentage averaged threshold voltage fluctuation values extracted for the two existing models in the literature along with new analytical model and EMC device simulation method for a single random interface trap positioned in the channel from source to drain of the MOSFET…………73

6.16 Threshold voltage distribution with their expected deviations for different random dopant configuration types when trap's effect is considered.........74

6.17 Threshold voltage fluctuation error bar plot considering different trap positions for the (i) EMC simulation method, (ii) analytical mobility fluctuation based model and (iii) analytical number fluctuation based model 74

Figure Page

6.18 Threshold voltage values for a set of 20 random dopant configurations for the conventional, shorter and larger halo doped 45 nm MOSFET 77

6.19 Threshold voltage fluctuation percentage values induced by an interface trap positioned from source to drain for the cases of conventional, shorter and larger halo doped 45 nm MOSFET…………………….............................78

6.20 Threshold voltage distribution with their expected deviation induced by trap for different random dopant configuration types for the cases of conventional and two halo pocket implanted MOSFET devices................78

6.21 Threshold voltage fluctuation percentage with their expected deviation as recorded for different trap positions along the channel for three MOSFET device types...79

6.22 ON-current fluctuation as effected by variation of single trap position (20 random dopant cases have been averaged per trap position) along the channel from source end (x=0) to drain end…………………………........80

6.23 ON-current degradation as a function of two traps' positions. The statistical ensemble used here consists of first seven random dopant distributions in both number and positions within the active region of the channel. x=0 denotes source end of the channel 81

CHAPTER 1

Introduction

As a consequence of recent advances in processing technology, it has now been possible to produce devices in which the active volume is so small that it contains only a small number of charge carriers. The examples are small area silicon metal oxide field effect transistors (MOSFET) and metal insulator metal (MIM) tunnel junctions. Over a span of the last decade (1998-2008), MOSFETs have reached decananometer (between 100 nm and 10 nm) dimensions with 40-50 nm physical gate length devices that have been already manufactured in the current production cycle. These transistors have been mass produced by the semiconductor manufacturing industries and device performance and reliability studies have already been conducted in research laboratories. The focus now is shifting towards experimental demonstration of device performance reaching 15 nm down to 10 nm physical gate length node. In this respect, today's commercialized driver MOSFETs in computer microprocessor and cellular, digital and ASIC markets are becoming truly atomistic in nature. The conventional way of describing, designing, modeling and simulating such miniature gate length devices assuming uniform continuous ionized dopant charge both in the channel region and bulk region of a MOSFET, in smooth device boundaries and interfaces is no longer valid. The granularity of the electric charge and the atomicity of the matter begin to introduce substantial variation in individual device characteristics. The variation in number and position of the

dopant atoms in the active channel region of decananometer MOSFETs makes each transistor microscopically different and inherently introduces significant spread of device parameters like on current and threshold voltage from one device to the next assembled per die and from die to die in the completely fabricated systems [1].

In simulations of these ultrasmall semiconductor devices, a number of important considerations have been either ignored or approximated in a manner which is not representative of the actual physical interactions within the devices. Foremost of these is the study of the Coulomb interaction between the electrons and the impurities and between the individual electrons themselves. This Coulomb interaction has two parts: first, the nature of discrete impurity and how this affects device performance and secondly, how the Coulomb interaction affects the transport of the carriers through the device. In addition to fluctuations of discrete dopants in the active channel region showing random values both in number and position, trapping of a single carrier charge in defect states near the Si:SiO_2 interface has an exchange area accompanied by related local modulation in carrier density and mobility contributing to transport across a gate-induced channel. This area within which the interaction of a trap and carriers in the inversion region takes place is comparable to the characteristic device dimensions and has been a source of profound reliability related failure of devices in terms of fluctuations in the amplitudes of reliable drain and gate current in such MOSFETs. Corresponding random telegraph signals (RTS) with amplitudes larger than 60% have already been reported at room temperature in

decananometer channel length devices [2]. Depending on the aggressively scaled device geometry, a single charge or a few discrete charges, trapped in hot carrier stress-induced or radiation-created defect states, will be sufficient to cause a pronounced degradation in decananometer MOSFETs.

A random telegraph signal with multiple on state and off state pulses appearing as an ensemble as a function of time is characterized by (i) pulse height which is computed as signal amplitude, (ii) the mean time the signal exhibits upper level or the high value of pulse known as capture time τ_c, and (iii) the mean time the signal exhibits lower level or the low value of pulse known as emission time τ_e. The bias voltage dependences of the capture and emission times allow one to determine the location of the defects. In MOSFETs with current decananometer technology nodes, they are found to reside in the oxide up to a few nanometer from the interface and hence within tunneling distance of the inversion layer. The rather anomalous nature concerning observed multilevel discrete switching in some ultrashort gate length and narrow width MOSFETs has been supported by the evidences of distribution of physical characteristics measured for the defects such as trap entropy (trap activation energy varying with τ_c or τ_e), trap energy E_T, trap position along the channel x_T and along the channel depth or oxide depth from the $Si:SiO_2$ interface y_T, thus accounting easily for the wide range of time constants necessary to generate the $1/f$ noise [3]. As parts of the review of established concepts of RTN based fluctuations in drain current and threshold voltage of scaled MOSFETs for sub-45 nm gate length, in Chapter 2, a survey of notable research publications has been enunciated with due emphasis on

documenting each paper's major technological contributions to modeling of RTS phenomenon. In Chapter 3, kinetics and physical origin and process of traps at the interface and inside SiO_2 are discussed to bring forth how traps interact with the channel electrons in a trapping detrapping process.

This research report aims at providing a fully comprehensive 3-D ensemble Monte Carlo (EMC) based device simulation with a single or a number of traps residing at the Si:SiO_2 interface. One of the derivative of random telegraph noise (RTN) is threshold voltage variation and its fluctuations in presence of random dopants and random interface trap which pose a long-standing reliability concerns as the device gate length is scaled aggressively to 45 nm and beyond. This report for the first time numerically extracts these parameters as a function of trap position in the channel from MOSFET source to drain close to the oxide interface and for device bias conditions at threshold and technology node-impacted geometry conditions. For accurate representation of trap's random trapping and detrapping of channel carriers in a temporal way, EMC device simulation is not the method of choice. This is due to the fact that in real time, capture and emission processes are of a few milliseconds to a second range. On the other hand, the EMC device simulation time for steady state convergence cannot be reduced below a few nanoseconds and time dependent capture and, therefore, capture and emission process cannot be properly modeled by the EMC simulation scheme. Therefore, in the EMC simulation study presently conducted, the trap is modeled as a static negative charge. The short range Coulomb interaction in the development of this 3D EMC simulation model is accounted for by using a

molecular dynamics (MD) routine [4-5]. Within this approach, the mutual Coulomb interaction amongst electrons and impurities is treated in the drift part of the MC transport kernel. Indeed, the various aspects associated with the Coulomb interaction, such as dynamical screening and multiple scatterings, are automatically taken into account. Since a part of the Coulomb interaction is already taken into account by the solution of the Poisson equation, the MD treatment of the Coulomb interaction is restricted only to the limited area near the charged particles. In Chapter 4, real space treatment of electron-electron and electron-ion interactions in conjunction to the 3-D Ensemble Monte Carlo device simulation scheme employed for this research are explained .

Accurate and physical models for RTF are essential to predict and optimize circuit performance during the design stage [6]. Currently, such models are not available for circuit simulation. The compound between RTF and other sources of variation, such as random dopant fluctuations (RDF), further complicates the situation especially in extremely scaled CMOS design. In the vicinity of a trap site, the electrostatic short range Coulomb forces between a trap, a number of carriers in flow within the trap's boundary and dopant ions just underneath the channel in the depletion region, modify the electrostatic surface potential in the channel from source to drain in spatially random and discrete manner. Accurate replication of these multiple peaks and valleys of the surface potential is critical to be accounted for by the analytical models for inversion conditions and when spatial inhomogeneity exists due to interface trap, inversion carriers and depletion region dopant ions. This aspect is not presently accounted

for by most analytical device models including the models presented in Refs. [7-8] that are related to the present research. In Chapter 5, two well-researched analytical models based on dopant number fluctuation [7] and percolation theory [9] are reviewed and their usefulness in defining threshold voltage and its fluctuation in presence of a set of different random dopant configurations and a single random interface trap are outscored. It will be shown that these two very well known models fail to account for large threshold voltage fluctuations that are revealed by 3D EMC device simulation for source side trap positions in the channel of a 45 nm MOSFET. Therefore a new model is proposed which, for the first time, highlights the carrier mobility fluctuations resulting from source side trap positions with the spatially variant short-range interaction force causing potential inhomogenous and random spikes in surface potential barrier near the source. It will be shown that the new proposed model most accurately represents the threshold voltage fluctuation trend as extracted from numerical EMC device simulation method. In Chapter 6, simulation results from EMC device simulation method and the three analytical models are compared for threshold voltage and its fluctuations in presence of random channel dopant configuration types and a single interface trap.

Since halo pocket implanted device engineering method is being increasingly implemented for transistor level threshold voltage control with aggressive scaling of the device for 45 nm node and beyond, study of trap induced threshold voltage fluctuations is very important in determining the reliability projections for such devices. The results obtained by EMC simulation for a

shorter and larger source and drain halo doped MOSFET on threshold voltage and its fluctuations in a random channel dopant configuration along with random interface trap will be also discussed in this Chapter. Chapter 7 concludes this research summarizing all the discussions and valuable observations. Future work with the possible simulation study for oxide traps that are within a certain depth in the SiO_2 close to the interface with the channel, will be pointed out in Chapter 8.

CHAPTER 2

Historical trends and survey of past seminal research articles on understanding and characterization of random trap and dopant fluctuations related attributes

The first scholarly article cited in this section with regard to understanding the random telegraph noise related phenomenon and characteristics is the seminal research work conducted by M. J. Kirton and M. J. Uren in their paper entitled "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low frequency (1/*f*) noise" which appeared in Journal of Advances in Physics in 1989 [3]. The authors of the above referenced article stated distinctive observation that the defects residing in oxide or Si:SiO_2 interface are not found to be simple Shockley-Read-Hall (SRH) type but show evidences of strong lattice relaxation on capture kinetics as well as large entropy change. In addition, the traps show a wide variation in all their characteristics such as energy level (E_T), capture activation energy (E_A) and cross-section (σ_E or σ_C); quite consistent with their amorphous environment. Then the authors made critical assessment on the long-running discourse over the origin of low frequency 1/*f* noise stemming from two contrasting established theories namely "carrier number fluctuation" versus "mobility fluctuation" and also discussed extracted outcomes from quantum 1/*f* noise theory. The authors found that a conclusive resolution to this debate could not be achieved owing to the lack of consensus emerging due to the little detailed information that can be extracted

from the conventional ensemble-averaged power spectrum. In addition, the seemingly complex nature of experimentally observed RTS characteristics has been reported in this article where the proposed explanations concentrated on collective capture into a defect cluster, Coulombic interaction within a defect cluster and physical reconfiguration within a set of metastable minima. The paper cited facts as an outcome from experiments carried out by typical conductance-voltage techniques to show that there are two classes of interface defects. The first includes those defects normally seen and which presumably reside at the interface and are characterized by a single time constant. The second class of defects resides in the oxide close to within a few nm from the oxide-semiconductor interface and exhibits a wide range of time constants and are rendered responsible for RTS and 1/*f* noise. In connection to this observation, the paper quoted experimental evidence of gate voltage dependence of observed RTS. The dependence of gate voltage measured in a 0.4 μm^2 n-channel MOSFET at room temperature revealed that as gate voltage is increased, the time in high current state (electron capture) is reduced dramatically while the time span in the low current state (electron emission) remains largely unaffected. Considering that there is only one defect energy level E_T within a few kT of the surface Fermi level E_F, the energy separation E_T-E_F becomes less positive as gate voltage V_G increases. Thus, for the linear region of operation of the MOSFET, the fractional occupancy of the defect site is governed by the Fermi-Dirac distribution with a

degeneracy factor g. The mean capture time constant $\overline{\tau_c}$ and the mean emission time constant $\overline{\tau_e}$ are related by

$$\frac{\overline{\tau_c}}{\overline{\tau_e}} = g \exp\left(-\frac{E_F - E_T}{kT}\right). \tag{2.1}$$

The possible decrease of $\frac{\overline{\tau_c}}{\overline{\tau_e}}$ ratio is explained by the fact that on electron capture into a localized electron state, it would appear that the negative electrostatic potential set up by the trapped charge is responsible for a localized increase in channel resistance. On the other hand, the numerical modeling outcome of equation (2.1) shows that $\bar{\tau}_e$ value is lower than $\bar{\tau}_c$ depending on trap type, i.e., for a repulsive type of trap, $(E_F - E_T) < 0$ making $\bar{\tau}_c / \bar{\tau}_e$ larger which must be taken into account when the above analysis is put forth. Through careful equations set up, the authors M. J. Kirton et al. [3] found that, for devices operating in strong inversion, the potential change at the trap is usually about half the change at the surface. Since the potential at the inversion layer charge centroid moves about half the rate of the surface potential, this places the trap in the middle of the inversion layer that is in the silicon rather than in the oxide. The authors further illustrated that single electron-trapping into the defect states inside the oxide provided the simplest explanation for the majority of the data though this could not rule out the possibility that a small proportion of the defects are indeed multi-electron trapping sites. The discussion continued to show the effect of single-electron capture model on the gate voltage dependence of capture time, the estimation of trap depth into the oxide for device operating around threshold

and the behavior of the emission time with gate voltage. The initial theories of carrier number fluctuations and changes in the mobility and inversion layer thickness coupled together still could not explain the experimental capture and emission time constant values as a function of gate voltage. In determining σ, the cross-section of the traps, an Arrhenius type equation form exists where the traps are thermally activated with an activation energy or barrier ΔE_B and a cross-section pre-factor σ_0 . It was found that the very strong dependence of τ_c on V_G was accounted for by a monolithically increasing capture cross-section with resulting effect in increasing σ_0 and ΔE_B remaining constant throughout the range of V_G. The authors then expounded the limitation of SRH based models of τ_c and τ_e that in the case of defect in the oxide of a MOS structure, there are the following two complications restricting the use of SRH based formula. First, the inversion layer charge is displaced from the defect site and second, as the gate voltage changes so does the electric field strength in the inversion layer. As the electric field strength increases, the inversion layer charge density peak moves closer to the interface, thus increasing wavefunction overlap. The original assumption of a uniform inversion layer charge density Q_n to calculate relative RTS amplitude ($\frac{\Delta I_{drain}}{I_{drain}}$) becomes less valid. In addition, the changing oxide field strength resulting from increase in V_G or decrease in oxide thickness lowers the tunneling barrier. The net result is an increase in σ_0. Besides, the invariant nature of ΔE_B or trap binding energy is not supported by experimental results particularly for weak inversion. Uren et al. found that in strong inversion, the electric field is

fully screened by the inversion layer leading to only minute change in ΔE_B if the trap is located at the oxide-semiconductor interface. But near threshold and weak inversion of MOSFET, the scenario changes implying that in order to model the experimental results, the trap binding energy ΔE_B is changing as a function of gate voltage over and above what one would expect from simple electrostatics alone. The authors successively found that the surface potential fluctuations near the threshold operation can be invoked to explain the behavior of ΔE_B as a function of gate voltage. The authors add their own insight into the physical process of trapping-detrapping by noting that in strong inversion, the electron number density is high and the trapped charge is fully screened by the inversion layer charge. However around threshold, the image charge of the trapped electron is shared between the gate, the channel and the depletion region and the number density is very sensitive to the gate bias. Thus the location of the image charge is changing very rapidly and so constitutes a rapidly changing local environment for the defect. This gives rise to modifications in the bonding and the dynamical properties of the trap which are reflected in V_G dependent enthalpy and entropy terms, respectively. One important aspect of the relative amplitude of the RTS, a reliable metric for RTS reliability analysis, is discussed here from the viewpoints of the author of the presently surveyed paper. Working with their initial hypothesis, the authors stated that after an electron got trapped into an Si:SiO_2 defect site at the interface, the reduction in source/drain current comes about through a reduction in the number of free carriers in the channel. In the strong inversion regime, the screening of the trapped charge is carried out by the

inversion layer electrons. As the gate voltage is reduced to threshold and below, the screening of the trapped charge is now principally shared by the depletion region and the gate and the estimation of reduction in total carrier number becomes accordingly complex. In moderate and weak inversion, there is a small area Δa in the vicinity of the trap where all changes in charge distribution takes place on electron capture into the oxide defect. This Δa is also based upon total exclusion of the inversion layer charge. From experimental evidence and model formulation, the average behavior was reasonably reproduced by Uren's theory although a large number of RTS amplitudes appear to be corresponding to significantly less or greater than the case of trapping of a single electron. In order to address this anomalous nature of multiple transitions in relative RTS amplitudes, the authors further commented that measured distribution of amplitudes in the small gate area devices was not related to any distortions out of nonhomogeneties specific to the small area or by the proximity of the device parameter, but is representative of the characteristics of the channel. Another reason for this widely varying amplitude pattern is embedded into the fluctuation of the surface potential in the inversion layer close to the interface due to a spatially random distribution of fixed charge near the Si:SiO_2 interface. Uren et al. cited the work of J. R. Brews [10] that as a result of surface potential fluctuation, the carrier drift mobility will be reduced and takes the form $\langle \mu \rangle = \mu_0 \left(1 - \frac{1}{2} \langle \sigma_{\varphi_s}{}^2 \rangle \right)$ where $\sigma_{\phi s}$ is the standard deviation surface potential fluctuations. In weak inversion this can lead to an inhomogeneous transport and a

measurable reduction in mobility. After citing all these relevant works of different authors in their paper, Uren concludes that the wide distribution of amplitudes is a real effect and is not fully accounted for by the presence of gate bias dependent charge exclusion area, multi electron capture or potential fluctuations. This brings the issue of carrier mobility fluctuations with changing trap scattering cross-sectional area. A positively charged scattering center is neutralized by electron capture and is thus turned off corresponding to a discrete increase in current. A neutral center upon capturing an electron becomes singly negatively charged giving rise to a reduction in current due to increased scattering. Therefore the range of amplitudes and their various locations may be accounted for by some scattering being more strategically located to the inversion carriers than the others. The temperature effect on relative amplitude variation becomes more prominent at lower temperatures where universal conductance fluctuations (UCF) become important. UCF arises in the regime in which the elastic scattering length is much smaller than the sample channel length L and the inelastic scattering length is larger than L. One then finds a large random component of the conductance which depends on the detailed relative positions of the elastic scattering sites. The authors further stated that the scattering rates in the silicon inversion layer are not known accurately at every temperature although at elevated temperature phonon scattering dominates over elastic Coulomb scattering. Finally the authors made a curious observation that recent findings on the noise in metallic microstructures provide striking evidence that by altering its configuration, a phase known as metastability, a defect can impact the sample

conduction resistivity via changes in nearby scattering cross-section. Then it might be possible that such changes in configuration with no change in charge state for the $Si:SiO_2$ interface defects could modulate the channel conductivity particularly when a number of them reside in the oxide and are very closely spaced. Therefore, some defect structures can become more efficient in modulating the inversion layer conductivities than others. But the paper could not confirm this for certainty by not being able to document any physical processes by which such structural changes in the trap state without mutation in the charge state of the traps can be proven feasible.

The second scholarly article on this topic is by E. Simoen, B. Dierickx, C. L. Claeys and G. J. Declerck entitled "Explaining the Amplitude of RTS Noise in Submicrometer MOSFET's" which was published in IEEE Transactions on Electron Devices in 1992 [11]. In their paper the authors first cited the propositions outlined by M.J. Uren et.al [3] surveyed previously that the model explaining the characteristics of relative amplitude change for RTS as a function of drive current from subthreshold to strong inversion has to take into account the channel resistance modulation due to the switching of a single interface trap which confirms the constant plateau at weak inversion. In strong inversion a roll off with I_D was observed but the wide scatter of the amplitudes of $\frac{\Delta I_D}{I_D}$ in the plateau region can be explained in terms of electrical active length L_t similar to Δa (cored-out area) as discussed by Uren et. al. [3]. The value of L_t is large at weak inversion and screening of the trap potential in strong inversion causes L_t to

drop. The authors of this paper claim that both models can be made compatible with each other by proposing a new analytical transport model that facilitates the discussion of the factors determining the RTS amplitude by the proper location and nature of the trap in two possible states, one being full and the other being empty. The model takes into account the change in carrier mobility induced by ionized or neutral impurity scattering but excludes the incorporation of more exact and complex short range and long range Coulomb force influencing the scattering process. In the case of unscreened Coulomb potential, the authors outline mathematical equation that the presence of a trapped electron at the interface will induce a charge to the channel conductivity $\sigma = \mu Q_S$ over some distance L_t either by changing the local surface potential (thus Q_S) or by varying the local mobility by introduction of an ionized scattering center. When the trap is charged, a channel electron will be scattered by the Coulomb potential associated with the charged state of the trap resulting in new channel conductivity within the active region of the length L_t surrounding the trap. In the case of screened Coulomb potential during strong inversion, L_t will be reduced due to screening and the potential fluctuations in this case extend over some screening length. The authors then documented three factors influencing the RTS amplitude, i.e., (1) completely blocked channel (also cited in previous article mentioned in this section), (2) the role of surface potential fluctuations and (3) the mobility effects. In the case of completely blocked channel, the resistance of the cored out region becomes infinitely high when occupied and the maximum RTS amplitude increases upon cooling which can be explained by the fact that the trap length L_t

increases. The authors find that in order to explain the wide scatter in the plateau of experimentally measured RTS amplitudes, the hypothesis of presence of completely blocked channel can be only achieved if L_t is a trap specific variable. Therefore, trap location and nature of trap are found to be physical causes of this scatter. The authors subsequently found less correlation with trap position of the scatter in the plateau values and the most plausible explanation the authors come up with is that there exists a correlation between trap exclusive zone $\sim L_t^2$ and trap's charged state specifically linked to the capture cross section σ_T as also suggested by Uren et al [3]. The values of σ_T hitherto extracted point towards capture by neutral or repulsive centers, i.e., acceptors close to the conduction band and donors close to the valence band. By transforming the time domain RTS amplitude characteristics plot into a power spectrum and extracting the corner frequency f_T from the spectrum, it can be shown that f_T is a sensitive function of σ_T implying that for a trap with smaller cross-section, f_T will be small while the corresponding amplitude will be large. The reverse is true for fast traps with larger capture cross-sectional area. This suggests that $\frac{1}{L_T{}^2}$ in the plateau region is roughly proportional with $\frac{1}{\sigma_T}$ for traps having the same energy. The role of surface potential fluctuations can be ushered in by the observation that generally current is not completely blocked by the charged trap and the surface potential fluctuation $\delta\varphi_s$ induced by one trap charge q at the interface of a n-MOSFET gives rise to scatter correlating roughly with $\frac{1}{Q_s'\upsilon}$ for υ between 1 and 2. From the

knowledge of Q_s with $\delta\varphi_s = 0$ and by explicit analytic equation of $\delta\varphi_s$ as a function of Q_s, Q_s' as a function of $\delta\varphi_s$ can be determined. The surface potential nonuniformity can arise from the fact that interface is far from ideal and contains both topographical (surface roughness and inhomogeneous oxide thickness) and chemical (interface fixed charge and defects as scattering center) imperfections. The fluctuation in $\delta\varphi_s$ can be spread over several kT. Consequently in weak inversion, current flow will be inhomogeneous and occur along a potential minimum path. In strong inversion, fluctuations are smeared out by screening and a homogeneous current flow occurs. Thus the authors pose their observation that in their transport model, the change in Q_s will affect the fractional conductivity change α_σ. In essence, to a large extent the scatter of amplitude values in the plateau region and subsequent roll-off can be attributed to a larger spread in Q_s' through a similar spread in $\delta\varphi_s$ values. The third case that local mobility modulation contributing to random scatter in amplitude is in commensurate observation with M. J. Uren et al's findings [3]. For the majority of anomalous signal amplitudes as experimentally evidenced, the authors put their viewpoints that some interface defects show configurational metastability, i.e., a complex center may change its local arrangement (symmetry, relative positions of the constituents) yielding a change in trap energy with respect to the surface Fermi level. This transition may even take place without change of charged state of the trap and is claimed to cause a long-range change in scattering cross-section (scattering efficiency). The authors formulate a useful equation to modify L_t in the

case of anomalous trap action by incorporating long range change in scattering $L_t = \frac{\mu^2 F}{qm^*}$ with m^* the carrier effective mass and F the electric field (affecting free flight drift of carriers without scatter). This new equation suggests that a different dependence on electrical parameters is observed for a "Coulombic" versus "anomalous" trap. The authors finish their research findings by invoking that RTS amplitude as a function of average lateral electric field ($\propto V_{ds}$) can be measured to properly account for the average distance a free carrier with drift velocity travels between two scattering events giving rise to additional change in $\Delta\mu$ owing to a statistical spread in τ_m, the momentum relaxation time. One final remark that can be reached from Declerck et. al. paper is that the actual drain current degradation computed by their model equations from subthreshold to strong inversion regions of a sub-100 nm gate length MOSFET is much worse compared to derivations extracted from M. J. Uren et al. model. Only in the limited case when $L_t > W$, i.e., channel width, it has been computationally verified that the drain current plateau values at the subthreshold region to weak inversion closely follows plateau values derived from M. J. Uren et al. model. Since on most occasions, L_t values even in low gate bias and low inversion charge density are found to be at least equal or a fraction of order higher than gate width W, Declerck et al. model cannot accurately predict the observed experimental and numerical simulation based (such as Monte Carlo scheme) drain current fluctuation pattern from subthreshold to strong inversion region of a MOSFET.

The third scholarly article cited here with regard to RTS analysis has a content full of comprehensive modeling of RTS noise amplitude and spectrum, and derivation of statistical quantities that can be incorporated in circuit simulation of submicrometer MOSFETs. This paper authored by G. I. Wirth is entitled "Modeling of Statistical Low-Frequency Noise of Deep-Submicrometer MOSFETs" and appeared in IEEE Transactions on Electron Devices in 2005 [12]. The authors of this article first unfolded the paper's objective that a detailed statistical model encompassing all aspects of LF or 1/*f* noise was not available and hence provided the insightful analytical derivation of statistical model parameters for proper emulation of variations of LF-noise performance of deep submicrometer devices. The authors in this paper built their model based upon an equivalent gate voltage fluctuation caused by the impact of variation of the charging state of the traps on drain current. The authors systematically derive a set of model equations for (i) equivalent gate voltage fluctuation as a function of trap density, and (ii) gate voltage related noise power spectral density SV_G per area in the channel at a certain location caused by the traps. From the knowledge of location of the trap with a distance x from the interface and the energy at frequency f , a closed form final expression of $SV_G(f)$ was derived that is continuous over the whole range of operating points of the MOSFET. The model can be fitted to experimental $SV_G(f)$ by taking the position dependent mobility into calculation and trap number fluctuation at a certain frequency with trap energy. Assuming the number of traps following a Poisson statistics, the normalized standard deviation of noise power density has been found to be inversely

proportional to the square root of the product of the number of traps at a decade frequency and the device area. The standard deviation also directly follows the square root of the ratio of average value of signal amplitude quadrupled to square of average value of amplitude squared. After this detailed derivation, the authors related the factors that affect the amplitude fluctuation related term of standard deviation. It has been found that that the variance of amplitude squared is a superposition of (i) the variance of the mobility with amplitude variation affected by the change in mobility, (ii) the variance of channel carrier density with amplitude affected by the channel carrier charge or number, and (iii) the variance of $\frac{\tau_c}{\tau_e}$, capture to emission mean time ratio with amplitude affected by the change of this ratio. Following the above quantification, the authors discussed the influence of mobility fluctuations, carrier number fluctuations and fluctuations in the capture and emission time ratio to quantify in a closed form analytical expression of the final form of standard deviation of noise power spectral density. The authors make important observation that scattering efficiency depends on inversion layer parameters like charge carrier velocity, carrier density and on the device geometry. If the vertical distance d from the interface where the trap is located, is a random variable, it contributes to the dispersion of noise. The authors then derive analytical expression to find the standard deviation of mobility fluctuation being inversely related to device area and directly related to critical radius r_C (the overlap region surrounding the inversion layer within which an interaction with a trap is encountered) squared. Then the authors found the

analytical expression for the standard deviation of carrier number fluctuation term. At low drain voltage V_{ds} the channel is uniform and $N_c(y) = N_c$ but for transistor operating in the saturation region RTS amplitude depends significantly on the lateral position y of a trap within the channel. The scattering in RTS amplitude due to the variance of $\frac{\delta N_C}{N_C(y)}$ increases with increasing drain bias and reaches a maximum when the device is operated in saturation region. The authors find that the variance of carrier number fluctuations depend on the drain to gate voltage ratio with an exponent five. The authors conclude their modeling analysis by investigating the influence of capture and emission time constant variations on RTS amplitude, a very notable analysis which has not been documented heretofore by other researchers. When $\tau_c = \tau_e$, the corresponding RTS amplitude will be largest. For asymmetric distribution of these time constants, RTS amplitude will be smaller. The authors introduced a term $\beta = \frac{\tau_c}{\tau_e}$ and conjectured that to evaluate the standard deviation of β analytically, the exact bias point dependence of τ_c and τ_e is needed and detailed time domain signal characterization is mandatory. Therefore, in the modeling analysis, a compact form of constant k_β is assumed by the authors. Lastly, in order to fit experimental data, the authors have used these analytical expressions to derive values for these parameters giving good agreement.

The fourth article surveyed in this is the important contribution of Professor Asen Asenov and co-authors presentedin their paper entitled “RTS Amplitudes in

Decananometer MOSFETs: 3-D Simulation Study" which was published in IEEE Transactions on Electron Devices in 2003 [2]. The authors conducted an atomistic 3D simulation study based on ensemble Monte Carlo to properly parameterize the effect of single carrier trapping on the drain current in decananometer MOSFETs. The authors make density gradient corrections to the drift diffusion approach. Main drawback of this work is that simulations do not take into account the local modulation in the mobility associated with the trapped charge which has been validated to be an important determining metric surveyed in papers discussed in previous paragraphs of this chapter. In addition, the simulation environment, as proposed by the authors, can handle the simulation of a single trap only and multitrap contributions with trap spacing have not been incorporated into their simulation model. For the random discrete dopants, Asenov et al. [2] found that in weak inversion the surface potential fluctuation results in current percolation through the valleys in the potential landscape and trapping of electrons in defect states positioned along the dominant current percolation paths will produce RTS with large amplitudes. In weak to moderately inverted MOSFETs, the largest RTS amplitude does not arise from trap located in the middle section of the channel but in the regions with the deepest valley of the potential landscape corresponding to the highest density of percolating current. Therefore the trapping of a single electron in the vicinity of a dominant but narrow current channel has a strong effect on the overall current of the device.

In a series of publications Professor Vasileska et al. [4-5] have proposed and implemented EMC device simulator that address the limitations of Asenov et al's

[2] simulation drawbacks. For instance, in the two classic papers cited in referred journals entitled “Ultrasmall MOSFETs: The Importance of the Full Coulomb Interaction on Device Characteristics” and “A Novel Approach for Introducing the Electron-Electron and Electron-Impurity Interactions in Particle-Based Simulations”, the simulation of the Coulomb interaction has been made more robust and precise by separate calculation of the short-range and the long range e-e and e-ion interaction. In these works, at high doping densities, it also showed that the carrier in the channel was interacting with several impurities (random dopants or ions) at any given instant of time.

From the discussion presented in this section, it is evident that the e-e and e-i interactions coupled with random traps having capturing or emitting single or multiple channel electrons are important determining factors in quantifying changes in RTS amplitudes and threshold voltage fluctuations as a function of trap positions. This dissertation utilizes the ground work done by Professor Vasileska and her co-workers to use their constructed EMC simulation environment to perform new simulations on trap-induced different reliability projections for sub micrometer MOSFET operations.

CHAPTER 3

Electrostatics of $Si:SiO_2$ Interface and Oxide Traps

The single most important interface in semiconductor technology is that between silicon and its thermally grown oxide. This interface with its propensity to surface micro-roughness after in-situ fabrication plays a crucial role in the performance of today's high speed MOSFET devices. The degree of perfection of the interface has been stipulated to be really exacting in terms of process integrity where a typical device-quality interface has defect densities on the interfacial plane of the order of 10^8-10^{10} cm^{-2} eV^{-1} resulting in defect densities of the order of 1 to 100 defects per square micron assuming the defects are located within one eV of energy distribution from the Fermi energy. As the device area is shrunk to aggressively scaled sub-μm^2 size with scaling-preserved process tolerances, the number of defect densities do show an upward trend and considering that 10^{11} cm^{-2} eV^{-1} values are at least readily encountered, the number of defects seem to reduce to less than 3 in number per square micron within an eV energy distribution for a device size of W×L = 50 nm × 50 nm. The reason reliability concern did not arise in wide gate area technology generation is because with a good number of traps lying within a few eV of Fermi energy, the spatial distribution of energy levels is more tighter making the energy barrier values ΔE_B a fraction of an eV. Hence the carriers trapped in traps easily reemit to inversion layers making RTS amplitude variation almost nonexistent. But in today's aggressively scaled device size, even though the trap numbers are countable and

sparse, these traps can be located deep within the oxide with higher ΔE_B differential and a carrier once trapped in a trapped site, may stay there for a prolonged period of time and never get reemitted to inversion layer causing severe RTS amplitude drawbacks. The surface level trap lying close to the interface can block the carrier flow in the channel by causing local potential fluctuations where significant spread of RTS variation can be observed for even a single trap closer to source side to mid-channel zone impeding the carrier flow. Also one way carrier gets trapped and detrapped is through tunneling from inversion layer to a trap location and in earlier technological generation with thicker gate oxide, tunneling was not as significant as it is today with the gate-oxide reaching nanometric thickness. The conclusion is with the channel electrons being random, presence of very few defects will suffice to cause notable RTS related device operation failure for current ongoing technological generation of MOSFETs.

In their research findings referenced in [13] involving characterization experiments from conductance and DLTS measurements on MOS capacitors, M. J. Uren et.al. revealed that all the effects on trapping or detrapping originate from defects in the oxide known as bulk oxide traps close to the interface and also surface traps located at the interface and close to the silicon conduction band edges. The bulk oxide traps are known for their slow time constants for charge exchange with mobile carriers in the inversion layer between source and drain of a MOSFET and these slow defects are found to affect the plateau region of RTS related drain current amplitudes at relatively low gate bias. On the other hand, surface or interface defects are known as 'fast' states and affect the moderate to

strong inversion region of operation of MOSFET at moderate to high gate bias. The hypothesis with which this complex trapping or detrapping of charge carriers by traps has been explained, is propounded as multiphonon capture and emission process. Before embarking on the authors' detailed analysis of the process, we briefly point the usual conceptualized understanding of trapping and detrapping as is commonly observed in the normal operation of a MOSFET [14].

Coulombic attractive centers, as the name implies, are charge centers that attract injected carriers (electron) and thus will be positively charged. These centers have the largest capture cross sections ranging from 10^{-12} to 10^{-14} cm^2. These positively charged centers owe their origin from sodium-content related trapping sites if thermal oxidation of dry oxygen ambient is preferably used. The neutral trap centers which are initially uncharged, have a capture cross section of 10^{-14} to 10^{-18} cm^2. Water vapor related traps are attributed to this branch of bulk oxide traps. The Coulombic repulsive center has the smallest capture cross section, ranging from 10^{-18} to 10^{-21} cm^2. Therefore an approaching carrier of the same negative charge sign of these traps will initially be repelled by Coulombic forces, but if it has enough energy to overcome this barrier, the short range forces can capture the carrier.

The detrapping mechanisms responsible to reemit the trapped charge are: (1) photon assisted depopulation, (2) phonon assisted depopulation, (3) impact ionization and (4) tunneling. In the photon assisted process, a photon with an energy greater than the trap depth energy is absorbed by the trapping carrier, giving it enough energy to escape from the trap. In the phonon assisted process

the trapped carrier receives its energy from thermal lattice vibrations. Impact ionization is a two carrier process in which a high energy carrier collides with a trapped carrier. The trapped carrier receives enough energy to escape the trap center and the original high energy carrier retains enough energy implying mostly elastic collision process so that it does not become trapped. Detrapping due to tunneling is a quantum mechanical process, present in highly degenerate substrate doping conditions in scaled MOSFET devices, by which a trapped carrier escapes by tunneling through a thin energy barrier to the conduction band or the oxide or through one of the interfaces to the conduction (valence) band of the substrate or gate material. Tunneling through the interface requires that the trap be located very close to the interface.

3.1 Multiphonon Capture And Emission Process

A configuration-coordinate diagram showing the changes in total energy of the system as an electron is transferred from the inversion layer into a 'slow' interface defect is shown in Figure 3.1. The energy zero in this figure corresponds to the empty trap with an electron available at the Fermi energy. The broken curve shows the variation in total energy as the empty defect distorts. The full curve enclosing the open circle shows the same with the electron in the conduction band. The full curve enclosing the full circle depicts the variation in total energy of the trap after it has captured an electron. At the crossover there is strong overlap between the inversion-layer state and defect state. This non-radiative transition is induced by transitions between vibronic states which differ in electronic energy but have the same total energy. On electron capture the defect

state is well away from equilibrium and the excess energy is dissipated by multiphonon emission.

In this kinetics, there has been found a wide ranging capture cross section values resulting from spread in pre-factor σ_0 reflecting the nature, symmetry and degeneracy of the traps as well as exchange interactions between initial and final state wavefunctions. Also discovered is a wide range of energy barrier values ΔE_B of the trap, much in agreement with capture process into defects in an amorphous material (SiO_2) with its consequent continuous distribution of trap environments. Another parameter worth mentioning here is the entropy of ionization of a trap site ΔS. On the release of electron back into the inversion layer, the main contributions to the increase in entropy as cited by M. J. Uren and co-authors are the following:

(i) the softening of the lattice in the immediate vicinity of the defect, (ii) the placement of the electron in an anti-bonding conduction band state and (iii) the change in trap degeneracy which give rise to a contribution proportional to $ln(g)$.

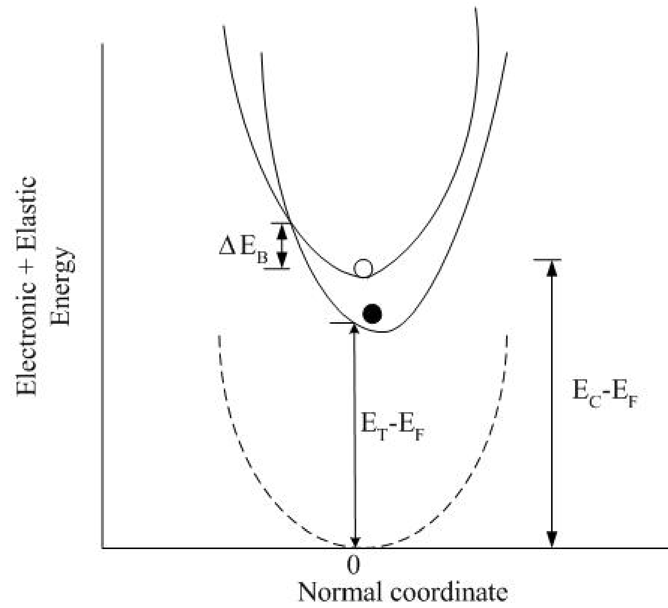

Figure 3.1 : Configuration coordinate diagram. The energy zero of the system corresponds to the empty defect with the electron at the Fermi level. This is shown by the broken curve. o labels the empty trap plus a free electron in the inversion layer . • marks the filled trap (adopted from Ref. [13]).

In addition, the magnitude of ΔS is sensitive to modifications in the trap environment brought about by changes in applied gate voltage which have an impact on trap's electronic configuration making it appear metastable.

CHAPTER 4

Real-Space Treatment of the Electron-Electron and Electron-Ion Interactions

In particle-based device simulation schemes one couples the Monte Carlo Transport Kernel with a Poisson equation solver as shown diagrammatically in Figure 4.1. Briefly, after the free-flight scatter sequence, particle-mesh coupling takes place that is followed by a Poisson equation solution for the electrostatic potential and the electric field needed in the subsequent free-flight scatter sequence.

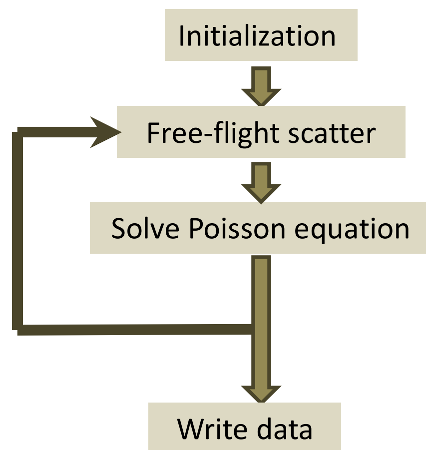

Figure 4.1. Typical flow-chart of a particle-based device simulator.

The Poisson equation is solved on a mesh that is determined by the Debye criterion. Namely, in critical device regions the mesh has to be smaller than the extrinsic Debye length [15]. If the mesh is infinitely small then the Coulomb potential is completely resolved. However, that would typically require a large number of node points. As in silicon devices, to get accurate results one has to

solve the 2D/3D Poisson equation every 0.1 fs, and the total simulation time is on the order of 5-10 ps, that means that the Poisson equation solution, which is the bottleneck for 3D simulations, has to be solved many times which, in turn, requires very efficient Poisson solvers. The time to solve the Poisson equation limits the number of node points that has to be used in the Poisson mesh. As the mesh has to be coarser that, in turn, reduces the amount of the short-range Coulomb interaction that is accounted for via the solution of the 3D Poisson equation. The short-range portion of the Coulomb interaction is typically accounted for by considering Coulomb scattering as additional scattering mechanism in the k-space portion of the Monte Carlo transport kernel. The proper calculation of electron-electron scattering and electron ion scattering requires a proper screening model. Screening requires evaluation of the distribution function, which is typically noisy and time consuming task [16]. Moreover, how much of the short-range Coulomb interaction and how much of the long-range Coulomb interaction is taken into account with the k-space approach is not really known and some overestimation or underestimation of the interaction usually occurs. Also, multiple scattering processes and dynamical screening are typically almost impossible to be accounted for.

To avoid the problem with the k-space treatment of the Coulomb interaction, a real space approach has been proposed by Lugli and Ferry [17] in which the electron-electron and the electron-ion interactions are accounted for via real-space molecular dynamics routine. It is important to note that direct application of the real-space molecular dynamics can be used for bulk systems only where it is not

required to solve the Poisson equation. This aspect has already been elaborated in the beginning of this section. Hence, an approach is needed that correctly accounts for the full Coulomb interaction in particle-based device simulators. The group from ASU has been in a sense a pioneer in this field and in our simulation modules we currently have implemented three approaches:

1. The Corrected Coulomb approach – an approach that we have introduced [5],
2. The particle-particle-particle-mesh coupling method due to Hockney and Eastwood [18],
3. Fast Multipole Method [19].

It is important to note that the Corrected Coulomb approach and the particle-particle-particle-mesh coupling methods are similar in philosophy. Namely, a correction force is calculated given the mesh and it is that correction force that is used in the molecular dynamics routine. The fast multipole method is completely different in philosophy in a sense that the Laplace equation is solved to account for charges at the ohmic contacts and afterwards only fast multipole method is used to account for the full Coulomb interactions between electrons and electrons and ions. The difference between these two ideologies is graphically shown in Figure 4.2.

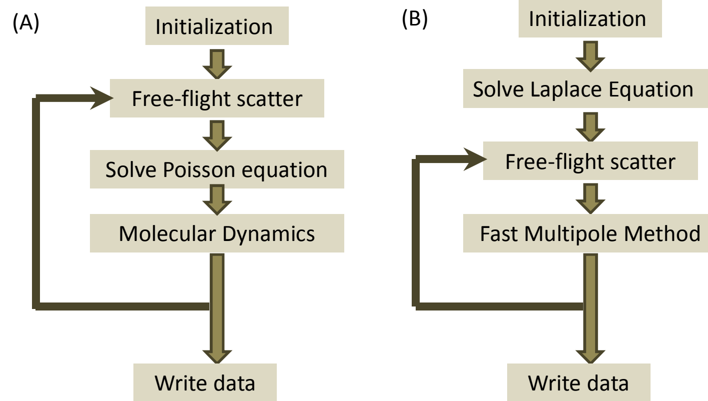

Figure 4.2. Philosophy behind the (A) corrected Coulomb approach, where correction force is used in the molecular dynamics routine, and (B) the fast multipole method where the full Coulomb interaction is being considered to get the force on the electrons in the free-flight portion of the Monte Carlo transport kernel.

In what follows, each of these methods is explained in more details. We first discuss the corrected Coulomb approach. Next the particle-particle-particle-mesh coupling method is discussed. Finally, the ideology behind fast multipole method is explained.

4.1 Corrected Coulomb Approach

Within the Corrected Coulomb approach the separation of the short-range and the long-range Coulomb interaction is accomplished in the following manner: a target and a fixed electron are placed in a 3D box and the separation between the target and the fixed electron is varied. For each separation of the target and the fixed electron the 3D Poisson equation is solved which gives the Hartree potential. The Hartree potential is used to calculate the Hartree force on the electron. Simultaneously, given the separation between the electrons, the

Coulomb force is calculated and the Hartree force is subtracted from the Coulomb force. This gives a correction force, which in general diverges when the separation between the target and the fixed electron is zero. Modification to the correction force has to be made to account for this divergence. The way that is accomplished is the following one. For distances smaller than the Bohr radius, linear interpolation of the force to zero is assumed. Since the correction force is significant for few mesh spacing, an outer radius is defined and all the electrons and/or ions that fall within the outer radius of the fixed electron are being considered using the electron-electron and electron-ion interaction to get the short range force on the target electron. That target force is added to the Hartree force and used in the subsequent free-flight portion of the Monte Carlo routine. Using this methodology, excellent agreement is achieved for the doping dependence of the low-field electron mobility between the simulation and the available experimental data. Results of these simulations can be found in Ref [4]. Also given in Ref. [5] are the implementation details of the corrected Coulomb approach.

4.2 Particle-Particle-Particle-Mesh Method

The particle-particle-particle-mesh (P^3M) algorithms are a class of hybrid algorithms developed by Hockney and Eastwood [18]. These algorithms enable correlated systems with long-range forces to be simulated for a large ensemble of particles. The essence of P^3M algorithms is to express the interparticle force as a sum of a short-range part calculated by a direct particle-particle force summation

and a long-range part approximated by the particle-mesh (PM) force calculation. Using the notation of Hockney, the total force on a particle *i* may be written as

$$\boldsymbol{F}_i = \sum_{j \neq i} \boldsymbol{F}_{ij}^{coul} + \boldsymbol{F}_i^{ext}. \qquad (4.1)$$

$\boldsymbol{F}_i^{ext}$ represents the external field or boundary effects of the global Poisson solution. $\boldsymbol{F}_{ij}^{coul}$ is the force of particle *j* on particle *i* given by Coulomb's law as

$$F_{ij}^{coul} = \frac{q_i q_j}{4\pi\varepsilon} \frac{(r_i - r_j)}{\left|r_i - r_j\right|^3}. \qquad (4.2)$$

Where $\boldsymbol{q}_i$ and $\boldsymbol{q}_j$ are particle charges and $\boldsymbol{r}_i$ and $\boldsymbol{r}_j$ are particle positions. In a P^3M algorithm, the total force on particle *i* is split into two sums

$$\boldsymbol{F}_i = \sum_{\substack{j \neq i \\ SRD}} \boldsymbol{F}_{ij}^{sr} + \sum_{\substack{j \neq i \\ GD}} \boldsymbol{F}_{ij}^{m}. \qquad (4.3)$$

The first sum represents the direct forces of particles *j* on particle *i* within the short-range domain (SRD), while the second sum represents the mesh forces of particles *j* on particle *i* over the global problem domain (GD) as well as the effect of material boundaries and boundary conditions on particle *i*. $\boldsymbol{F}_{ij}^{sr}$ is the short-range particle force of particle *j* on particle *i*, and $\boldsymbol{F}_{ij}^{m}$ is the long-range mesh force of particle *j* on particle *i*. The short-range Coulomb force can be further defined as

$$F_{ij}^{sr} = F_{ij}^{coul} - R_{ij}. \qquad (4.4)$$

Where $\boldsymbol{F}_{ij}^{coul}$ is given by Eq. (4.2) and $\boldsymbol{R}_{ij}$ is called the reference force. The reference force in Eq. (4.4) is needed to avoid double counting of the short-range force due to the overlapping domains in Eq. (4.3). The reference force should correspond to the mesh force inside the short-range domain (SRD) and equal to the Coulomb force outside the short-range domain. In other words, a suitable form

of reference force for a Coulombic long-range force is one which follows the point particle force law beyond the cutoff radius r_{sr}, and goes smoothly to zero within that radius. Such smoothing procedure is equivalent to ascribing a finite size to the charged particle. As a result, a straightforward method of including smoothing is to ascribe some simple density profile $S(r)$ to the reference inter-particle force. Examples of shapes, which are used in practice, and give comparable total force accuracy are the uniformly charged sphere, the sphere with uniformly decreasing density, of the form given in Eq. (4.5) and the Gaussian distribution of density. The second scheme gives marginally better accuracies in 3D simulations. For this case the reference force can be obtained [20] as in Eq. (4.5). Hockney advocates pre-calculating the short-range force, $F_{ij}^{sr}(r)$ defined in Eq. (4.4) including the reference force above for a fixed mesh. The reference, short-range and Coulomb force are each represented in Figure 4.3. It is important to extend the P^3M algorithm to nonuniform meshes for the purpose of semiconductor device simulation since practical device applications involve rapidly varying doping profiles and narrow conducting channels which need to be adequately resolved. A method similar to that used in Ref. [20] is depicted in Figure 3.3. Since the mesh force from the solution to the Poisson equation is a good approximation within about two mesh spaces, r_{sr} is locally chosen as the shortest distance which spans two mesh cells in each direction of every dimension of the mesh at charge i.

$$S(\mathrm{r}) = \begin{cases} \dfrac{48}{\pi r_{sr}{}^{4}}\left(\dfrac{r_{sr}}{2} - r\right), & r \le r_{sr}/2 \\ 0, & otherwise \end{cases},$$

$$\begin{cases} R_{ij}(r) = \dfrac{q_i q_j}{4\pi\varepsilon} \times \dfrac{1}{35 r_{sr}^2}(224\xi - 224\xi^3 + 70\xi^4 + 48\xi^5 - 21\xi^6) & \xi = \dfrac{2r}{r_{sr}} \text{ and } 0 \le r \le r_{sr}/2 \\ R_{ij}(r) = \dfrac{q_i q_j}{4\pi\varepsilon} \times \dfrac{1}{35 r_{sr}^2}(\dfrac{12}{\xi^2} - 224 + 896\xi - 840\xi^2 + 224\xi^3 + 70\xi^4 - 48\xi^5 + 7\xi^6) & r_{sr}/2 \le r \le r_{sr} \\ R_{ij}(r) = \dfrac{q_i q_j}{4\pi\varepsilon} \times \dfrac{1}{r^2} & r > r_{sr} \end{cases}$$

(4.5)

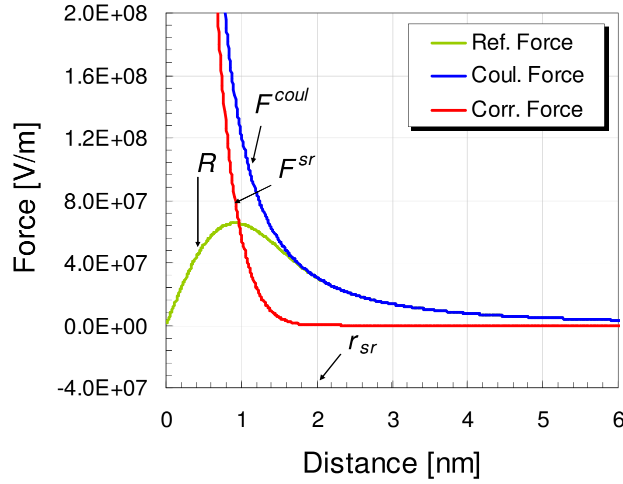

Figure 4.3. Illustration of the P^3M approach.

4.3 Fast Multipole Method

FMM was initially introduced by Rokhlin [21] as a fast solution method for integral equations for two-dimensional Laplace's equation. In Rokhlin's paper the term *FMM* did not appear but the main framework of FMM was constructed. After Rokhlin's work, Greengard [22] refined the algorithm, applied FMM to two and three-dimensional *N*-body problems whose interactions are Coulombic or gravitational in nature and showed the applicability of FMM to various fields. Greengard's 1987 Yale dissertation "*The Rapid Evaluation of Potential Fields in*

Particle Systems" won an ACM Distinguished Dissertation Award. In a system of N particles, the decay of the Coulombic or gravitational potential is sufficiently slow that all interactions must be accounted for, resulting in CPU time requirements of the order $O(N^2)$. Whereas, the FMM algorithm requires an amount of work proportional to N to evaluate all interactions to within roundoff error, making it practical for large-scale problems encountered in the fields of plasma physics, fluid dynamics, molecular dynamics, and celestial mechanics.

There have been a number of previous efforts aimed at reducing the computational complexity of the N-body problem. As mentioned in the previous sections particle-in-cell methods have received careful study and are used with much success, most notably in plasma physics. Assuming the potential satisfies Poisson's equation, a regular mesh is laid out over the computational domain and the method proceeds by:

1. interpolating the source density at mesh points,
2. using a fast Poisson solver to obtain potential values on the mesh, and
3. computing the force from the potential and interpolating to the particle positions.

The complexity of these methods is of the order $O(N + M \log M)$, where M is the number of mesh points. The number of mesh points is usually chosen to be proportional to the number of particles, but with a small constant of proportionality so that $M \langle\langle N$. Therefore, although the asymptotic complexity for the method is $O(N \log N)$ the computational cost in practical calculations is

usually observed to be proportional to *N*. Unfortunately, the mesh provides limited resolution, and highly non-uniform source distributions cause a significant degradation of performance. Further errors are introduced in step (3) by the necessity for numerical differentiation to obtain the force. To improve the accuracy of particle-in-cell calculations, short-range interactions can be handled by direct computation, while far-field interactions are obtained from the mesh, giving rise to so-called particle–particle/particle–mesh (P^3M) methods described in section 4.2 above. While these algorithms still depend for their efficient performance on a reasonably uniform distribution of particles, in theory they do permit arbitrarily high accuracy to be obtained. As a rule, when the required precision is relatively low, and the particles are distributed more or less uniformly in a rectangular region, P^3M methods perform satisfactorily. However, when the required precision is high (as, for example, in the modeling of highly correlated systems), the CPU time requirements of such algorithms tend to become excessive.

In FMM Rokhlin uses *multipole moments* to represent distant particle groups and introduces a *local expansion* to evaluate the contribution from distant particles in the form of a series. The multipole moment associated with a distant group can be *translated* into the coefficient of the local expansion associated with a local group (Figures 4.4 and 4.5). Interactions with particles which are nearby are handled directly.

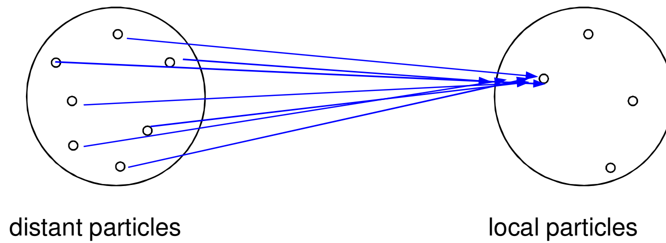

Figure 4.4. Conventional evaluation of contribution from distant particles: $O(N^2)$ algorithm (adopted from ref. [18]).

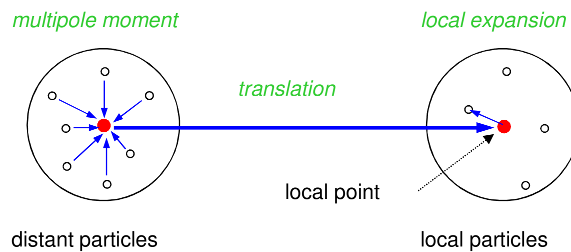

Figure 4.5. Evaluation with the multipole moment and the local expansion: $O(N)$ algorithm (adopted from ref. [18]).

In addition to Rokhlin's work, Greengard introduces a hierarchical decomposition of a data-space with a quad-tree in two dimensions and an oct-tree in three dimensions to carry out efficient and systematic grouping of particles with tree structures. The hierarchical decomposition is used to cluster particles at various spatial lengths and compute interactions with other clusters that are sufficiently far away by means of the series expansions.

For a given input configuration of particles, the sequential FMM first decomposes the data-space in a hierarchy of blocks and computes local

neighborhoods and *interaction-lists* involved in subsequent computations. Then, it performs two passes on the decomposition tree. The first pass starts at the leaves of the tree, computing *multipole expansion coefficients* for the Columbic field. It proceeds towards the root accumulating the multipole coefficients at intermediate tree-nodes. When the root is reached, the second pass starts. It moves towards the leaves of the tree, *exchanging* data between blocks belonging to the neighborhoods and interaction-lists calculated at tree-construction. At the end of the downward pass all long-range interactions have been computed. Subsequently, nearest-neighbor computations are performed directly to take into consideration interactions from nearby bodies. Finally, short- and long-range interactions are accumulated and the total forces exerted upon particles are computed. The algorithm repeats the above steps and simulates the evolution of the particle system for each successive time-step.

CHAPTER 5

Description of Analytical Models For Random Dopant Fluctuations (RDF) and Random Interface Trap Induced Threshold Voltage Fluctuations Assessment

3-D Ensemble Monte Carlo (EMC) based device simulation extracts the carrier dynamics and carrier transport characteristics under most bias conditions on the gate and drain contacts of a MOSFET device. However, the numerical simulation can result in prolonged time usage before reasonable extraction of device characteristics measurements can be performed on simulation data statistics. Analytical device physics based models can serve as efficient alternatives to above EMC simulation based scheme by estimating the fluctuations in threshold voltage and taking account of carrier transport features in the channel of a MOSFET under bias conditions. By formulation of analytically solvable equations set, analytical model based results can be compared with the threshold voltage and its fluctuation data extracted by EMC device based simulation procedure. Several analytical model based threshold voltage and its fluctuation characteristics computations have been proposed in the literature over the years till to date. In this dissertation, two widely used analytical models have been reviewed for their salient features [7-8], [9] in sub-sections 5.1 and 5.2 of this Chapter for estimation of random channel dopant and interface trap induced threshold voltage and its fluctuation. With the scaling of the MOSFET gate length, the impact of random dopant number variation in the channel coupled with

variations in the dopant placements leads to more severe spread of threshold voltage variation induced by a random interface trap interacting with carriers and dopant ions surrounding the trap. For extremely small geometry MOSFET devices, the analytical models propounded by [7-8] and [9] are not fully accurate, even at threshold conditions, in proper estimation of large threshold voltage deviations that result for trap's positioning closer to source at the channel interface. These large variations in threshold voltage in presence of source-side trap positions have been extracted from 3-D EMC based device simulations. In sight of these drawbacks of the above analytical models, a new analytical model has been proposed that combines the effects of dopant number fluctuation theory of [7] with the newly incorporated short range electron-electron and electron-ion-trap force induced effective surface mobility fluctuations. The feature of this new analytical model has been detailed in sub-section 5.3.

5.1 Dopant Number Fluctuation Based Analytical Model

To properly account for the random number and position of the dopant ions in the depletion region of the channel, the model presented in Ref. [7] accomplishes this in the following manner. The simulation domain is divided into small boxes by discretizing the channel length and width into small square cells of dimension l with a volume assisted by the depth of X that extends from the channel to ideally the maximum depletion width. The random dopant ions are positioned in each of these cell volumes in random number and assortment that is based on the uniform nominal doping density. Thus, the number of dopant ions that can reside in a volume cell is dependent on the dimensions of the cell (square

dimension l and depth dimension X). If this number is too small and close to unity, the calculated V_T will be too small and almost invariant from cell to cell. Therefore, the volume of the cell of dimension l and X are chosen in a way that for a certain random dopant configuration, a dopant number variation up to a maximum of 4 can be expected to reside in the cell. The required device parameters for the 45 nm physical gate length MOSFET are L (gate length) = 45 nm, W (gate width) = 50 nm, t_{ox} (oxide depth) = 0.9 nm and $N_A = 8.9\times10^{24}$ m^{-3}. It has been confirmed earlier that V_T variation for a typical channel random dopant correlates to a few nm depth from the interface [23]. With the above information, the designed cell dimensions are computed to be l = 10 nm and X = 4.5 nm with the maximum possible depletion depth W_{max} = 12.34 nm. The calculated threshold voltage V_T values using the expressions given in Ref. [7] are summarized in Table 1. After calculating the local cell threshold voltage from its dopant number value, all the threshold voltage values from all the cells in a 2D array have been averaged to extract the final form of threshold voltage for a particular random dopant configuration shown in Figure 5.1.

Table 5.1

The calculated threshold voltage values for dopant number distributions as arranged in the cell.

Number of atoms in the cell	Threshold Voltage (V)
0	0.0000
1	0.0218
2	0.1178
3	0.1919
4	0.2546

Calculation of Threshold Voltage

L \ W	0-10	10-20	20-30	30-40	40-50
7-17	2	4	4	3	4
17-27	3	0	4	2	4
27-37	3	4	4	4	4

Random Dopant Type 1

V_{th} = 0.2068 V

L \ W	0-10	10-20	20-30	30-40	40-50
7-17	2	4	4	2	4
17-27	4	3	3	4	3
27-37	4	4	4	4	3

Random Dopant Type 7

V_{th} = 0.2196 V

Figure 5.1. Cellular arrangement of random dopant ions shown for two random channel dopant configurations extracted from random dopant implant subroutine used in numerical EMC device simulation. The cell size is 10 nm spaced gate width (horizontal) direction and 10 nm spaced channel along source to drain (vertical) direction.

Once the reference V_T values for different random dopant type and distributions as arranged in the cells of the discretized channel region are extracted using the procedure described above, we have used the results from Ref. [8] to calculate the threshold voltage V_T fluctuation percentage for an interface trap positioned along the channel from source to drain of an effective 32 nm channel length nMOSFET. Since single interface traps are taken to be at locations that are 2 nm apart, the length l of the cell is now reduced to 2 nm while the width l' (different from square cell) is kept at 10 nm. This places a maximum of 2 atoms per cell for a particular trap to interact with. Since the random interface trap is located at the middle of the gate width, the trap will be positioned in the cellular array of width location bounded by 20-30 nm. A typical pictorial arrangement for random dopant ions as distributed and assorted in cellular array with a random

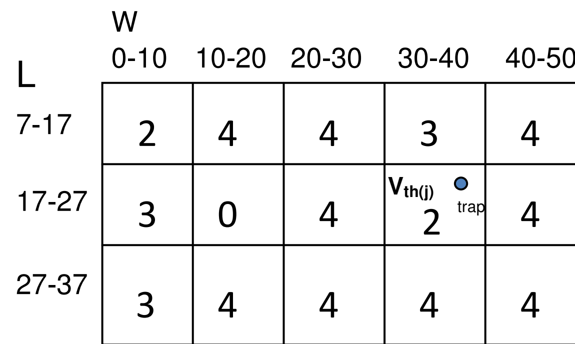

Figure 5.2. Cellular arrangement of random dopant ions and an interface trap located at a particular gate width (horizontal) and channel (vertical) direction positioned cell. (For this 2-D arrangement, V_{th} = 2068 V and V_{th}(j) = 0.1178 V).

interface trap is shown in Figure 5.2 where, for simplicity, the rather long arrangement of cells in the length direction for 2 nm case has been supplanted by previous 10 nm cell dimension in the channel length direction. In the original cellular arrangement where the trap is spaced 2 nm along the channel, first the trap's position in the jth location of the cell is determined from its channel direction position and gate width direction (which is always 20-30 nm cell in the *W* direction). Since the actual random dopant number present inside the jth cell can vary from 0-2, the corresponding $V_T(j)$ is computed as per equations given in the analytical model from Ref. [7]. Then for a particular trap, as described for a designated random dopant type using the equations detailed in the Ref. [8], threshold voltage difference ΔV_T is computed from knowledge of reference V_T and threshold voltage $V_T(j)$ when the trap is positioned at a particular channel site. Similar values are computed for all trap positions within the 32 nm channel length and for the set of 20 random dopant distributions. From ΔV_T values the fluctuation percentage relative to reference V_T value (Ref. [7]), for a particular random dopant type in presence of a particular interface trap position, is generated. Next, average over fluctuation percentage values is made over all random channel and bulk dopant distributions for a particular interface trap position along the channel from source to drain. The following equation sets are used for cell based V_T and ΔV_T calculations.

$$N_A = \frac{m}{l^2 X}. \tag{5.1}$$

$$\varphi_B = V_T \ln\left(\frac{N_A + \sqrt{N_A{}^2 + 4n_i{}^2}}{2n_i}\right). \tag{5.2}$$

$$\phi_f = V_T \ln\left(\frac{m}{2l^2 Xn_i} + \frac{1}{2}\sqrt{\left(\frac{m}{l^2 Xn_i}\right)^2 + 4}\right). \tag{5.3}$$

$$V_{ts} = V_{fb} + 2\varphi_B + \frac{1}{lC_{ox}}\sqrt{\frac{2q\varepsilon_s(\varphi_B + \phi_f(m))m}{X}}. \tag{5.4}$$

A short channel effect correction to V_{ts} of the above equation is invoked by the following equation (Ref. [24]),

$$\Delta V_t = \frac{24t_{ox}}{W_{dm}}\sqrt{\psi_{bi}(\psi_{bi} + V_{ds})}e^{-\frac{\pi L}{2(W_{dm}+3t_{ox})}}. \tag{5.5}$$

$$\Delta V_{th} = \left(\frac{q}{C_{ox}W_{eff}L_{eff}}\right)\exp\left(\frac{q}{nkT}(V_{th} - V_{th}(j))\right). \tag{5.6}$$

$$n = (C_{dep}/C_{ox}) + 1. \tag{5.7}$$

For the calculation of n in the equation (5.7) above, since the trap is lying very much close to the interface, therefore the vicinity of the trap's interaction zone is considered to be a few nm extending into the depletion region from the channel-oxide interface.

5.2 Percolation Theory Based Conduction Modulation Incorporated Analytical Model

As per Ref. [9] where R. W. Keyes observes that the randomness of the distribution of impurity atoms under the active gate area results in the average

doping in the depletion layer underneath the channel being spatially varying in the plane of the surface. The author of Ref. [9] further adopted a cube approximation introduced by Shockley [25] and proposed to divide the channel region of a MOSFET into cubes whose edge is equal to the thickness of the depletion layer. The probability distribution of the threshold voltages of the cubes can then be calculated by using the Poisson distribution of the impurity numbers. The conductivity of the array of cubes is treated by a modification of percolation theory. Ref. [9] is based on this finite percolation theory which is combined with the cube threshold (current conduction condition of the cube) probability distribution to yield the probability distribution of threshold voltages of a MOSFET in equilibrium. A transistor will be regarded as conductive if a path from source to drain through conductive elements exists. Figure 5.3 below shows examples of conductive and non-conductive transistors where the array size has been considerably small. The conductivity of such smaller arrays does not depend only on the fraction of conducting elements, but also on the disposition of the conductive elements within the array. The more the number of adjacent conducting cells that exists from source contact towards the drain, the more the conduction probability that a path for carriers exists from source to drain under the bias condition at threshold. From Figure 5.3, we can infer that even though case (a) cell configuration shows conductivity from source to drain due to the second cell array from the left side of the 2-D cell array, only 0.2 elements of this cellular arrangement are conductive. For Case (d) of Figure 5.3, 0.8 elements of the cellular arrangement are conductive. In this case, conduction probability that a

path exists from source to drain is low due to lesser number of adjacent cell numbers in all the 5 arrays that are “on” at threshold.

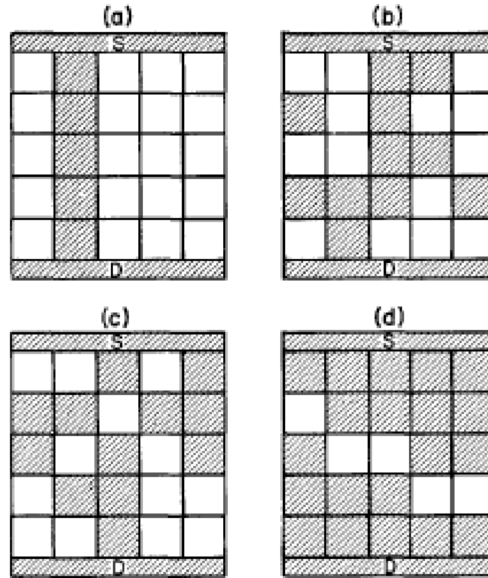

Figure 5.3. Examples of conducting [a and b] and non-conducting [c and d] arrays (Adopted from Ref. [9]).

The governing equations used in the analytical model of [9] are shown in order below:

$$P(m) = \frac{M^m e^{-M}}{m!}. \tag{5.8}$$

In the above equation, M denotes the average number of dopants in a cell and m is the actual dopant number in a cell.

Assuming p denotes the probability that a particular cell is ‘turned-on’,

$$p = \sum_{m=0}^{m_c} P(m). \tag{5.9}$$

The probability that L of the K regions into which the surface of the channel of the FET is divided are conductive is related to p by,

$$Y_K(L) = \frac{K!\, p^L (1-p)^{K-L}}{L!(K-L)!}. \tag{5.10}$$

The probability that L conductive elements possess a conductive path from source to drain,

$$Z_K(L) = \varphi\left(\frac{\left[\left(\frac{L}{K}\right) - \eta\right]}{\xi}\right). \tag{5.11}$$

Where φ(y) is the probability integral

$$\varphi(y) = (2\pi)^{-1/2} \int_0^y \exp\left(-t^2/2\right) dt. \tag{5.12}$$

The parameters ξ and η have the following values

$$\eta = 0.59 \qquad \xi = 0.149 \exp\left(-0.0636 K^{1/2}\right). \tag{5.13}$$

At threshold, we can determine the probability that a conductive path from source to drain exists,

$$Q = \sum_{L=0}^{L=K} Y_K(L) Z_K(L). \tag{5.14}$$

The equations (5.8)-(5.14) are used to calculate conduction probability Q for all 20 random dopants with K being the total number of elemental cell regions connecting source and drain and has a value of 15. The L value is determined for a particular cell array from source to drain based on the elemental cell's conductivity. The average number of dopant in a cell is M=1 and the dopant number at which a cell becomes non-conducting is m_c = 2. The connection

between Q and applied gate voltage can be established by the following set of equations

$$\frac{dQ}{dV} = \frac{dQ}{dS}\frac{dS}{dV}. \tag{5.15}$$

Here S is the charge per unit area of semiconductor surface in the depletion layer.

$$\frac{dS}{dV} = C_{ox}. \tag{5.16}$$

C_{ox} is the oxide capacitance per unit area.

$$\frac{dQ}{dS} = (\pi\sigma)^{-1} K^{3/8} \exp\left\{-\pi^{-1} K^{3/4} \left[(\Delta S/\sigma) - b\right]^2\right\} \tag{5.17}$$

$$b = (2\pi)^{1/2}(\eta - 0.5) \quad \Delta S = \frac{(m_c - M)q}{2X^2} \quad \sigma = \left(\frac{N_A}{X}\right)^{1/2} q/2. \tag{5.18}$$

Here X is depletion width and other symbols have their usual meanings.

Using equation (5.15), dQ is actually the difference between the Q values calculated from equation (5.14) for each random dopant configuration based cellular array before the addition of the trap and after the addition of the trap. The trap is designed to impact the carriers in its vicinity in the form shown in Figure 5.4 with the hatched cell marks. After calculating dV, from equation (5.15), the actual threshold voltage in presence of trap along the source to drain in the middle of the gate width is computed from knowing the gate voltage at threshold before the trap is introduced. This reference V_T value for a particular random dopant configuration has been previously calculated using the number fluctuation based analytical model (Ref. [7]).

The percolation model enabled threshold voltage values in presence of random dopants and random interface traps does not deviate more than 3 % from number fluctuation based threshold voltage values. This is due to the fact that there is a long array of cells (15 cells in total) from source to drain of a MOSFET and the value of M and m_c are also very small. So Q is very small (~10^{-4} to 10^{-5} range) and does not deviate appreciably as a result of trap's introduction and interaction with spatially inhomogeneous channel dopants and inversion carriers.

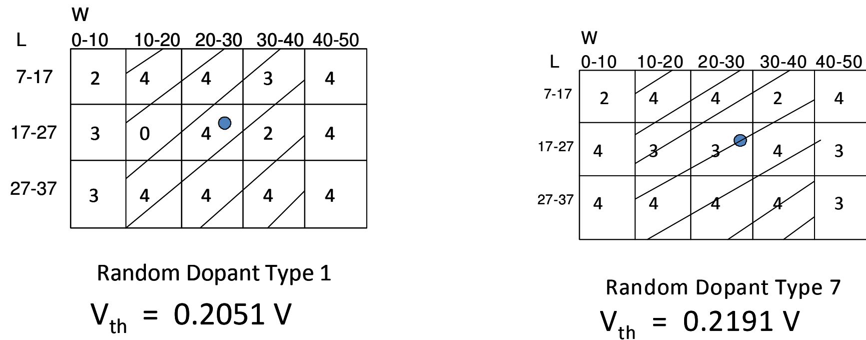

Figure 5.4. Calculation of threshold voltage shown in presence of an interface trap in the middle of the gate width for two different random dopant configurations. The hatched cells designate the trap's interaction zone.

5.3 Proposed Mobility Fluctuation Based Analytical Model With Inherent Number Fluctuation From Channel Dopants

The models discussed in sub-sections 5.1 and 5.2 of Chapter 5 are inadequate in proper replication of short range force interactions between a source side trap and neighboring channel dopants and inversion carrier electrons. From the knowledge of carrier mobility fluctuations resulting from surface potential barrier spikes at source side traps interactions with carriers and depletion ions, we

propose herein a new analytical model. The new model properly incorporates the low field (threshold condition) channel mobility fluctuations in presence of random dopants and random interface traps. The model has added versatility that the fluctuations due to random dopant ions in the depletion region are inherent in the calculation of V_T and its fluctuation.

The governing equations are taken from Ref. [26-27]. The key equation (5.19) that extracts the mobility values is referenced below:

$$\mu_{eff} = \frac{g_{ds} L}{W Q_n}. \qquad (5.19)$$

In this expression, g_{ds} is drain-to-source output conductance, Q_n is inversion charge density to a few nm depth at the interface, L is channel length and W is channel width.

As a first step, Q_n value is gathered by EMC simulation run for all 20 random dopants. Then in next step, from the MOSFET's I-V_{ds} characteristics for a fixed V_{gs}, g_{ds} value is extracted from the linear region of the drain current–drain voltage characteristics. A reasonable estimate of mobility variation is assumed to be within 80-120 cm^2/V-s for 45 nm channel length MOSFET at a doping concentration reaching 10^{19} cm^{-3}. To maintain linear region of operation, gate bias is maintained at V_{gs} value of 0.8 V and drain bias is swept in 0.02 V increments from 0.25 V to 0.45 V to gather the I_{ds}-V_{ds} characteristics from EMC simulation. Using the methodology explained above, g_{ds} is then extracted from this set of I_{ds}-V_{ds} characteristics. Q_n is measured at V_{ds} = 0.4 V and V_{gs} = 0.8 V. In step 3, the above policy is used for every position of the interface trap in the channel for a

specific random dopant type to extract effective channel mobility. In order to calculate the threshold voltage with effective mobility of carriers incorporated in the analytical model, a set of equations are used from Ref. [27] and are enumerated below:

$$\varphi_{inv} = \left(\frac{kT}{q}\right)\ln\left(\frac{N_{inv}}{n_i}\right). \tag{5.20}$$

$$\varphi_B = \left(\frac{kT}{q}\right)\ln\left(\frac{N_A}{n_i}\right). \tag{5.21}$$

$$\varphi_s = \varphi_{inv} + \varphi_B. \tag{5.22}$$

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C_{ox}}. \tag{5.23}$$

$$A_b = 1 + \zeta\frac{\gamma}{2\sqrt{\varphi_s - V_{bs}}}. \tag{5.24}$$

$$g_{ds} = \mu_{eff}C_{ox}\frac{W}{L}\left(V_{gs} - V_T - \frac{A_bV_{ds}}{2}\right). \tag{5.25}$$

From equation (5.20), surface inverted electron concentration extracted from EMC simulation run is used to compute surface potential φ_{inv} and equation (5.21) is used to arrive at final form of equation (5.22) to compute total band bending at the interface. Equation (5.24) is the bulk-charge factor adopted from Ref. [22] in which ζ is a fitting parameter. The value of ζ is found to be 6.1889 using the reference V_T value in equation (5.25) for random dopant configuration 1 before trap is introduced. Equation (5.25) is the crucial analytical expression where V_T is related to g_{ds} and μ_{eff}. The fitting parameter ζ value 6.1889 is used as a reference

in all successive V_T derivations for a set of random dopant configuration. The above process is repeated for all remaining random dopant types to extract the reference V_T values. Then for each interface trap position, corresponding V_T value is computed and V_T fluctuation is determined for each trap position for a reference random dopant type. The V_{ds} term in equation (5.25) is fixed at 0. 4 V to reduce DIBL effect and excessive drain induced charge sharing to roll off V_T further.

CHAPTER 6

Simulation Results Conducted on Threshold Voltage Extraction and Its Fluctuation Induced by Interface Traps

In this Chapter, we discuss the simulation results from the 3-D ensemble Monte Carlo (EMC) based device simulations to extract threshold voltage for different random dopant configurations and subsequently its fluctuations in the presence of a single charged trap and double charged traps within 1 nm apart at the semiconductor-oxide interface. Since accurate analytical model development to properly correlate with numerical EMC device simulation scheme is vital for understanding key effects on threshold voltage reliability concerns, we report results of threshold voltage and its fluctuations, in presence of a single trap, deduced from the existing analytical models [7-8], [9] and also the newly proposed model discussed in the previous Chapter. The importance of taking into account of short range electron-electron and electron-ion-trap force interaction as presently incorporated in the EMC device simulation method is also demonstrated by simulation plots. With aggressive device scaling, halo doping pocket implantation at the source and drain of a MOSFET plays a beneficial role in combating short channel effects such as V_T roll-off with reduction of channel length. New simulation results are presented in this Chapter with regard to assessment of threshold voltage fluctuations for the cases of smaller and larger halo-pocket based MOSFET device with a single interface trap positioned between source and drain. From these simulation results, important conclusions

can be inferred on whether halo doping based device engineering is favorably suited to maintain trap-induced threshold voltage fluctuations within a certain tolerable limit.

6.1 Simulation Results For The Case of A Single Charged Trap By Using EMC Device Simulation Method

The simulator, described in Chapter 4, has been used in the investigation of the random trap fluctuations in 45 nm technology node MOSFET device. In this case, in addition to the randomness of the position and the actual number of the impurity atoms, a random trap is introduced in the middle section of the channel and moved from the source to the drain of the channel. The effective channel length of 45 nm technology node is taken to be 32 nm. We consider ensemble of 20 devices with different random dopant distribution. The threshold voltage of each of these devices without the presence of the trap is shown in Figure 6.1.

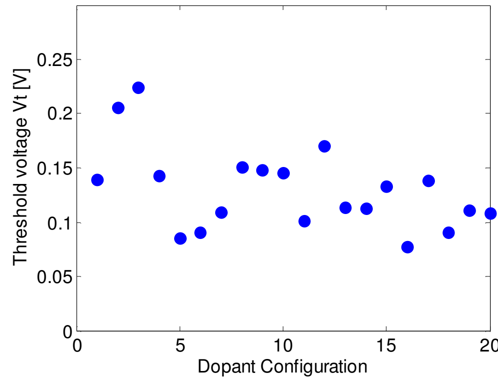

Figure 6.1. Threshold voltage fluctuations due to random dopant fluctuations (without traps) for a statistical ensemble of 20 devices with different number and different distribution of the impurity atoms.

The threshold voltages for all the different random dopant distributions were calculated as follows. First, a reference current value was computed from the drain current-gate voltage data statistics in the vicinity of low to moderate gate voltages at a low fixed drain bias voltage for a particular reference random dopant type. The gate voltage (distinctive for a particular random dopant type) at this fixed reference current value has been attributed to be the threshold voltage for the different random dopant type distributions. The slope adjustment method at a drain current value in the vicinity of the reference drain current value has been used to extract these threshold voltages. With addition of traps, the above method is applied for extracting threshold voltages (the gate voltage at the fixed calculated reference drain current with respect to the reference random dopant type (no trap case) as clarified above).

The total variation of the threshold voltage as a function of the trap position in the middle portion of the channel, when the single trap is moved from the source end to the drain end of the channel, is shown in Figure 6.2. We see that the threshold voltage increases from its average value when this trap is located at the source end of the channel. This is due to the fact that carriers see additional large potential barrier due to the presence of the charged trap and are reflected back in the source contact. The threshold voltage rapidly reduces when the trap is moved away from the source injection barrier because when the electrons are injected in the channel, although the electric field is small (due to small drain bias applied when measuring threshold voltage), they slowly drift towards the drain contact. The statistical sample of 20 dopant distributions is sufficient to give accu-

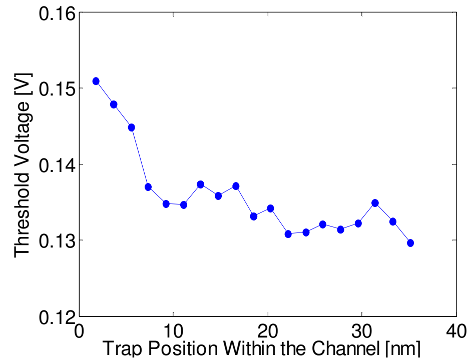

Figure 6.2. Threshold voltage variation for single trap's position (averaged over twenty random dopants per trap position) along the channel. In the X-axis, x = 0 denotes the source end of the channel.

-rate values on the percentage threshold voltage variation due to additional trap in the channel.

In Figure 6.3, we depict the threshold voltage fluctuation taken as a percentage relative to the values in Figure 6.1 as a function of the trap position when the trap is being moved from the middle of the source end of the channel to the middle of the drain end of the channel.

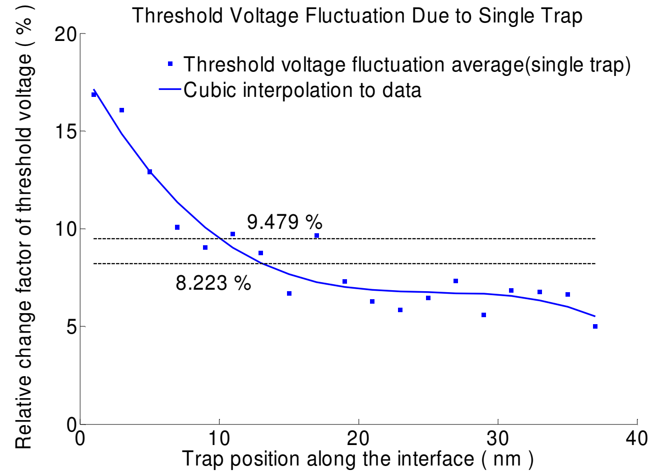

Figure 6.3. Threshold voltage fluctuation due to single trap's position along the channel (averaged over twenty random dopants per trap position). x=0 denotes source end of the channel.

An explanation of the results given in Figure 6.3 is schematically shown in Figure 6.4. At threshold voltage, the sheet electron density in the channel is small, therefore screening is not important. Traps near the source end of the channel have the largest influence since they are major obstacles to the electrons because of the large input barrier depicted in case (a) shown on the left panel of Figure 6.4. Traps near the drain end of the channel have smaller influence since electrons are accelerated by the small electric field – case (b) shown on the right panel of Figure 6.4.

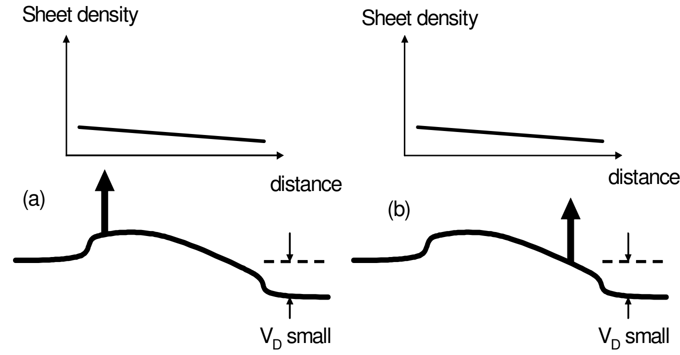

Figure 6.4: Schematic explanations of the results presented in Figure 6.3.

The threshold voltage standard deviation, averaged out for all 20 different random dopants analyzed as a function of trap position is shown in Figure 6.5. The simulation result confirms that when a significant number of dopant distributions is used as a parameter in the EMC simulation, the standard deviation fluctuation is well controlled and strongly coherent over different trap positions.

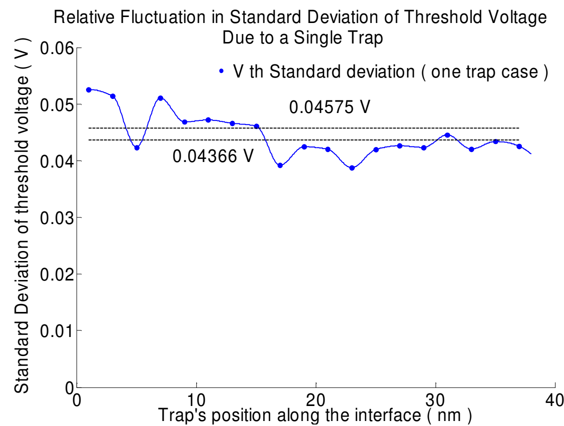

Figure 6.5. Extracted threshold voltage standard deviation as a function of trap position averaged over 20 random channel dopants (x=0 is source end of the channel).

6.2 Simulation Results For The Case of Two Charged Traps By Using EMC Device Simulation Method

As the number of traps is increased at the Si/SiO_2 interface, one parameter that aggravates the fluctuation values for threshold voltage (Figure 6.6) with its standard deviation (Figure 6.7), is the spacing between the traps. For this purpose, EMC device simulation is performed for enhancing the trap number from single to double but keeping the traps within 1 nm separation from one another. The plots on Figure 6.6 and Figure 6.7 underscore a very important feature of closely lying traps, i.e., adjacent traps alter the short range and long range Coulomb potential to the extent that some of the carriers when trapped at the source side, cannot surmount the steep potential barrier, due to the two adjacent traps' interactions, resulting in more degradation of device parameters such as threshold voltage compared to single trap environment.

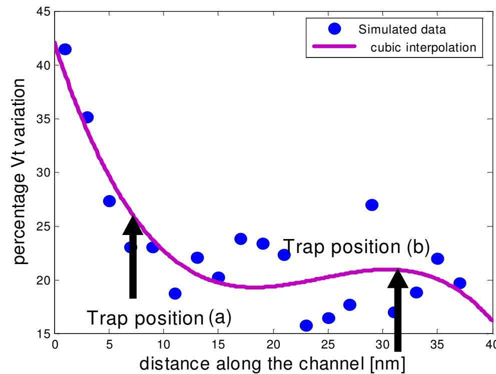

Figure 6.6. Percentage threshold voltage due to two traps located at the semiconductor/oxide interface and different positions along the middle section of the channel. 20 devices with different random dopant distributions have been averaged out. x=0 denotes source end of the channel.

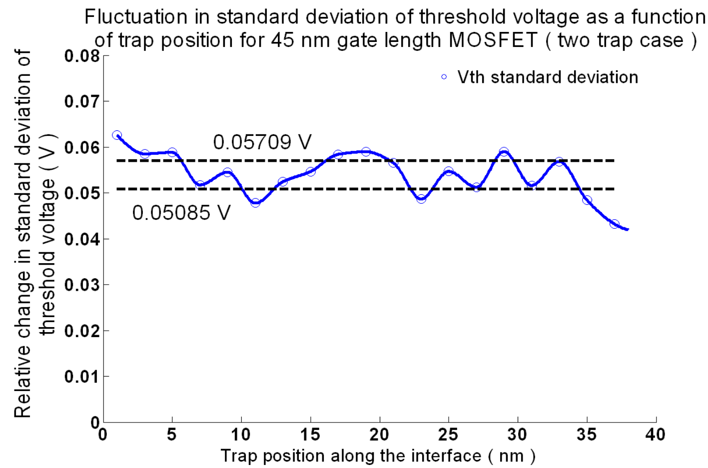

Figure 6.7. Threshold voltage standard deviation as a function of two traps' positions showing well behaved spatial correlation when sufficient number of random dopants are considered. x=0 denotes the source end of the channel.

6.3 Analytical Model Based Computations of V_T And Its Fluctuations in Presence of a Single Interface Trap for 45 nm n-MOSFET

In this subsection, we first present the results of extraction of V_T for different random dopant configurations and its fluctuations induced by a single interface trap. Figure 6.8 depicts the extracted threshold voltage distribution for different random dopant configurations taking account of the two existing analytical model based computations and EMC device simulation. Figure 6.9 shows the fluctuations in threshold voltage for different interface trap positions from source to drain of an effective 32 nm gate length MOSFET. The fluctuation trend of threshold voltage shown in this figure, for analytical model based derivations, is compared with 3-D EMC device simulation. The variation of the threshold

voltage as a function of random dopant configuration, for a trap which is placed in the center region of the channel, is shown in the plot of Figure 6.8 when the two analytical models and the EMC simulation scheme are used. From the figure, we see that consistent results of the threshold voltage distribution are reproduced by all three models. For the case of EMC simulation method, a constant drain bias of 0.5 V is used for all threshold voltage extractions in presence of interface random trap. Figure 6.9 illustrates the threshold voltage fluctuation extracted from analytical model [7-8], adjusted for trap's interactions with channel electrons inverted at threshold conditions, and also for EMC device simulation where usual short range interactions between trap to electron-electron and trap-electron-ion are accounted for. Deviation in V_T fluctuation values are noticed for EMC simulation model in comparison with analytical model due to the requirements of proper treatment of surface potential, mobility and inversion electron and dopant number fluctuations through 3D short range Coulomb force corrections. The analytical models thus exhibit inconsistencies in accurately replicating transport mechanism existing in the vicinity of a nearby trap in presence of random dopant ions and inversion electrons. Traps near the source end of the channel have the largest influence since they are major obstacles to the electrons because of the large input barrier experienced there. As the traps are positioned near the drain, due to the larger drift velocity and carrier excitation energy, trap's interaction with channel carriers is minimal and fluctuation deviation trend is more or less within a tolerance limit.

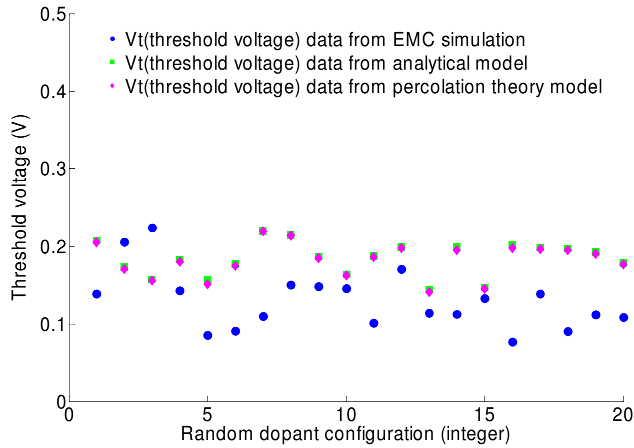

Figure 6.8. Threshold voltage as a function of different discrete random dopant configuration in the channel region when no interface random trap is present.

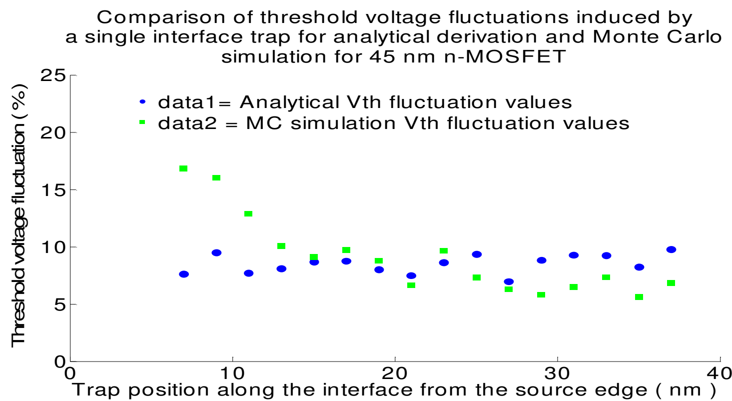

Figure 6.9. Threshold voltage fluctuations computed by the additional analytical model adjusted for random interface trap's interactions with channel electrons and EMC simulation method.

Figure 6.10 shows the expected deviations from mean values (errorbar) for threshold voltage fluctuation percentage observed in presence of a single interface trap positioned from source to drain for the cases of (i) EMC based device

simulation model, (ii) analytical number fluctuation based model and (iii) EMC based simulation method with no short range e-e and e-ion-trap interaction force. Figure 6.11 shows the importance of consideration of short range electro-electron and electron-ion-trap interaction force for proper estimation of large fluctuation values of threshold voltage in presence of source-side trap positions. These results highlight the importance of short range electron-electron and electron-ion-trap Coulomb interaction correction to the conventional particle-mesh coupling (PM) long range Coulomb interactions. In addition, it is evident that traps near the source end of the channel can cause significant mobility fluctuations apart from surface potential fluctuations impeding the electron flow and enhancing the local threshold voltage variations. Any trap positioned near the source junction will trap the carriers for a long time and create a repulsive Coulomb blockade well surrounding the trap. The electron thus trapped has lesser energy to surmount this well and depending on their number variation, trapped electron with less drift velocity will also have less energy as the natural progression from source side to drain side has been impeded by trap's presence at the source side. So, a significant mobility fluctuation will be added to carrier number fluctuation for carrier electrons trapped near the source side by a random interface trap. The figure also demonstrates that as the traps are moved away from the source towards the drain end of the channel, fluctuation pattern is within a few percentage tolerances between the analytical model and EMC device simulation model.

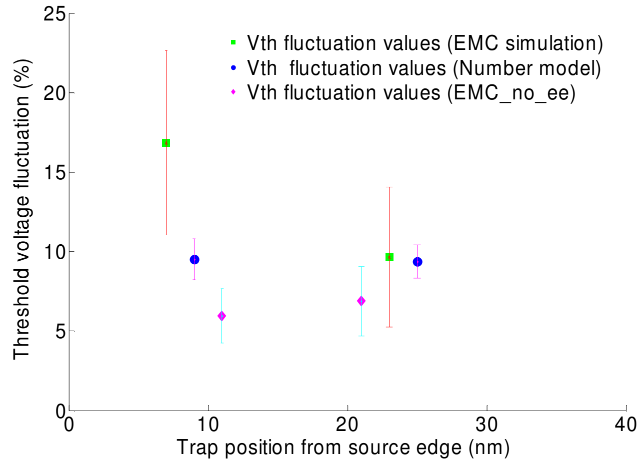

Figure 6.10. The errorbar plot of threshold voltage fluctuation percentage for interface trap positions near source and away from source along the channel for the cases of (i) EMC simulation method, (ii) analytical model 1 and (iii) EMC simulation method with no short range e-e and e-ion-trap force consideration.

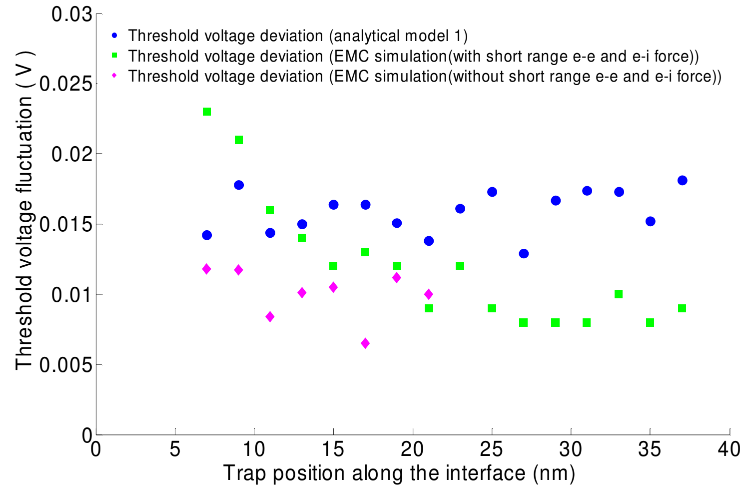

Figure 6.11. Threshold voltage fluctuation as a function of trap position at the interface in the channel region of the MOSFET for the first of the two analytical models and EMC simulation models with and without short range Coulomb force corrections.

6.3.1 V_T Extraction and Its Fluctuations Assessment By The Newly Proposed Mobility Fluctuations Based Model

The newly proposed mobility fluctuation based analytical model with its inherent incorporation of dopant number fluctuation in the channel underneath the depletion region addresses the deficiency shown in Figure 6.11 above for the cases of analytical models reported in [7-8], [9]. Figure 6.12 shows the statistical set of reference effective channel mobility values for the different designated types and distributions of random dopants in the channel and bulk region. Figure 6.13 shows the percentage average mobility fluctuations over a set of 20 random dopant types for the case of a single interface trap when the trap is moved from source junction edge to the drain junction edge of the MOSFET. The variation

and scatter in mobility values are due to spatially inhomogeneous channel thickness, dopant number variations (position and number in close proximity to a carrier electron) and short range spatial electron-electron and electron-trap-ion interactions. Figure 6.14 shows the threshold voltage values for the random dopant types considered for all three analytical models and EMC device simulation environment. Figure 6.15 shows the percentage threshold voltage fluctuations for analytical model 1 based on dopant number fluctuations in the channel [7-8], EMC device simulation method and new analytical model 3 (newly proposed) comprising of added channel mobility fluctuations to dopant number fluctuations, respectively. The figure clearly reveals that model 3 (newly proposed) is more compliant to accurate EMC device simulation based threshold voltage fluctuations in the vicinity of the source of an effective 32 nm channel length MOSFET. From the fluctuation trend of V_T extracted as a function of trap position for the case of channel effective mobility fluctuation exclusively, it can be concluded that the dopant number fluctuations and mobility fluctuations effects cannot be considered as additive to give rise to actual V_T fluctuation values predicted by new analytical model. Figure 6.16 shows the error bar plot of extracted threshold voltage values for different random dopant configuration types for the cases of (i) EMC simulation method, (ii) analytical model 1 and (iii) new mobility fluctuation based model 3. Figure 6.17 furthers depicts the error bar plot for threshold voltage fluctuation percentage values in presence of interface traps (source side, middle and near drain) for all the above cases.

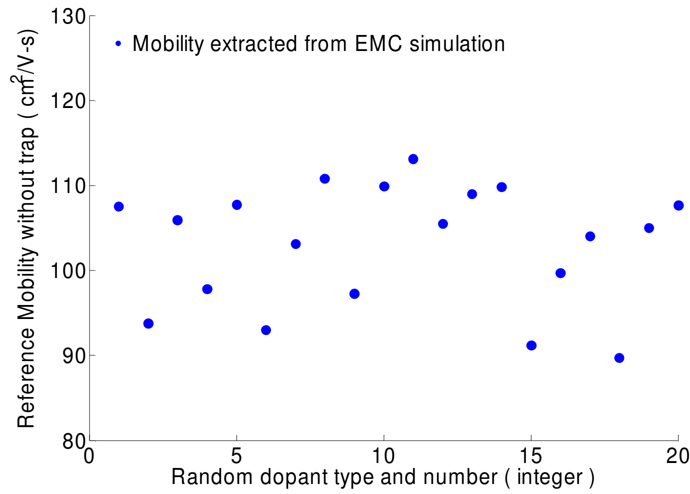

Figure 6.12. Effective channel mobility values for different statistical set of random dopants.

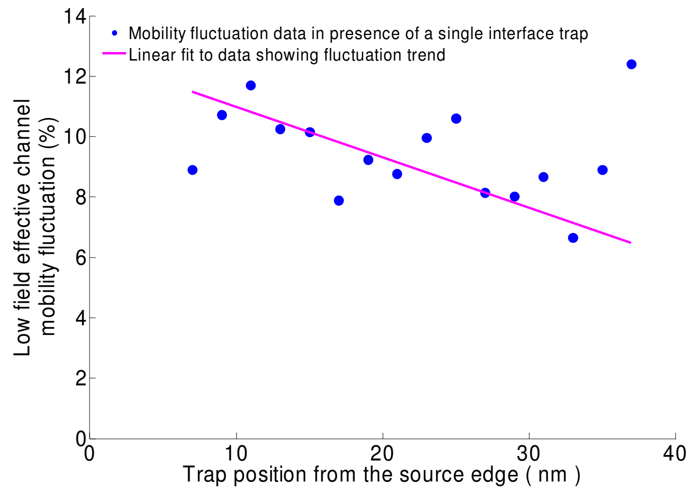

Figure 6.13. Effective channel mobility fluctuation as a function of trap position at the interface between source and drain junctions in the channel of the MOSFET.

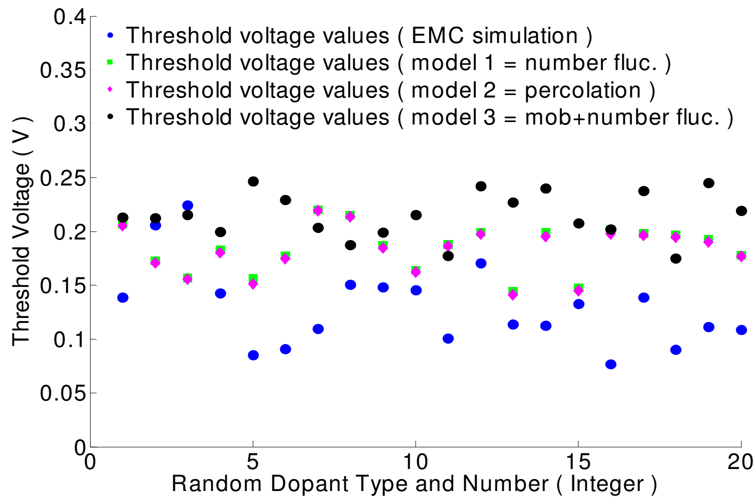

Figure 6.14. Threshold voltage values extracted for the two existing models in the literature along with the new analytical model and EMC device simulation for a statistical set of random dopant types designated as integer numbers.

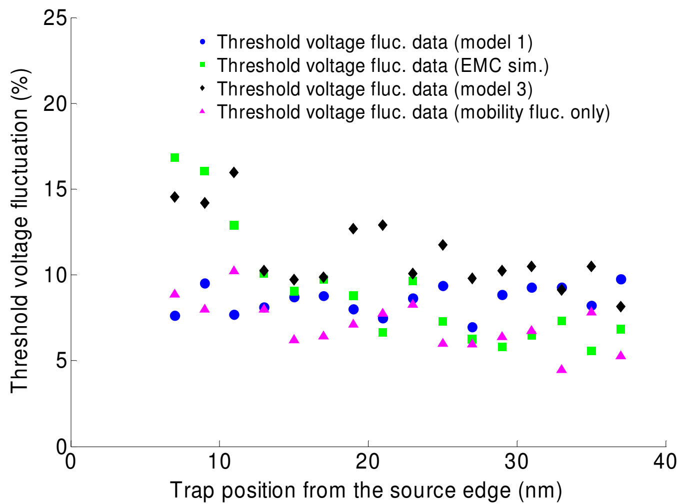

Figure 6.15. Percentage averaged threshold voltage fluctuation values extracted for the two existing models in the literature along with new analytical model and EMC device simulation method for a single random interface trap positioned in the channel from source to drain of the MOSFET.

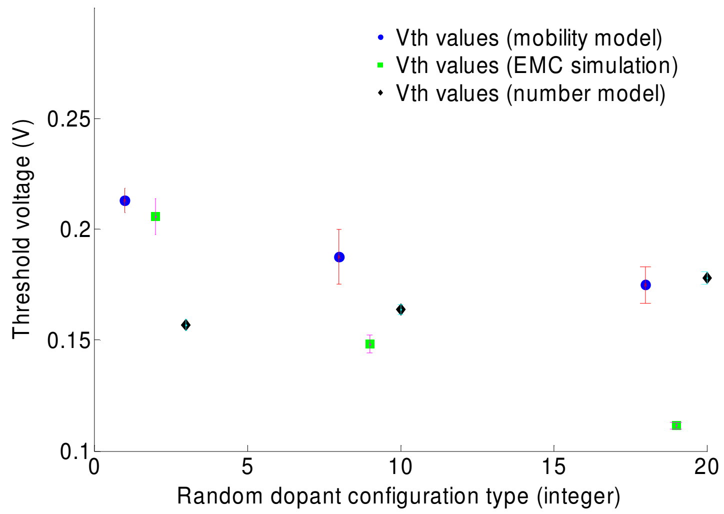

Figure 6.16. Threshold voltage distribution with their expected deviations for different random dopant configuration types when trap's effect is considered.

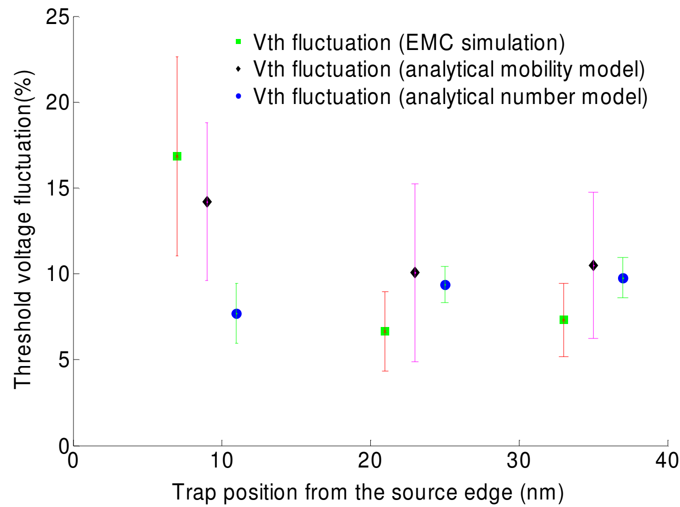

Figure 6.17. Threshold voltage fluctuation error bar plot considering different trap positions for the (i) EMC simulation method, (ii) analytical mobility fluctuation based model and (iii) analytical number fluctuation based model.

6.3.2 V_T Extraction and Its Fluctuations Assessment Using 3-D EMC Device Simulation Scheme For Conventional and Halo Pocket Implanted 45 nm MOSFET

Halo doping near the source and drain of a scaled MOSFET has been implemented as a potential device engineering method to improve the short channel effects of a MOSFET, i.e., improving the threshold voltage roll-off by reverse short channel effect. Since halo doped MOSFET has been adopted in the industry for a considerable period till now, studying the interface trap induced threshold voltage shifts that can be computed and subsequently verified by the available reliability failure window are of utmost importance. With this insight, we investigate and report threshold voltage(V_T) values for a set of twenty random channel and bulk dopant configurations and fluctuation percentage of V_T induced by an interface trap (as the trap is moved from source to drain in the active channel region at the interface) for the cases of conventional, smaller source and drain halo pocket implants and larger source and drain halo pocket implants by numerical simulation employing 3D Ensemble Monte Carlo (EMC) based device simulation.

Figure 6.18 shows the threshold voltage values for (i) conventional, (ii) smaller halo doped and (iii) larger halo doped MOSFET extracted for 20 set of random dopant configurations which are Poisson distributed from a mean average bulk dopant density and implanted in the channel and bulk of the scaled 45 nm device by a random dopant subroutine configured as a part of EMC device simulations. The smaller halo pocket size is 5.5 nm and the larger halo pocket size

is 11 nm and the same 20 set of random dopant profiles, drawn from a 1.1 × channel dopant density, are used inside the pocket volume. The reverse short channel effect on V_T is clearly visible for both smaller and larger halo doped MOSFET in comparison to conventional MOSFET. The plot in Figure 6.19 shows the threshold voltage fluctuation percentage as observed for a single interface trap position along the channel from the source to drain for the cases of (i), (ii) and (iii) as stated above. Due to higher average halo doping density as compared to the channel, the potential barrier near the source of the trap is higher for both the halo doped MOSFET cases than their conventional counterpart. In addition, for the case of device with the larger pocket length near the source, considerable fluctuations in threshold voltage exist for a few trap positions when compared to both smaller halo doped and conventional MOSFET devices. For trap positions near the drain of the MOSFET, larger halo doped MOSFET exhibits more fluctuation in threshold voltage due to formation of early potential barrier induced by trap positions inside the extended halo pocket length from the drain edge. The shorter halo doped MOSFET benefits from lower V_T fluctuations (for trap positions near the drain) arising from inversion pinch-off region extending deeper towards the drain. For the traps located in the channel, the fluctuations vary for all the three device types within a certain tolerance level. The distribution of depletion ions in the channel volume along with carriers-trap-ions short range force impacted drift velocity and mobility variations will play a crucial role for trap's interaction zone in the channel. Due to varied length of source side barrier induced by source side trap positions for shorter and larger

halo pocket respectively, the emerging drift velocity just at the edge of inception of channel will be largely different for these two device types and also for conventional MOSFET. From these simulation results, it is evident that halo doping near the source aggravates the reliability concerns for threshold voltage fluctuations when compared to conventional MOSFET for source side trap positions. For reliability projections of threshold voltage variations with regard to drain side trap positions, an optimal pocket size needs to be devised that is of the order of shorter halo pocket dimension presented in this simulation study. Figure 6.20 shows the error bar plot for threshold voltage distribution for different random dopant configuration types for the two halo pocket implanted MOSFET devices and conventional 45 nm MOSFET device. Figure 6.21 shows the error bar plot of the threshold voltage fluctuation percentage for the above case.

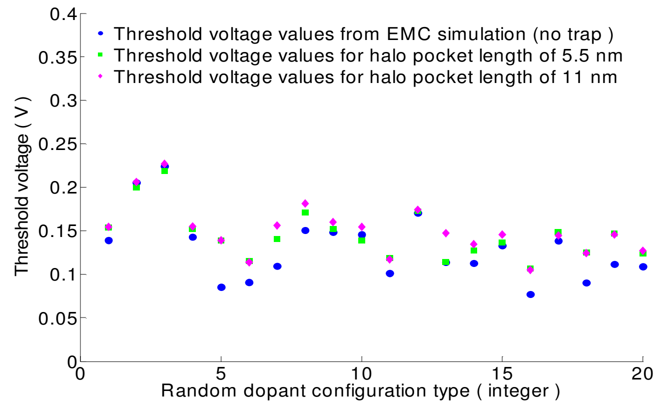

Figure 6.18. Threshold voltage values for a set of 20 random dopant configurations for the conventional, shorter and larger halo doped 45 nm MOSFET.

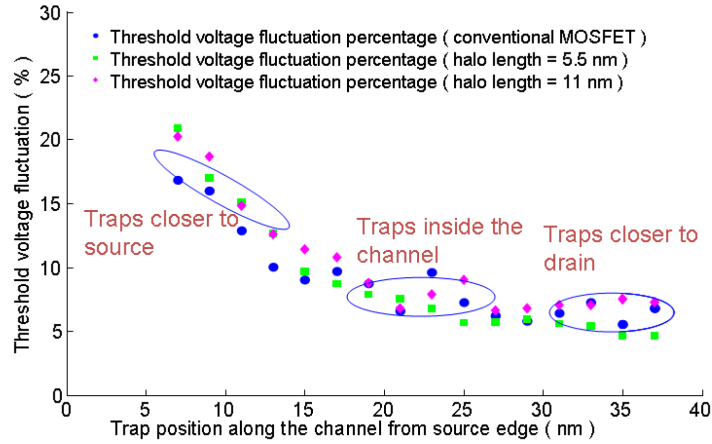

Figure 6.19. Threshold voltage fluctuation percentage values induced by an interface trap positioned from source to drain for the cases of conventional, shorter and larger halo doped 45 nm MOSFET.

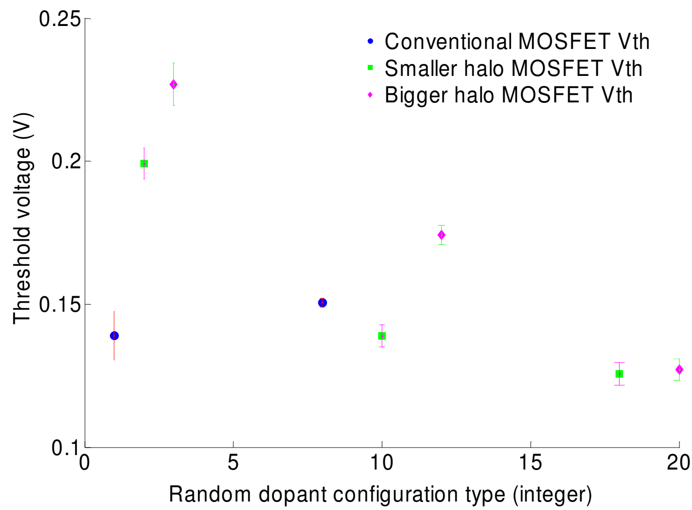

Figure 6.20. Threshold voltage distribution with their expected deviation induced by trap for different random dopant configuration types for the cases of conventional and two halo pocket implanted MOSFET devices.

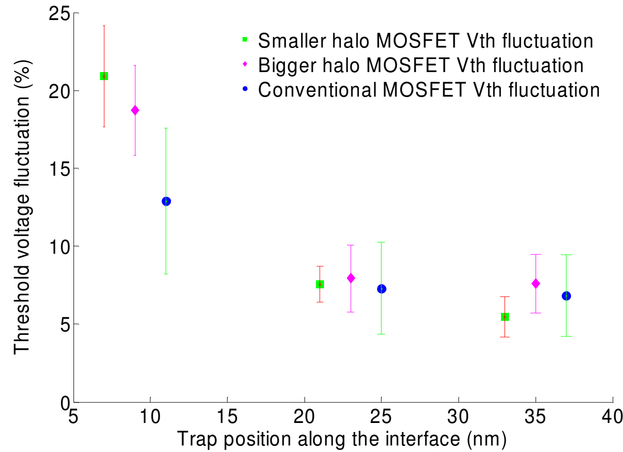

Figure 6.21. Threshold voltage fluctuation percentage with their expected deviation as recorded for different trap positions along the channel for three MOSFET device types.

6.4 Simulation Results from 3-D Ensemble Monte Carlo Based Device Simulation On Drive Current (saturation) Fluctuations Induced By a Single And Double Interface Traps In The Channel Of a 45 nm MOSFET

Apart from threshold voltage fluctuation that has been studied as a reliability failure metric in the digital and analog high-density VLSI circuits, potential barrier on reliable performance arises from on-drive current fluctuations of MOSFET devices which operate in the saturation region. In digital circuits the fluctuation in the ON-current can affect the speed of the circuit and cause delay in signal transmission in different parts of the circuit assembly and predominately affects signal integrity features such as signal glitches and skews. Since assessing the percentage fluctuations in ON-current in presence of random interface traps in the channel region from source to drain is of significant importance, we have

conducted EMC based device simulation for estimating drive current fluctuation percentage when there is a single and two traps at 1nm apart are present in the interface in the channel region of an effective 32 nm gate length MOSFET. Figure 6.22 shows the ON-current degradation as a function of the trap position when a single trap entity is considered. The on-current in our simulation is defined to be the drain current value when the device is in saturation. The saturation condition is taken to be at a gate bias of 0.8 V and drain bias of 0.7 V. As depicted on the figure, near the source end of the channel the current degradation due to the presence of a negatively charged trap is large because the trap introduces additional barrier for the current flow. When the trap is in the middle section of the channel the current degradation is smaller. Traps near the drain contact, whe-

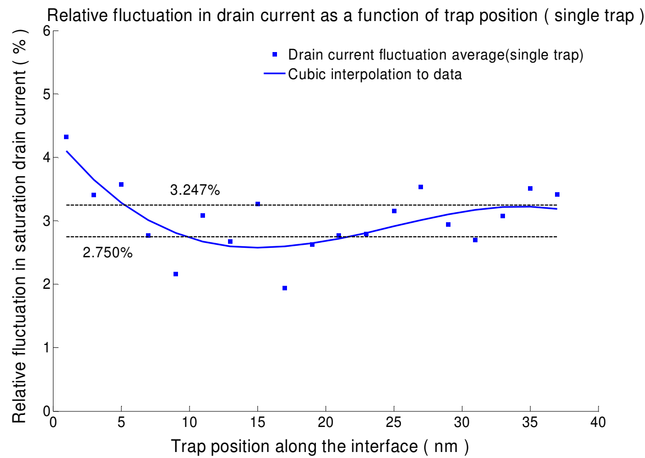

Figure 6.22. ON-current fluctuation as effected by variation of single trap position (20 random dopant cases have been averaged per trap position) along the channel from source end (x=0) to drain end.

-re the electron density is pinched off for the bias conditions used, are not effectively screened and a notable increase of the current degradation is observed.

ON-current fluctuations underscore a very important feature of closely lying traps for the case of double traps. Adjacent traps alter the short range and long range Coulomb potential to the extent that some of the carriers when trapped at the source location, cannot surmount the steep potential barrier due to closely spaced trap's interactions resulting in more degradation of device parameters, in this case, drain current compared to single trap environment. Figure 6.23 shows the ON-current fluctuation percentage as observed for the cases of double traps lying at the channel interface and are 1nm apart.

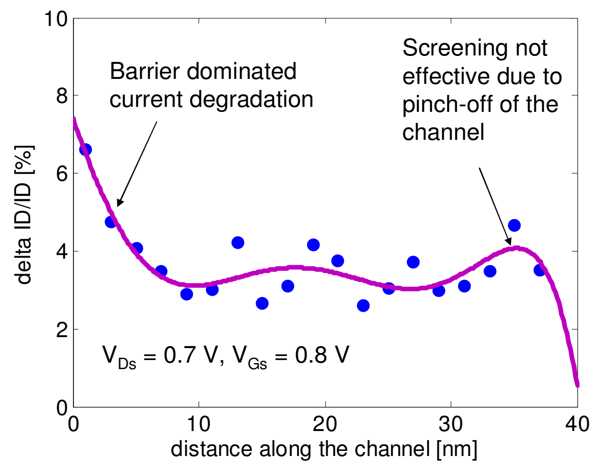

Figure 6.23. ON-current degradation as a function of two traps' positions. The statistical ensemble used here consists of first seven random dopant distributions in both number and positions within the active region of the channel. x=0 denotes source end of the channel.

CHAPTER 7

CONCLUSIONS

Random telegraph noise or signal (RTN/RTS) based device reliability study is emerging to be ever more important from the perspective of device scaling. With each generation of device scaling, the concepts of uniform channel sheet density and uniform bulk doping density are deemed inappropriate and only discrete positions and numbers of both channel and substrate doping densities result in a statistical way. Moreover, the random position and number of the traps are found to be totally uncorrelated with the random channel and bulk dopants. As a result of this, reliable projection of tolerable drain current (saturation) and threshold voltage degradation, two important device performance metrics for today's high-density digital and analog integrated circuits are becoming increasing difficult. In addition, proper analytical model that accurately takes into account of short range e-e and e-ion-trap force interactions in presence of random interface trap and random dopant is of utmost requirement for fast and efficient computation of threshold voltage without resorting to more complex numerical simulations. The interface traps are a result of process conditions, long term stress cycles on the MOSFET and possible hot carrier injection and they are most frequently encountered with respect to other type of defects like bulk defects (Non-stoichiometry and Schottky defects). Although the defect density at the interface varies and can never be accurately predicted, with scaling of the device, only a very few 10-100 defects or interface traps exist at the channel-SiO_2

interface and cumulative effects of the traps can be numerically simulated and analytically computed to extract the threshold voltage fluctuations.

In this dissertation, the effect of one and two random interface trap within 0.001 nm depth from the channel interface are studied on threshold voltage variations and its fluctuations with the aid of three analytical models and EMC based device simulation method aided with a novel molecular dynamics (MD) subroutine developed by the computational electronics research group of Arizona State University. From the comparison with EMC based device simulation model, it is confirmed that the reported analytical models previously cited in literature cannot account for spatially different mobility fluctuations that result from higher energy barrier created by an interface trap residing near the source of a MOSFET. Therefore, a mobility fluctuation based analytical model is developed that suffices to replicate the high spikes in the V_T fluctuation trend for source side trap positions as confirmed by 3-D accurate EMC device based simulation results. The number fluctuations due to dopant numbers are incorporated in the new model through the surface potential band bending at the oxide-semiconductor interface and inversion charge density calculations at threshold. From our EMC based device simulation, it has been demonstrated that the fluctuations in threshold voltage have been dependent on particular random dopant distribution type, i.e., its number within the channel area and its position, in addition having strong correlation on strategically positioned interface traps along the channel from source to drain. In order to truly represent the amplitude variation to show more dependence on spatial positioning of trap than specific random dopant type, the

expectation value of the statistic (drain current or threshold voltage amplitude change) or the average term needs to be studied out of a significant number of possible random channel dopant distributions. Since source and drain halo pocket implanted MOSFET device is a mainstream technology with rapid scaling of technology node exiting in industry practice today, we have performed EMC based device simulations on trap induced threshold voltage fluctuations assessment for a smaller and larger halo implanted 45 nm gate length MOSFET. The simulation results importantly reveal that although pocket implant at source and drain junction of a MOSFET is desirable for control of threshold voltage roll-off from the gate length scaling perspective, the fluctuations in threshold voltage are rather large even for a shorter halo doped MOSFET when the traps are closer to source at the channel interface. Therefore judicious choice has to be made with respect to halo doping pocket length and its mean average doping to strike a trade-off between tolerable V_T roll of and its fluctuation tolerance limit when a trap is encountered at the channel interface during long term operation of the MOSFET.

CHAPTER 8

Future Work

Currently the short-range and long range e-e and e-ion interactions do not accurately include the remote charge scattering induced by fluctuations of image charges induced on the gate within a cut-off range along with random and discrete inversion charges of the channel and bulk discrete charges. Due to the nature of ultrathin gate dielectric situation (0.9 nm thickness of SiO_2) for the scaled 45 nm gate length MOSFET, treatment of remote charge scattering by modification of Coulomb energy with regard to carriers occupied by a single trap either at the interface or inside the oxide, becomes more pronounced and non-negligible as this factor will lead to additional mobility reduction as the gate oxide becomes thinner. Therefore, one of the goals of the future research work is directed at inclusion of Coulomb interactions among mostly short-range discrete and random electrons in the inversion layer, ionized impurity in the depletion region and remote charges on the gate electrode.

After accounting for short-range image force on the gate, our work will also explore the effect of oxide lying traps distributed randomly from silicon–oxide interface to the gate-oxide interface. Polarization effects, due to electron occupied by a trap inside the dielectric, imparting spatially nonuniform dielectric constant of the oxide as a function of depth from the semiconductor-oxide interface will be considered using the method of images that enable computation of electric field contours correctly satisfying the boundary conditions at the dielectric interfaces.

Due to spatially nonuniform discrete field resulting an inversion layer charge and it image charge on the gate specifically in the short-range interactions, the image factor will neither be purely 1 at strong inversion near the $Si:SiO_2$ interface nor be 0 at the metal gate $:SiO_2$ interface. As for threshold voltage and its standard deviation fluctuation, we expect to see more variation in the computation of the image factor as we encounter weak inversion to moderate inversion region for extraction of threshold voltage, where image charges have greater impact on device characteristics. Our simulations are expected to replicate these differences in the fluctuation profile for threshold voltage maintaining the general trend, i.e., fluctuation gradually decreasing toward the metal-oxide interface location of oxide-imbedded traps in interaction with carriers from the inversion layer of the effective 32 nm gate length MOSFET.

REFERENCES

[1] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya and G. Slavcheva, "Simulation of Intrinsic Parameter Fluctuations in Decananometer and Nanometer-Scale MOSFETs", in IEEE Transactions On Electron Devices, Vol. 50, No. 9, pp. 1837-1852, (2003).

[2] A. Asenov, R. Balasubramaniam, A. R. Brown and J. H. Davies, "RTS Amplitudes in Decananometer MOSFETs: 3-D Simulation Study", in IEEE Transactions On Electron Devices, Vol. 50, No. 3, pp. 839-845, (2003).

[3] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/f) noise", in Advances in Physics, Vol. 38, No.4, pp. 367-468, (1989).

[4] W. J. Gross, D. Vasileska and D. K. Ferry, "3D Simulations of Ultra-Small MOSFETs with Real-Space Treatment of the Electron-Electron and Electron-Ion Interactions", VLSI Design, Vol. 10, pp. 437-452, (2000).

[5] W. J. Gross, D. Vasileska and D. K. Ferry, " A Novel Approach for Introducing the Electron-Electron and Electron-Impurity Interactions in Particle Based Simulations", IEEE Electron Device Letters, Vol. 20, No.9, pp.463-465, (1999).

[6] L. Brusamarello, G. I. Wirth and R. da Silva, "Statistical RTS model for digital circuits", Microelectronics Reliability, Vol. 49, Issues 9-11, pp. 1064-1069, (2009).

[7] X. Tang, V. K. De and James D. Meindl, " Intrinsic MOSFET Parameter Fluctuations Due to Random Dopant Placement", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 5, No. 4, pp. 369-376, (1997).

[8] K. Sonoda, K. Ishikawa, T. Eimori and O. Tsuchiya, "Discrete Dopant Effects on Statistical Variation of Random Telegraph Signal Magnitude", IEEE Transactions On Electron Devices, Vol. 54, No. 8, pp. 1918-1925, (2007).

[9] R. W. Keyes, "The Effect of Randomness in the Distribution of Impurity Atoms on FET Thresholds", Applied Physics, Vol. 8, pp. 251-259, (1975).

[10] J. R. Brews, "Carrier-density fluctuations and IGFET mobility near threshold", Journal of Applied Physics, Vol. 46, No. 5, May 1975, pp. 2193-2203.

[11] E. Simoen, B. Dierickx, C. L. Claeys and G. J. Declerck, "Explaining the amplitude of RTS Noise in Submicrometer MOSFETs", IEEE Transactions on Electron Devices, Vol 39, No. 2, pp. 422-429.

[12] G. I. Wirth, J. Koh, R.da Silva, R. Thewes and R. Brederlow, "Modeling of Statistical Low-Frequency Noise of Deep-Submicrometer MOSFETs", IEEE Transactions on Electron Devices, Vol. 52, No. 7, 2005, pp. 1576-1588.

[13] M. J. Kirton, M. J. Uren, S. Collins, M. Schultz, A. Karmann and K. Scheffer, "Individual defects at the Si:SiO_2 interface", Semiconductor Science Technology, Vol. 4, 1989, pp. 1116-1126.

[14] C. K. Williams, "Kinetics of Trapping, Detrapping and Trap Generation", Journal of Electronic Materials, Vol. 21, No. 7, 1992.

[15] D. Vasileska, S. M. Goodnick and G. Klimeck, Computational Electronics: Semiclassical and Quantum Transport Modeling, Taylor and Francis, June (2010).

[16] M. V. Fischetti and S. E. Laux, "Long-range Coulomb interactions in small Si devices. Part I: Performance and reliability," Journal of Appl. Phys., Vol. 89, pp. 1205–1231, (2001).

[17] P. Lugli and D. K. Ferry, "Degeneracy in the Ensemble Monte Carlo Method for High-Field Transport in Semiconductors", IEEE Trans. On Electron Dev., Vol. 32, No. 11, pp. 2431-2437, (1985).

[18] R. W. Hockney and J. W. Eastwood, Computer Simulation Using Particles (New York, McGraw-Hill, 1981).

[19] L. Greengard and V. Rokhlin, "A fast algorithm for particle simulations," J. Comput. Phys., Vol. 135, No. 2, pp. 280–292, (1997).

[20] C. J. Wordelman, U. Ravaioli, "Integration of a Particle-Particle-Particle-Mesh Algorithm with the Ensemble Monte Carlo Method for the Simulation of Ultra-Small Semiconductor Devices", IEEE Trans. On Electron Devices, Vol. 47, No. 2, pp. 410-416, (2000).

[21] V. Rokhlin, "Rapid solution of integral equations of classical potential theory", J. Comp. Phys., Vol. 60, pp. 187-207, (1985).

[22] R. Beatson and L. Greengard, "A short course on fast multipole methods," in Wavelets, Multi-level Methods and Elliptic PDEs (Leicester, 1996), *ser. Numer. Math. Sci. Comput.* New York: Oxford Univ. Press, pp. 1–37, (1997).

[23] D. Vasileska, H. R. Khan, S. S. Ahmed, C. Ringhoffer and C. Heitzinger, "Quantum and Coulomb Effects in Nanodevices", International Journal of Nanoscience, Vol. 4, No. 3, pp. 305-361, (2005).

[24] Y. Taur and T. H. Ning, Fundamentals of Modern VLSI Devices, Cambridge University Press, pp. 147, (1998).

[25] W. Shockley, "Problems Related To P-N Junctions In Silicon", Solid State Electronics, Vol. 2, pp. 35-67, (1961).

[26] J. He, X. Zhang, Y. Wang and R. Huang, "New Method for Extraction of MOSFET Parameters", IEEE Electron Devices Letters, Vol. 22, No.12, pp. 597-599, (2001).

[27] X. Zhou and K. Y. Lim, "Unified MOSFET Compact I-V Model Formulation Through Physics-Based Effective Transformation", IEEE Transactions on Electron Devices, Vol. 48, No. 5, pp. 887-896, (2001).