Low-power Design of a Neuromorphic IC and MICS Transceiver

by

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ABSTRACT

The first part describes Metal Semiconductor Field Effect Transistor (MESFET) based fundamental analog building blocks designed and fabricated in a single poly, 3-layer metal digital CMOS technology utilizing fully depletion mode MESFET devices. DC characteristics were measured by varying the power supply from 2.5V to 5.5V. The measured DC transfer curves of amplifiers show good agreement with the simulated ones with extracted models from the same process. The accuracy of the current mirror showing inverse operation is within ±15% for the current from 0 to 1.5mA with the power supply from 2.5 to 5.5V.

The second part presents a low-power image recognition system with a novel MESFET device fabricated on a CMOS substrate. An analog image recognition system with power consumption of 2.4mW/cell and a response time of 6μs is designed, fabricated and characterized. The experimental results verified the accuracy of the extracted SPICE model of SOS MESFETs. The response times of 4μs and 6μs for one by four and one by eight arrays, respectively, are achieved with the line recognition. Each core cell for both arrays consumes only 2.4mW.

The last part presents a CMOS low-power transceiver in MICS band is presented. The LNA core has an integrated mixer in a folded configuration. The baseband strip consists of a pseudo differential MOS-C band-pass filter achieving demodulation of 150kHz-offset BFSK signals. The SRO is used in a wakeup RX for the wake-up signal reception. The all

digital frequency-locked loop drives a class AB power amplifier in a transmitter. The sensitivity of -85dBm in the wakeup RX is achieved with the power consumption of 320μW and 400μW at the data rates of 100kb/s and 200kb/s from 1.8V, respectively. The sensitivities of -70dBm and -98dBm in the data-link RX are achieved with NF of 40dB and 11dB at the data rate of 100kb/s while consuming only 600μW and 1.5mW at 1.2V and 1.8V, respectively.

To my wife, Hyunok, and my sons, Panseo and Taeseo.

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CHAPTER 1

INTRODUCTION

Complementary Metal Oxide Semiconductor (CMOS) continues to scale down to meet the growing demand for low voltage and low power systems. The required power supply voltage will be as low as 1V for Radio Frequency (RF) and Analog Mixed-signal circuit designers in 2010 according to the International Technology Roadmap for Semiconductors (ITRS). Scaling of size and reduction in power supply voltages lead more integration and lower power consumption while they cause unavoidable performance problems such as limited output voltage swing due to reduced headroom and back compatibility problems. Furthermore, as CMOS scales down, the breakdown voltage reduces as well. The reduction in the breakdown voltage causes CMOS devices to fail their functionality in analog or RF and power management systems due to inductive loads such as voltage controlled oscillators (VCO), RF power amplifiers, and switch-mode DC-DC converters in which the transistors experience 2 to 4 times larger voltage than power supply [1]. For high breakdown voltage, lateral-diffused MOSFETs (LD-MOSFETs) have been used. However, LD-MOSFETs are not fully compatible with current CMOS process flows since they require process modifications to achieve high breakdown voltage. To overcome these limitations silicon-on-insulator Metal Semiconductor Field Effect Transistors (SOI MESFETs) have been fabricated and demonstrated in partially depleted (PD) process with no

changes to the standard CMOS process flow. Although the breakdown voltage depends on a channel access length (L_a, the distance from a gate to a source or drain), the maximum breakdown voltage exceeds 50V [1]. High voltage compliant MESFETs provide an elegant solution to the voltage scaling of advanced CMOS technologies. However, for SOI and silicon-on-sapphire (SOS) MESFETs to be used in the design of analog and RF systems, the accurate DC and RF behavioral models must be developed. The MESFETs which are typically operated in depletion mode can be modeled using the TOM3 model. The TOM3 model was originally developed for modeling the DC and RF characteristics of Gallium Arsenide (GaAs) MESFETs, but is suitable for fully depleted SOS MESFETs [2] since they are unaffected by a bias on the substrate. The 3-terminal TOM3 model can also be used for SOI MESFETs provided the source and substrate are at the same potential. An accurate TOM3 large signal Spice model for SOI MESFETs was successfully extracted and demonstrated as described in [3]. Fully CMOS compatible SOS MESFET based fundamental analog building blocks such as single ended and differential amplifiers and a high impedance current mirror have been fabricated using a SOS CMOS foundry with no changes to the standard CMOS process flow. The DC characteristics have been measured using supply voltages in the range 2.5 to 5.5V and show good agreement with the simulated results using a calibrated TOM3 model.

CHAPTER 2

CMOS COMPATIBLE FULLY DEPLETED MESFETS [2]

The MESFETs used for the analog building blocks were fabricated using a 3-layer metal digital SOS CMOS technology. Detailed fabrication process for partially depleted SOI (PD-SOI) MESFETs has been described in [1]. A similar approach has been used here for the FD-SOI MESFETs with the islands of Schottky gate material defined using a silicide block mask [2].

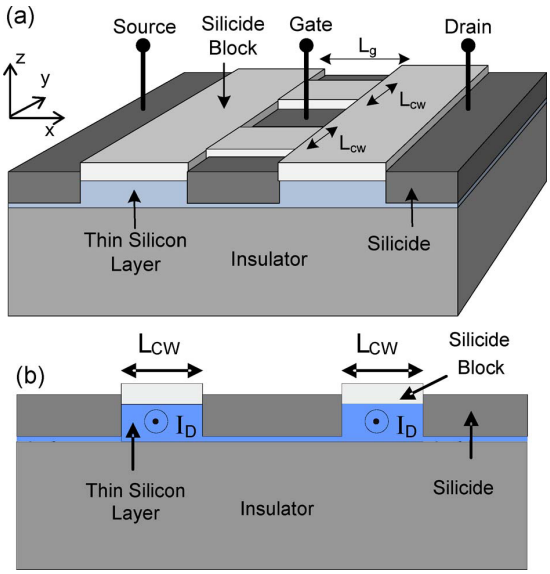


Fig. 1. a) 3D rendering of the FD-SOI MESFET showing two conducting channels confined between islands of silicide. Electrical contact to each silicide island is provided by vias to the first layer of metal interconnect (not shown). b) A cross section in the y-z plane through the center of the device showing the conducting channels formed underneath regions of silicide block [2].

Fig. 1 presents a 3D rendering of the device. The access regions were formed either from a silicide block layer, which is also used to define resistors in active regions or from a polysilicon layer used to define the MOS gate. The minimum feature sizes of the FD-SOI MESFETs are limited by the design rules of the technology used. For the 0.25μm SOS CMOS process the design rules allowed channel lengths, L_g, as small as 1.8μm with channel widths, L_{cw}, down to 0.25μm. The SOS MESFETs were designed to have multiple fingers, each finger having a number of nominally identical channels. The threshold voltage (V_{th}) of the SOS MESFETs used for the analog building blocks was -0.8V. The main feature of the SOI and SOS MESFET is their high voltage breakdown. Breakdowns in excess of 50V have been shown on a 3.3V PD-SOI process [1]. For the SOS MESFETs used here the breakdown voltage exceeds 7.5V [2]. Other features include being able to adjust the threshold voltages without changing any process steps, wide temperature operation and high linearity. Any standard SOI/SOS CMOS process can harness the advantage of both these devices to create the most efficient circuit for the specific application.

CHAPTER 3

DC CHARACTERIZATION [2]

The turn-on characteristics of n-MESFETs are shown in Fig. 2. The channel length L_g was 1.8μm with a total of 150 channels. The channel width L_{CW} was varied from 0.25 to 1μm. The device operates in depletion mode. The inset of Fig. 2 show the I_G-V_{GS} data for V_D=V_S=0V. The dashed line in the small additional window in Fig. 2 is the fit to the exponential function [4]

$$I_{diode} \sim AA'T^2 e^{-\Phi B/UT} e^{VG/nUT}$$

where U_T=kT/e.

From curve fits to experimental data, an ideality factor n=1.24 was extracted for n-MESFETs. The Schottky barrier Φ_B can be extracted from the fit, but this is complicated by the uncertainty in the conducting area A of the MESFET gate. If the gate current at V_{DS}=0V flows predominantly out of the four vertical edges of the silicide gate islands, then the total conductiong gate area is given approximately by $4NL_gT_{Si}$, where N is the number of channels and T_{si} is the thickness of the silicon channel. For the SOS devices, T_{Si} ≈100nm [5] and the total gate area is ~ 1.1 x 10^{-6} cm^2 for the devices with N = 150 channels. Assuming effective Richardson constants A^* of 110 and 32 A · cm^{-2} · K^{-2} [4], we derive barrier heights of 0.48 for the n-MESFETs. The measured barrier height for the n-MESFETs is lower than the ~0.6eV quoted for $CoSi_2$ [7] to n-Si but is still reasonable given the uncertainty in the gate area.

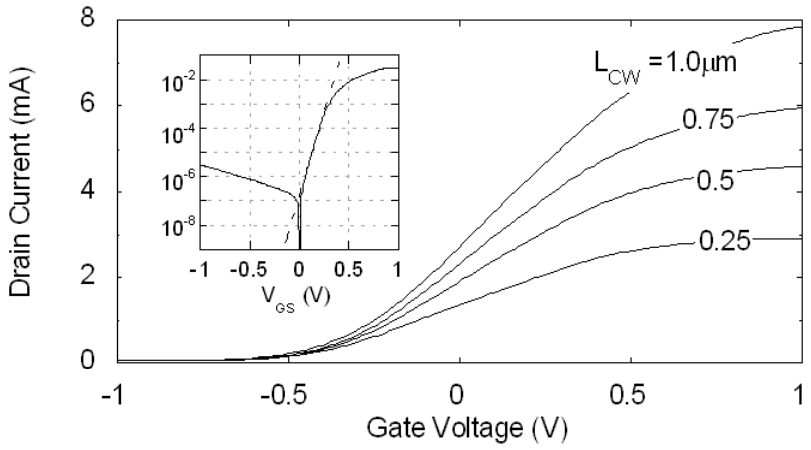


Fig. 2. The turn-on characteristics, I_D-V_{GS} for the n-MESFETS (V_{DS} = 2V) for different channel widths, L_{CW}. The insets show the magnitude of the gate current for L_{CW} = 0.25μm [2].

The magnitude of the threshold voltage increases as L_{CW} increases because of the greater lateral distance required to deplete the channel. The threshold voltage is plotted as a function of channel width in Fig. 3. It is clear that the threshold voltage of the FD-SOS MESFETs can be controlled by varying the physical dimension L_{CW}. This is an advantage compared to the PD-SOI MESFETs for which the threshold voltage is dictated by the SOI channel thickness and well doping and cannot be adjusted without making changes to the CMOS process flow. The dashed line in Fig. 3 is the linear fits to the data.

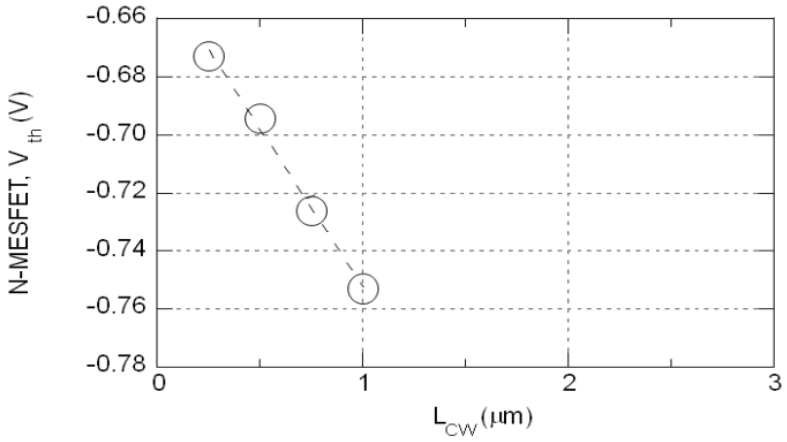


Fig. 3. Threshold voltage of the SOS MESFETs as a function of the channel width defined by the spacing between silicide islands, L_{cw}. The dashed lines are linear fits to the data [2].

Fig. 4 shows the I_d-V_{ds} family of curves for the n-channel device. Good output current saturation is observed for drain votages that greatly exceed the 3.5-V breakdown voltage of the CMOS transistors. The high-voltage capability of the FD-SOS MESFETs is in part due to the drift region between the ends of the channel and the drain contact that is a natural outcome of the nonself-aligned MESFET geometry [1].

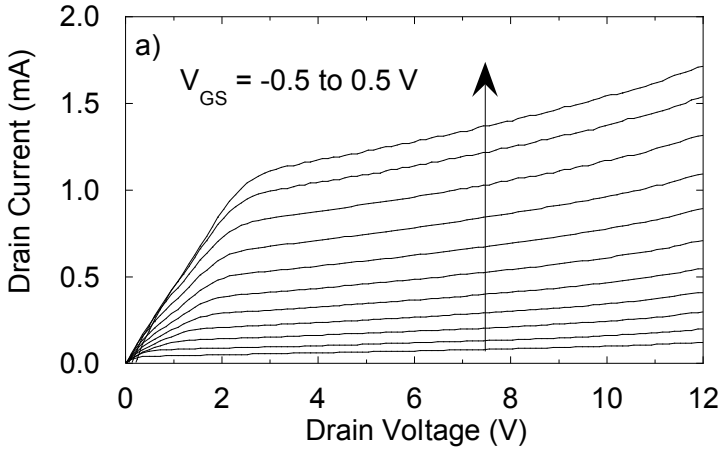


Fig. 4. The family of curves for the n-MESFET for gate voltages in the range –0.5 to +0.5 V in 0.1 V steps. Lg = 1.8μm and L_{CW} = 0.25μm [2].

CHAPTER 4

ANALOG BUILDING BLOCKS

4.1 Cross Coupled Current Mirror

GaAs MESFETs have been widely employed for the design of high speed communication circuits such as operational amplifiers and switched capacitor filters since they benefit from the high mobility transport properties compared to CMOS. However, the main drawback of GaAs MESFETs is the absence of a p-type MESFET [7-8] and also they do not integrate well with MOSFETs. Therefore analog circuits using GaAs MESFETs usually have been designed with only n-type MESFETs. Similarly, due to the lack of a p-type MESFET at the time of production in our process flow, an n-type only design was used for analog building blocks. In order to address this limition, an inverting current mirror formed with cross coupled gate source nodes is used. An inverting current mirror can be analyzed through the following small signal analysis as shown in Fig. 5.

$$I_{ref} = g_{m1} V_{s2s1} \tag{1}$$

$$I_{copy} = g_{m2} V_{s1s2} \tag{2}$$

Rewriting

$$V_{s1s2} = \frac{I_{copy}}{g_{m2}} = -V_{s2s1} \tag{3}$$

By substituting (3) into (1),

$$I_{ref} = g_{m1}(-\frac{I_{copy}}{g_{m2}}) = -\frac{g_{m1}}{g_{m2}} I_{copy} \quad (4)$$

Rewriting (4) gives us the final expression of the copied current.

$$I_{copy} = -\frac{g_{m2}}{g_{m1}} I_{ref} \quad (5)$$

where g_{m1} and g_{m2} are transconductance of M1 and M2, respectively. It is worth noting that the copied current is inversely proportional to the reference by the ratio of transconductance of devices M1 and M2.

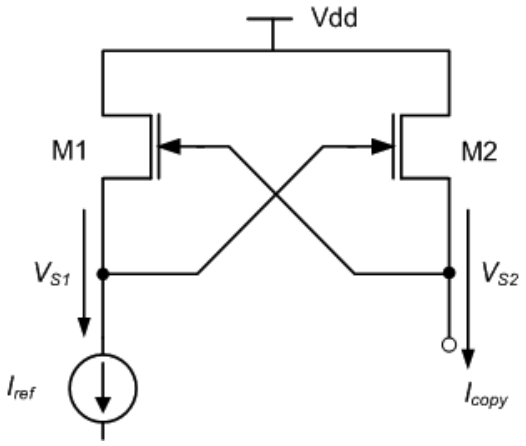


Fig. 5. Transistor level implementation of the cross coupled gate source inverting current mirror.

4.2 Amplifiers

The proposed amplifiers presented in Fig. 6 (a) and (b) consist of a SOS MESFET input pair and an inverting current mirror shown in Fig. 5 which replaces an active load. The main drawback of an SOS MESFET inverting current mirror is the lower output resistance at the output nodes compared to its CMOS conterpart. It is because the resistance at the

source of the devices M7 and M8 is $1/g_{m7,8}$ and they are in parallel with those of M5 and M6. As a result, the output resistance at the output nodes of the amplifiers (the drain nodes of M5 and M6 for the differential) is inversely proportional to the transconductance of devices M7 and M8 (for the differential). This inherent low output resistance causes the MESFET based amplifiers to have lower DC gain compared to a CMOS counterpart. To improve the output resistance and the DC gain, the high impedance current mirror which will be introduced in the next section is often employed in the design of high gain amplifiers. However, in this paper, since our goal is to validate the large signal Spice model to reproduce the measured results, the basic inverting current mirror depicted in Fig. 5 is used for an active load for simplicity at the expense of DC gain. All MESFETs operate in depletion mode. The channel length is set at 1.8 μm due to the design rule restrictions, L_{cw} = 0.25 μm, and there are 300 channels.

4.3 High Impedance Cascoded Current Mirror

For the high impedance cascoded current mirror design, the focus was on the fabrication and measurement of a fully CMOS compatible SOS MESFET inverting current mirror since lack of p-type MESFET makes the design of p-type current mirror impossible in contrast to CMOS counterpart. As explained earlier, the low output resistance of the basic current mirror shown in Fig. 5 limits its application. In order to increase the

output impedance, the configuration shown in Fig. 7 has been choosen for the current mirror.

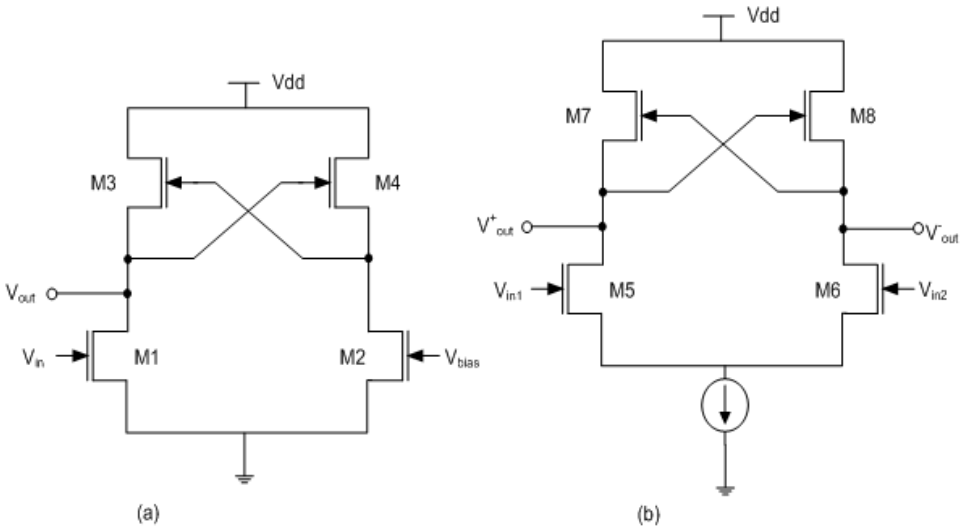


Fig. 6. (a) Single ended amplifier employing an inverting current mirror replacing an active load

(b) Differential amplifier employing an inverting current mirror replacing an active load

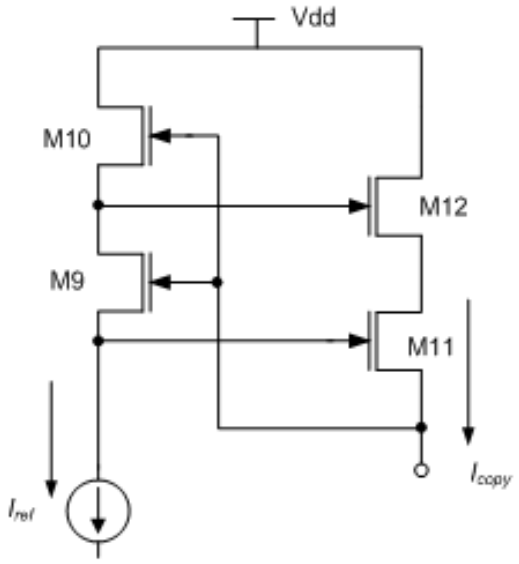


Fig. 7. High impedance cascoded current mirror

CHAPTER 5

MEASUREMENT RESULTS

Fig. 8 shows the measured and simulated results of the single ended amplifier with input swept from -1 to 1V with various power supplies. For the differential amplifier, the plot of the measured results is shown in Fig. 9 along with the simulated ones for the purpose of comparison. The gain of a single ended amplifier is designed to be around 5 *V/V*. However, for a differential amplifier, the gain is less than unity. Due to low output impedance as explained above, this amplifier is suitable for buffer applications. Because the input devices M5 and M6 require large drain source voltage to flow the bias current, this also keeps the gain and output impedance low. If a high gain, low drive amplifier is desired, a high impedance current mirror can be used to increase the gain of the differential amplifier. In our case, the main motivation of the differential amplifier is to apply it to low power Cellular Neural Networks (CNNs) for its nonlinear (sigmoidal) DC characteristic [9]. The DC characteristics fit well in terms of its compressive characteristics. Fig. 10 shows the measured and simulated outputs of the high impedance current mirror. As the reference current varies from 0 to 1.5 mA (for V_{DD} of 5.5V), the output current is copied from 1.5 mA to -100 μA showing the inverse operation as expected. Fig. 11 is the chip microphotograph of a single ended amplifier and high impedance current mirror. The tail current source for the

differential amplifier in Fig. 3 (b) was introduced externally on a testing board.

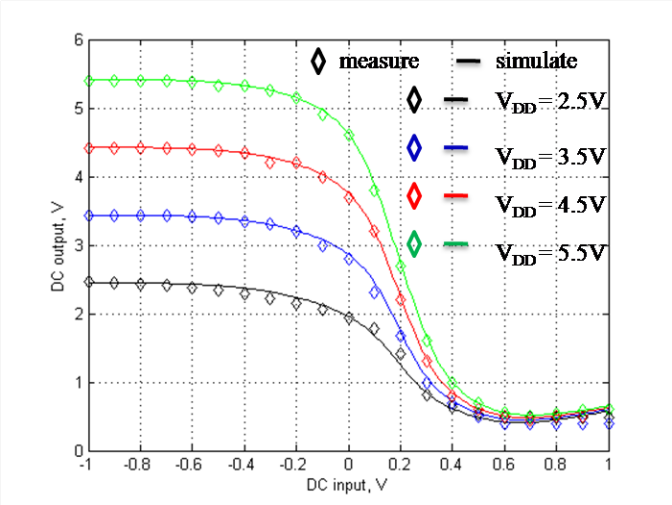


Fig. 8. Simulated and measured transfer curves for single ended amplifier.

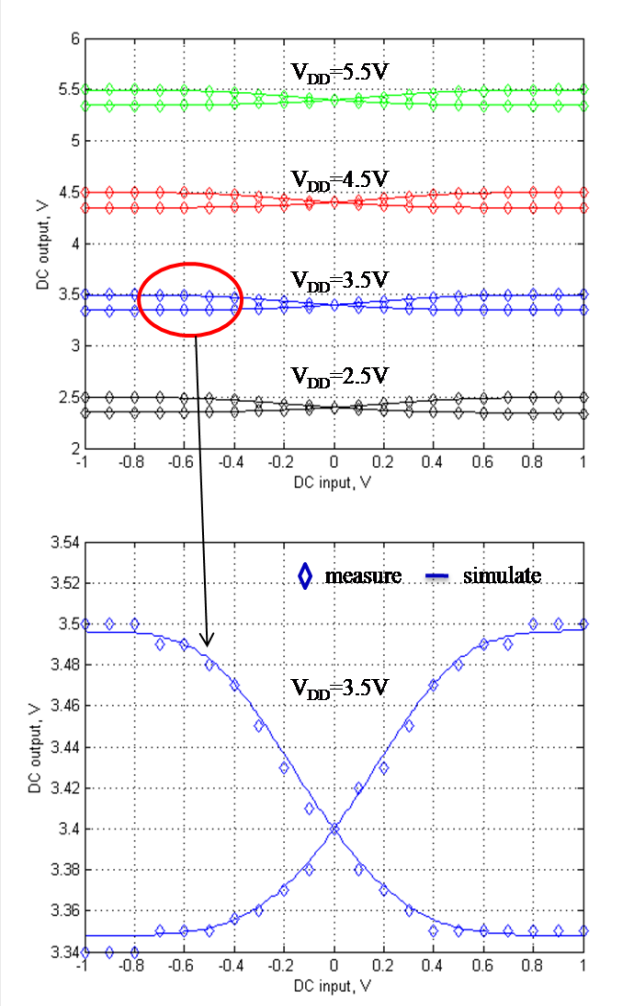


Fig. 9. Simulated and measured transfer curves for differential amplifier.

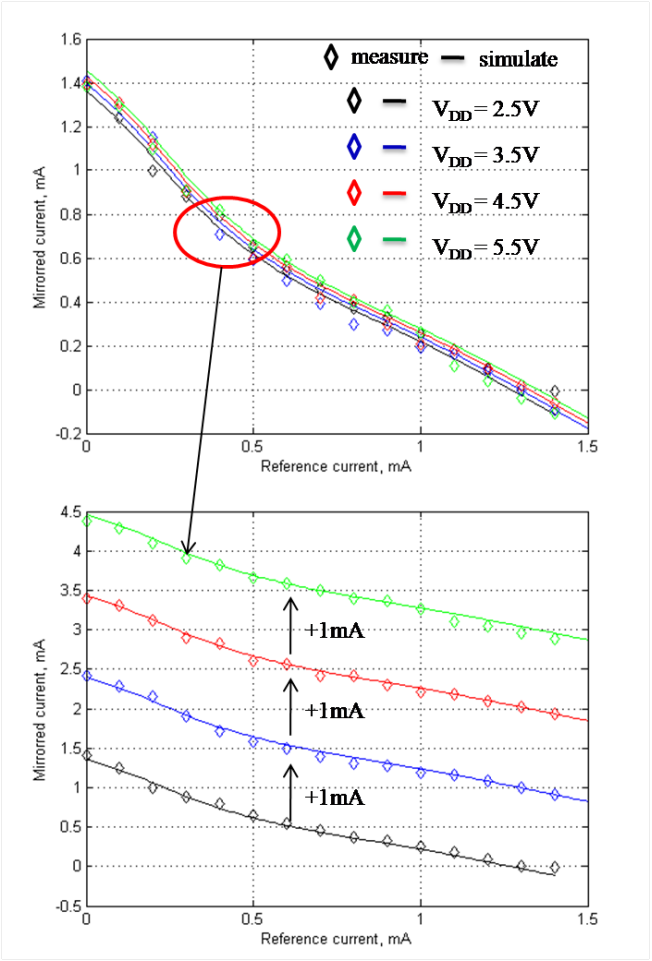
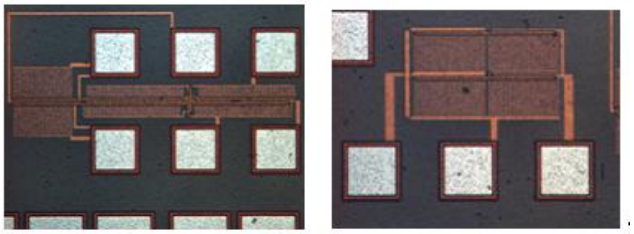


Fig. 10. Simulated and measured transfer curves for high impedance cascoded current mirror. In (b), intended current (1mA) is added for reproduction of (a) for clarity.



(a) (b)

Fig. 11. Die micrographs (a) single ended amplifier (b) high impedance current mirror.

CHAPTER 6

CONCLUSION

CMOS compatible MESFET based analog building blocks have been fabricated and measured. The single ended amplifier, differential and several current mirror topologies show good matching to extracted models over a wide range of the power supply. The measured results of the differential amplifier show good agreement with its simulated outputs. Measurement on the inverting high impedance current mirror exhibits close agreement with the simulated result over a wide range of the reference current from 0 to 1.5 mA for various power supply voltages. MESFET devices can be a viable alternative to high voltage compliant devices in deep submicron process.

PART II

SOS MESFET CELLULAR NEURAL NETWORKS

CHAPTER 1

INTRODUCTION

Digital Signal Processors (DSP) dominates variety of areas of signal and image processing. Analog information is converted into digital and processed within a digital domain inside of signal/image processing chips even though all physical signals are analog. Conventional digital signal processing methods have run into a speed bottleneck due to their serial computation. As a method to overcome this serious speed problem, J. J. Hopfiled proposed neural networks for signal/image processing [1]. These networks have characteristics of continuous-time dynamics, parallel processing, and globally interconnected network elements. Many researchers have tried to implement these networks in a very large scale integration (VLSI) technology, but their high degree of connectivity impedes their integration in a VLSI technology. In 1988, a new neural network architecture called “Cellular Neural Networks (CNNs)” was proposed by Leon O. Chua and Lin Yang [2]. Similar to Hopfiled’s networks, CNNs are continuous and real time networks. They also have connected network elements called “cells.” They differ from Hopfiled’s architecture in locally connected cells that are arranged in a regular grid of dimension one or two and not globally connected as in Hopfiled’s networks. A virtue of their grid-like array of cells that typically interact only with their nearest neighboring cells makes the implementation of CNNs in a VLSI technology simpler than one of Hopfiled’s networks. Many

researchers have succeeded in the implementation of CNNs in a VLSI technology [3-7].

Even though CNNs have several benefits in terms of their computational power, they have not been popular in a signal/image processing area. Current CNN chips that are comprised only of CMOS transistors suffer from their high power consumption and large chip size. In this paper, low power consumption as well as high speed was achieved by introducing SOS MESFETs for a CNN cell implementation. Furthermore, this novel device integrated in a CMOS process flow allows the CNN array to be interfaced with CMOS control processors and memory to create a “Universal Machine” or programmable image processing computer on a chip as shown in [8]. The main feature of SOS MESFETs is that it operates with equal or greater speed than MOSFETs because the gate capacitance of the SOS (SOI) MESFET is half that of the MOSFET for a wide range of drain currents [9]. It can be great advantage in a CNN design. As shown later in Fig. 25, a CNN standard uses parallel structures with at least 8 neighboring cells to a CNN cell. This means that input capacitance loading impacts overall power consumption of CNNs at higher operating speeds. MESFETs have at least 2-3X less input capacitance compared to MOSFET counterparts, minimizing capacitive loading and increasing speed of CNN cells [8]. Other features are high breakdown voltage and no modifications or changes to a standard CMOS process. This work describes analog image

recognition arrays for horizontal line recognition based on CNNs using a state-of-the-art silicon-on-sapphire (SOS) CMOS process with no changes to the silicon processing steps. This IC also verifies full compatibility of the MESFET device to a state-of-the-art CMOS process and accuracy of extracted DC characteristics of MESFETs. The transient characteristics are measured using several grayscale images that settle to the final recognition level and show good agreement with the simulated results from a calibrated TOM3 model extracted from the SOS MESFETs. The rest of the paper is organized as follows: Section II presents details on SOS MESFET-based CNNs in both system and transistor levels. Section III presents main experimental results. Finally, conclusions are drawn in section IV.

CHAPTER 2

CELLULAR NEURAL NETWORK

2.1 Basic Concept

2.1.1. Standard CNN [9]

The M X N standard CNN is defined by the M X N rectangular array of cells C(i,j) located at site (i,j), i = 1,2,…,M, j = 1,2,…,N.

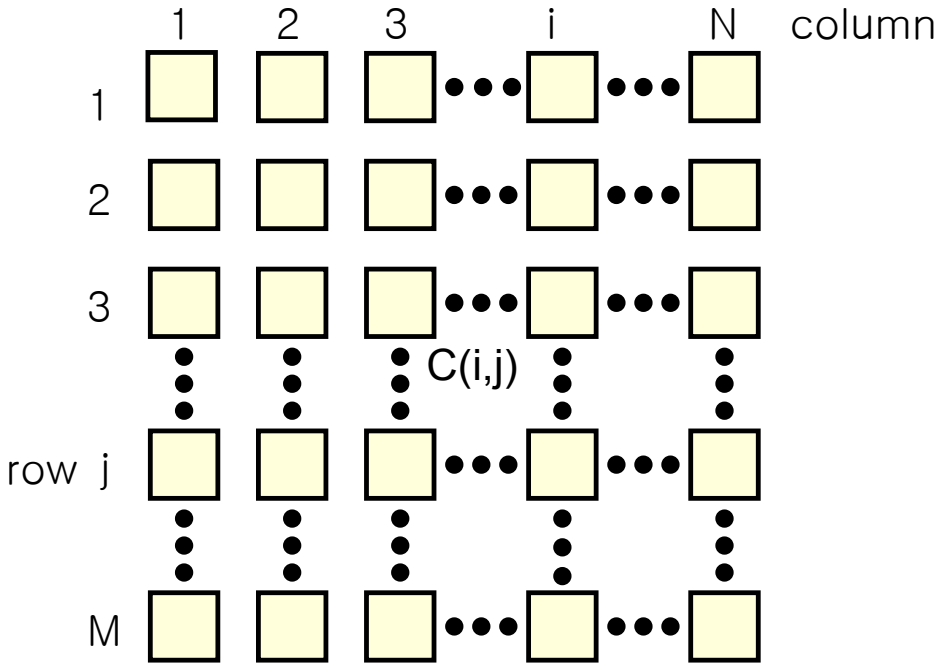


Fig.1. Standard CNN architecture

2.1.2. CNN cell [9]

Just as the word “pixel” is used to describe the smallest unit element of pictures displayed within a Liquid Crystal Display (LCD) on the common computer screen or television screen, the word “cell” is used to describe

the smallest unit element in CNN. In Fig. 1, a square represents a CNN cell and the circuit of each cell C(i,j) is shown below.

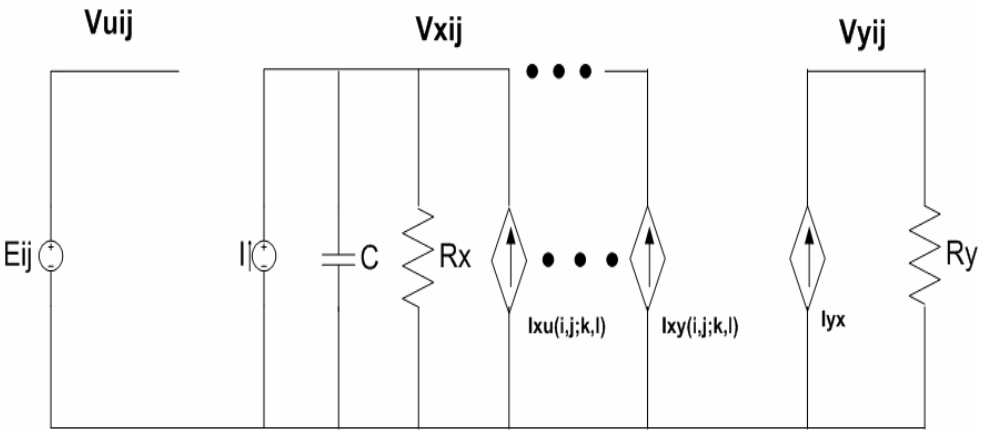


Fig.2. Basic CNN cell circuit

In Fig. 2, the unit cell has three main nodes at V_{uij}, V_{xij}, and V_{yij} and several dependent current sources that are represented by OTAs. It also has a capacitor and state resistor, Rx. The expressions for the currents of the dependent current sources are shown below.

$$I_{xu}(i,j;k,l) = B(i,j;k,l) \bullet V_{ukl}$$

$$I_{xy}(i,j;k,l) = A(i,j;k,l) \bullet V_{ykl}$$

$$I_{xy} = \frac{1}{2R_y}(|V_{xij} + 1| - |V_{xij} - 1|)$$

Using the above current equations, the CNN cell is mathematically defined as follows:

1. State equation

$$\frac{dV_{xij}}{dt} = -V_{xij} + \sum_{C(k,l)\in S_r(i,j)} A(i,j;k,l) \bullet V_{ykl} + \sum_{C(k,l)\in S_r(i,j)} B(i,j;k,l) \bullet V_{ukl} + z_{ij}$$

2. Output equation

$$V_{yij} = \frac{1}{2}\left|V_{xij} + 1\right| - \frac{1}{2}\left|V_{xij} - 1\right|$$

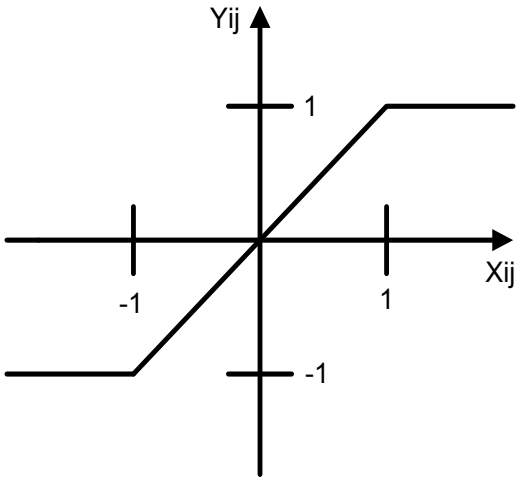


Fig.3. Transfer curve of the output

Fig. 3 shows the nonlinear transfer characteristics of the CNN cell.

2.1.3. Sphere of influence of cell C(i,j) [9]

The sphere of influence, $S_r(i,j)$, of the radius r of cell C(i,j) is defined to the set of all the neighborhood cells. CNNs cannot perform any functions within single cell. For CNNs to function properly, multiple cells must be grouped together. The smallest set of cells for any function of a CNN is called the sphere of influence $S_r(i,j)$ or the operational building block. In Fig. 4, there are two different spheres of influence of cell, creating an operational building block.

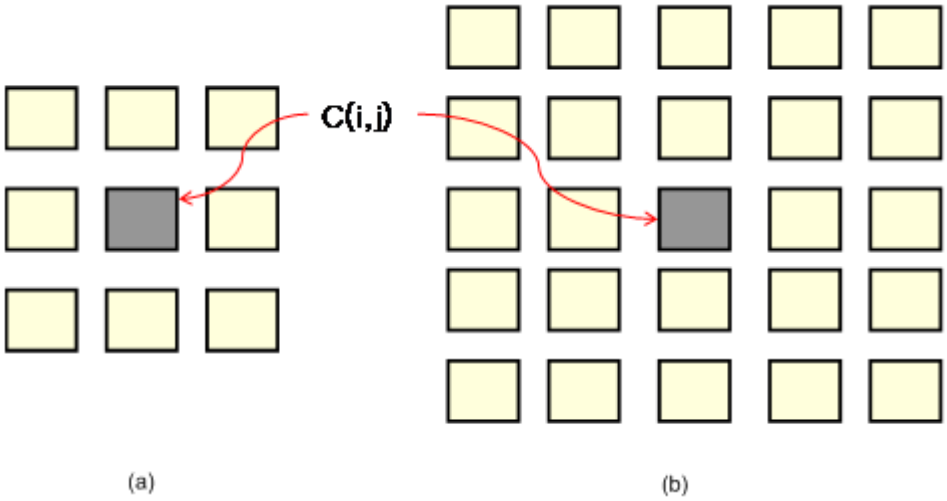


Fig.4. Sphere of influence of cell C(i,j) [12] (a) r = 1 (3 X 3 neighborhood), (b) r = 2 (5 X 5 neighborhood)

2.1.4. Template [9]

In equations (2.1) and (2.2), there are two undefined operators, A(i,j;k,l) and B(i,j;k,l). After investigating these equations, it is easily known that the two operators act like current weighting factors. In the equation (2.1), the input current, I_{xu} is generated by weighting B(i,j;k,l) to the input voltage, $V_{ukl.}$ In other words, the input current of the cell located at (i,j) is driven by multiplying the weighting factor and the input voltage of the cell located at (k,l). The operator A(i,j;k,l) uses the same process for B(i,j;k,l). These operators are called templates. The general structure of a template is shown below.

C(i−1,j−1)	C(i−1,j)	C(i−1,j+1)
C(i,j−1)	C(i,j)	C(i,j+1)
C(i+1,j−1)	C(i+1,j)	C(i+1,j+1)

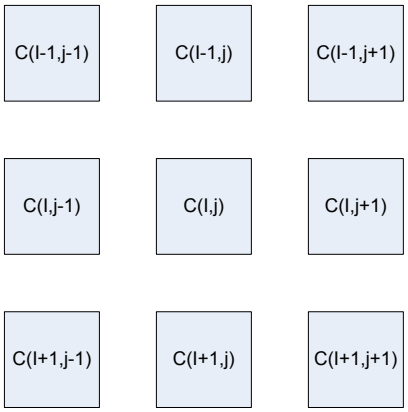
Fig.5. Template structure

The B template is usually called a control template, and the A template is called a feedback template.

2.2. Operation and Communication

2.2.1. Operation

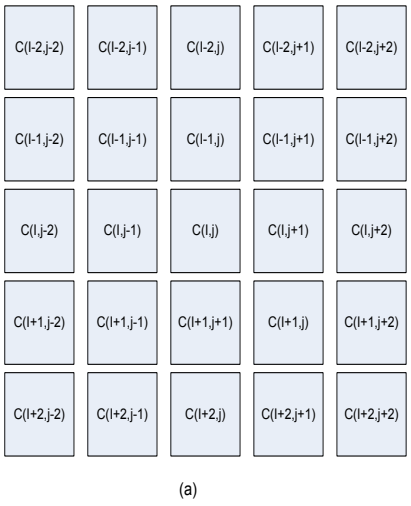
As explained in the above sections, the most important concepts are the unit cell, sphere of influence of cell (S_r) and the templates (A, B). The unit cell is the lowest level of CNN and the sphere of influence of cell (S_r) is a basic unit block where all operations are performed. Lastly, templates are sets of weighting factors for inputs (B template) and feedbacks (A template). In order to understand this better, it is required to understand the relationship between the sphere of influence of cell (S_r) and the templates. It is important to remember that the sizes of the two blocks must be the same. For example, if r = 1 for (S_r) then the sphere of influence of cell (S_r), which is called the operational building block, contains nine unit cells (3 X 3 matrix). In this case, two templates (A, B) should have the same sizes of matrices. Furthermore, if r = 2 then S_r has 25 unit cells (5 X 5 matrix) and the templates are also a 5 X 5 matrix.



C(i−1,j−1)	C(i−1,j)	C(i−1,j+1)
C(i,j−1)	C(i,j)	C(i,j+1)
C(i+1,j−1)	C(i+1,j)	C(i+1,j+1)

(b)

Fig.6. Example 1, r = 1 (a) sphere of influence of cell (b) template



C(i-2,j-2)	C(i-2,j-1)	C(i-2,j)	C(i-2,j+1)	C(i-2,j+2)
C(i-1,j-2)	C(i-1,j-1)	C(i-1,j)	C(i-1,j+1)	C(i-1,j+2)
C(i,j-2)	C(i,j-1)	C(i,j)	C(i,j+1)	C(i,j+2)
C(i+1,j-2)	C(i+1,j-1)	C(i+1,j)	C(i+1,j+1)	C(i+1,j+2)
C(i+2,j-2)	C(i+2,j-1)	C(i+2,j)	C(i+2,j+1)	C(i+2,j+2)

(b)

Fig.7. Example 2, r = 2 (a) sphere of influence of cell (b) template

In general, most CNNs contain r = 1 that is, the sphere of influence of cell (S_r) contains nine unit cells and templates A and B are of a 3 X 3 matrix. This means that the smallest size of CNN is 3 X 3. Unfortunately, no CNN with a 3 X 3 matrix can successfully perform the proper functions. The vertical and horizon line detection CNNs–the basic functions of

CNN—require at least a 4 X 4 CNN and will be discussed in the following chapters.

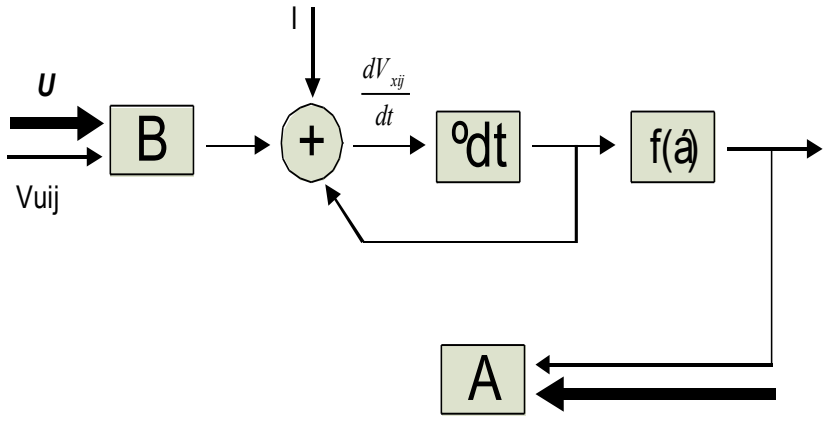


Fig.8. Operation of CNN unit cell [14]

The above figure shows the operation of a CNN unit cell. The notation Vuij is an input voltage of a selected cell as a basis and U is voltages from the nearest eight neighboring cells. All of these voltages are weighted to desired values by the B template. The A template controls the feedback voltages in the same way as the B template.

2.2.2. Communication

It is helpful to throw a template on a CNN matrix to understand how it communicates with neighboring cells. It is easy to be confused between a template and sphere of influence of cell (S_r) due to their same size of characteristic. Once again, it is important to remember that the sphere of influence of cell (S_r) is the smallest operational building block. In other

words, the CNN can be extended to more than a 3 X 3 matrix by attaching more unit cells on each side of an operational building block. The figure below demonstrates the operation of CNN more clearly.

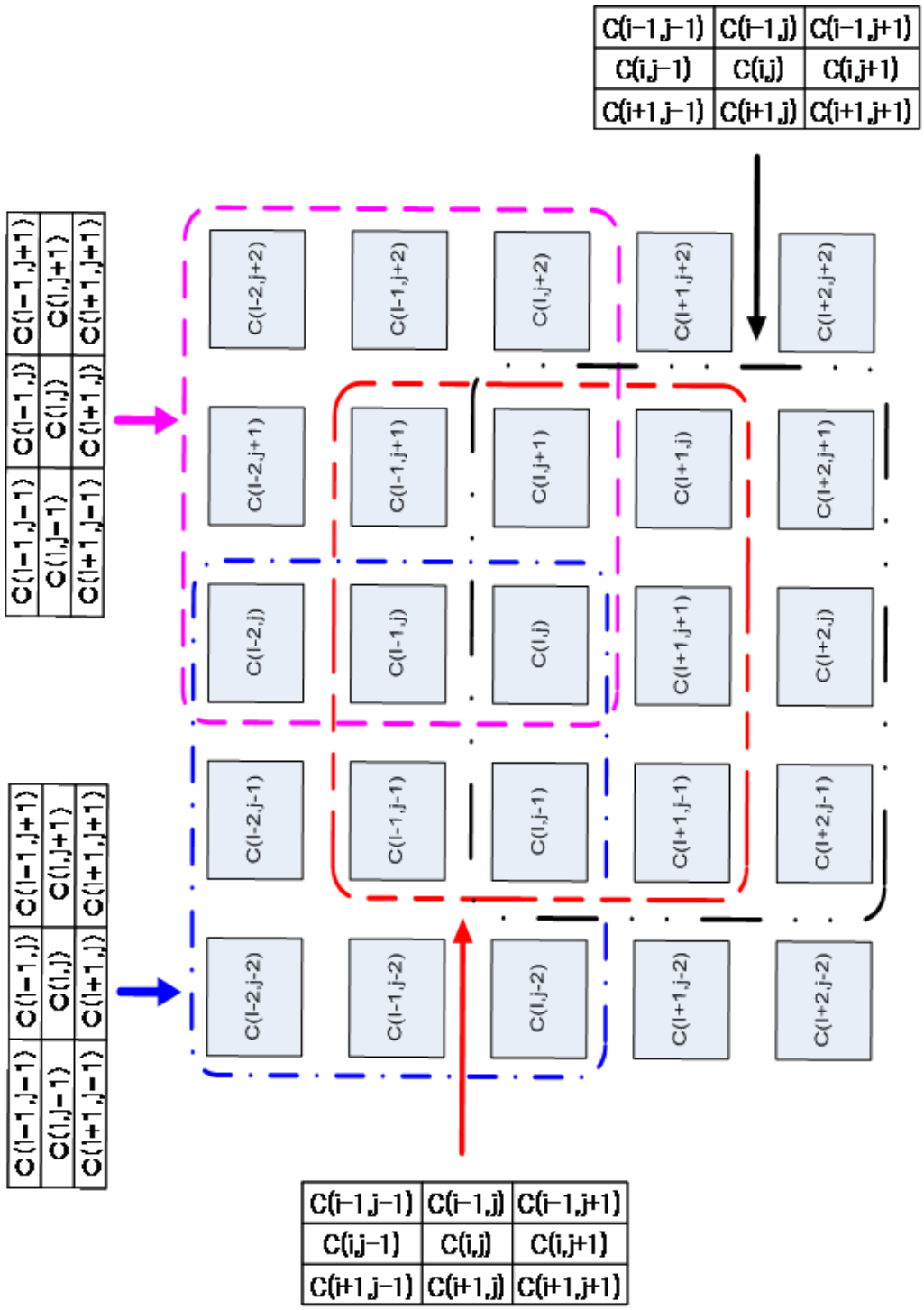


Fig.9. Projection of a template on CNN

As shown in Fig. 9, the template controls nine cells in a 5 X 5 CNN. If one unit cell is selected then the nearest eight neighboring cells are under the influence of a template. This is similar to applying a CNN with r = 2.

The following two figures help demonstrate CNN communication. Fig. 10 represents how the unit cell in a CNN sends its signal to the other eight neighboring cells. Diamond-shaped figures are dependent current sources which are controlled by voltage of the unit cell centered at the figure and two templates A and B. The weighted currents through the templates A and B are sent to the neighboring cells.

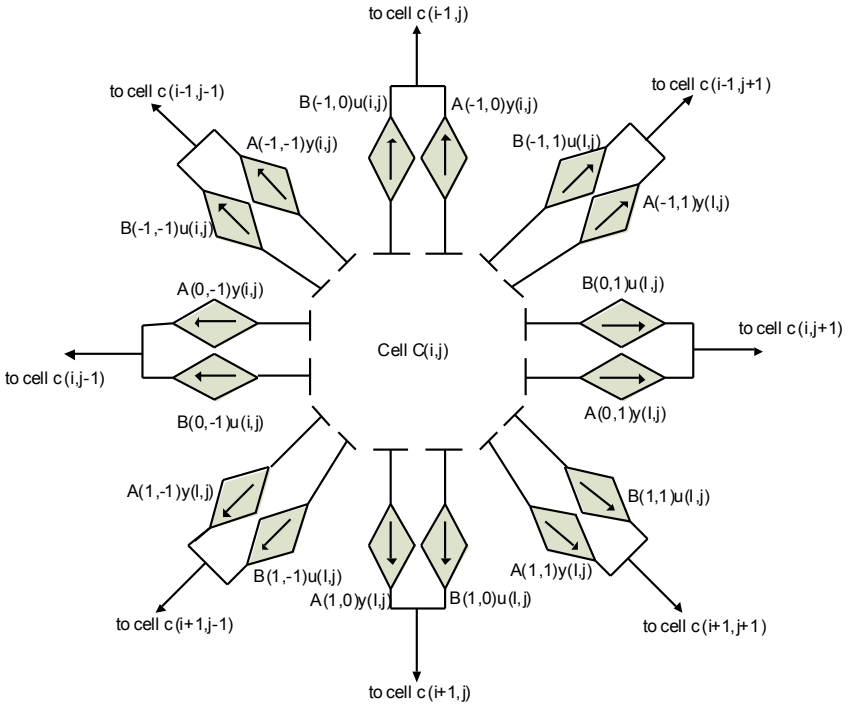


Fig. 10. Communication of CNN [14], sending signals to neighboring cells

The receiving currents from the eight neighboring cells in the unit cell located at the center of Fig. 10 are similar to the aforementioned. The

weighted currents through the two templates A and B sent from the unit cell located at the center of Fig. 3 reach the node at X(i,j) in Fig. 11.

There are three nodes, three different dependent current sources, two resistors and two capacitors in the unit cell circuit. The capacitor (Cu) at the node of U(i,j) is used to conserve the value of the input voltage and the capacitor (Cx) is the state capacitor and help conserve the value of the state node, X(i,j). The first dependent current source on the left side of Fig. 11 is a self-controlled source. In other words, the output current is generated by the input voltage of the unit cell itself and the template B. The second source is similarly controlled by the template A and the feedback voltage of the unit cell itself. The resistor, Rx, is called a state resistor and determines the voltage at the node of X(i,j). The current source on the right side of the figure is controlled by the voltage at the node of X(i,j). With this current, the resistor, Ry, represents the final output of the unit cell. The same procedures are done in all unit cells of CNN.

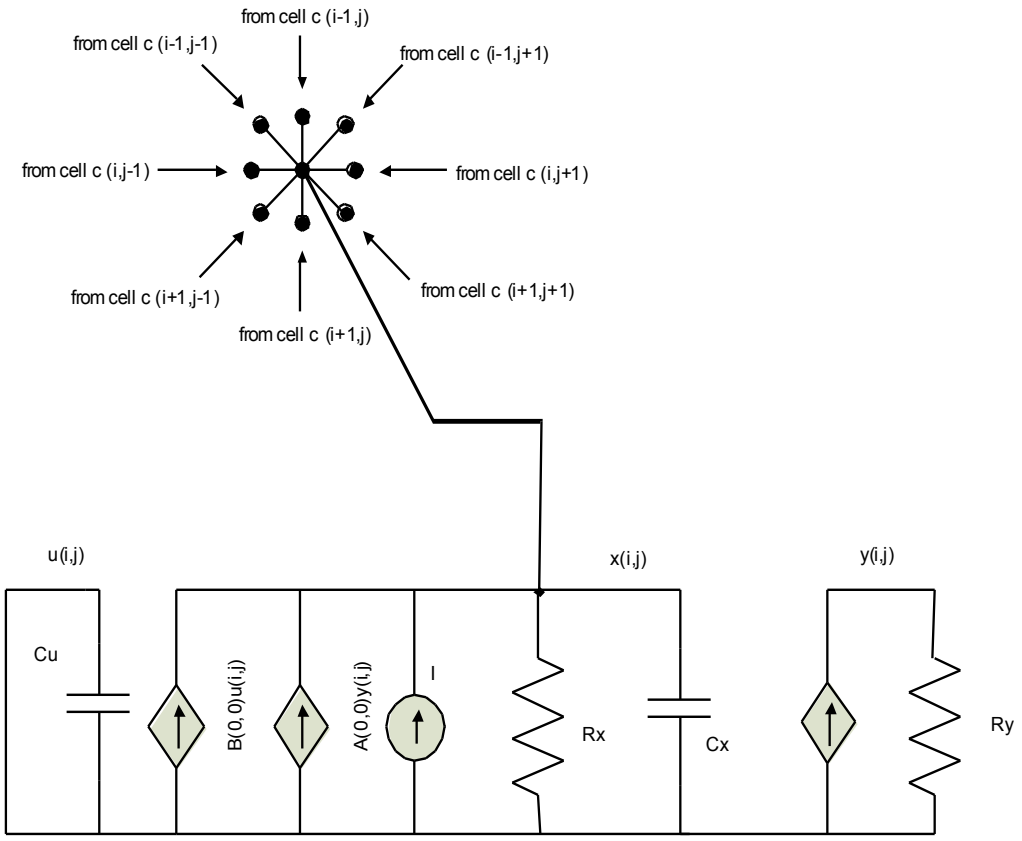


Fig.11. Communication of CNN [14], receiving signals from neighboring cells

The basic concepts, operation and communication of CNN have been explained in this section. The two architectures will be discussed in the following chapter.

2.3. CNN Architecture

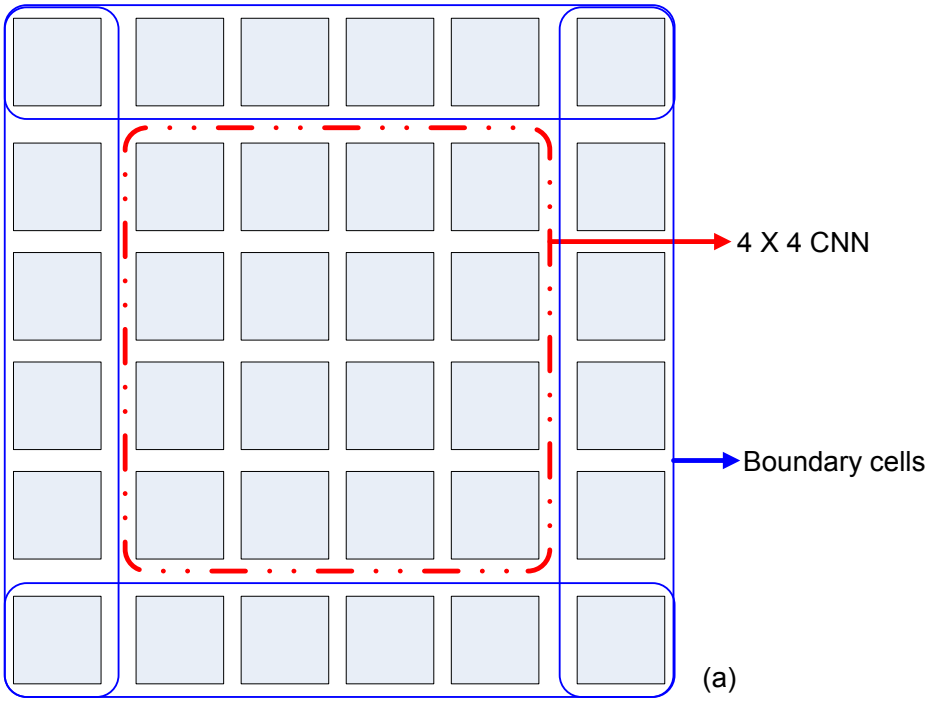
Since the theory of CNN was first proposed by L. O. Chua and L. Yang [9], a lot of researchers have focused their efforts on the implementation of CNN in VLSI technology. While some have had great success, their CNN chips were restricted in specific image processing. In

other words, these chips could do only one function intended by a researcher.

A CNN with only one function is called a Fixed-Templated CNN. A Fixed-Templated CNN also has only one template set, which has fixed weighting factors for the two templates A and B. However, image processing is not simple and must perform functions to process an image. This means that templates A and B should set with any combinations of weighting factors, which can be accomplished using a Universal CNN.

2.3.1. Fixed-Template CNN

The Fixed-Template CNN has only one template set. Some templates were developed for special purposes such as connected component detectors [17], hole fillers [18] and shadow detectors [19]. Among these fixed templates, a connected component detector was implemented in VLSI and published by J. M. Cruz and L. O. Chua in 1991. [11] The simplest sets are a vertical and horizon line detection CNN and the below figures represent the combination of each function. This thesis will be written on the basis of vertical and horizon line detection CNN due to their ease of design, simulation, and explanation. Fig. 12 shows the combination of the CNN architecture and two templates A and B for the vertical line detection.



0	1	0
0	2	0
0	1	0

(b)

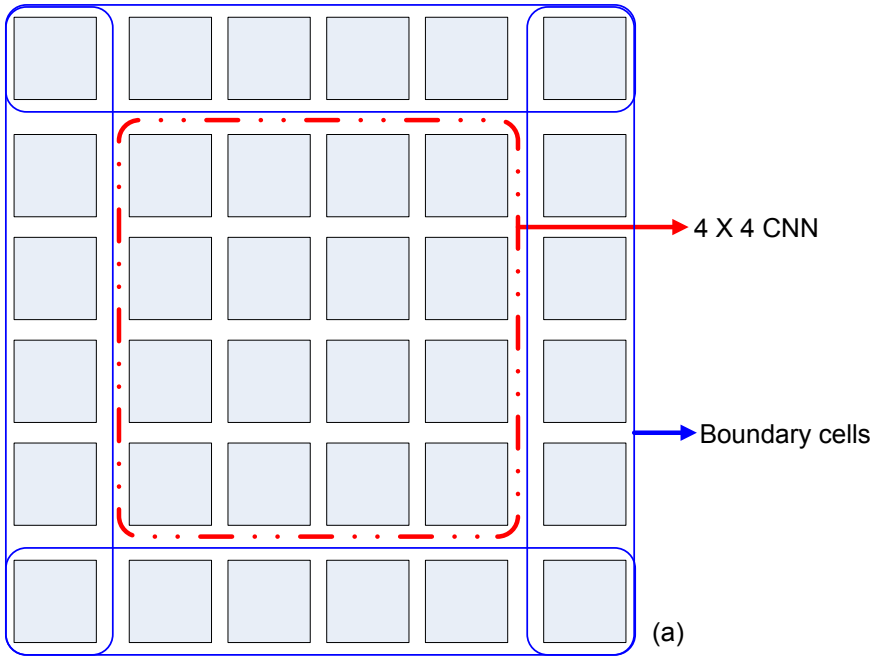
0	0	0
0	0	0
0	0	0

(c)

Fig.12. Vertical line detection templates and CNN (a) A template (b) B template

Under the control of two templates A and B, the CNN for the vertical line detection perform its function.

Another simple example of a Fixed-Template CNN is the horizon line detection. The operation of this CNN is very similar to that of the vertical line detection. The combination of CNN and two templates A and B is shown below.



0	0	0
1	2	1
0	0	0

(b)

0	0	0
0	0	0
0	0	0

(c)

Fig.13. Horizon line detection templates and CNN (a) A template (b) B template

2.3.2. Universal CNN

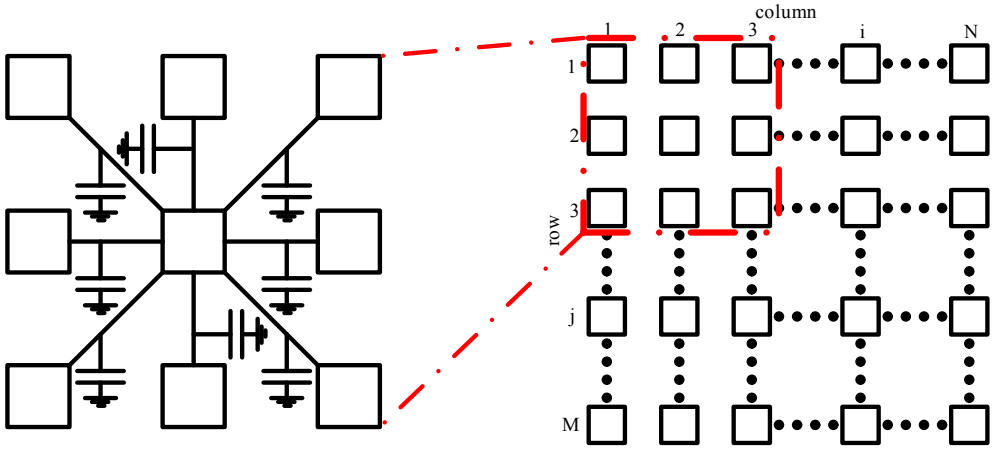
As demonstrated in the previous chapter, the weakest point of a Fixed-template CNN is in the limited operation. If the chip, having a Fixed-template, was developed on a chip level then the CNN chip could perform only one function intended by a developer. The chip for each function must be designed for CNNs required to perform multiple functions. Many researchers have been devoted to the development of a single CNN chip capable of performing multiple functions. A Universal CNN, which can

manage several functions including vertical and horizon line detection, connected component detection, hole filer, and shadow detection, was proposed to help achieve this goal. But before the Universal CNN can be fully utilized, one more component is required--an analog multiplier.

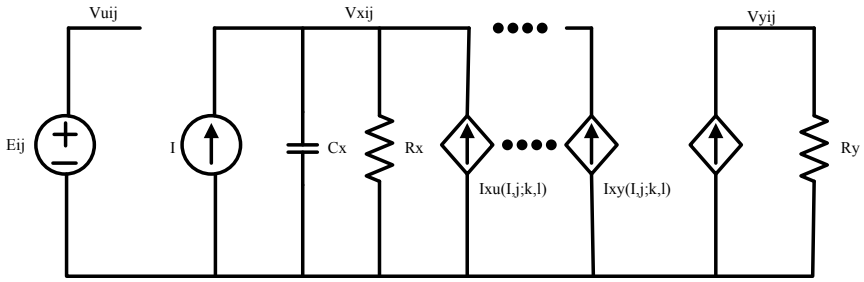
CHAPTER 3

ANALOG IMAGE RECOGNITION

In this work, analog image recognition arrays performing horizontal line recognition were demonstrated based on Cellular Neural Networks (CNNs) introduced in [9].



(a)



(b)

Fig. 14. (a) Standard CNN architecture. (b) CNN core cell

In Fig. 14(a), a square represents a CNN cell and the circuit of each cell C (i, j) is depicted in Fig. 14(b). The standard CNN cell includes several dependent current sources ($I_{xu(i,j;k,l)}$ and $I_{xy(i,j;k,l)}$), capacitor (C_x), and

resistors (R_x and R_y) [9]. The circuit of CNN core cell is modified to clarify the role of each component in a cell in Fig. 15. The capacitor C_u at the node of U (i, j) is used to conserve the value of the input voltage and the capacitor C_x is a state capacitor conserving the value of the state node X (i, j). The first dependent current source on the left side of Fig. 15 is a self-controlled source whose output current is generated by the input voltage of the unit cell itself and the weighting factor B. The second source is similarly controlled by the weighting factor A and the feedback voltage of the unit cell itself. The resistor R_x is a state resistor and determines the voltage at the node of X (i, j). The dependent current source at node Y (i, j) introduces an output current from a state voltage by the resistor R_x and is converted by the resistor R_y representing the final output of the unit cell.

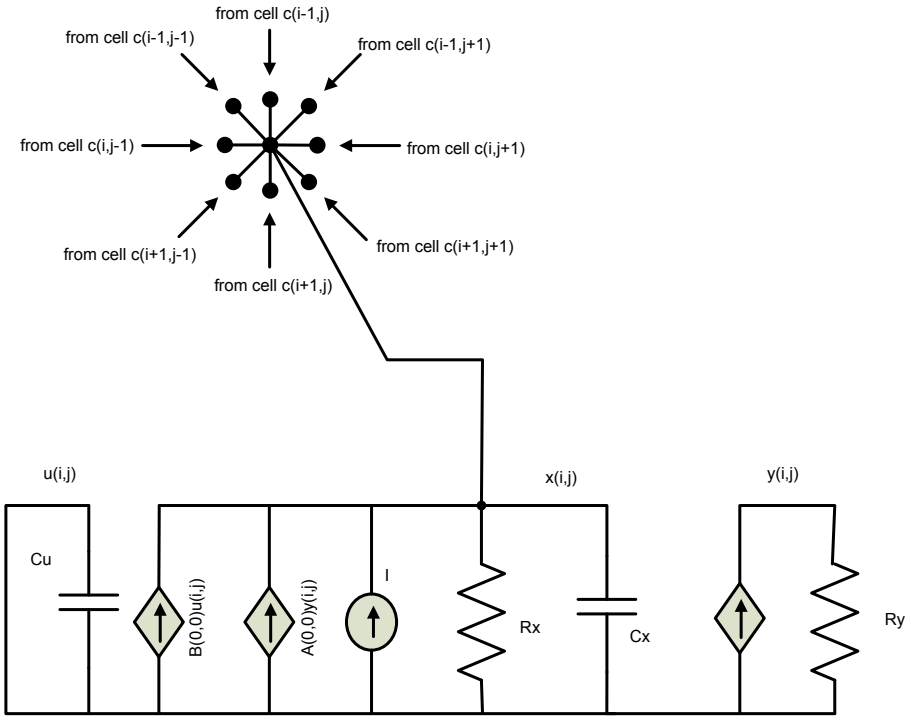


Fig. 15. The modified CNN core cell (Reprinted from [14])

The expressions for the currents of the dependent current sources in Fig. 14(b) are given as follow:

$$I_{xu}(i,j;k,l) = B(i,j;k,l) \times V_{ukl} \tag{1}$$

$$I_{xy}(i,j;k,l) = A(i,j;k,l) \times V_{ykl} \tag{2}$$

$$I_{yx} = \frac{1}{2R_y}\left(\left|V_{xij}+1\right| - \left|V_{xij}-1\right|\right) \tag{3}$$

The dynamics of each cell are expressed by the state equation.

$$\mathrm{C_x}\frac{\mathrm{dV_{xij}(t)}}{dt} = -\frac{1}{\mathrm{R_x}}V_{\mathrm{xij}}(\mathrm{t}) + \sum_{(k,l)\in S_r(i,j)} A(i,j;k,l) \times V_{ykl}(\mathrm{t}) + \sum_{C(k,l)\in S_r(i,j)} B(i,j;k,l) \times V_{ukl}(\mathrm{t}) + \mathrm{I} \tag{4}$$

The output of each cell is defined by a piecewise-linear.

$$V_{yij} = \frac{1}{2}(|V_{xij} + 1| - |V_{xij} - 1|) \quad (5)$$

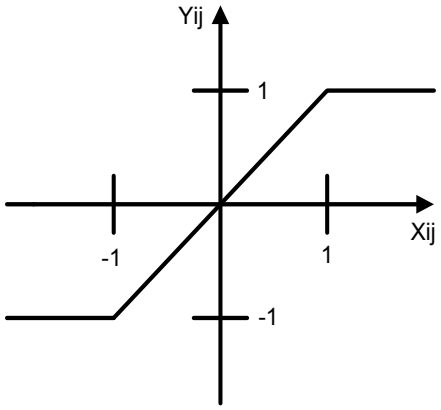


Fig. 16. The piecewise linear output transfer curve

In Equations (1) and (2), two operators, *A(i, j; k, l)* and *B(i, j; k, l)* are undefined. After investigating these equations, it is easily known that the two operators act like current weighting factors. In Equation (1), the input current (I_{xu}) is generated by weighting *B(i, j; k, l)* to the input voltage (V_{ukl}). More clearly, the input current of the cell located at (i, j) is driven by multiplying the weighting factor and the input voltage of the cell located at (k, l). The operator *A(i, j; k, l)* follows the same process for *B(i, j; k, l).* These operators are called templates. The B template is usually called a control template and the A template is a feedback template.

The implementation of a CNN circuit in a VLSI technology in [9] employed discrete elements like resistors and operational amplifiers. However, this approach is not suitable for implementing analog image

recognition arrays in a reasonable size. Thus a transconductance based model as shown in [14] is used here. This transconductance based operation of the CNN cell can be implemented by an Operational Transconductance Amplifier (OTA). As mentioned earlier a standard CNN cell includes several dependent current sources to demonstrate communication between cells. Also, a cell needs discrete elements such as resistors and capacitors. For the size of a CNN cell to be minimized, resistors were also implemented using OTAs as shown in Fig. 17. [20]

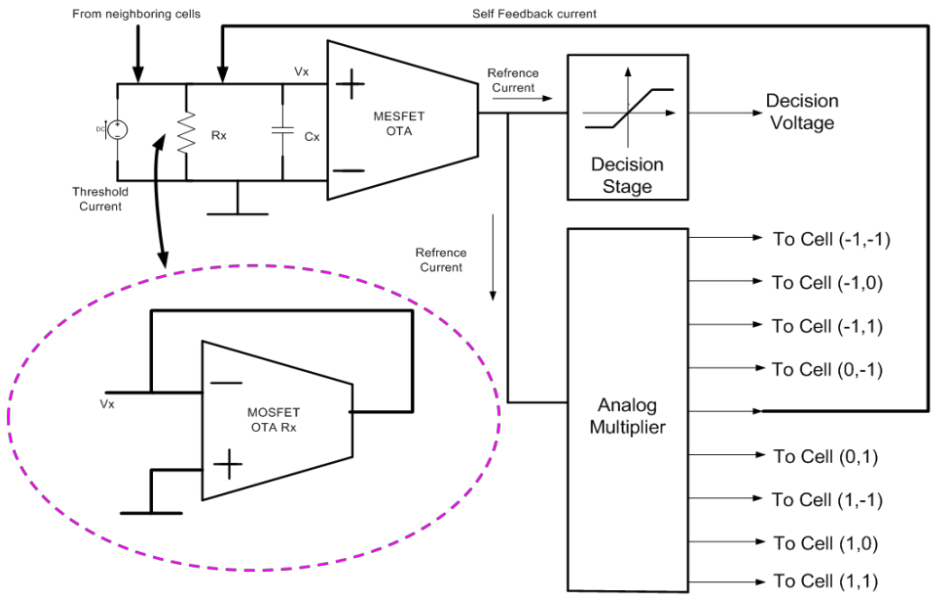
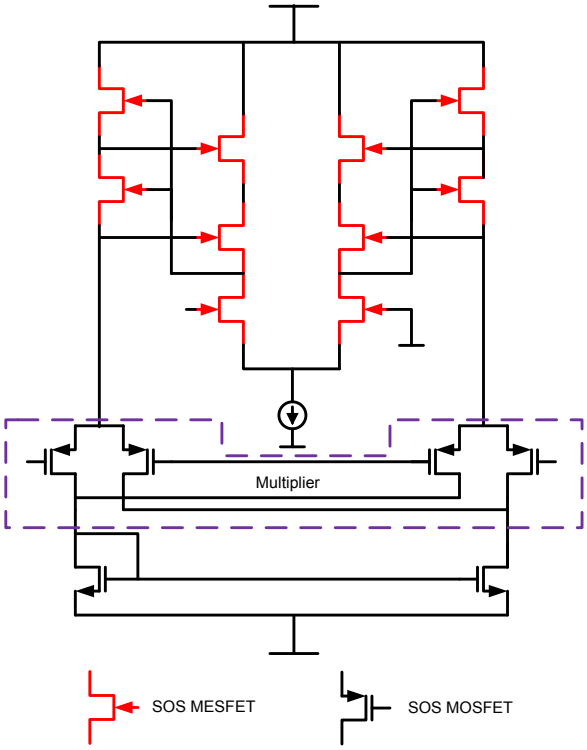


Fig. 17. The system level architecture of the proposed analog image processing

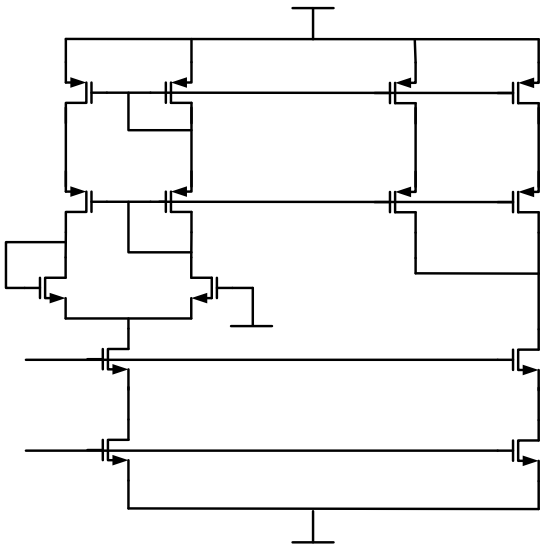
The function of a multiplier in Fig. 17 is the realization of templates by performing the multiplication of differential outputs from OTA-based

current sources in a CNN cell. The outputs of OTA-based dependent current sources are differential and become the inputs of a four-quadrant multiplier. The weighted currents from a cell are sent to the neighboring cells for intra-cell communication.

In this design, OTAs for dependent current sources are designed using MESFETs which are fully compatible to a current CMOS process. MOSFETs are employed in order to implement OTAs emulating discrete resistors. However, because a p-type MESFET was not available for this process flow, an n-type only design was used for the OTAs for dependent current sources. Schematics for both SOS MESFET-based OTAs and SOS-MOSFET based OTAs are depicted in Fig 18. The OTA for dependent current sources shown in Fig 18(a) includes an analog multiplier to adjust the transconductance of the OTA.



(a)



(b)

Fig. 18. (a) MESFET-based OTA with a multiplier for dependent current

sources. (b) MOSFET-based OTA for Rx.

Adjusting the transconductance by an analog multiplier allows CNN-based analog image recognition systems to perform a variety of CNN templates [9]. An analog multiplier is inserted into the OTA for dependent current sources in order to compare and contrast the cell implemented by both MESFETs and MOSFETs on a silicon-on-sapphire process. Fig 18(b) shows the configuration of the OTA for the resistor R_X. The resistor R_y is configured by the output resistance of the OTA for the resistor R_X. Details of OTAs for dependent current sources and discrete resistors have been described in [14].

CHAPTER 4

MEASUREMENT RESULTS

Analog image recognition arrays are implemented in one by four and one by eight arrays for the horizontal line recognition to verify full compatibility to the state-of-the-art CMOS process and accuracy of extracted DC characteristics of MESFETs with low power consumption. CNN-based analog image recognition systems are able to perform hundreds of image processing by adjusting templates using an analog multiplier as explained earlier [21], but in this work, the simplest image processing function (template) was chosen for simplicity. Each array was tested with grayscale images.

4.1. One by Four Array

The simplest CNN-based analog image recognition architecture is an array in one by four configuration as shown in Fig. 19.

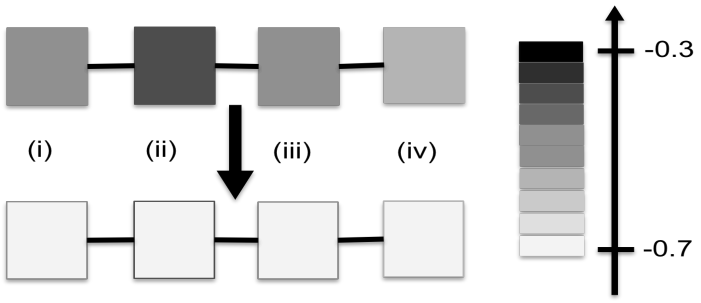


Fig. 19. Horizontal line detection in One by Four (a) input image (b) output image

One by four array was measured by applying several combinations of grayscale images at an image testing lab bench. Fig. 20 shows a micrograph of a one by four array for the horizontal line recognition. The CNN-based array for the horizontal line recognition has successfully been measured. Figures 21 and 22 shows the simulated and measured transient responses of the one by four array with grayscale input images. Each unit cell shows good agreement with the simulations using the extracted SOS MESFET model. The measured settling time is 4μs and 2.4μs for two different inputs in Fig. 21 and Fig. 22, respectively. Each unit cell consumes only 2.4mW of power.

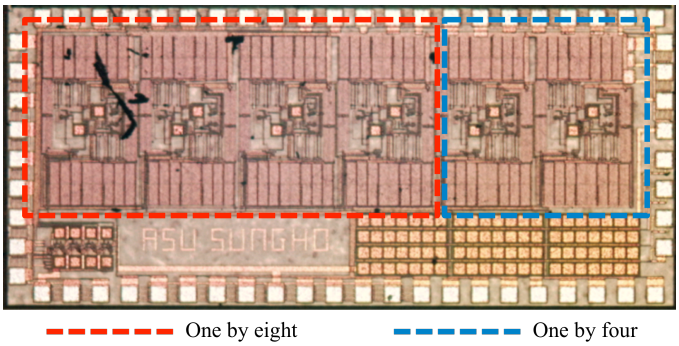
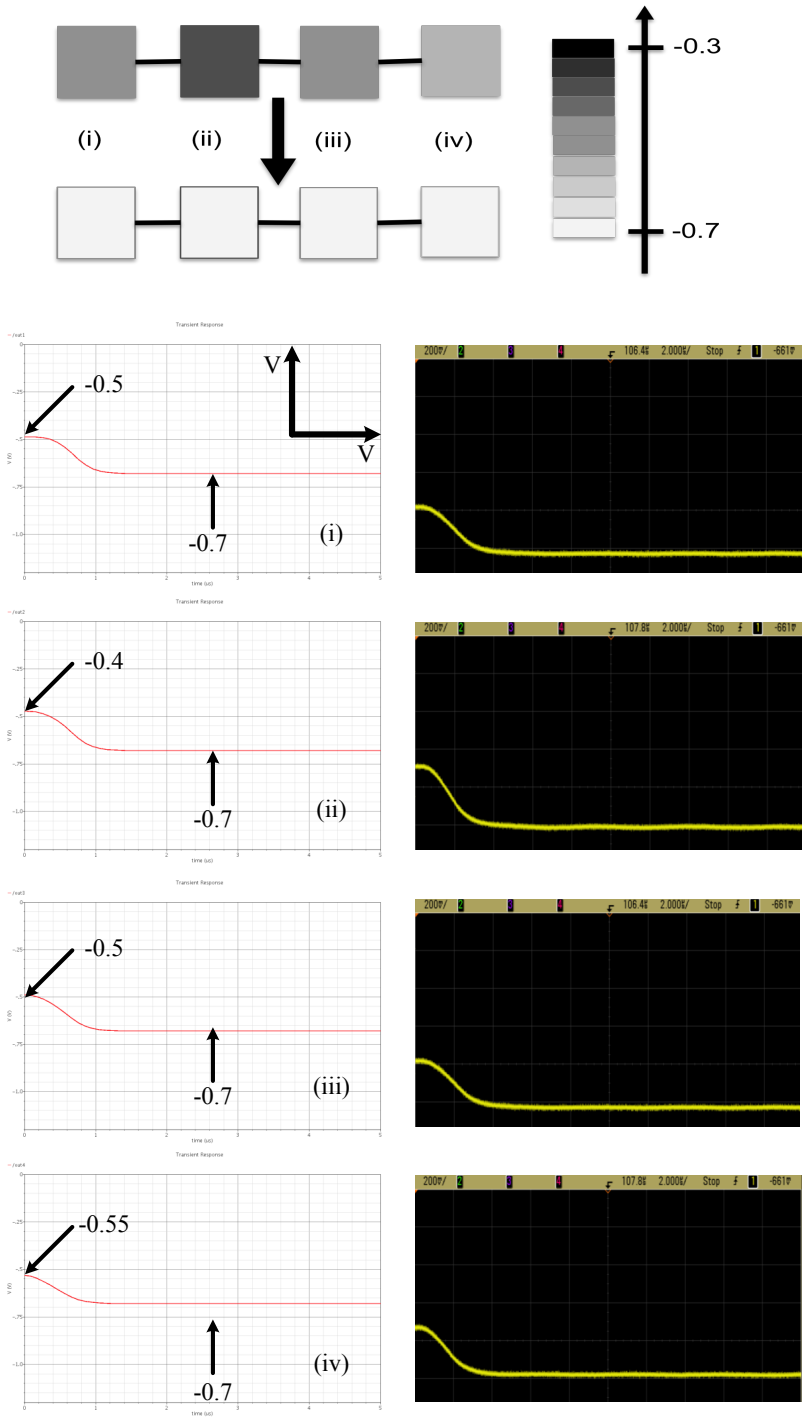


Fig. 20 Micrograph of CNN-based analog image processing arrays



(c) (d)

Fig. 21 (a) Input image (b) Output Image (c) Simulated output image (d)

Measured output image (200mV/div, 2μs/div)

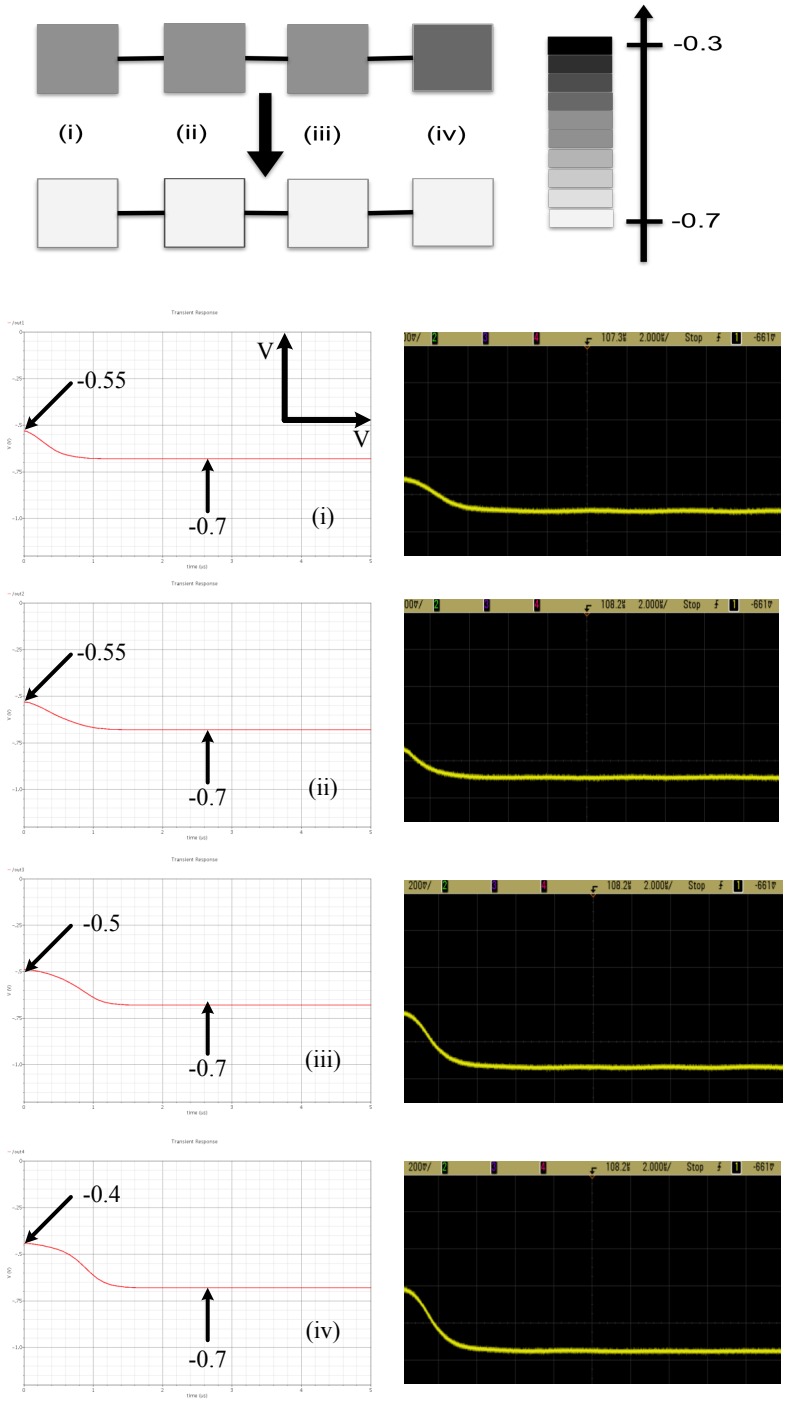


Fig. 22 (a) Input image (b) Output Image (c) Simulated output image (d) Measured output image (200mV/div, 2μs/div)

4.2. One by Eight Array

The one by eight CNN-based analog image recognition array is depicted in Fig. 23.

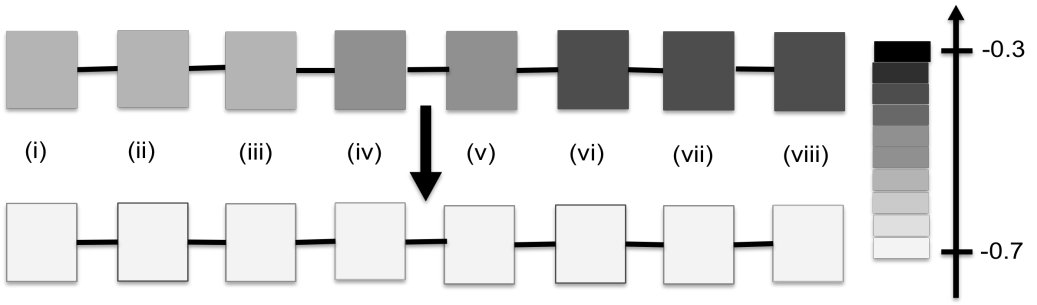


Fig. 23. Horizontal line detection in One by Eight (a) input image (b) output image

This array was measured with a grayscale input image as well. Fig 24 shows the simulated and measured transient responses of the one by eight array with grayscale input image. Good matching to the simulation using the extracted SOS MESFET model is verified again with the one by eight array. The measured settling time is 6μs. Each unit cell consumes only 2.4mW of power. A microphotograph of a one by eight CNN-based array is shown in a red-colored rectangular of Fig. 20.

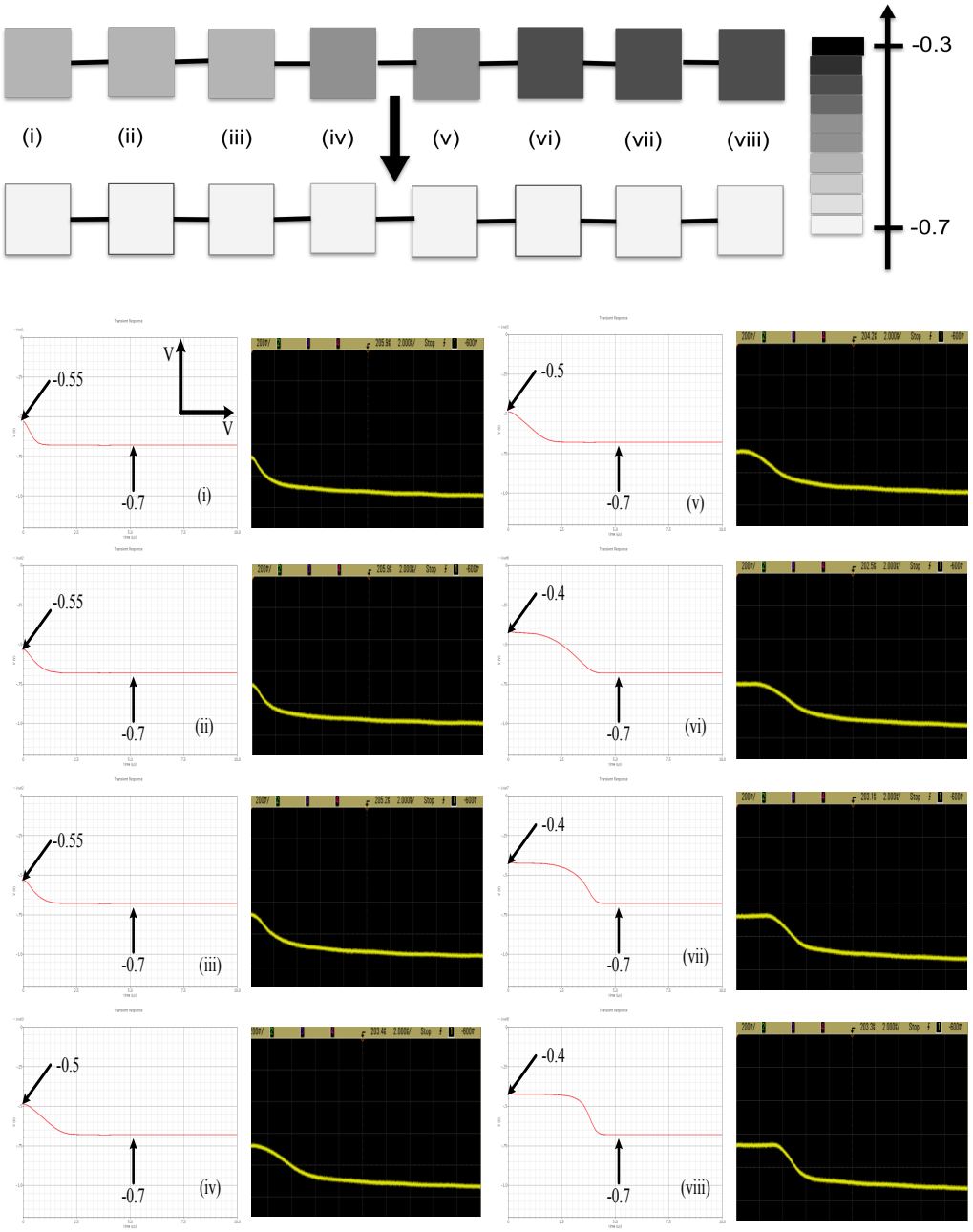


Fig. 24 (a) Input image (b) Output Image (c) Simulated output image (d) Measured output image (200mV/div, 2μs/div)

CHAPTER 5

CONCLUSION

Two CNN-based arrays are designed, fabricated and measured for high-speed, low-power image recognition systems. The arrays show good matching to extracted models for the grayscale images. The measured settling time is 4μs and 6μs for one by four and one by eight arrays with power consumption of 2.4mW for each cell. DC characteristics of n-MESFET devices fabricated using deep submicron CMOS technologies are quite accurate. Thus SOS MESFETs can be applied to high speed, low-power systems, for example, analog image processing systems.

PART III

CMOS LOW-POWER BFSK MICS TRANSCEIVER

CHAPTER 1

INTRODUCTION

For wireless connectivity providing the convenient and continuous health care to a patient within a limited range (~2m), Medical Implant Communication Service (MICS) and Body Channel Communication (BCC) have been arranged by FCC and widely adopted for implantable and wearable devices. Several implantable devices allowing for medical telemetry have recently been appeared in both commercial product lines [1] and research archives [2-5] with acceptable levels of reliability and performance. Implantable wireless health care systems, however, have faced a technical challenge associated with battery life. They must last over 5 years inside the human body without the possibility of recharging or replacing, which in turn requires the architectures of medical implants to be simplified as much as possible while being optimized to dissipate as little power as possible with reasonable performance. Various techniques have been proposed to deal with this challenge with life span of medical implants. A digitally controlled oscillator (DCO) using a sub-ranged, pre-distorted capacitor array is incorporated into the loop antenna as its inductive element. This approach achieves a wide tuning range, linear digital-to-frequency conversion, and high frequency resolution [3]. The unified transceiver concurrently operating in both MICS and BCC bands is introduced in [4], in which the on-body controller positions on a patient's skin allowing for the minimum detectable power of about -70dBm with sub-

mW power dissipation. In [5], reconfigurable RF front end contributes to the simplification of the transceiver architecture with an all digital frequency-locked loop (ADFLL) and the great reduction in power consumption in MICS band. In this paper, an energy efficient transceiver operating in MICS band (402 ~ 405MHz) with a binary frequency shift keying (BFSK) modulation for the data-link RX and on-off keying (OOK) for the wakeup RX is proposed. The folded LNA-Mixer is placed at the very front end of the data-link receiver to detect BFSK signals while realizing low power consumption. The MOS-C band-pass filter (BPF) filters out down-converted BFSK signals, followed by a continuous comparator generating a demodulated digital waveform. The SRO is used in a wakeup RX for the wake-up signal reception in order to remove the necessity of a local oscillator allowing for the reduction in a power dissipation. The all digital frequency-locked loop drives a class AB power amplifier in a transmitter and produce a non-linear BFSK output signals meeting the requirement of the FCC regulation.

The rest of the paper is organized as the followings. Section II introduces the system level operation of the proposed transceiver and in Section III techniques to address the low-power and low-voltage operation of the transceiver in a CMOS transistor level. Section IV presents the measured results of the proposed transceiver. Finally, conclusions are presented in Section V.

CHAPTER 2

TRANSCEIVER ARCHITECTURE

Fig. 1 shows the transceiver architecture which consists of a wakeup receiver (WRX), data-link receiver (DRX), and transmitter (TX) with an all digital frequency-locked loop (ADFLL). The detailed architecture of a WRX is introduced in Fig. 2 with the post-layout simulations at important nodes, consisting of a super regenerative oscillator (SRO), envelope detector (ED), and limiter (LIM).

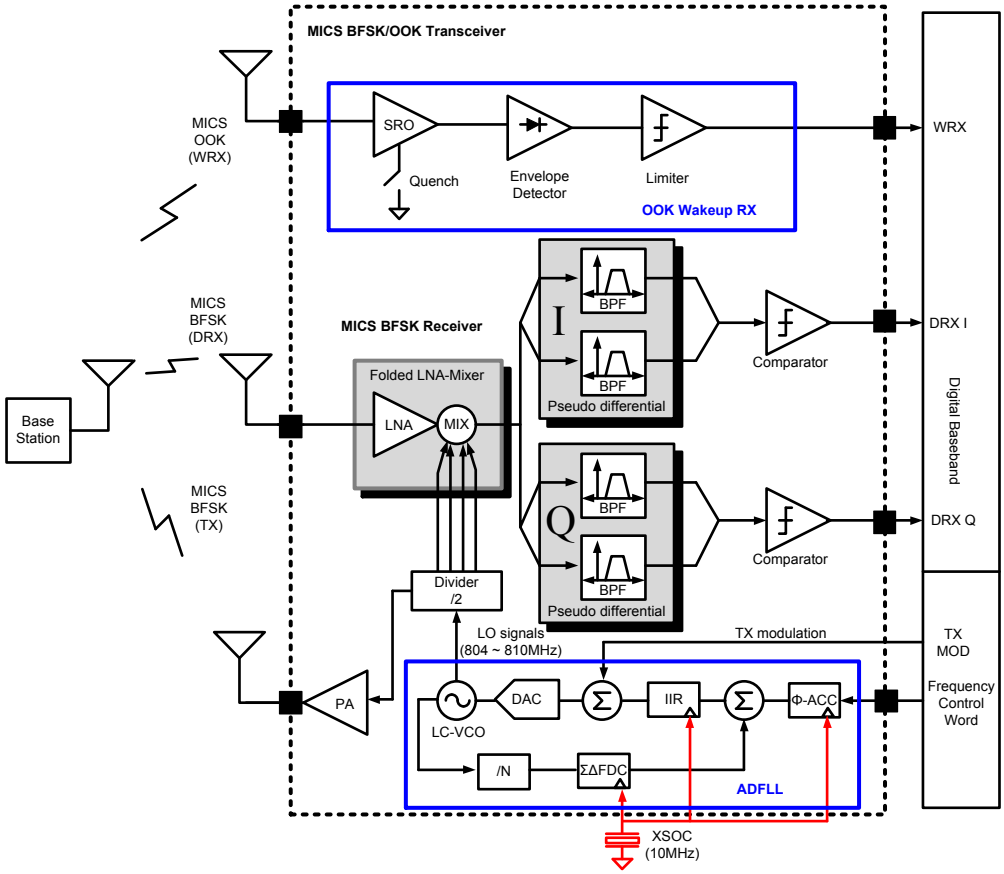


Fig.1. The block diagram of the proposed MICS transceiver

Fig. 1 shows the transceiver architecture which consists of a wakeup receiver (WRX), regular receiver (RX), and transmitter (TX) with an all digital frequency-locked loop (ADFLL).

The advantage of using a SRO is that a local oscillator can be omitted for reduction in the power consumption. Once the quench signal turns a SRO on, the oscillation envelope starts growing by the injected RF signals at an antenna and the envelope decays after the turning-off of the quench signal. The faster starting time of an oscillation envelope can be achieved as the injected signals are stronger because perturbation is proportional to the strength of the injected signals [6]. An envelope detector is operated in the sub-threshold region to minimize the power consumption. ED detects the peak amplitude of super-regenerated signals and filters out high frequency components in signals as well. A limiter at the back-end continuously demodulates the signals processed by ED for the reconstruction of the OOK modulated RF signals. The demodulated signals are sent to an external FPGA or PC for the further signal processing. The WRX achieves a sensitivity of -85dBm and a power consumption of 320μW at 100kb/s and -70dBm and 400μW at 200kb/s at 1MHz of the step controlled quench signal.

The data-link receiver (DRX) is comprised of a folded low-noise amplifier (FLNA) and mixer, band-pass filter (BPF) and comparator. MICS transceiver usually adopts either on-off keying (OOK) [2] or binary frequency shift keying (BFSK) modulation [3-5] for an energy efficient

design. The proposed RX chain adopts direct conversion BFSK modulation with the 150kHz offset because it offers better performance against interference than OOK [5]. The LNA is merged with the mixer in a folded configuration reusing the bias current. A typical MICS transceiver employs a passive mixer requiring a buffer stage to drive a transimpedance amplifier at the expense of extra current consumption [5]. The proposed LNA-Mixer configuration doesn't require a buffer stage reducing overall front-end power. The amplified, down-converted BFSK signals are filtered out by a MOS-C based G_m-C BPF with the center frequency of 150kHz. BPF is used here to relax the requirements of the DC offset and flicker noise instead of a low-pass filter (LPF) usually adopted in MICS RX chains. OTA-based G_m-C filters are widely used in conventional MICS RX chains at the expense of extra current consumption due to the common-mode feedback network (CMFB) to handle the effect of common-mode perturbations. The MOS-C based G_m-C BPF is pseudo differential so that the CMFB network is not necessary and it finally leads additional reduction in power consumption.

The sensitivities of -70dBm and -98dBm in the data-link RX are achieved with NF of 40dB and 11dB at the data rate of 100kb/s while consuming only 600μW and 1.5mW at 1.2V and 1.8V, respectively. The BERs of the data-link RX are less than 10^{-3} at the input powers of -70dBm at 1.2V and -98dBm at 1.8V at the data rate of 100kb/s.

The transmitter consists of an ADFLL and class AB power amplifier. The ADFLL operates as a MICS direct modulator in a data-link mode and drives a class AB power amplifier to produce the non-linear BFSK signals in a TX mode. The transmitter meets the requirement of the output power by 0dBm for a power consumption of 1.8mW from a 1.8V power supply [6].

CHAPTER 3

CMOS IMPLEMENTATION

3.1 Wakeup Receiver

The OOK modulated command signals, (A) in Fig. 2, are injected into gates of positively cross-coupled transistors M_1 – M_2 as shown in Fig. 3 and cause perturbation to push an oscillation envelope to build up faster than one in a stand-alone SRO super-regenerated by self noises. During a super-regenerative mode, a quench signal, (B) in Fig. 2, controls the conductance of the positive feed-back transistor pair. The sensitivity of SRO strongly relies on the waveform of a quench signal [7]. The step-controlled quench signal is externally generated and applied to the WRX in this design because of the great frequency selectivity. The cascoded two band-pass filters in Eq. 1 verifies the high selective frequency response of the step-controlled quench signal [7]. Following by the SRO, an envelope detector operating in the sub-threshold region extracts the envelope of regenerated signals by the SRO and a limiter generates demodulated digital waveforms.

$$F(\omega) = \frac{G_+/2C}{\sqrt{(G_+/2C)^2 + (\omega - \omega_o)^2}} \frac{|G_-|/2C}{\sqrt{(G_-/2C)^2 + (\omega - \omega_0)^2}} \quad (1)$$

In this equation, G+ is positive conductance of a LC resonator, G- negative conductance of an active device (M_1 and M_2). C is capacitance in a LC resonator.

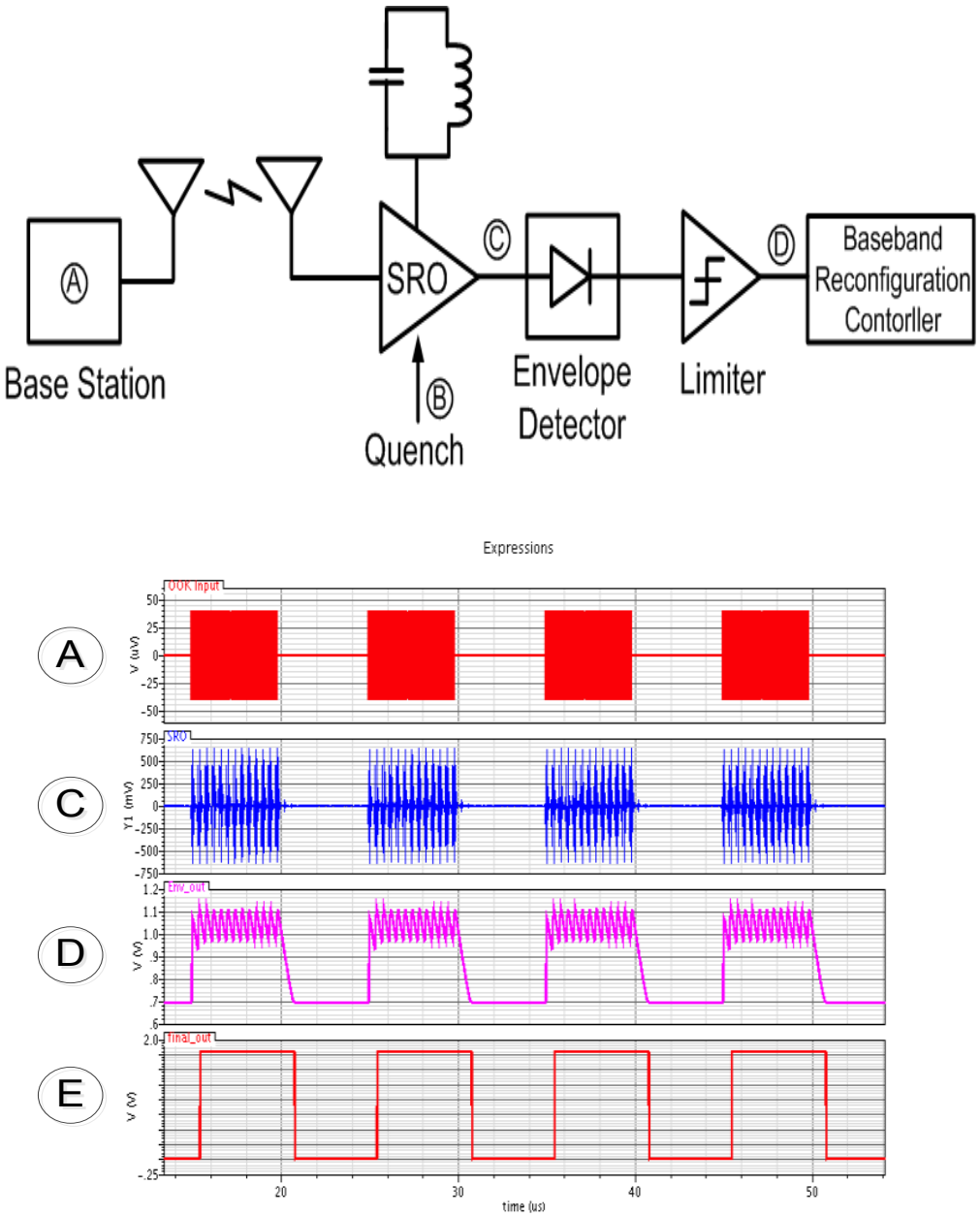


Fig. 2 The detailed schematic and waveforms at important nodes

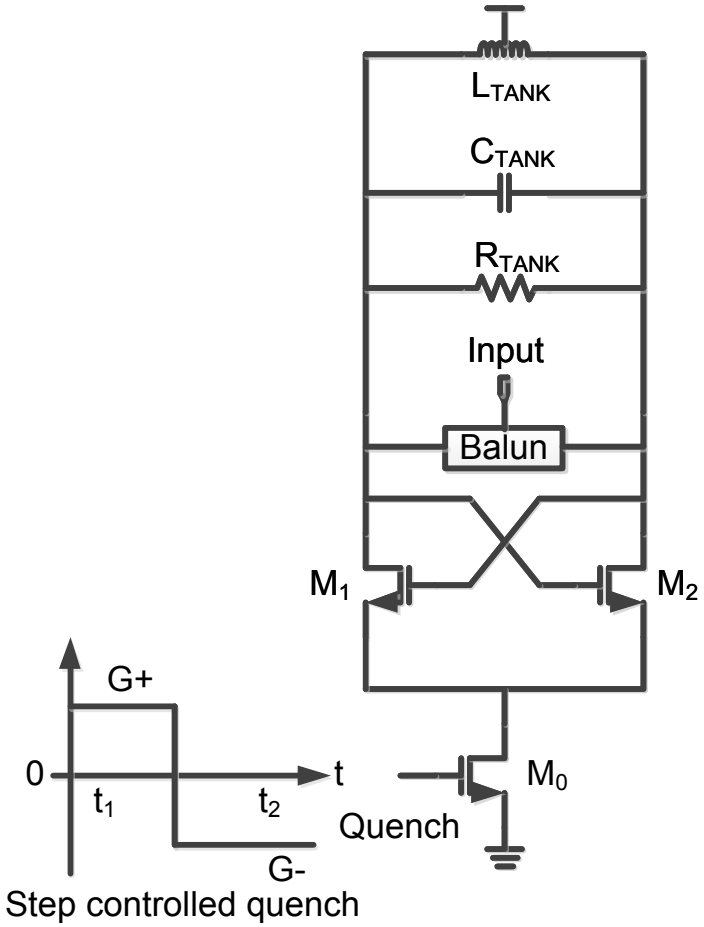


Fig. 3 The schematic of a super regenerative oscillator with a step controlled quench signal.

3.2. Folded LNA-Mixer

Fig. 4 shows the detailed schematic of the proposed fully differential folded LNA and quadrature mixer. The mixer is merged into common-gate (CG) LNA to reuse the bias current and the amplified input signals are converted into voltage quantities through the resistive mixer loads. The folded configuration of the proposed LNA-Mixer allows for high

linearity in a wide range of power supply. And it also enables a low power operation of the proposed DRX at low power supply voltages (below 1.2V). The performance of the DRX in various aspects are measured and presented in Section IV in more detail. The cross-coupled capacitors (C_1 and C_2) are inserted between gates and sources of devices M_1 and M_2 to increase the effective transconductance (G_{eff}) of GC-LNA with low DC bias currents [8]. The small signal resistance looking into M_1-M_3 and M_2-M_4 is much larger than that of a load of the LNA so that contribution of the load resistance to the input matching can be ignored. The small-signal half circuit model is drawn in Fig. 5 and the input matching is analyzed as the following.

$$Z_{IN} = sL_{IN} + \frac{1}{sC_{IN}} + \frac{sL_S}{sL_S(sC_S + G_{eff}) + 1} \tag{2}$$

At the resonant frequency, the imaginary part of the input impedance is cancelled and Eq. 2 becomes

$$R_{IN} \approx \frac{1}{G_{eff}} \tag{3}$$

$$G_{eff} = (1 + C_C / (C_C + C_{gs1,2}))g_{m1,2} \tag{4}$$

In equations above, L_{IN} is the inductor and C_{IN} the capacitor of the external matching network. L_S is the source degenerated inductor and $g_{m1,2}$ is the transconductance of the input pair. Lastly, C_C is the cross-coupled apacitors for enhancement in the effective transconductance of the LNA

and $C_{gs1,2}$ is the gate-source capacitance of the input transistors, M_1 and M_2.

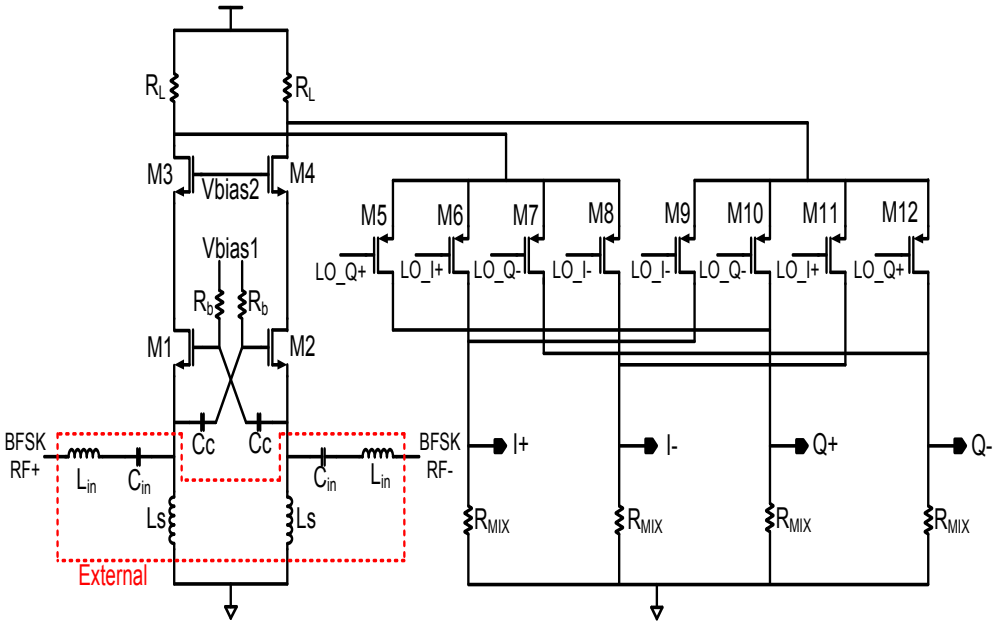


Fig. 4 Proposed folded LNA and Mixer

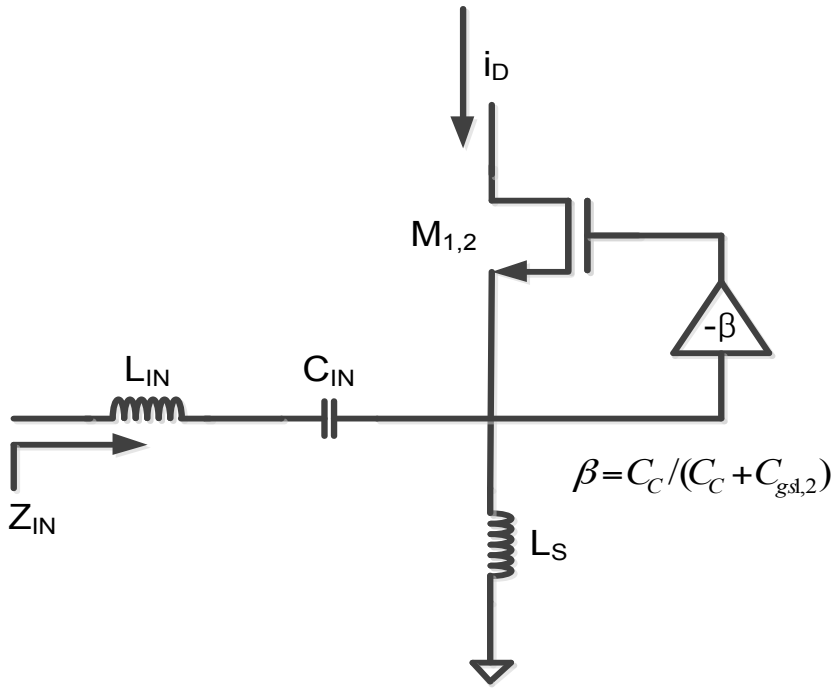


Fig. 5 Small-signal half circuit model of the proposed LNA for input matching

3.3. Channel-Selection Filter

In this design, pseudo differential all MOS-C based G_m-C BPFs are used to take both power efficiency and simple realization of ICs into account at the expense of mismatches in I and Q channels due to the absence of the CMFB network. The pseudo differential design allows for low supply voltage and low power consumption. The detailed schematic is depicted in Fig. 6. The G_m-C integrator is realized by a transconductor M_1, capacitor C_1, and a bias device M_4 [9]. Source degenerated devices, M_4 – M_6, are placed to enhance immunity to non-linearity [10]. The filter is

designed for a center frequency of 150kHz for ±150kHz-offset BFSK and tuned by a capacitor bank. The frequency response of the BPF is shown in Fig. 7 and the tuning range of frequency is from 70kHz to 250kHz with a 3dB gain.

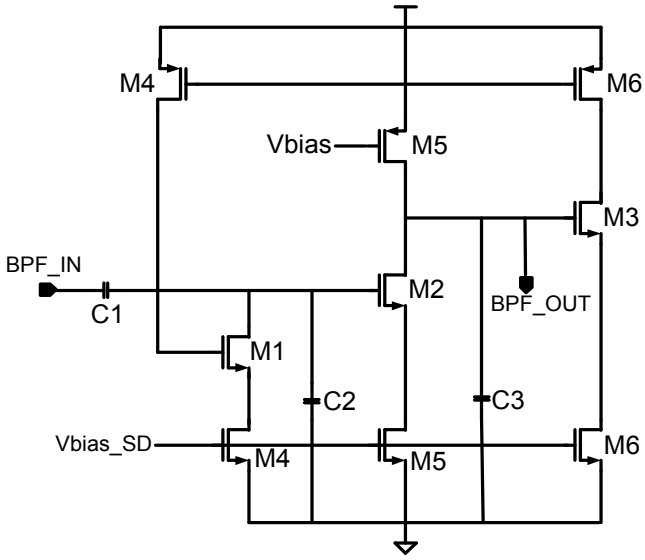


Fig. 6 The pseudo differential BPF with degenerations.

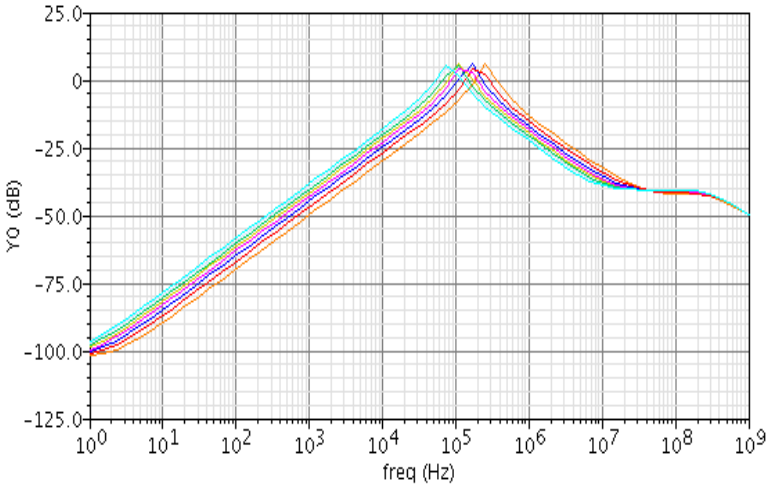


Fig. 7 Frequency response of the pseudo differential BPF. The tuned frequency ranges 70kHz to 250kHz with a 3dB gain.

The ADFLL operates as a MICS direct modulator and drives a class AB power amplifier for a nonlinear output amplifier.

The LC-VCO is fully implemented for the better phase noise. The output power is about -16dBm satisfying the FCC regulation. The phase noises of ADFLL are -70dBc, -95dBc, and -110dBc at 10kHz, 100kHz, and 300kHz offsets at various control voltages as shown in Fig. 8.

3.4. Transmitter with ADFLL

The ADFLL consists of a type-I phase-locked loop (PLL) scheme as shown in Fig. 1. The features of the ADFLL are (i) all digital implementation, (ii) programmable loop bandwidth, and (iii) fast locking [11]. The ADFLL operates as a MICS direct modulator and drives a class AB power amplifier for a nonlinear output amplifier. The LC-VCO is fully implemented for the better phase noise. The output power is about -16dBm satisfying the FCC regulation. The phase noises of ADFLL are -70dBc, -95dBc, and -110dBc at 10kHz, 100kHz, and 300kHz offsets at various control voltages as shown in Fig. 8.

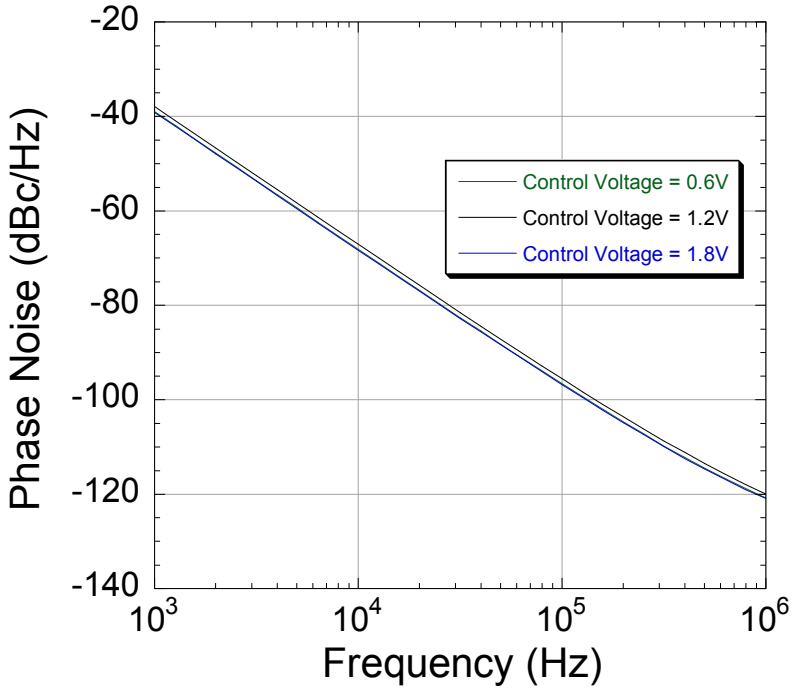


Fig. 8 The phase noise of ADFLL at various control voltages of 0.6, 1.2, and 1.8V.

CHAPTER 4

EXPERIMENTAL RESULTS

The MICS transceiver was fabricated in a 0.18μm 1-poly, 6-metal CMOS process and the active chip area is 9mm^2. The microphoto of the chip is shown in Fig 9. The average active power consumption is about 480μW and 600μW of the LNA+MIX and RX from a 1.2V power supply, respectively. The NF is less than 40dB at 1.2V achieving the minimum detectable signal level of -70dBm [4, 5]. This sensitivity is acceptable power level when the implanted devices communicate with an on-body controller within the limited communication range (~1m) [4]. The return loss of the folded LNA-Mixer at various power consumptions is measured and presented in Fig 10. The NF and voltage gain at various power consumptions are displayed in Fig 11. The achieved voltage gain of the folded LNA-Mixer and RX chain are 35dB and 51dB at the power supplies of 1.2V and 1.8V, respectively, while 11dB and 14.6dB for the folded LNA-Mixer at the same power supplies. The average NF is about 40dB and 11dB at 1.2V and 1.8V, respectively which means, in other words, the minimum detectable signal powers are -70dBm and -98dBm at 1.2V and 1.8V, respectively. Fig 12 shows measured digital waveforms at I and Q with 150kHz-offset BFSK RF signals with the carrier frequency of 400MHz at the input power of -85dBm. I channel leads Q channel by 90° when +150kHz-offset RF signal is detected at the front-end of the receiver chain and I lags Q by 90° in -150kHz-offset.

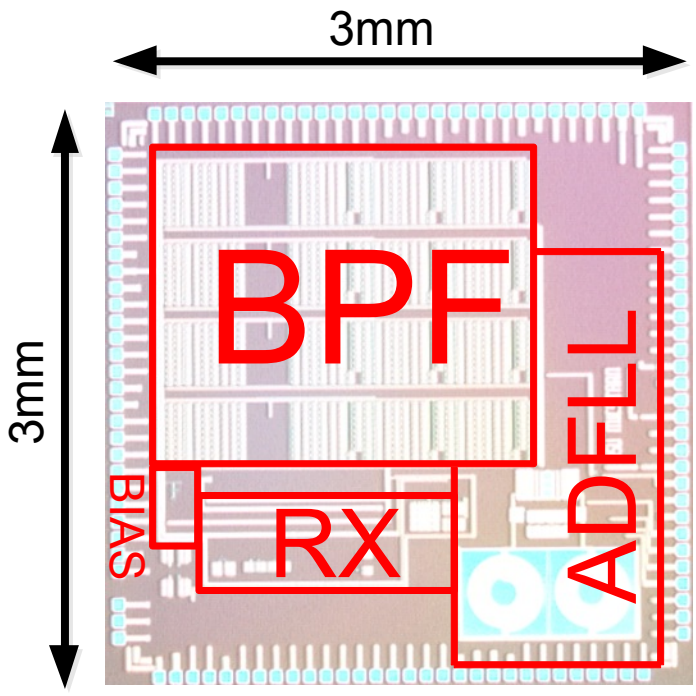


Fig. 9 Microphoto of the MICS transceiver in 1-poly, 6-metal 0.18μm CMOS.

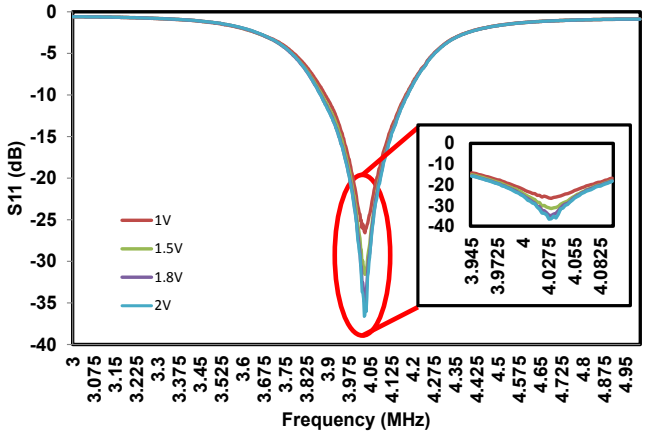


Fig.10 The input return ratio (S11) at various power supplies.

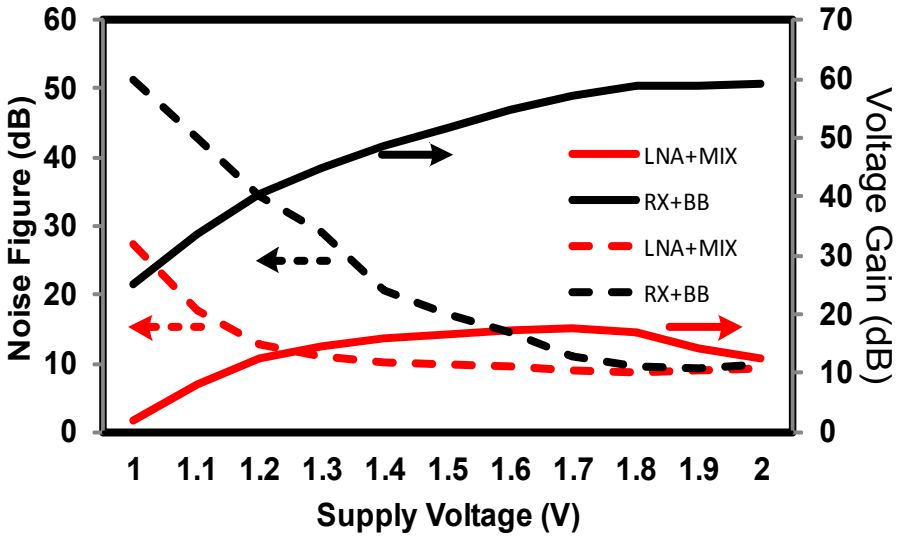


Fig. 11 Measured voltage gain and noise figure at various power supplies.

The WRX was measured by injecting OOK modulated signals of 400MHz at various data rates and quench frequencies and the measured demodulated waveforms are presented in Fig. 12. The sensitivities of -85dBm and -70dBm are achieved at the data rates of 100kb/s and 200kb/s with 1MHz of the step controlled quench signals, respectively. At the quench of 1.2MHz, the WRX achieves sensitivities of -68dBm and -60dBm at data rates of 100kb/s and 200kb/s, respectively.

Finally, the performance of the transceiver is summarized in Table I. In Table II, the performance of the proposed MICS transceiver is compared with the previous works at various aspects.

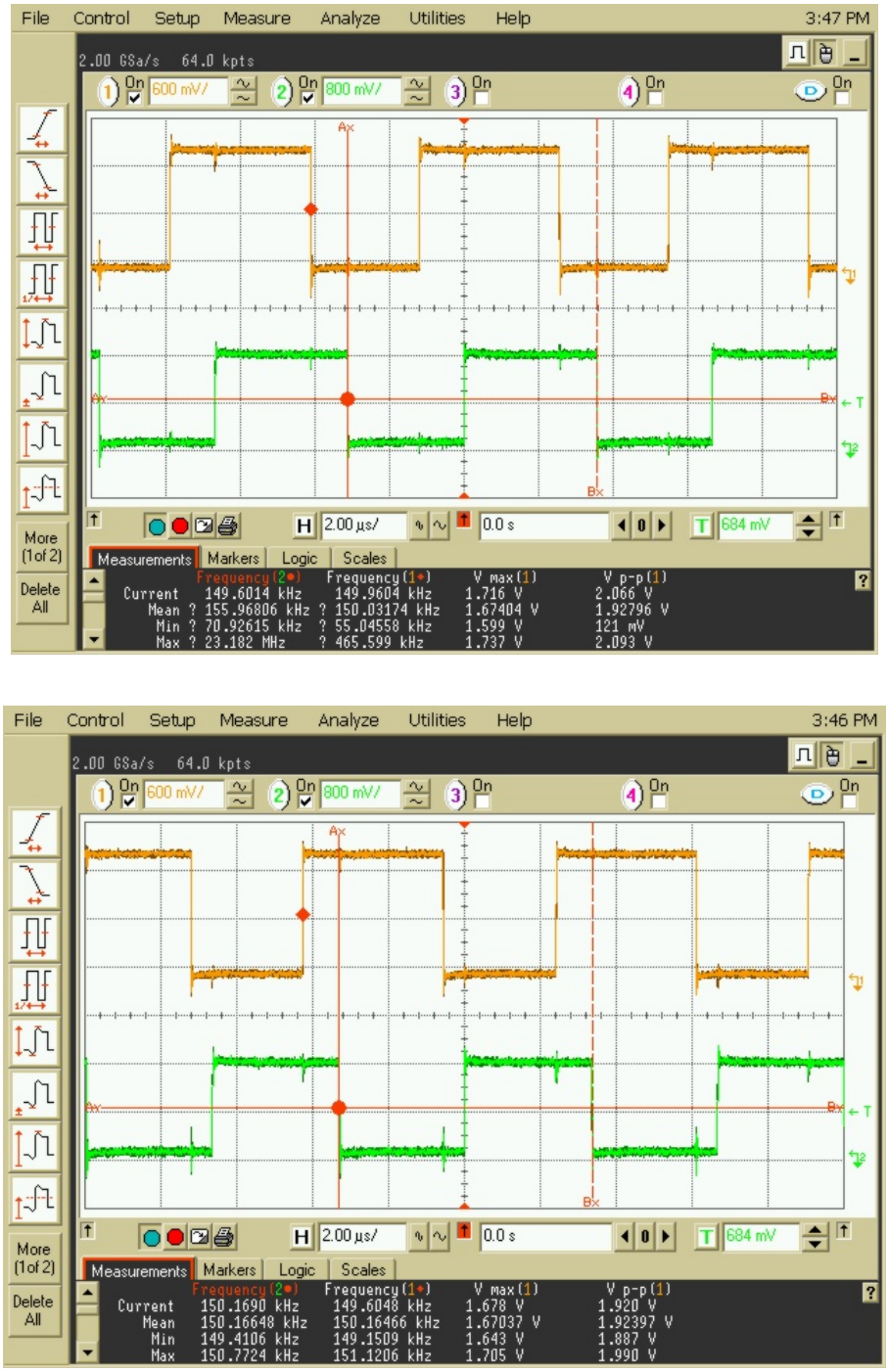


Fig. 12 Measured digital streams of the data-link receiver (i) I channel (top) and (ii) Q channel (bottom) at 400MHz BFSK.

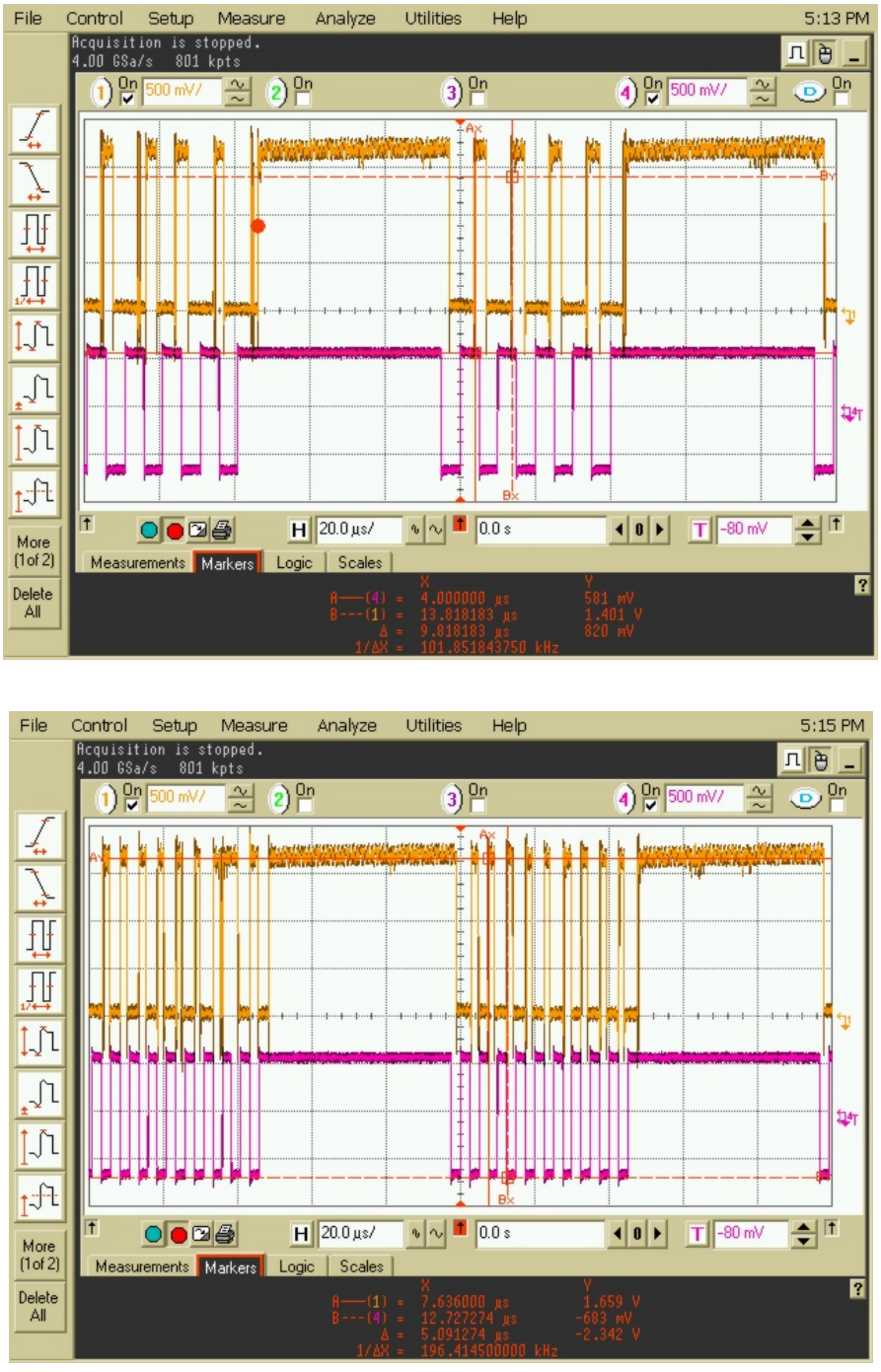


Fig. 13 Measured digital streams of the wakeup receiver (i) 100kb/s (top) and (ii) 200kb/s (bottom) at 1MHz .

TABLE I

SUMMARY OF THE TRANSCEIVER

Technology	0.18μm 1-poly, 6-metal CMOS	
Operating Frequency	402MHz – 405MHz	
Modulation	OOK for WRX BFSK for DRX	
Data Rate	100 kb/s to 200 kb/s for WRX 100 kb/s for DRX	
Sensitivity @ 10^{-3} BER	WRX*	-85dBm @ 100kb/s -80dBm @ 150kb/s -70dBm @ 200kb/s
	DRX	-70dBm @ 1.2V (NF = 40 dB) -89dBm @ 1.5V (NF = 20 dB) -98dBm @ 1.8V (NF = 11 dB)
Supply Current	WRX *	180μA @ 100kb/s 200μA @ 150kb/s 225μA @ 200kb/s
	DRX#	500μA @ 1.2V 630μA @ 1.5V 840μA @ 1.8V
Voltage Gain, RF+BB	35 dB @ 1.2V 44 dB @ 1.5V 51 dB @ 1.8V	
Voltage Gain, LNA+Mixer	11 dB @ 1.2V 14.3 dB @ 1.5V 14.6 dB @ 1.8V	

*1.8V power supply and 1MHz; #: excluding ADFLL

TABLE II

SUMMARY OF THE PERFORMANCE COMPARISON

	Parameter	This work	[3]	[4]	[5]
RX	Modulation	BFSK	OOK	BFSK	BFSK
	Sensitivity	-98dBm	-93dBm	35μVrms	-97dBm
	Data Rate (kb/s)	100	120	50	75
	Power Consumption (mW)	1.44* (1.2V) 2.5* (1.8V)	0.4	4.3 (PLL+BB)	2
TX	Modulation	BFSK	MSK	BFSK	BFSK
	Data Rate (kb/s)	100	120	200	100
	Power Consumption (mW)	1.8	0.35	4.3	1.6
	Output Power (dBm)	-16	N/A	0	-5

*: including ADFLL

CHAPTER 5

CONCLUSION

A low-power CMOS transceiver for the MICS band has been fabricated and measured in a 1-poly, 6-metal 0.18μm CMOS process. The folded LNA-Mixer configuration and MOS-C based G_m-C BPF allow for a low-voltage and low-power operation under the limited power capacity. The DRX chain shows -98dBm sensitivity with a 100kb/s and consumes only 2.5mW from a 1.8V power supply while shows -70dBm sensitivity and 1.44mW from a 1.2V power supply.

The sensitivity of -85dBm in the wakeup RX is achieved with the power consumption of 200μW from 1.8V at the data rate of 100kb/s and 220μW at 200kb/s with the 1MHz step controlled quench signals. This work demonstrates that implantable wireless devices such as Pacemakers consuming a sub-mA with reasonable performance can be designed.

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BIOGRAPHICAL SKETCH

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