Programmable Metallization Cell Devices for Flexible Electronics

by

Sunil Baliga

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Graduate Supervisory Committee:

Michael Kozicki, Chair
Dieter Schroder
Junseok Chae
Terry Alford

ARIZONA STATE UNIVERSITY

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ABSTRACT

Programmable metallization cell (PMC) technology is based on an electrochemical phenomenon in which a metallic electrodeposit can be grown or dissolved between two electrodes depending on the voltage applied between them. Devices based on this phenomenon exhibit a unique, self-healing property, as a broken metallic structure can be healed by applying an appropriate voltage between the two broken ends. This work explores methods of fabricating interconnects and switches based on PMC technology on flexible substrates. The objective was the evaluation of the feasibility of using this technology in flexible electronics applications in which reliability is a primary concern.

The re-healable property of the interconnect is characterized for the silver doped germanium selenide (Ag-Ge-Se) solid electrolyte system. This property was evaluated by measuring the resistances of the healed interconnect structures and comparing these to the resistances of the unbroken structures. The reliability of the interconnects in both unbroken and healed states is studied by investigating the resistances of the structures to DC voltages, AC voltages and different temperatures as a function of time. This work also explores replacing silver with copper for these interconnects to enhance their reliability. A model for PMC-based switches on flexible substrates is proposed and compared to the observed device behavior with the objective of developing a formal design methodology for these devices. The switches were subjected to voltage sweeps and their resistance was investigated as a function of sweep voltage. The resistance of the switches as a function of voltage pulse magnitude when placed in series with a resistance was

also investigated. A model was then developed to explain the behavior of these devices. All observations were based on statistical measurements to account for random errors.

The results of this work demonstrate that solid electrolyte based interconnects display self-healing capability, which depends on the applied healing voltage and the current limit. However, they fail at lower current densities than metal interconnects due to an ion-drift induced failure mechanism. The results on the PMC based switches demonstrate that a model comprising a Schottky diode in parallel with a variable resistor predicts the behavior of the device.

This dissertation is dedicated to my parents Dr. M. R. Baliga and Mrs. Bina Baliga, and my younger brother Sankarshan.

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INTRODUCTION

Programmable Metallization Cell (PMC) technology is based on an electrochemical phenomenon in which the application of a voltage between two electrodes fabricated on a solid electrolyte results in either the growth or dissolution of a metal filament between the two electrodes [1]. This technology has been used to fabricate memories [1-5], capacitive elements [6], and memory elements on flexible substrates [7]. The myriad applications that this versatile technology has been applied to, prove its robustness. Another potential area of research for PMC technology is its use in mechanically demanding applications. Such applications arise when the associated electronic circuits are subjected to extreme physical conditions like bending and torsion during routine operation in wearable electronics and flexible displays, or in cameras, laptops and other portable equipment where the bending of these circuits occurs during manufacture in order to improve packing density. The fabrication of PMC circuit elements that are capable of withstanding these conditions is feasible because the thin films that comprise the device, namely, the solid electrolyte films which are generally chalcogenide glasses and the metal films, are very flexible [8].

Interconnects are metal lines that are used to connect different circuit elements or sub-modules of the integrated circuit (IC) together. These lines carry currents from one point of the circuit to the other. As applications for ICs get more diverse and demanding, the specifications for the interconnects become more challenging to meet. The earliest issues encountered were directly related to the scaling of IC process technology. As semiconductor device technology was

scaled, interconnects needed to carry correspondingly greater current densities. The most direct consequence of scaling was, therefore, power dissipation in the interconnect due to joule heating and subsequent failure of the interconnect due to accelerated electromigration [9-11]. Electromigration is a phenomenon in which the electrons comprising the current would transfer their momentum to the atoms comprising the interconnect, resulting in their movement and causing the interconnect to eventually fail. Both of these problems were resolved primarily by replacing the material that was used to fabricate the interconnect [12]. The current area of focus in the electronics industry is the development of ubiquitous computing devices and networks. These applications include wearable computers [13, 14] and devices [15], body area networks, flexible devices [16, 17] and portable devices [18, 19]. The ability of such electronics to withstand mechanical stress, while being able to reconfigure itself for optimum performance simultaneously, is an implicit specification. This work focuses on demonstrating that PMC technology is capable of fabricating robust interconnects that can withstand a very high degree of mechanical stress, and switches that perform well in flexible electronics applications. Furthermore, in the case of fracture of such an interconnect, this work demonstrates that the interconnect can be healed by simply applying an appropriate voltage for a small amount of time, thus restoring the circuit to normal operating conditions. This work also proposes a circuit model for a PMC based switch on a flexible substrate and demonstrates that it predicts actual device behavior accurately.

BACKGROUND AND REVIEW

This section provides a developmental perspective of interconnect technology. Some novel interconnect fabrication principles, specifically designed for flexible substrates, are discussed. A review of properties for materials that would make them good substrates for flexible electronics applications is also presented. The evolution of PMC technology is also discussed, along with the electrochemical and fabrication principles which form the basis of this technology. The mechanical properties of some of the solid electrolyte systems are presented to justify their use in flexible electronics applications. A discussion on the property of memristance is presented to develop a background for the analysis of the PMC switch as a memristive system.

A. The evolution of interconnect technology

Interconnects are metal lines which are used to connect different devices and sub-modules on an IC in a pre-determined path in order to ensure that the circuit performs a specific function. From a manufacturing perspective, the IC interconnect is fabricated by first lithographically patterning the required interconnect layout and then selectively depositing thin films of the chosen metal. In the early days of IC manufacturing, this was arguably one of the simplest processes in IC manufacture, as metal deposition and lithography were far in advance of transistor design and processing. However, with advances in transistor technology in order to keep up with IC scaling, interconnect performance in beginning to define the performance of the IC. The issues which interconnects face include compatibility with the new materials that are going into IC

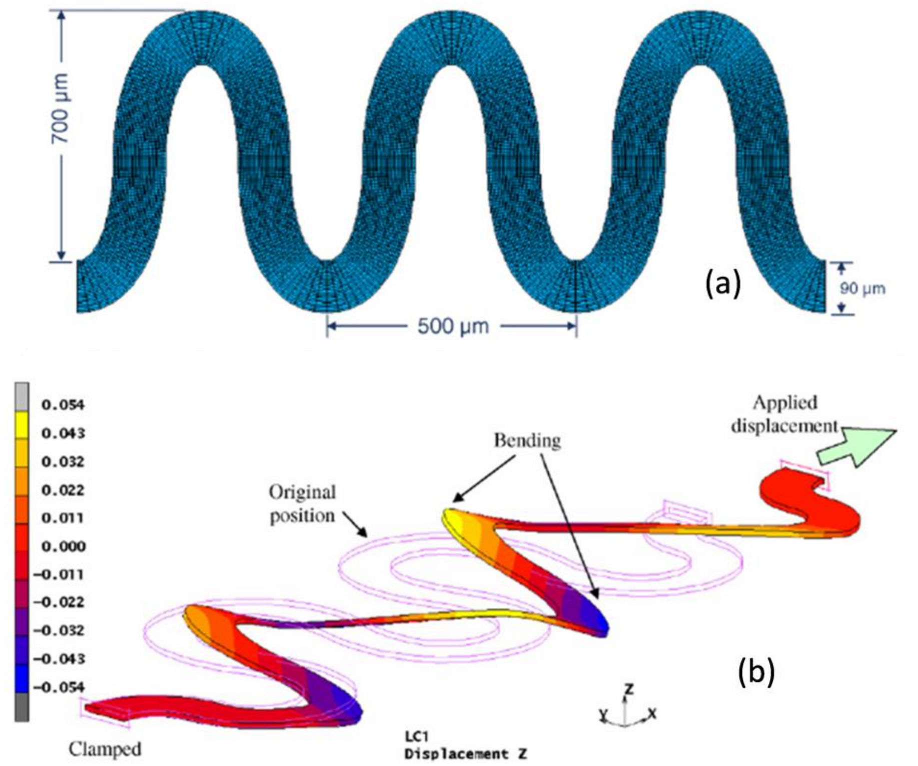


Fig. 1. (a) One of the possible optimized horseshoe-shaped interconnects that can withstand longitudinal strain on the substrate. (b) Mechanical behavior of the Cu-based horseshoe shaped interconnect when subjected 20 % out-of-plane longitudinal strain [39]

manufacture and reliability of the interconnects when subjected to increasingly high current densities during scaling. The higher current densities result in increased heat dissipation within the IC and also a higher probability of the onset of electromigration [20, 21]. These reliability issues were ameliorated by changing the interconnect material in the sub-100 nm nodes from aluminum (Al) [20-22] to copper (Cu) [23, 24]. The change in interconnect material improved the interconnect reliability and performance drastically. However, Cu is incompatible with silicon dioxide (SiO_2) and silicon (Si), since its diffusivity in both materials

is high [25, 26]. The presence of copper in silicon devices increases leakage current [25] and reduces the quality of dielectric films [26], reducing the lifetime of the circuit. In order to ensure that the entire IC is reliable, a material needed to be found which would act as a diffusion barrier between the Cu interconnect and the underlying Si or SiO_2 layer. Additionally, this layer needed to have excellent adhesion to the underlying layer and also capable of being deposited in the form of thin films. Many materials may be used for this purpose like titanium nitride (TiN) [27], tungsten nitride [28] and and tantalum nitride (TaN) [29]. The resulting process is known as the dual-damascene process [30]. Another reliability issue with interconnects has been delay through the line. A combination of the interconnect metal line and the inter-layer dielectric (ILD) produces a transmission line with distributed resistances and capacitances, which results in a delay through the line. With scaling, the values of the resistances and the capacitances have increased, resulting in the delay of the interconnect line now being comparable to the delay through the transistor itself. This results in the speed of the IC being limited more by the interconnect delays than by the delays associated with the transistors [31, 32]. In order to reduce delay, Cu interconnects with a low-k dielectric for the ILD have been used. However, the dual-damascene process is not compatible with the proposed ILDs and numerous integration challenges are presented when moving to the new ILD which include the mechanical and electrical instability of the material [33]. At present, no single, standard process exists for integrating the dual-damascene process with the low-k dielectric [32, 33]. Scaling trends continue to place demands on the material used

for the interconnect. Research has trended toward using Ag as a material for fabricating interconnects [34], as it has the highest electrical conductivity at room temperature, can be electroplated and produces films with low residual stress [34]. However, significant challenges remain with integrating Ag as an interconnect material. The most important factors are its very high rate of corrosion [34, 35] and its poor adhesion to most materials used in IC manufacturing processes [35].

The recent trend of the electronics industry to manufacture portable devices has produced significant challenges in the field of IC manufacture and reliability. The requirements of portability include small size, light weight, low power consumption and ability to resist and recover from mechanical stress. This translates to increased packing density for electronic components, low power IC design and novel materials with the required mechanical and electrical characteristics. The demand for increased packing density has led equipment manufacturers to focus on fabricating interconnects on flexible substrates [36]. These substrates can then be deformed in order to reduce their footprint [37]. However, these efforts have led to reliability issues as the Young's modulus and the yield strength of the metal which is used to fabricate the interconnect is different from that of the substrate, resulting in strain-induced fractures of the interconnects, at the strains values as low as 5% [38]. Improving the reliability of interconnects on flexible interconnects is being addressed by current research. A number of different approaches have been suggested in order to overcome this problem. Some of these are listed in the sections below.

1. <u>Structural solutions for stretchable and flexible electronics</u>

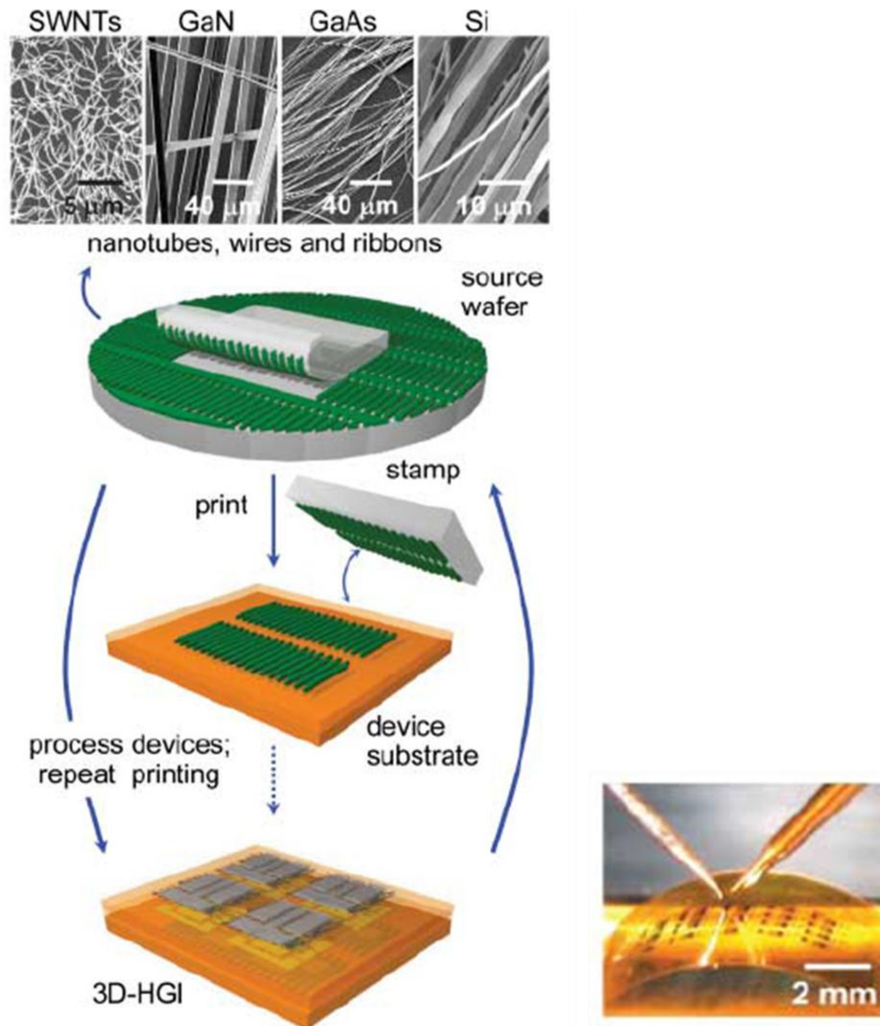


Fig. 2. Method for fabrication 3D vertical stacks of interconnects. The figure also shows the testing of these interconnects when mechanical stress is applied to it [40].

One of the solutions is to optimize the shape of the interconnect, or the interconnect layout, in order to be able to withstand a certain strain on the substrate. Optimization of the shape of the interconnect is done by detailed FEM analysis of different possible shapes and judicious selection of the right shape

based on the kind of application the circuit is likely to be used [39]. An optimized interconnect shape for withstanding longitudinal strain is shown in Fig. 1. The advantages of this solution is that it is the simplest to implement and can offer

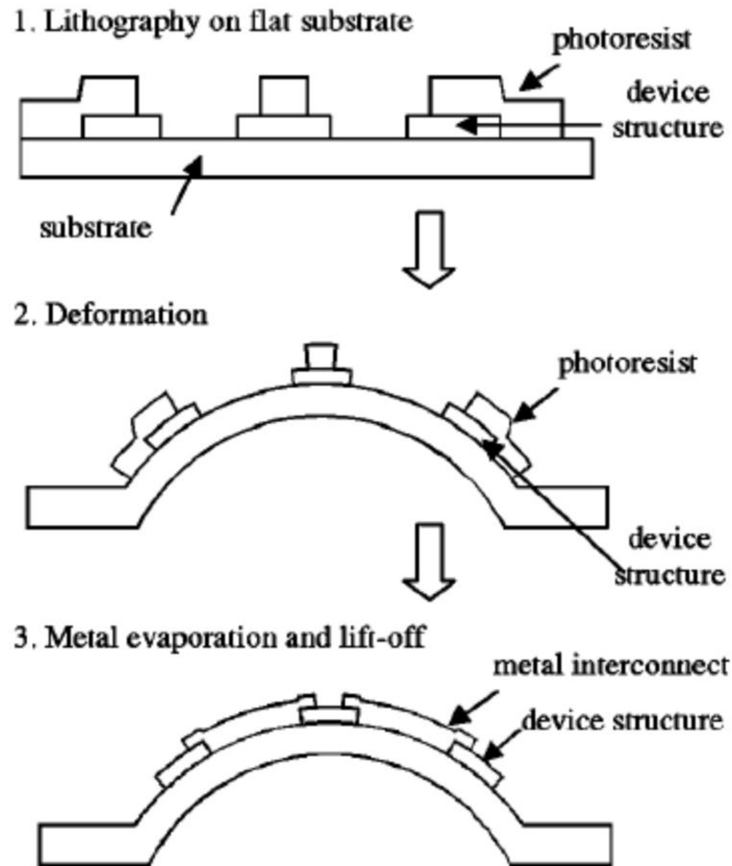


Fig. 3. Interconnect fabrication after pre-stressing in order to ensure connectivity at maximum tolerances [41].

considerable flexibility with little modification to the fabrication process. The greatest disadvantage is that the solution is not universal. If the circuit is deformed in ways that the designers did not foresee, then the advantage of the optimized design is lost and the device is just as prone to mechanical failure as a normal

interconnect. Secondly, almost every such interconnect would require more material than a normal interconnect line and the layout would have to be much more complicated in order to take into account shapes that are not normally encountered in semiconductor manufacturing. Finally, since the selection of the shape is based on a subjective selection based on FEM analysis, quality control of the devices becomes an issue as small changes in the shape of individual interconnects could greatly impact the reliability of the overall circuit.

3-D stacking of the circuit is a second structural approach that has been examined in research. In this approach, most of the critical interconnects are designed to run vertically downwards into the circuit. The metal lines are then supported by enclosing them in other materials like carbon nanotubes [40]. Fig. 2 shows how this can be implemented. This approach is considerably more complex in terms of fabrication than the previous methods. The reliability of this type of device is dependent on the kind of mechanical strain applied. It is best at withstanding longitudinal strain, rather than vertical strain.

A third structural approach to produce interconnects for flexible electronics would be to fabricate a set of sub-circuits on silicon islands deposited on a deformable substrate [41]. After fabricating the individual sub-circuits on the silicon islands, these islands are interconnected using metallization. However, although the interconnects are patterned before deforming the substrate, the deposition is done after deformation to maximum tolerances [41]. Fig. 3 demonstrates a fabrication process which implements this. This ensures that the islands remain interconnected even at high strains. The advantage of this approach

is that maximum tolerances are met and the interconnects remain stable under strain. However, this fabrication method does not address the issues of directional strain. The designer must still understand how the circuit will be strained before it is applied in order to optimize the design of the interconnect. It is also unlikely

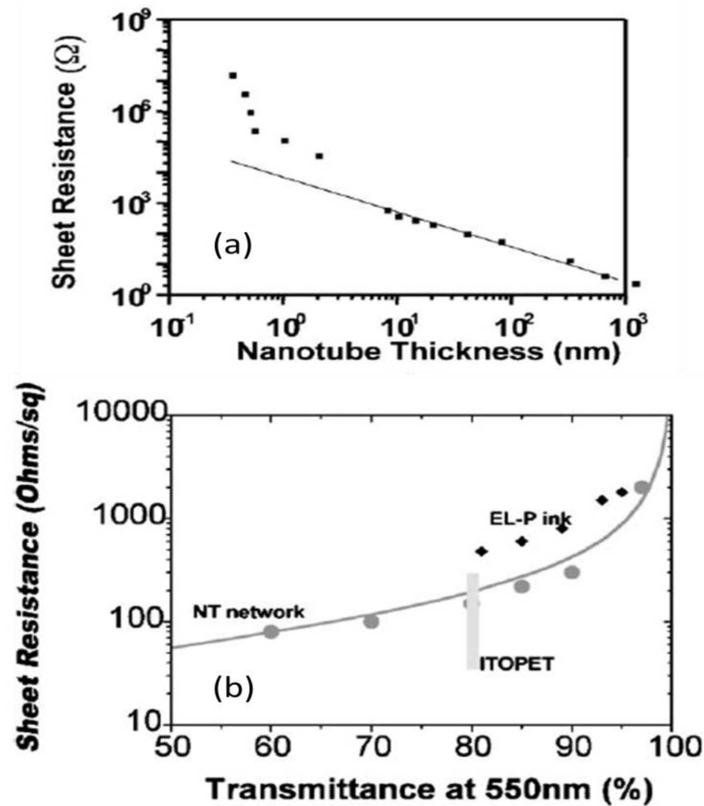


Fig. 4. (a) shows the decrease in sheet resistance with increasing nanotube thickness. (b) shows the increase in sheet resistance with increase in transmittance [47].

that this optimization can be carried out if the circuit is deformed in multiple directions.

2. <u>Material solutions for stretchable and flexible electronics</u>

While the section above illustrates solutions that modify the structure and shape of the interconnect while still using materials found in the current IC fabrication processes, this section presents solutions that are based on novel materials that can be used for interconnects on flexible substrates. All these

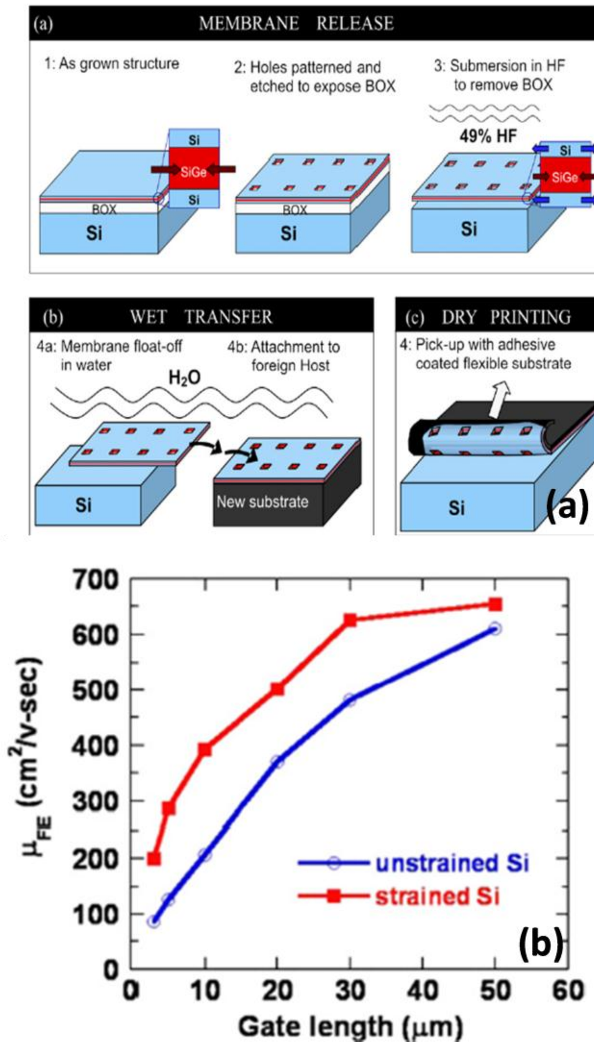


Fig. 5. (a) Fabrication of strained SiGe nanomembranes (b) Comparison of TFTs on nanomembranes with and without strain [49]

materials possess some properties that allow them to deform easily, without a marked change in resistance through them.

The most popular choice for interconnects in flexible electronics is gold. It has been used as an interconnect in a diverse range of applications in flexible electronics paper-based organic electronics [42], active-matrix displays based on organic transistors [43], carbon nanotube based semiconductor applications [44] and printed electronics [13]. Gold is useful because of its low Young's modulus [45] and very low resistance [46]. However, its disadvantages are that it is extremely expensive and that it is a deep-level impurity in CMOS processes, making it unviable in such manufacturing lines. A third problem with gold is that it sputters in molten form, thus increasing the chance of contamination within the deposition system.

Another material that can be used for interconnecting circuit elements on flexible substrates is a network of carbon nanotubes. Single-walled nanotubes (SWNTs) can be used as good conductors since they naturally take on the shape of a thin-walled tube when fabricated [47]. This material is especially useful because its optical properties are also tunable to make it transparent in the visible light range. This would produce a material that could compete with Indium-Tin-Oxide (ITO) in flexible display applications [47]. The disadvantage of this material is that the thickness of the carbon nanotubes determines both the sheet resistance of the film as well as the optical properties. In general, a trade-off needs to be made between the resistance and the optical properties [47]. Another disadvantage is the fabrication method of the carbon nanotube, which calls for

new materials and processes to be added to a conventional fabrication facility, which can be expensive.

A few other options include other metal interconnects like chromium, silver, aluminum and copper, which are good conductors, but are much more brittle than gold. Some semi-conductor materials like gallium nitride (GaN) and gallium arsenide (GaAs) can also be doped to behave like conductors. The advantage is that these materials can be fabricated to form ribbons, wires and nanotube structures [40]. However, these have process integration issues without the very high conductivity of metallic materials.

A third option is to use nanomembranes of various semiconductor materials and engineer them for the required conductivities [48, 49]. The conductivity can be modified in various ways like controlling the doping in the material, controlling grain size [50] or by introducing strain [48] in the material. Fig. 5 shows the fabrication of SiGe nanomembranes and the change in field-effect mobility for TFTs fabricated on it, when strain is applied to the nanomembrane. The advantage of this approach is the high degree of control that can be achieved in terms of the sheet resistance of the device. The small size of the device, in the thickness of a few hundred nanometers, also means that the packing density of the circuits can be increased significantly, compared to other techniques, without significantly trading off sheet resistance. The disadvantage of this method is that the fabrication process differs significantly from conventional fabrication processes, which makes integration difficult in the short term. The fact that sheet resistance changes significantly in the nanometer regime [49] also

places significant restrictions on the precision of the deposition and design processes.

B. Processing techniques for flexible and stretchable electronics

The processing techniques that can be used on substrates which are used for flexible electronics applications are limited primarily by their low glass

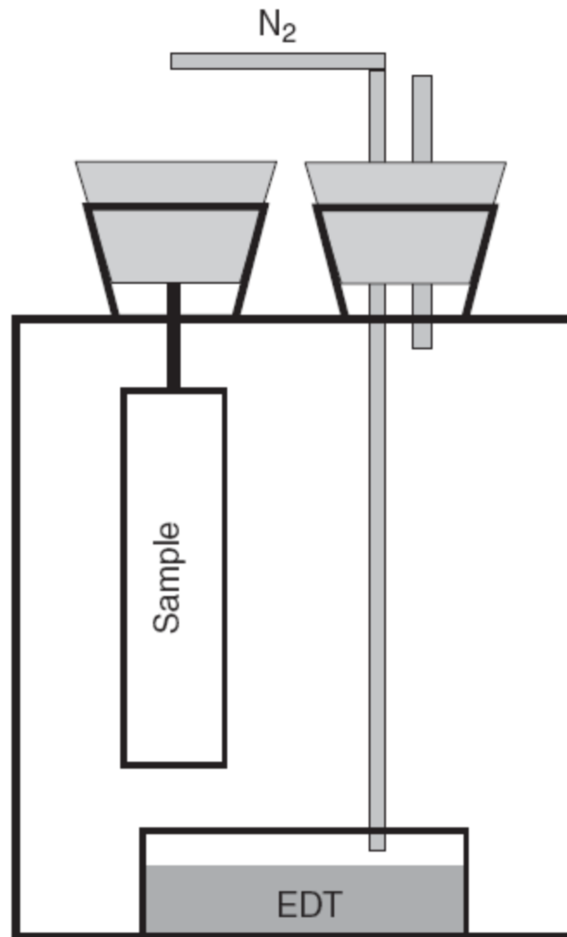


Fig. 6. Schematic of Organic vapor deposition, a variant of thermal vapor deposition, that improves film uniformity by making the deposition phase diffusion-limited. The nitrogen is heated as it is used to transport the source (EDT) to the sample [54].

transition temperatures and their tendency to flex and bow during the fabrication process. A new set of patterning and deposition techniques were designed specifically to deal with flexible substrates for the reasons stated above. Some of these techniques are discussed subsequently.

1. <u>Solution deposition of organic thin films</u>

Most polymers are deposited using a solution deposition technique. The polymer is first dissolved in a compatible solvent and the solution is then sprayed on or spun on the substrate. The solvent is then evaporated off the substrate, leaving behind the required polymer film [51, 52]. This process produces very uniform films of thicknesses as low as 100 nm. The advantages are the very high deposition rates achieved and the relative ease with which the process can be modified in order to accommodate very large area films [51]. The disadvantages are the interference between the solvent and the previously deposited layers and the inability to locally pattern complex circuit elements [51]. The interference phenomenon can be ameliorated by functionalizing the solvent in order to deposit multiple films at the same time, or perform multiple processing steps at the same time. But the results are generally a compromise on the performance of the circuit [51]. An interesting advance in the solution processing technique is the ink-jet printing technique [50, 51]. This allows considerable flexibility in the local patterning of circuit elements. Recent advances in the inkjet printing of organic compounds have produced circuit elements that can be patterned with sub-femtoliter accuracy [53]. This process places greater demands on polymer inks

including better uniformity and formulations that satisfy all the electrical and optical properties of the application, down to the micron level [51].

2. Vapor-phase deposition of materials

Vapor-phase deposition of thin layers is the most common form of processing for flexible electronics. It has been directly adapted from the semiconductor deposition technique called vacuum thermal deposition. The process involves the placing of the source in a boat and heating it in vacuum so that it sublimates. The substrate is placed in the path of the resulting gas flow and a thin layer of the source is deposited on the substrate [51]. The primary advantage of this method is that it is already a mature process in the semiconductor industry. The other advantage is that a potentially unlimited number of thin films can be grown as a stack using this method. The disadvantages are that there is a lot of wasted source material as the source not only coats the substrate, but also the entire chamber and the inherent film non-uniformity. The evaporation rate in different directions is non-uniform, resulting in a thinner film at the edges and a thicker film at the center. This can be a problem, particularly for large-area displays, where the substrate size is very large [51]. This problem is reduced considerably by using a variant of the thermal deposition technique called organic vapor-phase deposition (OVPD), where the film uniformity is controlled using a transport medium such as an inert gas or nitrogen [51, 54]. However, this is limited by the temperature required to vaporize the source and is typically used only for organic compounds. A third disadvantage relates to thermal deposition of compounds. As different elements within the

compounds have different partial pressures at a particular temperature, the rate of evaporation of each of these elements, and therefore, the deposition rates will be different. This results in a stoichiometric difference between the deposited film and the original source material [55]. Fig. 6 shows a schematic for a vapor-phase deposition system.

3. Thermal transfer of materials

This technique works only with heat sensitive materials at significantly lower temperatures than the glass transition temperature of the substrate. Therefore, it is used mostly for patterning organic materials. These materials are

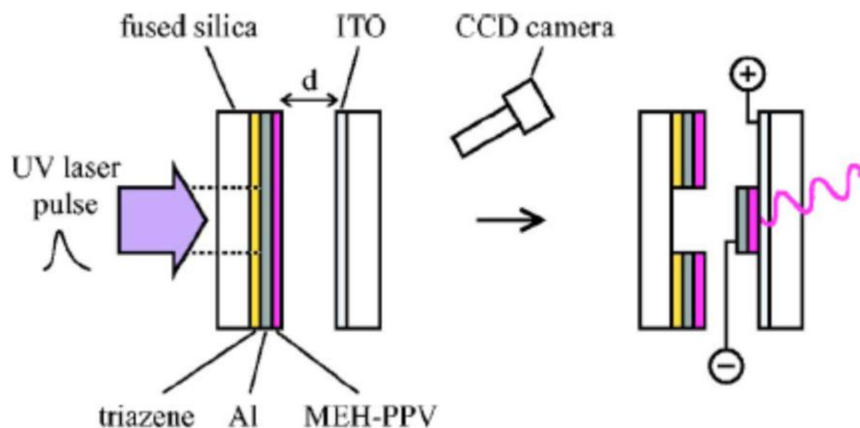


Fig. 7. Schematic of the thermal transfer principle. The laser decomposes the sacrificial triazene layer, resulting in the deposition of the remaining portion of the film on the receiving ITO layer. The UV laser is run in a pre-determined manner in order to transfer the required pattern onto the ITO film [56].

pre-deposited, without patterning, on a “donor” sheet. The donor sheet is then placed over the substrate and a localized heat source (like a laser) is run over the

donor in a pre-determined pattern. The result is the transfer of the required material from the donor sheet to the substrate [51, 56].

4. Direct patterning of electronic devices

Direct patterning of thin films is the process of transferring patterns onto the substrate using processes that are analogous to printing. Such methods include

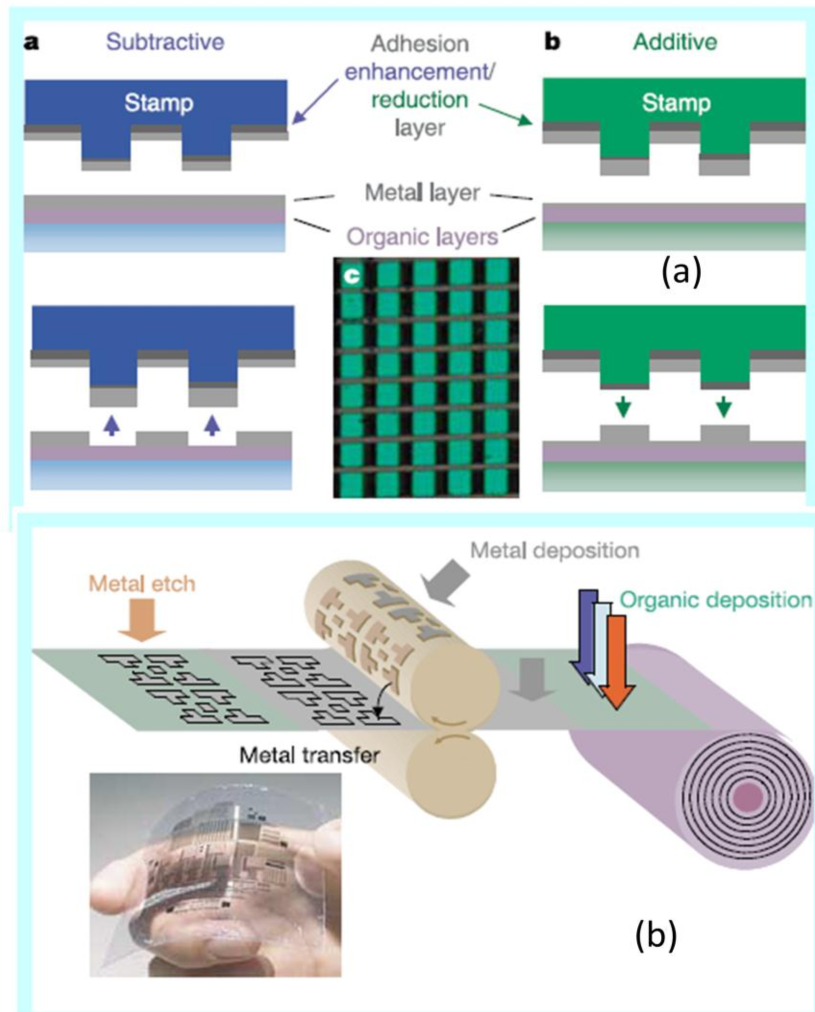


Fig. 8. (a) Schematic of cold welding. The figure demonstrates how a stamp can be used for selectively cold-welding patterns into the metal. (b) Schematic of roll-to-roll printing using equipment similar to a printing press, which makes the process very low cost [51].

imprinting a thin film of the functional material using a rubber or polymer stamp, cold welding, lithographically induced self-assembly or microcutting of the cathode metal after deposition of the underlying functional materials [50, 51, 57].

Cold welding is the binding of two clean surfaces of the same metal on contact or on the application of moderate pressure. By selectively applying the pressure, only certain parts of the second metallic film are allowed to stick, while the remaining portion may be removed easily. The stamp is made of a soft material, typically poly-dimethylsiloxane (PDMS), with a desired pattern embossed on it. An additional adhesion-prevention coating is placed on it to prevent the metal from sticking on the stamp [51].

Roll-to-roll printing is a very attractive form of processing flexible electronics. This process is very mature because the same equipment has been used in the printing industry for a long time. This processing technique can be easily adapted to flexible electronics because the substrate on which the electronic components need to be fabricated is flexible, making it similar to paper.

C. Review of properties of flexible substrates

Recent research has resulted in a number of materials that show promise as substrates for flexible electronics applications. However, there is no universal solution to the choice of a flexible substrate as different materials offer unique desirable properties for a particular application. As we make a choice of which substrate to use in order to fabricate flexible memory, we need to evaluate the criteria discussed below.

A fundamental property of the chosen flexible substrate is mechanical and thermal stability [58]. Mechanical stability ensures that the substrate does not crack as it is bent. Ideally, the substrate should be capable of flexing repeatedly without any significant degradation. This property also extends to the fact that the material does not show fatigue i.e. the material remains stable dimensionally and does not change in its size as it is stressed over time. Thermal stability ensures that the material does not deform drastically when subjected to temperature changes. This is especially important during device fabrication, during which temperature changes are fairly common. The change in dimensions due to changes in temperature is measured as the Coefficient of Thermal Expansion (CTE).

A low CTE substrate ensures that the flexible circuit can be fabricated with relatively little change to the original silicon process and also is capable of operating over a wide range of temperature. One of the main points of failure for flexible circuits is at the interface of the substrate, which is usually organic, and the device layers, which are almost always inorganic. A large CTE for the substrate results in stresses developing in the inorganic thin film layers in contact with the substrate. The result is usually either cracking or poor adhesion of the device layers to the underlying substrate.

Surface properties of the substrate are also extremely important. For example, planar surfaces are a prerequisite for the fabrication of almost all devices on flexible substrates. This is because most devices are deposited as thin films, which tend to have very poor step coverage. A non-planar surface would

result in parts of the substrate being exposed to the upper metallization layers. Another important surface property in the case of PMC devices is surface conductivity. The surface of the substrate on which the devices are fabricated should be conductive so that this can be the bottom electrode or cathode. A non-conductive surface, therefore, would have to be processed in order to make it conductive.

The final property that needs to be scrutinized is cost. This cost is not limited to the cost of the substrate, but also the cost of adapting the fabrication process to the substrate. One of the advantages of flexible substrates is cost savings. This is realized in most cases by migrating from the traditional wafer-by-wafer fabrication approach to the roll-to-roll fabrication process. The feasibility of this approach depends on the robustness of the substrate and the ease with which the substrate can be aligned during fabrication.

Many substrates show potential for flexible electronics applications. The ultimate choice depends primarily on a compromise between mechanical and thermal stability and cost of the substrate and the materials involved in the fabrication of the electronic devices.

1. Stainless steel foil

Stainless steel foil is a very attractive option as a flexible substrate. Metal foils generally have very high moduli of elasticity and are unlikely to deform during roll-to-roll processing. Stainless steel foils have a fairly high CTE, about 15-20 ppm higher than silicon. This may present problems when processing at elevated temperatures. The surface of metal films is usually extremely rough.

Planarization of metal films is usually a fairly involved process. The costs involved with procuring SS foils are usually low, but planarization usually elevates these costs [58]. Finally, the costs involved with processing SS foils are not much lower than processing other types of flexible substrates in preparation for device fabrication.

2. Glass

Thin glass substrates are extremely stable, both mechanically and thermally. The CTE of glass is extremely close to that of silicon, which makes the fabrication process very predictable and little change is required from the traditional silicon process in order to adapt it to the glass substrate. The engineering of the glass transition temperature for glass substrates is a very well understood process. The surface properties of glass are excellent as with polishing a very smooth surface can be obtained. Unfortunately, glass displays a reasonable degree only at thicknesses below 200 µm, which can be achieved using the float glass process. For flexible electronics, the required flexibility is reached only at thickness of about 30 µm [59]. These thicknesses can be achieved using Down Draw (DD) process [59]. However, producing glass at these thicknesses is extremely expensive and the surface becomes very rough. Additionally, flexible glass substrates are delicate and are not suitable for roll-to-roll processing. Glass substrates were not considered the ideal choice for substrates for flexible memory for all the reasons mentioned above.

3. Polymers

Polymers are the most versatile and inexpensive circuit elements used in flexible electronics. They can be synthesized to have a wide variety of properties like high melting temperature, high flexibility, high strength, different CTEs and other properties [58]. In addition, their adhesion to metal thin films is usually good. They are also amenable to roll-to-roll processing because of their high flexibility, robustness and light weight. The low cost is because the polymer manufacturing process is a high volume process. The disadvantages of using polymers are that the glass transition temperature of most of these materials is quite low and the CTE of these materials is also quite high. Substantial changes have to be made to the traditional manufacturing process by replacing most unit processes with alternative low temperature unit processes. In spite of these disadvantages, these substrates showed the highest potential for use as substrates in flexible memory.

Polyimide is a polymer that has been used in the electronics manufacturing industry for a long time. It is extremely stable at high temperatures, allowing for processing temperatures as high as 350°C and strong enough to withstand the rigors of roll-to-roll processing. It does have a CTE of about 20 ppm, which is much higher than that of silicon. The fabrication process needs to be a low temperature process to prevent the substrate from deforming too much as the circuitry is manufactured over it. This polymer was used as a substrate for fabricating PMC flexible memory.

Polytetrafluoroethylene (PTFE) is another polymer that has traditionally been used in the electronics industry. It is also a higher temperature plastic and allows for processing temperatures up to 250°C. Unfortunately, it is not a very good dielectric. Also, it is not thermally stable because of a high CTE. While it shows flexibility, a few other polymers have already demonstrated a greater degree of flexibility. This substrate was not considered for manufacturing PMC memory.

Polyethylenes are a family of polymers that show significant promise as flexible substrates. Two of these in particular – polyethylene terephthalate (PET) and polyethylene naphthalate (PEN) are very flexible and have a reasonably low CTE. The disadvantage of these polymers is that the fabrication process have to be very low-temperature. These polymers have glass transition temperatures in the range of 100°C-200°C. These substrates have yet to be considered as substrates for flexible memory.

Polyimide is generally the most popular choice for a flexible substrate as it allows for more options when developing a manufacturing process. PET and PEN are the other two choices. However, they are only considered if transparency is a prerequisite.

D. Review of solid electrolyte material systems and their compatibility with flexible substrates

A number of metal-glass combinations have been studied as solid electrolyte systems for some time now. A few of these electrolytes have shown great promise for use in memories, with the result that PMC devices with different

material combinations can be fabricated on conventional rigid substrates. The choice of a solid electrolyte for flexible circuit applications is, however, significantly restricted by fabrication process considerations. Specifically, the solid electrolyte should conform to the following specifications:

1. The fabrication process of the material combination should be lower than the glass transition temperature of the substrate.
2. The material combination should adhere well to any underlying metal layer.
3. The modulus of elasticity of the solid electrolyte material should be comparable to the modulus of elasticity of the substrate to prevent cracking and de-adherence on flexing
4. The material combination must continue to retain its solid electrolyte properties even on flexing, so that the memory properties are reasonably stable even when the device is subjected to mechanical stress.

Some material combinations that are good candidates for the solid electrolyte are given below.

1. <u>The silver-germanium selenide electrolyte</u>

The Silver-Germanium Selenide (Ag-Ge-Se) electrolyte is extremely simple to fabricate. It is made by depositing a Germanium Selenide base glass (Ge_xSe_{1-x}, $x < 0.33$) layer on the bottom electrode by physical vapor deposition. A layer of silver, approximately 1/3rd the thickness of the glass layer, is then deposited over the glass. This material combination is then exposed to ultra-violet

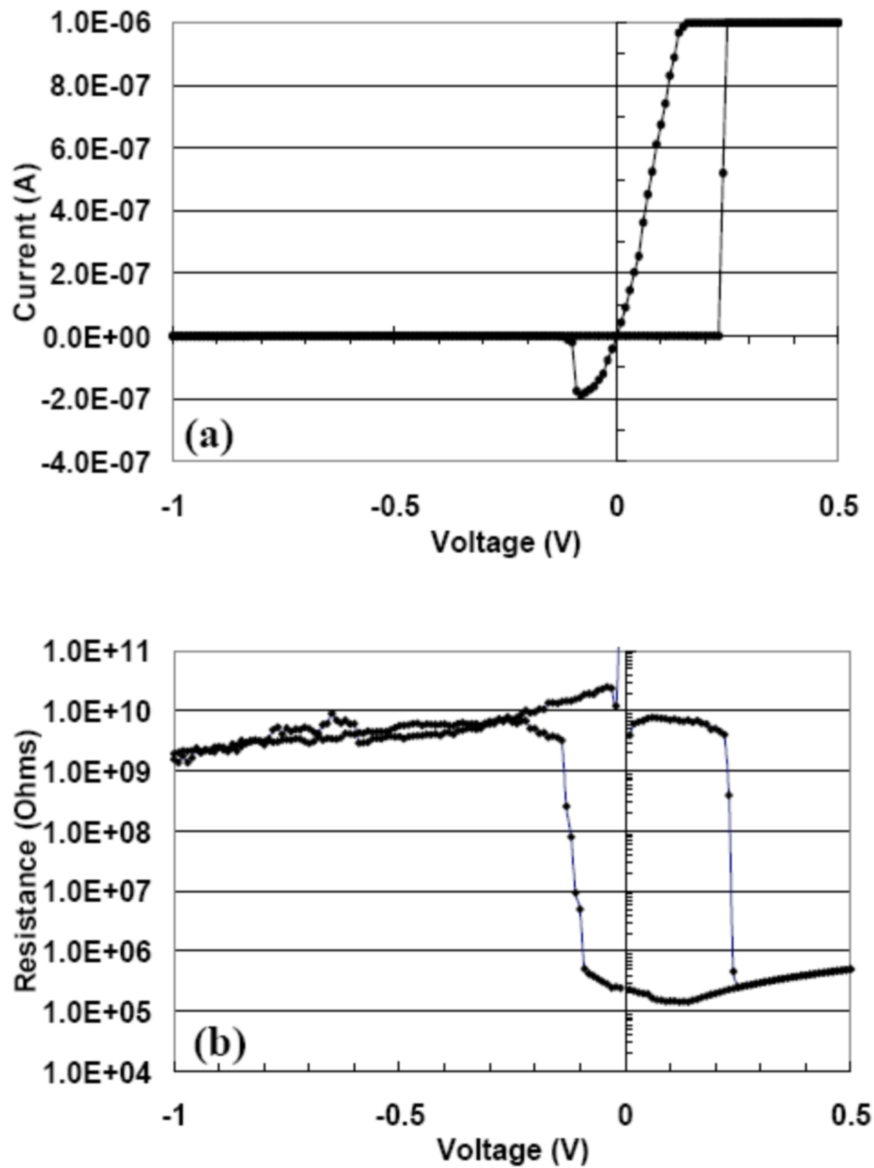


Fig. 9. (a) Current-voltage characteristic of a PMC device with a programming current compliance of 1μA (b) Resistance-voltage characteristic of the device. The ratio of the off to on state resistance is about 4 orders of magnitude [1].

(UV) light of wavelength 405 nm, at a power density of about 4 mW/cm^2 for about 20 minutes in order to dissolve the silver into the base glass to give the solid electrolyte [1]. In order to complete the device, the bottom electrode is made of an

electrochemically indifferent metal like nickel (Ni), while the top electrode is made of an easily oxidizable metal like silver (Ag).

The advantage of using the Ag-Ge-Se electrolyte stems primarily from the flexibility of the Ge-Se base glass, whose elastic modulus is very high and the low processing temperatures. The fabrication temperature of this electrolyte is almost room temperature, with the highest temperature being reached during physical vapor deposition of the glass and silver layers. No other high temperature processing step is required during fabrication as the electrolyte formation depends solely on the exposure to UV light. Another advantage of using this electrolyte is its low turn-on voltage of about 0.2 V for devices with a nickel (Ni) cathode [1].

2. The silver-germanium sulfide electrolyte

The silver-germanium sulfide (Ag-Ge-S) electrolyte system produces much more stable resistance states than the Ag-Ge-Se system. The on-off resistance ratio is also about 50 times higher [2]. The turn-on (about 450 mV) and turn-off (about -250 mV) thresholds are also much higher [2], making this system a little more energy intensive than the Ag-Ge-Se system. The primary advantage of this system is that it is capable of withstanding the high back-end-of-line (BEOL) processing temperatures found in conventional silicon processing lines. However, the electrolyte needs an anneal at 430°C for about 15 minutes during fabrication [2], which makes it incompatible with most flexible substrates, especially those that are polymer-based. The higher processing temperatures and the higher energy requirements make this electrolyte system a less than ideal choice for the purpose of fabricating PMC memories on flexible substrates.

3. The copper-germanium sulfide electrolyte

The Copper Germanium Sulfide (Cu-Ge-S) system exhibits lower programming resistance states than the Ag-Ge-S system, with the on-state resistance being about 15 kΩ and the off-state resistance being about 1 GΩ with a 10μA compliance current [2]. The write threshold (about 300 mV) and the erase threshold (less than 100mV) are also much lower than the Ag-Ge-S system [2], which makes it a low-power system. However, this system is very temperature sensitive, making the device characteristics very unpredictable as the temperature of operation is varied [2].

This is probably because copper is much more reactive electrochemically than silver, resulting electrochemical processes being much more dominant within the device than the externally applied programming currents and voltages. This system shows potential for use in the flexible substrate process. A greater understanding of the system is necessary before it can be used, however, since it is not known whether the electrochemical processes are accelerated when the system is subjected to mechanical stress.

4. The copper-silicon dioxide electrolyte

The most important attribute that works in favor of the copper-silicon dioxide (Cu/SiO_2) system is that the diffusion of copper through SiO_2 is very well-understood [26]. Another reason that this system is being investigated for applications as a solid electrolyte is that both materials are already available in conventional silicon manufacturing processes. However, this system is not suitable at all for flexible electronics applications. One reason for its

incompatibility is that the copper cannot diffuse into the SiO_2 matrix by photodiffusion as in the case of previous systems. This system requires a thermal diffusion step at 610°C for at least 15 minutes in order to form the solid electrolyte [60]. Another major disadvantage of this system is that the SiO_2 matrix is brittle and tends to crack rather than bend when subjected to mechanical stress. The on-off resistance ration is comparable to that of the Ag-Ge-S system with the write threshold (about 1.3 V) and the erase threshold (about -0.5 V) being slightly higher than those of the Ag-Ge-S system [60]. Thus, this electrolyte cannot be considered for flexible electronics applications, even though its switching behavior is comparable to the other electrolyte systems on conventional rigid substrates.

5. <u>The copper-transition metal oxide electrolyte</u>

Thus far, the copper-tungsten oxide (Cu/WO_3) system has been studied for applications as a solid electrolyte. This system shows great potential for use in flexible circuit applications. The primary reason for this conclusion is that the formation of this electrolyte is a room-temperature process, with the Cu diffusion into the WO_3 being governed only by exposure to UV light [3]. The off-state and on-state resistances differ by about 7 orders of magnitude and the programming currents are extremely low (about 1μA), resulting in very low power consumption [3]. The device exhibits a write threshold at around 400 mV and an erase threshold at around -200mV [3]. Preliminary retention testing shows that the devices based on this electrolyte show excellent performance, even at elevated

temperatures. We are currently investigating the effects of mechanical stress on this system.

E. Mechanical properties of germanium selenide (Ge-Se) glass

Chalcogenide glasses are much less brittle than silicate glasses. This section discusses the mechanical properties of Ge-Se glasses as a specific

Property	Property value for various Ge/Se†								
	0/100†	5/95	10/90	15/85	20/80	25/75	30/70	40/60	100/0‡
$\langle r \rangle$	2	2.1	2.2	2.3	2.4	2.5	2.6	2.7	4
ρ (g/cm^3)	4.28	4.31	4.34	4.36	4.37	4.36	4.32	4.36	5.15
E (GPa)	10.25	11.05	12.08	13.80	14.73	16.05	17.90	22.38	123.5
K (GPa)	9.60	10.01	10.43	11.22	11.47	12.21	12.64	16.43	70.95
ν	0.322	0.316	0.307	0.295	0.286	0.281	0.264	0.273	0.210
H (GPa)	0.39	0.57	0.77	1.05	1.38	1.72	2.02	2.35	7.37
H_V (GPa)	0.36	0.52	0.71	0.97	1.28	1.59	1.88	2.18	6.84
K_c (MPa·m$^{1/2}$)	0.16	0.09	0.12	0.22	0.28	0.22	0.20	0.16	0.59
$K_{c,\text{theo}}$ (MPa·m$^{1/2}$)§	0.197	0.211	0.227	0.250	0.265	0.283	0.304	0.351	0.965
$K_{c,\text{theo}}$ (MPa·m$^{1/2}$)¶	0.179	0.194	0.211	0.235	0.251	0.270	0.293	0.337	0.887

Table 1. Density, Elastic Modulus, Indentation Hardness and Toughness of Ge-Se glasses [61].

example of the properties of chalcogenide glasses. The goal of this section is to emphasize that chalcogenide glasses, and more specifically Ge-Se glasses, possess the necessary mechanical characteristics to be used in flexible electronics.

Ge-Se glasses are characterized by relatively low hardness values (0.39 GPa to 2.35 GPa) and fracture toughness values (0.1 MPa.m$^{1/2}$ and 0.28 MPa.m$^{1/2}$) [61]. As a comparison, silicon dioxide (SiO_2) films have hardness values between 7.9 GPa and 14.5 GPa [62] and fracture toughness values between 0.1 MPa.m$^{1/2}$ and 0.28 MPa.m$^{1/2}$ in air [63]. The low hardness values of Ge-Se films result in the brittleness factor being lower than that of silicate glasses. The brittleness factor is defined as shown below:

$$\text{Brittleness Factor} = \frac{\text{Hardness}}{\text{Fracture Toughness}} \qquad (1)$$

being lower than that of silicate glasses. Hardness and Young's Modulus of Ge-Se glasses increase with increasing germanium (Ge) content, but fracture toughness exhibits a maximum for $Ge_{20}Se_{80}$ [61]. The Young's Modulus of Ge-Se glasses (between 10.25 GPa and 123.5 GPa) are also much lower than silicate glasses (between 73.1 GPa and 145 GPa) [61], which means that chalcogenide films demonstrate more elastic deformation for the same amount of stress than silicate glasses. The preceding discussion shows that chalcogenide glasses, and more specifically Ge-Se glasses, can be used in engineering applications that require that demand mechanical flexibility. Mechanical characteristics for different compositions of Ge-Se glass are given in Table 1.

F. The memristance property

The concept of the memristor was first introduced by Leon Chua in 1971 [64]. The original paper described the device as a two terminal device which relates the flux linkage with the charge. Two types of memristors were discussed in [64]. The flux-controlled memristor, which is of interest, is described by the set of equations given below:

$$i(t) = W\big(\Phi(t)\big) \cdot v(t) \qquad (1)$$

$$W(\Phi) = \frac{dq(\Phi)}{d\Phi} \qquad (2)$$

Here i(t) is the time-dependent current, v(t) is the voltage, Φ(t) is the flux linkage and q(t) is the charge, which is dependent on the flux linkage. This was

considered the fourth circuit element, along with the inductor, the capacitor and the resistor. Although an electromagnetic field interpretation was developed and active memristor circuits were demonstrated, no passive circuits, i.e. one without an internal power supply, were demonstrated by the original paper, and were unknown at the time. A later paper, by Chua and Kang [65], generalized the concept of the memristive system to a much broader class of systems which are described by a set of equations given below:

$$\frac{dx}{dt}=f(x,v,t) \qquad (3)$$

$$i=G(x,v,t)\cdot v(t) \qquad (4)$$

where i(t) and v(t) are the time-dependent current and voltage respectively and x is a state variable, which does not necessarily have any correlation with any physical quantity within the system. This set of equations describes a voltage-controlled memristance system.

Interest in the memristance system was renewed when a team from HP published research demonstrating proof on concept for such a device [66]. The device comprised a thin film of titanium dioxide (TiO_2) with platinum (Pt) electrodes. The memristive behavior was attributed to the movement of oxygen vacancies within the device in response to an applied voltage. The formation of conductive filament bridges because of the arrangement of oxygen vacancies was said to be responsible for the observed changes in resistance of the device [67].

Many other candidates for passive memristors have emerged since this time. These include the oxide-based memristor integrated with CMOS logic [68],

spin-torque based memristors [69], the flexible solution-processed memristor [70] and the gadolinium oxide (Gd_2O_3) based memristor [71]. Each of these memristors can be optimized based on the requirements of the individual electronic application. The model that is proposed for PMC based switches in the subsequent sections demonstrates that these devices also show memristive behavior.

SILVER BASED SOLID ELECTROLYTE INTERCONNECTS

The previous section discussed the mechanical properties of chalcogenide glasses. It shows that the germanium selenide glass is the best candidate for a glass which is capable of withstanding mechanical stress as it is the most elastic. The silver doped germanium selenide system has been studied extensively as a solid electrolyte which can be used as a resistance change element. The ability of controlling device resistance based on the application of a voltage is a useful property for interconnects in flexible electronics applications. This property ensures that if a metal layer overlying a solid electrolyte layer fractures, then the signal voltages will promote the growth of a metallic electrodeposit between the edges of the fracture. Ideally, this would restore the resistance of the interconnect to its original value, thus greatly improving the reliability of the interconnect. This section discusses efforts in using this system to demonstrate self-healing interconnects. It discusses the fabrication, characterization and the reliability of these interconnect structures..

A. Fabrication

The interconnect test structures were fabricated directly on a R/Flex 1000 flexible substrate from Rogers Corp. which consists of a 25 μm thick polyimide layer on a 500 μm (approximate thickness) copper sheet. The polyimide has a glass transition temperature of approximately 250°C, which limits the processing temperatures used during subsequent processing. The fabrication process is based on the process outlined in [55]. However, the process has been adapted to be suitable for flexible substrates, based on previous work in this area [7, 72]. The

flexible material was first mounted on a rigid silicon substrate using double-sided carbon tape. This tape, typically utilized in electron microscope sample mounting applications, can withstand the moderate temperatures used in test structure fabrication while maintaining adhesion and minimizing any distortion in the flexible element due to temperature stresses. The multi-layer substrate was rinsed

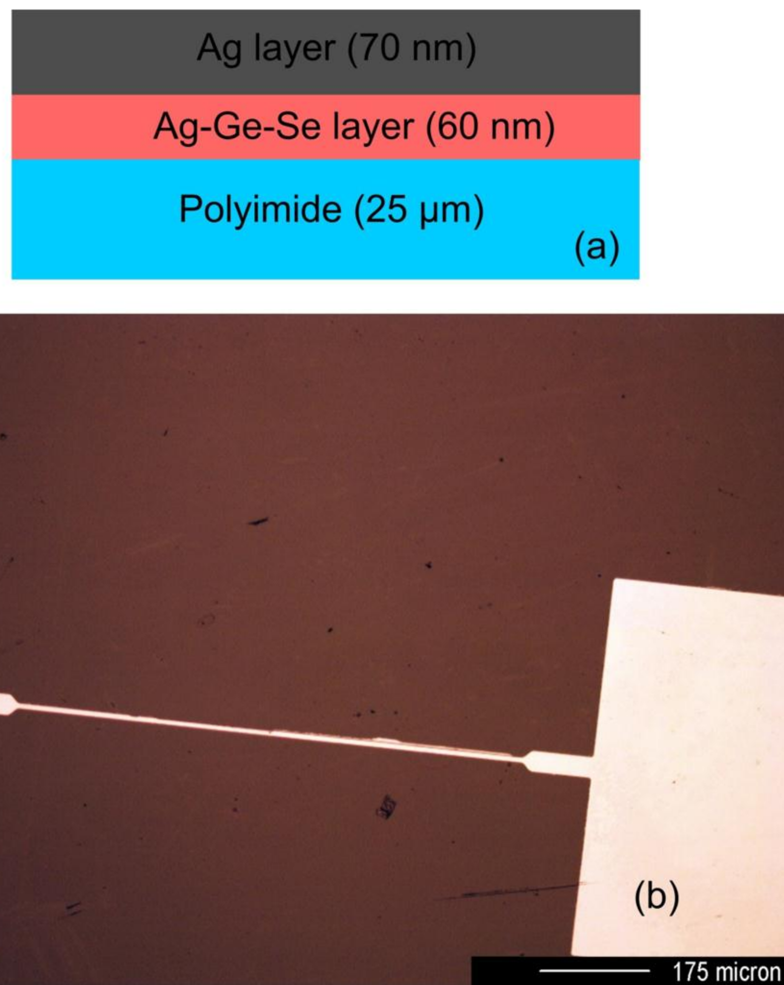


Fig. 10. (a) Schematic of the self-healing interconnect structure on polyimide, consisting of a 70 nm thick Ag layer on Ag-Ge-Se solid electrolyte. (b) Optical microscope image showing the top view of the structure. The test pattern is 10 µm wide and 775µm long, terminating in probe pads at either end.

using acetone, ethanol and methanol in a pre-fabrication cleaning step. As part of the lift-off patterning process, AZ 4330 photoresist was spun onto the surface of the polyimide at 3500 rpm for 30 sec. The sample was then soft-baked at 80°C for 17 min. in a convection oven in order to evaporate the resist solvent. This oven was used instead of a conventional hotplate because the thermal conductivities of the polyimide and mounting tape are low and hence hotplate soft-baking, as used for silicon substrates alone, would not be as effective. The photolithography step involved exposure of the resist to ultra-violet light at an intensity of 5 mW/cm^2 for 45 seconds through a dark field mask containing the interconnect pattern. Immersion in AZ 300 MIF developer for 90 sec was used to develop the pattern in the resist. The layers that make up the test structures were then deposited by thermal evaporation.

The thin films used to create the solid electrolyte comprised a 60 nm thick germanium selenide ($Ge_{33}Se_{67}$) glass layer and a 30 nm thick silver (Ag) layer. The Ag layer was photo-dissolved into the $Ge_{33}Se_{67}$ layer using a blanket UV exposure in the exposure system for 20 minutes to create the Ag-Ge-Se solid electrolyte [73]. The top Ag layer which forms the 70 nm thick interconnect lines was then deposited on the electrolyte.

A lift-off step was then carried out in acetone to pattern the electrolyte and interconnect layers. The flexible substrate was then de-bonded from the rigid substrate for stressing and characterization. The final device structure is shown in Fig. 10(a). A second set of control samples, with 70 nm thick Ag lines directly on the polyimide and no solid electrolyte layer, was also fabricated using the same

mask. The average resistances of both types of interconnect (including contact resistance), as measured using tungsten probes on micromanipulators connected to an Agilent 4155C, were approximately 75 Ω. Note that the sub-100 nm thickness of the metal combined with the inherent elasticity of the Ag-Ge-Se electrolyte allows these structures to be highly flexible [61] but it is still possible to induce failure using high tensile stress via small radius bending.

B. Characterization

This section outlines the various characterization methods used to investigate the behavior of the device. The first few tests were used to validate the self-healing property of the Ag/Ag-Ge-Se bilayer interconnect. The second series of tests were used to characterize the reliability of such an interconnect. Preliminary results on the reliability of the interconnect to both DC and AC voltages were investigated.

1. <u>Failure resistance and self-healing response of the solid electrolyte interconnect</u>

In order to test the self-healing response of the Ag/Ag-Ge-Se bilayer, a sample with these interconnects on polyimide was subjected to tensile stress by bending it around a mandrel of radius 5 mm for 5 minutes. The process was repeated 5 times to assure that a significant number of the interconnects had failed due to cracking. This process was repeated on a sample of Ag interconnects on polyimide. The stressed substrates were then flattened out for electrical characterization.

Fig. 11 shows examples of failed line resistance for both sample types. The resistance was measured using a 10 mV signal to minimize voltage-induced changes through electrochemical transport in the material. The measurement was

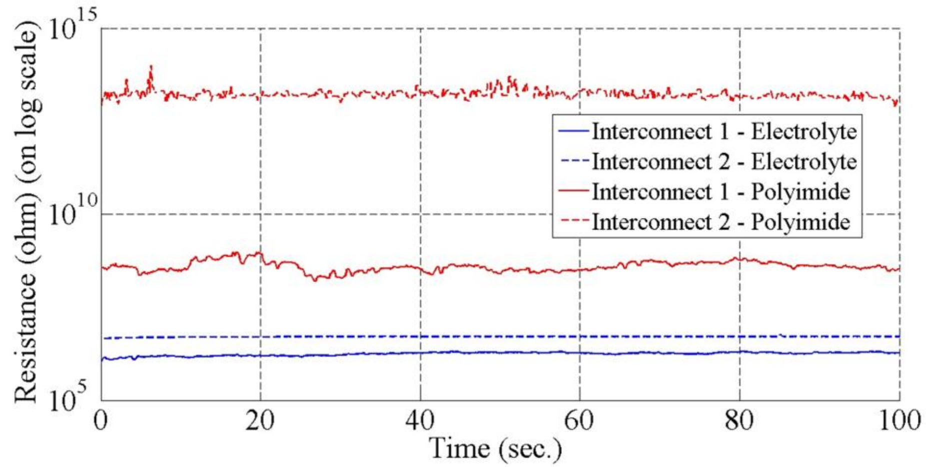


Fig. 11. Resistance of two failed Ag lines on Ag-Ge-Se solid electrolyte (red) and Ag directly on polyimide (blue).

made over a 100 second time period to ensure that the break resistances were stable. The results show that the failed interconnect lines formed on the solid

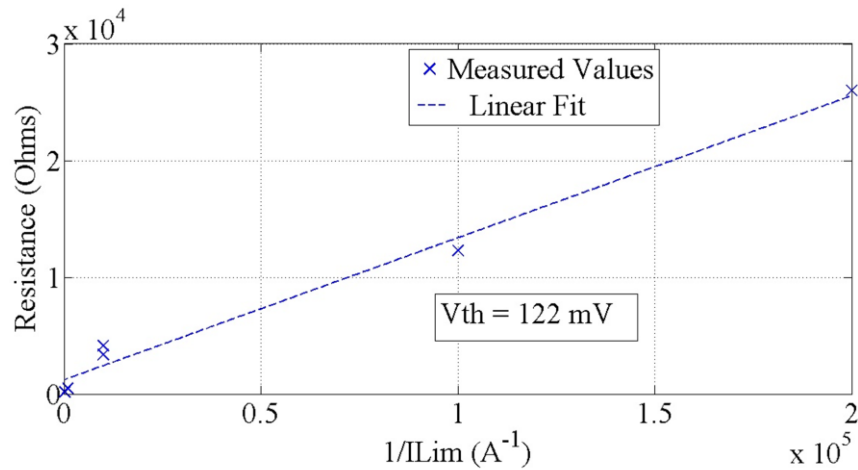


Fig. 12. Healed interconnect resistance plotted against the reciprocal of the current limit (2V DC healing bias).

electrolyte have significantly lower resistances (between 10^6 and 10^7 Ω) than those deposited directly on polyimide (>10^8 Ω). These results suggest that the solid electrolyte itself does not fracture during mechanical stressing due to its pliability and maintains at least partial continuity.

Fig. 12 shows the resistance of healed interconnect lines following the application of a 2V DC bias as a function of the reciprocal of the compliance current limit $1/I_{lim}$. The goal was to validate the fact that the electrochemical behavior of the device was consistent with the Ag-Ge-Se electrolyte system. As expected, the results reveal that the resistance of the healed interconnects decreases as the current limit increases. As described previously, this is a characteristic of devices based on PMC technology. The slope of the plot in Fig. 12 yields a V_{th} of 122 mV for these interconnect samples, which is close to the electrodeposition voltage seen in Ag-Ge-Se memory devices [1].

2. Analysis of the self-healing process

In the next set of experiments, three resistance states were examined in order to further characterize the self-healing process; (1) the resistance of the unbroken interconnect, (2) the resistance of the broken interconnect, and (3) the resistance of the interconnect after the healing voltage is applied. The samples were mechanically stressed as before and a 2V bias with a compliance current of 10 mA was used as the healing stimulus in all cases to ensure a low electrodeposit resistance. The resistance distribution shown in Fig. 13 is the result of testing 10 devices. The 3 phases of testing are shown: the as-fabricated resistance case, the resistances after the devices have been fractured and the resistances after the

devices have been healed. The fabricated 70 nm thick Ag interconnect has a length of 775 µm and a width of 10 µm which gives a theoretical resistance of approximately 45 Ω, based on the thin film resistivity value of 127 µΩ.cm given

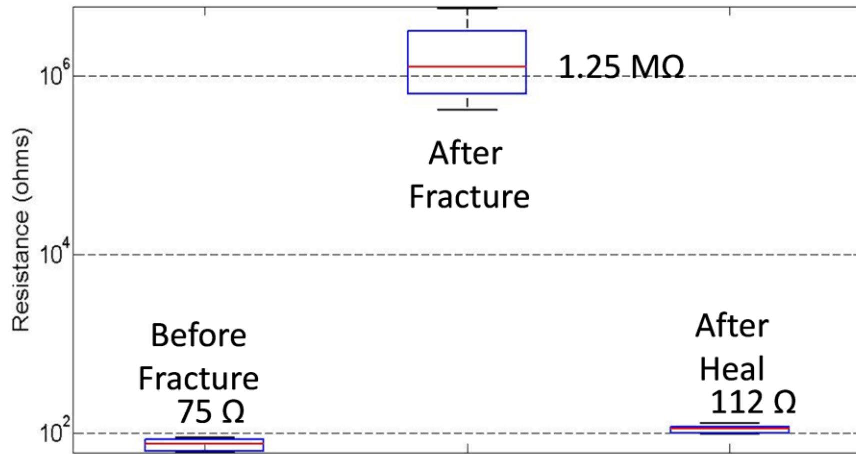


Fig. 13. Interconnect resistance distributions before fracture, after fracture and after healing. Each box represents the result of 10 samples.

in [74]. The average resistance measured before fracture is 30 Ω higher than this, which we believe is due to thickness variations in the film following deposition and the series resistance of the probe contacts and test system connections. We see that the resistances of the broken and healed states differ by about 3 orders of magnitude, however, the difference in resistance between the healed and unbroken interconnects is only a few tens of ohms on average for this compliance current. This validates the healing process, in which the goal is to restore the resistance of the interconnect close to its original value.

The elevated resistance after fracture given in Fig. 13 represents the resistance through the unbroken flexible solid electrolyte because of the lack of

continuity in the overlying Ag layer. This resistance can be used to estimate the size of the gap, assuming the crack spans the full width of the interconnect and the electrolyte maintains its original thickness and continuity after stressing. Since the resistivity of the solid electrolyte is in the order of 100 Ω.cm [4] and the resistance of the fracture (1.25 MΩ) may be calculated as shown below:

$$\frac{\rho_{Ge\text{-}Se} \cdot L}{W \cdot t} = R_{off} \qquad (1)$$

The estimated length L for a 60 nm thick, 10 µm wide (W) electrolyte in the gap is 750 nm. Note that such a small gap is difficult to image with an optical microscope and exposure to electrons in a scanning electron microscope stimulates electrodeposit growth which masks the gap features. Hence, we can only infer the break dimensions from the above calculations. The difference between the original and the healed resistance states (ΔR) is 37 Ω and this is the effective resistance of the electrodeposit itself. The bridging electrodeposit is likely to grow in a short dendritic pattern on the surface of the electrolyte between the fractured edges of the interconnect [75] but we can simplify this by assuming that the deposited connection can be approximated by a bar with an equilateral triangular cross-section which spans the length of the crack. Such geometry is typical in thick surface electrodeposits, in which the base of the feature is continually widened as the top is pushed upwards by the electrodeposition process [76]. For this geometry, we use the following set of equations to determine the dimensions of the electrodeposit:

$$\frac{\rho_{electrodeposit} \cdot L}{A} = \Delta R \qquad (2)$$

$$A = a^2 \frac{\sqrt{3}}{4} \qquad (3)$$

Here a is the length of the side and A is the area of the equilateral triangle respectively.

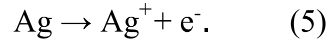
Using a value of 127 μΩ.cm for the resistivity of the Ag electrodeposit [74], the side of the equilateral triangle was calculated as 243 nm. The volume of the silver electrodeposit (V) is calculated to be $19.3\text{x}10^{-3}$ μm^3 using $V = A \cdot L$, where A is the area of cross-section of the electrodeposit and L is the crack length as before. The number of silver atoms that need to be reduced in order to produce this volume is then calculated using the following equation:

$$N_{Ag} = \frac{Density_{Ag} \times Volume_{Ag} \times NA}{At.\ Wt._{Ag}} \qquad (4)$$

The density of Ag is 10.49 g/cm^3, the atomic weight of Ag is 108, and the Avogadro number (NA) is $6.023\text{x}10^{23}$ atoms/mol. This gives us a value of $1.13\text{x}10^{9}$ atoms in the electrodeposit.

The electrodeposition current during the healing process is assumed to be limited by the initial fracture resistance (1.25 MΩ) and the healing voltage (2V), i.e., 1.6 μA. Note that the much higher compliance current is used to maintain sufficient voltage across the electrodeposit in order to continue the electrodeposition process and reach the lowest resistance. Most of this current flows through the metallic electrodeposit but the current responsible for continued deposition will still be flowing in the electrolyte and hence will remain in the μA

range during the entire growth time. The number of Ag ions to be reduced is equivalent to the number of atoms in the electrodeposit. These ions are reduced according to



$$Ag \rightarrow Ag^{+} + e^{-}. \qquad (5)$$

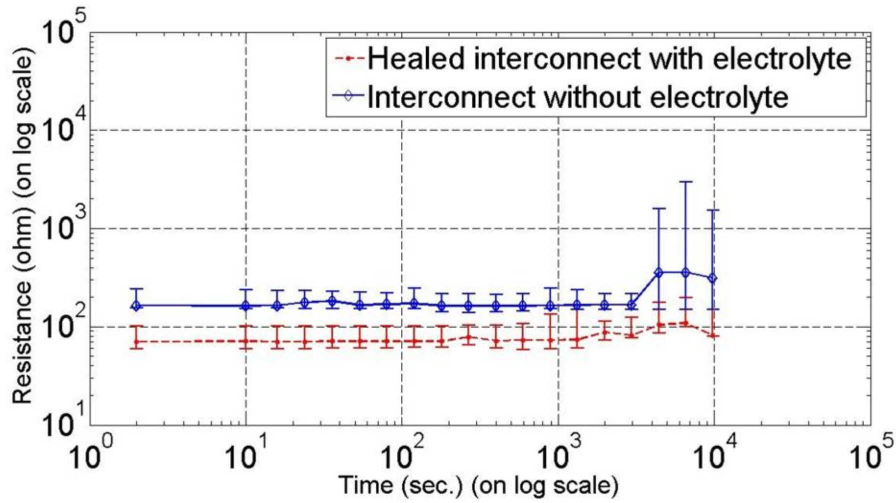


Fig. 14. Analysis of measured resistance values of interconnects with and without an underlying solid electrolyte layer. A constant current of 100 uA is applied to the interconnects for 3 hours.

requiring one electron per Ag^{+} ion for reduction. The time required for the break to heal is calculated using the equation given below:

$$t_{heal} = \frac{N_{Ag} \times 1.6 \times 10^{-19}\ C}{I_{min}} \qquad (6)$$

The numerator represents the total charge required to create the electrodeposit. Using this, the calculated value for healing time is 113 µs.

C. Reliability testing of the interconnects

DC current stress behavior of a healed interconnect structure, repaired at 2 V with 10 mA current limit, was compared to that of a silver interconnect without solid electrolyte. The current in all structures was maintained at 100 µA, leading to a current density of approximately 0.14 MA/cm^2, which is around one tenth the critical current density required to cause electromigration in Ag [26]. The testing was performed on 10 individual structures, with and without underlying solid electrolyte, and the measured values averaged as before. The average resistance of the structures is in the order of 100 Ω, which, for the stress current used, results in a potential difference of 10 mV along the conductors. Note that this voltage drop is too small to induce significant electrochemical effects during testing as the threshold for such reactions in this material system is 122 mV, as noted previously. The results for 3 hours of current stressing are shown in Fig. 14. The plot demonstrates that the resistance of both test structures (with or without solid electrolyte) does not change appreciably over the test period at these current magnitudes. The slight increase of resistance in both structures near the end of the test period is thought to be due to the degradation of the contact between the probes and the interconnect pads over time due to environmental factors. The difference in resistance between the two sample types is due to different average thicknesses of the Ag film on the two samples. These results suggest that at low current densities, the healed interconnect structure performs as well as the metallization without the solid electrolyte layer in terms of stability. The effect of constant voltage stressing at higher DC current density on Ag metallization on a

solid electrolyte layer was also assessed. Fig.15(a) shows the resistance vs. time plot for a constant voltage stress of 500 mV. Note that unlike the previous case, this voltage is sufficient to promote electrochemical effects. The current density in this case is 0.71 MA/cm^2, which is higher than before but still not above the critical current for electromigration. The interconnect maintains its initial

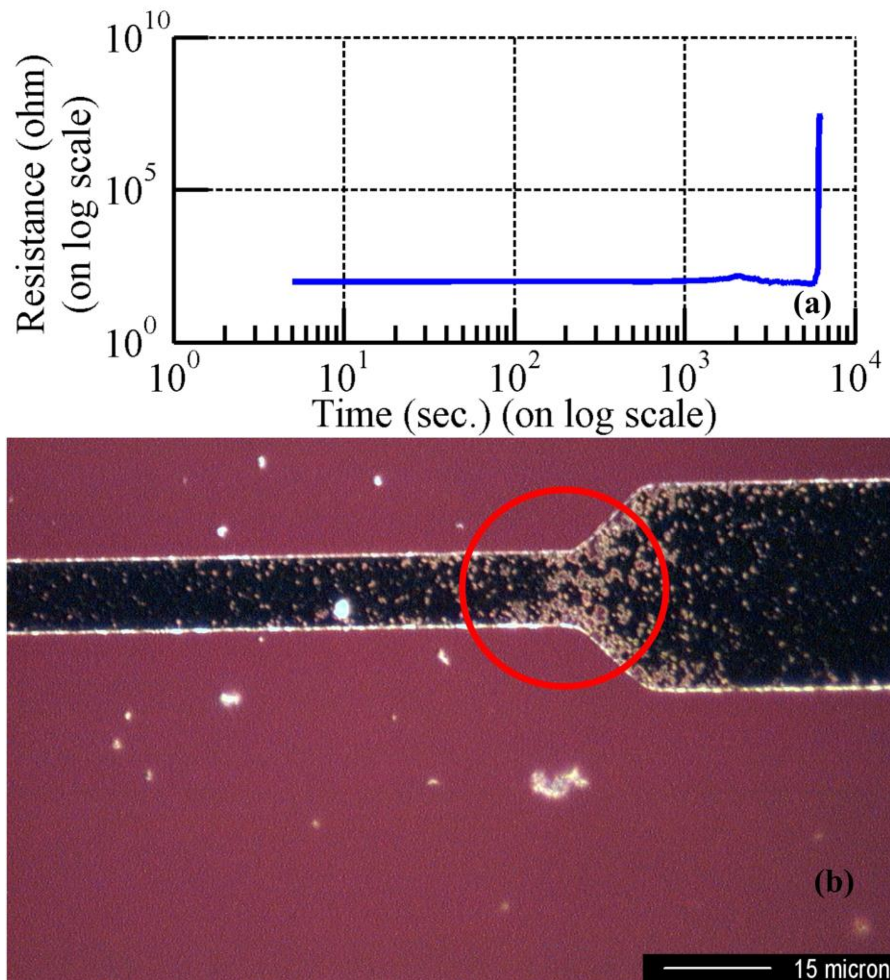


Fig. 15. (a) Constant voltage stressing of fabricated interconnect with a DC stressing voltage of 500 mV. The plot shows the variation of resistance of the metallization as a function of time. (b) Micrograph of the site of failure of the interconnect (circled).

resistance of approximately 100 Ω for around 2000 sec, at which point resistance fluctuations become evident. Continuity is disrupted around 6200 sec, which is very much lower than the expected time for electromigration-induced failure at the current density used [77]. An optical micrograph of part of the interconnect structure after failure is shown in Fig. 15(b). This section of the metallization shown in the figure was made positive with respect to the other end during stressing. The removal of silver from the area where the metal pattern narrows is clearly visible in the image (circled). These results suggest that, with sufficient potential difference, the underlying solid electrolyte layer promotes silver transport away from the "anode" or positive end (opposite to the direction of material movement expected in the case of electromigration) and this leads to the

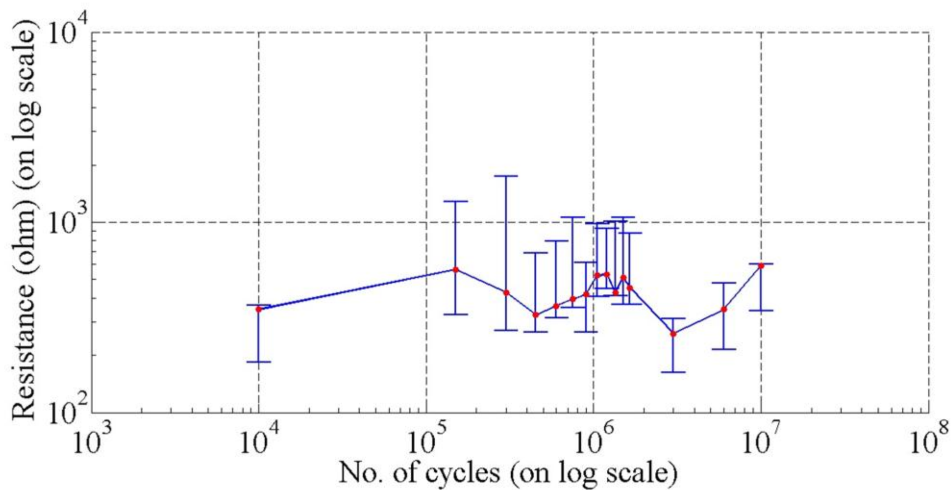


Fig. 16. Statistical analysis of the resistances of 5 interconnect devices after healing when subjected to AC voltage stressing. The plot shows the median of each resistance state (solid line) and the error bars show the 1st quartile and the 3rd quartile resistances associated with the corresponding number of cycles.

early failure observed for these electrical stressing conditions. The behavior of the healed solid electrolyte interconnect under AC voltage stress was also investigated. The samples were subjected to mechanical stress as before to induce failure in the interconnect and a 10 mA compliance current at 2 V was used in the healing process. The healed interconnects were then electrically stressed using a periodic square wave of 1.5 V amplitude and a frequency of 5 kHz. A series resistance of 1 kΩ was placed in series with the test structure to limit the test current. The AC current density in this test was around 0.1 MA/cm^2. Fig. 16 shows the results of the analysis of the resistance changes in 5 of the interconnect structures. The variations in the resistances over time are less than an order of magnitude, indicating that the healed interconnect is stable under AC bias. An increase in resistance towards the end of the test period is evident and this is again attributed to a probe contact issue, where the probes gradually drift across the contact pads over time due to slight vibrations in the test apparatus, and the effects of joule heating at the contacts due to current crowding and subsequent transport of material away from the points of contact.

The performance of the healed solid electrolyte interconnect structure was compared to that of the unbroken interconnect at low AC voltages. Fig. 17 shows the performance of both the fabricated and the healed interconnect samples. The resistance of the interconnects increases by a factor of about 1.4 after the healing process. The plot shows that the difference between the fabricated and the healed types of interconnects are statistically insignificant, demonstrating that the

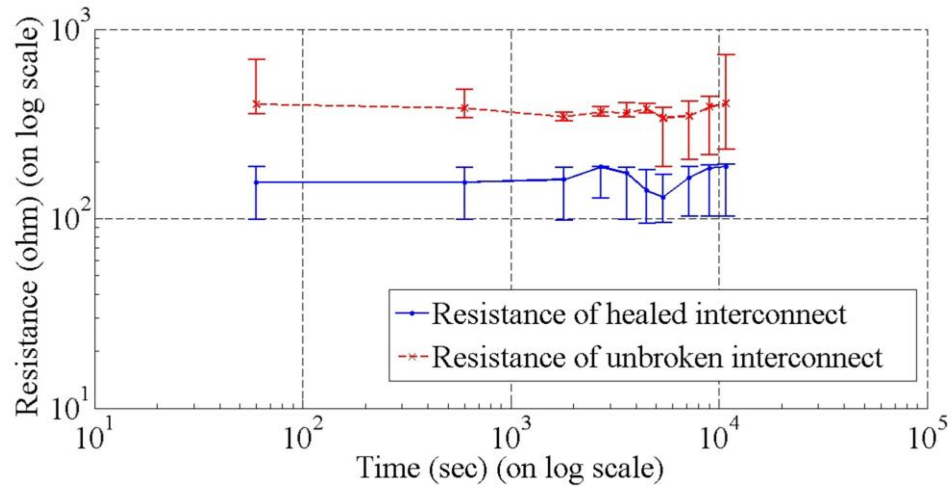


Fig. 17. AC testing of fabricated and healed interconnects. The stressing current density was 0.2 MA/cm^2. Healing conditions were 2 V and 10 mA compliance current.

electro-deposit largely preserves the properties of the originally fabricated interconnect when AC voltages are applied.

D. D.C. failure model for the interconnects

The plot in Fig. 15 shows the failure of the solid electrolyte interconnect when subjected to D.C. voltages of above a few hundreds of mV. This failure was

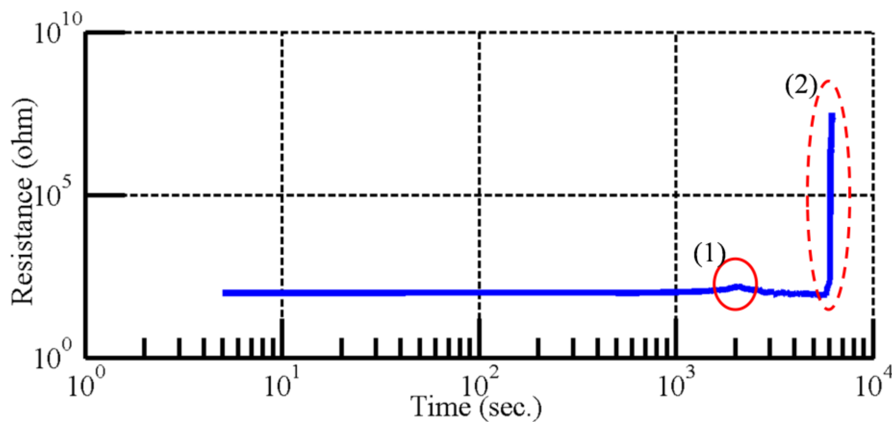


Fig. 18. Plot of resistance as a function of time for a stressing voltage of 500mV showing the saddle point (1) and final failure (2).

analyzed further so that a model could be developed to explain device failure based on the material characteristics of the device. Fig. 18 shows the same plot in Fig. 15 with two important points in the resistance evolution of the interconnect which are characteristic of this failure. The first is a saddle point, during which phase the resistance of the interconnect quickly increases before beginning to decrease again. The second point is usually a more gradual increase in resistance with a sudden catastrophic failure of the resistance at the very end. This time-to-failure is a function of both voltage and temperature. The model involved finding the dependence of the time-to-failure on the temperature and the applied stressing voltage and then relating them to the physical mechanisms which may have led to the failure. The two sections below show the development of the model.

1. Behavior of the time-to-failure as a function of applied voltage

This section shows the behavior of the time-to-failure as a function of voltage and temperature. Fig. 19(a) shows the variation of the time-to-failure as a function of stressing voltage. The time-to-failure was defined as the time taken by the interconnect to reach 10 times the initial resistance. Each data point is the result of testing at least 10 interconnects with the same voltage and temperature conditions. The stressing voltage was varied between 0.9 V and 2.5 V. The current through the interconnect was limited by the resistance of the interconnect itself. We see that the time-to-failure varies as the reciprocal of the stressing voltage. This implies that the failure is primarily a drift-driven process. The resulting electric field causes the ions at the interface of the metal and the solid electrolyte to drift towards the lower potential. The loss of these ions induces

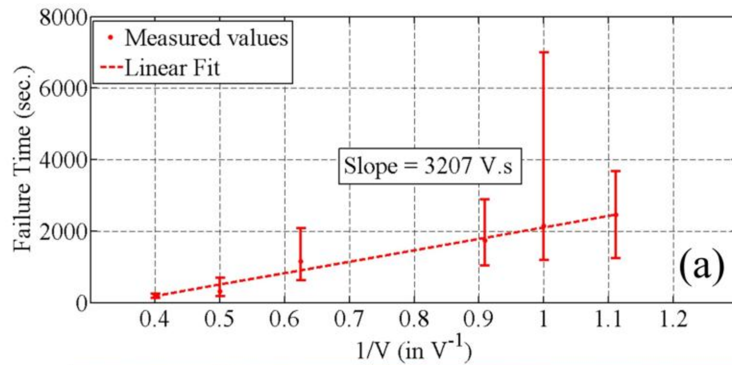


Fig. 19. (a) Time-to-failure as a function 1/V shows a linear relationship. (b) Image using differential interference microscopy shows the site of failure of the interconnect to be at the end where the higher voltage is applied. The site shows a change in thickness in the circled region.

some of the metal to ionize and move into the electrolyte at the interface. This process is self-sustaining and results in a gradual increase in the interconnect resistance over time and eventually results in interconnect failure. Fig. 19(b) shows an interference microscopy image of the interconnect which shows thickness variations near the anode end of the interconnect. We clearly see the gradual change in the metal thickness along the length of the interconnect.

The development of a model for this failure was done based on this mechanism. The model assumes that the thickness of the interconnect is uniform along its entire length. The resistance of the interconnect is then calculated as shown below:

$$R(t)=\frac{L}{\sigma_e W \tau(t)} \qquad (1)$$

Here R(t) is the time-dependent resistance of the interconnect, L is the length, which is 775 μm, W is the width of the interconnect, which is about 10 μm, σ_e is the electron conductivity in very rough silver films, which is about $2x10^4$ S/cm [74] and τ(t) is the time-dependent thickness of the overlying metal portion on the interconnect. Differentiating the above relation and solving for the thickness variation as a function of time we get the following relation:

$$\frac{\delta\tau}{\delta t}=-\frac{L}{\sigma_e W R^2}\frac{\delta R}{\delta t} \qquad (2)$$

The following equation gives the rate of change of volume (ν) with respect to time:

$$\frac{\delta\nu}{\delta t}=WL\frac{\delta\tau}{\delta t} \qquad (3)$$

Using eq. (2) in this relation, we get the following:

$$\frac{\delta\nu}{\delta t}=-\frac{L^2}{\sigma_e R^2}\frac{\delta R}{\delta t} \qquad (4)$$

The rate at which volume changes can be related to the rate at which the atoms in the interconnect are being lost to the electrolyte from the metal by the following equation:

$$\frac{\delta n}{\delta t}=\frac{D_{Ag}N_A}{M_{Ag}}\frac{\delta \nu}{\delta t} \qquad (5)$$

The density of Ag is D_{Ag} = 10.49 g/cm^3, the Avogadro number N_A = 6.023x10^{23} and the molecular weight of Ag is M_{Ag} = 108.

Using eq. (4) in eq. (5), the rate at which atoms are lost to the electrolyte is related to the resistance by the relation shown below:

$$\frac{\delta n}{\delta t}=-\frac{D_{Ag}N_A L^2}{M_{Ag}\sigma_e R^2}\frac{\delta R}{\delta t} \qquad (6)$$

The ion current density can then be calculated from the above relation by multiplying with the Ag^+ ion charge q = 1.6x10^{-19} C and dividing it by the cross-sectional area of the Ag^+ ion current A = W.$\tau(t)$ and substituting for $\tau(t)$ using eq. (1):

$$J=-\frac{D_{Ag}N_A L q}{M_{Ag}R}\frac{\delta R}{\delta t} \qquad (7)$$

We now use the relation $J = \sigma_{Ag}E_{elec}$ [78] where σ_{Ag} represents the conductivity of Ag in the Ag-Ge-Se electrolyte and is about 1.1x10^{-5} S/cm [4, 79], E_{elec} is the electric field in the electrolyte. The electric field is given by $E_{elec} = -\lambda V_A/L$ where V_A is the applied stress voltage and λ is the ratio of mobilities of Ag in the electrolyte and electrons in the overlying metal layer. This correction is necessary because the derivation so far assumes that the entire current which is observed is due to ions. However, this is not true since the current through the overlying metal layer is predominantly carried by electrons. The observed current density is the sum of the electron current density and the ion current density. Modifying eq. (7)

with these relations, we get the expression the rate of change of resistance as shown below:

$$\frac{1}{R}\frac{\delta R}{\delta t}=\frac{M_{Ag}\sigma_{Ag}\lambda V_A}{D_{Ag}N_A L^2 q} \qquad (8)$$

Integrating and solving for R(t), we get the result shown below:

$$R(t)= R_0 e^{\beta V_A t} \qquad (9)$$

where

$$\beta=\frac{M_{Ag}\sigma_{Ag}\lambda}{D_{Ag}N_A L^2 q} \qquad (10)$$

Eq. (9) shows that the resistance of the interconnect increases exponentially with time and the applied stress voltage. The time-to-failure (t_f)

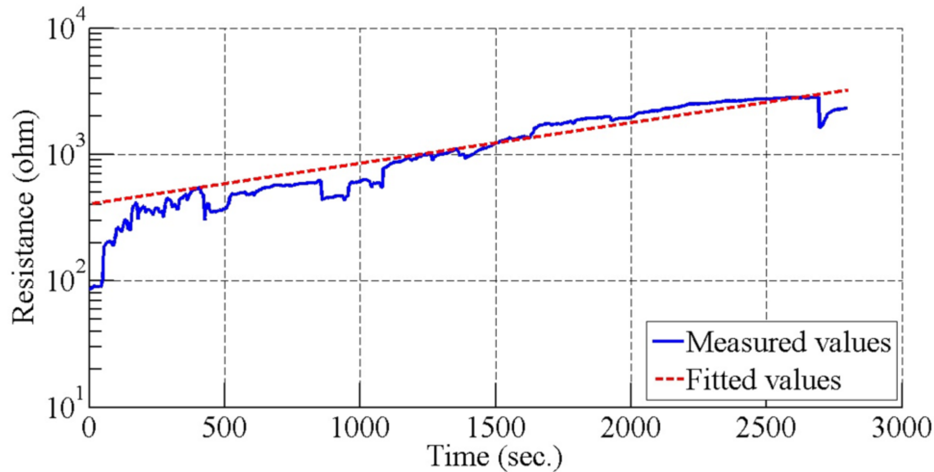


Fig. 20. Plot of resistance as a function of time comparing fitted and observed response.

may be calculated by assuming that the resistance at t_f is 10 times the initial resistance R_0. This gives us the result:

$$t_f=\frac{1}{\beta V_A}\ln(10) \qquad (11)$$

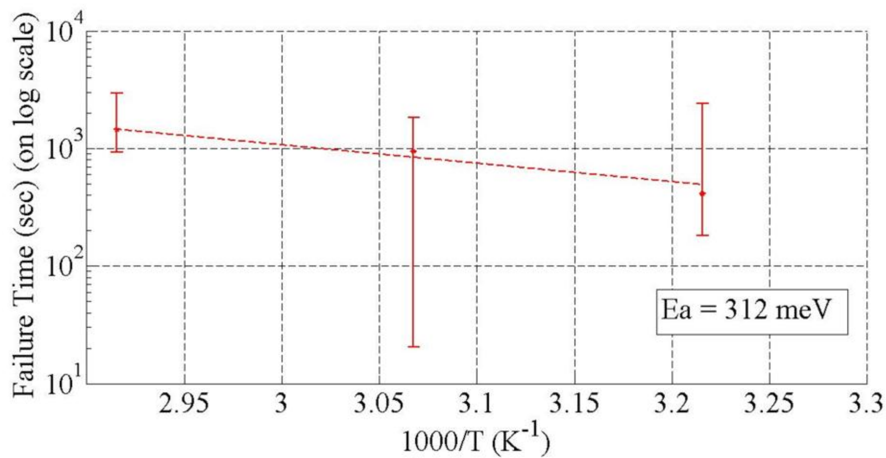


Fig. 21. Failure time as a function of 1000/T. The extracted activation energy for the interconnects is shown.

Eq. (11) shows that the time-to-failure is inversely dependent on the applied voltage. Using the slope from Fig. 19(a), we calculate the value of λ to be 6.1×10^{-5}, which matches the ratio of the electron to ion mobility in Ag-Ge-Se system published previously [79]. An illustrative plot of resistance as a function of time is shown in Fig. 20. The observed response is compared with the resistance calculated based on eq. (5). We see that the calculated values fit the observed values except during the initial portion of the stressing. It is assumed that this is the saddle point which is observed during the initial stressing phase. This shows that the failure is primarily driven by electrochemical drift of the ions. However, other mechanisms seem to accelerate the failure during the initial phase.

2. Behavior of the time-to-failure as a function of temperature

The applied voltage was kept constant at 1.6 V during temperature stressing. The temperature was varied between 90°C and 120°C. The resistance

evolution was observed as a function of time for 10 devices at each temperature point and an Arrhenius plot of the time-to-failure was made. Fig. 21 shows this plot. The activation energy (Ea) of the failure was extracted, which is shown to be 0.31 eV. This activation energy corresponds to the conductivity of Ag^+ ions in the Ge-Se matrix. This further shows that the failure of the interconnect is because of the drift of Ag^+ ions through the Ge-Se matrix.

3. <u>Behavior of the saddle point as a function of applied voltage and temperature</u>

The time at which the saddle point is reached was observed as a function of applied voltage. The voltage was varied between 0.8 V and 1.2 V. The

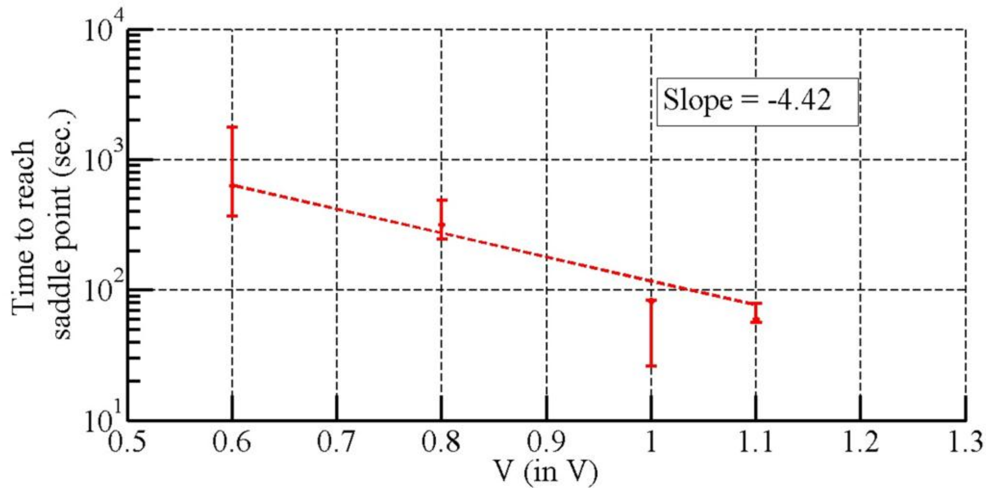


Fig. 22. Plot of time to reach saddle point as a function of stressing voltage shows exponential dependence.

temperature at which this point was measured was at 90°C. Ten devices were tested at each voltage point to get a median time at which the saddle point is reached. A plot of this time as a function of applied voltage was plotted. Fig. 22 shows this plot. The plot shows an exponential dependence of the time at which

the saddle point is reached to the applied voltage. One of the mechanisms we propose is that the appearance of this point shows the duration for which the transport mechanism is charge-transfer limited. In such a case, the Butler-Volmer equation [80] would dictate the appearance of the saddle point, which would explain the exponential behavior. However, further characterization of this point is required before a conclusion for the mechanism is reached.

This scenario is further supported by the Arrhenius plot of the time to reach saddle point shown in Fig. 23. The temperature was varied between 70°C

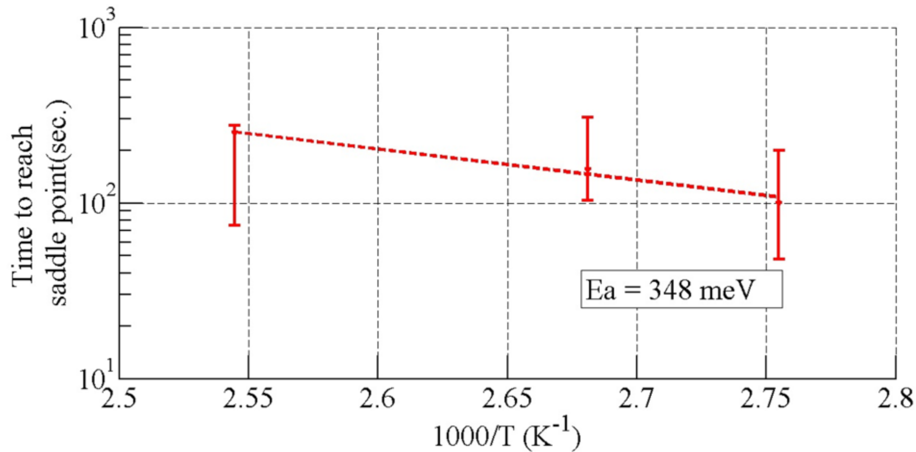


Fig. 23. Arrhenius plot of time to reach saddle point as a function of temperature.

and 120°C and interconnects were stressed using a voltage of 1 V. Each data point was again the result of measuring ten devices. The activation energy from the plot is about 0.35 eV, which again corresponds to the activation energy of the conductivity of Ag^+ ions in the Ge-Se electrolyte.

The characterization results discussed above show that the d.c. response of the solid electrolyte interconnect arises from two mechanisms. The first

mechanism is an electrochemical drift of ions and the resulting reduction of atoms from the overlying metal line, which causes an increase in resistance. The other mechanism which is observed is the electrochemical drift of the ions already in the electrolyte. At the beginning of the stressing, when the electrolyte is saturated with ions, the second mechanism dominates, with the saddle point being reached and the reaction being limited by the Butler-Volmer equation. Towards the latter half of the failure, the resistance change is determined more by the conversion of atoms to ions from the overlying metal line. These two mechanisms both cause a rise in resistance and eventual failure of the metal line.

COPPER BASED SOLID ELECTROLYTE INTERCONNECTS

The preceding section demonstrated that the silver based solid electrolyte showed self-healing properties. Further, the fact that the healed interconnects displayed similar behavior as the unbroken interconnects was also shown for both low d.c. and a.c. voltages. However, at d.c. voltages of the order of a few hundred mV, the interconnects demonstrated an electrochemical mode of failure. The silver overlying layer was replaced by copper to investigate if this would result in an improvement in the d.c. voltage that could be tolerated. This section presents the results of the fabrication and characterization efforts that were undertaken in this direction.

A. Fabrication

The copper based interconnects were fabricated in a manner similar to the silver interconnects. The flexible substrate, which was polyimide as mentioned in the previous section, was first bonded onto the rigid Si substrate using double-sided carbon tape. The substrate was then cleaned using a combination of acetone, iso-propanol and methanol before being rinsed in DI water. HMDS, followed by AZ-4330 photoresist, was spun on the substrate at a rate of 3500 rpm for about 30 sec. The sample was then soft-baked for about 17 min. in an oven at about 80°C. The next step involved exposing the sample through the interconnect pattern mask for about 45 sec. The incident power was about 5 mW/cm^2 and the wavelength of U.V. light was 436 nm. The pattern was then developed in the AZ-300 MIF developer for 90 sec. The germanium selenide layer was then deposited thermally. The base pressure was $3x10^{-6}$ Torr at a current of about 46 A. The source was

evaporated through a tungsten boat which was covered by a platinum wire mesh to simulate a semi-Knudsen cell. The deposition rate was about 1 Å/s and the final thickness was 60 nm. The copper was deposited by electron beam evaporation at a base pressure of $3x10^{-6}$ Torr. The thickness of this film, which would be photo-dissolved, was about 30 nm and was deposited at a rate of about 1 Å/s. The e-beam voltage was 10 kV, with the current being 70 A. The copper was then dissolved into the germanium selenide layer by exposing the sample to U.V. light with an intensity of about 8 mW/cm^2 and a wavelength of 436 nm for 20 min. The overlying metal interconnect layer was then deposited using the same electron beam evaporation conditions. The thickness of this layer was 60 nm. A lift-off step in acetone, which lasted about 4 hours, completed the process. The final structure of the device is shown in Fig. 24.

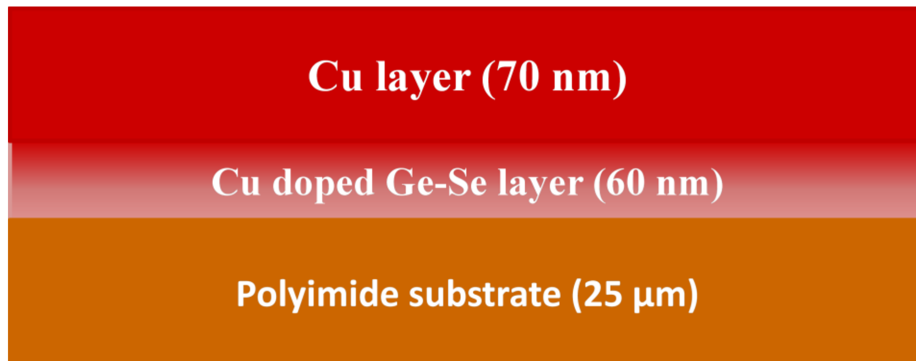


Fig. 24. Cross-section of the copper based germanium selenide solid electrolyte interconnect.

B. Characterization

The copper based interconnects were characterized for their healing potential. Fractures were induced in the interconnects by bending the across a

radius of 5 mm for 5 min., as was done for the silver based interconnects. This process was repeated multiple times to ensure that a large fraction of the

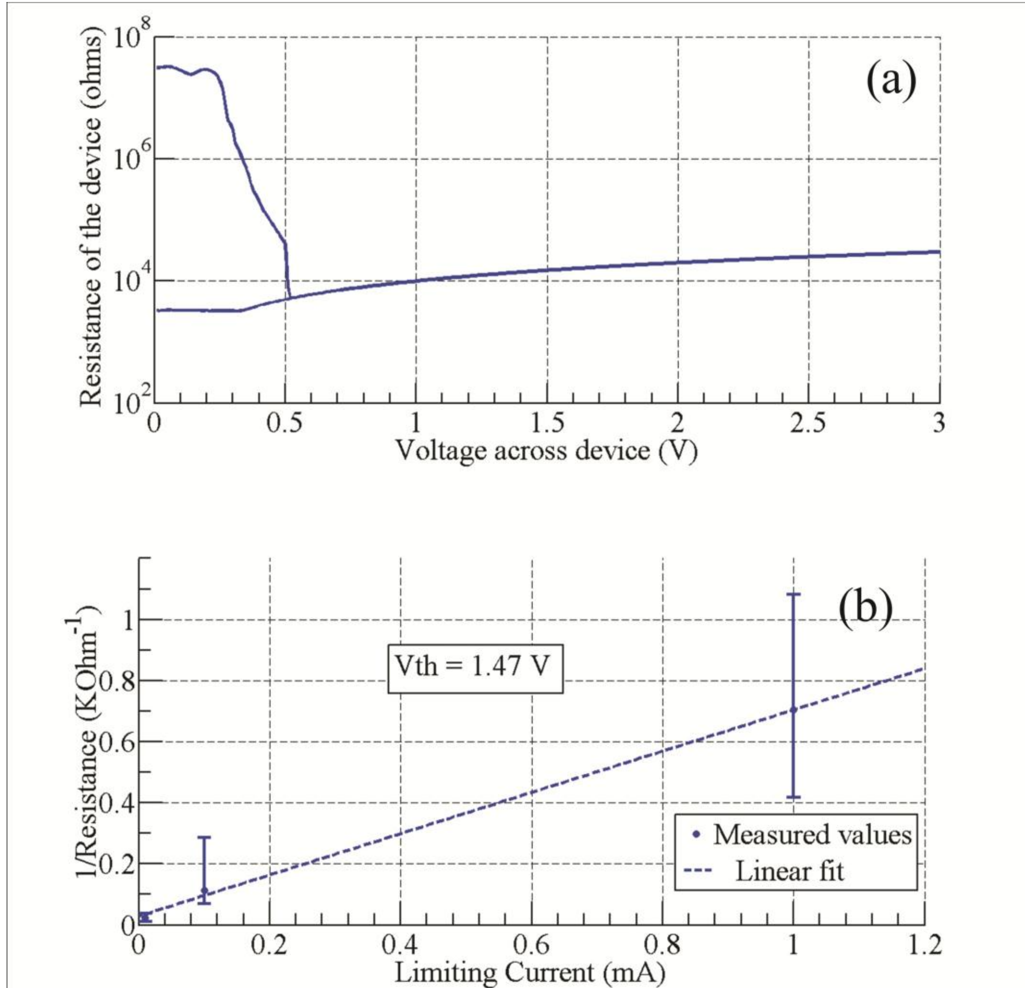


Fig. 25. (a) Resistance-voltage sweep to induce healing in the interconnect. The compliance current was 100 μA. (b) Plot of on-state conductance as a function of limiting current shows a linear dependence.

interconnects underwent mechanical failure. The devices were then tested for the healing property. The tendency of the interconnect to undergo electrochemical failure was also evaluated. Preliminary results of these tests are presented.

1. The self-healing property

A sample of copper based solid electrolyte interconnects was subjected to mechanical stress. This induced a fraction of the interconnects to fracture. These were then healed based on different compliance currents. A voltage sweep from 0 to 2 V was used to heal the interconnects. The resistance was read in the ohmic region on the reverse region of the sweep. Fig. 25(a) shows the variation of resistance as a function of applied voltage. The fracture resistance is about 10 MΩ, as observed. The interconnect heals at around 0.7 V and the measured resistance at this stage is dictated by the limiting current. During the reverse sweep, we see the ohmic region, which is observed as the constant resistance region. The resistance does not vary at this stage as the voltage is too low to sustain electrodeposition. Fig. 25(b) shows the on-state conductance, which is the resistance in the ohmic region, as a function of limiting or compliance current. Each point for the observed values is the result of measuring ten devices at the same compliance current. This plot shows a linear relationship as expected for PMC devices. The reciprocal of the slope gives the secondary threshold voltage, which in this case is about 1.47 V. A higher threshold voltage is disadvantageous for healing, since it shows that a higher voltage is required to induce the healing process but could be advantageous in terms of reliability because of less voltage-induced drift during normal operation of the interconnect, according to the electrochemical failure theory presented in the previous section. Some preliminary results for the observed failure during D.C. stressing are presented in the next section to support this hypothesis.

2. D.C. voltage stressing

The interconnects were stressed with D.C. voltages of the order of a few volts, with no limit on the current flowing through them. Unlike the silver based interconnects, the copper based interconnects do not fail due to electrochemical ion drift at room temperature. At voltages above 4 V, the copper interconnects fail, probably due to joule heating. A darkening of the surface of the interconnect is observed, probably due to oxidation, which is accelerated by temperature [81]. Unpassivated Cu films undergo temperature-accelerated oxidation at much lower temperatures than the melting point of Cu. The electrochemical failure is better observed at higher temperatures and voltages. Fig. 26(a) shows the behavior of the interconnect to D.C. voltages above 2 V at 80°C. We see that the interconnect does not fail in under 3 hours until the voltage reaches about 2.5 V. At this voltage, we clearly see a failure in 2 stages, as seen for the silver based interconnects. The fact that the interconnect does not fail at high voltages and currents, coupled with the requirement for high temperature, makes the copper based self-healing interconnects a very promising candidate for a reliable interconnect technology for flexible electronics in the future. However, a much more detailed study of the reliability of these interconnects needs to be executed before the feasibility of using them in applications can be evaluated. Fig. 26(b) shows that, unlike the silver based solid electrolyte interconnect in which the failure happens in the bulk of the material, the Cu based interconnect loses material along the edges. Further research is required to investigate why the

mechanism of transport favors material transport along the edges in the case of copper.

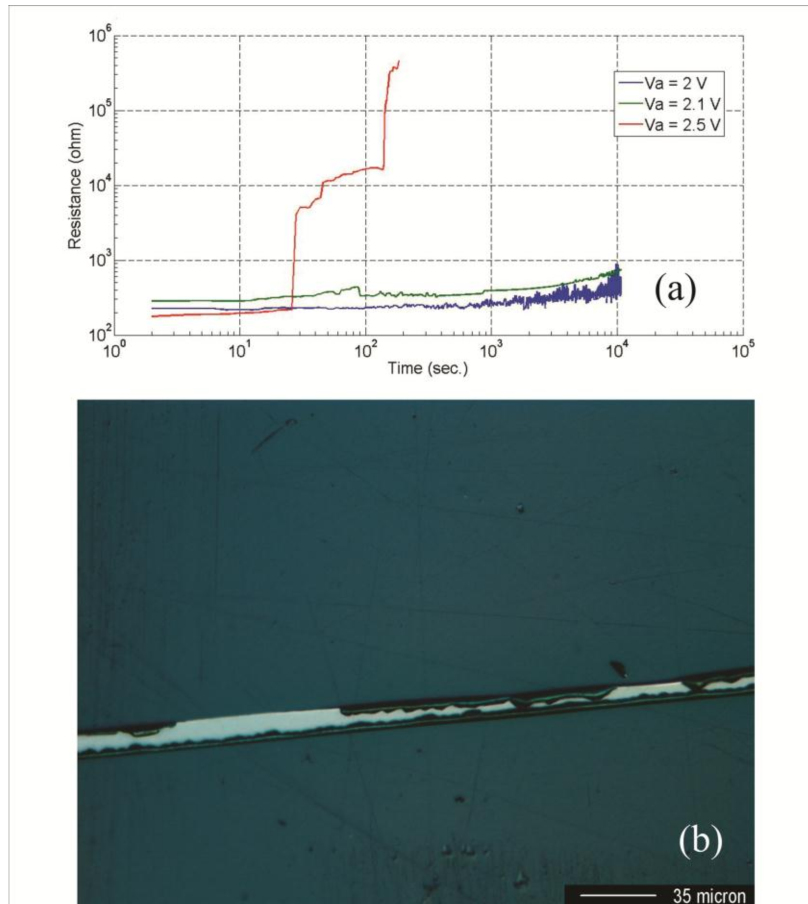


Fig. 26. (a) shows the failure of the interconnect at different voltages. (b) shows the movement of the metal along the edges of the interconnect. The interconnect failure due to electrochemical action is not dominant until the temperature reaches about 80°C and the interconnect does not fail under 3 hours at lower temperatures.

C. Reliability testing of the interconnects

The goal of the reliability testing of the interconnects was to investigate if the Cu-based interconnects could operate at higher current densities than the Ag based interconnects over 3 hours. The testing was done for 3 different phases of

interconnect operation. Ten devices were tested in each phase to ensure statistically reliable results. In the first phase, Cu interconnects without an underlying solid electrolyte layer were subjected to a current density of about 1 MA/cm^2 for about 3 hours by applying a constant voltage of 1 V across them. The results of these tests were considered the control sample as they represent the behavior of the standard Cu based interconnect. The results of the subsequent tests were compared with the control sample. The second phase involved subjecting Cu interconnects with an underlying Cu-Ge-Se solid electrolyte layer to similar current densities in the manner outlined above. This represents the behavior of the solid-electrolyte interconnect during normal operation, without any fractures induced in it. The third phase of testing involved inducing fracture in the solid electrolyte based interconnects by bending the sample around a mandrel of diameter 5 mm repeatedly. The resulting fractured interconnects were then healed by applying a voltage of 3 V with a limiting current of about 10 mA. These healed interconnects were then subjected to the current densities and voltages mentioned for the previous two phases. The results of this testing would reveal if introducing an underlying Cu-Ge-Se solid electrolyte results in a reduction in reliability at these current densities, and if healed interconnects perform as reliably as unbroken interconnects at these current densities.

Fig. 27 shows a plot of resistance as a function of time for all three phases. We see that the control sample shows almost no change in resistance at a current density of 1 MA/cm^2. This is expected as Cu interconnects are much more reliable than Ag interconnects as they are more resistant to electromigration. The slight

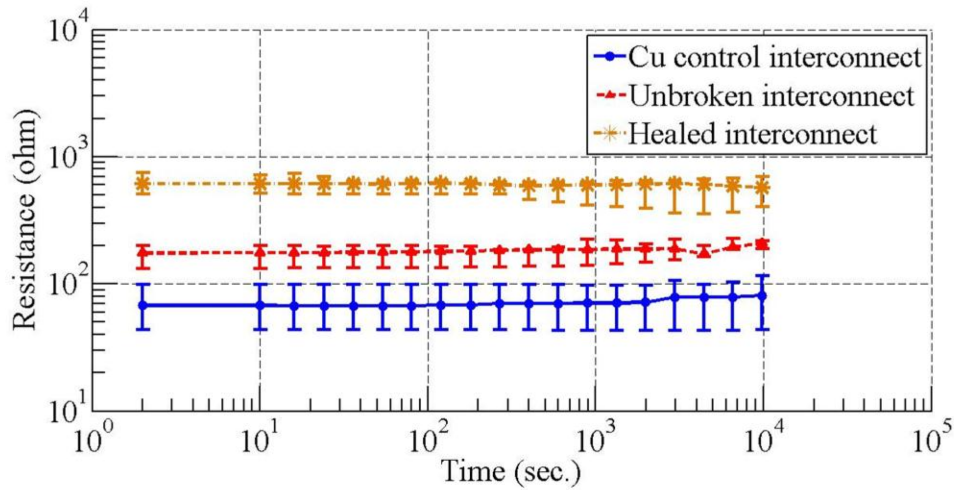


Fig. 27. Resistance as a function of time for Cu based interconnects. The current density is 1 MA/cm^2.

increase in resistance could be attributed to Joule heating at the probes and possibly due to some oxidation at the surface of the unpassivated film. The Cu interconnect with an underlying solid electrolyte, labeled “Unbroken interconnect”, shows a behavior very similar to the control sample. This leads to the conclusion that the introduction of the underlying solid electrolyte film in the interconnect does not impact the reliability of the interconnect at these current densities. The behavior of the resistance of healed solid electrolyte interconnect shows a slight reduction of the resistance over time. This plot demonstrates that the healed interconnect performs as reliably as the unbroken solid electrolyte based interconnect, and the control sample at the current densities used in the testing of these devices. Another observation from the plot is that the healing process reliably causes the resistance of the healed interconnects to be within an

order of magnitude of the unbroken interconnects and produces a healed resistance, which is stable over time.

This analysis shows that the Cu based interconnects are much more stable than Ag based interconnects. The unbroken and healed states of the Cu base interconnects remain stable at about 1.5 times the current density at which the Ag based interconnects are observed to fail. The Cu based interconnects can also operate at higher voltages. This means that Cu based interconnects can operate at higher power levels than Ag based interconnects. The calculated critical power density for Ag based interconnects from Fig. 15 is about 0.35 MW/cm^2. The Ag interconnect cannot be used beyond this power level, as it will fail in less than 3 hours. The Cu based interconnect remains stable at power densities of 1 MW/cm^2, as seen from Fig. 27. Thus, Cu based interconnects can handle power which is at least 3 times as high as the power which can be handled by Ag based interconnects.

SILVER DOPED GERMANIUM SELENIDE BASED SWITCHES FOR FLEXIBLE SUBSTRATES

The previous chapters have dealt with interconnect reliability, by ensuring the integrity of interconnects, even after being subjected to fractures. Another important aspect of reliability is reconfigurability of circuits. This ensures that many alternative paths exist for re-routing, should some parts of the circuit suffer catastrophic failure, thus minimizing loss of function. This chapter presents research done to adapt PMC devices as reconfigurable switches. Silver doped germanium selenide based switching devices have been demonstrated as memory devices for both rigid [1, 2, 5, 82] and flexible substrates [7, 72]. The ability of these switches to function when subjected to mechanical strain has also been qualitatively demonstrated [7, 72]. Although these devices have been extensively studied empirically [76, 83, 84], along with the materials that comprise the device [73, 79, 85-87], no satisfactory compact model exists which predicts the behavior of the device. This section provides the details of fabrication of a PMC device on a flexible substrate and proposes a compact model for this device. It also presents characterization results for this device which support the model. The model also shows that memristance is an emergent property of the device [64], which would make it useful as an element in computational logic circuits.

A. Fabrication

The fabrication process is an extension of the process described in [7]. The flexible polyimide substrate is bonded to a silicon substrate to prevent its deformation during the fabrication process using double-sided carbon tape. The

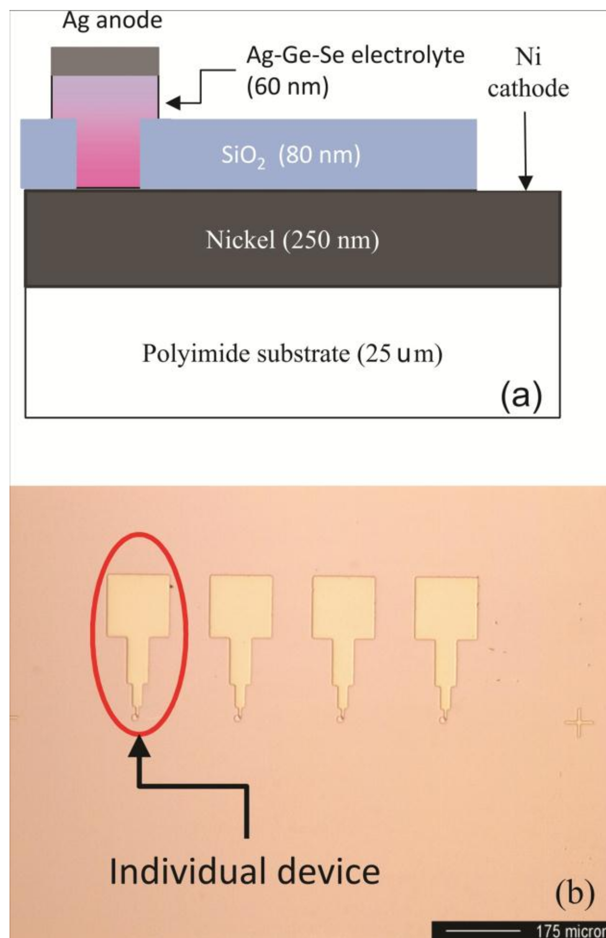


Fig. 28. (a) shows the different device layers with layer thicknesses. (b) shows the top view of the device, in which an individual device consists of a via between 2 µm to 10 µm in diameter and terminates in a square pad with an edge of 100 µm. The Ni cathode (not shown in fig.) is common to each die.

bottom cathode layer is an inert metal layer, which in this case in nickel (Ni). The insulating layer is deposited silicon dioxide (SiO_2). Both these layers are deposited successively in an e-beam system without breaking vacuum. The deposition rates did not exceed 1.5 Å/s to ensure good uniformity. The base pressure was $3x10^{-6}$ Torr. The Ni layer is about 150 nm thick while the SiO_2 layer

is 80 nm thick. The cathode is common to each die and is patterned, along with the vias, using the AZ-4330 photoresist. HMDS is spun on to the wafer at 3500 rpm for 30 sec. Photoresist is then spun on the resist at 3500 rpm for 30 sec. The sample is soft-baked in an oven at $80^{o}C$ for 10 min. to drive off the solvent from the resist. The sample is then exposed to UV light about 400 mJ/cm^2 with a wavelength of 436 nm. The pattern is then developed using the AZ-300 MIF photoresist for 90 sec. The sample is now placed in a 20:1 BOE etch solution for about 2 min. to etch the oxide at the cathode and via locations to expose the Ni metal. The resist is then stripped in acetone and a new layer or resist is spun on. The anode is then defined using the resist patterning technique mentioned above. A germanium selenide layer ($Ge_{20}Se_{80}$) is deposited up to a thickness of 60 nm followed by about 30 nm of silver (Ag) without breaking vacuum by evaporation. The evaporation rate was about 1 Å/s at a base pressure of $3x10^{-6}$ Torr. Photo-dissolution of the Ag layer in the Ge-Se layer is done by exposing the sample to UV light of wavelength 436 nm at a power of 4 mW/cm^2 for about 20 min. Another Ag layer, which is 35 nm thick, was deposited as the top electrode, at a deposition rate of 1 Å/s and a base pressure of $3x10^{-6}$ Torr. A final lift-off step was carried out in acetone to produce the patterned switches. The resulting devices had vias with diameters that ranged from 2 µm to 10 µm. Fig. 28(a) shows the final structure of the device. Fig. 28(b) shows the top view of the fabricated device.

B. Programming model

When a positive voltage is applied to the anode with respect to the cathode, the device is said to be in the programming state. The device resistance is eventually determined by the limiting current. The proposed model for the device consists of a Schottky diode in parallel with a variable resistor as shown in Fig.

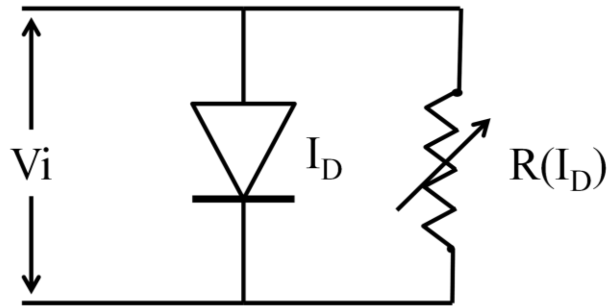


Fig. 29. Proposed programming model for the device.

29. The Schottky diode current represents the Faradaic current, while the variable resistor is the metallic wire between the two electrodes, which carries the electron current. The conductance of the variable resistor is a function of the integral of the diode current as the ions are reduced and collect on the metallic wire. A latent filamentary pathway [88, 89] is considered to exist between the electrodes at all times, including the off-state. Only the resistance of this filament varies as a function of applied voltage and time. The change in resistance is brought about by the reduction of Ag^+ ions on the electro-deposit. Such a model takes into account the behavior of the device to the current and the applied voltage. However, it does not take into account the initial formation of the Ag electrodeposit, and so cannot

be applied to analyze the initial few cycles of device behavior. It is important to note here that the Schottky diode does not represent the actual interface characteristic for the interface between the Ag electrode and Ag-Ge-Se solid electrolyte. The interface barrier is, in reality, a product of the formation of the Helmholtz Double Layer (DL) in the solid electrolyte, with the current characteristics being exactly described by the Butler-Volmer equation [90]. The theory of the Schottky diode, however, closely resembles the current-voltage relationship predicted by the Butler-Volmer equation. This is why the Schottky diode is used as an equivalent device in this model.

The derivation of the evolution of the resistance of the electro-deposit is based on the proposed model. If we assume that all the ionic current goes into the formation of the Ag electro-deposit, the rate at which the number of atoms being reduced is equal to the diode current. In such a case, if we assume a cylindrical cross-section of the electro-deposit initially and a uniform rate of reduction across the length of the electro-deposit, then the rate at which the electro-deposit area increases is given by the following relation:

$$\frac{dA}{dt} = \frac{M.I_D(t)}{D.N_A.h.e} \qquad (1)$$

Here M is the molecular weight of Ag, $I_D(t)$ is the diode current at time t, D is the density of Ag in the Ge-Se glass matrix, N_A is Avogadro's number, e is the charge on an Ag^+ ion and h is the height of the electro-deposit, which is also the thickness of the Ge-Se layer.

We know that the relationship between resistance and area of the resistor is as follows:

$$R(t)= \frac{\rho_{elec}.h}{A(t)} \qquad (2)$$

In this case, R(t) is the resistance of the electrodeposit, A(t) is the area of its cross-section and ρ_{elec} is the resistivity of the Ag electro-deposit in the Ge-Se matrix. This equation can be modified to the following relation:

$$\frac{dA}{dt} = -\frac{\rho_{elec}.h}{R(t)^2} . \frac{dR}{dt} \qquad (3)$$

Equating eqs. (1) and (3), we get,

$$\frac{1}{R(t)^2}\frac{dR}{dt} = -\frac{M \cdot I_D(t)}{\rho_{elec} \cdot h^2 \cdot e \cdot D \cdot N_A} \qquad (4)$$

where $I_D(t)$ is the standard Schottky diode current used in the above expression and is expressed by the following equation:

$$I_D(t)=A \cdot A^* T^2 e^{-\frac{\Phi_B}{k \cdot T}} \left(e^{\frac{V(t)}{n \cdot k \cdot T}} -1 \right) \qquad (5)$$

The evolution of the resistance of the electrodeposit is derived for some special cases shown below.

1. Constant voltage case: $V(t) = V_A$

The Schottky diode current is written as shown below:

$$I_D(t)=I_L[\exp\left(\frac{V_A}{n \cdot k \cdot T}\right) -1] \qquad (6)$$

This is then substituted in eq. (4). We also use the boundary condition, $R(0) = R_0$ and solve eq. (4). The result is shown below:

$$R(t)=\frac{R_0}{1+k_p \cdot I_L \cdot R_0 \cdot t \cdot [\exp\left(\frac{V_A}{n \cdot k \cdot T}\right)-1]} \quad (7)$$

The rate constant k_p represents the rate of change of electrodeposit conductance with time and can be calculated using the following relation:

$$k_p= \frac{M}{\rho_{elec} \cdot h^2 \cdot e \cdot D \cdot N_A} \quad (8)$$

Eq. (7) shows that the time-dependent resistance depends exponentially on the applied voltage and inversely on time of applied voltage. The dependence of the resistance on the applied current and the time for which it is applied demonstrates the property of memristance.

2. Voltage sweep: $V(t) = k_v.t$ where k_v is a constant

The Schottky diode current equation is re-written as follows:

$$I_D(t)=I_L \left[\exp\left(\frac{k_v \cdot t}{n \cdot k \cdot T}\right) - 1\right] \quad (9)$$

This is then substituted in eq. (4). We again use the boundary condition $R(0) = R_0$ and solve to get the result shown below:

$$R(t)=\frac{R_0}{1+k_p \cdot I_L \cdot R_0 \cdot \left[\frac{n \cdot k \cdot T}{k_v}\left\{\exp\left(\frac{k_v \cdot t}{n \cdot k \cdot T}\right) - 1\right\} - t\right]} \quad (10)$$

The value of k_p is this equation is the same as that given in eq. (8).

The voltage sweep also provides an opportunity to characterize the device behavior using current-voltage characteristics. An expression which relates the observed current to the applied voltage is derived below. Eq. (4) may be modified to relate resistance as a function of applied voltage as follows:

$$\frac{1}{R(t)^2}\frac{dR}{dV}\cdot\frac{dV}{dt} = -k_p I_D(t) \qquad (11)$$

For a linear voltage sweep, $dV/dt = k_v$. Using this in eq. (8) and solving using the boundary conditions $R = R_0$ for $V = 0$, the solution is as follows:

$$R(V) = \frac{R_0}{1+\frac{k_p \cdot I_L \cdot R_0}{k_v}\left[n\cdot k\cdot T\cdot\left\{\exp\left(\frac{V}{n\cdot k\cdot T}\right)-1\right\}-V\right]} \qquad (12)$$

Eq. (12) can then be used to provide the current-voltage characteristic shown on the next page:

$$I(V) = \frac{V}{R_0}\cdot\left[1+\frac{k_p \cdot I_L \cdot R_0}{k_v}\left[n\cdot k\cdot T\cdot\left\{\exp\left(\frac{V}{n\cdot k\cdot T}\right)-1\right\}-V\right]\right] \qquad (13)$$

Eq. (13) assumes that the current through the electro-deposit is much larger than the Faradaic current through the diode.

3. Programming using a voltage pulse $V = V_A$ and a current-limiting series resistor R_s

This scenario represents a practical situation where the PMC device is programmed using a voltage pulse, while limiting the current through the programming circuit. This limit is imposed by the series resistance R_s. This quantity of interest here is the programming time, since this could impose a limit on the speed of operation of the circuit. The substitution $Y(t) = 1/R(t)$, results in a simplified form of eq. (11) given below:

$$\frac{dY}{dt} = k_p \cdot I_L \cdot \left[\exp\left\{\frac{V_A}{(n\cdot k\cdot T).(1+R_s\cdot Y)}\right\} - 1\right] \qquad (14)$$

This equation assumes that the diode current is much smaller than the current through the electro-deposit, which results in the voltage across the device being defined entirely by the resistance of the electro-deposit. Eq. (11) does not have a direct analytical solution and approximations need to be made to solve it. The solution to the important case of $V_A > n.(\Phi_B + k.T)$ is presented here to illustrate device behavior.

Two assumptions are made in order to solve this equation:

1. The exponential portion of the equation dominates.
2. The inequality $Rs.Y < 1$ holds for the duration of the programming cycle, thus simplifying the eq. (14) to the one shown below:

$$\frac{dY}{dt}=k_p \cdot I_L \cdot \left[\exp\left\{\frac{V_A \cdot (1-R_s \cdot Y)}{n \cdot k \cdot T}\right\}\right] \tag{15}$$

Eq. (15) is solved with the boundary conditions $Y = 1/R_0$ for $t = 0$ and $Y = 1/R_{on}$ for $t = t_p$. The expression for the programming time is as follows:

$$t_p=\frac{n \cdot k \cdot T}{k_p \cdot I_L \cdot R_s \cdot V_A \cdot U}\left[U^{\frac{R_s}{R_{on}}}-U^{\frac{R_s}{R_0}}\right] \tag{16}$$

Here $U = \exp(V_A/n.k.T)$.

Eq. (16) shows that for large values of applied voltage, the programming time depends exponentially on applied voltage. As the applied voltage is reduced, the programming time begins to depend inversely on applied voltage.

C. Device characterization

The device was characterized for its programming behavior. The observed current-voltage behavior was compared to the behavior predicted by the model.

The barrier height (Φ_B) and the ideality factor (n) for the Schottky diode are extracted to verify the model for Ag doped Ge-Se devices. The case for pulse programming is also investigated. The programming time is investigated as a function of applied voltage to see if the pulse programming model accurately represents the behavior of the device.

The value for the rate constant k_p was calculated using standard values for the quantities in eq. (8), which are given here. The thickness of the Ge-Se layer is

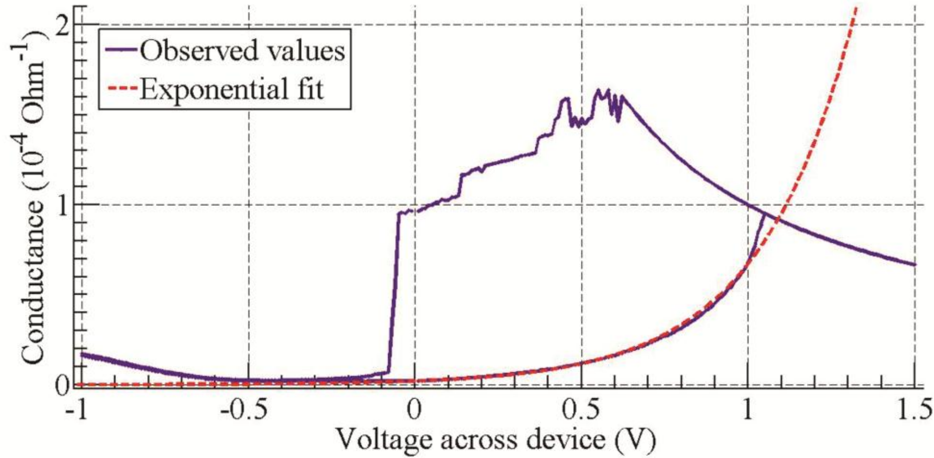


Fig. 30. Exponential fit for the programming model of the electrodeposit. The compliance current is 100 μA. The fit is for the region between 0 V to 1 V.

60 nm. The standard values of the constants used are 6.023×10^{23} atoms/mol for N_A, 1.6×10^{-19} C for e and 108 g/mole for M. The resistivity of the electrodeposit ρ_{elec} is about a factor of 100 more than that of the resistivity of Ag thin films, which is about 40 μΩ-cm [74] and the density of Ag (D) is scaled accordingly as well. The standard density of Ag is 10.49 g/cm^3. Substituting these values in eq. (8), we get the value shown on the next page,

$$k_p = 7.419\text{x}10^{10}\ V^{-1} \cdot s^{-1}. \qquad (17)$$

1. Voltage sweep behavior

We see from eq. (13) that for voltages larger than n.k.T, the exponential term dominates and the current through the electrodeposit may be modeled as an exponential function. Fig. 30 shows an example plot for one such fit. In this case, the fit is the approximated version of the conductance of the device using eq. (13) and is given as follows:

$$Y(V) = \frac{k_p \cdot I_L \cdot n \cdot k \cdot T}{k_v} .\exp\left(\frac{V}{n \cdot k \cdot T}\right) \qquad (18)$$

Using the exponential fits, we can calculate I_L and n as all other quantities are known. Arrhenius plots of the coefficient of the exponential function further improve our estimates of the ideality factor of n. The Arrhenius plot of I_L allows us to calculate the barrier height (Φ_B) of the Schottky diode. For this example, the linear coefficient is about 2.2 μS. Equating this to the appropriate portion of eq. (18) and using a sweep rate value (k_v) of 0.5 V/s, we get I_L to be about $9.66\text{x}10^{-17}$ A, or a reduction of 610 Ag^+ ions on the electrodeposit every sec. The off-state resistance calculated using eq. (18) is about 44 kΩ, which is very close to the off-state resistance of 63 kΩ measured actually. It is important to note that this off-state resistance does not refer to the off-resistance of the virgin device. Instead, the devices being measured have already been subjected to a few sweeps to condition them prior to these measurements. The result of these conditioning sweeps is to ensure the presence of conductive filamentary pathways, even in the

off-state. This is likely to be the case during the normal operation of the device in electronic applications.

Another important plot is the on-state resistance as a function of the reciprocal current. The experimental observation in this plot has been that there is a linear dependence between these two quantities, with the slope being that of the secondary deposition threshold voltage. Fig. 31(a) shows the predicted and observed programming resistance characteristic curves during a positive voltage sweep. The sweep is between 0 V to 2 V. The compliance current is 100 μA. The general character of the behavior predicted by the model is very similar to the characteristic observed from the device behavior. The observed programmed resistance is very close to the predicted programmed resistance to within a few hundreds of ohms. However, we see an abrupt change in the resistance of the observed characteristic. This is not predicted by the model. This results in the model predicting a higher turn-on voltage, or primary threshold voltage, than the observed primary threshold voltage. The reason for this abrupt switching may be because of a stronger tunneling current as the thickness of the electrolyte between the two ends of the electrodeposit in the observed case becomes progressively smaller. A second reason may be because of a change of regime of the current, where the current goes from being diffusion-controlled by a Schottky-like barrier, to be charge-transfer controlled at the electrodes while the Ag^+ ions exhibit drift behavior in the electrolyte itself.

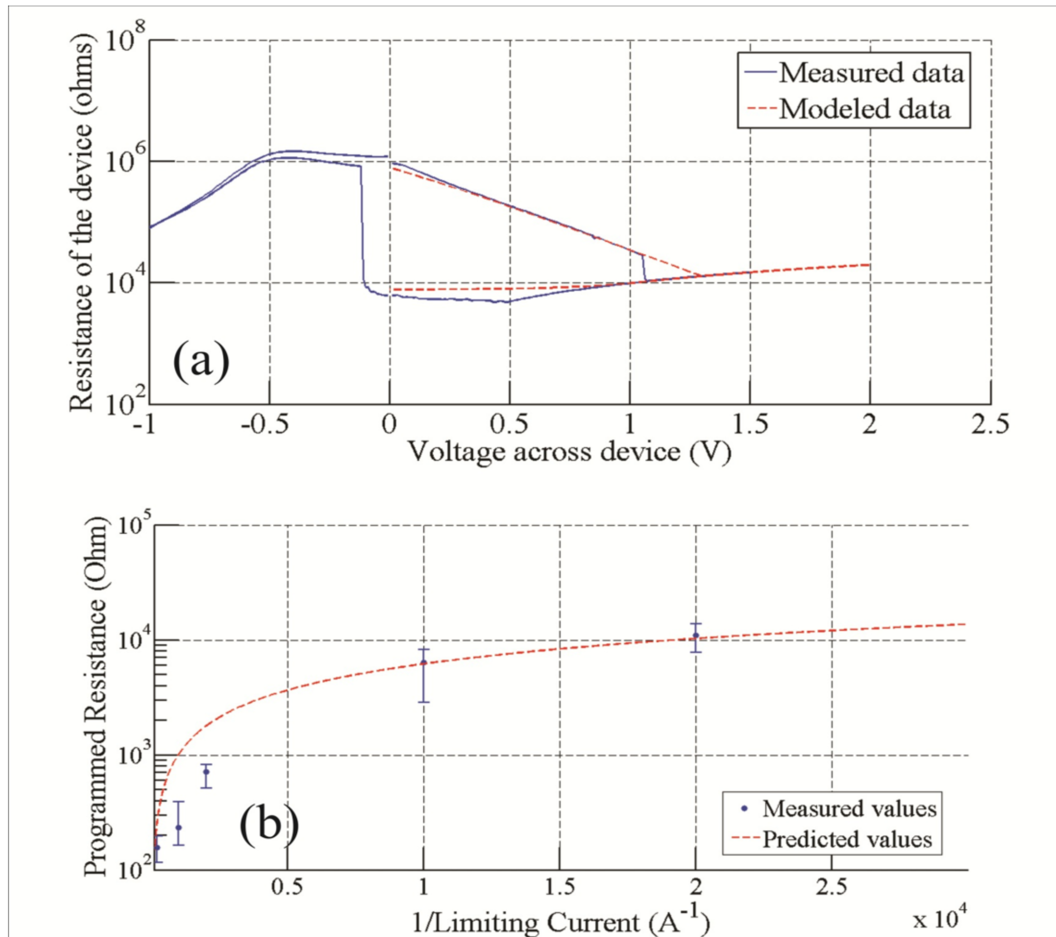


Fig. 31. (a) Comparison of the predicted and actual resistance-voltage characteristics for a compliance current of 100 μA. (b) Comparison of the predicted and actual programmed resistances as a function of the reciprocal of compliance current.

Fig. 31(b) shows the plot of programmed resistance as a function of the reciprocal of compliance current. The observed values, shown by dots representing the median of the measured values flanked by error bars, are compared to the predicted values, which are represented by the dotted line. Each point in the observed values represents the result of measuring ten randomly chosen devices. Each device was swept between -1 V and 1.5 V. The limiting

current range was between 50 μA and 5 mA. The on-state resistance was measured in each case. Multiple sweeps were necessary in each case to ensure stable switching. The model predicts the on-state resistance quite well. It seems to under-estimate the resistance slightly for the lower compliance currents and over-estimate it for higher compliance currents. This discrepancy may be because of the approximations made during the derivation of the model and also because of not accounting for mechanisms other than the diffusion-controlled current.

The characterization of the Schottky diode was done next to further improve the model. The Schottky diode is characterized by its ideality factor (n) and the barrier height (Φ_B). Both these quantities can be calculated from temperature plots. The temperature was varied between 23°C and 120°C. Ten randomly chosen devices were swept between -1 V and 2 V. The compliance current in each case was 100 μA. The on-state resistance was measured and the diode saturation current (I_L) was extracted in each case using eq. (18). The Schottky current equation predicts that a plot of the I_L/T^2 should be an exponential function of 1/T. Fig. 32(a) shows that this is the case. The slope of this plot should yield the barrier height (Φ_B). This plot yields

$$\Phi_B=0.12 \text{ eV}. \qquad (19)$$

This barrier height indicates the reason for the dominance of the ohmic characteristic below 120 mV during the reverse sweep. Below 120 mV, the Schottky diode turns off, resulting the current being entirely due to the electron

current flowing through the electro-deposit. The resistance of the electro-deposit itself does not vary as there is no ionic current in this region of the characteristic.

Figure 32(b) shows the reciprocal of the slope of the exponential term as a function of the thermal energy k.T. The slope of this plot helps us extract the ideality factor (n). In our case, this yields an n = 5. This shows that the barrier has a very high density of interface states and hence is a very poor Schottky diode. It

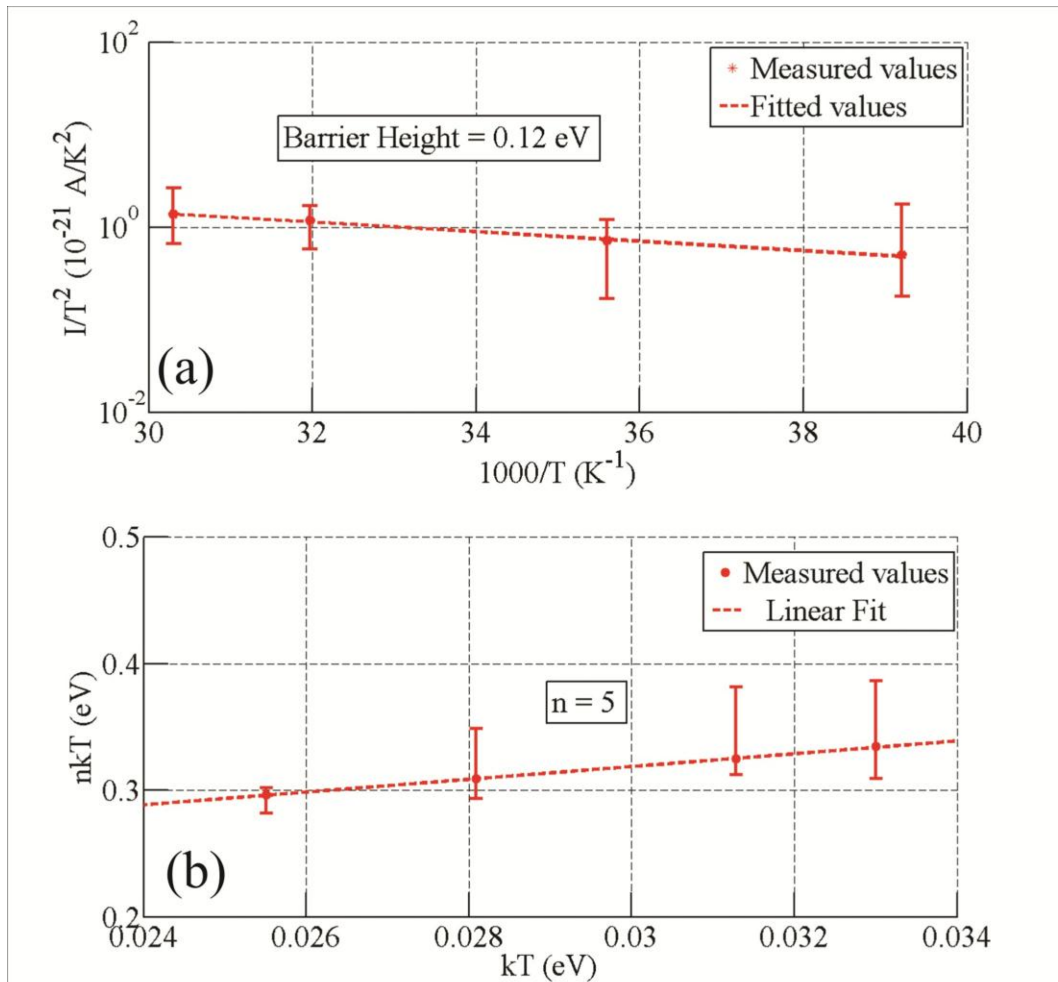


Fig. 32. (a) I/T^2 as a function of 1/T to characterize the barrier height of the Schottky diode. (b) Diode thermal voltage plotted as a function of thermal energy (kT) to characterize ideality factor (n)

is likely that such a high density of interface states causes the barrier to be governed more by the Bardeen limit than the Schottky limit. Therefore, the barrier is less likely to be controlled by the work-function differences than by the interface state density. This is a reasonable scenario since the interface consists of amorphous materials, which gives rise to randomly distributed localized energy states, resulting in a very high intermediate state density in the forbidden energy gap of the solid electrolyte. Further investigation is necessary in order to study the properties of the barrier.

A modified version of eq. (12), which gives the relation between the programmed resistance and sweep rate, is shown below.

$$\frac{1}{R_{on}} = \frac{1}{R_0} \cdot \left[1 + \frac{k_p \cdot I_L \cdot R_0}{k_v} \left[n \cdot k \cdot T \cdot \left\{ e^{\frac{V_1}{n \cdot k \cdot T}} - 1 \right\} - V_1 \right] \right] \qquad (20)$$

The programmed conductance is inversely proportional to the sweep rate. This shows that the programmed resistance can be controlled by using both the

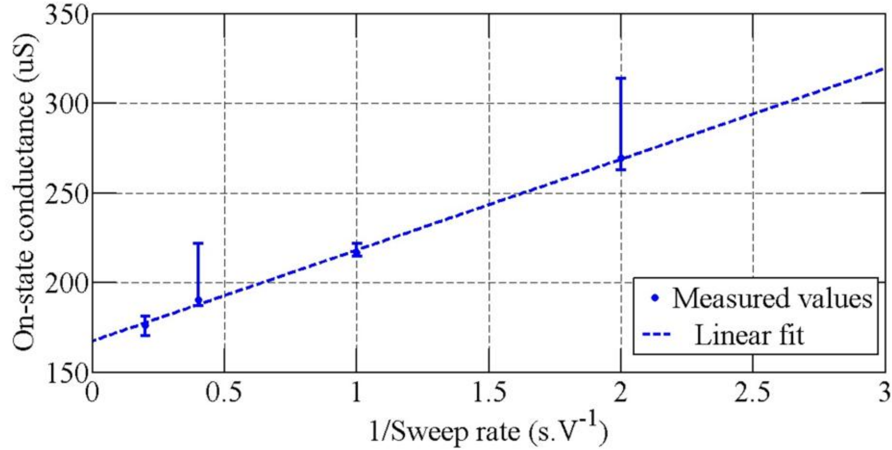


Fig. 33. On-state conductance as a function of the reciprocal of sweep rate (kv) showing linear dependence. Each data point is the result of measuring 10 devices. The compliance current is 100 µA.

compliance current and the sweep rate. Further, the extraction of the voltage V_1 would provide us further insight into other factors that may be used in controlling the programmed resistance. The design of this experiment consisted of sweeping devices between -1 V and 2 V in both directions with a compliance current of 100 μA. The sweep rates were varied between 0.5 V/s and 5 V/s. This was done by varying the step size in sweep mode of the 4155 between 10 mV and 100 mV. A plot of $1/R_{on}$ as a function of $1/k_v$ was made. Fig. 33 shows such a plot. Each data point was the result of 10 randomly chosen devices. The plot clearly brings out the linear relationship between the quantities. The linear fit gives us a slope of 51 s / V.Ω. Since the experiment was done at room temperature, we can use the values of k_p and I_L calculated previously to extract V_1, which is found to be 2.13 V. This shows that, within the range of experimental error, the slope depends strongly on the maximum voltage used to program the device. The dependence of programmed conductance of the device on sweep rates is also seen in PMC devices on rigid substrates.

2. Pulse programming behavior

The behavior of the PMC device when subjected to voltage sweeps provides very good insight into the current-voltage characteristic of the device and the behavior of the device to current limiting. However, in practical switching or memory circuits, these devices would be subjected to voltage pulses and current limiting circuitry for routine programming and erase operations. The investigation of device behavior when subjected to such pulses, therefore, assumes great importance. The setup used for testing in our case was a waveform

generator, which generated the voltage pulses, in series with the PMC device, with a series resistor, which limited the current through the device. An oscilloscope was used to determine the voltage variation through the device as a function of time. Since the off-state resistance of the device is high enough to be comparable to the impedance of the oscilloscope, it is not valid to measure the

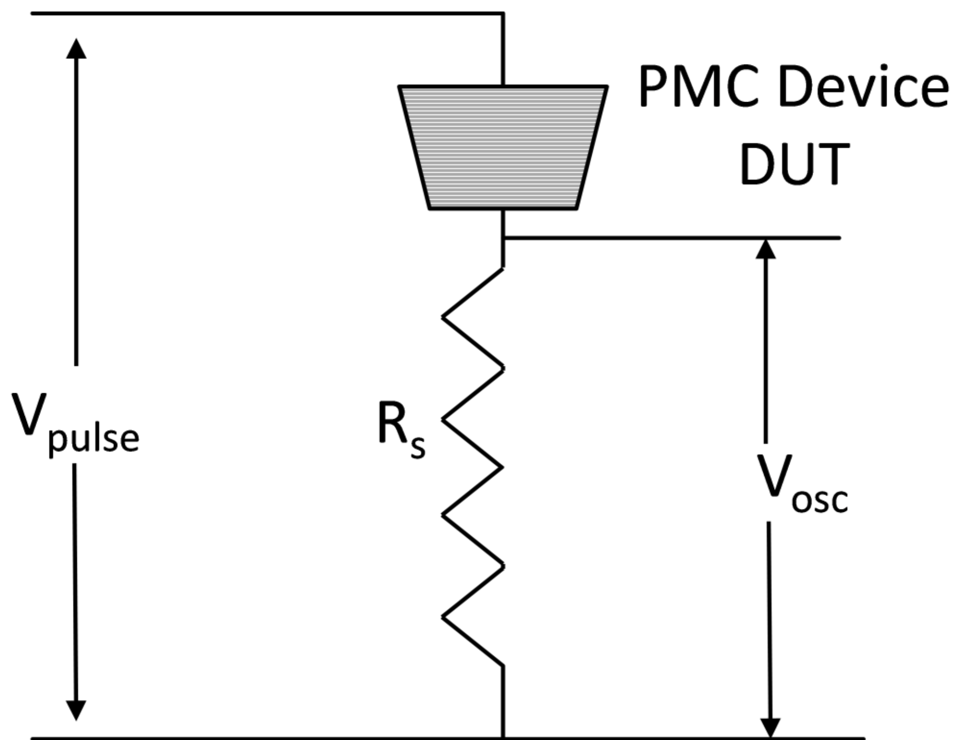


Fig. 34. Pulse programming using a waveform generator and an oscilloscope.

resistance of the device through the entire cycle. Instead, the voltage was measured across the limiting resistance, while ensuring that the series resistance chosen had a value at least an order of magnitude lower than the input impedance

of the oscilloscope. Fig. 34 shows the setup to test the pulse programming behavior of the device.

Fig. 35(a) shows a pulse measurement with the setup outlined above. A voltage pulse of 2 V is applied to the setup for a duration of 50 ms. The device resistance evolves over time. Initially, its evolution is constrained by the limiting current flowing through it because of the series resistor. Later, the constraint is because of the progressively smaller voltage that is being applied across it. The device resistance eventually saturates around the value of the series resistor. Fig. 35(b) shows the device resistance estimated using the voltage measured across the series resistance. This is done by noting that the device and series resistance form a voltage divider network and the applied voltage divides across the two based on the standard voltage divider equation. The voltage divider equation is modified to calculate the resistance of the device under test as shown below:

$$R_{DUT}(t)=R_S\cdot\left[\frac{V_A}{V_{DUT}(t)}-1\right] \qquad (20)$$

The programming time was considered to be the point at which the device resistance reached about 1.6 times that of the series resistance. This was chosen to ensure that eq. (15) remains valid during the calculation of the programming time. The programmed resistance needs to be larger than the series resistance for the equation to remain valid, according to the assumptions made in the derivation of this equation.

The next experiment was designed to investigate the dependence of programming time on the magnitude of the applied voltage pulse. The magnitude of the voltage pulse was varied between 1.5 V and 4 V. Ten devices were chosen randomly for each voltage point. A limiting series resistor of 5 kΩ was used in all cases. The programming time for each trial was calculated. Fig. 36 shows the variation of programming time as a function of applied voltage. The dashed line

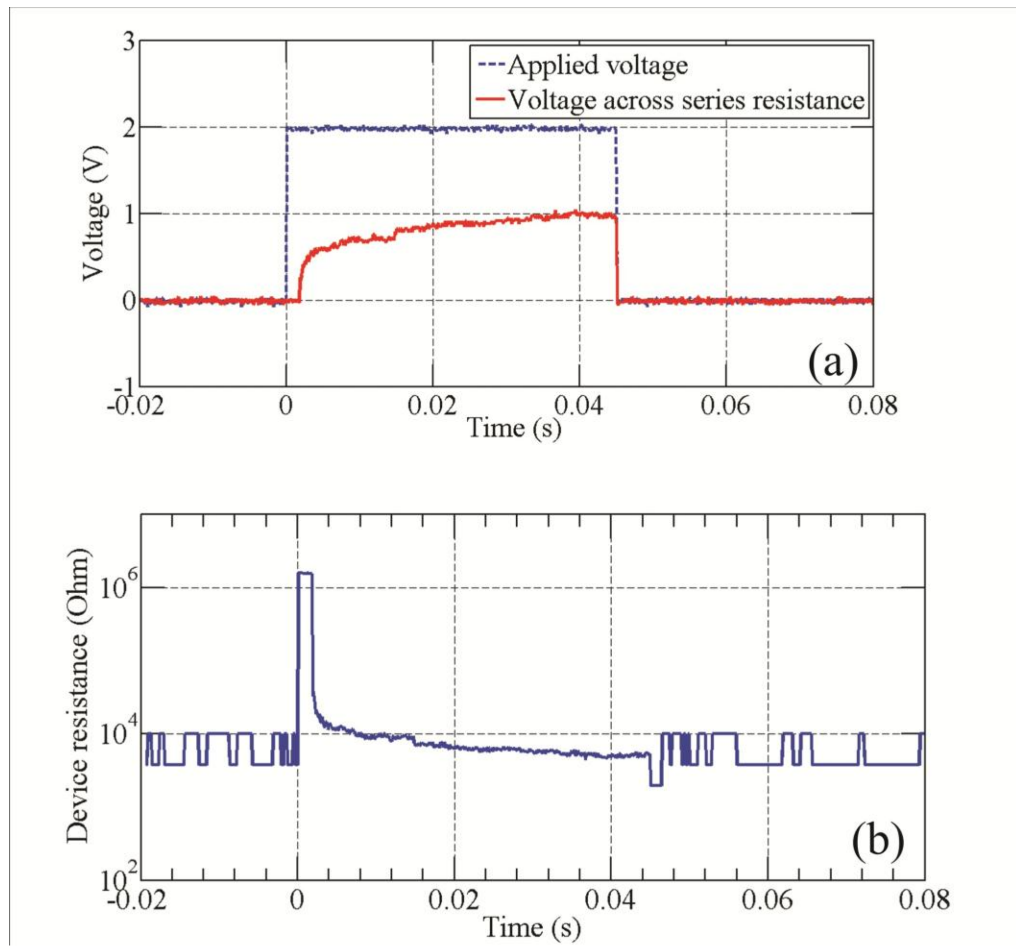


Fig. 35(a) Input and output voltage pulse measurements. (b) Resistance evolution of the PMC device in response to a voltage pulse. The series resistance is 5kΩ.

shows the predicted variation according to eq. (16). The medians in the measured data are represented by the dots, while the error bars represent the 25th and 75th percentiles. We see that the model predicts the programming time very accurately, with the measured values being approximately the same as the predicted values and both plots showing a similar trend, suggesting that this model can be used to estimate programming times for PMC devices during the pulse programming process.

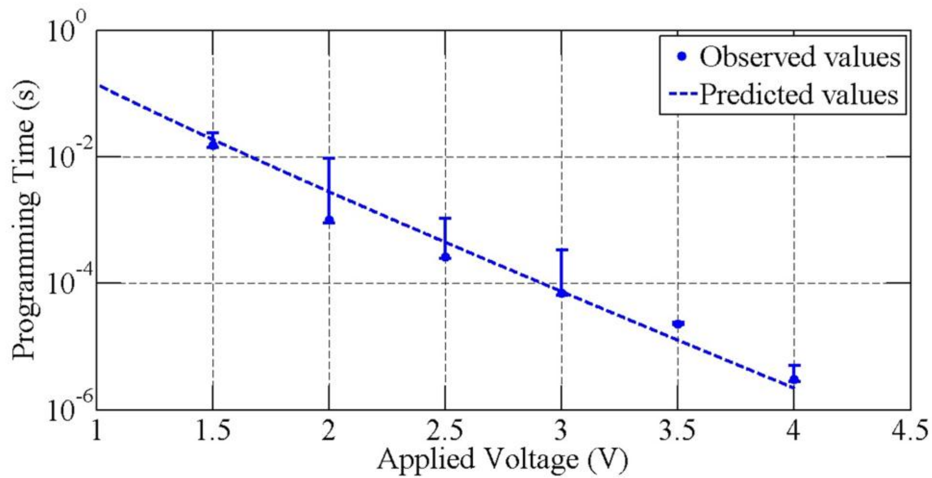


Fig. 36. Programming time as a function of magnitude of the applied voltage pulse. The series resistance is 5kΩ.

SIMULATION OF P.M.C. BASED SWITCHES

The model outlined in the previous section used simulation extensively to show the validity of the proposed model. Analytical solutions to the equations are not possible for all but the simplest conditions. Hence, the need to develop powerful numerical simulation tools for these scenarios. All models were developed using MATLAB® Simulink®. The development of these models was

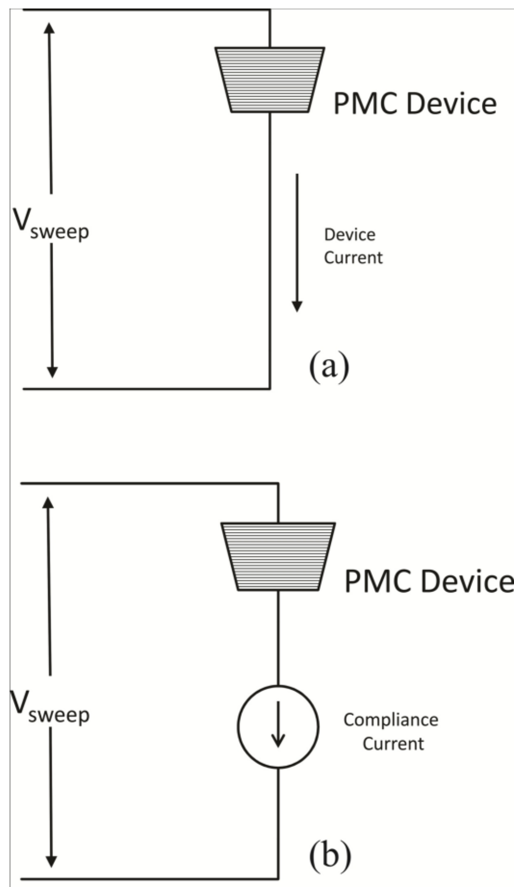


Fig. 37. (a) Voltage sweep model for device until current reaches compliance limit. (b) Voltage sweep model of the device beyond the current compliance limit.

executed in two phases for the voltage sweep case and the pulse programming case. These two cases are explained below.

A. Voltage sweep model

The voltage sweep consisted of sweeping the voltage and measuring the current to determine the resistance of the device. However, the current was not allowed to increase without limit. Instead, a compliance current limit was imposed on the device, beyond which the current was not allowed to increase during the remaining part of the sweep. We know that we can control either the voltage across the device or the current through the device, but not both simultaneously. Therefore, the voltage sweep model which was developed started off by applying the input voltage entirely across the device until the current through the device reached the compliance current limit. Beyond this voltage, the circuit was visualized as the device in series with a constant current source, with the input voltage being applied across both these. Fig. 37 shows the equivalent circuits for each of these scenarios.

The mathematical models for the voltage sweep case were derived based on Fig. 37. The system implements a modified form of the eq. (4) from the previous section and solves the equation given below:

$$Y(t)=Y_0+k_p\cdot\int I_D(t)\cdot dt \qquad (1)$$

The initial conductance Y_0 is the off-state conductance of the device. In order to speed the simulation of the device, the sweep rate was increased by a factor of 1000. This was compensated by introducing a correction multiplier of

1000 in the I_L. The resistance as a function of time was calculated as the reciprocal of Y(t) during the plotting of the resistance-voltage characteristic. The model consists of 4 components as shown in Fig. 38(a):

1. The ramp generator which generates the input voltage sweep

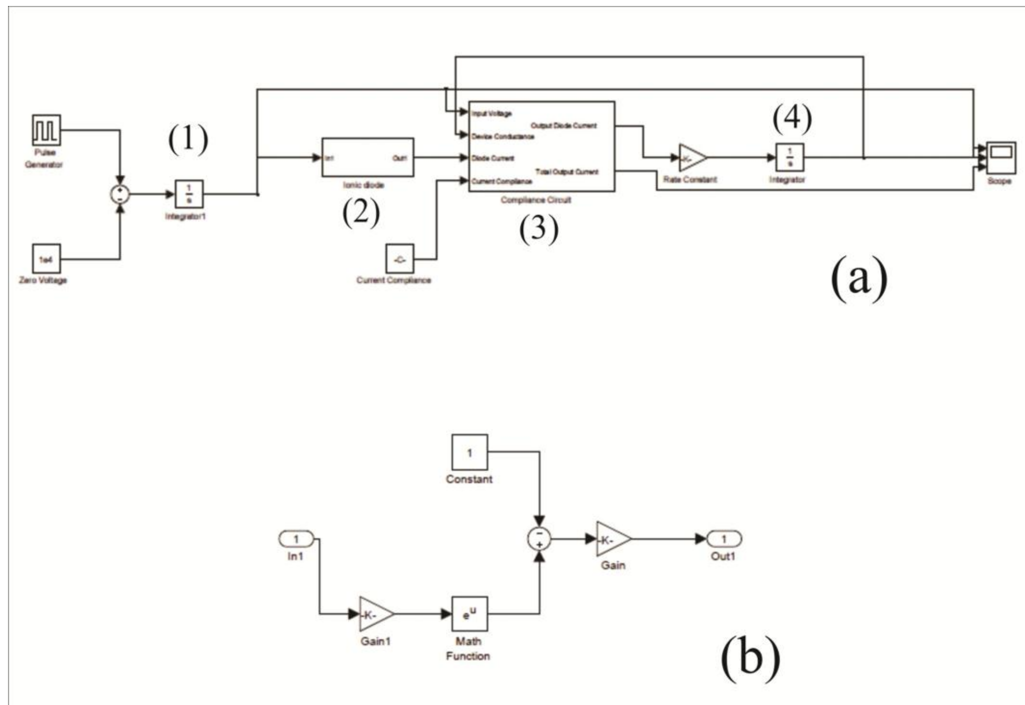


Fig. 38. (a) Mathematical model of the voltage sweep model showing all components. (b) Ionic diode model showing the implementation of the Schottky diode equation.

2. The ionic diode which is used to modulate the conductance of the Ag electrodeposit
3. The compliance circuit which enforces the compliance current requirement and modulates the voltage across the ionic diode accordingly
4. The conductance integrator which integrates the Faradaic current as calculated by the compliance circuit model and provides the change in conductance.

Fig. 38(b) shows the model of the ionic diode. This model implements the Schottky diode equation given as follows:

$$I_D(V)=I_L\cdot\left[\exp\left(\frac{V}{n\cdot k\cdot T}\right)-1\right] \qquad (2)$$

The compliance current circuit is used to determine whether the voltage-limited model in Fig. 37(a) or the current-limited model in Fig. 37(b) will be used. It also produces the ionic current which should be generated, depending on the model used. This unit takes in 4 inputs:

1. The input sweep voltage
2. The device conductance
3. The diode current that would have been generated based solely on sweep voltage with no compliance limit
4. The actual current compliance limit

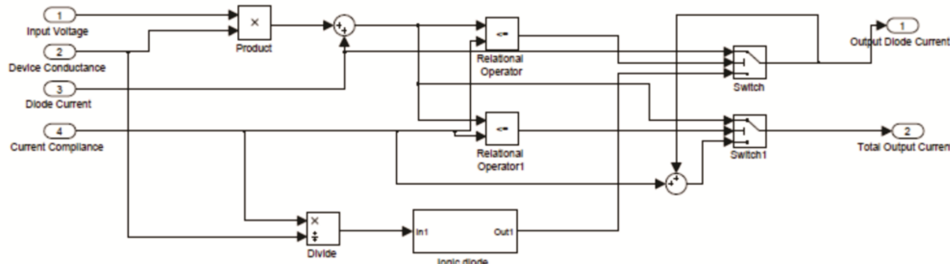


Fig. 39. Compliance current decision model.

A decision on which model is used is made by using these 4 inputs by comparing the total current generated without the compliance limit against the compliance limit. This is done using the following equation:

$$V(t)\cdot Y(t)+I_D(t)>I_{compliance} \qquad (3)$$

If the result is true, then the current-limited model is used, otherwise the voltage-limited model is used.

In the case of the current-limited model, the voltage across the diode is determined by the equation given below:

$$I_L \cdot \left[\exp\left(\frac{V}{n \cdot k \cdot T}\right) - 1\right] + V \cdot Y(t) = I_{compliance} \qquad (4)$$

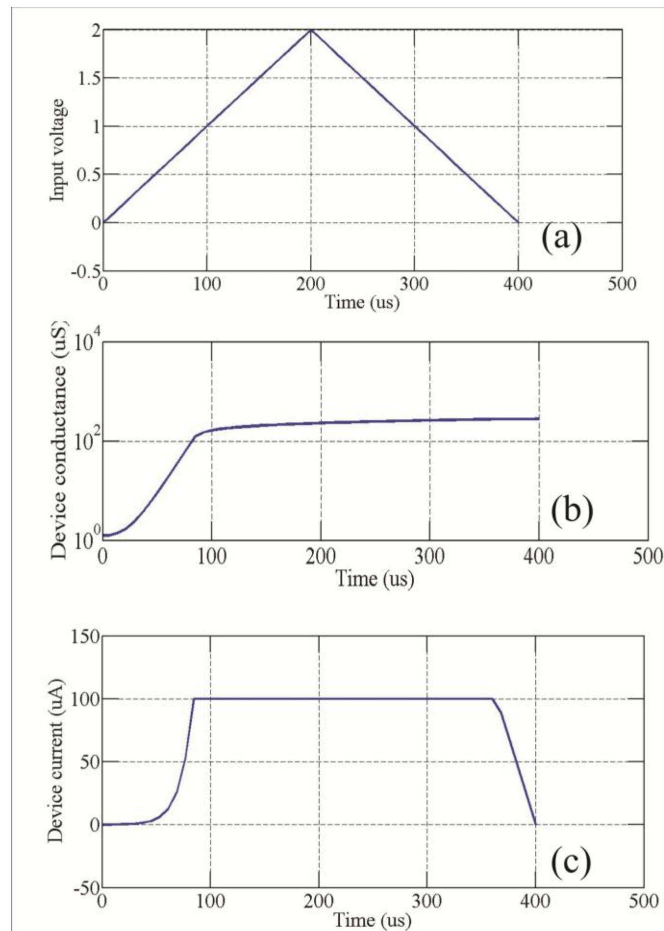


Fig. 40. (a) Input voltage as a function of time. (b) Device conductance as a function of time. (c) Total current through the device as a function of time.

This is a transcendental equation which can only be solved numerically. In order to simplify the simulation, the entire compliance current is assumed to flow through the electrodeposit and the diode current is considered to make a negligible contribution to the overall current. This gives us a device voltage given as follows:

$$V=\frac{I_{compliance}}{Y(t)} \qquad (5)$$

in the current-limited regime. The mathematical model implementing this is shown in Fig. 39 and is the compliance current unit shown in Fig. 38(a).

The evolution of the conductance as seen in the scope at the end of the model is shown in Fig. 40(b) and the total current as a function of time as seen in the scope is shown in Fig. 40(c). The scaling of the sweep rate with respect to real-time is clearly seen here. We also note that the scaling of the Schottky saturation current to compensate for this high sweep rate is also valid, with the current reaching compliance at approximately the same voltage as in real-time.

After establishing the validity of the model with respect to the corrections in sweep rate and saturation current, we proceed to plot the current-voltage and the resistance-voltage sweeps to see if these are comparable to the measured values. Fig. 40 shows the results of these investigations. We see a sample plot of the current-voltage characteristic in Fig. 41(a), showing device behavior at a compliance current of 100 μA. Fig. 41(b) shows the resistance behavior at different compliance currents. These figures show that the predicted device

behavior very closely matches the programming behavior of the PMC device in the sweep case.

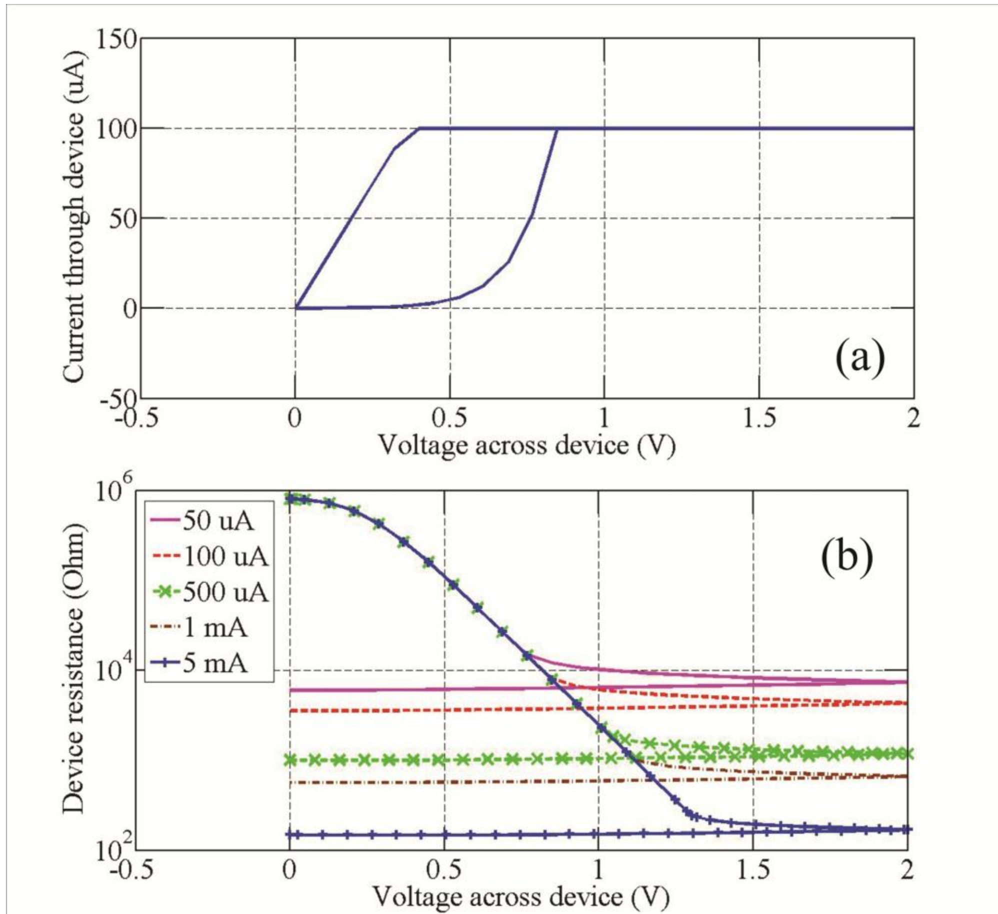


Fig. 41. (a) Simulated current-voltage sweep for a compliance current of 100 μA. (b) Simulated resistance-voltage sweeps for different compliance currents.

B. Pulse programming model

When used as a switch or a memory device, the PMC device would generally be subjected to voltage pulses. This makes it important to be able to

simulate the device under pulsed conditions. The current through the circuit would also be limited using a series resistance. The simulated circuit in this case would be given by Fig. 34.

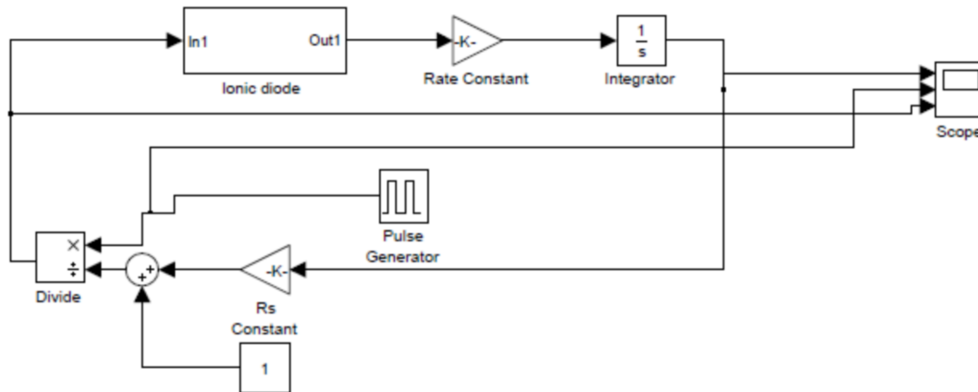


Fig. 42. Voltage pulse programming model.

The mathematical model for this scenario is an implementation of the equation given below:

$$\frac{dY}{dt} = k_p \cdot I_L \cdot \left[\exp\left\{ \frac{V_A}{(n \cdot k \cdot T) \cdot (1 + R_s \cdot Y)} \right\} - 1 \right] \qquad (6)$$

The voltage across the diode is given by the voltage divider method between the electrodeposit and the series resistor. The diode current is assumed to be negligible throughout the programming process. Fig. 42 shows the implementation of this equation. A voltage pulse is generated using the pulse generator, which defines both the amplitude and the duration of the pulse. The pulse is then passed through the voltage divider network, which consists of the

divide block and the adder block. The adder block adds a constant 1 and the product of the series resistance and the time-dependent device conductance term, which is the output of the integrator. This voltage from the voltage divider is then

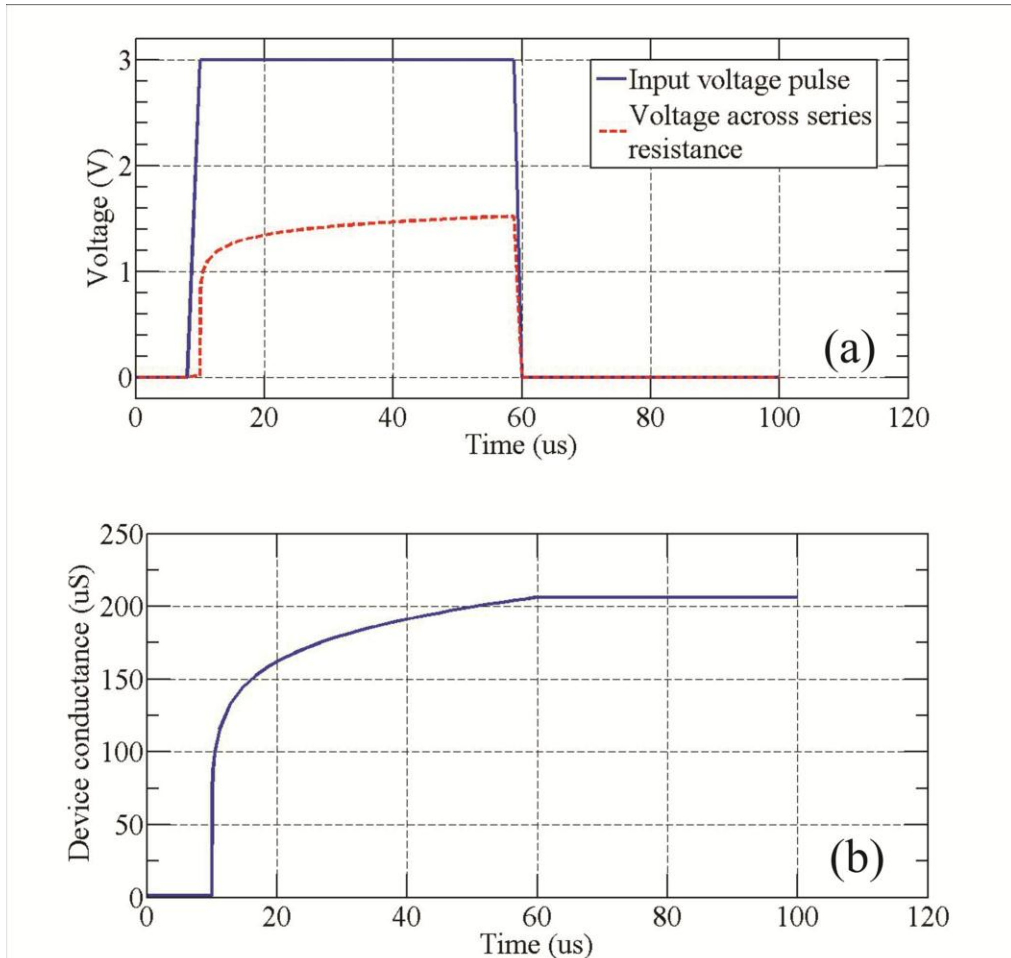


Fig. 43. (a) Voltage behavior as a function of time. (b) Conductivity variation as a function of time. The voltage pulse has a magnitude of 3 V and the series resistance is 5kΩ.

passed into the Ionic Diode block, which produces the ionic current required in the PMC device. This is then passed through the rate constant and integrator

blocks to give the conductance of the electrodeposit. This model should provide an accurate description of the observed device behavior.

Fig. 43 shows the simulated device behavior as a function of time. A voltage pulse of 3 V is applied to the model. The series resistance is 5 kΩ. Fig. 43(a) shows the input voltage pulse and the voltage variation across the series resistance as the electrodeposit forms. Fig. 43(b) shows the evolution of the conductance of the electrodeposit as a function of time. The conductance increases drastically at the very beginning, as expected, when most of the applied voltage appears across the device, and then gradually levels off later as the resistance of the electrodeposit approaches that of the series resistance.

The simulated conductance can be used to extract the resistance of the device as a function of time. This allows us to calculate the programming time required by the device. This is the time required by the device to reach a particular resistance based on the applied voltage pulse of a given magnitude and the given series resistance. The variation of programming time as a function of applied voltage has been explored in the previous section, for both the simulated and the observed cases and it has been shown that the model accurately predicts programming time.

The following discussion explores the behavior of the programming time as a function of series resistance for a voltage pulse of the same magnitude. While a relation is presented in the simulated case, no measurements have been made to verify that the relation holds true for actual devices. This is because of the limitations of the measurement equipment, which does not allow us to measure

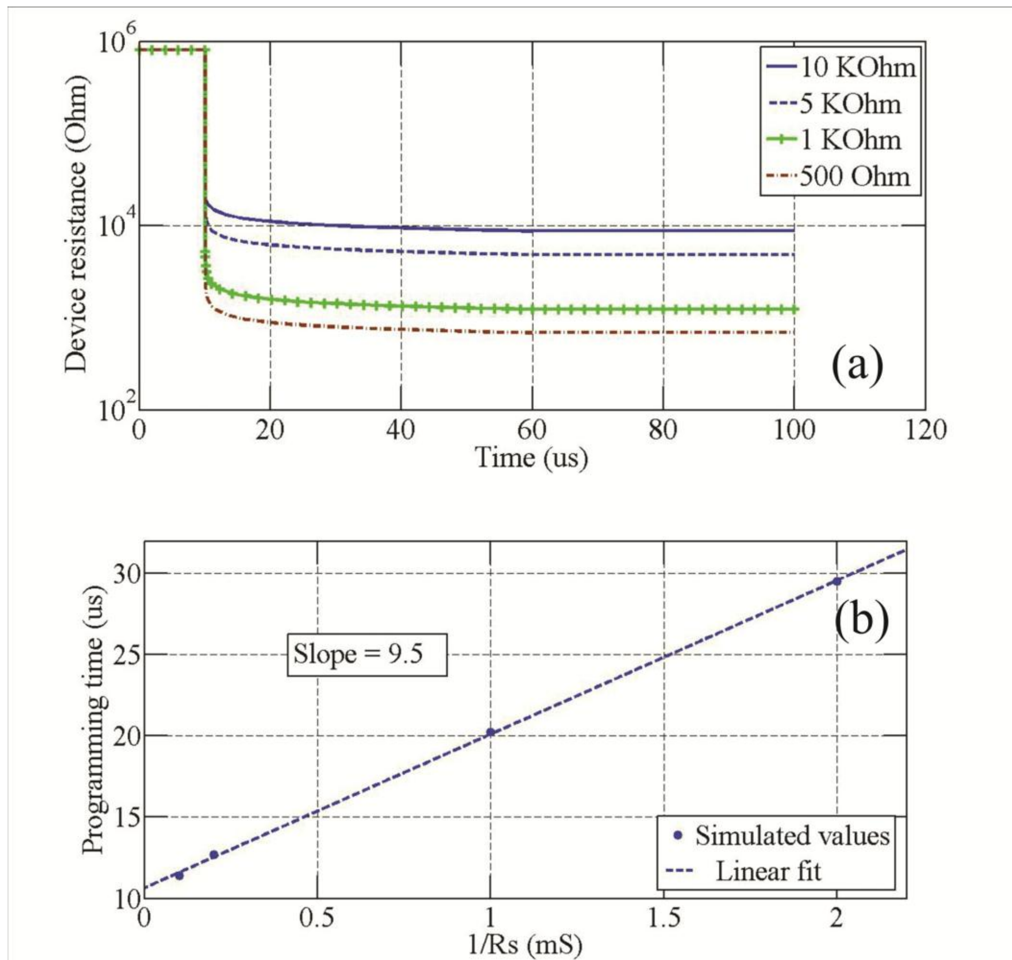


Fig. 44. (a) Resistance as a function of time for different series limiting resistances. (b) Programming time as a function of 1/Rs showing a linear relationship. The voltage pulse magnitude in all cases is 3 V.

fine changes in device resistance with respect to time very accurately. Better low-noise measurements are required to enable further testing for this scenario. As defined in the previous section, the device is considered to be programmed when the device resistance is equal to 1.6 times the series resistance. Fig. 44(a) shows the evolution of resistance as a function of time for different series resistances. The voltage pulse magnitude in all cases was 3 V. Fig. 44(b) shows the

programming times, extracted from Fig. 43(a), as a function of the reciprocal of series resistance. This gives us a linear fit, which verifies eq. (13) given in the programming model.

The device simulations discussed above demonstrate that the model accurately predicts PMC device behavior. The observed measurements closely match the simulated results. A suggested improvement would be to incorporate the tunneling current seen in Schottky diodes into this model to make it complete. Other charge transport regimes may also need to be investigated to improve the model.

CONCLUSION

A flexible interconnect structure using silver metallization on thin solid electrolyte films which has promising self-healing properties has been fabricated. Silver/electrolyte (Ag-Ge-Se) bilayers were fabricated on polyimide substrates. These were subsequently damaged by small radius bending. The damaged interconnects could be repaired by applying a small bias to stimulate Ag electrodeposition in the stress-induced cracks. The resistance of the electrodeposit is inversely proportional to the current limit used in the healing process with a constant of proportionality of 122 mV. A current limit of 10 mA is therefore capable of returning the resistance of a failed interconnect to within a few tens of ohms of its original value. The repaired interconnect behaves much like an unbroken structure under small signal conditions (moderate direct current density and low potential difference, e.g., 10 mV). Unfortunately, a DC voltage drop in the order of several hundred mV promotes ion transport away from the positive terminal in the underlying electrolyte and this ultimately causes erosion and failure of the metallization in a time that is considerably less than that expected for electromigration induced failure. The ion transport and erosion effect is mitigated by the use of AC signals which will result in reduced net ion movement. This was demonstrated by applying a symmetric ±1.5 V signal on healed structures, which resulted in a similar performance to interconnect without the underlying solid electrolyte, even at this high potential difference. The D.C. reliability of these self-healing structures was investigated further and it was found that the failure is explained with an ion drift limited model, in which the

ions drift based on the local electric field, which accelerates the dissolution of metal into the electrolyte. This was done by investigating the failure time of the interconnects as a function of stressing voltage and as a function of temperature. The combination of these two tests revealed that the failure is not due to electromigration, based on Black's equation [20] but on the Butler-Volmer equation [91], resulting in an exponential increase in resistance of the line.

Copper (Cu) is now the standard interconnect material used in fabrication processes, after its introduction for the sub-100 nm range of technologies [27, 30]. Previous research has focused on using Cu as a mobile ion for memories based on PMC technology. Cu-based PMC memory cells have been demonstrated using germanium sulfide (Ge-S) [2] and SiO_2 [92, 93] as the solid electrolyte. The behavior of the solid electrolyte bilayer interconnect using Cu as the interconnect material was investigated. The solid electrolyte layer was germanium selenide (Ge-Se). A comparison of the self-healing properties of the two metals, Cu and Ag, was made. The results showed that much higher voltages were required by the Cu based interconnects to produce the healing effect. The healing characteristic produced a secondary deposition threshold of 1.47 V, which is much larger than the 122 mV threshold observed for the Ag based interconnects. The Cu based interconnects were also much more susceptible to mechanical fracture. This was observed qualitatively, when a larger fraction of the interconnects fractured at lower mechanical stresses. The advantages of the Cu based interconnect, however, are that they can withstand larger D.C. voltages and do not show ion migration related failure until voltages of about 3 V are reached

and also require elevated temperatures. This ensures that the Cu based interconnects can work at elevated power levels compared to Ag based interconnects. More research needs to be conducted on Cu-based solid electrolyte interconnects to further characterize their behavior in flexible electronics environments.

The next section dealt with a programming model for Ag doped germanium selenide based PMC switches. A unique model, which consisted of a Schottky diode in parallel with a variable resistor, was proposed, with the resistance of the variable resistor depending on the integral of the diode current. The predicted behavior of this model was compared to the observed behavior of the fabricated devices. A detailed comparison of the voltage sweep case and the pulsed programming cases showed that the model predicts the actual device well. The predicted programmed resistances were predicted to within a few hundreds of ohms. The pulsed programming case also demonstrated that the programming time could be predicted to within less than an order of magnitude. A related section showing the numerical simulation of the model explains the limitations of the model and accounts for the limitations of the electrical measurement setup used. These two sections demonstrate the validity of the model and could provide a foundation for a formal design methodology for the design of PMC switches.

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