Mixed Oxide Thin Film Transistors for Flexible Displays

by

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ABSTRACT

A low temperature amorphous oxide thin film transistor (TFT) backplane technology for flexible organic light emitting diode (OLED) displays has been developed to create 4.1-in. diagonal backplanes. The critical steps in the evolution of the backplane process include the qualification and optimization of the low temperature (200 °C) metal oxide process, the stability of the devices under forward and reverse bias stress, the transfer of the process to flexible plastic substrates, and the fabrication of white organic light emitting diode (OLED) displays.

Mixed oxide semiconductor thin film transistors (TFTs) on flexible plastic substrates typically suffer from performance and stability issues related to the maximum processing temperature limitation of the polymer. A novel device architecture based upon a dual active layer enables significant improvements in both the performance and stability. Devices are directly fabricated below 200 ºC on a polyethylene naphthalate (PEN) substrate using mixed metal oxides of either zinc indium oxide (ZIO) or indium gallium zinc oxide (IGZO) as the active semiconductor. The dual active layer architecture allows for adjustment in the saturation mobility and threshold voltage stability without the requirement of high temperature annealing, which is not compatible with flexible colorless plastic substrates like PEN. The device performance and stability is strongly dependent upon the composition of the mixed metal oxide; this dependency provides a simple route to improving the threshold voltage stability and drive performance. By switching from a single to a dual active layer, the saturation mobility increases

from 1.2 cm^2/V-s to 18.0 cm^2/V-s, while the rate of the threshold voltage shift decreases by an order of magnitude. This approach could assist in enabling the production of devices on flexible substrates using amorphous oxide semiconductors.

DEDICATION

I dedicate this work to my children, Cassandra and Xavier.

ACKNOWLEDGMENTS

I would like to start off by thanking my wife, Tracy, for all of her support and inspiration during this endeavor as well as my children, Cassandra and Xavier, for keeping my spirits up with their boundless enthusiasm. I would also like to thank my Mother and Father for all of their support they have given me over the years. I cannot imagine how this experience would have proceeded without your support and your company.

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TABLE OF CONTENTS

Page

Page

Page

LIST OF TABLES

Table Page

LIST OF FIGURES

Figure Page

Page

Page

Page

Page

CHAPTER 1

INTRODUCTION

1.1 Overview

Mixed metal oxide semiconductors have attracted much interest in the display research community recently due to their significantly improved device performance over amorphous silicon, the current industry standard. These mixed metal oxides open up the possibility of even higher resolution displays and may enable low temperature processing for flexible displays.

This thesis is organized as follows. The motivation behind the push towards amorphous oxide semiconductors and flexible displays is described in this introductory chapter. The implementation and optimization of an amorphous oxide semiconductor process on flexible substrates is described in Chapter 2, and Chapter 3 focuses specifically on the optimization of the active layer deposition process to enhance device performance. Finally, Chapter 4 provides summary conclusions and suggestions for further studies.

1.2 Brief Background on Thin Film Transistors

The typical thin film transistor (TFT) components are the gate, gate dielectric, active layer, source, and drain as illustrated in Figure 1.1. The following paragraph will briefly describe the function for each layer in the device.

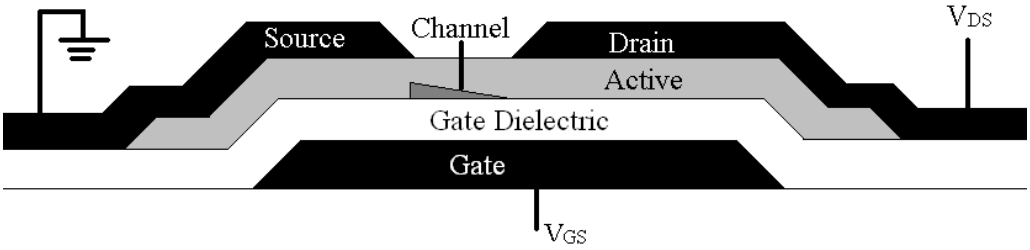

Figure 1.1: Basic thin film transistor (TFT) components and structure

The function of the gate is to induce the formation of a conductive channel in the active layer when a positive voltage is applies to the gate relative to the source. The active layer then conducts carriers, either electrons for n-channel devices or holes for p-channel devices. This thesis will focus on n-channel devices and all subsequent descriptions will be for n-channel devices unless otherwise noted. When the gate potential is negative, an electric field is induced in the channel that repels delocalized electrons away from the active layer/gate dielectric interface, which prevents conduction of carriers through the semiconductor. Conversely when the gate potential is positive, the electrons begin to accumulate within 5 nm of the gate dielectric[1]. Application of a potential (voltage) across the channel can induce current in the device. In this case, electrons pass from the grounded source to the biased drain through the conductive channel in the semiconductor when a voltage greater than the threshold voltage (approximately minimum potential required to turn the device on) is applied.

The gate voltage (V_{GS}) and drain voltage (V_{DS}) can be controlled independently, and transistors are usually characterized by holding one of the terminals at a constant voltage and sweeping over a specific range of the other voltage. Once the sweep is complete, the terminal that was held constant is stepped to a new value and the sweep is completed again. A family of curves is generated after the sweeps are completed. Sweeps of the drain voltage with the gate voltage held constant are known as the output curves. For output curves, it is typical to step through 4-5 gate voltage in the range of 0-20 V. The sweep occurs from 0 to 20 V. The output curves should intersect at the origin. If the x-intercept is significantly greater than 0, then current crowding is occurring at the drain, which could indicate the presence of a barrier. The output curves are also used to extract the drain conductance, which is simply the slope in the linear region, and to determine if there are any short channel effects.

For transfer curves, it is typical to step through 2-5 drain voltages in the range of -20 to 20 V. Sweeps generally start at -20V (forward sweeps), but can also start at +20V (reverse sweeps). Difference between the forward and reverse sweeps, commonly referred to as hysteresis, can indicate the presence of defects in the active layer or gate dielectric. The ratio of the maximum drain current I_{DS} (sometimes referred to as the on current I_{on}) divided by the minimum I_{DS} (leakage current or I_{off}) is commonly referred to the as the On/Off ratio. In display applications, the On/Off ratio is usually related to the contrast ratio. Other key parameters than can be extracted are described in the following sections.

There are typically three identifiable operating regimes for a transistor as illustrated in the example transfer and output curves shown in Figure 1.2. An exponential increase in current with increasing gate voltage is observed at low potentials in the subthreshold regime. The slope of the current increase is an important device metric known as the subthreshold slope. Subthreshold slope is defined as the gate voltage required to induce a decade increase in the drain current at a constant drain voltage. Further increasing the potential results in the linear regime, which can be described by the square-law model:

$$ID_{lin} = \mu_{sat} C_{ox} \left(\frac{W}{2L} \right) \left[\left(V_G - V_T \right) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (1.1)$$

where μ_{sat} is the saturation mobility; C_{ox} is the gate dielectric capacitance; (W/L) is the aspect ratio of the device; V_T is the threshold voltage; V_G is the gate voltage; and $V_{DS\ is}$ the drain to source voltage.

At low V_{DS}, the squared term at the end of eqn 1.1 is insignificant and the device behaves like a variable resistor with the drain current proportional to the drain voltage. As V_{DS} increases, electrons in the region surrounding the drain are depleted, creating a pinch off point and the device is considered saturated. The drain current reaches a plateau when V_D is equal to $V_G - V_T$. This value is referred to as the saturation voltage (V_{DSAT}).

The value for V_{DSAT} can be inserted into eqn 1 to solve for the saturation current:

$$I_{Dsat} = \mu_{sat} C_{ox} \frac{W}{2L} \left(V_G - V_T \right)^2 \quad (1.2)$$

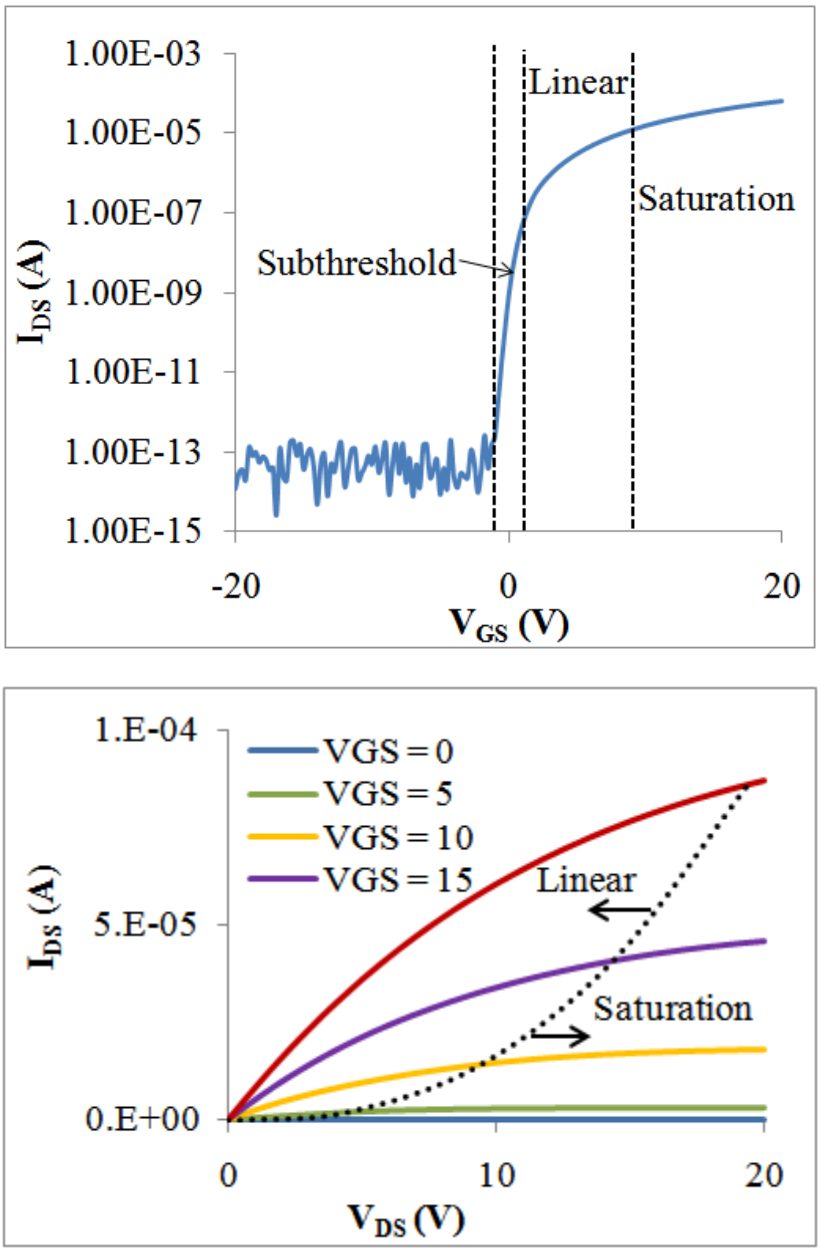

Figure 1.2: Transfer curve and output curves demonstrating subthreshold, linear, and saturation regimes

In saturation mode, the device functions as a constant current source where the drive current is dependent on the gate voltage. The shape of the channel in Figure 1.1 is representative of a device that is at the onset of saturation. When

the device is in saturation, the saturation mobility can be extracted using eqn 1.2 by plotting $\sqrt{I_{Dsat}}$ vs. V_G and calculating the slope:

$$\mu_{sat} = \frac{2L}{WC_{ox}}\left(\frac{\partial\sqrt{I_D}}{\partial V_G}\right)^2 \qquad (1.3)$$

The saturation mobility is a useful metric for quantifying the quality of the transistor as it characterizes how quickly an electron can move through the active layer. As eqn. 2 shows, a higher mobility leads to a higher current. In emissive display applications, current is usually related to brightness.

The threshold voltage (V_T) can also be determined from the same $\sqrt{I_{Dsat}}$ vs. V_G curve by extracting the x-intercept as demonstrated in Figure 1.3. The V_T of the device in Figure 1.3 is approximately 0.7 V. The V_T is the voltage at which the onset of an inversion layer is formed in the active layer and can be thought of as the "on" voltage of the transistor. A value between 0 and 2 V is usually preferred.

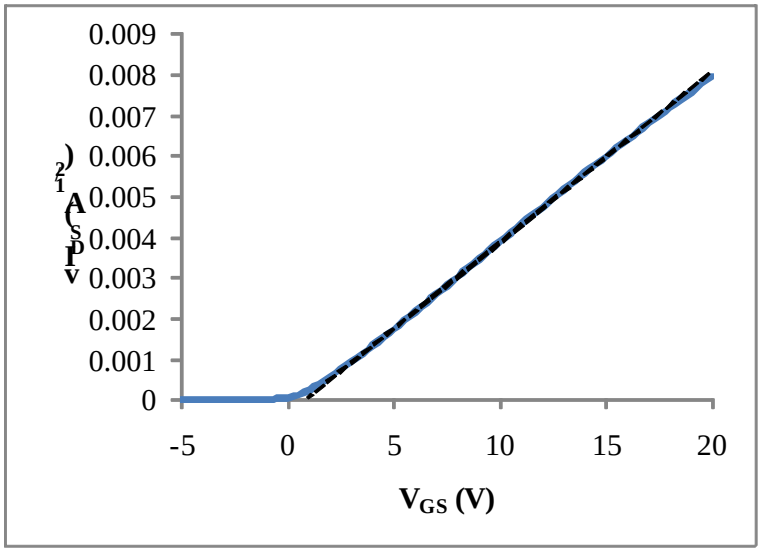

Figure 1.3: Extraction of V_T from the $\sqrt{I_D}$ vs. V_G curve

1.3 Introduction to Semiconductor Processing Techniques

Semiconductor device fabrication consists of a sequence of thin film processing steps comprising multiple additive and subtractive techniques including photolithographic patterning in order to achieve the three-dimensional transistor structure presented in Figure 1.1. At its most basic level, these processes add (additive process) or remove (subtractive process) material in order to form a device structure. Thin film processes explored in this thesis include sputter deposition, plasma enhanced chemical vapor deposition, photolithography, wet etching, and dry etching. A brief description of each process is described below.

1.3.1 Sputter Deposition

Sputtering is a process where atoms or clusters of atoms are ejected from a surface after an incident ion created in a plasma impinges on the surface with sufficient energy. The energy from the incident ion is imparted to target species which can travel up to the surface and may ultimately aid in the ejection of one or more atoms from the surface, in the same manner as a cue ball in billiards[2]. The threshold energy for sputtering is around 20-30 V, but sputter yields increase until several hundred volts of ion energy, where implantation becomes significant[3].

Sputter deposition in semiconductor processing usually takes placed in a vacuum at a pressure between 5 and 10 mTorr. The low pressure allows for the formation of a plasma, which can be thought of as an ionized gas, when a direct current (DC) or radio frequency (RF) field is applied to the chamber. The low

pressure also increases the mean free path, which is the average distance between collisions, allowing for ballistic transport of atoms and molecules.

For sputter deposition, a target is used as the actively driven electrode, where positive ions impinge and vaporize the target surface, creating a plume of effluents that are intentionally deposited onto a substrate. Sputtered films maintain excellent stoichiometric control, especially in comparison to an electron beam or thermally evaporated material[3].

1.3.2 Plasma Enhanced Chemical Vapor Deposition

Low temperature, high quality films can be grown via plasma-enhanced chemical vapor deposition (PECVD) at much lower temperatures than conventional CVD. A glow discharge is used instead of purely thermal energy to generate the reactive species that deposit onto the surface. For example, the activation energy of silane (SiH_4) is 1.5 eV for high-temperature CVD and 0.025-0.1 eV for PECVD[3]. Additional substrate heat is used to improve reaction speed, film density, local crystalline order, and conformality.

1.3.3 Photolithography

Photolithography starts with the casting of a UV sensitive organic film, known as photoresist, on to the substrate. The organic material can be spin cast (dispensed while the wafer is spinning at a speed between 500 and 5000 RPM), sprayed in a process similar to an industrial paint spray, or forced through a slotted opening as in extrusion or slot dye coating. The coat process is usually

followed by a bake at a temperature between 95 and 120 °C to bake off the majority of the volatile solvents in which the UV sensitive organic material was dissolved. A pattern is transferred into the organic film by exposing the organic film to UV light through a patterned mask. The opaque portion of the mask protects the underlying portions of the organic film from the UV radiations while the transparent portion allows UV light to expose the surface. In the case of positive photoresist (negative photoresist demonstrate the opposite behavior), the solubility of the photoresist in a basic solution is increased. The weakened photoresist is susceptible to dissolution in a developer. Following the develop process, the wafers are rinsed and baked on a hot plate to remove any residual water. This final bake can occur between 105 and 150 °C, depending upon the photoresist. At higher temperatures, the organic photoresist begins to soften allowing the patterned features to reflow and form into structures with tapered sidewalls.

1.3.4 Etching

Following the photolithography process is an etch process that is designed to transfer the pattern from the photoresist into the underlying layer by removing the material that is not protected by the photoresist mask. There are two principal techniques used to etch semiconductor materials. The first is wet etching, which simply uses a controlled mixture of acids, oxidizers, and/or bases to chemically remove the layer. Wet etching is generally isotropic (non-directional) and can be

very selective for the underlying layer over the photoresist if the correct chemical mix is chosen.

An alternative method is dry etching, which uses a reactive plasma to etch materials. Relatively inert gases can be introduced into a vacuum chamber where an electric field is applied to generate a plasma. Reactions in a plasma can result in the formation of highly reactive ions and free radicals. Anisotropic (directional) etching is possible due to the presence of a negative charge at the anode of the chamber. If a wafer is placed on the anode, positive ions can be directed to the wafer. This form of dry etching is known as reactive ion etching (RIE).

1.4 Flat Panel Display Processing

Before discussing flexible display technology, it is important to understand the basics behind conventional flat panel display processing that yields rigid planar displays. Processing begins with a substrate, typically borosilicate glass. Glass is chosen because the substrate material must be transparent to visible light in order for the backlight of the flat panel to shine through to the viewer (in the case of conventional liquid crystal displays). The glass substrate is generally free from mobile contaminants such as sodium that can degrade amorphous silicon thin film transistors (TFTs)[4]. A schematic of a typical liquid crystal display (LCD) is illustrated in Figure 1.4.

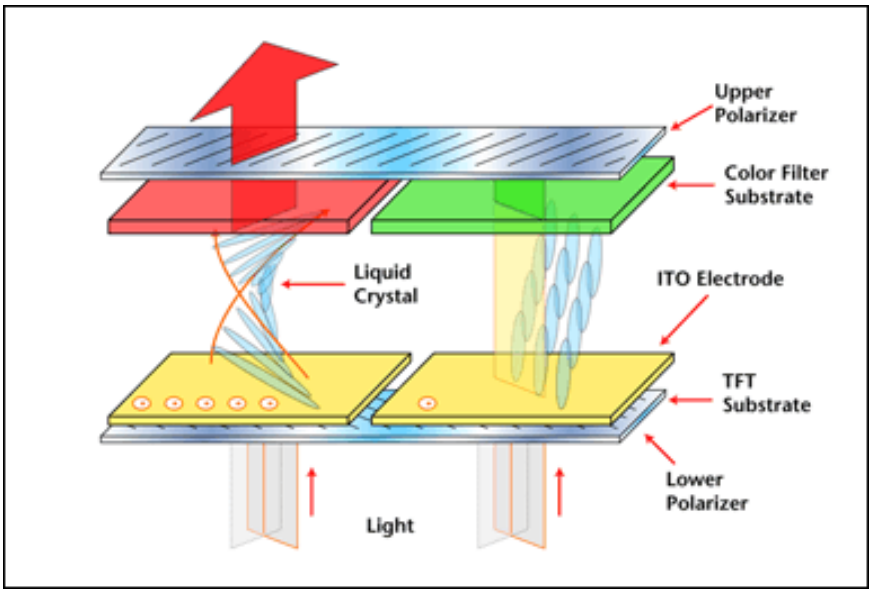

Figure 1.4: LCD schematic. The TFT substrate and lower polarizer comprise the back plane, while the ITO electrode, liquid crystals, color filter, and upper polarizer comprise the front plane

The display fabrication begins with the back plane, which contains thin film transistor (TFT) elements as well as the anode for the liquid crystals (in the case of LCDs). Controlling each pixel with a TFT (commonly referred to as active matrix displays) results in a wider viewing angle, reduced "ghosting" of images, and lower power consumption than passive matrix displays[4]. The individual TFT layers are generally between 50 and 400 nm thick. Most of the dielectric and semiconductor layers are silicon based, which is convenient with respect to thermal expansion because the substrate is also silicon-based and has a similar thermal expansion coefficient[4].

There are four common layouts for the TFT layers as shown in Figure 1.5. These are inverted staggered trilayer, inverted staggered bilayer, staggered, and coplanar TFT architectures.

The inverted staggered trilayer structure is most commonly applied to amorphous silicon based TFTs due to its superior performance over the other structures[5] and its ability to be fabricated with a large margin for error[4]. Amorphous silicon (a-Si:H) is preferred because the source material for the amorphous silicon (SiH_4 gas) is readily available and the PECVD deposition process for amorphous silicon can be tightly controlled[4].

In the inverted staggered trilayer architecture, the gate layer is deposited first. Metals are typically preferred; although doped polysilicon has been used in Complementary Metal Oxide Semiconductor (CMOS) technology. The gate metal impacts the threshold voltage (as described in section 1.2) of the transistor through the work function difference between the gate metal and the semiconductor. Common gate metals include aluminum, molybdenum, chromium, and tungsten, and alloys of those metals[4]. The deposition of the gate is usually performed by sputtering.

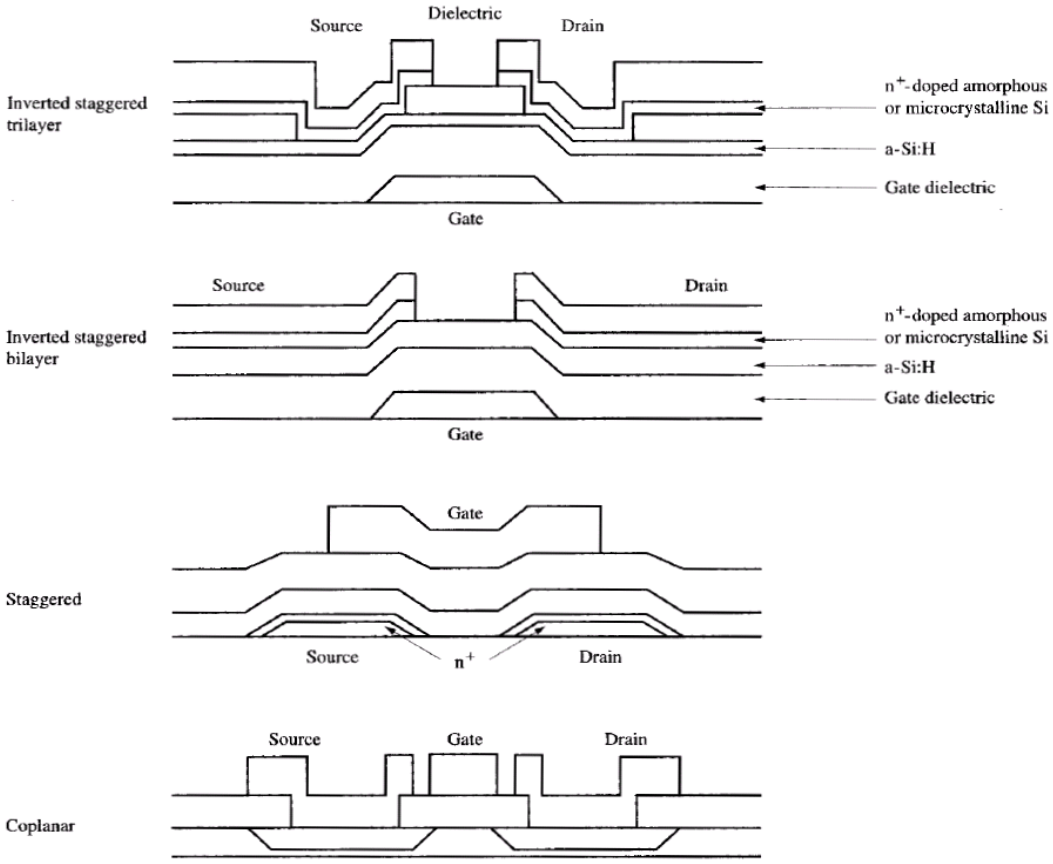

Figure 1.5: Cross-sectional view of inverted staggered trilayer, inverted staggered bilayer, staggered, and coplanar TFT architectures

The deposition of the gate dielectric, the semiconductor active layer, and the active layer passivation follow the patterning of the gate. These layers can be grown sequentially in the same PECVD chamber or in separate chambers. Sequential deposition in the same chamber can improve the semiconductor / dielectric interface by lowering the interface density of states. The deposition conditions can dramatically impact device performance. For example, the SiH_2/SiH ratio has been shown to increase with increasing power[6] due to the increase in free hydrogen in the plasma. This increase in the SiH_2 concentration in

the film leads to increased threshold voltage and decreased on current. Higher power can also lead to the roughening of the underlying gate dielectric, which can reduce the mobility of carriers in the channel by providing scattering sites. The temperature of the deposition process can also greatly affect the TFT performance. At higher temperatures, diffusion of hydrogen is encouraged, which facilitates the passivation of dangling silicon bonds. The reduction in dangling bonds improves device performance and stability[7]. However, increasing the temperature also decreases the amount of hydrogen in the plasma. For a-Si:H deposition, the optimal process temperature usually falls between 200 and 280 ºC.

The choice of the gate dielectric and channel passivation material can also significantly affect the device performance. Hydrogenated silicon nitride is the preferred choice because the hydrogen in the film can passivate dangling bonds in the a-Si:H better than silicon dioxide[4].

The active and passivation layers are etched to create islands of the active material. The isolation of the active material allows for individual control of each pixel. The gate dielectric is not etched to provide isolation to the gate metal from subsequent metal depositions. The etch process can be followed by the deposition of an additional passivation layer to protect the exposed sidewall of the active layer or can proceed directly to another photolithography/etch cycle to open contacts to the gate and active layer.

Once contacts are opened, a heavily doped silicon layer is deposited. The purpose of this heavily doped layer (termed "*n*+" in NMOS devices where electrons are the carriers) is to bridge the work function difference between the a-

Si:H active layer and the source/ drain metal, which creates an ohmic (linear current/voltage characteristics) contact. The resistivity of this *n*+ layer should be minimized as the contact resistance accounts for approximately 10 % of the total on resistance of the TFT[4]. The deposition of the source/drain metal follows the deposition of the *n*+ layer. The choice of metal can affect the performance of the devices. Metals with low resistivities such as aluminum or copper are typically selected to reduce losses over long metal runs.

The pixel anode is then defined with the following processing steps. An additional dielectric layer is deposited on the source/drain metal to reduce parasitic capacitance effects from the source/drain metal and is usually greater than 1 μm thick. The pixel anode is formed in a transparent conducting oxide such as indium tin oxide (ITO). Transparency is required as light from the LCD backlight must pass through the anode. The anode is usually passivated with another dielectric to complete the back plane process.

The display front plane comprises the remaining processes required to complete the display. The front plane in an LCD consists of the liquid crystals, polarizers, color filter, and the cathode. The liquid crystal realign when an electric field is generated between the anode and the cathode allowing polarized light to pass. When there is no field present, the light is reflected. The intensity of the field determines the amount of light allowed to pass. Red, green and blue color filters (and more recently yellow filters as well) can be added to allow for generation of a wide gamut of colors. Once the front plane is complete, device

drivers and packaging are incorporated to complete the display. This work focuses on the backplane technologies.

1.5 Introduction to Flexible Displays

Flexible displays have captured manufacturing interests over conventional flat panel displays due their thinner profile, conformability, robustness with respect to breakage and lighter weight. These advantages could lead to a new generation of flexible displays that could be shaped to fit most any conceivable application including wearable displays integrated into clothing, foldable or rollable displays that could be stored while not in use, and conforming and unique-shaped displays for equipment consoles. Robust and lightweight flexible displays could conceivably replace glass-based displays in cell phones and televisions. An example of an electrophoretic flexible display is shown in Figure 1.6.

Figure 1.6: Flexible display produced on 125 µm thick stainless steel foil

1.5.1 Flexible Substrate Materials

The fabrication of the flexible display starts with the choice of the substrate material. There are three main classes of flexible substrates: flexible glass[8], metal foil[9,10,11] and polymeric[12,13,14] films. The ideal substrate would be colorless and transparent (for bottom emitting organic light emitting diode, or OLED, emissive displays), flexible and rollable, low-cost, resistant to chemical attack, dimensionally stable under thermal cycling and would have low permeability to water and oxygen and thus able to act as an intrinsic barrier layer. If this barrier layer were inherent in the substrate, simply laminating two film sheets together would be sufficient to package the device at low cost. No material has emerged that fills all of these needs simultaneously (see Table 1.1).

Table 1.1: Comparison of substrate properties of interest for stainless steel, plastics such as polyethylene naphthalate (PEN) and polyimide (PI), and glass

Property	**Stainless Steel**	**Plastics (PEN, PI)**	**Glass**
Weight (g/m^2)	800	120	220
Safe bending radius (cm)	4	4	40
Visually transparent?	No	Some	Yes
Max process temp (°C)	1000	180, 300	600
CTE (ppm/°C)	10	16	5
Elastic Modulus (GPa)	200	5	70
Permeable O_2, H_20	No	Yes	No
Planarization necessary?	Yes	Yes	No
Electrical conductivity	High	Low	Low

1.5.1.1 Flexible Glass

Thin sheets of glass can be made flexible with very small thicknesses (less than 100 µm). Glass at a thickness between 400 and 700 µm is the current standard substrate material for flat panel display fabrication, acting as perfect impermeable barrier layers and offering superior optical properties, ultra-smooth surfaces, and low thermal expansion coefficients. However, glass sheets that are sufficiently thin to also be flexible are highly susceptible to breaking and cracking along the edges if even slightly mishandled. Coating the glass sheets with a thin

polymer layer around the edges and surface makes the substrates less prone to breaking during minor handling mistakes in production and also reduces the influence of existing defects. Even with this hybrid approach, flexible glass substrates cannot currently be used in large scale manufacturing due to low yield related to glass breakage[8].

1.5.1.2 Stainless Steel

Stainless steel (SS) is a strong candidate for applications where transparency is not required. SS foils, produced with thicknesses of 125 µm, provide durable, flexible substrates that tolerate high temperature processes with much better dimensional stability than plastic. The foils provide a perfect diffusion barrier to oxygen and water vapor and have proved to be successful substrates for both amorphous and crystalline silicon-based TFTs used to make top-emitting active matrix OLED devices[9]. Finally, at 10 ppm/°C, SS films also have a lower CTE than polymer films. The steel foils, however, have a rough surface due to rolling mill marks and are highly conductive, so an insulating spin-on-glass (SOG) planarization layer must be coated on top of the stainless steel. This ensures flat, non-conductive surfaces that will translate into accurate device registration on subsequent layers.

1.5.1.3 Plastic Films

Plastic engineered films are very appealing substrate materials for flexible electronics due to their low cost and toughness, of which Dupont's Teonex brand of polyethylene naphthalate (PEN), is a leading candidate. As seen in Figure 1.7, PEN shows a remarkably smooth, defect-free surface quality after pretreatment with an adhesion layer. PEN has a Young's modulus three times greater than typical amorphous plastic films due to its semicrystalline, biaxially oriented nature.

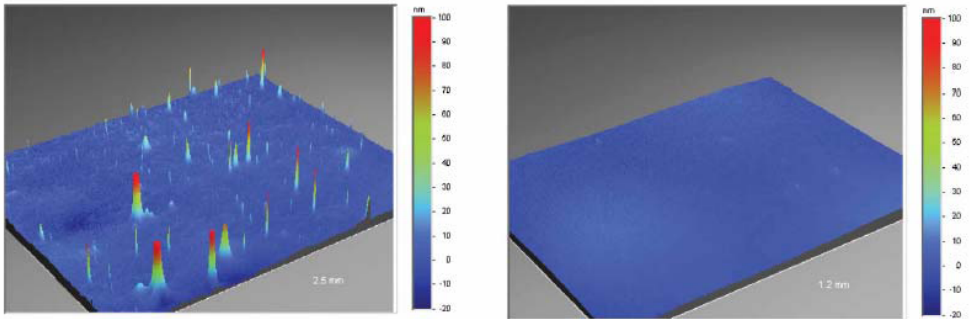

Figure 1.7: Atomic force microscope height images showing the surface smoothness of a) industrial grade polyethylene naphthalate (PEN) and b) DuPont's surface tailored Teonex® Q65 film[15]

Natural thermal expansion also needs to be taken into account when dealing with thin film stacks on polymers. Thermal expansion is based on a number called coefficient of thermal expansion (CTE) of the material. Relative to other polymers, PEN has a relatively low CTE of about 13 ppm/ °C, but what is important is that the substrate is coupled with a layer that has a similar CTE. Any mismatch in thermal expansion coefficients during thermal cycling could cause high levels of residual stress and film cracking.

1.6 Manufacturing Challenges for Flexible Displays

Currently, there are four primary approaches toward constructing flexible displays: roll-to-roll processing, transfer processing, substrate laser release processing, and bond/debond processing. The roll-to-roll approach involves processing directly on a roll of flexible material. The roll is loaded at one of the equipment and fed through the equipment for processing to a reel on the output side. An example demonstrating the transfer of a photoresist pattern into a layer of indium tin oxide (ITO) by wet etching[16] is shown in Figure 1.8. The material is first fed into the $CuCl_2$ ITO Etch bath using a series of rollers. The material proceeds directly to the resist strip bath containing NaOH which is followed by rinsing in DI water and drying with heated nitrogen. The feed rate is constant through all of the baths so each individual bath must be designed to allow adequate residence time of the material for each process to complete. All processing takes place on the freestanding flexible material.

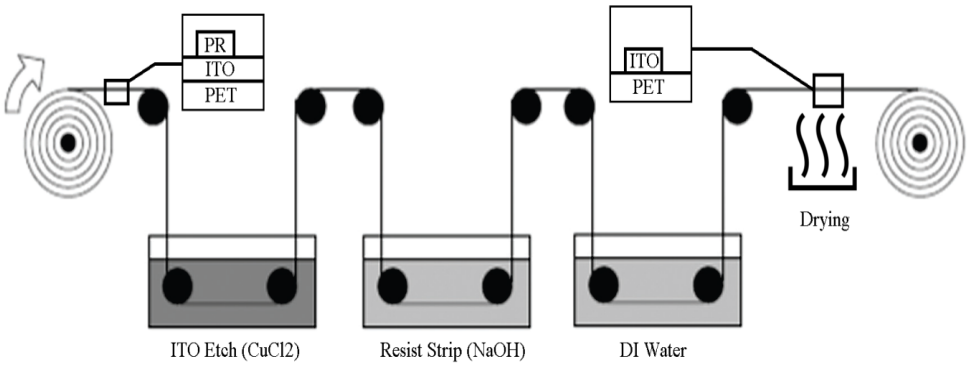

Figure 1.8: Schematic of roll to roll ITO etch and resist strip process

However, current semiconductor processing technologies are geared toward the handling of rigid substrates. Examples of semiconductor processing

equipment are demonstrated in Figure 1.9. Figure 1.9(a) shows a wet bench that processes batches of 25 wafers at a time. This wet bench would be the plate to plate processing analog of the roll to roll ITO etch demonstrated in Figure 1.8. The 25 wafers are first placed in the bath in the far left by the robot to etch the ITO, then the wafers are pulled from the ITO etch placed and placed in the NaOH resist strip bath. Once the resist is stripped, the wafers are placed into the quick dump rinse tank at the front of the bench (the water spray nozzles for this tank are visible in Figure 1.9(a)). Once the wafers have been rinsed, the wafers are placed into the spin rinse dryer (SRD) which is partially visible at the right edge of Figure 1.9(a).

The equipment in Figure 1.9(b) is a Rite Track 8800 photoresist coater and developer. Wafers are placed into a boat that holds 25 wafers at left end of the track at the bottom of Figure 1.8(b) for adhesion layer coating (usually hexamethyldisilazane), followed by resist dispense, solvent bake out on a hot plate, and cooling on a water-chilled plate. The wafers are pulled from the right end of the track and sent to the next processing step. As opposed to the roll to roll process presented in Figure 1.8, the wafers in these batch operations are always handled from the back (non-processing) side of the wafer.

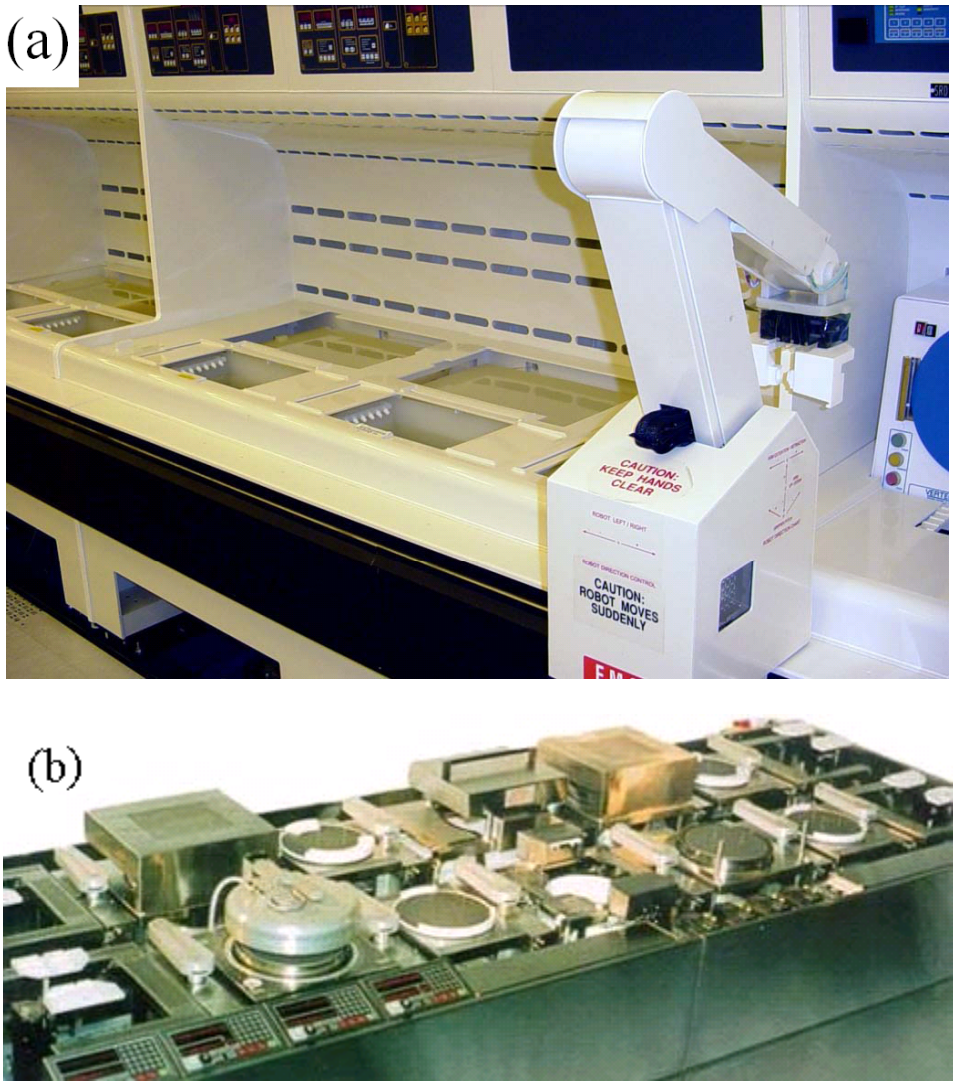

Figure 1.9: Images of (a) automated batch processing wet etch hood and (b) photoresist coater and developer track

Since most semiconductor processing equipment is geared towards plate to plate processing, significant investment in equipment and processing is required for the integration of roll-to-roll technology. As shown in Figure 1.7, the process side of the substrate comes into contact with rollers multiple times which could lead to defects and device failure.

An alternative methodology that utilizes the more traditional plate-to-plate processing is a pattern transfer process such as Surface-Free Technology by Laser Annealing (SUFTLA)[17]. The SUFTLA process involves fabricating TFTs on to a glass substrate as described in Section 1.4 with one major difference. An amorphous silicon exfoliation layer is deposited on to the glass substrate prior to the deposition of any of the device layers. Once the device fabrication is complete, another substrate (the fist transfer substrate) is glued to the process side of the glass wafer using a UV-curable, water-soluble adhesive. Once this adhesive is cured, a XeCl excimer laser (λ = 307 nm) is used to melt the a-Si exfoliation layer, which releases hydrogen to force the substrate apart. The rest of the device layers are protected because the a-Si absorbs most of the radiation.

The now liberated backside of the device is glued to a flexible plastic substrate using a permanent, non-water soluble adhesive. The first transfer substrate is cut up and the entire assembly is soaked in water to dissolve the water soluble, temporary adhesive[17]. The equipment for the SUFTLA transfer process is expensive relative to other semiconductor processing equipment and is not considered feasible for production. In addition, the processing time increases as the substrate area increases and is only appropriate for wafer-scale processing[18].

A third option, known as Electronics on Plastic by Laser Release (EPLaR)[19], involves spin casting a thick polyimide layer (50-100 µm) to a glass substrate as shown in Figure 1.10. Once the polyimide is cast, the process flow follows the basic display manufacture process presented in Section 1.4. Once the TFT fabrication is complete, the polyimide is released from the glass substrate via

excimer laser similar to the SUFTLA process. The basic process flow is illustrated in Figure 1.10. Like the SUFTLA process, the EPLaR process main disadvantage are the cost and processing time of the laser release process as substrate size increases. The maximum process temperature is set by the glass transition temperature of the polyimide. In addition, the polyimide may not be desirable for applications where visible light must shine through the substrate as polyimide films tend to have an orange tint.

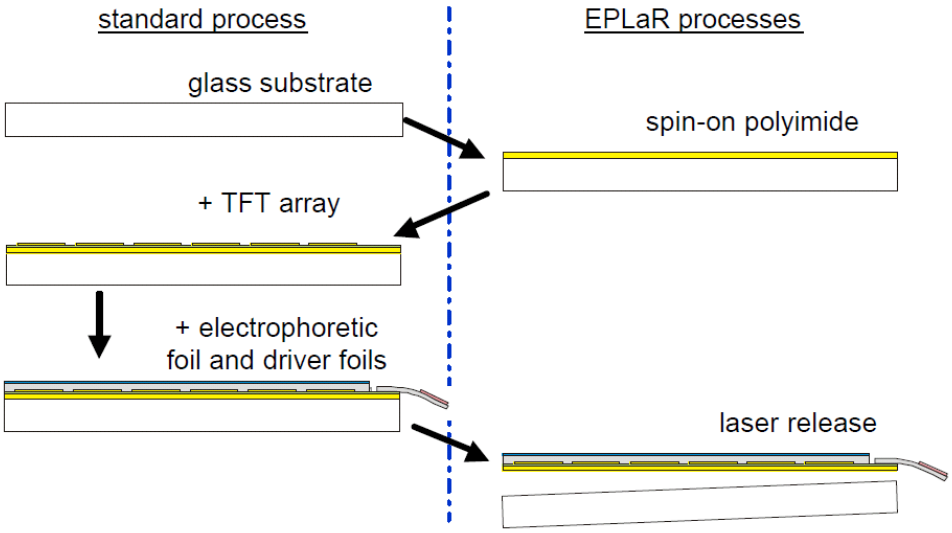

Figure 1.10: Basic process flow of the EPLaR process[19]

The fourth option, known as the bond/debond involves processing a flexible substrate bonded temporarily to a rigid carrier. The basic process flow for the bond process is shown in Figure 1.11[20]. A temporary adhesive is spin-coated on to a rigid carrier. If the adhesive is thermally cured, a bake usually follows the spin process. The flexible substrate is then mounted to the adhesive-coated carrier through a toll laminator. The adhesive is cured either by UV exposure or by

baking or a combination of both. The processing of the TFTs proceeds as described in Section 1.4. The maximum processing temperature depends on the glass transition temperature of the substrate.

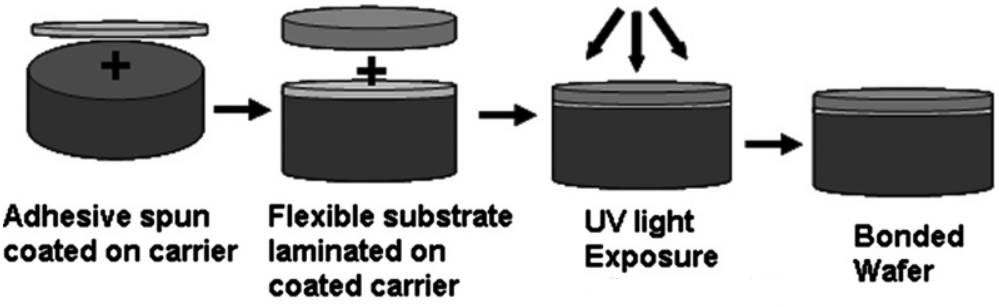

Figure 1.11: Bond process flow

The rigid carrier suppresses the bowing of the flexible substrate during processing to provide the requisite dimensional stability during device fabrication. Following device fabrication, the flexible substrate can be debonded from the rigid carrier to yield a flexible display.

The main advantages of the bond/debond process are that the process requires little additional investment to an already existing display fab. Unlike the SUFTLA and EPLaR processes, the bond/debond process is scalable to larger area substrates without significant alterations to the process. The main disadvantages of the bond/debond process is controlling the substrate deformation (i.e., warp and bow), which can cause wafer handling our pattern alignment issues and preventing delamination of the flexible substrate during processing. However, Haq, et al., has demonstrated a suitable bond/debond process that is capable up to 200ºC[21]. The present work utilizes the bond/debond process for the fabrication of flexible back planes.

There are many additional issues related to processing of flexible substrates irrespective of the technique used for handling the flexible substrates, including substrate defectivity, low melting temperature of the substrate, and substrate deformation during processing. These issues can severely limit the performance of electrical devices fabricated on flexible substrates. For example, the current technology of choice for active matrix LCD displays is hydrogenated amorphous silicon (a-Si:H). In commercial flat panel display TFT array fabrication, the amorphous silicon active layer as well as most of the dielectric layers is deposited at temperatures in excess of 300 °C on rigid glass substrates. This relatively high processing temperature allows for the optimal drive performance and device longevity as discussed in Section 1.4. The low melting temperature of plastic substrates generally prohibits processing above 200 °C; resulting in a lower performance, less stable a-Si film. Therefore, it would be desirable to explore a TFT technology that could be deposited at a lower temperature compatible with transparent colorless plastic substrates, but still demonstrate high performance and stability and be deposited over a large area in a production environment. One potential replacement for a-Si:H is transparent oxide semiconductors, which is the focus of this thesis.

1.7 Mixed Metal Oxides

Transparent oxide semiconductors have drawn considerable attention due to their electrical (high mobility in the amorphous phase) and optical (> 90 % visible light transmission) properties[22,23,24]. The term “transparent oxide

semiconductors" covers a wide range of metal oxides including those of gallium, indium, zinc, aluminum, zirconium, hafnium, and tin that exploit their spherically symmetric *s* orbital conduction bands to produce their attractive properties. The spatial spread of the vacant *s* orbital allows direct overlap between neighboring metal atoms resulting in higher mobility than the sterically hindered hybrid sp^3 orbitals of amorphous silicon. There has been tremendous interest in examining oxide semiconductors as a replacement for a-Si:H in the fabrication of thin film transistors (TFTs) for active matrix flat panel displays[25] due to their improved saturation mobility[26,27] and threshold voltage stability[28,29] in comparison to a-Si:H. This increased mobility allows for the shrinking of the TFTs that control the individual pixels of the display and subsequently allows for the creation of higher resolution displays with improved yield.

1.7.1 Composition of the Mixed Metal Oxide

The choice of the active layer composition has a significant effect on the device characteristics. Probably the most common mixed metal oxide semiconductor reported in literature is indium gallium zinc oxide (IGZO). Each of the metal oxide components of IGZO has a specific function. Indium oxide (In_2O_3) is a transparent conducting oxide. It is the overlapping spherical *s*-orbitals of the indium oxide that contributes the most to the high electron mobility of mixed metal oxide semiconductors. In comparison, carriers in amorphous silicon are transported through covalently bonded overlapping sp^3 or *p* orbitals. In the amorphous phase, the covalent bonds can be strained and impede transport. The *s*

orbitals of the amorphous mixed metal oxide are insensitive to local strained bonds and thus, electron transport is not affected significantly[30].

The zinc oxide introduces crystalline disorder into the mixture due to its hexagonal wurtzite structure. Indium oxides typically exist in bixbyite-type cubic crystals. When sufficient concentrations (~1:1 atomic ratio is common) of both oxides are present, no single structure can dominate, which results in the formation of an amorphous film. Amorphous films are desirable because they can be atomically smooth and do not have grain boundaries which can impede device performance[31]. The role of the zinc oxide is not purely structural, as zinc oxide also contributes to the high mobility of electrons in IGZO.

The gallium oxide introduces stability with respect to oxygen vacancies. Gallium-oxygen bonds are stronger than zinc-oxygen or indium-oxygen bonds. The gallium suppresses the formation of oxygen vacancies; this acts to decrease the electron mobility, but improves the long term stability of the device[32]. In spite of the vacancy suppression, it is still possible to fabricate a device with a field effect mobility of 10 cm^2/V-s with a V_T less than 1 V after 10 000 h of gate bias stress[28]. Much research is being focused on the choice of the vacancy suppressor. Aluminum[32], zirconium[31], and hafnium[33] have all shown significant decreases in mobility with a significant improvement in the long term stability of the device. Some of the key device parametric results along with the maximum process temperature are shown in Table 1.2. Included in the table are the current results for the a-Si TFT process at the Flexible Display Center (FDC) for comparison and recent “state of the art” results that have been published.

Due to concerns of the large range availability of gallium and indium, some groups, such as John Wager's group at Oregon State University, have chosen to focus on zinc tin oxide (ZTO)[24]. The performance of ZTO is comparable to IGZO, but requires a high temperature anneal (between 300 and 600°C) in order to achieve the same performance.

Table 1.2: Comparison of mixed metal oxide TFT performance for various materials

	μ_{sat} (cm^2/V-S)	V_T shift	V_T stress (s)	Max Process T (ºC)
a-Si:H[33]	0.77	0.6	30000	350
FDC a-Si:H[34]	0.7	10.4	10000	200
IGZO[35]	11	0.47	10000	250
ZrInZnO[30]	3.9	1	216000	350
HIZO[32]	9.3	0.43	57600	250
ZTO[36]	13.3	8	100000	400

1.7.2 Mixed Metal Oxide on Flexible Substrates

Although the performance of mixed metal oxides is superior to a-Si:H, the maximum process temperature typically exceeds 250 °C. It is important to note that the temperatures listed in Table 1.2 are only the maximum reported temperature. In most cases, the temperature of the active layer post deposition anneal is quoted, but the temperature of the PECVD steps is not listed. Thus, it is not surprising that reported performance on flexible substrates has lagged behind the results presented in Table 1.2. In addition, most reported results have used lift off processes or materials that would be incompatible with commercial display manufacturing.

IGZO TFTs have been fabricated on polyethylene terephthalate (PET) substrates[38] using the basic device structure shown in Figure 1.12. The maximum

process temperature for the process was listed as 90 ºC for the PECVD of the gate dielectric. Most of the layers were patterned using lift off. In, addition, the source/drain metal is IZO, which is too resistive (60 Ω/), for use in large area displays.

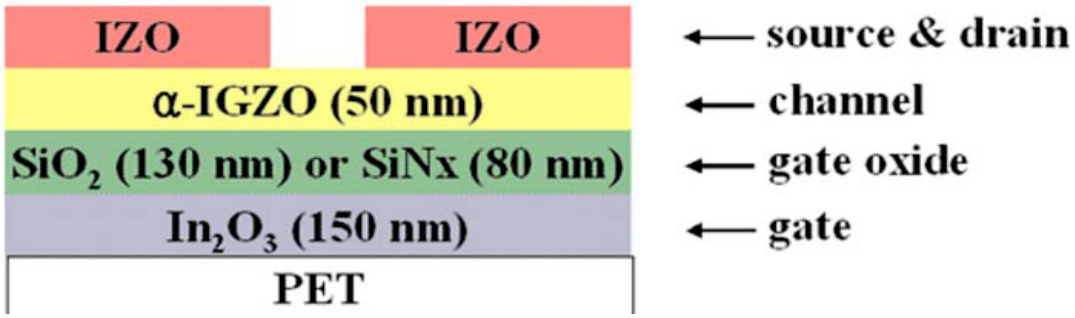

Figure 1.12: Basic device structure presented by Lim, et al.[38]

The device performance was comparable to the results presented in Table 1.2 with μ_{sat} of 12.1 cm^2/V-s and a V_T of 1.25 V. However, the leakage for these devices was on the order of 5 nA, which is approximately a factor of 1000 greater than desirable. In addition, device stability was presented in terms of shelf life, which means that the devices were not stressed for many minutes or even hours as they would during the regular operation of an electronic device. Instead, the devices were placed on a shelf and left to age and tested over a 6 month interval. The device performance did not significantly shift, which is desirable, but unremarkable.

Jackson, et al.[39] demonstrated ZTO TFTs fabricated on stainless steel flexible substrate with a saturation mobility of 14 cm^2/V-s. The maximum processing temperature was 300 ºC for the SiON gate dielectric. In addition, a 250

ºC anneal was performed after the deposition of the ZTO active layer. The more difficult patterning steps, specifically the ZTO patterning and the ITO source/drain contact, were performed by shadow masking during the deposition cycle. While the saturation mobility is comparable to other groups processing on rigid substrates, the threshold voltage is -16V and the leakage current is 0.1 nA. The extreme negative value for the threshold voltage is undesirable because of the large negative voltage that would be required to turn off the device. With a sufficiently negative gate voltage, any display fabricated with this technology would have low contrast.

Nomura, et al.[40], demonstrated IGZO TFTs with the structure shown in Figure 1.13 on polyethylene terephthalate (PET) sheets. Like Jackson, Nomura's group patterned most of the layers via shadow masking. The gate and source drain in this case are both ITO, which could not be used in a large area display.

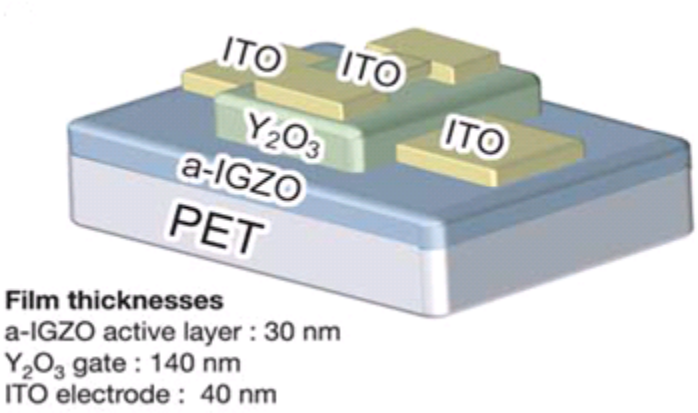

Figure 1.13: Flexible IGZO TFT structure presented by Nomura[40]

The saturation mobility reported by Nomura ranged from 6 to 9 cm^2/V-s on PET substrates. The leakage current for the devices was approximately 100

nA, which is far too high for use in a practical electronic device. The threshold voltage stability was not reported.

1.8 Conclusions

Although there have been many reports on mixed metal oxide device and their incorporation on flexible substrates, most of the work was conducted using processes and/or materials that would not be suitable for large scale production on large area displays. There appear to be many challenges in incorporating mixed metal oxides into a manufacturable process that have not been solved. While the drive performance, specifically the saturation mobility, of device fabricated on flexible substrates is comparable to the performance of the same devices on rigid substrates, most of the work presented has demonstrated poor off characteristics and limited or no long term V_T stability data. Chapters 2 and 3 will address some of these manufacturing issues and will present manufacturable solutions to the problem illustrated in Chapter 1. The work presented makes use of the bond/debond technique for processing on flexible substrates as the bond/debond process requires little additional capital equipment to be incorporated into an already existing display manufacturing facility.

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CHAPTER 2

HIGH PERFORMANCE MIXED OXIDE SEMICONDUCTOR TRANSISTORS ON FLEXIBLE POLYETHYLENE NAPHTHALATE SUBSTRATES

2.1 Introduction

The integration of high performance mixed metal oxide TFTs on flexible substrates requires the optimization of many individual semiconductor processes. The optimization process focused on the following processes: gate, gate dielectric, active layer deposition, active layer etching, source/drain metallurgy, and interlayer dielectric (ILD). These processes were optimized systematically through Design of Experiments (DOE) by fabricating transistors and evaluating the electrical performance.

An inverted staggered trilayer design similar to that previously described by Kaftanoglu et al.[1] was selected for the TFT as shown in Figure. 2.1. All processing conditions were selected to be compatible with fabrication of devices on flexible poly (ethylene naphthalate) (PEN) substrates. Devices were initially fabricated on silicon substrates capped with 300 nm of thermal SiO_2 to allow for cross-sections of the etch processes to be examined more easily.

The initial deposition baseline process conditions and the composition of the ZIO target were chosen based on previous results published by Itagaki[2]. The device parameters of transistors fabricated with this process were used as a baseline to compare future experimental results. In total, 60 wafers were processed under this baseline condition with 600 TFTs characterized. Once the

baseline was established, process improvements were sought through Design of Experiments.

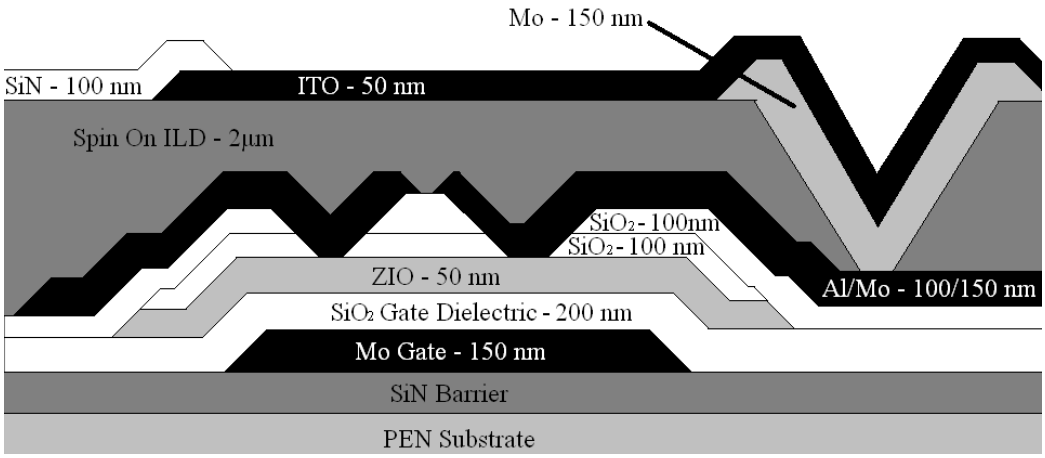

Figure 2.1: Inverted staggered trilayer TFT structure with active mesa sidewall passivation

Transistor performance data are measured for 20 individual test transistors with a 96-µm channel width W and 9-µm channel length L (W/L = 10.67) distributed at different locations on each wafer; every wafer in every lot is tested. We focused on the following seven key TFT performance parameters: drive current, effective saturation mobility, threshold voltage, subthreshold slope, hysteresis, and drain-source leakage current (off current) which served as responses in the DOE analysis. In addition, the performance of these parameters was also monitored with respect to electrical stress. The completed backplanes could be fabricated into bottom emitting OLED displays to demonstrate the results of the process development.

2.2 Experimental

2.2.1 Substrate

Most of the initial development was completed on thermally oxidized 150 mm silicon wafers. The substrates were nominally 675 µm thick with a crystal orientation of <100> and a bulk resistivity between 5-30 Ω-cm. The oxide layer was 300 nm thick. The function of the oxide layer was to insulate the gate metal from any potential parasitic effects of the silicon substrate.

Experiments were also conducted on flexible polyethylene naphthalate (PEN) substrates. The PEN substrate (125 µm thick) was obtained from DuPont Teijin Films (trade name Teonex Q65A) and was temporarily bonded to a 640 µm thick alumina carrier (CoorsTek) for processing[3].

A UV curable adhesive (Product no WFP20141- 94B) was obtained from Henkel Corporation and spin-coated on to the alumina carrier. A protective film (SEC Blue Low Tack Squares P/N 18133-7.50) was applied to the PEN prior to lamination to protect the processing side of the PEN from particles from the process. The PEN is cut approximately to a diameter of 144 mm to prevent the PEN from overlapping the edge of the alumina carrier and interfering with automatic flat finding modules in some of the process equipment.

The flexible PEN substrate was laminated to the adhesive-coated alumina carrier using a Western Magnum hot roll laminator. The adhesive was cured by exposing the adhesive to UV light (315-400 nm wavelength) through the transparent PEN substrate for 20 s in a Dymax curing unit. The bonded substrate

was baked under vacuum for one hour at 180 °C to test the viability of the bond to withstand the TFT fabrication processes.

The undersized PEN substrate results in a small amount of residual adhesive left at the edge of the alumina carrier. The adhesive is sensitive to many of the standard TFT processes and must be removed or else the material will embrittle and break off, forming particulates. The protective low tack tape is used as a mask to protect the PEN while the exposed adhesive is removed via oxygen plasma. The blue tape is then removed from the PEN substrate. The wafer is then cleaned in soapy solution consisting of 80 mL of Detergent 8 and 4L of DI water to facilitate desorption of contaminants followed by a rinse in a quick dump rinser (QDR) and spin dry in a spin rinse dryer (SRD). Following the rinse, a 300 nm thick layer of SiN is deposited on the surface to protect the PEN from future processing steps. The substrate is now ready for thin film processing.

The PEN/adhesive/alumina substrate system is designed to enable processing in typical semiconductor FAB equipment without handling issues associated with substrate deformation or photolithography alignment registration issues as described previously by Haq, et al.[3]. Device performance on PEN was generally equivalent to silicon. As the process improved, small differences between devices fabricated on PEN and devices fabricated silicon began to emerge due to significant reductions in the process variability. Therefore, 2-4 silicon wafers were always included in any PEN experiment to serve as a baseline.

2.2.2 Gate

The TFTs were fabricated with an inverted staggered design meaning that the gate metal is deposited first. At the Flexible Display Center, there are several choices for the gate metal including: molybdenum, aluminum doped with 1 % silicon by mass, “pure” aluminum, tantalum, ZIO, IGZO, and ITO. The mixed oxides ZIO, IGZO, and ITO were all eliminated because of their high sheet resistance (> 80 Ω/□). The gate itself does not need to carry current; however there are other locations with a contact down to gate that do carry significant current.

Molybdenum was chosen because of the ease of sloping the sidewall during etch and the smoothness of the surface compared to aluminum and tantalum. A smooth sidewall is important to ensure good step coverage of the subsequent thin film deposition. Inadequate step coverage can lead to drain to gate shorts, which can adversely affect the performance of a display TFT array.

A rough gate metal surface followed by conformal deposition by the gate dielectric and active layer could result in the artificial lengthening of the channel by scattering. If non-conformal deposition occurs, the gate could make contact with the active layer resulting in a short.

The molybdenum gate metal is deposited to a thickness of 150 nm. At this thickness, the sheet resistance is 1.0 Ω/□, which is more than adequate to handle the current flowing through the molybdenum at the locations where power lines must drop down to the gate level to pass under other power lines.

Following the deposition step, the wafers are cleaned with a soapy mixture of Detergent 8 (5 % by vol.) and DI water in an ultrasonic tank. The wafers are then rinsed in a quick dump rinser (QDR) with DI water and dried in a spin rinse dryer (SRD).

After cleaning, the wafers are patterned with a photoresist (AZ Materials 5214E) layer. The wafers first pass through a vacuum oven where a thin coat of hexamethyldisilazane (HMDS). The photoresist is spun to a thickness of 1.5 µm. Following the spin, the wafers are baked on a hot plate at 105 °C for 60 s. The spin and bake take place on a Rite Track 8800 automated cassette to cassette track coater. The wafers are given a unique serial number near the wafer flat at this step using an SSI-1000 exposure tool that exposes small circular dots. The wafer is translated through the field of view to produce characters. The main gate pattern is defined by UV light exposure in a Canon MPA 600-MF projection aligner. The stepper magnification ratio is 1:1 meaning the exposed pattern is the same dimension as the pattern on the mask. The exposure energy density is 140 mJ/cm^2. The wafers are then puddle developed for 60 seconds using AZ MIF 300 developer followed by a final hard bake at 140 °C for 60 s. This final reflow bake partially melts the resist resulting in the formation of rounded features due to surface tension on the melted resist.

The rounded features have sloped edges that can be easily transferred to the underlying material through a non-selective etch process. In this case, the selected etch process is dry etching. A dry etch allows for greater control of the sidewall profile and critical dimension (CD) than wet etching. The dry etch takes

place in an Applied Materials 8330 (AMAT 8330) batch etch system. The AMAT 8330 can etch 18 × 150 mm wafers at a time.

2.2.3 Gate Dielectric and Passivation

There were three candidate materials (SiO_2, SiN, and Al_2O_3) for thin film dielectric layers. These three materials were evaluated by fabricating metal-insulator-metal (MIM) capacitors and testing the breakdown characteristics of the insulator. The materials were then inserted into the TFT process where the output and transfer characteristics were compared.

To dry etch the dielectric layers, a reactive ion etch (RIE) (Tegal 901) was utilized operating at 200 Watts, 400 mTorr, nominal substrate temperature of 40 °C, and a gas feed consisting of 10 sccm of CHF_3 and 20 sccm of O_2.

2.2.4 Active Layer Deposition

A ceramic target with a composition of 60% zinc oxide and 40% indium oxide by mass, similar to the composition reported by Itagaki[2], was utilized for deposition of the active layer in the initial development work. The ZIO was deposited using DC reactive sputtering (MRC 603 sputtering system) operating at 200 W (0.439 W/cm^2) at a pressure of 6 mTorr and a nominal substrate temperature of 40 °C. A mixture of argon and oxygen (2 % O_2) was used as the deposition feed gas.

The initial deposition baseline process conditions and the composition of the ZIO target were chosen based on previous results published by Itagaki. The

process conditions for this baseline condition were 6 mTorr operating pressure, 200 W operating power, 4 sccm of O_2 and 200 sccm Ar. In total, 60 wafers were processed under this baseline condition with 600 TFTs characterized.

2.2.5 Active Layer Etching

Photolithographic patterning of the layers was performed using a Canon MPA-605 aligner with AZ Materials 5214 photoresist. After etching, the photoresist was stripped in a Gasonics L3510 downstream microwave plasma asher.

To dry etch the ZIO active layers, the AMAT 8330 was operated at 1000 W (0.314 W/cm^2), 10 mTorr, a nominal substrate temperature of 95 °C, and a feed gas consisting of 100 sccm of HCl, 20 sccm of O_2, and 10 sccm of CH_4. A similar dry etch process was reported by Saia, et al.[4] for indium tin oxide (ITO).

Two wet etch processes were explored for the patterning of the ZIO active layer. The first consisted of a commercial buffered HF (10% by volume) and deionized water mixture (Ultra Etch NP 10:1 manufactured by KMG Electronic Chemicals). The buffered hydrofluoric acid mixture was also used to etch silicon dioxide dielectric layers. Diluted HF is commonly used to etch zinc oxide based materials during TFT fabrication[5,6,7,8].

The second wet etch consisted of a mixture of 37% HCl (45% by volume), 69.5% HNO_3 (5% by volume), and deionized water (50% by volume). This mixture is common in LCD manufacturing for the patterning of indium tin oxide

(ITO)[9] as it does not attack glass, which is a common substrate for display applications.

To characterize the structure of the devices, a field emission scanning electron microscope (FESEM, JEOL 6300) was employed. Samples on silicon wafers were cleaved to fit into the FESEM and gold coated in a Hummer 6.2 sputter system for 120 s to a thickness of approximately 15 nm. Cross-section samples were mounted in a sample holder with the cleaved side of interest facing the gold target while top-down samples were mounted with the processed side of the wafer of the wafer facing the target.

2.2.6 Contact Etching

A Mesa Passivation deposition follows the active layer etching. The mesa passivation is 100 nm thick and protects the exposed sidewall of the metal oxide active layer from future processing. The layer is composed of PECVD SiO_2 and uses the same process conditions described in the gate dielectric section.

In the inverted staggered trilayer device setup, contacts must be opened to the gate and the metal oxide active layer. These two layers are at different levels meaning that the respective contacts' vias will be at different depths. In the a-Si process, separate masks were fabricated for the two contacts as the a-Si contact was the shallower via. Etching SiN or SiO_2 selectively with respect to a-Si is very difficult without using hydrofluoric acid (HF). Buffered HF does not etch a-Si, but the critical dimension (CD) of the contacts can be blown out during the requisite overetch to open the deeper gate contacts. In order to preserve the CD of

the active contacts, separate masks were used to open the active contact and gate contact.

This design feature was incorporated into the mixed oxide TFT process because the a-Si TFT mask sets were used to initially characterize the mixed oxide TFT performance. As stated in Section 2.1.4, the mixed oxide materials are vulnerable buffered HF. Since buffered HF is not an option, dry etching must be used[10].

A controllable slope was obtained using the Tegal 901 RIE system. The pressure is set to 400 mTorr, the power to 150 W, the O_2 gas flow was set to 10 sccm and the CHF_3 was set to 20 sccm. The process was originally designed for a contact etch that opened on to ITO. It was determined that OLED diodes that were fabricated on ITO that had been etched by CHF_3 outperformed OLED diodes fabricated on ITO that had been etched by SF_6. It was reasoned that the carbon from the CHF_3 was scavenging oxygen from the surface of the ITO creating an oxygen deficient surface that reduced the contact resistance. Both the gate and active contacts are opened with the same process for the same duration in anticipation of combining the etch steps in a future design.

2.2.7 Source Drain Metallurgy

As with the gate metal, there is a large selection of materials available to choose from including: molybdenum, aluminum doped with 1% silicon by mass, “pure” aluminum, tantalum, ZIO, IGZO, and ITO. Initial experiments focused on molybdenum as the source/drain metal due to its usage by many groups pursuing

metal oxide TFTs[6,11,12]. However, the sheet resistance for molybdenum is 1.0 Ω/□ which was determined to be too high for display applications based on simulations, especially as the display resolution increased beyond QVGA. In addition, these initial experiments only focused on fabricating TFTs without subsequent display builds, and therefore only required processing through source/drain metal. Additional layers are needed to fabricate the pixel anode. These additional layers require etching processes that are not highly selective to Mo.

Ideally, the source/drain layer should be resistant to fluorine plasmas as the next layer deposited (ILD) is 2 µm and is etched in an SF_6/O_2 plasma. Mo etches rapidly in this plasma process and would be easily removed during the overetch of the ILD. Therefore, it was decided to explore materials that are impervious to fluorine plasma. Two materials, ITO and Al with 1% silicon were considered viable candidates because they were already qualified for use in the a-Si TFT process. However, a literature search indicated that Al/ITO contacts were undesirable due to the formation of insulating aluminum oxide at the interface[13]. In addition, Barquinha, et al.[12], had noticed severe current crowding in the output characteristics at low drain voltage in devices fabricated with Al S/D contacts indicating the creation of a large barrier between the aluminum and the metal oxide active layer. Instead, it was decided to use Al in combination with an interfacial layer. In this experiment, Ta and Mo were chosen as the contact layers. An additional cell featuring ITO was also included.

The source/drain metal is deposited in a KDF 744 or an MRC 603 sputtering system. The initial development was performed using 150 nm of molybdenum sputtered at 1000 W at 6 mTorr with 100 sccm of Ar. TFTs using the standard molybdenum source/drain metal were compared with devices featuring ITO, a bilayer featuring 200 nm of Al doped with 1 % by wt Si with a 50 nm Ta contact layer, and a bilayer featuring 200 nm of Al with a 150 nm Mo contact layer.

2.2.8 Interlayer Dielectric (ILD)

The PTS-R ILD process begins with the coating of a 100 nm thick SiO_2 wetting layer. A wetting layer is necessary because the solvents used to dissolve PTS-R are corrosive to aluminum. SiO_2 was chosen over SiN because the relative etch rate of SiO_2 is slower than both SiN and PTS-R. The SiO_2 is at the bottom of the via. During the etch, the PTS-R will be etched faster than the SiO_2 resulting in a shallow slope at the bottom of the via.

The PTS-R is syringe dispensed on to the SiO_2 using a manual syringe on a Rite Track 8800 coater track. The wafers are soft baked at 200 ºC for 1 min to drive off most of the solvents and then cured in a Despatch Oven at 200 °C for 1 h. The PTS-R is then capped with a 100 nm SiO_2 layer to protect the PTS-R from the harsh etch chemistries of the later processes. AZ 9260 resist is spun to a thickness of 3.3 µm with a reflow bake at 140 °C to slope the sidewalls.

2.2.9 Pixel Anode

The pixel anode consists of a 150 nm molybdenum plug, 50 nm ITO layer, and 100 nm SiN Overglass passivation layer. The Mo plug serves as an interfacial layer between the aluminum source/drain metal and the ITO anode[13] and a contact for the Mg/Ag OLED cathode metal. For top emitting OLED designs, the anode also serves as a reflector that blocks light from passing through the TFT and the substrate. The Mo deposition process is identical to the deposition of the gate metal. The metal is sputter deposited in a KDF 744 or MRC 603 sputter tool to a thickness of 150 nm. The sheet resistance at 150 nm is 1 Ω/□. The Mo plug is photo patterned and etched in the same manner as described in Section 2.2.2.

The ITO layer is reactively sputtered in a KDF 744 using 5000 W of RF power at a frequency of 13.56 MHz. The target is a ceramic target that is 90 % indium oxide by mass and 10 % tin oxide. The pressure is set to 3.5 mTorr by flowing 5 sccm of O_2 and 100 sccm of Ar. The ITO is etched using the same dry etch that was described in Section 2.4 for the active layer.

The ITO is capped with a 100 nm SiN passivation layer (Overglass) to define the active pixel area and to prevent dirt from bridging neighboring ITO anodes. The layer is etched using the same process described in Section 2.7 for the contact etch. Once the resist is stripped using the Gasonics L3510 ash process described previously, the samples are rinsed in the QDR and dried in the SRD. The back plane process is considered complete after this step.

2.2.10 OLED Display Build

OLED backplanes feature two transistors and one capacitor in each pixel. The electrical schematic for an OLED pixel is shown in Figure 2.2

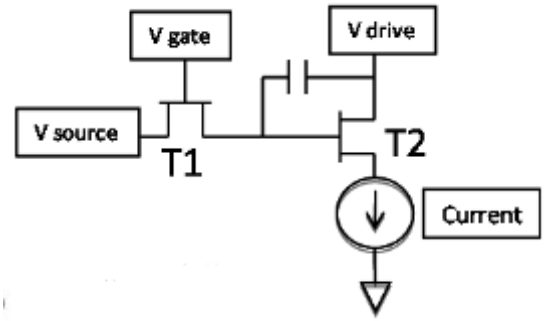

Figure 2.2: OLED pixel circuit diagram

The display operates by “scanning” the gate voltage along one of the axes of the display. Voltage is applied to only one gate line at a time. The amount of time it takes for all of the gate lines to be activated determines the refresh rate. For example, a 60 Hz display will cycle through every gate line 60 times in 1 s. The gate voltage is set significantly above the source voltage (usually 12-15 V) to put the row select TFT (T1 in Figure 2.2) in the linear region. In this mode, T1 behaves like a variable resistor where the drive current is proportional to the source voltage. The source line voltage is adjusted for each line during the gate scan and determines the amount of charge that will be stored to the capacitor. Since T1 is off during most of the cycle, a capacitor is needed to make sure that the OLED is lit for the entire cycle. The voltage applied to the gate of the drive TFT (T2 in Figure 2.2) is set by the voltage applied by V source during the gate

scan. V drive is constant and is set to a value that places T2 in saturation (usually 12-15 V). In saturation, T2 behaves like a constant current source that is controlled by the gate voltage which is set by the source voltage applied to T1. OLEDs are current controlled diodes. As the current increases, the luminance of the OLED emitting materials increases. In a color display, blue, green, and red emitting materials can be deposited in adjacent pixels. By adjusting the current (and thus the luminance) of the adjacent pixels, one can create a wide gamut of colors. In this work a monochromatic flexible OLED is fabricated.

2.3 Results

2.3.1 Gate

The original etch process was developed for the FDC's a-Si TFT process as described by Raupp, et al.[14] where adequate results were achieved when the thickness of the SiN gate dielectric was increased from 200 nm to 300 nm. Initial experiments with the original gate etch combined with the 200 nm thick silicon dioxide gate dielectric demonstrated limited gate to source shorting at crossovers. The shorting was hypothesized to have originated from either pinholes in the silicon dioxide or inadequate step coverage of the silicon dioxide over the gate metal sidewall. Data presented in the gate dielectric section indicated that pinholes in the dielectric were unlikely so the gate metal etch profile was studied.

The step coverage of the SiO_2 gate dielectric and passivation layers was investigated by fabricating wafers through all processing steps until the contacts had been opened. At this point, the ZIO active layer is protected by the Mesa

Passivation and the IMD and is only exposed where the source/drain contacts were opened. Six wafers processed with the standard gate metal etch were dipped in a mixture of 37% HCl (45% by volume), 69.5% HNO_3 (5% by volume), and deionized water (50% by volume). This mixture is common in LCD manufacturing for the patterning of indium tin oxide (ITO)[9] and also etches ZIO. The HCl/HNO_3 mixture was selected because the etch rate of SiO_2 in the mixture is negligible. The contacts were opened to allow the mixture to attack the exposed ZIO to provide a visual reference. The wafers were submerged in the bath for 8 minutes and examined under a microscope. Figure 2.3 shows a microscope image after the dip.

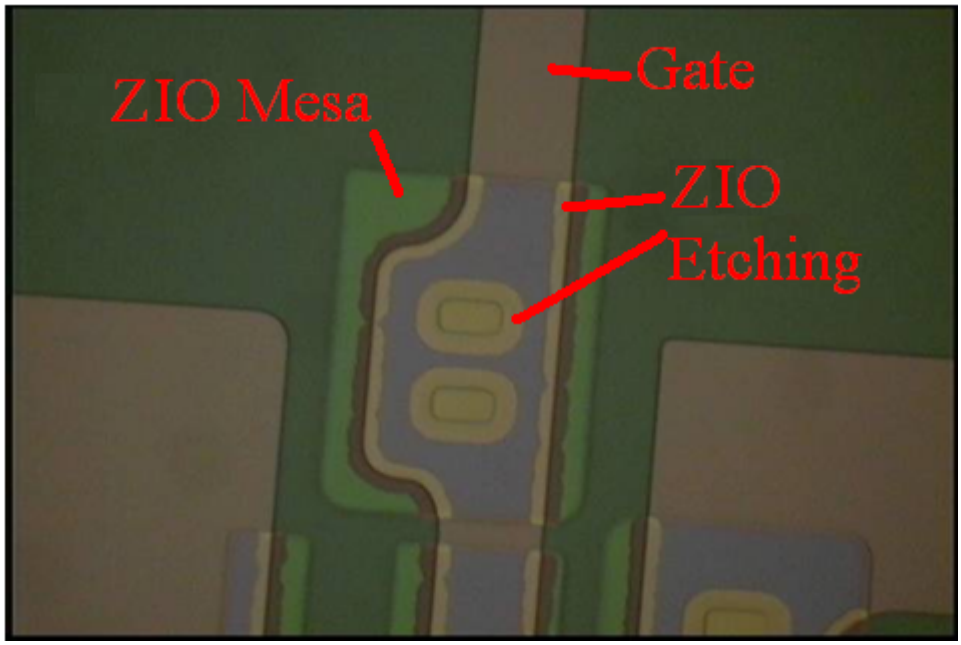

Figure 2.3: The ZIO active layer has been attacked by the HCl/HNO_3 mixture where the active layer crosses over the gate.

The image shows that significant IGZO etching took place at the contact openings (expected) and at locations where the IGZO crossed over the gate metal. The IGZO was not etched along boundaries where there was no gate metal crossover further supporting the hypothesis of inadequate step coverage over the gate metal. Additional wafers were processed through the full process and were examined in a JEOL 6100 field emission scanning electron microscope (FESEM). Figure 2.4 demonstrates a typical gate metal crossover.

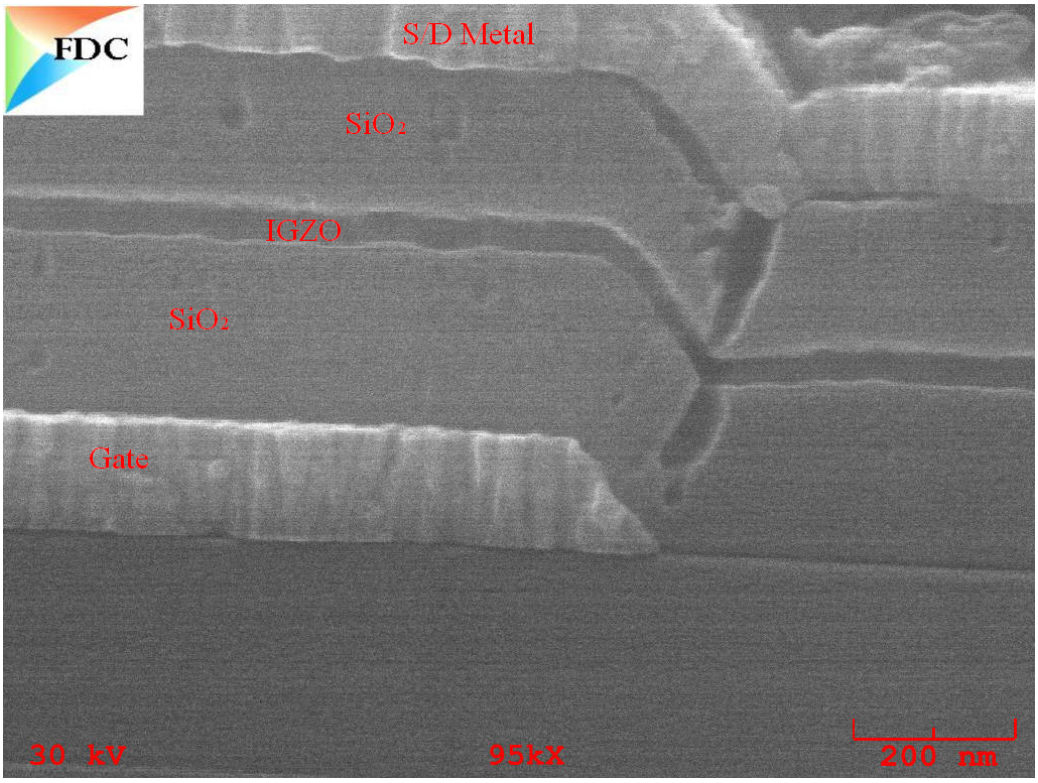

Figure 2.4: FESEM Micrograph demonstrating voids in the gate dielectric, IGZO active, and passivation layers

The micrograph shows that there are voids present in the IGZO active and SiO_2 passivation layers. Although the voids in this micrograph do not extend completely to the gate in this particular micrograph, there is sufficient evidence to suggest that the coverage is inadequate.

It was decided to adjust the slope of the gate etch instead of altering the SiO_2 deposition process to improve the conformality of the deposition process. Changing the gate dielectric characteristics to improve step coverage could have unintended deleterious effects on the device performance. Changes to the gate metal etch sidewall profile would allow for improved step coverage without risking drastic changes to the device performance.

The etched sidewall angle was decreased by simply increasing the oxygen to chlorine ratio from 1:1 (80 sccm: 80 sccm) to 6:1(90 sccm: 15sccm) while maintaining the pressure at 15 mTorr and power at 600 W. The increase in the oxygen concentration increased the photoresist erosion rate resulting in a flatter sidewall profile as shown in Figure 2.5.

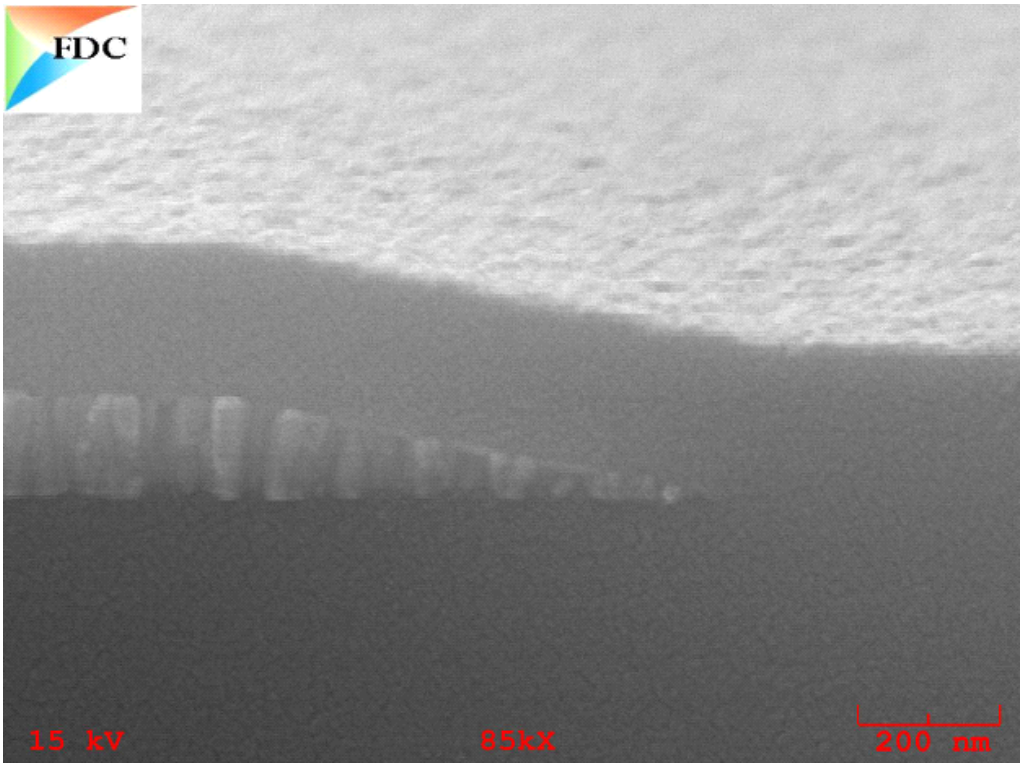

Figure 2.5: FESEM micrograph showing improved step coverage with reduced sidewall profile angle

Devices fabricated with the new etch process did not show a statistically significant difference when compared to devices fabricated with the original etch process. However, the functional TFT yield increased significantly from 50 % to 83 %, as the number of source to drain shorts in the array decreased.

2.3.2 Gate Dielectric and Passivation

Aluminum oxide was eliminated because the breakdown voltage was less than 20 V for more than half of the capacitors fabricated. This breakdown level is woefully inadequate for TFTs where the gate to source voltage reaches a maximum of 20 V during test. Breakdown tests on capacitor structures featuring

300 nm of silicon nitride indicated that the breakdown voltage is 230 ± 31 V, and a 3-sigma lower limit (137 V) that is significantly larger than the maximum expected operating voltage. Breakdown tests on capacitor structures featuring 100 nm of silicon oxide indicated that the breakdown voltage is 313 ± 32 V, with a 3σ lower limit (217 V) that is significantly larger than the maximum expected operating voltage.

The SiN deposition process was designed for use with a-Si TFTs. With respect to a-Si:H, the known critical materials properties that correlate with film quality and resulting TFT performance include N:Si atomic ratio, hydrogen concentration, and SiH_2/SiH ratio[4]. Film stress is important for process integration issues including film adhesion, whereas index of refraction has been shown to be a good indicator of film quality[15] with indices in the 1.85–1.90 range, exhibiting the best performance and specifically the lowest V_t. Using the available literature as a guide, a baseline 180 °C PECVD process was developed using conditions that produced a nitrogen-rich film (N:Si atomic ratio >1.6) with an average index of refraction of 1.85. The SiH2/SiH ratio was minimized by employing a low applied power density and high hydrogen dilution factor of more than 50:1 (silane to molecular hydrogen flow rate), which resulted in a slow deposition rate process (~1 nm/s).

Fourier Transform Infrared Spectroscopy (FTIR) demonstrates the presence of a significant amount of hydrogen as indicated by the presence of a peak at 2200 cm^{-1} in Figure 2.6[16]. The other peaks correlate to SiN breathing

mode at 500 cm^{-1} and stretching mode at 845 cm^{-1}, Si–NH–Si bending mode at 1100 cm^{-1}, and NH stretching mode at (3320 cm^{-1}).

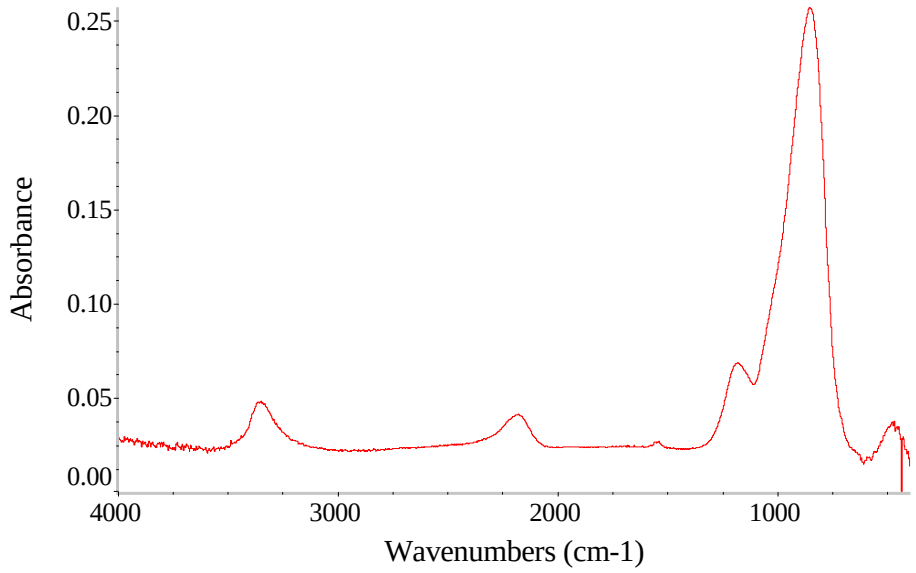

Figure 2.6: FTIR Spectra of Typical SiN Gate Dielectric Layer

SiN is a more desirable choice as a gate dielectric than SiO_2 because of its higher dielectric constant (7.0) in comparison to SiO_2 (3.9). The dielectric constant and the dielectric thickness determine the capacitance per unit area as defined by the following equation:

$$C_{gate} = \varepsilon_0 \varepsilon / t_{gate} \qquad (2.1)$$

where C_{gate} is the gate dielectric capacitance per unit area, ε_0 is the permittivity of a vacuum (8.854×10^{-12} F/m), ε is the dielectric constant of the gate dielectric, and t_{gate} is the thickness of the gate. A larger C_{gate} is desirable as transistors are

dependent on the electric field applied in the active region. In addition, a higher dielectric constant allows for smaller capacitors to be fabricated which can free up space to improve yield or allow for higher density arrays.

However, SiN depositions usually incorporate a significant amount of hydrogen. Hydrogen is a known donor in oxide transistors[52], so minimizing the hydrogen content was believed to be an important factor in the device lifetime. The silicon oxide deposition process therefore avoided the use of hydrogen as a process gas. It was expected that some hydrogen would remain in the film because of the presence of silane, so an attempt was made to minimize any peaks in the FTIR related to hydrogen. The etch rate of the SiO_2 film was tested in a 1:10 mixture of Buffered Oxide Etch (BOE) and water. The FTIR spectra and BOE etch rate were compared to the spectra and BOE etch rate of thermal oxide films grown by Rogue Valley.

Figure 2.7 shows the absorbance spectra in the 4000–500 cm^{-1} range for three films deposited at SiH_4 to N_2O flow ratios of 5:2000, 35:2000, and 65:2000. These values constitute two of the axial runs as well as the center point for the central composite design used to screen and optimize the SiO_2 film. A spectra from a 300 nm thick thermal oxide film from Rogue Valley is also included.

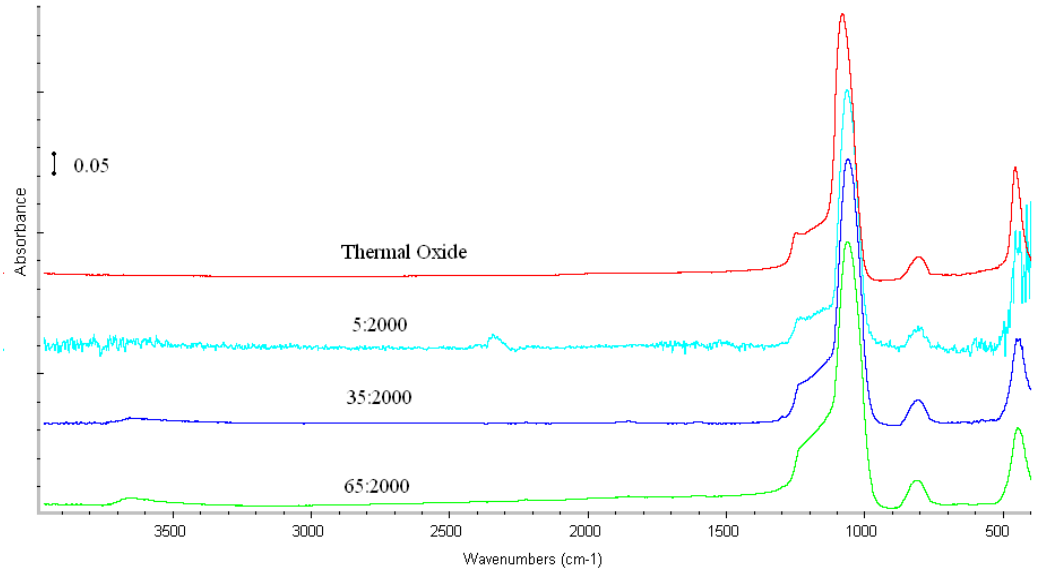

Figure 2.7: Transmission infrared spectra for as-deposited SiO2 films at fixed applied plasma power, total pressure, and nitrous oxide flow rates for three different SiH_4:N_2O flow ratios.

All of the spectra show the expected absorption bands at 450 cm^{-1}, 800 cm^{-1}, and 1040 cm^{-1}. These peaks are attributed to the rocking, bending, and stretching of the Si–O bond[18,19]. The large peak at 1040 cm^{-1} has a shoulder that seems to peak at 1250 cm^{-1}. The ratio of the peak height to the shoulder should give a relative comparison for the density of the film[520]. A lower peak height at 1250 cm^{-1} relative to the peak height at 1040 cm^{-1} indicates a more dense film. The film density appears to increase with lower silane flow.

With the exception of the thermal oxide film, all of the spectra show evidence of the presence of hydrogen due to the broad and shallow peak near 3650 cm^{-1} that is typically attributed to silanol (Si–OH) stretching vibrations[18]. Eliminating the presence of hydrogen in PECVD grown SiO_2 is usually

accomplished with a high temperature anneal post process. The required anneal temperature to effectively eliminate the appearance of silanol in the FTIR spectra can be as low as 350 ºC which is far above the glass transition temperature for most plastics. Since the ultimate goal is process on PEN, which has a glass transition temperature is approximately 240 ºC; it was decided to simply minimize the ratio of Si–OH to Si–O.

The process featuring a feed gas flow ratio of 35:2000 (SiH_4: N_2O) was eventually selected for the baselining experiments because the deposition rates of the lower silane concentration films were below 0.25 Å/s. The deposition rate for the selected process is 2.8 Å/s. Breakdown tests on capacitor structures featuring 1000 Å of silicon oxide indicate that the breakdown voltage is 313 +/- 32 V, while the BOE etch rate is 34.3 +/- 0.5 Å/s.

TFTs were grown with the same basic structure but with different gate dielectrics to compare the effect of the gate dielectric composition. Devices with 300 nm of SiN as a gate dielectric were considered shorted between the source and drain as there was limited control of the drain current by the gate voltage. Devices with 200 nm of SiO_2 as a gate dielectric demonstrated expected transistor behavior with adequate off current as shown in Figure 2.8.

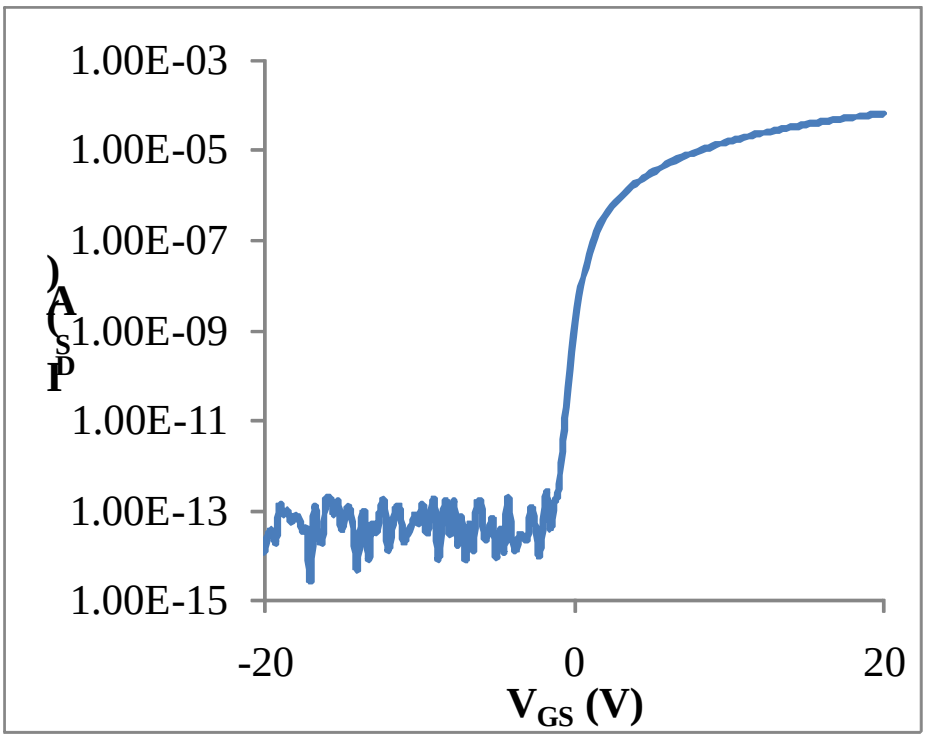

Figure 2.8: I_{DS}-V_{GS} curve of TFT with 200 nm SiO_2 gate dielectric

It was hypothesized that the hydrogen from the SiN migrated into the active layer and reacted with the metal oxide to create oxygen vacancies thus swelling the carrier concentration. In an attempt to prevent the hydrogen from reacting with the metal oxide active layer, another experiment was completed with a two layer gate dielectric consisting of 200 nm of SiN in contact with the gate metal and 50 nm of SiO_2. The capacitance of the SiN and SiO_2 can be added together and expressed as an effective SiO_2 thickness of 161 nm. Devices fabricated with this two layer stack should demonstrate a higher current than devices with 200 nm of SiO_2 as the gate dielectric.

Devices fabricated with the SiN/SiO_2 demonstrated a higher drive current (56.2 µA) in devices with a 9 × 9 µm IGZO active area than devices fabricated

with a single layer of SiO_2 (22.1 μA). However, there were still a significant number of failures with high source to drain leakage. Of the 168 devices tested, 125 (74.4 %) demonstrated leakage greater than 1 μA. None of the 168 devices with the single layer of SiO_2 demonstrated a leakage higher than 0.4 pA. The results suggest that increasing the thickness of the SiO_2 would help reduce the leakage even further. However, additional increases in the SiO_2 thickness would decrease the capacitance. Since the devices with the single layer of SiO_2 demonstrate consistently low leakage, it was concluded that the single layer of SiO_2 was the most appropriate gate dielectric given the selection.

2.3.3 Active Layer Deposition

The mixed oxide material to be tested was zinc indium oxide (ZIO). The ZIO layer was deposited by reactive DC sputtering using a ceramic target with a composition of 60 % zinc oxide and 40 % indium oxide to allow for direct comparison to results reported by Itagaki[2].

The median performance of the baseline, as well as the median performance after active layer deposition optimization, is summarized in Table 2.1. The saturation mobility of the baseline is much lower than reported by other groups while the subthreshold slope is much higher[22,23,25].

Screening experiments indicated a strong dependence on the oxygen content in the feed gas. If the oxygen gas flow was shut off, the film sheet resistance dropped to 300 Ω/□ on a 50 nm thick film. Devices fabricated at conditions with no oxygen added would fail to turn off. The optimal setpoint was

therefore the minimum possible setpoint of the oxygen mass flow controller. This minimum setpoint resulted in a feed gas mixture that was 2 % oxygen.

Table 2.1: TFT performance parameter summary for the ZIO process (initial baseline through active layer deposition optimization)

Parameter	Initial Baseline	Post ZIO Optimization
Drive Current (μA)	23.8	49.6
Sat. Mobility (cm^2/V-s)	1.36	2.29
Subthreshold Slope (V/dec)	1.31	0.51
Threshold Voltage (V)	3.3	1.6
Log (S-D Leakage (A))	-12	-13.1
Hysteresis (V)	0.25	0.25

Once the oxygen concentration was set, further optimization of the process pressure and power revealed that the threshold voltage could be reduced with no deleterious effects by increasing the sputter power. The drive performance improvement was statistically significant, but still paled in comparison to results from other groups with similar material sets[22,23,25]. Details of the process improvements necessary to improve the device performance are covered in detail in Chapter 3.

2.3.4 Active Layer Etching

2.3.4.1 Wet ZIO Etch

To provide calibration for the etch rates, blanket-coated ZIO wafers are examined as a function of the etch composition. A standard buffered HF (10 vol-%) etch can fully remove a 50 nm thick ZIO film within 5 s. By switching to a 5

vol-%HCl/45 vol-%HNO_3 mixture in water, the ZIO etch rate is reduced to 6.1 nm/min. The slower etch rate of the HCl/HNO_3 is desirable for process control; the typical duration of an etch process is on the order of 5-10 min. The extremely fast etch rate of the buffered HF makes precise CD control difficult as the total etch time required is only several seconds.

With the relative etch rate understood for the two wet chemistries, lithographic patterning of the ZIO provides a route to understand how the etch chemistry impacts the sidewall morphology of the wet etch. Figure 2.9 illustrates the sidewall profile obtained using the buffered HF etch. This sidewall has a dimpled appearance, which can lead to difficulties in conformal coverage in comparison to a smooth surface. For traditional rigid substrates such as silicon or glass, this morphology generally does not significantly adversely impact yield, but deposition conformality requires higher temperatures that can pose serious problems for flexible plastic substrates. Additionally, the uneven sidewalls could lead to local thickness variations in the subsequent film depositions. The variation would, at a minimum, require additional overetching during subsequent etching steps to prevent shorting. In a worst case scenario, thin films may have difficult covering the topology to yield voids in the structure that could be detrimental to performance.

To explain the origins of the dimpled morphology, the relative selectivity of the wet etch for zinc oxide and indium oxide can be significantly different, which will leave pockets of one oxide. This selectivity difference creates rougher surfaces at the line edge than a more non-selective etch would generate. In

addition to the rough sidewall, the ZIO is still not fully cleared from the line using the fast HF wet etch. Two potential causes for the particles in the field are again the relative etch selectivity that might not fully clear the area or formation of particles at the sidewall by selective dissolution of one component of the metal oxide. If loose particles are formed, this could significantly impact device yield in a manufacturing environment. The particles can be eliminated by increasing the etch time. However, there is a tradeoff because a patterned film will continue to be etched laterally during this overetch. Despite the significant difference in etch rate between the buffered HF and HCl/HNO_3 solution, a similar sidewall profile is also obtained when using HCl/HNO_3 for the wet etch. Figure 2.9 shows that there are still pieces of the etched film in the field

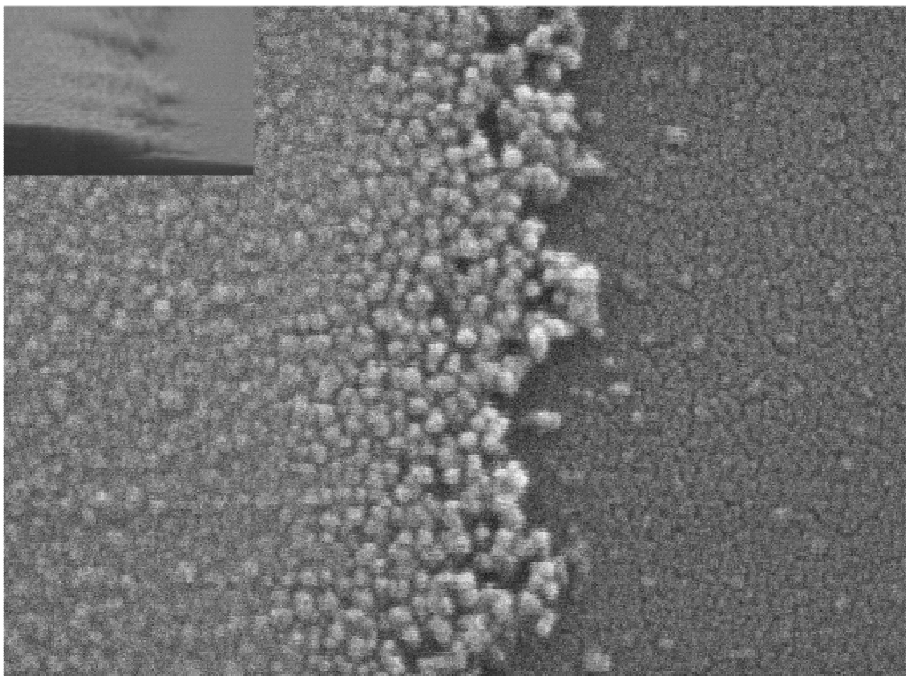

Figure 2.9. Micrographs of lithographically patterned line edge using a buffered HF etch of ZIO. Inset illustrates a cross-section of the patterned feature. The sample was gold flashed prior imaging.

In addition to the concerns regarding sidewall uniformity present in the wet etch of ZIO, there are additional potential complications in the selected device architecture (Figure 2.1); due to the overlay, the same mask is used in the etch of both ZIO and the SiO_2 channel passivation layer. In this case, the relative etch rates for the ZIO and SiO_2 are important to controlling the final lithographically defined features. For both wet etch chemistries, the ZIO etches significantly faster than the SiO_2 layer (138 nm/min for HF and <0.2 nm/min for HCl/HNO_3). This difference in etch rate could lead to a substantial undercut of the SiO_2 passivation, which is unfavorable for step coverage of the source/drain metal. Figure 2.10 illustrates a representative cross-section micrograph of the features formed using the buffered HF wet etch when the SiO_2 passivation layer and subsequent deposition/patterning are included to create an operating TFT. The ZIO layer in this case is etched laterally, which creates a 1 µm overhang in the SiO_2 passivation layer. The HCl/HNO_3 etch also yields a significant overhang that is similar to that obtained from buffered HF.

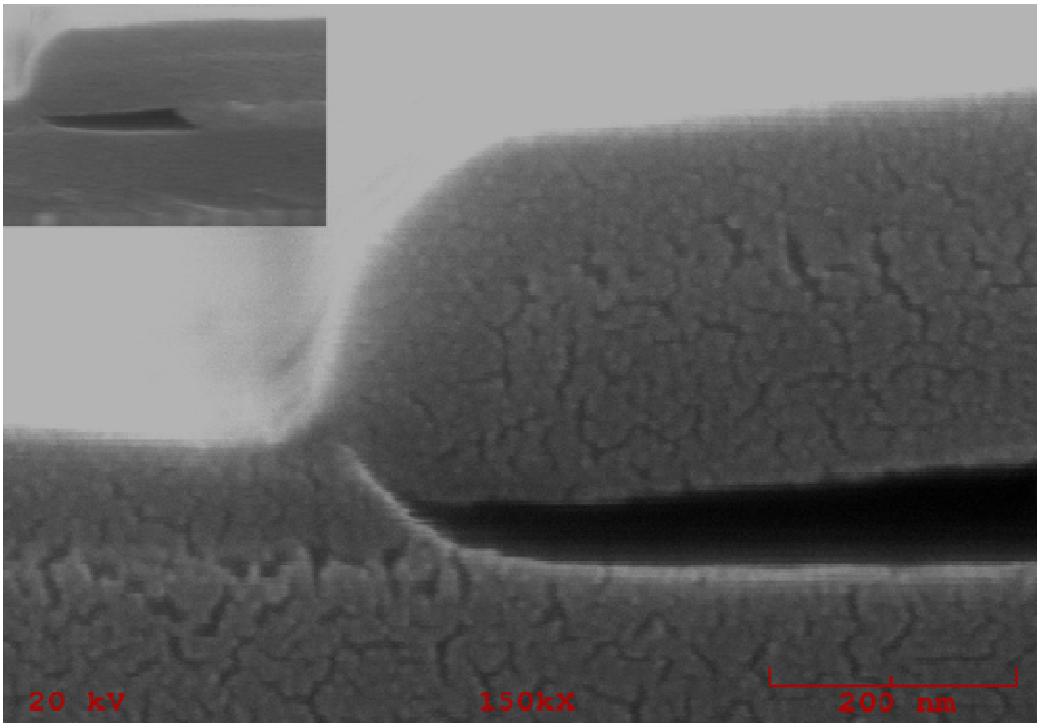

Figure 2.10: Cross section micrograph of wet etch for ZIO when passivation layer and subsequent deposition/patterning are included. The ZIO is undercut, but there is still adequate step coverage for an operational TFT

The subsequent deposited layer for mesa sidewall passivation is able to cover the sidewall, but the mesa sidewall passivation appears to be forming a crack. A top down schematic of the device structure is presented in Figure 2.11. The overhang shown in Figure 2.10 is represented by the solid (green online) line surrounding the rectangular ZIO active area. Conductive Mo or Al could be deposited into the area underneath the overhang during the subsequent source/drain metal sputter deposition. Metal deposited under the overhang would be shielded from the directional RIE etch of the source drain etch. Ultimately this mechanism would yield a continuous thread of metal capable of shorting the

source to the drain as illustrated in Figure 2.11, which would degrade device yield.

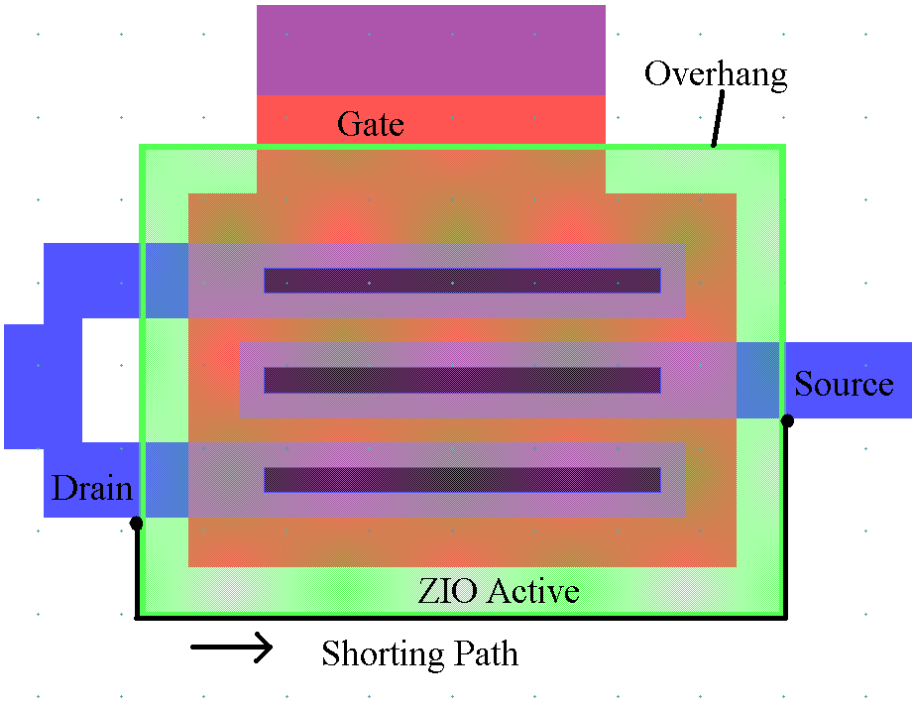

Figure 2.11: Schematic of potential short path that can develop from the undercutting wet etch chemistry

To further investigate the impact of the wet etch undercut, the transistor performance for a total of 60 TFTs is tested for each of the two wet etch processes with no statistical difference in performance between buffered HF and HCl/HNO_3 etch. In both cases, the device yield was less than 50% with a significant number of these failed devices exhibiting shorting of the source and drain; this finding is consistent with the proposed shorting from undercutting of the ZIO (Figure 2.10). To further illustrate these issues with these devices, I_{off} is

<1 μA for only 34 of the 120 devices tested. The results show intrawafer variation; a single wafer typically has some devices with reasonable transistor characteristics randomly mixed with transistors that exhibit significant shorting between the source and the drain. The mean TFT performance using the wet etch (among the 49 devices that exhibit transistor characteristics) is a V_T of -3.42 ± 1.47 V, μ_{sat} of 6.57 ± 0.73 cm^2/V-s, a SS of 2.41 ± 1.01 V/decade, an on current (I_{on}) of 35.3 ± 3.3 μA/(W/L), and a median I_{off} of 61.2 nA/(W/L).

2.3.4.2 Wet ZIO Etch with Etch Stopper Structure

In order to avoid the undercut problem, separate etch of the ZIO layer and the passivation layer could be performed with an additional passivation layer deposited after patterning the source/drain material to cover the exposed portions of the ZIO active layer. This additional passivation layer protects the ZIO from adsorbed oxygen or water from the environment which can result in a decrease in TFT performance[7]. The architecture of the etch stopper is shown in Figure 2.12.

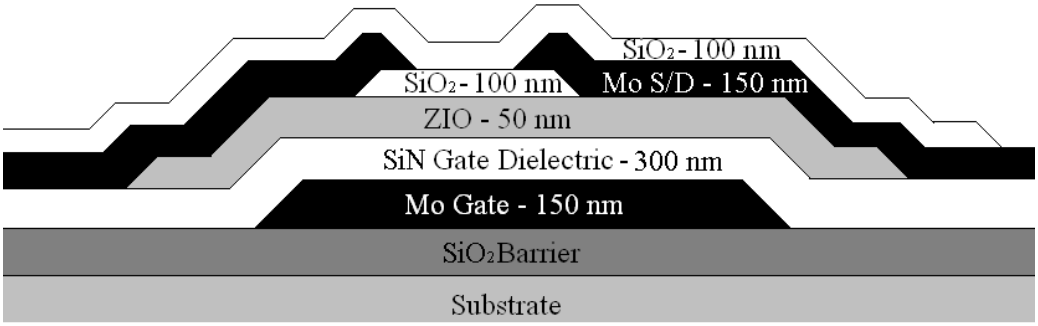

Figure 2.12: Schematic of the device architecture including an etch stopper structure

In this process flow, the gate dielectric, the ZIO active layer and the channel passivation layer or "etch stopper" layer are deposited sequentially as described in the prior section. However, the etch stopper layer is patterned first using the SiO_2 dry etch process. A separate photolithographic mask is subsequently used to pattern the ZIO active layer, which is etched with the buffered HF solution. This patterning scheme eliminates the undercut issue as evidenced by improvement in the device yield to nearly 80 %. Additionally, the median I_{off} for the devices is reduced to 0.59 pA/(W/L). However, the drive performance decays with this structure with the median V_T increasing to 3.66 V, the median μ_{sat} decreasing to 1.09 cm^2/V-s, while the subthreshold is 2.09 V/decade, and the I_{on} is 3.1 μA/(W/L). The decreased drive performance can be attributed to exposure of the ZIO active layer during the etch stopper etch and the oxygen plasma ash processes. In particular, the oxygen plasma ash can inject oxygen into the ZIO, which fills oxygen vacancies to decrease the carrier concentration.

2.3.4.3 Dry Etch

The previous results demonstrate the sensitivity of the ZIO active layer to processing. Therefore, protection of the active layer with adequate passivation prior to further processing is desired, but this approach requires concurrent patterning of the channel passivation and the ZIO active layer. However, this scheme yields unfavorable results when using the standard wet etches.

Greater control over the etch selectivity and sidewall morphology can be achieved using a dry etch. For an etch at 10 mTorr with the RF power set to 1000 W (0.314 W/cm^2, 414 V DC self bias) and a gas feed consisting of 10 sccm of O_2, 100 sccm of HCl, and 20 sccm of CH_4, an etch rate of 4.8 ± 0.7 nm/min for the ZIO is achieved with a selectivity to SiO_2 of 1.49, a selectivity to SiN of 1.67, and a selectivity to photoresist of 0.1. The low selectivity to SiO_2 should act to prevent the etch process from undercutting the SiO_2 passivation layer as observed previously for both wet etch chemistries. Lithographic pattering of the blanket-coated ZIO wafers is performed to understand how the dry etch process impacts the sidewall morphology. Figure 2.13 illustrates a top view of the sidewall. The sidewall edge is more uniform than for the wet etch process shown in Figure 2.9. The total thickness of the active layer is approximately 50 nm, but the length of the sidewall is approximately 150 nm indicative of a sidewall slope of ~ 20º. Moreover, the sidewall is smoother than the choppy sidewall obtained from the wet etch (Figure 2.9); this morphology should enable improved step coverage of subsequent depositions. Additionally, no residual material can be observed in the field (right side of Fig. 2.13), which indicates a complete etch of the ZIO.

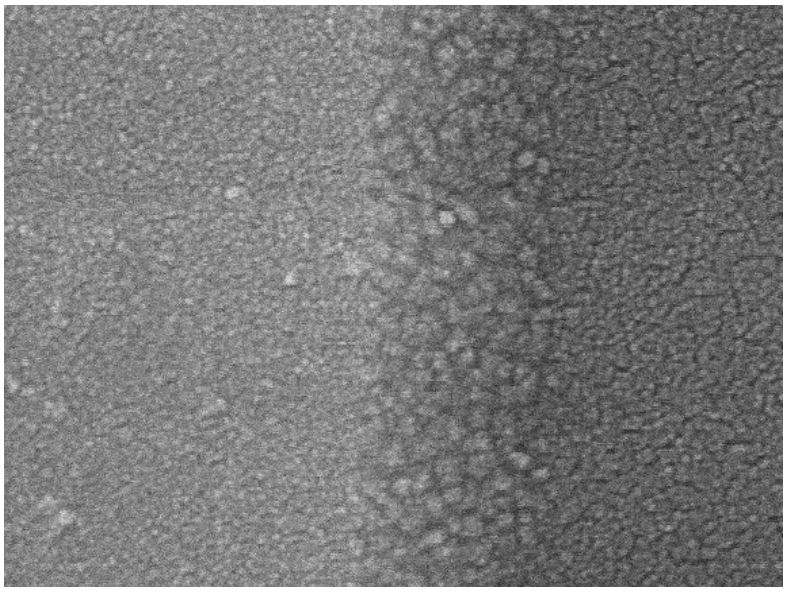

Figure 2.13: Micrograph of the dry etched ZIO sidewall. The sample was gold flashed prior to viewing in the FESEM.

To further evaluate the dry etch process, devices are fabricated using the structure presented in Figure 2.1. Figure 2.14 illustrates a typical etch profile of device using the ZIO dry etch and the step coverage of the subsequent depositions. The sidewall angle is approximately 24^{o} from the horizontal and can easily be covered by the subsequent line of sight thin film depositions. There is no indication of a step coverage issue that was present with the wet etch.

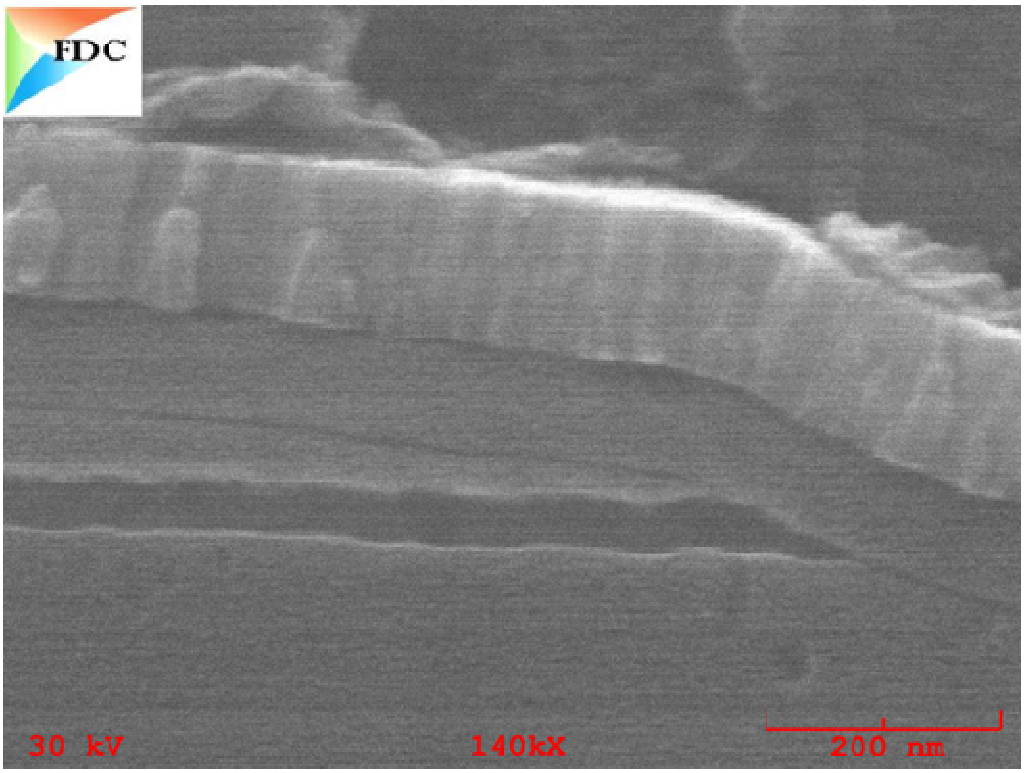

Figure 2.14: Typical ZIO dry etch profile with subsequent layer deposition.

As the structure appears to be improved relative to the wet etch, the TFT device performance is also investigated to confirm the improvement. Devices fabricated with the dry etch process exhibit a median source to drain leakage of 0.56 pA (52 fA/(W/L)), which is approximately 3 orders of magnitude lower than the original wet etch. Of the 80 devices tested, I_{off} is not larger than 4.2 pA (0.4 pA/(W/L)) for any single device. Moreover, the drive performance is comparable to the wet etch structure as I_{on} was 8.2 ± 2.0 μA/(W/L), the mean μ_{sat} was 6.42 ± 1.12 cm^2/V-s, the V_T was 4.85 ± 0.65 V, and the SS was 1.04 ± 0.08 V/dec. Table 2.2 summarizes the differences in performance obtained from the wet and dry etch when using the inverted staggered device structure.

Table 2.2: Comparison of wet and dry etch TFT mean parametric performance with the inverted staggered structure

	Wet (HF and HCl/HNO_3)	Dry
V_T (V)	-3.42 (1.47)	4.85 (0.65)
μ_{sat} (cm^2/V-s)	6.57 (0.73)	6.42 (1.12)
SS (V/decade)	2.41 (1.01)	1.04 (0.08)
I_{on} (μA/(W/L)	35.3 (3.2)	8.2 (2.0)
Median I_{off} (pA/(W/L)	61.2	0.052

The results indicate a significant decrease in the I_{off} and SS with limited degradation in the drive performance when using a dry etch. The significant improvement in the yield is predominately attributed to the improved sidewall profile of the dry etch, which prevents high I_{off} (shorting). However, the dry etch process increases the V_T, which could however be corrected by tuning of the active layer deposition processes. Nonetheless, a positive V_T is typically more desirable than a negative V_T as the device needs to be "off" when the voltage is zero.

A dry etch of ZIO leads to better performance than a wet etch due to improvements in etch selectivity and full passivation of the active layer during processing. The wet etch processes exhibits a large selectivity to ZIO over SiO_2 and SiN dielectric layers. To overcome this selectivity issue, separate patterning of the passivation and the active layer can be utilized in an etch stopper type device layout, but then the ZIO is exposed to other processes without passivation. A dry etch minimizes the etch selectivity between ZIO and the dielectric and

provides improved sidewall profile control and accordingly step coverage of the subsequent depositions. The SS and V_T are higher than desirable for the dry etch, but the etch is consistently reproducible with high device yield. The yield improved from 28 % to 100 % by using the dry etch in place of the wet etch. Future work will focus on improving the V_T and SS by optimizing the gate dielectric and active layer deposition processes. The dry etch provides a route to a consistent etch process for the active layer and enables future process optimization for ZIO-based devices.

2.3.5 Source/Drain Metallurgy

The 96 × 9 µm TFTs were characterized and analyzed for this experiment. The control cell featured 150 nm of molybdenum as the source/drain metal. The cell featuring the ITO source/drain metal demonstrated the statistically lowest mobility (7.82 cm^2/V-s) and lowest drive current (405 µA). The decreased drive current is attributed to the line resistance of the ITO. The sheet resistance of ITO at 50 nm thick is 80 Ω/□ and there are roughly 40 squares between the TFT and the prober pads resulting in a significant voltage drop. Therefore, the actual applied drain voltage was likely much lower than the output drain voltage.

The cell featuring tantalum was not expected to perform well because tantalum forms an insulating oxide much like aluminum. However, the mean drive current (417 µA) and saturation mobility (10.3 cm^2/V-s) were comparable, but statistically poorer than the control cell (546 µA and 12.6 cm^2/V-s). The median saturation mobility was much closer to the control cell (12.4 cm^2/V-s

versus 12.5 cm^2/V-s for the control cell) indicating that there may have been a few devices skewing the mean performance.

Approximately 12 out of the 60 devices tested from the Ta/Al cell feature a drive current that is less that 10 µA. These poor performing devices typically demonstrate a non-zero intercept in the output characteristics as shown in Figure 2.15 which is an indication of current crowding and the presence of a significant barrier between the source and drain. The barrier is likely tantalum oxide, which is a dielectric.

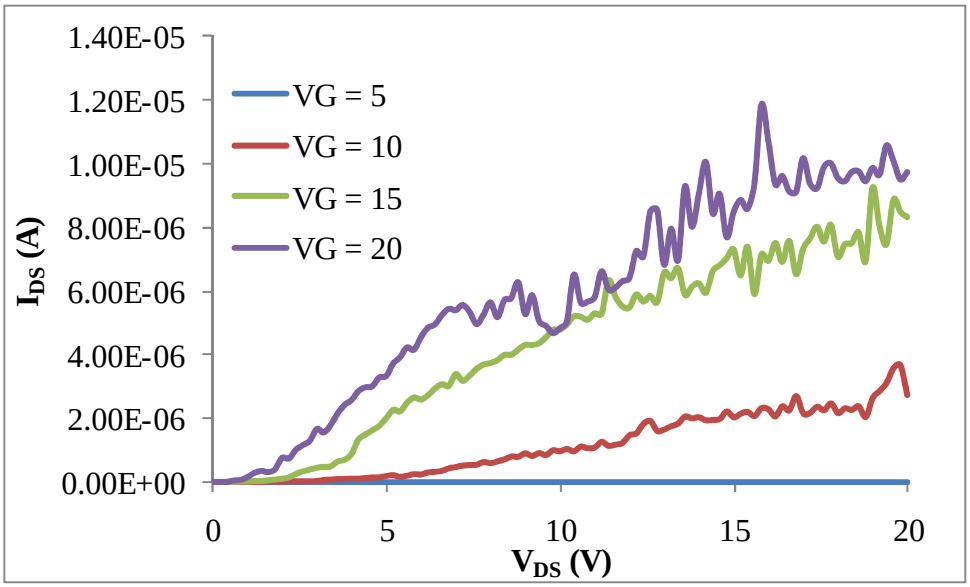

Figure 2.15: Output characteristics of a device with Ta/Al source/drain metal demonstrating current crowding at low VDS.

The cell featuring the Al/Mo bilayer demonstrated statistically improved drive current (598 µA) and saturation mobility (14.3 cm^2/V-s) over the control cell. In addition, the median source to drain leakage was two orders of magnitude

(1.6 fA versus 269 fA for the control cell) lower. The reduction in leakage is attributed to the oxidation of the aluminum source/drain layer. The source/drain layer in this experiment is exposed to the atmosphere because processing was stopped immediately after source/drain etching. The control cell features molybdenum which forms a weakly conducting oxide. The test setup is outside of the cleanroom so contamination may have been attracted to the exposed conductive molybdenum oxide during test operations. The Al/Mo bilayer devices may have been protected by the formation of an insulating native oxide on the aluminum. The results indicate that the Al/Mo bilayer is adequate for the source/drain material.

2.3.6 Interlayer Dielectric (ILD)

Initially, 500 nm SiN was used as the ILD layer. However, the PECVD grown SiN is conformal and does not planarize topology. In addition, electrophoretic displays fabricated with 500 nm of SiN demonstrated evidence of cross talk (Figure 2.16a). Thicker depositions of SiN were not considered reliable because of the stress of the film. In addition, the SiN does not address the need for planarity as OLED displays fabricated on topology demonstrate luminance variations (Figure 2.16b)

The poor visual appearance of displays fabricated with SiN ILD resulted in a search for a new material to serve as the ILD. Spin on glass (SOG) materials have been gaining in interest because of their low dielectric constant (3.0) and planarizing ability[21]. Most SOG's are applied in liquid form and are cured by

applying thermal energy. In most cases, the temperature of the cure is in excess of 400 ºC which far exceeds the melting temperature of most polymer substrates. However, a spin on glass material from Honeywell (trade name PTS-R) was found to have a cure temperature of 200 °C at a thickness of 2 µm. The material was ordered and incorporated into the TFT process flow. The low dielectric constant of the PTS-R significantly reduced the crosstalk in electrophoretic displays (Figure 2.16c) and its ability to planarize improved intrapixel luminance uniformity (Figure 2.16d).

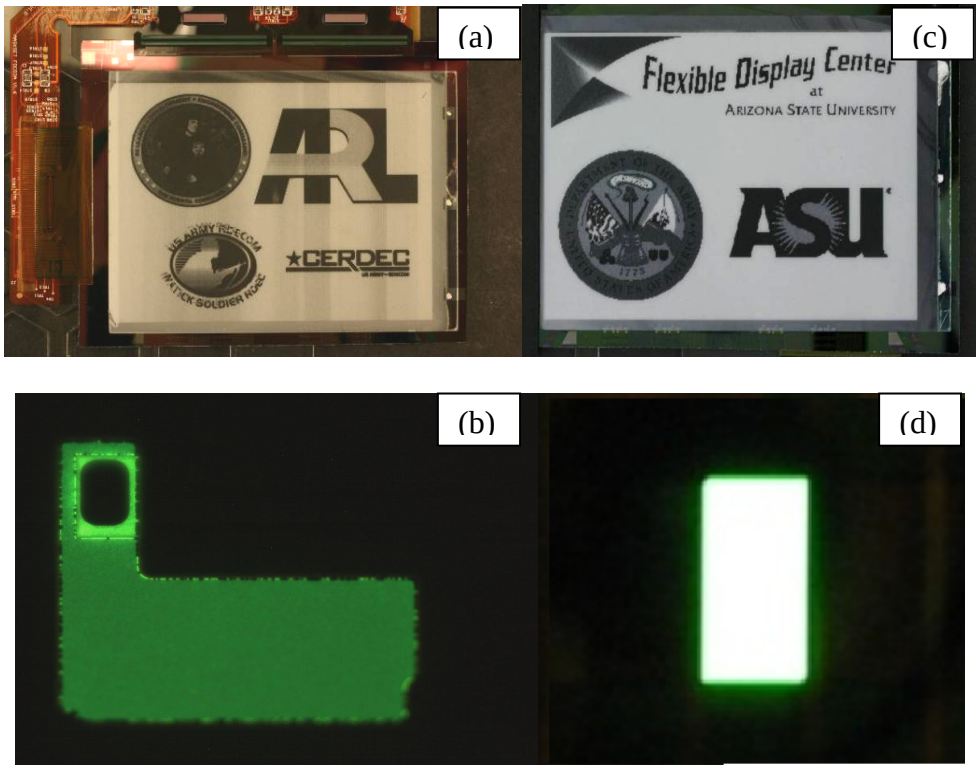

Figure 2.16: Electrophoretic display with SiN non planarizing ILD (a) and with PTS-R (b) and OLED pixel fabricated with SiN ILD (c) and with PTS-R (d)

The ILD is etched in a Tegal 901 reactive ion etcher (RIE) with the process pressure set to 400 mTorr, the power set to 200 W, the SF_6 flow set to 10 sccm and the O_2 flow set to 20 sccm. The O_2/SF_6 ratio is a main factor in determining the etch rate of the PTS-R and the photoresist. The flow ratio was adjusted to achieve a 1:1 selectivity between the PTS-R and the photoresist yielding a sidewall slope of approximately 35º from the horizontal. The shallow slope allows for adequate step coverage of the relatively thin anode layers (Figure 2.17). The resist is stripped by oxygen plasma etching in the Tegal 901 at a substrate temperature of 45 °C or by wet stripping in a bath of Baker's PRS 3000 solvent strip at 60 °C, followed by an intermediate rinse in room temperature 100 % isopropanol, QDR, and SRD. Either process is considered statistically equivalent. The low temperature Tegal 901 was chosen over the more conventional Gasonics L3510 microwave downstream asher and Tegal 965 barrel asher due to issues with cracking in the PTS-R under the higher temperature conditions of the Tegal 965 and Gasonics L3510. It was determined that the substrate temperature had to remain below 120 °C to prevent the PTS-R from cracking.

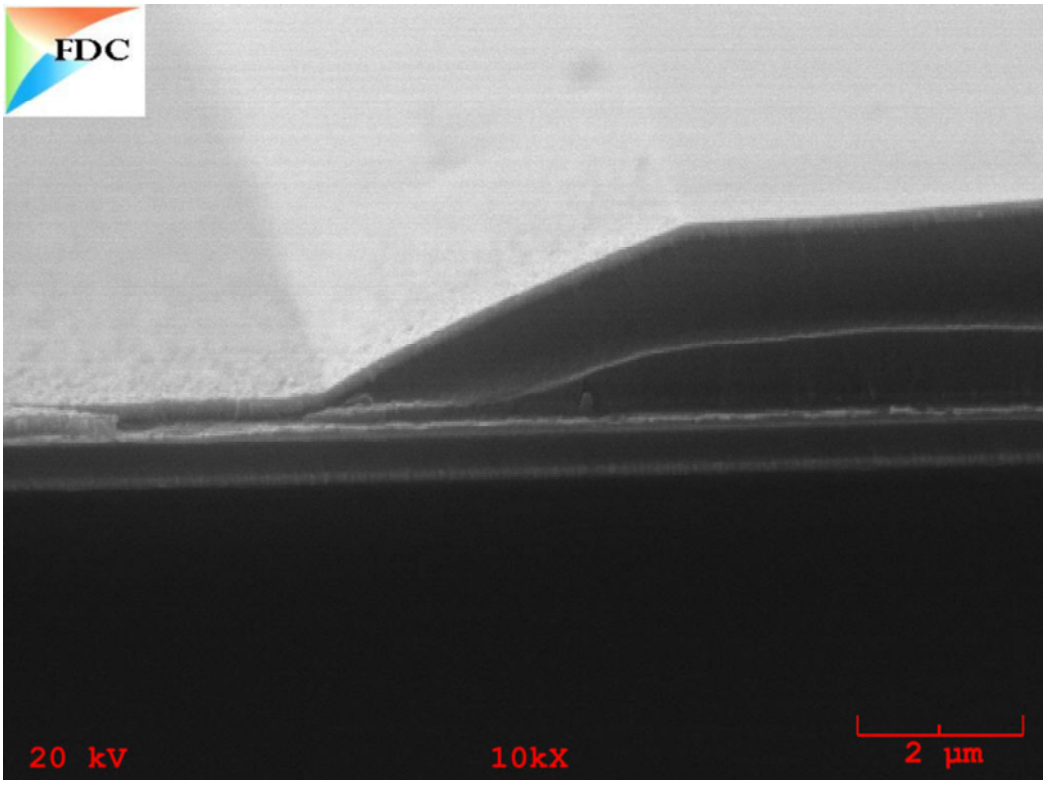

Figure 2.17: SEM micrograph demonstrating sloped ILD etch

It is difficult to verify the via integrity through inspections in the FESEM. Therefore, an electrical test was developed for testing individual pixels in completed backplanes. The test relies on the continuity of the anode materials from the probe contact to the contact with the source of the pixel TFT. A schematic of the test setup for an OLED array is shown in Figure 2.18.

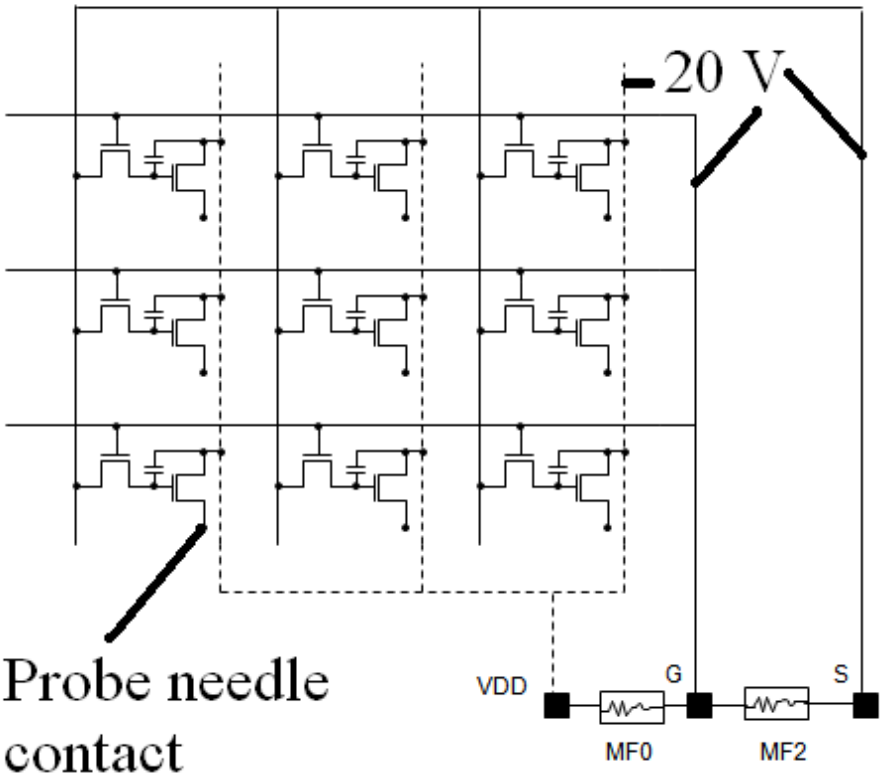

Figure 2.18: Array test circuit

A grounded probe needle contacts every pixel at the source of the drive TFT while power is applied to the VDD, gate (G), and source (S) terminals. A "low" current value indicates that there is either an issue with one of the TFTs or a discontinuity in the via. A QVGA array has 76800 pixels, so a lot of data can be collected quickly and a visual map of the array can be generated. In these visual maps, a white pixel indicates a short in a severe case or a "hot" pixel (high current) in a less-severe case, and a black pixel represents an open circuit in a severe case or a "cold" pixel in a less-severe case. A high-yield high quality array would show a map of a nearly even "deep blue sea." A typical, high-yield array map is shown in Figure 2.19.

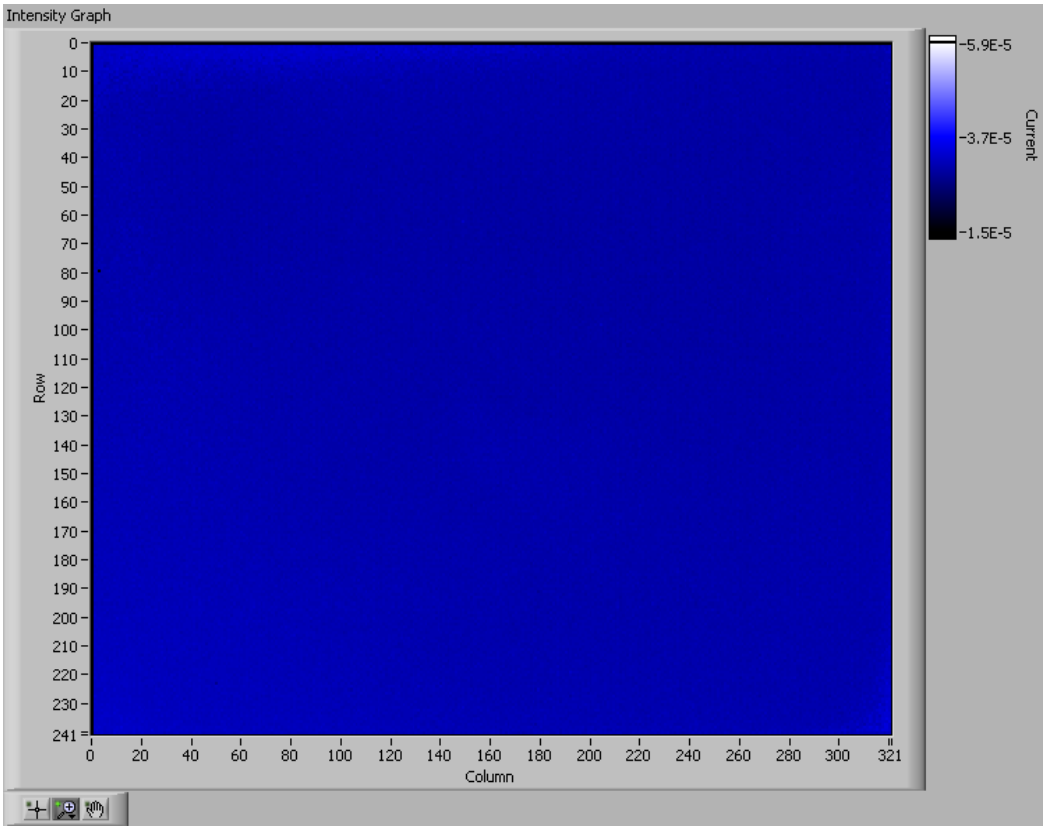

Figure 2.19: Array current map demonstrating good yield

Poor yield was initially observed when SiN was used as the ILD wetting and capping layer. Occasionally, arrays would demonstrate large “dark” spots in the array map that were indicative of either an issue with the TFT or a discontinuity in the via. An example of a defective array map with “dark” spots is shown in Figure 2.20.

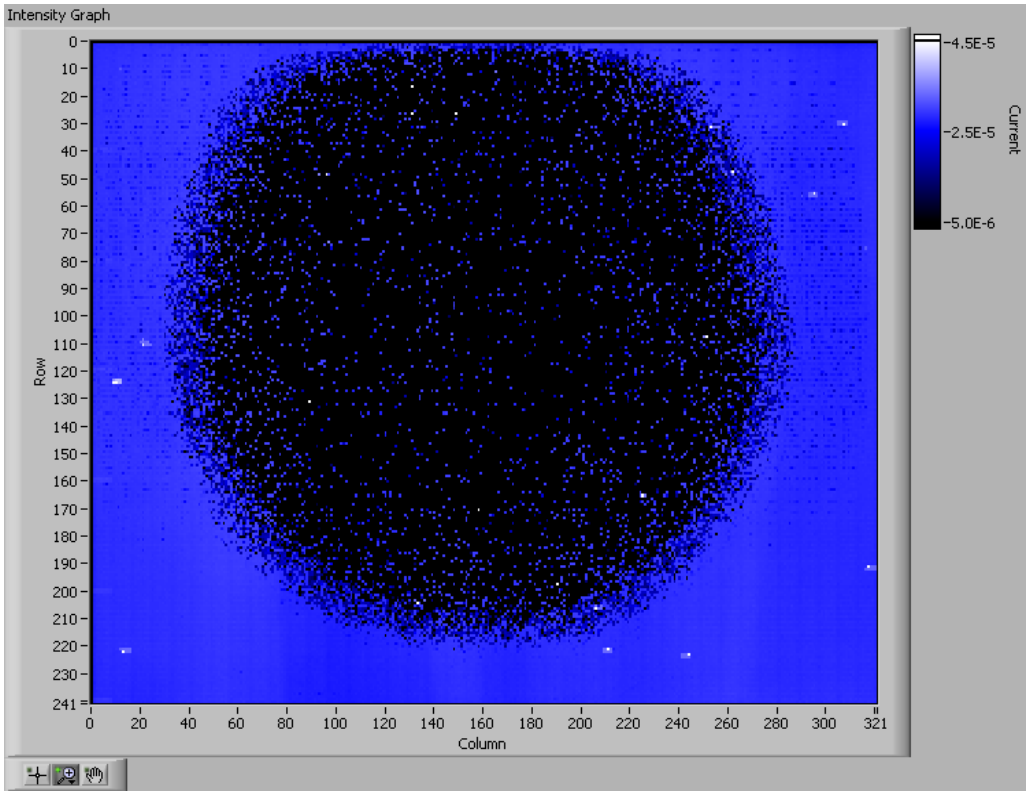

Figure 2.20: Array map demonstrating poor yield

A FESEM analysis of the defective area indicated poor step coverage by the subsequent metal deposition due to a reentrant profile of the SiN wetting and capping layers. The SiN was etching laterally faster than the photoresist or the PTS-R yielding an undercut profile at the top and bottom of the via. An example demonstrating an undercut with poor step coverage is shown in Figure 2.21.

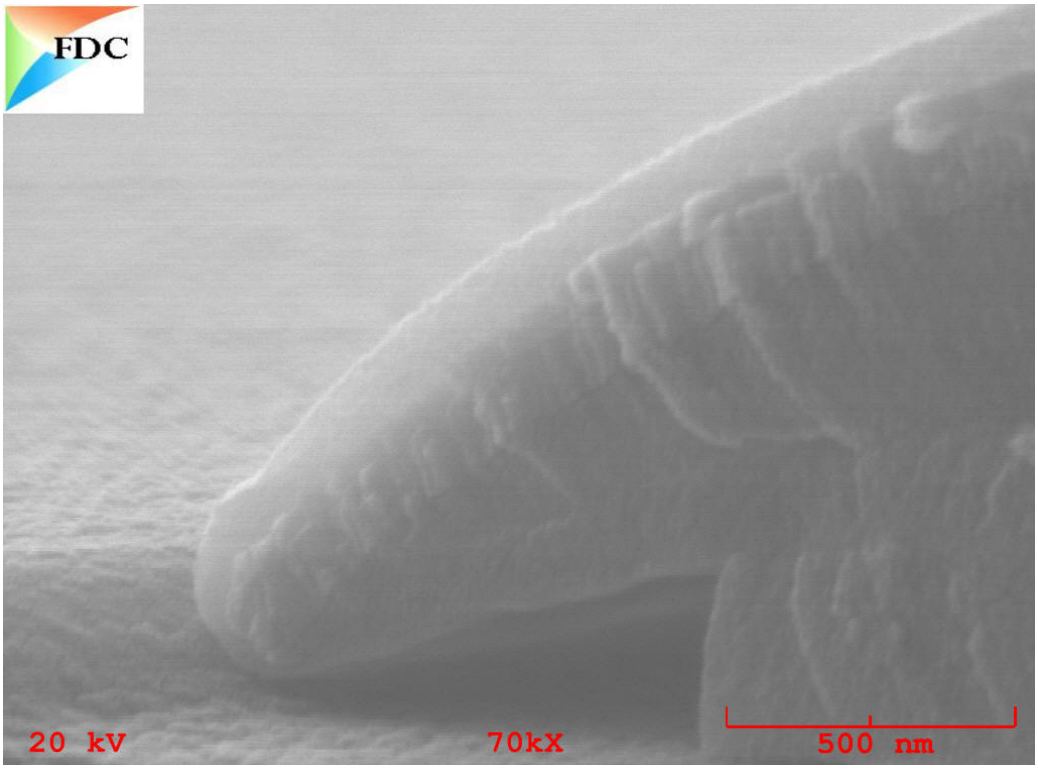

Figure 2.21: Undercutting of the SiN wetting layer and demonstration of step coverage issues for subsequent depositions.

The issue was resolved by switching to SiO_2, which etches at approximately one-half the etch rate of the PTS-R and the photoresist. The lateral etch rate of the SiO_2 is low enough that a reasonable etch profile is obtained.

2.3.7 Stress Testing

The threshold voltage shift at various DC bias conditions was compared with amorphous silicon. As seen in Figure 2.22, the change in threshold voltage is comparable to amorphous silicon for the negative DC bias stress conditions, with the threshold voltage changing by as much as –2.2 V. However, for positive DC bias stress, the threshold voltage shifts between 0.2 – 1.3 V after 10 000 s of

stress, which is significantly less than the shift observed in amorphous silicon TFTs. The standard deviation for the voltage shift at 10 000 s is typically between 0.3-1.0 V depending on the bias condition.

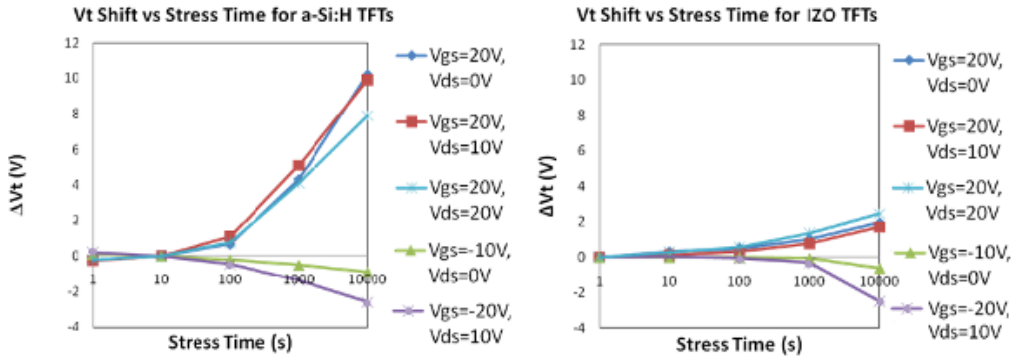

Figure 2.22: Comparison of threshold voltage degradation of a-Si:H and ZIO TFTs

The improved DC stress stability of ZIO in comparison to amorphous silicon is readily observable when examining the change in the output current of the drive transistor (T2) of the OLED pixel circuit as shown in Figure 2.23. As the current degrades, the luminance of the OLED will also degrade. One can see that the a-Si pixel current drops approximately 2.5 µA (37 %) after two hours of operation, while the drop in the ZIO pixel current is only 0.3 µA (3 %).

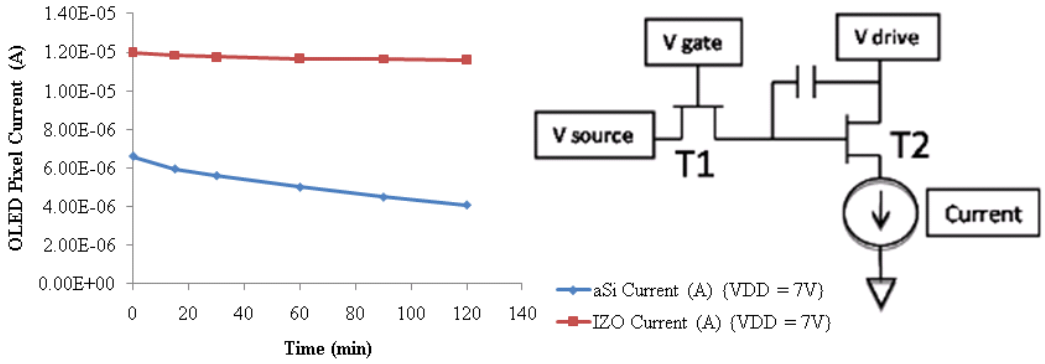

Figure 2.23: Test setup and results of constant voltage test

2.3.8 OLED Display Build

The OLED device structure has a median efficiency of 5.8 cd/A, and was developed by Xiaohui Yang at the FDC. The details of the OLED process are discussed elsewhere[32]. A fully built QVGA OLED display is shown in Figure 2.24.

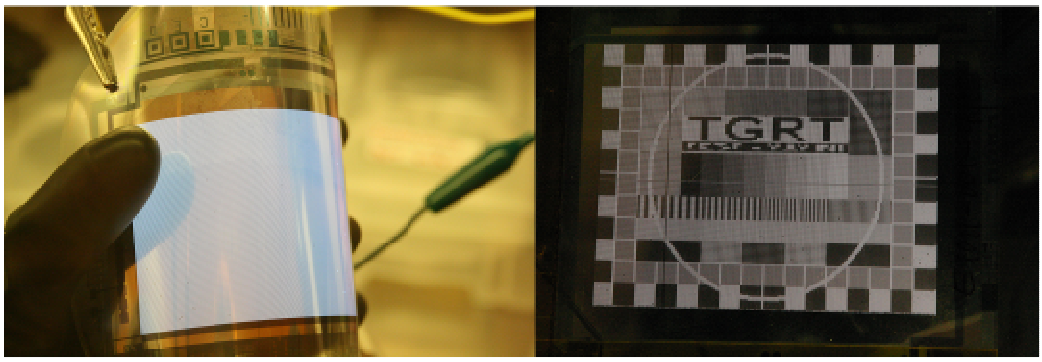

Figure 2.24: FDC's completed white active matrix OLED display with ZIO TFTs

The display resolution is a QVGA, which contains 320 columns of pixels and 240 rows of pixels, and is nominally 4.1" along its diagonal with an aperture ratio of 34.4 %, and a pixel density of 98.7 ppi. Each individual pixel consumes an area that is 67600 μm^2, and contains two transistors and one capacitor. The select transistor dimensions are 75 μm by 11 μm, while the drive transistors dimensions are 240 μm by 11 μm. The capacitor has a capacitance of 1.12 pF. The maximum luminance is 600 cd/m^2.

2.4 Conclusions

We have embarked on a critical path in flexible zinc indium oxide active-matrix backplane technology development that includes the following elements described in this chapter:

- Baseline low-temperature ZIO process development and improvement on a 6-inch pilot line to produce quality transistor arrays with reasonable yields
- Optimization and statistically-based improvement of ZIO drive performance
- Threshold voltage stability improvements over amorphous silicon
- Transition to processing on flexible plastic with current bond-debond process tools and materials
- Successful fabrication of white OLED displays with ZIO backplane technology

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CHAPTER 3

NEW ACTIVE LAYER DEPOSITION PROCESS BASED UPON DUAL-LAYER CONCEPT

3.1 Introduction

Critical properties in pixel circuit design include the threshold voltage and its shift due to voltage stress. The shift in threshold voltage will eventually result in incomplete turn-off or incomplete turn-on of the affected pixels depending on the direction of the shift. Stabilization of the threshold voltage for metal oxide semiconductors can be achieved through one or more high temperature (>300 ºC) post processing steps[1]. Unfortunately, these high temperature steps are incompatible with processing on flexible plastic substrates, such as polyethylene naphthalate (PEN). There is a substantial development effort in the display community to shift from glass to flexible plastic substrates that would provide a more rugged, thinner, and lightweight display backplane. PEN is compatible with much of the same cleaning chemistries as glass[2]. Moreover, PEN is an insulator like glass and thus avoids parasitic coupling capacitance that can affect devices fabricated on metal foils that could withstand the higher temperature post-processing. The colorless and highly transparent PEN material could provide an ideal substrate for low power, bottom emission, organic light emitting diode (OLED) displays.

In this chapter, the influences of composition and thickness of dual layer transparent oxide semiconductors on the performance of TFTs are systematically examined. The use of a dual layer architecture allows the independent control of

mobility and threshold voltage through compositional variations in the dual active layer. With proper tuning of the active layer compositions, the required device properties can be achieved without the use of a high temperature anneal, which is critical for the use of mixed metal oxides for flexible electronics and display applications.

3.2 Experiment

3.2.1 TFT Fabrication

To deposit the metal oxide layer, two different targets were utilized: 60 % zinc oxide and 40 % indium oxide (ZIO) by mass and 33.3 % indium oxide, 33.3 % gallium oxide, and 33.3 % zinc oxide (IGZO) by mass. So that we could directly compare our dual layer devices with previously-reported single layer devices, these sputter target compositions match the target compositions used by Itagaki[3] for ZIO and Lim[4] and Kwon[5] among others for IGZO.

The TFTs were fabricated with a bottom gate, inverted, staggered design. The transistors function as n-type devices in enhancement mode. The backplane TFT structure was similar to that previously described by Kaftanoglu et al.[6], except here the two active layers were IGZO/ZIO. This device architecture is illustrated in Figure 3.1.

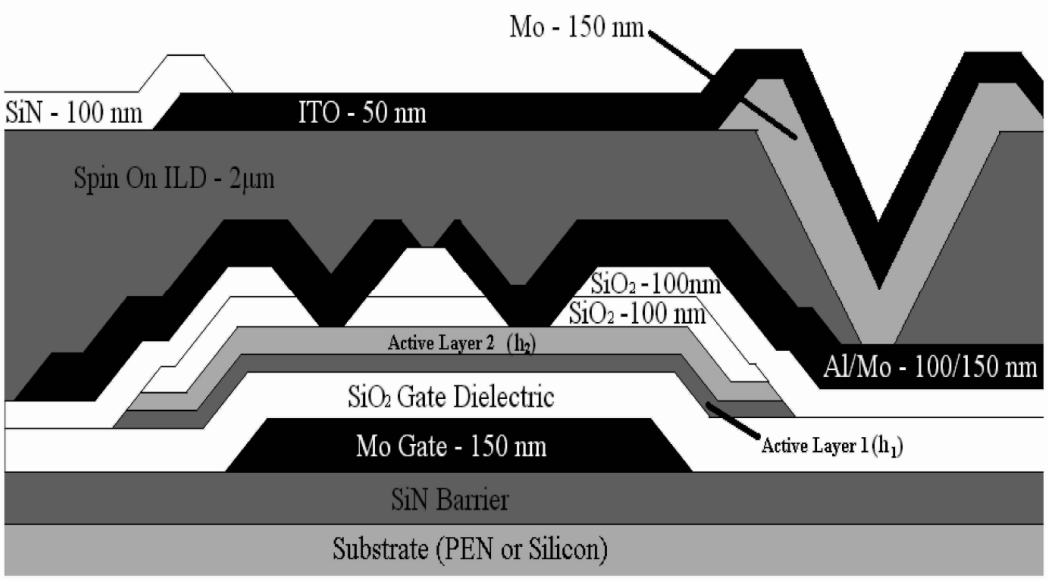

Figure 3.1: Schematic of the backplane pixel structure

The PEN substrate (125 µm thick) was obtained from DuPont Teijin Films (trade name Teonex Q65A) and was temporarily bonded to an alumina carrier (150 mm diameter, CoorsTek) for processing as described previously[7]. To rule out any potential substrate effects, TFTs were also fabricated on silicon substrates (150 mm) under identical process conditions and protocols as those used for PEN substrates; there were no statistical differences in the device performance between those fabricated on silicon or PEN. Devices were fabricated using the process steps described as follows. The substrates were cleaned in a PCT megasonic tank with a mixture of Alconox Detergent 8 (5 % by vol) and deionized water. A silicon nitride substrate barrier film was deposited by PECVD (AMAT P5000) followed by deposition of the molybdenum gate metal by DC sputtering (MRC 603). The gate dielectric (SiO_2, 20 nm thick) and passivation layers were all deposited by PECVD (AKT 1600 deposition system) at a process temperature of

180 ºC. The dual active layer was deposited using DC reactive sputtering (MRC 603 sputtering system) operating at 300 W at a pressure of 16 mTorr and a nominal substrate temperature of 40 °C. Active Layer 1, with thickness h_1, was the layer in contact with the gate dielectric and Active Layer 2, with thickness h_2, was the layer in contact with the source and drain. The cumulative thickness of active layers ($h_1 + h_2$) was maintained at 50 nm. The deposition of both active layers was always completed in situ without breaking vacuum to prevent atmospheric oxygen from altering the composition of the active layers in the interfacial region. A mixture of argon and oxygen (varied from 0 to 10 % oxygen) was used as the deposition feed gas. The molybdenum/aluminum source and drain were deposited by DC sputtering (MRC 603). The thick spin-on interlayer dielectric from Honeywell (trade name PTS-R) that encapsulates the TFT was cured at 200 °C for 1 h in a N_2 environment; this is the maximum temperature for the entire process. The pixel anode consisted of sputter deposited (KDF 744) molybdenum and indium tin oxide (10 % tin oxide by weight) layers. Each pixel was passivated by silicon nitride. Etching of the individual layers was completed using an AMAT 8330 dry etcher for the metal and active layer etching and a Tegal 901 parallel plate reactive ion etcher for all dielectric etching. AZ Materials 5214 photoresist was patterned using a Canon MPA-605 aligner for each photolithography step. The photoresist was stripped in a Gasonics L3510 downstream microwave plasma asher. All TFTs were fabricated with W/L = 10.5 and L = 9 μm.

For comparison purposes, single layer IGZO and ZIO TFTs were first

separately fabricated to establish the baseline electrical characteristics of each film as well as the dependence of the electrical performance on the active layer deposition process conditions. Dual active layers were then deposited with the same target material (either the IGZO or ZIO target) with process conditions altered after the completion of the first layer to generate a more resistive second layer (Active Layer 2) to prevent source to drain shorting. The thicknesses of the individual layers were varied, but the cumulative thickness was maintained at 50 nm. Dual active layers were also deposited with varying layer composition through sequential deposition using one sputter target and then the other. This experimental design enabled systematic investigation of the role of the dual active layer on the performance of metal oxide-based TFTs.

3.2.2 Test Setup

The TFT electrical performance was quantified using a probe station with a Keithley 4200 Semiconductor Characterization System (SCS). Transistor performance was measured for 10 individual test transistors distributed across the wafer. For each deposition condition, 12 wafers were processed and examined for a total of 120 devices tested per processing condition; this testing scheme provided a route to quantify intrawafer and wafer-to-wafer variations in device performance. For each TFT, the saturation mobility and the threshold voltage were extracted from the drain current (I_D) as a function of the gate voltage (V_G) transfer characteristics of the test transistors. This parameter extraction assumed

that the device was in saturation and that the saturation drain current can be expressed as

$$ID_{sat} = \mu_{sat} C_{ox} (W/(2L))(V_G - V_T)^2 \text{ when } V_G > V_T \quad (3.1)$$

where μ_{sat} is the saturation mobility; C_{ox} is the gate dielectric capacitance; (W/L) is the aspect ratio of the device; and V_T is the threshold voltage. Both the threshold voltage and saturation mobility were extracted graphically from the $\sqrt{I_D}$ versus V_G curve using the intercept and maximum slope, respectively. The performance of these parameters was also monitored with respect to electrical stress, where devices were stressed at either V_G = +20 V or V_G = -20 V with the drain voltage set to 0 V. The shift in the threshold voltage was determined after stressing for 10 min.

3.3 Results

3.3.1 Single Active Layer Devices

To provide a baseline comparison for the dual layer devices, electrical properties of analogous single component active layer devices are examined first. Figure 3.2 illustrates a representative transfer curve for a single layer transparent oxide-based transistor. Typically, both the saturation mobility and threshold voltage can readily be extracted from the transfer curve by a linear fit of the square root of the drain current as a function of the gate voltage. However in this case, there is non-ideal behavior in V_{GS} near the threshold voltage; a gradual rise in I_{DS} with increasing V_{GS} occurs instead of the textbook “hockey stick” curve.

This aberrant behavior in Figure 3.2 is likely related to the parasitic access resistance to the channel, which can be modeled as a barrier device in the source circuit. Nonetheless, it is possible to extract an “effective” saturation mobility and threshold voltage from this transfer curve to assess the performance of the device as a function of processing conditions. Statistically identical performance is obtained for devices fabricated on either PEN or silicon wafers.

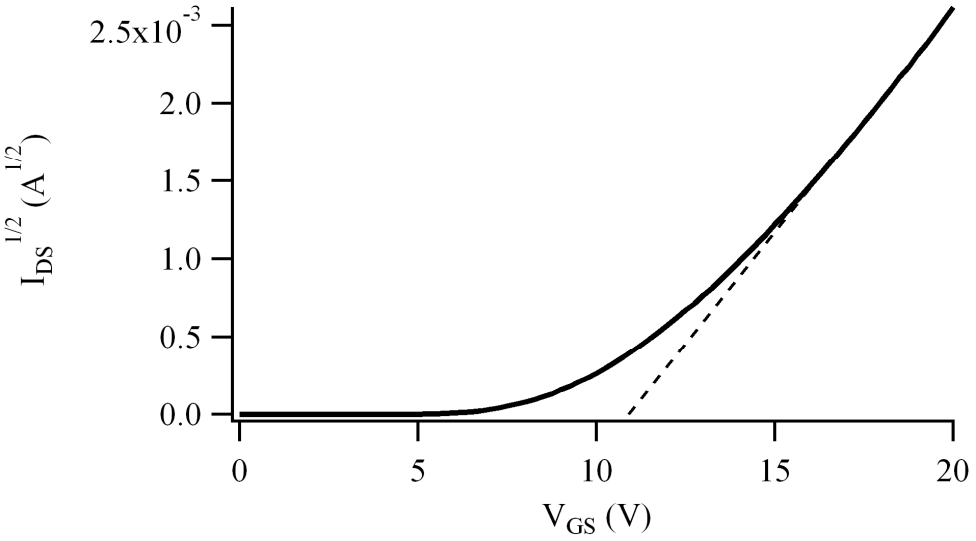

Figure 3.2: Representative transfer curve for a ZIO based transistor using a single layer channel. The dashed line is the best fit used to extract threshold voltage (11 V) and saturation mobility (2.1 cm^2/V-s).

Figure 3.3 shows how the oxygen concentration in the feed gas impacts the saturation mobility and threshold voltage for ZIO based transistors. For the range of conditions studied, a lower oxygen concentration in the feed gas leads to a desirable increase in the mobility and a decrease in threshold voltage. As the oxygen concentration in the feed gas is decreased it is likely that oxygen vacancy

concentration in the deposited active layer increases. With 0 % O_2 in the feed gas, the transfer curve for all devices has an appearance similar to the example shown in Figure 3.4, in which the devices exhibit a lack of appreciable modulation of the drain current by the gate voltage. Thus oxygen cannot be completely eliminated in the feed gas since the resultant devices will be constantly 'on' due to the low resistivity of the film. These results are consistent with previously reported oxygen feed gas dependencies reported by Wager and coworkers[8].

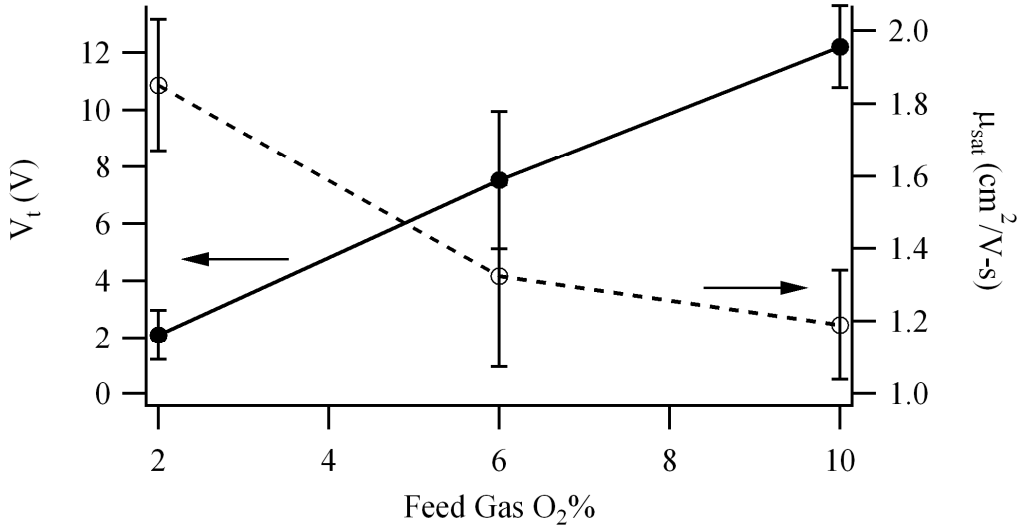

Figure 3.3: Impact of oxygen concentration in the feed gas during deposition of the active layer on threshold voltage (●) and saturation mobility (■) (W/L = 10.5)

3.3.2 Dual Active Layer Devices

Device performance can be improved by simply combining films with desirable features. For example, a film deposited with no oxygen in the feed gas with a resistivity of approximately 0.003 Ω-cm is too conductive for use as a single active layer and results in a short of the source to the drain (Figure 3.4).

However, this increased conductivity is desirable in the first layer of a dual layer stack. Such a structure allows for a higher density of carriers near the gate dielectric interface without shorting the device. For the second layer, a ZIO film featuring 2% oxygen concentration in the deposition feed gas would be resistive enough at 10 Ω-cm to reduce the source to drain leakage current to 10^{-13} A when the device is in the off state. All dual layer devices described in this article utilize 2 % oxygen concentration in the deposition feed gas for the second layer.

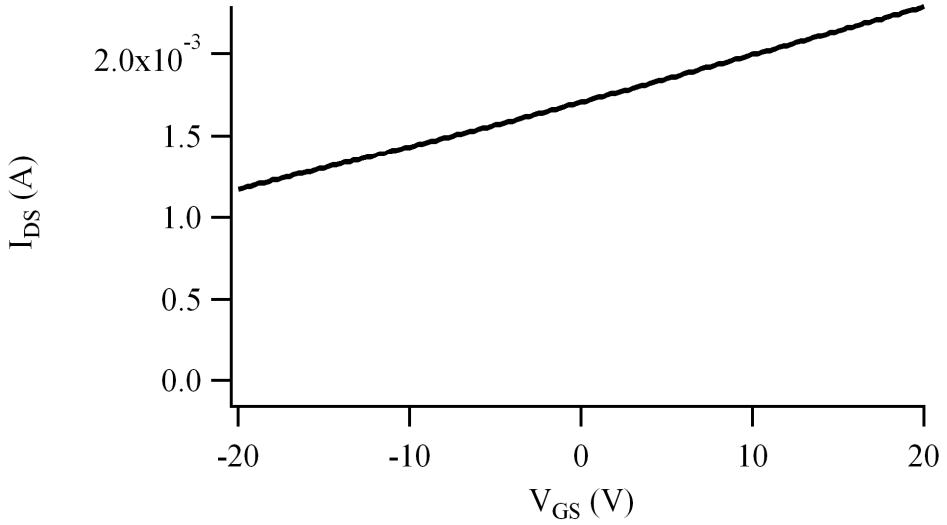

Figure 3.4: Transfer curve of device fabricated without O_2 in the feed gas. This device lacks the ability to significantly modulate the drain current with applied potential and is considered as a failed device.

This strategy was used to fabricate a series of dual layer devices; Figure 3.5 shows the threshold voltage (a), saturation mobility and on-off ratio (b) of the resultant dual layer stacks versus first active layer thickness h_1 with total thickness held constant at 50 nm. Note that the data points at $h_1 = 0$ represent the values for the respective single layer ZIO or IGZO devices. The dual layer devices exhibit

substantially higher saturation mobility and substantially reduced threshold voltage than the corresponding single layer devices. Greater performance improvements are observed for ZIO than for IGZO.

At h_1 = 10 nm for ZIO and h_1 = 20 nm for IGZO, the device yield is greater than 95 %. The typical failed devices do not turn off as demonstrated by the lack of adequate modulation of the drain current by the gate voltage (low on-off ratio) as shown in the example in Figure 3.4. As h_1 increases further beyond thicknesses reported in Figure 3.5, the fraction of devices that fail to turn off increases sharply and thus we have not reported their performance as the yield is unacceptable.

The improvement in the performance based on modulation in h_1 can be attributed to a decrease in the access resistance to the channel. The conductive channel, where the electrons flow from the source to the drain, is generally only a few nm thick[1]. In a top contact/bottom gate device, the current must transit an unmodulated region of the semiconductor between the contact and the induced channel. The resistivity of the first layer, at approximately 0.003 Ω-cm, decreases the overall resistivity of the semiconductor and thus reduces the access resistance for the device.

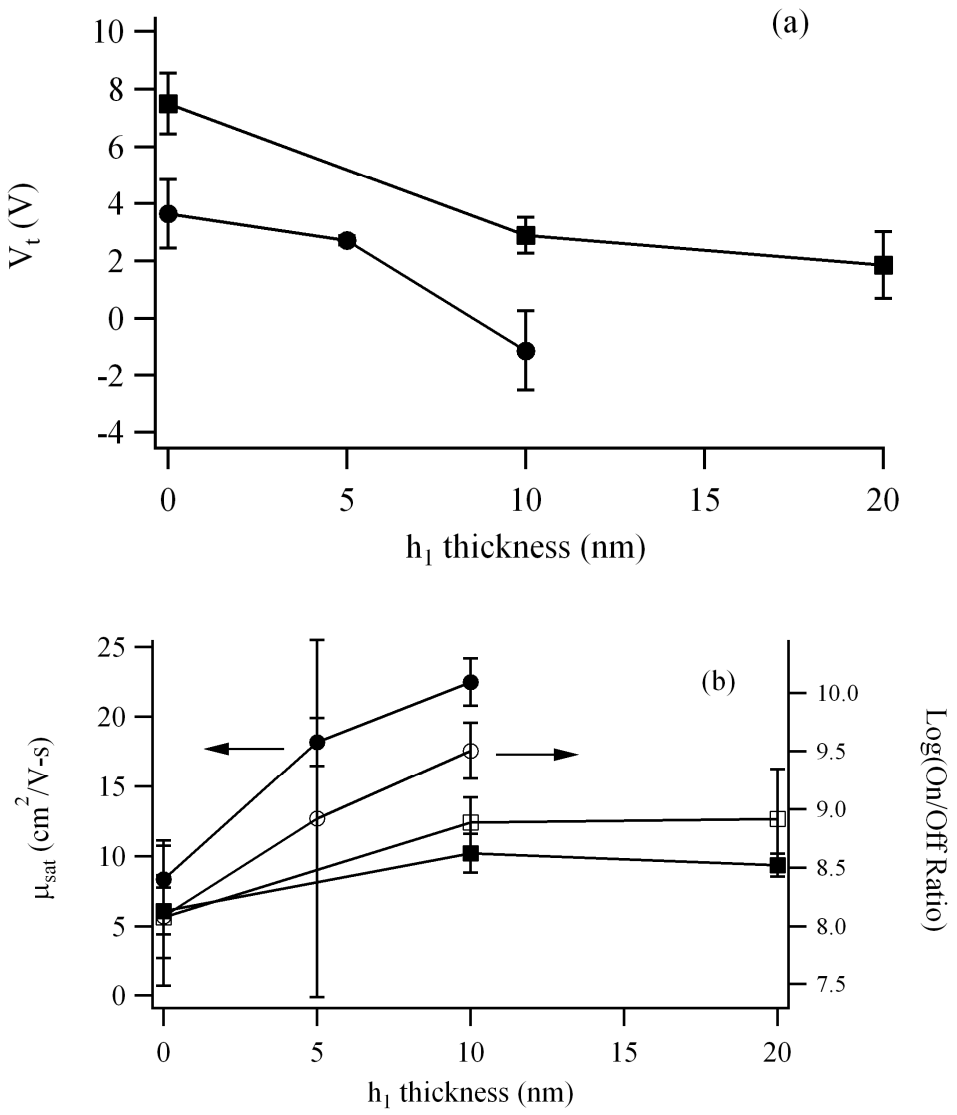

Figure 3.5: Impact of the thickness of the first active layer on (a) threshold voltage, (b) saturation mobility (closed symbols), and On/Off ratio (open symbols) for (●) ZIO and (■) IGZO devices. The cumulative thickness of the first and second layers is maintained at 50 nm in all cases.

In addition to the static performance difference, there is a change in the behavior of the devices under DC gate bias stress depending on h_1. The change in

the threshold voltage after 10 min of operation is compared in Figure 3.6 for various h_1.

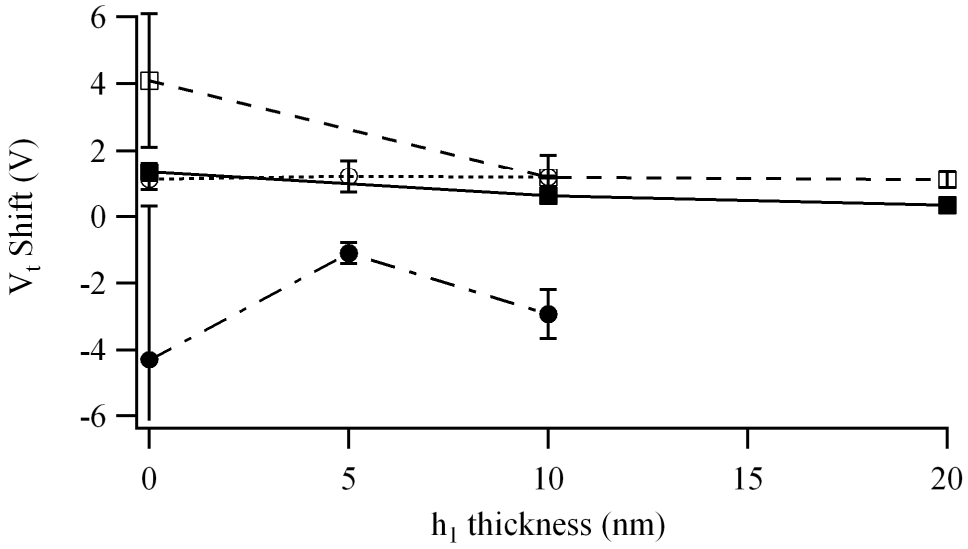

Figure 3.6: Impact of h_1 on the threshold voltage shift induced by stress condition for (●, ○) ZIO and (■, □) IGZO with V_{GS} = -20 V for 10 min (closed symbols) and +20 V for 10 min (open symbols).

The composition of the active layer and h_1 have little effect on the threshold voltage shift during positive gate bias stress as the shift is approximately 1 V in most cases. However, the threshold voltage shift due to negative bias stress is strongly dependent upon the composition of the active layer. ZIO based devices exhibit a negative shift in the threshold voltage, while devices fabricated with IGZO TFTs show a positive shift. In addition the threshold voltage shift for ZIO devices is strongly dependent on active layer 1 film thickness, whereas the shift for IGZO is less sensitive to layer 1 thickness. A large negative shift in the threshold voltage can lead to the TFT failing to turn off unless held at a negative

potential, which is not practical for TFTs in operation. Conversely, the devices exhibiting a positive threshold voltage shift will require an increasing amount of voltage to turn on until the threshold voltage drifts beyond the capability of the electronics controlling the TFTs or exceeds the breakdown voltage of the gate dielectric. Moreover for OLED applications, the variation in threshold voltage will lead to instabilities in the brightness and difficulties in color control. Thus, minimization of the threshold voltage shift is desired. This shift in the threshold voltage is typically related to mobile ions (for example, hydrogen from the PECVD silicon nitride or silicon oxide dielectrics), trapping of carriers due to oxygen vacancies, the creation of the defect states near the gate dielectric interface or in the active layer bulk, or any combination thereof. With this background, it is possible to understand the mechanisms by which the threshold voltage shift is dependent upon the composition and h_1.

To understand the compositional impact of the difference in performance between ZIO and IGZO, the nature of the cation interaction with oxygen must be considered. Gallium bonds with oxygen are much tighter than analogous bonds between oxygen and indium or zinc; this difference will results in fewer generated oxygen vacancies for materials containing gallium. During reverse gate bias of the device, these vacancies can ionize and diffuse toward the gate. The net result is a negative shift in the threshold voltage over time when a negative gate bias is applied. As a result, the threshold voltage shift for IGZO under negative gate bias is less than that for ZIO (Figure 3.6). It is presently unclear why the threshold shift depends on h_1. As h_1 decreases, it appears that the parasitic access resistance

increases as evidenced by a transfer curve that is comparable to the extraction demonstrated in Figure 3.2. As the device is stressed, the access resistance drops due to the creation of oxygen vacancies and the threshold voltage extraction actually improves. The improving fit may exaggerate the perceived shift in the threshold voltage since the basis for parameter extraction is in effect different.

3.3.3 Mixed Active Layer Devices

To further explore the performance of dual layer devices, a series of TFTs were fabricated through sequential deposition of ZIO and IGZO with varying composition of the active layers. Device architectures were systematically fabricated in which h_1 consisted of an oxygen deficient layer from one target while h_2 consisted of a more resistive layer deposited using the other target. As for all devices previously examined, the sum of h_1 and h_2 was set to 50 nm. Four device architectures with such "mixed" active layers were tested as described in Table 3.1.

Figure 3.7 shows the dependence of threshold voltage, on/off ratio and saturation mobility on the device structure as listed in Table 3.1. The mean saturation mobility (9 cm^2/V-s) and on/off ratio ($6x10^8$) of devices d_1 and d_2, which were fabricated by first depositing IGZO (h_1) and subsequently ZIO (h_2) without breaking vacuum, are not statistically different from the saturation mobility and on/off ratio of devices that were fabricated with a dual layer of IGZO that were presented in Figure 3.5. The same is true of devices d_3 and d_4,

which were fabricated with ZIO as h_1 and IGZO as h_2 and feature a saturation mobility of 18 cm^2/V-s and on-off ratio of 2×10^9. This mobility and on/off current ratio are not statistically different from the dual layer ZIO-only devices presented in Figure 3.5. The results again show that the initial device performance is strongly dependent on the h_1 thickness and composition.

Table 3.1: Active layer thickness and composition of devices fabricated using both IGZO and ZIO.

Device	d_1	d_2	d_3	d_4
h_1 target	IGZO	IGZO	ZIO	ZIO
h_1 feed gas O_2%	0%	0%	0%	0%
h_1 thickness	10 nm	20 nm	5 nm	10 nm
h_2 target	ZIO	ZIO	IGZO	IGZO
h_2 feed gas O_2%	2%	2%	2%	2%
h_2 thickness	40 nm	30 nm	45 nm	40 nm

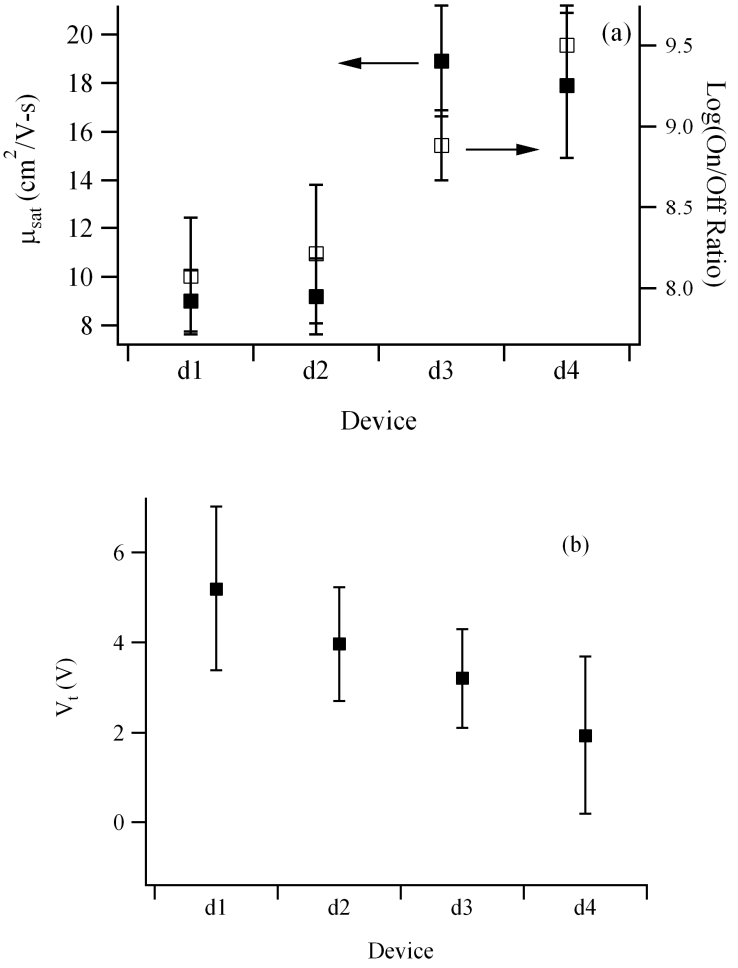

Figure 3.7: Initial saturation mobility, On/Off Current, (a) and threshold voltage (b) of devices described in Table 3.1.

The increased conductivity of h_1 also results in a much cleaner extraction of the threshold voltage as shown by a representative TFT in Figure 3.8a. The transfer characteristics of the same device are also included (Figure 3.8b). The improved fit of the transfer curve is likely attributable to the lower resistivity of the active layer and thus the lower access resistance to the channel.

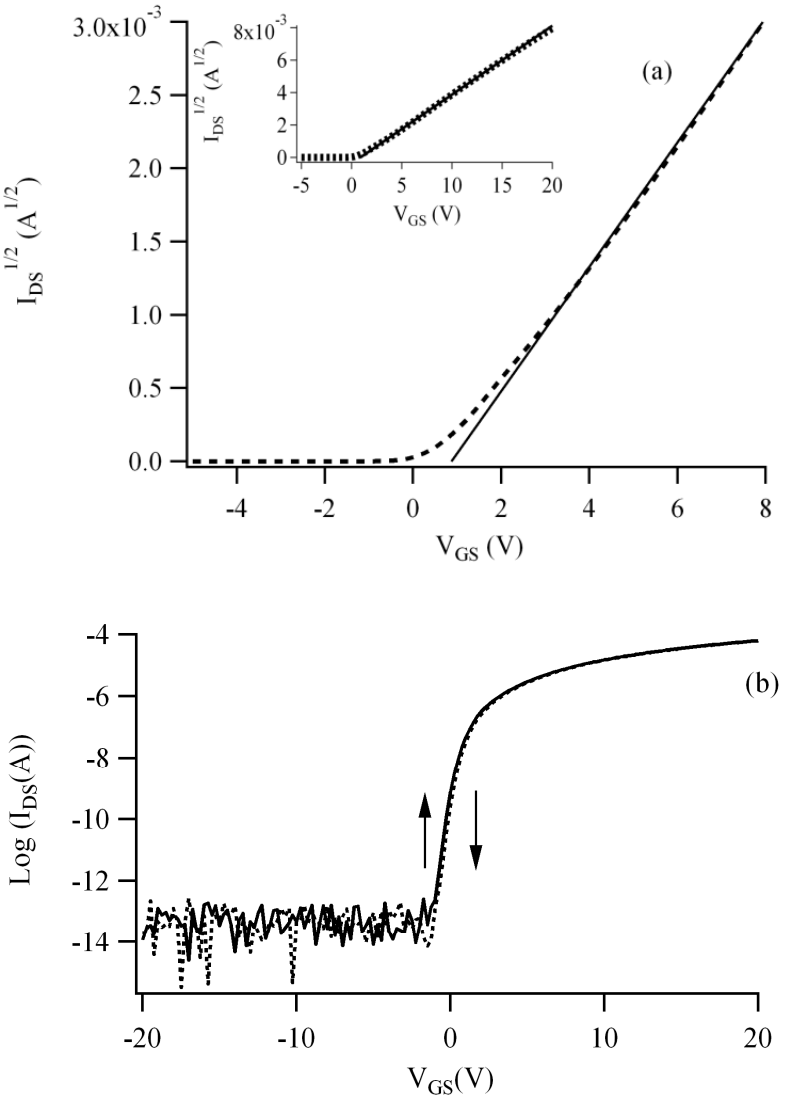

Figure 3.8: Threshold voltage extraction (a) and transfer characteristics (b) showing forward sweep (solid line) and reverse sweep (dashed line) of selected d_2 dual active layer TFT.

The average threshold voltage shift based on the device structures described in Table 3.1 is shown in Figure 3.9. Devices d_1 and d_2, which feature IGZO as h_1, show a small, but statistically significant negative shift in the threshold voltage. This behavior is in contrast to the behavior observed for the

dual IGZO active layer device shown in Figure 3.6. The same behavior is observed for devices d_3 and d_4 which feature ZIO as h_1. In both cases, it would appear that the threshold voltage shift due to negative gate bias stress is dependent on the composition of h_2.

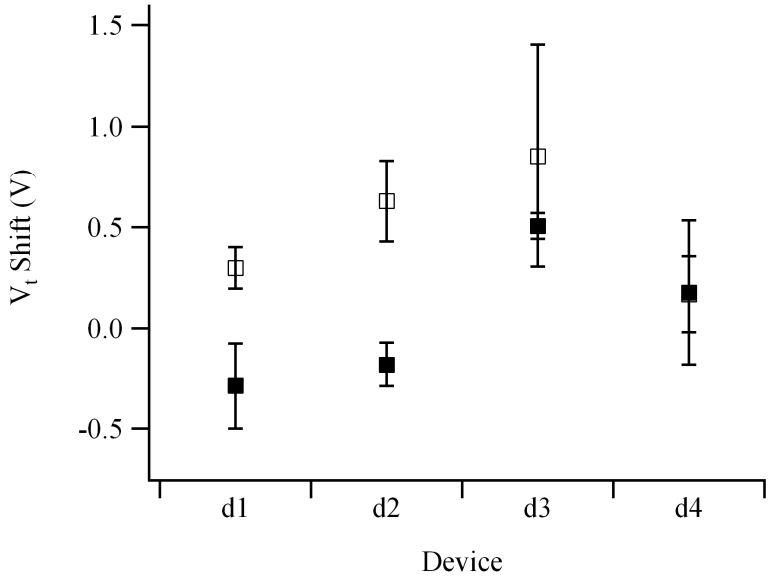

Figure 3.9: Threshold voltage shift versus device structure and stress condition with V_{GS} = -20 V for 20 minutes (closed symbols) and +20 V for 20 minutes (open symbols).

As the threshold voltage shift is predominantly dependent upon the composition of the second layer in the active stack, the source for oxygen vacancies (and ultimately the device instability) appears to be within or transported through this layer. If the vacancies are initially present when deposited, then it would be expected that turning off the transistors during the initial characterization of the device would be difficult. Thus, the vacancies are likely generated during operation. One potential source for such vacancies is

through reaction of the molybdenum source-drain metal with the oxide semiconductor to generate oxygen vacancies at the contact with the second layer h_2. Gallium bonds to oxygen are stronger than the analogous indium or zinc bonds to oxygen, therefore ZIO should be more susceptible to forming vacancies than IGZO. As Fig. 9 demonstrates, devices fabricated with ZIO as the second layer h_2 exhibit a negative shift in the threshold voltage under negative gate bias stress as one would expect if oxygen vacancies were being generated. Devices with IGZO as h_2 actually demonstrate a positive threshold voltage shift under negative gate bias stress, which suggests that oxygen vacancy generation is not the dominant defect generation process.

3.4 Conclusions

A novel device structure for high performance and improved stability TFTs has been developed that is based upon a dual active layer architecture. Devices with this dual active layer exhibit improved performance and stability under gate bias stress when compared to their single layer counterparts. The film properties of the first layer in contact with the gate dielectric are critical in determining the initial saturation mobility and threshold voltage, while the properties of the second layer in the active stack appear to control the threshold voltage stability. By judiciously selecting the components of the two active layers, it is possible to achieve both high performance and good stability that cannot be easily obtained with a single layer device without high temperature annealing. The procedures used in the fabrication of these devices are extendable to a

production process, in particular for manufacturing on flexible substrates where high temperature anneals are not possible.

3.5 References

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CHAPTER 4

CONCLUSIONS AND FUTURE WORK

4.1 Conclusions

Flexible OLED displays based on mixed oxide TFTs have been successfully fabricated on PEN substrates. These TFTs were processed at a maximum temperature of 200 °C and have a saturation mobility of up to 18 $cm^2/V\text{-}s$.

The second chapter established key processing breakthroughs in establishing a reasonable process baseline. Some of these notable process breakthroughs include the reduction of the gate etch sidewall angle, the establishment of SiO_2 gate dielectric of choice, the optimization of the active layer deposition by adjusting the process parameters, the selection of a dry etch process over a wet etch for improved step coverage of the active layer, exploration and selection of various source/drain metallurgy, establishment of a planarizing ILD process to enable high density top emission OLED displays, and migration of the process to flexible substrates.

The third chapter established a novel structure for high performance and improved stability TFTs based upon a dual active layer architecture. Devices with this dual active layer exhibit improved performance and stability under gate bias stress when compared to their single layer counterparts. The film properties of the first layer in contact with the gate dielectric are critical in determining the initial saturation mobility and threshold voltage, while the properties of the second layer in the active stack appear to control the threshold voltage stability. By judiciously

selecting the components of the two active layers, it is possible to achieve both high performance and good stability that cannot be easily obtained with a single layer device without high temperature annealing. The procedures used in the fabrication of these devices are extendable to a production process, in particular for manufacturing on flexible substrates where high temperature anneals are not possible.

4.2 Future Work

There is still much to research with respect to mixed oxide TFTs. Mixed oxide devices have shown instability with respect to irradiation in the visible green and lower wavelengths. The instability has been attributed to oxygen vacancy formation and has not been addressed in literature.

The mixed oxide deposition process is crucial to the performance of the TFT. Other techniques for depositing the mixed oxide could be explored including solution processing and RF sputtering.

Although rigid displays have been demonstrated at resolutions of up to 3840 × 2160 at a 70” diagonal, flexible displays have yet to be demonstrated above 4.0” along the diagonal at the FDC. Scaling the flexible mixed oxide TFT process to the FDC’s Gen II glass (370 × 470 mm) pilot line to enable larger diagonal demonstrations would represent a significant accomplishment.

4.2.1 Irradiation Bias Stability

One fundamental issue with mixed oxide semiconductors that has recently been discussed in the literature is the light stability of mixed oxide TFTs during operation[1,2,3]. The optical band gap of mixed oxide semiconductors typically falls between 3.0 and 3.3 eV, but can demonstrate absorption of light down to 2.6 eV (yellow) depending on the quality of the oxide film. When exposed to light, mixed oxide TFTs demonstrate a sizable negative shift in the threshold voltage that depends on the intensity and wavelength of the radiation. As the intensity increases and the wavelength decreases, the threshold voltage shift becomes increasingly negative. The decrease in the threshold voltage is attributed to the formation of oxygen vacancies in the active layer. An example for IGZO could be expressed by the following chemical reaction[3]:

$$\text{a-IGZO} \rightarrow \frac{1}{2}\mathrm{O}_2(g) \uparrow + \ddot{V}_O + 2e^- \tag{4.1}$$

This light instability is a major issue for displays which generate their own light (OLED) or allow light to pass through the display (LCD). Sensitivity to green and blue light would not be acceptable as the display would quickly fail.

A total of 28 IGZO devices fabricated using the dual layer process presented in Chapter 3 were subject to UV irradiation in a Dymax flood exposure unit with lamp intensity of 75 mW/cm^2 at primary lamp wavelength of 365 nm. Each group of 28 devices was subject to varying intervals (10s, 100s, 1000s, and 10000s) of irradiation under the UV lamp. The wafers were then tested using the probe setup described in Chapters 2 and 3 with approximately 10 minutes of delay

in between the irradiation and the TFT characterization. The results were tabulated and compared with the initial TFT measurements prior to any exposure. Figure 4.1 shows that saturation mobility increases and negative threshold voltage shifts increase with increasing UV exposure; these results are consistent with the literature.

The results presented by Yao[3], indicate that the original oxygen content in the film is a strong factor in determining the magnitude of the V_T shift. The reaction mechanism presented suggests that it may be possible to stress mixed oxide devices in process to improve the device performance as well as the UV light stress stability.

The effect of in process irradiation could be explored by exposing wafers to a specific dosage based on the results from Figure 4.1 at various steps in the process. For example, if oxygen vacancy generation is occurring as a result of UV irradiation, then it may be possible to boost the performance by exposing the wafers to UV irradiation after the deposition of the active layer but prior to the passivation deposition.

UV irradiation after the active layer deposition may generate too many vacancies, so the UV treatment should be applied between different steps after the active layer passivation has been deposited. The UV irradiation could be conveniently applied by a Dymax flood exposure unit.

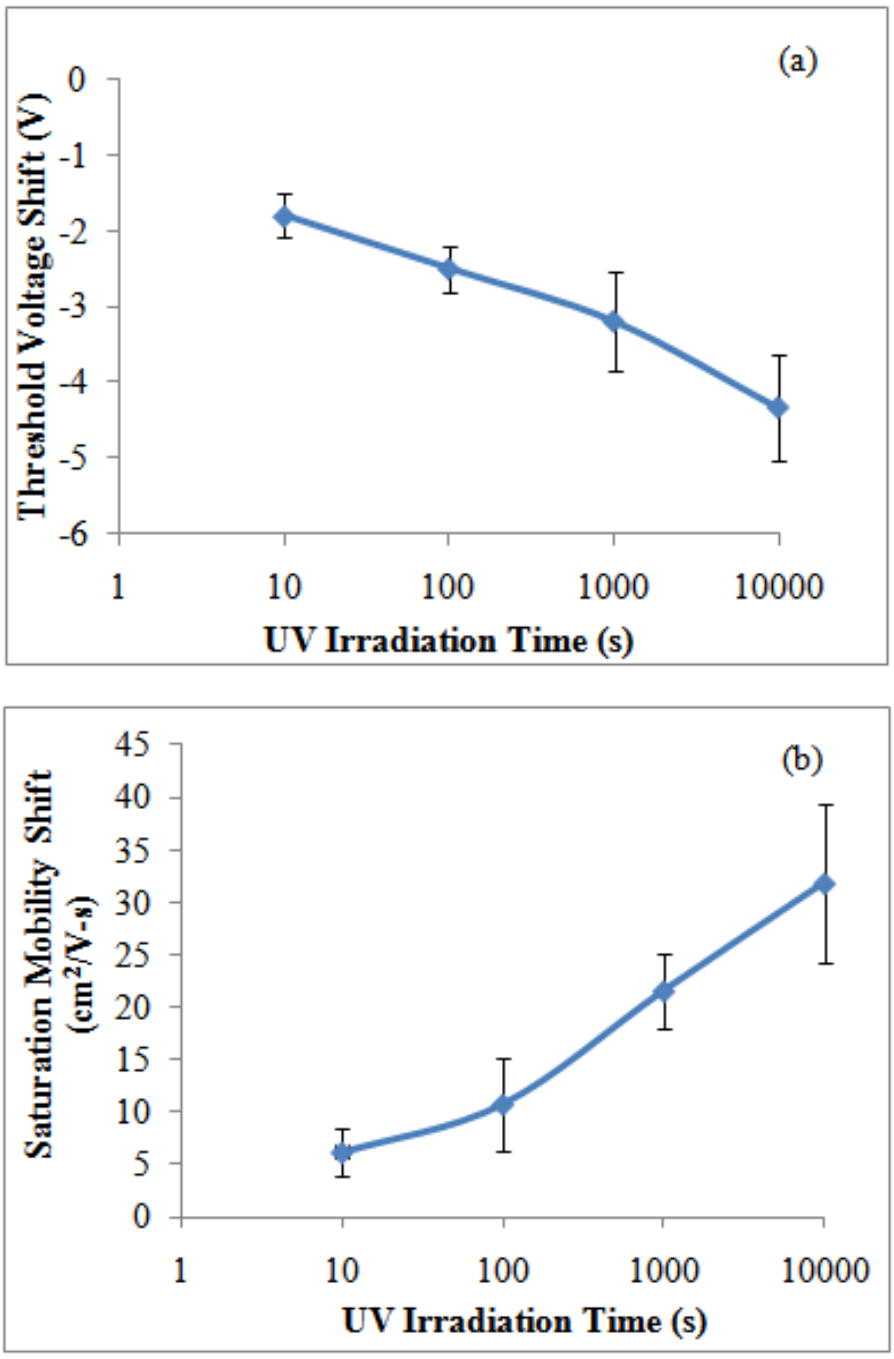

Figure 4.1: Threshold voltage shift (a) and saturation mobility shift (b) as a function of UV irradiation time.

It is also important to understand any potential recovery mechanisms if they exist. It would be an unfair comparison if only initial performance of the UV treated TFTs was compared with untreated TFTs. The potential gains of the UV treatment are not useful unless the gains are relatively permanent. Therefore the recovery time of the devices should be determined by storing UV treated wafers in the dark and recharacterizing the TFT performance at regular intervals. If the recovery process is slow (i.e. longer than 2-3 weeks), then it may be possible to accelerate the recovery by heating the devices. Since the primary defects created during UV exposure of mixed oxide semiconductors are oxygen vacancies, studying the recovery characteristics at different temperatures could allow for the extraction of the activation energy required to eliminate oxygen vacancies.

4.2.2 Solution Processed Mixed Oxides

Advances continue to be made in solution processing of mixed metal oxides. Solution processing has some advantages over traditional vacuum sputtering including process uniformity, control of the film composition, and lower cost of equipment, while disadvantages include generally high curing temperature, poorer device performance, and lower throughput[4,5,6,7,8].

Recent breakthroughs in solution processing have brought maximum processing temperatures down to 200 °C[6,7] for the active layer, but the TFT performance continues to lag behind conventionally sputtered mixed oxides. In addition, some groups claim low temperature processing for the active layer, but use a high temperature (350 °C) PECVD SiO_2 gate dielectric. As the temperature

of the cure increase over 450°C, a saturation mobility of 2.5 cm^2 /V-s is possible[8]. Solution processing may be a viable avenue for fabricating flexible displays and should be explored.

Precursor formulations are well-defined, so it would be easy to reproduce results first on silicon substrates due to the high curing temperature reported by most groups. Once a baseline has been established, incremental changes to the process could be made with the intent to reduce or eliminate the high temperature cure. For example, both spin and spray coating are available to coat the precursors. The different coating techniques may affect the final density of the film. Instead of using thermal annealing, it may be possible to cure the material using a plasma or UV light[9]. Doping the precursor material may also have an effect on the required cure temperature as well as the device performance. For example, Ahn, et al., demonstrated a factor of 5 improvement in the saturation mobility of spin cast tin doped zinc oxide quantum dot TFTs by adding $SnCl_2$ to the zinc oxide quantum dot suspension prior to spinning[10]. The optical properties of these films could be compared to sputtered deposited mixed oxide films during the initial characterization of the process. For process temperatures that are compatible with PEN substrates, TFTs can be fabricated on flexible substrates and compared with TFTs of conventionally deposited materials.

4.2.3 RF Sputtering

The work in the previous two chapters focused on DC sputtering in an MRC 603. RF sputtering is the more common approach with ceramic

targets[11,12,13,14]. However, no systematic study has demonstrated which deposition process is preferred. There are concerns that DC reactive sputtering can result in the poisoning of the target if the reaction rate is faster than the sputtering rate[15,16], which has been demonstrated for silicon oxide and silicon nitride films. Target poisoning could cause a gradual shift in the deposition of the mixed oxide material leading to gradual shift in performance.

The process presented in Chapter 3 utilizes a two step deposition process where the first step does not use oxygen. The target is lit before the wafers are in front of the target so it is possibly that the poisoned portion of the target is removed before the wafers are exposed to the process. In addition, the process has been in place for less than 6 months and the current IGZO target has been lit for approximately 10 hours. The expected end of life for this target is approximately 100 hours. Long term tracking of the TFT results will be necessary to determine if target poisoning is occurring.

A comparison between RF and DC sputtering can be achieved in Sunic SUNICEL Plus 400 vacuum deposition system available at the FDC. The sputter chambers in the system are set up to allow for DC or RF sputtering of the same target. An experiment could be set up where the gas flow, pressure, active layer thickness and target composition are the same. The deposition rate at same numerical power setting is expected to be different for DC versus RF applied power. Therefore, it will either be necessary to adjust the deposition time to match the thickness or the deposition power setting to adjust the rate. Both methods should be explored independently.

4.4 Process Scaling to Gen II Pilot Line

The work presented in the previous two chapters was completed on 150 mm substrates. The current state of the art in flexible mixed oxide displays is a 4" diagonal QVGA. Consumer demand will eventually push for larger flexible displays, so it will be necessary to demonstrate the scalability of the processes. Already, Samsung has demonstrated a 70" Ultra Definition (3840 × 2160, which is 4 times the current "HD" standard) display using mixed oxide technology (Figure 4.2) and conventional display glass, suggesting that the technology is capable of scaling to large sizes.

Figure 4.2: Samsung 70" UHD display using mixed oxide technology[17]

Scaling to the Gen II process line will require qualification of multiple new processes. The SiO_2 gate dielectric and passivation PECVD process were developed in the AKT 1600, which can handle Gen II substrates. However, all of

the other processes will need to be recharacterized, including the active layer deposition. Some of the expected challenges include: scaling the bond/debond process to Gen II substrates, controlling the uniformity of the active layer deposition, minimizing the stress of the films, and reducing defectivity to a level that is adequate to fabricate a larger display.

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