A DC-DC Multiport Converter Based

Solid State Transformer

Integrating Distributed Generation and Storage

by

Sixifo Daniel Falcones Zambrano

A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved June 2011 by the
Graduate Supervisory Committee:

Raja Ayyanar, Chair
Konstantinos Tsakalis
Daniel Tylavsky
George Karady

ARIZONA STATE UNIVERSITY

August 2011

ABSTRACT

The development of a Solid State Transformer (SST) that incorporates a DC-DC multiport converter to integrate both photovoltaic (PV) power generation and battery energy storage is presented in this dissertation. The DC-DC stage is based on a quad-active-bridge (QAB) converter which not only provides isolation for the load, but also for the PV and storage. The AC-DC stage is implemented with a pulse-width-modulated (PWM) single phase rectifier. A unified gyrator-based average model is developed for a general multi-active-bridge (MAB) converter controlled through phase-shift modulation (PSM). Expressions to determine the power rating of the MAB ports are also derived. The developed gyrator-based average model is applied to the QAB converter for faster simulations of the proposed SST during the control design process as well for deriving the state-space representation of the plant. Both linear quadratic regulator (LQR) and single-input-single-output (SISO) types of controllers are designed for the DC-DC stage. A novel technique that complements the SISO controller by taking into account the cross-coupling characteristics of the QAB converter is also presented herein. Cascaded SISO controllers are designed for the AC-DC stage. The QAB demanded power is calculated at the QAB controls and then fed into the rectifier controls in order to minimize the effect of the interaction between the two SST stages. The dynamic performance of the designed control loops based on the proposed control strategies are verified through extensive simulation of the SST average and switching models. The experimental results presented herein show that the transient responses for each control strategy match those from the simulations results thus validating them.

Dedicated to the memory of my beloved son Adrian.

You are my inspiration.

I miss you a lot and I cannot wait to see you again.

ACKNOWLEDGMENTS

Firstly, I thank my Lord for giving me the strength I have needed throughout my academic career. Special thanks to my beloved mom, Felícita Zambrano, for setting the good example and getting me started despite our low income. Thanks a lot to my beloved wife, Merci Manaloto, for her unconditional support. Many thanks to my dear advisor, Prof. Raja Ayyanar, for the opportunity he gave me to work for him as an RA, for his guidance, his patience, his support during difficult times, and for believing in me. I also want to thank Prof. Daniel Tylavsky for the opportunity to work with him as a TA and his caring during my knee injury. I extend my gratitude to my committee members, Prof. Konstantinos Tsakalis and Prof. George Karady, for their support. Finally, thanks to my dear colleagues, Dr. Xiaolin Mao and Dr. Harish Krishnamurthy, for their collaboration and advice. This work was partially supported by the FREEDM Systems Center.

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NOMENCLATURE

#links	Number of links
*	Operating point
AC	Alternating current
AC-DC	Conversion from AC voltage to DC voltage
A_p	Plant A state-space matrix
B_p	Plant B state-space matrix
CCA	Cycle-by-cycle average
CCS	Code Composer Studio™
CLC	Capacitive-inductive-capacitive filter
C_p	Plant C state-space matrix
DAB	Dual-active-bridge
DC	Direct current
DC-DC	Conversion from DC voltage to DC voltage
DER	Distributed energy resources
DES	Distributed energy storage
DG	Distributed generation
DHB	Dual-half-bridge
d_j	Port *j* DC conversion ratio
D_p	Plant D state-space matrix
DSP	Digital signal processor
FID	Fault identification device
FREEDM	Future renewable electric energy delivery and management
f_s	Switching frequency
g_{jk}	Gyration gain from *j* into *k*
HF	High frequency
HVAC	High voltage AC
HVDC	High voltage DC
IEM	Intelligent energy management
IFM	Intelligent fault management
IGBT	Insulated gate bipolar transistors
I_j	Port *j* DC side CCA current
i_j	Port *j* DC side instantaneous current
i_j'	Port *j* DC side instantaneous current referred to port 1
I_{jk}	CCA current from port *j* into *k*
i_{Lj}	Port *j* leakage inductor current
i_{Ljk}	Link inductor current between ports *j* and *k*
KB	Bump-transferring matrix
KLQR	LQR gain matrix
LC	Inductive-capacitive filter
L_{DAB}	DAB leakage inductance
L_j	Port *j* leakage inductance
L_j'	Port *j* leakage inductance referred to port 1
L_{jk}	Link inductance between ports *j* and *k*
L_m	HF transformer leakage inductance
LQR	Linear quadratic regulator
L_{THj}'	Port *j* Thevenin inductance
LVDC	Low voltage DC
m	Number of source ports

MAB	Multi-active-bridge
max	maximum
MHB	Multi-half-bridge
MIMO	Multiple-input-multiple-output
n	Number of MAB ports
N/A	Not applicable
N_j	Port j HF transformer number of turns
$P_{DAB\_\max}$	Max MAB power when operating in DAB mode
PHEV	Plug-in hybrid electric vehicles
P_{jk}	CCA power from port j into k
$P_{MAB\_L\_\max\_pu}$	Max per-unit power for each MAB load port
$P_{MAB\_Link\_\max}$	Max MAB link power
$P_{MAB\_Link\_\max\_pu}$	Max MAB link power in per-unit
$P_{MAB\_\max\_pu}$	Max MAB power in per-unit from source ports into load ports
$P_{MAB\_S\_\max\_pu}$	Max per-unit power for each MAB source port
P_p	Plant state-space representation
$P_{QAB\_1S\_1L\_\max\_pu}$	Max QAB power in per-unit for one-source-one-load scenario
$P_{QAB\_1S\_2L\_\max\_pu}$	Max QAB power in per-unit for one-source-two-load scenario
$P_{QAB\_1S\_3L\_\max\_pu}$	Max QAB power in per-unit for one-source-three-load scenario
$P_{QAB\_2S\_1L\_\max\_pu}$	Max QAB power in per-unit for two-source-one-load scenario
$P_{QAB\_2S\_2L\_\max\_pu}$	Max QAB power in per-unit for two-source-two-load scenario
$P_{QAB\_3S\_1L\_\max\_pu}$	Max QAB power in per-unit for three-source-one-load scenario
$P_{QAB\_Link\_\max\_pu}$	Max QAB link power in per-unit
PSM	Phase-shift modulation
PV	Photovoltaic
PWM	Pulse-with modulation
q	Number of load ports
QAB	Quad-active-bridge
r	Number of forwarding ports
SISO	Single-input-single-output
SST	Solid state transformer
TAB	Triple-active-bridge
THB	Triple-half-bridge
u_p	Plant control variable
VA	Volt-ampere
V_{Batt}	Battery voltage
V_C	Capacitor voltage
v_j	Port j AC side voltage
V_j	Port j DC side voltage
v_j'	Port j AC side voltage referred to port 1
V_j'	Port j DC side voltage referred to port 1
V_L	Inductor voltage
V_{PV}	PV voltage
v_{THk}'	Port k Thevenin voltage
WT	Wind turbine
x_p	Plant state variable
y_p	Plant output variable
ZVS	Zero voltage switching
α	required phase-shift angles between forwarding ports and source ports
α_{QAB}	Required QAB phase-shift angles between forwarding and source ports

β	required phase-shift angles between forwarding ports and load ports
ΔV	Voltage increment
$\Delta\phi$	Phase-shift angle increment
ϕ	Allowable magnitude for MAB phase-shift angles
ϕ_j	phase-shift angle for port j
ϕ_{jk}	phase-shift angle between ports j and k
ψ	Nonlinearity function

I INTRODUCTION

The introduction covers backgrounds on the Solid State Transformer (SST) and the Multi-port DC-DC converters. These two areas provide the motivation for the work presented herein.

A. Background on SST

In the last decade, the Smart Grid concept has drawn the attention of researchers and industry as a feasible solution to the challenges that the entire electrical system is facing due to the growth in load, the increasing penetration of renewables and the deployment of the distributed generation at the consumer end [1].

Currently, the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center is working in several areas in its efforts to contribute with the modernization of the power distribution system and help develop the standards for the implementation and optimal operation of this portion of the future Smart Grid [2]. Fig. 1 depicts the structure of the distribution system envisioned by the FREEDM Systems Center.

The power-electronics-based transformer, or so-called SST, is one of the key components of the FREEDM distribution system. In addition to serving as a regular distribution transformer, the SST provides ports for the proper integration of distributed energy resources (DER) and distributed energy storage (DES), thus enhancing the reliability of the distribution system [3]. Additionally, the SST enables the implementation of distributed intelligence through a secure communication network (COMM) to ensure stability and optimal operation of the distribution system. Another important component of the FREEDM distribution system is the Fault Identification Device (FID), which is a fast protection device deployed to enable Intelligent Fault Management (IFM) [4].

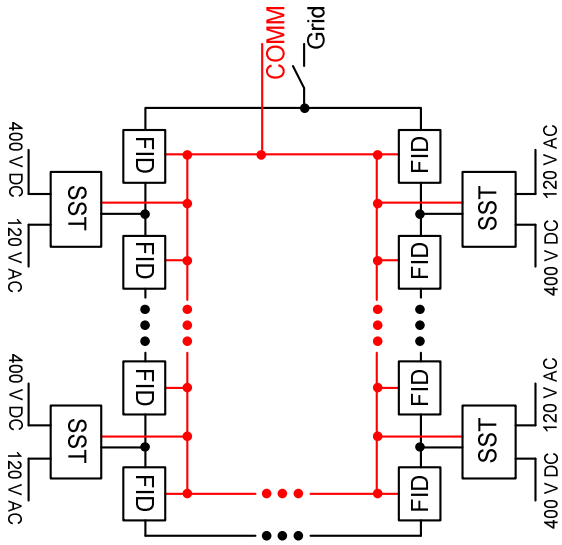


Fig. 1. Envisioned SST based distribution system.

Besides the advantage of its reduced size and weight due to its high frequency (HF) transformer [5], the SST makes use of state-of-the-art Power Electronics devices that allows it to provide additional functionalities such as on-demand reactive power support to grid, power quality, current limiting, storage management and a DC bus for end use. Poor load power factor and harmonics are isolated from the distribution system, thus improving the overall system efficiency. Additionally, the selection of new generation materials for semiconductors and magnetics may help improve its efficiency when compared to a regular transformer of the same ratings. Fig. 2 shows the SST interfacing photovoltaic (PV) generation, storage, electric loads as well as plug-in hybrid electric vehicles (PHEV).

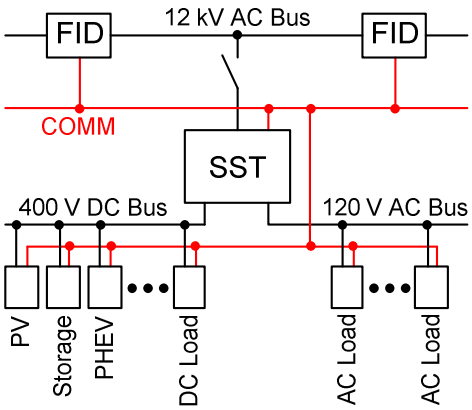


Fig. 2. Integration of DES, DER and intelligent loads through the SST.

B. Background on Multi-port Converters

In the last decades, the interest in renewable sources of energy has increase, considerably. They represent a potential solution to mitigate environmental issues and reduce the dependence on traditional sources of energy for electrical generation. The need of technology for adapting these non-traditional types of energy into the system has motivated the development of new generation power electronics converters. As illustrated in Fig. 3, the future homes will make use of power converters to integrate all the available sources of electrical energy, including renewables as wind turbine (WT) and PV. These power converters have to meet efficiency, flexibility, power density, reliability and safety requirements.

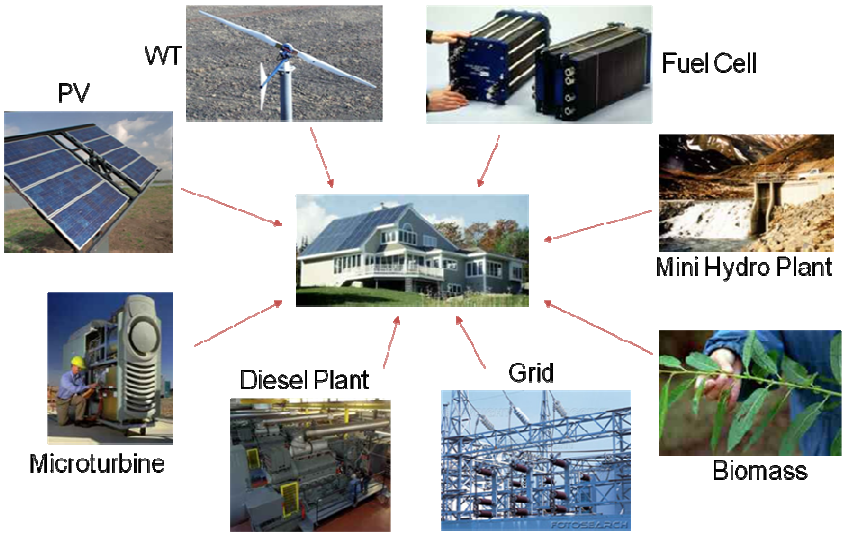


Fig. 3. Available sources of electrical energy for consumer

A generation of power converters that has been proposed by researchers for the integration of distributed generation (DG) and storage is the family of multi-port DC-DC converters [6]. Their advantage lies in the integration of several sources with minimum DC-DC conversion stages. The traditional and integrated configurations introduced in [6] are shown in Fig. 4 and Fig. 5, respectively. The latter may require a reduced the number of components while providing galvanic isolation.

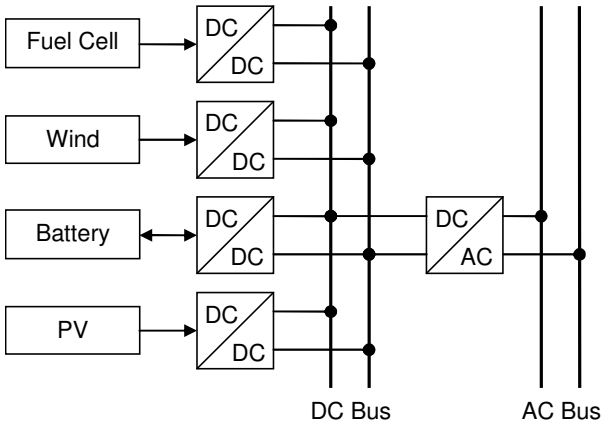


Fig. 4. Conventional power conversion through two-port DC-DC converters

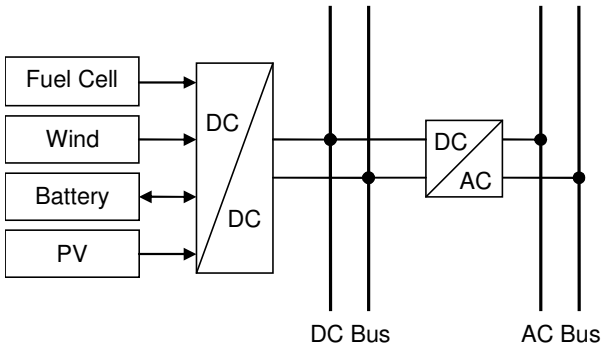


Fig. 5. Integrated power conversion through a multi-port DC-DC converter

C. Research Objectives

Since the SST and the multi-port converters are two key areas of research, the work presented herein has been motivated by the better integration that the SST can achieve with the use of multi-port converters.

As seen in the next chapter, the three-stage configuration that has been identified as a potential candidate for the SST implementation relies on a DC bus for PV and storage integration. This is achieved through separate DC-DC converters as depicted in Fig. 6. Without isolation, the voltage ratings of these devices must be selected mainly based on the DC bus voltage rating. If voltage ratings are not compatible and/or isolation is required, then additional isolation is needed, thus increasing the size of the system. Furthermore, separate controllers for each DC-DC converter are to be designed. In this design process, the stability of the interconnected DC-DC converters must be ensured.

The proposed SST is based on a particular type of multi-port converter, called quad-active-bridge (QAB) converter, to integrate PV and storage. This SST topology eliminates the need of additional isolation and only an integrated controller for the DC-DC stage may be required. The block representation of the proposed SST topology is shown in Fig. 7.

Since little information is available on the literature for the QAB converter, a detailed analysis is required. Furthermore, an average model for any multi-active-bridge (MAB) converter is developed and expressions to calculate the rated power of any MAB port are derived. This is the basis for the dynamic analysis and control design of the DC-DC stage of the proposed SST topology.

The control design for the SST DC-DC stage is performed using both the conventional single-input-single-output (SISO) approach and a more modern multiple-input-multiple-output (MIMO) approach. Furthermore, the SISO controller is complemented with a novel technique to deal with the cross-coupled characteristics of the QAB.

Additionally, the control design for the SST AC-DC stage introduces a technique to deal with the interactions that result when the above two SST stages are interconnected. The performance of the controls is verified through extensive simulation of both switching and average models of the SST. Experimental results from the hardware implementation of a prototype SST are presented for validation purposes. Since no contributions are made on the SST DC-AC stage, it is modeled with a current source during its analysis and simulation, and implemented with an electronics load when testing the prototype SST.

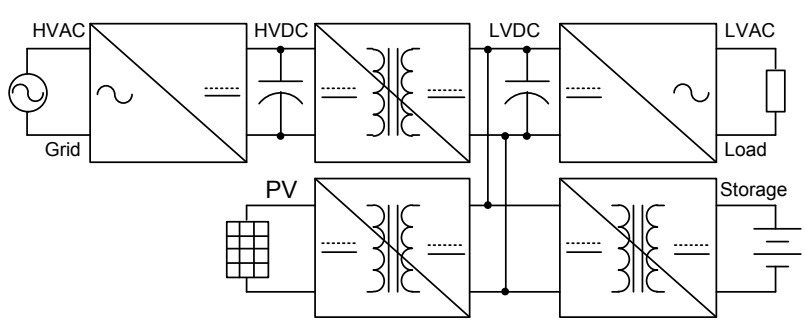


Fig. 6. SST with PV and storage interfaced to LVDC link through separate isolated converters.

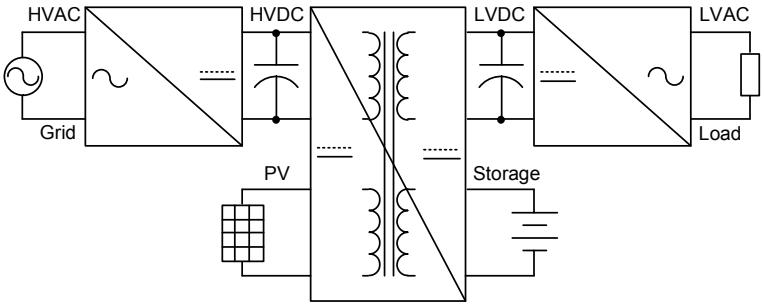


Fig. 7. QAB-based SST with storage and PV.

II REVIEW OF PREVIOUS WORK

This chapter includes literature review on both the SST and the MAB converters. Some of the related work performed by the author of this dissertation is these two areas is also summarized herein.

A. Literature Review on SST

The SST review starts with the available topologies for the implementation of the SST, considering their limitations and strengths to support additional functionalities as compare to a regular distribution transformer. Simulations of some of the functional capabilities are presented based on a three-stage SST topology.

The basic structure of a SST is depicted in Fig. 8. The isolation is achieved through an HF transformer. The grid voltage is converted into a higher frequency AC voltage through the use of power-electronics based converters before to be applied to the primary side of the HF transformer. The opposite process is performed on the HF transformer secondary side to obtain an AC and/or DC voltage for the load.

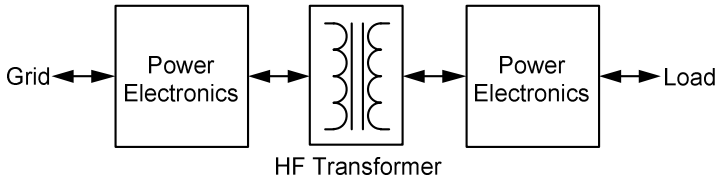


Fig. 8. Basic SST structure.

1) SST Topologies

The selection of the appropriate topology for the SST implementation is a key aspect. In [7] the issue is addressed by comparing some of the potential topologies that support bidirectional power flow as a minimum requirement. In order to select these potential topologies for comparison, a number of topologies proposed for SST as well as for general AC-AC power conversion have been surveyed therein.

An approach to classify the SST topologies and select the appropriate configuration according to the specific needs was introduced in [8]. In this classification, as seen in Fig. 9, four SST configurations that cover all the possible SST topologies are identified: a) single-stage with no DC link, b) two-stage with low voltage DC (LVDC) link, c) two-stage with high voltage DC (HVDC) link, and d) three-stage with both HVDC and LVDC links. The DC link of the third configuration is not appropriate for DES and DER integration since it is high voltage and has no isolation from the grid; therefore, topologies under that classification are not practical for SST implementation.

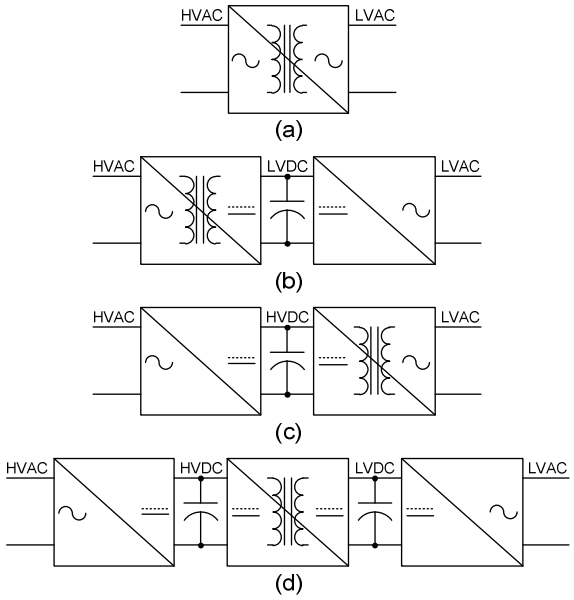


Fig. 9. SST configurations: (a) single-stage, (b) two-stage with LVDC link, (c) two-stage with HVDC link, and (d) three-stage.

Presently, insulated gate bipolar transistors (IGBT) and HF transformers with distribution voltage ratings are not readily available. In order to solve this problem, a modular approach can be used to meet this requirement, in which the high voltage AC (HVAC) sides of several modules are series connected [9]. Additionally, by using the interleaving approach, the ripple currents may be reduced which translates into smaller filter size. Fig. 10 shows a fully modular single-stage configuration. A modular two-stage

configuration is shown in Fig. 11 where only the AC-DC stage is modular. Fig. 12 shows a modular three-stage configuration.

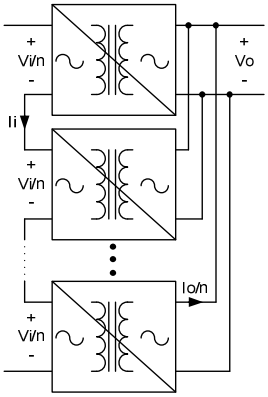


Fig. 10. Modular single-stage SST.

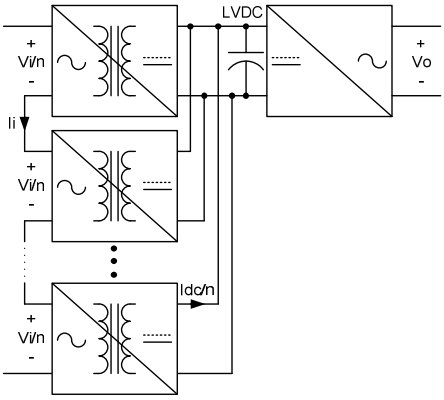


Fig. 11. Modular two-stage SST.

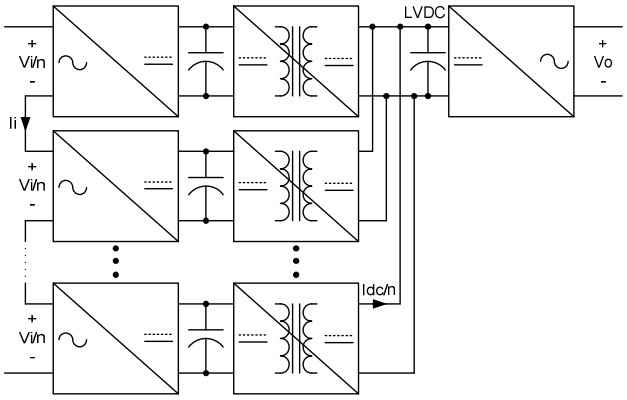


Fig. 12. Modular three-stage SST.

Six representative SST topologies have been identified in [7]:

a) A single-stage SST comprising AC-AC Full-bridge converter modules.

b) A single-stage SST comprising AC-AC Flyback converter modules.

c) A two-stage SST comprising AC-DC isolated Boost converter modules and a pulse with modulated (PWM) dual-phase inverter.

d) A two-stage SST comprising AC-DC Dual Active Bridge (DAB) converter modules and a PWM dual-phase inverter.

e) A three-stage SST comprising a cascaded-full-bridge multilevel rectifier, DC-DC DAB modules and a PWM dual-phase inverter.

f) A three-stage SST comprising a diode-clamped multilevel rectifier, DC-DC Full-bridge converters and a PWM dual-phase inverter.

The single-stage SST topologies require simple control. Their main drawback is the lack of capabilities that the presence of a DC link offers, e.g. input power factor correction. Fig. 13 and Fig. 14 show the AC-AC Full-bridge based SST and the AC-AC Flyback based SST, respectively. For simplicity, both SST topologies are implemented with a single AC-AC module.

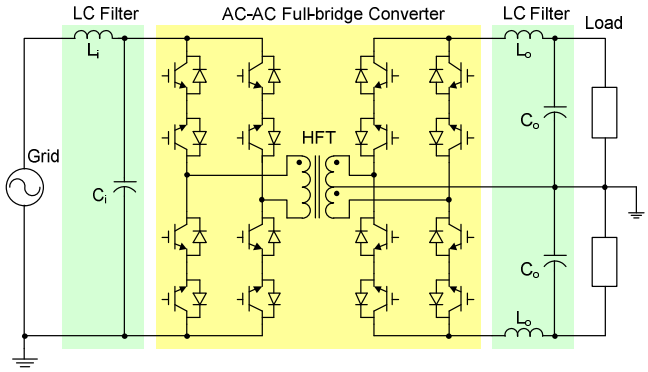


Fig. 13. Single-stage SST based on an AC-AC Full-bridge converter.

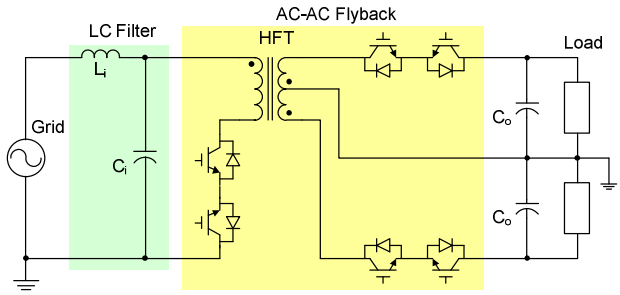


Fig. 14. Single-stage SST based on an AC-AC Flyback converter.

The two-stage SST topologies offer a LVDC link for DER and DES integration. However, due to their lack of a HVDC link, the LVDC link voltage may have a larger 120Hz ripple, caused by the 120Hz ripple currents generated by both AC sides. The selection of a larger capacitance leads to lower bandwidth voltage regulation. Fig. 15 and Fig. 16 show the AC-DC Isolated Boost based SST and the AC-DC DAB based SST, respectively. Both are also implemented with a single AC-DC module.

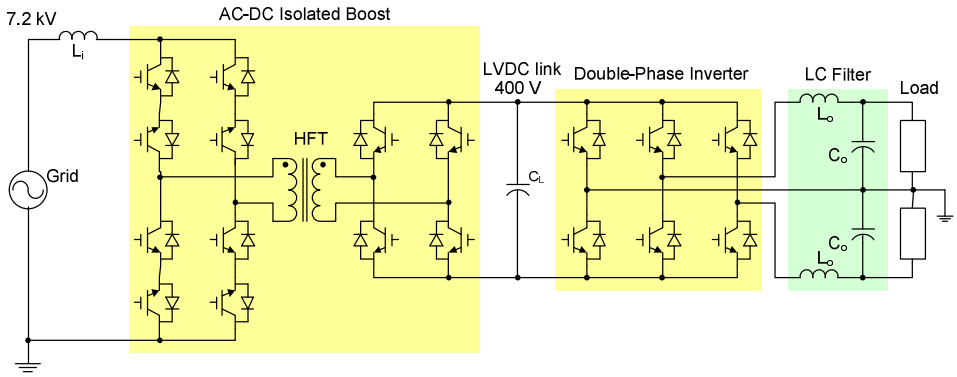


Fig. 15. Two-stage SST based on an AC-DC Isolated Boost converter.

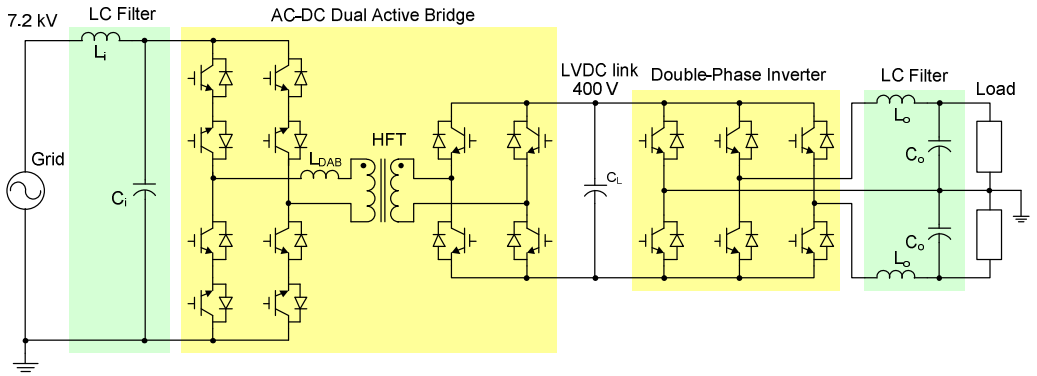


Fig. 16. Two-stage SST based on an AC-DC DAB.

The three-stage SST topologies offer superior controllability that enables all of the functions that are desirable for an SST [10]. The main drawback of this SST topology is the large number of components which translates into possibly lower efficiency and reliability. Fig. 17 and Fig. 18 show the fully modular versions of the DC-DC DAB based SST and the DC-DC Full-bridge based SST, respectively.

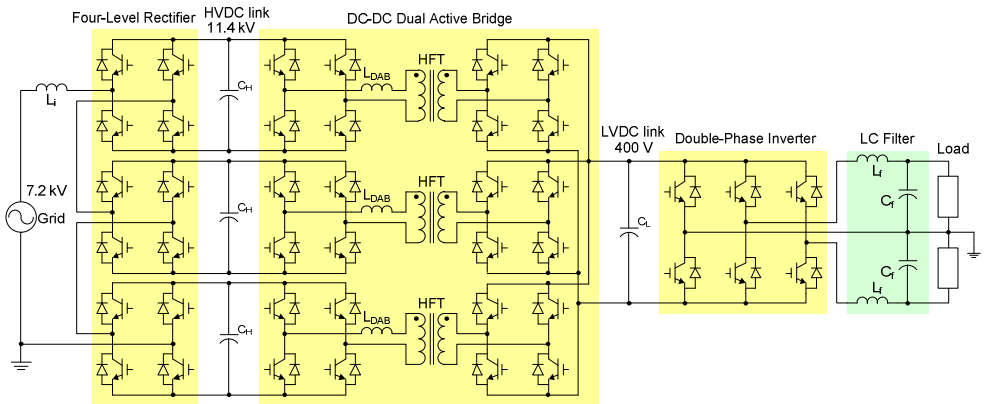


Fig. 17. Modular three-stage SST based on a Four-level Rectifier and three DC-DC DAB converters.

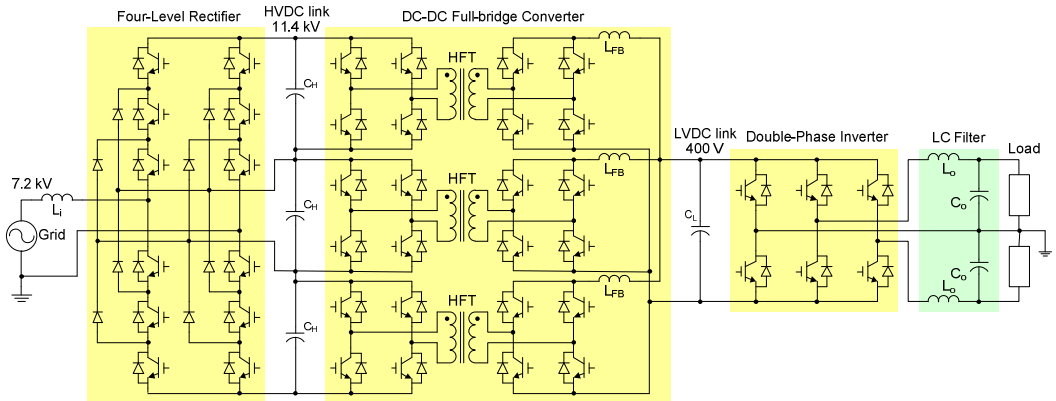


Fig. 18. Modular three-stage SST based on a Four-level Rectifier and three DC-DC Full-bridge converters.

2) Three-stage DAB-based SST Average Model

The three-stage SST topology in Fig. 17 receives the most interest from the FREEDM since its converters require well established control techniques [11]. The work performed in [10] is to provide a black-box model of that topology to support system level analysis and control/protection design for Intelligent Energy Management (IEM) and IFM thrusts using MATLAB™/ Simulink®. The full average model of the selected SST topology is shown in Fig. 19. The presence of the two DC links decouple the SST AC ports, simplifies the controls, enables reactive power support to the grid and provides a LVDC link for DER and DES.

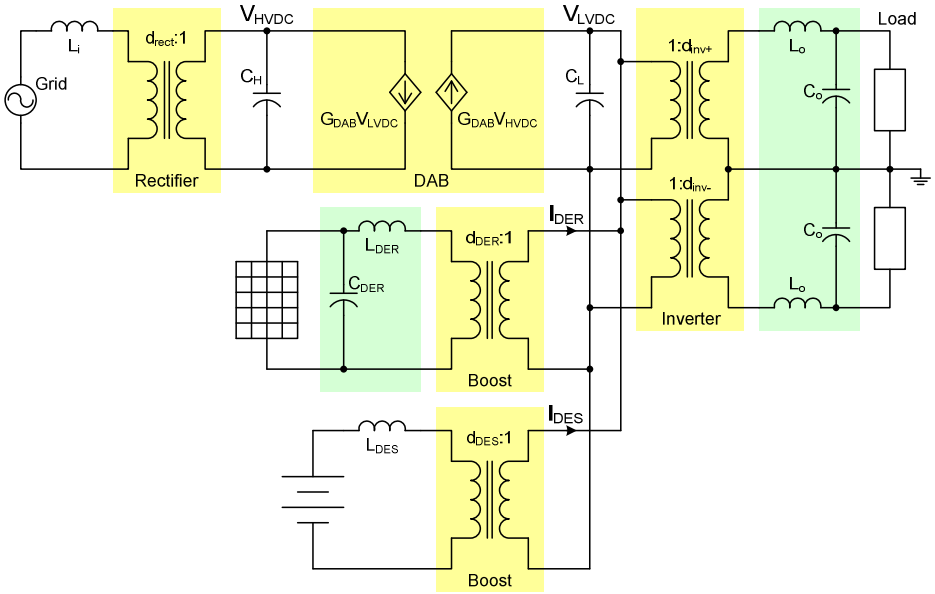


Fig. 19. Three-stage DAB-based SST Average Model.

The above SST average model, along with all the required controls, has been embedded into a Simulink® block. The controls and data ports of the SST block have been implemented with standard Simulink® blocks, whereas the electrical ports have been implemented with SimPowerSystems® blocks. Additionally, the SST block has been placed into a custom library as seen in Fig. 20. This library also includes blocks that model a boost converter for a battery and a photovoltaic (PV) module with its converter. These two extra blocks can be connected to the SST LVDC link and function as current sources. A Simulink® model using the developed blocks is shown in Fig. 21.

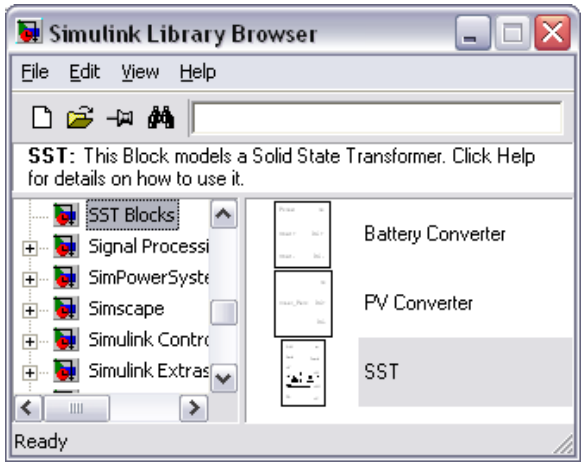


Fig. 20. SST Simulink blockset.

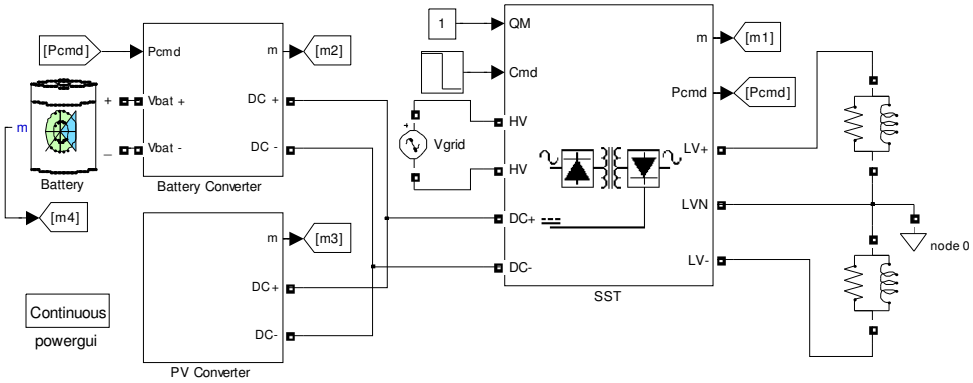


Fig. 21. Simulink model with developed SST block.

The FREEDM test bed, referred to as the green hub, has been modeled using the developed SST block for testing the dynamic performance of the hub centralized and distributed controls under different types of faults and disturbances with and without communication. The Simulink® model of the green hub is shown in Fig. 22.

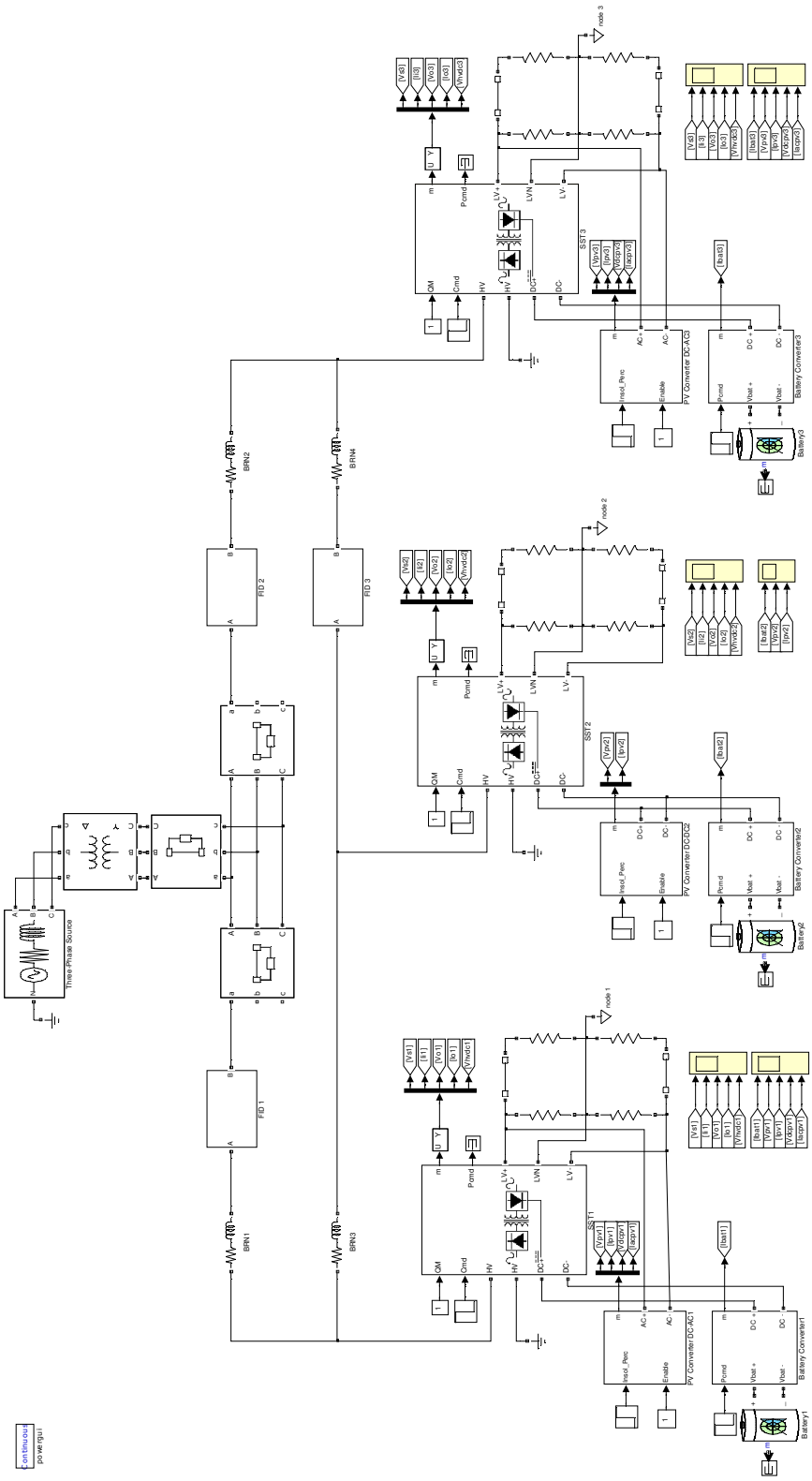


Fig. 22. FREEDM Green Hub Simulink Model.

The long simulation times when testing higher level controls on larger SST-based systems are not practical. In order to solve this problem, a simplified SST average model is proposed in [12]. The new model, as seen in Fig. 23, allows for faster simulation of the system-level controls without loss of detail on the system dominant dynamics. Fig. 24shows the comparison of some waveforms from running both the simplified and the full SST models for a system with only one SST. In this case, the simulation times are 1.1 s and 18.5 s, respectively, on a 3GHz Pentium 4 PC. When simulating the green hub, the simulation times are 8.3 s and 284.6 s, respectively.

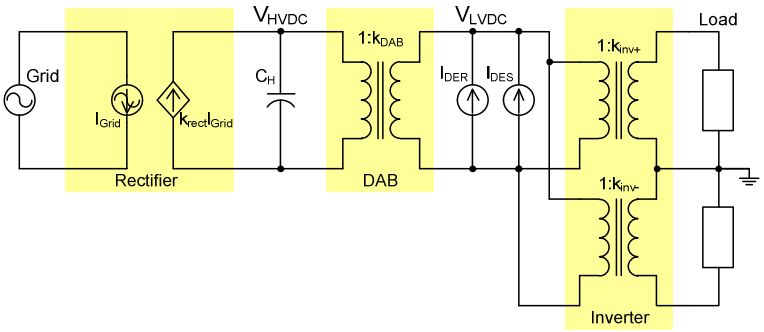


Fig. 23. Three-stage SST simplified average model.

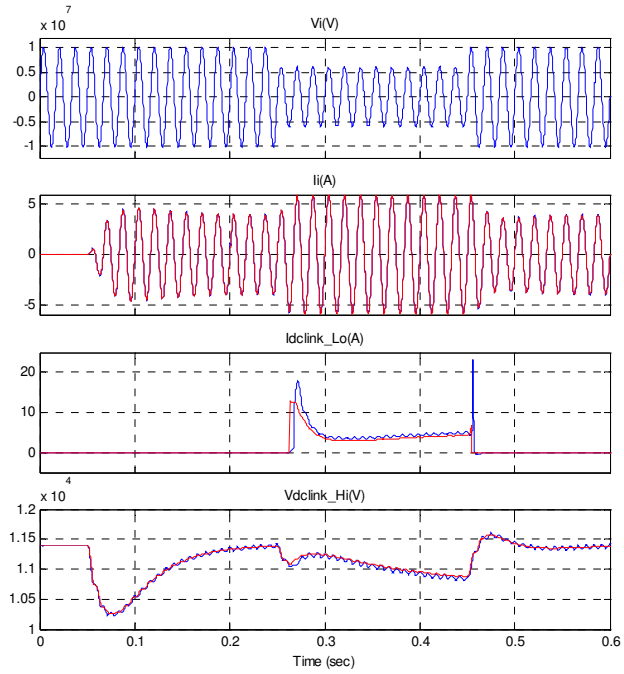


Fig. 24. Simulation results from full and simplified SST models

3) SST Functional Capabilities

Some of the desired SST functional capabilities have been simulated in [10] and [12] using the full average model of the three-stage DAB-based SST topology. A brief review of the SST functional capabilities is presented below.

a) Output voltage regulation. Under normal conditions, the output voltage at each phase is independently controlled to be 120Vrms for most types of loads.

b) On-demand reactive power support to grid. The SST responds to a reactive power command for grid support by injecting or absorbing reactive current into the grid. The actual amount of reactive power is subject to the SST VA rating.

c) Output over current protection. This is achieved through an inner current loop that limits the instantaneous load current. As a result, the SST output switches from a constant-voltage mode into a constant-current mode.

d) Input over current protection. During input voltage sags, the SST input current increases in order to keep the input active power constant. If the input current tends to increase beyond its maximum allowed value, the controls enter into a constant input current mode. In this mode, the input active power no longer meets the load active power demand. As a result, the HVDC voltage will drop at a constant rate.

e) Under voltage trip on HVDC link. The SST discontinues serving the load when the HVDC voltage reaches its minimum allowed value to avoid over modulation on the grid side. At this point, the output voltages are forced to zero.

f) LVDC link for distributed generation and storage. The LVDC link is available to connect DES, DER and DC loads. DES and DER units are required to function as current sources to avoid interference with the LVDC link voltage regulation.

g) Storage management. During transients, the SST generates an active power command for a connected DES device when the active power drawn from the grid is less than the load demand. This helps the SST ride through sustained input voltage sags. In steady state operation, the SST executes the pre-scheduled charging/discharging of the DES.

h) Islanded mode of operation. When the distribution system is disconnected from the grid, the SST input side can be commanded to switch from the normal power-injection mode into a voltage regulation mode, which is achieved through droop-control techniques.

The simulation results from testing some of the above functional capabilities are shown in Fig. 25 through Fig. 29. The transient response to a step reference command for reactive power support is seen in Fig. 25. Here the HVDC voltage remains unperturbed.

However; during voltage sags at the grid side, the HVDC voltage dips during the transitory power balance mismatch as seen in Fig. 26.

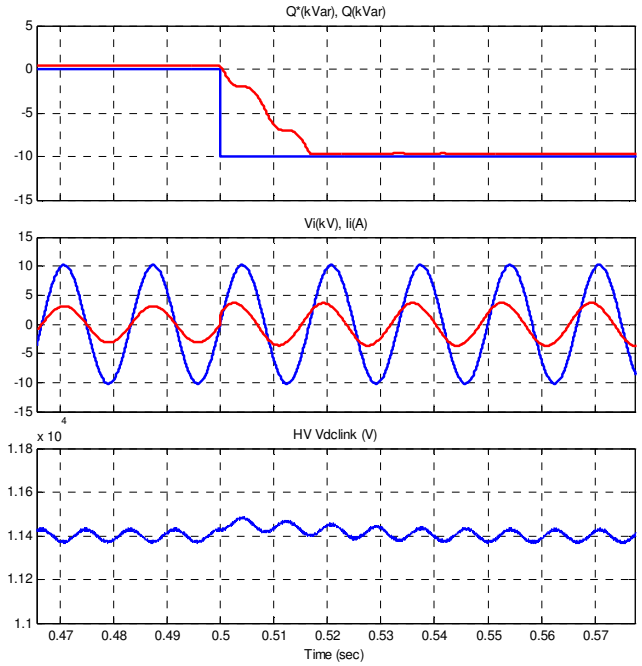


Fig. 25. On-demand reactive power support capability.

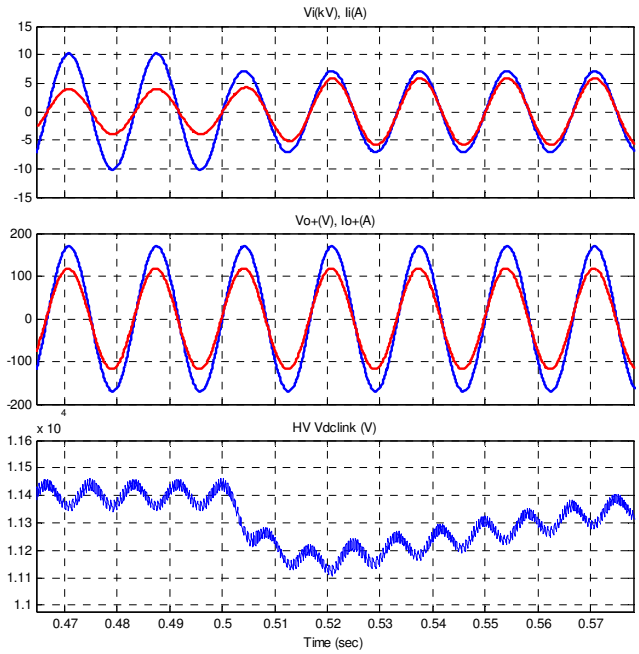


Fig. 26. Simulation results from SST average model demonstrating high-side voltage sag ride-through capability.

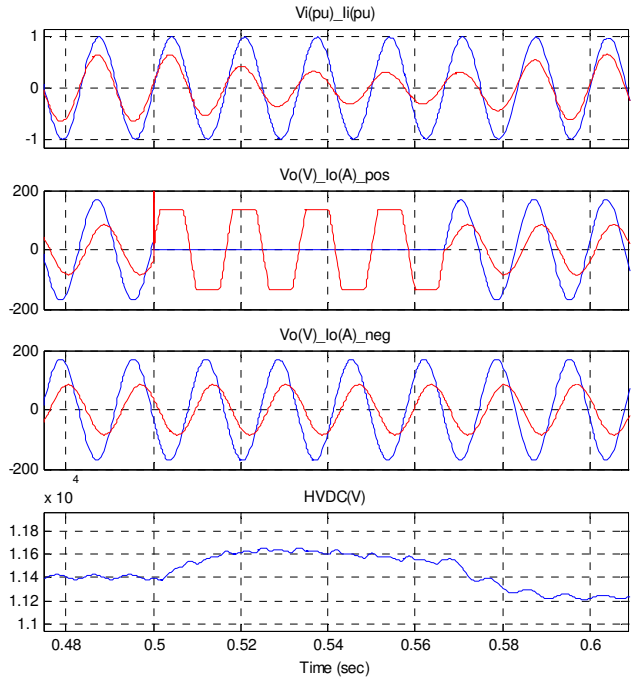


Fig. 27. SST transient response to output fault currents.

Output current limiting is observed in Fig. 27 during a fault at one of the SST outputs. During this time, the active power drawn from the grid is reduced and the truncated shape of the current is maintained to enable the operation of external fault protection devices which detect the high slope of the current at zero-crossing.

Fig. 28 shows the input current limiting feature in action during sustained input voltage sags at rated power load conditions. The HVDC under-voltage protection trips to prevent the discharge of the HVDC link capacitor. The addition of storage allows the SST to send a command for active power support in order to prevent the HVDC link capacitor from discharging as seen in Fig. 29.

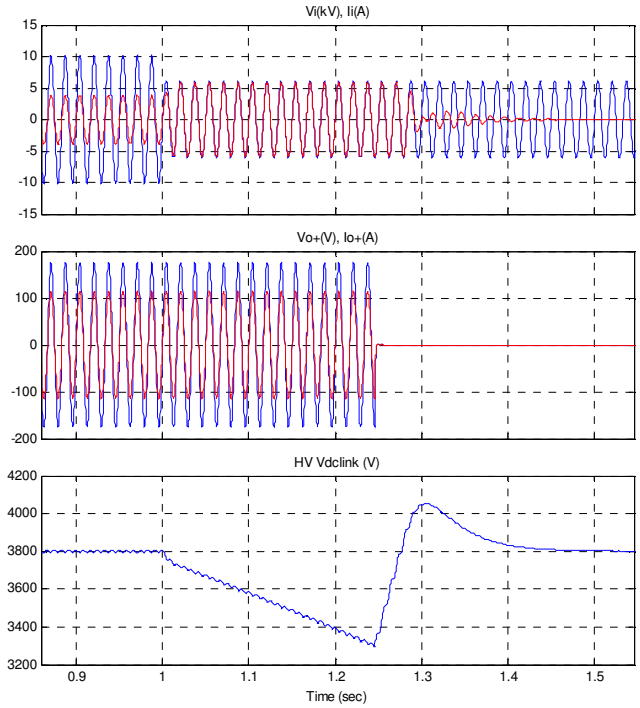


Fig. 28. SST input over current and HVDC link under voltage protection.

The low switch losses and switch count in single-stage SST topologies are at the expense of limited functionalities. For instance, the presence of the LVDC link decouples the input and output, allows for reactive power support to grid and input voltage sag ride-

through. The HVDC link on the three-stage SST topologies helps improve the LVDC link voltage regulation. This is done by transferring the 120 Hz voltage ripple onto the HVDC link. Table 1 summarizes the functional capabilities of each topology compared in [7].

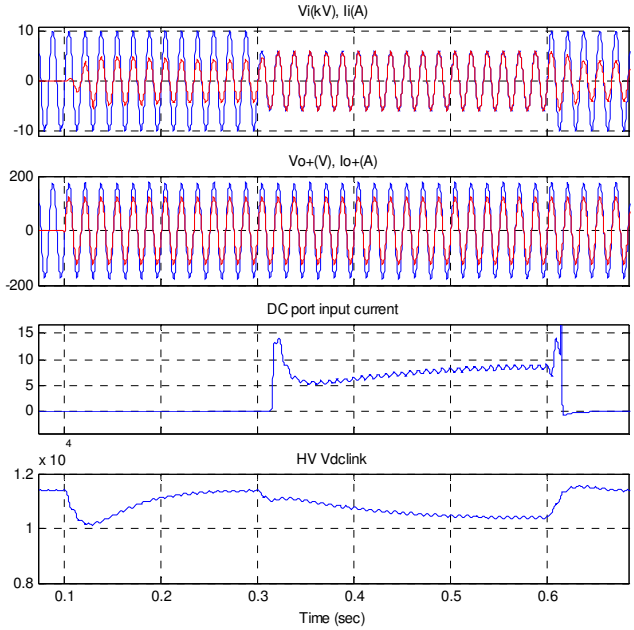


Fig. 29. SST and storage transient response to input voltage sag.

Functionality	Single-stage		Two-stage		Three-stage	
	AC-AC Flyback	AC-AC Full Bridge	AC-DC Boost + Inverter	AC-DC DAB + Inverter	Cascaded Full-bridge Multilevel Rectifier + DAB + Inverter	Diode-clamped Multilevel Rectifier + Full-bridge + Inverter
Bidirectional power	Yes	Yes	Yes	Yes	Yes	Yes
LVDC for DES and DER	No	No	Yes	Yes	Yes	Yes
DES management	No	No	Yes	Yes	Yes	Yes
Reactive power support to grid	No	No	Yes	Yes	Yes	Yes
HVDC link regulation	N/A	N/A	N/A	N/A	Good	Good
LVDC link regulation	N/A	N/A	Good	Poor	Very good	Very Good
Output voltage regulation	Poor	Poor	Good	Good	Good	Good
Input current regulation	No	No	Very good	Good	Very good	Very good
Input voltage sag ride through	Poor	Poor	Good	Good	Very good	Very good
Input current limiting	No	No	Yes	Yes	Yes	Yes
Output current limiting	No	No	Yes	Yes	Yes	Yes
HVDC undervoltage protection	N/A	N/A	N/A	N/A	Yes	Yes
HVDC overvoltage protection	N/A	N/A	N/A	N/A	Yes	Yes
LVDC undervoltage protection	N/A	N/A	Yes	Yes	Yes	Yes
LVDC overvoltage protection	N/A	N/A	Yes	Yes	Yes	Yes
independent frequency	No	No	Yes	Yes	Yes	Yes
independent power factor	No	No	Yes	Yes	Yes	Yes
Modularity Inplementation	Simple	Simple	Simple	Hard	Simple	Simple

* N/A = Not applicable

Table 1. Functional capabilities supported by the SST topologies.

B. Literature Review on MAB converters

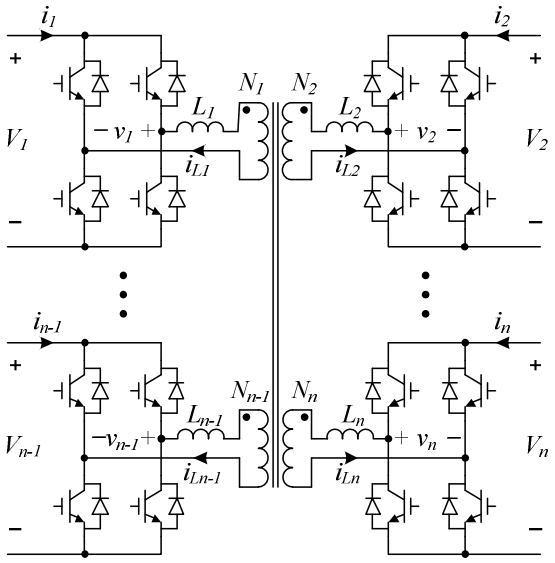


Fig. 30. Generalized MAB switching model.

The MAB converters are comprised of n full-bridge modules magnetically coupled through an n-winding HF transformer as illustrated in Fig. 30. The power that flows between any two ports is controlled through phase-shift modulation (PSM) of the square wave voltages generated at their corresponding AC sides. The dual-active-bridge (DAB) converter introduced in [13] and shown in Fig. 31 can be considered the simplest MAB converter. The equation derived therein for the DAB cycle-by-cycle average (CCA) power can be extended to any MAB converter. Thus the CCA power transferred from port j into port k of an MAB converter is given by

$$P_{jk} = \frac{V_j' V_k'}{2\pi f_s L_{jk}} \phi_{jk} \left(1 - \frac{|\phi_{jk}|}{\pi} \right), \quad \phi_{jk} = \phi_j - \phi_k , \tag{1}$$

where ϕ_j and ϕ_k are the corresponding phase-shift angles, respectively; V_j' and V_k' are the corresponding DC voltages referred to port 1, respectively; f_s is the switching frequency; and L_{jk} is the equivalent leakage inductance between ports j and k. L_{jk} is referred to as the link inductance hereinafter and its calculation is derived in the next section.

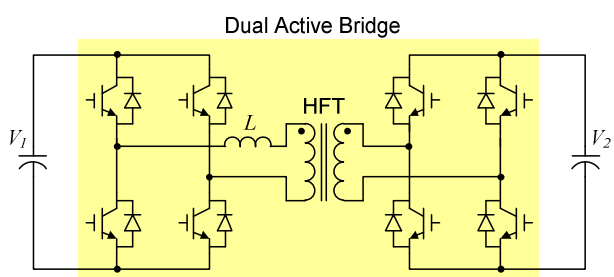


Fig. 31. DAB converter.

The MAB converters have recently gained the attention of researchers as potential solutions for the integration of renewables with isolation [6],[13]-[18]. The advantages of this type of converters are 1) interconnection of sources with different voltage ratings by adjusting the HF transformer turn ratios; 2) single controller design; 3) zero voltage switching (ZVS) capability; 4) and high power density. On the other side, the complexity

of the HF transformer as well as the controller design considerably increases with the number of ports. The ZVS operating region for a DAB converter derived in [13] is shown in Fig. 32.

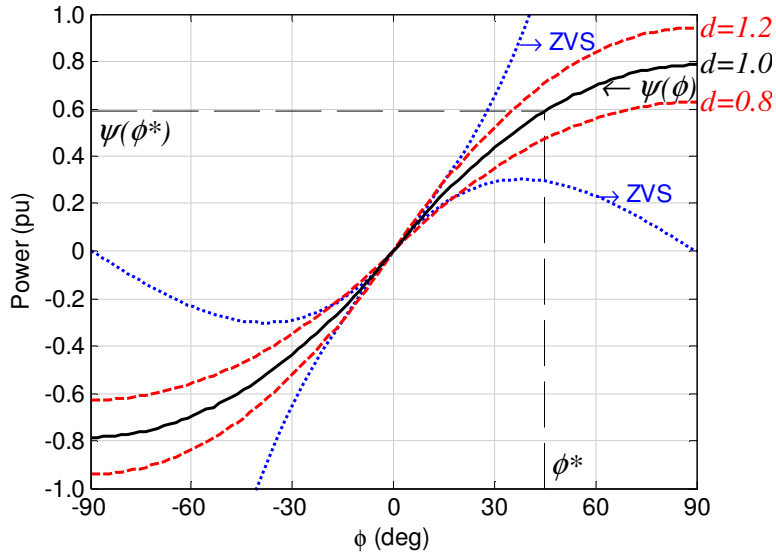


Fig. 32. ZVS operating region of a DAB converter.

The triple-active-bridge (TAB) converter was proposed by [14] and [15]. An attempt to unify all the multiport bidirectional DC–DC converters was made in [6]. Therein, the half-bridge modules are seen as replacement of the full-bridge modules as voltage-fed ports to reduce the switch count. As a result, the dual-half-bridge (DHB) and the triple-half-bridge (THB) converters are derived. In [15], the ZVS is achieved for wide voltage-range operation on one of the TAB DC sides through duty ratio control.

A simple control technique for a TAB-based PV generation system with storage is presented in [16]. This system is shown in Fig. 33. Therein, the controller takes into account the cross-coupling characteristics of the TAB converter to achieve transient ride through support from the storage. The CCA current on the DC side of port 3 is given by (2) and plotted as a function of two of its phase-shift angles in Fig. 34. The observed non-linear characteristics of the TAB converter are also shared by the other MAB converters.

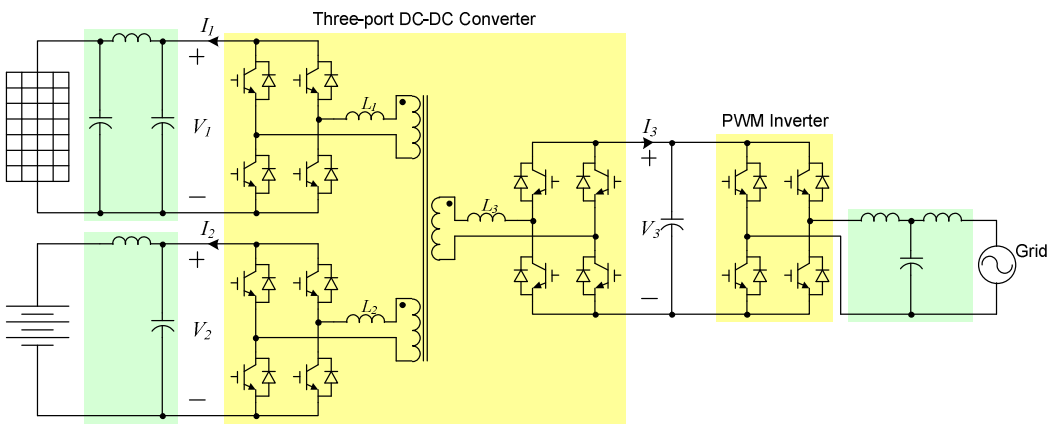


Fig. 33. TAB-based PV generation system with storage.

$$I_3 = \frac{N_1}{N_3}\frac{V_1}{2\pi f_S L_{31}'}\phi_3\left(1-\frac{|\phi_3|}{\pi}\right)+\frac{N_1^2}{N_3 N_2}\frac{V_2}{2\pi f_S L_{32}'}(\phi_3-\phi_2)\left(1-\frac{|\phi_3-\phi_2|}{\pi}\right) \tag{2}$$

In [17] and [18], the authors introduce the QAB converter; however, its analysis is brief and no hardware results have been provided to date.

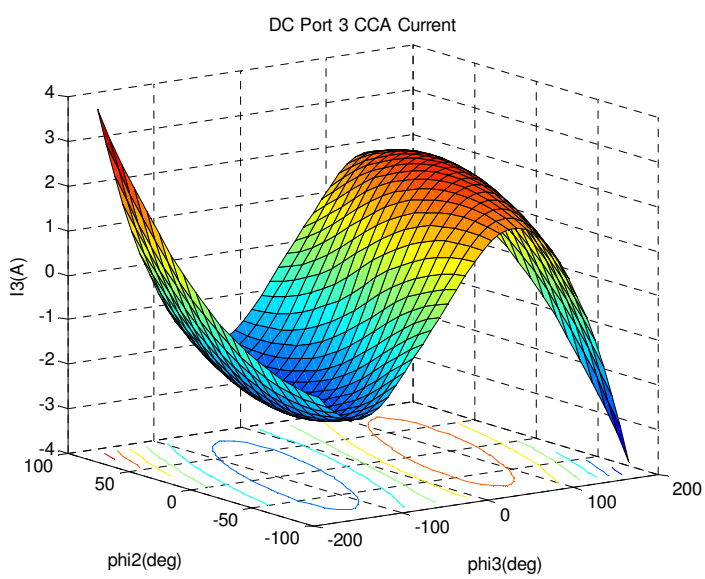


Fig. 34. TAB port 3 CCA DC current as a function of two phase-shift angles.

C. QAB-based SST Topology

The thee-stage DAB-based SST with the integration of PV and storage through separate non-isolated converters is shown in Fig. 35. The proposed SST topology, presented herein, replaces the DAB with a QAB. The two remaining ports are reserved for PV and storage integration. The power will be injected into SST not through the LVDC link, but directly through the HF transformer as seen in Fig. 36.

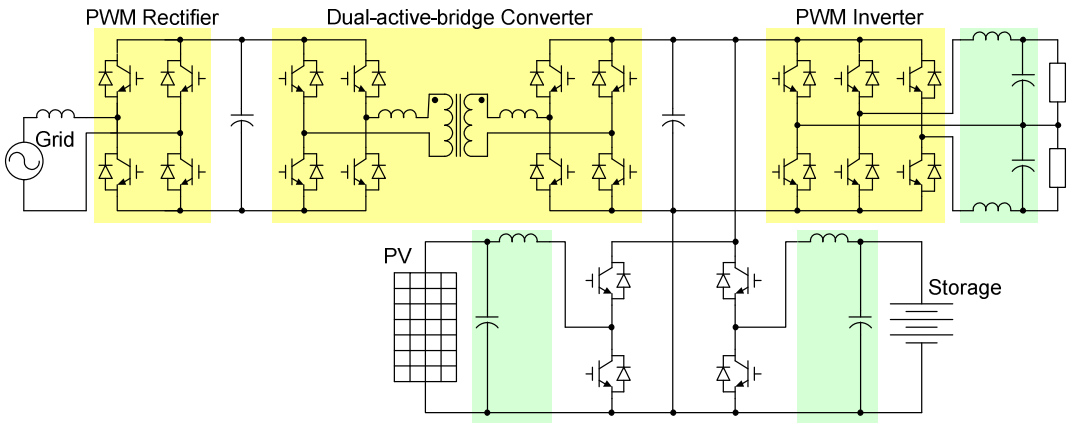


Fig. 35. DAB-based SST with storage and PV interfaced to LVDC link.

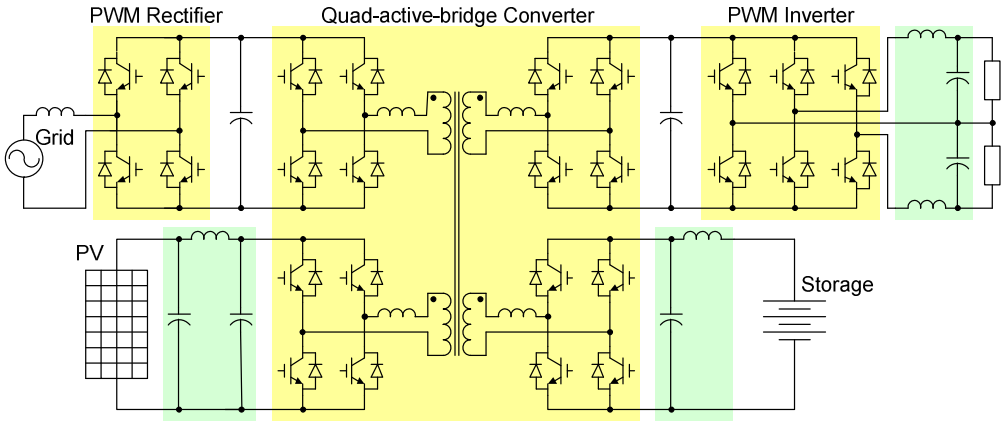


Fig. 36. QAB-based SST with storage and PV.

A detailed analysis of the QAB converter is performed in the next chapter. This is the basis for the control design of the DC-DC stage of the SST.

III MAB AVERAGE MODEL

This chapter starts with the calculation of the MAB link inductances. Then, a unified gyrator-based average model is developed for any MAB converter controlled through PSM. Expressions to determine the power rating of the MAB ports are also derived. For illustration, these results are applied to the QAB converter.

The purpose of the work presented below is to obtain a generalized average model for any MAB converter. This model will simplify the MAB analysis, speed up its simulation, and help identify control strategies for specific applications. In [13]-[18], the equations for the CCA currents on the DC side of the ports are derived from (1) for the particular type of MAB converter analyzed therein and usually represented as a lumped current or power source. This approach hides the interaction between any two individual ports.

For the following analysis, some assumptions are required. For simplicity, the effect of the mutual-leakage inductances within the HF transformer is not considered. This is a good approximation if the self-leakage inductances are modified with the addition of external inductors to the AC side of each port. A more detailed model for the HF transformer, as in [19], would be worth considering in a future work. For convenience, the inductances, currents and voltages are reflected to the primary winding of the HF transformer. The HF transformer magnetizing inductance L_m and the link inductances L_{jk} are defined at port 1.

A. MAB Link Inductances

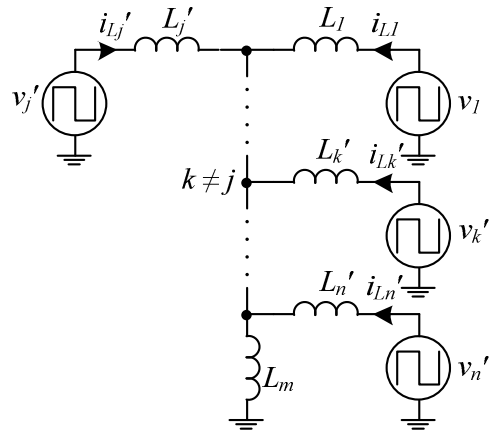


Fig. 37. MAB "Y" equivalent AC circuit referred to port 1.

The AC side of the MAB in Fig. 30 can be represented by the "Y" equivalent circuit in Fig. 37, where the voltages, currents and leakage inductances have been reflected to the primary winding by using (3). In order to identify the CCA power flow between any two ports, the "Δ" equivalent circuit in Fig. 38 is considered.

$$v_j' = \frac{N_1}{N_j} v_j \,,\; i_j' = \frac{N_j}{N_1} i_j \,,\; L_j' = \left(\frac{N_1}{N_j}\right)^2 L_j \,. \tag{3}$$

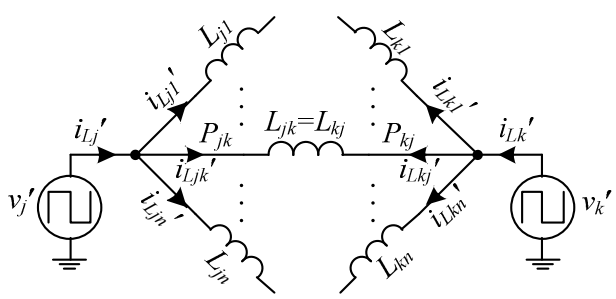


Fig. 38. MAB "Δ" equivalent AC circuit referred to port 1.

The above representation mimics a transmission system with equivalent link-inductors connecting the AC ports to one another. The number of possible links that

results is calculated with (4). Fig. 39 shows how the complexity of the MAB converter increases dramatically as the number of ports increases.

$$\#links = C_2^n = \frac{n!}{(n-2)!2!} \tag{4}$$

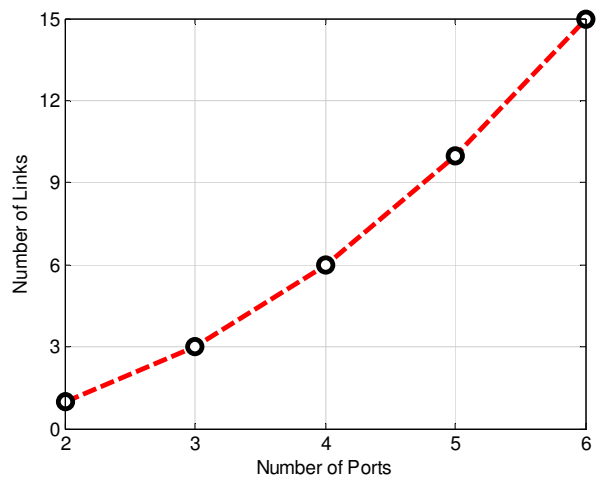


Fig. 39. Number of MAB links as a function of its number of ports.

The AC current i_{Ljk} through the link inductor L_{jk} flows from port j into port k and its waveform can be generated with the corresponding AC voltages, v_j and v_k, as seen in Fig. 40. As a result, by the Superposition principle, the AC current i_{Lj} through the inductor L_j is given by

$$i_{Lj} = \sum_{k \neq j}^{n} i_{Ljk} \ . \tag{5}$$

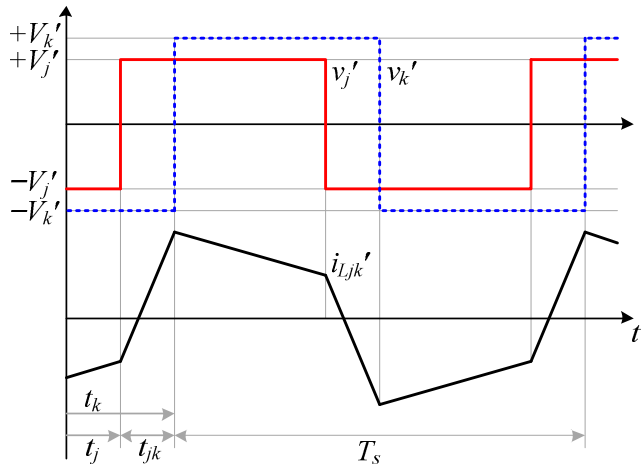


Fig. 40. Link-inductor AC current between MAB ports j and k referred to port 1.

The calculation of the link inductance L_{jk} between ports i and j requires the application of the Superposition principle and Thevenin's theorem. From the circuit in Fig. 37, The Thevenin-equivalent inductance L_{THj}, defined at port 1 and associated with port j, is calculated to be

$$L_{THj} = \left(\frac{1}{L_m} + \sum_{k \neq j}^{n} \frac{1}{L_k'} \right)^{-1}. \tag{6}$$

Likewise, the Thevenin-equivalent AC voltage v_{THk}, defined at port 1 and associated with port k, is given by

$$v_{THk} = \frac{\left(\frac{1}{L_m} + \sum_{l \neq j,k}^{n} \frac{1}{L_l'} \right)^{-1}}{L_k' + \left(\frac{1}{L_m} + \sum_{l \neq j,k}^{n} \frac{1}{L_l'} \right)^{-1}} v_k'. \tag{7}$$

The reduced equivalent circuit under analysis is shown in Fig. 41. Alternatively to (1), the CCA power from port j into port k can be also determined from (8). By simple inspection, when comparing (1) and (8), the link inductance between the two ports is obtained from (9).

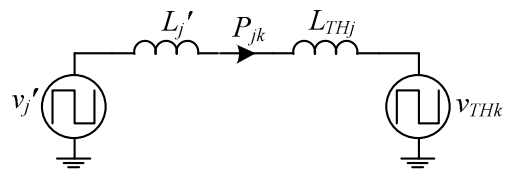


Fig. 41. Thevenin equivalent AC circuit between MAB ports *j* and *k*.

$$P_{jk} = \frac{V_j' V_{THk}}{2\pi f_s \left(L_j' + L_{THj}\right)} \phi_{jk} \left(1 - \frac{\left|\phi_{jk}\right|}{\pi}\right) \tag{8}$$

$$L_{jk} = \left(L_j' + L_{THj}\right) \left[L_k' \left(\frac{1}{L_m} + \sum_{l \neq j,k}^{n} \frac{1}{L_l'} \right) + 1 \right] \tag{9}$$

B. MAB Gyration Gains

In [20], Ehsani *et al.* apply the Gyrator theory to the DAB converter. Therein, the DAB is recognized as a natural gyrator converter since the CCA DC current at one port is proportional to the DC voltage of the opposite port. The involved proportionality gain is called the gyration gain. The same concept can be extended to the MAB converter. This allows the representation of the CCA current on the DC side of any port as a linear combination of the DC voltages of the remaining ports.

The portion of the total CCA current flowing into the DC side of port *j* that is generated by the presence of port *k* is given by

$$I_{jk} = \frac{P_{jk}}{V_j} = \frac{N_1^2}{N_j N_k} \frac{V_k}{2\pi f_s L_{jk}} \phi_{jk} \left(1 - \frac{\left|\phi_{jk}\right|}{\pi}\right), \tag{10}$$

then, the corresponding gyration gain is

$$g_{jk} = \frac{I_{jk}}{V_k} = \frac{N_1^2}{N_j N_k} \frac{1}{2\pi f_s L_{jk}} \phi_{jk} \left(1 - \frac{\left|\phi_{jk}\right|}{\pi}\right). \tag{11}$$

By Superposition principle, the total CCA current flowing into the DC side of port *j* is

$$I_j = \sum_{k \neq j}^{n} I_{jk} = \sum_{k \neq j}^{n} g_{jk} V_k \ , \tag{12}$$

where V_k represents the DC voltage at any other port. The resulting gyrator-based average model for the *j-th* port of the MAB is illustrated in Fig. 42. This model can be extended to multi-port half bridge (MHB) converters after using the appropriate scaling factor for the voltages [21], [22]. Equation (13) remarks how the symmetry of the model can used to reduce the number of calculations by half. The above average model suggests that, through PSM, the gyrator gains could be modulated in order to extend the application of this type of topologies to AC conversion [23].

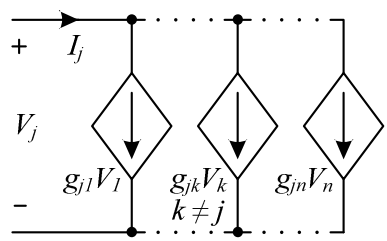


Fig. 42. Gyrator type average model for MAB DC port *j*.

$$P_{kj} = -P_{jk} \ , \ L_{kj} = L_{jk} \ , \ g_{kj} = -g_{jk} \tag{13}$$

C. MAB Port Power Rating

Under a particular power flow scenario, the MAB converter is assumed to operate at its maximum (max) power when at least one phase-shift angle reaches the allowed magnitude. Furthermore, the power rating of an MAB port is constrained by the scenario that results in the max power flowing into or from it. Therefore, the power rating of the full bridge of an MAB port may depend on whether it operates as a source port or as a load port.

If a nonlinearity $\psi(\phi)$ is defined as

$$\psi(\phi) = \phi\left(1 - \frac{|\phi|}{\pi}\right), \tag{14}$$

then, the maximum power that can flow from port j into port k can be expressed as

$$P_{jk\_\max} = \frac{d_j d_k V_1^2}{2\pi f_s L_{jk}} \psi(\phi), \tag{15}$$

where ϕ is a design parameter that represents the allowable magnitude for all MAB phase-shift angles, and $d_j = V_j'/V_1$ and $d_k = V_k'/V_1$ are the DC conversion ratios of ports j and k, respectively.

When the DC conversion ratio approximates to one, the DAB converter is shown to achieve ZVS operation of at light loads in [13]. For wide operating range of DC conversion ratios, a duty ratio control technique to ensure ZVS is presented for the triple-active-bridge (TAB) converter and later generalized for any MAB converter in [15]. Another duty ratio control technique is proposed in [14] in order to minimize the overall TAB converter losses. According to [18], the QAB converter can operate in a DAB mode by disabling two of its ports. In general, an MAB converter can operate in a DAB mode by disabling *n-2* ports.

For simplicity, it is assumed herein that

$$d_j = \frac{V_j'}{V_1} = 1,\ L_j' = L_1,\ \forall j \in [1, n],\ L_m = \infty. \tag{16}$$

By combining (9) and (16), it follows that any MAB link inductance is simplified as

$$L_{jk} = n L_1. \tag{17}$$

Furthermore, by combining (1) and (17), the max power that can flow between any two MAB ports, $P_{MAB\_Link\_\max}$, also referred to as max MAB link power hereinafter, can be simply expressed as

$$\frac{P_{MAB\_Link\_\max}}{n} = \frac{P_{DAB\_\max}}{2}, \tag{18}$$

where $P_{DAB\_\max}$ is the max power that can flow when the MAB converter operates in a DAB mode. The max MAB link power in per-unit is given by

$$P_{MAB\_Link\_\max\_pu} = \frac{P_{MAB\_Link\_\max}}{P_{Base}} = \frac{2}{n}\psi(\phi), \quad P_{Base} = \frac{V_1^2}{2\pi f_s L_{DAB}}, \tag{19}$$

where $L_{DAB}=2L_1$ according to (17).

Intuitively, the maximum power delivered by a source port takes place when the magnitude of the phase-shift angles between it and the load ports reach the allowed value ϕ. Furthermore, a source port can further increase its throughput by redirecting power through passive ports, i.e. those ports with zero net power flow, referred to as forwarding ports hereinafter. In general, the power flow for a MAB converter operating with m source ports, q load ports and r forwarding ports at max power levels is depicted in Fig. 43, where the links represent the total power transferred between two sets of ports, α is the required magnitude for the phase-shift angles between the forwarding ports and the source ports, and β is the required magnitude for the phase-shift angles between the forwarding ports and the load ports.

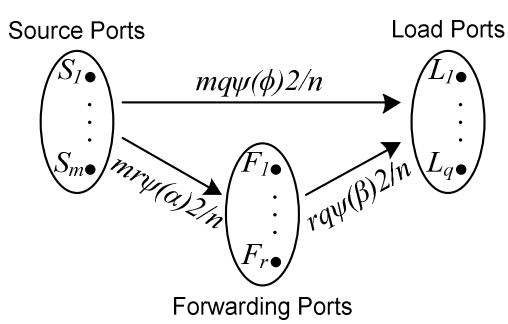


Fig. 43. MAB power flow among source, load and forwarding ports at max power levels.

Under the conditions summarized in Fig. 43, it can be noted that

$$\phi = \alpha + \beta\,,\ n = m + q + r\,. \tag{20}$$

For zero-net power flow at the forwarding ports, it is found that

$$\beta = \psi^{-1}\left(\frac{m}{q}\psi(\alpha)\right), \tag{21}$$

which can be used in combination with (20) to solve for α and β. For the particular case when $m=q$, then $\beta=\alpha=\phi/2$. The total max MAB power in per-unit transferred from the source ports into the load ports is given by

$$P_{MAB\_\max\_pu} = \frac{2m}{n}\left[q\,\psi(\phi) + r\,\psi(\alpha)\right] = \frac{2q}{n}\left[m\,\psi(\phi) + r\,\psi(\beta)\right]. \tag{22}$$

Consequently, the per-unit max power for each source port is found to be

$$P_{MAB\_S\_\max\_pu} = \frac{2}{n}\left[q\,\psi(\phi) + r\,\psi(\alpha)\right]. \tag{23}$$

Similarly, the per-unit max power for each load port is given by

$$P_{MAB\_L\_\max\_pu} = \frac{2}{n}\left[m\,\psi(\phi) + r\,\psi(\beta)\right]. \tag{24}$$

The rated power of each port will result from the analysis of all the valid combinations of m, q and r to find the worst case scenario. The approach developed herein will be illustrated through the analysis of the QAB converter in the next section.

D. QAB Converter Analysis

Since the QAB converter has been selected for the implementation of the SST SC-DC stage, it will be analyzed herein following the approach developed for the MAB converters in the previous section. The switching model of the QAB converter is shown in Fig. 44 while its "Y" and "Δ" equivalent AC circuits as referred to port 1 are shown in Fig. 45 and Fig. 46, respectively. The involved link inductances can be calculated with (9).

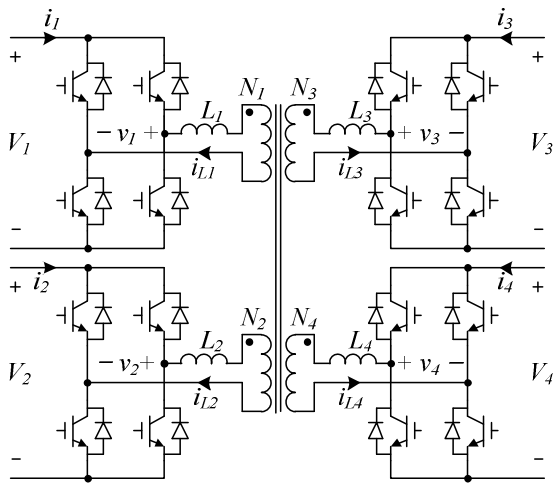


Fig. 44. QAB switching model.

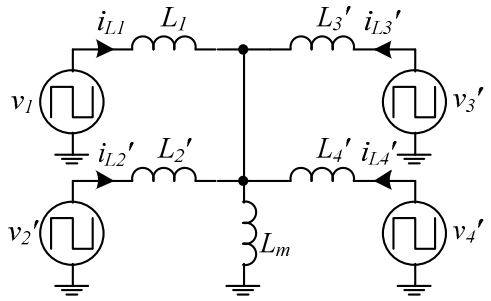


Fig. 45. QAB “Y” equivalent AC circuit referred to port 1.

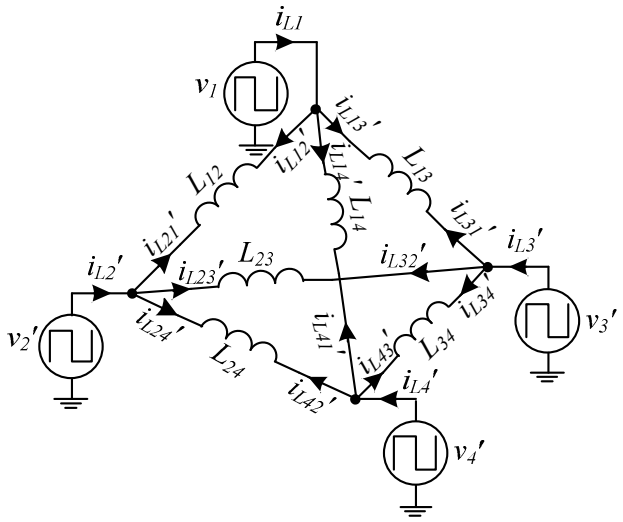


Fig. 46. QAB “Δ” equivalent AC circuit referred to port 1.

Based on Fig. 46, the idealized steady-state QAB waveforms for unity conversion ratios are illustrated in Fig. 47, where the currents on the DC side of the QAB ports have been plotted along with their corresponding CCA values. The gyrator-based average model for the QAB converter is presented in Fig. 48, where the involved gyration gains can be calculated by using (11).

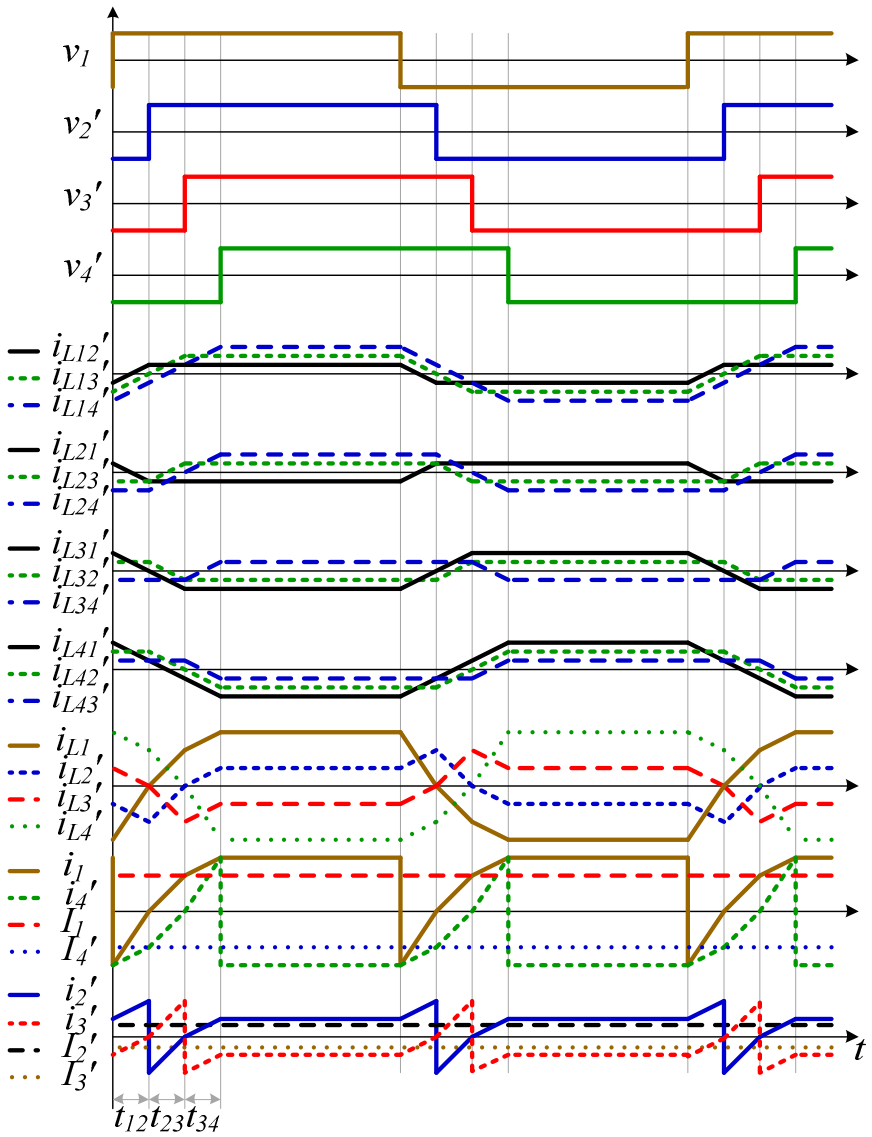


Fig. 47. Idealized steady-state QAB switching waveforms for unity DC conversion ratios.

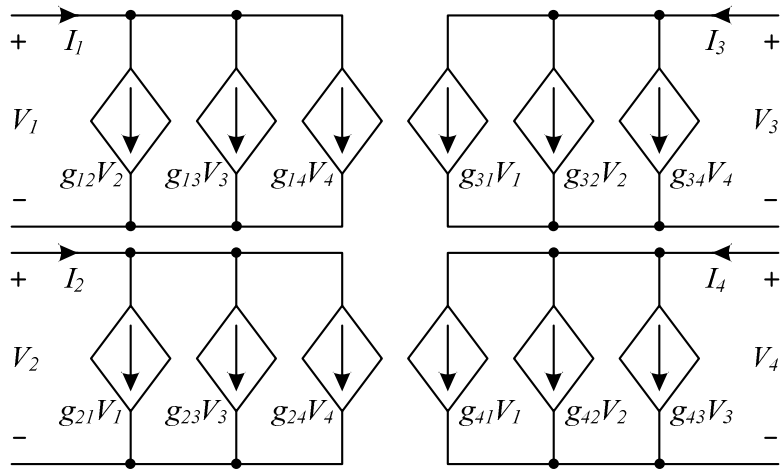


Fig. 48. QAB gyrator-based average model.

When the max QAB link power has been reached between any two ports, the direction of the QAB power flow depends on the number of source, forwarding and load ports. Fig. 49 illustrates the power flow for different operating scenarios. The required phase shift-angle α_{QAB} can be obtained from solving (25). It is important to note that ports not sinking or sourcing power will automatically operate as forwarding ports. The only way a QAB converter can have ports with no participation in the power flow is by turning it into a TAB or a DAB converter [18].

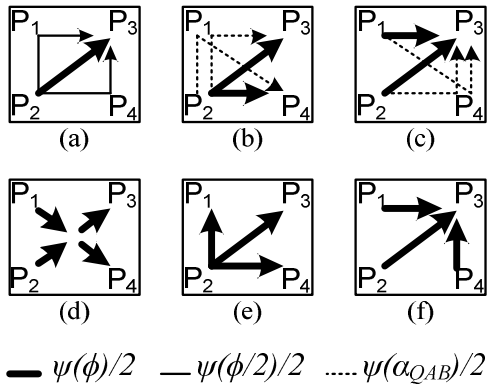


Fig. 49. QAB power flow scenarios at max power levels: (a) one-source-one-load, (b) one-source-two-load, (c) two-source-one-load, (d) two-source-two-load, (e) one-source-three-load, and (f) three-source-one-load.

$$\phi = \alpha_{QAB} + \psi^{-1}\left(2\psi\left(\alpha_{QAB}\right)\right) \tag{25}$$

Depending on the particular application, some QAB ports might not be allowed to operate in all the scenarios depicted in Fig. 49, e.g. the PV port can only source power in steady state for the proposed SST topology; therefore, the ports associated with the grid and the battery cannot simultaneously source power under the scenario represented in Fig. 49 (d), nor can either of them source power under the scenario represented in Fig. 49 (e).

Based on (19), the max QAB link power in per-unit is found to be

$$P_{QAB\_Link\_\max\_pu} = \frac{1}{2}\psi(\phi). \tag{26}$$

When operating in the one-source-one-load scenario, as in Fig. 49 (a), the total max QAB power in per-unit is

$$P_{QAB\_1S\_1L\_\max\_pu} = \frac{1}{2}\psi(\phi) + \psi\left(\frac{\phi}{2}\right). \tag{27}$$

For both scenarios operating with one forwarding port, i.e., one-source-two-load and two-source-one-load, as in Fig. 49 (b) and (c), respectively, the total max QAB power in per-unit is

$$P_{QAB\_1S\_2L\_\max\_pu} = P_{QAB\_2S\_1L\_\max\_pu} = \psi(\phi) + \psi\left(\alpha_{QAB}\right). \tag{28}$$

The total max QAB power in per-unit when operating in the two-source-two-load scenario, as in Fig. 49 (d), is found to be the same as that of the DAB converter as follows

$$P_{QAB\_2S\_2L\_\max\_pu} = P_{DAB\_\max\_pu} = \psi(\phi). \tag{29}$$

Finally, the total max QAB power in per-unit for both the one-source-three-load and three-source-one-load scenarios, as in Fig. 49 (e) and (f), respectively, is

$$P_{QAB\_1S\_3L\_\max\_pu} = P_{QAB\_3S\_1L\_\max\_pu} = \frac{3}{2}\psi(\phi). \tag{30}$$

The total max QAB power in per-unit for each scenario has been plotted as a function of ϕ in Fig. 50. The rated power for each QAB port can be determined depending on the corresponding worst case scenario it may operate. Fig. 50 suggests that, when the QAB converter only operates in the one-source-one-load scenario, turning the QAB converter into a DAB converter in order to minimize losses may result in a reduced capacity, depending on the selected ϕ.

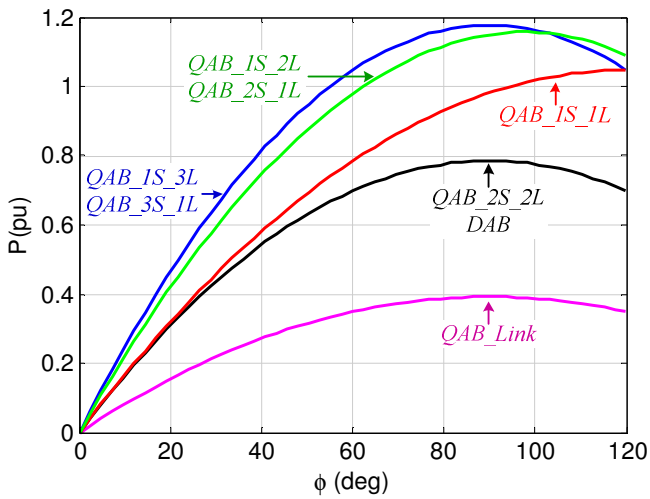


Fig. 50. QAB power curves to determine power rating of source and load ports.

IV SST DC-DC STAGE CONTROL DESIGN

The present chapter focuses on the control design for the DC-DC stage of the proposed SST topology. Both single-input-single-output (SISO) and multiple-input multiple-output (MIMO) types of controllers are designed. A novel technique that complements the SISO controller and takes into account the cross-coupling characteristics of the QAB converter is also presented herein. The block diagram in Fig. 51 summarizes all the controls required for the operation of the SST DC-DC stage.

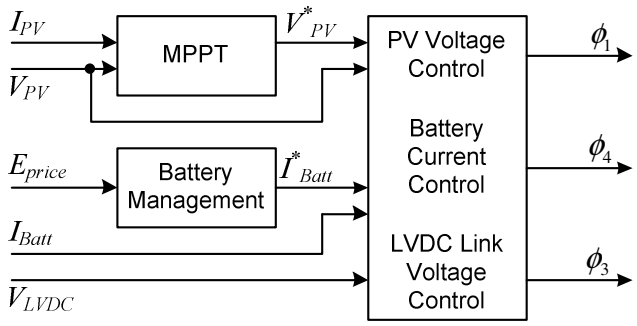


Fig. 51. QAB-based SST controls block diagram.

The switching model of the complete QAB-based SST is shown in Fig. 52. This model has been simplified as in Fig. 53 in order to analyze the SST DC-DC stage. Since the current on the DC side of QAB port results from the rectification of its corresponding inductor current, it has large ripple amplitude with twice the switching frequency. In order to prevent these ripple currents from reaching the PV and storage, CLC and LC filters are added to their corresponding ports, respectively. The ports corresponding to the HVDC and LVDC links are to be back-to-back connected to the rectifier and inverter, respectively; therefore, only DC link capacitors are needed. The HVDC link is modeled as an independent DC voltage source. This port will act as a slack DC bus in order to balance the QAB power flow, including losses. At the other end, the inverter is modeled with an independent DC current source discharging the DC link capacitor. This is a

simple way of modeling the CCA of the DC current absorbed by the inverter stage. A more accurate model requires this current to change in order to keep the load power constant.

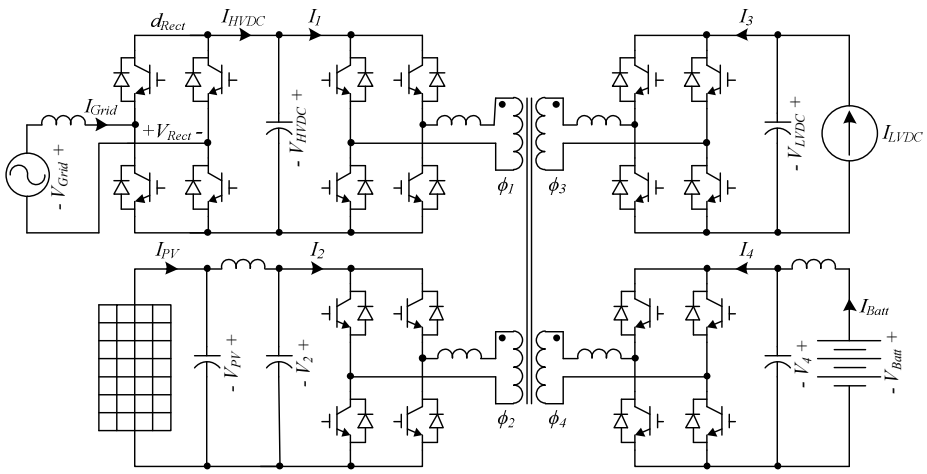


Fig. 52. SST switching model.

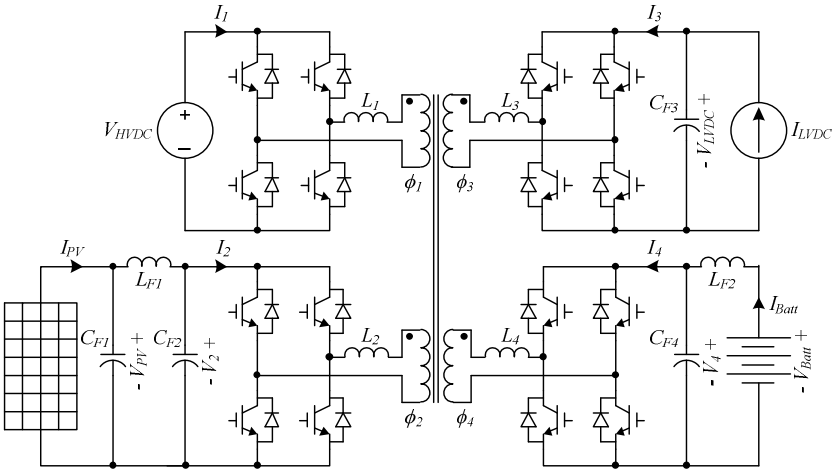


Fig. 53. SST DC-DC stage switching model.

The QAB DC ports are assigned as follows: DC port 1 corresponds to the HVDC link; DC port 2 corresponds to the PV + CLC filter; DC port 3 corresponds to the LVDC link; and DC port 4 corresponds to the battery + LC filter, as seen in Fig. 53

A. SST DC-DC Stage Plant Modeling

In order to simplify the plant modeling, the stray resistances associated with switching, conduction and hysteresis losses within the system have been neglected. Therefore, the modes associated with the external filters are the predominant dynamics of the system. As a result, the designed controller will be based on a loss-less plant, which is a conservative assumption to ensure the stability of the actual system. The block diagram of the SST DC-DC stage is shown in Fig. 54. The input, outputs and disturbances are highlighted in green, red and blue, respectively. Port 1 phase-shift angle ϕ_1 has been set to zero. The CCA current on the DC side of each port is represented by a nonlinearity ψ_j defined as

$$I_j = \sum_{k \neq j}^{4} g_{jk} V_k = \psi_j\left(\phi_j, \phi_{k \neq j}, V_{k \neq j}\right) = \sum_{k \neq j}^{4} \frac{N_1^2}{N_j N_k} \frac{V_k}{2\pi f_s L_{jk}} \left(\phi_j - \phi_k\right)\left(1 - \frac{\left|\phi_j - \phi_k\right|}{\pi}\right), \tag{31}$$

$$j, k \in \{1, 2, 3, 4\}.$$

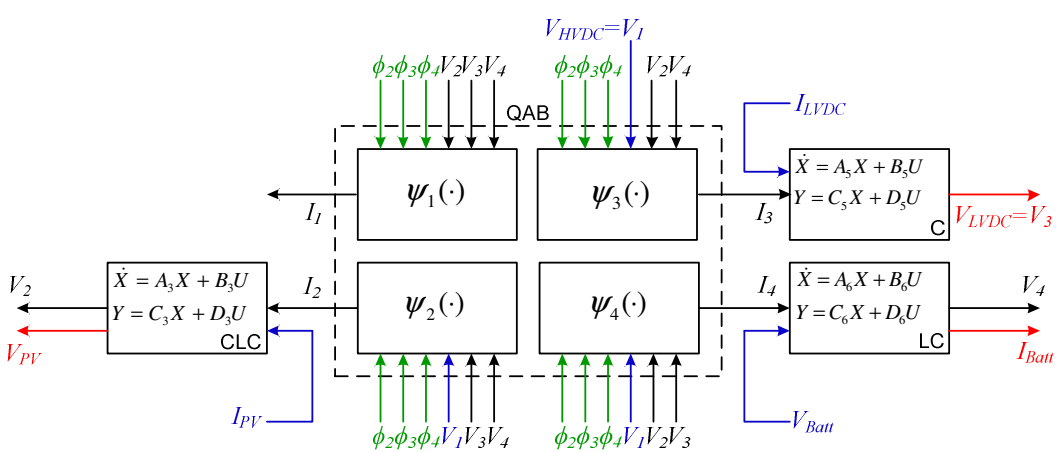


Fig. 54. SST DC-DC stage block diagram.

In order to obtain a state-space representation of the plant, the QAB portion of the plant needs to be linearized around the operating point *. The linearized model that

represents the variation of the currents in (31) as a function of the variations of the DC voltages and the variations of phase-shift angles is

$$\Delta I_j \approx \sum_k G_{jk}\Delta\phi_k + \sum_{l\neq j} H_{jl}\Delta V_l \,, \qquad j,k,l \in \{2,3,4\}, \tag{32}$$

where

$$\Delta I_j = I_j - I_j^*,\ \Delta\phi_k = \phi_k - \phi_k^*,\ \Delta V_l = V_l - V_l^*. \tag{33}$$

The expressions to obtain the coefficients corresponding to the phase-shift angles are shown below. For $k=j$ the coefficients are given by

$$G_{jj} = \left.\frac{\partial I_j}{\partial \phi_j}\right|_* = \sum_{l\neq j}^{4} \frac{N_1^2}{N_j N_l}\frac{V_l^*}{2\pi f_s L_{jl}}\left(1 - \frac{2\left|\phi_j^* - \phi_l^*\right|}{\pi}\right), \tag{34}$$

and for $k\neq j$ the coefficients are given by

$$G_{jk} = \left.\frac{\partial I_j}{\partial \phi_{k\neq j}}\right|_* = -\frac{N_1^2}{N_j N_k}\frac{V_k^*}{2\pi f_s L_{jk}}\left(1 - \frac{2\left|\phi_j^* - \phi_k^*\right|}{\pi}\right). \tag{35}$$

The coefficients corresponding to the DC voltages are obtained from

$$H_{jl} = \left.\frac{\partial I_j}{\partial V_l}\right|_* = \frac{N_1^2}{N_j N_l}\frac{1}{2\pi f_s L_{jl}}\left(\phi_j^* - \phi_l^*\right)\left(1 - \frac{\left|\phi_j^* - \phi_l^*\right|}{\pi}\right). \tag{36}$$

The state-space representation of the plant is defined as

$$P_p = \left(A_p, B_p, C_p, D_p\right) \tag{37}$$

with control variables defined as the angle variations around *

$$u_1 = \Delta\phi_1 = \phi_1 - \phi_1^*,\ u_2 = \Delta\phi_3 = \phi_3 - \phi_3^*,\ u_3 = \Delta\phi_4 = \phi_4 - \phi_4^*; \tag{38}$$

and outputs defined as the variations of the PV voltage, LVDC voltage and battery current around *, respectively. They also represent the first state variables

$$x_1 = y_1 = \Delta V_{PV} = V_{PV} - V_{PV}^*$$

$$x_2 = y_2 = \Delta V_{LVDC} = V_{LVDC} - V_{LVDC}^* \tag{39}$$

$$x_3 = y_3 = \Delta I_{Batt} = I_{Batt} - I_{Batt}^*$$

with the remaining state variables defined as

$$x_4 = \Delta V_2 = \Delta V_{C2} = V_{C2} - V_{PV}^*$$

$$x_5 = \Delta I_{L1} = I_{L1} - I_{PV}^* \tag{40}$$

$$x_6 = \Delta V_4 = \Delta V_{C4} = V_{C4} - V_{Batt}^* .$$

Then, the corresponding state-space matrices are

$$A_p = \begin{bmatrix} 0 & 0 & 0 & 0 & -1/C_{F1} & 0 \\ 0 & 0 & 0 & H_{32}/C_{F3} & 0 & H_{34}/C_{F3} \\ 0 & 0 & 0 & 0 & 0 & 1/L_{F2} \\ 0 & H_{23}/C_{F2} & 0 & 0 & 1/C_{F2} & H_{24}/C_{F2} \\ 1/L_{F1} & 0 & 0 & -1/L_{F1} & 0 & 0 \\ 0 & H_{43}/C_{F4} & -1/C_{F4} & H_{42}/C_{F4} & 0 & 0 \end{bmatrix},$$

$$B_p = \begin{bmatrix} 0 & 0 & 0 \\ G_{31}/C_{F3} & G_{33}/C_{F3} & G_{34}/C_{F3} \\ 0 & 0 & 0 \\ G_{21}/C_{F2} & G_{23}/C_{F2} & G_{24}/C_{F2} \\ 0 & 0 & 0 \\ G_{41}/C_{F4} & G_{43}/C_{F4} & G_{44}/C_{F4} \end{bmatrix}, \tag{41}$$

$$C_p = \begin{bmatrix} I_{3x3} & 0_{3x3} \end{bmatrix},\ D_p = \begin{bmatrix} 0_{3x3} \end{bmatrix}.$$

For convenience, the state vector is represented as

$$X_p = \begin{bmatrix} x_1 & x_2 & x_3 & x_4 & x_5 & x_6 \end{bmatrix}^T = \begin{bmatrix} y_1 & y_2 & y_3 & x_4 & x_5 & x_6 \end{bmatrix}^T = \begin{bmatrix} Y & X_r \end{bmatrix}^T \tag{42}$$

B. Bump-transferring Matrix

This section only applies to the SISO type of control approach. Herein, the linearized model the QAB in (32) is reduced to depend only on the phase-shift angles; therefore, the variations on the DC voltages are assumed to be disturbances.

For convenience, the nonlinear model of the QAB converter in (31) is simply expressed by a nonlinearity vector Ψ defined as

$$I = \begin{bmatrix} I_2 & I_3 & I_4 \end{bmatrix}^T = \Psi(\Phi), \;\; \Phi = \begin{bmatrix} \phi_2 & \phi_3 & \phi_4 \end{bmatrix}^T, \tag{43}$$

where the vector I only includes the CCA currents that drive the corresponding plant outputs. G_Ψ is the transfer function matrix of the linearized model of the QAB converter around the operating point * with its main diagonal and off-diagonal entries given by (34) and (35) respectively.

In order to deal with the cross-coupling characteristics of the QAB converter, a decoupling stage can be implemented at the plant input through the inverse of G_Ψ [24]. This is depicted in Fig. 55 (a), where $G_C = diag[G_{c2}, G_{c3}, G_{c4}]$ is the controller transfer function matrix to be derived in the next section using a SISO approach; ΔE is the variation on the error vector; ΔI_{est} is an estimate of ΔI, i.e. the variation on I; and $\Delta\Phi$ is the variation on Φ. Furthermore, due to the non-linear characteristics of the QAB converter, for an extended operating region, a gain scheduling technique can be implemented to update the entries of G_Ψ [14].

An alternative approach to minimize the interaction between the control loops due to the cross-coupling characteristics of the QAB converter is selecting different bandwidths for the control loops [15]. As a result, the loop with the higher bandwidth will determine the direction of $\Delta\Phi$ during transients. Furthermore, a technique briefly introduced in [16] to manipulate the direction of $\Delta\Phi$ in order to improve the dynamic performance of a particular TAB port can be extended to the QAB converter, and in

general to any MAB converter. This is depicted in Fig. 55 (b), where $\Delta\Phi_{est}$=[$\Delta\phi_{2est}$, $\Delta\phi_{3est}$, $\Delta\phi_{4est}$]^T is an estimate of $\Delta\Phi$ and K_B is defined herein as the Bump-transferring matrix.

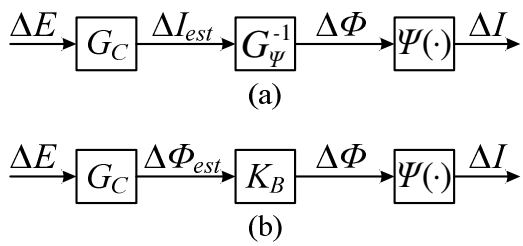


Fig. 55. QAB control strategies: (a) control loop decoupling through the inverse of the plant gain matrix, and (b) manipulation of controls direction through the Bump-transferring matrix.

The selection of K_B consists in setting which direction the QAB power flow should follow when power in injected from any port. Considering that the power is drawn instead will result in the same matrix. For this analysis, the possible power flow scenarios identified in Fig. 49 will be applied to the power variations. This technique enables a port to transfer the power variation (or power bump) onto the ports with lower bandwidth loops. The loop with the lowest bandwidth loop can only transfer the power variation to the slack port, which in this application is the HVDC port. This occurs because the proportions in which the power variation is divided among the QAB links, as indicated in Fig. 49, tends to be dynamically modified by the control loops working at different bandwidths.

When the direction of $\Delta\Phi_{est}$ is not altered, i.e. K_B equals the identity matrix, and power is injected at a high-bandwidth port, the power flow tends to follow the direction shown in Fig. 49 (e) being divided among the other three ports. On the other hand, if the power is drawn, the direction is as shown in Fig. 49 (f).

In order to redirect the power variation to a single port, as in figure Fig. 49 (a), the K_B matrix is obtained in three steps. Given that ϕ_1 is fixed to zero, in order to transfer the power variation from the PV port onto the HVDC port, then

$$\Delta\Phi = \begin{bmatrix} \Delta\phi \\ \Delta\phi/2 \\ \Delta\phi/2 \end{bmatrix} = \begin{bmatrix} 1 & & \\ 0.5 & 1 & \\ 0.5 & & 1 \end{bmatrix} \begin{bmatrix} \Delta\phi \\ 0 \\ 0 \end{bmatrix}. \tag{44}$$

Similarly, in order to transfer the power variation from the LVDC port onto the HVDC port, then

$$\Delta\Phi = \begin{bmatrix} \Delta\phi/2 \\ \Delta\phi \\ \Delta\phi/2 \end{bmatrix} = \begin{bmatrix} 1 & 0.5 & \\ & 1 & \\ & 0.5 & 1 \end{bmatrix} \begin{bmatrix} 0 \\ \Delta\phi \\ 0 \end{bmatrix}. \tag{45}$$

In order to transfer the power variation from the battery port onto the HVDC port, then

$$\Delta\Phi = \begin{bmatrix} \Delta\phi/2 \\ \Delta\phi/2 \\ \Delta\phi \end{bmatrix} = \begin{bmatrix} 1 & & 0.5 \\ & 1 & 0.5 \\ & & 1 \end{bmatrix} \begin{bmatrix} 0 \\ 0 \\ \Delta\phi \end{bmatrix}. \tag{46}$$

Finally, after combining these three partial results, power variations will always get transferred to the HVDC port by using

$$K_B = \begin{bmatrix} k_{22} & k_{23} & k_{24} \\ k_{32} & k_{33} & k_{34} \\ k_{42} & k_{43} & k_{44} \end{bmatrix} = \begin{bmatrix} 1 & 0.5 & 0.5 \\ 0.5 & 1 & 0.5 \\ 0.5 & 0.5 & 1 \end{bmatrix}. \tag{47}$$

Since the HVDC voltage regulation usually has a low bandwidth, a practical selection of K_B is to minimize the disturbances on the HVDC link, which allows for a reduction on the size of the HVDC capacitor. This can be achieved by the transferring any power variation onto the battery port. In order to transfer the power variation from the PV port onto the battery port, then

$$\Delta\Phi = \begin{bmatrix} \Delta\phi \\ 0 \\ -\Delta\phi \end{bmatrix} = \begin{bmatrix} 1 & & \\ & 1 & \\ -1 & & 1 \end{bmatrix} \begin{bmatrix} \Delta\phi \\ 0 \\ 0 \end{bmatrix}. \tag{48}$$

In order to transfer the power variation from the LVDC port onto the battery port, then

$$\Delta\Phi = \begin{bmatrix} 0 \\ \Delta\phi \\ -\Delta\phi \end{bmatrix} = \begin{bmatrix} 1 & & \\ & 1 & \\ & -1 & 1 \end{bmatrix} \begin{bmatrix} 0 \\ \Delta\phi \\ 0 \end{bmatrix}. \tag{49}$$

In order to transfer the power variation from the HVDC port onto the battery port, (46) can be used. After combining these partial results, the required K_B is given by

$$K_B = \begin{bmatrix} 1 & & 0.5 \\ & 1 & 0.5 \\ -1 & -1 & 1 \end{bmatrix}. \tag{50}$$

In summary, the approach presented herein takes into account the cross-coupling characteristics of the QAB converter to improve the dynamical performance of a selected port. This can be generalized to any MAB converter based on its power flow analysis.

C. SST DC-DC Stage SISO Controller

The required transfer functions of the filters at the DC side of the QAB ports as seen in Fig. 53 are defined as

$$G_{PV}(s) = \frac{V_{PV}(s)}{I_2(s)},\ G_{LVDC}(s) = \frac{V_{LVDC}(s)}{I_3(s)},\ G_{Batt}(s) = \frac{I_{Batt}(s)}{I_4(s)}. \tag{51}$$

The block diagram in Fig. 56 shows the SISO type of control loop for the PV voltage implemented herein. The gains associated with the feedback signal conditioning, as well as the DSP digital to analog conversion (ADC) and PWM modules have been intentionally omitted for simplicity. The control loops for the LVDC voltage and the battery current share the same structure and are shown in Fig. 57 and Fig. 58, respectively. Depending on the way the saturation limits are implemented on the DSP,

when one of the loops saturates, it may require K_B to be set to the identity matrix in order to avoid interference with the other control loops.

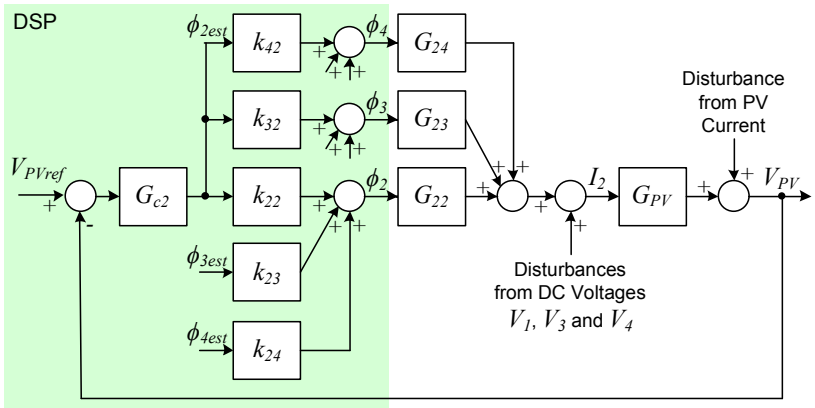


Fig. 56. Simplified PV voltage control loop.

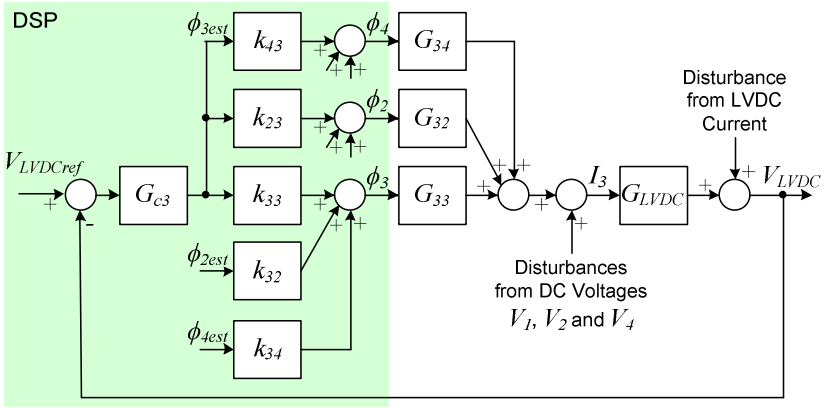


Fig. 57. Simplified LVDC voltage control loop.

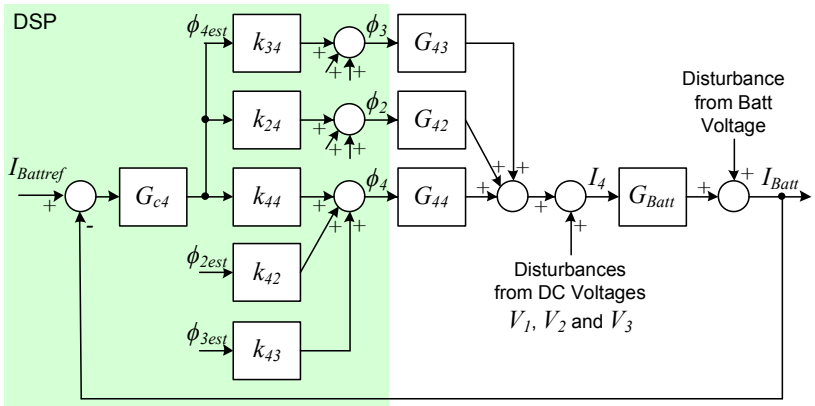


Fig. 58. Simplified battery current control loop.

The entries of G_C have been designed with the k-factor technique [25]. The LVDC loop is selected to be the fastest and the battery loop to be the slowest as seen in the Bode plot in Fig. 59.

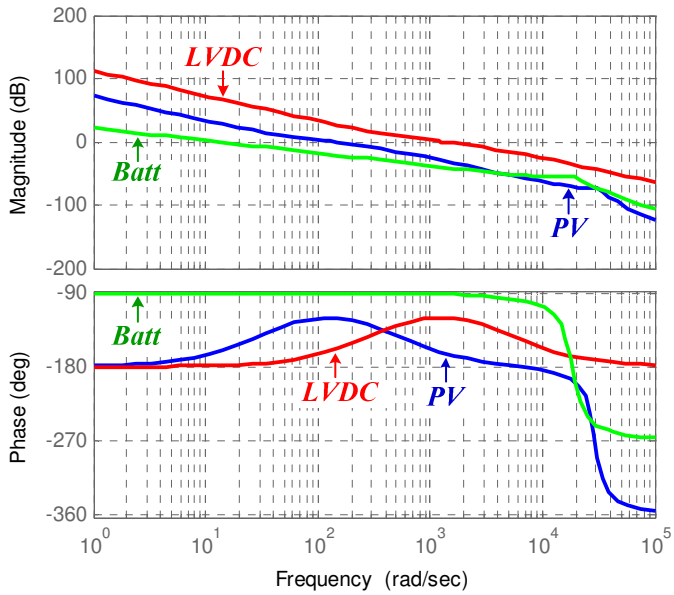


Fig. 59. Bode plot of SST DC-DC stage open-loop gains.

D. SST DC-DC Stage MIMO Controller

As an alternative to the SISO controller designed in the previous section, a MIMO type of control loop can be considered in order to incorporate the DC voltages as plant state variables [26], [27]. The MIMO controller is designed using the Linear Quadratic Regulator (LQR) technique. The availability of voltage and current sensors within the circuit allow for a full-state feedback type of control as the LQR controller.

Since the LQR controller applies proportional gains to the error signals, additional filtering can be implemented within the controller to keep sensor noise from propagating to the controller output. This is done by augmenting the given plant P_p in (37) with a first order filter at its input. The state-space representation of the filter stage is

$$P_f = \left(A_f, B_f, C_f, D_f\right) \tag{52}$$

with state-space matrices

$$A_f = -w_f I_{3x3},\ B_f = w_f I_{3x3},\ C_f = I_{3x3},\ D_f = 0_{3x3}, \tag{53}$$

where w_f if the filter corner frequency in rad/s. The resulting nominal plant is obtained from

$$P_n = P_p P_f = \left(A_n, B_n, C_n, D_n\right), \tag{54}$$

with a new state vector that includes the filter state variables

$$X_n = \left[Y\ X_r\ X_f\right]^T. \tag{55}$$

Additionally, the nominal plant P_n is augmented with integrator at its output to guarantee zero-steady-state. The additional state variables are obtained from

$$\dot{z}_1 = y_1,\ \dot{z}_2 = y_2,\ \dot{z}_3 = y_3. \tag{56}$$

Finally, state-space matrices of the design plant are

$$A = \begin{bmatrix} 0_{3x3} & C_n \\ 0_{9x3} & A_n \end{bmatrix},\ B = \begin{bmatrix} 0_{3x3} \\ B_n \end{bmatrix} \tag{57}$$

with the state vector

$$X = \left[Z\ Y\ X_r\ X_f\right]^T. \tag{58}$$

The augmentation process to obtain the design plant is illustrated in Fig. 60. The LQR controller design process follows below to determine the control gain matrix K_{LQR} defined as

$$U = -K_{LQR}X = -\left[K_y \quad K_z \quad K_r \quad K_f\right]\left[Z\ Y\ X_r\ X_f\right]^T \tag{59}$$

for the obtained design plant.

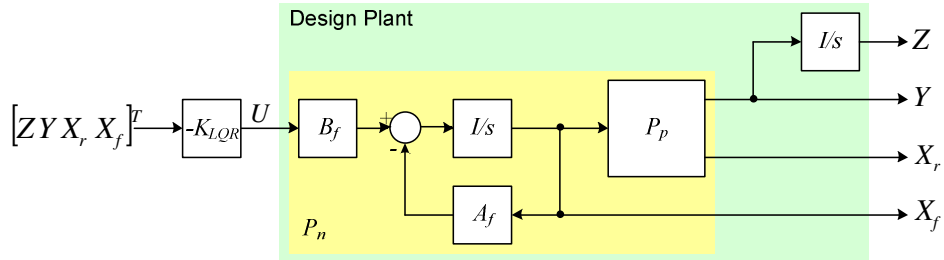


Fig. 60. Design plant for LQR controller.

From [26] and [27], the linear full-state feedback control law in (59) is the solution to the optimization problem: minimize the infinite-horizon quadratic continuous-time cost functional

$$J = \frac{1}{2}\int_0^\infty \left(X^T QX + U^T RU\right) d\tau \tag{60}$$

subject to the linear time-invariant dynamic constraint

$$\dot{X} = AX + BU \tag{61}$$

and initial condition

$$X(0) = X_0 . \tag{62}$$

The control gain matrix is obtained from

$$K_{LQR} = R^{-1} B^T P \tag{63}$$

where P is the unique solution of the Control Algebraic Riccati Equation (CARE):

$$PA + A^T P - PBR^{-1} B^T P + Q = 0 . \tag{64}$$

The control weighting matrix is positive definite and given by

$$R = rI_{3x3} \tag{65}$$

where the parameter r is adjusted manually. The state weighting matrix is positive semi-definite and given by

$$Q = M^T M \tag{66}$$

where

$$M = [M_L \quad M_H] \tag{67}$$

is used for shaping the singular values (SV) of the frequency response of the open loop gain [26]. Then, for SV matching at low frequencies:

$$M_L = \left[C_n(-A_n)^{-1} B_n - D_n\right]^{-1},\ M_H = 0_{3x9}. \tag{68}$$

The SV plots of the frequency response of the open loop gain and the closed loop gain are shown in Fig. 61. A low frequency un-damped mode, which results from the interaction of the filters due to the cross-coupled characteristics of the QAB, is observed. The dispersion observed at the zero-crossing suggests that the bandwidth vary depending on the controls direction.

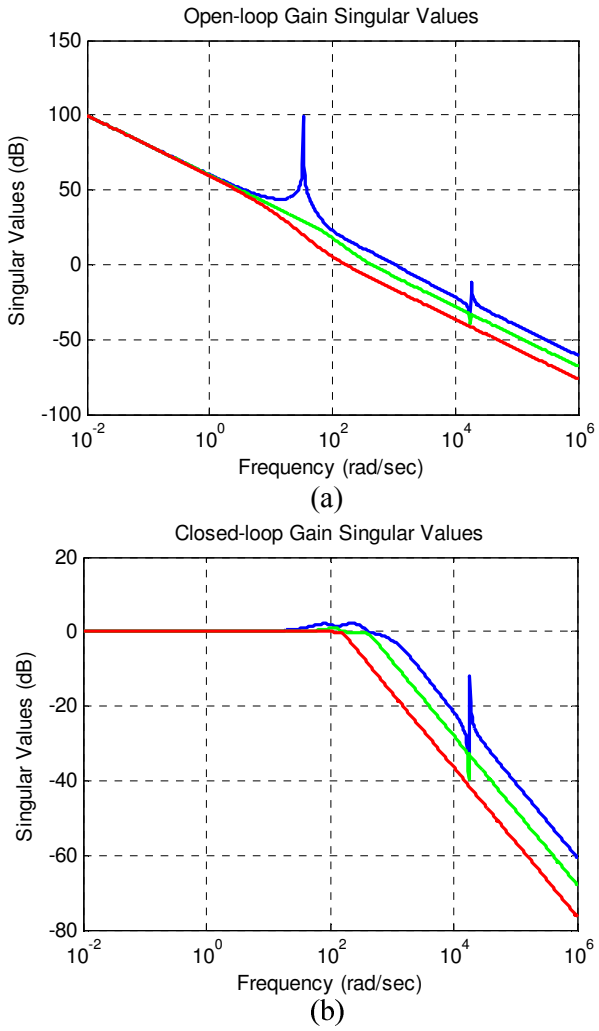


Fig. 61. Singular values of the frequency response of a) open loop gain, and b) closed loop gain, with LQR controller.

The closed loop gain transient response to a step reference command is shown in Fig. 62. Some interaction between the channels is observed. The dynamic performance of this controller is acceptable for the purpose of demonstrating a functional QAB-based SST. The final structure of the LQR controller to be implemented for the DC-DC stage of the SST is depicted in Fig. 63.

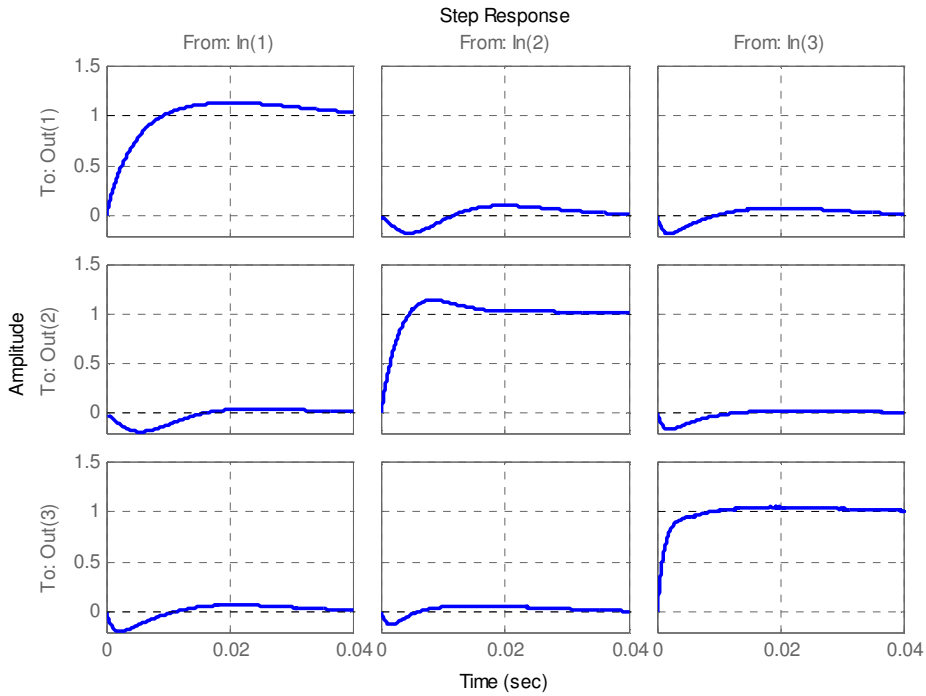


Fig. 62. Closed loop gain transient response to step reference command, with LQR controller.

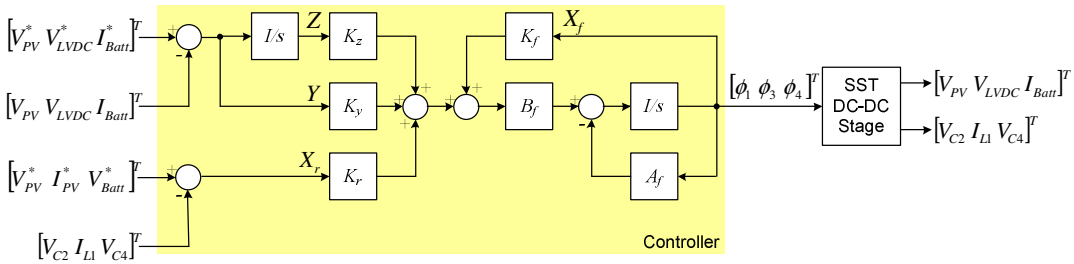


Fig. 63. SST DC-DC stage LQR controller.

An alternative approach for designing the controller is the H-infinity technique [26]. Good properties of the system dynamics can be enforced by applying appropriate constraints. Since this type of controller is not full-state feedback, the addition of a filter for estate-estimation increases the size of the controller. The better dynamic performance of the H-infinity controller can be observed from the SV plots of the frequency response of the open loop and closed loop gains in Fig. 64. This controlled technique is worth

considering in a future work. The only draw back is the complexity of the controller, since it requires more processing from digital controllers for fast systems as power converters. However, its implementation is possible if enough processing bandwidth is available. The closed loop gain transient response to a step reference command is shown in Fig. 65.

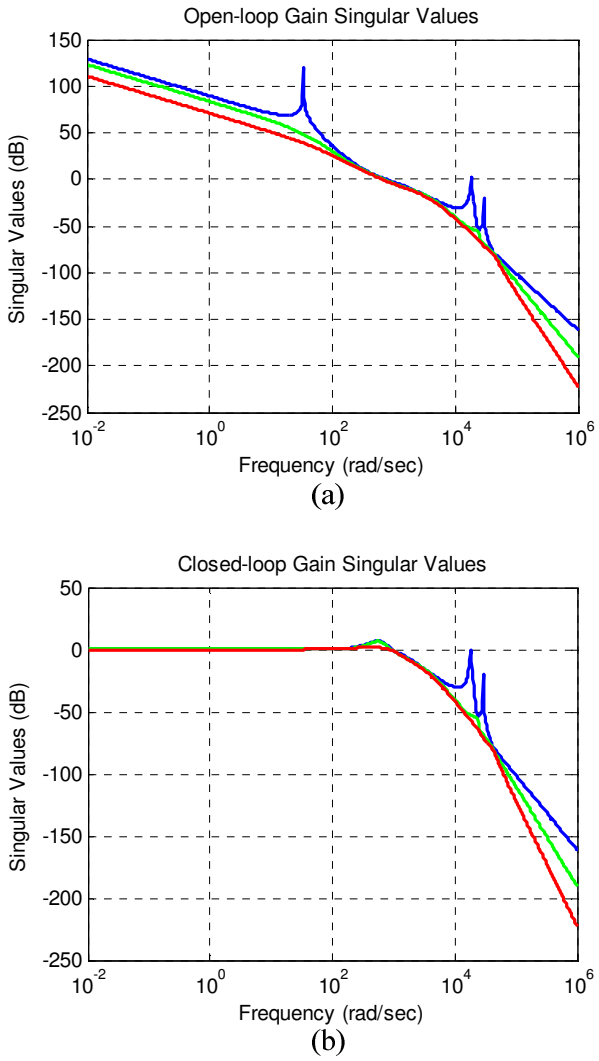


Fig. 64. Singular values of the frequency response of a) open loop gain, and b) closed loop gain, with H-infinity controller.

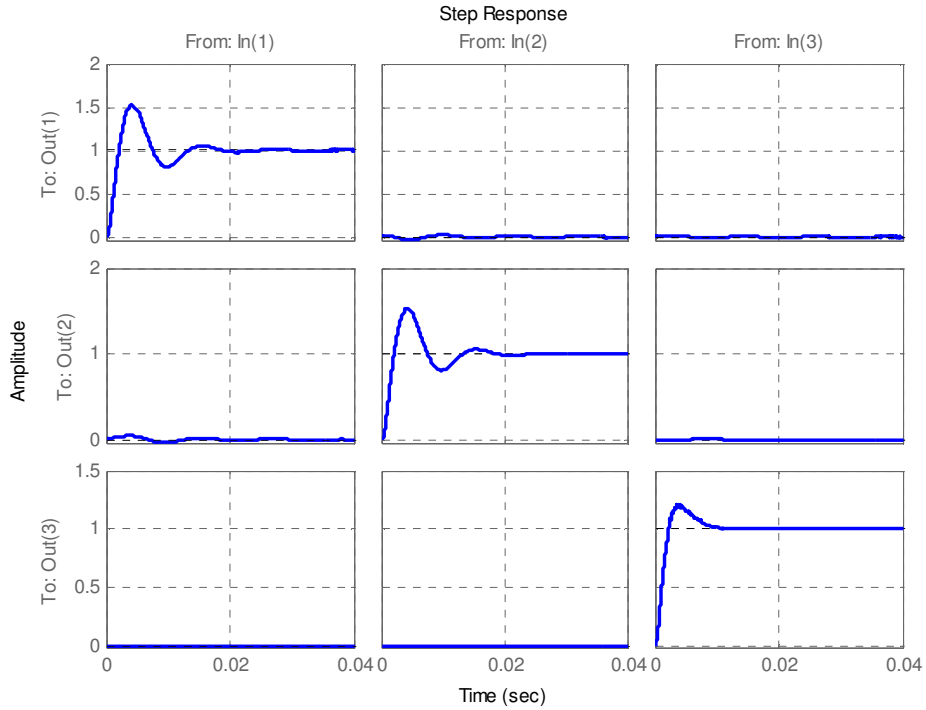


Fig. 65. Closed loop gain transient response to step reference command, with H-infinity controller.

The LQR controller is selected herein for the hardware implementation when assembling the complete prototype SST, since having access to the measurements of all the state variables enables a feedforward technique for the SST AC-DC stage that will be introduced in the next chapter.

V SST AC-DC STAGE CONTROL DESIGN

This chapter presents the analysis of the SST AC-DC stage. The average model is obtained and used to derive the required transfer functions for the designed of the SISO type of controllers for the grid current and HVDC voltage and are connected in a cascaded fashion. Fig. 66 shows the switching model of the SST AC-DC stage considered in this analysis, where the QAB port 1 is modeled with a current source representing the corresponding CCA current.

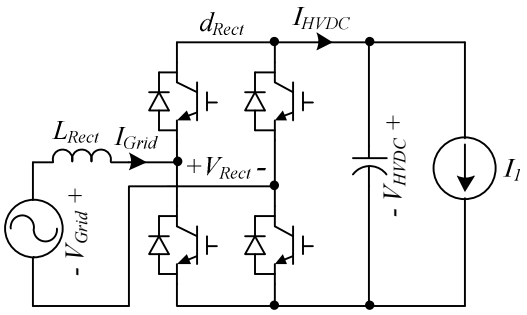


Fig. 66. SST AC-DC stage switching model.

A. SST AC-DC Stage Plant Modeling

The rectifier power poles can be modeled with an ideal transformer as seen in Fig. 67 [25]. The duty ratio, defined in (69), is the control variable and its modulated to regulate the HVDC voltage, ultimately.

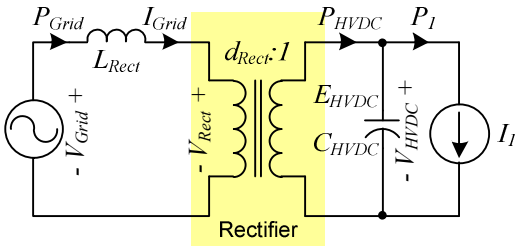


Fig. 67. SST AC-DC stage average model.

$$d_{Rect} = \frac{V_{Rect}}{V_{HVDC}} \tag{69}$$

The grid current is given by

$$I_{Grid} = \frac{V_{Grid} - V_{Rect}}{sL_{Rect}}, \tag{70}$$

where V_{Rect} is the voltage generated by the rectifier. The CCA value of the current at the HVDC side is given by

$$I_{HVDC} = d_{Rect} I_{Grid}. \tag{71}$$

This current drives the HVDC voltage as follows

$$V_{HVDC} = \frac{I_{HVDC} - I_1}{sC_{HVDC}}. \tag{72}$$

The nonlinear characteristics of the rectifier can be simply represented with a nonlinearity ψ_{Rect} as seen in the block diagram depicted in Fig. 68. The input, outputs and disturbances are highlighted in green, red and blue, respectively.

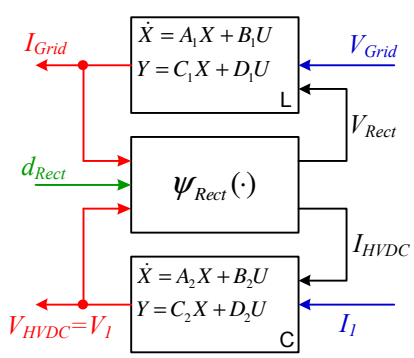


Fig. 68. SST AC-DC stage block diagram.

In order to obtain a linear model of the plant for the outer loop, the HVDC voltage can be represented in terms of the energy of the HVDC capacitor. The energy is calculated from

$$E_{HVDC} = \frac{1}{2} C_{HVDC} V_{HVDC}^2 , \tag{73}$$

and it is related to the power injected into the HVDC link, P_{HVDC}, by

$$E_{HVDC} = \frac{P_{HVDC} - P_1}{s} , \tag{74}$$

where

$$P_{HVDC} = P_{Grid} = \frac{1}{2} V_{Gridpk} I_{Gridpk} . \tag{75}$$

This is based on the assumption that the rectifier is a lossless converter; the 120Hz harmonic is disregarded; and it is operating at unity power factor.

B. Phase-locked Loop

The phase-locked loop (PLL) structure considered herein is presented in [28]. Fig. 69 shows its block diagram. After linearizing the PLL model around the 60Hz frequency, the variation on the error is given by

$$\Delta e \approx \frac{V_{Gridpk}}{2} \Delta \delta . \tag{76}$$

As a result, the transfer function considered for the design of the low pass filter G_{LPF} is

$$G_{PLL}(s) = \frac{e(s)}{\omega(s)} = \frac{V_{Gridpk}}{2s} . \tag{77}$$

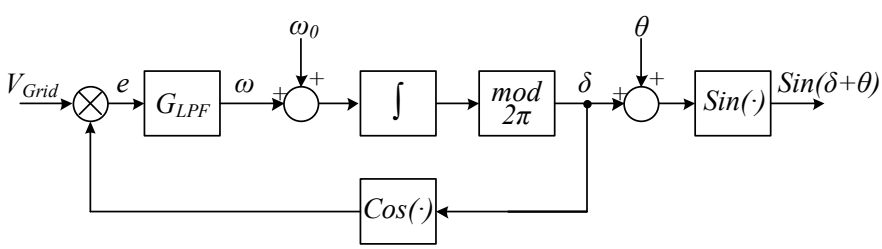


Fig. 69. PLL block diagram.

C. Cascaded Controllers

The required controllers for the SST AC-DC stage are depicted in Fig. 70. The inner loop corresponds to the grid current control which is designed to follow a sinusoidal reference. The outer loop corresponds to the HVDC voltage control.

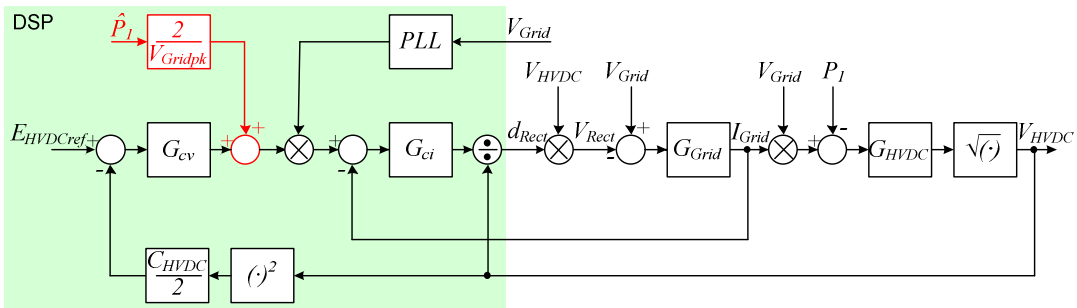


Fig. 70. SST AC-DC stage cascaded controllers.

The transfer function considered for the design of the current loop controller is given by

$$G_{Grid}(s) = \frac{I_{Grid}(s)}{V_{Rect}(s)} = -\frac{1}{sL_{Rect}}, \tag{78}$$

while the transfer function considered for the design of the voltage loop controller is given by

$$G_{HVDC}(s) = \frac{V_{HVDC}^2(s)}{P_{Grid}(s)} = \frac{2}{sC_{HVDC}}. \tag{79}$$

In order to minimize the interaction between the two SST stages a novel technique is presented herein. The power P_1 required by the QAB port 1 is estimated based on the measured QAB DC voltages and the phase-shift angles generated by the LRQ controller and is fed into the HVDC voltage loop. The estimated P_1 power is obtained from

$$\hat{P}_1 = V_{HVDC}\hat{I}_1 = V_{HVDC}\left(g_{12}V_{C2} + g_{13}V_{LVDC} + g_{14}V_{C4}\right). \tag{80}$$

This technique is an alternative to the one proposed in [29] for the three-stage DAB-based SST in Fig. 35 which can only be extended to any MAB converter as long as each port can be modeled as a power source/load. However, the technique presented herein and summarized by (80) can be applied to any type of source/load at any MAB port.

In order to verify the performance of all the designed controls, intensive simulations of both the SST AC-DC stage and the complete SST are performed. Additionally, a hardware prototype is implemented for validation purposes. These results are presented in the next two chapters. The Bode plots corresponding to the HVDC voltage and the grid current loops are shown in Fig. 71.

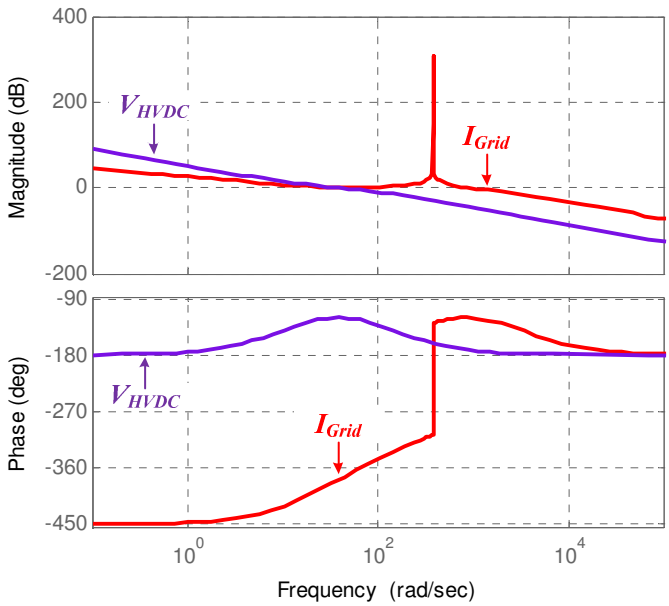


Fig. 71. Bode plot of SST AC-DC stage open-loop gains.

VI SIMULATION RESULTS

The simulation results of the SST topology introduced in chapter II are presented in this chapter. The system features the controllers designed in chapters IV and V. The selected simulation package is MATLAB™/Simulink® complemented with PLECS® blockset. MATLAB™ offers powerful tools for control design. Simulink® has a large library of blocks for implementing the controls, while PLECS® adds additional libraries for simulation of power electronic circuits.

A. SST DC-DC Stage

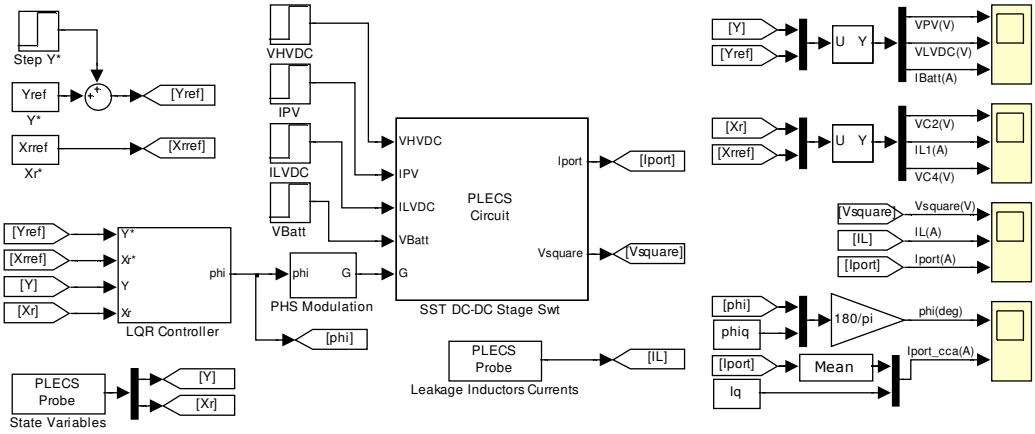


Fig. 72. QAB-based SST DC-DC stage Simulink model.

The simulation setup of the SST DC-DC stage makes extensive use of Simulink® sub-system blocks as well as PLECS® sub-circuit blocks. Fig. 72 through Fig. 75 show the details of the Simulink® model.

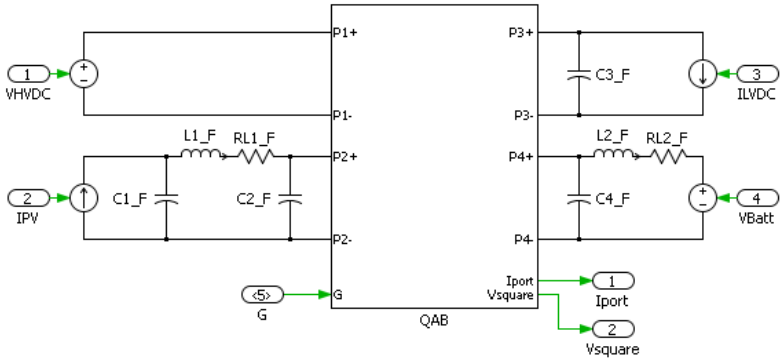


Fig. 73. QAB-based SST DC-DC stage PLECS circuit.

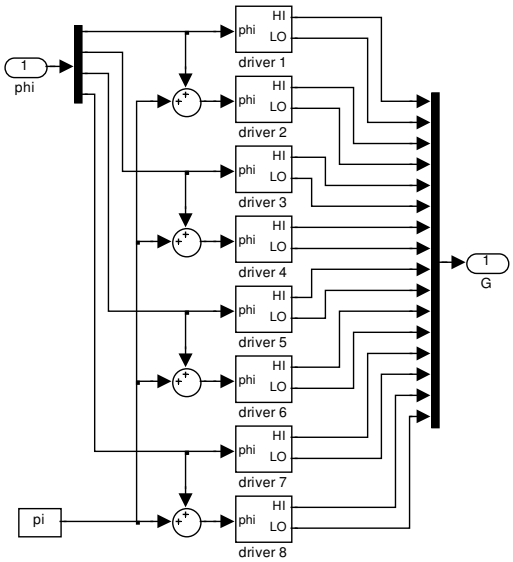


Fig. 74. PSM gate-pulse-generation Simulink sub-system.

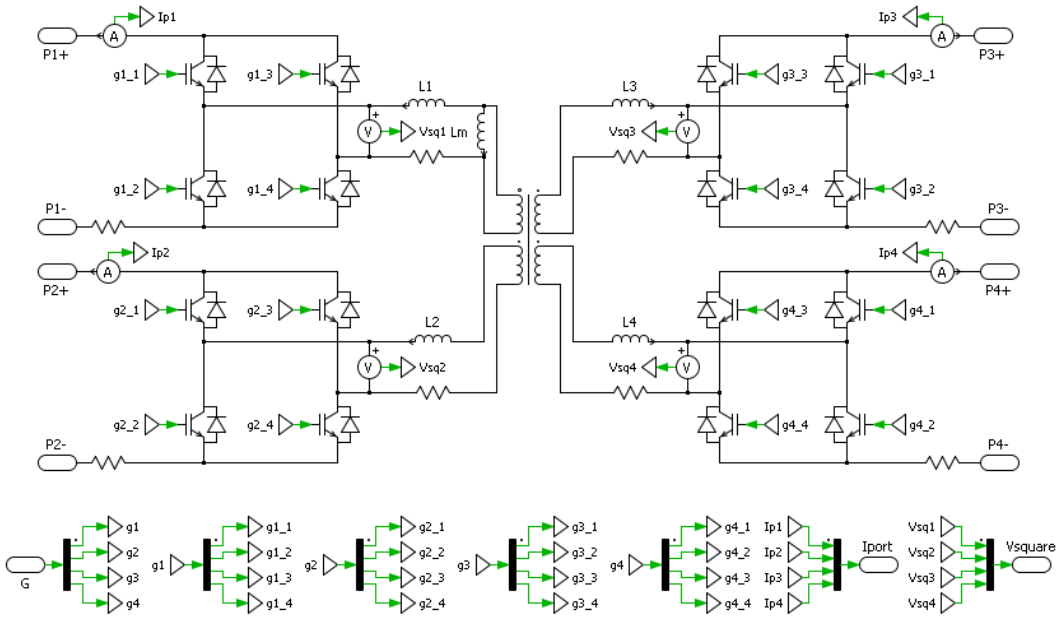


Fig. 75. QAB PLECS sub-circuit.

The QAB steady-state switching waveforms for ϕ_2 = -25°, ϕ_3 = -50° and ϕ_4 = -75° are shown in Fig. 76.

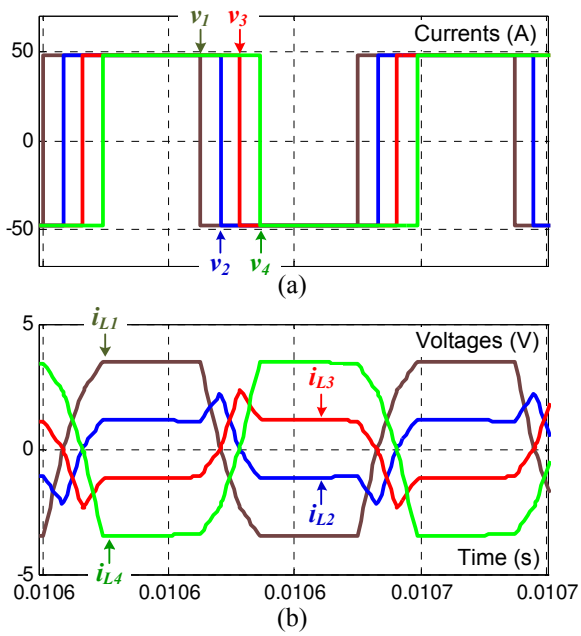


Fig. 76. Simulation Results: QAB steady-state switching waveforms for ϕ_2 = -25°, ϕ_3 = -50° and ϕ_4 = -75°.

1) SISO Controller

The simulation results corresponding to the SISO controller are presented in this section. The Simulink sub-model of the SISO controller is shown in Fig. 77 through Fig. 79.

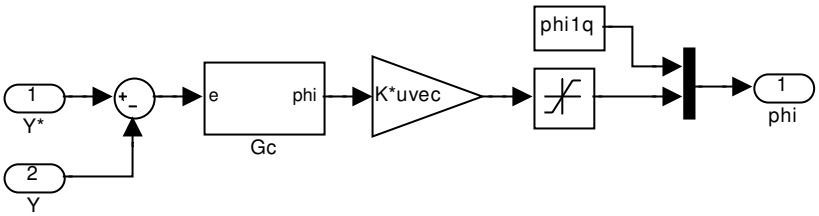


Fig. 77. SISO controller: Simulink sub-system.

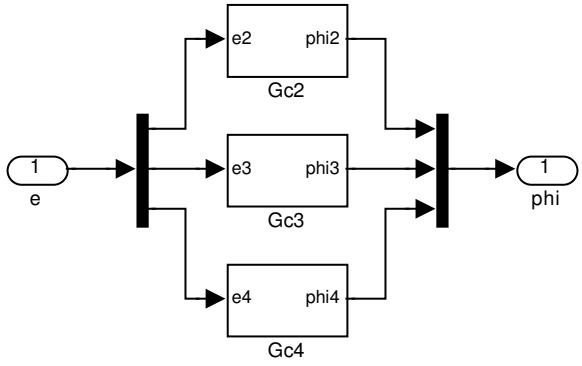


Fig. 78. SISO controller: Gc Simulink sub-system.

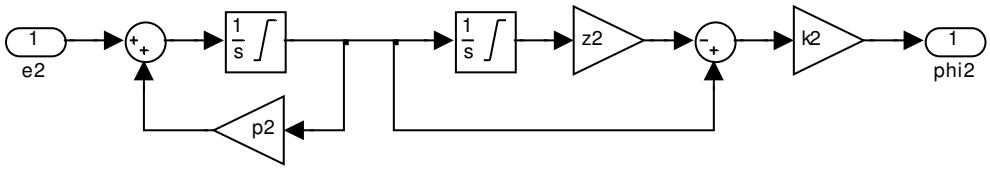


Fig. 79. SISO controller: Gc2 Simulink sub-system.

The transient response when K_B equals the identity matrix is seen in Fig. 80. It can be observed that, following the disturbance, the power variation is distributed among the remaining ports. This causes the PV voltage to dip. In steady state, the power is balanced by the HVDC link. When K_B is selected to transfer the power variation onto the HVDC port, the transient response is seen in Fig. 81. It can be observed that, the disturbance has little effect on the PV and battery ports. Fig. 82 shows the transient response when K_B is selected to transfer the power variation onto the battery port. As a result, the disturbance has little effect on the PV port and the rate of change of the HVDC current is minimized.

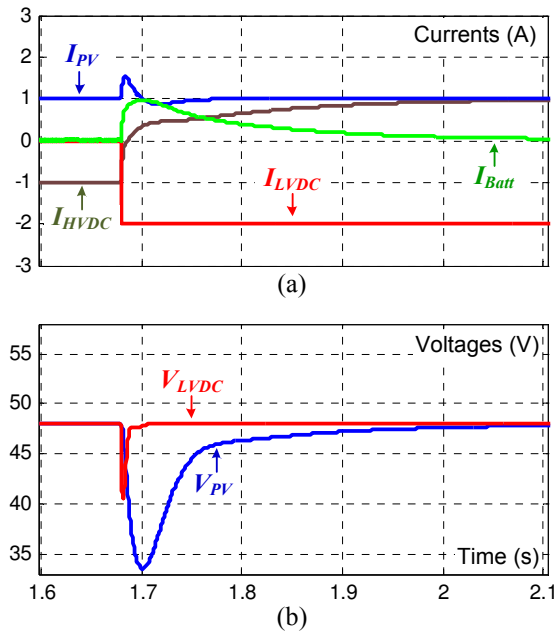


Fig. 80. SISO controller simulation results: SST DC-DC stage transient response to a step-load when K_B equals the identity matrix.

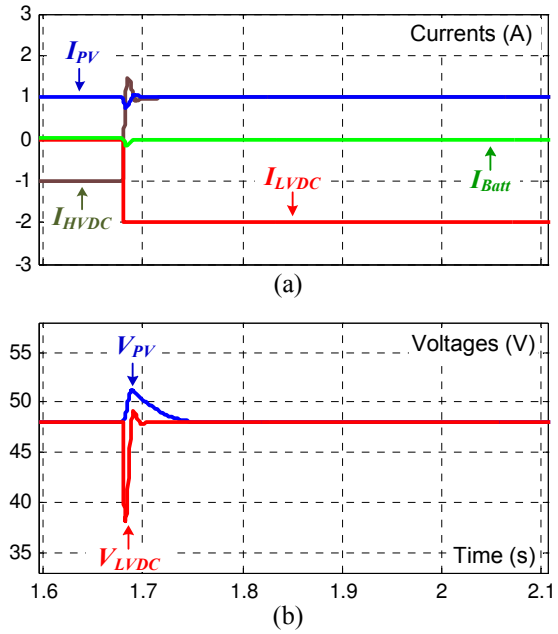


Fig. 81. SISO controller simulation results: SST DC-DC stage transient response to a step-load when the power variation is transferred onto the HVDC link.

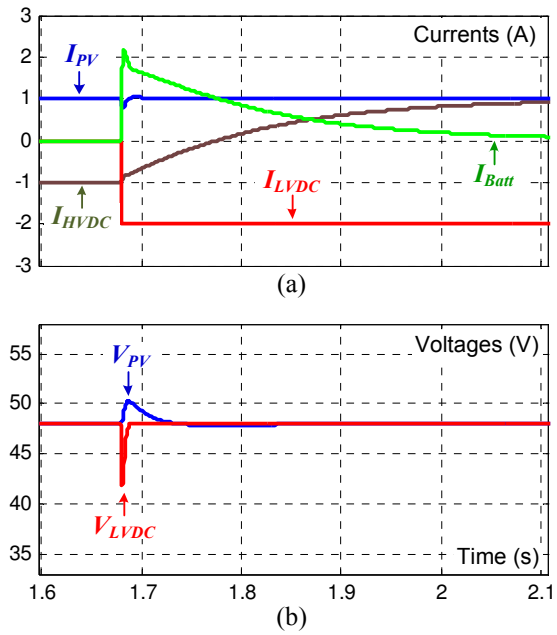


Fig. 82. SISO controller simulation results: SST DC-DC stage transient response to a step-load when the power variation is transferred onto the storage.

2) MIMO Controller

The simulation results corresponding to the MIMO controller are presented in this section. The Simulink sub-model of the MIMO controller is shown in Fig. 83.

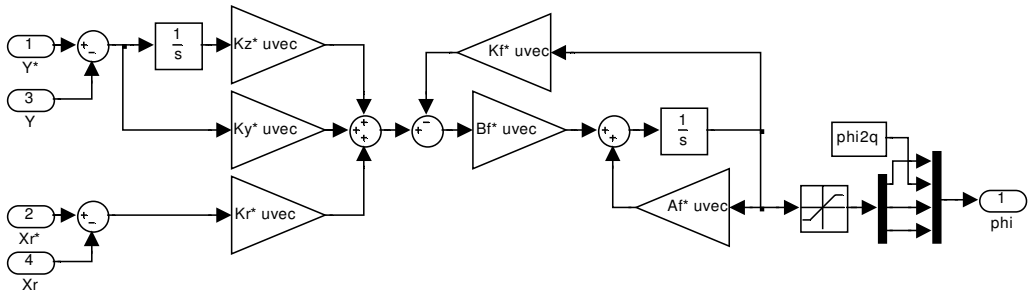


Fig. 83. MIMO controller: Simulink sub-system.

In order to verify the dynamic performance of the LQR controller, a step load current at the LVDC port is applied to the DC-DC stage. As observed in Fig. 84 and Fig.

85, the outputs show good reference command following under disturbances. It can be observed that settling times of the outputs when using MIMO controller are not far apart as opposed to those from the SISO controller.

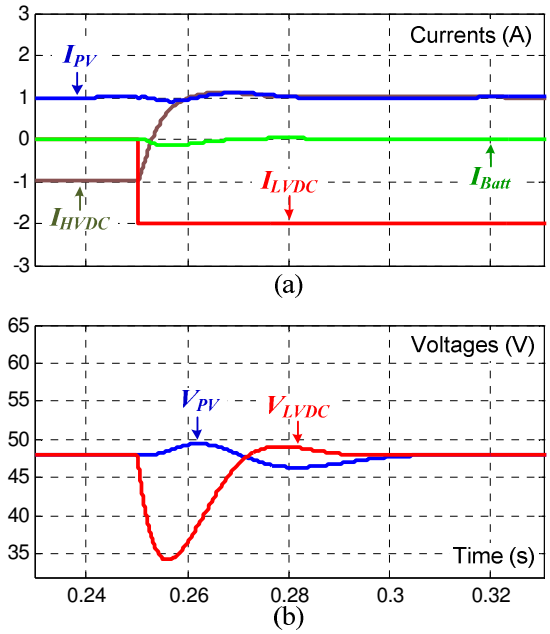


Fig. 84. MIMO controller simulation results: SST DC-DC stage transient response to an increasing step-load.

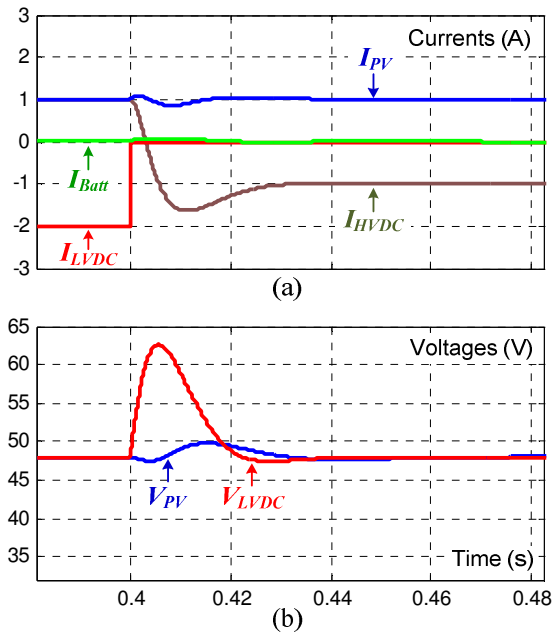


Fig. 85. MIMO controller simulation results: SST DC-DC stage transient response to a decreasing step-load.

B. SST AC-DC Stage

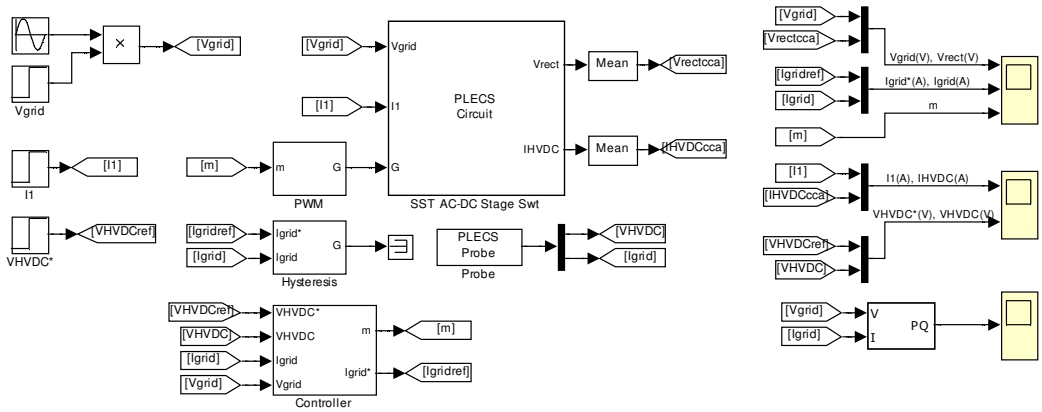


Fig. 86. SST AC-DC stage Simulink model.

The simulation setup of the SST AC-DC stage also makes extensive use of Simulink® sub-system blocks as well as PLECS® sub-circuit blocks. Fig. 86 through Fig. 89 show the details of its Simulink® model.

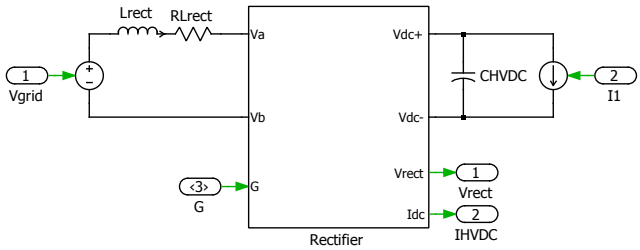


Fig. 87. SST AC-DC stage PLECS circuit.

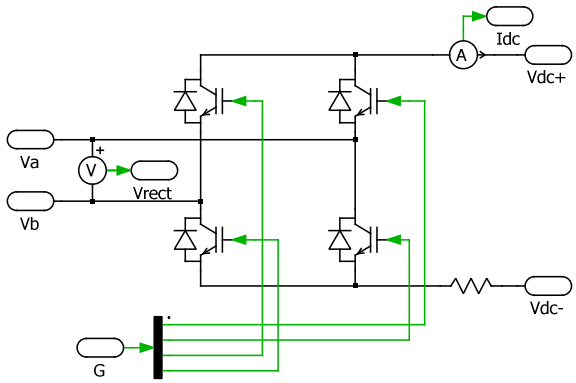


Fig. 88. Rectifier PLECS sub-circuit.

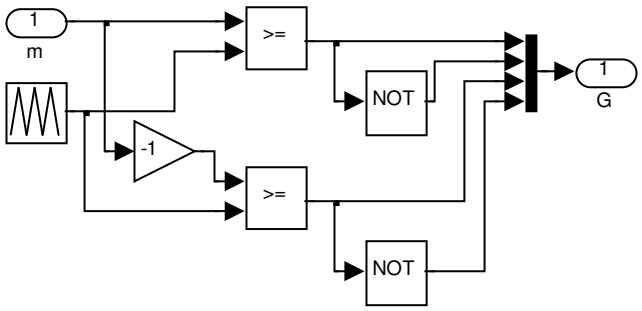


Fig. 89. PWM gate-pulse-generation Simulink sub-system.

In order to verify the dynamic performance of the designed cascaded controllers, a step load current at the HVDC port is applied to the AC-DC stage. As observed in Fig. 90, the output shows good reference command following under disturbances.

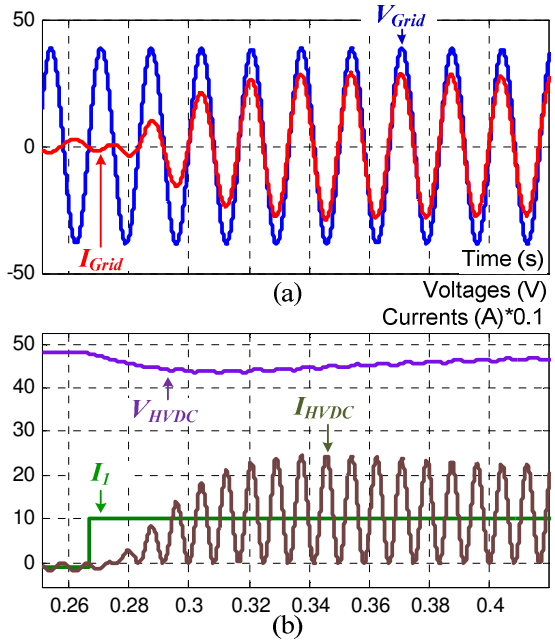


Fig. 90. Simulation results: SST AC-DC stage transient response to a step-load.

C. Complete SST

In this section, the simulation of the interconnected AC-DC and DC-DC stages is performed. In order to verify the dynamic performance of all the SST controls, a step load current is applied at the LVDC port of the SST. As observed in Fig. 91 and Fig. 92, the outputs show good reference command following under disturbances. However, the performance of the HVDC voltage regulation greatly improves when using the feedforward approach as seen in Fig. 92. As a consequence, the grid current does not overshoot.

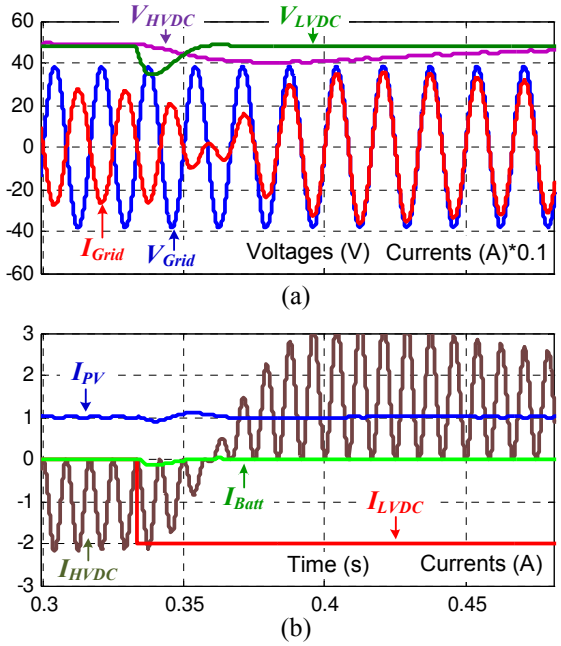


Fig. 91. Simulation results: SST transient response to a step-load without P1 feedforward.

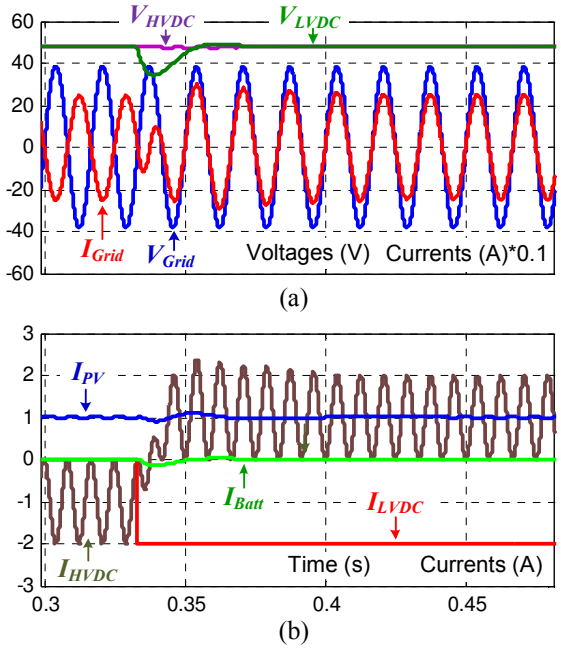


Fig. 92. Simulation results: SST DC-DC stage transient response to a step-load with P1 feedforward.

VII EXPERIMENTAL RESULTS

The present chapter shows the results of the hardware implementation of the SST topology introduced in chapter II. The system features the controllers designed in chapters IV and V. The prototype was developed in the Power Electronics Lab at ASU to verify the dynamic performance of all the controllers on the actual plant.

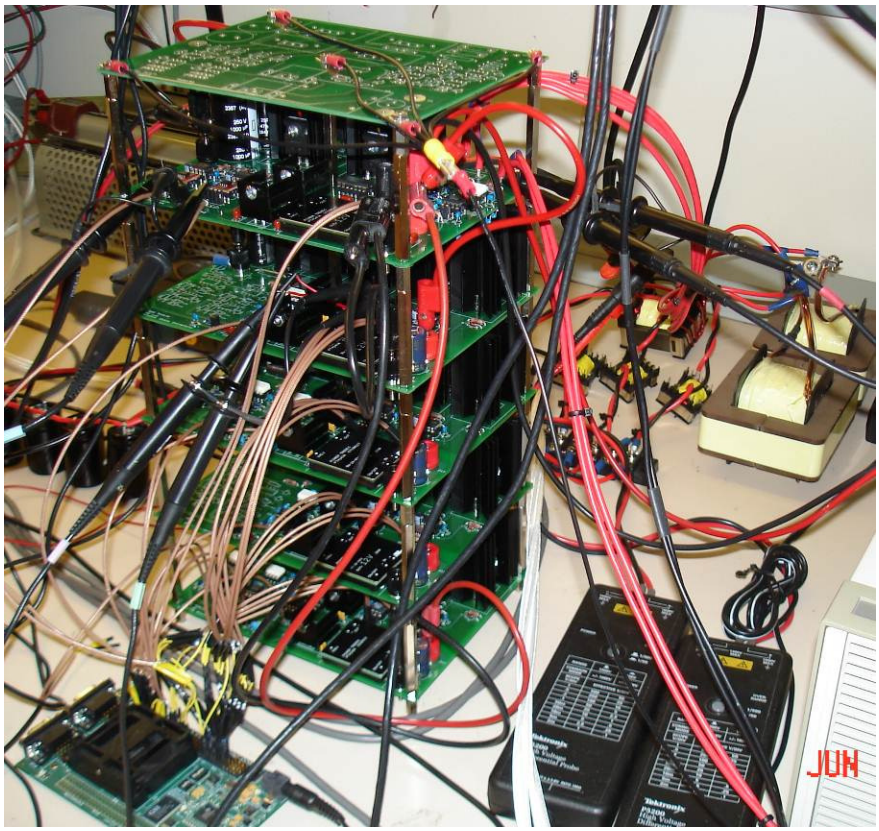


Fig. 93. SST hardware implementation.

The developed prototype seen in Fig. 93 has been originally designed with a rated power of 1KW with a switching frequency of 20KHz. The DC voltage is set to 48V for each QAB port; however, the HF transformer turns ratio can be modified for different voltage ratings. The grid voltage is stepped down to 28Vrms before connecting it to the rectifier.

The controls are implemented on a Texas Instruments™ TMS320F28335 digital signal processor (DSP). Target Support Package™ block-set for MATLAB™/ Simulink® is used to generate the C-code for the DSP which is installed on a Zdsp™ F28335 board from SPECTRUM DIGITAL, whereas TI Code Composer Studio™ (CCS) is used to load the C-code onto the DSP.

A. SST DC-DC Stage

Fig. 94 through Fig. 96 show the structure of the SST DC-DC stage controller to generate the code to be loaded into the DSP.

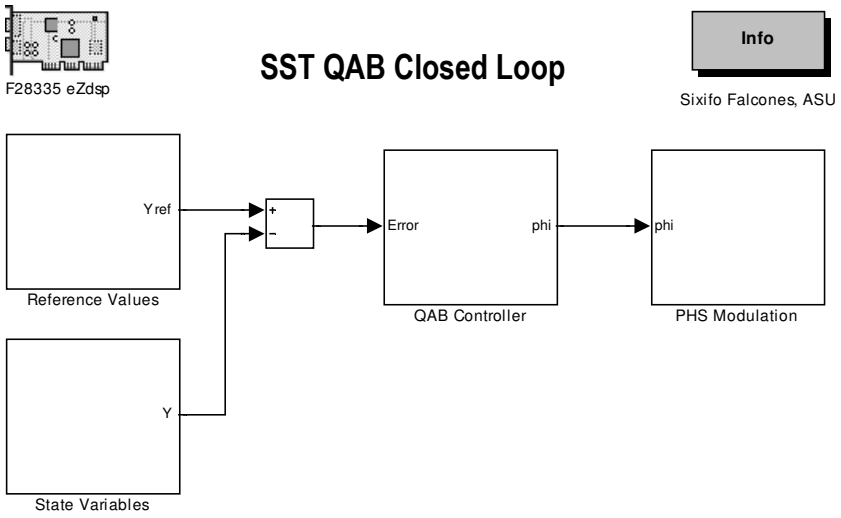
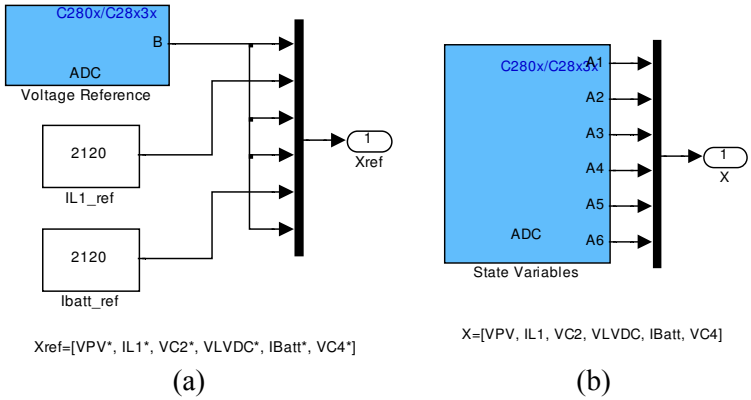


Fig. 94. DSP program defined in a Simulink model.



(a) (b)

Fig. 95. Acquisition of (a) reference and (b) feedback signals.

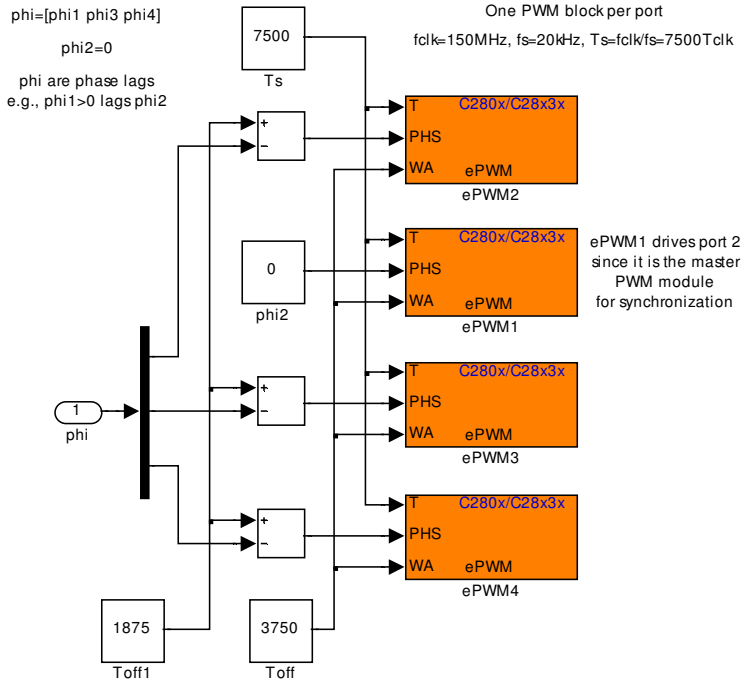
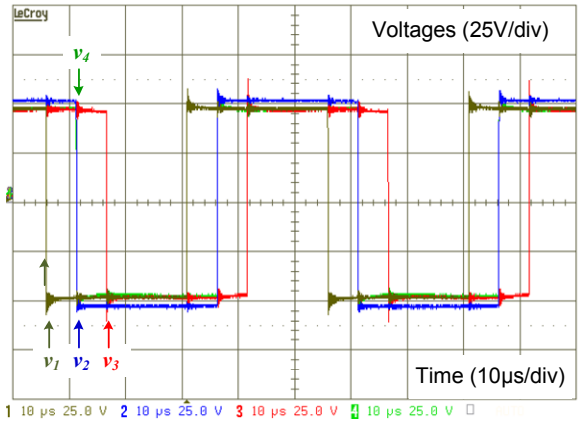
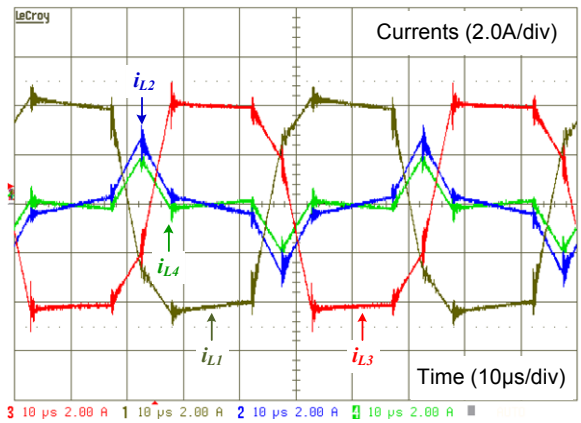


Fig. 96. Generation of PSM pulses.

The measured QAB steady-state switching waveforms for ϕ_2 = -38°, ϕ_3 = -76° and ϕ_4 = -38° are shown in Fig. 97.



(a)



(b)

Fig. 97. Experimental results: QAB steady-state switching waveforms for ϕ_2 = -38°, ϕ_3 = -76° and ϕ_4 = -38°.

1) SISO Controller

Fig. 98 shows the model of the SISO controller to generate the code to be loaded into the DSP. For the verification of the close-loop operation, a step current at the LVDC link is applied. The transient response when K_B equals the identity matrix is seen in Fig. 99, whereas the transient responses when K_B is selected to transfer the power variation onto the HVDC port and to the battery port are seen in Fig. 100 and Fig. 101, respectively.

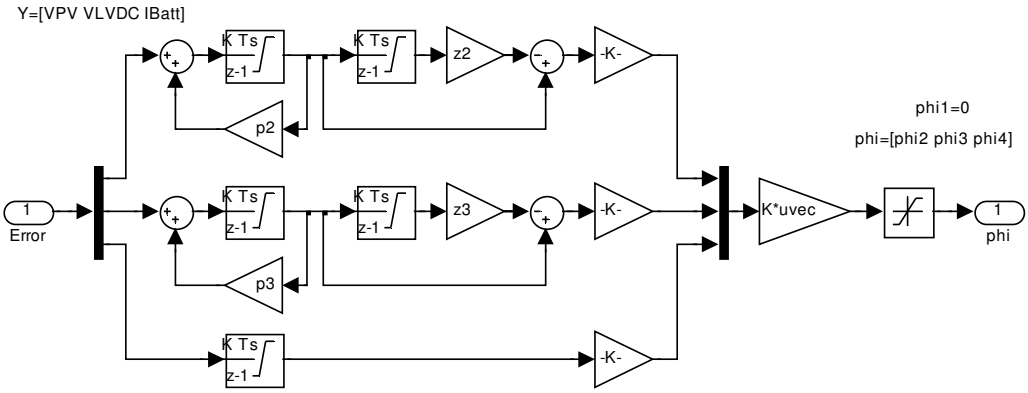
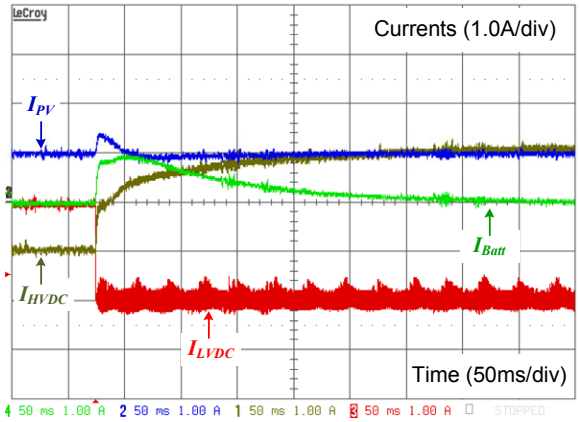
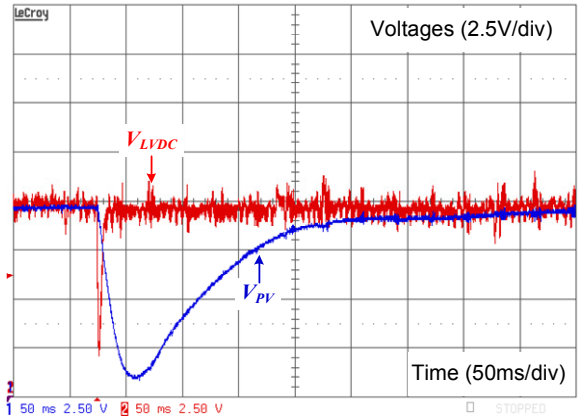


Fig. 98. Implementation of SISO controller with Simulink standard blocks.

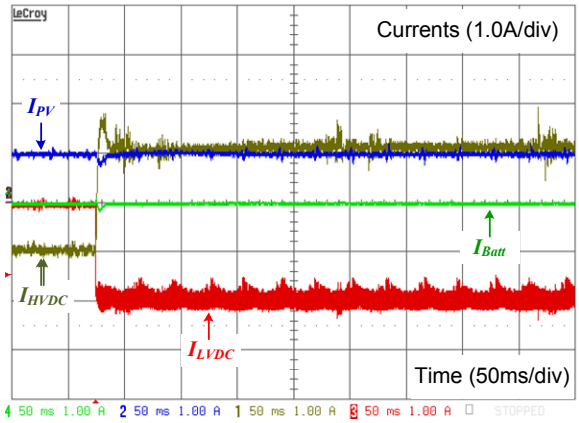


(a)

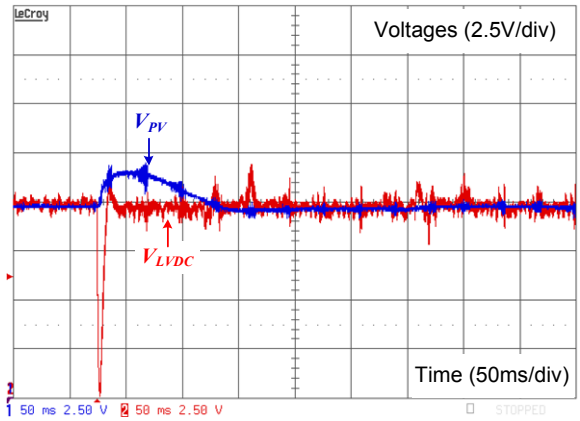


(b)

Fig. 99. SISO controller simulation results: SST DC-DC stage transient response to a step-load when K_B equals the identity matrix.

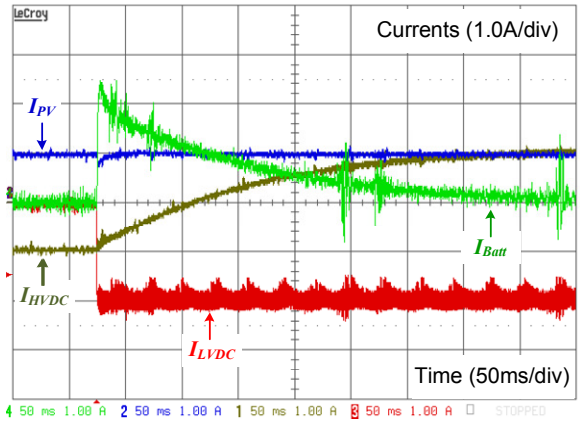


(a)

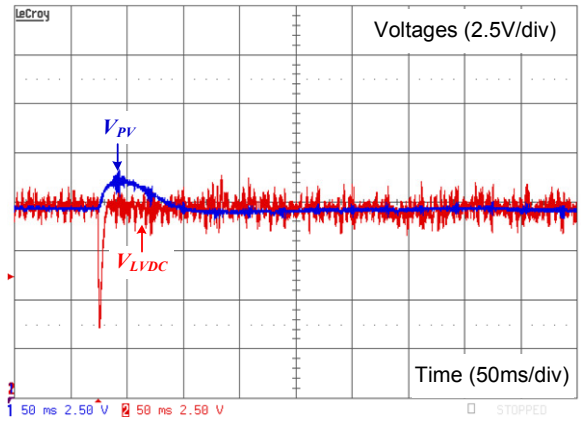


(b)

Fig. 100. SISO controller simulation results: SST DC-DC stage transient response to a step-load when the power variation is transferred onto the HVDC link.



(a)



(b)

Fig. 101. SISO controller simulation results: SST DC-DC stage transient response to a step-load when the power variation is transferred onto the storage.

The above experimental results for the SISO controller closely match those from the simulation results in Fig. 80 though Fig. 82, thus validating them.

2) MIMO Controller

Fig. 102 shows the model of the LQR controller to generate the code to be loaded into the DSP. For the verification of the close-loop operation, a step current at the LVDC link is applied. The transient responses are seen in Fig. 103 and Fig. 104.

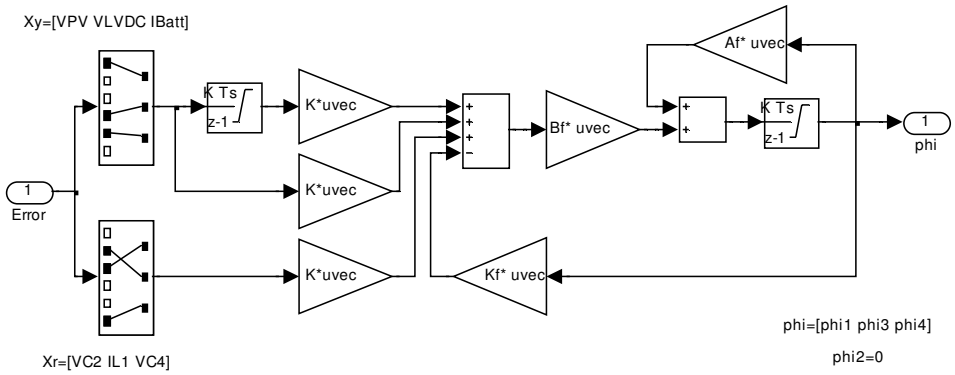
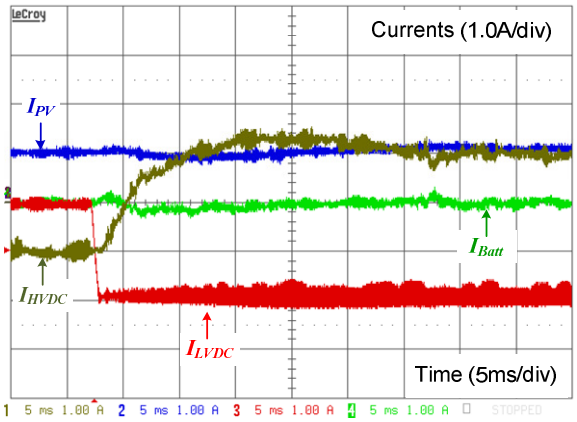
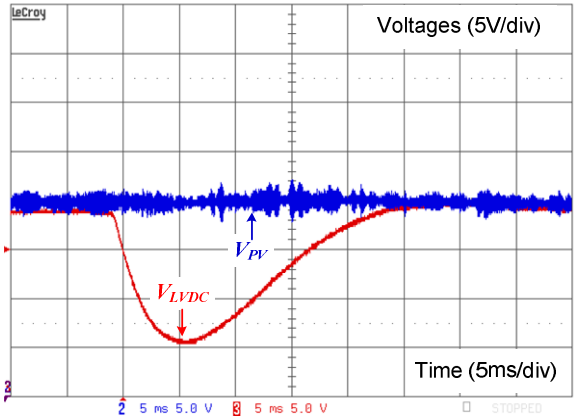


Fig. 102. Implementation of LQR controller with Simulink standard blocks.

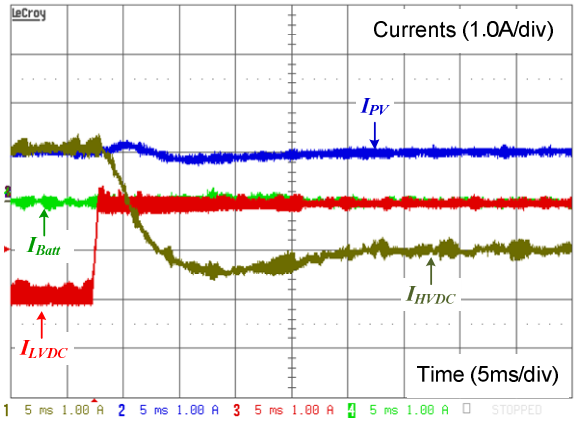


(a)

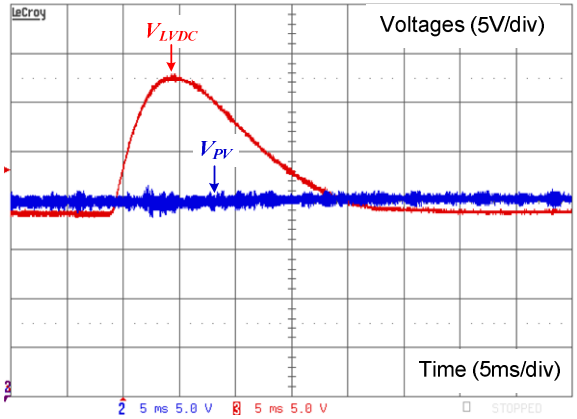


(b)

Fig. 103. MIMO controller simulation results: SST DC-DC stage transient response to an increasing step-load.



(a)



(b)

Fig. 104. MIMO controller simulation results: SST DC-DC stage transient response to a decreasing step-load.

The above experimental results for the MIMO controller closely match those from the simulation results in Fig. 84 and Fig. 85, thus validating them.

B. SST AC-DC Stage

Fig. 105 through Fig. 107 show the structure of the SST AC-DC stage controller to generate the code to be loaded into the DSP.

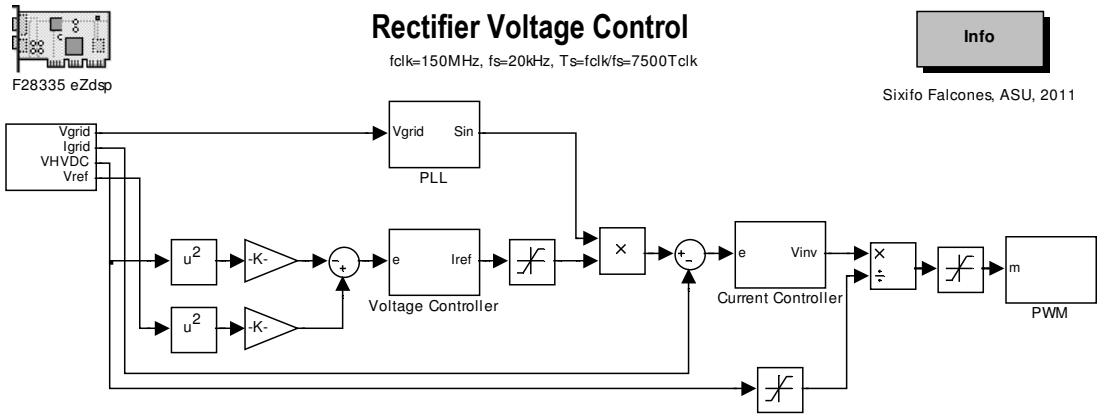


Fig. 105. SST AC-DC stage DSP program defined in a Simulink model.

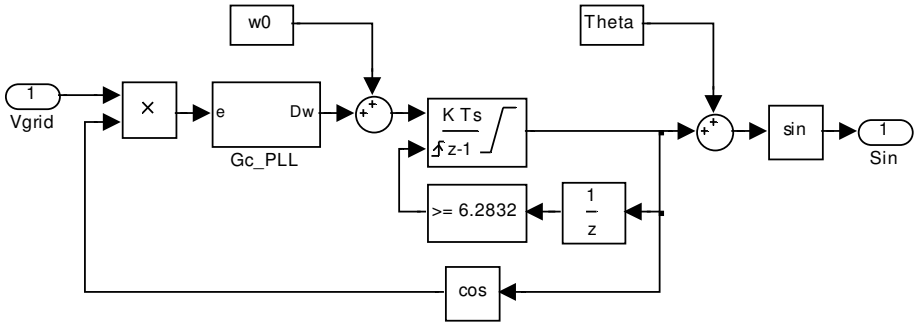


Fig. 106. PLL sub-system defined in a Simulink model.

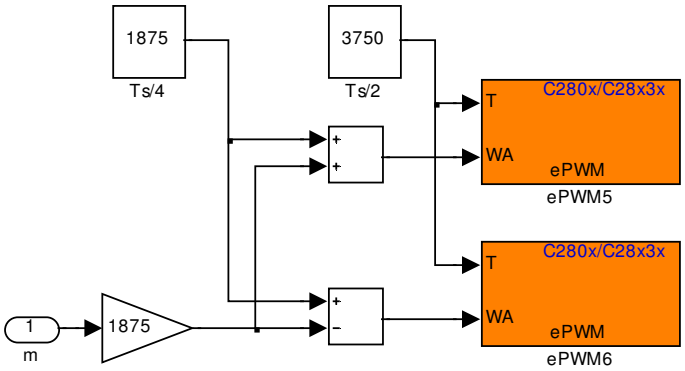


Fig. 107. PWM sub-system defined in a Simulink model.

For the verification of the performance of the cascaded controllers in close-loop operation, a step current at the HVDC link is applied. The transient responses are seen in Fig. 108 and Fig. 109.

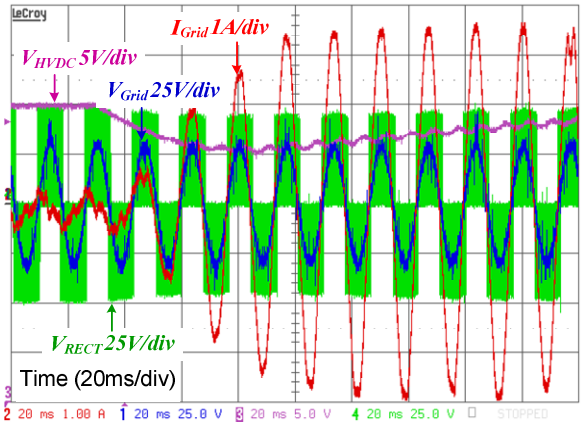


Fig. 108. Experimental results: SST AC-DC stage transient response to an increasing step-load.

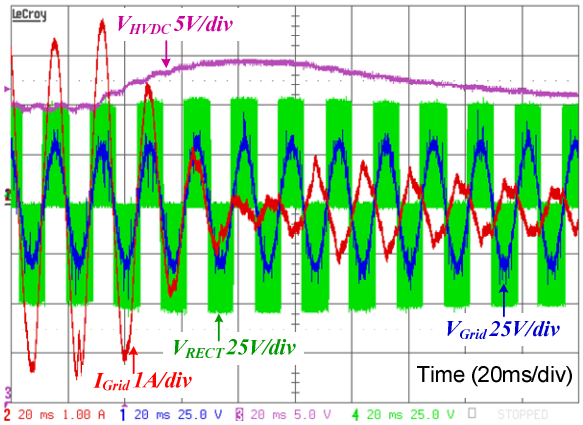
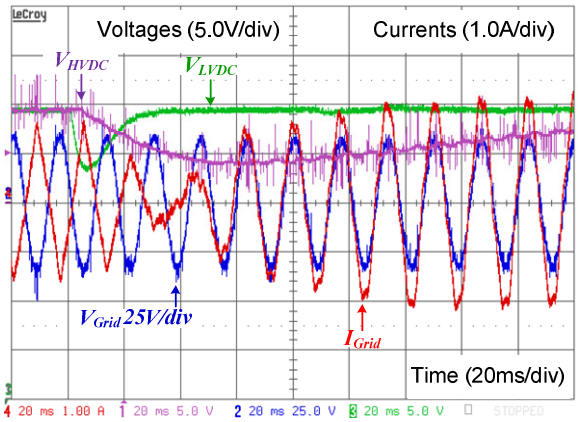


Fig. 109. Experimental results: SST AC-DC stage transient response to a decreasing step-load.

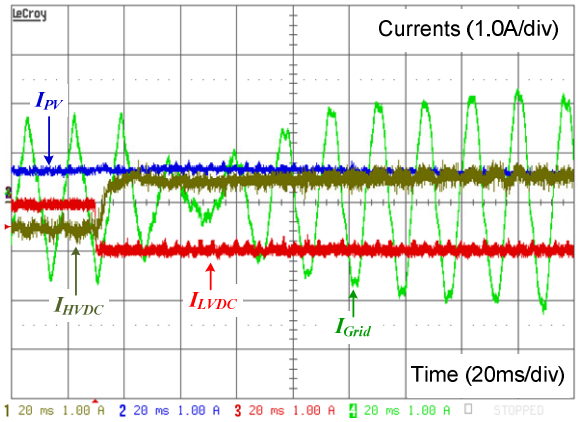
The scale of HVDC voltage is reduced to observe its transient response. The experimental results in Fig. 108 validate the simulation results in Fig. 90.

C. Complete SST

For the verification of the performance of all the SST controllers in close-loop operation, a step current at the LVDC link is applied while current is being injected at the PV port. The transient responses are seen in Fig. 110. Fig. 110 (a) shows how the grid current changes its phase in order to regulate the HVDC voltage.



(a)



(b)

Fig. 110. Experimental results: Complete SST transient response to an increasing step-load.

VIII CONCLUSION

A SST topology based on a quad-active-bridge (QAB) converter which provides isolation for the load, as well as DG and storage has been proposed herein. A gyrator-type large-signal average model has been developed for a general multi-active-bridge (MAB) converter and used to significantly speed up the simulation of the DC-DC stage of the QAB-based SST. Additionally, the expressions to determine the power rating of an MAB port have been derived and used to determine the power rating of the QAB ports considering the operating characteristics of the SST application.

Two control approaches have been followed to design the controls for the SST DC-DC stage: SISO and MIMO. A control technique that complements the SISO controller and takes into account the cross-coupling characteristics of the QAB converter has been introduced herein. This technique allows improving the dynamic performance of the HVDC of the SST. Alternatively, a full-state-feedback MIMO controller as the LQR has also been designed. This type of controller allows the access to all state variables, thus enabling a feedforward technique to enhance the performance of the HVDC voltage regulation on the AC-DC stage. The power demanded by the QAB is estimated and fed into the AC-DC stage controller. This is a simple yet effective approach that helps minimize the interaction between the two SST stages.

The dynamic performance of the designed QAB control loops based on the proposed SISO technique as well as the MIMO approach are verified through extensive simulation of the SST average and switching models. When enabling the feedforward technique for the operation of the complete SST, the HVDC voltage regulation significantly improves. The experimental results show that the transient responses for each control strategy match those from the simulations results thus validating them.

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