Self-Heating Effects In Nanowire Transistors

by

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ABSTRACT

One of the challenges in future semiconductor device design is excessive rise of power dissipation and device temperatures. With the introduction of new geometrically confined device structures like SOI, FinFET, nanowires and continuous incorporation of new materials with poor thermal conductivities in the device active region, the device thermal problem is expected to become more challenging in coming years.

This work examines the degradation in the ON-current due to self-heating effects in 10 nm channel length silicon nanowire transistors. As part of this dissertation, a 3D electrothermal device simulator is developed that self-consistently solves electron Boltzmann transport equation with 3D energy balance equations for both the acoustic and the optical phonons. This device simulator predicts temperature variations and other physical and electrical parameters across the device for different bias and boundary conditions. The simulation results show insignificant current degradation for nanowire self-heating because of pronounced velocity overshoot effect. In addition, this work explores the role of various placement of the source and drain contacts on the magnitude of self-heating effect in nanowire transistors.

This work also investigates the simultaneous influence of self-heating and random charge effects on the magnitude of the ON current for both positively and negatively charged single charges. This research suggests that the self-heating effects affect the ON-current in two ways: (1) by lowering the barrier at the

source end of the channel, thus allowing more carriers to go through, and (2) via the screening effect of the Coulomb potential.

To examine the effect of temperature dependent thermal conductivity of thin silicon films in nanowire transistors, Selberherr's thermal conductivity model is used in the device simulator. The simulations results show larger current degradation because of self-heating due to decreased thermal conductivity .

Crystallographic direction dependent thermal conductivity is also included in the device simulations. Larger degradation is observed in the current along the [100] direction when compared to the [110] direction which is in agreement with the values for the thermal conductivity tensor provided by Zlatan Aksamija.

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CHAPTER 1

INTRODUCTION

Electronics industry is the largest industry in the world since 1998 with global sales of over 1 trillion dollars. With ever increasing innovation in electronics industry, it is expected that this industry will grow even faster in the next decade [1]. The core of the electronic industry owes its success to semiconductor industry and it all began at Bell Laboratories with the invention of the bipolar transistor in 1947 [2]. The grown junction transistors were later realized with the introduction of single-crystalline materials. The silicon based bipolar integrated circuits (ICs) were invented in 1959 with the advancement of reliable and high quality oxide growth on silicon wafers and introduction of planar process. Polysilicon gate technology that allowed self-alignment of the gate to the source/drain of the device and the low interface-state density of the Si/SiO_2 material system and further refinements in the understanding of surface effects eventually led the migration from bipolar devices to field-effect devices. Kahng and Atalla [1] introduced Metal-oxide-semiconductor field-effect transistor (MOSFET) in 1960, thus opening the door for semiconductor industry revolution. The introduction of complementary metal–oxide–semiconductor devices (CMOS) in 1968 resulted in a significant reduction in power dissipation and the overlap capacitance, improving the overall frequency/switching performance of the integrated circuits. Since the invention of the point-contact bipolar transistor in 1947, the number and

diversity of different semiconductor devices have grown greatly as sophisticated technology, new materials with their distinctive properties, and broadened knowledge of the underlying physical processes have been applied to the making and innovation of new devices that have literally changed the world.

Innovations of heterostructures—from heterostructure bipolar transistors to lasers by Professor Herbert Kroemer [3] earned him a Nobel Prize in Physics in 2000 and have paved the way for novel heterostructure devices including those in silicon. A wide variety of ingenious devices have been made possible because of the unique properties of the variety of semiconductor materials. To date, there are about 60 major devices, with over 100 device variations related to them. Table 1.1 [1] lists most of the basic semiconductor devices invented and used over the past century with the date of their introduction.

TABLE 1.1

MAJOR SEMICONDUCTOR DEVICES

- 1874: Metal-semiconductor contact
- 1907: Light emitting diode
- 1947: Bipolar junction transistors (BJT)
- 1954: Solar cell
- 1957: Heterojunction bipolar transistor
- 1958: Tunnel diode
- 1959: Integrated circuits

- 1960: Field-effect transistors (FETs)
- 1962: Semiconductor lasers.
- 1966: Metal-semiconductor FET
- 1967: Nonvolatile semiconductor memory
- 1974: Resonant tunneling diode (RTD)
- 1980: Modulation (MOD) FET
- 1994: Room-temperature single-electron memory cell (SEMC)
- 2001: 15 nm MOSFET
- 2010: silicon-based optical data connection (Intel Corporation)

The MOSFET and related integrated circuits now constitute about 90% of the semiconductor device market [1]. The modern semiconductor microelectronics industry is driven by the continuous scaling of field-effect transistors making devices smaller, faster and cheaper. Indeed, the single and most important factor driving the continuous device improvement has been the semiconductor industry's relentless effort to reduce the cost per function on a chip. The way this is done is to put more devices on a chip while either reducing manufacturing costs or holding them constant. This leads to three methods of reducing the cost per function. The first is transistor scaling, which involves reducing the transistor size in accordance with some goal, i.e. by keeping, for example, the electric field constant from one generation to the next. With smaller transistors, more can fit into a given area than in previous generations. The second method is circuit

cleverness, which is associated with the physical layout of the transistors with respect to each other. If the transistors can be packed into a tighter space, then more devices can fit into a given area than before. The third method is to make a larger die where more devices can be fabricated.

1.1 Device Scaling

The most important concern in device engineering is the aforementioned method of scaling, which has paved the way for a continued increase and improvements in system performance and motivated the Semiconductor Industry Association (SIA) [4] to bring out roadmaps for semiconductor technology since 1992. These roadmaps correspond to a worldwide consensus outlook of the main trends in the semiconductor industry spanning across 15 years into the future, taking history as a guide. Recent roadmaps [5] incorporate participation from the global semiconductor industry and research organization, including the United States, Europe, Japan, Korea, and Taiwan. They basically assert the aspiration of the industry to continue with Moore's law [6], which is often most simply stated as the doubling of transistor performance and quadrupling of the number of devices on a chip every three years. Indeed, the phenomenal progress signified by Moore's law has been achieved through scaling of the metal-oxide-semiconductor field effect transistor (MOSFET) from larger to smaller physical dimensions. Scaling of CMOS technology has progressed relentlessly from a line width of 10 μm in the 1970's to the present day line-width of 22 nm. There are two important features that are helping this become possible [7]: (1) Continued and constant

improvements in lithography for device scaling, as described by Dennard et al. [8] . For 22nm technology, Intel is using 193nm lithography steppers. At the Berkeley labs extreme ultraviolet (EUV) lithography at a wavelength of 13nm is currently in use and shows the active quest of advanced lithography techniques and the relentless devotion to scaling. (2) The introduction of new materials and device structures has led the effort of device scaling to improve performance. Substantial effort has been put to integrate new materials in the integrated circuits while ensuring both manufacturability and reliability of the devices. Intel 45nm high-k metal gate silicon technology helped to dramatically increase processor energy efficiency, thus equating to more powerful computing experiences and greater flexibility of design. Also the introduction of silicon-germanium in CMOS technology is another example of using new materials to boost performance while the devices are scaled.

The device size in conventional silicon MOSFET is scaled in all dimensions which results in smaller oxide thickness, junction depth, channel length, channel width and isolation spacing. The current state-of-the-art process technology is 22 nm and it marks the third generation of high-k metal gate transistors produced by Intel Corporation. But even smaller dimensions transistors are expected in the very near future. The SIA is predicting the continuous exponential scaling of silicon MOSFETs and integrated circuits until the year 2016, when devices with 15 nm features become commercially available. Intel Corporation also recently demonstrated transistors with physical gate length of 10 nm [9]. These smaller

devices promise to serve the basis for the most advanced integrated circuit chips containing more than one trillion (> 10^{12}) devices. One of the benefits of this device miniaturization is reduced unit cost per function. In case of dynamic random access memory (DRAM) circuits, the cost per bit of memory chips has halved every two years for successive generations [1]. The intrinsic device switching time also decreases as devices are scaled. We see a device speed increase by four orders of magnitude since 1959. IC functional throughput rates increase is a direct result of higher switching speed. This will enable digital ICs to execute data processing and numerical calculation at terabit-per-second rates in the near future. Devices consume less power as they become smaller. As a result, device scaling also reduces the energy required for each switching function. Since 1959, the energy dissipation per logic gate has decreased by over one million times [1].

But this exponential growth in the complexity of integrated circuits which resulted in a hundred-million-fold increase in transistor count per chip over the last five decades is finally facing its barrier. Challenges faced in the past have been overcome because of the intensive hard work of researchers and scientists but this time the barriers to device scaling appear to be more difficult and have already forced to apply new strategies on the design of future devices. Many critical device dimensions like transistor gate length and dielectric thickness are reaching physical limitations. It is extremely challenging to maintain dimensional integrity at the limits of scaling. As the feature sizes approach the wavelength of

ultraviolet light, manufacturing processes like lithography become particularly difficult. Controlling the oxide thickness is very challenging as the oxide is made up of just a few monolayers. The dielectric scaling issue is overcome for now by introducing hafnium based dielectric from 45 nm technology. In general, the processes are now requiring atomic-layer precision. There are also some basic device issues in addition to the processing issues. It requires clever innovations to avoid barriers due to the fundamental physics that constrains the conventional MOSFET devices to scale beyond 15nm technology. Some of the basic limits [10] are: (1) quantum-mechanical direct band-to-band tunneling of carriers through the thin gate oxide; (2) quantum-mechanical tunneling of carriers from source to drain and from drain to the substrate of the MOSFET; (3) control of the density/number and location of the dopant atoms in the MOSFET channel and source/drain regions; (4) voltage-related effects such as subthreshold swing, built-in voltage and minimum logic voltage swing; (5) Short-channel effects such as threshold voltage roll-off and drain-induced barrier lowering (DIBL); (6) hot carriers effect reducing device reliability; (7) the reduction of the source/drain junction depth resulting in increase in the parasitic resistance, and (8) other application-dependent power-dissipation limits. There are more challenges like sustaining linearity, low noise figure, power-added-efficiency and transistor matching for analog/RF applications. According to quantum mechanical principles and restated by George Bourianoff of Intel Corporation, heat dissipation will eventually limit any logic device using an electronic charge [11].

An analysis has been done on an arbitrary switching device which is made up of a single electron in a dual quantum well and separated by an energy barrier and operating at room temperature. The investigation shows that the amount of power pulled off the material surface eventually limits device density and switching frequency. For passive cooling techniques with no active or electro thermal elements, this limit is about 100 watts per square centimeter. These basic challenges to device scaling have led to gloomy predictions of the imminent end of technological advances in the semiconductor industry and at the same time have increased interest in advanced alternative technologies that rely on something other than the electronic charge – like spin or photon fields –to store computational state.

1.2 Need for Alternative Device Technologies

Many semiconductor researchers and scientists around the world now think that the pace of performance improvement of conventional CMOS devices, as achieved through conventional scaling, will slow down in very near future. Many advocate a focus on novel and exploratory devices, low-temperature operation, and increased functional integration as means of sustaining the industry trend of system performance improvement. It is suggested that the current rate of transistor performance improvement can be sustained for another 10 to 15 years, but only through the development and introduction of new materials and new transistor

structures. In addition, a major improvement in lithography will be required to continue size reduction.

A figure of merit for MOSFETs for unloaded circuits in digital integrated circuits is the so-called CV/I time delay [10], where C is the gate capacitance, V is the voltage swing, and I is the current drive of MOSFET. To drive loaded circuits, the most important parameter is the current drive of the MOSFET. Considering both the CV/I metric and the benefits of a large current drive, it is observed that device performance can be improved by: (1) inducing larger charge density for a given gate voltage drive; (2) enhancing the carrier transport by improving the mobility, saturation velocity, or ballisticity; (3) scaling device further by improvement of lithography, and (4) decreasing parasitic capacitances and parasitic resistances by self-aligned and raised source/drain structures. To take advantage of these opportunities, there are basically two technological options: new materials and novel device structures. In many cases, the introduction of a new material requires the use of a new device structure, or vice versa.

i. High-k Metal Gate and Strained Silicon, SiGe Technology

To engineer devices beyond current scaling limits, IC companies are pushing the planar, bulk silicon CMOS design while simultaneously implementing alternative gate stack materials (high-k dielectric [12] and metal gates), band engineering methods (using strained Si [13], [14], [15] or SiGe [16]), and alternative transistor structures.

Intel has led the industry in transistor gate dielectric scaling using silicon dioxide (SiO_2) for seven logic-process generations over the last 15 years. But as transistors shrink, leakage current can increase. Managing that leakage is crucial for reliable high-speed operation, and is becoming an increasingly important factor in the chip design. Intel has made a significant breakthrough in solving the chip power problem, identifying a new "high-k" (Hi-k) material called hafnium to replace the transistor's silicon dioxide gate dielectric, and new metals to replace the polysilicon gate electrode of NMOS and PMOS transistors. These new materials, along with the right process recipe, reduce gate leakage more than 100-fold, while delivering record transistor performance. To achieve this milestone for the 45nm node, Intel silicon research evaluated 100's of material combinations to find the right starting point for development.

High-k stands for high dielectric constant, a measure of how much charge a material can hold. Different materials similarly have different abilities to hold charge. Air is the reference point for this constant and has a "k" of one. "High-k" materials, such as hafnium dioxide (HfO2), zirconium dioxide (ZrO2) and titanium dioxide (TiO2) inherently have a dielectric constant or "k" above 3.9, the "k" of silicon dioxide. The dielectric constant also relates directly to transistor performance. The higher "k" increases the transistor capacitance so that the transistor can switch properly between and "on" and "off" states, with very low current when off yet very high current when on.

After years of research, Intel identified the right high-k material and the right type of gate electrode materials to achieve record performance for both NMOS and PMOS technologies. By moving to a new high-k material, Intel was able to keep the drive current at the same level as with older materials—and overcome the leakage. The entire semiconductor industry is struggling with the heat of chips, which increases exponentially as the number of transistors increase. Leakage control via new high-k materials is one of many steps toward making transistors run cooler. Because high-k gate dielectrics can be several times thicker, they reduce gate leakage by over 100 times. As a result, these devices run cooler. At the same time, Intel has engineered and demonstrated metal gate electrodes—which sit on top of the gate dielectric—that are compatible with high-k dielectrics. This shift to a new material is one of the most significant in the evolution of the metal-oxide silicon (MOS) transistor, which has had a silicon dioxide dielectric gate since its introduction in the 1960s.

Intel made a significant breakthrough in the 90nm process generation by introducing strained silicon on both the N and PMOS transistors. NMOS strain was introduced by adding a high-stress layer that wrapped around the transistor (a process sometimes named CESL, or contact etch-stop layer after the most common layer used for the stressor). PMOS strain was introduced by replacing the conventional source/drain region with strained SiGe (a process often called embedded-SiGe or e-SiGe). The addition of strain in both NMOS and PMOS

enhanced the channel mobility, resulting in improved drive current (and improved performance) for both NMOS and PMOS.

Strain causes the Si atoms to stretch apart by ~1%. Strain provides mobility improvement in two ways. The first is by reducing the effective mass of the silicon. The second is by moving carriers to places with good effective mass (or reducing movement of carriers to places with bad effective mass).

The way this works for electrons is as follows. For a MOSFET built on the typical (100) surface, <110> channel orientation, the eqi-energy surfaces of the conduction band are oriented with two "out-of-plane" ellipsoids with good (low) effective mass and four "in-plane" ellipsoids with poor (high) effective mass. When the MOSFET is strained, the energy bands split, with the "out-of-plane" ellipsoids having lower energy. The electrons move from the high energy "in-plane" ellipsoids (with the poor effective mass) to the low energy "out-of-plane" ellipsoids (with the good effective mass). When the stress values get over ~2 GPa, the majority of the electrons are in the ellipsoids with the lowest effective mass. Low effective mass means better mobility and higher drive current for better performance. In addition, the splitting of the bands reduces scattering. Lower scattering means better mobility and higher drive current for better performance.

The way this works for holes is as follows. For a MOSFET built on the typical (100) surface, <110> channel orientation, the eqi-energy surfaces of the valence band form an unusually shaped surface, with four "wings" and four "feet." When the MOSFET is uniaxially strained, the shear components warp the bands to form

an optimal "disk" or "hockey puck" eqi-energy surface. This "hockey-puck" shape has significantly lower effective mass in the direction of hole propagation, but higher effective mass in the other two directions (to improve the density of states, and to provide increased separation between the first and second subband for lower scattering). Lower effective mass and reduced scattering means better mobility and higher drive current for better performance. An effective hole enhancement of about 50% can be achieved by using the SiGe technology [17] at room temperature (T=300 K).

ii. SOI Technology: FD SOI devices, dual gate device structures, FinFETs, nanowire transistors

Many researchers are now adopting alternative transistor designs. Most explored alternative transistor structures are partially-depleted (PD) and fully-depleted (FD) silicon-on-insulator (SOI) devices. Nowadays there is also a wide interest and extensive research in double-gate (DG) structures and FinFET transistors [18]. These transistors have better electrostatic integrity and theoretically have better transport properties than single-gated FETs. A FinFET is a form of a double gate transistor which has surface conduction channels on two opposite vertical surfaces and has current flow in the horizontal direction. The channel length is given by the horizontal separation between source and drain and is usually determined by a lithographic step combined with a side-wall spacer etch process. In conclusion, the semiconductor industry is now approaching the end of an era of

scaling gains by mere shrinkage of device dimensions, and entering a post-scaling era, a new phase of CMOS evolution in which innovation is demanded simply to compete. It is expected that trends in benefits to density, switching performance, and power will be continued through such innovations. Thus, rather than coming to an end, a new era of CMOS technology is just beginning.

Silicon-On-Insulator devices:

SOI devices has been considered as one of the best methods for enhancing the performance of CMOS over that offered by conventional scaling for the last four decades. The first SOI transistor was introduced back in 1964. These devices were partially depleted devices and were fabricated on silicon-on-sapphire (SOS) substrates [19] . SOS technology found success in applications for various military and civilian projects and still today finds use in commercial high-frequency circuits. When the first SOI substrate became available for experimental MOS device production, partially depleted (PD) technology was the first choice to consider as derived from SOS understanding [19]. SOI was not suitable to work as a substrate for conventional applications before the 1990s. There were many problems for its widespread usage, the main ones being SOI material quality, device design, and the acceptable progress in bulk CMOS performance through scaling. The local substrate (body) of the MOS SOI device floats electrically and as a result the substrate-source bias is not fixed. As a result, the device threshold voltage changes as the substrate-source voltage changes

which is known as the kink effect, or increase in the output conductance of the device. This effect is caused by the increase in impact ionization in body-source bias V_{BS} with increasing drain-source bias V_{DS}. Using fully-depleted (FD) SOI devices minimizes floating-body effects. The SOI film thickness is much smaller than the channel depletion width in FD devices and as a result the body charge is fixed. Because of the much reduced potential barrier, any impact ionization charges (majority carriers) flowing into the depleted body are readily swept to the source. Because of this, during the early development of SOI technology, the main focus was on fully-depleted (FD) SOI devices since the kink effect and other floating-body effects such as dynamic threshold voltage variation were considered serious problems. FD-SOI devices also show benefit in the improvement with respect to short-channel effects. The thin silicon body in FD-SOI devices is depleted of mobile carriers for all bias conditions. Carriers in the inversion layer encounter a smaller average electric field than in standard bulk silicon devices with heavy channel doping. Subthreshold slopes are also significantly improved in FD-SOI devices than bulk silicon transistors.

The performance advantage of SOI over bulk Si MOSFET is caused by the elimination of the area junction capacitance, the lack of a reverse body effect in stacked circuits, and the fact that the SOI body is slightly forward biased under most operating conditions. Devices fabricated in this way are also found to be advantageous over their bulk silicon counterparts in terms of reduced parasitic

capacitances, reduced leakage currents, increased radiation hardness, as well as inexpensive fabrication process.

IBM launched the first fully functional SOI mainstream microprocessor in 1999 marking that SOI technology was becoming the state-of the art technology for future low-power ICs. Since then AMD recently implemented an x86-64 core in 32 nm SOI with high-K metal gate technology [20]. It occupies 9.69 mm^2, contains more than 35 million transistors (excluding L2 cache), and operates at frequencies in excess of 3 GHz. The process uses dual strain liners and e-SiGe (embedded Silicon Germanium) to improve performance. Transistors are fabricated in various threshold voltages and lengths to facilitate performance/leakage tradeoffs. The clock tree reduction, power gate, and power monitoring techniques applied encourage many interesting design points in the 2.5 to 25 W low-power mobile and desktop market space.

Fully depleted devices (finFETs or ETSOI) are promising for control of short channel effects in highly scaled devices. But in these devices, due to the scaled geometry, the source/drain resistance is a critical challenge that needs to be addressed. In finFETs, especially in tight pitch, the series resistance RSD related to contact resistance (Rco) between the silicide and Si S/D limits the drive current. I. Ok *et al*. [21] demonstrated encouraging modulation of Rext in n-finFETs by engineering the Al dose in the S/D of thin fins that are needed to maintain the short channel effects.

SOI is opening a number of opportunities in the low power arena. In many applications, from hand-held devices to large servers, power is becoming a limiting factor. One of the attractions of the SOI technology is its low-power behavior. For a given CMOS generation, SOI provides higher performance than a comparable bulk technology. This performance headroom allows for operation at lower voltage and lower power (as much as 2–3 times). In other words, the lowest-active- power technology is the highest-performance technology operated at low voltage. One concern expressed about the use of SOI for low power has been its high off-current, I_{off}. However, as one reduces the voltage to lower the SOI active power, the SOI I_{off} decreases much faster than that of bulk, matching the bulk-Si I_{off} at low voltage. With the increased use of wireless technology, SOI CMOS offers some unique opportunities in the mixed signal and radio-frequency (rf) circuits. Wireless technologies require high performance transistors and low-loss passive devices (inductors and capacitors). SOI allows the use of high-resistivity substrate (>2 KΩ-cm), which can result in high Q for the passive elements (i.e., inductor Q greater than 30), which would minimize the crosstalk among analog and digital circuits.

Over the last 2-3 years there has been significant progress in the demonstration of device and technology elements on FD devices on very thin SOI. Work by Majumdar focused on the FD device on 8 nm SOI [22]. They were able to obtain excellent nFET. Their pFET suffered from high parasitic source-drain resistance, caused by the dopant loss to the BOX, which was aggravated by the damage

during the implantation. Cheng [23] extended the earlier work to thinner SOI, metal gate and a novel non-implanted S/D [24]. For doping the S/D they rely on the doped faceted epi S/D and then driving the extension doping out of the doped epi. Because of the minimum damage, the p+ doping is much higher for the pFET S/D and they were able to get excellent pFETs.

For a low power technology, in addition to the "nominal" devices, a number of other devices (i.e. different gate oxide thickness and multi- V_T, passives such as diodes, varactors, etc.) are needed. Cheng and colleagues have demonstrated that these alternative devices can be made on the thin fully depleted SOI, one does not have to go to a hybrid technology (i.e. FD and bulk, or FD and PD SOI) [25].

A requirement of a new technology feature is its extendibility. At post-20 nm node, L < 20 nm is required. There are two paths for extending FD device on thin SOI: One is to go to thinner SOI (<6 nm). It is estimated that at 4 nm SOI film thickness, L of <15 nm is feasible. As one goes to below 3-4 nm, the effect of scattering off the bottom interface becomes important and there may be a limiter. The other approach is to put the thin SOI on thin BOX [26]. Thin BOX not only improves the short channel effect, but it also allows V_T control through the application of back-bias. As the bulk technologies move to 22 nm, body effect is diminished. FD device on thin BOX maybe the only path to apply back-bias (with reasonable voltages) at these nodes. The challenge with FD on thin BOX is the integration of multiple oxide devices.

Double-Gate (DG) transistors have emerged as promising devices for nano-scale circuits due to their better scalability compared to bulk CMOS. Among the various types of DG devices, quasi-planar SOI FinFETs are easier to manufacture compared to planar double-gate devices. DG devices with independent gates (separate contacts to back and front gates) have also been developed. DG devices with symmetric and asymmetric gates have also been demonstrated. Such device options have direct implications at the circuit level. Independent control of front and back gate in DG devices can be effectively used to improve performance and reduce power in sub-50nm circuits. Independent gate control can be used to merge parallel transistors in non-critical paths. This results in reduction in the effective switching capacitance and hence power dissipation.

One of the major advantages of using double gate transistors is the lower leakage current. The major leakage components in double gate devices are: (a) subthreshold leakage and (b) gate leakage [27]. In double gate structures, presence of two gates and ultra-thin body helps to reduce the Short-Channel Effect (SCE), which significantly reduces the subthreshold leakage current. Lower SCE in DG devices and the higher driver current (due to two gates) allows the use of thicker oxide in DG devices compared to bulk-CMOS structures. This helps to reduce the gate leakage current. Moreover, lower SCE allow the use of lower body doping (body can even be intrinsic) in DG devices compared to bulk-CMOS structure. Hence, to induce equal inversion charge, DG devices require

lower electric field compared to bulk-CMOS structure, which also helps to reduce the gate leakage current in DG devices [28].

Most of these SOI and multi-gate devices have a general "wire-like" shape with a gate electrode that controls the flow of current between source and drain and they are often referred as Nanowire transistors.

1.3 Self-Heating Effects in SOI Transistors

The role of the buried oxide on the thermal conductivity reduction:

Silicon-on-insulator (SOI) technology is a potential challenger to bulk silicon technology for future VLSI applications due to its potentially increased circuit speeds and simpler fabrication process [29]. These advantages arise from the presence of the buried insulating layer; most commonly silicon dioxide, which reduces the parasitic source/drain-to-substrate junction capacitance, limits the depth of the source/drain junction to form simple shallow junctions, and allows full dielectric isolation of the device to eliminate latchup. But, the low thermal conductivity of the underlying silicon dioxide layer, which is about two orders of magnitude less than that of silicon, inhibits cooling in SOI devices and causes severe self-heating. This results in higher channel operating temperatures and is evidenced by the negative differential conductance at high gate biases that is characteristic of most SO1 devices [30], [31]. The temperature rise is significant and dependent on the buried oxide thickness, silicon thickness, and channel-metal contact separation. The device mobility is reduced as a result of the elevated

temperatures and results in reduced maximum drain saturation current and more complicated device modeling. In addition, high channel temperatures lead to increased interconnect temperatures at the silicon-metal contact and make conduction cooling through the source, drain, and interconnects important [32]. It should also be noted that the thermal conductivity of the silicon films decreases as the film thickness is reduced due to boundary scattering of phonons, which further exacerbates self-heating and hence device performance.

As device density and clock frequency continue to increase, it has become very important to remove heat from deep inside the ultra large scale integrated circuit structures in the modern nano-electronics industry. Recently a lot of new semiconductor thermoelectric coolers and structures, such as thermionic [33] and nanowire coolers [34] have been proposed, developed and investigated to address heat removal from integrated circuits. For example, thermionic emission current in heterostructures can be used to attain cooling by emission of hot electrons over a barrier layer from cathode to anode. It is possible to effectively build a temperature gradient using such structures within the range of the electron mean free path (a few hundred nanometers), which can be used to remove the heat from a hotspot region.

In summary, as semiconductor technology approaches to two-dimensional and three-dimensional transistor structures that are more isolated from the substrate, self-heating effects are becoming increasingly important. This issue is more important for SOI technology since the device is isolated from the substrate by a

low thermal conductivity buried silicon dioxide layer and by the copper interconnects that are enclosed by low thermal conductivity dielectric materials [35]. It is now extremely challenging to accurately model thermal phenomenon and hence design microelectronic devices and thin film structures at micro and nanoscale level.

The role of phonon boundary scattering:

The buried silicon-dioxide layer in SOI circuits has a very low thermal conductivity, which results in a large thermal resistance between the device and the chip packaging. This is a major problem for transistors that experience brief pulses of heating, such as ESD protection devices. Lateral conduction parallel to the plane of the wafer in the silicon device layer can strongly reduce the temperature rise in active regions, such as the transistor channel [32].

Heat conduction in silicon is dominated by phonon transport, even in the presence of large concentrations of free charge carriers. When the thickness of a thin semiconducting layer approaches the phonon mean free path, scattering at the boundaries influences the thermal conductivity. As a result, the device-layer thermal conductivity is reduced compared to that of bulk silicon due to scattering mechanisms in the layer that are not present in the bulk material, such as those depicted in Fig 1.1. Phonon-boundary scattering is particularly important at low temperatures, where the mean free path would otherwise become arbitrarily large. While phonon-boundary interactions govern the thermal conductivity of any

silicon sample at low enough temperatures, the reduction is more severe and extends to higher temperatures for thin layers than for bulk samples.

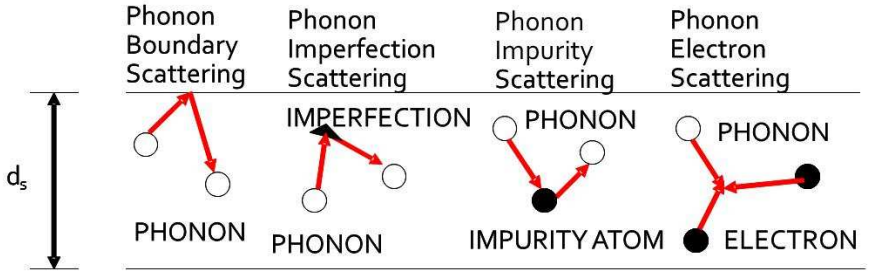

Fig 1.1: Phonon scattering mechanisms which reduce the thermal conductivity of SOI device layers compared to that of bulk intrinsic silicon. The thermal conductivity of silicon is dominated by phonon transport.

Also important is phonon scattering on imperfections, which exist in larger concentrations in SOI substrates than in bulk material. The higher concentrations result from steps in the wafer fabrication process, such as SIMOX implantation and the epitaxial growth process of BESOI wafers. While the impact of these imperfections on electrical transport has been studied, there has been little progress on modeling or measuring their impact on heat transport. Finally, the impurities and additional free carriers in doped semiconducting regions impede heat transport compared to that in bulk intrinsic silicon.

Using kinetic theory, the thermal conductivity can be expressed as:

$$K=\frac{1}{3}C_s\bar{v}\lambda = \frac{1}{3}C_s\bar{v}\Lambda \quad (1.1)$$

where C_s is heat capacity per unit volume, $\bar{v}$ is the average phonon velocity and λ is boundary and impurity scattering affected averaged phonon mean free path. Using Matthiessen's rule, the thin film and impurity effects can be combined and the phonon mean free path can be approximated as

$$\frac{1}{\lambda}=\frac{1}{\Lambda_b}+\frac{1}{t_{Si}}+\frac{1}{\Lambda_{imp}} \quad (1.2)$$

where Λ_b is the phonon mean free path in undoped, bulk silicon (depends only on the anharmonic phonon-phonon interactions and hence only on temperature), and Λ_{imp} is the mean phonon-impurity scattering length.

1.4 Emergence of Nanowire Technology:

Great advances in integrated circuit technologies have been accomplished during the past four decades that resulted in electronic devices with higher device density, faster clock rate and lower power consumption [36]. This rapid development of integrated circuit technology is primarily due to MOSFET downscaling trends that have continued to the present day. However, as the devices reach deep sub-100 nm scale, conventional scaling methods which maintain the device's basic structure while shrinking its size face increasing technological and fundamental challenges. For example, device size fluctuations

will result in a large spread in device characteristics at the nanoscale, affecting key parameters such as the threshold voltage and on/off current. Increasing demand on the resolution of the equipment and expenses of building and operating the facilities also pushes the traditional approach towards its practical limit and hinders device scaling from reaching true atomic level [37],[38]. To sustain the historical scaling trend beyond CMOS, novel one-dimensional (1D) structures, including carbon nanotubes (CNTs) and semiconductor nanowires (NWs), have been proposed as the active components (as well as interconnects) in future nanoscale devices and circuits. In this case, the critical device size is defined during the growth (chemical synthesis) process and can be controlled with atomic scale resolution. To date, great efforts and progress has been made in the field of CNTs, although CNT based applications are still hindered by difficulties to produce uniform, semiconducting nanotubes. On the other hand, semiconductor NWs can be prepared with reproducible electronic properties in high-yield, as required for large-scale integrated systems.

In addition, recent studies have suggested that SiNWs FETs can exhibit transport characteristics that are comparable to or exceed the best planar devices fabricated by top-down approaches [39]. These latter results are intriguing because they indicate that these SiNW FETs may offer advantages compared to lithographically patterned silicon nanostructures. To understand these results will require better control of diameter and surface properties, including reduction of

the SiNW diameters to the molecular scale, where it may be possible to achieve true 1D behavior [40], [41].

Furthermore, the well-controlled NW growth process implies that materials with distinct chemical composition, structure, size and morphology can be integrated [42]. Such an ability to build specific functions into the system during growth may, in turn, lead to bottom-up assembly of integrated circuits [42], which offer the potential of parallel production of massive number of devices with similar material and electrical/optical properties. Drastically different from the 'top-down' paradigm commonly used in today's semiconductor industry, this 'bottom-up' paradigm, analogous to the way that nature works, may prove to be a suitable solution to the technological challenges as devices approach atomic size.

General trends in nanoelectronics:

(i) Nanoelectronic Devices

Homogeneous doped NWs represent key building blocks for a variety of electronic devices [43]-[46]. A prototypical example of such a device with broad potential for applications is the NW field-effect transistor (NWFET). For example, studies of NWFETs fabricated from boron-[47] and phosphorus-doped [48] Si NWs have shown that the devices can exhibit performance comparable to the best reported for planar devices made from the same materials. Studies have also demonstrated the high electron mobility of epitaxial InAs NWFETs with a wrap-around cylindrical gate structure surrounding a nanowire [49]. More

generally, controlled bottom-up assembly and synthetic elaboration of NWs offers unique opportunities. The crossed NW architecture enables device properties to be defined by the assembly of the NW components and not by lithography, and has been utilized to demonstrate logic gate structures, basic computation, and selective addressing [44]. Synthesis of axial modulation-doped NW heterostructures has enabled the creation of address decoders and coupled quantum structures without a critical use of lithography [45], while the design of radial Ge/Si core–shell NW heterostructures demonstrated a true performance benefit of NWFETs compared with state-of-the-art planar devices [46].

(ii) Nanowire Nanosensors

Field-effect transistors fabricated using individual NWs are ultrasensitive nanosensors for detecting a wide range of gases, chemicals, and biomedical species in both commercial and research applications [50], [51]. The high-performance characteristics of NWFETs, such as high surface-to-volume ratio and specially designed surface structures, are key factors that lead to very high sensitivity. More important to overcoming the sensitivity limitations of previous planar FET sensors is the 1D morphology of these nanoscale structures. Specifically, binding to the surface of a nanowire leads to depletion or accumulation of carriers in the "bulk" of the nanometer-diameter structure versus only the surface region of a planar device [50]. NWFETs can be configured as highly selective and highly sensitive detectors by linking recognition or receptor

groups to the surface. This was first demonstrated with Si NWFETs, which were used for detection of pH, metal ions, and proteins [52]. More generally, these unique features of semiconductor nanowires have led to sufficient sensitivity and selectivity to enable the detection of viruses at the single-virus level [50] and sequence-specific DNA detection at the femtomolar level [51].

(iii)Nanophotonics

Nanowires represent attractive building blocks for active nanophotonic devices, including light-emitting diodes (LEDs), lasers, and detectors [53], [54]. Significantly, the ability to assemble and electrically drive nanoscale sources and detector blocks could allow for fully integrated nanophotonic systems for use in applications ranging from biodetection through information processing. The crossed NW approach was the first to demonstrate true nanoscale LEDs, or nanoLEDs. In this work, nanoscale *p*–*n* diodes were created by crossing well-defined *p*-type and *n*-type InP NWs, and subsequent device measurements showed that band edge emission is observed at the nanoscale cross-points in forward bias [55]. This concept has enabled the assembly of a wide-range of nanoLEDs on a single chip, with emission ranging from ultraviolet through near-infrared in a manner not possible with conventional planar technology [53].

(iv) Nano-Biotechnology

Integration of nanosystems and biosystems is a multidisciplinary field that has the potential for tremendous impact on biology, chemistry, physics, biotechnology, and medicine. The combination of these diverse areas of research promises to yield revolutionary advances in healthcare, medicine, and the life sciences through, for example, the creation of new and powerful tools that enable direct, sensitive, and rapid analysis of biological and chemical species. Patolsky et al. [50] have demonstrated the first application of NW nanosensors for ultrasensitive detection of proteins down to individual virus particles as well as multiplexed recording of these species using distinct NW elements within a sensor device. In addition, Patolsky et al. [56] have demonstrated an unprecedented approach for investigating the electrical properties of hybrid structures consisting of arrays of NWFETs integrated with the individual axons and dendrites of live mammalian neurons, where each nanoscale junction can be used for spatially resolved, highly sensitive detection, stimulation, and/or inhibition of neuronal signal propagation. Arrays of nanowire–neuron junctions enable simultaneous measurement of the rate, amplitude, and shape of signals propagating along individual axons and dendrites. The configuration of nanowire–axon junctions in arrays, as both inputs and outputs, makes possible controlled studies of partial to complete inhibition of signal propagation by both local electrical and chemical stimuli. This revolutionary development opens a new field in integrated nano-biotechnology.

(v) Nanoelectromechanical Systems

The development of novel technologies for wireless nanodevices and nanosystems is critically important for in situ, real-time, and implantable biosensing and biomedical monitoring. Nanosensors are currently under intense development for ultrasensitive and real-time detection of biomolecules. An implanted wireless biosensor, for example, requires a power source, which may be provided directly or indirectly. It is highly desirable for wireless devices (and required for implanted biomedical devices) to be self-powered without the need for finite-lifetime batteries. Using aligned ZnO NWs grown either on a crystal substrate or a polymer substrate [58], an innovative approach has been demonstrated for converting nanoscale mechanical energy into electric energy [57]. By deflecting the aligned NWs using a conductive atomic force microscope (AFM) tip in contact mode, the energy that was first created by the deflection force and later converted into electricity by the piezoelectric effect has been measured to demonstrate a nanoscale power generator. The operation mechanism of the electric generator relies on the unique coupling of piezoelectric and semiconducting dual properties of ZnO as well as the elegant rectifying function of the Schottky barrier formed between the metal tip and the NW [59].

Synthesis of nanowires:

First nanowire fabrication:

Charles M. Lieber and his group was one of the first few researchers to fabricate nanowires. They demonstrated [60] the general synthesis of high-quality single-crystal nanowires (NWs) of group IV, III–V, and II–VI semiconductors by developing the laser-assisted catalytic growth (LCG) method which exploits laser ablation to generate nanometer-diameter catalytic clusters that define the size and direct the growth of the crystalline nanowires by a vapor–liquid–solid (VLS) mechanism. Field-emission scanning electron microscopy and transmission electron microscopy investigations showed that the GaAs nanowires are produced in >90% yield, are single crystals with <111> growth axes, and have diameters varying from three to tens of nanometers, and lengths extending to tens of micrometers.

The same research group later demonstrated [61] the synthesis of high-quality single-crystal SiNWs with well controlled diameters by using well-defined Au nanocluster catalysts and silane (SiH4) as the vapor-phase reactant. Transmission electron microscopy studies of the materials grown from 5, 10, 20, and 30 nm nanocluster catalysts showed that the nanowires had mean diameters of 6, 12, 20, and 31 nm, respectively, and were thus well defined by the nanocluster sizes. High-resolution transmission electron microscopy demonstrated that the nanowires have single-crystal silicon cores sheathed with 1–3 nm of amorphous oxide and that the cores remain highly crystalline for diameters as small as 2 nm.

In general, there are two basic approaches of synthesizing nanowires: top-down and bottom-up approach. We will discuss these two approaches along with current experimental approaches in the fabrication of nanowires.

(i) Bottom-up approach:

The bottom-up approach, in which functional structures are assembled from well-defined chemically and/or physically synthesized nanoscale building blocks represents a powerful alternative approach to conventional top-down methods [62], [63]. The bottom-up approach has the potential to go far beyond the limits and functionality of top-down technology by defining key nanometer-scale metrics through synthesis and subsequent assembly—not by lithography. Moreover, it is highly likely that the bottom-up approach will enable entirely new device concepts and functional systems and thereby create technologies that we have not yet imagined. For example, it is possible to seamlessly combine chemically distinct nanoscale building blocks that could not be integrated together in top-down processing and thus obtain unique function and/or combinations of function in an integrated nanosystem.

To enable this bottom-up approach for nanotechnology requires a focus on three key areas that are at the heart of devices and integration. First, the bottom-up approach necessitates nanoscale building blocks with precisely controlled and tunable chemical composition, structure, size, and morphology, since these characteristics determine their corresponding physical properties. To meet this

goal requires developing methods that enable rational design and predictable synthesis of building blocks. Second, it is critical to develop and explore the limits of functional devices based on these building blocks. Nanoscale structures may behave in ways similar to current electronic and optoelectronic devices, although it is also expected that new and potentially revolutionary concepts will emerge from these building blocks, for example, due to quantum properties. Third and central to the bottom-up concept will be the development of architectures that enable high-density integration with predictable function, and the development of hierarchical assembly methods that can organize building blocks into these architectures.

Semiconductor NWs are generally synthesized by employing metal nanoclusters as catalysts via a vapor liquid–solid (VLS) process (see Fig 1.2) [64]. In this process, the metal nanoclusters are heated above the eutectic temperature for the metal–semiconductor system of choice in the presence of a vapor-phase source of the semiconductor, resulting in a liquid droplet of the metal/semiconductor alloy. The continued feeding of the

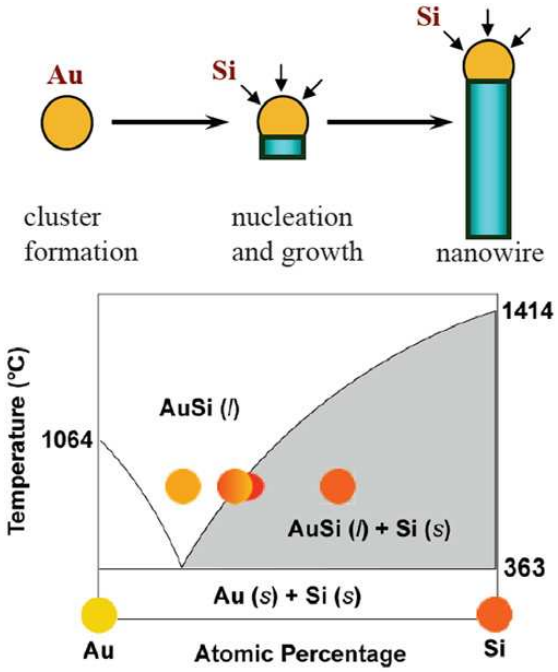

Fig 1.2: Schematic of VLS growth of Si nanowires (SiNWs). (a) A liquid alloy droplet. AuSi is first formed above the eutectic temperature (363 ◦C) of Au and Si. The continued feeding of Si in the vapor phase into the liquid alloy causes oversaturation of the liquid alloy, resulting in nucleation and directional nanowire growth. (b) Binary phase diagram for Au and Si illustrating the thermodynamics of VLS growth. Figure taken from Ref. [64].

semiconductor reactant into the liquid droplet supersaturates the eutectic, leading to nucleation of the solid semiconductor. The solid–liquid interface forms the growth interface, which acts as a sink causing the continued semiconductor incorporation into the lattice and, thereby, the growth of the nanowire with the alloy droplet riding on the top. The gaseous semiconductor reactants can be generated through decomposition of precursors in a chemical vapor deposition (CVD) process or through momentum and energy transfer methods such as pulsed

laser ablation [65] or molecular beam epitaxy (MBE) [66] from solid targets. So far, CVD has been the most popular technique. In CVD–VLS growth, the metal nanocluster serves as a catalyst at which site the gaseous precursor decompose, providing the gaseous semiconductor reactants. In the case of SiNW growth (Fig 1.2), silane (SiH_4) and Au nanoparticles are normally used as the precursor and catalysts, respectively.

This nanocluster-catalyzed VLS growth approach, particularly for CVD or CBE processes, offers the ability to fine tune the diameter, morphology, and, critically, the electrical properties of the nanowires in a flexible and controllable fashion. For example, modulation doping can be achieved by adjusting the dopant concentration *in situ* during nanowire growth [67]. Radial and axial nanowire heterostructures that offer intriguing electrical properties can be produced by switching on and off different source materials during the VLS growth process [68]. The ability to control nanowire growth down to the atomic level is one of the main factors leading to the great success that nanowire research enjoys today.

Besides the VLS approach, a simple thermal evaporation/vapor transport deposition approach has also been shown to be effective in growing 1D structures, in particular metal oxide (e.g. ZnO, In_2O_3 and SnO_2) NWs. Such NWs have been studied in applications ranging from optoelectronics devices [69], field-effect transistors [70], ultra-sensitive nanoscale gas sensors [71] and field emitters [72]. In particular, ZnO NWs have attracted a lot of interest due to the large exciton

binding energy (60 meV), high electromechanical coupling constant and resistivity to harsh environment [73].

(ii) Top-down approach:

In the top-down approach, small features are patterned in bulk materials by a combination of lithography, etching, and deposition to form functional devices and their integrated systems. The top-down approach has been exceedingly successful in many venues, with microelectronics being perhaps the best example today. There are a few variants of fabrication approaches reported for the realization of NWs and devices using the top–down technique. All approaches start with the silicon wafers as the substrate and involve lithography and etching processes for starting pattern definition. Different process steps such as hardmask trimming [74], etching in H_2 ambient [75], and/or stress-limited oxidation processes [53] follow to convert the silicon structures defined in the earlier step into NWs. The stress-limited oxidation is usually carried out at low temperature to keep the grown oxide in stress to progressively slow down the oxidation rate, thus leaving a nanometer-scale silicon core embedded in the oxide. The stress-limited oxidation was first reported on vertical 1-D nanorod structures by Liu *et al.* [76], wherein the silicon columns of about 40–50 nm in diameter and about 1000 nm in height were subjected to long oxidation (up to more than 40 h) at low temperatures (800 C) that reduced the core of the silicon to less than 5 nm. Kedzierski *et al.* [77] made use of this stress-limited oxidation for obtaining the

lateral NWs and utilized those as transistor channels, with the thick stress-limited grown oxide serving as the gate dielectric. Although the gate dielectric thickness was large (~25 nm), the devices showed good performance in terms of on-current, on-to-off-current ratios, drain-induced barrier lowering (DIBL), as well as sub-threshold slope (SS). As an alternative approach for reducing the fins to NWs, hydrogen annealing of an ultra-narrow fin has been used by Yang *et al.* [78]. NWs with 10-nm diameter and truncated cylindrical shape have been fabricated. The fabricated sub-10-nm gate-length NW FETs in omega gate architecture showed very low OFF-state leakage current and excellent gate delay. Hydrogen annealing has also been reported by Ernst *et al.* [79] with vertically stacked NW for high-performance circuits. Tezuka *et al.* [75] have applied hydrogen annealing/etching for Si and SiGe NWs to reduce the sidewall roughness.

Another approach to define Si-NWs and GAA (Gate All Around) transistors has been reported by Suk et al. [74] and Yeo et al. [80]. In this approach, silicon fin is split into two NWs—twin Si-NW—using the hard-mask trimming process. The lateral dimensions of NWs are defined by trimming of the hard mask, while the vertical dimensions are given by the thickness of the silicon epitaxial layer on top of a sacrificial SiGe layer. The GAA transistors fabricated on these 8-nm-thick wires with grown oxide as the gate dielectric and damascene poly-silicon gate electrodes down to the physical gate length of 15 nm show excellent gate control and other characteristics.

Recently Yangyuan Wang *et al*. [81] showed a new method to fabricate high-performance gate-all-around silicon (Si) nanowire transistors (SNWTs) based on fully Si bulk (FSB) substrate using top-down approach. Their device showed better heat dissipation capability due to the large fan-out of Si S/D region connecting with the bulk substrate, which provides efficient path for the heat dissipation, especially for multi-wire cases.

Y.Q. Fu et al. [82] used deep reactive ion etching (DRIE) as a tool for the realization of nanostructures and architectures, including nanopillars, silicon nanowires or carbon nanotubes. They actually combined top-down fabrication methods with the bottom-up synthesis of one-dimensional nanocomponents. The field-emission properties of carbon nanotubes/Si pillars hybrid structures are measured, as well as the transport properties of large-area nanowires obtained via nanowire lithography. The potential of DRIE for the fabrication of three-dimensional nanostructures is also revealed.

Recently J. W. Peng and co-workers [83] presented a complementary metal–oxide–semiconductor-compatible top–down fabrication of Ge nanowires along with their integration into pMOSFETs with “HfO2/TaN” high-k/metal gate stacks. Lateral Ge wires down to 14 nm in diameter are achieved using a two-step dry etch process on a high-quality epitaxial Ge layer. To improve the interface quality between the Ge nanowire and the HfO_2, thermally grown GeO_2 and epitaxial-Si shells are used as interlayers. The I_{ON}/I_{OFF} ratios of six orders were achieved on the 14-nm-diameter GeNW pMOSFET with thermally grown GeO_2

shell. The interfacial epitaxial-Si layer was demonstrated to be an effective mobility booster toward the integration of high-mobility Ge channel transistors.

1.5 Previous Work on Modeling Silicon Nanowires:

In our present work we model ultra-narrow channel SOI MOSFET first proposed and fabricated by Majima et al. [84] and schematically shown in Fig. 1.3. In this device structure, the threshold voltage not only depends on the SOI thickness but also on the channel width, because horizontal carrier confinement also takes place in the narrow channel. It is referred to this channel width dependency of the threshold voltage by quantum confinement as the quantum mechanical narrow channel effect. To achieve better control of the gate over the channel the gate oxide thickness in this work is assumed to be 1 nm, not 34 nm as depicted in the Fig. 1.3 taken from Ref. [84].

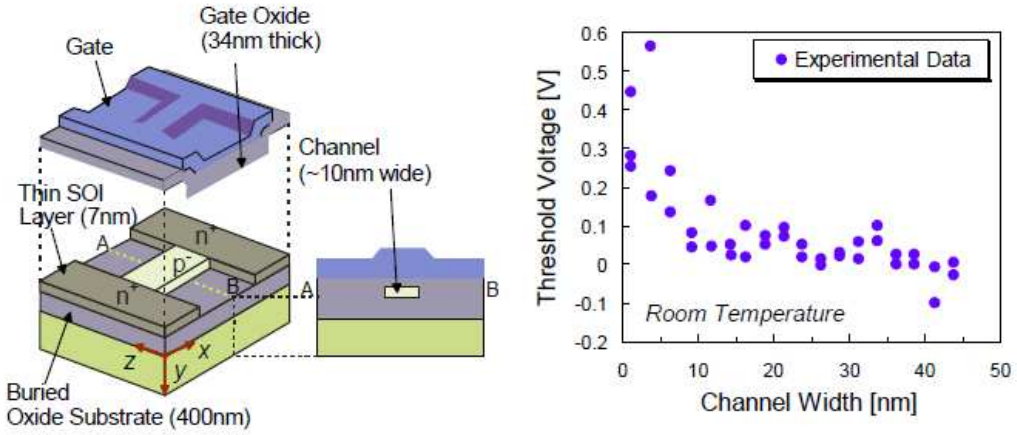

Figure 1.3: (a) Device structure of ultra-narrow channel FD-SOI device structure. (b) Threshold voltage fluctuations as a function of channel width and device variations for the same channel width due to the presence of unintentional dopants at random locations in the channel [84].

Threshold voltage in bulk-MOSFETs with polysilicon gates is traditionally controlled through channel profile engineering [85]. However, in a sub-100 nm FD-SOI device, this leads to problems such as channel dopant fluctuation, sub-threshold swing degradation, mobility reduction and threshold voltage sensitivity to oxide thickness. To avoid these issues, the silicon body is usually intrinsic or lightly doped and the threshold voltage is solely determined by the metal workfunction. Choosing the proper material for the gates is a problem by itself. In addition, fluctuations in the device characteristics due to discrete/ unintentional doping, also noticeable in the results of Fig. 1.3(b) in the FD SOI device structure, can pose serious problems in transistor matching for circuit applications [87],

[88]. The researchers in the Nanostructures Research Group at Arizona State University have already shown that even in conventional transistors there is a significant mismatch in the threshold voltage between devices with different number and different distribution of the impurity atoms [86]. As similar fluctuations have been observed in the experimentally measured threshold voltage of the FD-SOI devices [Fig. 1.3(b)], it becomes necessary to examine the role of possible unintentional doping on the narrow-width FD-SOI device operation.

One of the important parameters that determine the performance of a silicon nanowire FET is the low-field electron mobility. Irena Knezevic et al. [89] investigated the electron mobility in a rectangular SiNW (the SiNW of Fig 1.3) by considering electron scattering due to acoustic phonons, intervalley nonpolar optical phonons and imperfections at the Si-SiO_2 interface. They computed the low-field mobility by using a self-consistent Poisson–Schrödinger–Monte Carlo transport solver. To investigate the behavior of the phonon-limited and surface-roughness-limited components of the mobility they decreased the wire width from 30 to 8 nm. At low and moderate transverse fields the transport is characterized by the phonon-limited mobility which is found to decrease with decreasing wire width because of the increase in the electron-phonon wavefunction overlap. They found surface roughness scattering to decrease with decreasing width due to volume inversion [89]. This group also investigated [90] the effects of electron and acoustic phonon confinements on the low-field electron mobility of this SiNW structure. They found that for very thin nanowires, the mobility continually

decreases with increasing spatial confinement and becomes almost independent of the transverse electric field. The main reasons for this behavior are: first the increase in the field-independent, confinement-induced part of the surface roughness scattering, and second the increase in intrasubband phonon scattering.

Eric Pop et. al [91] described the implementation of a Monte Carlo model for electron transport in nanoscale devices using analytic, nonparabolic electron energy bands, which are computationally efficient and sufficiently accurate for SiNW structures. They introduced an empirically fine-tuned set of deformation potentials for intervalley scattering, which enables more accurate electron transport simulations in both strained and unstrained silicon. Their work represents a different approach to analytic-band MC codes, because it distinguishes between intravalley scattering with LA and TA phonons and includes an analytic dispersion for all the phonon modes.

The group of Eric Pop extended their work for further applications in computing detailed phonon generation spectra [92]. They found the generated phonon spectrum in strained silicon to be different from bulk silicon at low electric fields due to band splitting and scattering selection rules which favor *g*-type and reduce *f*-type phonon emission. However, heat generation is essentially the same in strained and bulk silicon at high fields, when electrons have enough energy to emit across the entire phonon spectrum despite the strain-induced band splitting.

The group of Klimeck [93] investigated the bandstructure carrier velocity and ballistic current in silicon nanowire (NW) transistors with different

crystallographic orientations. They used a 20 band $sp^3d^5s^*$ spin-orbit-coupled, semiempirical, atomistic tight-binding model with a semiclassical, ballistic field-effect-transistor model. Infinitely long, uniform, cylindrical, and rectangular NWs, of cross sectional diameters/sides ranging from 3–12 nm were considered. For a comprehensive analysis, n-type and p-type metal-oxide semiconductor (NMOS and PMOS) NWs in [100], [110], and [111] transport orientations were examined. Their analysis showed the PMOS [111] NWs are the ones with the highest performance from all NW categories, whereas the PMOS [100] the ones with the lowest performance. The [110] oriented NWs, on the other hand, are the ones with both high NMOS and PMOS carrier velocities and on-current, and therefore more suitable for CMOS applications.

Extensive work, that examines the role of unintentional dopants on the magnitude of the threshold voltage and on-current of the SiNW of Fig 1.3, has been carried out by Shaikh Ahmed [126]. Here we want to extend this work to include the self-heating effects and examine how they affect the performance of the nanowire transistor of Fig. 1.3.

1.6 Thermal Conductivity Modeling of Silicon Nanowire:

The thermal conductivity of silicon is dominated by phonon transport and, for the case of thin films, can be reduced by phonon scattering on boundaries and by imperfections related to the fabrication process.

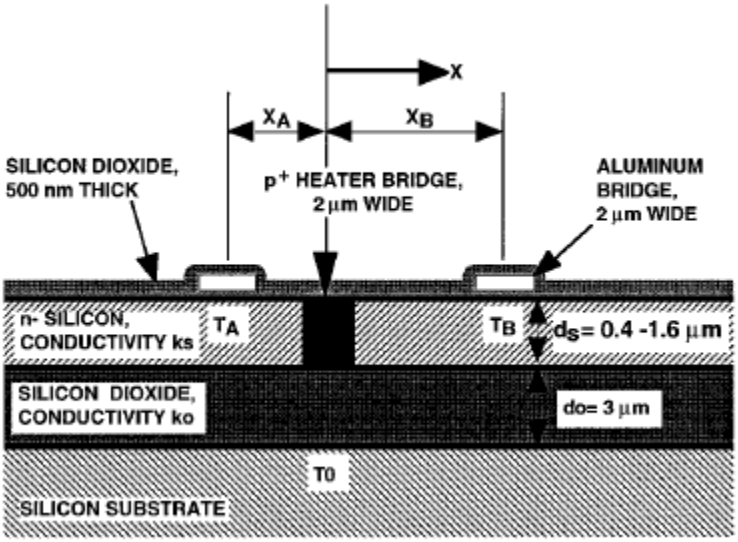

Fig 1.4: Cross-sectional schematic of the experimental structure used to measure the lateral thermal conductivity of single-crystal silicon layers in SOI substrates [94].

M. Asheghi et al. [94] provided experimental data and phonon transport analysis that quantify the impact of phonon-boundary scattering on heat conduction in crystalline silicon layers. For their experimental data they used the microfabricated structure shown in Fig 1.4. The exact solution is well approximated by

$$T(x) - T_0 = \frac{P'}{2}\sqrt{\frac{d_0}{k_0 d_s k_s}}\exp\left(-\frac{x - x_0}{L_H}\right) \tag{1.3}$$

where P' is the heater power per unit length, T_0 is the substrate temperature beneath the structure, d_s and d_o are the silicon and oxide thicknesses, respectively,

k_0 is the vertical thermal conductivity of the oxide, and k_s is the lateral thermal conductivity of the silicon.

For their theoretical analysis Asheghi and co-workers used a version of the thermal conductivity integral for silicon [95], which accounts for phonon dispersion and distinguishes between the contributions of transverse and longitudinal modes, together with a solution to the Boltzmann transport equation along thin layers [96]. The modified form of the conductivity integral is

$$k = \sum_{i=L,T1,T2} \frac{1}{3} v_i^2 \int_0^{\theta_i/T} C_i(\tau_b)_i F\left(\frac{d_s}{(\Lambda_b)_i}\right) dx_w \tag{1.4}$$

where the subscripts i=L, T1, T2 refer to the single longitudinal and the two transverse phonon modes, respectively, v_i is the appropriate phonon group velocity, Θ_i is the Debye temperature of the solid, $x_\omega = h_p\omega/k_BT$ is the non-dimensional phonon frequency, C_i is phonon specific heat per unit volume and non-dimensional frequency, the Boltzmann constant is $k_B = 1.38\times10\text{-}^{23}$ J K^{-1}, and Planck's constant divided by 2π is $h_P = 1.602\times10^{-34}$ Js. The conductivity reduction due to phonon-boundary scattering is calculated independently for each differential step in the phonon frequency spectrum using the solution to the Boltzmann transport equation, which is realized through the function F. The relaxation time in the absence of phonon-boundary scattering, τ_b, is that determined previously for bulk silicon [95]. The boundary scattering reduction function F depends on the ratio of the layer thickness, d_s, and the appropriate phonon mean free paths for transverse and longitudinal modes, $(\Lambda_b)_i = v_i(\tau_b)_i$. The

reduction function F is calculated using the exact solution to the Boltzmann transport equation for the mean-free path reduction along a thin layer [96]

$$F(\delta) = 1 - \frac{3}{8\delta^2} + \frac{3}{2\delta^2}\int_1^\infty \left(\frac{1}{t^3} - \frac{1}{t^5}\right)\exp(-\delta t)dt \qquad (1.5)$$

where $\delta = d_s/\Lambda_b$ is the reduced thickness. This expression assumes that phonons are diffusely scattered or emitted from the boundaries of the layer.

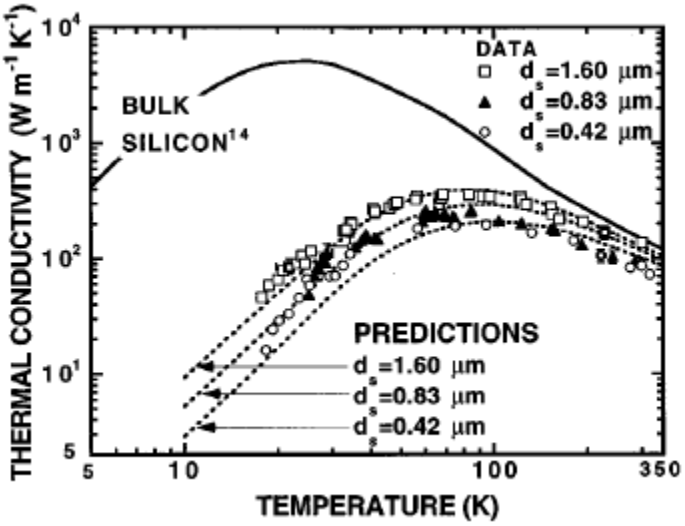

Fig 1.5: Thermal conductivities of single-crystal silicon layers with thicknesses 0.42 μm, 0.83 μm, and 1.6 μm [94]. Also included are recommended values for bulk silicon and predictions based on the phonon-boundary scattering analysis.

Fig 1.5 compares temperature-dependent thermal conductivity data for silicon layers with the predictions of Eqs. (2.2) and (2.3), and with the recommended

values for bulk samples [94]. The predictions use the conductivity model for bulk samples and the solution to the Boltzmann equation with no fitting parameters. The layer conductivities are strongly reduced compared to the bulk values, and the qualitative agreement with the data supports the conclusion that boundary scattering dominates. Fig. 1.5 also shows that the data agree well with predictions for the 1.6-μm-thick silicon over-layer between 30 and 300 K. The effect of surface roughness is more significant at lower temperatures where the population of the long wavelength phonons increases.

The impact of phonon-boundary scattering is demonstrated more clearly in Fig 1.6, which plots the thermal conductivity reduction of the silicon layers compared to the recommended bulk values as a function of thickness and temperature. The reduction in thermal conductivity of the 1.6 μm sample is small and not experimentally significant at room temperature, suggesting a microstructure and purity that closely resemble those in bulk crystals. Measurements shown in Fig 1.6 predict that the size effect on the conductivity can exceed two orders of magnitude for layers of thickness near one micrometer at temperatures less than 10 K. This could be very important for low-temperature sensors made from single-crystal silicon layers. The predictions also indicate that the reduction could exceed 50% for layers thinner than 0.1 μm at room temperature, which has very important implications for the cooling of transistors in SOI circuits. For SOI transistors based on ultrathin device layers (less than 50 nm), the thermal conductivity could be reduced as much as 70%.

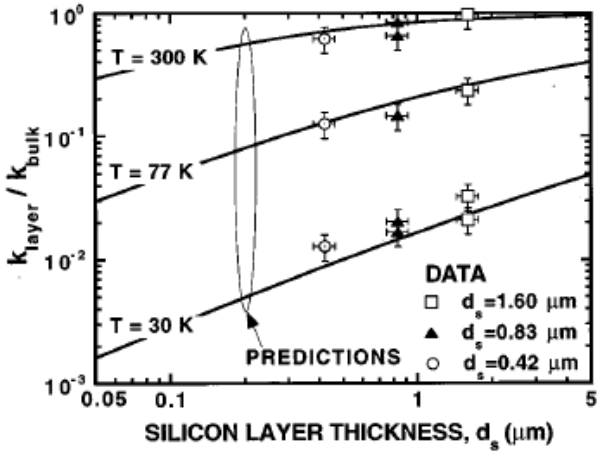

Fig 1.6: Thermal conductivity reduction due to phonon-boundary scattering [94].

For one-dimensional (1D) nanowires and nanotubes a systematic experimental study of size effect on Si nanowire thermal conductivity was done by Li Shi and co-workers [98]. Their results show that Si nanowire thermal conductivity is much lower than the corresponding bulk value, which can be explained by increased phonon boundary scattering. Furthermore, the experimental results for a 22 nm diameter silicon nanowire shows that the low-temperature behavior of its thermal conductivity significantly deviates from Debye T^3 law, which suggests possible changes in the phonon dispersion relation due to confinement.

Fig 1.7 shows a typical microdevice used in the experiments done by Li Shi et al. An individual Si nanowire thermally connects two suspended microfabricated microstructures. The thermal conductivity of the bridging nanowire can be estimated by four-point measurement of voltage drop and resistance of the resistors.

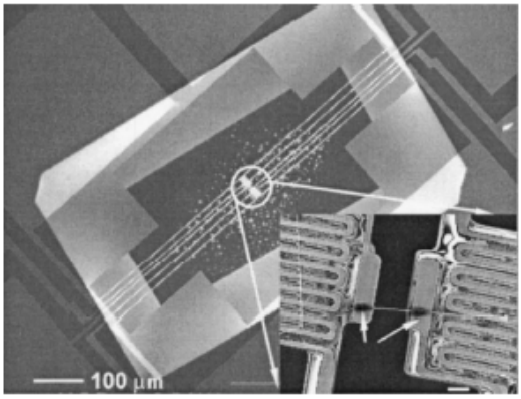

Fig 1.7: SEM image of the suspended heater used by Li Shi et al. [98]. The lower inset shows a 100 nm Si nanowire bridging the two heater pads, with wire-pad junctions wrapped with amorphous carbon deposits. The scale bar in the inset represents 2μm.

Shown in Fig 1.8 (a) are the measured thermal conductivities for intrinsic single-crystalline Si nanowires of different diameters (22, 37, 56, and 115 nm). Compared to the thermal conductivity of bulk Si [99], there are two important features that are common to all the nanowires which are measured: (i) The measured thermal conductivities are about two orders of magnitude lower than that of the bulk and, as the wire diameter is decreased, the corresponding thermal conductivity is reduced. This clearly indicates that enhanced boundary scattering has a strong effect on phonon transport in Si nanowires. (ii) For the 37, 56, and 115 nm diameter wires, thermal conductivities reach their peak values around 210, 160, and 130 K, respectively. This is in sharp contrast to the peak of bulk Si that occurs at about 25 K. The shift of the peak suggests that, as the wire diameter

is reduced, the phonon boundary scattering dominates over phonon–phonon umklapp scattering, which decreases the thermal conductivity with an increase in temperature. In addition, the thermal conductivity of the 22 nm diameter wire does not exhibit a peak within the experimental temperature range.

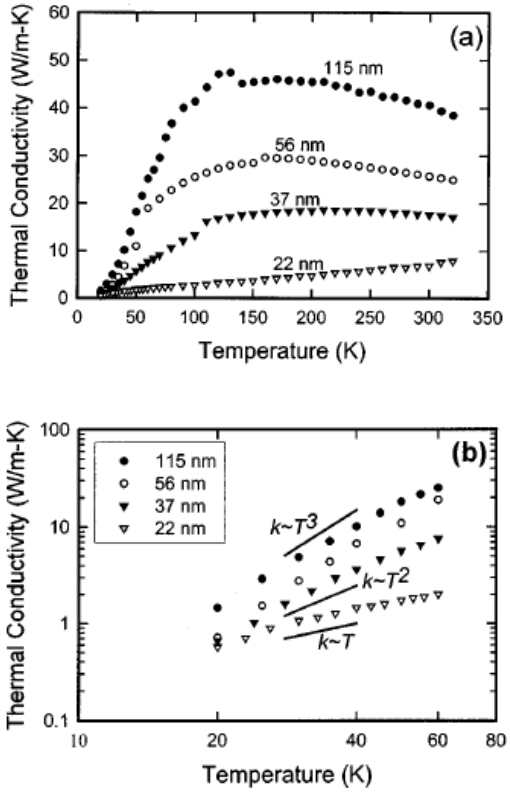

Fig 1.8: (top) Measured thermal conductivity of different diameter Si nanowires [98]. The number beside each curve denotes the corresponding wire diameter. (bottom) Low temperature experimental data on a logarithmic scale. Also shown are T^3, T^2, and T^1 curves for comparison.

The temperature dependence of the thermal conductivity between 20 and 60 K is plotted on a log–log scale in Fig 1.8(b). It can be seen that the data for the 115 and

56 nm diameter wires fit Debye T^3 law quite well in this temperature range. This suggests that boundary scattering, which is frequency and temperature independent, is the dominant phonon scattering mechanism, such that the thermal conductivity follows the temperature dependence of specific heat.

Natalio Mingo and co-workers [100] presented a theoretical approach to calculate thermal conductivity of semiconductor bulk and nanodevices using an ab initio approach that invokes no adjustable parameters and is valid over a wide temperature range around room temperature. Their approach implements an exact iterative solution of the phonon Boltzmann equation (PBE) for phonon transport, which explicitly incorporates the quantum mechanical phonon-phonon scattering processes and solves self-consistently for the phonon distribution function. The only inputs required for the exact solution of the PBE are the harmonic and anharmonic interatomic force constants (IFCs), and these are determined from first principles using density functional perturbation theory. Without any fitting parameters, they obtained excellent agreement (<5% difference at room temperature) between the calculated and measured intrinsic lattice thermal conductivities of silicon and germanium.

Aksamija et al. [101] presented a calculation of the full thermal conductivity tensor for (001), (111), and (011) surface orientations of the silicon-on-insulator (SOI) nanomembrane, based on solving the Boltzmann transport equation in the relaxation-time approximation with the full phonon dispersions, a momentum-dependent model for boundary scattering, as well as three-phonon and isotope

scattering. The interplay between strong boundary scattering and the anisotropy of the phonon dispersions results in thermal conduction that strongly depends on the surface orientation and exhibits marked in-plane vs. out-of-plane anisotropy, as well as slight in-plane anisotropy for the low-symmetry (011) SOI. In-plane thermal conductivity is highest along (100) on Si (011) and lowest in Si (001) due to the strong scattering of the highly anisotropic TA modes with (001) surfaces.

CHAPTER 2

3D THERMAL PARTICLE-BASED DEVICE SIMULATOR

For properly treating heating in nanometer devices without any significant approximations it is required to solve the coupled Boltzmann transport equations for the electron and phonon systems together. More accurately, the problem is to solve the coupled electron – optical phonons – acoustic phonons – heat bath problem, where each sub-process requires different time scales and need to be addressed individually and added into the complete picture via a self-consistent loop. We, thus, have to solve the coupled system of semi-classical Boltzmann transport equations for the distribution function *f*(k,r,t) for electrons and *g*(k,r,t) for the phonons of the form:

$$\left(\frac{\partial}{\partial t}+v_e(k)\cdot\nabla_r+\frac{e}{\hbar}E(r)\cdot\nabla_k\right)f=\sum_q\left\{W_{e,q}^{k+q\to k}+W_{a,-q}^{k+q\to k}-W_{e,-q}^{k\to k+q}-W_{a,q}^{k\to k+q}\right\}$$

$$\left(\frac{\partial}{\partial t}+v_p(q)\cdot\nabla_r\right)g=\sum_k\left\{W_{e,q}^{k+q\to k}-W_{a,q}^{k\to k+q}\right\}+\left(\frac{\partial g}{\partial t}\right)_{p-p} \qquad (2.1)$$

where $W_{e,q}^{k+q\to k}$ is the electron transition probability from k+q to k due to emission of phonon q. Similarly $W_{a,q}^{k+q\to k}$ is the process of absorption. Since the probabilities W depend on the product $f \bullet g$ of the electron and phonon distribution functions, the system is nonlinear. The scattering terms W result in the transfer of energy

between electrons and phonons and the timescale is in the order of 0.1ps. Phonon velocity, $\boldsymbol{v_p}$ is two orders of magnitude lower than the electron velocity, $\boldsymbol{v_e}$ and this results in a multi-scale problem for the equation set (2.1) since the left hand sides involve different time scales. This implies transfer of heat by the lattice is much slower process than that of charge transfer.

The transfer of energy from electrons to the high-energy optical phonons is very efficient process. But since optical phonons possess negligible group velocity they do not participate significantly in heat diffusion. The optical phonons transfer their energy to acoustic phonons and it is the acoustic phonons that transfer energy away from the heat generation region. The transfer of energy between phonons is relatively slow process and, as a result, a non-equilibrium situation may also exist between optical and acoustic phonons bath. Figure 2.1 shows the main path of transport of thermal energy and the corresponding time constants [113].

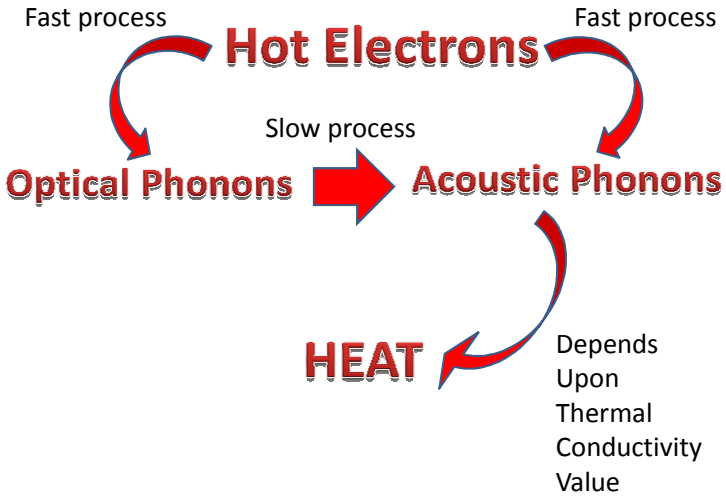

Fig 2.1. The most likely path between energy carrying particles in a semiconductor device is shown along with corresponding scattering time constants [92].

2.1 Derivation of the Hydrodynamic Equations:

According to Fig 2.1, the energy is transported by scattering between electrons and optical phonons (T_{LO}) first, and then optical phonons transfter their energy to acoustic phonons equated with the lattice temperature (T_A) [114]. But, it is very difficult to directly solve phonon Boltzmann equation since mathematically expressing the anharmonic phonon decay process is difficult if not impossible. In addition to this it is required to solve separate phonon Boltzmann equation for each mode of the acoustic and optical branches. So, to simplify the global picture some approximations need to be made. We concentrate more on accurately calculating the I-V characteristic of the device while treating the self-heating

being a by-product of the current flow through the device in a more approximate manner. This approximation is still more accurate than a local heat conduction model. Majumder *et al.* [115], [116] derived the optical phonon and the acoustic phonon energy balance equations from the phonon Boltzmann equations. These energy balance equations can also be derived starting from the energy conservation principle. For high electric field, E ≥ 10^6 V/m, electrons lose their energy to optical phonons and optical phonons decay to acoustic phonons, as shown in Fig 2.1. Using the first law of thermodynamics, the energy conservation equations for optical and acoustic phonons are:

$$\frac{\partial W_{LO}}{\partial t} = \left(\frac{\partial W_e}{\partial t}\right)_{coll} - \left(\frac{\partial W_{LO}}{\partial t}\right)_{coll} \tag{2.2}$$

$$\frac{\partial W_A}{\partial t} = \nabla(\kappa_A \nabla T_A) + \left(\frac{\partial W_{LO}}{\partial t}\right)_{coll} \tag{2.3}$$

where *We,* W_{LO} and W_A are electron, optical phonon and acoustic phonon energy densities, respectively. Here it is assumed that optical phonons group velocity is nearly zero and hence the thermal conductivity associated with them is nearly zero. Next we have

$$dW_{LO} = C_{LO} dT_{LO} \quad \text{and} \quad dW_A = C_A dT_A \tag{2.4}$$

Here C_{LO} is the specific heat capacity for optical phonons and can be estimated from the Einstein model while C_A is the specific heat capacity for acoustic phonons and can be estimated from Debye model. Now, using the relaxation time approximation (RTA), the collision terms can be expressed as

$$\left(\frac{\partial W_e}{\partial t}\right)_{coll} = n \cdot \frac{\frac{3}{2}k_B T_e + \frac{1}{2}m^* v_d^2 - \frac{3}{2}k_B T_{ph}}{\tau_{e-ph}} \tag{2.5}$$

$$\left(\frac{\partial W_{LO}}{\partial t}\right)_{coll} = C_{LO}\frac{T_{LO} - T_A}{\tau_{LO-A}} \tag{2.6}$$

where *Te* is the electron temperature, v_d is the electron drift velocity and T_{ph} is either optical or acoustic phonon temperature depending on which kind of phonons electrons interact with. If we combine Eqs. (2.2)-(2.6), we get:

$$C_{LO}\frac{\partial T_{LO}}{\partial t} = \frac{3}{2}nk_B\left(\frac{T_e - T_{LO}}{\tau_{e-LO}}\right) + \frac{nm^* v_d^2}{2\tau_{e-LO}} - C_{LO}\left(\frac{T_{LO} - T_A}{\tau_{LO-A}}\right) \tag{2.7}$$

$$C_A\frac{\partial T_A}{\partial t} = \nabla(\kappa_A \nabla T_A) + C_{LO}\left(\frac{T_{LO} - T_A}{\tau_{LO-A}}\right) \tag{2.8}$$

The first two terms in the right-hand side of Eq. (2.7) represent the energy gain from the electrons, where n is the electron density and v_d is the drift velocity, while the last term is the energy loss to the acoustic phonons. The latter appears as

a gain term on the RHS of (2.8) while the first term on the RHS of (2.8) accounts for the heat diffusion.

2.2 Discretization of the Hydrodynamic Equations:

The discretization of the 3D Poisson equation is described in Ref. [117] and is not repeated here for compactness of the report. Following the same procedure for the case of spatially varying thermal conductivity, the discretized equation for the lattice temperature is of the form:

$$B_{i,j,k}T_{i,j,k-1} + C_{i,j,k}T_{i,j-1,k} + D_{i,j,k}T_{i-1,j,k} + E_{i,j,k}T_{i,j,k} + F_{i,j,k}T_{i+1,j,k} + G_{i,j,k}T_{i,j+1,k} + H_{i,j,k}T_{i,j,k+1} + f_{i,j,k} = 0 \tag{2.9}$$

where the central coefficient in the seven point stencil is

$$E_{i,j,k} = -(B_{i,j,k} + C_{i,j,k} + D_{i,j,k} + F_{i,j,k} + G_{i,j,k} + H_{i,j,k} + n_{i,j,k} + p_{i,j,k})$$

and the coefficients that couple the central node to the neighboring nodes in the x-, y- and z-direction are calculated using (for temperature and spatially-varying thermal conductivity and general non-uniform mesh)

$$B_{i,j,k} = \frac{2K_{i,j,k-1/2}}{\Delta z_{k-1}(\Delta z_k + \Delta z_{k-1})}; \qquad C_{i,j,k} = \frac{2K_{i,j-1/2,k}}{\Delta y_{j-1}(\Delta y_j + \Delta y_{j-1})};$$

$$D_{i,j,k} = \frac{2K_{i-1/2,j,k}}{\Delta x_{i-1}(\Delta x_i + \Delta x_{i-1})}$$

$$F_{i,j,k} = \frac{2K_{i+1/2,j,k}}{\Delta x_i(\Delta x_i + \Delta x_{i-1})}; \qquad G_{i,j,k} = \frac{2K_{i,j+1/2,k}}{\Delta y_j(\Delta y_j + \Delta y_{j-1})};$$

$$H_{i,j,k} = \frac{2K_{i,j,k+1/2}}{\Delta z_k(\Delta z_k + \Delta z_{k-1})}$$

Equation (2.9) and the 3D Poisson equation are solved using the Incomplete Lower Upper (ILU) decomposition method. Within incomplete factorization schemes [118] for 3D problems, the matrix A is decomposed into a product of lower (L) and upper (U) triangular matrices, each of which has six non-zero diagonals in the same locations as the ones of the original matrix A. The unknown elements of the L and U matrices are selected in such a way that the five diagonals common to both A and A'= LU are identical and the four superfluous diagonals represent the matrix N, i.e., A'=A+N. Thus, rather than solving the original system of equations Ax=b, one solves the modified system LUx=b+Nx, by solving successively the matrix equations LV=b+Nx and V=Ux, where V is an auxiliary vector. It is important to note that the four superfluous terms of N affect the rate of convergence of the ILU method. Stone [119] suggested the introduction of partial cancellation, which minimizes the influence of these

additional terms and accelerates the rate of convergence of the ILU method. By using a Taylor series expansion, the superfluous terms appearing in A' are partially balanced by subtracting approximately equal terms.

For the case of anisotropic thermal conductivity tensor, the derivation of the corresponding partial differential equations and their finite difference versions goes as follow:

$$\kappa\nabla T = \begin{bmatrix} \kappa_{11} & \kappa_{12} & \kappa_{13} \\ \kappa_{21} & \kappa_{22} & \kappa_{23} \\ \kappa_{31} & \kappa_{32} & \kappa_{33} \end{bmatrix} \begin{bmatrix} \partial T/\partial x \\ \partial T/\partial y \\ \partial T/\partial z \end{bmatrix} \tag{2.10}$$

$$= (\kappa_{11} + \kappa_{21} + \kappa_{31})\frac{\partial T}{\partial x} + (\kappa_{12} + \kappa_{22} + \kappa_{32})\frac{\partial T}{\partial y} + (\kappa_{13} + \kappa_{23} + \kappa_{33})\frac{\partial T}{\partial z}$$

$$= \kappa_x \frac{\partial T}{\partial x} + \kappa_y \frac{\partial T}{\partial y} + \kappa_z \frac{\partial T}{\partial z}$$

Then:

$$\nabla \cdot \kappa\nabla T = \frac{\partial}{\partial x}\left(\kappa_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(\kappa_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(\kappa_z \frac{\partial T}{\partial z}\right) \tag{2.11}$$

Now,

$$\frac{\partial}{\partial x}\left(\kappa_x \frac{\partial T}{\partial x}\right) i,j,k = \frac{\kappa_{x_{i+1/2}} \frac{\partial T}{\partial x}|_{i+1/2} - \kappa_{x_{i-1/2}} \frac{\partial T}{\partial x}|_{i-1/2}}{\Delta x}$$

$$= \frac{\kappa_{x_{i+1/2}}}{\Delta x}\frac{T_{i+1} - T_i}{\Delta x} - \frac{\kappa_{x_{i-1/2}}}{\Delta x}\frac{T_i - T_{i-1}}{\Delta x}$$

$$= \frac{\kappa_{x_{i+1/2}}}{\Delta x^2} T_{i+1} - \left(\frac{\kappa_{x_{i+1/2}} + \kappa_{x_{i-1/2}}}{\Delta x^2}\right) T_i + \frac{\kappa_{x_{i-1/2}}}{\Delta x^2} T_{i-1}$$

So,

$$\nabla.\kappa\nabla T = \frac{\kappa_{x_{i+1/2}}}{\Delta x^2} T_{i+1} - \left(\frac{\kappa_{x_{i+1/2}} + \kappa_{x_{i-1/2}}}{\Delta x^2}\right) T_i + \frac{\kappa_{x_{i-1/2}}}{\Delta x^2} T_{i-1}$$

$$+ \frac{\kappa_{y_{j+1/2}}}{\Delta y^2} T_{j+1} - \left(\frac{\kappa_{y_{j+1/2}} + \kappa_{y_{j-1/2}}}{\Delta y^2}\right) T_j + \frac{\kappa_{y_{j-1/2}}}{\Delta y^2} T_{j-1}$$

$$+ \frac{\kappa_{z_{k+1/2}}}{\Delta z^2} T_{k+1} - \left(\frac{\kappa_{z_{k+1/2}} + \kappa_{z_{k-1/2}}}{\Delta z^2}\right) T_k + \frac{\kappa_{z_{k-1/2}}}{\Delta z^2} T_{k-1} \tag{2.12}$$

After rearranging terms we arrive at the following coefficients:

$B_{i,j,k} = \frac{\kappa_{z_{k-1/2}}}{\Delta z^2}$; $C_{i,j,k} = \frac{\kappa_{y_{j-1/2}}}{\Delta y^2}$; $D_{i,j,k} = \frac{\kappa_{x_{i-1/2}}}{\Delta x^2}$, $F_{i,j,k} = \frac{\kappa_{x_{i+1/2}}}{\Delta x^2}$; $G_{i,j,k} = \frac{\kappa_{y_{j+1/2}}}{\Delta y^2}$; $H_{i,j,k} = \frac{\kappa_{z_{k+1/2}}}{\Delta z^2}$ and $E_{i,j,k} = -\left[\frac{\kappa_{x_{i+1/2}} + \kappa_{x_{i-1/2}}}{\Delta x^2} + \frac{\kappa_{y_{j+1/2}} + \kappa_{y_{j-1/2}}}{\Delta y^2} + \frac{\kappa_{z_{k+1/2}} + \kappa_{z_{k-1/2}}}{\Delta z^2}\right]$.

These coefficients are then substituted into Eq. (2.9) which is solved using the ILU method.

The justification for the diagonal approximation for the thermal conductivity tensor is evident from the results presented in Figures 2.2-2.4 where we plot all the components of the thermal conductivity tensor for different crystallographic directions as calculated by Aksamija and co-workers [120].

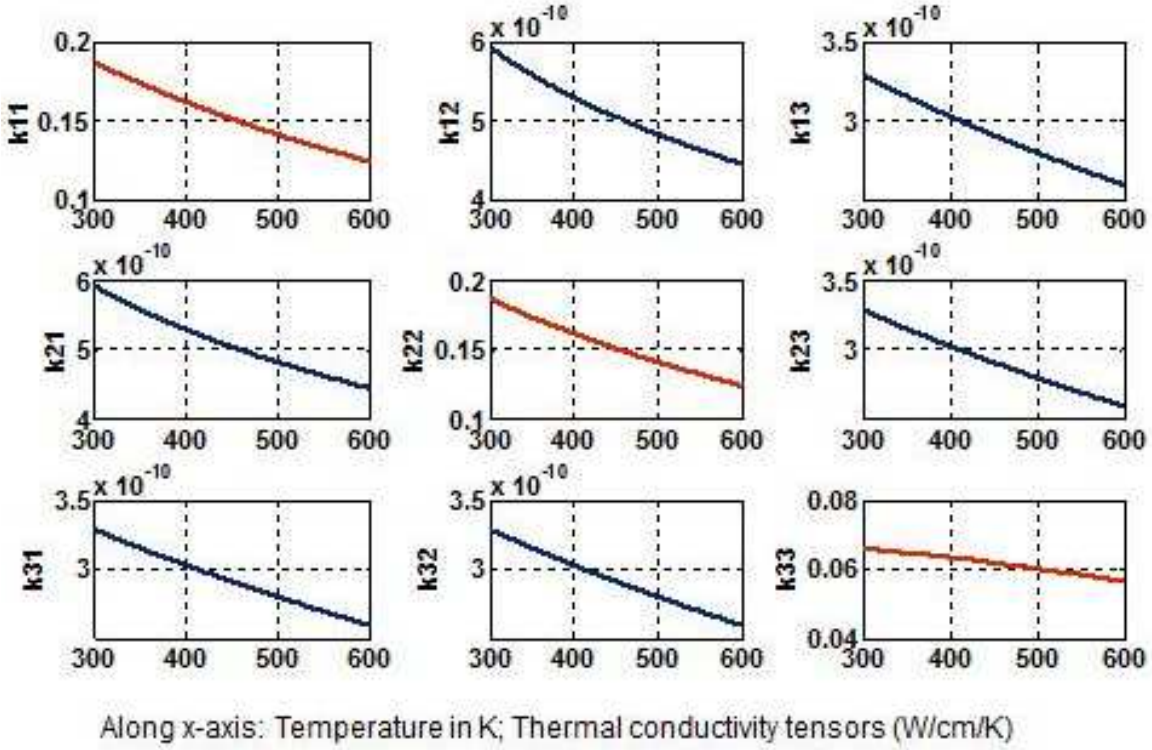

Figure 2.2 Thermal conductivity tensor temperature dependence for (100) surface orientation. Notice that the off-diagonal thermal conductivity tensor values are much smaller than the diagonal ones [120].

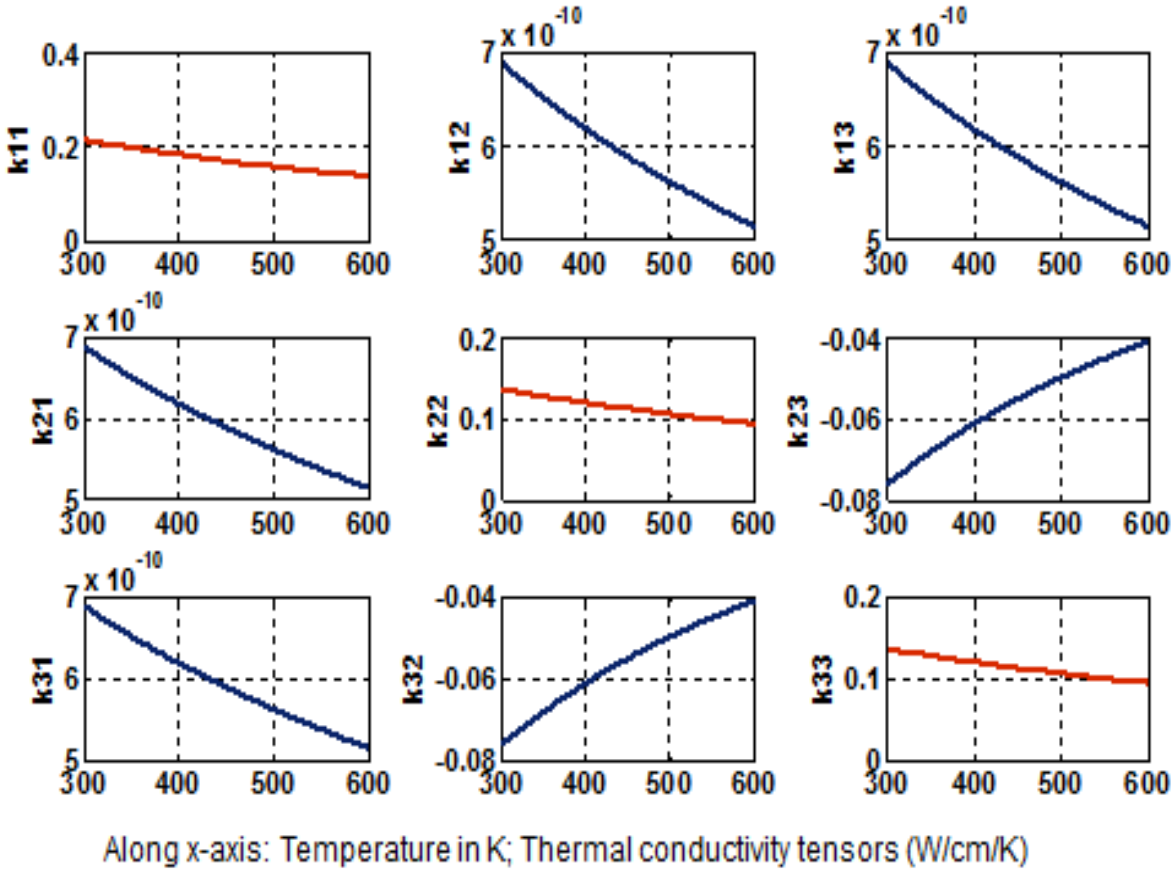

Figure 2.3 Thermal conductivity tensor temperature dependence for (110) surface orientation. Notice that the off-diagonal thermal conductivity tensor values are much smaller than the diagonal ones [120].

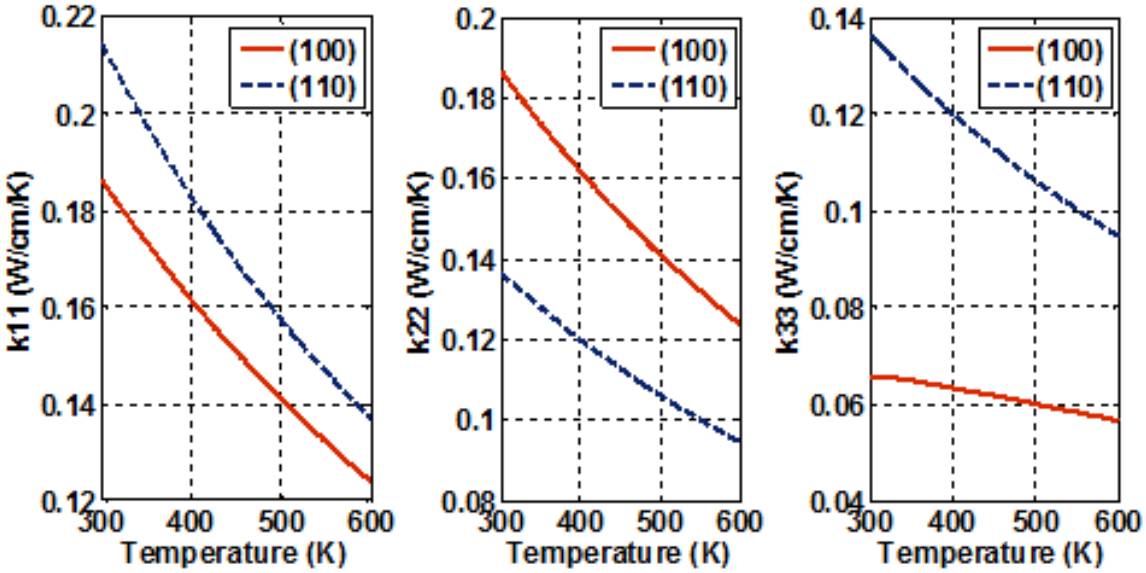

Figure 2.4 Comparison of diagonal thermal conductivity tensors temperature dependence for (100) and (110) surfaces. k11 corresponds to k_{xx}, k22 to k_{yy} and k33 to k_{zz}.

2.3 Boundary Conditions and Averaging and Smoothing of Variables:

2.3.1 Equivalence between ϕ and T:

From Fourier's law, the 1D heat flux is given by $q = -\kappa\, dT/dx$, where q is the heat flux vector, T is the local temperature and κ is the thermal conductivity. Ohm's law on the other hand gives that $J = \sigma E = -\sigma\, d\phi/dx$. Therefore heat flux is analogous to current density and temperature corresponds to electrostatic potential.

2.3.2 Proper boundary conditions:

When we solve Poisson's equation for the electrostatic potential ϕ, at least one node in the device must have Dirichlet boundary conditions connecting the simulated system to the environment. In an analogous manner, to properly solve the phonon energy balance equations, the device should be attached to a heat sink somewhere along the boundary. The thermal boundary conditions chosen need to reflect the physics of the individual device, as well as those in the surrounding environment. The substrate is typically treated as a thermal contact in commercial simulation packages such as the Silvaco ATLAS simulation package [121] (THERMAL3D module). In the case of SOI technology, the boundary condition should be applied to the bottom of the Si substrate. It has been shown by Raleva *et al.* [122] that, due to the relatively high thermal conductivity of Si, assuming 300K on the back of the BOX layer is actually a good approximation. Assuming a worst case scenario that all neighboring devices are fully turned on, then Neumann boundaries should be used on the sides to reflect that no net heat transfer occurs between identical devices. On the top surface, neglecting radiation losses and thermal conduction to the air, Neumann conditions are appropriate as well given the relative small degree of heat conduction in this direction. However, metallic interconnects such as the gate, source and drain contacts, do have a high thermal conductivity, and can serve as effective heat sinks (assuming this heat is transferred away from the device and not to adjacent devices). In this present work, we have treated the gate metal as a potential heat

sink, and have left the source and drain floating (Neumann boundary conditions), which is consistent with prescriptions given in the Silvaco ATLAS package. In fact, Raleva *et al.* [122] considered the change of thickness of the gate metal and the boundary condition at the end of the gate, and did not observe much influence on the current degradation, where the gate metal was treated as a material characterized by its own thermal conductivity. Since current nano-scale devices use metal gates to avoid poly-silicon depletion, an isothermal assumption is justifiable.

2.3.3 Electro-Thermal Particle-Based Device Simulator Description

Figure 2.5 shows the generic flow chart of the coupled electron EMC/phonon balance equation solver developed as part of this research. Since it is difficult to couple a particle based picture for electrons (which is inherently noisy) with a continuum model for the phonons, the variables taken from the Monte Carlo (MC) solver (e.g. the electron density, drift velocity and temperature) must go through both temporal and spatial averaging to achieve convergence of the coupled scheme. The smoothness of the variables being transferred to the energy balance solver depends on the number of simulated particles in the model. The BTE for electrons is solved within each 'outer iteration' using the Ensemble Monte Carlo (EMC) method for a time period of 10 ps to ensure that steady state conditions have been achieved. The required variables are then passed to the thermal solver, which gives the updated optical and acoustic phonon

temperatures. This constitutes one Gummel cycle or "one outer iteration" [123], [124].

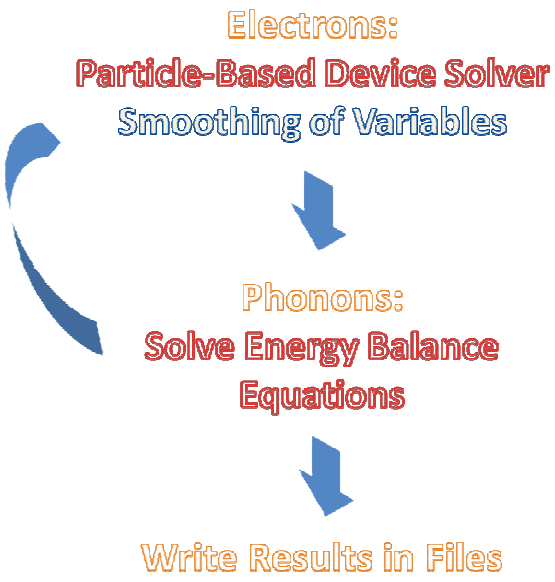

Figure 2.5 Flow-chart of the ASU electro-thermal simulator.

Next we introduce the concept of temperature dependent scattering tables which are needed to couple the spatially dependent phonon temperatures solved on a grid over the device domain to the particle based EMC. We create one energy dependent scattering table for each combination of acoustic and optical phonon temperature [125], [126]. These scattering tables introduce more steps in the EMC phase shown in Figure 2.6 on the right panel. This is because to choose a scattering mechanism for a given electron energy it is necessary to find the corresponding scattering table. In order to do that electron's position on the grid is identified first to find the acoustic and optical phonon temperatures in that grid

point and then the scattering table with "coordinates" (T_L,T_{LO}) is selected. These scattering tables are pre-calculated in the initialization stages of the simulation for a range of temperatures and do not require much CPU time or memory resources. An interpolation scheme is then used for temperatures for which there are no appropriate scattering table.

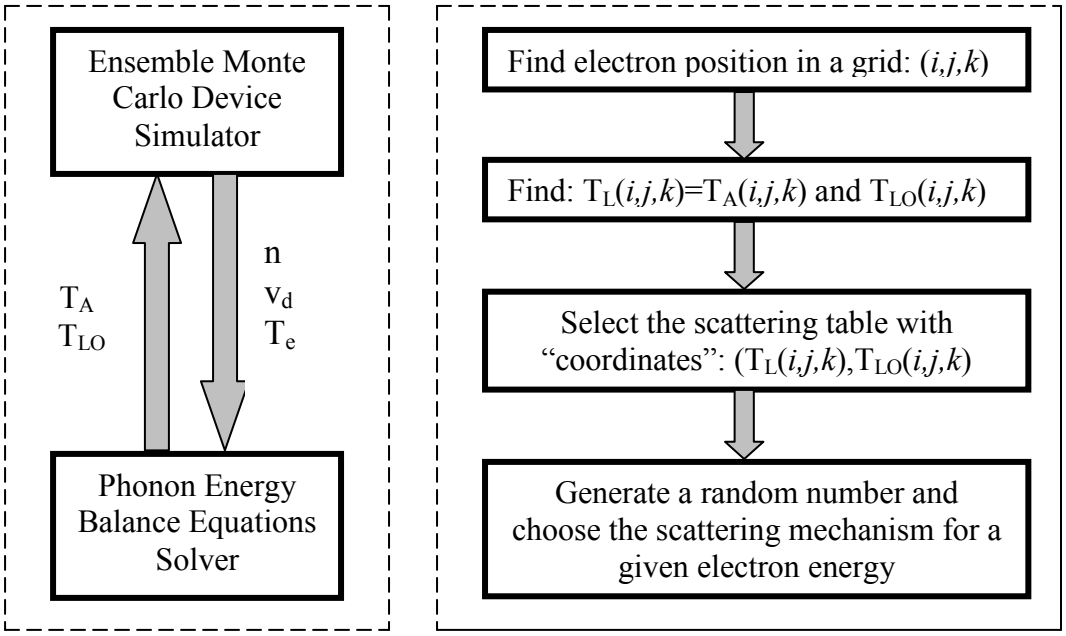

Figure 2.6 Left panel – Exchange of variables between the two kernels. Right panel: Choice of the proper scattering table [113].

It is required to do a space-time averaging and smoothing of electron density, drift velocity and electron energy to properly connect the particle-based picture of electron transport with the continuous, "fluid-like" phonon energy balance

equations. The electrons are assigned to their nearest grid point at the end of each MC time step after the MC simulation phase has reached steady state. Then an averaging is done for the drift velocities and thermal energies with the number of electrons at the corresponding grid points. After the MC phase, a time averaging of the electron density, drift velocity and thermal energy is performed, and the electron temperature distribution is calculated. It is assumed that the drift energy is much smaller than the thermal energy. Most of the grid points, especially at the interfaces, are rarely populated with electrons and as a result the smoothing of these variables is necessary. Otherwise, this may lead to artificially low lattice temperatures in those points, unless sufficient statistics are gathered. The exchange of variables between electron and phonon solvers is shown on the left panel of Figure 2.6.

CHAPTER 3

SIMULATION RESULTS

3.1 Constant Thermal Conductivity Results

The dimensions of the silicon nanowire transistor (SNWT) being investigated at present are the following: The channel length is 10 nm; the silicon film width, which is equal to the source/drain junction depth, is 7 nm; the channel width is 10 nm; the BOX width is 10 nm; the source/drain doping is 1×10^{19} cm^{-3}; and the channel doping is 1×10^{17} cm^{-3}. For the case when we use constant thermal conductivity, the thermal conductivity value is set to 13 W/m/K.

For simulating the steady-state behavior of the device, we start the system in some initial condition, with the desired potential applied to the contacts. Then the simulation is run in time steps until it reaches steady-state. A common initial condition to start with is charge neutrality where particles are assigned randomly according to the device doping profile, so that, initially, the system is charge neutral on the average. After the charges are assigned randomly in the device, we then assign charges to each mesh point by using a particle-mesh coupling method and solve Poisson's equation. Next, the forces get interpolated on the grid and the particles are accelerated over the next time step. After the system reaches steady-state and MC simulation time ends, we calculate the steady-state current through a specified terminal.

At this point, the average electron density, drift velocity, and electron temperature are calculated on a grid to feed into the thermal part of the simulation. The electron thermal energy is much larger than the electron drift energy and electron temperature is calculated from the thermal energy.

The phonon energy balance equation is then solved and the acoustic and optical phonon temperatures are calculated. Dirichlet boundary condition is applied at the gate contact and at the bottom of the BOX and is set to 300K during simulation. Neumann boundary conditions for the heat transfer are used in all other outer surfaces. The tolerance used in the "thermal" ILU algorithm is 0.001 and leads to very fast convergence.

After the phonon temperatures are calculated from the phonon energy balance equations, they are fed back to the next starting point of the MC free-flight scattering phase. Now, we have scattering table for each mesh point corresponding to the acoustic and optical phonon temperatures of that point. So, the electron position defines which scattering table to be used and then by generating a random number, the scattering mechanism is chosen for the given electron energy [130].

At the device plane under the gate oxide, we have made two choices to see the role of the gate electrode. In case 1 we have assumed that the gate electrode is far from the device active region and in case 2 we have assumed that we have copper metal gates in the proximity of the channel. Copper has thermal conductivity of 400 W/m-K. In both case 1 and case 2 Neumann boundary conditions are

assumed at the edges of the metal boundaries. Results for both case 1 and case 2 are summarized in Figure 3.1 [131], [132]. From the results presented in the middle and bottom panel of Figure 3.1 we might conclude the following:

- Both lattice and optical phonon temperatures are higher for the structure described as case 1 and the acoustic and optical phonon temperatures are strongly dependent upon the size of the silicon contact area.
- For structure described as case 2 we see that the metal contacts transfer the heat very effectively which leads to smaller lattice and optical phonon temperatures. Thus, we might conclude that if we want effective heat removal in the structure we need to have the metal contacts as close as possible to the active channel region. This is very important conclusion from a circuits design standpoint.
- In the bottom panels of Figure 3.1 we plot the optical phonon temperatures for case 1 and case 2. In both cases the optical phonon bottleneck discussed in conjunction with Figure 2.1 is evident.
- The larger lattice heating for case 1 leads to larger current degradation which is evident from the results presented in Figure 3.2, where we plot the convergence of the solver and in Figure 3.3 where we plot the drift velocity for $V_G=V_D=1$ V.

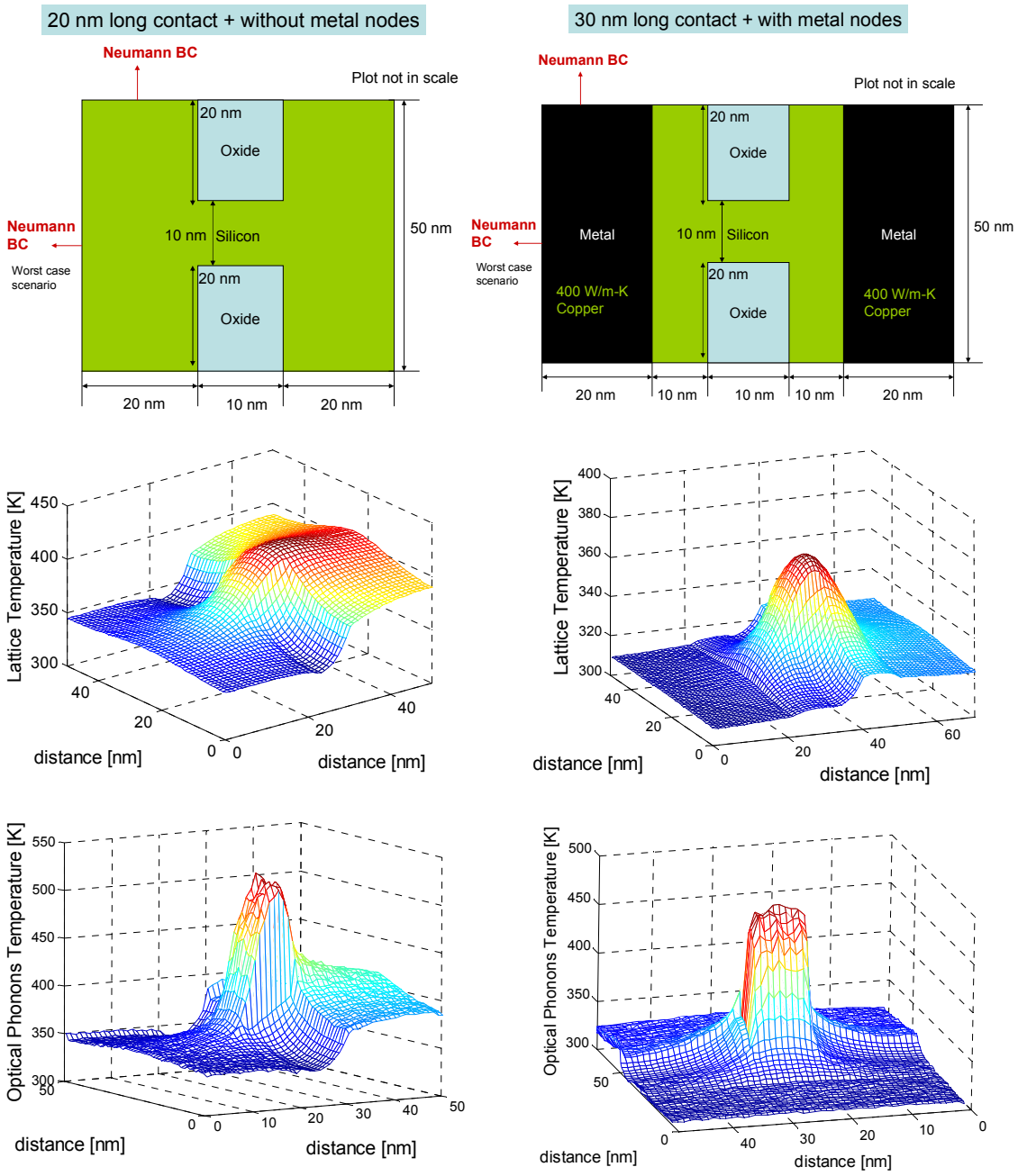

Figure 3.1. Top left panel – plane underneath the gate oxide for case1. Top right panel – plane underneath the gate oxide for case 2. Middle panel – acoustic phonon temperature (left – case 1, right – case2). Bottom panel optical phonon temperature (left – case 1, right – case 2).

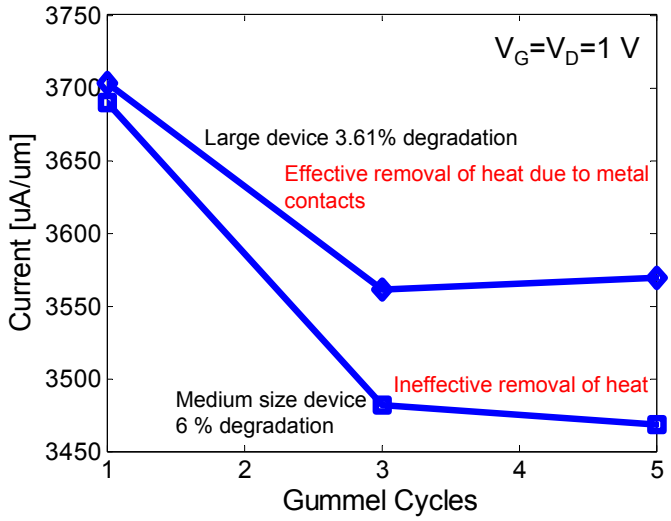

Figure 3.2. Convergence of the electro-thermal solver for case 1 (medium size devise) and case 2 (large size device) Gummel cycle=1 corresponds to isothermal case.

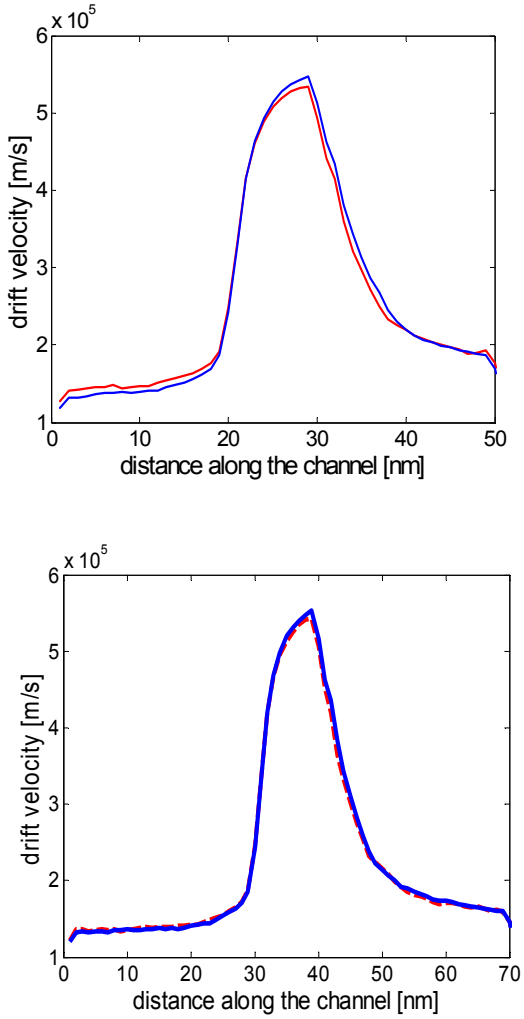

Figure 3.3. Average drift velocity for V_G=V_D=1 V for case 1 – top panel and case 2 – bottom panel. Solid lines are isothermal simulations and dashed lines are electro-thermal simulations.

3.2 Constant vs. Temperature Dependent Thermal Conductivity Model

We next show in Figs. 3.4-3.10 for the constant and Figs. 3.11-3.17 for the case of the temperature dependent thermal conductivity model the optical and the lattice temperature profiles for different bias conditions: V_G=0.8, 0.9 and 1.0 V and V_D=0.8, 0.9 and 1.0 V. As expected, in both the constant and the temperature dependent thermal conductivity model there are hot-spots at the drain end of the channel and in all the bias combinations considered the optical phonons represent, due to their dispersion-less nature, significant barrier to the heat flow. Both the acoustic/lattice and the optical phonons temperatures progressively increase with increasing either the gate or drain bias. In the case when gate bias is increased, more carriers exist in the channel that can acquire significant energy from the electric field. For the case of increasing drain bias, electric fields are higher which accelerates the carriers to higher energy states. The peak optical phonon and lattice temperatures for the case of constant and temperature dependent thermal conductivity model are shown in Fig. 3.19. Yet another feature that characterizes the results for constant and temperature dependent thermal conductivity models is the fact that there is much larger lattice temperature hot spot for the case of the temperature dependent thermal conductivity [133].

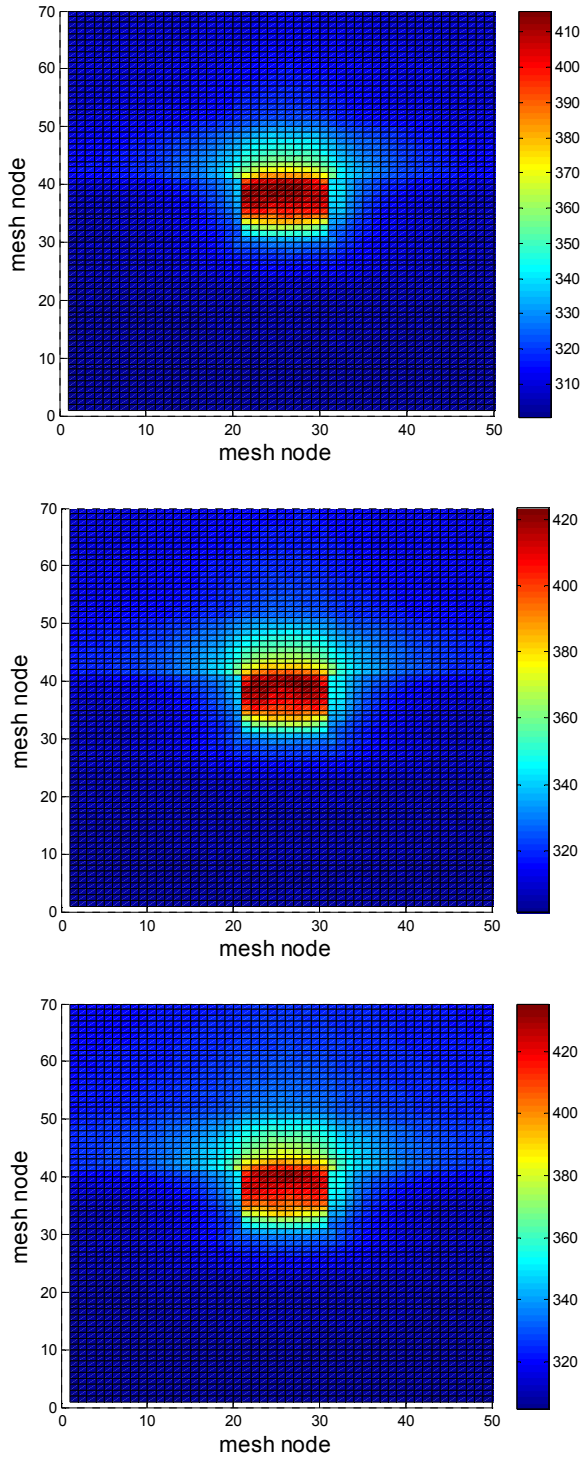

Figure 3.4 Optical phonon temperature for the case of VG=0.8 V and VD=0.8, 0.9 and 1.0 V. Constant thermal conductivity model is used in these simulations.

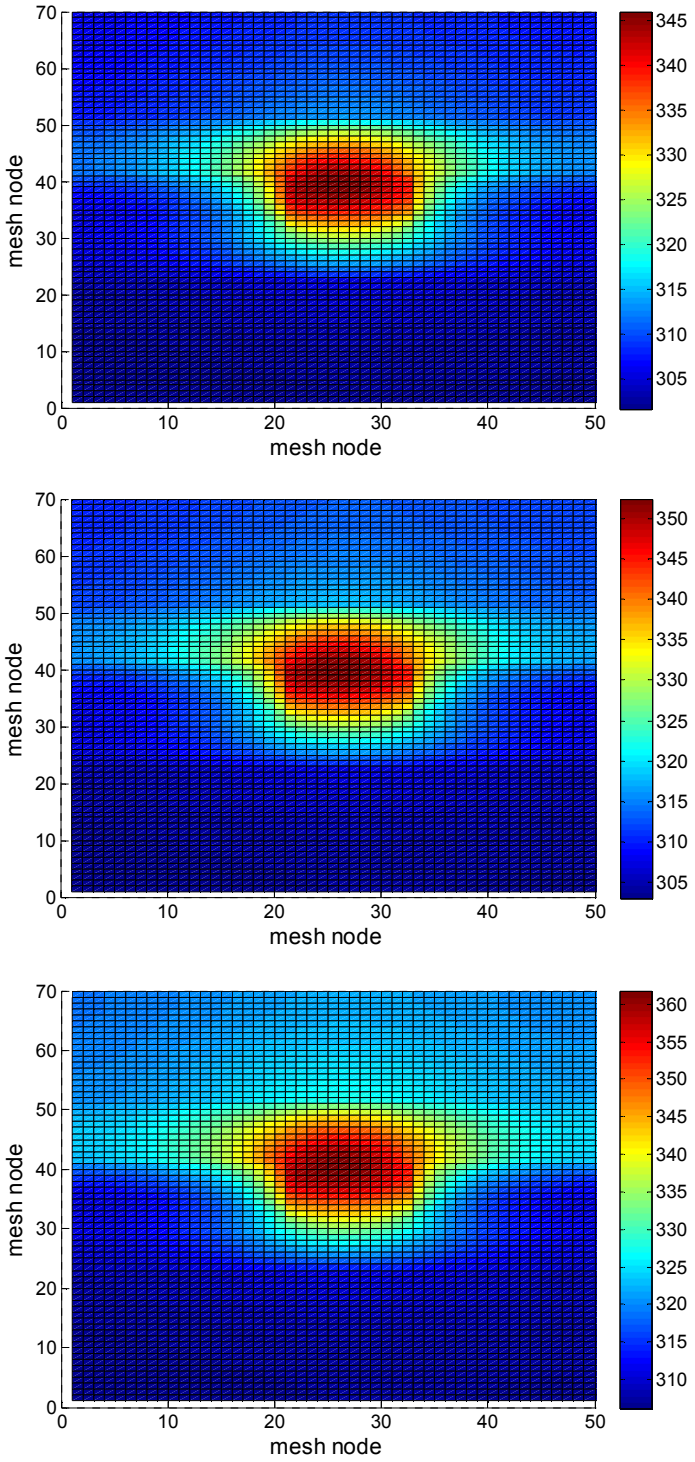

Figure 3.5 Lattice temperature profile for the case of constant thermal conductivity model. VG=0.8 V and VD=0.8, 0.9, and 1.0 V.

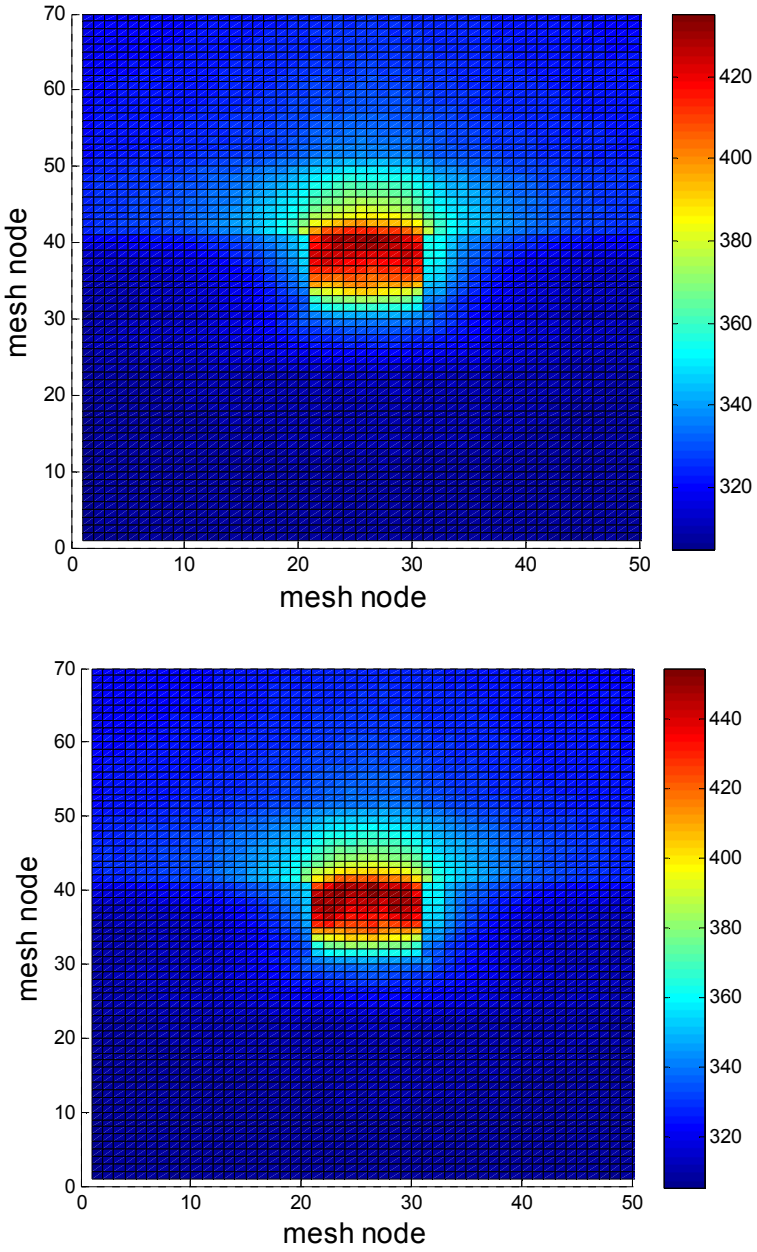

Figure 3.6 Optical temperature profile for the case of constant thermal conductivity model. VG=0.9 V and VD=0.9 and 1.0 V.

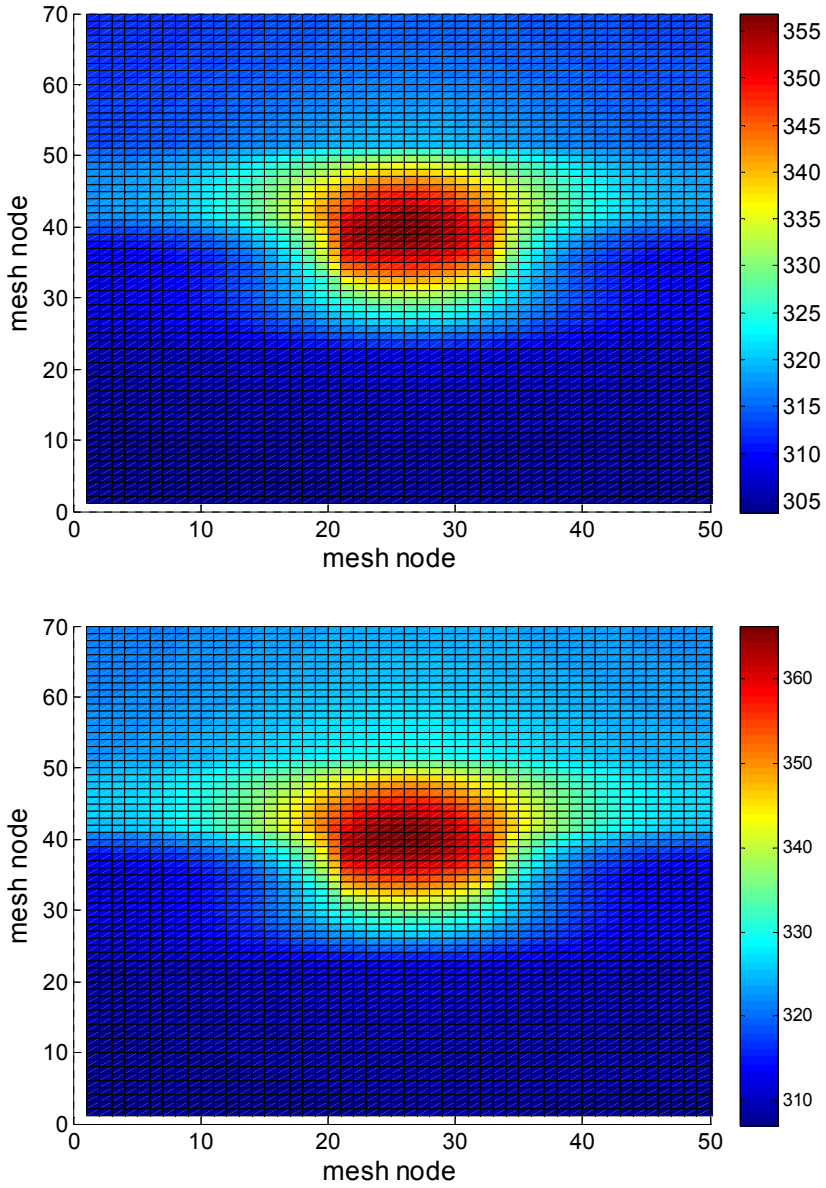

Figure 3.7 Lattice temperature profile for the case of constant thermal conductivity model. VG=0.9 V and VD=0.9 and 1.0 V.

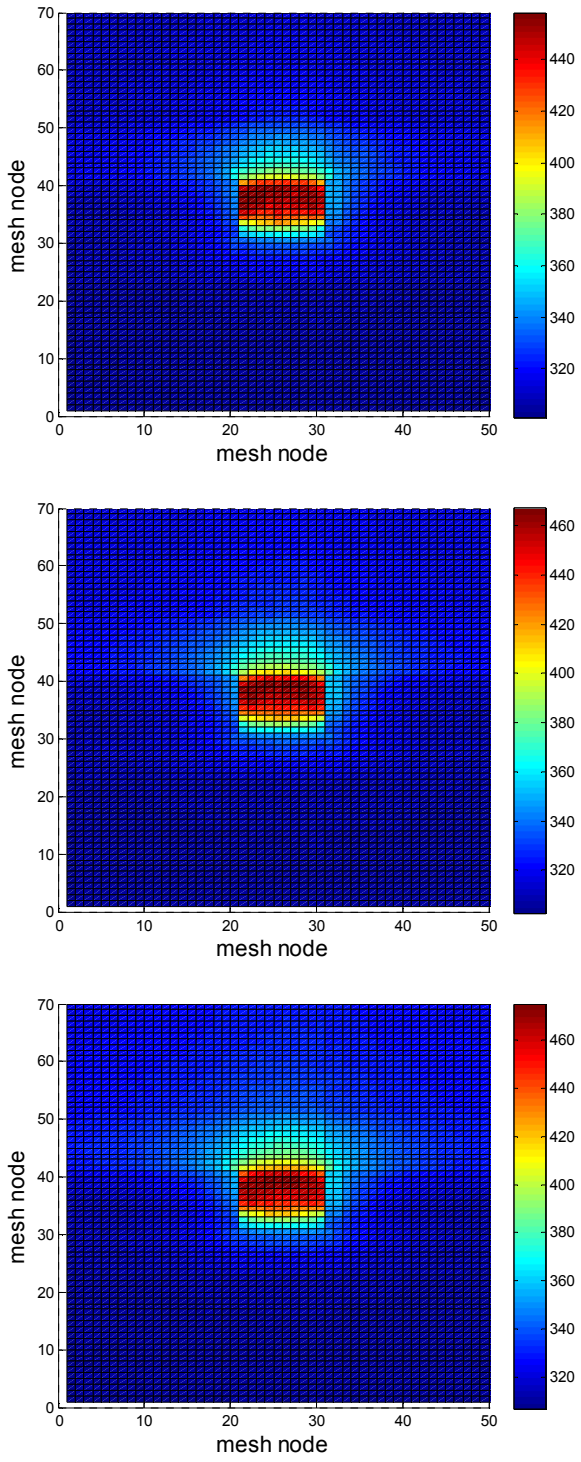

Figure 3.8 Optical temperature profile for the case of constant thermal conductivity model. VG=1.0 V and VD=0.8, 0.9, and 1.0 V.

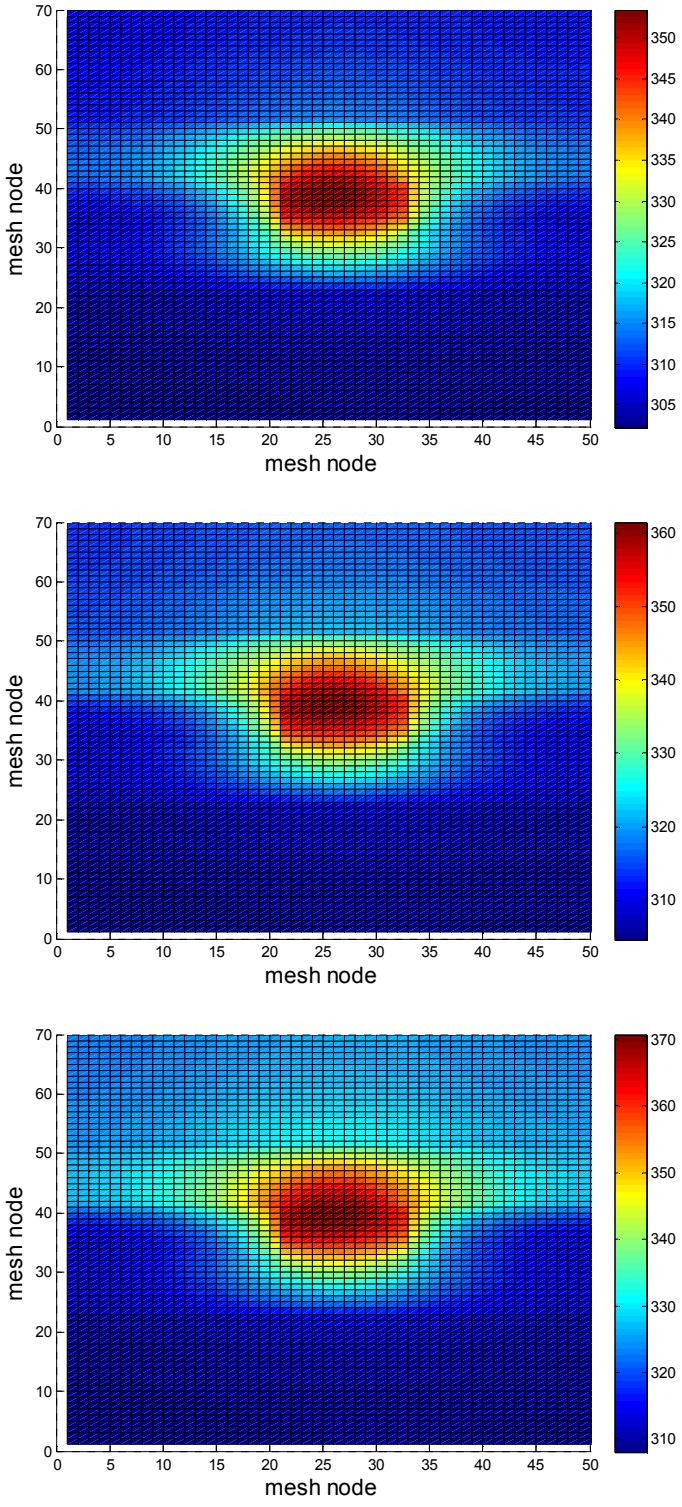

Figure 3.9 Lattice temperature profile for the case of constant thermal conductivity model. VG=1.0 V and VD=0.8, 0.9, and 1.0 V.

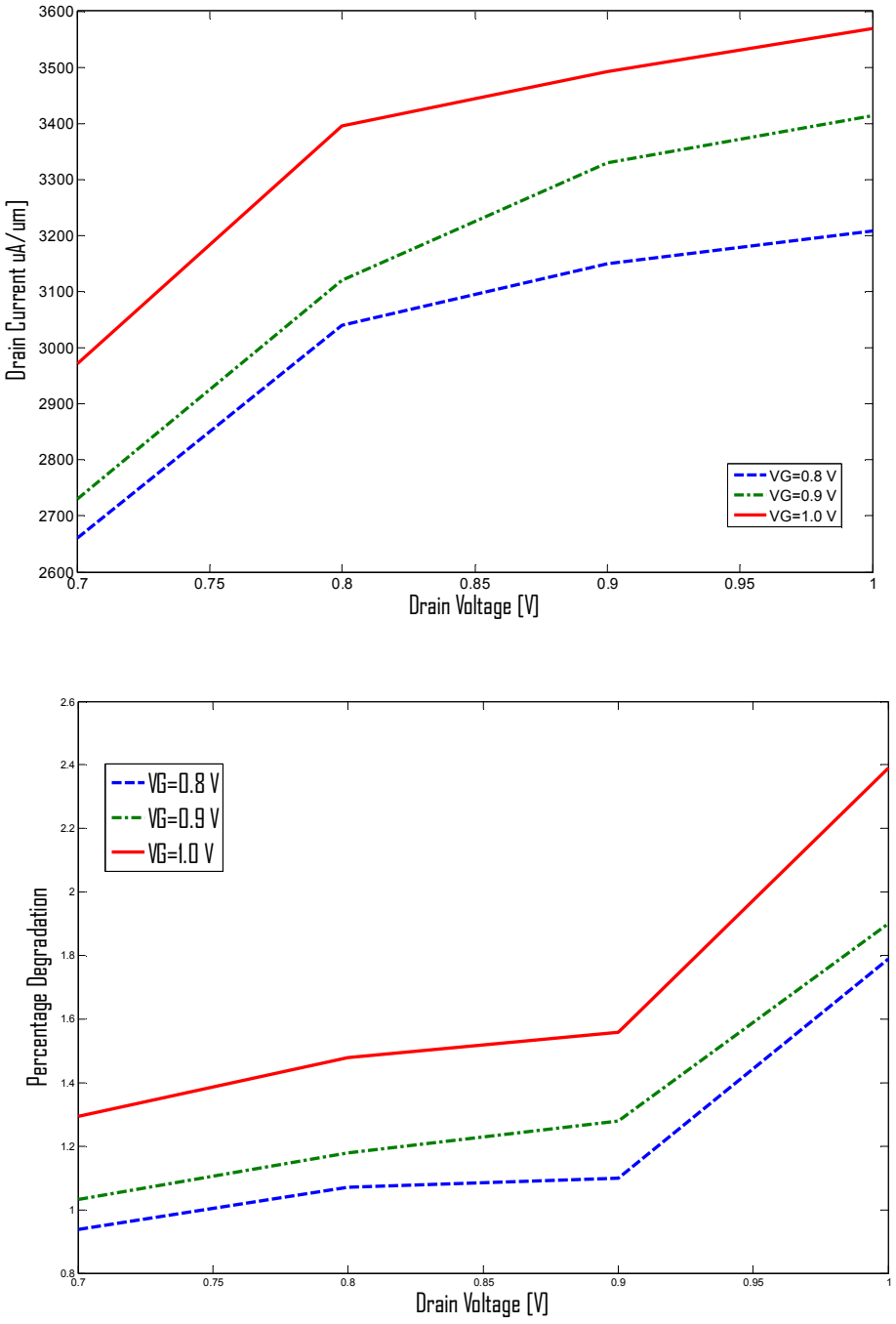

Figure 3.10 IV Characteristics (top panel) and current degradation (bottom panel) for the case of the constant thermal conductivity model. Notice that the current degradation increases significantly for VG=1 V due to the larger density of carriers in the channel which is able to accumulate more excess energy.

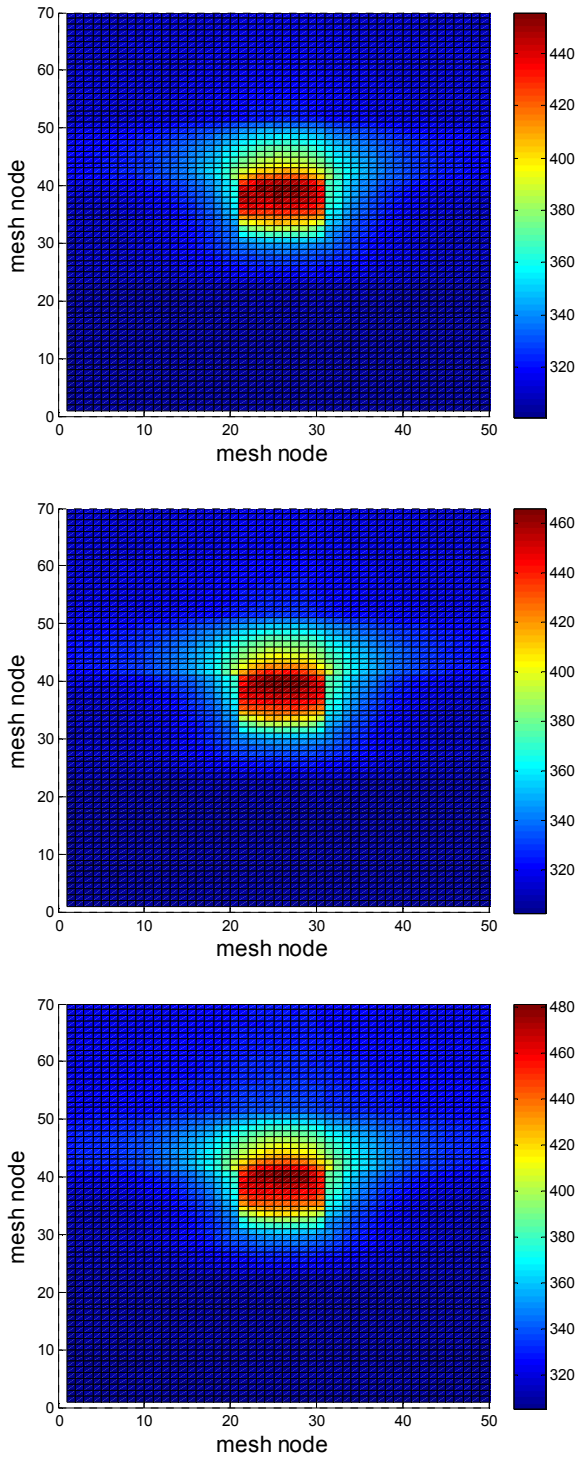

Figure 3.11 Optical phonon temperature for the case of VG=0.8 V and VD=0.8, 0.9 and 1.0 V. Thickness and temperature dependent thermal conductivity model is used in these simulations.

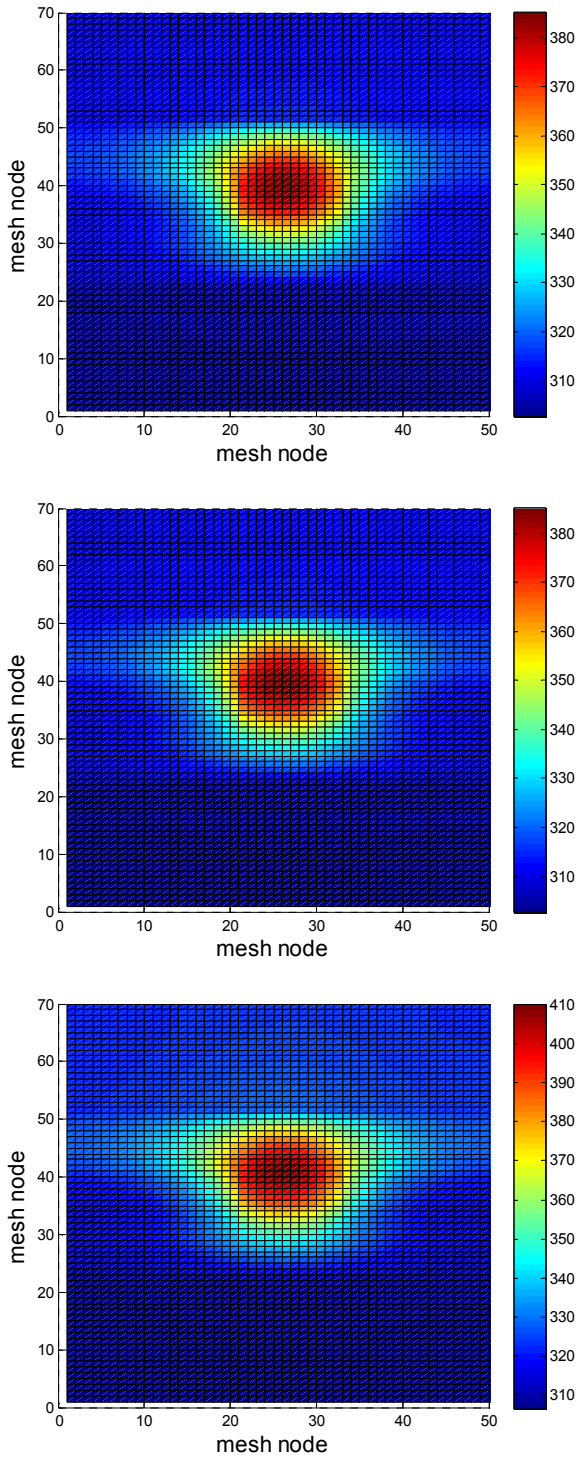

Figure 3.12 Lattice temperature for the case of VG=0.8 V and VD=0.8, 0.9 and 1.0 V. Thickness and temperature dependent thermal conductivity model is used in these simulations.

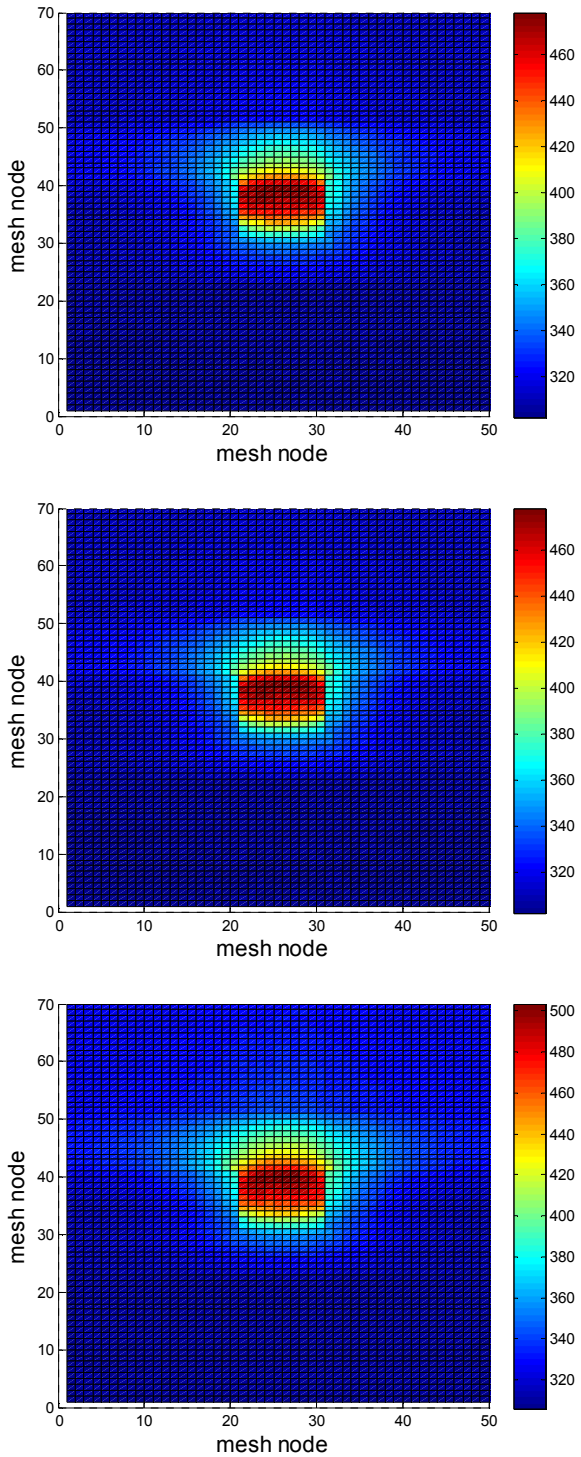

Figure 3.13 Optical phonon temperature for the case of VG=0.9 V and VD=0.8, 0.9 and 1.0 V. Thickness and temperature dependent thermal conductivity model is used in these simulations.

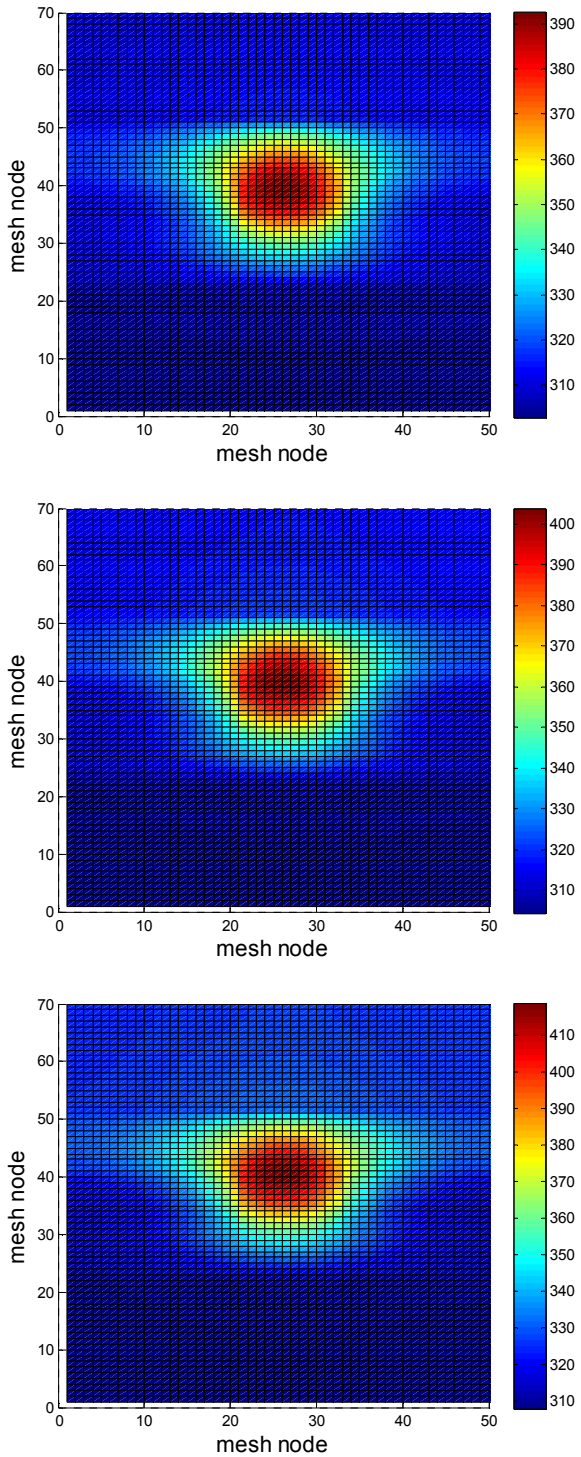

Figure 3.14 Lattice temperature for the case of VG=0.9 V and VD=0.8, 0.9 and 1.0 V. Thickness and temperature dependent thermal conductivity model is used in these simulations.

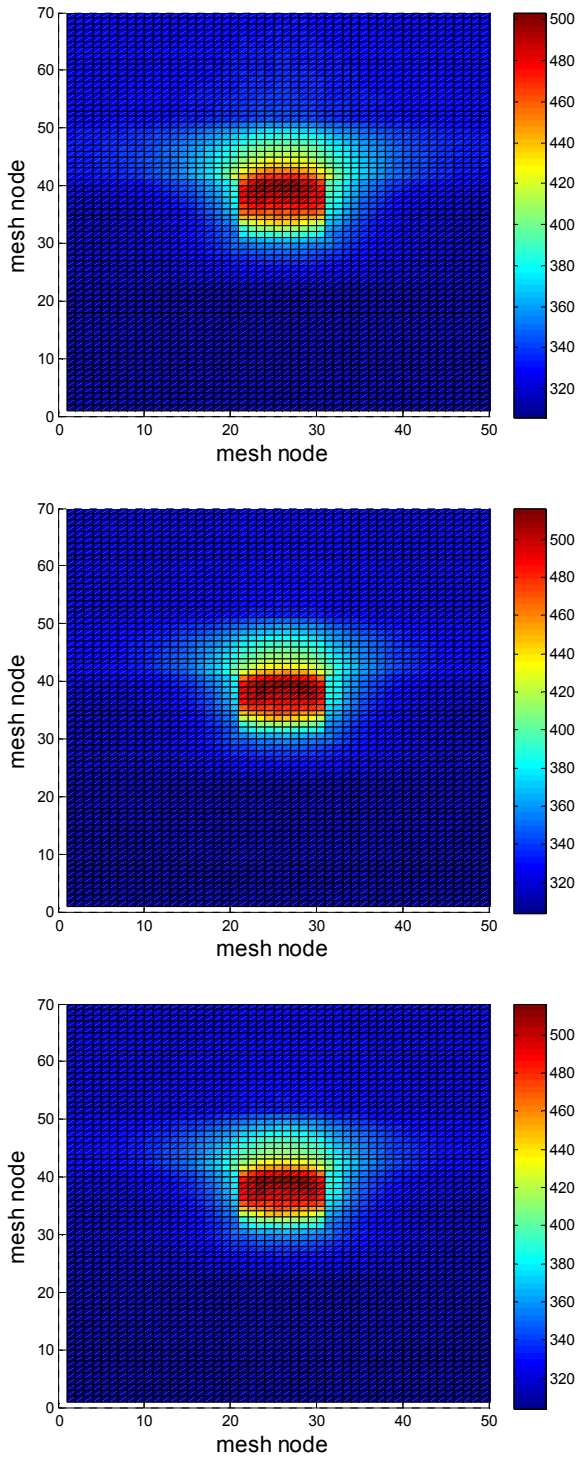

Figure 3.15 Optical phonon temperature for the case of VG=1.0 V and VD=0.8, 0.9 and 1.0 V. Thickness and temperature dependent thermal conductivity model is used in these simulations.

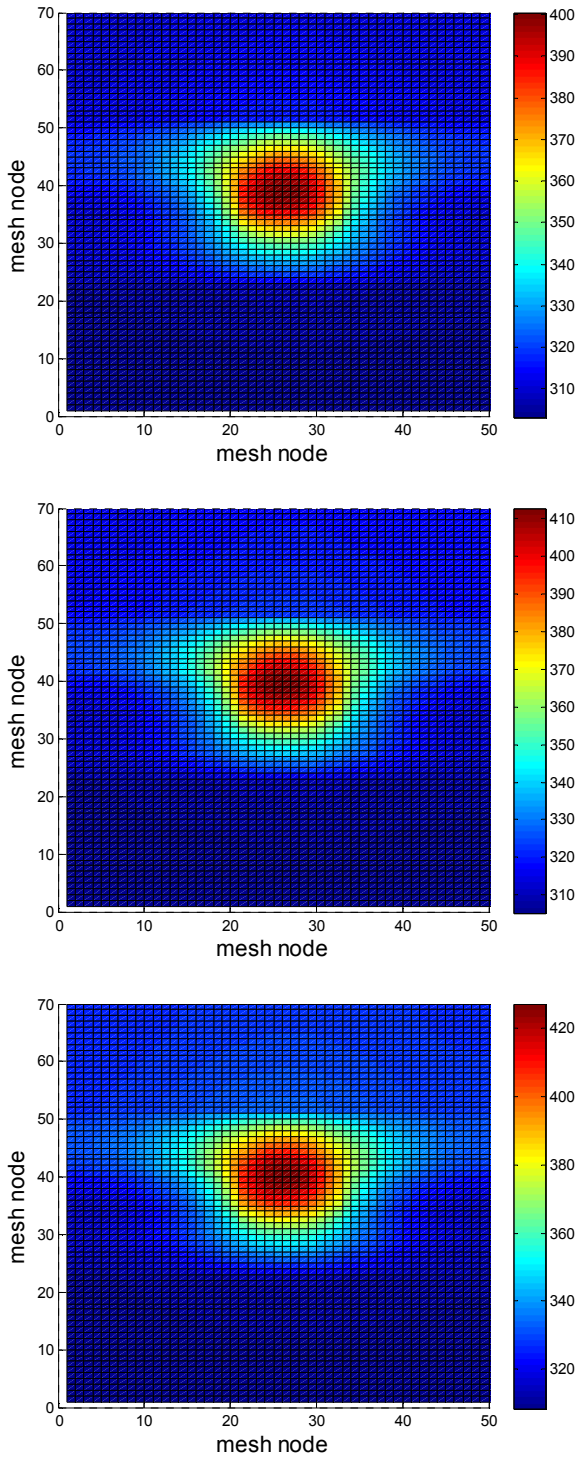

Figure 3.16 Lattice temperature for the case of VG=1.0 V and VD=0.8, 0.9 and 1.0 V. Thickness and temperature dependent thermal conductivity model is used in these simulations.

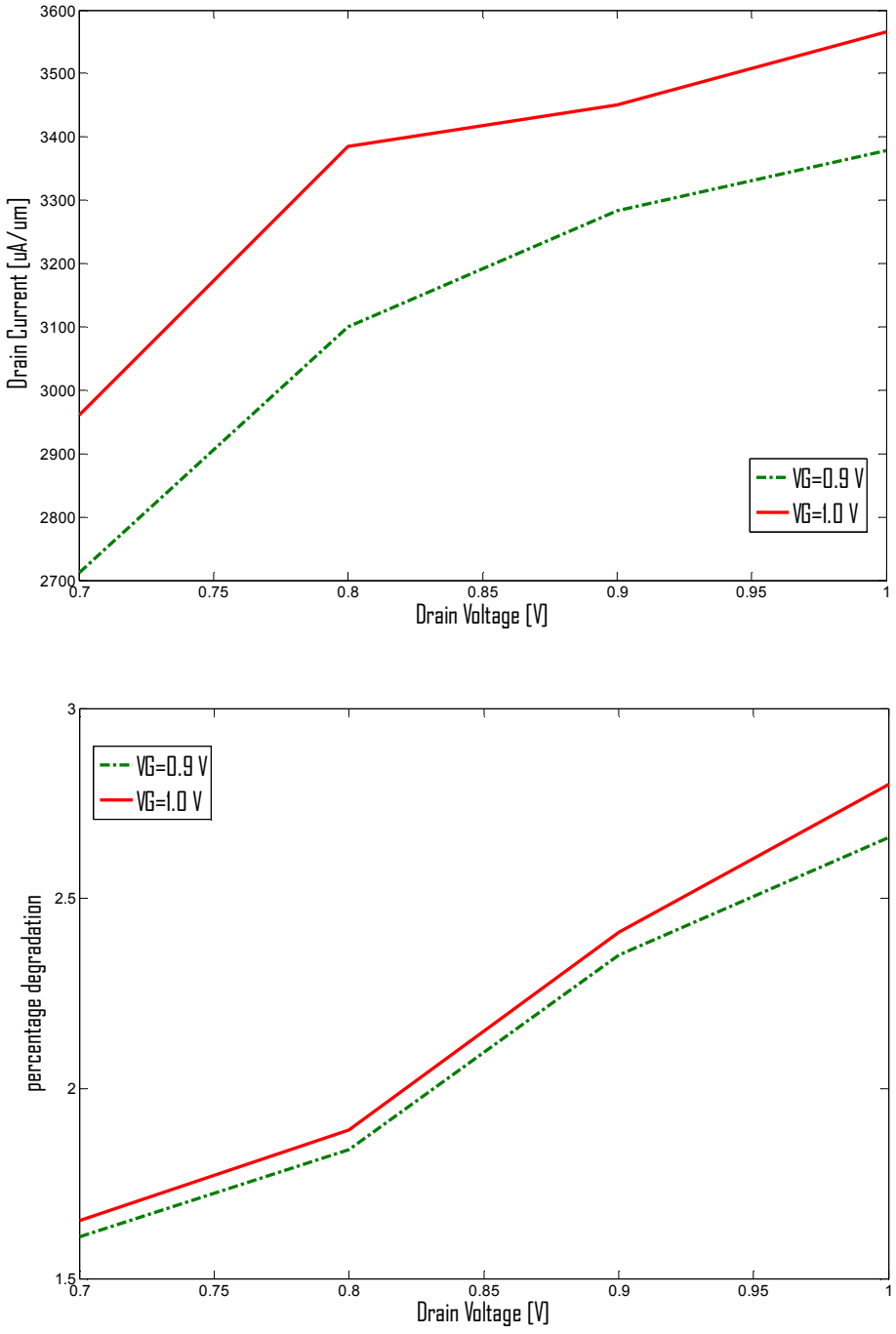

Figure 3.17 IV Characteristics (top panel) and current degradation (bottom panel) for the case of the temperature and thickness dependent thermal conductivity model. Notice that the current degradation increases significantly for VG=1 V due

to the larger density of carriers in the channel which is able to accumulate more excess energy.

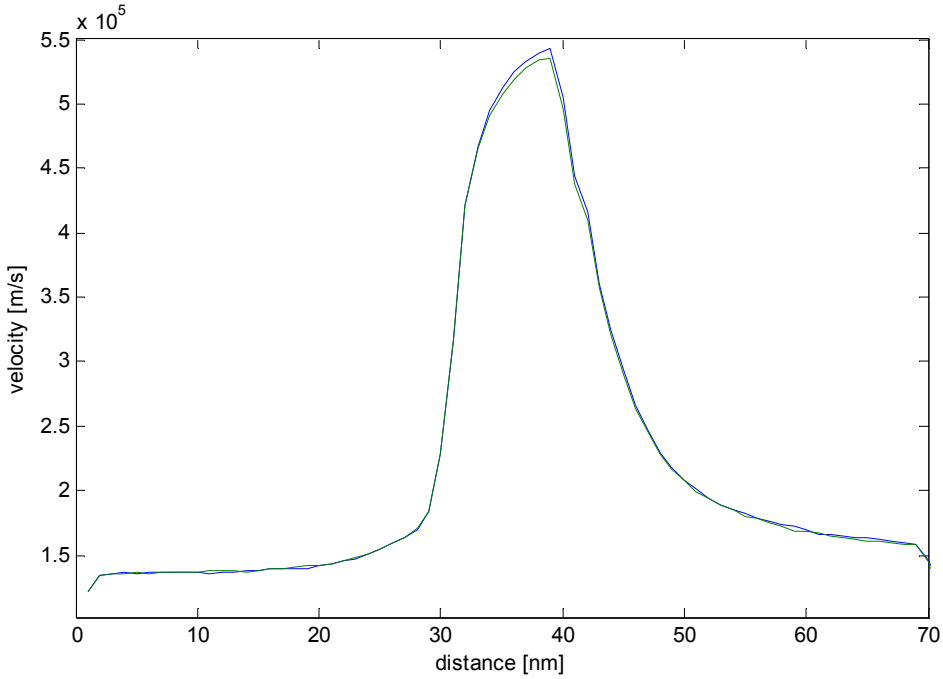

Figure 3.18 Velocity along the channel for VG=VD=1.0 V for the case of a constant and temperature and thickness dependent thermal conductivity model. As expected, the inclusion of the temperature dependence in the thermal conductivity leads to slight degradation in the peak drift velocity as the thermal conductivity is reduced. This is reflected in the results presented in Fig. 3.19 for the case of constant and temperature dependent thermal conductivity model. The peak lattice temperatures are higher for the case of temperature dependent thermal conductivity model.

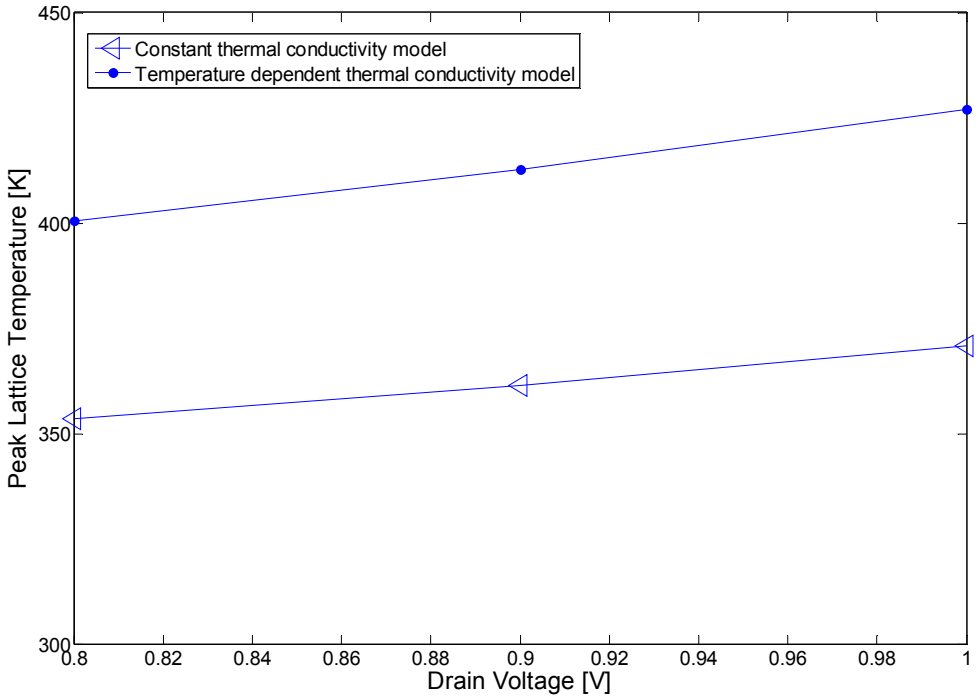

Figure 3.19 Peak temperatures for the case of constant/temperature dependent thermal conductivity model.VG=1. V and VD=0.8, 0.9 and 1.0 V.

3.3 Simulation Results for the case of anisotropic thermal conductivity tensor

Anisotropy in the thermal conductivity is accounted for using the equations for the acoustic phonon balance equation given in expressions (2-12). To study transport in 'arbitrary' crystallographic directions further modifications of the original Monte Carlo device simulator designed for transport in [100] crystallographic direction had to be made. The code is still not developed in its final state as interface-roughness is not properly accounted for. In fact, different crystallographic directions such as [100] and [110] have different values for interface roughness. Nevertheless, the thermal conductivity aspects are being

preserved and for [100] direction higher peak lattice temperatures are observed when compared to [110] case. The peak lattice temperature for [100] direction is 481.1 K and the peak lattice temperature for the [110] direction is 467.8 The two temperature profiles are shown in Figure 3.20 below. The current degradations are in accordance with the peak lattice temperatures. Namely, for [100] orientation of current transport, the current degradation due to self-heating effects is 2.4% and for [110] orientation of the current transport is 2.2%. Again, very small values for the current degradation are obtained because of the ballistic nature of the carrier transport in the structure.

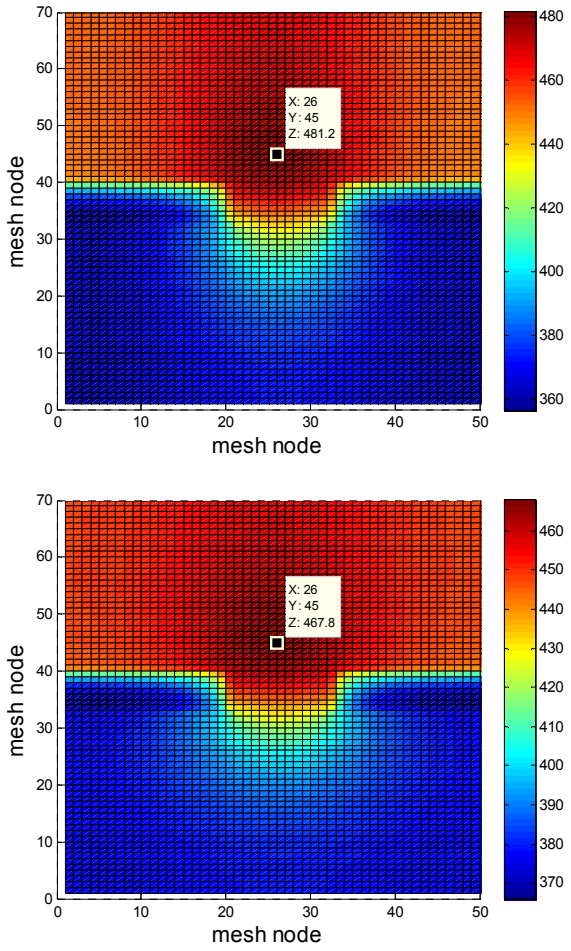

Figure 3.20. Lattice temperature profiles for [100] (top panel) and [110] (bottom panel) for VG-VD=0.8 V.

3.4 Self-Heating and Coulomb Effects due to single trap

We first present the simulation results for the current degradation for the case of positively charged and negatively charged trap placed at the middle of the source end of the channel [134]. These results are shown in Figure 3.21. From the results presented in this figure there are several general features that can be deduced. Namely, positively charged trap lowers the potential barrier near the source end of the channel thus allowing for more carriers to go through and, therefore the ON-current is the highest for both isothermal and thermal conditions. Contrary to this, negatively charged trap increases the source injection barrier and, therefore smaller number of carriers can get into the channel, therefore the smallest current. The influence of self-heating effects for both positively and negatively charged trap is more clearly shown in Tables 1 and 2, respectively. Namely, for the case of no trap/impurity, the current degradation is 2.41%, in agreement with earlier investigations made on this structure. For the case of positively charged trap, the degradation is 2.51% which is higher than the case of no trap. More importantly, when we consider the isothermal case with no impurity and with positively charged impurity, then the change in the current due to the barrier effect (lowering of the source injection barrier – see Figure 3.22) is 0.82%. In the case of thermal simulations, the screening of the potential leads to no/impurity vs. positive impurity degradation of 0.72%.

The situation is rather different for the case of negatively charged impurity. In that case, the percentage degradation in the current is 2.11%, smaller than what

we have obtained for the case of positively charged impurity. This is to be expected as for negatively charged impurity there are less carriers in the channel, therefore less heating. The isothermal no impurity vs. negative impurity case degradation from Table 2 is -0.77%, and the thermal is -0.47%.

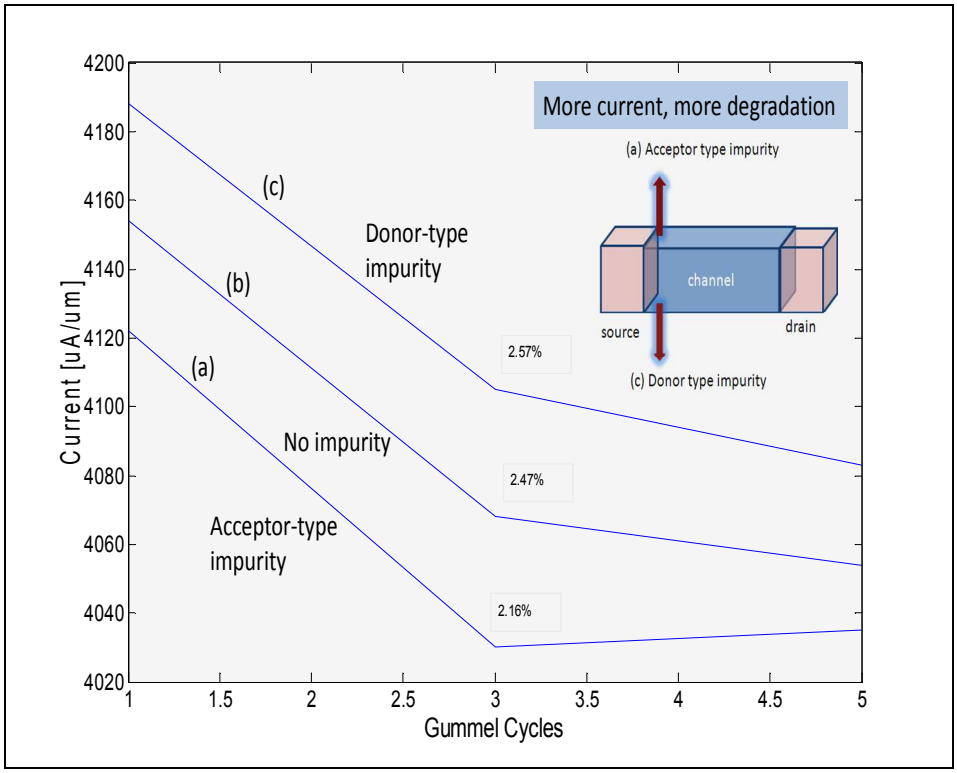

Figure 3.21. Convergence of the thermal solver as a function of Gummel cycles [10] for the case of (a) acceptor type impurity, (b) no impurity, and (c) donor type impurity.

In summary, we have presented simulation results for the degradation of the ON-current in the presence of both negatively and positively charged impurity placed in the middle of the source end injection barrier. We have observed that

screening and the barrier effects (Figure 3.22) act in opposite directions. Namely, the larger the barrier, the smaller the number of carriers that get through, the smaller the screening and the smaller the overall self-heating effect. For the case of smaller barrier, more carriers get through so screening of the charged impurity is stronger but also, the self-heating effects are more pronounced. Hence, the interplay of self-heating and Coulomb effects is very complicated in nanowire transistors and both have to be accounted for to get proper estimates of the ON current. The optical and the lattice temperatures for the case of positively charged/negatively charged impurity are shown in Figure 3.23 . The velocity profile along the channel for the case of positive/negative impurity is presented in Figure 3.24 . There are no noticeable differences in the velocity profile as the traps are placed in the vicinity of the source end of the channel and screening by the electrons at the source end is significant. If the traps were placed one mesh into the channel more noticeable effects in the velocity profile would have been observed. This is in agreement with the observations presented in Ref. [88]. We would like to point out that this is a first study in which the simultaneous influence of Coulomb and self-heating effects is being considered.

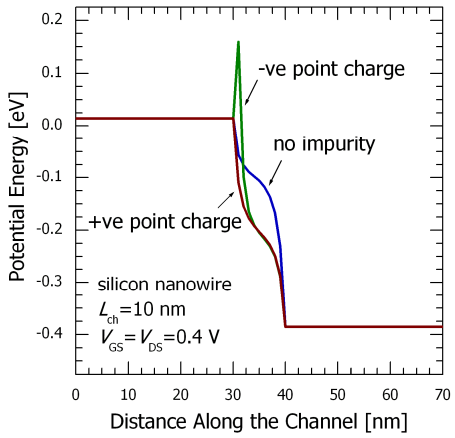

Figure 3.22 Conduction band for the case of no trap, positive trap and negative trap.

Table 3.1. Positive impurity case(current uA/um)

	No Impurity	With Impurity	Degradation
Isothermal	4154	4188	0.82%
Thermal	4054	4083	0.72%
Degradation	2.41%	2.51%	

Table 3.2. Negative impurity case(current uA/um)

	No Impurity	With Impurity	Degradation
Isothermal	4154	4122	-0.77%
Thermal	4054	4034	-0.47%
Degradation	2.41%	2.11%	

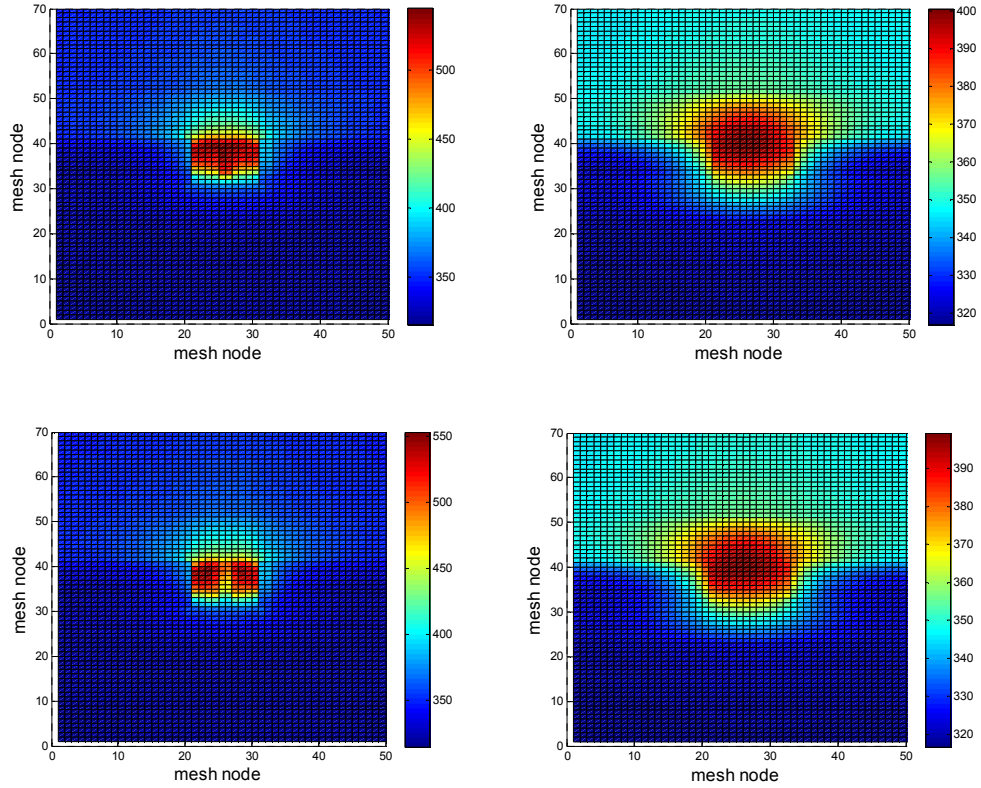

Figure 3.23 Optical (left panel) and lattice (right panel) temperature profiles for the case of positive impurity (top panels) and negative impurity (bottom panels). Applied bias is VG=VD=1.2 V.

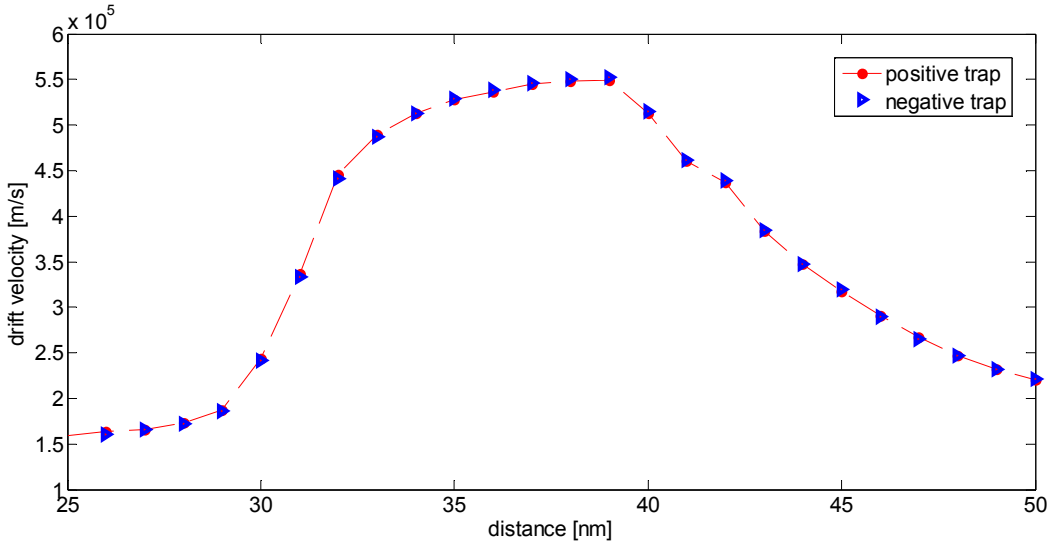

Figure 3.24 Drift velocity along the channel for VG=VD=1.2 V.

CHAPTER 4

CONCLUSIONS AND FUTURE WORK

Conclusions:

We investigated the role of self-heating effects on the electrical characteristics of a 10 nm wide, 7 nm thick and 10 nm long channel of a silicon nanowire transistor using a 3D Monte Carlo device simulator that includes self-consistent solution of the energy balance equations for both acoustic and optical phonons. One of the purposes of this work was to examine whether self-heating effects will degrade the nanowire FET output characteristics (ON state). Our 3D electro-thermal device simulator is the first device simulator that self-consistently solves the Boltzmann transport equation for the electrons (coupled to a 3D Poisson equation solver) with a 3D energy balance solvers for the acoustic and the optical bath. The convergence in the simulation occurs when lattice temperature variation is insignificant after few Gummel iterations.

Because SiO_2 has very low thermal conductivity, and the nanowire itself has low thermal conductivity (because of phonon boundary scattering in the rectangular cross section), it was expected that self-heating effects are more pronounced in the nanowire transistor. But we find insignificant current degradation because of self-heating due to considerable non-stationary electron transport in this structure that manifests itself via pronounced velocity overshoot effect. These findings are

in agreement with previous result for 2D device simulations of fully-depleted SOI devices.

We also investigated the role of the source and drain contacts on self-heating effect in nanowire transistors. Two different configurations of the nanowire transistor were examined: (a) when the contacts are far away from the active region of the device, and (b) when the contacts are in the vicinity of the channel. Our simulations showed the metal contacts transfer the heat very effectively which leads to smaller lattice and optical phonon temperatures and hence smaller degradation in the current when the contacts are in the vicinity of the channel. Thus, we conclude that if we want effective heat removal in the structure we need to have the metal contacts as close as possible to the active channel region. This is very important conclusion from a circuits design standpoint.

We also examined the simultaneous influence of self-heating and random trapping effects on the magnitude of the ON current of this silicon nanowire transistor. We presented simulation results for the degradation of the ON-current in the presence of both negatively and positively charged impurity placed in the middle of the source end injection barrier. We observed that screening and the barrier effects act in opposite directions. Namely, the larger the barrier, the smaller the number of carriers that get through, the smaller the screening and the smaller the overall self-heating effect. For the case of smaller barrier, more carriers get through so screening of the charged impurity is stronger but also, the self-heating effects are

more pronounced. Hence, the interplay of self-heating and Coulomb effects is very complicated in nanowire transistors and both have to be accounted for to get proper estimates of the ON current. We would also like to point out that this is a first study of this type in the literature.

We also included the temperature dependence of thermal conductivity for modeling self-heating effect in the nanowire transistor. We used two approaches for including temperature dependent thermal conductivity. In the first approach we used Selberherr's thermal conductivity model. Selberherr have parameterized the temperature dependence of the bulk thermal conductivity in the temperature range between 250 and 1000 K. This model for the thermal conductivity is then implemented into the energy balance equation for acoustic and optical phonons in our electrothermal device simulator. From our simulations, we found the thermal conductivity of the thin silicon film in nanowire transistor shows pronounced temperature dependence and hence more temperature rise in the device active region. This, in turn, leads to more current degradation due to self-heating. In the second approach of modeling self-heating effects with temperature dependence thermal conductivity, we used directional dependent thermal conductivity tensor provided by Dr. Z. Aksamija. We performed simulations for both [100] and [110] crystallographic directions. We observe larger degradation in the current along the [100] direction when compared to the [110] direction which is in agreement with

the values for the thermal conductivity tensor provided to us by Dr. Zlatan Aksamija.

Suggestions for future work:

To further investigate the effect of thin film thermal conductivity on self-heating effect of nanowire transistors one may want to explore changing thickness of silicon film layer to see the impact of both temperature and thickness dependence of the thermal conductivity. These simulations will give more accurate predictions of self-heating in this nanowire transistor and will help to determine correct silicon layer thickness to be used for device design.

Another interesting investigation is coupling of a phonon Boltzmann solver to the electron Boltzmann solver for more detailed simulation of self-heating. Solving phonon Boltzmann equation is very tedious and time consuming and coupling the phonon and electron solver will be even more challenging. But if implemented, it will give more accurate predictions of device characteristics with self-heating.

To study the performance of the solid-state coolers used to remove heat from hot spots of the device, one can include these thin film microcoolers in the electro-thermal simulator. Thermoelectric cooling using the Peltier effect can effectively be used to reduce the degrading device performance due to self-heating. Incorporating these thermoelectric cooling simulations into the electro-thermal simulator will completely model the nanowire transistor device characteristics under real operating conditions.

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